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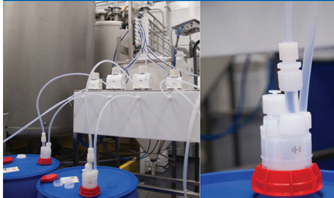
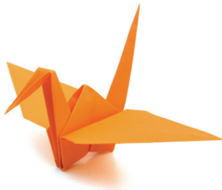
New defect reduction strategies



Resolving thermal management issues

Self-folding 3D cell grippers



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editor'sview

By Mark Andrews, Technical Editor

Opportunities drive new defect reduction strategies

THE SEMI trade group recently announced that semiconductor fab equipment sales were up 30 percent compared to 1Q 2017. While device and process tool sales are setting records, forward-looking supply chain vendors are already addressing challenges that need solutions for positive growth beyond 2018.

According to IC Insights researchers, one of the fastest growing markets and forecast upside darlings is the automotive sector. Cars and light trucks that today utilize somewhere between 400 and 700 semiconductors are forecast to become rolling 'data centers' as manufacturers automate many functions to increase safety and fuel economy. Indeed, many major auto makers are forecasting all electric vehicle (EV) fleets by 2050. If fully-autonomous vehicles move from test tracks to daily commuting, onboard semiconductors could top 5,000.

IC Insights reported that the automotive chip market has seen extraordinary performance cycles since its double-digit 2014 upswing. 2015 saw markets actually shrink, followed by nearly 11 percent growth in 2016. The 2017 auto chip market was worth (USD) $27.2 billion. But future growth depends on a number of 'what-if' scenarios, including whether manufacturers can deliver self-driving vehicles.

One of the important challenges that the semiconductor supply chain needs to face is how to effectively transition to serving auto manufacturers who have substantially different requirements than consumer device makers. As our cover feature article from Linde Electronics points out, existing auto supply chain chip providers are a tight-knit group able meet very tough performance requirements year after year. Vendors entering that space to facilitate on-board artificial intelligence or other highly advanced applications face a tough road. Smartphone chips, for example, are typically expected to operate two to five years; manufacturers accept a 10 percent failure rate. But on the automotive side, semiconductors have to operate up to 15 years with a zero percent target failure rate. Linde shares its strategies for success in the automotive jungle.

Also addressing the critical need for defect reduction in next-generation technologies is Brewer Science that advocates utilizing the latest tool and analytical techniques to meet manufacturer's requirements for defect elimination in devices below 10 nm.

With ample evidence of growth across both manufacturing equipment and end use sectors, it is easy to adopt a business-as-usual attitude. However, future success at challenging new geometries under tough standards requires vigilance and the rigorous application of lessons learned at 10 nm and above. Getting smaller is not getting any easier.

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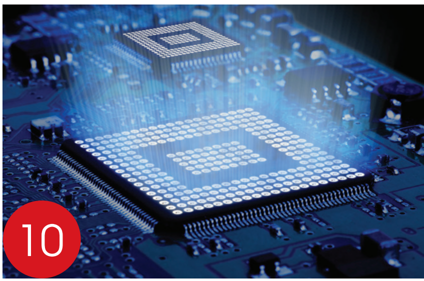

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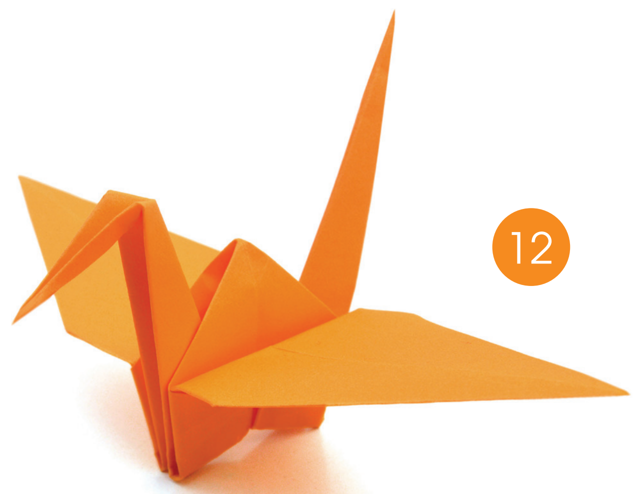


Infineon gears up for stronger long-term growth

INFINEON TECHNOLOGIES is seeing strong long-term growth drivers in its target markets – automotive, industrial, IoT and security applications – where business momentum is gathering pace. As part of its long-term planning process, Infineon is realigning its target operating model, which sets target values for revenue growth, segment result margin and the investment-to-sales ratio over the cycle.

On 12 June 2018, Infineon held a Capital Markets Day for investors and analysts in London, during which its strategy and realigned target operating model will be explained in more detail.

"A broad range of structural trends will drive growth in the coming years: electro-mobility, renewable energies, factory automation, data centers and a steadily increasing number of battery-powered, connected devices," points out Reinhard Ploss, CEO of Infineon.

"Thanks to our leading technologies and differentiated manufacturing expertise, we have established an excellent position in the markets in which we operate. We are determined to exploit the opportunities that result from this and, accordingly, apply a rigorous approach to investing.

"Our current plans are aimed at providing the necessary level of manufacturing capacity to meet expected growth. It is currently forecast that, by the middle of the coming decade, more than half of the power semiconductors produced by Infineon will be manufactured on 300 mm wafers (in Dresden/Germany and Villach/Austria). This will enable us to improve our profitability further, despite higher

depreciation expense".
In view of the current strength of the order book and based on a euro/US dollar exchange rate of 1.20, Infineon expects revenue to grow at least in the coming 2019 fiscal year by a minimum of 10 percent. For the fiscal years following this accelerated growth period, Infineon assumes that revenue will grow at an average annual rate of 9 percent (previously 8 percent).

Given that this superior growth is being driven in particular by strong demand for power semiconductors – an area in which Infineon's in-house manufacturing capabilities provide a competitive advantage – it is necessary to adjust the investment-to-sales ratio:
On average, annual investments are expected to amount to 15 percent (previously: 13 percent) of revenue. Approximately 2 percentage points of this figure will continue to relate to the capitalisation of development costs in accordance with IFRS, with the vast bulk of the remainder relating to manufacturing and IT equipment.

Any increase/decrease in revenue growth compared to the above-stated 9 percent will – for each percentage point – result in a slightly less pronounced change in the investment-to-sales ratio.

In addition to the investment-to-sales ratio described above, further investments in the low three-digit million euro range in total are planned over the coming years to enable Infineon to exploit additional business opportunities and react appropriately to structural changes. Furthermore, Infineon intends to invest a total of approximately €700 million in front-end cleanrooms and certain larger-scale office buildings during the coming five-year planning horizon. Of the investments in Villach (Austria) that have recently been announced, this figure includes the 300 mm cleanroom and the research and development building.

Implementation of these measures on the stated scale will temporarily result in an investment-to-sales ratio well above the ratio envisaged in the target operating model. Due to the increased investment activity, Infineon expects depreciation of property, plant and equipment in relation to revenue to increase by approximately three percentage points over the next five fiscal years. However, by increasing the share of cost-efficient 300 mm manufacturing and further measures, the gross margin is projected to be maintained at the level of the 2018 fiscal year.

In addition, Infineon plans to gradually improve the segment result margin from its current target level of 17 percent by ensuring that operational expenses rise at a lower rate than revenue. Selling expenses are expected to increase by 90 percent of the rate of revenue growth, while general and administrative expenses are expected to increase by 60 percent of the rate of revenue growth.

SemiGen announces new foundry capabilities

US-BASED SemiGen has announced that after moving into a new state-of-the art facility it has increased its foundry and screening capabilities. It now offers wafer processing of 100 to 150 mm silicon wafers, as well as alumina and aluminium nitride substrates up to just over 100mm (4.25 inches). Services provided include any combination of photolithography, wet etch, dry etch, metallisation, grinding, polishing, as well as in-process metrology.

Recent investments in RF Test and Hi-Reliability environmental test capabilities has also enabled SemiGen to offer solutions for High-Reliability screening of amplifiers, FETs, MMICs, transistors, diodes, and other active and passive circuits and components.

Tests are performed and are delivered with full documentation in accordance with MIL-PRF-19500, MIL-PRF-38534, and MIL-PRF-38535 requirements. Element evaluation and screening options from Class H, Class K, TX, TXV, S-level, as well as custom SCD driven requirements are available.

Applied Materials breakthrough accelerates chip performance

APPLIED MATERIALS has announced a breakthrough in materials engineering that accelerates chip performance in the big data and AI era.

In the past, classic Moore's Law scaling of a small number of easy-to-integrate materials simultaneously improved chip performance, power and area/cost (PPAC). Today, materials such as tungsten and copper are no longer scalable beyond the 10nm foundry node because their electrical performance has reached physical limits for transistor contacts and local interconnects.

This has created a major bottleneck in achieving the full performance potential of FinFET transistors. Cobalt removes this bottleneck but also requires a change in process system strategy. As the industry scales structures to extreme dimensions, the materials behave differently and must be systematically engineered at the atomic scale, often under vacuum.

To enable the use of cobalt as a new conducting material in the transistor contact and interconnect, Applied has combined several materials engineering steps – pre-clean, PVD, ALD and CVD – on the Endura platform. Moreover, Applied has defined an integrated cobalt suite that includes anneal on the Producer platform, planarization on the Reflexion LK Prime CMP platform and e-beam inspection on the PROVision platform. Customers can use this proven, Integrated Materials Solution to speed time-to-market and increase chip performance at the 7nm foundry node and beyond.

"Five years ago, Applied anticipated an inflection in the transistor contact and interconnect, and we began developing an alternative materials solution that could take us beyond the 10nm node," said Dr. Prabu Raja, senior vice president of Applied's Semiconductor Products Group. "Applied brought together its experts in chemistry, physics, engineering and data science to explore the broad portfolio of Applied's technologies and create a breakthrough Integrated Materials Solution for the industry. As we enter the big data and AI era, there will be more of these inflections, and we are excited to be having earlier and deeper collaborations with our customers to accelerate their roadmaps and enable devices we never dreamed possible."

While challenging to integrate, cobalt brings significant benefits to chips and chip making: lower resistance and variability at small dimensions; improved gapfill at very fine dimensions; and improved reliability. Applied's integrated cobalt suite is now shipping to foundry/logic customers worldwide.

ZEISS half-year figures: High-tech drives growth

CARL ZEISS has announced positive results for first half of financial year. The company attributes growth in the semiconductor manufacturing segment thanks to future-oriented EUV technology.

The first six months of fiscal year 2017/18 (ended 31 March 2018) saw its revenue rise by 9 percent to EUR 2.773 billion (1st six months of 2016/17: EUR 2.550 billion), and as much as 13 percent after adjustments for currency effects.

At EUR 380 million, the earnings before interest and tax (EBIT) were high despite clearly negative currency effects compared to the previous year (EUR 384 million). The EBIT margin is at 14 percent. Incoming orders hit EUR 2.839 billion (1st six months of 2016/17: EUR 2.743 billion).

"It is our business in the high-tech fields of semiconductor manufacturing technology, industrial metrology and medical technology in particular that are enabling our growth and helping further advance the ZEISS Group," said Prof. Dr. Michael Kaschke, President and CEO of ZEISS. "We are benefitting once again from our balanced and future-oriented portfolio and our broad global footprint."

Orbotech and IME to develop advanced packaging solutions

ORBOTECH a global supplier of yield-enhancing and process-enabling solutions for the manufacture of electronics products, and A*STAR's Institute of Microelectronics (IME), have announced a joint lab agreement confirming Orbotech as a partner in IME's FOWLP joint lab and as a member of the IME FOWLP development line consortium.

Orbotech's Emerald UV Laser Drilling solution is one of the key processes available in the FOWLP joint lab development line. The Emerald delivers advanced UV drilling performance for today's most challenging IC substrate and assembly applications, including 3D packages, stacking and package on package. The FOWLP development line at IME's facilities at Singapore Science Park II, and its new facilities at Fusionopolis Two, will allow IME and its partners to develop technologies that will serve a wide range of markets including consumer electronics, healthcare and automotive."Orbotech is honored to be part of IME's FOWLP development joint lab and FOWLP development line consortium," said Dr. Abraham Gross, Corporate Executive Vice President, Chief Technology Officer and Head of Innovation of Orbotech. "This collaboration builds on the long-term relationship that IME has with Orbotech's SPTS Technologies, a leading supplier of advanced packaging solutions. We are always pleased to cooperate with technology and process innovation initiatives that push the electronics packaging industry forward and enable solutions for complex challenges. The Emerald UV Laser Drilling system is just one of the building blocks that we, at Orbotech, provide to enhance the quality and efficiency of the production process for 3D IC and other complex high density packaging structures."

Teledyne E2v awarded second phase of €42 million for custom image sensors

THE EUROPEAN SPACE AGENCY (ESA) has awarded Teledyne e2v, a division of Teledyne Technologies, with the second phase of a €42M ($47M) contract to produce high-end Charge Coupled Device (CCD) visible light image sensors for the PLATO (Planetary Transits and Oscillations of stars) mission. PLATO is a planet hunting spacecraft that will seek out and research Earth like exoplanets around Sun like stars.

About 100 Teledyne e2v large area CCDs will allow the mission to detect minute changes in the apparent brightness of stars, orbited by planets.

Teledyne e2v completed the first manufacturing phase of the contract, including the production of high end CCD wafers and the procurement and production of other key items.

After a successful review of the first phase, Teledyne e2v has been authorised to start work on phase two of this prestigious contract. This includes manufacturing the wafers and the assembly, test and delivery of 114 CCDs. Together, they will form the biggest optical array ever to be launched into space (currently planned for 2026).

During its lifetime, PLATO will precisely measure the size, mass and age of planets, survey a large area of the sky and study the full diversity of thousands of stars and planetary systems across our galactic neighbourhood. To date, astronomers know of several thousand exoplanets orbiting distant stars.

Many of them were discovered by the Kepler and CoRoT space missions, which were also equipped with Teledyne e2v's CCD image sensors. PLATO is expected to discover many more exoplanets, which will then be further investigated and analysed by ground based telescopes, generating a huge amount of follow up activity by the astronomy community.

PLATO will be made up of 26 telescopes mounted on a single satellite platform.

Each telescope will contain four 20Mpixel Teledyne e2v CCDs in both full-frame and frame-transfer variants, for a full satellite total of 2.12 Gpixels. This is over twice the equivalent number for GAIA, the largest camera currently in space. As with GAIA, all ofthe PLATO CCD image sensors will be designed and produced in Chelmsford, UK.

GLOBALFOUNDRIES 180UHV tech platform enters volume production

GLOBALFOUNDRIES has announced that its 180 nm Ultra High Voltage (180UHV) technology platform has entered volume production for a range of client applications, including AC-DC controllers for industrial power supplies, wireless charging, solid state and LED lighting, as well as AC adapters for consumer electronics and smartphones.

The increasing demand for highly cost-effective systems requires integrated circuits (ICs) that achieve significant area savings while reducing bill-of-materials (BOM) and printed circuit board (PCB) footprint by integrating discrete components onto the same die. GF's 180UHV platform features a 3.3 V LV CMOS baseline, with options for HV18, HV 30 and 700V UHV, that delivers significant area savings for both digital and analog circuit blocks, compared to the traditional 5V bipolar CMOS DMOS (BCD) technologies.

"GF's leadership in providing high voltage solutions makes the company a perfect strategic partner for On-Bright's power supply technologies," said Julian Chen, CEO of On-Bright, the leading market player in AC-DC switch mode power supply products.

"GF's new 180UHV process integrates UHV components into the same IC with 180 nm digital and analog by incorporating On-Bright know-how in the design. The technology has reduced On-Bright's switched-mode power supply cost and footprint to give our AC-DC switch mode power supply products additional system-level benefits."

As part of a modular platform based on the company's 180 nm process node, GF's 180UHV process technology delivers a 10x increase in digital density compared to previous generations for integrated AC-DC conversion.

For AC-DC conversion, the platform integrates high voltage transistors with precision analog and passive devices to control high input and output voltages of AC-DC SMPS circuits.

The process is qualified up to 150°C to accommodate the high ambient temperatures of power supply and LED lighting products.

ASM Amicra looks to a new era

AMICRA Microtechnologies, a vendor of back-end processing equipment for advanced packaging applications and silicon photonics assembly, is entering a new era of growth and market capitalization by becoming a part of ASM Pacific Technology Ltd. (ASMPT). Effective April 2018, the company was renamed ASM AMICRA Microtechnologies GmbH. The well-known AMICRA management team, consisting of Dr. Johann Weinhaendler, Rudolf Kaiser and Horst Lapsien, remains in place.

The acquisition of 100% of the shares of AMICRA Microtechnologies GmbH by Singapore-based ASM Pacific Technology Ltd. (ASMPT) will considerably expand and strengthen AMICRA's strategic position. ASMPT, as an innovative and quality-driven strategic investor in the electronics manufacturing industry having a well-developed distribution network in Asia, complements AMICRA's technology position and worldwide business activities very well. The transaction will especially serve the fast growing silicon photonics assembly equipment market but also the general high-precision flip-chip and die bonding markets.

ASMPT, headquartered in Singapore and listed on the Hong Kong Stock Exchange, is the world's largest back-end semiconductor equipment supplier and SMT solutions provider. ASM AMICRA Microtechnologies GmbH will be integrated into ASMPT's back-end equipment segment. AMICRA's corporate structure and global organization will remain in place, as well its long-time proven management team.

AMICRA started out in 2001 with five employees. In the mean time, it has developed into an internationally known vendor and leading supplier of high-precision die bonders for the advanced packaging and photonics assembly market. AMICRA now employs 130 at its headquarters in Regensburg, Germany, and in twelve sales and tech support offices around the world. AMICRA products will now constitute an important growth factor for the global leader in back-end equipment. ASMPT's commanding market position is based on

its continued technological innovation, its foresight in investing ahead of the curve, commitment to quality, and strong value-adding services to customers.

ASMPT currently invests about ten percent of its revenues in R&D. This makes it an ideal partner for an innovation and technology leader in photonics and optical device packaging such as AMICRA.

Following its successful penetration of the worldwide markets for high-precision die-attach equipment, especially in the rapidly growing silicon photonics assembly segment, AMICRA saw a perfect opportunity to merge with a strong strategic partner to better support its growing international customers base. With ASMPT's economic scale and well established supply chains and customer support capabilities, this will allow AMICRA to take the next step in the development of its business.

Dr Johann Weinhaendler, a member of the AMICRA executive management team, stated: "We are delighted to work with ASMPT. The expanded operational base offered by ASMPT is very important to us. We will continue to be a reliable partner to our existing and new customers focused on their specific needs and requirements. We will continue to offer excellent support, as well as innovative solutions. AMICRA's sub-micron high-accuracy die bonder product is complementary to the ASMPT group's existing portfolio and the AMICRAs leading position in the photonics assembly market, gives a high growth potential for AMICRA and ASMPT. We are confident that this joining of forces will further strengthen our growth opportunities and deliver even higher added value to our common customers."

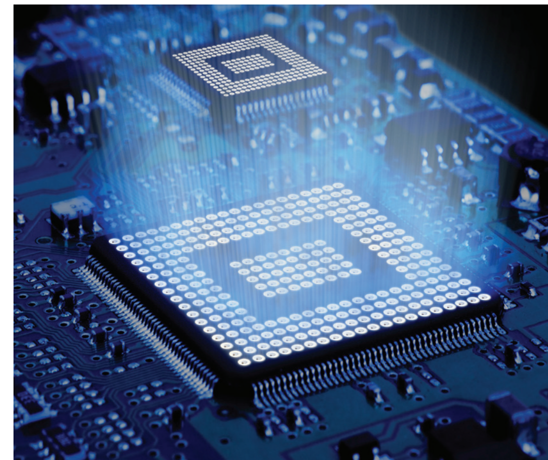
Imec and Unisantis unveil ultra-scaled EUV-enabled surrounding gate transistor

imec, the research and innovation hub in nano-electronics and digital technology, and Unisantis Electronics Singapore Pte Ltd (Unisantis), a developer of Surrounding Gate Transistor (SGT) semiconductor technology, have announced significant progress in the joint development of a process flow targeting an SGT 6T-SRAM cell with areas between 0.0184 and 0.0205 square micrometre, meeting or exceeding the dense cell area in a N5 technology node. Studies show that the vertical gate-all-around SGT-based cells have a 20-30% reduced area compared to horizontal gate-all-around FETs, while also outperforming these in terms of operating voltage, standby leakage and stability. The Surrounding Gate Transistor is a vertical gate-all-around architecture that was developed at Unisantis as the basis for a universal silicon technology platform for DRAM, NAND, Flash, and SRAM.

"SGTs have all the advantages of horizontal gate-all-around transistors, allowing a near-perfect electrostatic control of the transistor channel," says Professor Fujio Masuoka, Director and CTO at Unisantis and inventor of the SGT concept. "But because the channel is a vertical pillar, the concept has the potential for a significant area reduction compared to horizontal nanowire-based transistors."

Imec and Unisantis worked out the key process flow and steps for a 6T-SRAM cell using SGT. Through a novel Design process Technology Co-Optimization (DTCO), the researchers were able to develop an SRAM bit-cell area of 0.0205 square micrometer, using a minimum pillar pitch of 50 nm. This is a 24 percent improved scaling factor compared to the smallest SRAM designs to date, and makes the design ready for N5 technology node.

Imec demonstrates cooling solution for high performance chips



IMEC, leading research and innovation hub in nano-electronics and digital technology, announced that it has demonstrated for the first time a low-cost impingement-based solution for cooling chips at package level. This achievement is an important innovation to tackle the ever-increasing cooling demands of high-performance 3D chips and systems.

High performance electronic systems are coping with increasing cooling demands. Conventional solutions realize cooling through combining heat exchangers that are bonded to heat spreaders that are then attached to the chip backside.

These are all interconnected with thermal interface materials (TIM) that create a fixed thermal resistance that can't be overcome by introducing more efficient cooling solutions. Direct cooling on the chip backside would be more efficient, but current direct cooling microchannel solutions create a temperature gradient across the chip surface.

The ideal chip cooler is an impingement-based cooler with distributed coolant outlets. It puts the cooling liquid in direct contact with the chip and sprays the liquid perpendicular to the chip surface. This ensures that all the liquid on the chip surface has the same temperature and reduces the contact time between coolant and chip. However, current impingement coolers have the drawback that they are silicon-based and thus expensive, or that their nozzle diameters and use processes are not compatible with the chip packaging process flow.

Imec has developed a new impingement chip cooler that uses polymers instead of silicon, to achieve a cost-effective fabrication. Moreover, imec's solution features nozzles of only 300μm, made by high-resolution stereolithography 3D printing. The use of 3D printing allows e customization of the nozzle pattern design to match the heat map and the fabrication of complex internal structures. Moreover, 3D printing allows to efficiently print the whole structure in one part, reducing production cost and time.

"Our new impingement chip cooler is actually a 3D printed 'showerhead' that sprays the cooling liquid directly onto the bare chip," clarifies Herman Oprins, senior engineer at imec. "3D prototyping has improved in resolution, making it available for realizing microfluidic systems such as our chip cooler. 3D printing enables an application-specific design, instead of using a standard design."

Imec's impingement cooler achieves a high cooling efficiency, with a chip temperature increase of less than 15°C per 100W/cm^2 for a coolant flow rate of 1 l/min. Moreover, it features a pressure drop as low as 0.3 bar, thanks to the smart internal cooler design. I

t outperforms benchmark conventional cooling solutions in which the thermal interface materials alone already cause a 20-50°C temperature increase. Next to its high efficiency and its cost-effective fabrication, imec's cooling solution is much smaller compared to existing solutions, matching the footprint of the chip package enabling chip package reduction and more efficient cooling.

SCREEN signs MoU with National Tsing Hua University

SCREEN Semiconductor Solutions has signed a memorandum of understanding (MoU) with National Tsing Hua University (NTHU) in a ceremony commemorating the launch of the massively E-beam direct write lithography for 12-inch Si wafers (MEB12) program.

NTHU combined with international semiconductor equipment and software suppliers will establish the first massively electron beam direct writing (MEBDW) innovative semiconductor industry-university alliance to develop the state-of-the-art maskless lithography technology.

The MEBDW lithography technology enables "on-chip security", making Taiwan the world's first development and pilot production for security chips with unique IDs, providing information security for the Internet, AI, electronic payment and automotive chips.

The MEB12 program participants include the world's only commercial MEBDW lithography equipment manufacturer, Mapper Lithography B.V., from the Netherlands and U.S. design software supplier Synopsys, Inc. SCREEN will support the MEB12 program with both DUO lithography coat/develop track and SU-3200 single wafer cleaning systems.

As one of the MEB12 project initiators, Professor Po-Wen Chiu of NTHU's Department of Electrical Engineering and chairman of the Centre for Nanotechnology, Materials Science, and Microsystems, pointed out: "This project is a successful case to use Taiwan's strong penetration capability in the semiconductor manufacturing sector, to form an alliance with international semiconductor giants and build up the most advanced commercial 12 inch MEBDW lithography process line in the campus, making NTHU the world's first university to have this unique R&D capability."

"We are very pleased to be supporting NTHU in Taiwan as they pioneer the MEB12 alliance," noted Tadahiro Suhara, president of SCREEN Semiconductor Solutions. "This is a testament to the value our SCREEN equipment technology and resources bring to innovative IoT applications."

Imec ‘s cooling solution for high performance chips

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The ideal chip cooler is an impingement-based cooler with distributed coolant outlets. It puts the cooling liquid in direct contact with the chip and sprays the liquid perpendicular to the chip surface. This ensures that all the liquid on the chip surface has the same temperature and reduces the contact time between coolant and chip. However, current impingement coolers have the drawback that they are silicon-based and thus expensive, or that their nozzle diameters and use processes are not compatible with the chip packaging process flow.

Imec has developed a new impingement chip cooler that uses polymers instead of silicon, to achieve a cost-effective fabrication. Moreover, imec’s solution features nozzles of only 300μm, made by high-resolution stereolithography 3D printing. The use of 3D printing allows e customization of the nozzle pattern design to match the heat map and the fabrication of complex internal structures. Moreover, 3D printing allows to efficiently print the whole structure in one part, reducing production cost and time.

“Our new impingement chip cooler is actually a 3D printed ‘showerhead’ that sprays the cooling liquid directly onto the bare chip,” clarifies Herman Oprins, senior engineer at imec. “3D prototyping has improved in resolution, making it available for realizing microfluidic systems such as our chip cooler. 3D printing enables an application-specific design, instead of using a standard design.”

Imec’s impingement cooler achieves a high cooling efficiency, with a chip temperature increase of less than 15°C per 100W/cm^2 for a coolant flow rate of 1 l/min. Moreover, it features a pressure drop as low as 0.3 bar, thanks to the smart internal cooler design. It outperforms benchmark conventional cooling solutions in which the thermal interface materials alone already cause a 20-50°C temperature increase. Next to its high efficiency and its cost-effective fabrication, imec’s cooling solution is much smaller compared to existing solutions, matching the footprint of the chip package enabling chip package reduction and more efficient cooling.

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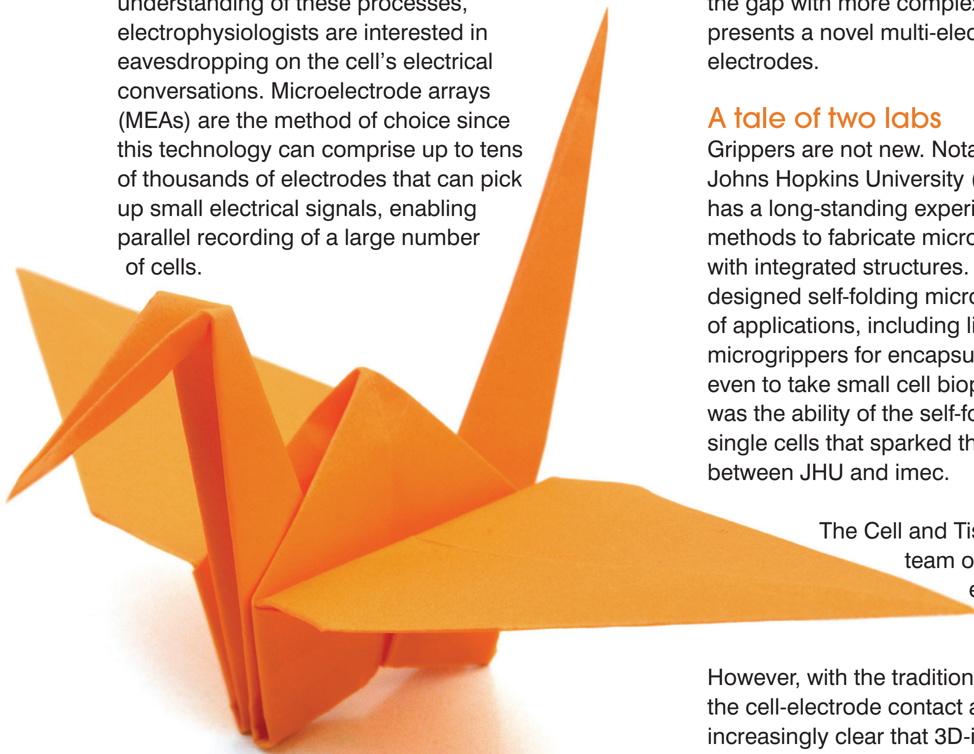
Origami for cells:

self-folding 3D cell grippers for recording

Imec develops self-folding microgrippers that wrap around cells and function as a recording shell for better cell-contact and higher signal quality.

Many cell types in our body have the ability to generate electrical signals, the most prominent of which include heart and brain cells. It is through the coordinated activity of these so-called electrogenic cells that the brain is capable of highly intricate information processing, and the heart can efficiently perform its function. In order to gain more profound understanding of these processes, electrophysiologists are interested in eavesdropping on the cell's electrical conversations. Microelectrode arrays (MEAs) are the method of choice since this technology can comprise up to tens of thousands of electrodes that can pick up small electrical signals, enabling parallel recording of a large number of cells.



But cells whisper. The tiny signals are often only a few microvolts in amplitude and disappear in the noise. The key way to achieve high signal quality is to maximize the cell-electrode contact and electrical coupling. Current MEA-technology, however, has reached its limitation, as it is inherently 2D because of the wafer-based fabrication paradigm. Bridging the gap with more complex 3D interfacing, imec presents a novel multi-electrode chip with self-folding electrodes.

A tale of two labs

Grippers are not new. Notably, the Gracias Lab at Johns Hopkins University (JHU) in Baltimore (USA) has a long-standing experience researching new methods to fabricate micro- and nanoscale devices with integrated structures. For example, the lab designed self-folding microgrippers for a wide range of applications, including life sciences, such as mobile microgrippers for encapsulating red blood cells or even to take small cell biopsies from living tissue. It was the ability of the self-folding structures to grasp single cells that sparked the idea for a new project between JHU and imec.

The Cell and Tissue Technologies (CTT) team of imec has built up extensive expertise regarding in vitro recordings of electrogenic cells using MEAs. However, with the traditional, flat electrode layouts the cell-electrode contact area is limited. It became increasingly clear that 3D-interfacing is the way to go. And so the idea arose to incorporate tiny electrodes in the panels of Gracias' microgrippers. The collaboration between imec and JHU materialized in a JHU-summer internship and continued in the PhD-

topic of Jordi Cools, main imec-researcher on this project: "The question is: can we improve the interface by wrapping the electrodes around the cell and obtain better recordings that way? The collaboration with the Gracias Lab was the ideal way to find out because it is a perfect match between their expertise in self-folding materials and our state-of-the-art nanotechnology knowledge and cleanroom infrastructure."

…The result is a first-of-its-kind chip with self-folding electrodes, that takes a leap forward from 2D planar recording to 3D cell interfacing…

It takes two layers

Each of the four arms of the microgripper contains a patterned and individually addressable electrode, allowing parallel and simultaneous readout from all sides of the cell. The secret to the folding lies in the hinges that are composed of a nanoscale SiO/SiO2 bilayer. Because of the lattice mismatch between these two layers, the thin film is intrinsically stressed.

"This is how it works: the microgrippers are first patterned on top of a dissolvable sacrificial layer. When the sacrificial layer is dissolved by the cell culture medium, the intrinsic stress of the bilayer is released and the panels with the embedded electrodes subsequently fold towards the middle, capturing any cell laying on top," Jordi explains. "The majority of the fabrication was performed in imec's III/V lab clean room, except for the deposition of the bilayer for which we could count on the expertise of CMST, an imec research group at Ghent University."

The bilayer is not only critical for the correct functioning of the grippers, but also for their performance. Jordi continues: "Using an ultrathin bilayer, we could make the panels flexible and curve during folding, so that they conformed to the shape of the cell. At the same time the panels are soft enough not to damage the cells. We demonstrated this by culturing primary heart cells on the grippers. The soft shell wrapped tightly around them, and – more importantly – the cells remained viable and functional, maintaining their electrical activity.

…Because the panels were literally pressing the electrodes against all sides of the cell, the measured signal amplitudes proved to be two times stronger than on a traditional 2D planar MEA configuration, simulated by unfolded grippers…

Moreover, our gripper design allowed for simultaneous recordings of every electrode on each of the four folded arms, making it possible to track signal propagation in the cells contained within the shell. The fact that this chip is capable of recording 3D spatiotemporal electrical signatures from captured cells is a unique advantage over traditional MEAs."

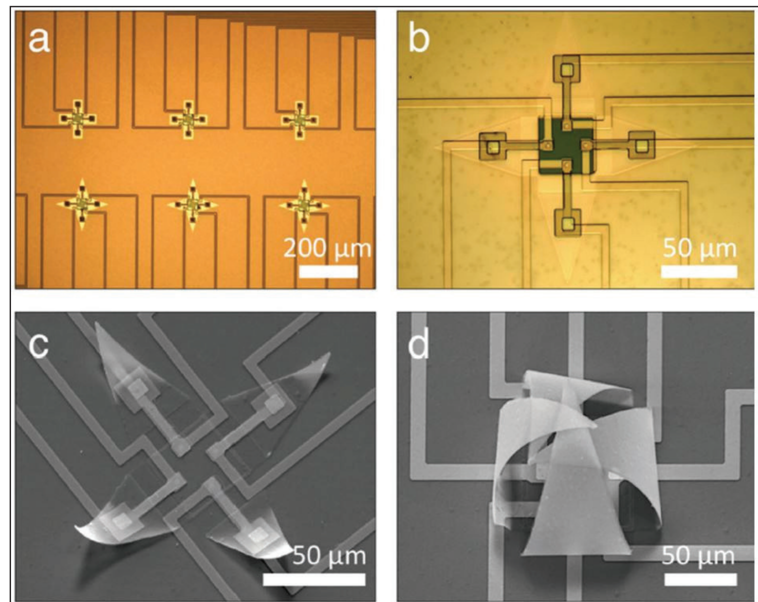


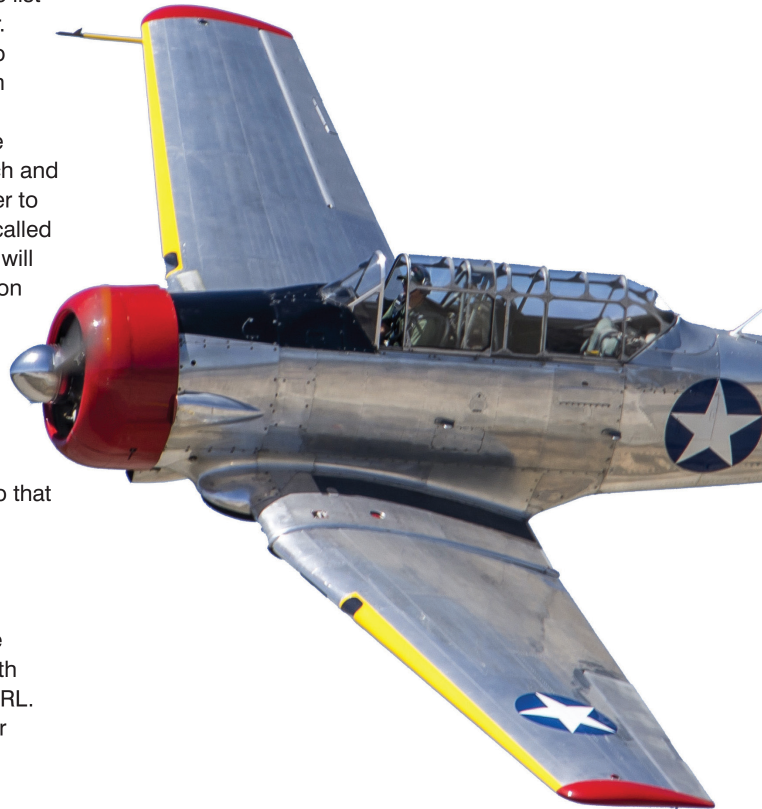
Fig 1: a) An array and b) a single planar micro-fabricated gripper with open panels, electrodes, and interconnects. Scanning electron microscopy (SEM) pictures of c) a semi-closed shell structure, illustrating the transition from the open to the closed configuration, and d) a completely closed shell with four individually addressable electrodes.

A firm grip on the future

The microgrippers herald the start of a new generation of MEAs, where dynamic cell-electrode interfacing and recording substitutes the traditional static electrode designs. Dynamic electrodes 'work' instead of trusting on a coincidental interface. Accordingly, future research efforts will focus on the next major step of combining these cell-sized multi-electrode shells with microelectromechanical systems (MEMS) in order to have precise control over the position and force of the gripper arms. Furthermore, future electrodes could be equipped with small needles to enable intracellular recordings or coated with drugs for drug screening or discovery.

"A large contributor to the success of this project was the excellent collaboration with the Gracias Lab in JHU," comments Dries Braeken, R&D manager Life Sciences and supervisor of Jordi's PhD. "It underlines the importance of fostering research ties with our partners. One of these joint efforts is the summer internship program in which we host every year three to five JHU students to work in the imec labs.

While they learn about our facilities and know-how, in turn we get familiar with the expertise of the JHU labs. That is how new science ideas take shape. The gripper-project is a successful illustration of this: what started off as a 10-week summer program, turned into a long-lasting collaboration. And it is only the beginning. As we continue with the program, I am convinced more new collaborative research opportunities will arise."



TO DATE, there have been no instances that link air quality to PEs, but that doesn't remove it from the list of variables to continue to research and consider. This is where highly advanced sensors come into play, sensors designed and developed by a team of scientists and engineers in both the Air Force Research Laboratory and the Air Force Life Cycle Management Centre. Although still in the research and development phase, this team is working together to complete a second-generation sensor package called the Real-Time Air Quality Sensor, or RTAQS, that will sense and assess cockpit air quality in real-time on high performance aircraft during flight.

"Most of the information to determine unexplained PEs is collected post-flight so much of the evidence is likely gone," explained Doug Hopkins, 711th Human Performance Wing chief engineer. "RTAQS is intended to close the gap so that we know what happens during the flight."

The first version of this sensor package was developed in 2015 and was a collaborative effort between the Airman Systems Directorate and the United States School of Aerospace Medicine, both within the 711th Human Performance Wing of AFRL. Researchers at the NASA-Glenn Research Center were also part of this collaboration.

AFRL-AFLCMC

collaborate on real-time air quality sensor

WHEN MOST THINK of hypoxia-like physiological events (PEs) some pilots have experienced in the cockpits of aircraft such as the recent propeller-driven T-6, the common assumption is an issue with the on-board oxygen generating system supplying oxygen to the pilot. But there are several other variables to consider, one being air quality.

"We had a first-generation sensor package that we flight-tested at Edwards Air Force Base in an F-16, we got some results, and then came back to the lab to look for ways we could enhance that sensor with additional capabilities," said Jennifer Martin, a 711HPW research chemist.

The team is now testing sensors that could be put on the next version of that original package in order to improve the performance of its air quality testing. "We're in the early stages – just moving from the first generation sensor package design to the next," explained Martin. "These sensors could enable us to rule out air quality as a root cause and they can focus on other variables such as equipment malfunction, bleed air and environmental control systems to try to figure out the driving force for physiological events." This team's research is part of the military's on-going effort to find what Air Force Chief of Staff Gen. David Goldfein calls "the smoking gun" in regards to PEs. Part of this research is looking at what other work has been done that could be leveraged with Air Force research. "RTAQS contains several embedded sensors, some of which were originally developed by NASA for use aboard the International Space Station," explained Martin. "NASA collaborated with us and

Makel Engineering, the technical integrator for the electronics and packaging. We're also leveraging the AFRL Small Business program via a Phase II Small Business Innovation Research award with Makel to help mature this technology."

Another part of this research is the testing phase, where these developmental sensors are put in simulated environments that are capable of mimicking what happens during flight. The Air Force Life Cycle Management Center, also headquartered at Wright-Patterson Air Force Base, provided these environments, namely their accelerometer validation for this testing. David Ryerse, biomedical test technician with AFLCMC, explained that this equipment has the capability to give different vibration profiles of aircraft and vehicles.

"We were contacted by 711HPW to use our vibration tables," stated Ryerse. "This table is able to do various aircraft profiles such as a jet or a high-vibration vehicle such as an Army Humvee. Whatever profile they wanted to see, we were able to produce the proper vibration profiles. They wanted to be able to see how each of these affected the accelerometer and the data."

Future versions of RTAQS are planned to sense accelerometry data in addition to air quality, said Mike Brother, 711HPW research scientist.
While the team wants to be able to see what chemicals are in the air, another goal is to be able to link those chemicals to a certain event during flight in order to inform the Root Cause Corrective Action teams from AFLCMC, who are responding to the physiological event.

"With this type of real-time sensing capability, we're trying to correlate maneuvers, aircraft parameters, as well as environmental conditions to possible conditions that could affect air quality," said Michael Brothers, a research scientist with 711HPW
These sensors could also contribute to the life cycle maintenance needs of the aircraft, which could possibly improve resource efficiency, explained Grant Slusher, who is also a research scientist with 711HPW. "There's a distribution in how the aircraft's parts wear out," explained Brothers. "Maybe it's two months or maybe it's eight months, but if a maintainer has to go in and check everything after four months, it wouldn't be known if the part went bad at two months or if it's still good and might go another four months. So to have a sensor that could automatically indicate that would reduce manpower needs, reduce down time, and maximize resources."

The team of collaborators has funded studies to test operational aircraft at numerous Air Force bases, said Martin. "We're also working to design a smaller version of the sensor that's specific to various cockpit space constraints and that could meet the longer-term vision of fleet-wide integration."

The team explained that they plan to have a number of different versions of this sensor to plug-and-play with various weapon systems and the program office needs in both the AF and US Navy. They also discussed the importance of their collaborations with academics and small businesses to see if down the line, some of their research can be more easily transitioned to other Department of Defense manned airborne platforms.

"The long term vision of this research is both to develop a sensor package for use in both PE root cause investigations and to integrate air quality sensors into all of our manned airborne platforms," explained Claude Grigsby, technical advisor for 711HPW's Human-Centered ISR Division. "These types of sensors could ultimately be utilized for immediate autonomous activation of back-up oxygen systems if an issue with the air supply is detected. When this work was initiated, as follow-up to previous PE investigations supported by the 711th Human Performance Wing, our goal was to create a capability where the pilot no-longer has to function as the sensor in the system."

Jennifer Martin, research chemist with the 711th Human Performance Wing, displays the first generation version of the real-time air quality sensor (RTAQS) package. This sensor is the culmination of a collaborative effort between the 711HPW, NASA-Glenn, and Makel Engineering, Inc. to measure air quality during flight. (U.S. Air Force photo/Gina M. Giardina

Driving growth, safety, and quality in automotive electronics

Sophisticated electronic systems continue to increase their impact across today's automotive sector. Radar, LiDAR, and a host of new artificial intelligence (AI)-based systems are becoming the norm as vehicle makers seek to improve safety, performance and efficiency on the road to fully autonomous vehicles. Linde Electronics describes ways that the automotive manufacturing supply chain can meet tight performance standards in pursuit of global market opportunities.

By: Dr. Paul Stockman, Head of Market Development, and Greg Shuttleworth, Technical Quality Manager, Linde Electronics

In 1913, Henry Ford revolutionized manufacturing with the inauguration of the first assembly line to produce automobiles, which reduced the time to make a new car from 12 hours to 2.5 hours, and more importantly, drove down the cost by 65%. Semiconductor manufacturing has been a beneficiary of this approach, as increasing automation has been complementary to the geometry shrinking forces responsible for Moore's Law. Both industries manufacture on a very high volume: there were approximately 87 million passenger vehicles and 87 million 300mm equivalent wafers fabricated in 2017. Today, robotics drives both industries to further cost reduction and improved quality.

More and more, these industries are connected, as electronic systems and semiconductors become a larger part of the total automotive bill of materials, and automotive applications become a larger percentage of the total semiconductor market. At the same time, electronics are responsible for a larger portfolio of car functions, progressing rapidly towards an anticipated revolution of fully automated driving vehicles. While electronics become more safety critical in vehicle operation, the quality requirements of the semiconductor components are increasing in ways the industry has not seen before. We can see in the daily financial news the competing headlines between large strategic plays in automated driving investments and developments punctuated by reports of crashes by test vehicles and private owners pushing their cars into uncharted levels of self-driving.

In this article, we look first at the expanding market and drivers that are linking the growth of the semiconductor and automotive businesses. Next, we evaluate the status of automotive semiconductor quality requirements and the developing needs for further specifications. Finally, we look further into the supply chain to examine the role that semiconductor process materials play in enhanced requirements for safety and quality.

Market overview

Electronic systems and passenger vehicles are both significant contributors to the global economy, representing about 2% each of global GDP, and their growth is increasingly interdependent. According to NXP, electronic systems represent more than one-third of the bill of materials for new cars. The chips themselves, including OSDs (optical, sensors, and discretes) now average nearly (USD) $500 per vehicle. From the semiconductor industry perspective, automotive ICs and OSDs are 13% of application sales, and growing almost twice as fast as the overall industry. Just like PCs and smartphones, we expect the chip value of the overall electronics assembly to increase as the applications become a more critical part of vehicle operation.

This growth potential has attracted attention from many of the major players in semiconductor manufacturing as they try to both directly benefit from the higher multiples of the automotive sector, and to influence what kinds of chip designs will control future vehicles.

Many recent mergers and acquisitions have been viewed through the lens of increasing the acquirer's position in automotive applications: NXP's acquisition of Freescale, which had a larger share of automotive chip sales, and Qualcomm's pending takeover of NXP. Likewise, On Semiconductor increased its share by acquiring Fairchild, and Infineon has bought Wolfspeed and International Rectifier for silicon carbide technology important for power control in electrified vehicles.

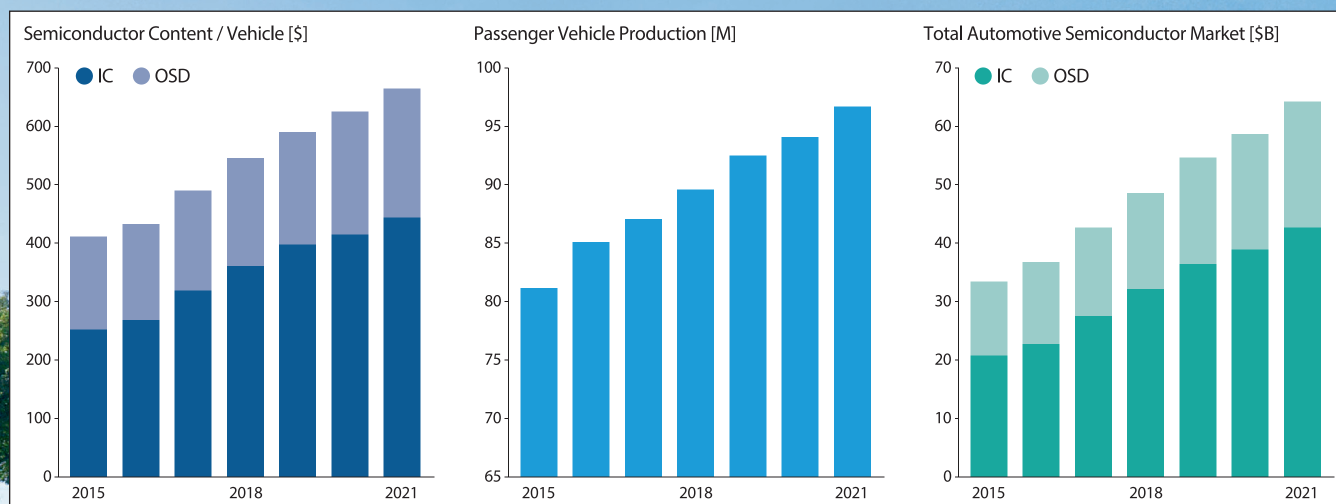


Figure 1: Growth of automotive, semiconductor and vehicle markets [adapted from IC Insights]

Even more strategic plays have been pursued in the past year by Intel and Samsung. Intel has made a portfolio of automotive acquisitions, capped recently by the $15 billion purchase of Mobileye for chip designs that support assisted and autonomous driving for customers like Tesla and BMW. For its part, Samsung purchased Harman for $8 billion. Known best for its premium car audio offerings, Harman's products also include automotive navigation, communication, and cybersecurity. It brings with it a customer portfolio of most of the major vehicle manufacturers in Europe, Japan, and the United States.

Primary drivers

While we may think of semiconductors as being rather recent introductions, associated with many of the comfort, convenience, and infotainment options now available, computer chips have long been an integral, if unseen, part of the cars we drive.

- **Operations and environmental controls**
  In 1968, just ten years after the modern IC industry was born, Volkswagen introduced an electronic control unit (ECU) manufactured by Bosch for regulation of fuel injection. As emission and fuel efficiency requirements became more stringent, ECUs were made standard on most vehicles manufactured. Controllers have proliferated in cars ever since: engine temperature, electronic steering and braking, automatic transmissions, as well as controls for smaller parts like wipers, mirrors, and illumination. Airbag sensors/actuators and anti-lock brakes have made driving safer.

- **Convenience, comfort and infotainment**
  More obvious in modern cars are the proliferation of many electronic functions, which have a higher density than our connected offices and homes. Conveniences and comfort functions are almost everywhere accessible in the vehicle: power windows, climate control, charging ports, remote operations, as well as those actually related to driving like cruise control and passive seatbelt use indicators. More recently, infotainment offerings have also quickly advanced from radio and recorded media players to include multiple display screens for indicators, controls, navigation, and entertainment in addition to connectivity for the vehicle and the devices we bring inside it. As a safety feature, the US National Highway Traffic Safety Administration has required rear-view cameras for vehicles less than 4500 kg sold after May 2018.

- **ADAS to full autonomy**
  The basics of ADAS (advanced driver assistance systems) are already in premium vehicles today: adaptive cruise control, lane departure warnings, and drowsy driver detection are just a few of the controls and sensors available. However, these are just the beginning of what is anticipated to be a rapidly advancing revolution in driving technology, which will transform the operation of driving from one where the driver is assisted passively by various electronic information and controllers, to one where the vehicle operates fully autonomously, that is independently, of any occupant in the vehicle.

The roadmap to full autonomous driving is populated not only with significant developments in technology, but also with safety protocols. Various automotive authorities have created stages on this roadmap, such as the SAE (Society of Automotive Engineers) characterization in Figure 2. Common protocols among autonomous vehicles will need to be agreed to benefit from information sharing between vehicles.

To achieve fully autonomous driving, sensors and controllers are just the beginning of the electronics requirements. Extreme amounts of data will need to be received, prioritized, analyzed, and shared in real time. Intel estimates that cars will generate data at a rate of nearly 0.75 Gb/s, or around

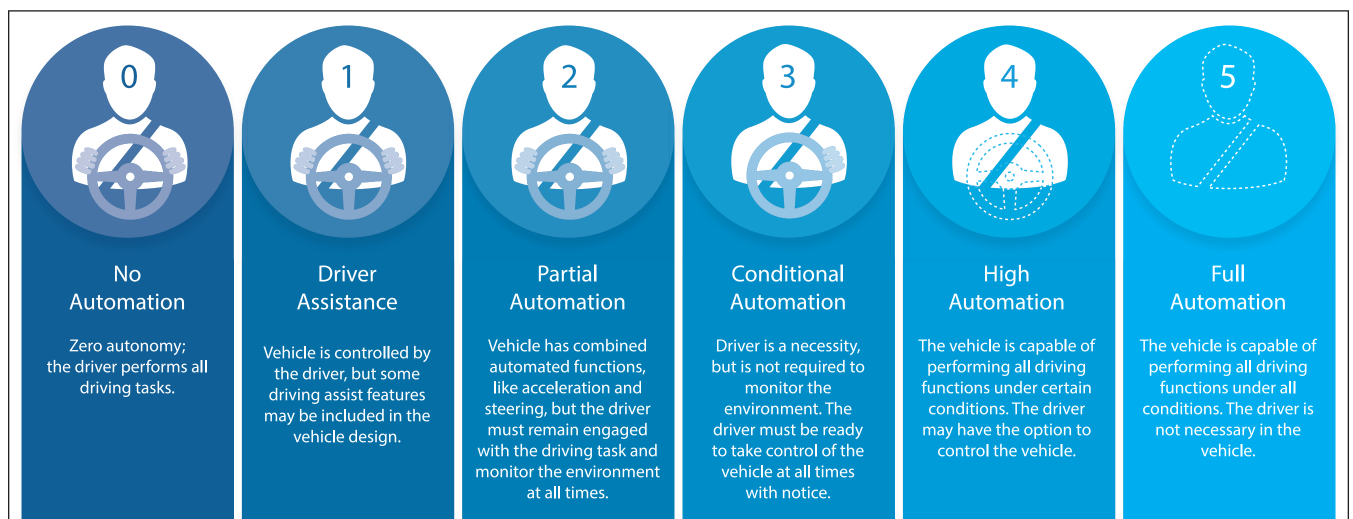


Figure 2: SAE designated level of autonomous driving capability

4 Tb per average 90-minute usage per day, rivaling the fastest broadband connections available today. Processors like emerging GPUs for artificial intelligence are thought to be the likely means of dealing effectively with data-rich processing, which gives companies like Nvidia and AMD and the foundries that supply them access to this emerging application. And autonomous vehicles will need to receive and share relevant data with each other, which will require new levels of cloud connectivity and capacity, explaining the strong early investment in ADAS from cloud giants like Baidu, Google, and Microsoft.

- **Electrification**
  In a development roadmap roughly parallel to autonomous driving, electrification of powertrains will also transform the automotive industry and become a new growth application for semiconductors. Already available from established and new automobile manufacturers either as fully electric vehicles or as hybrid electric motor-combustion engine models, electrified vehicles have roughly double the semiconductor content per vehicle. The adoption of electric vehicles is driven by environmental concerns – the reduction of greenhouse gas, NOx, and particle emissions – as well as improvement of vehicle performance and maintenance. Bolstering adoption is the future ban of sales of combustion engines by major economies like India, China, and much of Europe by 2040. Already, 3% of vehicles sold in 2017 were electric.

Diverse electronics content

Automotive electronics is an application that cannot be defined by specific technologies or applications, which benefits almost all sectors of the semiconductor industry. Currently, it is characterized by a very large portfolio of products based on mostly mature technologies, spanning from discrete, optoelectronics, MEMS and sensors, to integrated circuits and memories.

Figure 3 shows the distribution of silicon content from an analysis of an early electrified car in 2014. Important to note is that this car has no autonomous driving capability. If all vehicles made today had the same level of electronics intensity as this example car, the semiconductor content would require the equivalent of 600,000 wafer starts per month of 300mm fab capacity.

Enhanced quality

Until now, the automotive electronics market has been the preserve of specialized semiconductor manufacturers with long experience in this field. The reason for this is the specific know-how required for quality management. As applications proliferate, become safety critical, and progress towards leading-edge processes, enhanced quality protocols will be required.

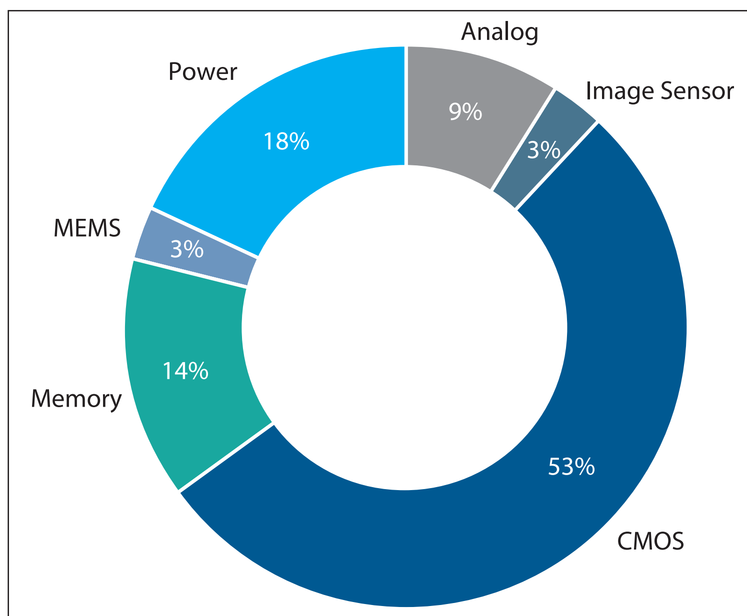


Figure 3: Semiconductor content in BMW i3 in relative silicon area [adapted from Applied Materials]

A component failure that appears harmless in a consumer product could have major safety consequences for a vehicle in motion. Furthermore, operating conditions of automotive electronics components (temperature, humidity, vibration, acceleration, etc.), their lifetime, and their spare part availability are differentiators to what is common for consumer and industrial devices.

Currently, some of the most technologically advanced vehicles integrate around 450 semiconductor devices. As they become significantly more sophisticated, the semiconductor content will drastically increase, with many components based on the most advanced semiconductor technology available. Introducing artificial intelligence will require advanced processors capable of computing a massive amount of data stored in high-performance and high capacity memory devices. This implies that not only the most advanced semiconductor processes will be used, but that these will need to achieve the highest degree of reliability to allow a flawless operation of predictive algorithms.

It is expected that smart vehicles capable of fully autonomous driving will employ up to 7,000 electronic components. In this case, even a failure rate of 1ppm, already very low by any standard today, would lead to 7 out of 1,000 cars with a safety risk. This is simply unacceptable. The automotive electronics industry has therefore introduced quality excellence programs aimed at a zero-defect target. Achieving such a goal requires a lot of effort and all constituents of the supply chain must do their part.

The automotive electronics industry is one of the most conservative in terms of change management. Long established standards and documentation procedures

Typical operating conditions for different electronics market segments

	Consumer	Industrial	Automotive
Temperature	0 to 40°C	-10 to 70°C	-40 to 160°C
Operation time	2 to 5 years	5 to 10 years	Up to 15 years
Humidity	Low	Environment	0% to 100%
Supply	Average 1 year	2 to 5 years	Up to 30 years
Tolerated failure rate	<10%	<<1%	Target: 0% failure

Figure 4: Typical operating conditions for different semiconductor applications

ensure traceability of design and manufacturing deviations. Qualification of novel or modified products is generally costly and lengthy. This is where material suppliers can offer competence and expertise to provide material with the highest quality standards.

What does this mean for a material supplier?

As a direct contact to its customer, the material supplier is responsible for the complete supply chain from the source of the raw material to the delivery at the customer's gate. The material supplier is also accountable for long-term supply in accordance with the customer's objectives.

There are essentially two fields where the material supplier can support its customer: quality and supply chain.

Given the constraints of the automotive electronics market, material qualification must follow extensive procedures. While a high degree of material purity is a prerequisite, manufacturing processes are actually more sensitive to deviations of material quality, as they potentially lead to process recalibration. Before qualification starts, it is critical that candidate materials are comprehensively documented. This includes the manufacturing process, the transport, the storage, and, where appropriate, the purification and transfill operations. Systematic auditing must be regularly performed according to customers' standards. As a consequence, longer qualification times are expected. Any subsequent change in the material specification, origin, and packaging must be duly documented and is likely to be subject to a requalification process.

Material quality is obviously a critical element that must be demonstrated at all times. This requires the usage of high-quality products with a proven record. Sources already qualified for similar applications are preferred to mitigate risks. These sources must show long-term business continuity planning, with process improvement programs in place. Purity levels must be carefully monitored and documented in databases.

State-of-the-art analysis methods must be used. When necessary, containment measures should be deployed systematically. Given the long operating lifetime of automotive electronic components, failure can be related to a quality event that occurred a long time before.

Because of the necessary long-term availability of the electronics components and the material qualification constraints, manufacturers and suppliers will generally favor a supply contract over several years. Therefore, the source availability and the supply chain must be guaranteed accordingly.

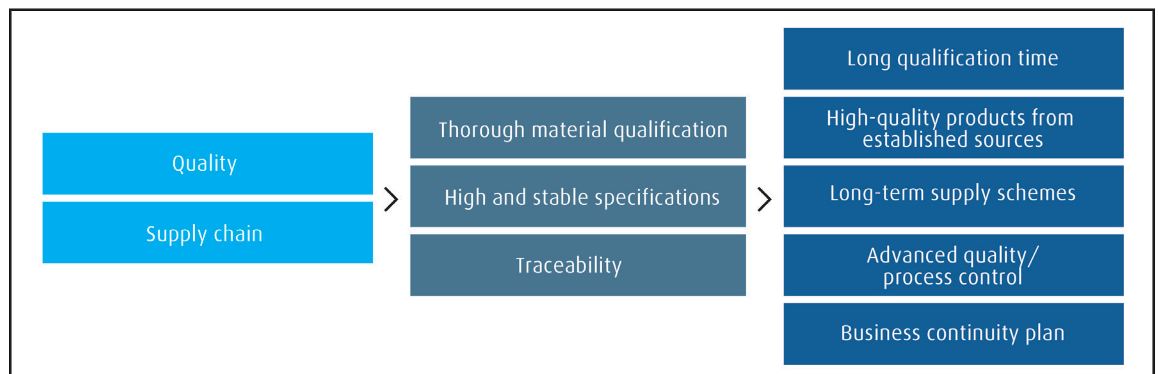


Figure 5: Quality and supply chain control determine supplier planning and actions

Material suppliers are implementing improved quality management systems for their products to fulfill the expectations of their customers, in terms of quality monitoring and traceability. Certificate of analysis (COA) or consistency checks are not sufficient anymore; more data is required. In case deviation is detected, the investigation and response time must be drastically reduced and allow intervention before delivery to the customer. Finally, the whole supply chain must be monitored.

Several tools must be implemented to maintain a reliable supply chain of high-quality products: statistical process and quality controls (SPC/SQC), as well as measurement systems analysis (MSA), allow systematic and reliable measurement and information recording for traceability. Implementing these tools particularly at the early stages of the supply chain allows an "in-time" response and correction before the defective material reaches the customer's premises. Furthermore, some impurities that were ignored before may become critical, even below the current detection limits. Therefore, new measurement techniques must be continuously investigated to enhance the detection capabilities.

Finally, a robust supply chain must be ensured. It is imperative for a material supplier to be prepared to handle critical business functions such as customer orders, overseeing production and deliveries, and other various parts of the supply chain in any situation. Business continuity planning (BCP) was introduced several years ago to identify and mitigate any risk of supply chain disruption.

Analyzing the risks to business operations is fundamental to maintaining business continuity. Materials suppliers must work with manufacturers to develop a business continuity plan that facilitates the ability to continue to perform critical functions and/or provide services in the event of an unexpected interruption. The goal is to identify potential risks and weakness in current sourcing strategies and supply chain footprint and then mitigate those risks.

Because of the efforts necessary to qualify materials, second sources must be available and prepared to be shipped in case of crisis. Ideally, different sources should be qualified simultaneously to avoid any further delay in case of unplanned sourcing changes. Material suppliers with a global footprint and worldwide sourcing capabilities offer additional security. Multiple shipping routes must be considered and planned to avoid disruption in the case, for instance, of a natural disaster or geopolitical issue affecting an entire region. Material suppliers need to be aware and monitor regulations specific to the automotive electronics industry such as ISO/TS16949 (quality management strategy for automotive industries). This standard goes above and beyond the more familiar ISO 9001 standard. By understanding the expectations of suppliers to the automotive industry, suppliers can ensure alignment of their quality systems and the documentation requirements for new product development or investigations into non-conformance.

Future of automotive electronics

With the increasing automation of future vehicles, new and more advanced semiconductor technologies will be used and vehicles will become supercomputers and data centers on wheels. Most of these components (logic or memory) will be built by manufacturers relatively new to the automotive electronics world—either integrated device manufacturers (IDM) or foundries.

In order to comply with the current quality standards of the automotive industry, these manufacturers will need to adhere to more stringent standards imposed by the automobile industry. They will find support from materials suppliers like Linde that can deliver high-quality materials associated with a solid global supply chain with acquired global experience in automotive electronics.

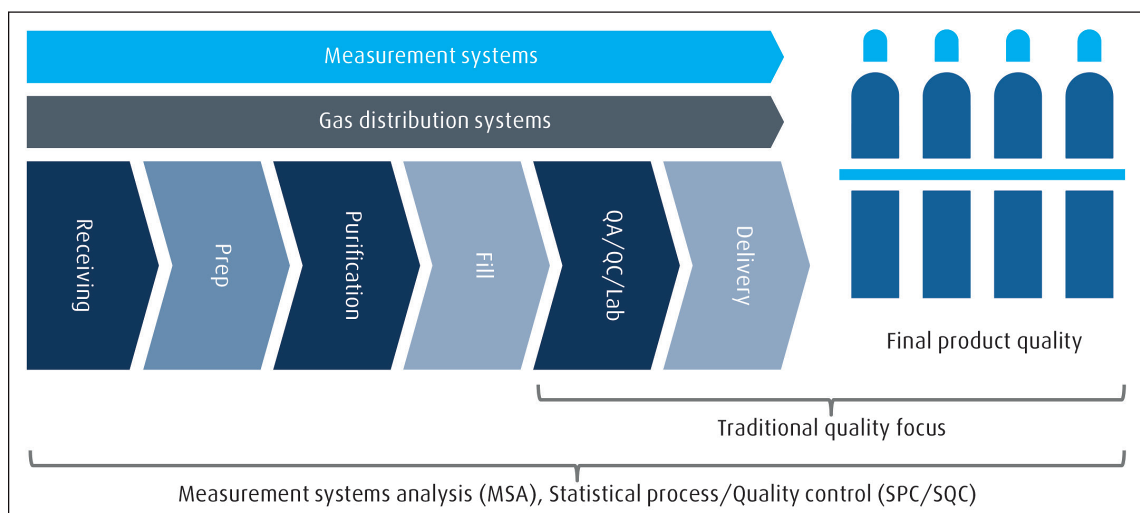


Figure 6: Enhancing material quality requires expanding traditional quality focus

Future nodes require new defect **reduction strategies**

Existing defect reduction protocols have proven less than ideal for reducing waste and speeding production as transistor geometries shrink and process complexity increases. Brewer Science offers insights into tools and analytical techniques that can improve defect elimination in devices below 10 nm.

By Darin Collins, Director of Metrology, Brewer Science

AS THE SEMICONDUCTOR INDUSTRY migrates to advanced lithography at the 10-nm node and beyond, standard best practices for defect reduction will be insufficient. Contamination levels will need to be measured in parts per trillion (ppt). Defect reduction at this level requires improvements in analytical tools, quality control (QC) and quality engineering (QE). Semiconductor manufacturers looking to reduce defect levels for advanced nodes must carefully control and characterize their entire supply chain, starting with raw materials. Raw materials suppliers typically provide data on the purity levels of their chemicals, but purity is insufficient to give semiconductor manufacturers confidence that the material will enable them to meet their yield requirements. They need data on the detailed impurity profiles at the level of parts per billion (ppb) or ppt. This requires either going to their materials suppliers' sub-suppliers or conducting extensive testing on all materials received.

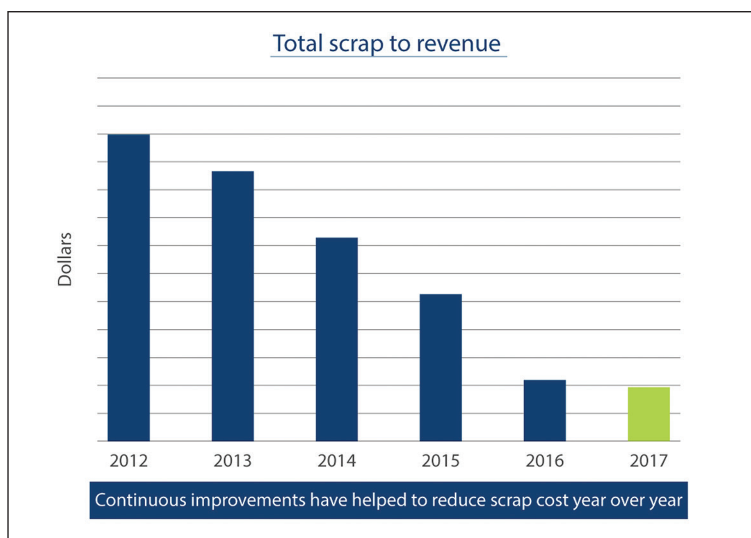


Figure 1: Brewer Science's scrap cost as a percentage of revenue, showing reduction each year.

What can raw materials suppliers do to differentiate themselves and gain the confidence of potential customers in the semiconductor industry? Quite a bit. At least three primary opportunities exist for companies developing materials and processes to support semiconductor and microelectronic device fabrication: data collection and analysis; factory automation; and a cultural emphasis on quality.

Although it is not yet standard industry practice, some suppliers provide mass spectrometry data on their chemicals. Such data describe levels of multiple metal impurities at the ppb or ppt level, and can track the history of these impurity levels. Brewer Science, for example, monitors levels of at least 10 common metal contaminants, with detection levels ranging from 4 to 13 ppt, and provides the resulting data to customers. Semiconductor manufacturers can work with a certain level of impurities, so long as values are consistent and manufacturers understand how different impurities are affecting their yields. By continuously tracking data on metal impurities, chemical precursors and other contaminants, any deviation from the baseline shows up. The better manufacturers understand how these deviations affect device yield, the better they

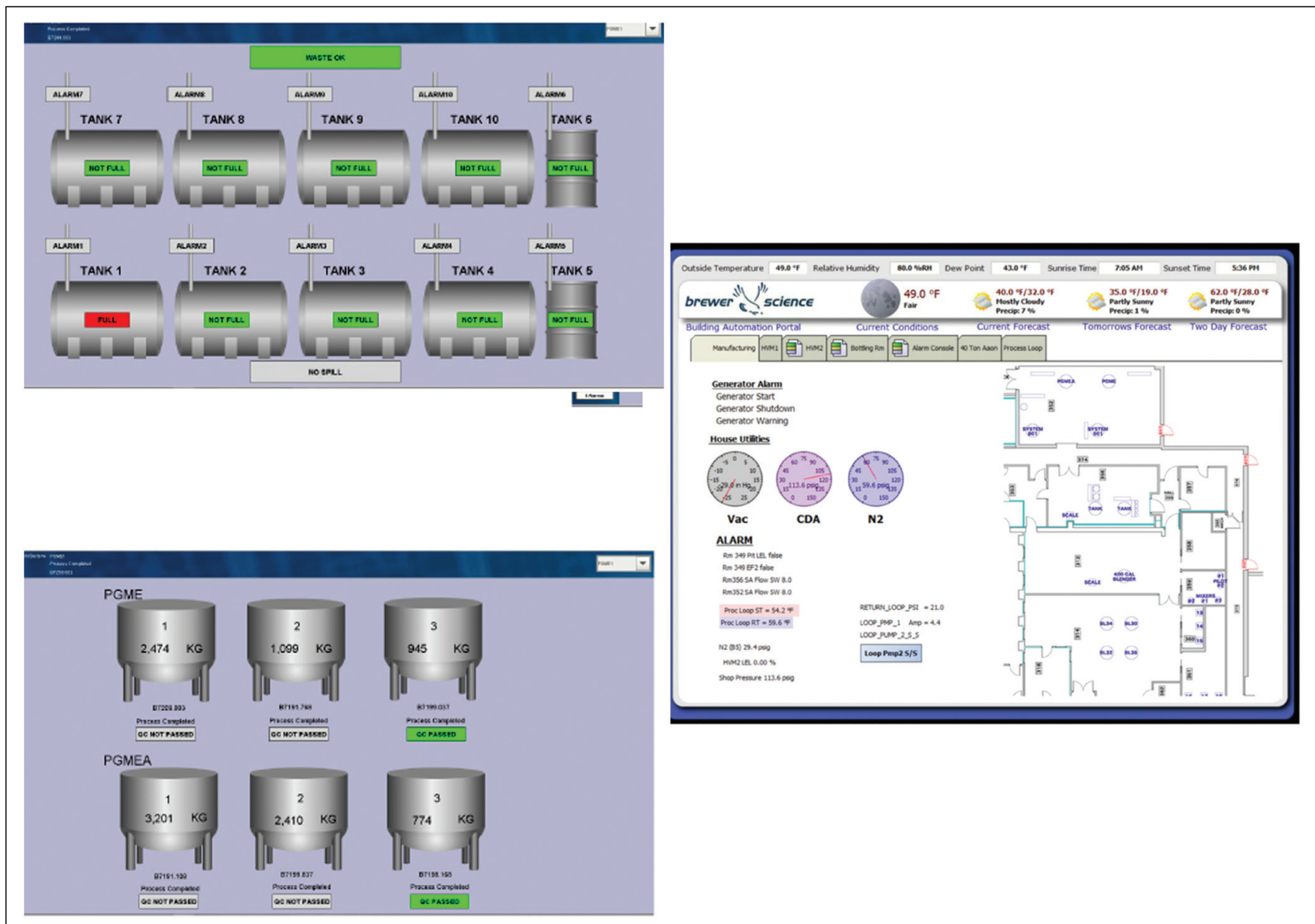


Figure 2: Factory automation portal. In this example, tank 1 has an issue that needs to be addressed).

can optimize their process to keep yield as high as possible. The approach must be collaborative in order for these slight deviations to be understood. Suppliers can incorporate several techniques to decrease the level of impurities in their products and improve consistency in impurity profiles. These practices include factory automation, closed-loop systems and failure mode effects analysis (FMEA).

Factory automation improves production quality in several ways. In the world of manufacturing, there should ideally be no such thing as employee error, and factory automation is a necessary step toward decreasing it. Factory automation that improves product consistency can dramatically reduce the volume of product scrapped, even as production quantities increase (Figure 1).

An optimized factory automation setup (Figure 2) will allow employees to see every part of the manufacturing process on a single screen, enabling them to easily monitor those and act immediately if anything is out of specification. Alarms and alerts in real time can be sent via text and email, allowing employees to monitor systems remotely via their smartphones.

An automated factory creates a massive stream of data. Quality engineers can analyze these data to continuously improve their processes. These results allow employees to understand the impact of quality improvements, and empower them to focus on product quality. Having a history of the impurity profile of a product makes it easier to know where to tighten processing specifications to produce a more consistent result.

Factory automation also reduces the possibility of contamination. At Brewer Science, the blending and bottling of chemicals occurs in a closed-loop system (Figure 3). What is today a competitive advantage will soon be necessary to attract customers. As their own defect requirements tighten, semiconductor manufacturers will begin demanding higher levels of cleanliness, automation and characterization from their raw materials suppliers. The traditional advanced on-wafer defect instrumentation isn't able to detect the impact of raw materials in the supply chain. Typical solutions are found in the sub-supplier detection capability and process stabilization.

QE plays an important role in achieving continuous improvement. While FMEA is a standard tool in many manufacturing environments, it isn't always used optimally. The ideal approach to FMEA is to evaluate all possible failure modes together and incorporate lessons learned to avoid repeating mistakes. FMEA is useful at many stages of product development: when

Figure 3: Closed-loop system from feed stream in preparation for blending materials at Brewer Science's facility in Vichy, Missouri.

a product or process is first being designed; when it is being applied in a new way; or when analyzing failures or planning improvements for an existing product or process.

In semiconductor manufacturing, keeping yields high is critical to achieving cost control. Incoming raw materials may pass the manufacturer's specifications, but the yield on a 300-mm wafer might be too low to be cost-competitive. In that case, semiconductor manufacturers need to re-evaluate their entire process, starting with raw materials.

If the purity of incoming materials is partially responsible for yield loss, the material supplier needs to work with their customer, the semiconductor manufacturer, to help fix the problem. Choosing suppliers that are on the leading edge of automation and characterization will help avoid potential problems. Such suppliers should also be responsive in the case of yield issues linked to their materials.

Computational chemistry stands as the next step in further improving raw materials purity. Molecular modeling can point the way to improvements at the molecular and atomic levels that will be needed to design the next generation of raw materials for semiconductor manufacturing. Modeling can predict the interaction of specific metal contaminants with a polymer base and model flow during spin coating to predict defect distribution. Computational fluid dynamics can model fluid flow at a microscopic level to ensure consistent mixing during material production and to further drive down defect density. Brewer Science is already using such modeling to improve product performance.

Last but not least, a cultural focus on quality and people plays a vastly important role in these processes and techniques. It requires people's commitment to quality from the top down, going beyond product/process to become a mindset for success in innovation. Empowering the technicians to make meaningful changes and understand the effects on the customer, and the customer's customer, will emphasize the individual contribution to technology advancement.

Tomorrow's semiconductor devices will demand a new level of defect reduction. A process that incorporates a focus on quality throughout the supply chain should enable manufacturers to meet ever-more-stringent requirements and produce high-yielding devices.

Repeatable wafer processing with highly accurate results from the all new Logitech LP70

LOGITECH are set to launch an all new multi-station precision lapping & polishing system. Featuring innovative features and functionalities this highly automated system will be the ideal solution for multi-wafer processing for applications that require high specification surface finishes and flatness.

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Logitech are showcasing this system at SEMICON West 2018.

To find out further information on this system, launch dates, process capabilities and much more contact the technical experts at Logitech at:
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Flat wafers and warped wafers imaged acoustically

If a wafer can be imaged as though it were flat, devices with defects can be removed after dicing and the warping of individual wafers can be measured.

Tom Adams, consultant, Nordson-Sonoscan explains why this is important

A WAFER just sawn from an ingot may be found to have one or more internal anomalies, typically voids. As the wafer goes through later processes, it may be found to have anomalies such as warpage or bonding problems. These anomalies can cause losses of various kinds during later processing. Warpage, for example, may cause breakage during dicing, while voids may turn into pinholes during polishing of the wafer, or, if not detected, may turn into various types of eventual field failures.

Silicon, gallium arsenide and other commonly used wafer materials are all good to excellent transmitters of energy in the form of ultrasound. This means that they can be imaged by acoustic micro imaging tools in multiple imaging modes. Acoustic imaging is non-destructive and can locate, image and analyze any internal structural anomaly. Wafer types that have been imaged acoustically include unpolished and fully processed wafers, solar cells (i.e., PERC), MEMs, 3D ICs, Sensors, LEDs, Lab-on-Chip and Chip-on-Wafer applications. The materials involved include silicon, glass, GaAs, sapphire, and combinations of materials.

For purposes of this article wafers are divided into two categories: flat wafers and warped wafers.

Acoustic imaging of flat wafers

Flat wafers, whether blank or patterned, can be imaged in small quantities on a laboratory-style acoustic micro imaging tool from Sonoscan's C-SAM tool line, as is often done for analytical purposes. In production environments, larger quantities are imaged automatically by the AW300 tool. When blank wafers are imaged before polishing or impregnation, the goal is typically to look for anomalies within the wafer itself. After further processing steps, imaging may be looking at the adhesion of a chip to the wafer. The AW300 tool requires an operator only to initiate the imaging sequence, which uses imaging parameters defined by a recipe designed specifically for a given wafer configuration. Imaging follows these steps:

- A robotic arm removes two wafers from the wafer carrier and places them on the tool's imaging stages. (A tool may have multiple carriers, robotic arms, stages and transducers.)
- The ultrasonic transducer begins scanning. The wafers are scanned simultaneously to increase throughput. As the transducer moves, a jet attached to the transducer maintains a column of water between the transducer and the wafer.
- Several thousand times a second, the transducer pulses ultrasound into the wafer and receives the echoes from any material interfaces the pulse strikes. The amplitude of a given echo will determine the color of the pixel at that location in the acoustic image of the wafer.
- At the conclusion of scanning, the robotic arm lifts the wafer and places it in the drying area. The imaging data for the lot of wafers being imaged may be stored in the AW300 or sent via SECS/GEM to the user's Factory Information System. In either case, Digital Image Analysis™ software is used to separate wafers into reject and accept.

If the targets of imaging are individual unpolished wafers, the most likely internal anomaly is a void that formed when the ingot was cast. The transducer scans a few millimeters above the top surface of the wafer. A pulse of ultrasound from the transducer will enter the wafer and, if it happens to strike a void, be reflected as an echo back to the transducer a few millionths of a second later. The speed of ultrasound through silicon and other wafer materials is so high that the echo from one pulse is received before the next pulse is launched.

Reflection is caused by the material interface between the silicon of the wafer and the air the void. Ultrasound at these high frequencies does not travel through air, so it does not pass through the void. The difference in physical properties between silicon and air is so great that nearly all the ultrasound is reflected as a very high amplitude echo. The pulse also encounters two other material interfaces, one between the top of the wafer and the water column, and one between the bottom of the wafer and the air beneath it. These interfaces can be excluded from imaging by instructing the transducer to accept for imaging only those echoes originating from the depth of interest. The echoes are said to be gated on that depth.

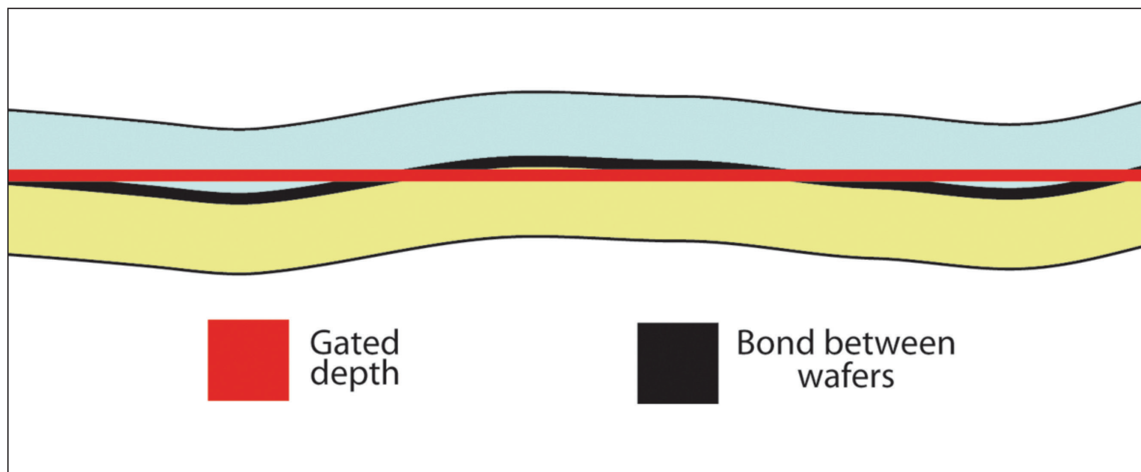


Figure 1. The transducer accepts echoes only from the gated depth (red). Warping makes much of this depth unreachable

When the automated tool is imaging wafers having two or more layers, the depth of greatest interest is bonding between the layers. Here the gated depth might be only slightly thicker than the bonding material. The bulk of the wafers above and below the bond may be ignored, particularly if they have already been scanned as individual wafers. A few examples of depths imaged: the bond between two SOI wafers, the seal on devices in a MEMS wafer, and adhesion between sapphire layers on an LED wafer. The purpose of imaging is to find anomalies such as voids or delaminations within the bond. If there is a reliable history that shows that anomalies in specific locations or anomalies below a certain size pose no danger to long-term performance, devices with these anomalies may be accepted.

Wafers can become warped in various ways. When the wafer is cut from the ingot, it may experience mechanical stresses that result in warping. Non-uniform heating can also warp a wafer, as can some doping or deposition processes. Wafers of large diameter (300 mm, usually) may be extremely thin. If a wafer is too thin to support its own weight, any number of circumstances can lead to warping.

When chips or other items are bonded to a wafer, the bonding process itself can create mechanical stresses that result in warping. So can significant thermal differences between the wafer and the item being bonded.

One of the problems in the imaging of warped wafers is that the transducer is set to focus on features that lie at a specific depth below the transducer - 0.5 inch, for example. A gate of desired thickness is set at this depth, meaning that only return echo signals whose transit time indicates that they originated at a material interface within that gate are accepted for imaging. Timing starts at the Front Interface Echo - the echo sent back from the interface from the top of the wafer and the water couplant. Echoes from all other depths are ignored. What is measured is the time difference internal interface between the front interface and the internal interface..

On a flat wafer or wafer pair, this system works nicely. But if the wafer is warped, the gated depth will be bouncing in and out of the depth that the transducer is focused on.

The diagram in Figure 1 shows, with some vertical exaggeration for clarity, the cross section through a warped bonded wafer pair. The heavy dark line is the bond between the wafers. The red line marks what would be the optimum focus depth if the wafer were

Wafers can become warped in various ways. When the wafer is cut from the ingot, it may experience mechanical stresses that result in warping. Non-uniform heating can also warp a wafer, as can some doping or deposition processes. Wafers of large diameter (300 mm, usually) may be extremely thin. If a wafer is too thin to support its own weight, any number of circumstances can lead to warping.

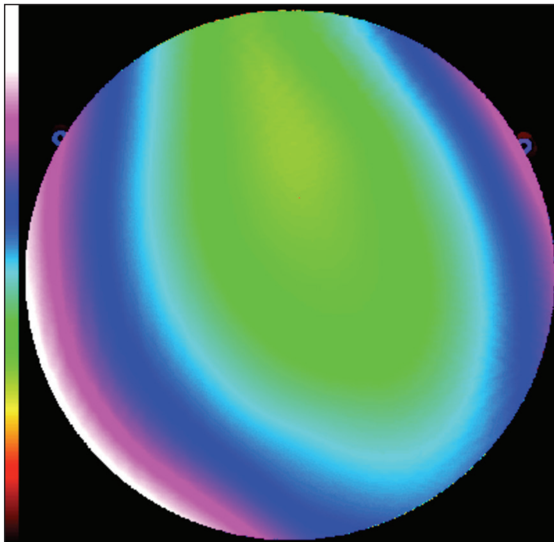


Figure 2. A warped wafer imaged by a vertically stationary transducer. Green regions are infects, but other regions are not.

flat. If the scanning transducer blindly follows the gate and accepts echoes (if any) only from that depth, there will be serious differences in the amplitude of signals during a scan.

Across much of this wafer pair, the transducer will be receiving no echoes because the gate is in the bulk of one of the wafers, and not at the bond. Only here and there does the gate actually encompass the part or all of the thickness
of the bond.

The gated depth is usually kept as thin as is feasible to avoid imaging features at multiple depths in the same image. There are a few sample types - high-voltage ceramic capacitors are one - where it is customary to gate on essentially the whole thickness of the sample because its uniform internal structure means that an internal defect such as a delamination is serious at any depth. In a bonded wafer pair, however, the gate is kept thin on the assumption that the wafer will be flat. The wafers above and below the bond are unlikely to have internal features, especially if they have been imaged individually before bonding.

If warping is severe, the biggest risk might not be missing the gate, but that the transducer that is moving at a speed that can exceed 1 m/s a few millimeters above may strike a high spot on the wafer, with likely damage to both items. The largest variation in surface elevation on badly warped 300 mm wafers is about 6 mm.

So how does one successfully scan and image even a modestly warped wafer? Sonoscan noted that the transducer receives thousands of echo signals per second from the sample's top surface. These echoes are not used in imaging internal features, but they can be used to measure the distance from the transducer to the surface thousands of times a second.
What Sonoscan developed was Quantitative Dynamic Z (QDZ), a system that constantly reads the altitude of the transducer above the warped wafer's surface and instantly adjusts the transducer's altitude to follow the contours of that surface. Contour following keeps the gated depth constantly in focus during scanning even if the wafer its warped. Since the transducer is instantly adjustable, the gated depth is always the same distance from the transducer, and the acoustic image of a warped wafer will appear to be the image of a flat wafer.

Figure 2 is the C-SAM image of a 300 mm wafer that is seriously warped. Colors show the contours: regions that match the green tones in the color map at left are in within the gated depth and will be imaged properly. A small faint yellowish area at the center of the green region is slightly higher.

The other regions - blue, pink, and at the lower left, white - indicate regions that are progressively lower than the gated depth. These regions will be imaged poorly
(no usable data) or will be missed completely.

Figure 3 is the same wafer imaged by the module that uses QDZ to constantly adjust the transducer's elevation to maintain a constant distance from the wafer's undulating surface. The result is that the wafer is imaged as though it were flat, and all regions are imaged within the gated depth - even the small faint greenish-yellow area near the top. Devices having structural defects have been identified and can now be removed after dicing. The warping of individual wafers can also be measured to assess their suitability for stacking. Enabling the transducer to image almost any wafer as though it were physically flat has solved these problems.

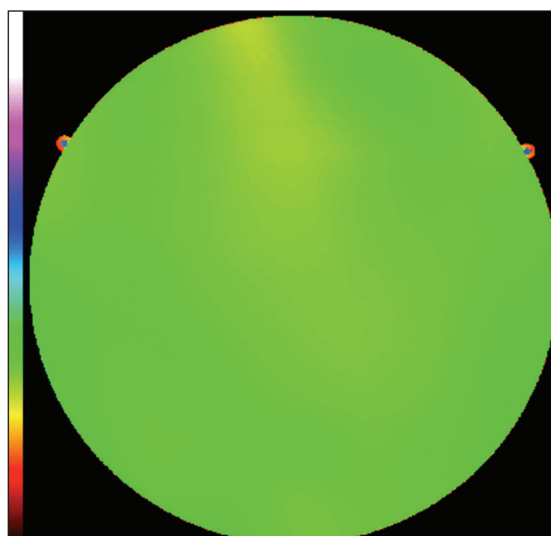


Figure 3. The same wafer imaged by the instantly adjustable transducer. All regions are imaged successfully.

CVD diamond

resolves thermal management issues in high performance electronics

Gallium nitride (GaN) and advanced silicon technologies offer sizeable power density enhancements compared to legacy solutions. But greater density presents thermal management challenges. Designers typically de-rate performance, add bulky heat spreaders or utilize active heat dissipation to ensure resilience and longevity. According to Element Six, CVD diamond could offer more effective, smaller and less complex solutions for 5G and other high power electronic systems.

By Firooz Faili, Head of CVD Thermal Products at Element Six.

DIAMOND possesses a remarkable set of properties, making it the most effective material for solving thermal management problems. Microwave-assisted undoped CVD (chemical vapor deposition) enables control of grain size, grain purity and grain interfaces to generate high-quality, high repeatability, polycrystalline diamond at the targeted thermal conductivity level needed for particular applications. Commercially, CVD diamond is readily available in six different grades with thermal conductivities ranging from 700 to 2000 W/mK and bulk resistivity from 0.001 Ωm for doped diamond to 10^{12} Ωm for undoped diamond.

A crucial element in developing disruptive technology is the control of basic building block engineering. The use of CVD grown diamond as a high-performance heat spreader can ensure the effective performance of a wide range of disruptive electronics from GaN solid state RF X-band PAs to advanced ASICs to laser diodes. Naturally, understanding the fundamentals of the science and engineering of the thermal properties of grown diamond is an essential part of this process. Element Six, part of the De Beers Group of companies, has spent over 25 years in developing, understanding and characterizing CVD technology and CVD diamond material, operating worldwide with primary manufacturing facilities in the UK and US.

Diamond, the ultimate substrate material

In designing a thermal management system, it is important to consider both the material and the application methodology to minimize channel temperatures and deliver long-term device operation. To date, the integration of SiC (400 W/mK) substrates with GaN has provided the best option for GaN HEMT and MMIC technology for high power applications. However, despite the use of SiC substrate, adequate heat spreading is still the limiting factor in determining the maximum power dissipation for GaN based electronics. As such, the path to long-term reliability is often achieved by de-rating the maximum power dissipation. A far better heat spreading solution incorporating CVD diamond (2000 W/mK) has the potential for a factor of 3× or greater increase in power density relative to current state-of-the-art GaN devices. (Figure 1 compares performance of various substrate materials.)

While GaN-based electronics are capable of delivering ultrahigh current and power density performance, the failure of many high-end electronic systems is directly attributable to the lack of adequate thermal management.

Semiconductor devices continue to increase in power density. For high power RF and Optoelectronics, using CVD diamond enables devices to run at increased power levels without raising junction operating temperature, thereby delivering longer lifetimes and better reliability.

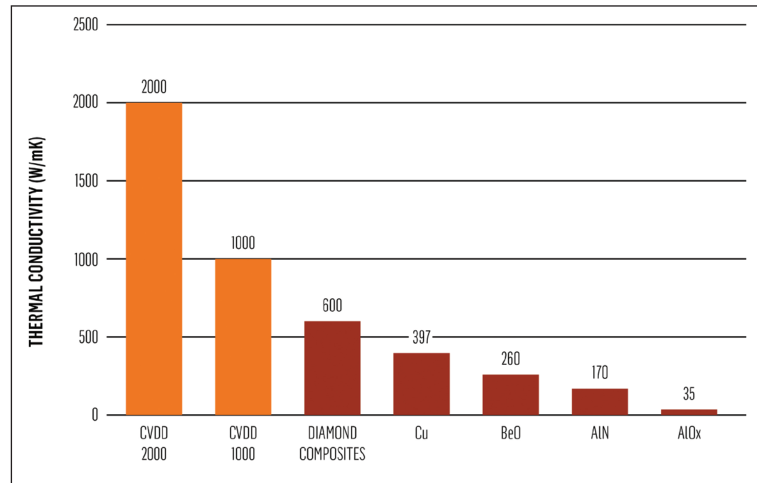


Figure 1: Comparison of CVD diamond with 'traditional' heat spreading materials

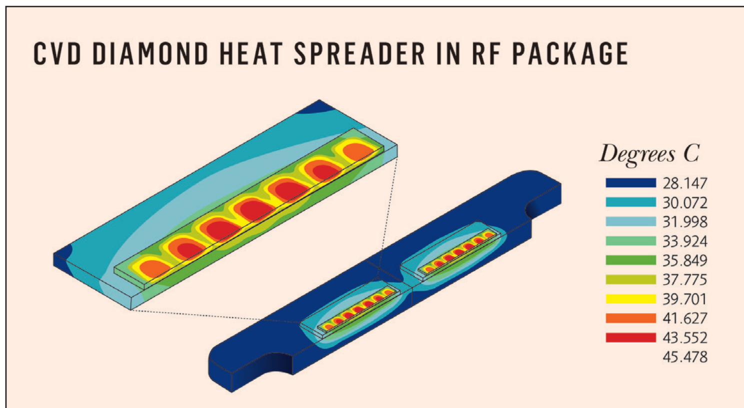
A packaged RF application example

To demonstrate the impact of a diamond heat spreader in a practical example, an RF-amplifier design was analyzed. In this example, a packaged VDMOS (Vertical Diffused Metal Oxide Semiconductor) power amplifier was initially made with a BeO (Beryllium oxide) heat spreader on a CuMo (Copper / Molybdenum) flange. The end-user was interested in lowering the overall thermal resistance of the system design while also avoiding the use of BeO due to its toxicity.

Boron doped, electrically conductive CVD diamond, a unique material for high frequency packaged electronics.

As an electrically conductive heat spreader, thick, boron doped diamond (BDD) with metallic conductivity (0.05 Ω-cm resistivity) is an ideal replacement for the commonly used metal/diamond configuration or other heat spreaders such as copper, copper/refractory or copper laminate. Mounting of RF/microwave devices on a BDD heat spreader enables better isolation of the ground plane at below 1.5 GHz, and in reduction of conductive losses at and above 1.5 GHz due to the increased skin depth.

RF current flows on a metal surface and for typical metals (Cu or Au) at above 1.5 GHz the already very thin skin depth continues to decrease with increasing RF frequency. The decrease in skin depth results in a surface resistance increase and hence increasing conductive losses. Above 1.5 GHz, in comparison to Cu and Au, BDD has nearly two orders of magnitude greater skin depth at the same RF frequency (Figure 3). The higher conduction cross-section of BDD not only enables better RF performance by improving the ground-plane isolation, but also in reducing



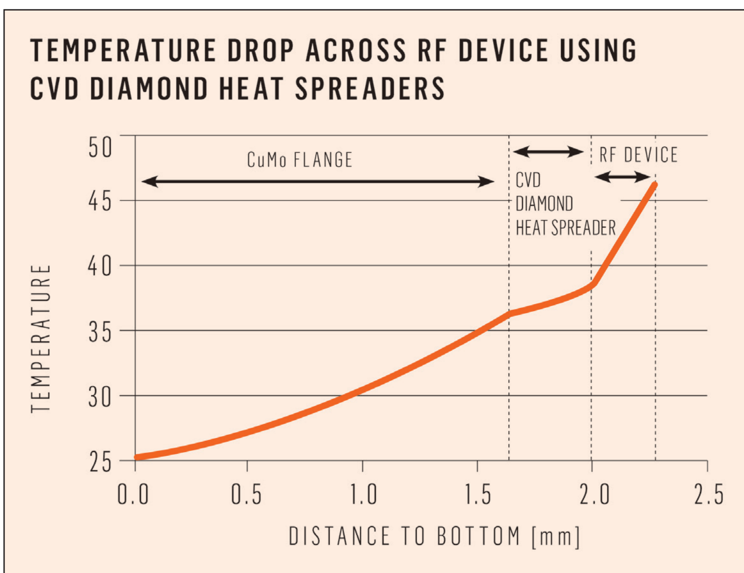


Figure 2 demonstrates the temperature profile junction-to-case for one of the optimal designs derived from this modelling. The CVD diamond heat spreader solution was found to have 30% lower thermal resistance at 0.300 mm in thickness at a thermal conductivity of 1000 W/mK (the original solution used a 1.00 mm thick BeO heat spreader). The lower thermal resistance of the diamond heat spreader has led to this device functioning with better RF linearity performance and with improved reliability due to its reduced junction temperature.

conductive losses at higher frequencies. Using thick BDD with metallic conductivity, instead of the standard metal/diamond enables better isolation of the ground plane below 1.5 GHz by increasing the skin depth. The metallic-like heat spreader reduces the slow wave mode and the capacitive coupling between ground planes found in metallised dielectrics below 1.5 GHz. It should be noted that a gold metallization might still be beneficial in reducing the electrical resistance of the BDD substrate.

For electronic applications operating below 1.5 GHz, the standard metallized diamond heat spreader (1000-2000 W/mK) may introduce unwanted couplings between grounds due to the capacitive coupling of the metallized ground plane at this frequency range. In this region it is functionally beneficial to sacrifice some of the ultra-high thermal conductivity of diamond by making it electrically conductive.

CVD diamond, the future of high frequency resistive components

Though the frequency range of 5G network system is not yet decided, the standardization of 5G network system is well underway.

While the network communications (between each base station) system will be using the 28-30 GHz frequency range to achieve a high data rate of exchange, it is expected that 6-8 GHz and/or up to 10 GHz will be used for personal cellular connections. On the amplifier front, GaN-based HEMTs appear to be the only solution for high power/high frequency operation in the 28-30 GHz range.

Currently most major network system manufacturers (Ericsson, Nokia, Huawei, etc.) are focusing on a method of phased array (128 channel) communication for 5G in the 6-8 GHz frequency range. With increasing frequencies there is a need for component size reduction, which results in increasing demand for more efficient thermal management. CVD diamond is uniquely positioned to provide the solution not just for amplifiers, but also as a resistive component for devices such as isolators, limiters and phase shifters.

The millimeter wave market demands solutions that offer gigahertz performance at high output power levels. With the designation of the operating spectrum for 5G at above 6 GHz, and high-performance phased array radars operating in the X- and Ku-bands, there is significant drive for passive components able to handle high power density at higher frequencies. To date beryllium oxide (BeO) and aluminum nitride (AlN) have been the preferred substrates for high power RF resistors. These ceramic materials have relatively high thermal conductivity and enable resistors to handle tens to hundreds of watts when operating at L- and S-bands (1-4 GHz).

However, when operating from X-band up to Ku-band (8-30 GHz), the trade-off between maximizing the dissipated power and reducing resistor parasitic effects leads to a diminished ability to dissipate a few watts when using BeO or AlN substrates. This limitation in management of power at higher frequency will become a bottleneck for extending high power applications above S-band. What is proposed here is an enabling solution for RF resistors capable of operating above 8 GHz while handing over 100 W by using CVD diamond as the resistor substrate.

Figure 4 summarizes the values of the key parameters affecting performance for the different high thermal conductivity substrates used in RF resistors. It is evident that AlN, with the highest permittivity and the lowest thermal conductivity will perform worse than BeO, and that diamond—having the best combination

of low permittivity and highest thermal conductivity – would excel as a high frequency resistive substrate. Diamond's permittivity is ~15-35% lower than those of BeO and AlN respectively and remains stable with changes in frequency and temperature, varying by only 5% from low frequencies up to tens of gigahertz, and only shifting by 730 ppm/°C from room temperature up to a few hundreds of degrees centigrade. Temperature is also important when considering thermal conductivity. At 125°C the thermal conductivity values for AlN and BeO are reduced by 30-40% compared to performance at room temperature.

Thermal conductivity of the purest single crystal diamond may exceed AlN and BeO by a factor of ~10-15, which roughly means that a resistor using diamond should be able to handle 10-15 times more power. When considering polycrystalline diamond as a resistive substrate with thermal conductivity ranging from 1000 W/mK to 1800 W/mK, a 4-8x improvement in performance over that of AlN and BeO could be realized.

A word on cost

A subject worthy of an extended article by itself, the cost of diamond heat spreader technology should be viewed from two primary angles. Firstly, a consideration of cost should be made when standard heat spreaders cease to perform in cooling high power density devices in RF, microwave and ASICs. Secondly, and perhaps more importantly, is that the cost of performance improvement could and should always be optimized multi-dimensionally. The ratio of device to spreader area, the spreader thickness and the CVD diamond heat spreader thermal conductivity all play primary roles in controlling thermal resistance and cost. As a result, it is imperative to follow a proper performance/cost model to optimize diamond heat spreader benefits.

Summary

Significant thermal-management improvements within electronic systems can be realized by using CVD diamond. The integration is relatively straightforward as CVD diamond can be a direct replacement for AlN (Aluminium nitride), BeO (Beryllium oxide) or other advanced ceramics. Attention to detail at the interfaces is important to keep overall thermal resistance low, thereby optimizing the effectiveness of the diamond.

Through improved synthesis technology, advanced processing and on-going cost reduction efforts, CVD diamond has become a crucial enabler as a heat spreader and heat dissipater for high power density RF applications. It is expected that this trend will continue in the years to come, in line with the ever-increasing need for smaller and more powerful electronic devices and systems, including the growing demand for defense as well as upcoming 5G wireless applications.

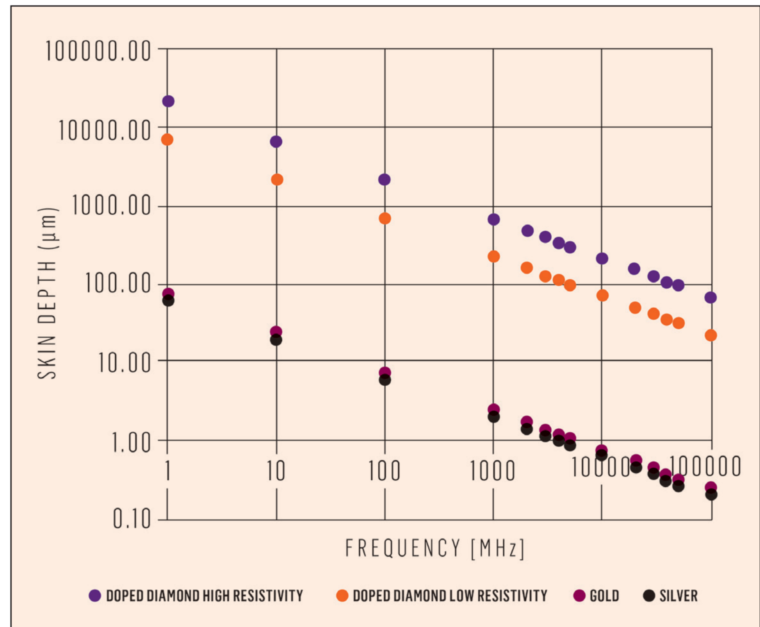


Figure 3: Skin depth for conductors at increasing operation frequency. Boron doped diamond heat spreader at various frequencies

	ε_r	tan δ	κ (W/mK)	α (ppm/K)
AlN	8.8[2] (8.5 GHz)	3.5×10^{-3} (8.5 GHz)[2]	188[3]	3.55[6]
BeO	6.75[2] (8.65 GHz)	4×10^{-4} (8.7 GHz)[2]	260-300[4]	6.48[6]
Diamond	5.72[1]	5×10^{-5} (>1 GHz)[1]	>2000[5]	1.79[6]

Figure 4: Resistive substrates properties (permittivity, loss tangent, thermal conductivity and thermal expansion)

Further reading

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Imec pushes the limits of EUV lithography single exposure for future logic and memory

Imec has made considerable progress towards enabling extreme ultraviolet (EUV) lithography single exposure of N5 32 nm pitch metal-2 layers and of 36 nm pitch contact holes. Greg McIntyre, Peter De Bisschop, Danilo De Simone, Frederic Lazzarino and Victor Blanco from the imec patterning team explain some of the key steps and highlight the impact on the semiconductor industry.

WITH PIONEER WORKS starting in the late 1980's, the road towards EUV infrastructure development and readiness has been a challenging one. Although EUV lithography has a number of similarities to, e.g., 193 nm optical lithography, it presents unique characteristics. For example, with a short imaging wavelength of 13.5nm, EUV radiation is not transmitted through ambient air and is strongly absorbed by all solid materials. Challenges to EUV development included for example the light source (with sufficient power to enable cost-effective production), mask inspection and defectivity, and photoresist issues.

The successful integration of EUV lithography into semiconductor manufacturing would however bring many benefits. For example, the ability to print features with single exposure EUV lithography instead of with multi-patterning 193nm lithography leads to enhanced process simplification and reduced cost per wafer. This has driven the semiconductor industry to continue improving on the scanner, source and mask infrastructure.

In recent years, significant progress has been made for all critical issues. For example, with a recent power demonstration of 250 W, the light source now has

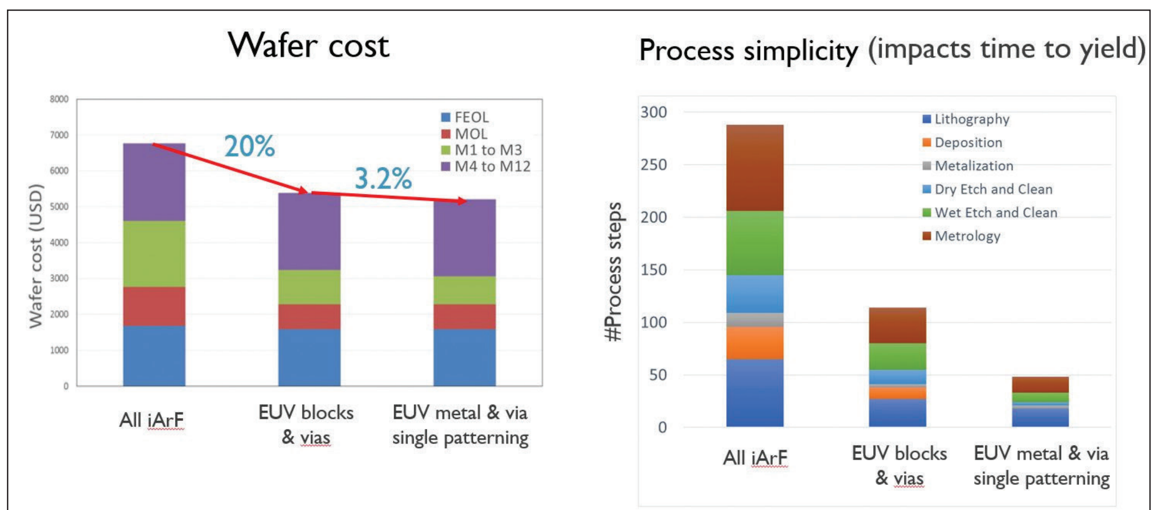

Fig 1: (Left) Benefits of using EUV lithography single exposure in terms of wafer cost and (right) process simplicity

shown capability to meet the roadmap target and ensure sufficient throughput in terms of wafers per hour. First insertion of EUV lithography in high-volume manufacturing is expected in the critical back-end-of-line (BEOL) metal and via layers of the foundry N7 logic technology node (with metal pitches in the range of 36-40 nm), in the 2018-2019 timeframe.

Exploring the options for N5 and beyond

In the meantime, imec and its partners are weighing the options for the following node (32nm pitch and below). At these dense pitches, various patterning approaches are being considered that differ in terms of complexity, wafer cost, and time to yield. These approaches include variations of EUV multi-patterning, hybrid EUV and immersion multi-patterning, and EUV single exposure. Last year, at the 2017 SPIE Advanced Lithography Conference, imec presented many advances in hybrid multi-patterning (hybrid 193i-EUV) by combining, e.g., 193 nm immersion-based self-aligned quadrupole patterning (SAQP) of 32 nm pitch metal lines with a direct EUV print of the block layers.

At the same time, imec has been pushing the limits of EUV single exposure for logic and memory technology nodes, as further benefits can be expected from a single exposure step in terms of process simplicity, wafer cost and time to yield. For example, imec calculated a 20% reduction in wafer cost when transitioning from an all 193 nm immersion-based solution to a solution where blocks and vias are patterned with EUV single exposure. A further 3.2% reduction is expected for EUV single patterning of the critical metal lines and vias. Equally important is time-to-yield, which heavily depends on process complexity. The example of the figure below shows a reduction in roughly 60% required process steps for the hybrid 193i-EUV technique when compared to the all immersion-based solution, and roughly 80% with EUV single exposure. This can translate to days or weeks reduction in the turn-around time for a single wafer lot. Considering a very large number of lots are required to develop a technology, this can result in a significant advantage.

Yet, several challenges still need to be tackled before these small and dense features can be patterned with EUV single exposure. Despite tremendous progress, critical issues remain with respect to e.g. the resist performance, stochastic failures, photomask, metrology and inspections and pattern transfer. In addition, a more fundamental understanding of the critical EUV processes, such as the resist reaction mechanisms, is still lacking. At the 2018 SPIE Advanced Lithography Conference, imec has demonstrated promising advances in all these areas, focusing on two primary use cases: the logic N5 32 nm pitch metal-2 layer, and 36 nm pitch contact holes for dense DRAM applications.

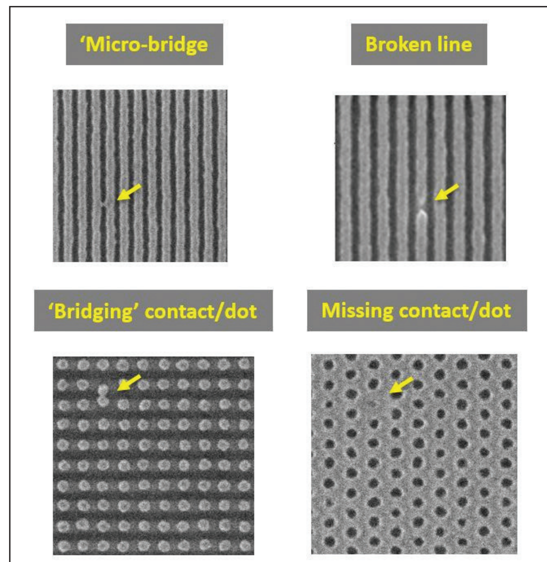

Fig 2: Stochastic printing failures observed after printing (top) lines/spaces, and (bottom) contact holes.

EUV stochastic printing failures: limiting the applicability of EUV lithography

The term 'stochastic effects' refers to random, local variability that occurs between structures that should in principle print identically. These effects have always been part of lithography. Best known is critical dimension (CD) variability, which is quantified through metrics such as line-width roughness, line-edge roughness or local CD uniformity. Over the years, these metrics have been intensively studied. However, next to CD variability, stochastic effects can give rise to local, random failures such as micro-bridges and broken lines (when printing lines/spaces), or bridging contacts and missing contacts (when printing contact arrays). These failures are less understood. They are typically generated throughout the complex resist-pattern-formation process itself. Now that dimensions

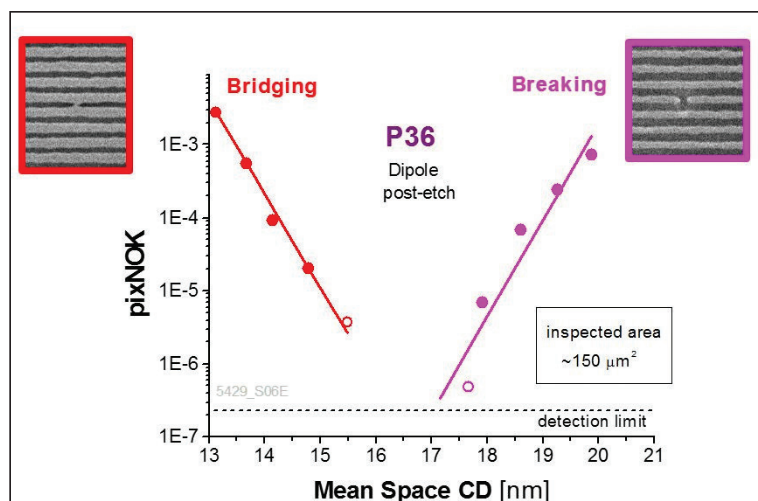

Fig 3: Example of the impact of failure mechanisms on the available target CD-range for dense lines/spaces (36nm pitch). Exposure dose was at ~32mJ/cm².

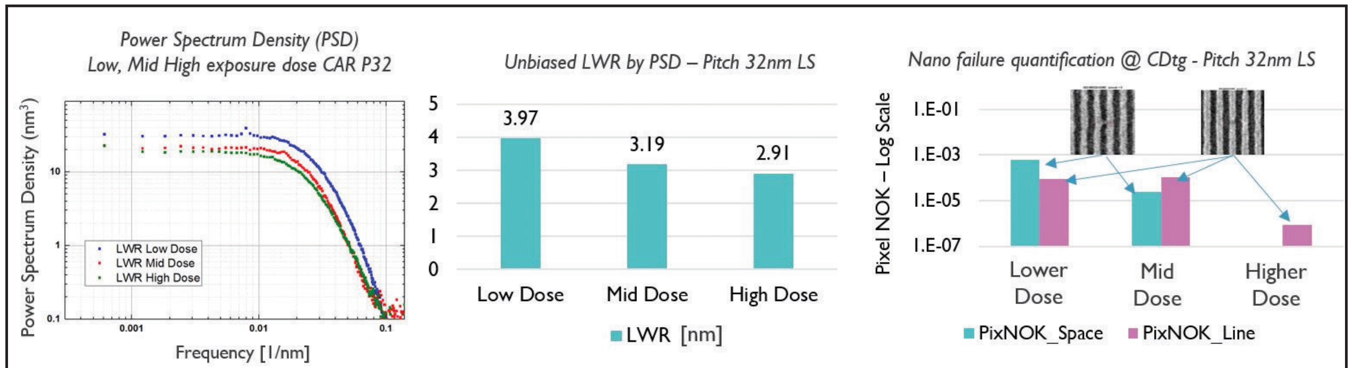

Fig 4: Pitch 32nm line-space: power spectrum density, unbiased LWR and failure analysis for low, mid and high exposure dose EUV chemically amplified resists.

are shrinking and less photons are available during EUV exposure compared with traditional 193nm (immersion) lithography, these failures are expected to increasingly impact the yield of future devices.

To gain more fundamental insights, imec has continued its systematic study of stochastic failures, for both lines/spaces and contact arrays. The team focused on the quantification of the stochastic failures and investigated their dependency on experimental parameters (such as dose, resist, CD). The final goal was to understand how these stochastic effects limit the applicability of EUV lithography, and to identify the knobs that allow minimizing the number of failures. The new method for quantifying the stochastic printing failures consists in automatically counting the relative number of failures (i.e., the missing and bridging contacts, and the line breaking and micro-bridges) that are visible in a series of SEM images. Although this SEM-based technique can only be applied to a limited inspection area, the method is ideally suited for determining the process parameters affecting the number of stochastic failures.

The number of stochastic failures is found to depend on many experimental parameters, providing several knobs for optimization. For example, it largely depends on target CD (line or space), or on the target diameter of the contact hole. E.g., micro-bridges and missing contacts are more abundant as the width of the space or the size of the contact is smaller. This behavior also varies with pitch: for dense pitches, the number of missing (and bridging) contacts

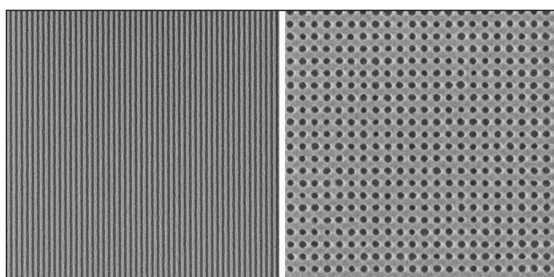

Fig 5: Pitch 32 dense line-space patterning and pitch 36 dense orthogonal contact hole patterning in single EUV exposure (at 45mJ/cm2 and 33mJ/cm2 exposure dose, respectively, on ASML NX3300 EUV scanner tool)

increases rapidly as the size of the contacts becomes smaller (or larger). These stochastic failures limit the available CD-window – the CD-range for which neither type of printing failure is observed – and hence the applicability of EUV lithography.

Importantly, the amount of stochastic failures also has a strong dose dependency: with increasing exposure dose, the number of failures decreases significantly. This implies that exposure dose is a very important knob for reducing the number of stochastic failures. In recent years, resist vendors have been optimizing resists for enhanced resist sensitivity. This way, the resist exposure dose could be reduced close to the cost-effective target of 20mJ/cm2, as to guarantee sufficient wafer throughput. Our findings, however, call for using larger exposure doses as a way to mitigate the stochastic printing failures.

Characterization of the resist performance: introducing new metrics

Over the years, imec, in collaboration with many materials partners, has assessed different resist materials strategies, including chemically amplified resists (CARs, originally developed to work with optical lithography), metal-containing resists and sensitizer-based resists. For most of these materials, comparable performance improvement in terms of resist resolution has been achieved. And the knobs have been identified to enhance the resist sensitivity, and as such enabling more efficient absorption of EUV light.

At the 2018 SPIE Advanced Lithography Conference, imec introduced a comprehensive way of characterizing EUV resists. As an illustration, the characterization was applied on 32 nm dense line/space patterns and on 36nm dense contact hole pitch, for chemically amplified resists. New types of metrics were introduced to judge the quality of the pattern. To quantify resist roughness on resist lines, the imec team used 'power density spectrum' (PSD) as a new metric to compare different resist processes.

This metric is complementary to the traditional metrics based on scanning electron microscopy (SEM) with the benefits of removing the SEM noise (unbiased resist roughness) and looking at the variance of

the variable (linewidth for LWR, line edge position for LER) per unit frequency. Frequency is one over length, so that high frequencies represent short line length scales and low frequencies represent long line length scales. The team also introduced the metric for counting stochastic printing failures, as to provide an early stage assessment on the patterning fidelity of the examined resists at low, mid and high exposure dose. By using all the metrics, a lithographic performance comparison has been made between various resists. Two positive tone chemically amplified resists have been identified at the exposure dose of 45mJ/cm2 and 33mJ/cm2 for logic (pitch 32 nm dense line/space) and for memory (pitch 36 nm dense contact holes) use cases, respectively.

Resist smoothening by post processing: a novel approach

Right after resist exposure and development, post-processing techniques are applied to further smoothen down the resist lines. Imec, in collaboration with etch tool vendors and material suppliers, has proposed new approaches to smoothening, providing encouraging initial results for dense features. In the study, the team focused on 32nm pitch lines/spaces (16nm half pitch (hp)), but the approach can be extended to dense contact holes and pillars.

With the further down-scaling of dimensions, the gap between achievable smoothening (expressed e.g. in terms of line-edge roughness) and the required target is getting increasingly larger. And this makes smoothening of 16nm hp resist lines very challenging. For example, at these small dimensions, the height of the photoresist lines after litho and development is becoming very small (typically 25 – 27nm), leaving very little budget for patterning the underlying layers. Also, top roughness, and defects such as footing, scumming, line interruption and non-bridging are playing an increasingly important role. These roughness and defects are transferred down during subsequent process steps, impacting the device performance.

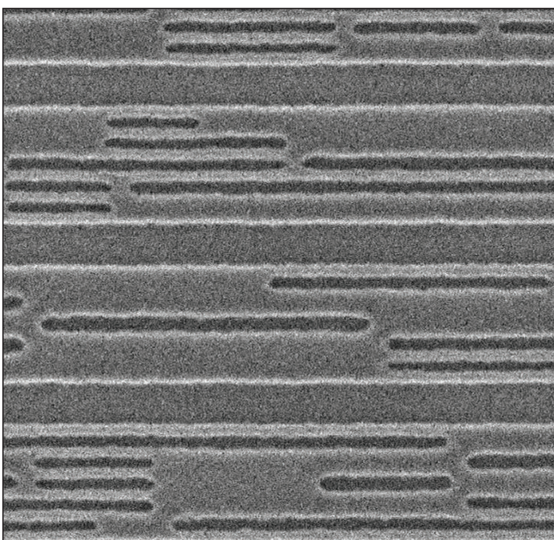

Fig 6: SEM image of a metal-2 logic pattern after litho using retargeting. Note different CD's for isolated and dense features

Imec has first set up a baseline process for chemically amplified and metal-containing resists, allowing to determine the initial process parameters in terms of line-edge roughness, line-width roughness and line CD. Then, various etch approaches (including e.g. direct current super-position and quasi-atomic layer etching) are explored and the knobs are identified that lead to optimized resist smoothening. Although continued optimizations are being done, reductions in post-etch roughness with these techniques have shown roughly 20-30% improvement when compared to a conventional etch technique.

The imec team is also investigating alternative smoothening paths, such as stack optimization. Here, it is investigated how changing the layers underneath the resist (such as photoresist under layer, mask or oxide) impact the etch process and mitigate roughness. Besides stack optimization, novel techniques such as plasma-based smoothening and photoresist encapsulation are being explored. Importantly, new metrology such as power density spectrum and 3D-AFM have been introduced and further developed to optimize resist assessment before and after smoothening.

Computational litho techniques: the benefits of using SRAFs and retargeting

Resist materials advances alone are not sufficient to meet the requirements of EUV lithography single patterning. Imec has also focused on co-optimizing the photomask, film stack, EUV exposure and etch towards an integrated patterning flow to achieve full patterning of the structures. The team also explored the use of advanced computational lithography techniques to improve the patterning of a metal-2 logic layer.

For this metal-2 layer, source optimization (i.e., the optimal illumination setting of the scanner to print this clip), optical proximity correction (OPC) model calibration and OPC have been performed using Tachyon computational lithography software. To optimize the printing of 32 nm pitch lines/spaces, imec has explored the use of design-for-manufacturing (DfM) techniques, i.e. sub-resolution assist features (SRAFs) and retargeting. With SRAFs, specific features (such as scattering bars) are added at mask level, that do not print onto the wafer but do help enlarging the process window for the target features. With retargeting, the original line width or space is changed to enlarge the process window. For example, isolated features are printed wider in order to reduce the number of defects. The team applied the techniques on a traditional dark field mask with positive tone photoresist.

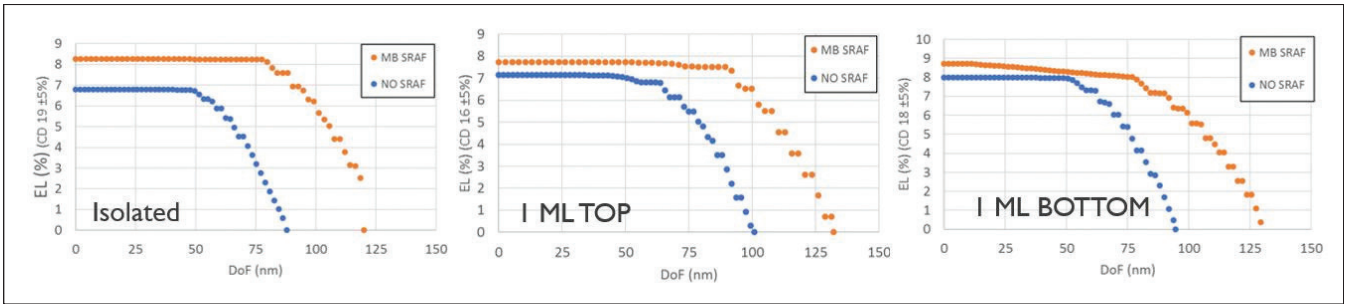

Fig 7: Wafer data showing increased EL and DoF when SRAFs are applied on typical structures within the logic

The use of both SRAFs and retargeting was found to have a number of advantages. First, when using SRAFs, experimental data showed an increased exposure latitude (EL) and depth-of-focus (DoF, the range of focus that keeps the resist profile of a given feature within all specifications for a specified exposure range). Next, applying retargeting increases the defect-free CD process window for printing logic structures as shown in the figure below. And finally, the techniques allow to print metal line tip-to-tips more uniformly (i.e., with regular CD) across different feature types.

Conclusion

Imec, together with its partners, is exploring various options to optimally enable and implement EUV lithography. In this work, imec has pushed the limits of single exposure EUV for printing critical 32nm pitch metal layers and 36nm pitch contact holes. This has been achieved through an increased understanding and optimization of various contributors – including resist performance, stochastic printing failures, photomask, metrology and inspections, and pattern transfer.

The ability of EUV to do single patterning is expected to have a big impact on the roadmap and cost of near-term technology nodes.

The results have been presented in multiple papers at the 2018 SPIE Advanced Lithography Conference.

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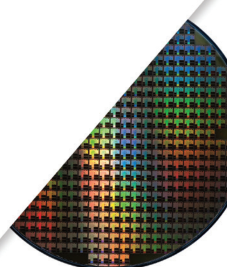

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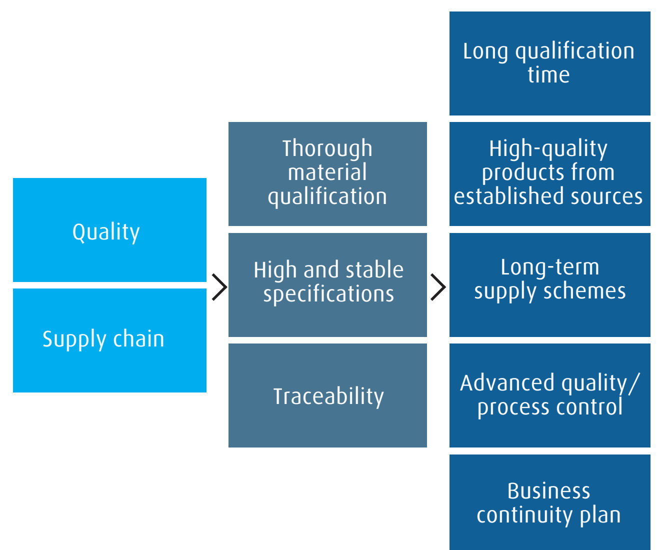

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