



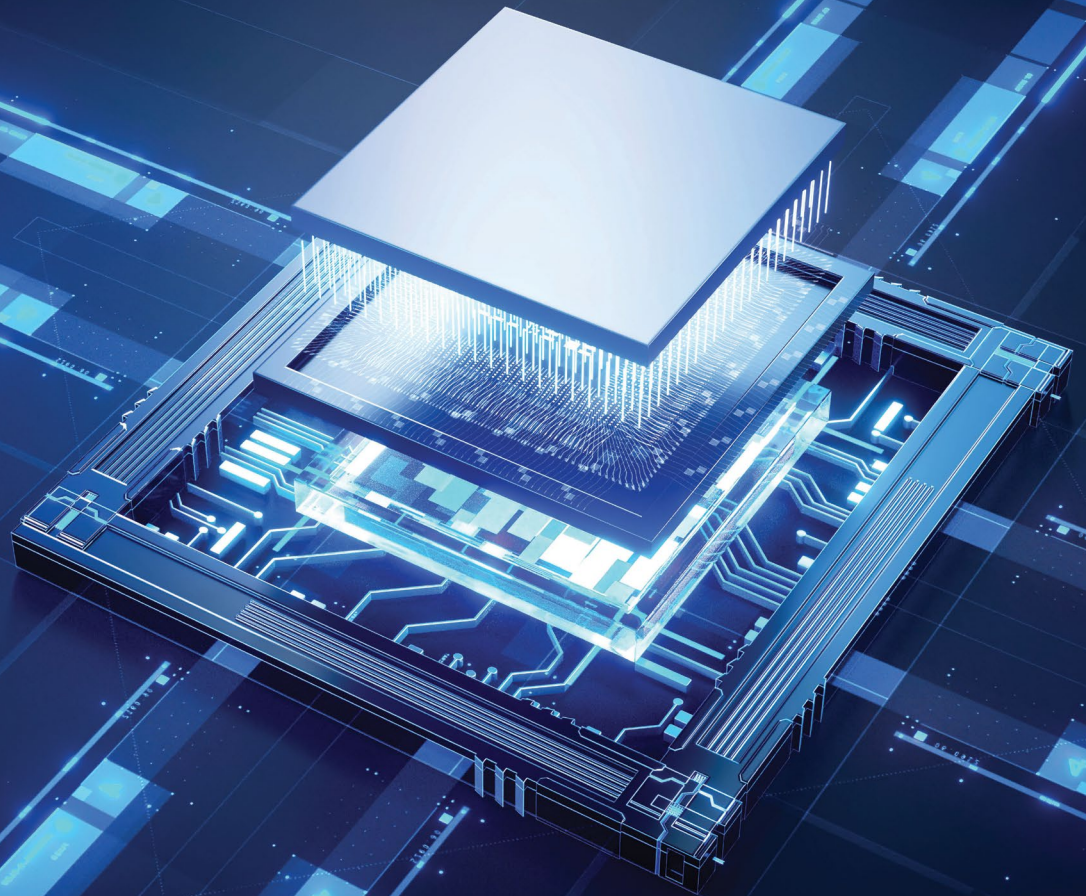
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WHY SUBFAB SYSTEMS ARE BECOMING CRITICAL IN THE AI-DRIVEN ADVANCED PACKAGING ERA



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Physical AI changes the semiconductor equation

➤ The semiconductor industry has spent the past few years responding to an extraordinary expansion in AI computing. The immediate priority has been to deliver more performance, more memory bandwidth and more efficient acceleration for increasingly demanding models, with the data centre emerging as the principal battleground.

Physical AI changes that equation.

As AI moves from generating text, images and code towards controlling machines that sense, plan and act in the physical world, the definition of a suitable AI processor becomes considerably more complicated. The industry is no longer simply being asked to make models run faster. It must enable those models to operate continuously, within tight power budgets, at the edge and, critically, with predictable timing.

This is a significant shift.

A cloud-based AI application can generally tolerate some degree of latency. A robot cannot necessarily do so. If an autonomous machine encounters an unexpected obstacle or a person enters its operating area, the system may have only milliseconds to interpret the situation and respond. Physical AI therefore demands a much closer relationship between inference and the real-world timescale in which the machine operates.

That puts heterogeneous computing firmly in the spotlight. CPUs, GPUs and NPUs are not competing simply to become the one processor that does everything; they can increasingly be viewed as complementary resources. A CPU can provide general-purpose orchestration, a GPU can deliver bursts of highly parallel compute, while an NPU can handle persistent AI workloads at substantially lower power.

For semiconductor designers, this means that performance per watt, latency and determinism may become just as important as peak AI performance.

It also strengthens the case for processing intelligence locally. Sending sensor data continuously to the cloud is

not always practical for autonomous machines, particularly where connectivity is unreliable, latency is critical or battery life is limited. More capable edge silicon will consequently be required, alongside techniques such as quantisation, pruning and other forms of inference optimisation that reduce both computation and data movement.

Yet silicon alone will not solve the Physical AI challenge.

The industry also needs software ecosystems capable of exploiting heterogeneous hardware without making every robotics deployment a bespoke engineering project. Open frameworks, portable models and software abstraction will be essential if Physical AI is to scale beyond highly controlled pilot projects.

And then there is safety. AI controlling a physical machine introduces consequences that simply do not exist when a model is generating a paragraph of text. Functional safety, deterministic execution, operating boundaries and mechanisms capable of overriding autonomous behaviour will all have to evolve alongside the underlying models.

Perhaps most importantly, Physical AI expands the semiconductor opportunity beyond the traditional AI accelerator market. Sensors, edge processors, memory, connectivity, power-efficient compute and specialised silicon will all become components in increasingly intelligent physical systems.

The semiconductor industry's AI revolution has therefore not reached its conclusion. It may be entering a second, potentially broader phase.

The first challenge was teaching machines to understand and generate information. The next is teaching them to act on that understanding safely and efficiently in the real world.

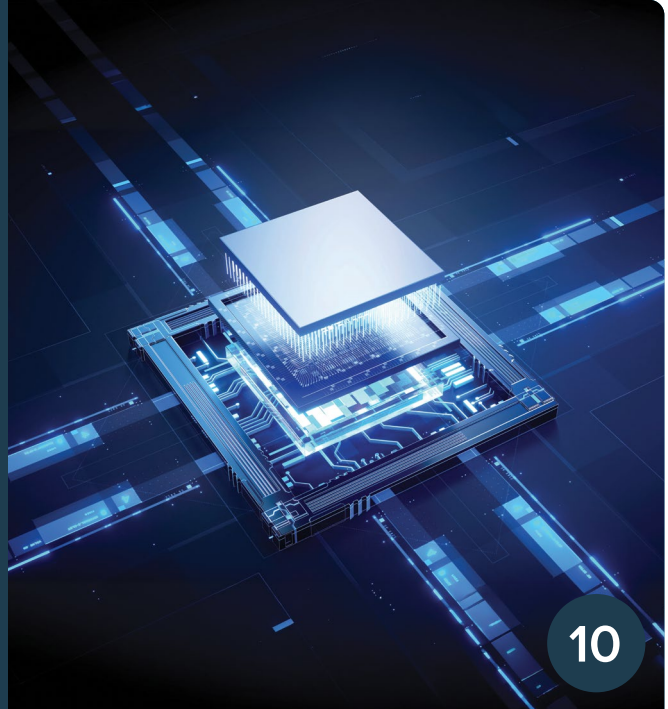
For the chip industry, that means the future of AI may be measured not only in tokens per second, but in how intelligently, efficiently and reliably silicon can make machines move.

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Qnity advances AI packaging

Qnity has introduced an integrated materials platform for advanced 2.5D and 3D packaging, targeting fine-pitch interconnects, HBM, chipllets and emerging substrate architectures through metallization, bumping, dielectric and patterning technologies.

QNITY ELECTRONICS has introduced an integrated materials and process technology platform targeting the manufacturing challenges associated with next-generation 2.5D and 3D semiconductor packaging, including chiplet-based architectures, high-bandwidth memory (HBM) and advanced substrate technologies.

The platform brings together metallization, solder bumping, dielectric materials and fine-line patterning processes, addressing the increasing requirements for interconnect density, coplanarity, critical-dimension control and manufacturing yield as AI accelerator architectures become more complex.

Advanced packaging approaches such as Chip-on-Wafer-on-Substrate (CoWoS), Embedded Multi-die Interconnect Bridge (EMIB) and HBM require increasingly precise control of plated structures and interconnect geometry.

Qnity's portfolio supports SnAg micro-bumps, copper-to-copper direct and hybrid bonding, as well as high-

resolution dielectric and patterning processes.

The company reports that its processes can support 2 μm line/space metallization while maintaining tight critical-dimension control and low defectivity.

For HBM and other fine-pitch applications, the company's solder plating technology is designed to provide controlled micro-bump formation and improved coplanarity across mixed-pitch structures.

Copper deposition technologies are also aimed at improving within-die uniformity and plating consistency, which become increasingly important as interconnect dimensions shrink and package architectures increase in scale.

The materials platform additionally addresses the dielectric and lithography requirements of advanced packaging. Thick dry-film photoresist technology is designed for high-aspect-ratio copper pillar formation and fine-feature patterning, while dry-film photo-imageable dielectric materials target

fan-out panel-level packaging and advanced substrates.

Glass-core substrate applications are another focus, with the dielectric technology supporting through-glass via (TGV) filling and reliability requirements.

Such substrate architectures are attracting increasing interest as the semiconductor industry looks for higher-density interconnects and scalable packaging platforms capable of supporting larger and more complex AI systems.

The broader development reflects a shift toward greater integration between materials engineering and packaging process development.

As AI, chiplets, HBM and heterogeneous integration drive higher interconnect densities and increasingly three-dimensional structures, controlling dimensional uniformity, surface characteristics, coplanarity and defectivity across multiple process steps is becoming critical to achieving reliable high-volume manufacturing.



Everspin and Teledyne HiRel partner to advance MRAM for aerospace and defense

New partnership will bring Everspin 256Mb PERSYST MRAM into Teledyne HiRel Semiconductors' memory solutions for mission-critical systems.

EVERSPIN TECHNOLOGIES, a developer and manufacturer of MRAM solutions, and Teledyne HiRel Semiconductors, a business unit of Teledyne Technologies Incorporated and a leading supplier of high-reliability semiconductor solutions, today announced a strategic partnership to accelerate adoption of Everspin's MRAM in aerospace, defense and other demanding systems. This collaboration will begin with the 256Mb PERSYST spin-transfer torque MRAM (STT-MRAM), a non-volatile memory that combines RAM-like speed with the ability to retain data through power loss, system resets and unexpected interruptions.

Through the new partnership, Teledyne HiRel will initially offer Everspin's 256Mb PERSYST STT-MRAM as part of its memory products portfolio for military and aerospace customers, with target applications including avionics, VPX and single-board computer platforms, radar and electronic warfare payloads, satellite electronics, autonomous systems and other next-generation electronic solutions. The agreement also covers other PERSYST STT-MRAM products, including 64Mb and 128Mb options, giving customers additional density choices as program requirements vary.

As component availability, lifecycle planning and long-term supply become greater considerations for programs with long service lives, customers are evaluating persistent memory options that enable fast writes, high endurance and data retention through power loss. These capabilities are especially important for startup, configuration storage, event logging, recovery and other functions that must remain available throughout the product's service life.

Because PERSYST enables frequent writes with high endurance and retains data without battery backup, it can replace or complement NOR flash in applications that need faster updates or power-loss-safe storage, reducing a program's reliance on battery-backed SRAM, hold-up power or capacitor-backed memory schemes. By combining RAM-like access with non-volatility, MRAM can also help simplify architectures that would otherwise require separate volatile memory, non-volatile storage, backup power, wear-leveling strategies or complex data-protection circuitry. Teledyne HiRel will back this new capability with product guidance, screening flows, qualification documentation, procurement support and obsolescence management.

"Aerospace and defense programs require memory solutions that can sustain long operating lifecycles, documented qualification requirements and reliable performance in harsh environments," said Mont Taylor, Vice President of Business Development at

Teledyne HiRel Semiconductors. "By adding Everspin's PERSYST STT-MRAM to our non-volatile memory portfolio, we give customers a qualified path to specify persistent memory for their most critical applications."

"PERSYST MRAM delivers a unique combination of endurance, instant-on data retention and high-performance operation," said Sanjeev Aggarwal, President and CEO of Everspin Technologies. "Through our partnership with Teledyne HiRel, customers gain access not only to advanced MRAM technology, but also to the screening expertise and supply continuity needed throughout extended program timelines. This collaboration helps reduce adoption barriers while providing confidence in long-term product availability."

PERSYST MRAM products will ship from Teledyne HiRel Semiconductors' facility in Milpitas, California, with customer availability anticipated in the fourth quarter of 2026.



IFX Technologies launches as a European DeepTech Platform for functional fluid technologies

Newly established DeepTech venture combines an internationally established technology platform with industrially validated applications, focusing on the growth markets of Semiconductors & Electronics, Energy & Chemicals, and Industrial Maintenance.

IFX TECHNOLOGIES GmbH launches as a new European DeepTech company for functional fluid technologies in demanding industrial processes. Building on the internationally established intelligent fluids® technology platform, an extensive IP portfolio, existing customer relationships, and an experienced team, IFX Technologies is focused on further technological development and international scaling.

At the core of the company is the proprietary IFX Technology Platform – a patented generation of functional multiphase fluids. Its high degree of variability allows the fluids to be precisely tailored to different materials, processes, and industrial requirements, enabling highly effective and selective cleaning and separation processes. This provides a profitable and sustainable alternative to conventional solvent-based processes.

Applications include material separation processes such as the removal of paints/coatings and adhesives/resins, as well as other demanding cleaning processes involving oils/greases and process-related organic contaminants. The water-based, pH-neutral, non-flammable, and readily biodegradable fluids significantly reduce process times, energy consumption, and Total Cost of Ownership, combining technological efficiency with measurable economic and environmental benefits.

The IFX technology is not a vision for the future: it has already been qualified by leading semiconductor and industrial companies in Europe and is in series production use. Its application spectrum ranges from highly specialized processes such as photoresist stripping and metal lift-off in the semiconductor industry to industrial maintenance applications and the

cleaning of production equipment and heat exchangers in the energy and chemical industries.

At the same time, increasing regulatory pressure on conventional chemicals and solvents worldwide is accelerating the shift toward economically viable alternatives and creating additional growth opportunities for IFX Technologies.

“With IFX Technologies, we are taking an already industrially established technology platform into its next phase of growth. Our goal is to address specific industrial challenges with solutions that are more powerful, economical, and sustainable than conventional processes,” said Christian Römlein, CEO and Co-Founder of IFX Technologies GmbH.

IFX Technologies is supported by Heing® Venture Architects as an investor and value-creation partner.

“With IFX Technologies, we are taking an already industrially established technology platform into its next phase of growth. Our goal is to address specific industrial challenges with solutions that are more powerful, economical, and sustainable than conventional processes,” said Christian Römlein

Heing® is a global partnership for industrial transformation that builds and scales technology-driven companies.

“Industry needs alternatives that deliver not only environmental benefits but, above all, compelling economics. This is precisely where we see the strength of IFX: an industrially validated platform technology with measurable customer value and significant potential for international scaling. Together with the experienced team, we intend to systematically expand this position,” added Manuel Hein, Founder & Managing Partner of Heing® Venture Architects.

IFX Technologies is also laying the foundations for further growth internationally. The company has been selected for the KAUST ScaleX 2026 Cohort of King Abdullah University of Science and Technology (KAUST) in Saudi Arabia. The program supports international technology companies in entering and scaling within the Saudi Arabian market and provides IFX with access to a strong network of industry, research, and strategic partners – serving as a starting point for further expansion into Arab markets.

With its headquarters in Leipzig, production in Leuna, and a highly qualified team, IFX Technologies has a strong foundation for further international expansion. Together with strategic partners, the company plans to expand its production, sales, and service capabilities across Asia, the GCC countries, India, and the United States – particularly through regional joint ventures and partnerships.

In doing so, IFX is laying the foundation for scaling its technology platform internationally across new markets and industrial applications.

ASML begins construction of new Eindhoven campus

New campus will add manufacturing capacity in support of ASML's planned growth needs.

ASML Holding N.V. (ASML) marked the start of construction of its second major industrial campus in the Brainport region, the Netherlands. Together with partners, the company celebrated the milestone with a groundbreaking ceremony at Brainport Industries Campus (BIC) North, launching a multi-phase development project that will eventually span approximately 350,000 square meters and provide potential capacity for up to 20,000 workplaces.

The new location ensures that key activities remain closely connected within the region and are an integral part of the company's global network. The milestone was celebrated during a ceremony attended by the Dutch Prime Minister Rob Jetten and representatives from government, customers, suppliers, knowledge institutions and regional partners.

"The growing global demand from the semiconductor industry requires continuous investments," said

Christophe Fouquet, President and CEO of ASML. "As part of our global expansion plans, BIC North provides the space and flexibility we need to continue innovating and supporting our customers around the world. It will complement our existing office space and manufacturing capacity in the Brainport region and further strengthen our footprint in the Netherlands.

This milestone would not have been possible without close collaboration with local, regional and national authorities and we are particularly grateful for the support we have received from the City of Eindhoven."

A new location, introducing an innovative way of working

The first phase of BIC North, expected to be completed in 2029, will house at least 3,000 employees, bringing together production, logistics and supporting office activities in one integrated industrial campus. These workplaces are primarily intended for

teams relocating from existing ASML locations.

A key element of the campus will be ASML's new flow factory, ASML's next-generation innovative manufacturing operating model for the TWINSCAN factory. This model is designed to enable faster, more efficient and higher-scale module production and installation. It streamlines the flow of materials and work through the factory, helping improve productivity while maintaining high-quality standards. The approach follows proven models used in other industries such as automotive and aerospace.

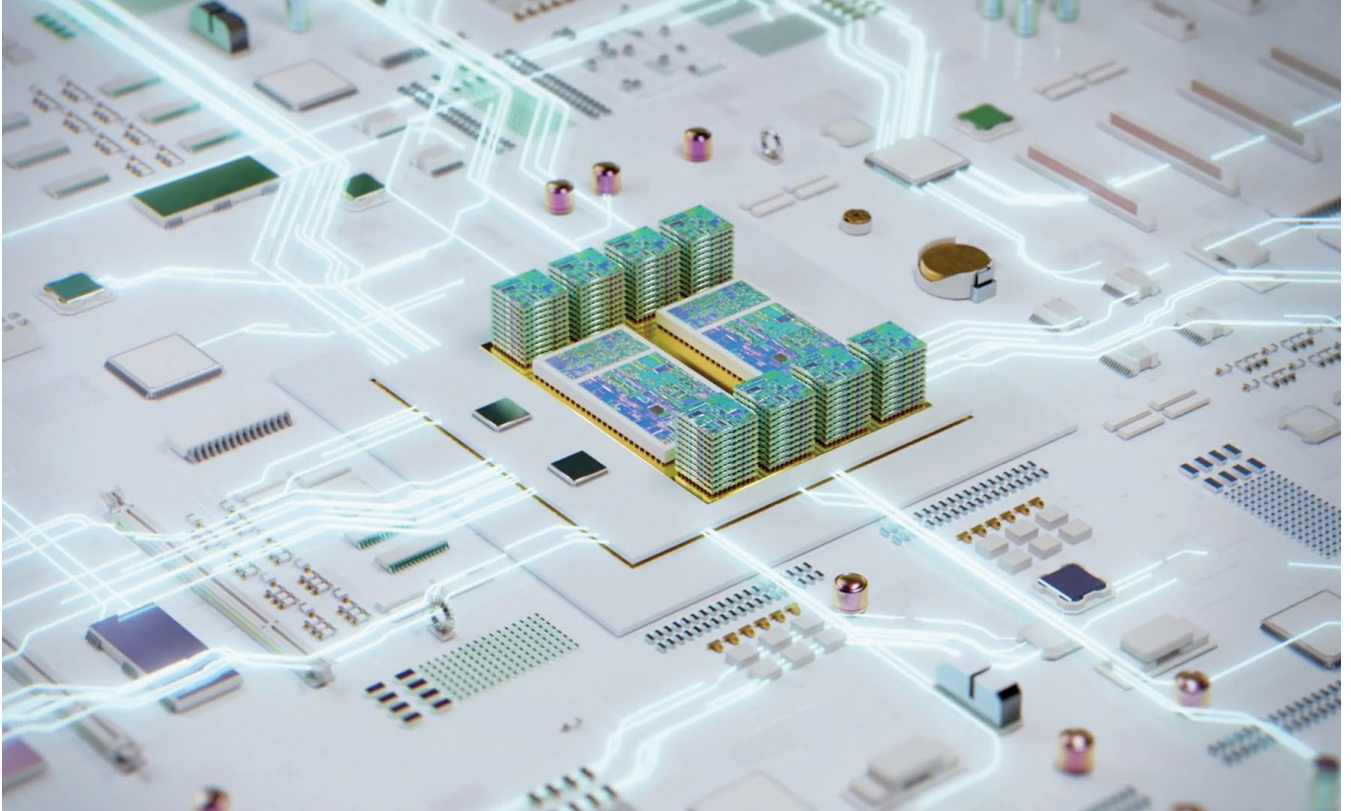
Future footprint in the brainport region

In the long term, the BIC campus could accommodate up to 20,000 workplaces, depending on future requirements, providing the flexibility needed to support industry growth.

ASML's future footprint in the Brainport region will comprise three complementary campuses: a dedicated headquarters campus (De Run 1000) and an industrial campus (De Run 6000/7000) in Veldhoven, alongside the company's second industrial campus at BIC North in Eindhoven. Together, these locations will support ASML's innovation, manufacturing and corporate activities in the region.

The development of BIC North reflects the close collaboration between ASML, governments, knowledge institutions and many other stakeholders. Through public-private partnerships, ASML and its partners continue to invest in long-term priorities such as talent development, affordable housing and equal opportunity, helping to support sustainable growth for both the company and the Brainport region.





Why subfab systems are becoming critical in the AI-driven advanced packaging era

As AI drives advanced packaging towards greater complexity and scale, vacuum, exhaust and abatement systems are becoming critical to improving semiconductor manufacturing throughput, yield and sustainability.

BY RACHEL REN, EDWARDS VACUUM

THE SEMICONDUCTOR industry is undergoing a fundamental transition. For decades, performance improvements were largely achieved through transistor scaling, guided by Moore's Law. Today, that paradigm is no longer sufficient to meet the demands of emerging applications, most notably artificial intelligence (AI).

AI workloads, particularly those associated with large language models and generative systems, are driving unprecedented increases in compute density, memory bandwidth, and system complexity. As a result, the semiconductor market is accelerating toward the trillion-dollar threshold faster than previously anticipated, reflecting not only

cyclical recovery but structural transformation.

However, the most significant shift is not simply in demand, but in how performance is delivered. The industry is moving from device-centric scaling to system-level optimization, where integration, interconnect, and infrastructure increasingly define performance limits.

Within this context, advanced packaging has emerged as a critical enabler of AI systems. Yet beneath this visible transformation lies a less discussed but equally important constraint: subfab infrastructure. Vacuum, exhaust, and abatement systems, historically treated as support utilities, are rapidly becoming

essential to enabling throughput, yield, and sustainability in advanced manufacturing.

AI and the shift to system-level scaling

AI workloads impose a unique set of requirements on semiconductor systems. Unlike traditional computing applications, they demand simultaneous scaling across multiple dimensions: compute throughput, memory capacity, interconnect bandwidth, and power efficiency. These requirements have exposed the limitations of relying solely on transistor scaling to drive performance.

As a result, the industry has converged on a system-level architecture that

integrates advanced logic, high-bandwidth memory (HBM), and advanced packaging technologies such as 2.5D interposers, 3D stacking, and chiplet-based designs.

This approach enables performance gains by optimizing data movement and system integration rather than relying exclusively on device shrink.

Advanced packaging has therefore transitioned from a back-end process to a primary driver of system performance. Heterogeneous integration allows designers to combine logic, memory, and specialized accelerators in close proximity, reducing latency and increasing bandwidth. Industry analysts have highlighted that technologies such as hybrid bonding and wafer-level integration are essential to sustaining performance growth in high-volume manufacturing.

This shift also reflects a broader change in scaling philosophy. Performance is no longer defined by the smallest feature size, but by the efficiency with which components are integrated into a complete system.

Advanced packaging as the “Middle-End”

The evolution of advanced packaging is redefining the traditional boundaries of semiconductor manufacturing. Historically, the industry was divided into front-end processes for transistor fabrication and back-end processes for assembly and packaging. Today, advanced packaging occupies an

intermediate domain often described as the “middle-end.”

This middle-end combines elements of both FE and BE. Processes such as through-silicon vias (TSV), redistribution layers (RDL), and hybrid bonding rely on FEOL-class techniques, including etch, chemical vapor deposition (CVD), and atomic layer deposition (ALD). At the same time, these processes are closely tied to system-level integration and final device assembly.

The result is a convergence of process complexity and integration requirements. Advanced packaging is no longer a passive assembly step; it is a yield-critical, performance-defining stage of manufacturing. Increasingly, these processes are being integrated directly into leading-edge wafer fabs, further blurring the distinction between front-end and back-end operations.

The emerging constraint: Subfab infrastructure

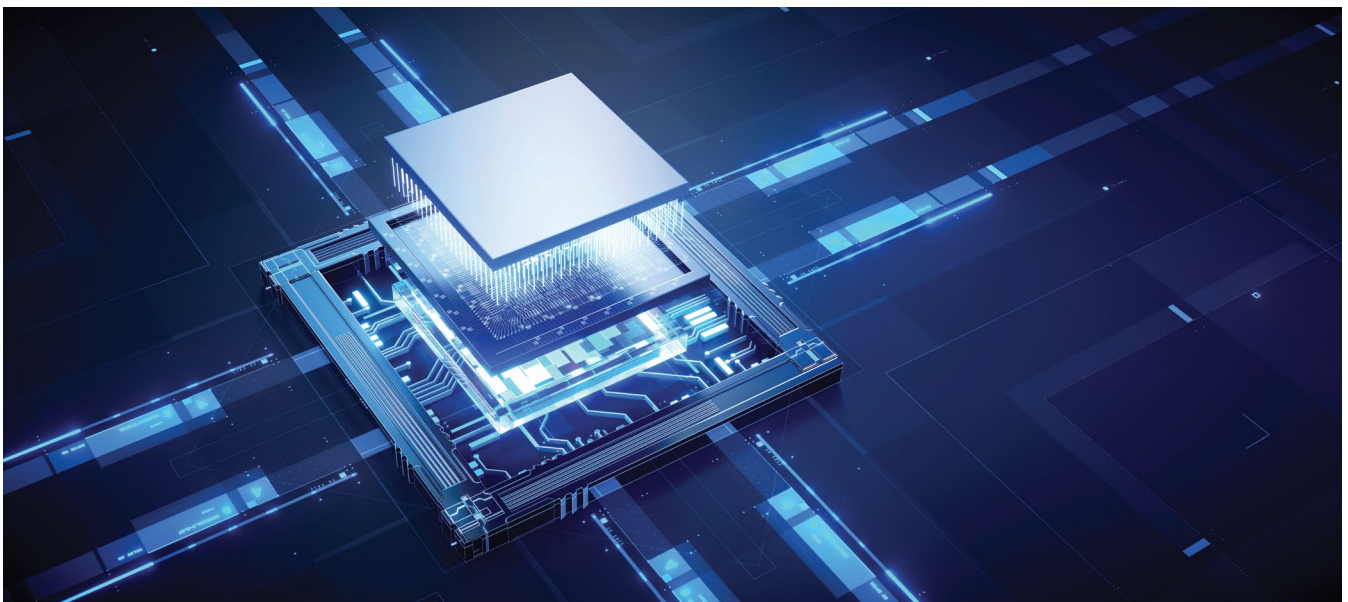
While attention has focused on device architectures and packaging technologies, the supporting infrastructure within the subfab is becoming a critical determinant of manufacturing performance. Subfab systems are responsible for maintaining vacuum conditions, managing process exhaust, and ensuring safe and efficient handling of process byproducts. These functions are essential for enabling the advanced processes required in both FEOL and advanced packaging environments.

In modern high-volume manufacturing, subfab environments are highly complex systems. A single fab may contain thousands of vacuum pumps and abatement units. Typically, each process chamber is supported by a dedicated dry vacuum pump, while each multi-chamber process tool shares a common abatement system that treats exhaust from all of its chambers. Failures or inefficiencies in these systems can have immediate and significant impacts on throughput and yield.

As process complexity increases, the role of subfab infrastructure is shifting from passive support to active performance enabler. This shift is driven by several converging challenges.

Advanced packaging processes are characterized by higher material volumes and more complex process flows than traditional back-end operations. Steps such as TSV etch and dielectric deposition require higher gas flow rates, tighter pressure control, and more stringent process stability.

These requirements place new demands on vacuum systems. Pumping speed and stability directly influence process cycle time and uniformity. Faster pump-down times enable higher throughput, while stable vacuum conditions reduce process variation and defect formation. In high-volume manufacturing, even small improvements in these parameters can translate into significant gains in productivity and cost efficiency.



The relationship between vacuum performance and manufacturing output is therefore becoming increasingly direct. Subfab systems are no longer peripheral to productivity; they are integral to it.

Materials innovation and chemical complexity

The introduction of new materials and processes has significantly increased the chemical complexity of semiconductor manufacturing. Advanced packaging and leading-edge FEOL processes involve a wide range of reactive gases, condensable byproducts, and corrosive chemistries.

These conditions present substantial challenges for vacuum and exhaust systems. Condensation of byproducts within pumps or exhaust lines can lead to blockages, increased power consumption, and eventually system failure. At the same time, efforts

to prevent condensation, such as increasing operating temperature, can accelerate corrosion and material decomposition.

Balancing these competing effects requires a detailed understanding of process chemistry and careful design of thermal and material systems. Failure to manage these interactions can result in reduced equipment lifetime, increased maintenance requirements, and unplanned downtime.

Thermal management beyond the process chamber

Thermal control has traditionally been focused on the process chamber, where temperature directly affects film deposition and etch performance. However, as process complexity increases, thermal management must extend throughout the entire gas handling pathway, including forelines, pumps, and exhaust systems.

Chemical reactions do not cease at the chamber boundary. Byproducts can continue to react or condense within the vacuum system, influenced by local temperature and pressure conditions. Maintaining an appropriate thermal profile across this extended system is critical to prevent both condensation and decomposition.

This creates a narrow operating window. Temperatures that are too low promote condensation and particle formation, while temperatures that are too high can lead to unwanted chemical reactions and material degradation. Achieving the correct balance is essential for maintaining process stability and yield.

Footprint constraints and equipment density

Another significant challenge arises from the increasing density of process tools within advanced fabs. To maximize productivity and return on capital investment, manufacturers are deploying multi-chamber cluster tools with up to ten or more process modules per platform.

While tool density increases, available subfab space does not. Supporting systems must fit within the footprint of the process tool, often referred to as the tool "shadow." As a result, vacuum and abatement systems must deliver higher performance within increasingly constrained physical dimensions.

Industry trends indicate a need for substantial reductions in equipment footprint, on the order of 20–30%, while simultaneously increasing capacity.

This creates a fundamental engineering challenge: delivering higher pumping speed and flow capacity without increasing system size. Solutions require innovations in system design, modularization, and integration.

Energy consumption

Energy efficiency has become a central concern in semiconductor manufacturing, driven by both economic and environmental factors. Subfab systems are among the largest consumers of energy within a fab. Estimates suggest that vacuum and abatement systems can account for approximately 20% of total facility energy consumption, and in some process tools, vacuum alone represents more than half of total power usage.

Infrastructure is now a scaling lever

IN THE ADVANCED PACKAGING ERA, SUBFAB PERFORMANCE DIRECTLY IMPACTS YIELD, UPTIME, AND SUSTAINABILITY



At the same time, the industry is under increasing pressure to reduce greenhouse gas emissions and meet sustainability targets. Analysis of vacuum system lifecycle emissions indicates that the vast majority, approximately 97%, are associated with energy consumption during operation.

This makes energy efficiency a key lever for both cost reduction and environmental impact. Improvements in pump design, system integration, and operational control can significantly reduce energy usage while maintaining or improving performance.

Digitalization and predictive maintenance

The increasing complexity of subfab systems has driven the adoption of digital technologies and data-driven approaches. Modern fabs generate large volumes of data from sensors monitoring pressure, temperature, vibration, and flow. When combined with advanced analytics and domain knowledge, this data can be used to predict equipment failures and optimize system performance.

Predictive maintenance represents a significant advancement over traditional preventive approaches. By identifying early indicators of degradation, maintenance can be scheduled proactively, reducing unplanned downtime and extending equipment life.

Moreover, integrating data across the entire vacuum and abatement system enables a holistic understanding of system behavior. Interdependencies between components can be identified and addressed, improving overall reliability and performance.

Sustainability as a system-level constraint

Sustainability is rapidly emerging as a defining constraint in semiconductor manufacturing. TSMC recently committed to achieving net-zero emissions by 2050, reflecting a broader industry recognition that environmental impact must be addressed alongside performance and cost.

While the semiconductor sector is not a major direct emitter of greenhouse gases, its indirect footprint driven by energy-intensive manufacturing and the rapid growth of AI infrastructure

is significant and expanding. The industry increasingly applies the Greenhouse Gas Protocol framework, which categorizes emissions into Scope 1 (direct), Scope 2 (purchased energy), and Scope 3 (value chain), to guide sustainability strategies across operations and supply chains.

Subfab systems play a central role in this effort. Vacuum and abatement infrastructure directly influence all three emission scopes: they consume substantial power, manage process exhausts, and impact downstream efficiency. As a result, sustainability in the subfab is no longer a compliance issue but a system-level engineering challenge.

Advances in abatement and energy-efficient vacuum technologies are already delivering measurable impact. In 2020, Edwards' abatement systems prevented approximately 17.7 million tons of CO₂-equivalent emissions at customer facilities comparable to the annual emissions of cities such as Madrid and Milan. These results illustrate the scale at which subfab innovation can contribute to industry-wide decarbonization.

Looking ahead, achieving sustainability targets will require tighter integration between process tools and subfab systems, real-time energy optimization, and continued collaboration across the supply chain. Subfab infrastructure is therefore becoming a critical lever, not only for manufacturing performance, but for enabling sustainable scaling in the AI era.

From support function to strategic lever

The cumulative impact of these trends is a fundamental redefinition of the role of subfab infrastructure. No longer confined to a supporting role, subfab systems now directly influence key manufacturing outcomes, including yield, throughput, reliability, and cost of ownership.

This shift reflects a broader transition within the semiconductor industry toward system-level optimization. As processes become more complex and interconnected, performance depends on the coordinated operation of all system components. Subfab infrastructure is an integral part of this system.

The semiconductor industry is entering an era where scaling is no longer defined solely by device dimensions. Instead, it is increasingly determined by the ability to integrate and manufacture complex systems at scale.

Conclusion

The semiconductor industry is entering an era where scaling is no longer defined solely by device dimensions. Instead, it is increasingly determined by the ability to integrate and manufacture complex systems at scale.

Advanced packaging has emerged as a critical enabler of this transition, providing the means to overcome the limitations of traditional scaling. However, the effectiveness of these technologies depends on the performance of the underlying infrastructure.

Subfab systems, vacuum, exhaust, and abatement, are now central to achieving the throughput, yield, and sustainability required for next-generation manufacturing. They are no longer invisible utilities but strategic assets that directly influence competitive performance.

In the AI-driven era, the winners will not only be those who design the most advanced chips, but those who can manufacture them efficiently, reliably, and sustainably. Achieving this will require a holistic approach that integrates device innovation, process development, and infrastructure engineering.

Ultimately, the path forward is clear: scaling is no longer just about the chip, it is about the infrastructure that enables it.



Streamlining sub-system integration: Bridging the gap between PLC networks and SECS/GEM hosts

Why PLC networks and SECS/GEM hosts operate so differently, the practical challenges engineers face when bridging them, and the role protocol gateways play in solving the problem.

BY EINNOSYS TECHNOLOGIES

SEMICONDUCTOR FABs are built on a patchwork of equipment, and much of it doesn't speak the same language. Process tools, sub-systems, and material handling equipment are frequently controlled by industrial PLCs, while the fab host systems communicate exclusively in SECS/GEM. When these two worlds need to exchange data — as they increasingly must for MES connectivity and Industry 4.0 initiatives — engineers run into a fundamental interoperability problem. PLC to SECS/GEM integration has become one of the more overlooked but critical pieces of equipment connectivity in modern semiconductor manufacturing, and getting it right has a direct impact on data quality, uptime, and factory automation maturity.

Why PLC networks and SECS/GEM Hosts operate differently

PLCs were designed for deterministic, real-time control of physical processes — reading sensors, actuating valves, sequencing motion, and enforcing

safety interlocks. Their communication protocols, such as Mitsubishi MC Protocol, Siemens S7, and Omron FINS, are optimized for speed and reliability at the machine level, not for describing equipment state to a factory host.

SECS/GEM, by contrast, is a semiconductor-specific communication standard defined under SEMI E5 (SECS-II) and SEMI E30 (GEM). It was built to describe equipment state, event reporting, alarm handling, and recipe management in a structured, host-facing format that MES and factory systems can consume consistently across different tool vendors. A SECS/GEM host doesn't care how a valve was actuated — it cares whether the equipment is idle, processing, or in an alarm state, and it expects that information in a standardized message format.

The result is two protocol worlds built for different purposes: one optimized for control at the machine, the other

optimized for visibility at the factory level. Bridging them requires more than a simple data pipe — it requires translation.

Common challenges in sub-system integration

Integration engineers who have tried to connect PLC-controlled sub-systems to a SECS/GEM host directly tend to run into the same set of obstacles:

- **Protocol mismatch.** PLC protocols expose raw registers and tags, not GEM-compliant state models or event reports.
- **No native equipment state model.** PLCs typically don't track equipment states (idle, setup, executing, alarm) in a way that maps cleanly to GEM's state machine expectations.
- **Alarm and event structure.** SECS/GEM expects structured alarm and event reporting (via Collection Events and Alarm IDs), while PLC alarm data is often just discrete bits or fault codes.
- **Recipe parameter handling.** Recipe download/upload workflows

expected by a GEM host have no direct equivalent in most PLC programs.

- **Legacy of equipment constraints.** Older PLC-controlled tools were never designed with host connectivity in mind, and reprogramming the PLC logic itself is often not practical or supported by the OEM.

These challenges explain why direct, custom point-to-point integrations tend to be fragile, expensive to maintain, and difficult to replicate across multiple tools or fab lines.

The role of protocol translation

Protocol translation is the layer that resolves this mismatch. Rather than forcing a PLC to natively “speak” SECS/GEM — which is rarely realistic given PLC programming constraints — a translation layer sits between the two systems, reading data from the PLC in its native protocol and re-expressing it as GEM-compliant equipment state, event, and alarm data for the host.

This approach keeps the PLC’s control logic untouched while giving the SECS/GEM host the structured, standards-compliant information it expects. It also isolates protocol-specific complexity in one place, rather than distributing it across every PLC program the fab needs to integrate.

PLC communication protocols used in semiconductor equipment

A functional integration layer typically needs to support a range of protocols, since fabs rarely standardize on a single PLC vendor or communication method:

- Ethernet/IP - common in Allen-Bradley/Rockwell-controlled equipment.
- Profinet - widely used in Siemens-based automation
- Siemens S7 - native protocol for Siemens PLC families
- Mitsubishi MC Protocol - common across Mitsubishi-controlled sub-systems
- Omron FINS - used in Omron-controlled equipment
- Modbus TCP - a widely adopted, vendor-neutral industrial protocol
- OPC UA - increasingly used as a modern, standards-based data exchange layer

Supporting this breadth of protocols matters because semiconductor fabs are rarely single-vendor environments; a practical integration layer has to accommodate whatever mix of controllers is already installed on the floor.

Data acquisition from PLCs

The integration layer polls or subscribes to relevant PLC registers and tags to acquire process values, status bits, and fault codes in real time.

Real-time equipment monitoring

That raw data is mapped into a live equipment status model, giving visibility to whether a tool is running, idle, in setup, or faulted.

Protocol conversion

Native PLC data is converted into SECS/GEM-compliant messages, following the structure expected by SEMI E5/E30.

Equipment status reporting

State changes are reported to the SECS/GEM host as they occur, keeping the host’s view of equipment status current.

Alarm & event management

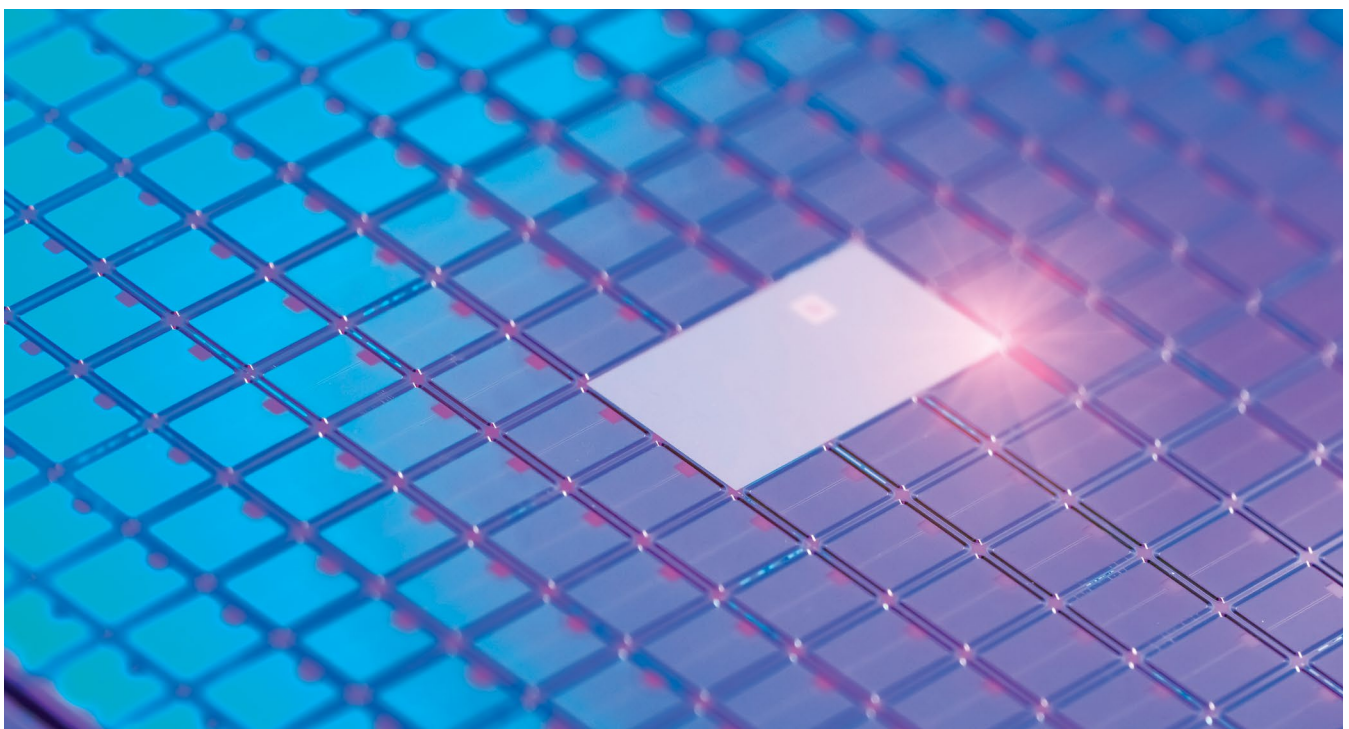
PLC fault codes and discrete alarm bits are mapped to structured Alarm IDs and Collection Events, so the host receives standardized alarm and event data instead of raw codes.

Recipe parameter collection

Where applicable, recipe parameters are collected from or written to the PLC in a way that satisfies GEM’s recipe management expectations.

How a PLC-to-SECS/GEM gateway works

In practice, most successful implementations follow a consistent architecture: PLC Network → Protocol Gateway → SECS/GEM Host → MES → ERP, with bidirectional communication at each stage. The gateway



continuously acquires data from the PLC side, translates it into GEM-compliant messages, and forwards it to the host. Commands and recipe data can also flow in the reverse direction, from the host down to the PLC, depending on the equipment's automation requirements.

This layered approach means the PLC program itself requires little to no modification, the SECS/GEM host receives standards-compliant data regardless of the underlying PLC vendor, and the integration can be replicated across similar tools without re-engineering the approach each time.

Benefits of standardized equipment communication

Bridging PLC networks and SECS/GEM hosts through a proper translation layer delivers benefits that extend well beyond a single tool:

- Consistent MES connectivity across a mixed-vendor equipment fleet
- Faster equipment onboarding, since new tools can reuse the same integration approach
- Improved data quality for yield analysis, OEE tracking, and equipment health monitoring
- Reduced engineering overhead compared to custom, tool-specific integrations
- A practical path to modernize legacy equipment without replacing existing PLC control logic
- Better support for Industry 4.0 initiatives, since standardized data is

what makes higher-level analytics and automation possible in the first place

Real-world semiconductor applications

This kind of integration shows up across several areas of the fab:

- Material handling and conveyance sub-systems controlled by PLCs that need to report status to a central MES
- Facilities and utility equipment (chillers, pumps, gas delivery skids) where GEM-level visibility is increasingly expected
- Legacy process tools where the core equipment controller predates SECS/GEM support but still needs to participate in factory automation
- OSAT and back-end equipment, where a mix of PLC-controlled sub-systems must be unified under a single host communication scheme

Best practices for future-proof integration

Engineers planning this kind of integration project generally benefit from a few consistent practices:

- Map equipment states early. Define how each PLC status maps to GEM state models before implementation begins, not during it.
- Standardize alarm and event definitions across tools where possible, to keep host-side handling consistent.
- Choose a gateway approach that supports multiple PLC protocols,

since fab equipment mix rarely stays single-vendor for long.

- Validate against SEMI E5/E30 compliance, rather than building a custom, host-specific message format.
- Plan for scalability. An integration approach that works for one tool should be reusable across similar tools without a full re-engineering effort.

Manufacturers evaluating this kind of protocol gateway approach can look to solutions such as [elInnoSys EIGEMHMI](#) one example of how PLC-to-SECS/GEM connectivity has been implemented in practice, alongside other established equipment connectivity providers in the space.

Conclusion

As semiconductor fabs continue to push toward tighter MES integration and Industry 4.0 maturity, the gap between PLC-controlled sub-systems and SECS/GEM hosts is one that can't be ignored. Protocol translation, rather than custom point-to-point integration, offers a scalable and maintainable path forward — preserving existing PLC control logic while giving factory hosts the standardized, structured data they need. For fabs working through PLC to SECS/GEM integration, that translation layer is quickly becoming a foundational piece of factory automation infrastructure rather than an optional add-on.



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SEMI signals continued semiconductor investment as AI reshapes global industry

The semiconductor industry continues to experience strong investment momentum as artificial intelligence drives demand for manufacturing capacity, advanced technologies and skilled workers, while governments and industry organisations seek to strengthen regional semiconductor ecosystems.

THE LATEST ANNOUNCEMENTS from SEMI point to an industry being reshaped not only by AI-related chip demand, but also by the infrastructure required to manufacture those devices, the workforce needed to support expansion, and efforts to connect emerging semiconductor companies with established players.

At the European level, SEMI is calling for the proposed Chips Act 2.0 to provide a broader and more predictable framework for investment across the semiconductor value chain. In the US, a new Industry Advisory Committee has been established to help address the workforce requirements associated with expanding domestic microelectronics manufacturing. Meanwhile, SEMI's latest equipment data shows continued capital investment in semiconductor production, while a partnership with Silicon Catalyst aims to strengthen links between semiconductor startups and the established industry.

Together, the announcements illustrate the breadth of the semiconductor

industry's current expansion, extending from wafer production and manufacturing equipment to skills, policy and early-stage innovation.

Equipment investment continues to accelerate

One of the clearest indicators of current industry momentum comes from SEMI's Worldwide Semiconductor Equipment Market Statistics (WWSEMS) report.

Global semiconductor equipment billings reached **US\$40.53 billion in the second quarter of 2026**, representing a 23% increase compared with the same quarter in 2025 and an 11% increase from the first quarter of 2026. The result marked a second consecutive record quarter for global semiconductor equipment billings.

SEMI attributes the continued growth in equipment demand to investment in manufacturing capacity associated with AI, as semiconductor companies and their customers expand infrastructure to support rising demand for computing.

The geographical breadth of the growth is also significant. SEMI reported that investment was increasing across Asia, North America and Europe, highlighting the increasingly global nature of semiconductor capacity expansion.

The equipment figures provide an important indication of where semiconductor industry spending is being directed. While AI has become a major source of demand for advanced processors and memory, the resulting growth is also creating requirements further upstream in the manufacturing ecosystem.

New or expanded semiconductor fabs require a wide range of manufacturing equipment, process technologies and materials. As a result, the current AI investment cycle is translating into demand across a much broader portion of the semiconductor supply chain than chip designers and manufacturers alone.

The equipment market therefore provides one measure of how AI-related

demand is feeding through into physical manufacturing capacity.

Wafer demand follows AI expansion

The same underlying trend can be seen in SEMI's latest data on silicon wafer shipments.

Worldwide silicon wafer shipments increased by 7.4% year-on-year in the second quarter of 2026, reaching **3,573 million square inches (MSI)** compared with 3,327 MSI in the second quarter of 2025. Shipments also increased by 9.1% compared with the first quarter of 2026, when they stood at 3,275 MSI.

SEMI's Silicon Manufacturers Group said the growth was being driven by AI-related demand extending beyond advanced logic and memory into areas including power devices and photonics.

That broader demand profile is important because AI infrastructure increasingly encompasses more than the processors used to run AI models. Power management, networking, optical communications and other supporting technologies are becoming increasingly important as data-centre computing requirements grow.

At the same time, SEMI reported signs of recovery in industrial and automotive markets. However, memory pricing pressures were contributing to constrained demand in the PC and smartphone markets.

The combination of these trends suggests a semiconductor market in which different application segments are moving at different speeds. AI-related investment is providing a major source of growth, while some traditional electronics markets remain subject to more challenging conditions.

For wafer manufacturers, the overall direction nevertheless remains positive. Device manufacturers are continuing to invest in capacity expansion, with SEMI expecting silicon wafer demand growth to continue.

Europe looks to Chips Act 2.0

Against this backdrop of global capacity expansion, SEMI is also seeking changes to Europe's policy framework.

On 8 September, SEMI Europe renewed its call for European policymakers

to use the proposed **Chips Act 2.0** to strengthen semiconductor competitiveness and supply-chain resilience. Its latest position paper sets out nine policy recommendations covering the semiconductor ecosystem.

The organisation argues that European semiconductor competitiveness needs to be considered across the entire value chain, encompassing design, materials, equipment, manufacturing and advanced packaging.

SEMI says several elements of the European Commission's draft legislative text already reflect priorities raised by the organisation and its members, but believes the proposal provides an opportunity for further strengthening during the co-legislative process.

Among SEMI's recommendations is an expanded **First-Of-A-Kind framework** covering the complete semiconductor value chain. It is also calling for faster and more predictable investment and permitting procedures, greater industry participation in Chips Act governance and what it describes as an ambitious and balanced EU budget.

Other recommendations address Europe's production-cost disadvantage, demand-side initiatives, supply-chain monitoring and workforce development.

The emphasis on the whole value chain is significant. Semiconductor resilience is increasingly being considered in terms of access to equipment, materials, manufacturing processes, packaging capabilities and engineering expertise, rather than simply the number of semiconductor fabs located within a particular region.

For Europe, the policy challenge is therefore not solely about attracting wafer fabrication capacity. It also concerns whether the wider ecosystem can support investment and innovation at sufficient speed and scale.

Among SEMI's recommendations is an expanded First-Of-A-Kind framework covering the complete semiconductor value chain.

SEMI says it will continue working with European institutions, member states and industry stakeholders during the legislative process.

Workforce becomes a strategic constraint

Investment in fabs and equipment also creates another requirement: people with the technical expertise to design, operate and maintain increasingly sophisticated semiconductor manufacturing infrastructure.

In the US, the **National Network for Microelectronics Education (NNME)** has established its inaugural Industry Advisory Committee to help shape a national semiconductor workforce strategy.

The initiative is supported by the US National Science Foundation in partnership with the Department of Commerce, with the SEMI Foundation serving as the NNME's Hub Operator. The committee brings together representatives from semiconductor manufacturers, equipment and materials companies, universities, community colleges and workforce organisations.

The move comes as the US experiences substantial investment in domestic semiconductor manufacturing and corresponding demand for skilled workers.

According to a national workforce landscape analysis cited by SEMI, the US semiconductor industry could face a talent gap of approximately **127,000 to 157,000 workers by 2030**.

The composition of the advisory committee reflects the breadth of skills required. Its members include representatives from Micron Technology, the University of Illinois Urbana-Champaign, Qnity, Lam Research, Columbus State Community College, ASML, SEMI, GlobalFoundries, AMD, Rensselaer Polytechnic Institute, Samsung Semiconductor, Intel and Apple.

The committee will identify emerging workforce challenges, validate employer requirements, inform education and training strategies, strengthen connections across the semiconductor ecosystem and provide input into national workforce initiatives.

This approach reflects the increasingly specialised nature of semiconductor manufacturing. Expanding production capacity requires not only engineers and scientists, but also technicians, equipment specialists, process experts and other personnel able to support advanced manufacturing operations.

The NNME is intended to create a more coordinated national system linking employers, education providers, workforce organisations and regional partners, with the aim of developing industry-aligned talent pathways.

Connecting startups with the semiconductor ecosystem

While policy, manufacturing capacity and skills represent established elements of semiconductor competitiveness, another SEMI initiative is focused further upstream on innovation.

SEMI and semiconductor accelerator **Silicon Catalyst** have signed a strategic partnership intended to strengthen connections between semiconductor hardware startups, investors, manufacturers and technology companies.

The memorandum of understanding was signed at SEMICON Taiwan 2026. The partnership is designed to provide SEMI members with access to Silicon Catalyst's startup portfolio and innovation ecosystem, while giving Silicon Catalyst companies greater access to SEMI's global network of companies, investors, technology partners and industry resources.

The collaboration will initially involve activities in Taiwan, the Americas and Europe, with the intention of extending participation across SEMI's global network.

Startup-focused programmes will also be developed around SEMICON exhibitions, including Startup Zones, investor engagement programmes and technology showcases. The initiative will begin with the Silicon Startups Zone at SEMICON Taiwan and subsequently expand to other major SEMICON events.

The rationale is closely connected to the pace of technological development associated with AI. SEMI says semiconductor companies increasingly

require faster access to emerging technologies, new business models and new sources of innovation.

Silicon Catalyst brings a specialised focus on semiconductor hardware startups. Founded in 2015, the accelerator says it has engaged with more than 5,000 semiconductor startups worldwide, with more than 1,500 applications and over 150 portfolio companies admitted.

The partnership consequently provides a mechanism for connecting early-stage semiconductor technologies with the much larger manufacturing, investment and technology ecosystem represented by SEMI.

An industry being reshaped on multiple fronts

Taken together, the latest SEMI announcements illustrate how the semiconductor industry's current expansion extends well beyond the immediate increase in demand for AI processors.

Equipment billings are reaching record levels as manufacturers invest in additional capacity. Silicon wafer shipments are rising, with AI demand extending into power and photonics applications. European policymakers are being urged to strengthen the investment and regulatory environment across the semiconductor value chain. In the US, workforce organisations are attempting to address a potentially significant shortage of skilled personnel. At the same time, startup

initiatives are seeking to shorten the path between emerging semiconductor technologies and established industry players.

The common factor is the scale and breadth of investment required to support the next phase of semiconductor development.

AI is providing a major source of demand, but meeting that demand requires an ecosystem capable of supplying manufacturing equipment, wafers, materials, advanced packaging, power technologies, photonics, engineering expertise and new semiconductor architectures.

The latest SEMI figures indicate that investment in this ecosystem is already substantial. The policy and workforce initiatives highlighted by the organisation suggest that industry competitiveness will increasingly depend on whether regions can turn that investment into sustainable manufacturing and innovation capacity.

For semiconductor manufacturers and suppliers, the result is an industry environment in which capacity, technology, talent and access to emerging innovation are becoming increasingly interconnected. The next stage of semiconductor growth will therefore depend not simply on producing more chips, but on strengthening the wider infrastructure required to design, manufacture and commercialise them.





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Semiconductor inspection equipment set for 7.9% CAGR growth through 2034

According to the latest Semiconductor Inspection Equipment Market Research Report, the value of the global semiconductor inspection equipment market was calculated at USD 6.8 billion in 2025.

BY ASHISH KOLTE, MARKETING MANAGER AT DATAINTELO

THE ROBUST growth rate can be attributed to increased demand for advanced node logic devices along with quick implementation of AI in semiconductor inspection equipment.

It is forecasted that the global semiconductor inspection equipment market will experience a growth rate of 7.9% from 2026 to 2034 and will attain a market value of USD 13.4 billion by 2034. The high growth rate is attributed to the declining process nodes, AI-enabled defect classification, and adoption of advanced packaging techniques.

Why inspection equipment has become a critical component

Current chip production processes leave very little margin for error. With shrinking geometries below the 3nm node, a single defect could cause

significant damage to the yield rate of chips produced on that wafer. This is why the development of inspection and metrology equipment has transitioned from an auxiliary process control step to the most critical category of capital equipment in the fabrication facility.

Semiconductor inspection equipment includes the equipment used to inspect for defects, contamination, and pattern anomalies on wafers during their fabrication process – from the inspection of bare-wafer surfaces, patterned layer defects analysis, CMP endpoint detection, and wafer packaging inspection. With the shrinking defect budget of semiconductor manufacturers at the advanced process nodes, the use of this equipment has transitioned from the back-office to the core of the fab investment strategy.

Recent developments shaping the market

Several recent events show how rapidly this market is changing:

Advanced node transitions are driving new categories of defects.

The shift to gate-all-around (GAA) nanosheet transistors, now in commercial production at Samsung and ramping at TSMC, has introduced three-dimensional channel structures that traditional brightfield optical tools cannot fully characterize. This has accelerated demand for electron beam inspection systems capable of resolving sub-surface and buried-interface defects.

AI-powered inspection has gone mainstream.

Automated defect classification (ADC) systems, once limited to roughly 70–80% accuracy under rule-based logic,

are now achieving above 95% accuracy while cutting nuisance alarm rates significantly. Leading equipment makers have folded machine learning directly into their inspection platforms, and AI-enabled systems are commanding a notable price premium over legacy tools a trend that is lifting average selling prices across the market, not just unit volumes.

Advanced packaging is opening a new front-end-to-back-end demand channel.

Hybrid bonding, fan-out wafer-level packaging, and 2.5D/3D chip stacking require inspection of bond pads just 1–2 micrometers in pitch, pushing adoption of X-ray CT, scanning acoustic microscopy, and 3D optical profilometry tool categories that sit largely outside the traditional front-end inspection suite.

Government-backed fab construction continues to expand the installed base.

Acts like CHIPS and Science Act of USA, European Chips Act, and Japanese Semiconductor Incentives by METI are responsible for triggering a spate of new fab projects not only in the US, Germany, Japan, but worldwide. Every new fab is a new multimillion dollar contract for inspection and metrology equipment starting from litho verification to wafer sort.

Market outlook 2025–2034

In terms of region, Asia Pacific continues to be the main contributor to demand in the market accounting for nearly half of the total global market value in 2025 due to the presence of highly advanced foundries and memory fabs in Taiwan, South Korea, Japan, and China. North America stands second as a market segment followed by Europe, where its contribution is due to lithography and process control applications owing to fabs located in Germany and Ireland. The regions of Latin America and Middle East & Africa continue to contribute smaller shares but higher growth rates due to the development of electronics manufacturing ecosystems.

Optical inspection technology holds the dominant position in the market owing to its high throughput capacity and cost-effectiveness in various process layers, yet electron beam inspection is expected to be the fastest growing technology segment through 2034 due to the emergence of defects, which can only be detected by e-beam resolution owing to EUV lithography and multi-patterning. On the application side, defect detection remains the largest use case, while metrology covering critical dimension measurement, overlay, and film thickness is growing at a faster clip as

3D device structures demand more volumetric characterization. Looking at technology dimensionality specifically, 3D inspection is the standout growth category, expanding roughly 3 percentage points faster annually than 2D methods as NAND stacks exceed 300 layers and advanced packaging interfaces require full volumetric inspection.

Industry context: A capital equipment cycle unlike prior ones

To understand why inspection equipment specifically is outgrowing the broader chip market, it helps to look at what is happening one level up, in overall wafer fab equipment (WFE) spending. Industry association SEMI has repeatedly revised its equipment spending forecasts upward through 2026, now projecting worldwide 300mm fab equipment spending to rise 18% to roughly \$133 billion in 2026 and a further 14% to about \$151 billion in 2027 — the first time the industry has crossed the \$150 billion mark. SEMI has attributed this to AI-driven data center and edge compute demand resetting the scale of semiconductor manufacturing investment, alongside continued national self-sufficiency programs.

That broader capex surge matters for inspection equipment specifically



because process-control tools are consuming a rising share of every dollar spent on new fab capacity, not a fixed one. KLA Corporation, the market's dominant vendor, closed fiscal 2026 (ended June 30, 2026) with \$13.58 billion in total revenue and told investors that its Advanced Packaging process control systems revenue is now expected to grow to approximately \$1.1 billion in calendar 2026, up more than 70% year-over-year nearly twice the growth rate of the advanced packaging market itself.

On the company's fiscal Q4 2026 earnings call, CEO Rick Wallace pointed to accelerating investment tied to AI infrastructure, continued strength in leading-edge foundry logic, and increasing process control intensity across memory and advanced packaging as the drivers behind the quarter's record revenue. That single data point inspection revenue growing roughly twice as fast as the underlying packaging market it serves is a useful proxy for the "rising content per wafer" dynamic that underpins the 7.9% CAGR forecast for the broader inspection equipment category.

Regulatory developments senior decision-makers should track

Export policy has become as important to this market's near-term trajectory as technology roadmaps. Three developments stand out: **VEU status expiration reshapes China-based fab operations.** VEU authorization for the three firms, which allowed TSMC, Samsung, and SK Hynix to purchase U.S.-controlled

semiconductor manufacturing tools and ship them to their Chinese facilities on an individual basis instead of having to receive shipment-by-shipment authorization, expired on December 31, 2025. On January 1, 2026, all three firms have been required to apply individually for their own annual export licenses from the Bureau of Industry and Security (BIS). All three received approval for the current cycle, but the shift from a standing exemption to an annually renewable license gives Washington a lever it can adjust every year — a meaningful planning variable for any inspection equipment OEM serving these accounts.

Congress has been advocating for stronger measures than those adopted by the executive branch.

In February 2026, a bipartisan congressional delegation formally requested the Departments of Commerce and State to switch from the current case-by-case policy concerning the export of semiconductor manufacturing equipment to China to a blanket ban since, once in the country, the controls regarding end use are practically impossible to enforce. Furthermore, in January 2026, the Foreign Affairs Committee of the House of Representatives introduced a bill that would give Congress a veto right over AI chip export licenses which now rest with the Department of Commerce. Both bills have yet to pass but indicate that the regulation concerning the export of inspection equipment that can be used in sub-14nm manufacturing is ambiguous.

China's capital spending is proving more resilient to controls than the equipment mix. SEMI data shows China is expected to retain the largest single-country share of global 300mm fab equipment spending even as growth moderates, with 2026 outlays estimated around \$39 billion sustained largely by mature-node capacity expansion under central government support, even as the most advanced inspection and lithography tools remain restricted. For OEMs, this bifurcates the China opportunity: robust volume demand for inspection tools qualified for mature nodes (14nm–28nm and above), alongside a structurally capped ceiling on sales of leading-edge e-beam and EUV-related inspection systems.

Adoption trends worth watching

Beyond the headline CAGR, a few adoption patterns are shaping how and where inspection budgets are being spent:

- **Process control intensity is rising faster than wafer starts.** Rather than inspection equipment demand tracking unit volume growth in chip production, fabs are adding more inspection and metrology steps per wafer at each successive node — a trend KLA and other vendors have specifically called out as a distinct growth driver from unit volume.
- **Advanced packaging inspection is shifting budget outside the traditional front-end.** With KLA's advanced packaging process control revenue growing roughly 70% year-over-year against overall company growth in the high teens, back-end and mid-end-of-line inspection categories (X-ray CT, scanning acoustic microscopy, 3D optical profilometry) are becoming a distinct budget line for OEMs and fab operators rather than an adjunct to front-end tool sets.
- **AI-native purchasing decisions.** Machine learning has been heavily integrated into inspection processes, leading fab facilities to focus just as much on the accuracy of the classification process and reducing false positives as on the resolution of optical and electron beam systems.
- **License-cycle risk is entering vendor account planning.** With annual re-licensing now required for equipment shipments into major Chinese-operated fabs, OEMs





serving these accounts are having to build regulatory renewal risk directly into revenue forecasting and inventory planning in a way that wasn't necessary under the prior VEU framework.

Key growth factors

- Shrinking process geometries:**
 Sub-3nm and emerging angstrom-era nodes are tightening defect budgets to the point where inspection intensity per wafer is rising sharply, particularly at leading foundries running well over 100 in-line inspection and metrology steps per advanced logic wafer.
- AI and automation:**
 Machine learning-driven defect classification and "virtual inspection" techniques are improving detection accuracy while helping fabs prioritize which wafers need physical inspection, adding both efficiency and revenue-per-tool gains.
- Heterogeneous integration:**
 The move away from monolithic scaling toward chiplets, interposers, and hybrid bonding is creating an entirely new demand pool for back-end and mid-end-of-line inspection tools, evidenced by the outsized growth rates vendors are now reporting in this category specifically.
- Fab build-out due to policy:**
 Both the reshoring efforts and the diversification geopolitically for semiconductor production capacity are keeping up a multi-year pipeline of fab construction, each of which demands an entire set of process

control tools — a pipeline SEMI now forecasts will help drive annual 300mm equipment spend beyond \$150B beginning in 2027.

○ Increase in chips for autos and AI:

Electric cars and AI accelerators require very tight defect levels, which increases the need for inspection capability in logic, memory, and power semiconductors.

Challenges on the horizon

The market's growth is not without friction. Export control policy is now an active, moving variable rather than a settled backdrop: the end of VEU status for Chinese fab operations, congressional pressure for a blanket SME export ban, and BIS's annual license-renewal cycle all introduce a layer of regulatory uncertainty that inspection equipment OEMs did not have to underwrite as heavily even two years ago.

The industry is still vulnerable to the cyclical nature of semiconductor capital spending that has been evident for years, with capital spending in memory especially susceptible to volatile swings dependent on pricing trends for DRAM and NAND. And the expense and engineering complexity of advanced-generation inspection equipment, particularly EUV mask inspection equipment, continues to increase the barriers to entry, with competitive advantage held by few suppliers and with smaller fabs and OSATs relying on financing or

service-based business models to gain access to state-of-the-art technology.

Key insights for decision-makers

Collectively, the data suggests that the industry is no longer growing just because there are more chips being made — it is growing because each succeeding generation of chips is requiring more inspection and metrology content than the previous one. For fab operators, this argues for treating process control capacity planning as a multi-year commitment tied to node roadmaps and packaging strategy, not a line item that scales linearly with wafer starts. For equipment OEMs and their investors, the advanced packaging and 3D inspection categories currently offer the clearest evidence of demand outpacing the broader market, while exposure to Chinese fab customers now carries a regulatory renewal risk that warrants explicit scenario planning. And for policymakers and industry observers, the inspection equipment market has become a useful, fast-moving barometer of how national semiconductor strategies, export policy, and the AI infrastructure buildout are intersecting in real time. Precision has stopped being just a manufacturing requirement it has become a genuine point of competitive and strategic differentiation heading into the next decade.

Read a full report: <https://dataintel.com/report/semiconductor-inspection-equipment-market>

AI infrastructure boom shifts from chip race to supply-chain race

AI infrastructure spending has entered a new phase, with demand outpacing semiconductors, memory and power capacity despite record earnings across the technology ecosystem. This earnings season reveals that capital investment, geopolitics and supply-chain resilience, not compute demand alone, are increasingly determining the pace of AI deployment, reshaping competitive dynamics across the global semiconductor value chain, according to GlobalData.

AN ANALYSIS of GlobalData's Company Reports Database reveals that SK Hynix's net income jumped 397.5% year-on-year, Samsung's 486.7% — both riding an HBM shortage that has sold out DRAM through 2026. Micron posted a staggering 1,398.3% net income surge on 345.7% revenue growth, confirming that AI accelerators are as memory-hungry as they are compute-hungry, with supply still lagging.

NVIDIA's net income more than tripled (up 210.6%) on data-center demand, though operating cash flow growth of 83.6% trailed capex growth — down 70.9% QoQ but up 43.2%

YoY — showing how much cash is being redirected into supply-chain commitments, including securing extra TSMC capacity for H200 production.

Murthy Grandhi, Company Profiles Analyst at GlobalData, comments: "TSMC's 77.4% net income growth against a 33.8% YoY capex rise reflects its race to add advanced-node capacity, which is running short of AI demand. Constellation Energy's 1,247.5% net income growth underscores that power, not chips, is now the binding constraint — a point hyperscalers have made explicitly on recent earning calls."

Two outliers break from the boom. Intel's net loss narrowed 278.1% YoY on a genuine turnaround: its 18A node hit high-volume manufacturing in January 2026 with yields improving about 7% monthly, its 9.9% CHIPS Act equity stake has appreciated on paper, and NVIDIA, Microsoft, Amazon and Apple have all opened foundry talks — though Intel does not expect meaningful foundry revenue before 2027. Marvell's net income fell 80.6% YoY despite 27.6% revenue growth, showing custom-silicon suppliers can see margins squeezed by ramp costs even amid strong AI demand.

Company Name	HQ	Latest Quarter Revenue (\$B)	QoQ %	YoY %	Net Income (\$B)	QoQ %	YoY %	Cap Ex (\$B)	QoQ %	YoY %	CFO (\$B)	QoQ %	YoY %
Alphabet	United States	119.8	9.0%	24.2%	112.2	79.3%	297.9%	-80.6	125.9%	103.3%	84.9	85.3%	32.8%
Apple	United States	109.4	-1.6%	16.4%	29.8	0.7%	27.1%	-6.8	56.5%	-28.2%	117.0	41.6%	43.1%
Samsung Electronics	South Korea	94.2	42.7%	69.2%	33.1	144.1%	486.7%	-12.8	-65.1%	35.8%	29.8	-50.8%	145.9%
Microsoft	United States	90.0	8.6%	17.7%	35.8	12.5%	31.3%	-115.9	44.7%	79.6%	182.9	43.5%	34.4%
NVIDIA	United States	81.6	19.8%	85.2%	58.3	35.8%	210.6%	-1.8	-70.9%	43.2%	50.3	-51.0%	83.6%
Meta Platforms	United States	60.8	8.0%	28.0%	15.8	-40.8%	-13.6%	-49.1	158.5%	66.6%	64.1	98.9%	29.2%
Micron Technology	United States	41.5	73.7%	345.7%	28.2	104.9%	1398.3%	-19.6	66.5%	92.2%	45.7	125.0%	287.5%
TSMC	Taiwan	40.8	9.2%	36.0%	22.7	17.5%	77.4%	-27.2	140.8%	33.8%	47.6	112.1%	32.0%
SK Hynix	South Korea	37.0	60.2%	198.1%	28.4	165.0%	397.5%	-5.5	-72.5%	21.9%	18.5	-50.7%	191.8%
Broadcom	United States	22.2	14.9%	47.9%	9.3	26.7%	87.5%	-0.5	92.4%	97.1%	18.8	127.0%	48.0%
Intel	United States	16.1	18.8%	25.4%	-11.0	195.9%	278.1%	-6.2	70.3%	-29.1%	8.1	639.2%	183.0%
Constellation Energy	United States	11.1	83.1%	63.8%	1.6	268.1%	1247.5%	-1.3	56.8%	58.2%	0.4	-90.0%	297.2%
Vertiv Holdings	United States	3.3	23.6%	24.1%	0.5	27.6%	53.5%	-0.3	153.1%	240.6%	1.9	143.4%	198.1%
Marvell Technology	United States	2.4	9.0%	27.6%	0.0	-91.3%	-80.6%	-0.2	56.4%	30.3%	0.6	-63.5%	91.9%

➤ 14 Chip and AI bellwether Companies Source: GlobalData IntelligenceCenter and Annual Reports

Hyperscalers' capex is the real story. Microsoft, Alphabet and Meta each posted capex growth above 65% YoY, matching public guidance: Alphabet has raised 2026 spending to \$175–190 billion, Meta to \$125–145 billion, Microsoft toward \$120–190 billion. Combined, the four hyperscalers are on pace for roughly \$700–\$725 billion in 2026 capex — up about 77% from 2025, the largest peacetime capital cycle in corporate history, funded even as free cash flow tightens.

Grandhi adds: "Geopolitics is now embedded in these numbers. In January 2026, the Trump administration invoked Section 232 to impose a 25% tariff on select advanced AI chips, with a two-phase plan that could raise rates further while rewarding domestic production. Separately, the Bureau of Industry and Security shifted H200 and MI325X export reviews for China from presumptive denial to case-by-case approval, capped near 50% of prior US sales — a partial reopening that still left buyers like ByteDance, Alibaba and

Tencent able to secure only a fraction of the over two million H200s they'd ordered. TSMC, Samsung and SK Hynix lost blanket Validated End-User exemptions on 1 January 2026 and now need annual US licenses to ship equipment into their China fabs."

Layered atop this is Pax Silica, the US-led pact signed by two dozen nations in December 2025 to lock allied countries — including India, Japan, South Korea and the Philippines — into a trusted semiconductor and critical-minerals chain outside China's orbit.

India is a direct beneficiary. Micron's Sanand, Gujarat assembly-and-test plant, inaugurated February 2026, is now packaging DRAM and NAND for Micron's global supply chain — an India-origin option arriving just as DRAM prices rose roughly 90% in Q1 2026. The Tata Electronics-PSMC wafer fab at Dholera has passed the halfway mark, targeting trial production by December 2026 at the 28nm node — mature by global standards, but enough to cut

"The risk isn't slowing AI demand, but power, memory and licensing constraints capping deployment speed."

India's reliance on imported logic and power chips.

Grandhi concludes: "GlobalData sees none of this capex as optional now: HBM and advanced-node capacity are sold out, tariffs and export licensing are permanent cost variables, and Pax Silica signals self-reliance blocs — not free trade — will govern chip supply chains for the rest of the decade. The risk isn't slowing AI demand, but power, memory and licensing constraints capping deployment speed."

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Transforming technology into reliable industrial solutions



Sérgio Tavares COO at HFA, discusses the company's mission to be a leading technology partner in the industrialization and production of electronics in Europe.

SIS: Can you give us an overview of HFA's mission and core activities within the semiconductor industry, particularly in the context of Europe's evolving ecosystem?

ST: We are an electronics manufacturing services (EMS) company with strong expertise in: high-density and complex SMT; THT; electromechanical integration; functional testing; coating; kitting, etc. We also have a dedicated line for the assembly of precision electronics.

In a European context where strategic autonomy is widely discussed, HFA positions itself as a very important ally between design and the market.

Our focus is not just on manufacturing - it's on ensuring reliability, flexibility,

and close technical proximity to the customer.

SIS: How does HFA position itself strategically within Europe's semiconductor landscape, and what competitive advantages does it bring compared to other European and global players?

ST: Europe is strengthening its capacity in chip design and manufacturing. The value chain doesn't end with the wafer - it ends with the functional product in the field.

HFA positions itself at the end of this chain, providing chip packaging services in HMLV (High Mix Low Volume), just like its other EMS services.

SIS: Europe has recently rolled out significant semiconductor initiatives

and funding programs. How has HFA engaged with these European initiatives, and what impact have they had on your development plans?

ST: HFA currently has a strong presence in the microelectronics agenda, with a very significant investment planned and approved under co-financing programs for this segment. We strongly believe that these incentives will help companies position themselves competitively in the market. HFA aims to be one of the leading European players in HMLV (High Mix Low Volume) chip packaging.

SIS: Supply chain resilience has become a major focus across the semiconductor sector. How has HFA navigated supply chain challenges, and what steps are you taking to strengthen European supply chain independence?





ST: HFA is also facing supply chain challenges. However, as a result of the transformations of recent years, we are now much more focused on having:

- Early demand visibility;
- Risk assessment by component;

What we do:

- Collaborative planning with clients;
- We have a highly capable DFM team that can propose alternative components to our clients;
- Diversification and qualification of suppliers;
- Strategic stock reinforcement in critical components; We believe that resilience here is more linked to the ability to produce reliable information and the capacity for adaptation than to the ability to maintain large stocks.

SIS: Sustainability and energy efficiency are key trends in semiconductor manufacturing. How is HFA addressing environmental concerns within its products and operations?

ST: Sustainability is a part of our day to day to reduce our footprint in every single board we produce:

- Energy optimization of SMT and THT lines, which are the largest energy consumers in our industry;
- Use of more environmentally friendly products, e.g., soldering alloys, fluxes, cleaning products, etc.;
- We seek partnerships with certified suppliers;
- Reduction of waste of raw materials and consumables;
- Monitoring of industrial consumption;
- Installation of energy management equipment that switches

between the grid, batteries, and the instantaneous production of our solar panel park;

- Reducers and timing of water consumption terminals;
- Installation of a reservoir for rainwater accumulation;
- Low-consumption lighting systems;

SIS: Talent and skills shortages are often cited as barriers for Europe's semiconductor ambitions. What is HFA doing to attract and retain technical talent, and how do you see the broader skills ecosystem evolving?

ST: At HFA, we have been making a strong investment in the continuous training of our employees, as well as for new employees with a very robust onboarding program with extensive initial training.

- Continuous internal training;
- Proximity to schools and universities;
- Clear and well-defined career progression plan;
- Development of technical career paths that are as valued as management career paths;
- In the case of semiconductors, we have a small laboratory equipped with an ISO 6 clean room for skills development in the field of microelectronics.

SIS: Collaboration seems vital for Europe's semiconductor ambitions. Can you share examples of partnerships - industrial, academic, or governmental - that have been particularly impactful for HFA?

ST: We have an internship and trainee program aligned with several universities that has proven to be fundamental. We also have companies within the HFA Group that are linked to semiconductors, with whom we work very closely to develop joint solutions in order to bring solutions to market in the European context.

SIS: Looking ahead, what are HFA's priorities for growth within the European semiconductor sector over the next 3 to 5 years, and what role do you see the company playing in shaping Europe's semiconductor future?

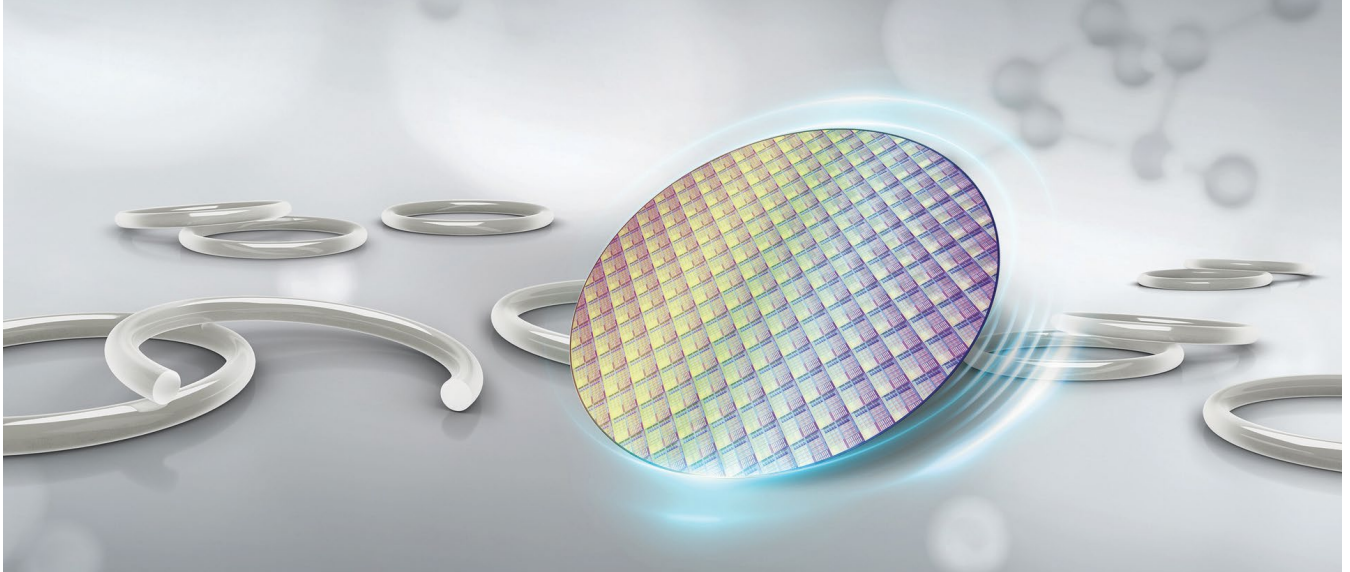
Our priorities are clear:

- Strengthening our technological capacity;
- Industrial automation and digitalization;
- Growing our footprint in strategic European sectors (energy, defense, mobility, industry...)

We want to position HFA as:

- A leading industrialization partner for both EMS services and semiconductors.
- A resilient and technologically advanced company;
- An active contributor to European industrial autonomy;

The European future of semiconductors depends not only on manufacturing chips — it depends on transforming technology into reliable industrial solutions. And that's where HFA wants to be.



Redefining semiconductor sealing: The shift toward fluorosurfactant-free materials

The demand for advanced technologies like AI, 5G networks and high-performance computing is pushing the limits of semiconductor manufacturing. As chip designs continue toward miniaturization, the margins for error shrink to near zero. In this environment, even the most microscopic contamination can negatively affect yield rates and inflate the total cost of ownership.

BY KEVIN KAUFENBERG, BUSINESS DEVELOPMENT SPECIALIST, SEMICONDUCTOR, TRELLEBORG SEALING SOLUTIONS

WHILE MANUFACTURERS invest in advanced lithography and deposition equipment, they often overlook one of the most critical components safeguarding the process: the polymer seals. Traditional sealing materials struggle to keep pace with the extreme temperatures, aggressive chemistries and strict purity requirements of modern fabrication facilities. Furthermore, a shifting regulatory landscape is forcing the industry to reevaluate the chemical makeup of these essential components. Semiconductor manufacturers therefore need to embrace the next-generation of sealing materials that ensure performance without compromising environmental responsibility.

The hidden vulnerabilities in semiconductor manufacturing

Semiconductor fabrication environments are notoriously hostile. Processes such as plasma-enhanced

chemical vapor deposition (PECVD), atomic layer deposition (ALD) and dry etching subject equipment to intense plasma fields, corrosive gases and continuous thermal cycling. Under these extreme conditions, standard elastomeric seals can degrade rapidly.

When seals break down, they release trace metals and generate particulate matter. This outgassing and particle emission directly contaminates the wafer environment. In advanced nodes where features are measured in nanometers, a single particle can ruin an entire chip. The result is unplanned downtime, frequent maintenance intervals and a catastrophic impact on production yield. For semiconductor manufacturers facing the pressures of high-yield demands, minimizing these contamination incidents is not only a technical goal but critical to the bottom line.

Beyond the physical degradation of materials, the industry faces a looming regulatory challenge. Many high-performance fluoroelastomers (FKMs) and perfluoroelastomers (FFKMs) rely on fluorosurfactants during the polymerization process. While effective for manufacturing these complex polymers, fluorosurfactants are facing increasing global scrutiny due to their environmental persistence. Chipmakers are now caught in a difficult position: they must reduce their environmental footprint and regulatory risk without sacrificing the performance required by advanced node manufacturing.

Innovation through fluorosurfactant-free elastomers

The solution may lie in advanced material science. Forward-thinking suppliers recognize that the industry cannot choose between process reliability and

environmental compliance. By eliminating fluorosurfactants from the manufacturing process, polymer engineers have developed a new class of sealing materials that meet both demands simultaneously.

These next-generation materials, such as the PureFab® fluorosurfactant-free elastomers developed by Trelleborg Sealing Solutions, set a new standard for purity and stability. They provide an environmentally responsible alternative that improves upon the performance of traditional compounds.

To assess the impact of these materials, it is necessary to examine their performance across three critical dimensions:

- Plasma resistance and extreme purity**

In plasma-heavy processes, seal erosion is a constant threat. New unfilled FFKM formulations, such as Isolast® PureFab® JPF50, are engineered without organic or inorganic fillers. This structural purity translates to plasma resistance against a wide range of aggressive chemistries and common thin-film precursors. By exhibiting ultra-low outgassing and minimized particle generation, these high-purity seals significantly reduce contamination risks and help maximize process yields.

- Unyielding temperature stability**

Thermal degradation is a primary cause of seal failure in processes like rapid thermal processing (RTP) and diffusion furnaces. Standard elastomers lose their elastic recovery and mechanical strength when exposed to continuous high-heat cycles. Advanced high-temperature FFKMs can now perform at continuous service temperatures up to +572 °F/ +300 °C. Materials engineered for these environments maintain dimensional stability under continuous high loads, resisting the cracking and brittleness that plague lesser polymers. This temperature stability ensures long-term seal integrity, extending the life of critical equipment.

- Cost-efficient chemical resistance**

Not every application within a fabrication facility requires the extreme performance, or carries the premium cost, of an FFKM. For transfer modules, load locks and general vacuum handling systems,

advanced FKM materials like Trelleborg's PureFab® VPF 20 offer a highly effective bridge. Formulations utilizing a non-fluorosurfactant base polymer combined with a high-purity synthetic filler system deliver robust mechanical strength and excellent chemical compatibility. They provide a cost-efficient alternative that still upholds the stringent cleanliness requirements of contamination-sensitive environments.

Accelerating time-to-market and reducing total cost of ownership

The transition to fluorosurfactant-free materials is about much more than regulatory compliance. It is a strategic move that directly impacts a manufacturer's bottom line. When seals resist plasma erosion, withstand extreme temperatures and maintain their integrity against harsh chemicals, the entire manufacturing process becomes more stable.

Equipment front-end modules (EFEM), chamber lids and gas delivery systems can operate for longer periods between scheduled maintenance. This increased process uptime is a critical success indicator for any fabrication facility. By reducing the frequency of seal replacement, manufacturers lower their direct maintenance costs and eliminate most costs associated with offline tools.

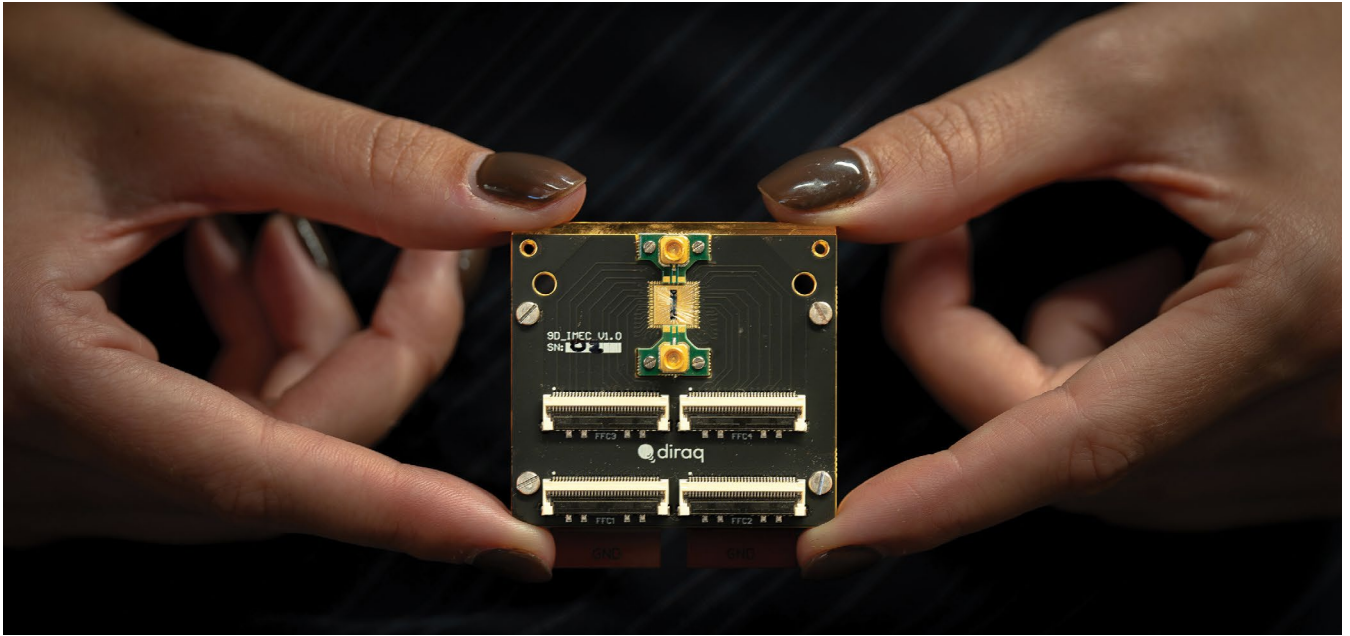
The exceptional purity of these advanced materials ensures that trace metal content and ionic extractables remain virtually nonexistent. This meticulous contamination control, often supported by production in ISO 5 cleanroom environments, directly translates to higher wafer yields. By improving yield rates and extending equipment life, these innovative sealing solutions drastically reduce the total cost of ownership.

Partnering for process excellence

The challenges of modern chip design should not be solved in isolation. As the industry pushes toward smaller nodes and more complex architectures, the physical demands on manufacturing equipment will only intensify. Manufacturers need more than component suppliers; they require engineering partners like Trelleborg that understand the intricate balance of material science, process chemistry and regulatory foresight.

To maximize yield and accelerate time-to-market, chipmakers must evaluate every aspect of their process architecture. Advanced material solutions that eliminate fluorosurfactants while enhancing thermal and chemical resistance represent a vital step forward.





From 2D transistors to quantum processors: imec pushes semiconductor integration beyond conventional scaling

The semiconductor industry's search for continued performance gains is increasingly extending beyond conventional transistor scaling. As artificial intelligence drives demand for greater compute density, memory capacity and bandwidth, while wireless systems move towards mmWave and sub-THz frequencies, semiconductor researchers are exploring new materials, architectures and integration techniques to extend what can be achieved within established manufacturing frameworks.

BY IMEC

A SERIES of recent developments from imec illustrates the breadth of this transition. The Belgian research and innovation centre has reported advances in heterogeneous integration of III-V chipllets on silicon, a new narrowband receiver architecture for ultra-wideband (UWB) systems, ferroelectric memory devices, 2D-material transistors, backside interconnects for three-dimensional integration and silicon-based quantum processors.

Although these technologies address very different applications, they share a common objective: finding ways to extract more functionality and performance from semiconductor

systems without relying solely on conventional planar scaling.

The approaches range from integrating III-V materials with silicon CMOS and stacking devices vertically, to introducing atomically thin transition-metal dichalcogenides (TMDs), ferroelectric materials and silicon spin qubits into manufacturing flows increasingly based on 300mm semiconductor processing.

For the semiconductor industry, the significance lies not simply in the individual device demonstrations, but in the effort to make emerging technologies compatible with the infrastructure, design methodologies

and process discipline of mainstream semiconductor manufacturing.

Heterogeneous integration moves towards system-level RF platforms

One of the clearest examples is imec's development of a 300mm RF silicon interposer platform designed to integrate III-V chipllets with Si-CMOS.

The platform is being developed for applications including mmWave and sub-THz wireless systems and high-speed data-centre applications. It combines three developments: high-density embedded capacitors, a modelling framework for RF passive components and laser-assisted bonding

for assembling III-V chiplets onto the interposer.

The underlying challenge is increasingly familiar. As wireless systems move to higher frequencies and electronic and photonic interfaces in data centres approach their performance limits, achieving high-performance signal handling can result in greater system complexity, power consumption, cost and physical footprint.

III-V materials such as indium phosphide (InP), gallium arsenide (GaAs) and gallium nitride (GaN) offer properties that are attractive for high-frequency and high-performance applications, while silicon CMOS provides the manufacturing scalability and cost advantages associated with the established silicon industry.

Rather than attempting to build every function in one semiconductor technology, heterogeneous integration allows different materials to be used where their properties are most advantageous. In this architecture, performance-critical functions can remain in compact III-V chiplets, while the silicon interposer provides low-loss interconnections and accommodates passive components.

The development builds on previous imec work. In 2024, the organisation demonstrated InP chiplet integration on a 300mm RF silicon interposer with negligible insertion loss at 140GHz. In 2025, the platform was extended to demonstrate record-low insertion loss up to 325GHz.

The latest work addresses some of the practical requirements for moving such an approach towards a more complete system platform.

Moving passives away from the chiplet

A significant element is the development of a new metal-insulator-metal capacitor, or MIMCAP, architecture.

Passive components can occupy a significant proportion of a chiplet's area. Moving functions such as decoupling capacitors from the III-V chiplet to the interposer can therefore allow the active chiplet to become smaller while simultaneously making better use of the interposer's available area.

According to imec, the new architecture produces a 10-to-100-fold increase in capacitance density compared with typical on-chip capacitors in III-V technologies.

The MIMCAP uses a high-k aluminium-hafnium-oxide dielectric combined with three-dimensional oxide-stud structures in the back-end-of-line.

The importance of the development is therefore architectural as much as device-specific. By treating the interposer as more than a passive routing layer, designers can distribute functionality across the package or system, placing each component where its characteristics are most useful.

That approach is increasingly relevant as semiconductor systems become more heterogeneous. Rather than treating the die as the sole location for functionality, advanced packaging allows the system architecture to incorporate different process technologies, materials and passive components.

Modelling becomes part of the integration challenge

Another component of the RF platform is a modelling framework for interposer passives.

At frequencies approaching the sub-THz range, small physical variations can have a significant impact on electrical performance. Designers therefore need models capable of predicting how passive components behave as their geometry changes.

Imec's framework has been validated to approximately 300GHz and is designed to predict circuit performance without requiring every geometrical variation to be separately simulated or physically measured. The stated objective is to reduce development time while improving predictability.

The current framework focuses on transmission lines but is being extended towards inductors and MIM capacitors.

This illustrates an important characteristic of heterogeneous integration: the challenge is not simply manufacturing the individual components. It is creating a sufficiently accurate design environment in which their interactions can be predicted before fabrication.

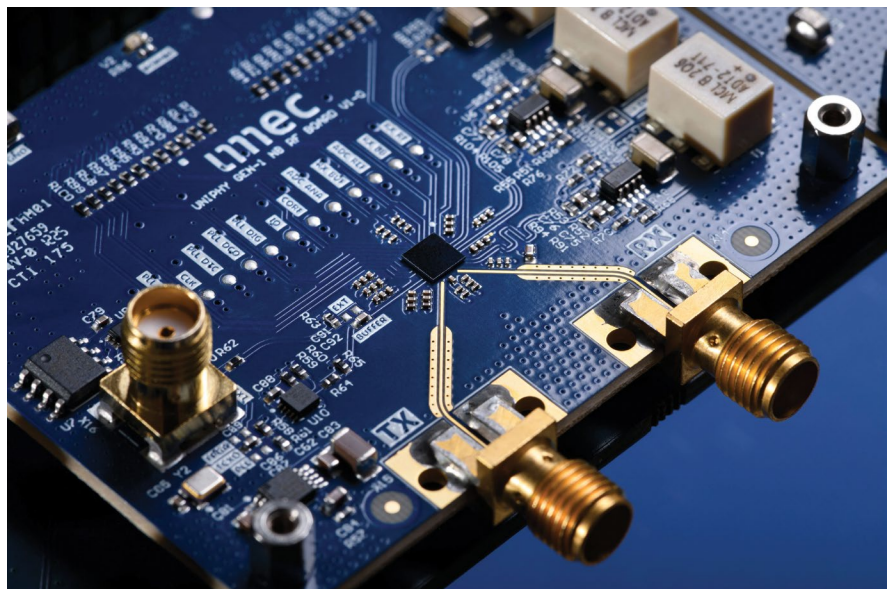
Laser bonding addresses thermal constraints

The third element is assembly.

III-V chiplets may need to be integrated onto interposers that already contain temperature-sensitive materials and structures. Conventional bonding processes can impose thermal budgets that complicate this integration.

Imec has therefore demonstrated laser-assisted bonding for assembling III-V chiplets on a passives-rich RF interposer. The approach is intended to avoid damaging temperature-sensitive layers while maintaining the required alignment accuracy.

The reported alignment accuracy was below 600nm, with rotational



misalignment below 0.05 degrees across 43 devices. RF measurements after assembly showed reflection below -15dB over the 110-170GHz range.

Together, the developments point towards a more complete manufacturing platform rather than a single component demonstration, with imec identifying low-volume manufacturing as a next stage in its technology development.

UWB moves towards longer-range positioning

A second imec development focuses on ultra-wideband wireless communication, where the challenge is not transistor scaling but maintaining reliable, precise positioning in increasingly crowded wireless environments.

Imec has developed a narrowband receiver compliant with the narrowband assistance mechanism defined in the forthcoming IEEE 802.15.4ab UWB standard. The implementation is reported to enable a fourfold increase in ranging distance, while a complete transceiver architecture combining receiver, transmitter and standard innovations has demonstrated up

to a 32-fold improvement in ranging performance.

UWB is already being deployed in smartphones, wearables, automotive systems and IoT devices, but range, scalability and resistance to interference remain challenges, particularly in dense wireless environments.

The IEEE 802.15.4ab approach introduces narrowband assistance, using signalling in the 5-6GHz range alongside UWB for discovery, synchronisation and coordination. The narrowband link can allow systems to operate at lower signal levels while supporting greater range and multi-user scalability.

This creates a demanding receiver design problem. The receiver needs a sufficiently low noise figure to detect weak signals, while also tolerating strong Wi-Fi signals operating in nearby or overlapping frequency bands.

Imec's solution uses a second-order transimpedance amplifier with controlled filtering, implemented in a 22nm CMOS process. The architecture suppresses strong out-of-band interference

early in the signal chain

while maintaining sensitivity to the desired signal.

An adaptive clip detector adds another layer of control. When strong interference is detected, the receiver can switch to a more robust operating mode

with additional filtering and gain control. Under lower-interference conditions, it can remain in a lower-power mode.

The reported receiver consumes less than 6mW, achieves a 9dB improvement in dynamic range over state-of-the-art implementations, has a 3.2dB noise figure and tolerates Wi-Fi blockers around -32dBm.

Potential applications include robot-to-robot coordination and AR glasses that need to understand and interact with their physical surroundings. The work is therefore relevant not only to conventional wireless connectivity but also to emerging systems in which precise spatial awareness is part of the computing architecture.

Ferroelectric devices target AI-era memory requirements

Memory is another area where conventional scaling is encountering increasingly difficult constraints.

AI workloads are creating demand for substantially greater memory capacity, bandwidth and energy efficiency. At the same time, technologies such as DRAM and SRAM are becoming more difficult to scale using established approaches.

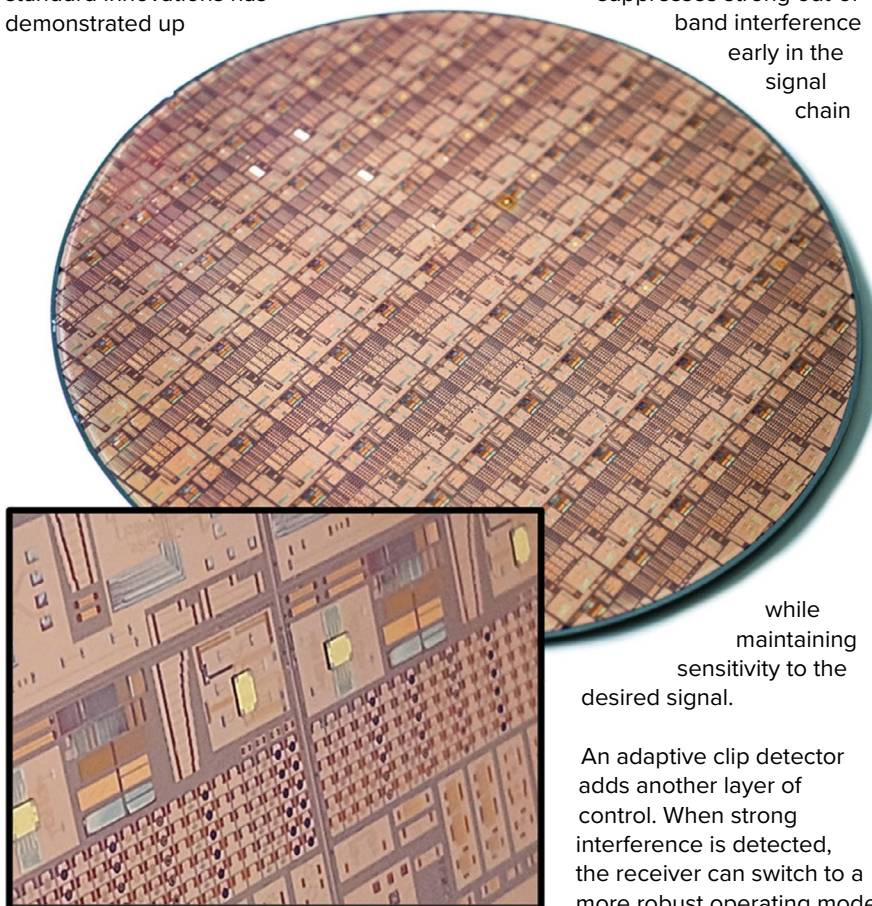
Imec is consequently investigating ferroelectric materials as a route towards low-voltage and high-density memory.

Recent results cover two complementary device concepts: ferroelectric capacitors and vertically stacked ferroelectric field-effect transistors (FeFETs). The former could support future DRAM-like memory concepts, while the latter could enable compact three-dimensional memory architectures.

The capacitor work demonstrates operation at approximately 1.3V while maintaining remnant polarisation above $40\mu\text{C}/\text{cm}^2$ and endurance of at least 10^{13} cycles.

Separately, imec has demonstrated vertically stacked IGZO-based FeFETs, including a five-word-line stack fabricated on 300mm wafers. A dual-gate architecture is used to improve erase efficiency.

The significance of the vertical architecture is straightforward:



increasing memory density does not necessarily have to depend on making every individual device smaller. Devices can also be stacked.

This is increasingly important as three-dimensional integration becomes a recurring theme across logic, memory and advanced packaging. Ferroelectric devices offer another route towards exploiting vertical space while potentially reducing operating voltage.

Imec describes the two research tracks as complementary. The same materials and integration knowledge can inform both capacitor and FeFET development, while three-dimensional integration techniques developed for FeFETs can potentially be applied to future ferroelectric capacitor arrays.

The technologies remain at the research stage. Remaining challenges include FeFET endurance and erase performance, together with further voltage scaling and reliability optimisation for ferroelectric capacitors. The next steps include system-level evaluation and development of fully integrated three-dimensional memory architectures.

2D materials take another step towards the fab

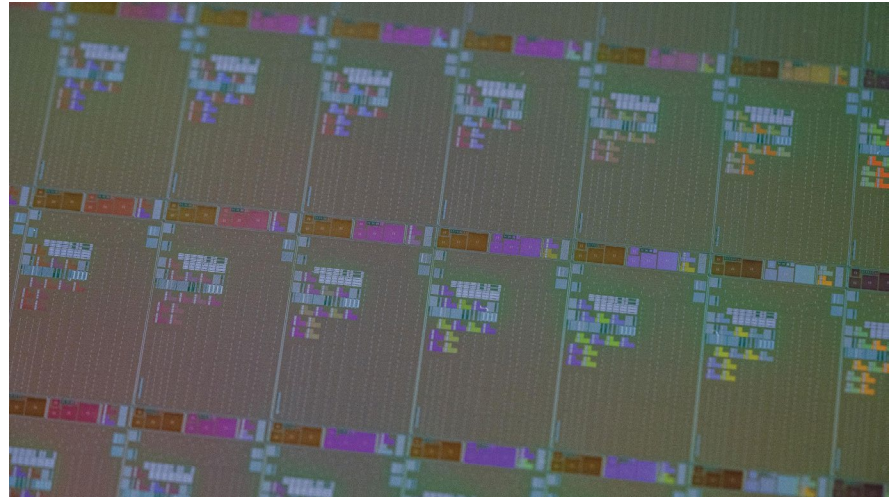
Perhaps one of the most consequential developments in the portfolio is the demonstration by imec, ASML and TSMC of scaled transistors based on two-dimensional materials on 300mm wafers.

Transition-metal dichalcogenides such as MoS_2 , WS_2 and WSe_2 have attracted attention because their atomically thin channels offer strong electrostatic control at very small dimensions.

The difficulty has been moving from laboratory-scale demonstrations to manufacturing processes compatible with semiconductor industry requirements.

The latest work demonstrates nFETs using MoS_2 and pFETs using WS_2 or WSe_2 with a **50nm contacted poly pitch (CPP)**, patterned using EUV lithography. Imec describes this as the first demonstration of scaled n- and pFETs based on these materials at this CPP.

The achievement is particularly significant because CPP includes both



gate length and source/drain contact length. Contacts have traditionally presented a major scaling challenge for 2D devices: while the atomically thin channel can be made very small, the surrounding contact structures can consume substantially more space.

The reported process achieved 50nm CPP without compromising the performance of the 2D n- and pFETs. Single-patterning EUV lithography was used in collaboration with ASML.

The devices also demonstrated low off-current at zero gate voltage, with pFETs based on WSe_2 performing close to the best reported laboratory devices.

Importantly, the n- and pFETs were integrated on the same 300mm wafer. The reported operational transistor rate was 94%, with an $I_{\text{max}}/I_{\text{min}}$ ratio greater than 10^5 .

The manufacturing approach uses a reverse thin-film transistor flow in which the TMD channel is transferred onto pre-patterned tungsten-filled trenches acting as contacts, followed by deposition of an overlapping gate.

The combination of 300mm processing, EUV patterning and CMOS-like integration makes the work relevant to the longer-term question of whether 2D materials can become part of an industrial technology roadmap rather than remaining primarily laboratory devices.

The research is also being positioned for applications beyond conventional frontside logic. Imec identifies potential roles for 2D materials in ultra-scaled

logic, back-end-of-line integration and wafer backside applications.

Backside connectivity becomes a critical part of 3D scaling

As semiconductor architectures become increasingly three-dimensional, the interconnections between the front and back of the wafer become just as important as the devices themselves.

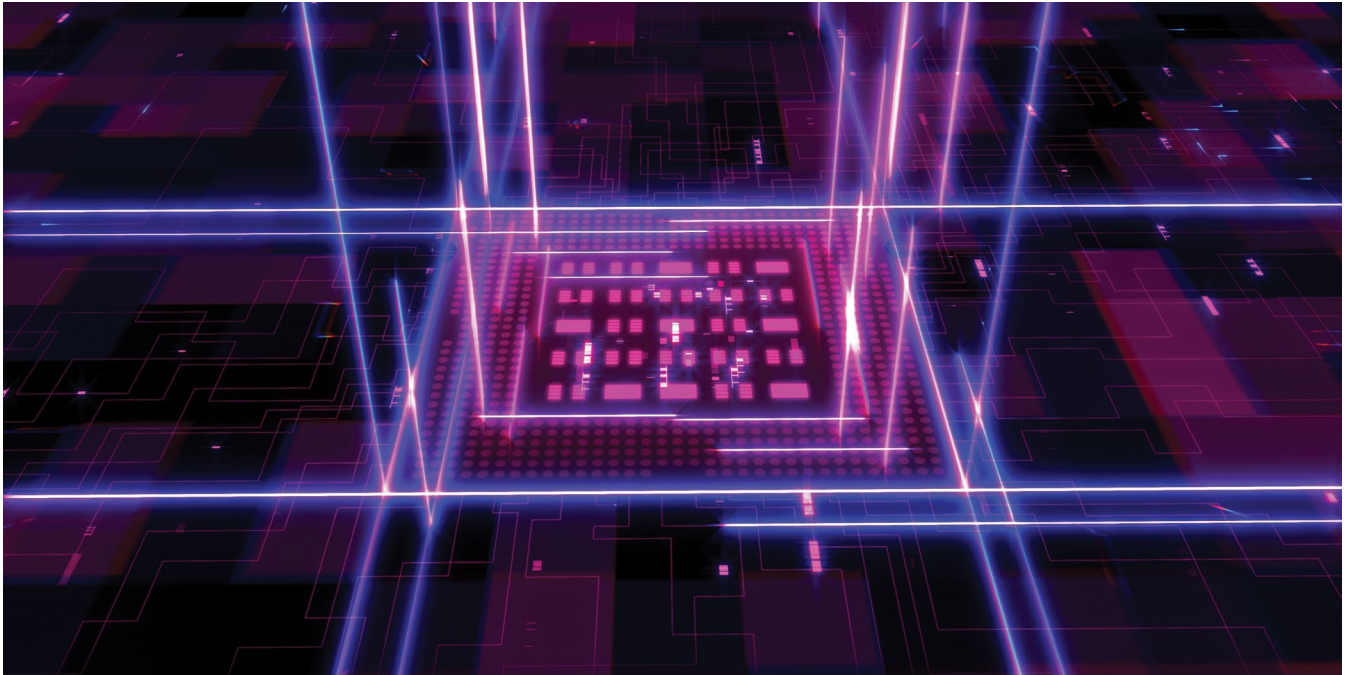
Imec and Sony Semiconductor Solutions have demonstrated a new approach to highly dense backside through-silicon vias (TSVs), using a self-aligned local backside dielectric isolation, or local BDI, module.

The approach is intended to provide dense front-to-back connectivity while reducing some of the electrical and manufacturing constraints associated with conventional via-middle TSV structures.

The resulting TSVs reportedly have lower aspect ratio, three times lower resistance, a three-times larger overlay window and lower leakage compared with conventional via-middle TSVs.

The issue is rooted in the geometry of conventional TSVs. High-density front-to-back connections can require narrow vias passing through relatively thick silicon, creating challenges for metallisation, alignment and electrical performance.

The local BDI approach instead forms a self-aligned isolation structure locally at the overlap between the TSV and active frontside region. The resulting geometry permits wider TSV connections.



Imec reports a 50% larger bottom and top critical dimension compared with the relevant via-middle approach, together with a threefold improvement in resistance. The demonstrated overlay tolerance extends to 30nm for a standard-cell configuration with 115nm cell height.

Another important characteristic is that the process can operate through bulk silicon up to 500nm thick. This could be relevant to applications such as DRAM, where a relatively thick silicon layer may remain on the backside.

The development highlights a broader shift in semiconductor integration. Backside processing is increasingly becoming an active component of device architecture rather than simply a packaging consideration.

For advanced logic and memory, the ability to move power, signals and functionality through the wafer can provide additional architectural freedom as frontside routing becomes increasingly constrained.

Silicon quantum computing enters the 300mm manufacturing equation

The most unconventional development in the group moves beyond conventional semiconductor computing altogether.

Imec and Diraq have demonstrated coherent operation and readout of an

eight-qubit silicon MOS spin-qubit array fabricated on imec's 300mm CMOS-compatible spin-qubit platform.

The result extends previous work beyond individual and two-qubit devices and provides evidence that increasingly complex silicon quantum systems can be manufactured using industrial semiconductor processing.

Silicon spin qubits are attractive partly because they can potentially exploit semiconductor industry's existing manufacturing infrastructure, supply chains and process expertise.

The new eight-qubit linear array builds on a 2025 demonstration showing that industrially manufactured silicon spin qubits could achieve fidelity levels relevant to quantum error correction. The latest work extends that manufacturing approach to a larger array while maintaining the coherence and controllability required for future scaling.

An important aspect of the demonstration is the scaling of the readout architecture. The larger array does not require a corresponding increase in sensor count, wiring density or thermal load. Such scaling characteristics are important because wiring and readout can become significant constraints as quantum processors grow.

The devices were manufactured using imec's 300mm silicon spin-

qubit platform, built around nearly a decade of process optimisation and engineering.

That connection to established semiconductor manufacturing is central to the significance of the work. Quantum computing has often been discussed as a fundamentally different manufacturing challenge, but silicon spin qubits create the possibility of using techniques derived from mainstream CMOS production.

The eight-qubit demonstration is not, by itself, a large-scale quantum processor. However, it addresses an important intermediate question: whether semiconductor manufacturing can support increasingly complex quantum devices without losing the properties required for quantum operation.

Integration is becoming the industry's new scaling language

Taken together, these developments point towards a semiconductor technology landscape in which "scaling" increasingly means more than shrinking the transistor.

The III-V interposer work uses heterogeneous integration to combine different semiconductor materials. The 2D-material programme introduces atomically thin channels into 300mm processing. Ferroelectric memory explores new materials and vertical architectures. The Sony- imec TSV work

develops new routes for connecting frontside and backside circuitry. The UWB receiver demonstrates how architectural innovation can improve wireless performance within an established CMOS process. The silicon quantum work applies semiconductor manufacturing to an entirely different computing paradigm.

The common denominator is integration.

For decades, semiconductor progress has been closely associated with increasing transistor density through lithographic scaling. That remains important, but the economics and physical constraints of advanced nodes are encouraging a more distributed approach.

Performance-critical functions can be fabricated using different materials and assembled together. Passive components can be moved from chiplets onto interposers. Memory can be stacked vertically. Electrical connections can be routed through the backside of the wafer. Novel channel materials can be introduced where silicon becomes increasingly constrained. Quantum devices can be fabricated using CMOS-compatible infrastructure.

This is not necessarily a replacement for transistor scaling. Rather, it represents an expansion of the semiconductor design space.

From research demonstration to manufacturing platform

The repeated appearance of 300mm processing across these developments is particularly significant.

A technology can demonstrate impressive device performance on a laboratory wafer while remaining far from practical semiconductor manufacturing. Industrial adoption requires reproducible processing, alignment, yield, process control, compatible materials, equipment availability and eventually economic viability.

The work on 2D materials explicitly addresses this lab-to-fab transition. The III-V interposer programme similarly combines device, passive, modelling and assembly technologies into a more complete platform. The quantum

work applies CMOS-compatible manufacturing to increasingly complex qubit arrays.

In each case, the question is shifting from “can the device work?” towards “can the technology be integrated, manufactured and scaled?”

That distinction will become increasingly important as semiconductor companies seek alternatives and complements to conventional scaling.

The technologies described here remain at different levels of maturity. Some, such as the RF interposer and UWB receiver developments, are being developed towards application and industry integration, while the ferroelectric memory, 2D transistor and quantum computing programmes remain more firmly in the research and technology-development phase.

Nevertheless, the direction is clear.

The next generation of semiconductor systems is likely to depend on multiple forms of integration operating simultaneously: heterogeneous materials, chiplets, three-dimensional stacking, backside processing, advanced packaging, novel memory devices and increasingly specialised computing architectures.

A broader definition of semiconductor innovation

The significance of imec's latest research is therefore less about any single breakthrough than about the convergence of multiple technology paths.

AI is creating pressure for more compute and memory capacity. High-frequency wireless systems are pushing semiconductor devices and interconnects towards mmWave and sub-THz operation. Data-centre architectures are demanding increasingly efficient signal handling and power delivery. Meanwhile, applications such as robotics and augmented reality require low-power sensing, positioning and communication.

Meeting these requirements will require semiconductor technologies that can combine different materials and functions while remaining compatible

with manufacturing ecosystems capable of producing them at scale.

The III-V RF platform addresses this through chiplets and interposers. The UWB work combines narrowband assistance with UWB positioning. Ferroelectric devices explore alternative routes to memory density and low-voltage operation. 2D materials seek to extend transistor scaling beyond conventional silicon channels. Backside TSVs provide additional connectivity for three-dimensional systems. Silicon spin qubits demonstrate how CMOS manufacturing can be extended into quantum computing.

The unifying idea is that future semiconductor performance may increasingly come from **integration at multiple levels**, rather than from transistor dimensions alone.

For the semiconductor industry, that creates a more complicated technology roadmap, but also a wider range of opportunities. The challenge will be converting promising device concepts into processes that can operate within the economic, manufacturing and reliability constraints of the semiconductor supply chain.

The latest research suggests that this transition is already under way. The 300mm wafer is becoming a common platform not only for conventional CMOS, but also for heterogeneous chiplets, emerging memory, 2D materials, backside interconnects and silicon quantum devices.

That may ultimately prove to be one of the defining characteristics of the post-planar semiconductor era: not a single successor to CMOS, but an increasingly diverse set of technologies connected by sophisticated integration and manufacturing platforms.

For the semiconductor industry, that creates a more complicated technology roadmap, but also a wider range of opportunities.

FoxSemicon's Thailand expansion: Building a strategic hub for the future of semiconductor manufacturing

Grace Lee, VP/CIO at Foxsemicon Integrated Tech, explains how Foxsemicon's major investment in Thailand marks an important step in the evolution of the global semiconductor equipment supply chain. She outlines the strategic thinking behind its Thailand expansion, the role of advanced manufacturing, automation and sustainability, and how the company is helping strengthen regional supply chain resilience while supporting the next generation of semiconductor technologies and talent.

THE GLOBAL SEMICONDUCTOR industry is undergoing profound transformation. Surging demand from artificial intelligence (AI), high-performance computing (HPC), advanced packaging technologies, and next-generation electronics is driving unprecedented investment across the semiconductor ecosystem. At the same time, geopolitical uncertainty, supply chain disruptions, and growing concerns around resilience have prompted manufacturers to rethink their global production strategies.

Against this backdrop, FoxSemicon Integrated Technology has made one of the most significant semiconductor

investments in Thailand in recent years. Following an investment exceeding 10.5 billion baht in 2024 and the inauguration of a major manufacturing facility in Chonburi in 2025, the company is positioning Thailand as a critical pillar of its global manufacturing network.

In an extensive interview, FoxSemicon outlined its vision for Thailand, discussed the future of semiconductor equipment manufacturing, and shared its perspective on automation, advanced packaging, talent development, and supply chain resilience. The message was clear: Thailand is not simply an additional

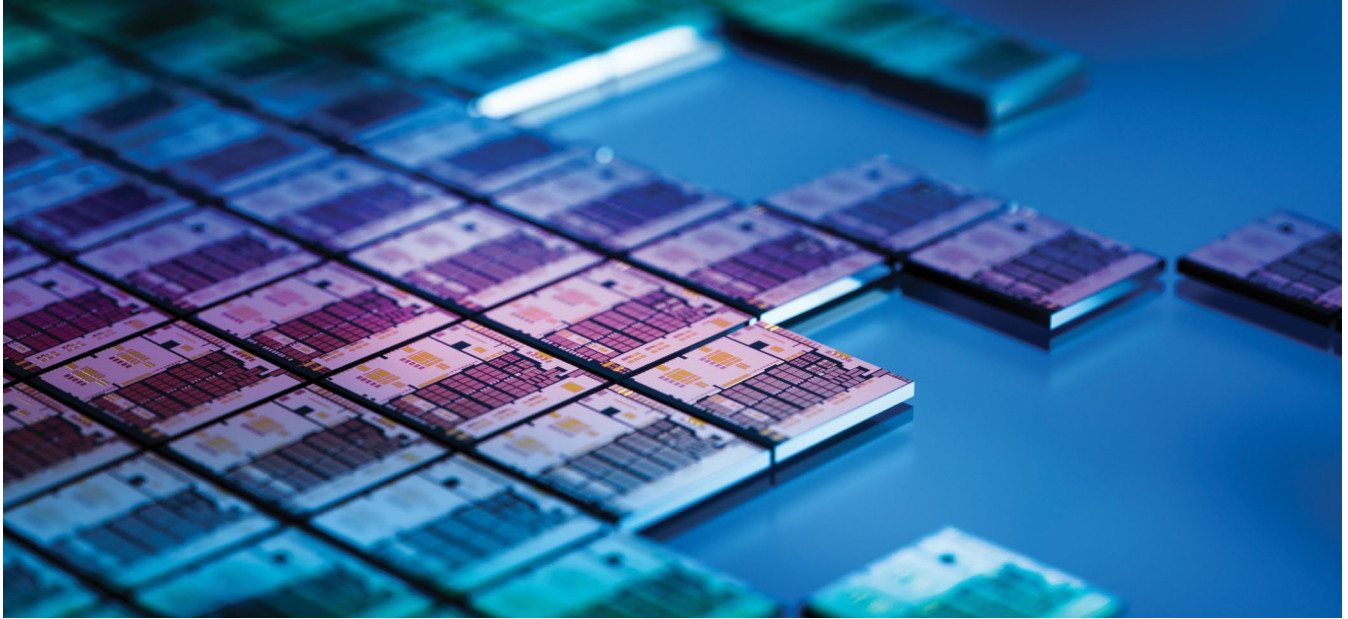
production location. It is becoming a strategic manufacturing hub with a key role to play in the future of the global semiconductor industry.

Why thailand?

Before committing to its major investment, FoxSemicon conducted a comprehensive assessment of potential manufacturing locations across Southeast Asia. After evaluating multiple countries, Thailand emerged as the preferred destination for three primary reasons.

First, Thailand offers a combination of strong infrastructure, political and economic stability, and government





support for high-technology industries. For a company making long-term investments in advanced manufacturing, these factors provide confidence that operations can be scaled sustainably over many years.

Second, Thailand's geographic position at the heart of Southeast Asia offers considerable logistical advantages. With access to regional transportation networks and proximity to key Asian manufacturing centres, Thailand enables more efficient supply chain coordination and facilitates faster responses to customer requirements worldwide.

The third factor relates specifically to FoxSemicon's manufacturing locations. Its Rayong facility is situated within Amata City Rayong Industrial Estate, one of Thailand's most established industrial zones. The estate hosts a large concentration of international manufacturers, particularly Japanese companies, creating a mature industrial ecosystem supported by experienced engineering talent, reliable suppliers, and strong manufacturing expertise.

According to FoxSemicon, these advantages collectively make Thailand an ideal location for long-term expansion. The investment is not merely about adding production capacity. It represents a strategic move designed to strengthen the company's global manufacturing footprint, improve supply chain resilience, and support future growth in semiconductor equipment manufacturing.

Chonburi: A new mega site for global operations

The inauguration of FoxSemicon's Chonburi facility marked a major milestone in the company's global strategy.

The plant serves as a "mega site" within FoxSemicon's worldwide manufacturing network, complementing operations in Taiwan, China, and the United States. More importantly, it introduces a vertically integrated manufacturing model that differentiates the company from many competitors.

Within a typical semiconductor equipment supply chain, critical manufacturing processes such as precision machining, sheet metal fabrication, surface treatment, assembly, integration, and quality inspection are often distributed among multiple suppliers and locations. FoxSemicon's Chonburi facility brings many of these processes together under one roof.

This level of integration delivers several benefits. It enhances operational efficiency, reduces production lead times, improves coordination, and supports more consistent quality control. It also gives FoxSemicon greater flexibility when responding to changing customer requirements and fluctuations in global demand.

The Chonburi facility also plays a crucial role in supporting product development activities. FoxSemicon's presence in Silicon Valley allows engineers to work closely with customers during

new product introduction (NPI) phases. Once products are certified and ready for volume production, manufacturing can be transferred efficiently to Thailand, where the company can scale production quickly and cost-effectively.

This combination of early-stage collaboration in the United States and high-volume manufacturing in Thailand creates what FoxSemicon describes as a "one-stop solution" extending from product development through to global production.

Resilience in an uncertain world

Few industries have experienced the impact of geopolitical tensions and supply chain disruption more acutely than semiconductors.

FoxSemicon believes that success in today's market depends on far more than cost efficiency alone. Instead, companies must build manufacturing networks capable of withstanding uncertainty while maintaining continuity of supply.

The company's response has been to strengthen its global footprint through geographically diversified manufacturing operations and vertically integrated production capabilities. Rather than concentrating manufacturing in a limited number of locations, FoxSemicon has established facilities across multiple regions to reduce operational risk and enhance business continuity.

This approach also extends to sourcing strategies. The company is actively

working to diversify its supplier base, with Thailand playing an increasingly important role.

Rather than simply importing materials and components, FoxSemicon is investing in the development of local suppliers. By helping Thai companies improve manufacturing processes, quality systems, and engineering capabilities, the company hopes to integrate more local firms into the global semiconductor equipment supply chain.

The ultimate objective is not merely diversification for its own sake. FoxSemicon aims to build an agile and resilient manufacturing ecosystem capable of supporting customers through future market volatility and technological change.

Supporting advanced semiconductor manufacturing

Although confidentiality agreements prevent FoxSemicon from naming specific products manufactured in Thailand, the company operates across some of the most advanced segments of semiconductor equipment manufacturing.

Its expertise spans deposition technologies including physical vapour deposition (PVD), chemical vapour deposition (CVD), and atomic layer deposition (ALD), along with etch systems, metrology equipment, and refurbishment services.

The facilities in Thailand manufacture critical modules and components used in semiconductor production equipment. These systems directly influence manufacturing precision, process stability, and production yields, making them fundamental to advanced chip fabrication.

As AI processors, HPC systems, and advanced packaging technologies continue to evolve, equipment requirements become increasingly demanding. For example, ALD technologies are becoming essential as semiconductor manufacturing moves below the two-nanometre process node.

By expanding its global manufacturing network and investing in Thailand, FoxSemicon intends to support customers as the industry transitions



toward increasingly advanced technologies.

Building thailand's semiconductor ecosystem

One of the most notable aspects of FoxSemicon's Thailand strategy is its emphasis on domestic supply chain development.

The company has stated that at least a quarter of its raw materials will be sourced locally. However, local procurement is viewed as more than a cost-saving measure. Instead, it forms part of a wider effort to create a sustainable semiconductor manufacturing ecosystem within Thailand.

FoxSemicon is working closely with Thai suppliers in areas including precision machining, sheet metal fabrication, surface treatment technologies, and high-precision components. The goal is to help local companies achieve the quality and manufacturing standards required by international semiconductor customers.

As supplier capabilities mature, more Thai firms will gain opportunities to participate in global semiconductor markets. This development could significantly strengthen Thailand's position within the regional technology landscape.

FoxSemicon believes that continued investment by semiconductor

manufacturers, combined with improvements in local capabilities, could establish Thailand as a major semiconductor equipment manufacturing hub in Southeast Asia.

Talent development: A critical priority

While advanced facilities and sophisticated equipment are essential, FoxSemicon emphasises that people remain the foundation of the semiconductor industry.

Modern semiconductor equipment manufacturing requires expertise across a broad range of disciplines, including materials science, mechanical engineering, electrical engineering, automation, software development, precision machining, surface treatment, quality management, and supply chain management.

Developing expertise in these areas requires substantial time and investment. Recognising this reality, FoxSemicon has made workforce development one of its highest priorities in Thailand.

The company is collaborating with universities, technical institutions, and academic partners to strengthen connections between education and industry. Internship programmes and industrial-academic partnerships are intended to nurture the next generation of semiconductor professionals.

According to FoxSemicon, building factories is relatively straightforward compared with developing a sustainable pipeline of skilled engineers and technicians. By sharing decades of manufacturing experience and technical knowledge, the company hopes to contribute meaningfully to Thailand's long-term semiconductor ambitions.

Key ingredients for national success

Thailand is currently developing a national semiconductor strategy, and FoxSemicon believes the initiative demonstrates a strong commitment to becoming a more significant player in the global industry.

From the company's perspective, three factors will be particularly important.

The first is talent development. Expanding the pool of skilled engineers, technicians, and manufacturing professionals will be essential to sustaining long-term industry growth.

The second is creating a strong domestic supply chain. Increased participation by local suppliers will enhance manufacturing efficiency, strengthen industrial capabilities, and improve resilience.

The third is collaboration across the broader ecosystem. Successful semiconductor industries rely on close cooperation between government agencies, universities, research institutions, industry partners, and investors.

FoxSemicon believes Thailand is moving in the right direction and is well positioned to attract additional investment if momentum continues.

The future of automation and smart manufacturing

As semiconductor manufacturing enters the angstrom era, automation is becoming increasingly important.

Through its subsidiary, Kainova Technology, FoxSemicon develops automation solutions for wafer handling, photomask management, and advanced packaging applications.

The company believes next-generation semiconductor manufacturing will require far greater levels of automation due to increasing complexity, tighter

tolerances, and the introduction of new materials such as glass substrates.

These materials are larger and more fragile than traditional silicon wafers, creating new challenges for handling systems and production equipment.

Automation is also evolving beyond simple material transport. Future systems will link process tools across entire fabrication facilities, enabling smarter and more efficient manufacturing environments.

According to FoxSemicon, automation will become a fundamental enabler of future semiconductor production by improving equipment utilisation, efficiency, quality, and overall return on investment.

AI, In-Situ monitoring and yield improvement

Another key technology area highlighted by FoxSemicon is real-time process monitoring.

Traditional process verification often occurs only after wafers have completed manufacturing steps. By the time defects are identified, significant losses may already have occurred.

In-situ sensing technologies allow manufacturers to monitor process conditions continuously within semiconductor equipment. This enables immediate detection of process variations, tighter endpoint control, and improved consistency.

When combined with AI-driven analytics, the benefits become even more significant.

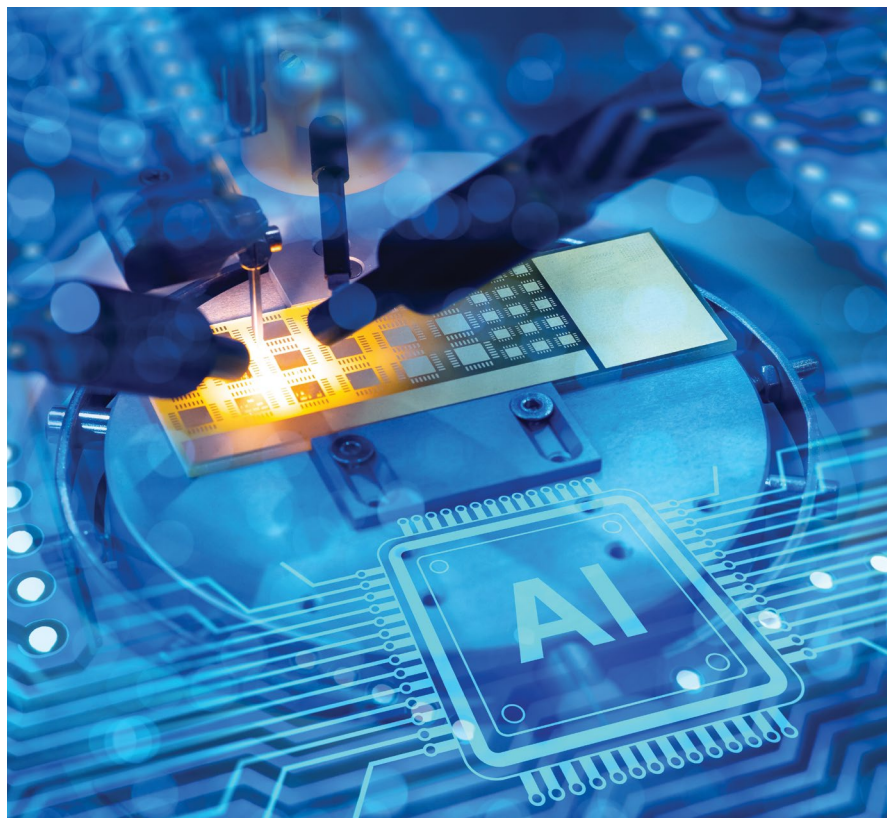
AI can analyse vast quantities of operational data, identify emerging issues, optimise process parameters, predict equipment degradation, and support predictive maintenance strategies.

The result is improved equipment uptime, higher productivity, enhanced process stability, and ultimately better manufacturing yields.

FoxSemicon believes future semiconductor equipment will increasingly incorporate intelligent decision-making capabilities powered by real-time data analysis and artificial intelligence.

Advanced packaging moves centre stage

Advanced packaging has rapidly become one of the most



important areas of semiconductor innovation.

Driven by AI, HPC, high-bandwidth memory (HBM), and next-generation data centre applications, demand is growing for solutions that deliver higher performance, lower power consumption, and greater bandwidth.

FoxSemicon believes that over the next five years, industry focus will shift increasingly toward advanced packaging, heterogeneous integration, and system-level integration rather than exclusively pursuing smaller process nodes.

Technologies such as panel-level packaging, advanced modules, and heterogeneous integration are expected to evolve simultaneously, serving different application needs rather than competing for a single dominant position.

Importantly, these trends align closely with FoxSemicon's manufacturing expertise. Advanced packaging requires sophisticated deposition, etch, metrology, and automation technologies, all areas in which the company has established extensive capabilities and partnerships.

Beyond semiconductors

While semiconductors remain its primary focus, FoxSemicon is also expanding into aerospace, medical devices, and robotics.

Although these industries serve different markets, they share common manufacturing requirements including precision, reliability, traceability, and stringent quality standards.

FoxSemicon believes the competencies it has developed over decades in semiconductor manufacturing are highly transferable. Expertise in precision machining, quality assurance, system integration, and global manufacturing management provides a strong foundation for expansion into adjacent high-technology sectors.

The company's emphasis on "copy exactly" manufacturing, ensuring products meet identical standards regardless of production location, is particularly valuable for industries with strict regulatory and performance requirements.

Sustainability as a core strategy

Sustainability is becoming increasingly important throughout the semiconductor supply chain, and FoxSemicon has embedded environmental considerations into its long-term strategy.

The company has implemented global programmes focused on greenhouse gas management, energy efficiency, water conservation, and sustainable supply chain practices.

In Thailand, sustainability principles were incorporated from the outset. Facilities were designed with comprehensive wastewater treatment systems and energy management programmes aligned with the company's global environmental standards.

FoxSemicon's view is that manufacturing excellence and sustainability are mutually reinforcing goals. Improving operational efficiency, conserving resources, and reducing environmental impact all contribute to long-term business resilience and value creation.

A global industry with regional manufacturing

Looking ahead, FoxSemicon does not believe the semiconductor industry is moving toward isolation or deglobalisation.

Rather, it sees the future as a balance between regional manufacturing and global collaboration.

Production capacity may become more geographically distributed as companies seek greater resilience. However, innovation, equipment development, materials technology, and engineering expertise will remain highly international in nature.

No single country or region possesses every element required for advanced semiconductor manufacturing. As a result, global collaboration will remain fundamental to industry success.

FoxSemicon's network spanning Taiwan, China, Thailand, and the United States reflects this philosophy, combining regional responsiveness with globally integrated operations.

Thailand's growing global importance

FoxSemicon's outlook for Thailand is exceptionally positive.

The company expects the nation to become one of the flagship hubs within its global manufacturing network, supporting advanced manufacturing, supplier development, talent cultivation, and smart factory initiatives.

More broadly, FoxSemicon believes Thailand has the potential to emerge as one of Asia's leading semiconductor equipment manufacturing centres. Continued investment in skills, infrastructure, and industrial ecosystems could position the country as a critical contributor to the global semiconductor supply chain.

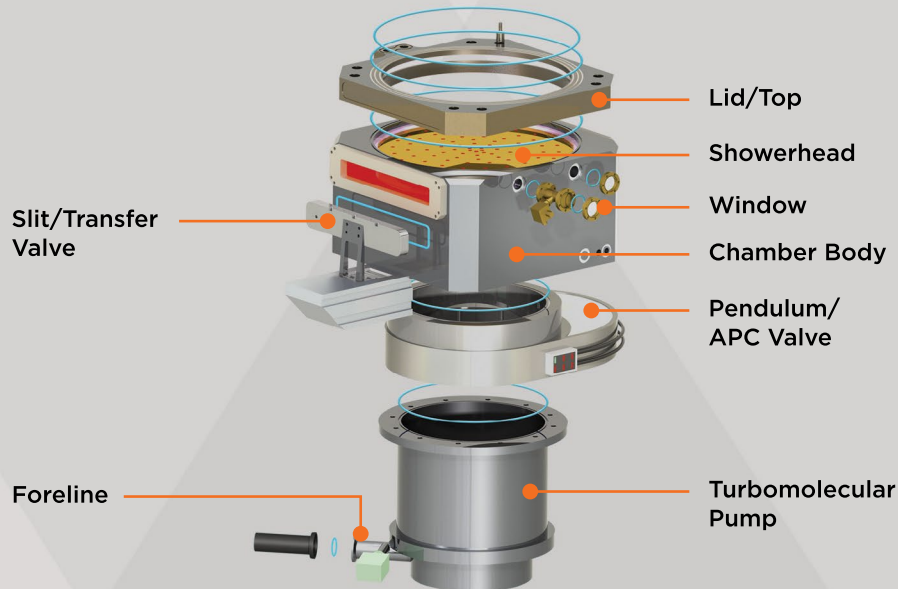
For FoxSemicon, Thailand represents far more than a manufacturing location. It is a strategic partner in the next phase of semiconductor industry growth, one that combines advanced manufacturing capabilities with a growing ecosystem of suppliers, talent, and innovation.

As demand for AI, advanced computing, and next-generation electronics accelerates, the company's investment suggests that Thailand's role in the global semiconductor landscape may be only just beginning.

FoxSemicon believes Thailand has the potential to emerge as one of Asia's leading semiconductor equipment manufacturing centres. Continued investment in skills, infrastructure, and industrial ecosystems could position the country as a critical contributor to the global semiconductor supply chain.



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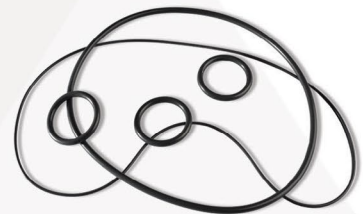
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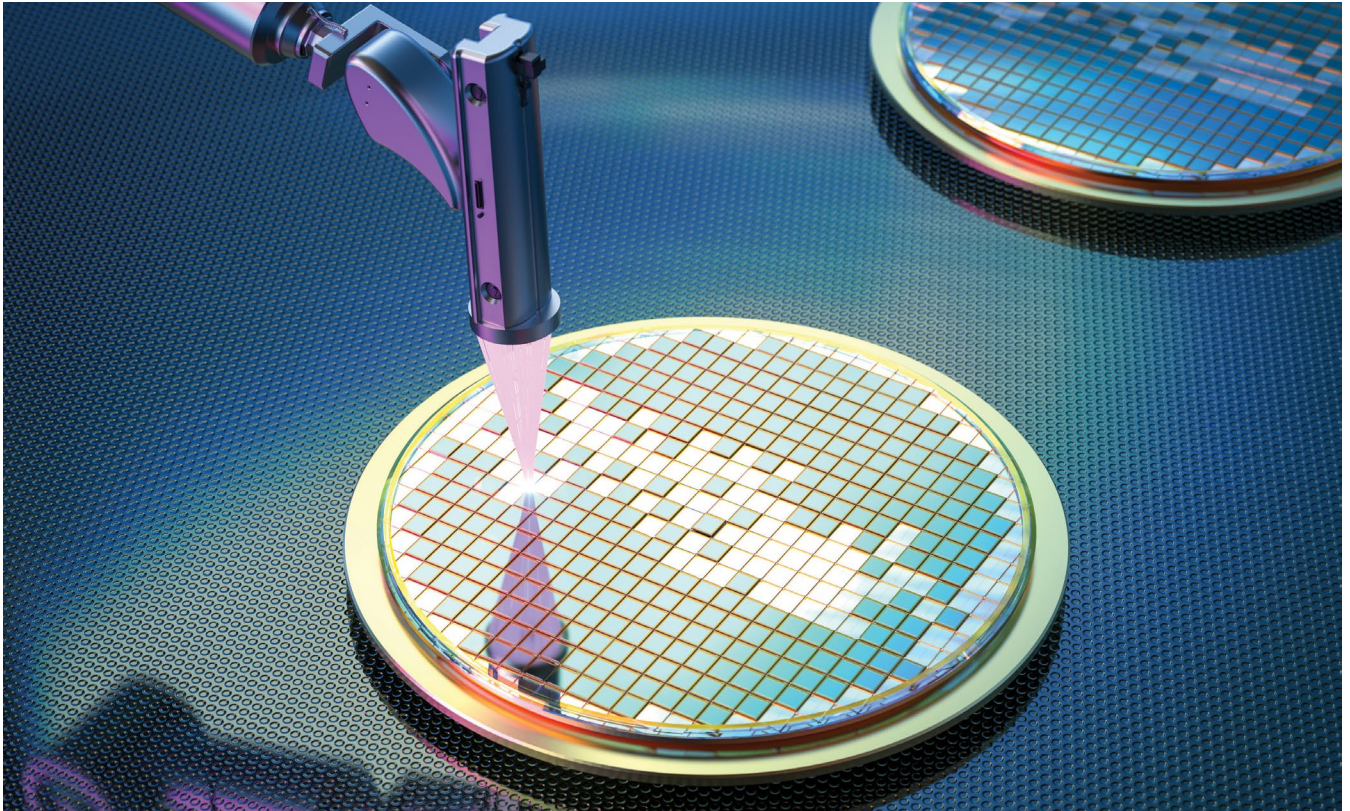
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The materials challenge behind High-NA EUV readiness

As the semiconductor industry moves toward high-numerical aperture (NA) extreme-ultraviolet (EUV) lithography, much of the attention has focused on exposure tools, optics, patterning performance, and the promise of continued transistor scaling. One of the most significant advances in lithography, High-NA systems enable the tighter patterning requirements needed for future logic and memory devices. Lithography tools alone, however, will not determine the success of the next scaling era.

BY LI YANG, JOHN COLLINS, CHRISTOPHER CAROFF, AND THAO NGUYEN, GELEST, A MITSUBISHI CHEMICAL GROUP COMPANY

INCREASINGLY, semiconductor manufacturers are recognizing that materials readiness has become one of the most critical enablers of High-NA EUV adoption.

The industry's ability to achieve the required levels of resolution, line-edge roughness, process window, defectivity, and manufacturability will depend not only on advances in optics and patterning schemes, but also on the underlying materials that make those processes possible.

Among the most promising candidates for future High-NA EUV processes are metal oxide resists (MORs) and dry resist platforms. These advanced materials offer potential advantages in EUV sensitivity, pattern fidelity, and process control. However, they also introduce new challenges involving precursor chemistry, impurity control, analytical characterization, thermal stability, and manufacturing scalability.

As feature dimensions continue to shrink and process windows narrow,

seemingly insignificant variations in precursor chemistry can have outsized effects on lithographic performance. The path to High-NA EUV therefore requires a broader view—one that encompasses not only lithography systems, but the entire materials ecosystem supporting them.

Why materials matter more for High-NA

The increased numerical aperture of next-generation EUV systems promises improved imaging resolution,

but it also increases sensitivity to process variability defects that could limit yield. Likewise, variations in material composition that were once insignificant can affect pattern formation, roughness, critical dimension control, and process repeatability.

This means the requirements for resist materials extend beyond basic photosensitivity. They must be more precisely engineered to provide consistent performance across increasingly demanding manufacturing environments while maintaining the stability and purity necessary for high-volume production.

This challenge has helped drive interest in MOR systems, particularly tin-based chemistries, which offer attractive properties for EUV applications. One reason tin has emerged as a leading candidate for MOR development is its strong interaction with EUV radiation. Because EUV photons are expensive to generate, efficient absorption is a critical requirement for photoresist materials. Tin can efficiently capture incoming energy at the 13.5 nm wavelength used in EUV lithography, generating the reactions necessary for pattern formation. This makes it particularly attractive for next-generation MOR architectures.

Although spin-on MOR approaches have demonstrated promising

lithographic performance, they also reveal a key challenge: moisture sensitivity. Moisture present in solvents can react with precursors, introducing embedded defects and impacting film quality that become increasingly problematic as dimensions shrink. These limitations have contributed to growing interest in dry resist approaches.

Dry resist precursors and vapor-phase processing

Dry resist technologies represent a fundamentally different approach to resist formation. Rather than relying on spin-coated liquid materials, dry resist systems use chemical vapor deposition (CVD) techniques to form resist layers directly on the wafer. One of the major advantages of this approach is the ability to precisely engineer precursor chemistry. The selection of ligands - often referred to as leaving groups - plays a central role in determining water reactivity, chemical stability, deposition characteristics, and storage requirements.

These design choices create a complex optimization problem. Greater reactivity may improve deposition performance but can reduce storage stability. Successful precursor development therefore requires balancing multiple competing requirements simultaneously.

Dry resist systems offer additional benefits including tighter film thickness control, reduced particle generation and potentially broader process windows. Combined with dry development techniques, they have demonstrated the potential for improved roughness performance and reduced exposure dose requirements relative to conventional chemically amplified resists. However, these benefits can only be realized if the underlying precursor materials meet extremely demanding purity standards.

As semiconductor geometries shrink, the tolerance for contamination continues to decrease. For advanced CVD processes, precursor purity becomes a first-order manufacturing concern. Even trace levels of impurities can alter deposition behavior, introduce defects, or affect lithographic performance.

Tin chemistry presents unique challenges in this regard. Several synthetic routes exist for preparing tin-based precursors, including metathesis reactions and redistribution pathways. Unfortunately, these processes can generate a range of closely related impurity species that may be difficult to detect using conventional analytical methods.

From a manufacturing perspective, identifying and controlling these



impurities is essential. Understanding impurity profiles helps researchers develop purification strategies, improve synthesis processes, and deliver materials suitable for high-volume semiconductor production. The challenge is not simply achieving high purity once; it is achieving it repeatedly, consistently, and at manufacturing scale.

Historically, semiconductor materials have relied heavily on analytical techniques such as gas chromatography (GC), gas chromatography-mass spectrometry (GC-MS), high-performance liquid chromatography (HPLC), inductively coupled plasma mass spectrometry (ICP-MS), and thermal analysis methods.

For many organometallic tin precursors, traditional chromatography presents significant limitations. Some tin compounds decompose before vaporization under atmospheric conditions, making GC-based analysis difficult or impossible. Likewise, many of these materials are intentionally designed to be highly reactive with water, creating challenges for HPLC methods that would require extremely dry mobile phases and analytical environments. These limitations necessitate alternative approaches capable of providing both structural information and impurity detection with high sensitivity.

The Growing Importance of ^{119}Sn NMR

One analytical technique that has emerged as particularly valuable for tin precursor development is Tin-119 (^{119}Sn) nuclear magnetic resonance (NMR) spectroscopy. Unlike traditional chromatography methods, ^{119}Sn NMR can provide detailed insight into precursor composition without requiring destructive testing or complex sample preparation. The technique offers parts-per-million sensitivity and high spectral resolution, enabling researchers to identify impurity species that may otherwise remain undetected.

For precursor developers, this capability is increasingly important. As lithography processes become more sensitive to material variation, the ability to accurately characterize trace impurities becomes essential for process optimization, manufacturing readiness, and product performance. Researchers have demonstrated that analytical parameters must themselves be carefully selected and controlled; variations in measurement conditions can negatively influence the ability to consistently detect low-concentration impurities.

In this sense, advanced characterization is a competitive differentiator. The industry's ability to understand materials at a deeper level directly impacts its ability to manufacture them reliably. Characterization alone is not

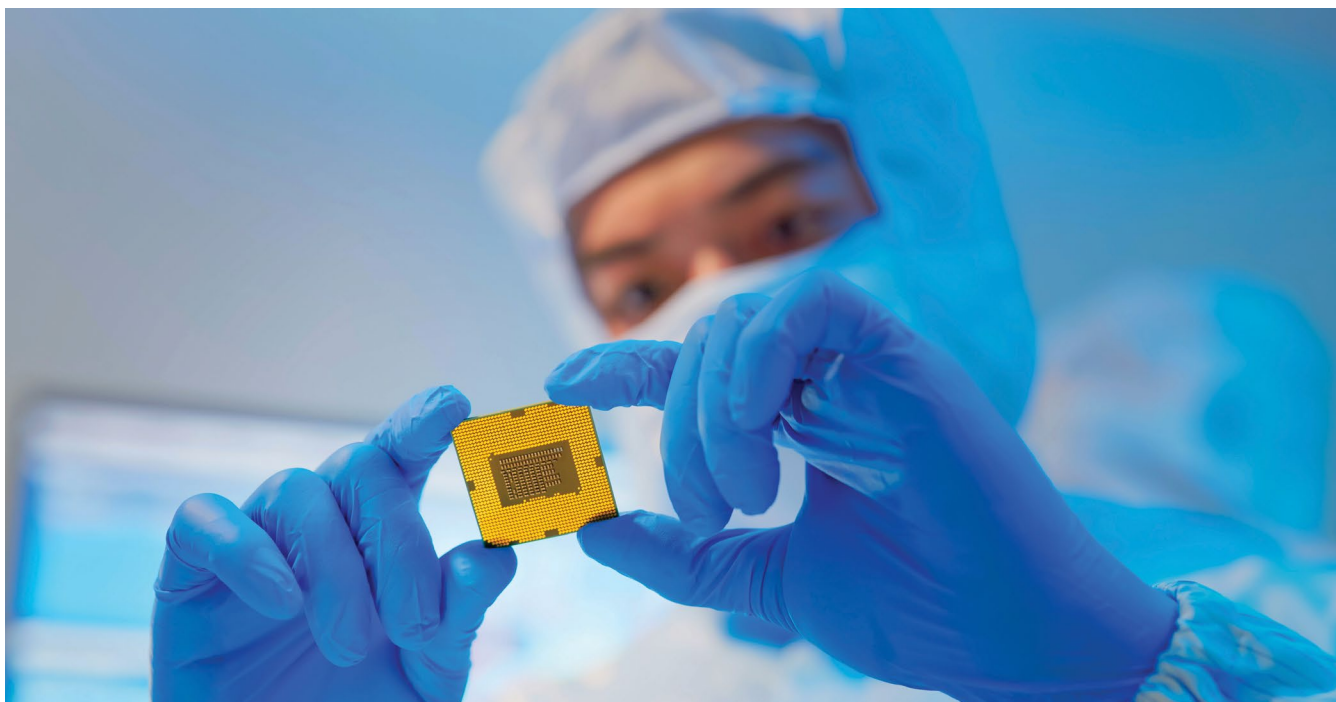
enough; High-NA EUV materials must ultimately transition from laboratory-scale research to industrial-scale manufacturing. This introduces another set of requirements centered on thermal stability, supply chain robustness, and production consistency.

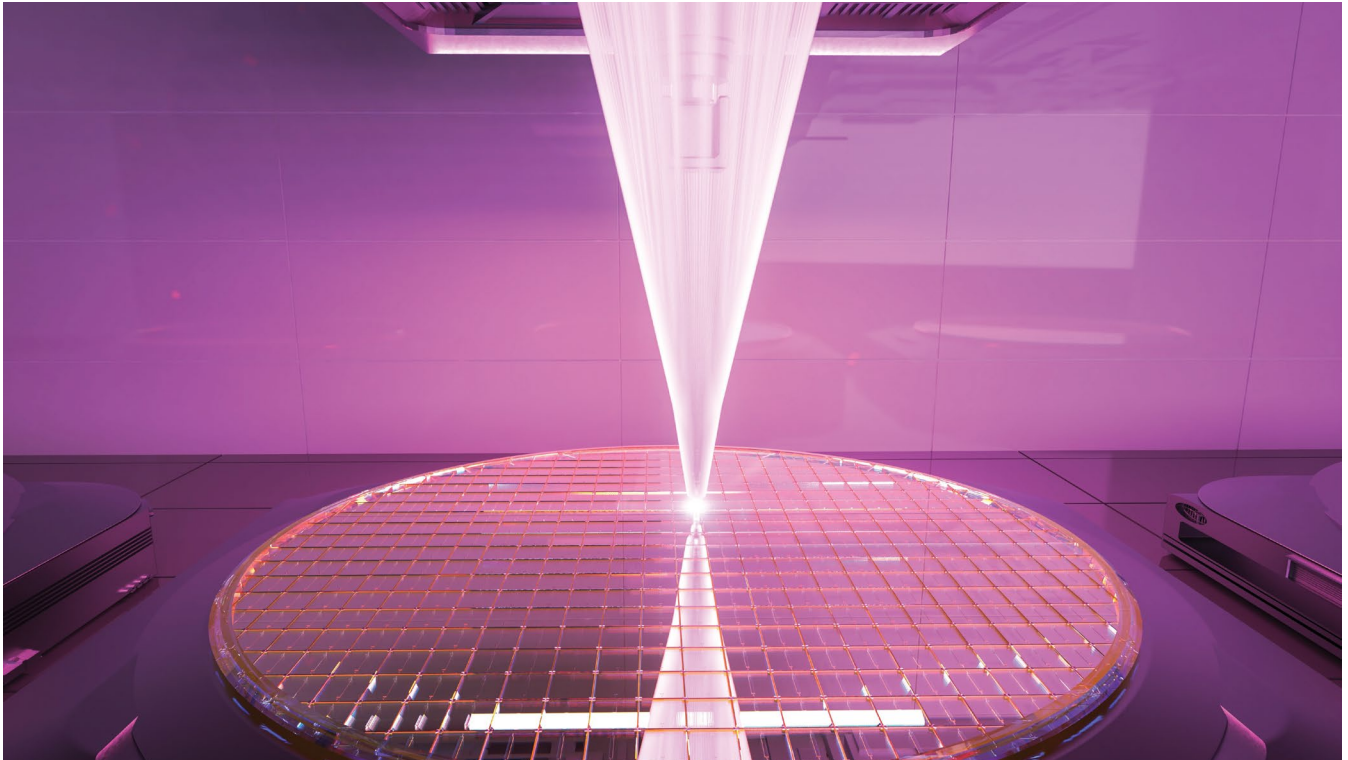
Process window and thermal stability

For CVD precursors, thermal stability directly influences storage, transportation, and process performance. Materials must remain stable under operational conditions while maintaining the volatility and reactivity required for vapor-phase delivery and deposition.

Recent work with next-generation tin precursors demonstrates how detailed stability studies can help identify optimal synthesis and manufacturing conditions. By understanding how process variables influence precursor stability, suppliers can improve consistency and reduce batch-to-batch variation.

This focus on manufacturing readiness is becoming increasingly important as semiconductor manufacturers evaluate materials for future production nodes. Qualification decisions are no longer based solely on lithographic performance; suppliers must also demonstrate the ability to provide secure, scalable, and repeatable





production capabilities suitable for supporting high-volume manufacturing.

Designing the next generation of precursors

The search for improved MOR materials continues. Researchers are actively exploring new precursor designs intended to improve sensitivity, reduce exposure dose requirements, and enhance patterning performance.

One area of investigation involves understanding how bond dissociation energies influence ligand removal during EUV exposure. The ability to efficiently cleave EUV-reactive ligands can affect resist sensitivity and overall lithographic performance. Although bond dissociation energy represents only one factor among many, it serves as a useful early-stage indicator when screening new molecular precursors.

Recent development efforts have already produced multiple generations of candidate precursors exhibiting improved lithographic characteristics, including reductions in exposure dose and improvements in pattern quality metrics. In addition to tin, researchers are investigating other high-absorption materials that could contribute to next-generation resist platforms as the industry advances toward the 2 nm era and beyond.

Collaboration vital to success

Perhaps the most important lesson emerging from High-NA EUV development is that no single company or technology can solve these challenges alone.

Lithography suppliers, materials developers, semiconductor manufacturers, research organizations, and equipment providers must work together to accelerate innovation cycles and align technology roadmaps.

The interdependence between lithography performance, materials chemistry, and manufacturing capability is becoming increasingly apparent. Progress in one area often depends on advances in another.

For materials suppliers, closer engagement with device manufacturers provides valuable feedback that can guide precursor development. For semiconductor manufacturers, early collaboration helps ensure materials are optimized for future process requirements before large-scale deployment begins.

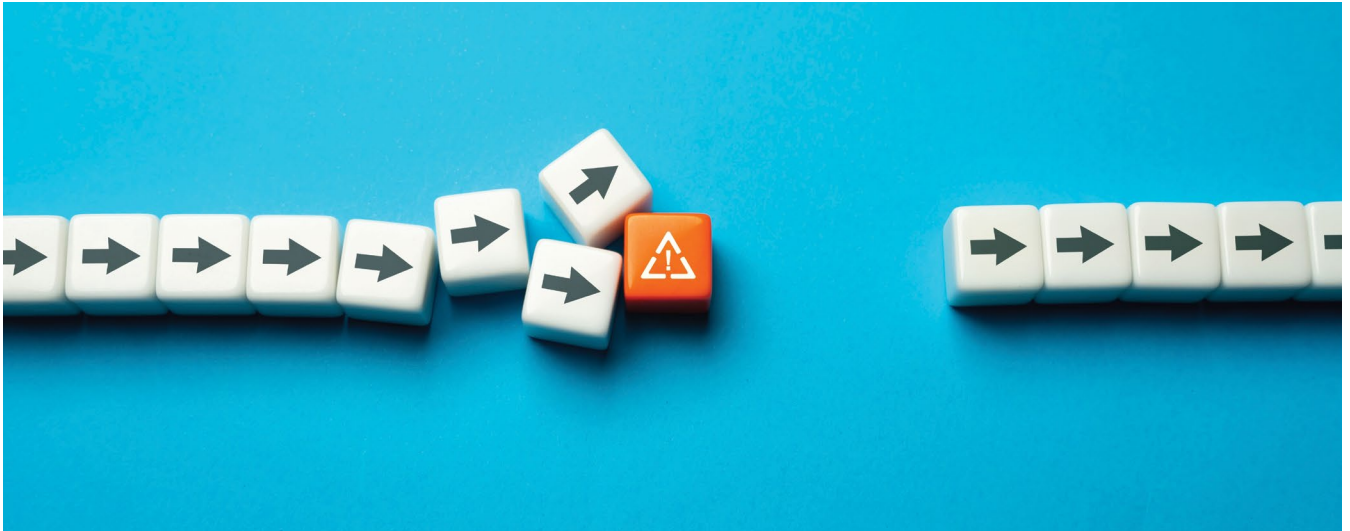
The transition to High-NA EUV lithography represents more than a lithography upgrade; it is an ecosystem challenge that demands coordinated innovation across multiple disciplines.

The next wave

The semiconductor industry often measures progress through the capabilities of its most visible tools. High-NA EUV scanners undoubtedly represent a remarkable engineering achievement and will play a central role in future scaling.

The ability to fully realize the benefits of High-NA EUV lithography may depend just as much on less visible innovations occurring within the materials supply chain. High-purity precursors, advanced analytical methods, scalable manufacturing processes, and collaborative development models are all emerging as critical elements of future lithography success.

As the industry prepares for the next generation of semiconductor manufacturing, materials readiness has become every bit as important as optical readiness. Gelest, for example, has constructed a 50,000-square-foot facility at its U.S.-based headquarters that will increase the company's production of precursor chemicals for use in dry-resist EUV lithography - broadening its ability to support advanced markets such as microelectronics, medical devices and automation. Addressing today the need to position themselves for the optical future will enable companies like Gelest to define the success of High-NA EUV lithography going forward.

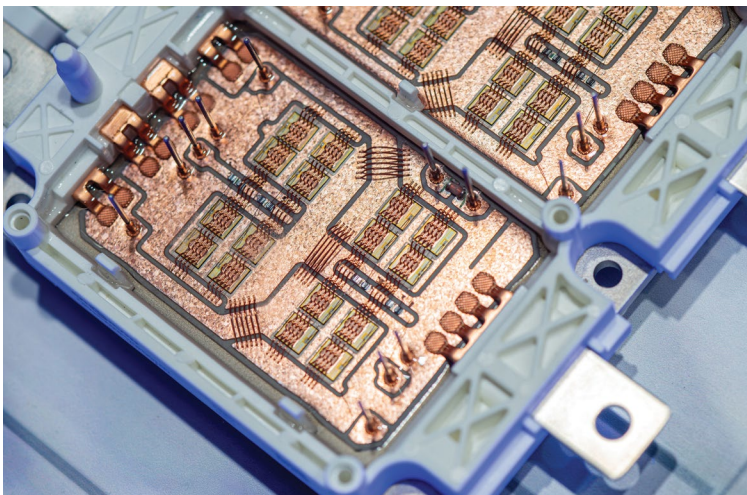


Why KGD is the make-or-break gate for advanced packaging and power modules

Known Good Die testing helps manufacturers detect defects earlier, improve module yield and reliability, and reduce downstream packaging and production costs.

BY COSMIC

IN SEMICONDUCTOR manufacturing, the cost of a defect rises at every subsequent step downstream. Testing at Known Good Die (KGD) stage is not a premium option reserved for research labs, it is a production necessity for maximizing yield, reliability, and optimizing total cost of ownership in advanced packaging and power module production. For device makers, the question is no longer whether to test the die, but how to define and execute a KGD strategy that is fast enough for production, rigorous enough to protect module quality, and reproducible enough to scale from lab characterization to high-volume manufacturing.



The industrial context: Smaller dies, denser modules, higher stakes

The relentless drive towards smaller, faster, and more powerful semiconductors makes process optimization a strategic imperative. As packaging becomes more advanced and modules integrate multiple dies, the penalty for shipping a defective die into assembly grows dramatically. A single faulty or underperforming die inside a multi-die package can compromise the entire module, triggering field failures, warranty costs, and brand damage that far exceed the cost of catching the defect earlier.

For power devices, the stakes are even higher. Modules for automotive, industrial, and energy applications must meet stringent reliability expectations under high voltage, high current, and harsh thermal cycling. In this context, KGD is not just about electrical functionality; it is about ensuring that only fully validated dies proceed to advanced packaging or module integration, minimizing downstream assembly costs and improving overall product reliability.

What “Known Good Die” really means in practice

“Known Good Die” is often used as a shorthand for “tested die,” but in production-grade environments it carries a more precise meaning: a die that has passed a defined set of electrical, parametric, and stress tests under controlled conditions that are

representative of its intended application. This makes KGD testing a critical process step, not merely a quality assurance formality. Beyond defect screening, parametric KGD testing also enables die-to-die matching, ensuring that all elements of a finished module switch in harmony and share the load symmetrically.

From a decision-maker's perspective, KGD is a risk-management tool. It shifts defect detection upstream, where the cost per escaped defect is lowest, and it provides a clear quality gate between wafer-level operations and downstream assembly. From a technical perspective, KGD defines which tests are mandatory, under what conditions (temperature, stress profiles, timing), and with what coverage (number of sites, statistical sampling, correlation to final test).

This requirement spans all three principal power-semiconductor technologies used in modern modules: silicon (Si), silicon carbide (SiC) and gallium nitride (GaN). Mature Si devices require robust screening of leakage, breakdown, switching and ruggedness. SiC devices place additional importance on high-field leakage, gate-oxide integrity, dynamic behaviour and parametric consistency. GaN devices demand close control of leakage, threshold and on-resistance stability, together with dynamic effects associated with high-speed switching such as trapped charge screening.

The risks of skipping or under-specifying KGD

When KGD is skipped or underappreciated, manufacturers effectively bet that wafer-level screening and final module testing will catch all critical defects. In mature, low-complexity products this may have been acceptable. In advanced packaging and high-reliability power modules, it is increasingly risky.

Typical failure modes that KGD aims to catch include:

- Dies with marginal breakdown voltage or leakage that may pass room-temperature tests but fail under thermal stress or high temperature operation.
- Devices with inconsistent avalanche or short-circuit behavior, which can lead to early failures in automotive or industrial applications.

If these dies reach module assembly, the cost of rework, scrap, and field returns can dwarf the investment in a robust KGD flow. Moreover, in safety-critical applications, an escaped defect can have consequences beyond economics, affecting system safety and regulatory compliance.

What a production-grade KGD system must deliver

A KGD strategy is only as good as the hardware and methodology that implement it. For device makers evaluating or upgrading their KGD capability, several requirements stand out.

Speed and throughput without compromising coverage

KGD sits between wafer test and final test in the value chain. If it is too slow, it becomes a bottleneck; if it is too light, it fails to protect downstream operations. A production-grade KGD test cell must therefore support high throughput while maintaining comprehensive test coverage. Platforms that enable ultra-fast AC and DC testing across multiple sites allow manufacturers to screen more dies per hour without sacrificing the depth of characterization needed to declare a die “known good.”

Built-in stress and robustness tests

For power semiconductors, electrical functionality is not enough. KGD must include stress tests that probe robustness under realistic operating conditions. Avalanche testing, short-circuit testing, and dynamic reverse bias tests are essential to ensure that dies can survive transient overvoltages, fault currents, and harsh switching environments. A KGD flow that integrates these stress tests as standard provides a much stronger guarantee of field reliability.

Reproducibility from lab to production

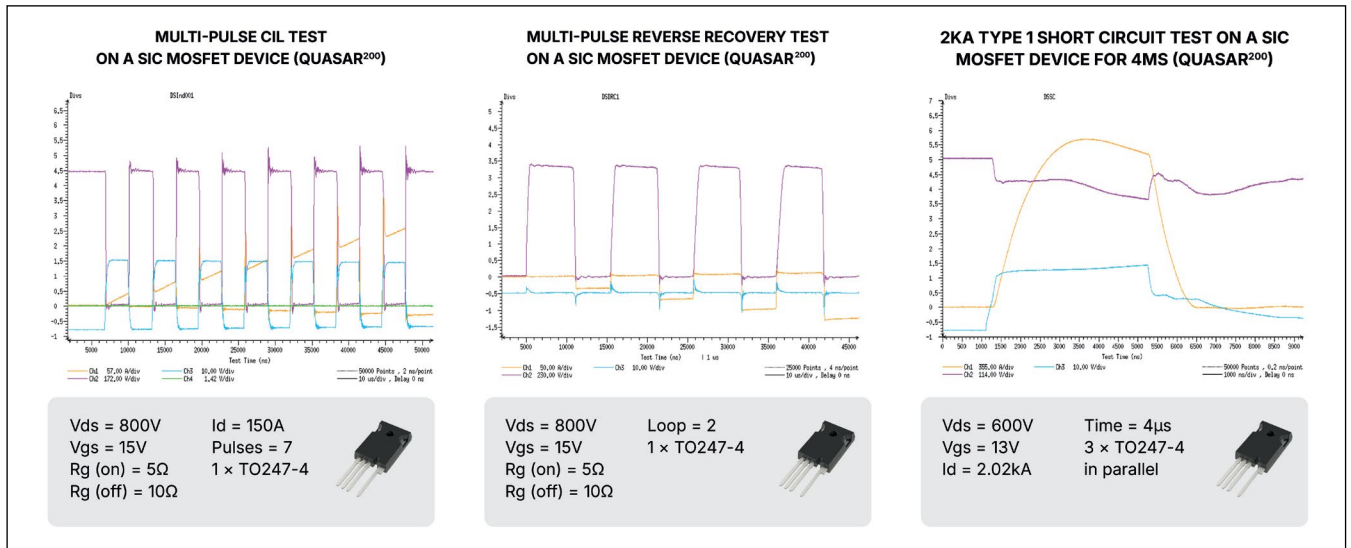
One of the most valuable aspects of a well-designed KGD platform is reproducibility. The same test architecture and loadboard philosophy used in lab characterization should scale to wafer-level KGD and final test with minimal re-engineering. This “lab-to-production” continuity reduces correlation issues, shortens qualification cycles, and ensures that the definition of “good” remains consistent across stages. For decision makers, this translates into faster time-to-quality, lower NRE costs, and more predictable yield ramps.

Cosmic's approach: A flexible, high-power KGD platform

Cosmic's equipment portfolio illustrates how these requirements can be met in a single, flexible platform. The M2 Rotary Edition, for example is ideal for testing power devices on any rotary or conveyor handler from bare KGD through to packaged

➤ M2 Rotary Edition features modular test generators which can be installed next to each test site for highest performance and minimal footprint





discretes and modules. Designed to maximize units per hour (UPH) in high-volume production environments, M2 ensures precision, repeatability, and reliability without compromising test accuracy.

M2 supports ultra-fast AC and DC testing, enabling high-throughput screening without sacrificing test depth.

The index-parallel architecture assigns dedicated generators to specific sites on the Rotary handler. This enables the system to run at the handler's maximum mechanical speed: on typical Rotary handlers, this translates into throughputs on the order of 15,000 units per hour for packages such as DPAK and TO-220. From an operational standpoint, this approach aligns with the industrial imperative highlighted in KGD literature: process optimization is strategic, and testing must be both rigorous and scalable. By enabling the same test philosophy from lab characterization through wafer-level and KGD through to final test, Cosmic's approach ensures measurement correlation and comprehensive test at every stage of production.

Implications for decision makers: TCO, yield, and risk

For R&D and operations leaders, the KGD decision is ultimately a total cost of ownership (TCO) calculation. Investing in a robust KGD flow entails capital expenditure, test development time, and ongoing operational costs. However, these must be weighed up by:

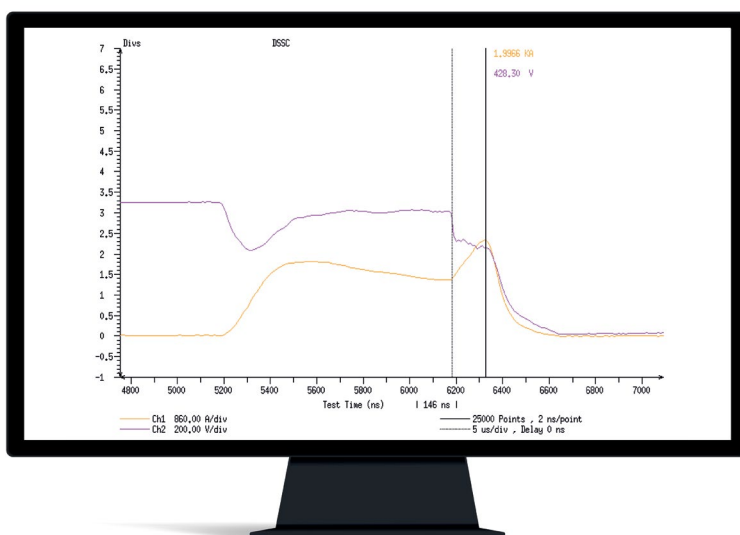
- Reduced scrap and rework in packaging and module assembly, as defective dies are filtered earlier.
- Higher effective yield at module level, since fewer bad dies enter the assembly line.
- Lower field failure rates and warranty costs, particularly in automotive and industrial applications where reliability is paramount.
- Faster qualification and ramp-up, thanks to reproducible test architectures that correlate from lab to production.

In high-mix environments, the flexibility of the KGD platform also matters. A system that can handle multiple device types and handler modes on the same architecture reduces the need for parallel lines and duplicate equipment, improving asset utilization and simplifying maintenance and training.

From strategy to execution: Defining your KGD roadmap

Implementing or upgrading a KGD flow is not just a procurement decision; it is a process redesign. Device makers typically benefit from a phased approach:

- **Define the KGD specification:** Identify which electrical, parametric, and stress tests are mandatory for each product family, and under what conditions (temperature ranges, stress profiles, timing).
- **Map the test flow:** Align KGD tests with wafer-level screening and final test to avoid gaps or unnecessary duplication. Ensure that the definition of "good" is consistent across stages.
- **Select a flexible, production-grade platform:** Choose a KGD handler that supports the required



throughput, stress tests, and handler modes, and that can scale from engineering batches to high-volume production.

- Validate correlation and reproducibility:** Run correlation studies between lab, wafer, KGD, and final test to ensure that results are consistent and that the KGD gate is effectively reducing downstream defects.
- Monitor and iterate:** Use KGD data to refine test coverage, adjust stress profiles, and identify process drifts at wafer level, turning KGD into a continuous improvement loop rather than a static checkpoint.

KGD as a strategic lever, not a cost center

In the current landscape of advanced packaging and high-reliability power modules, KGD is best viewed not as a cost center but as a strategic lever for yield, reliability, and brand protection. The industrial imperative is clear: process optimization is essential, and testing must be both rigorous and scalable. Platforms that combine speed, flexibility, and built-in stress testing—while maintaining reproducibility from lab to production—enable device makers to ensure that only fully validated dies proceed to advanced packaging or module integration.

For decision makers, the message is straightforward: a well-designed KGD strategy, supported by the right equipment and methodology, reduces downstream assembly costs, improves overall product reliability, and strengthens the foundation for next-generation semiconductor products.

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SCREEN

Shaping the future of semiconductor technology through global collaboration

A global R&D network is accelerating next-generation semiconductor manufacturing through collaboration and open innovation.

BY SCREEN'S R&D NETWORK AND NORTH AMERICAN INITIATIVES

Changes transforming semiconductor development

THE semiconductor industry is evolving at an unprecedented pace, driven by continued scaling of advanced logic devices, increasing memory stacking density, heterogeneous integration, and advances in advanced packaging technologies. As manufacturing processes become increasingly sophisticated and complex, it is becoming more difficult for any single company to address all technological challenges alone.

To respond to these changes, SCREEN Semiconductor Solutions Co., Ltd. (hereafter "SCREEN") is strengthening a global R&D network that connects Japan, North America, and Europe. Through collaboration with universities, research institutes, and technology partners worldwide, SCREEN is

accelerating the development of next-generation semiconductor technologies.

As a leading supplier of wafer processing equipment to the global semiconductor industry, SCREEN maintains the No. 1 global market share in wafer cleaning equipment* and offers a broad portfolio of solutions supporting semiconductor manufacturing, including lithography, annealing, inspection and measurement systems.

As semiconductor technologies advance and process requirements become increasingly complex, SCREEN continues to expand its research and development activities through partnerships with universities, research institutes, and technology organizations around the world. Through these efforts, the company is accelerating

next-generation semiconductor innovation and creating new opportunities for growth.

*Based on SCREEN in-house research.

ATCA: The core of SCREEN's North American R&D strategy

As an important hub within SCREEN's global R&D network, SCREEN established the SCREEN Advanced Technology Center of America (ATCA) in Albany, New York, in December 2025. Located within the Albany NanoTech Complex, one of the world's leading semiconductor research facilities, ATCA is SCREEN's newest overseas R&D center and provides a unique environment for technology validation and process evaluation aligned with leading-edge device development. SCREEN's presence in Albany will enable direct evaluation of how process technologies affect actual semiconductor device performance. ATCA engineers will work alongside SCREEN researchers, onsite partners, and other members of the Albany semiconductor ecosystem, giving them strong visibility into emerging process and integration challenges. ATCA will also serve as a hub for North America-focused partnerships with universities, start-ups, and suppliers, while creating a new pathway for future employees to join SCREEN and develop their careers and technical skills.

ATCA is currently building the infrastructure needed for full-scale 300 mm research activities, centered on SCREEN's core expertise in wafer



➤ ATCA: SCREEN Advanced Technology Center of America, Albany, NY

cleaning technologies and positioned for future expansion into thermal processing and advanced packaging applications. SCREEN's presence within the Albany ecosystem will ignite new ideas and support acceleration of new technology into SCREEN products.

Technology initiatives supporting ATCA

The SCREEN Group has built its businesses around its core technologies, "Surface Control & Processing" and "Imaging & Patterning," cultivated over many years, and has delivered a wide range of solutions across diverse industries. In the semiconductor equipment business, the company is also advancing science-based technology development in areas such as Process Simulation, Reaction Engineering, Data Intelligence, and Particle & Defectivity to address the growing complexity of semiconductor devices and manufacturing processes.

At ATCA, these technology foundations are combined with collaborations involving North American research institutes and industry partners to accelerate the evaluation and practical application of technologies for next-generation semiconductor manufacturing.

One example is SCREEN's research activities in reaction engineering near Boston, Massachusetts. Researchers are exploring chemical reaction mechanisms and novel chemistry while pursuing process innovations that can contribute to reduced environmental impact. Knowledge gained through these efforts is shared across SCREEN's global R&D network, including ATCA, to support future technology development.

Co-Innovation with the north american semiconductor ecosystem

One of ATCA's distinguishing features is its location at the center of North America's advanced semiconductor ecosystem. In Albany, semiconductor manufacturers, equipment suppliers, materials companies, universities, and research institutions work together to advance next-generation semiconductor technologies. ATCA serves as a bridge connecting SCREEN with this ecosystem, helping the company identify emerging technology trends and future customer



➤ PTC: SCREEN Process Technology Center, Hikone, Japan

requirements while accelerating collaboration with partners.

This environment enables the early validation of new technology concepts and supports research activities aligned with future semiconductor roadmaps. More than simply a research facility, ATCA functions as an open innovation hub where external expertise and SCREEN's technologies come together to create next-generation process solutions.

Collaboration with IBM and Applied Materials

Through collaboration with leading North American research organizations and technology companies, SCREEN is advancing the development of next-generation semiconductor technologies.

Through its collaboration with IBM, SCREEN is conducting research aimed at the High NA EUV era and future device technologies. Guided by future device roadmaps, the companies are evaluating and developing advanced process technologies for next-generation semiconductor manufacturing.

SCREEN is also collaborating with Applied Materials through activities at the META Center in Albany and the EPIC Center in Silicon Valley. By combining SCREEN's expertise in wafer cleaning, wet etch, and surface preparation technologies with Applied Materials' strengths in materials engineering, the companies are driving the development of next-generation process solutions.

By linking these collaborations with ATCA's activities, SCREEN aims to accelerate technical discussions, technology validation, and process evaluation with research partners while helping improve yield, performance, and reliability for increasingly complex semiconductor devices.

Connecting research and product development through ATCA and PTC

SCREEN continues to strengthen an integrated development framework that connects research, technology validation, and product development through collaboration between ATCA in the United States and the Process Technology Center (PTC) in Japan.

Located in Hikone, Japan, PTC serves as the company's primary center for equipment and process development. Through customer demonstrations and development activities based on customer requirements, PTC transforms manufacturing challenges into practical products and solutions.

Meanwhile, ATCA explores and evaluates future technologies through collaboration with North American research institutes and technology partners. Knowledge and evaluation results generated at ATCA are transferred to PTC and product development organizations, helping accelerate the conversion of new ideas into customer value.

Looking ahead

As semiconductor technology continues to advance, collaboration across companies, universities, and research

institutions will become increasingly important in fields such as new materials, novel device architectures, heterogeneous integration, advanced packaging, and sustainable manufacturing technologies.

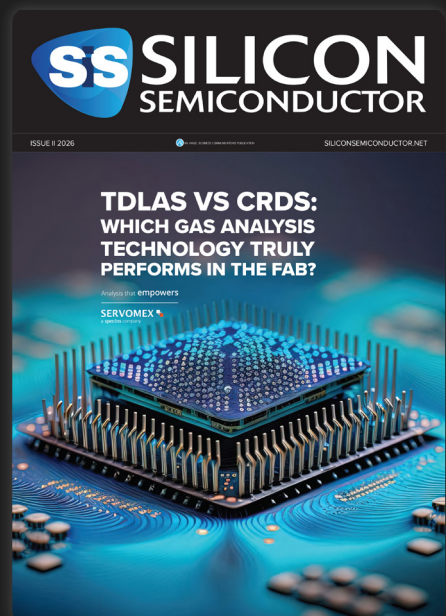
SCREEN is pursuing next-generation semiconductor innovation by integrating co-innovation within the North American semiconductor ecosystem centered on ATCA, science-based technology development in specialized areas, and product and process development activities at PTC.

By connecting expertise and technologies from around the world and transforming new ideas into validated technologies, products, and solutions, SCREEN seeks to contribute to the sustainable growth of the semiconductor industry. Guided by its mission, "A Better Tomorrow with Our Partners," SCREEN will continue driving innovation through global collaboration and open partnerships.



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Custom silicon comes of age

As AI, automotive electrification, industrial automation and personalised healthcare drive unprecedented demand for specialised computing, custom silicon is emerging as one of the industry's most important growth engines. **Ram Vedantham, Head of Semiconductor Delivery at HCLTech**, explains why general-purpose processors are increasingly insufficient, how engineering partnerships are becoming critical to success, and why post-silicon validation may be the next competitive battleground.

THE SEMICONDUCTOR INDUSTRY is entering a new phase of evolution. For decades, growth was driven largely by increasingly powerful general-purpose processors that could serve a broad range of applications. Today, however, the rapid rise of artificial intelligence, edge computing, advanced automotive architectures and data-intensive workloads is pushing traditional silicon approaches towards their limits.

As a result, enterprises, hyperscalers, OEMs and technology innovators are increasingly turning to custom silicon to achieve the performance, efficiency and differentiation that off-the-shelf devices can no longer deliver.

According to Ram Vedantham, who leads semiconductor delivery at HCLTech, this shift represents far more than a simple technology trend. It signals a fundamental transformation in how products are architected, developed and brought to market.

"We are seeing a fundamental shift between very general-purpose catalogue devices and processors into a more specialised, fine-tuned, end-application-oriented approach," says Vedantham. "That is what is driving custom silicon growth."

The perfect storm driving custom silicon

The forces behind custom silicon adoption are numerous, but they share a common theme: modern applications increasingly require domain-specific optimisation.

Artificial intelligence is perhaps the most visible example. AI training and inference workloads demand specialised architectures capable of processing vast quantities of data while maintaining acceptable power consumption. This has created demand for custom CPUs, GPUs, TPUs and AI accelerators designed around specific workload requirements.

The trend extends beyond cloud and hyperscale environments. Edge AI applications require highly efficient processing in constrained power envelopes, while networking infrastructure must evolve to support increasingly complex data flows between distributed intelligent systems.

At the same time, the semiconductor market itself is expanding at a remarkable pace.

"The industry was originally expected to reach the trillion-dollar mark around 2030," Vedantham observes. "Now it appears that figure may be reached significantly earlier."

Several sectors are contributing to that acceleration.

In automotive applications, the transition from distributed electronic control units towards

zonal architectures is dramatically increasing semiconductor content. The simultaneous rise of electric and hybrid vehicles further amplifies demand for highly specialised silicon.

Healthcare represents another significant growth opportunity. Personalised medicine and advanced diagnostics increasingly require compact systems that combine sophisticated sensing technologies with powerful local processing capabilities.

Industrial automation, factory digitisation and government-related applications are creating similar requirements. Across these markets, organisations seek devices that combine high computational performance with small form factors, robust security and application-specific functionality.

Another powerful driver emerged in the wake of the pandemic.

Supply-chain resilience and design sovereignty have become board-level priorities for many organisations and governments. Rather than relying exclusively on standard solutions sourced through global supply chains, companies increasingly want greater control over critical technology assets.

“We are seeing regions become more autonomous and independent in terms of being self-sufficient for their semiconductor needs,” says Vedantham.

Beyond performance: The real value of custom silicon

While performance remains a key attraction, the value proposition of custom silicon extends well beyond raw computing capability.

Historically, semiconductor design centred on optimising power, performance, area and development time. Those metrics remain important, but new factors are gaining prominence.

Among the most critical is performance-per-watt.

“The AI data centre has changed the discussion,” Vedantham explains. “It’s no longer just about performance. It’s about how much performance you can deliver per watt.”

This is particularly important as AI infrastructure scales. Energy consumption has become both an economic and operational challenge, making efficiency a strategic differentiator.

Custom silicon also enables organisations to create genuine product differentiation. By tailoring architectures around specific workloads and integrating unique capabilities, companies can develop solutions that competitors cannot easily replicate.

This differentiation increasingly relies on close integration between hardware, software and security. Rather than treating these elements separately, many organisations now view them as components of a unified architecture.

“There’s a need to integrate hardware, software and security into a joint ownership model,” says Vedantham.

The result is greater control over intellectual property, stronger competitive positioning and the ability to optimise complete systems rather than individual components.

Supply-chain advantages further strengthen the case. Custom silicon programmes allow organisations to develop deeper relationships across their supplier ecosystems while building greater resilience into future product roadmaps.

Ultimately, however, success still begins with delivering the right power-performance profile for a specific application.

“Power, performance and area remain the starting point,” Vedantham notes. “Everything else builds on that foundation.”

The capability gap

Despite widespread recognition of custom silicon’s strategic importance, many organisations struggle to execute successful programmes.

The challenge is not one of ambition. Rather, it is a combination of economics, expertise and complexity.

Leading-edge semiconductor development is extraordinarily expensive. Advanced AI data-centre-class devices can require investments

exceeding hundreds of millions of dollars before reaching production.

Beyond financial commitments, organisations must also address architecture development, verification, physical design, software integration, manufacturing coordination and post-silicon validation.

Verification complexity in particular has become a significant challenge.

As SoCs integrate more functionality, larger numbers of IP blocks and increasingly sophisticated interfaces, validation requirements continue to expand. Modern verification environments must simulate and analyse behaviour across a huge range of operating conditions long before first silicon arrives.

Attracting and retaining skilled engineering talent presents another major obstacle.

“Talent availability is critical,” says Vedantham. “You need strong teams capable of implementing extremely complex architectures.”

The challenge extends across the entire development lifecycle, from front-end architecture and RTL design through physical implementation, firmware integration and post-silicon validation.

Infrastructure requirements represent yet another barrier. Advanced verification platforms, characterisation laboratories and silicon bring-up facilities require substantial investment that many organisations find difficult to justify independently.

These realities are increasingly driving companies towards specialised

As SoCs integrate more functionality, larger numbers of IP blocks and increasingly sophisticated interfaces, validation requirements continue to expand.

engineering partners capable of providing expertise, reusable IP, development frameworks and ecosystem relationships.

The rise of strategic engineering partnerships

As custom silicon becomes more mainstream, the role of engineering service providers is changing fundamentally.

According to Vedantham, successful partners must be able to support customers throughout the entire lifecycle, from architecture definition to deployment.

That means far more than simply supplying engineering resources.

An effective partner must be able to contribute system-level expertise, design capabilities, verification methodologies, physical implementation skills, post-silicon validation and software integration.

Equally important is the ability to bridge traditionally separate disciplines.

“We should be there at each phase of deployment,” Vedantham says.

HCLTech’s semiconductor organisation currently combines thousands of hardware engineers with embedded software and firmware specialists, enabling integrated hardware-software development approaches.

The company has also focused heavily on reusable IP blocks, automation frameworks and AI-assisted development methodologies.

AI itself is becoming an increasingly important engineering tool.

“We are developing AI-based frameworks that can significantly reduce development cycles,” Vedantham explains.

Reducing design schedules by even a modest percentage can create substantial competitive advantages in markets where first-mover positioning often translates directly into market share.

Another differentiator is domain expertise.

Semiconductor requirements vary dramatically across automotive, industrial, telecoms and medical applications. Understanding the system-level context surrounding a chip often proves as important as understanding the silicon itself.

As custom silicon adoption expands into new sectors, that combination of semiconductor and application knowledge becomes increasingly valuable.

Building repeatable silicon platforms

Although custom silicon adoption continues to rise, many organisations

remain focused on individual projects rather than scalable platform strategies.

Vedantham believes the next phase of industry evolution will centre on transforming custom development into more repeatable and reusable frameworks.

Several technology trends are helping enable that transition.

Chiplet architectures are becoming increasingly important, particularly in high-performance AI applications. By combining multiple specialised dies within a single package, chiplets offer opportunities to improve scalability, reduce development costs and accelerate product development.

Standards such as UCle are also enhancing interoperability between chiplets and heterogeneous system components.

At the same time, advanced packaging technologies are enabling more sophisticated integration approaches, creating architectures that would have been impractical only a few years ago.

However, these opportunities introduce new complexities.

“The architecture becomes more modular and reusable,” Vedantham explains, “but it also creates significant packaging and design challenges.”

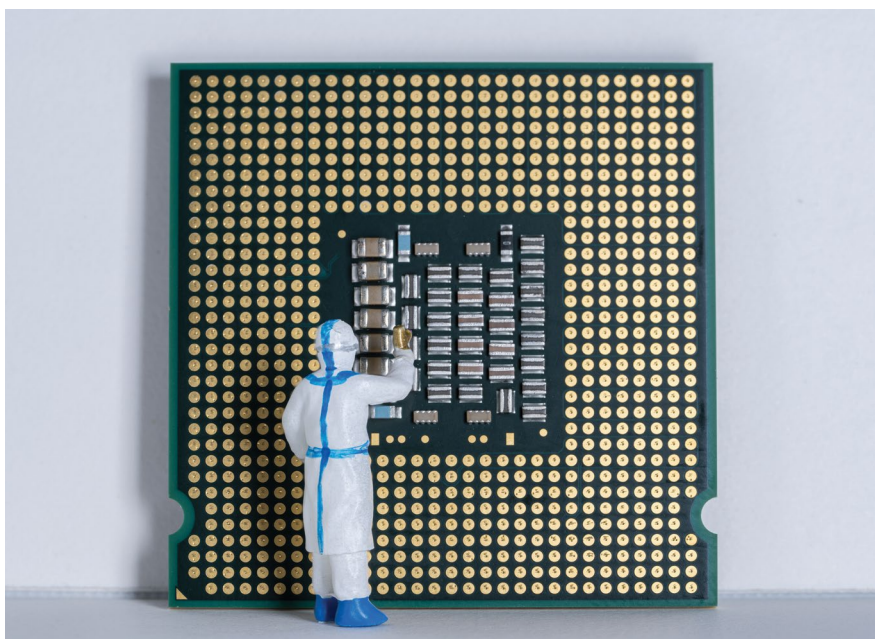
To address those challenges, organisations increasingly seek design-as-a-service models that allow them to focus on application differentiation rather than building complete semiconductor competencies internally.

For many companies, semiconductor development is not a historic core strength. Yet it has rapidly become essential for competitive differentiation.

That creates a growing opportunity for solution partners capable of bridging the gap between system requirements, silicon development and manufacturing ecosystems.

Why post-silicon matters more than ever

As silicon complexity continues to grow, the industry’s attention is increasingly shifting beyond tape-out towards post-silicon engineering.



Historically, much of the industry's focus centred on design and verification. Today, validation, characterisation, qualification and failure analysis have become equally critical.

This growing importance reflects the scale and complexity of modern devices.

Advanced AI processors can incorporate extraordinarily large die sizes while operating at cutting-edge process nodes. Multiple die stacks, heterogeneous architectures and sophisticated packaging technologies introduce additional validation challenges.

Many issues do not reveal themselves until silicon arrives from the foundry.

RF performance characteristics, analogue behaviours, package interactions and thermal effects frequently require extensive post-silicon investigation.

"The complexities involved in chip development do not always appear during the pre-silicon stage," says Vedantham. "They often emerge after silicon arrives."

As a result, bottlenecks in validation and qualification increasingly determine time-to-market performance.

Inside HCLTech's advanced semiconductor lab

To address these challenges, HCLTech has invested heavily in post-silicon infrastructure through its Advanced Semiconductor Lab (ASL).

The facility represents part of a broader semiconductor infrastructure investment programme exceeding \$60 million, including laboratories focused on semiconductor engineering, qualification and equipment.

At the centre sits the ASL facility itself, a 40,000-square-foot engineering environment featuring approximately 25,000 square feet of Class 1K and Class 10K cleanroom space.

Vedantham describes the laboratory as one of the company's most significant strategic investments.

"It is a critical cog in the entire silicon development flow," he says.

Advanced AI processors can incorporate extraordinarily large die sizes while operating at cutting-edge process nodes. Multiple die stacks, heterogeneous architectures and sophisticated packaging technologies introduce additional validation challenges.

The facility supports the complete post-silicon lifecycle, including functional validation, performance validation, automated test engineering (ATE), characterisation, reliability testing, qualification and failure analysis.

Capabilities extend to board design and manufacturing, allowing programmes to progress from first silicon through to high-volume production readiness within a single environment.

Equipment includes RF and electrical characterisation platforms, advanced test systems from suppliers such as Advantest and Teradyne, electron microscopy tools, failure-analysis systems and focused ion beam (FIB) technology.

An SMT production line further enables rapid prototyping and manufacturing support.

Accelerating time to market

The strategic value of integrating these capabilities lies in eliminating traditional hand-off delays.

In many development programmes, pre-silicon and post-silicon activities occur across different organisations, facilities and geographical regions. Knowledge transfer challenges frequently create delays and increase risk.

HCLTech's integrated approach aims to remove those barriers.

By combining design expertise with post-silicon validation resources,

engineering teams maintain continuity throughout the development process.

This creates opportunities to identify critical risks earlier, prioritise validation efforts more effectively and accelerate root-cause analysis when issues arise.

Perhaps most importantly, advanced failure-analysis tools enable rapid investigation and correction of silicon issues.

"When anomalies occur, we can identify them, validate potential fixes and proceed with greater confidence," says Vedantham.

The result is shorter validation cycles, improved yields and faster progression towards high-volume manufacturing.

As semiconductor complexity continues to increase, such capabilities are likely to become increasingly important.

The heart of the system

For Vedantham, the future of semiconductor innovation extends far beyond individual products or technologies.

He believes the industry is undergoing a broader transformation in how semiconductors are perceived and valued.

"We are entering uncharted territory," he says. "The semiconductor is no longer just a component in the system. It is the heart of the system."

As AI continues to reshape computing, as vehicles become increasingly software-defined, and as industries embrace intelligent automation, custom silicon will play a central role in enabling the next generation of innovation.

The opportunities are enormous, but so too are the challenges. Success will require deeper collaboration across the semiconductor ecosystem, greater investment in design and validation infrastructure, and new approaches to engineering partnerships.

For companies willing to embrace that shift, the rewards may be substantial. As the trillion-dollar semiconductor era approaches, custom silicon is rapidly moving from competitive advantage to competitive necessity.



International suppliers: Finding your footing in New York's semiconductor boom



If you supply chemicals, gases, equipment components, precision parts, packaging, logistics services or any of the dozens of other inputs a semiconductor fabrication plant requires, you have probably heard that something significant is happening in New York state.

BY JEFF DAVIS, WHO COLEADS BARCLAY DAMON LLP'S SEMICONDUCTOR TEAM AND CO-CHAIRS THE FIRM'S PROJECT DEVELOPMENT PRACTICE AREA, WITH ASSISTANCE FROM LAURYN FULTON, A BARCLAY DAMON ASSOCIATE

YOU ARE NOT wrong, but what you may not fully appreciate is how quickly the window to participate is closing and what it actually takes to walk through it as an international supplier.

New York is in the early stages of building one of the most consequential semiconductor manufacturing corridors in the world. Micron Technology has committed up to \$100 billion to develop a chip campus outside Syracuse in Clay, New York. GlobalFoundries is expanding its operations in Malta in the Capital Region. Wolfspeed operates a silicon carbide wafer facility mid-corridor in Marcy. Together, these investments are creating a concentrated, multisite procurement environment that simply did not exist five years ago.

For international suppliers, this is not just a business opportunity—it is a

strategic inflection point. But the rules for entering this market are different from what many overseas companies are accustomed to. The procurement frameworks, regulatory requirements, legal structures and incentive programs that govern participation in New York's buildout require deliberate preparation. Here is what you need to know.

Understand the landscape before you move

New York's semiconductor boom is not happening in isolation. It is the direct result of two interlocking policy frameworks: the federal CHIPS and Science Act (CHIPS Act), which provides tens of billions of dollars in incentives for domestic semiconductor manufacturing and supply chain development, and New York's own Green CHIPS program, which adds another layer of state-level support

designed to attract not just the fabs themselves but the ecosystem of suppliers that makes them run.

This policy context matters for international suppliers for a simple reason: The companies receiving these incentives have made commitments to domestic and regional supply chain development as conditions of receiving public funding. That creates both an opportunity and an expectation. Fabs want suppliers who can demonstrate a credible presence in the region, not just a willingness to ship from overseas.

This dynamic has a practical consequence: The time to qualify is now, during the construction and early ramp-up phase, not after production stabilizes. Supplier qualification processes and local ramp-up/buildout can be long. If you are not in those

conversations today, you risk being excluded from a generation of procurement relationships.

Get your legal and regulatory house in order

The single most common mistake international suppliers make when approaching the U.S. market is underestimating the legal and regulatory lift required to operate here. This is not a criticism—it reflects a genuine difference between the U.S. business environment and that in Europe, Asia or elsewhere. But this mistake can cost you months of time and significant credibility with prospective customers.

The first priority should be establishing a proper U.S. legal entity. Operating through a foreign parent without a U.S. subsidiary creates complications in contracting, liability, tax treatment and—critically in this sector—national security review. Semiconductor supply chains are subject to heightened scrutiny under the Committee on Foreign Investment in the United States, export control regulations administered by the Department of Commerce and in some cases the requirements attached to CHIPS Act funding. These are nothing insurmountable, but they all require advance planning.

Export control compliance deserves particular attention. The Export Administration Regulations (EAR)

govern the transfer of many semiconductor-related technologies, materials and equipment. If your products are classified under Export Control Classification Numbers (ECCNs) that require licenses for certain end uses or destinations, you need to understand how those obligations interact with your planned U.S. operations before you sign your first contract.

For suppliers from certain countries, there are additional layers: The CHIPS Act's "guardrails" provisions restrict CHIPS funding recipients from expanding semiconductor capacity in "countries of concern," and those restrictions flow through to suppliers in some circumstances. Your legal team needs to map your supply chain against these requirements before you make commitments.

Establish a physical presence and do it strategically

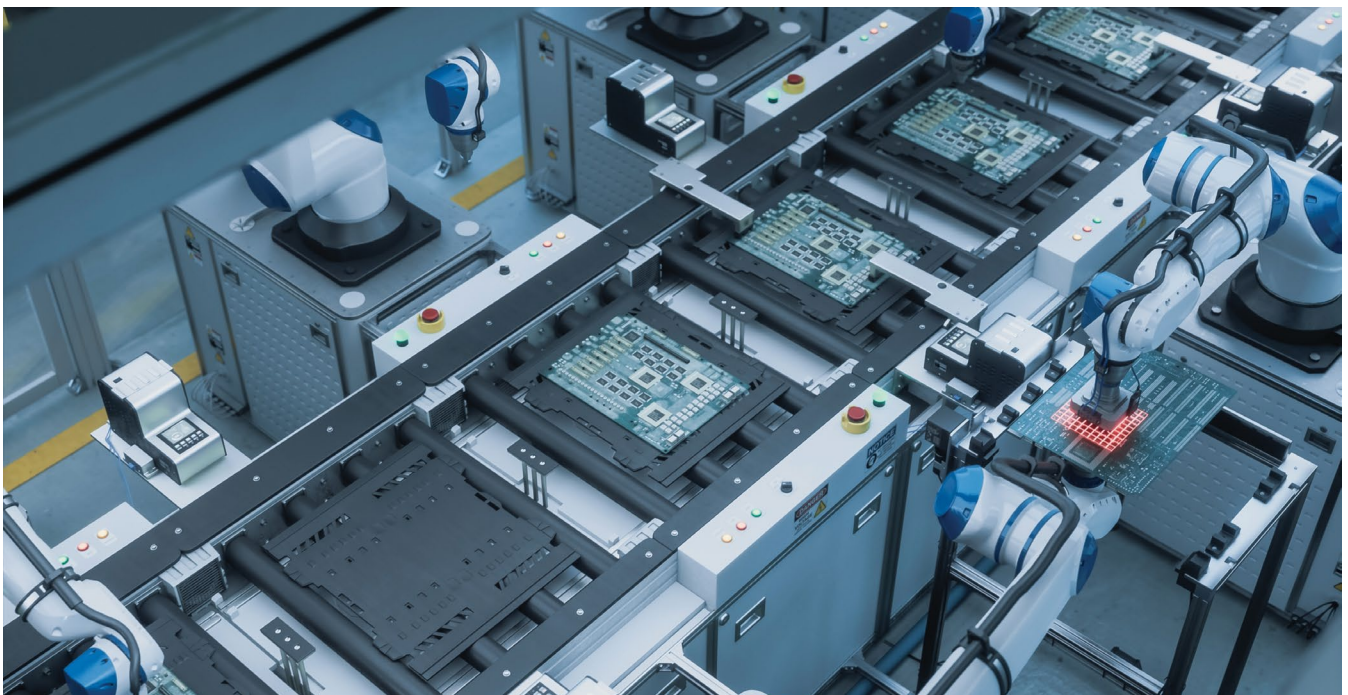
New York's fabs are not simply buying from catalogs. They are building supply chain relationships with companies that can provide responsive, regionally proximate support. For international suppliers, that means some form of U.S. presence is effectively a prerequisite, whether that is a stocking warehouse, a field service operation, a technical support office, or a light manufacturing or value-added reselling facility. The good news is that New York has made significant investments in site readiness

specifically to lower this barrier.

The state's FAST NY Shovel-Ready Grant Program funds infrastructure improvements—power, water, road access—at prequalified industrial sites across the state. For a supplier looking to establish a regional footprint, these pre-prepared sites can meaningfully compress the timeline and reduce up-front capital requirements.

Location matters beyond logistics. The corridor from Syracuse through the Capital Region to Mohawk Valley is where the concentration of fab activity is highest, and proximity to that corridor signals commitment. Local economic development agencies—CenterState CEO in the Syracuse region, the Center for Economic Growth in the Capital Region—are active partners for incoming suppliers and can facilitate introductions, site identification and connection to workforce pipelines.

Do not overlook the workforce dimension. New York has invested heavily in semiconductor-specific training through its community college system and State University of New York network. If your U.S. operation requires technical staff, that talent pool exists and is being actively developed. Building early relationships with regional workforce development organizations signals to your fab customers that you are a long-term partner, not a temporary opportunist.



Capture the incentives but sequence them correctly

New York's incentives stack for semiconductor supply chain companies is genuinely significant but it requires careful sequencing to capture. Incentives are not automatic; they are negotiated commitments tied to specific investment milestones, job creation targets and performance conditions. The most common mistake is treating incentives as an afterthought rather than integrating them into your entry planning from the start.

State level

The primary vehicle for supply chain companies is the Green CHIPS / Excelsior Jobs Program administered by Empire State Development. These are pay-for-performance programs offering fully refundable tax credits tied to net new job creation and qualified capital investment. Enhanced tiers are available for semiconductor supply chain projects, and the credits can be material (the Excelsior program offers jobs credits up to 7% of wages per net new job, up to 7% for R&D expenditures, and up to 3% of qualified capital expenditures; higher tax credits are available for projects qualifying under the Green CHIPS program), but they require application and approval by the state before you begin your project, not after.

Local Industrial Development Agencies offer an additional layer that many international companies overlook. IDAs can provide property tax abatements, sales tax exemptions on construction materials and equipment, and mortgage recording tax exemptions. For a supplier making a meaningful capital investment in a New York facility, the IDA benefits can represent millions of dollars in avoided cost. The catch: IDAs require public hearings, cost benefit analysis and annual reporting, and the IDA must pass an "inducement resolution" before construction begins and major equipment is purchased.

Federal level

The CHIPS Act offers over \$52 billion in incentives to boost domestic semiconductor manufacturing, including vital support for supply chain companies. Funding is overseen by the CHIPS for America program to build a robust ecosystem for materials, equipment and advanced packaging.

The key financial and operational incentives under the CHIPS Act include:

- **Manufacturing grants:**
\$39 billion in direct subsidies is available. While initially targeting large chipmakers, eligibility explicitly includes suppliers of specialized tooling, equipment, chemicals and foundational materials.
- **Advanced Manufacturing Investment Credit (Section 48D):**
A 35% tax credit is available for capital investments in semiconductor manufacturing facilities and the production of specialized semiconductor manufacturing equipment.
- **Research and Development consortia:**
\$11 billion is dedicated to R&D. Supply chain vendors can participate in programs via the National Semiconductor Technology Center and the National Advanced Packaging Manufacturing Program.
- **Direct pay option:**
Taxpayers can treat the 35% investment tax credit as a direct payment against their federal tax liabilities.
- **Defense funding:**
Additional opportunities and funding are available through the Department of Defense's Microelectronics Commons to support prototyping and commercializing defense-oriented components.

The CHIPS Act has important considerations for suppliers that receive CHIPS Act incentives, including a prohibition for 10 years against expanding, building or significantly upgrading advanced semiconductor manufacturing facilities in countries of concern, such as China or Russia, and compliance and clawbacks if a recipient violates the foreign expansion restrictions.

The NY SMART I-Corridor initiative, funded through the federal Tech Hubs program, is a collaborative initiative across upstate New York to accelerate supply chain readiness. The Supply Chain Activation Network identifies capability gaps and connects suppliers with fab procurement teams, and innovation vouchers through NY THRIVE can connect your technical staff to university facilities and research resources. These are not financial incentives in the traditional sense, but they are relationship-building tools that

The CHIPS Act offers over \$52 billion in incentives to boost domestic semiconductor manufacturing, including vital support for supply chain companies. Funding is overseen by the CHIPS for America program to build a robust ecosystem for materials, equipment and advanced packaging.

can accelerate your path to vendor qualification.

Build for the long term

The suppliers who will build enduring positions in New York's semiconductor ecosystem are not the ones who show up with a compelling sales pitch and a quick-turnaround proposal. They are the ones who demonstrate their physical presence, their quality systems, their contractual commitments, and their understanding of New York's processes and regulations.

That means investing in relationships before you have a contract to show for it. It means engaging with regional economic development organizations not just as a path to incentives but as a way to build credibility in the community. It means being honest with prospective customers about where you are in your qualification journey and what your timeline looks like. And it means treating the legal and operational infrastructure of your U.S. entry as a strategic asset, not a compliance checkbox.

New York's semiconductor buildout represents a generational opportunity for international suppliers. The fabs being built today will operate for decades. The supply chains being assembled now will define who participates in the next chapter of advanced manufacturing in the U.S. The companies that do the work to enter this market correctly will be positioned as indispensable partners for a very long time.

The window is open, and the opportunity to act is now.

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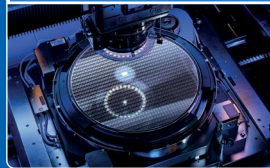
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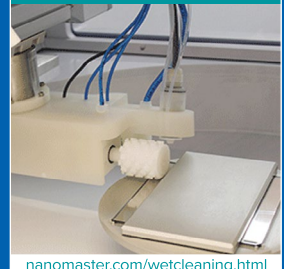


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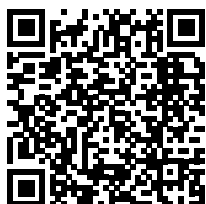
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