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Bonding & dielectric materials deliver 5G, IoT device packaging solutions

VOLUME 43 ISSUE IV 2022
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VIEWPOINT

By Mark Andrews Technical Editor

Silicon sales continue growth through Q2, is a turnaround coming?

THE SEMI trade industry association announced in mid-September that Q2 equipment billings continued the breakneck pace that has set and broke records regularly since 2020. Silicon seems to have avoided the pandemic trauma that devastated humanity, but for how long?

As of this writing US President Joe Biden took a 'victory lap' after signing the so-called Chips Act into law that will channel more than $50 billion into research and direct support for companies building fabs within US borders. The EU has its version. Can we expect equipment sales to continue booming for as long as the money flows? Time will tell.

With few signs of any serious headwinds other than global inflation running above 30-year highs and a population still pandemic weary, what could go wrong? Economists are already making cautionary statements and the US Federal Reserve will meet shortly; the Fed is expected to raise interest rates yet again to cool a steamy economy. How long can spend-spend-spend outpace save-save-save? Take a tip from someone who saw the Tech Bubble burst 22 years ago and who recalls when Apple stock sold for under $10 a share: Nothing is forever.

In this issue of Silicon Semiconductor we look at some exciting new permanent bonding electronic materials advances from Brewer Science that in addition to delivering top performance without the extreme production demands of other solutions, is a photo imageable dielectric with unbeatable benefits for 5G and IoT applications, amongst many. Edwards Vacuum shares new insights into the rapidly evolving subfab equipment revolution, including the challenge vendors face when customers want improved performance, substantially increased capabilities and a form factor shrink up to 30 percent. Edwards believe collaboration is key to creating win-win solutions.

We also look to the experts at LAM Research who are unveiling their new SPARC technology that enables ever-shrinking transistors to fit into ever-downsizing packages, all with substantially improved performance. And our friends at Onto Innovation detail how they have 'super-sized' their new JetStep X500 system that dramatically increases exposure fields up to 250x250mm, effectively slashing the number of exposures needed in FOPLP, along with a score of other money-saving benefits.

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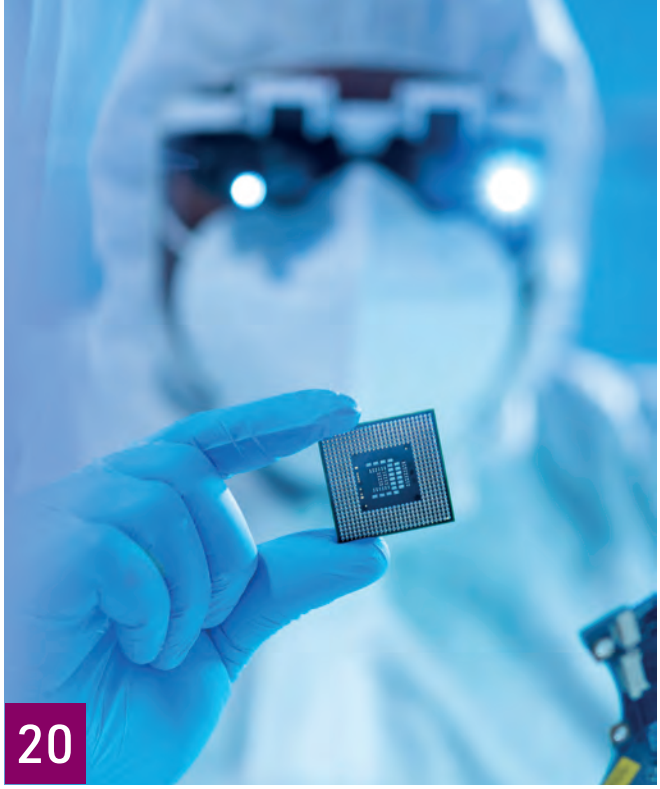

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Advantest to enable data analytics solutions

Semiconductor test equipment supplier Advantest Corporation has rolled out the Advantest ACS Solution Store, an advanced online platform that provides ease of access to ACS real-time data infrastructure solutions and software applications.

CUSTOMERS can conveniently discover, purchase and securely deploy all available ACS solutions from Advantest and a broad spectrum of analytics ecosystem partners across the semiconductor lifecycle process. In addition, the ACS Solution Store enables application developers from these partner firms to publish, promote, distribute and manage their Advantest-certified apps.

"The Advantest ACS Solution Store provides another key cornerstone for our ACS business model and strategy," said Michael Chang, vice president and general manager of ACS at Advantest.

"It will facilitate access to all ACS offerings for our customers, as well as give them and our partners the ability to develop and publish their own apps on our open ecosystem platform – ultimately, helping all participants in the ACS value chain to achieve transformational business results." Capabilities incorporated in the ACS Solution Store include browsing for available ACS solutions in an online catalog and discovering how the solutions help customers transform data into real-time production control, delivering significant ROI for the semiconductor manufacturing process.

In addition, automated software distribution is enabled via the ACS Container Hub for containerized apps, which ensures an easy, secure and reliable deployment of the apps in the test fleet. Key benefits of the ACS Solution store include:

- **Purpose Built:** enabling customers to buy and deploy Advantest-certified ACS apps from ecosystem partners with assured quality, verified security and guaranteed compatibility on Advantest test equipment.
- **Optimized and Integrated:** to provide customers with solutions tailored to deliver improved yield, quality, OEE and time to market.
- **Convenient:** a one-stop ecosystem portal where customers can seamlessly and securely deploy ready-made or custom-built company and partner apps from a single, trusted source, maximizing the value they can realize from ACS Edge and ACS Nexus, the key building blocks of the ACS real-time data infrastructure.
- **Versatile:** open solution ecosystem enables third-party developers and customers to develop data analytics solutions powered by ACS real-time data infrastructure.

Advantest launched ACS as part of its Grand Design strategy to enhance edge and cloud infrastructure services, data analytics and AI/machine learning solutions as a means of helping customers accomplish data-driven workflows.

Mycronic receives order for three SLX mask writers

MYCRONIC AB has received an order for three SLX mask writers from an existing customer in Asia. The order value is in the range of USD 17-21 million. Two systems are planned for delivery during the fourth quarter of 2023, while the third system is planned for delivery during the first quarter of 2024.

The SLX laser mask writer meets rising demand for photomasks for the semiconductor industry and a future need for replacement and modernization. Photomasks manufactured by laser mask writers are of high importance and account for 70-75 percent of all photomasks produced for semiconductor manufacturing. SLX is a new and modern mask writer based on the same technology as Mycronic's mask writers for displays.

"SLX's modern and flexible platform is well suited to meet different customer needs, which in this case is manifested by a repeat SLX order from an existing customer. This time the order is for three systems in two different configurations", says Charlott Samuelsson, Sr VP Pattern Generators at Mycronic.

Mycronic provides mask writers for display manufacturing and production of semiconductors.

EV Group expands collaboration with ITRI

EV Group (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets, has announced that it has expanded its collaboration with the Industrial Technology Research Institute (ITRI).

ONE OF the world's leading applied technology research institutes based in Hsinchu, Taiwan, on developing advanced heterogeneous integration processes.

With the support of the Department of Industrial Technology (DoIT) of the Ministry of Economic Affairs (MOEA), Taiwan, ITRI established the Heterogeneous Integration Chip-let System Package Alliance (Hi-CHIP) to help create an ecosystem covering package design, testing and verification, and pilot production, to achieve the goal of supply chain localization and expand business opportunities. As a member of the Hi-CHIP Alliance, EVG has provided several of its most advanced wafer bonding and lithography systems, including the LITHOSCALE® maskless exposure lithography system, EVG®850 DB automated debonding system, and GEMINI®FB hybrid bonding system.

The installation of these high-volume-manufacturing platforms at ITRI's state-of-the-art facility will help enable EVG's and ITRI's shared customers to accelerate the development and transfer of new heterogeneous integration processes from R&D to customers' fabs.

In semiconductor manufacturing, 3D vertical stacking and heterogeneous integration – the manufacturing, assembly and packaging of multiple different components and dies into a single device or package – are increasingly important for higher performance beyond transistor scaling. 3D and heterogeneous integration are enabling high-bandwidth interconnects in advanced packaging to achieve overall system performance gains, and thus have become a crucial driver for artificial intelligence (AI), autonomous driving and other high-performance computing applications. As a result, the MOEA is proactively following up and bridging the resources with national-scale R&D projects such as "AI Chip Heterogeneous Integrated Module Advanced Manufacturing Platform" and "Programmable Heterogeneous 3D Integration".

According to Dr. Robert (Wei-Chung) Lo, Deputy General Director of Electronic and Optoelectronic System Research Laboratories at ITRI, "As part of ITRI's mission to drive industrial development,

create economic value, and enhance social well-being through technology R&D, we focused on developing new 3D and heterogeneous chip integration processes and forging close cooperation across the supply chain to enable continued development and growth of the semiconductor industry.

Having the same fully automated high-volume-manufacturing systems in our research facility that our customers have in their fabs, including these new wafer bonding and lithography solutions from EV Group, enables our customers to immediately transfer process recipes developed at ITRI to their own fabs – providing short ramp-up time from lab to fab."

Intel signs agreement with Brookfield to jointly invest up to $30 billion

Intel Corporation has announced a first-of-its-kind Semiconductor Co-Investment Program (SCIP) that introduces a new funding model to the capital-intensive semiconductor industry.

AS PART OF its program, Intel has signed a definitive agreement with the infrastructure affiliate of Brookfield Asset Management, one of the largest global alternative asset managers, which will provide Intel with a new, expanded pool of capital for manufacturing build-outs.

SCIP is a key element of Intel's Smart Capital approach, which aims to provide innovative ways to fund growth while creating further financial flexibility to accelerate the company's IDM 2.0 strategy. Intel's agreement with Brookfield follows the two companies' memorandum of understanding announced in February 2022. Under the terms of the agreement, the companies will jointly invest up to $30 billion in Intel's previously announced manufacturing expansion at its Ocotillo campus in Chandler, Arizona, with Intel funding 51% and Brookfield funding 49% of the total project cost. Intel will retain majority ownership and operating control of the two new leading-edge chip factories in Chandler, which will support long-term demand for Intel's products and provide capacity for Intel Foundry Services (IFS) customers. The transaction with Brookfield is expected to close by the end of 2022, subject to customary closing conditions.

"This landmark arrangement is an important step forward for Intel's Smart Capital approach and builds on the momentum from the recent passage of the CHIPS Act in the U.S.," said David Zinsner, Intel CFO. "Semiconductor manufacturing is among the most capital-intensive industries in the world, and Intel's bold IDM 2.0 strategy demands a unique funding approach. Our agreement with Brookfield is a first for our industry, and we expect it will allow us to increase flexibility while maintaining capacity on our balance sheet to create a more distributed and resilient supply chain."

Sam Pollock, CEO of Brookfield Infrastructure, said, "By combining Brookfield's access to large-scale capital with Intel's industry leadership, we are furthering the advancement of leading semiconductor production capabilities. Leveraging our partnership experience in other industries, we are pleased to come together with Intel in this important investment that will form part of the long-term digital backbone of the global economy."

Benefits of the Transaction

Intel's partnership with Brookfield is expected to enhance the company's strong balance sheet by allowing Intel to tap into a new pool of capital below its cost of equity while protecting its cash and debt capacity for future investments and continuing to fund a healthy and growing dividend. Over the next several years, the structure is expected to provide a $15 billion cumulative benefit to Intel's adjusted free cash flow and is expected to be accretive to Intel's earnings per share during the construction and ramp phase. SCIP provides Intel the ability to replicate the co-investment model with other partners for other build-outs globally.

Intel's Smart Capital Approach

SCIP is an important component of Intel's overall Smart Capital approach, which is designed to allow the company to adjust quickly to opportunities in the market, while managing its margin structure and capital spending.

Through SCIP, Intel is accessing strategically aligned capital to increase its flexibility and help efficiently accelerate and scale its manufacturing build-outs. This type of co-investment also shows how private capital is unlocked and becomes a force multiplier for government incentives for semiconductor manufacturing expansion.

In addition to SCIP, the other key elements of Smart Capital include:

Smart capacity investments:
Intel is aggressively building out relatively low-cost shell space, which gives the company flexibility in how and when it brings additional capacity online based on milestone triggers such as product readiness, market conditions and customer commitments. In 2021, approximately 35% of Intel's capital expenditures was spent on infrastructure.

Government incentives:
Intel is continuing to work with governments in the U.S. and Europe to advance incentives for domestic manufacturing capacity for leading-edge semiconductors. Considerable progress has been made over recent months, as President Biden signed into law the CHIPS and Science Act of 2022 that includes funding for $52 billion in incentives for the U.S. semiconductor industry; the U.S. Congress is making strides with the FABS Act, which will establish a semiconductor investment tax credit in the U.S.; and the European Chips Act has added 15 billion euros to an existing 30 billion euros in public investments to build new infrastructure, among other advancements.

Customer commitments:
IFS is working closely with potential customers, and several have indicated willingness to make advance payments to secure capacity. This provides Intel with the advantage of committed volume, de-risking investments while providing capacity corridors for its foundry customers.

External foundries:
The company intends to continue its use of external foundries where their unique capabilities support Intel's leadership products.

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Keysight enable system-on-a-chip makers with new test solutions

Keysight Technologies has announced that the company's new 224G Ethernet test solutions enables system-on-a-chip (SoC) makers to validate next generation electrical interface technology, accelerating 1.6 terabit per second (1.6T) transceiver design and pathfinding.

5G, ARTIFICIAL INTELLIGENCE (AI) and internet of things (IoT) applications are driving growth in data traffic, creating unprecedented bandwidth demands in networks and data centers. High-speed digital interfaces that support 224 Gbps per lane data connection speeds offer increased bandwidths and underpin 1.6 terabit per second (1.6T) high-speed interconnect technology.

Improved data throughput and efficiency in data center networks also reduce power consumption and cost. Keysight is the only provider of bit error ratio tester (BERT) solutions capable of generating and analyzing 224 gigabit per second (224 Gbps) signals.

"Keysight is pleased to enable Synopsys, and other semiconductor makers, capture early market opportunities associated with the transition from 800 gigabit per second (800G) to 1.6T," said Dr. Joachim Peerlings, vice president of Network and Data Center Solutions at Keysight Technologies. "Keysight's unique portfolio of high-speed digital interface test solutions enable Synopsys to validate the performance of 224G IP designs accelerating 1.6T design and pathfinding."

The M8050A BERT offers users a unique 224 Gbps test solution for electrical design and validation of transceiver SoCs used in data centers and networks for transferring large amounts of data at high speeds. Keysight's M8050A BERT provides signal integrity that enables accurate characterization of receivers used in next-generation data center networks and server interfaces. Synopsys used Keysight's M8050A BERT, M8199 Arbitrary Waveform Generator (AWG) and Infiniium UXR-Series Oscilloscope to develop and validate 224G serializer/deserializer (SerDes) IP designs.

"High-performance computing systems depend on high-speed, low-latency interfaces to process massive amounts of data with minimal power," said John Koeter, senior vice president of marketing and strategy for the Solutions Group at Synopsys. "As a leading provider of high-speed Ethernet IP solutions, Synopsys utilizes Keysight's comprehensive digital interface test solutions to validate the performance of the PHY IP, enabling designers to meet their design and system-level requirements for high-performance computing, networking and AI SoCs."

At the European Conference on Optical Communication (ECOC) 2022 in Basel, Switzerland, Keysight and Synopsys will demonstrate the industry's first common electrical interface (CEI) SoC supporting 224Gbps.

Exhibition visitors can view the demonstration at the booth hosted by the Optical Internetworking Forum (OIF), an industry organization that promotes the development and deployment of interoperable networking solutions and services for optical networking products, network processing elements and component technologies.

Park Systems acquires Accurion GmbH

Park Systems Corp. has announced that it has acquired Accurion GmbH, a privately held company that develops and manufactures imaging spectroscopic ellipsometers and active vibration isolations

THIS ACQUISITION adds to Park's portfolio of atomic force microscopy and white-light interferometric microscopy. Financial details of the transaction were not disclosed.

Headquartered in Goettingen, Germany, Accurion GmbH has pioneered the field of imaging spectroscopic ellipsometry. Originally a spin-off from the Max Planck Institute for biophysical chemistry, the company started out designing the Brewster angle microscope for the characterization of ultrathin films.

As these microscopes turned out to be sensitive to vibrations, the division of active vibration isolation followed.

Accurion's Imaging Ellipsometers combine the benefits of ellipsometry and optical microscopy in a single device. The unification of the two technologies creates a unique metrology tool that redefines the limits of both ellipsometric measurements and polarization-contrast microscopy.

The enhanced spatial resolution of imaging ellipsometers expands ellipsometry into new areas of microanalysis, microelectronics, and bio analytics.

"This is Park's very first business acquisition in the company's history, and we are very excited to add this storied, high-tech company to our business," said Dr. Sang-il Park, CEO of Park Systems. "

Accurion's imaging ellipsometers and active vibration isolation will have wide range of product and business synergies with Park's existing line of atomic force microscopy that will benefit our customers and investors alike."

"We are honored to become a part of Park Systems," added Stephan Ferneding, co-founder and CEO of Accurion. "We are excited that Park's expertise and global sales and service reach in automated systems for industrial manufacturing will take the business to the next level.

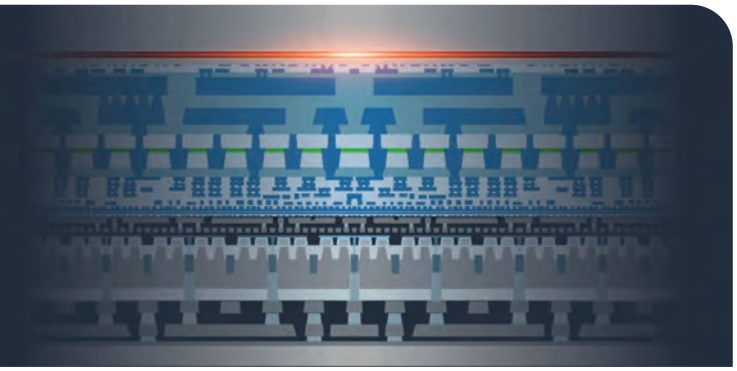
We look back on 30 years of valuable experience enabling technological and scientific progress for customers around the world. We look forward to continuing the success together with a strong partner like Park Systems."

EV Group revolutionizes 3D integration

EV Group (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets, has introduced NanoCleave™, a revolutionary layer release technology for silicon that enables ultra-thin layer stacking for front-end processing, including advanced logic, memory and power device formation, as well as semiconductor advanced packaging.

NANOCLEAVE is a fully front-end-compatible layer release technology that features an infrared (IR) laser that can pass through silicon, which is transparent to the IR laser wavelength. Coupled with the use of specially formulated inorganic layers, this technology enables an IR laser-initiated release of any ultra-thin film or layer from silicon carriers with nanometer precision.

As a result, NanoCleave enables silicon wafer carriers in advanced packaging processes such as Fan-out Wafer-level Packaging (FoWLP) using mold and reconstituted wafers as well as interposers for 3D Stacked ICs (3D SIC). At the same time, its compatibility with high-temperature processes enables completely novel process flows for 3D IC and 3D sequential integration applications – enabling hybrid and fusion bonding even of ultra-thin layers on silicon carriers, thereby revolutionizing 3D and heterogeneous integration as well as material transfer in next-generation scaled transistor designs. EV Group's revolutionary NanoCleave layer release technology uses an infrared (IR) laser that can pass through silicon and inorganic release materials to enable an IR laser-initiated release of any ultra-thin film or layer from silicon carriers with nanometer precision. Source: EV Group.



Company executives will be available to discuss this IR laser transfer technology breakthrough at SEMICON Taiwan, taking place at the Taipei Nangang Exhibition Center Hall 1 (TaiNEX 1) in Taipei, Taiwan, from September 14-16. Event attendees can visit EVG at Booth #L0316 (4th Floor) to learn more.

Silicon Carriers Benefit 3D Stacking and Back-end Processing

In 3D integration, carrier technologies for thin-wafer processing are key to enabling higher performance systems with increasing interconnection bandwidth. Glass carriers have become an established method for building up device layers through temporary bonding with organic adhesives, using an ultraviolet (UV) wavelength laser to dissolve the adhesives and release the device layers, which are subsequently permanently bonded onto the final product wafer. However, glass substrates are difficult to process with semiconductor fab equipment that have been designed primarily around silicon, and that require costly upgrades to enable glass wafer processing. In addition, organic adhesives are generally limited to processing temperatures below 300°C, which limits their use to back-end processing.

Enabling silicon carriers with inorganic release layers avoids these temperature and glass carrier compatibility issues. In addition, the nanometer precision of IR laser-initiated cleaving opens up the possibility of processing extremely thin device wafers without changing processes of record. Subsequent stacking of such thin device layers enables higher bandwidth interconnects and opens up new opportunities to design and segment dies for next-generation high-performance systems.

Next-generation Transistor Nodes Demand Novel Layer-transfer Proces

At the same time, transistor roadmaps for the sub-3-nm node are calling for new architectures and design innovations such as buried power rails, backside power delivery networks, complementary field-effect transistors (CFETs) and even 2D atomic channels, all of which will require layer transfer of extremely thin materials. Silicon carriers and inorganic release layers support process cleanliness, material compatibility and high processing temperature requirements for front-end manufacturing flows. However, until now, silicon carriers had to be completely removed using grinding, polishing and etching processes, which results in micron-range variations across the surface of the working device layer, making this method unsuitable for thin-layer stacking at advanced nodes.

EVG's new NanoCleave technology utilizes an IR laser and inorganic release materials to enable laser debonding on silicon with nanometer precision. This eliminates the need for glass substrates for advanced packaging, avoiding temperature and glass carrier compatibility issues, and enables the ability to transfer ultra-thin (single micron and below) layers via carriers in front-end processing without changing the processes of record. The nanometer-precision of EVG's new process supports advanced semiconductor device roadmaps calling for thinner device layers and packages, increased heterogeneous integration, and reduced processing costs through thin-layer transfer and the elimination of glass substrates.

Vedanta to set up semiconductors and display fab units in India

In a move that aims to put India on the global silicon map and make the country self-sufficient in the critical area of semiconductors and displays, Vedanta, the world's sixth largest diversified natural resources group, signed two Memorandum of Understanding (MoUs) with the Government of Gujarat to set up a semiconductor fab unit, a display fab unit and a semiconductor assembling and testing unit in the key industrial state, in line with Prime Minister Narendra Modi's vision to make the country a hub of futuristic technologies.

THE PROJECT, which will be taken up by the Vedanta-Foxconn JV announced earlier this year, envisages a total investment of USD 20 Billion and an employment potential of around 100,000 people. Vedanta will hold 60% of the equity in the JV while Foxconn will own 40%. The JV will look at setting up a semiconductor manufacturing plant in the next two years.

The MoU signing ceremony was attended by Union Minister Shri Ashwini Vaishnav, Gujarat Chief Minister Shri Bhupendrabhai Patel, Vedanta Group Chairman Anil Agarwal, Vedanta's Global Managing Director, Display and Semiconductors, Akarsh Hebbar, Mr. Brian Ho, VP, Foxconn Semiconductor Group and a host of other dignitaries. The project will attract electronics ecosystem players across the value chain entailing manufacturers of highly sophisticated and sensitive equipment, materials (high purity Gases, chemicals, wafers, photomasks), equipment service providers etc.

The proposed semiconductor manufacturing fab unit will operate on the 28nm technology nodes and the display manufacturing unit will produce Generation 8 displays catering to small, medium and large applications.

On this occasion, Union Minister for Electronics and Information Technology, Shri Ashwini Vaishnav, said: "The project is in line with Hon. Prime Minister Shri Narendra Modi's vision for achieving self-reliance in the field of semiconductor manufacturing. I congratulate Vedanta and Foxconn for taking this initiative and bringing the semiconductor plant to India." Semiconductors and displays are critical to establishing India as an electronics hub and will help attract suppliers and device assemblers to setup base in India. The Indian semiconductor market was valued at $27.2 billion in 2021 and is expected to grow at a healthy CAGR of nearly 19% to reach $64 billion in 2026.

Speaking on the occasion, Vedanta Chairman Mr. Anil Agarwal, said: "We are delighted to announce that Gujarat will be the location for our display and semiconductor fab ventures. The state is well known globally for being a manufacturing hub and I hope that India's upcoming, cutting-edge electronics ecosystem will thrive, with every state benefitting to develop their electronic manufacturing hubs. We are privileged to take one step further in supporting Prime Minister Modi's vision of aatmanirbhar Bharat in this strategic sector."

The decision to set up the project in Gujarat comes after Vedanta and Foxconn announced in February that they will form a joint venture company in India. Vedanta has a presence in electronics and technology business through group companies Avanstrate Inc. and Sterlite Technologies.

Hon Hai Technology Group ("Foxconn") is the world's largest electronics manufacturer. Hon Hai is also the leading technology solution provider, and it continuously leverages its expertise in software and hardware to integrate its unique manufacturing systems with emerging technologies.

Mr. Brian Ho, VP, Foxconn Semiconductor Group, said, "I am delighted that the semiconductor plant will come up in the industrial state of Gujarat. We applaud the efforts made by the Government of Gujarat, home of Prime Minister Narendra Modi, to attract semiconductor development and upgrade government efficiency. Gujarat is recognized for its industrial development, green energy, and smart cities. The improving infrastructure and the government's active and strong support increases confidence in setting up a semiconductor factory. We look forward to working with our partners and the Gujarat leadership to further enhance the infrastructure required to cater to the ambitious semiconductor project."

The broad plans for a semiconductor unit in India were announced after the COVID-19 pandemic upended global supplies of crucial electronic components used in everything from smartphones to cars. India has vowed to spend $30 billion to overhaul its tech industry and build local chip supply chains to avoid being dependent on foreign producers.

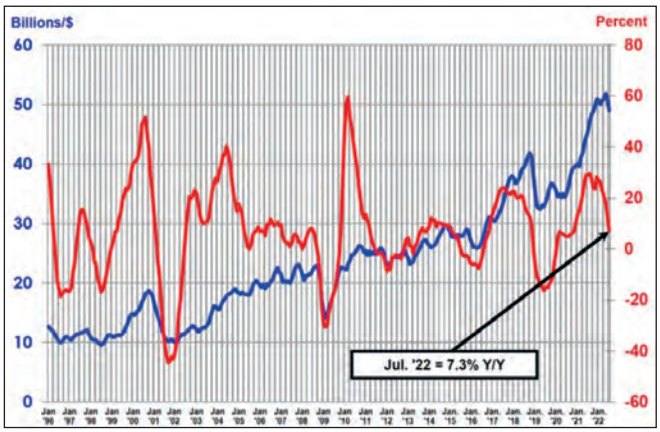
Global semiconductor sales increase 7.3%

The Semiconductor Industry Association (SIA) has announced global semiconductor industry sales were $49.0 billion in the month of July 2022, an increase of 7.3% over the July 2021 total of $45.7 billion, but a decrease of 2.3% compared to the June 2022 total of $50.2 billion

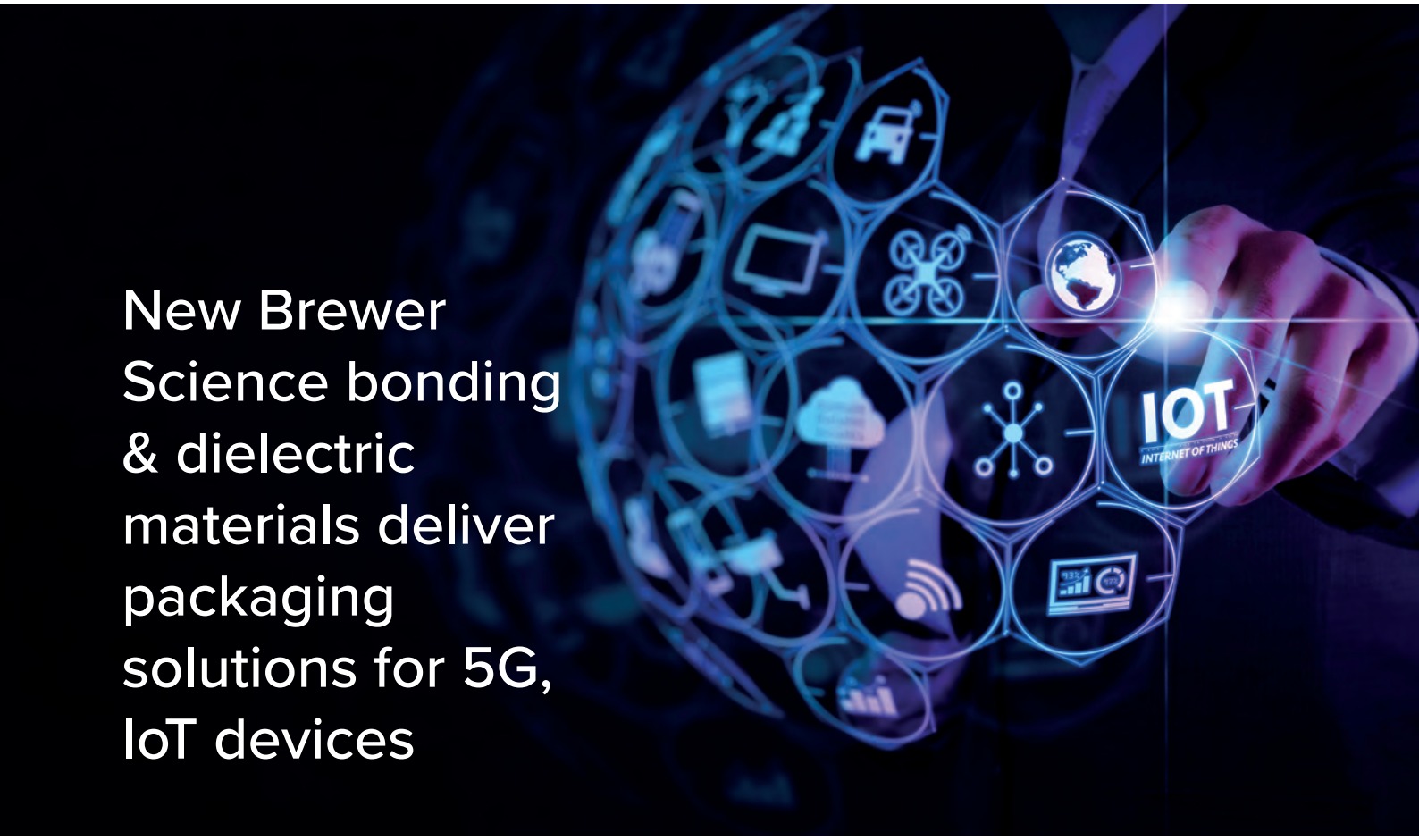
MONTHLY SALES are compiled by the World Semiconductor Trade Statistics (WSTS) organization and represent a three-month moving average. SIA represents 99% of the U.S. semiconductor industry by revenue and nearly two-thirds of non-U.S. chip firms.

"Global semiconductor sales remained strong in July, easily topping the total from last July, but market growth has slowed substantially in recent months, with year-to-year sales increases dropping into the single digits for the first time since December 2020," said John Neuffer, SIA president and CEO. "Sales into the Americas market increased 20.9% year-to-year to lead all regions."

In addition to the Americas, year-to-year sales were up in the Europe (15.2%) and Japan (13.1%), and Asia Pacific/All Other (4.1%), but down in China (-1.8%). Month-to-month sales increased in Europe (2.7%) and Japan (0.6%), but decreased in the Americas (-2.3%), China (-3.5%), and Asia Pacific/All Other (-3.5%).



For comprehensive monthly semiconductor sales data and detailed WSTS forecasts, consider purchasing the WSTS Subscription Package. For detailed historical information about the global semiconductor industry and market, consider ordering the SIA Databook.



New Brewer Science bonding & dielectric materials deliver packaging solutions for 5G, IoT devices

Semiconductor IC packaging techniques include the utilization of 3D integration to increase chip density, maximize performance and reduce power consumption. Brewer Science, a global technology leader in the development and manufacturing of innovative materials and processes, has introduced its latest packaging solutions utilizing a permanent bonding material and a photo-imageable dielectric for the fabrication of cutting-edge semiconductors as well as 5G and IoT microelectronic devices.

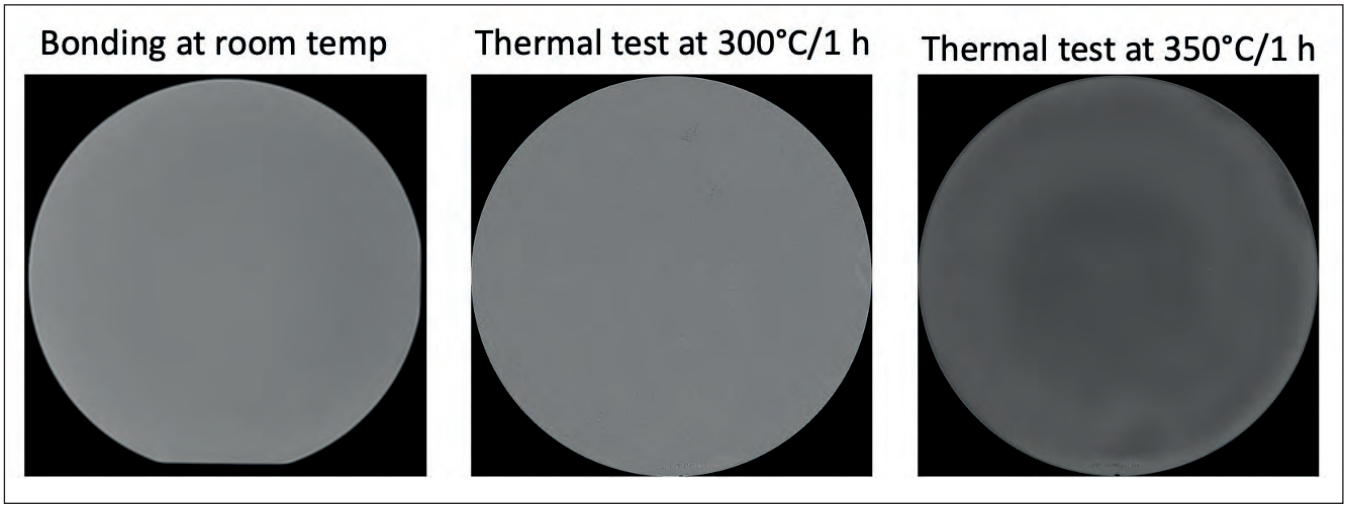
BY BARON HUANG, MEI DONG, AND ZIWEI LIU, BREWER SCIENCE

Permanent Bonding Material with High Thermal Budget

BONDING TWO components together permanently is applied in many fields of advanced packaging to offer a z-axis direction of integration for the fabrication of three-dimensional integrated circuits (3D ICs). Such permanent bonding techniques include direct/fusion bonding, anodic bonding, soldering, and thermocompression. While fusion bonding is still the most frequently used permanent bonding technology in today's semiconductor industry, there is a fast-growing trend for adhesive bonding.

Adhesive bonding, which develops a bond connecting one surface to another using a polymeric material as the intermediate layer, brings significant advantages including: 1) improved design flexibility; 2) good surface planarization and adaptability to surface topography; 3) lower bonding temperature for protecting sensitive components; and 4) better tolerance to particles. With all these merits, adhesive bonding has recently received much attention for microelectromechanical systems (MEMS) packaging and heterogeneous integration to assemble individual IC components such as logic chips, memory chips, and image sensor devices together into high-density, ultra-thin integrated packages. Such modules are needed for high-performance computing applications such as artificial intelligence (AI), data centers, 5G, and high-end mobile products.

Brewer Science previously introduced its first permanent bonding adhesive, the PermaSOL® family of materials, at the European 3D & Systems Summit.



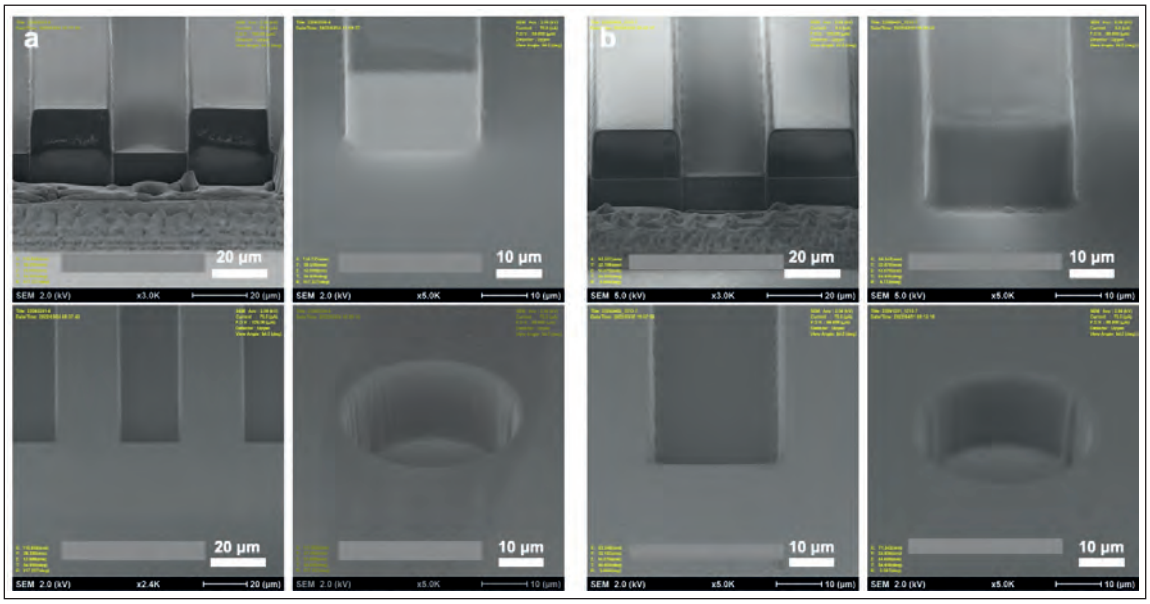
➤ Figure 1. C-SAM images of next generation PBM after bonding at room temperature (left), after thermal testing at 300 °C for 1 hour (center), and after thermal testing at 350 °C for 1 hour (right)

PermaSOL materials were designed to address chip-level and wafer-level packaging requirements by providing reliable bonds with good thermal stability and with low moisture absorption. Brewer Science is now introducing its next generation of permanent bonding materials (PBM) with excellent thermal stability and an improved thermal budget up to 350°C. These materials further provide room temperature bonding with low pressure, low dielectric constant, high chemical resistance, and long shelf life.

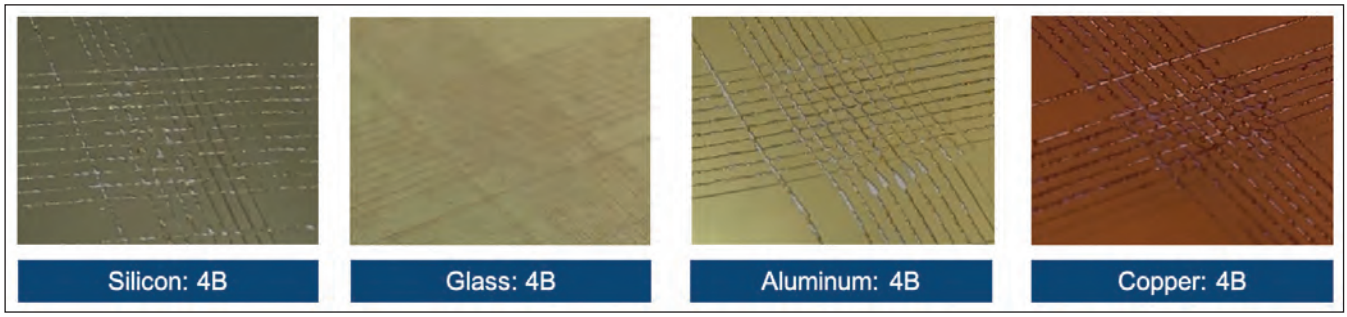
In comparison to benzocyclobutene, a widely used bonding adhesive, the Brewer Science next generation PBM exhibits even lower curing temperature, smaller tensile strength and modulus, and larger CTE. These characteristics make the Brewer Science material a 'super low-stress resin' providing the benefits of low warpage, which brings up promising opportunities for applications on flexible substrates.

Next generation PBM exhibits good thermal stability with a decomposition temperature above 470°C in a nitrogen atmosphere. The bonding can be achieved at 25°C, 2 kN, for 2 minutes, due to the intrinsic flexibility and fluidity of the material.

Figure 1 shows the bonding quality of the next generation PBM characterized by a SONIX Scanning Acoustic Microscope, demonstrating a void-free bondline. After bonding, the adhesive material is solidified via a thermal curing process. The material starts to cure at 160°C. Over 90 percent curing is realized when cured at 250°C for 3 minutes or 220°C for 30 minutes. A high temperature (300°C and 350°C) thermal test was also conducted on the cured material to further investigate its thermal stability. The C-SAM images in Figure 1 shows that next generation PBM has a good thermal budget: defect-free and low shrinkage after heat treatments at 300°C and 350°C for one hour.



➤ Figure 2. SEM/FIB images of (a) low-loss PID material on silicon substrate; (b) low-loss PID material on Ti/Cu substrate



➤ Figure 3. Cross hatch tape peel testing suggests good adhesion of low-loss PID material to various substrates, including Si, Glass, Al, and Ti/Cu surfaces

Low-loss photo-imageable dielectric

With the exploding demand for high-rate data connectivity, new spectrum for 5G mobile networks is being rapidly deployed worldwide. Since 2019, service providers have initiated a race for the 5G market—put another way: the fifth-generation technology standard for broadband cellular networks. Many network operators subsequently reported realizing the fascinating capabilities of 5G, including superior speeds and low latencies, which quickly expanded the number of use cases and further boosts the demand for data and performance.

In this 5G era, there is a growing demand for new materials and new packaging architectures to ensure low signal loss for high bandwidth millimeter wave (mmWave) RF transmission. Also needed is reliable measurements, especially in wafer level packaging, 3D integration, TSV filling, and stress-buffering applications. The 5G spectrum utilizes higher frequencies, which can lead to a greater risk of signal loss.

Photo-imageable dielectric (PID) with low-loss is now in the spotlight, especially for high-speed and high-frequency applications. Various polymeric dielectric materials have been evaluated as PID for packaging high-speed and high-frequency devices, including polybenzoxazole, polyimide, polysiloxane, and epoxy/phenol. However, most of them show a dielectric constant greater than three and with a dissipation factor of around 0.02, which might be fine for the existing applications with frequencies in the sub-6 GHz bands, but cannot meet the requirement and future challenges to be found with frequencies at 60 GHz or beyond for 5G mmWave communication.

Herein, Brewer Science has developed a new low-loss PID material to meet the growing demand for 5G mmWave and IoT applications. The dielectric constant (Dk) for the Brewer Science low-loss PID material is measured to be 2.6 at 10 GHz and at 108 GHz, while the dissipation factor (Df) is 0.0016 at 10 GHz and 0.0041 at 108 GHz. Furthermore, the low-loss PID material can be patterned at low UV exposure dosages, around 300 mJ/cm2; it provides good line/space resolution with an aspect ratio around 1:1; patterned line/space, trench, and via features are shown in Figure 2. A steep sidewall angle close to 90 degrees that is free of footing/rounding is also observed in SEM/FIB images of the low-loss PID material.

Besides the need for a low dielectric constant and loss tangent, additional requirements for the photo-imageable dielectric include strong adhesion, good thermal stability and reliability as well as low moisture uptake, high elongation, low shrinkage, and high photosensitivity. The adhesion quality for the Brewer Science low-loss PID material was examined by crosshatch tape peel testing.

Figure 3 shows the low-loss PID has a good adhesion (4B) to various substrates, including silicon, glass and aluminum as well as titanium and copper surfaces. Other properties of the low-loss PID material are summarized in table 1, which shows the material can meet or even exceed the demands for a wide range of applications for the packaging of high-speed and high-frequency devices.

Summary

This paper introduces a newly developed permanent bonding material (PBM) and a low-loss photo-imageable dielectric (low-loss PID) from Brewer Science. Its general material properties are summarized in Table 1. These materials offer many benefits including excellent thermal stability, low bonding temperature and pressure as well as low Dk and Df in addition to strong adhesion to various substrates. These many beneficial qualities make them attractive candidates to meet the growing demand for 5G and IoT device packaging where reliability, efficiency, and performance are critical to success.

➤ Table 1. Properties of Brewer Science's next generation PBM and low-loss PID materials

Material	Electrical properties		Mechanical properties			Thermal properties			
	Dk (10 GHz)	Df (10 GHz)	Tensile strength (MPa)	Elongation (%)	Modulus (GPa)	CTE (ppm/ °C)	Tg (°C)	Td (°C)	Curing temp (°C)
PBM	2.6	0.0056	28.7	90.9	0.71	113	35.7	470	150
Low-loss PID	2.6	0.0016	12.4	112	0.17	157	85	350	180

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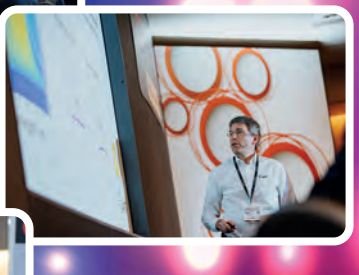


Evolving subfab vacuum challenges demand collaborative solutions

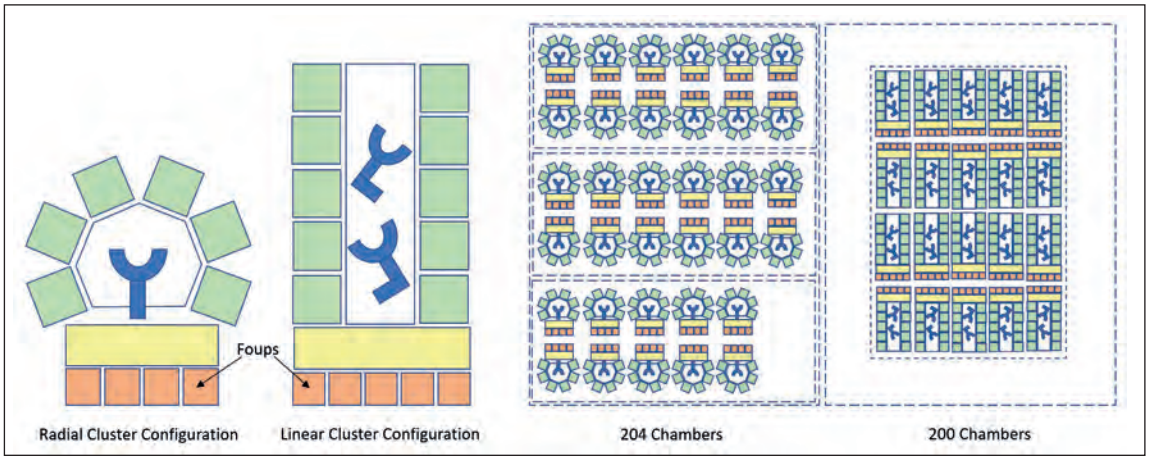
Semiconductor manufacturing is no longer focused on Dennard scaling as a principal means to improve performance and reduce costs. Coordinated, lock-step efforts have given way to a sometimes-bewildering collection of new materials and technologies, often adding complexity in the form of new and different process tools, techniques and chemistries. This evolving IC production environment means manufacturers and suppliers need to collaborate in developing next-generation solutions that positively impact climate change, reduce costs and improve device performance.

BY MATT HALSEY, EDWARDS VACUUM

SEMICONDUCTOR MANUFACTURING technologies continue to diversify at all levels, from device architecture to multi-chip and chiplet integration schemes, through an expanding variety of advanced packaging technologies. Long gone are the days when device manufacturers advanced lock step down a road map focused almost exclusively on shrinking device sizes. Gone too is the luxury of developing a new process tool to meet a widely acknowledged, well defined set of requirements, with the assumption that there would be time to fine tune the design based on customer feedback after the product introduction.

In an environment with multiplying pathways to technical and commercial success, close collaboration between device manufacturers and equipment suppliers will acquire increasing importance as both seek to hasten development cycles, reduce time-to-market for new products, and target new products more precisely on key applications.

These same pressures apply in the subfab as well, where exist the essential systems that support the process tools above. Most semiconductor manufacturing processes require a vacuum; consequently, loss of that vacuum will take down a production line just as surely as a failure in the tool itself. Integrating new processes and materials into the production line must include careful consideration of the impacts on the vacuum systems tasked with removing excess gases and byproducts from the tools. Failure to do so will inevitably lead to more frequent maintenance, shorter service lifetimes and reduced reliability. In the worst case, it will result in unplanned down time with all its associated costs.



➤ Figure 1 shows how cluster tools might be reconfigured from the traditional radial layout to linear. The tools (and the pumps below) occupy less space, but the required pumping capacity remains the same.

In addition to changes in processes and materials, vacuum challenges in the subfab include shrinking space, increasing energy costs, and growing concern about the sustainability of the manufacturing process. Many of the design choices will require carefully balanced trade-offs among conflicting requirements.

The Process

The ever-increasing capital cost of new manufacturing capacity at advanced process nodes exerts relentless pressure on manufacturers to increase throughput in order to amortize higher fixed costs over a larger product output. For vacuum systems, higher throughput usually means higher flow rates and larger pumps.

Changes in process chemistry include the use of more aggressive reactions with harsher chemicals which require more resilient pumps. Pumps must incorporate materials and coatings that can withstand process gases and their by-products, as well as the corrosive chemicals used to clean process chambers.

Higher (and sometimes lower) temperatures for critical processes like atomic layer deposition and chemical vapor deposition require pumps that can handle the greater temperature range. Tolerances for rapidly spinning rotors are very tight and thermal expansion must be carefully managed. Materials used for seals at more conventional temperatures may not withstand higher temperatures. Often the temperature profile of the pump and associated piping must be carefully managed to avoid deposition of condensable materials.

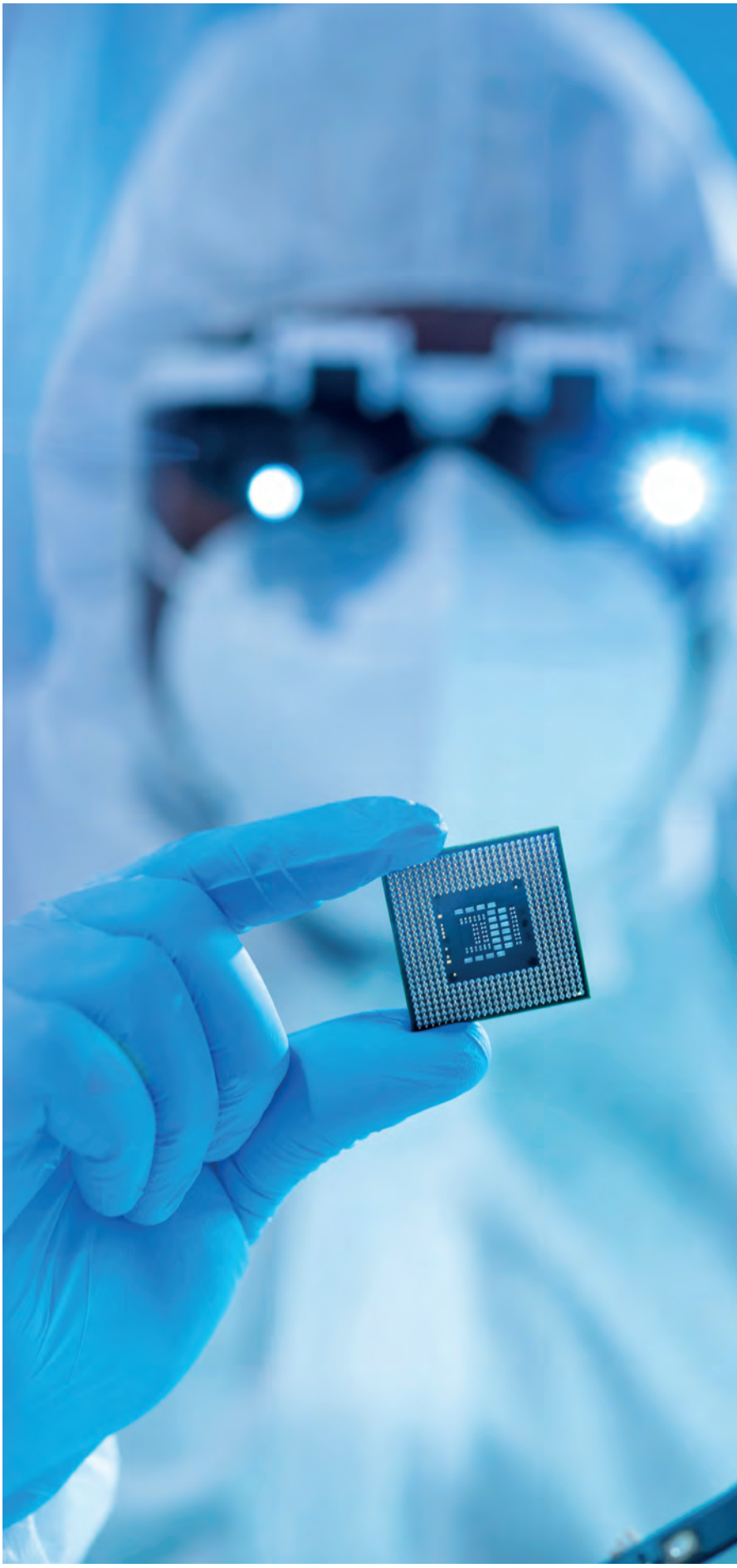
Subfab space

Demands for higher throughput are leading manufacturers to put more smaller tools in less space in the fab. Following the convention that supporting systems must fit within the footprint of the process tool as projected down to the subfab, pumps and abatement must also fit in less space while handling increased flows. This can be especially challenging for pumps where the physical size of the pump has a direct relationship to its pumping capacity. Fab operators are currently looking for a 20-30% reduction in pump footprint, just to keep up with decreasing tool size. Stacking pumps in the subfab offers one solution, but there are limits related to safety and maintenance concerns.

Figure 1 shows how cluster tools might be reconfigured from the traditional radial layout to linear. The tools (and the pumps below) occupy less space, but the required pumping capacity remains the same.

Utility costs

Semiconductor manufacturing is energy intensive. The energy invested in a completed device can be



5.4 MJ (1.5 kWh) or more per square centimeter. Power is expensive and prices are increasing. Manufacturers are demanding more energy efficient systems, often for the simple reason that it reduces operating costs, with a sustainability aspect secondary to this.

Unfortunately, the desire for reduced energy consumption often conflicts with the need for increased pumping speed and pump temperature. Vacuum pumps do mechanical work, and, in the simplest analysis, more work takes more energy. The problem is exacerbated in harsh applications where additional power may be required to overcome resistance caused by material deposition within the pump or heavy particle loads in the process exhaust stream.

Implementation of idle mode technologies that reduce power consumption when the supported tool is not operating promise some relief; but again, harsh processes pose a specific challenge to vacuum systems where a halted pump may be difficult to restart reliably in the presence of deposition buildup and high particle loads.

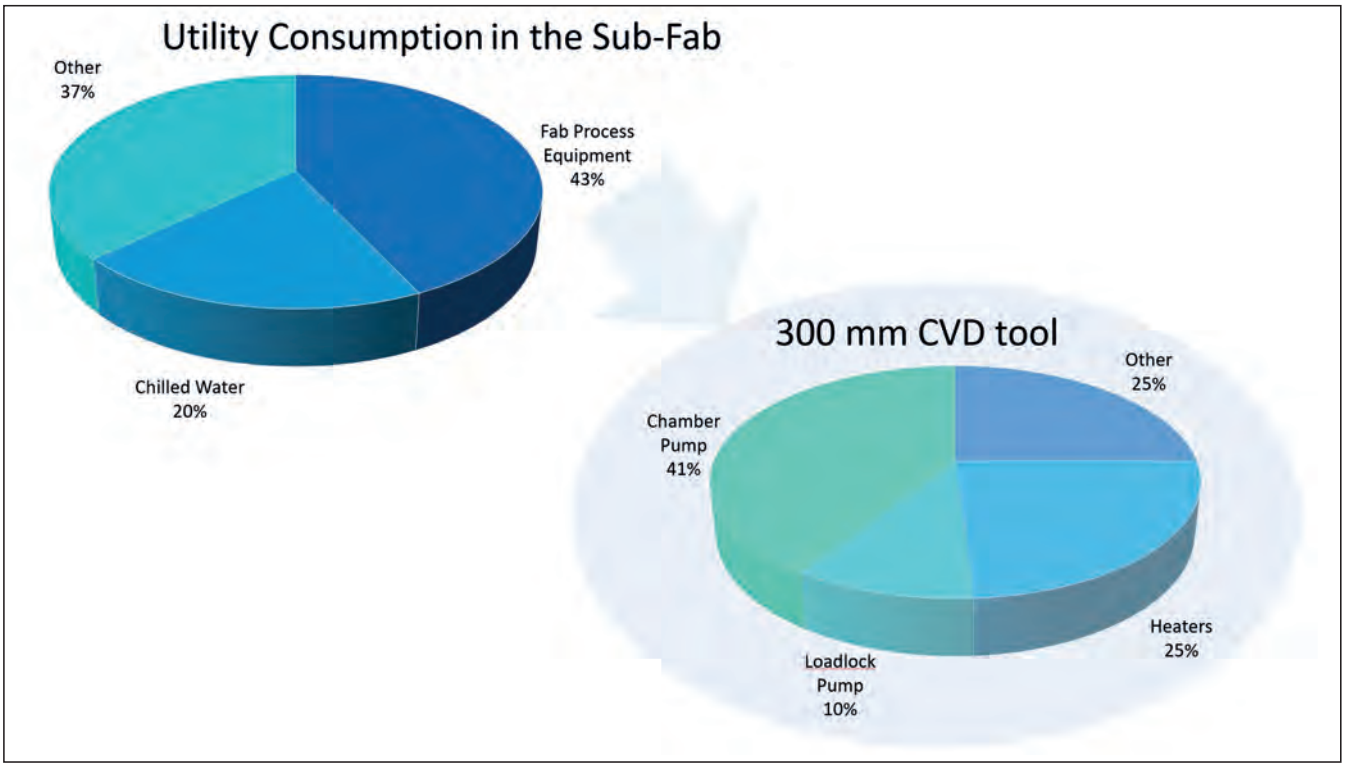
The urgency of power concerns varies somewhat by region; power availability in Taiwan is severely restricted and energy efficiency is a high priority. In Europe, energy prices have soared recently, largely as a result of the war in Ukraine and the heavy reliance on natural gas as an energy source across the EU. Geopolitical tensions seem unlikely to diminish in the near term, adding additional pressure to demands for energy efficiency.

Sustainability

There is now a complete consensus within the scientific community that our environment is warming and that the warming is the result of human activity. Every industry, including semiconductor manufacturing, has an obligation to do everything possible to reduce the carbon emissions that are the primary cause of warming. Relative to some industries, semiconductor manufacturing is not a large direct emitter of greenhouse gases (GHG). But manufacturing ICs does consume vast amounts of energy, most of which currently comes from burning fossil fuels. The solution lies ultimately in the conversion of power generation to renewable sources, and as an industry with significant financial and political influence, we must advocate for that conversion.

However, the greatest potential for short-term reductions in GHG emissions lies in reducing our power consumption by improving our energy efficiency and minimizing the use of supporting utilities, all of which cost energy to produce.

Some of the trends we have mentioned work against reducing power consumption, such as the need for higher flow rates and temperatures. Fortunately, the most powerful influence – the always present drive to reduce costs – aligns directly with the environmental imperative to reduce power consumption. This powerful combination has driven broad commitment across the industry to embrace principles of environmental stewardship. As part of the Atlas Copco Group, Edwards Vacuum has signed on to the Science Based Target Initiative,



➤ Figure 2 In this example from an ISMI study, more than half of the power consumed by a CVD process tool is attributed to vacuum generation.

which commits participants to take all possible actions to limit global warming to less than 2°C. SEMI, our industry association, has updated its guidance (S23) to semiconductor manufacturers and equipment manufacturers to provide a basis for measuring energy consumption that will facilitate comparisons and encourage greater efficiency.

Vacuum requirements vary greatly from process to process. Some, like plating and chemical mechanical polishing, require no vacuum. Some, like EUV lithography and atomic layer deposition, require constant turnovers of chamber gases under vacuum conditions. Figure 2 shows an example taken from an ISMI Fab and Equipment Energy Study showing the power consumption attributed to a chemical vapor deposition (CVD) tool.

Most estimates allot something like 40% of overall fab power consumption to process equipment. In the case of CVD, over half of that power goes to creating and maintaining vacuum - 41% for chamber vacuum provided by dry pumps in the subfab and another 10% for the load lock pump on the tool itself. This is consistent with estimates that put power consumption for process vacuum at 20% of overall energy usage in semiconductor manufacturing. Clearly, improvements in the energy efficiency of vacuum systems can make a significant contribution to energy savings. Demands to take verifiable action to support sustainability goals is mounting throughout the supply chain and in capital markets. Downstream companies, especially consumer-facing companies, are under mounting pressure from customers to enhance their sustainability.

This ripples up the supply chain where subfab equipment can be a critical enabler. In an internal study at Edwards, we found that 97% of all GHG emissions (carbon dioxide equivalent) generated over the lifetime of a vacuum pump, including all inputs (power, water, cooling, nitrogen, etc.) from initial manufacture to final disposal, comes from energy consumed during use, which makes reductions in these emissions a primary target for equipment manufacturers.

Summary

Semiconductor manufacturers and their equipment suppliers face a constantly evolving array of often conflicting design and development priorities. Tightly coordinated advances toward the monolithic goal of smaller transistors has given way to a sometimes-bewildering collection of new materials and technologies.

In this environment it is more important than ever for equipment and device manufactures to collaborate closely in developing the next generation of solutions, working together to gain a better understanding of these evolving challenges from those who must live with them every day.

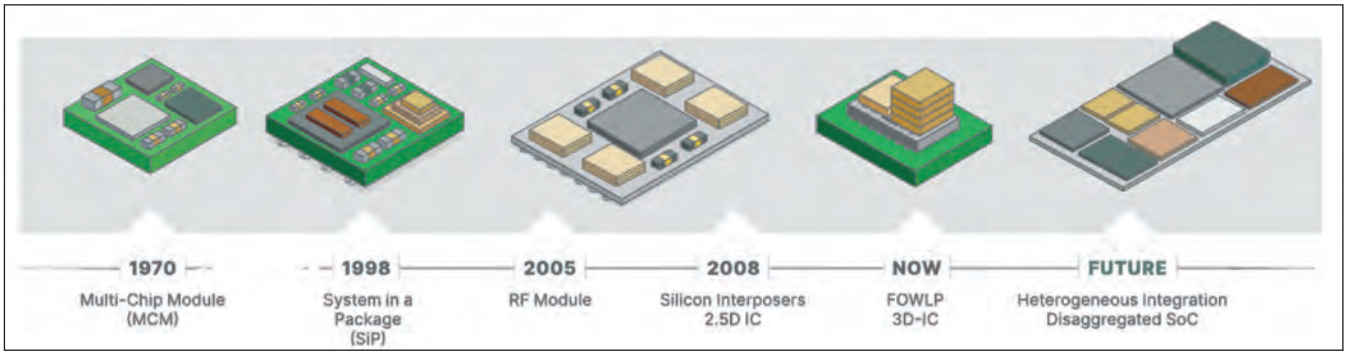
Onto Innovation's 'XL' fine resolution large field lithography dramatically cuts FOPLP pattern distortion

Heterogeneous integration enables multiple chips from varying Silicon processes to deliver superior performance. In large panel packages, present day limits on exposure field size forces manufacturers to 'stitch' together multiple reticles, which slows throughput and increases costs. Onto Innovation's new JetStep® X500 system dramatically increases the exposure field up to 250 x 250 mm, slashing the number of exposures needed and cutting costs in FOPLP applications.

BY JOHN CHANG, COREY SHAY, JAMES WEBB AND TIMOTHY CHANG,
ONTO INNOVATION INC.

HIGH-PERFORMANCE compute, 5G, smartphones, data centers, automotive, artificial intelligence (AI) and the Internet of Things (IoT) – all rely on heterogeneous integration to achieve next-level performance gains. By combining multiple silicon nodes and designs inside one package, ranging in size from 75mm x 75mm to 150mm x 150mm, heterogeneous integration is one factor bringing us closer toward an era in which technology is beneficially embed into nearly all aspects of our lives whether it's in the smart factories where we work, the self-driving cars that navigate the cities in which we live, the mobile devices that connect us to each other and the wearable devices that help us live healthier lives.

Regardless of the speed to which we are approaching this promising new era, this transition comes with increasing challenges, ones that are constrained by increasingly stringent requirements. The next-generation of heterogeneous integration technologies, and the fan-out, panel-level packaging that often accompanies it, will demand even tighter overlay requirements to accommodate larger



➤ Figure 1. Heterogeneous integration enables next-generation device performance gains by combining multiple silicon nodes and designs inside one package, so the package size is expected to grow significantly. (Source: Cadence)

package sizes with fine-pitch chip interconnects on large-format, 510mm x 515mm flexible panels. (Fig 1)

As redistribution layers (RDL) are added, these processes may cause stresses to both the surface and inside of the substrate, stresses that may cause warpage and formation change. If the substrate suffers deformation from high pressure, high temperature or other process steps, the deformation can cause a pattern shift from the nominal position and affect the overlay results in the lithography process on large-format panels. If left uncorrected during the exposing process, these factors can result in serious overlay errors.

Adding to these challenges, advanced packages will soon require a resolution of 1µm, while advanced integrated circuit substrates (AICS) will require a resolution of 3µm. In addition, the budget for overlay is getting tighter due to the fine resolution process. In the case of AICS, the typical overlay yield is about 95% to 97% per layer.

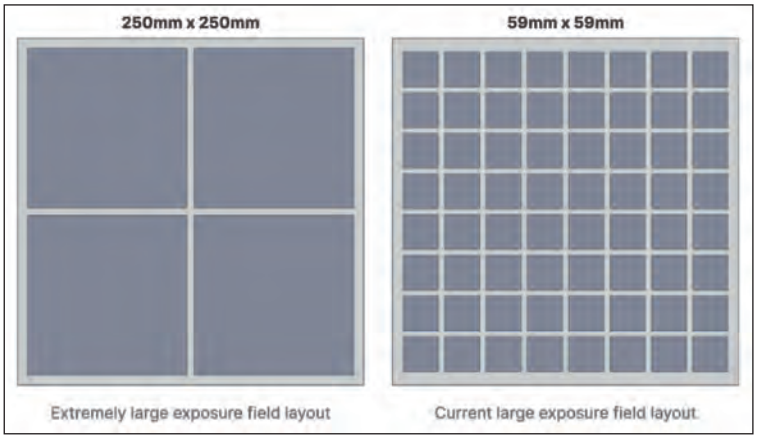
How might an extremely large exposure field, fine-resolution lithography system deal with these heterogeneous integration challenges? To better understand the capabilities of such a tool, in this case Onto Innovation's JetStep® X500 system, we examined the use of metrology data from the lithography system, combined with overlay analysis algorithms, to identify the error terms and distortion components of the test vehicle and find a solution/strategy to correct the errors. Designed specifically for the demands of high-volume manufacturing, this new lithography technology meets these challenges and successfully demonstrates how its users can achieve the stringent overlay requirements posed by heterogeneous integration.

The Trouble with Stitching

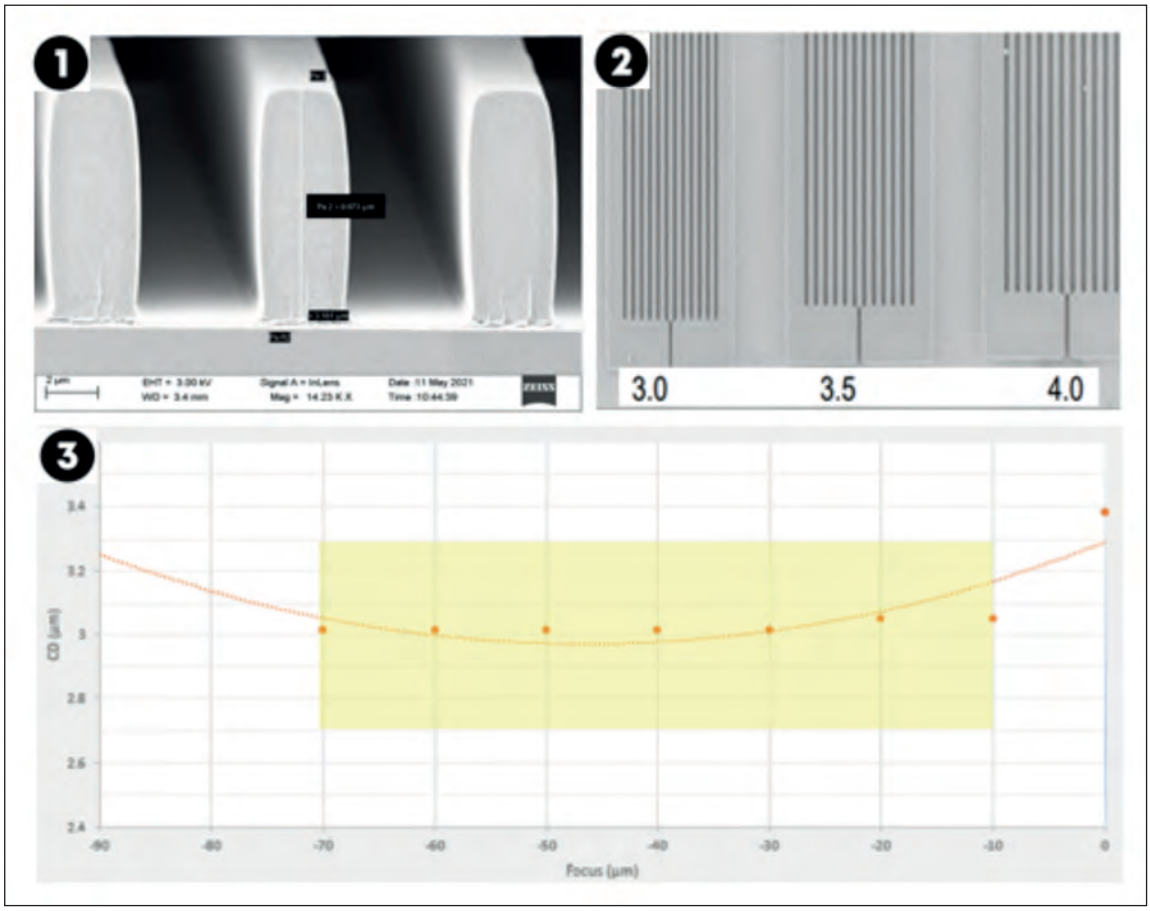
Heterogeneous integration requires the integration of multiple chips into a single 75mm x 75mm or 150mm x 150mm package for increased functionality, a challenge for today's advanced packaging steppers, which have a limited exposure field of 59mm x 59mm. For most steppers, processing these two large package sizes requires the use of multiple exposure shots to complete a package because of the limited exposure field size. This method, known as "stitching," requires multiple reticles and has low throughput, which increases costs. However, increasing the stepper field size to sizes larger than 150mm x 150mm removes the need for stitching and increases throughput significantly.

While it takes 64 shots for current advanced packaging steppers with an exposure field of 59mm x 59mm, a stepper with an extremely large exposure field can expose a panel with just four (4) shots, an achievement that eliminates the need for image stitching and exceeds the overlay and critical uniformity requirements for these packages. (Fig 2)

The 250mm x 250mm exposure field offered by the JetStep X500 system allows the user to process one or more large packages in a single shot and requires fewer shots to complete a substrate. This offers a significant throughput increase over regular exposure fields. This extremely large exposure field, fine-resolution lithography system is equipped with a 2.2x magnification projection lens, which enables



➤ Figure 2. The layout of an extremely large exposure field (250mm x 250mm) and a regular exposure field (59mm x 59mm) on a 510mm x 515mm panel. With the extremely large exposure field, a panel can be completed with just four (4) shots; with a current large exposure field, a panel requires 64 shots to complete.



➤ Figure 3. Extremely large exposure field, fine-resolution lithography system resolution performance: 1. Cross section copper seed wafer image of 3µm line/space with 10µm thick dry film resist, which is a 1:3.3 aspect ratio. 2. Isolated and dense area resolution results of 3µm, 3.5µm and 4µm line/space. 3. Bossung curve of 3µm line/space with a 10µm-thick dry film resist. The X axis is focus (µm), and the Y axis is CD (µm). A 60µm depth of focus is observed in 3µm line/space with 10µm-thick dry film resist.

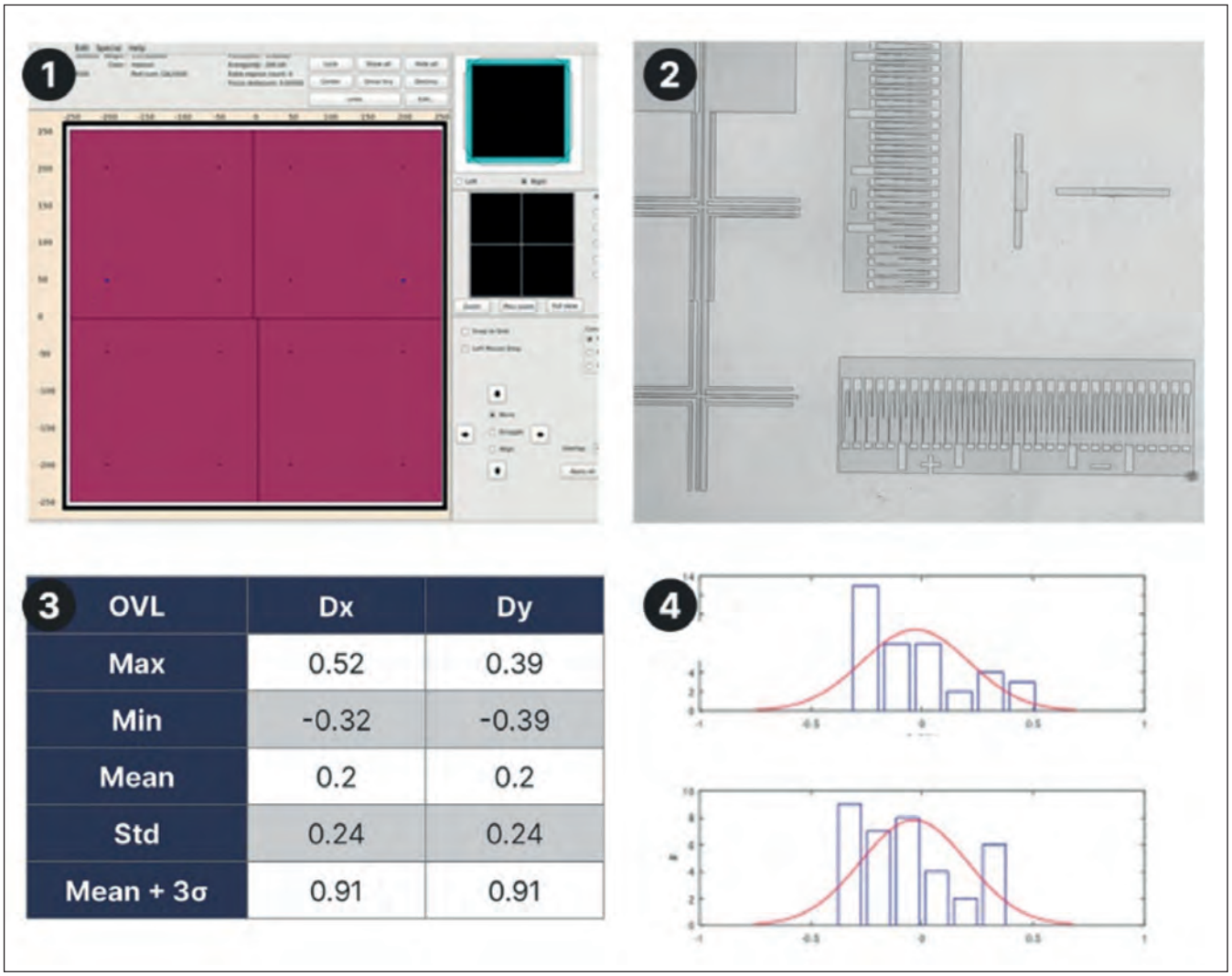
exposure fields up to 250mm x 250mm, and offers 3µm line/space resolution. In addition, the system has ±400ppm magnification compensation and ±100ppm anamorphic magnification compensation, with an overlay of < 1µm.

In order to demonstrate the resolution performance of this lithography system, we selected a copper clad laminate (CCL) and Ajinomoto build-up film (ABF) substrate with 10µm-thick dry film resist. As seen in Fig 3, in only four shots the lithography system demonstrated a line/space resolution of 3µm, while offering a depth of focus up to 60µm, an indication that the extremely large exposure field, fine-resolution lithography system is suited for the high-volume manufacturing needs of larger package sizes with fine-pitch chip interconnects on large-format panels.

In order to test the overlay performance of the lithography system, we selected a 510mm x 515mm glass panel with 1.4µm liquid resist. The test vehicle was run with a site-by-site correction method at four (4) shots per panel to build the second layer (Fig 4). We then checked the overlay error between layer 1 and layer 2 to determine its performance. The overlay error was determined by reading the location of overlapped verniers.

Each exposure field contains 3 x 3 measurement points, and 2 x 2 shots a panel were measured to determine the overlay performance of the lithography system. According to our overlay performance analysis, the extremely large exposure field, fine-resolution lithography system demonstrated a deviation X mean +3 sigma of 0.91µm and a deviation Y mean +3 sigma of 0.91µm. These numbers indicate an extremely large exposure field, fine-resolution lithography system can achieve the aggressive overlay number of less than 1µm that will be required for advanced packaging.

Each exposure field contains 3 x 3 measurement points, and 2 x 2 shots a panel were measured to determine the overlay performance of the lithography system. According to our overlay performance analysis, the extremely large exposure field, fine-resolution lithography system demonstrated a deviation X mean +3 sigma of 0.91µm and a deviation Y mean +3 sigma of 0.91µm



OVL	Dx	Dy
Max	0.52	0.39
Min	-0.32	-0.39
Mean	0.2	0.2
Std	0.24	0.24
Mean + 3σ	0.91	0.91

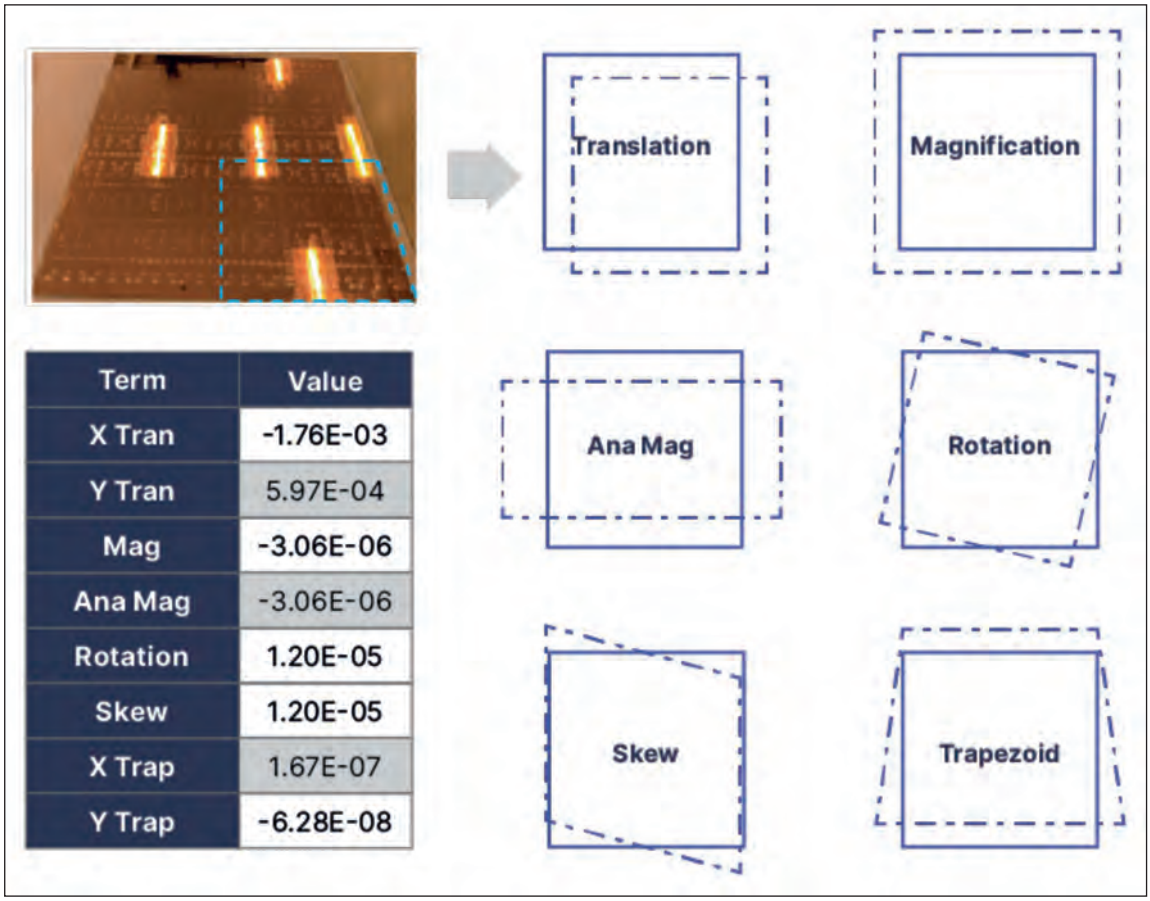
➤ Figure 4. The overlay performance of the extremely large exposure field fine-resolution lithography system: 1. Exposure layout for overlay demonstration, with four (4) shots per panel at 250mm x 250mm a shot. 2. Overlapped verniers built by the first layer and second layer: the overlay performance was determined by reading the verniers. 3. Overlay statistics table. 4. Dx and Dy distribution chart: the mean is close to center, and no peak distribution is observed.

Correcting Overlay Errors

To demonstrate the ability of the extremely large exposure field, fine-resolution lithography system to correct errors on the substrate, we used the system's intra-field correction and global correction capabilities. The system's global correction capabilities offer translation, rotation, scale and orthogonality corrections, while the system's intra-field correction capabilities offer translation, rotation, magnification, radial distortion and trapezoid corrections. By combining global and intra-field correction capabilities, we were also able to test anamorphic magnification and skew corrections.

The stepper uses a reflective alignment system (RAS), which can recognize the alignment mark on the substrate, and grid stage information; which pairs with RAS to identify the pattern deviation of the substrate. The metrology data generated by the lithography system was combined with the following algorithms: a propriety algorithm and Dolana. These four exposure shots of the stepper then were analyzed for error terms and distortion components. With metrology data collected by the lithography system and analyzed by the Donala algorithm, we identified error terms and distortions in the test vehicles (Fig 5). In addition, we identified anamorphic pincushion and third radial distortion when describing errors in a full-panel model; however, the error terms change when fitting in a quadrant of the panel (lens field). The error terms change to include translation, magnification, anamorphic magnification, rotation, skew and trapezoid.

For each quadrant of the 510mm x 515mm panel, we found various error terms and distortion signatures, indicating that a global solution correction cannot fully correct test vehicle error and distortion; a unique correction is needed for each quadrant to correct the unique errors during exposure. By doing this, we were able to achieve successful overlay

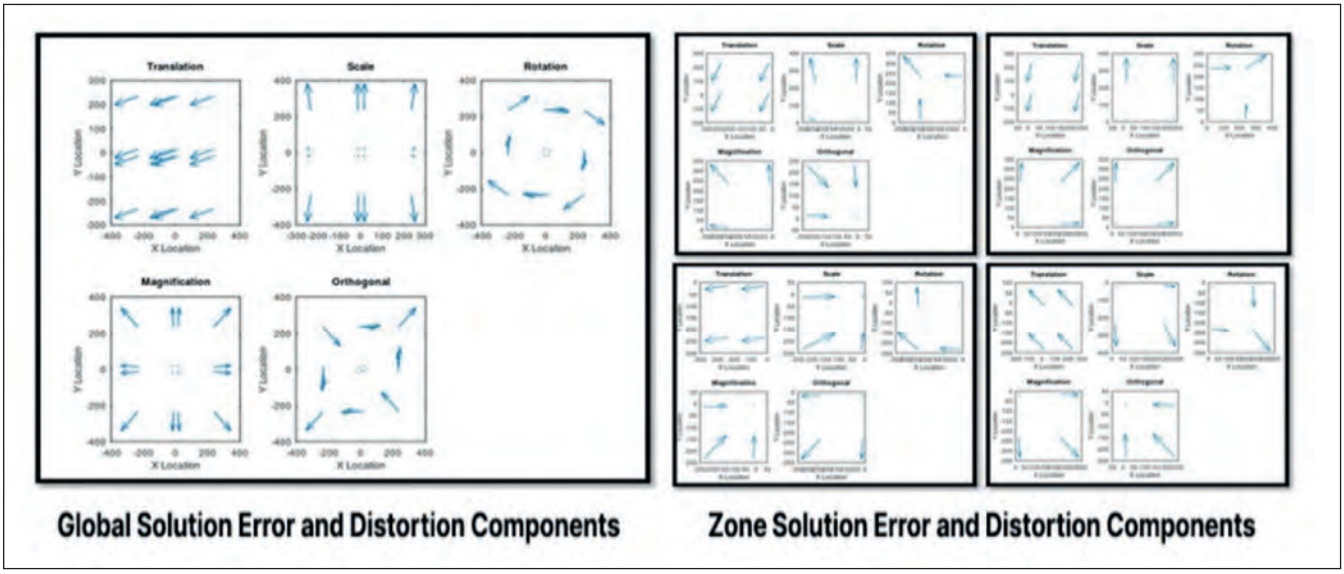


Term	Value
X Tran	-1.76E-03
Y Tran	5.97E-04
Mag	-3.06E-06
Ana Mag	-3.06E-06
Rotation	1.20E-05
Skew	1.20E-05
X Trap	1.67E-07
Y Trap	-6.28E-08

➤ Figure 5. Error terms and distortion components are identified in a quadrant of a 510mm x 515mm test vehicle. The numbers in the table are the coefficients used in the equations of the algorithm that describe each term fit.

results. Fig 6 shows vector maps for global solution corrections and zone solution corrections; these two vector maps are from the same test vehicle. According to the vector maps, global solution translation corrections show that translation errors vector toward the down-left direction, but in the bottom-right quadrant of the zone correction solution, the translation errors vector toward the upper-right direction, which is the opposite direction of the global solution correction. Other correction components can be observed in different directions or trends in each quadrant.

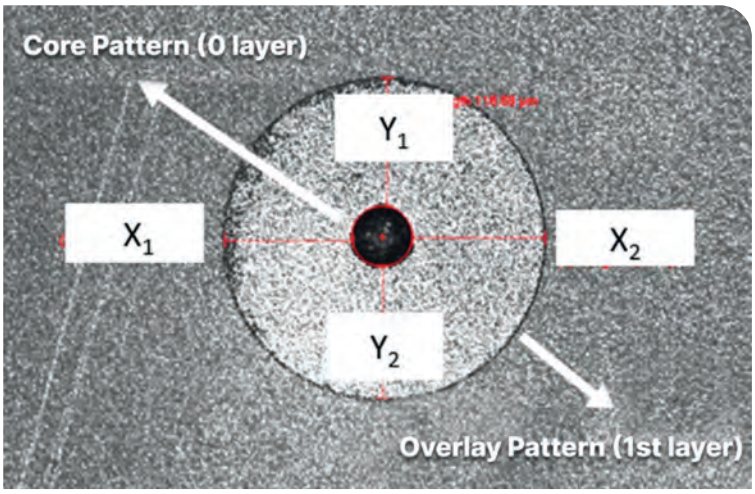
The test vehicle was processed with liquid film. Using the lithography system, combined with a proprietary algorithm, corrections were generated for each quadrant of the test vehicle. The corrections were used during exposure, and then



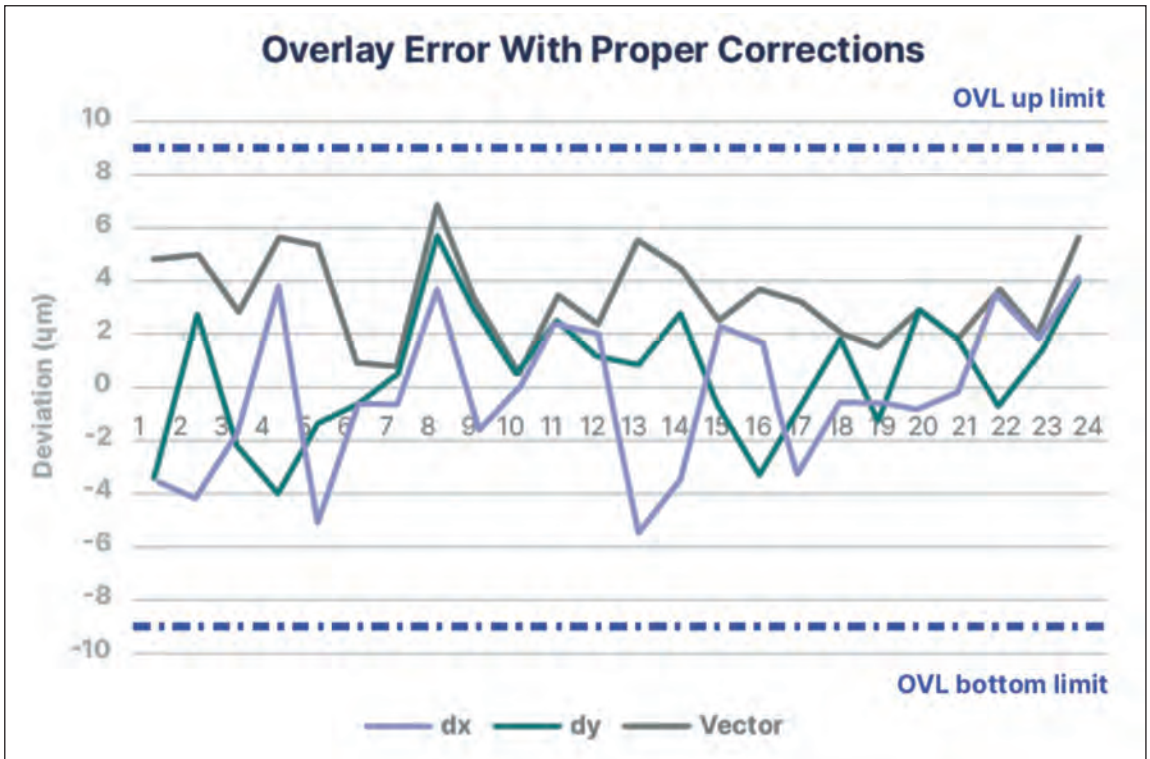
➤ Figure 6. Global solution correction vs. zone solution correction.

the test vehicle was taken to development. Overlay measurements were taken by optical microscope using measurement software, with six (6) measuring points per zone, four (4) zones per panel, totaling 24 measuring points per sampling. Four (4) measuring points were at the four (4) corners, the top-right, top-left, bottom-right and bottom-left corners. Two (2) measuring points were at the center of the zone. These measuring points were used to verify the overlay results of the entire area of the test vehicle. Fig 7 describes how the overlay deviation X, deviation Y and vector were defined.

Fig 8 shows the overlay results of the test vehicle. The deviation X maximum is 5.42µm and shifts right; the deviation Y maximum is 5.72µm and shifts upward. Based on the substrate provider database, if the distortions and errors are recognized well and corrected properly, the final overlay error can be expected to be less than 10µm. The final overlay error vector results are less than 7µm, and dx and dy values are within ±6µm. This indicates that the errors

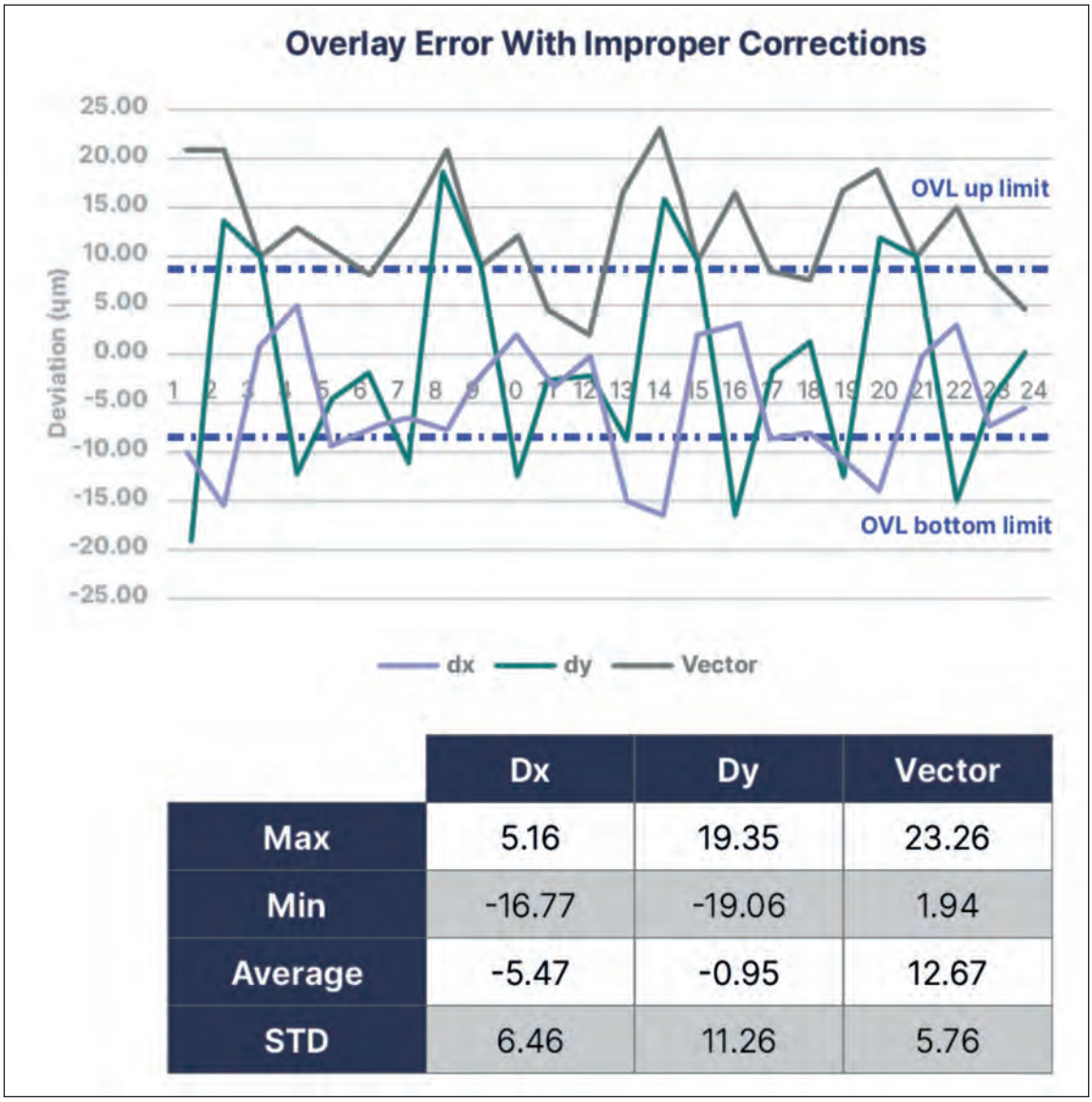


➤ Figure 7. Overlay measuring method to determine the overlay dx, dy and vector. Center black spot is core pattern, the bigger circle is of the overlay pattern, dx = X1-X2, dy = Y1-Y2 and error vector = (dx2+dy2).



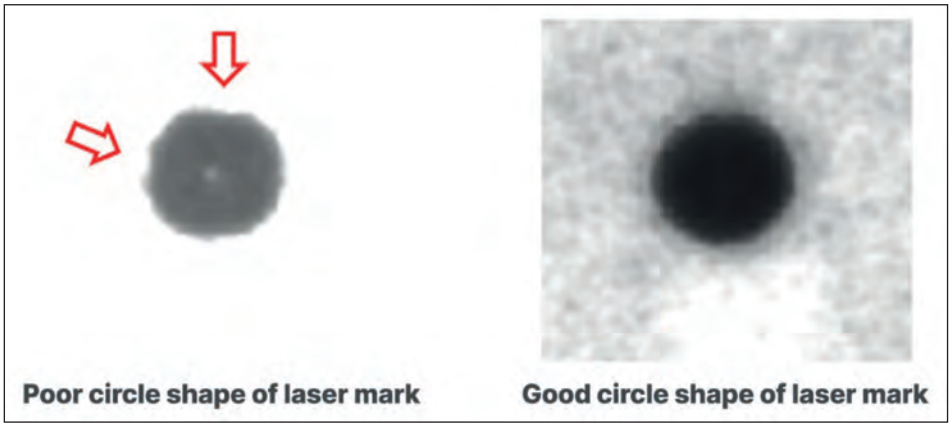
	Dx	Dy	Vector
Max	3.94	5.72	6.94
Min	-5.42	-3.94	0.58
Average	-0.24	0.57	3.37
STD	2.89	2.47	1.74

➤ Figure 8. Test overlay results with proper corrections and method. The unit of measurement is µm. Overlay pattern, dx = X1-X2, dy = Y1-Y2 and error vector = (dx2+dy2).



	Dx	Dy	Vector
Max	5.16	19.35	23.26
Min	-16.77	-19.06	1.94
Average	-5.47	-0.95	12.67
STD	6.46	11.26	5.76

➤ Figure 9. Overlay results using improper corrections and method. These numbers indicate that improper corrections and method were applied during exposure resulting in poor overlay. The unit of measurement is µm.



➤ Figure 10. Alignment marks by laser drill system. The left figure has a poor shape compared to the right figure. This situation could result in alignment solution errors and affect final overlay. Alignment marks could contain one or multiple laser marks.

and distortions of the test vehicle were recognized correctly and corrected as expected. If the errors and distortions were not corrected properly, the overlay error vector could be 20µm or higher. (Fig 9) We observed translation, rotation, scale, magnification, anamorphic magnification, skew, trapezoid and orthogonality errors in the test vehicle.

These errors needed to be corrected by a lithography tool to achieve better overlay results. In addition, we also observed various trending errors and distortion

signatures in each quadrant of the 510mm x 515mm panel. These observations indicate that a zone solution correction should be applied during exposure to enable better overlay results.

Analysis indicates that reasonable overlay results can be achieved by using proper corrections and zone solution corrections. However, better overlay numbers are to be expected when using yield predictions derived by the proprietary algorithm.

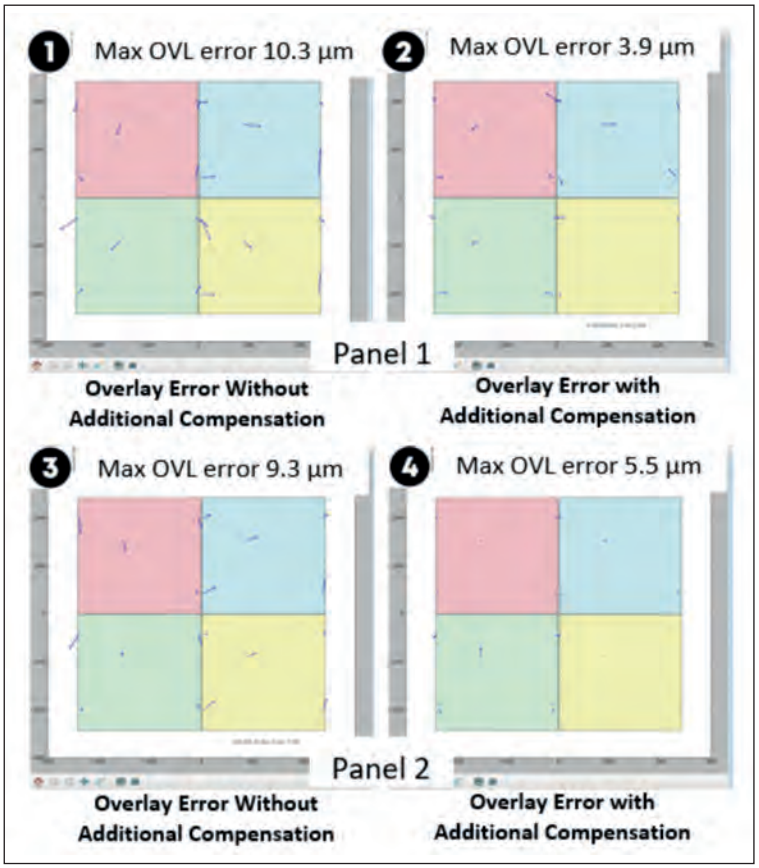
The 510mm x 515mm panel test vehicle was made using the AICS FOPLP process; the alignment marks on the test vehicle were created by a laser drill system (Fig 10). Due to the limitations of the laser drill system, we expected and observed lower accuracy and poor laser mark shape control, leading to an alignment solution error.

This alignment solution error can result in overlay errors, even though the lithography system or metrology system recognizes the alignment marks. Based on this finding, an additional offset may be needed to address this issue.

To address alignment solution errors, additional compensation by zone dimension is proposed. A proprietary algorithm was used for predicting the overlay results with additional compensation. The algorithm was used for analyzing the correctable terms based on current overlay errors.

Following the removal of correctable errors, we predicted the final overlay results. Fig 11 shows the overlay results with and without additional compensation. Based on our predictions, overlay error can be reduced by 4µm or more.

As a result of heterogeneous integration and high-performance requirements, resolution soon will be down to 1µm in advanced packaging and 3µm in AICS. In addition, the budget for overlay is getting tighter due to the fine resolution process. In AICS,

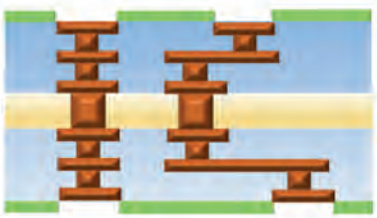


➤ Figure 11. The overlay error with and without additional zone compensation. The prediction results indicate additional compensation can reduce overlay error.

Yield Threshold	97%	
	Yield	Yield Loss
Layer1	97.00%	3.00%
Layer2	94.09%	5.91%
Layer3	91.27%	8.73%
Layer4	88.53%	11.47%
Layer5	85.87%	14.13%
Layer6	83.30%	16.70%
Layer7	80.80%	19.20%
Layer8	78.37%	21.63%
Layer9	76.02%	23.98%
Layer10	73.74%	26.26%
Layer11	71.53%	28.47%
Layer12	69.38%	30.62%
Layer13	67.30%	32.70%
Layer14	65.28%	34.72%
Layer15	63.33%	36.67%

Yield Threshold	98%	
	Yield	Yield Loss
Layer1	98.00%	2.00%
Layer2	96.04%	3.96%
Layer3	94.12%	5.88%
Layer4	92.24%	7.76%
Layer5	90.39%	9.61%
Layer6	88.58%	11.42%
Layer7	86.81%	13.19%
Layer8	85.08%	14.92%
Layer9	83.37%	16.63%
Layer10	81.71%	18.29%
Layer11	80.07%	19.93%
Layer12	78.47%	21.53%
Layer13	76.90%	23.10%
Layer14	75.36%	24.64%
Layer15	73.86%	26.14%

	Yield Increased
Layer1	1.00%
Layer2	1.95%
Layer3	2.85%
Layer4	3.71%
Layer5	4.52%
Layer6	5.29%
Layer7	6.01%
Layer8	6.70%
Layer9	7.35%
Layer10	7.96%
Layer11	8.54%
Layer12	9.09%
Layer13	9.60%
Layer14	10.08%
Layer15	10.53%



➤ Table 1. Overlay yield table. In this table, the original yield threshold is set to 97%. The final yield loss is 16.7% with six (6) layers of packaging; yield then improved to 98%. The final yield loss is 11.42%, with a 1% improvement to yield; final yield increased 5.29%. The right figure is an example of six (6) layers packaging.

the typical overlay yield is about 95% to 97% per layer (Table 1). A 97% yield threshold is selected for lithography process; this means a 3% yield loss per layer. With six (6) layers in packaging, a 16.7% yield loss can be expected. With an improved yield of 1%, a yield improvement of 5.29% can be expected.

Conclusion

Based on the data we obtained, an extremely large exposure field, fine-resolution lithography system can achieve 3µm resolution and is able to achieve a mean overlay of +3 sigma less than 1µm.

The data also indicates that an extremely large exposure field, fine-resolution lithography system can successfully identify error terms and distortion components in a 510mm x 515mm CCL+ABF stacked panel and correct these to achieve good overlay. According to the analysis and discussion in this study, we understand that proper error and distortion corrections, zone solution correction and additional compensation are key to achieving the best overlay numbers in FOPLP.

In the next few years, with resolution becoming smaller and overlay budgets growing tighter, overlay control will become more important in heterogeneous integration. This study provides users with a path to achieve aggressive overlay requirements.

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EDWARDS

Next-generation low-k films can address present, future fabrication challenges

Smaller transistors packed more tightly into ever-shrinking packages are characteristic of new DRAM or logic devices. But greater density can also produce crosstalk and isolation issues. The experts at Lam Research explain how tunable, low-k films deliver upgraded dielectric performance that can have tremendous strategic leverage at the most fundamental level of IC development, both today and tomorrow.

BY AARON FELLIS, VICE PRESIDENT AND GENERAL MANAGER OF DIELECTRIC ATOMIC LAYER DEPOSITION PRODUCT DIVISION AT LAM RESEARCH

IMAGINE BEING in a large room filled with people, each of whom has an important piece of information that you need. All of them will gladly tell you what they know, but there's a problem: they're all speaking at once. The more densely packed the room, the harder it is to distinguish the words of the person you're trying to focus on from the surrounding cacophony.

The issue is crosstalk, defined by Wikipedia as "any phenomenon by which a signal transmitted on one circuit or channel of a transmission system creates an undesired effect in another circuit or channel." And if you're in the business of manufacturing memory and logic devices with billions of DRAM cells or logic transistors in extremely close proximity, you're facing a situation a lot like that room full of talkative people.

Consider the typical DRAM cell: a capacitor, which holds a charge representing a 1 or 0; an access transistor; and a bitline, through which the capacitor's charge is read. Over time, in the quest for greater density, speed and minimized power consumption, these structures have gotten smaller, and in recent years have evolved into 3D designs. In parallel, both the sensing voltage (ΔV) and cell capacitance (Cs) have been reduced with each

technology generation, thus necessitating a similar reduction in bitline capacitance (CBL).

In our roomful-of-people analogy, those reductions are the equivalent of the person you're listening to speaking less distinctly, making it even more difficult to isolate their words. And similar dynamics are at work in the logic sector, where ever-greater parasitic capacitances (both between gates and between gates and gate contacts) have increased the risk of crosstalk.

Crosstalk has been with us since the earliest days of electronics, and fortunately there is a well-known way of addressing it: isolation. In our crowded room this might involve placing a sound baffle around each person; on an IC, isolation can often be accomplished with better dielectric films.

"Better" in this case doesn't just mean a lower dielectric constant (k), although that's an important factor. Films must also deposit without risk of damage to other circuit elements, and be able to survive subsequent thermal processing, etching, cleaning, and other steps without any change in their properties. They must be defect-free and uniform. And in this era of 3D circuit features, thickness uniformity is not enough — a film's properties must also be uniform even when deposited in the vertical dimension.

There's also an additional factor that comes into play: every advanced chipmaking organization faces intense competition and strives to develop its own unique methods for eking out a bit more yield here, a little more performance there. Engineers responsible for these process tweaks benefit from versatility and flexibility in the films they work with — the ability to tune a film's composition to achieve different properties, including etch selectivity. Further, the higher density and complexity of each new technology generation makes these performance and yield gains more challenging to achieve. To revisit the roomful-of-people analogy, it's as if the room gets ever-smaller, while the people talk louder. There's less space for isolation but more need for it.

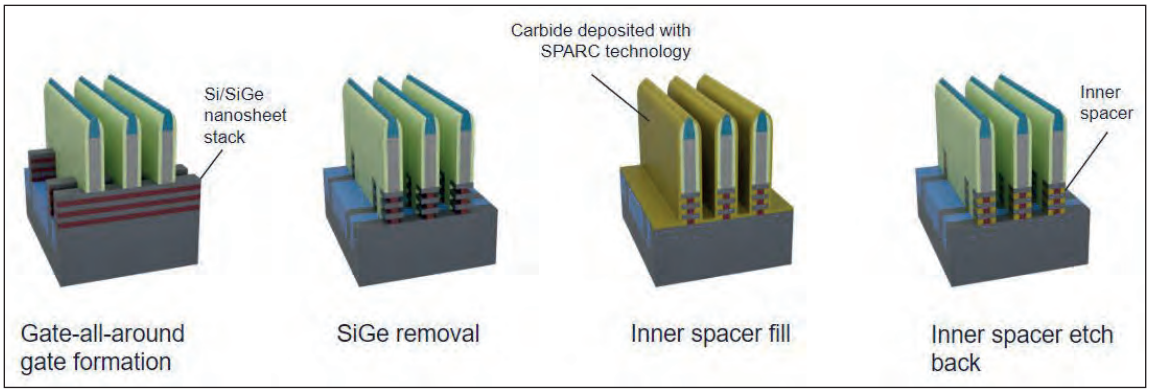
In the pre-3D era, process and integration engineers seeking isolation solutions could look to well-proven methods for deposition of tunable planar dielectrics or conformal SiO2 and nitrides. But today, there's a need for both tunability and conformality, as well as the ability to deposit films containing Si-C bonds, such as silicon oxy-carbide (SiCO). These are required for greater etch selectivity, which is an increasingly important factor in many applications, from gate-all-around (GAA) spacers to BEOL dielectrics to advanced lithography processes. At the same time, there's growing concern about plasma damage to circuit features.

So, what's the way forward in the quest for isolation? One avenue is a new deposition technique, SPARC, that aligns well with these emerging needs. In addition to maintaining uniform composition and film properties throughout the depth of high-aspect-ratio features, SPARC enables deposition of highly conformal SiCO thin films, which provide effective isolation when used as low-k spacers in both logic and DRAM devices.

Within the SiCO family, the SPARC method enables wide composition tuning, while still maintaining excellent conformality. Dense, robust SiCO films with k of ~4-4.4 and low leakage can be deposited directly on metals such as Co, W, etc., without oxidizing the underlayer. The films show excellent adhesion while also being hermetic. Even at low deposition temperatures of 400°C, the carbon is fully cross-linked with very few or no terminal methyl groups, providing thermal and chemical stability compared to other SiCO films.

Importantly, all this is accomplished in a non-plasma environment. Ground-state radicals in the downstream interact only with specific bonds in carefully chosen precursor molecules. The choice of radical and precursor molecules makes bond-breaking selective, thereby creating precursor radicals that have very low sticking coefficients and consequently excellent step coverage. Si-C bonds are not broken during the deposition step, and any O, N, or C bound to silicon in the precursor molecule is retained. The design and choice of precursor are driven by the desired film type to provide that wide composition tuning.

During this process, the ratio of Si-C bonds can be increased, with a reduction in Si-O bond density. Even with films deposited at different temperatures,



➤ SPARC-deposited films bring key properties to gate-all-around applications, including low k value, conformality, high pattern loading, uniform thickness, and excellent etch selectivity.

From a big-picture perspective, this means there's less need to pursue other avenues towards improved performance, all of which necessarily come at a cost and can introduce new complications. It's a great example of how a relatively subtle upgrade at a fundamental level can have tremendous leverage. The high flexibility and adaptability of the SPARC process opens the door to a wide range of conformal films and compositions

the amount of cross-linked carbon is the primary driver for etch selectivity over density or total amount of carbon in the film. In addition, these SiCO films have zero wet etch rate (WER) in typical wet chemistries such as dilute HF and hot phosphoric acid, and thus offer near-infinite wet etch selectivity. The films are also continuous and pinhole-free down to at least 15Å, unlike ALD SiN films which need to be at least 30Å to be pinhole-free.

What does this look like in practice? Let's go back to our DRAM cell example: as noted earlier, the continued node-to-node decline in cell capacitance has spurred a corresponding reduction in bitline capacitance to improve sensing (i.e., the ability to "hear the cell speak").

A significant component (perhaps half) of bitline capacitance derives from coupling between the bitline and storage node cell (SNC). Since the 20nm node, the use of air gaps has been a means of reducing this coupling. Note the light-green lines on either side of the air gaps — these are dielectric films that must meet many stringent standards including conformality, adhesion, hermeticity, dielectric constant, and breakdown voltage. The characteristics of SPARC-deposited SiOC enable lower-capacitance coupling than traditional materials, and hence greater DRAM performance.

In logic, gate spacers have long been known as a means of reducing parasitic capacitances both between gates and between gates and gate contacts, thus reducing the risk of crosstalk. The spacer concept has been carried over into 3D gate-all-around (GAA) architectures, but there's an additional wrinkle: the spacer material must also serve as a lateral etch stop. Again, the combination of characteristics exhibited by SPARC-deposited SiOC films is an excellent match for the situation. In addition to its electrical properties, SiOC's high anisotropy and excellent etch selectivity offer improved fab-line performance over other options.

In both these examples, minimization of crosstalk is just one consideration among many. But it's important to keep in mind that this minimization has great significance to the overall circuit development process, because it reduces the burden on the capacitor and transistor, making it easier for them to perform their desired functions. From a big-picture perspective, this means there's less need to pursue other avenues towards improved performance, all of which necessarily come at a cost and can introduce new complications. It's a great example of how a relatively subtle upgrade at a fundamental level can have tremendous leverage. The high flexibility and adaptability of the SPARC process opens the door to a wide range of conformal films and compositions. For example, it can be used to deposit silicon carbon nitride (SiCN) films, again with a high level of tunability. High-quality conformal boron-based films, such as boron carbide (BC) and boron carbon nitride (BCN), have also been successfully deposited; they offer different sputtering and etch behavior than their Si-based counterparts.

One especially interesting potential application is for advanced patterning techniques, such as Self-Aligned Quadruple Patterning (SAQP), self-aligned gate and contact (SAGC), and fully self-aligned via (fSAV), that are being developed for production of increasingly complex 3D structures. All rely on materials with distinct etch selectivity to achieve new levels of overlay accuracy; they essentially require unique combinations of spacer, hardmask, and etch-stop materials, both planar and conformal, that exhibit near-perfect etch selectivity to one another in various plasma etch and wet chemistries. Films based on BC and BCN are good candidates because they also provide suitable k, conformality, electrical properties, and other characteristics.

Likewise, SPARC-deposited films based on silicon carbide (Si-C) could prove very useful in 3D NAND memory hole fabrication as they offer good selectivity against oxides and nitrides, as well as tunability. And in any situation where plasma-based processing presents an issue, the ability to use radicals to create films of choice can put interesting new options into play.

Few industries evolve faster than semiconductor manufacturing, and that poses ongoing challenges for developing and integrating the ever-changing mix of production processes. As the industry continues to face new issues like 3D integration and enduring challenges like crosstalk, it will require ingenuity and creativity to keep pace, as well as innovative tools like SPARC that support these efforts to ensure that each piece of information is heard clearly.

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Eliminating EMI helps ensure accurate test, measurement

As semiconductors shrink with each new generation, inspecting devices on-wafer or as singulated die becomes increasingly complex thanks to environmental and co-located electronic sources of magnetic interference. The experts at Spicer Consulting explain the issues and remedies to help ensure fast and accurate test and metrology assessments.

THE NEED for ever-faster computing has led to semiconductors shrinking dramatically in size over the years. A pace we see anticipated by 'Moore's Law' that in the 1960s predicted the ever accelerating march of integrated circuit (IC) evolution that has held up through the early 21st century. While next-generation semiconductors may follow classical Dennard scaling techniques, the future will include 2D/3D devices, some employing chiplets, while others will improve performance and lower costs through 'down-sizing' just as Gordon Moore, Intel co-founder, predicted decades ago.

Cutting edge devices today are now at single-digit nanometre scale, yet even for older devices the steady march towards ever-smaller transistors has complicated test and measurement. Quality control of such small components can be tricky due to the very high level of magnification required to inspect the different circuits. TEMs and SEMs offer the accuracy required, but since they are sensitive to disturbances, it is important to remove any interference – such as vibrations and external magnetic fields – to ensure good resolution.

➤ The Spicer Consulting SC11 Analysis System offers a comprehensive way to assess vibrations, acoustic waves and magnetic fields.

External interferences reduce image quality

Semiconductors need to be as small as possible to improve their performance and reduce their energy consumption. Size reduction boosts performance thanks to the simple fact that reducing component size decreases the distance that electrons need to travel, which generates less heat and minimises energy loss; shorter circuit pathways also translate into faster signal processing.

Regardless the benefits of semiconductor evolution, both the manufacture and verification of such small devices is challenging, and only TEMs and SEMs can provide the required magnification to successfully image different parts of silicon wafers as they move along fab production lines.

Accurate positioning of the scanning electron beam has a great impact on image quality; in practical applications, deviations of the beam cannot be larger than the examined part. Disturbances such as vibrations, or the electromagnetic interferences created by AC and DC sources, will all shift the position of the electron

beam and decrease the resolution; AC fields show up as jagged lines in the image, while DC fields create wavy features. Unfortunately, these types of perturbations are quite common in environments where the semiconductors are produced and tested since, in order to save space, sensitive imaging instruments often have to share quarters with large pieces of industrial equipment. It is therefore important to perform an environmental survey prior to the installation of the electron microscope to ensure high quality imaging. Spicer Consulting, a leader in magnetic field cancellation, offers the SC11 Analysis System that has been designed for this task, measuring vibrations, acoustic waves and magnetic fields in the X, Y and Z directions. The results of these measurements are visualised graphically, helping the user to find the optimal location for their instrument.

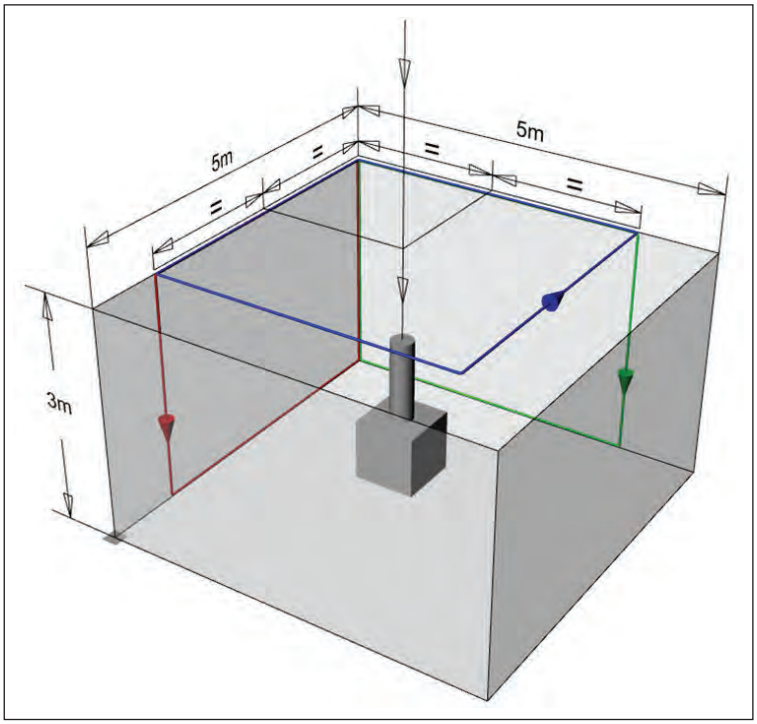
Cancelling magnetic fields

Even if a microscope is installed in the part of a lab that shows the lowest interference, there will still be some disturbances; DC magnetic fields are always present, including the Earth's field, and many instruments create AC fields with a frequency of ~60 Hz.

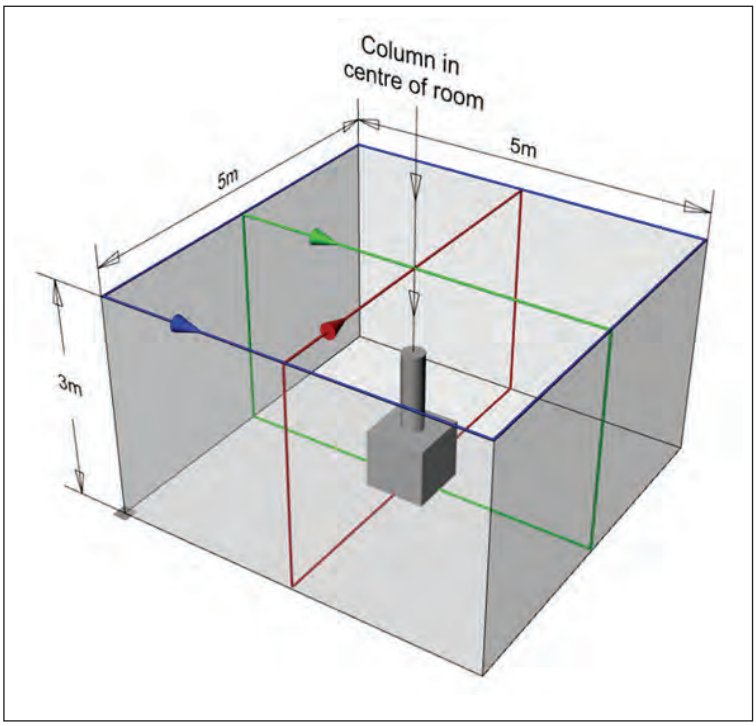
There are several ways to remove these magnetic fields. One of them is mu-metal shielding with metal sheets made from a ferromagnetic nickel–iron alloy with very high permeability. However, this solution is extremely expensive and has several limitations, as the material's permeability decreases with suboptimal handling. A more reliable solution is to install an active magnetic field cancellation system that can be used to handle stray magnetic fields from the surrounding instruments, as well as the changes in the Earth's field due to large moving ferromagnetic objects like elevators or metal doors. A common choice is Spicer's SC24 system, which consists of a magnetic field control unit, one or more magnetic field sensors and 3-axis cables that can cancel out the detected fields.

Cable positioning

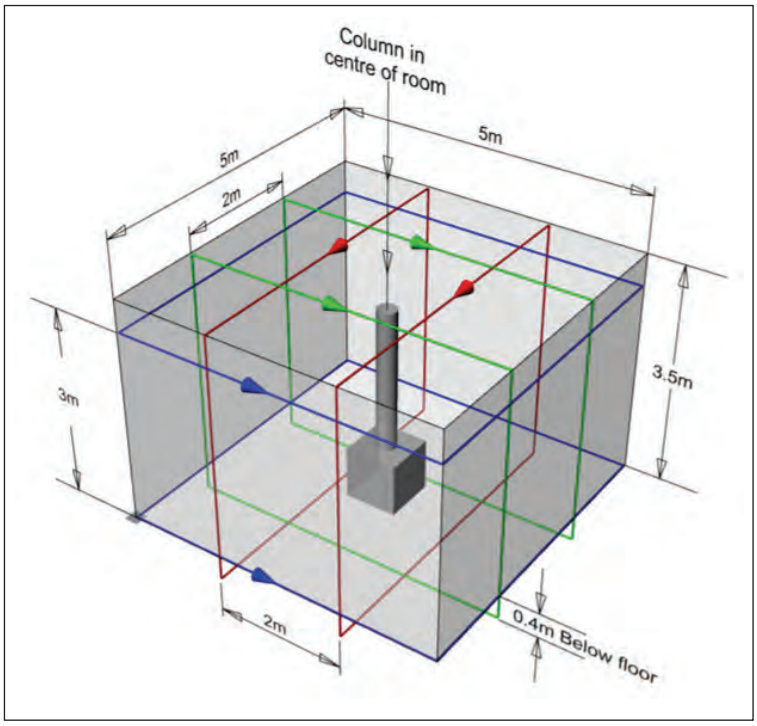
In application, the cables are positioned to form closed loops around the electron microscope – keeping the magnetic field around its column static. Cables can be positioned in different ways to find the optimal balance of complexity, cost and performance. The simplest and cheapest solution is to draw the cables (X, Y and Z) in three loops, forming three planes that do not intersect the microscope (figure 1), where the X and Y planes are parallel, and the Z plane is orthogonal to the column length. The benefits of this solution are that there are no cables on the floor, and no significant alterations to the room are required. However, the dynamic range and the cancelled volume are smaller, since the cables are further from the column. This set-up can be used for SEMs that have small columns and do not need a large volume of cancelled space that surrounds the instrument.



➤ Figure 1: The most simple way to alleviate magnetic interference is diagrammed above.



➤ Figure 2: This diagram illustrates cable placement for enhanced interference mitigation.



➤ Figure 3: For large TEMs, new labs under construction, or labs in which remodeling won't disturb normal operations, this diagram illustrates an optimized interference mitigation solution that involves dual loop cables and burying some cable portions below floor level.

If better performance is required, the X and Y cables should cross the room directly above the microscope column (figure 2), since drawing the loops closer will enhance the system's cancelling ability. For large TEMs or new labs, where remodelling would not disturb the other instruments, the optimal solution is to use dual loop cables and bury parts of them below the floor (figure 3). This solution gives the best performance and is recommended for TEMs with a Gatan Imaging Filter (GIF), since the GIF is situated below the microscope column and requires cancelling at a lower height. For existing microscope installations in which burying cables is not an option, the bottom sections of the cables can be at floor level and covered with suitable cable protectors. However, this will compromise the X and Y cancelling performance at GIF height.

Choosing the right sensors

The SC24 can be used with either one or two sensors of the same type. Using two sensors together, positioned on either side of the column, creates a 'virtual' sensor that measures the field at the spot of interest, by taking an average of the two measurements. The SC24 is available with two sensor types: SC24/AC for the detection of AC fields, and SC24/AC+DC for, as the name suggests, both AC and DC fields. The SC24/AC can cancel out disturbances with a frequency of 2.5Hz to 5kHz, with a cancelling factor greater than 50 at 60Hz, while the SC24/DC+AC can successfully cancel from 5kHz down to DC, with a cancelling factor of 100 at 60Hz and larger than 400 at DC.

For large TEMs or new labs, where remodelling would not disturb the other instruments, the optimal solution is to use dual loop cables and bury parts of them below the floor

Summary

Smaller semiconductors offer many benefits that continue to revolutionize OEM product development; semiconductors indeed impact almost every aspect of modern life. But the ever-shrinking size of ICs raises new challenges for manufacture and quality control (QC) testing. In order to properly investigate these components for defects, large degrees of magnification and exceptionally high accuracy are required. Electron microscopes offer a practical solution, but since they are very sensitive to changes in magnetic fields, it is important to cancel out any localised disturbances to ensure good image quality. Spicer Consulting provides instruments that can be used both to detect and to cancel the external magnetic fields, offering effective solutions that suit any lab or budget.

➤ The Spicer Consulting SC24 offers multiple sensor choices and a wide range of frequency interference cancellation options.

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How to Mitigate the Challenges of Bulk Gas Purification & Enhance Industry Innovation

There are several drivers for innovation in gas purification today, as the speed of technology continues to accelerate. The semiconductor industry is just one area where gas purification is critical, as high purity gas helps create these essential materials in a world that's demanding more of them than ever before.

BY ARM PURIFICATION

ACCORDING TO International Data Corporation (IDC), worldwide semiconductor revenue is expected to reach $661 billion USD by the end of 2022, a 13.7% year-over-year growth rate that follows 2021's strong revenue results of $582 billion USD. Chips will be increasingly important across nearly all industries, driven by growing semiconductor usage in cars, appliances, factories, computers, phones, accessories, and much more.

For complex gas purification with large flow rates, bulk gas purification is the right choice. But bulk purification comes with its own set of challenges – especially in mission-critical industries like the semiconductor sector.

Why Bulk Gas Purification is Necessary in Semiconductor Manufacturing

Ultra pure gas is required in advanced semiconductor manufacturing – and yet, even "ultra high purity" gas often fails to meet the required purity thresholds at the consistency needed to support stringent industry demands. In addition, technology is constantly advancing, and the list of desired contaminants for removal continues to expand, making achieving the desired outlet purity even more complex.

Gas purifiers are essential for upholding specific requirements for gas purity – and their effectiveness can make or break the integrity of large-scale processes. It's important to ensure your ideal gas purification solution meets all of your application requirements for gas type, flow rate, and pressure. For processes that require complex gas purification, bulk gas purification is ideal – yet challenging.

Key Challenges Associated with Bulk Gas Purification

Bulk applications require large flow rates and long lifespans, but ensuring impurities are removed and safety standards are maintained can be challenging when working with reactive or flammable gases with varying requirements.

The greatest challenges associated with gas purification include:

- **Maintaining Purity.** Maintaining purity can be difficult to ensure without the right system in place. There are a number of challenges with regards to purity, including the certification of impurities, identification of impurities, and material compatibility and degradation issues.
- **Ensuring Accurate Monitoring.** Monitoring the operation of bulk gas purification systems can be challenging. There's a need for readings to take place in real time, which is essential in order to safeguard processes. If data can't be accessed on demand, teams will be working from outdated information, leading to inaccuracies.
- **Meeting Safety Standards.** Large flow rates of reactive or flammable gases can be dangerous, so the purifier must be working properly and have safeguards and indicators that prevent issues, and mitigating them safely if they do occur, while notifying operators of the alarmed state of the unit.
- **Enabling Process Flexibility.** Innovative manufacturing approaches has become more complex, and is driving demand for more exacting delivery of specialty gases at precise pressures, temperatures, and flow rates. It can be challenging to maintain process flexibility across many variables.

Comprehensive Solutions for Complex Purification Challenges

The solution to overcoming the challenges associated with bulk gas purification lies in the equipment chosen. Organizations should make sure they implement the right system that ensures proper gas purification. The right system will ensure ultra high purity gas delivery, offer customizable features, handle large flow rates, and optimize yield. ARM Purification's bulk gas purifiers are designed to meet the specific requirements of a multitude of gas delivery systems, with innovative solutions that meet today's challenges of bulk gas purification.

Key features include:

- **Ultra High Purity Gas Delivery.** ARM Purification's bulk purifiers maintain the highest levels of purity and deliver gases in their purest form through the use of fabricated control manifolds, piped assemblies/manifolds, and purification technologies.
- **Customizable Aspects.** Small bulk purifiers (up to 60Nm3/hr) have a range of modularity options and offer customizable configurations that accommodate a wide range of high purity needs via specifications on enclosures, instrumentation, controls, and hardware. Larger bulk purifiers are built with the same mechanical and control features and we offer standard skid mounted designs for ease of movement and installation.
- **Large Flow Rates.** Bulk gas purifiers are equipped to safely handle large flow rates, allowing bulk purifiers to provide large-scale solutions for mission-critical processes that require ultra high purity gases.
- **Yield Optimization.** Advancing technology has led to increasingly high expectations for productivity and efficiency, challenging fabs to produce more wafers at rapid rates. ARM Purification's purifiers are built to endure wear and tear of continuous operation, and are designed with the needs of the bulk gas user in mind.

Overcome Challenges with the Right System & Proven Partner

Having the right system in place is critical for overcoming challenges and finding innovative solutions in a rapidly advancing world. For more than 20 years, ARM Purification's purifiers have been trusted by customers around the world to uphold the most stringent gas purity standards and meet and overcome complex gas purification challenges.

ARM Purification's experts help customers with application-specific challenges, and offer services from analytical services to refurbishment, regeneration, and end-to-end solutions – all combined with best-in-class service. This makes ARM Purification the ideal option for companies looking to uphold rigorous and mission-critical demands for pure process bulk gas.

To learn more about how the bulk gas purification system can empower operations and enhance innovation visit www.armpurification.com

➤ The greatest challenges associated with BULK gas purification include maintaining purity, ensuring accurate monitoring, meeting safety standards, and enabling process flexibility.

Co-packaged optics for hyperscale data centres

Equipping datacentres to meet ever-increasing service demands is bringing SiP and PIC components together into hybrid co-packaged optic (CPO) modules, an approach that challenges engineers and researchers to meld the technologies without performance or power compromises. EPIC explores ways major manufacturers are working to keep the data moving through microelectronic and photonic innovation.

BY IVAN NIKITSKIY, PROGRAM MANAGER, PHOTONICS TECHNOLOGIES,
EUROPEAN PHOTONICS INDUSTRY CONSORTIUM (EPIC)

WITH DATA CENTRE TRAFFIC growing at an unprecedented pace, fuelled by advances in AI and Machine Learning, networking infrastructure must scale in capacity while maintaining or even reducing its total power consumption and footprint. How is the industry going to move forward to hyperscale data center operations with the introduction of next-generation / second- generation Co-Packaged Optics (CPO)? Here we overview how the large industry players, members of EPIC – the European Photonics Industry Consortium – address user requirements for CPO from different perspectives.

HiSilicon (a Huawei company), China

Huawei is a major player in co-package optics, and their Advanced Photonic section develops the photonic optical components that go into Huawei's larger systems. They are currently addressing the challenges of developing 100 Tbit/s co-packaged optics. Eric Bernier, Leader of Advanced Photonics at HiSilicon Technologies in Canada, the former ASIC Design Center of Huawei explains: the general consensus within the industry is that at the bandwidth required by a 100 Tbit/s switch, it becomes impossible to move the data electronically without consuming the entire power budget for the switch chip. As a consequence, at 100 Tbit/s, co-packaged optics are essential. But from a module perspective, it's not possible to double the number of modules because of reliability issues and also because it becomes harder to package.

As a result, the solution for achieving the required higher density will be to increase the capacity of the co-packaged optics to around 200 Gbit/s per fiber coming out of each module with multiple wavelengths per fiber. This will require inputting more optical power into the system, and although a lot of progress has been made, Bernier believes that ultimately, they will need new technology.

For this reason, they are presently engaged on two research projects initiated by The International Photonics Advocacy Coalition (IPAC). One aims to develop a standard form factor for the external laser source, and the other is looking at the issues, the system architectures and the evolution of the electronics that are limiting 100 Tbit/s co-packaged optics. Currently, it is generally assumed that any future device will incorporate a connector because it will be easier for the supply and assembly chains. However, if the aim is to increase density while simultaneously reducing the power requirement on the staircase, the connector may have to be eliminated.

Senko Advanced Components Inc., Japan:
Tiger Ninomiya, Senior Technologist at Senko Advanced Components in the US, identifies four main challenges for CPO connectors in a data centre switch applications: 1) an increase in fiber count and how to arrange the fibers in and out; 2) a use of external laser sources; 3) a change in face plate density that requires reserved spaces for laser sources and TRx channels, and 4) the challenge of internal fiber routing as fibers are now inside the system.

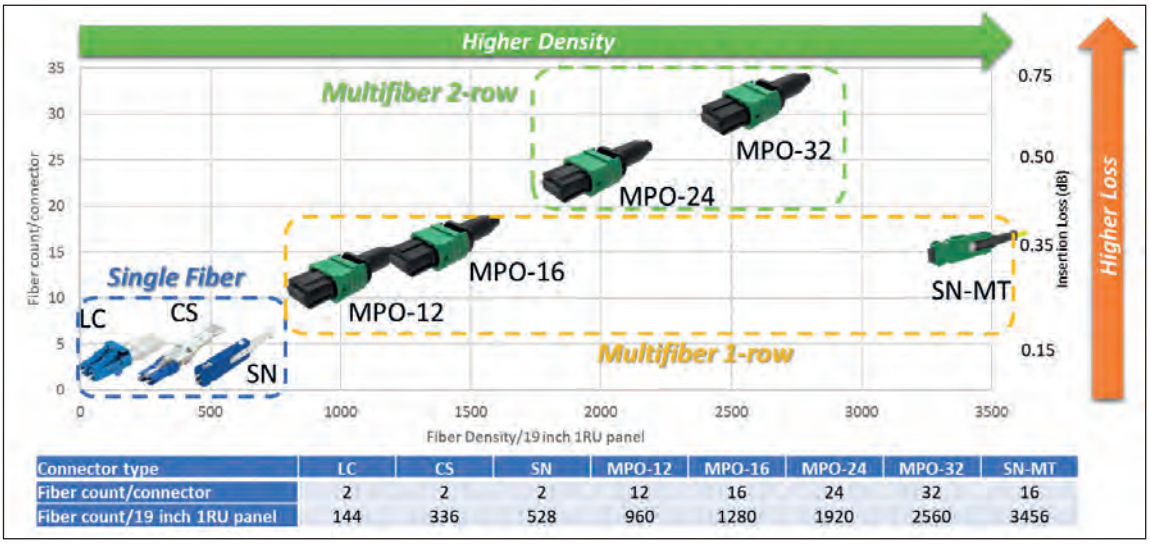
As regards to fibre count increase, the 12.8 terabit switch typically has 32 ports with eight fibers per transfer module that adds up to a total of 256 fibers in the case of using parallel optics. Similarly, the 51.2 terabits switch with CPO has 16 modules embedded on the switch ASIC substrate. And with parallel optics, each one of CPO optical engines can have up to 64 fibers, which adds up to a total of 1,024 fibres just for TRx – 4 times what they are dealing with now.

The issue with faceplate density derives from the need to have more fibers and to find space for external laser sources. The MPO connector has better density over duplex types of connectors. However, there is a correlation between fiber count per connector and optical performance. With a larger fiber count, it becomes challenging to maintain the lower loss, especially having multiple rows of multi fibers such as MPO-24 and MPO-32.

Senko is addressing this issue with their SN-MT connector carrying 16 fibers per connector, which improves fiber density at the panel while maintaining lower loss. Compared with MPO connectors, the SN-MT is roughly half the size and has a 2.7x density increase compared with MPO-16F. SN-MT even provides a better density than MPO-24 and MPO-32, while using a 1-row type ferrule, the optical performance is comparable to 1-row MPO. Senko also uses other technologies to overcome face plate density issues. These include fiber routing options for mid-board connectors; a fibre routing shuffle box, and backplane connectors. The Consortium of On-Board Optics (COBO) and Co-Packaged Optics Working Group, which Tiger is chairing, aims to provide technical guidance and standards for CPO implementations focusing on optical connectivity and remote laser sources. In July 2022 they released a white paper on optical connectivity that details how these technologies can be utilized. [1]

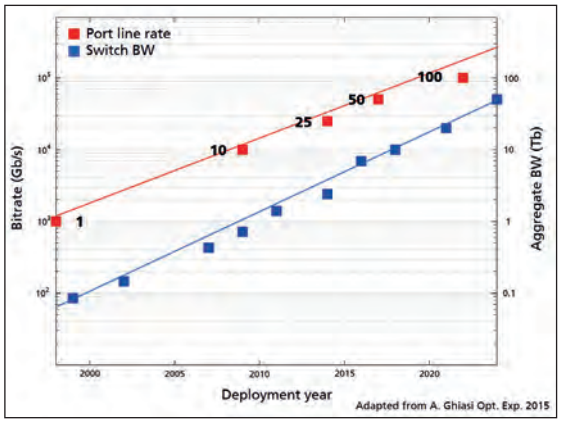
OFS Optics (a Furukawa company), USA:
OFS Optics has been involved across many different specialty fibre applications and markets for the better part of 30 years. Specifically in the telecom and datacom space, they work mainly with OEMs supplying erbium doped fibres, polarization maintaining fibres, and low bend loss fibres. Recently, OFS has been developing new novel fibre types such as hollow core and multi-core fibres. They are also developing external laser source (ELS) modules for co-packaged optics. For John Earnhardt, Director of Sales at OFS Speciality, the transition of going from copper dominant to fiber dominant has created a number of challenges.

From a fiber optic perspective, with both PM and single mode fibres, there's the issue of mode field diameter. In some cases, users want a conventional nine micron type mode field diameter and in other cases they want atypical mode field sizes that interface directly with the chip – options might be in a three micron mode field and a couple of options in between three and nine micron.



Connector type	LC	CS	SN	MPO-12	MPO-16	MPO-24	MPO-32	SN-MT
Fiber count/connector	2	2	2	12	16	24	32	16
Fiber count/19 inch 1RU panel	144	336	528	960	1280	1920	2560	3456

➤ Figure 1. Evolution of fiber density, insertion losses, and fiber count per connector by Senko Advanced Components Inc.



➤ Figure 2. Evolution of switch and transceiver bandwidths. Adapted from [2]

Low bend loss is becoming increasingly important as transceiver modules shrink in size and go to QSFPDD and OSFP and there will likely be pressure on low bend loss as well in the CPO area. With PM fibres, there are potential issues regarding traditional PM properties like beat length and PER and so on. Another area of concern is multi-path interference, particularly with the move to low bend loss fibres together with potential mis-match the mode field diameters when splicing together two fibres.

In addition to optical considerations, there are mechanical ones. In this regard, they are seeing increasing pressure to improve their tolerances, in relation, for example to core clad offset, core diameter and clad diameter. The mechanical properties directly impact the overall efficiency of laser delivery through fibres. As regards the question of clad diameter i.e., 80 micron or 125 micron, their initial ELS samples were based on a 125 cladding diameter, but they are seeing pressure for more 80 micron fibres, both PM and SMF for transceivers and other types of applications. OFS is also seeing two emerging trends in fiber coating. One is a smaller diameter, for example, moving from 165 to 135 micron for 80 micron cladding. The other is the increasing demand for alternative coatings that will survive at least for a short-term duration at higher temperatures with solder reflow, and possibly for a longer term duration in some photonic packages with local hot spots.

Fraunhofer IZM (Institute for Reliability and Microintegration), Germany:
In the last decade, Fraunhofer IZM have been innovating in the area of computing and data center applications using photonic interconnects. They contribute in the areas of system concept and design, photonic- and RF- component design, signal integrity & board design, silicon photonics interposer, developed with through silicon wire technologies, 3D integration, flip chip assembly, co-packaging, system evaluation and benchmarking. In the field of CPO they started with a flagship project for data centre interconnects with the goal to utilize optical interconnections and 3D integration technologies to make data centres and high-performance computers faster on all levels: rack-to-rack, board-to-board and chip-to-chip. More recently, they have been involved in the MASSTART project, which was set up to facilitate the high volume manufacturing of Tb/s inter and intra data center transceivers. For Tolga Tekin, Group Manager at Fraunhofer IZM, a major challenge for data center network topology is that more than 70% of the traffic stays inside the data center. This means that the interfaces need to have enough capability and symmetry to connect all of the nodes. The transceiver data rate follows the Ethernet switch port speed. The serializer/deserializer (SerDes) speed is defining the port speed of the transceiver. The packaging constraints limit chip radix to 256 (512) ports/ASIC. Even though the SerDes arrays are constantly evolving to support higher bitrate, the power consumption of SerDes increases with bitrate.

The acceptance of the solutions depends on their costs. For the typical single mode data center transceiver, the target is $1 per Gbps, so the cost of the optics for a transceiver with 32 ports on the switch front panel is $10-13k, making the transceiver cost for the entire data center around $50 million. Accordingly, Fraunhofer is developing a cost cutting strategy based on decoupling the I/O from the logic system. The effect is to reduce the power consumption of chip I/O from 180 watts for their 25 terabit switch ASIC to 40 watts. At the same time, they have been able to increase the link reach thereby reducing loss from 12 dB to 1 dB. Recently completed EU-project L3MATRIX has been devoted to large-scale silicon photonics matrix for low power and low cost data centres.

This project aimed to improve the underlying network technology with photonic switching to enable scale performance whilst keeping power consumption under control. In the co-packaged optics, a fiber array is coupled directly using micro lens arrays combined with integrated III-V and silicon photonics and directly attached to the switch ASIC. They have focused on 25 terabit switches with co-packaged optics using a 2D transceiver array based on silicon photonics with integrated III-V materials. These devices address up to 256 lanes and use integrated lasers by bonding III-V layers on silicon photonics in Mach-Zehnder configuration. Altogether, the future of Co-Packaged Optics is about creating a new ecosystem, which is going to involve efforts from component manufactures and higher level system integrators to create a network, involving everyone in the industry, to develop the right standards and to design and integrate these new components and to scale production.

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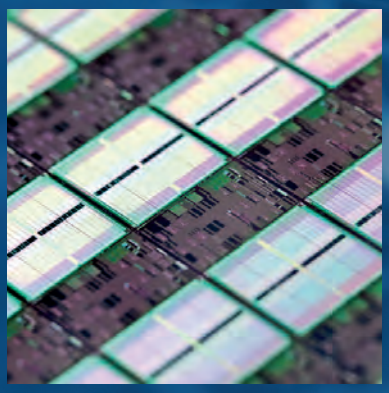

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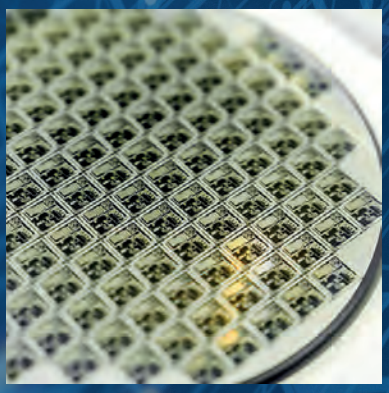

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