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WHEN IT CAN'T FAIL

Greene Tweed's Chemraz® FFKM Seals: Unsung Heroes

VOLUME 44 ISSUE IV 2023
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INSIDE

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VIEWPOINT

By Phil Alsop, Editor

Optimism, pessimism and realism – where should the balance lie?

I TALK to almost anyone in the semiconductor industry and there's not one voice that seems to dissent from the much heralded and much quoted $1 trillion, 2030 market expansion roadmap. And yet, talk to anyone about one of the three Ss that cast a significant shadow over the industry right now – Supply Chain, Skills and Sustainability – and there's a little less confidence that the industry is on top of these challenges. Challenges which will have a direct impact on the achievement, or not, of the 2030 target. But only a little less.

Onshoring/reshoring and the various CHIPS Acts are apparently going to vanquish any supply chain problems that are a hangover from the pandemic or the result of ongoing geopolitical tensions – never mind the time and expense to build new fabs.

Hardly a day goes by without some skills or education-related news crossing my computer screen, and yet many of these programmes will not produce the semiconductor personnel required to fill the many vacancies which exist now, let alone the new jobs created by expansion, overnight. There are few shortcuts to learning a technology comprehensively – I've been involved in the storage networking industry for 20+ years, but would still not call myself an expert. And, yes, there are different skills required for different jobs within the semiconductor space, but I wonder just how much of a skills shortfall we might encounter between now and...2030. Although AI could just fill some of the gap.

As for sustainability, there's no doubt that technology and the environment can work together for mutual benefit, but to achieve such synchronicity, there does need to

be something of a revolution – we can't slowly, slowly evolve to address climate change. There will need to be step changes and some short-term disruption unless, of course, sustainability ambitions are allowed/continue to take second place to the digital imperative. This summer's weather extremes across the globe would suggest such an approach might be unwise.

In summary, rather than have the extremes of optimism and pessimism when it comes to the industry's future (and, let's face it extremes of any sort tend not work for the majority), maybe it's time for an era of realism? The glass is neither half full nor half empty, but contains just the right amount of liquid, so long as due consideration and balance is given to the three Ss and the impact they will undoubtedly have on the industry's future.

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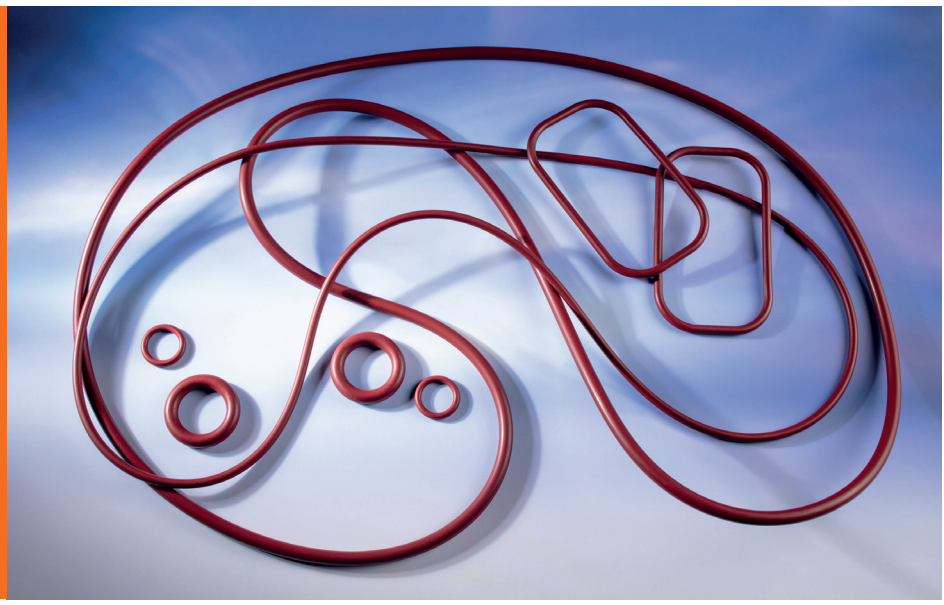
SILICON SEMICONDUCTOR

Greene Tweed: when it can't fail

For years, the world will tell stories about what happened when we ran out of semiconductors during the pandemic. But industry insiders will remember this time for one more reason. The crunch highlighted the vital importance of some inconspicuous but indispensable component makers that power the intricate machinery of chip manufacturing



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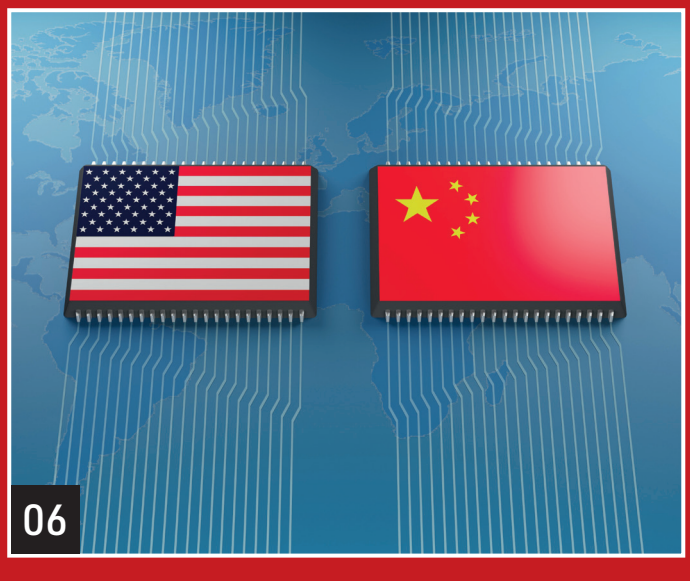

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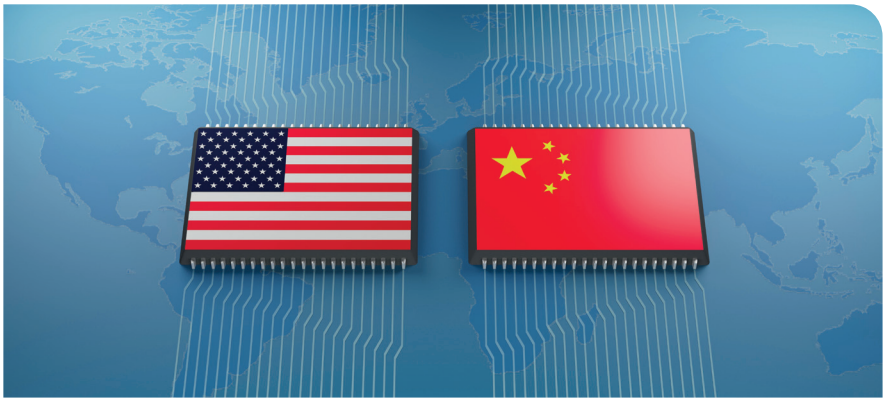
Chips as currency

Leo Charlton, Technology Analyst at IDTechEx, discusses America, China, and the AI Race.

RUNNING in the background to the more visible, very real wars occurring around the world at present, there is another, economic and industrial in nature. This is a trade war between two principals: the USA and China. The potential consequences of this trade war are incredibly significant to global geopolitics, as how the interaction between the two parties is handled will determine a basis for any future cooperation between the two principals as well as their respective allies.



This trade war is over the production of semiconductor chips, those small pieces of (mainly) electronic circuitry that are found in many modern-day devices, from smartphones to televisions, cars to computers. In IDTechEx's recent report "AI Chips 2023-2033", the market research company highlights the part that artificial intelligence (AI) plays in this trade war, where the race for AI supremacy has become a national concern.

The Shortage, Where Demand Exceeds Supply

But before discussing the role of AI, it is more instructive to start at the beginning or thereabouts. This does not require going so far back in time - only five years, in fact, to 2018. From January of that year, under the presidency of Donald Trump formerly and now President Joe Biden, the US has enforced several layers of restrictions and barriers to trade on China where semiconductors are concerned, each successive layer aiming to plug a hole that the previous layer(s) had left. These restrictions are shown below.

The reasons for these restrictions are multiple, starting with simple economics (where the US wishes to halt China's growing market share in the semiconductor supply chain) before moving onto interwoven concerns such as risk exposure and the use of semiconductors for militaristic purposes.

With regards to geographic risk exposure, since 2020, there has been a global chip shortage, where demand for semiconductor chips has exceeded supply. This shortage exposed US design companies to the risk of relying upon South-East Asia manufacturing capabilities, as lead times elongated to upwards of 3 months by the beginning of the crisis.

A number of complementing factors caused the global chip shortage. Principle among them is the COVID-19 Pandemic, which saw a rise in demand (due to more people working from home and so in need of personal computers) and a fall in supply (due to lockdowns across Asia resulting in plants being shut down). Other factors include the rise of data mining (where GPUs are needed, thus once again increasing demand); a drought that hit Taiwan in 2021, resulting in problems with producing ultra-pure water to clean factories and wafers; fires at several fabrication facilities owned by Asahi Kaseri, Renesas and ASML; and difficulties procuring neon (used for lasers in chip manufacture) due to the Russia-Ukraine War, as Ukraine was responsible for providing more than 90% of the US semiconductor-grade neon.

These events combined would likely be enough for a country such as the US to consider investing in their own production capabilities (where the US Chips and Science Act of 2022 is discussed in more detail in the aforementioned IDTechEx report). But the level of spending on semiconductor imports by China, as well as the blurred line between commercial and military ventures in the country, has led the US to become wary of outfitting a rival economy with the tools to surpass them in key technology areas. This is where AI comes into play.

AI as a Motivator

In addition to the restrictions presented above, on August 26th, 2022, the US government placed a ban on AMD and Nvidia from exporting chips that can be used to support AI workloads to China. According to an August SEC Filing made by Nvidia, this comes in the form of a license agreement, effective immediately, for any future export to China (including Hong Kong) and Russia of Nvidia's A100 and forthcoming H100 integrated circuits. Any systems that incorporate the A100 and H100 ICs are also covered by the new license requirement, as well as any future integrated circuits that are roughly as advanced as the A100. The filing asserts that the US government has indicated that the new license requirement will address the risk that the covered products may be used in a military capacity by China or Russia. In a similar fashion, a spokesperson for AMD - speaking with Reuters - said that the company had received new license requirements that effectively put a stop on exports of AMD's MI250 AI chips to China.

This information alludes to the fact that the restrictions imposed upon Chinese companies by the US government are not simply a matter of trying to take some control of the supply chain from the APAC region but also a matter of national security. The measures are an attempt by the US to arrest China's AI surge by preventing the type of advanced technologies that are needed for China to realize AI supremacy (a not unfounded concern, as by 2018, China had filed 2.5X more patents in AI technologies than the US). Such is the interwoven aspect of commercial and military endeavors in China that the Biden administration has effectively stopped trying to block military-affiliated exports while retaining commercial exports and the revenue that generates. As such, to quote the Center for Strategic & International Studies, "High-end AI chips can no longer be sold to any entity operating in China, whether that is the Chinese military, a Chinese tech company, or even a US company operating a data center in China".

AI not only promises to be one of the biggest drivers of economic advances within the next quarter century, but for China, AI mastery represents the ability to perfect a model of governance in keeping with existing architectures. The effectiveness of AI models comes largely down to the quality and breadth of the training data set provided. Given that China can collect significant volumes of citizen data, the country is poised to reap the benefits of widespread AI usage.

China's Response

China has - until recently - been rather quiet in the face of these restrictions, although some displeasure was expressed when TSMC (a Taiwanese semiconductor fabricator that accounts for the vast majority of leading-edge node manufacture globally) announced plans to build new fabrication facilities in Arizona, USA, last year. But in July 2023, China struck back, with restrictions placed on the export of Gallium and Germanium, materials that are used in certain semiconductor chip manufacture.

Germanium is used in applications such as thermal imaging cameras, solar panels, and telecommunications, where germanium can be used in photodiodes to convert light signals to electrical ones. Gallium is often paired with arsenic to form gallium arsenide, a compound semiconductor that can operate at higher temperatures and frequencies than silicon. At present, China produces around 98% of the world's gallium and controls around 68% of global refined germanium production in various countries, according to the US Geological Survey. The impact that restrictions on these material exports have on the US and allied countries is not to be downplayed.

Outlook

Both European and Asian delegates alike have warned against these ongoing restrictions by both principals, given that the onus on the shoring up of national interests currently involves punishing the other party concurrently. And the harder that the US pushes against China, the harder that China will lean into plugging money into their own domestic supply chain (and given that in 2021 China spent the equivalent of USD$432 billion on imported microprocessors, money that they may no longer be able to be spend on imports, China is certainly not short of funding).

As with most countries, China has not looked to develop an isolated, front-to-back domestic semiconductor supply chain to date, as they have had the option to work with superior foreign partners rather than domestic firms that do not meet the same standards; design companies could work with established fabs in Taiwan rather than inferior domestic fabs, and Chinese fabs could buy foreign semiconductor manufacturing equipment (SME) with proven quality. Now that they are cut off from these possibilities, China must look to growing domestic capabilities.

In the short term, this will prove to be very difficult for China. While the country has been stockpiling chips and SMEs in anticipation of these imposed controls (the 7 nm chip produced by SMIC was produced using existing deep ultraviolet (DUV) machines), these resources will eventually run out, and so China must look to develop domestic capabilities if their semiconductor industry isn't to completely dry out, at least in terms of the more advanced node processes. It seems likely that, for the next few years, China will have to rely on more mature node processes in the creation of new chips.

From a survey of 91 smartphones released from 2020 with AI coprocessing capabilities, the trend is for successively-released models to move to leading-edge nodes. Given that MediaTek, Qualcomm, and Apple are the industry leaders in the smartphone SoC space, it is unlikely that Chinese companies will be able to compete appreciably in this space any time soon. However, where leading-edge nodes are not as necessary to functioning edge devices - such as in matters of security and industrial settings - China may indeed be able to find more traction through the short-term focus on mature node technologies. Source: IDTechEx

This being said, it is unlikely that China will have no foreign support at all, at least in terms of SME and components supply. Companies that have a large stake in the Chinese market - such as Zeiss, a German company that supplies mirrors to ASML for their extreme ultraviolet (EUV) lithographic machines, and where China is their fastest growing market - may be unwilling to relinquish revenues generated from China. In an effort to abide by the US export controls, companies may engineer out the US inputs or components in their products such that they can sell these without repercussions in China.

In the longer term, there is cause for cautious optimism for China. Forced to work together in a way that they have not done previously, China's fabs, design companies, and SME firms may form an ecosystem that is not only stronger from the forced collaboration but also more thoroughly isolated from global supply chain disruptions than most other countries (and, in addition, free from US controls). This comes with significant hurdles, but these may be removed or - at the least - lessened should other countries feel the adverse economic effects of being unable to bolster their raw material supply.

The story is far from being finished, but with a projected growth of US$257.6 billion by 2033 for AI chips alone, there is much to be gained and lost over the next ten years.

Semiconductor IP unleashes next-gen potential!

Future Market Insight forecasts that the global semiconductor intellectual property (IP) market is poised to achieve a noteworthy milestone by 2033, surpassing a substantial valuation of US$ 13.10 billion.

WITH A PROJECTED CAGR of 6.7%, this growth trajectory indicates a significant rise from its estimated worth of US$ 6.83 billion in 2023.

The semiconductor IP market is experiencing growth due to the escalating demand for automation and the rapid adoption of IP Core products in the consumer electronics industry. There is an ever-growing demand for cutting-edge electronic devices, such as smartphones, tablets, and wearable gadgets. The utilization of semiconductor IPs is enhancing the capabilities of IoT products.

The industry is also expanding rapidly because of the increasing prevalence of internet access and the growing utilization of smart connected devices, which further contribute to market growth. Semiconductor IP provides pre-designed and verified components that help these companies accelerate their product development cycles. Semiconductor IP enables companies to cater to market demands swiftly by leveraging ready-made components. Developing semiconductor chips from scratch is a challenging process that requires significant time, effort, and investment. Companies strive to shorten their time-to-market and minimize development costs in today's fast-paced industry. Semiconductor IP addresses these challenges by offering pre-designed IP blocks and subsystems.

The semiconductor industry experiences constant advancements in manufacturing technologies, including smaller process nodes and enhanced integration capabilities. These technological breakthroughs present new design challenges that require specialized semiconductor IP solutions. To meet these demands, semiconductor IP providers develop and offer IP solutions optimized for the latest technological advancements. The semiconductor intellectual property market thrives due to the growth of emerging markets like automotive electronics, industrial automation, robotics, and smart infrastructure. These emerging markets have unique requirements, such as functional safety, reliability, and power efficiency. Semiconductor IP providers meet these demands by offering application-specific IP solutions. The market growth is also supported by the increasing acceptance of wireless technology-driven devices and the substantial investments made by key players in the development of advanced wireless products.

Furthermore, prominent market players are actively investing in the global expansion of wireless technology devices to meet consumer demands. This surge in wireless technology development and investment creates a heightened demand for IP solutions, including silicon-based design IP, interface IP, and processor IP. The electronics industry is characterized by ever-evolving technology. The semiconductor sector is facing physical limitations in manufacturing existing materials. The detection of patented technology is increasingly challenging due to the integration of patented components within devices. Disentangling these components and determining the ownership of each patent has become difficult. The shrinking feature sizes in current semiconductor fabrication processes require more advanced analysis tools for circuit detection and extraction. This directly influences licensing activities and the value of companies' patent portfolios.

With the proliferation of connected devices and the ever-looming cyber threats, security has become a paramount concern in semiconductor design. Security IP, including encryption/decryption and hardware authentication, is witnessing a substantial surge in demand. IP vendors that prioritize and excel in security-related solutions can capitalize on the pressing need to safeguard data and protect systems.

Consolidation has become a prevailing trend in the semiconductor IP market, with larger companies acquiring smaller IP vendors to strengthen their portfolios and expand their market reach. This trend is expected to continue as companies strive to offer comprehensive solutions to their customers. Smaller IP vendors with unique and differentiated offerings present attractive acquisition targets, opening up lucrative opportunities.

Key Takeaways

- The semiconductor intellectual property industry in the United Kingdom is anticipated to rise, exhibiting a CAGR of 5.4% through 2033.
- The United States held a 15.4% share of the global semiconductor intellectual property industry in 2022.
- With a CAGR of 8.2% over the forecast period, India is predicted to develop rapidly in the semiconductor intellectual property industry.
- In 2022, Japan had a 3.3% share of the semiconductor intellectual property industry globally.
- The semiconductor intellectual property industry in China is expected to flourish, registering a CAGR of 7.6% over the forecast period.
- Germany accounted for 8.1% of the global semiconductor intellectual property industry in 2022.

Competitive Landscape in the Semiconductor Intellectual Property Market

Key players are engaged in various activities to maintain their competitiveness and drive innovation. They invest significantly in research and development to create advanced and cutting-edge semiconductor IP solutions.

Embarking on a new growth cycle?

The trillion-dollar semiconductor industry is on the brink of a fresh phase of expansion, driven by advancements in AI, quantum computing, 5G, and specialized applications.

ACCORDING TO Yole Intelligence, semiconductor device revenue peaked in 2022 at US$573 billion and is expected to retreat 7% to US$534 billion in 2023. This industry plays a critical role in enabling technological advancements across various sectors, including mobile & consumer, infrastructure, automotive, industrial, and more.

In its new Overview of the Semiconductor Devices Industry 2023 report, the company, part of Yole Group, asserts that the industry has experienced a sustained 6.4% CAGR growth over the past few decades. This industry is driven hard by increasing demand for mobile & consumer electronics, the rise of internet usage such as social media, and the rapid digital transformation of all industries. Integrated circuits are becoming smaller, more powerful, and capable of handling complex tasks, paving the way for new technology advancements such as artificial intelligence, machine learning, and edge computing. This evolution presents numerous opportunities and challenges for leading companies, requiring them to invest massively in R&D and capital expenditure for new foundries to maintain significance in this fast-paced landscape.

Pierre CambouMSc, MBA, Principal Analyst, Yole Intelligence, explains: “The semiconductor device industry relies heavily on global ecosystems, making supply chain resilience and risk mitigation crucial for sustained success. Recent disruptions and geopolitical tensions have highlighted the vulnerabilities of the semiconductor supply chain.”

The semiconductor industry is geographically concentrated in a few places, primarily the US, Taiwan, Korea, Japan, Europe, and mainland China. The dominance of US-based semiconductor device companies is

historical; in the last five years, they have maintained a 53% market share. “If we combine all types of semiconductor company business models, i.e., adding the open foundries, OSAT, equipment, and material companies, the market share of US companies drops to 41%”, explains Pierre Cambou. “Then, if only the added value is considered, the US share becomes 32%, and this number has been diminishing at a rate of 1 percentage point per year in the last five years.”

To go further, Yole Group shared its vision of the industry with ATREG, a company specialized in the disposition of infrastructure-rich advanced technology manufacturing assets, including semiconductor fabs and cleanrooms. Both companies reflected on the fortunes of the global semiconductor industry to date and discuss how the major players need to invest to secure their supply chain and chip capacity.

Indeed, over the last five years, there have been significant changes in the chip-making industry, such as Intel losing its crown to two relatively new contenders, Samsung and TSMC. Stephen Rothrock, ATREG’s CEO & Founder, and Pierre Cambou had the opportunity to debate the state of the global semiconductor industry landscape and its evolution. In a wide-ranging discussion, they covered the market and its growth prospects, as well as the global ecosystem and how companies can optimize supply. Discover the first part of the discussion here, and the second part, centered around how to ensure chip supply amid growing geo-political tensions and economic realities affecting semiconductor production, here.

Semiconductor technology trends are no longer single-threaded. At the center of competition is the More Moore node race in the manufacturing process, currently 7nm, 5nm, and 3nm, as well as upcoming smaller nodes. These cutting-edge processes allow for higher transistor density, improved performance, and energy efficiency, though they pose significant challenges regarding development costs, yield rates, and manufacturing complexity.

The semiconductor industry is, therefore, actively exploring innovative solutions through More-than-Moore approaches. And radical innovations are there. Therefore, advanced packaging, photonics integration, quantum computing, and neuromorphic computing will play their role in the expansion of the industry serving a growing diversity of semiconductor device types.

Catalyze Program promises decarbonisation

Collaboration aims to accelerate the adoption of renewable energy and reduce carbon emissions throughout the global semiconductor value chain.

SCHNEIDER ELECTRIC has launched Catalyze, a new partnership program aimed at accelerating access to renewable energy across the global semiconductor value chain.

Unveiled during SEMICON West 2023, Catalyze is a 'first-of-its kind' program of collaboration among key semiconductor and technology industry leaders to address the supply chain emissions within their industry. The program joins other Schneider Electric supply chain partnership initiatives that seek to leverage the power of supply chain cohorts, including the Energize program for the pharmaceutical industry, and Walmart's Gigaton PPA program.

Intel, one of the world's leading semiconductor design and manufacturing companies, and Applied Materials, Inc., the world's largest semiconductor and display equipment company are the inaugural corporate sponsors of the Catalyze program. Together with Schneider Electric, the companies will encourage suppliers from throughout the semiconductor industry ecosystem to join the Catalyze program and help accelerate the value chain's transition to renewable energy and a low carbon future.

As the global demand for semiconductors in consumer and commercial products increases, the carbon footprint continues to grow, making it imperative for semiconductor industry leaders to collaborate to drive greater use of renewable energy and achieve a more sustainable path to growth. The shared goal of the Catalyze participants will be to encourage the industry's thousands of suppliers to take bold climate action through decarbonization. This is a challenging task, due to the complexity of the value chain, data availability and reliability, and the difficulties in defining the boundaries of such emissions.

Catalyze Program Elements

The Catalyze program strives to:

- Combine energy purchasing power across the semiconductor value chain to accelerate the deployment of renewable energy projects
- Provide suppliers – who may not have the capability on their own – with the opportunity to participate in the market for utility-scale power purchase agreements (PPAs)
- Increase awareness of the availability of renewable energy in specific global regions where the semiconductor value chain is operational, to increase greater adoption
- Continue to assist suppliers who have made commitments to reduce their carbon emissions and/or sign on to this program
- Educate companies in the semiconductor value chain about the importance of developing operational models to use in their supply chain programs – to close net-zero ambition gaps
- Engage thousands of suppliers simultaneously through digital technology platforms, to drive swift and measurable actions in their supply chain decarbonization
- Lead the way for the industry to drive definitive next steps.

Sponsoring companies will collaborate on the development of the program – including identifying focus areas and suppliers – as well as encouraging other semiconductor companies to consider the program for their own value chains

"At Schneider Electric, our purpose is to empower companies to make the most of our energy and resources, bringing progress and sustainability together for everyone. Our mission is to be a digital partner for Sustainability and Efficiency, and the Catalyze partnership program is an excellent example of how companies in key global industries can collaborate to accelerate decarbonization," said Peter Herweck, CEO of Schneider Electric.

"Switching to renewable energy is an important step to reduce greenhouse gas emissions. Intel has achieved 93 per cent renewable electricity in our global operations and remains committed to reaching 100 per cent by 2030," said Intel's Keyvan Esfarjani, Chief Global Operations Officer. "Intel is proud to be a founding member of Catalyze to help remove barriers to choosing greener energy. Ultimately, we want our entire value chain to achieve net-zero as we continue to deliver leading technologies that power our digital world."

"Applied Materials has been working with our suppliers to instill sustainability best practices through our SuCCESS2030 initiative, and we are excited to build on our momentum with the Catalyze program," said Gary Dickerson, President and CEO, Applied Materials. "Promoting closer collaboration across the value chain is key to accelerating carbon emissions reduction. We look forward to working with our partners to drive higher output of clean energy for the global semiconductor industry."

The program will initially focus on suppliers with energy load in specific markets in the semiconductor value chain where renewable energy is currently available, with the intention to expand globally where specific interest and renewable energy market opportunities align.

Applied Materials and Fraunhofer IPMS launch European Semiconductor- Metrology Tech Hub

New hub will provide state-of-the-art metrology systems to accelerate semiconductor research and enhance development projects with chipmakers and ecosystem partners across Europe, particularly in ICAPS market segments.

Applied Materials and the Fraunhofer Institute for Photonic Microsystems IPMS have revealed a landmark collaboration to create Europe´s largest technology hub for semiconductor metrology and process analysis.

To be located at the Center Nanoelectronic Technologies (CNT) of Fraunhofer IPMS in Dresden, the technology hub is situated in the heart of Silicon Saxony, Europe's largest semiconductor cluster. The hub will be equipped with Applied Materials' state-of-the-art eBeam metrology equipment, including its VeritySEM® CD-SEM (critical dimension scanning electron microscope) systems, and staffed by Applied engineers and R&D experts.

"Fraunhofer IPMS and its partners will benefit from access to Applied's industry-leading eBeam metrology systems", said Dr. Benjamin Uhlig-Lilienthal, Head of Business Unit Next Generation Computing at Fraunhofer IPMS. "The new technology hub will offer advanced wafer-level metrology in our industrial CMOS environment with Fraunhofer IPMS's unique ability to loop wafers directly with semiconductor manufacturers."

"Our collaborative metrology hub will accelerate learning cycles and the development of new applications for the Fraunhofer Institute, Applied Materials and our customers and partners in Europe," said James Robson, Corporate Vice President for Applied Materials Europe. "This unique technology hub will have the capability to test and qualify processes on a variety of substrate materials and wafer thicknesses critical to applications across the diverse European semiconductor landscape."

Metrology is crucial in the production of microchips as it enables the accurate measurements needed to precisely monitor and control the quality of individual semiconductor manufacturing steps and sequences. Chipmakers use metrology equipment at critical points to help validate physical and electrical characteristics and maintain target yields.

TSMC, Bosch, Infineon, and NXP establish joint venture

Plans to bring advanced semiconductor manufacturing to Europe.

TSMC, Robert Bosch GmbH, Infineon Technologies and NXP Semiconductors plan to jointly invest in European Semiconductor Manufacturing Company (ESMC) GmbH, in Dresden, Germany to provide advanced semiconductor manufacturing services. ESMC marks a significant step towards construction of a 300mm fab to support the future capacity needs of the fast-growing automotive and industrial sectors, with the final investment decision pending confirmation of the level of public funding for this project.

The project is planned under the framework of the European Chips Act. The planned fab is expected to have a monthly production capacity of 40,000 300mm (12-inch) wafers on TSMC's 28/22 nanometer planar CMOS and 16/12 nanometer FinFET process technology, further strengthening Europe's semiconductor manufacturing ecosystem with advanced FinFET transistor technology and creating about 2,000 direct high-tech professional jobs. ESMC aims to begin construction of the fab in the second half of 2024 with production targeted to begin by the end of 2027.

The planned joint venture will be 70% owned by TSMC, with Bosch, Infineon, and NXP each holding 10% equity stake, subject to regulatory approvals and other conditions. Total investments are expected to exceed 10 billion euros consisting of equity injection, debt borrowing, and strong support from the European Union and German government. The fab will be operated by TSMC.

"This investment in Dresden demonstrates TSMC's commitment to serving our customers' strategic capacity and technology needs, and we are excited at this opportunity to deepen our long-standing partnership with Bosch, Infineon, and NXP," said Dr. CC Wei, Chief Executive Officer of TSMC. "Europe is a highly promising place for semiconductor innovation, particularly in the automotive and industrial fields, and we look forward to bringing those innovations to life on our advanced silicon technology with the talent in Europe."

Dr. Stefan Hartung, chairman of the Bosch board of management: "Semiconductors are not only a crucial success factor for Bosch. Their reliable availability is also of great importance for the success of the global automotive industry. Apart from continuously expanding our own manufacturing facilities, we further secure our supply chains as an automotive supplier through close cooperation with our partners. With TSMC, we are pleased to gain a global innovation leader to strengthen the semiconductor ecosystem in the direct vicinity of our semiconductor plant in Dresden."

"Our joint investment is an important milestone to bolster the European semiconductor ecosystem. With this, Dresden is strengthening its position as one of the world's most important semiconductor hubs that is already home to Infineon's largest frontend site," said Jochen Hanebeck, CEO of Infineon Technologies.

"Infineon will use the new capacity to serve the growing demand particularly of its European customers, especially in automotive and IoT. The advanced capabilities will provide a basis for developing innovative technologies, products and solutions to address the global challenges of decarbonization and digitalisation."

"NXP is very committed to strengthening innovation and supply chain resilience in Europe," said Kurt Sievers, President and CEO of NXP Semiconductors.

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SEMI connects more than 2,500 member companies and 1.3 million professionals worldwide to advance the technology and business of electronics design and manufacturing. The breadth and depth of our events, programs and services help members accelerate innovation and collaboration on the toughest challenges to growth.

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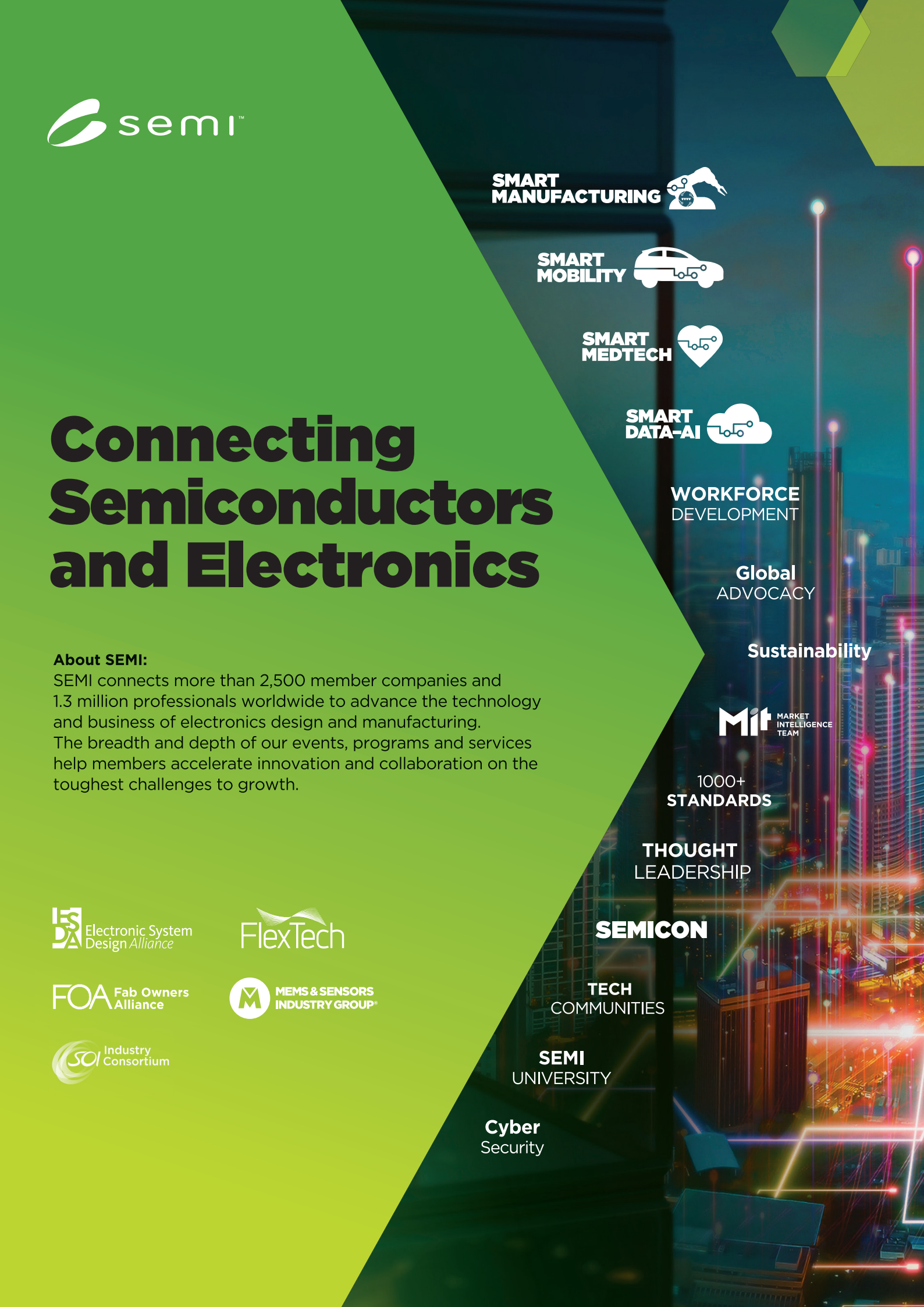
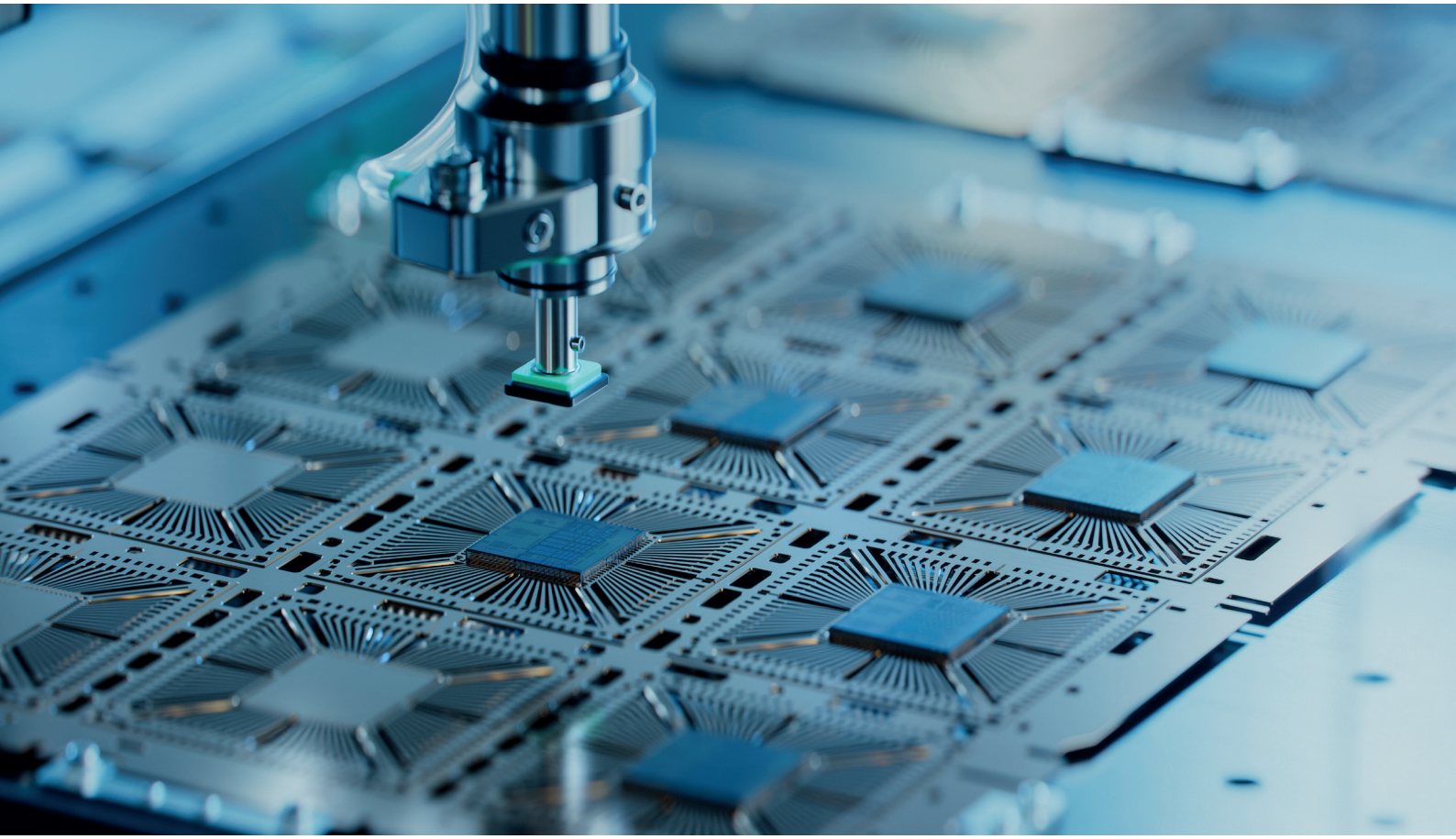




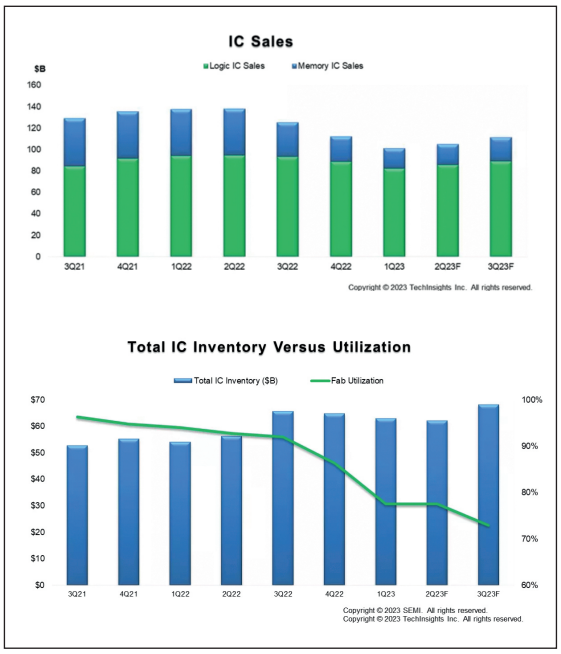
Industry on track for recovery, but near-term headwinds remain

With sequential IC sales declines beginning to moderate, the global semiconductor industry appears to be nearing the end of a downcycle and is expected to begin to recover in 2024, SEMI, in partnership with TechInsights, reported in the Semiconductor Manufacturing Monitor.

In Q3 2023, electronics sales are projected to post healthy quarter-on-quarter growth of 10%, while memory IC sales are expected to log double-digit growth for the first time since the downturn started in Q3 2022. Logic IC sales are predicted to remain stable and improve as demand gradually recovers.

Headwinds will continue for the semiconductor manufacturing sector in the second half of the year, SEMI and TechInsights reported. Drawdowns of high inventory at integrated device manufacturer (IDM) and fabless companies will continue to suppress fab utilization rates to much lower levels than those in the first half of 2023. The weakness is projected to extend declines in capital equipment billings and silicon shipments for the rest of the year despite stable results in the first half of 2023. Market indicators point to a semiconductor industry bottoming at the end of the first half of 2023, and the industry has since started a recovery, setting the stage for continued growth in 2024. All segments are projected to log year-over-year increases in 2024, with electronics sales surpassing its 2022 peak.

“The slower-than-expected demand recovery will delay the normalization of inventory until the end of 2023, later than we previously anticipated, leading to additional reductions in fab utilization rates in the short term,” said Clark Tseng, Senior Director of Market Intelligence at SEMI. “However, recent trends suggest that the worst is over for ICs. We anticipate



➤ Sources: SEMI (www.semi.org) and TechInsights (www.techinsights.com), August 2023

semiconductor manufacturing will bottom in Q1 2024."

"While semiconductor markets have seen a sharp downturn the last four quarters, equipment sales and fab construction have been performing much better than expected," said Boris Metodiev, Director of Market Analysis at TechInsights. "Government incentives have been driving new fab projects and strong backlogs have helped equipment sales." The Semiconductor Manufacturing Monitor (SMM) report provides end-to-end data on the worldwide semiconductor manufacturing industry. The report highlights key trends based on industry indicators including capital equipment, fab capacity, and semiconductor and electronics sales, and includes a capital equipment market forecast.

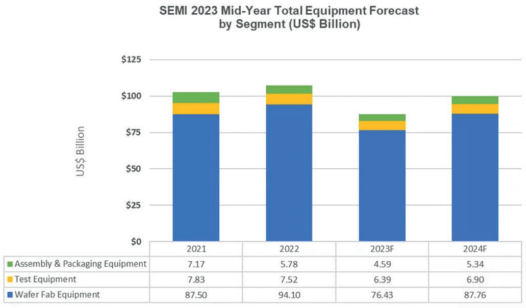
The SMM report also contains two years of quarterly data and a one-quarter outlook for the semiconductor manufacturing supply chain including leading IDM, fabless, foundry, and OSAT companies. An SMM subscription includes quarterly reports.

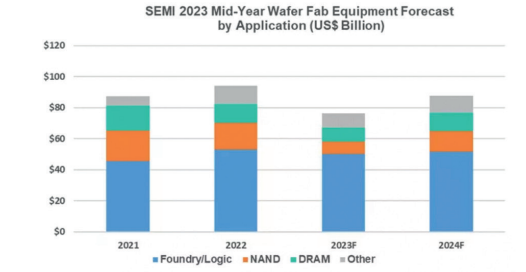
Equipment sales to hit $87 billion in 2023

Global sales of total semiconductor manufacturing equipment by original equipment manufacturers next year are forecast to bounce back from a projected contraction of 18.6% to $87.4 billion in 2023 following the industry record of $107.4 billion in 2022, SEMI announced today in its Mid-Year Total Semiconductor Equipment Forecast – OEM Perspective at SEMICON West 2023. The expected 2024 recovery – to $100 billion – will be driven by both the front-end and back-end segments. "Despite current headwinds, the semiconductor equipment market is set to see a strong rebound in 2024 after an adjustment in 2023 following a historic multi-year run," said Ajit Manocha, SEMI president and CEO. "Projections for robust long-term growth driven by high-performance computing and ubiquitous connectivity remain intact."

Semiconductor Equipment Sales by Segment
Sales of wafer fab equipment, which includes wafer processing, fab facilities and mask/reticle equipment, are projected to decrease 18.8% to $76.4 billion in 2023 – more than the 16.8% decline predicted by SEMI in the 2022 year-end forecast. The wafer fab equipment segment is projected to account for the bulk of the recovery to $100 billion in 2024, generating $87.8 billion in sales, a 14.8% increase.

The 2022 decline in back-end equipment segment sales is expected to continue in 2023 due to challenging macroeconomic conditions and softening semiconductor demand. Semiconductor test equipment market sales are projected to contract by 15% to $6.4 billion in 2023, while assembly and packaging equipment sales are expected to drop by 20.5% to $4.6 billion in the same year. However, the test equipment and assembly and packaging equipment segments are expected to expand by 7.9% and 16.4%, respectively, in 2024.





➤ Source: SEMI July 2023, Equipment Market Data Subscription

➤ Source: SEMI July 2023, Equipment Market Data Subscription

Silicon Area Shipment Trends - Semiconductor Applications Only

Millions of Square Inches

	1Q 2022	2Q 2022	3Q 2022	4Q 2022	1Q 2023	2Q 2023
Total	3,679	3,704	3,741	3,589	3,265	3,331

Data cited in this release include polished silicon wafers, including those used as virgin test wafers, as well as epitaxial silicon wafers, and non-polished silicon wafers shipped by the wafer manufacturers to end users.

Semiconductor equipment sales by application

Equipment sales for foundry and logic applications, accounting for more than half of total wafer fab equipment receipts, are expected to drop 6% year-over-year to $50.1 billion in 2023, reflecting softer end-market conditions. Demand for leading-edge foundry and logic in 2023 is expected to remain stable, with a slight softening balanced out by a rise in spending on mature nodes. Foundry and logic investments are projected to increase 3% in 2024. DRAM equipment sales are expected to fall 28% to $8.8 billion in 2023 due to continuing weak consumer and enterprise demand for memory and storage but rebound 31% to $11.6 billion in 2024. NAND equipment sales are projected to decrease 51% to $8.4 billion in 2023 and surge 59% to $13.3 billion in 2024.

Semiconductor equipment region sales

China, Taiwan and Korea are expected to remain the top three destinations for equipment spending in 2023 and 2024. While Taiwan is forecast to regain the lead in 2023, China is projected to return to the top position in 2024. Equipment spending for most regions tracked is expected to fall in 2023 before returning to growth in 2024. TThe SEMI forecast is based on collective input from top equipment suppliers, the SEMI Worldwide Semiconductor Equipment Market Statistics (WWSEMS) data collection program and the industry-recognized SEMI World Fab Forecast database. The Equipment Market Data Subscription (EMDS) from SEMI provides comprehensive market data for the global semiconductor equipment market.

Worldwide silicon wafer shipments increase

Worldwide silicon wafer shipments increased 2.0% quarter-over-quarter to 3,331 million square inches in the second quarter of 2023, down 10.1% from the 3,704 million square inches recorded during the same quarter last year, the SEMI Silicon Manufacturers Group (SMG) reported in its quarterly analysis of the silicon wafer industry. “The semiconductor industry continues to work through excess inventory in various market segments, necessitating that fabs operate below full capacity,” said Anna-Riikka Vuorikari-Antikainen, Chairman of SEMI SMG and Chief Commercial Officer at Okmetic. “As a result, silicon wafer shipments are lagging their 2022 peak. Second-quarter wafer shipments held steady quarter-on-quarter with 300mm showing quarterly growth among all wafer sizes.”

Silicon area shipment trends – Semiconductor applications only

Silicon wafers are the fundamental building material for the majority of semiconductors, which are vital components of all electronic devices. The highly engineered thin disks are produced in diameters of up to 12 inches and serve as the substrate material on which most semiconductors are fabricated. The SMG is a sub-committee of the SEMI Electronic Materials Group (EMG) and is open to SEMI members involved in manufacturing polycrystalline silicon, monocrystalline silicon or silicon wafers (e.g., as cut, polished, epi). The SMG facilitates collective efforts on issues related to the silicon industry including the development of market information and statistics about the silicon industry and the semiconductor market.

SEMICON West 2024 dates

SEMI has announced that SEMICON West 2024 at the Moscone Center in San Francisco will be held July 9-11.

SEMICON West is moving to Phoenix for a five-year annual rotation and shifting from its longstanding July event dates to October beginning in 2025. The exhibition and conference will be held again in Arizona in 2027 and 2029, with all three appearances at the Phoenix Convention Center. Phoenix will first host SEMICON West Oct. 7-9, 2025. The event will continue to be held at the Moscone Center in San Francisco on the alternating years and over the long term.

“We look forward to bringing the remarkable excitement pervasive at SEMICON West 2023 to next year’s exhibition and conference,” said Joe Stockunas, President of SEMI Americas. “Semiconductor industry growth, sustainability and talent will remain major themes at SEMICON West 2024 as we again provide a stage for critical insights and conversations key for the industry to flourish in the years to come.”

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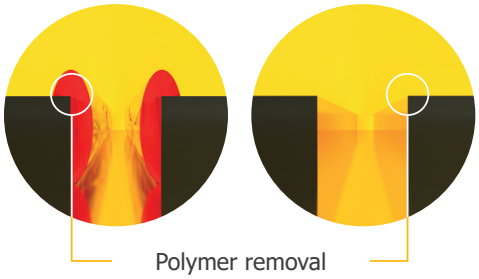
GREEN GOALS.
YELLOW SOLUTIONS.

PERC™ PROCESS FOR SUSTAINABLE POLYMER REMOVAL



perc™ enables simple and flexible polymer removal. Due to its unique process flexibility, it is used to remove any kind of polymer residues after dry etching processes like metal-, oxide-, silicon- or VIA etching.

The perc™ function is based on inline spiking technology. DI water applied with a very small quantity of acid/alkaline-based media is used to clean the wafer surface. Unique spiking and mixing technologies guarantee accurate concentration and flow for each wafer.

100 %	Polymer removal	**140 %**	Throughput increase
79,8 %	Reduction of chemical consumption	**99,95 %**	Reduction of waste treatment
100 %	Elimination of solvents	**58,3 %**	Reduction of costs per wafer

Compared to conventional processes

MORE INFO

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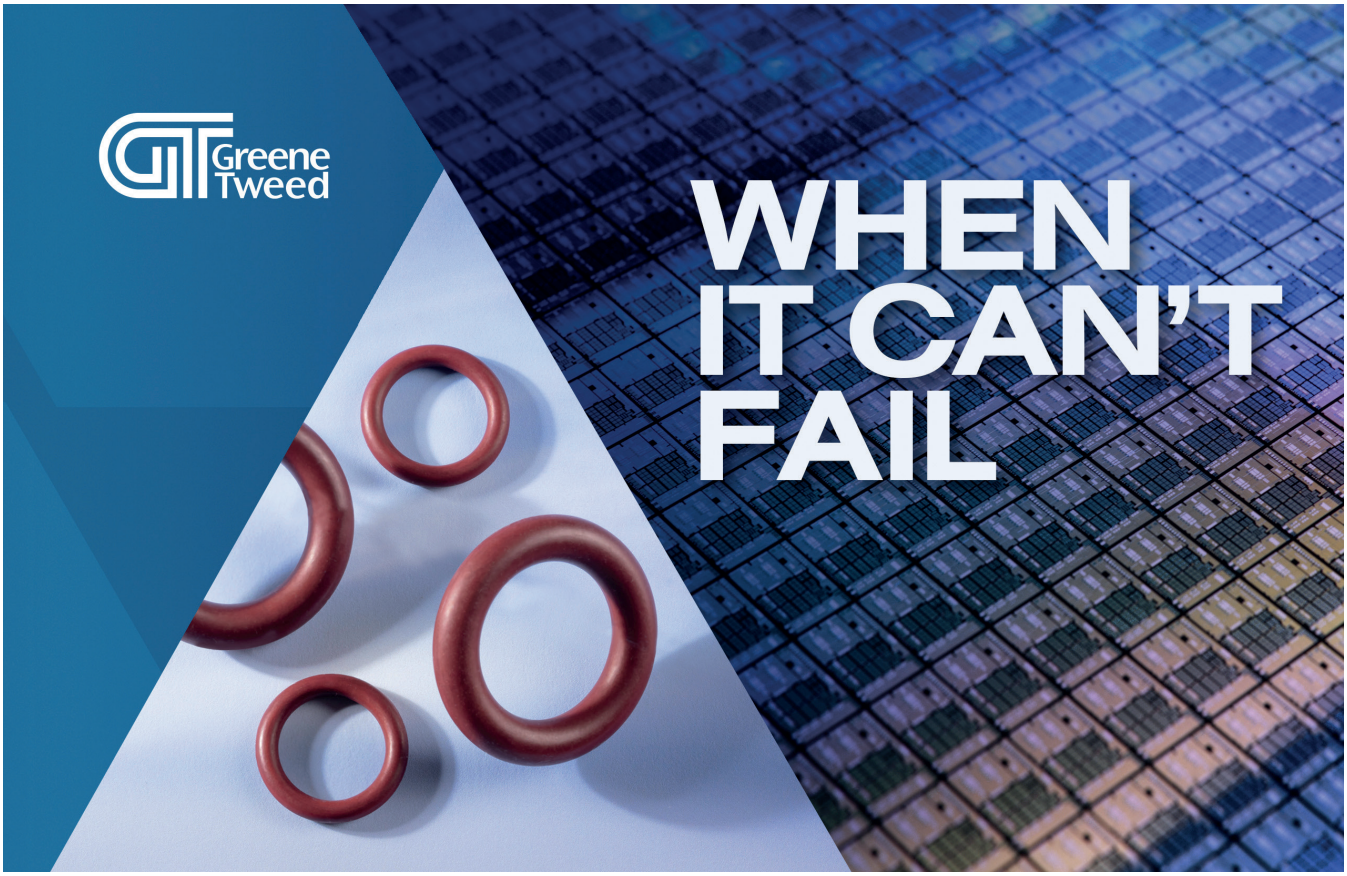


Greene Tweed: When it can't fail

For years, the world will tell stories about what happened when we ran out of semiconductors during the pandemic. But industry insiders will remember this time for one more reason. The crunch highlighted the vital importance of some inconspicuous but indispensable component makers that power the intricate machinery of chip manufacturing.

By Nick McNeal, Director Semiconductor Strategy, Greene Tweed; Thyag Sadasiwan, Director Chemraz®, Greene Tweed; and Pragati Verma, Content Specialist, Greene Tweed

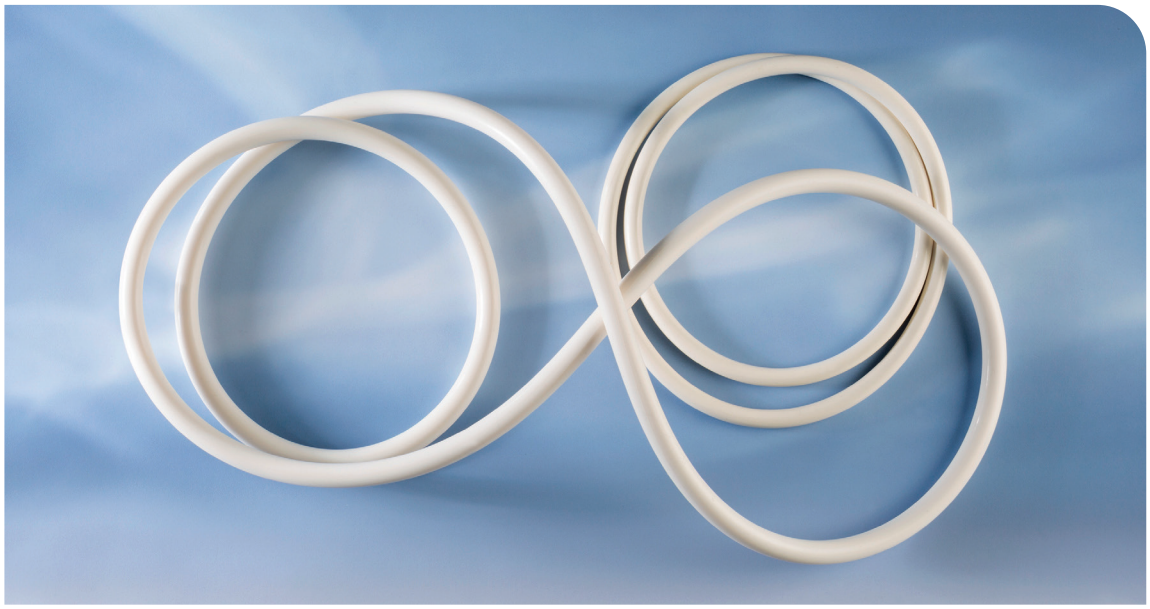
Greene Tweed's Chemraz® FFKM seals: unsung heroes

GREENE TWEED is a remarkable example of such a company working behind the scenes to manufacture sealing solutions that outperform and outlast in the world's harshest semiconductor manufacturing applications. For 160 years, we've equipped critical sectors with materials and engineered components that deliver certainty for their crucial operations.

Our Perfluoroelastomer (FFKM) Chemraz® o-rings and sealing solutions, for instance, meet the critical demands of modern chip fabrication by preventing contamination while withstanding aggressive chemicals and extremely high temperatures.

For decades, we have been at the forefront of the complex FFKM production process. These high-performance materials need specific ingredients. So, disruptions can occur even if a single ingredient is in short supply. An unexpected and tumultuous industry-wide supply crunch gripped several FFKM ingredients due to several factors, including pandemic lockdowns and geopolitical events such as the Russia-Ukraine war.

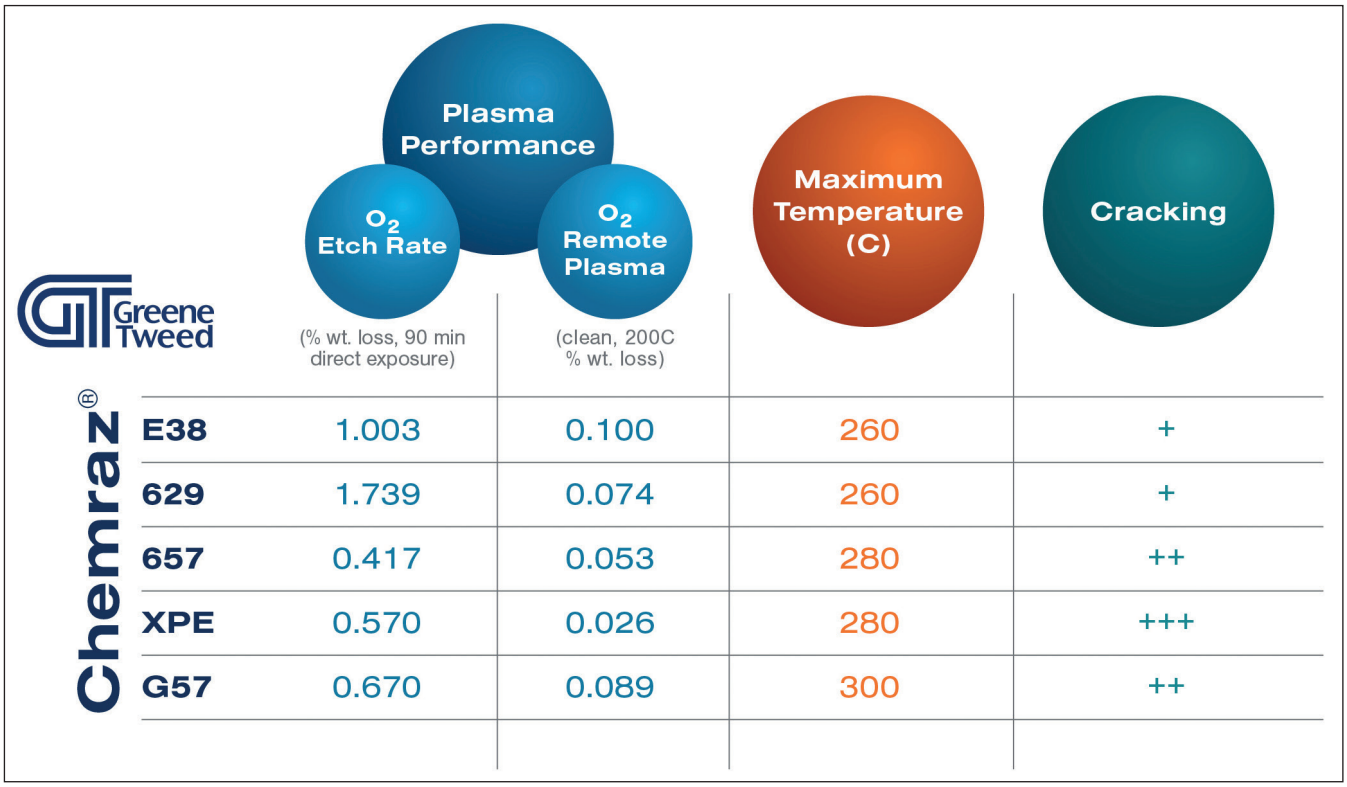
The situation was exacerbated by an announcement from a major supplier that it will stop producing all fluoropolymers, fluorinated fluids, and certain additive products by the end of 2025. The disruption could not come at a worse time – It coincided with a global surge in demand for



chips. FFKM material was in short supply at the very moment when semiconductor manufacturers needed it to go into overdrive. Soon, the FFKM industry found itself caught in the middle of a perfect storm, where supply delays could cause serious impediments to semiconductor availability and the resultant economic recovery.

It's not hard to see how these disruptions have made chipmakers acutely aware of how dependent the semiconductor industry is on FFKM seals. What's more, the criticality of FFKM sealing solutions will only grow as chipmakers pack more and tinier transistors in their chips and turn to more demanding processes that rely on ultraclean processing. Greene Tweed was the first sealing solutions company to use cleanroom manufacturing in the US and we intimately understand the significance of ultraclean operations in the semiconductor industry.

We understand that our FFKM Chemraz® sealing solutions are critical to perform in the harshest environments of modern semiconductor fabrication processes and improve uptime, reduce contamination, and boost wafer yield.



➤ Chemraz® FFKM sealing solutions are known for their exceptional resistance to extreme temperatures, chemicals, and plasma environments.

All your semiconductor sealing questions, answered

DO YOU need an elastomer o-ring or sealing solution built to withstand aggressive liquids, gases, and plasma at extreme temperatures found in the harshest semiconductor applications? Here are answers to the key sealing questions facing semiconductor manufacturers:

What kind of seals work best for semiconductor manufacturing processes?

Perfluoroelastomer (or FFKM) sealing material, known for its exceptional resistance to aggressive chemicals, extreme temperatures, and plasma environments, is ideal for a manufacturing process as aggressive as semiconductor fabrication.

Greene Tweed offers Chemraz® sealing solutions, known for their exceptional resistance to extreme temperatures, chemicals, and plasma environments.

What sets Greene Tweed's Chemraz® sealing solutions apart?

At Greene Tweed, we take pride in our Chemraz® sealing solutions that are engineered to outperform and outlast in the world's harshest environments. For 160 years, we've equipped critical sectors, including the semiconductor industry, with materials and engineered components that perform – no excuses, no exceptions.

With the broadest temperature range and unmatched chemical resistance among all elastomeric materials, Chemraz® is the prime choice for the most challenging semiconductor applications. Our superior quality, precision engineering and customizability result in less downtime, and higher wafer processing yields.

What kind of semiconductor manufacturing processes benefit from Greene Tweed's Chemraz® sealing solutions?

Chemraz® FFKM sealing solutions are ideal for a wide range of semiconductor equipment such as:

- Conductor Etch
- Dielectric Etch
- PECVD
- ALD
- RTP
- Wet Cleans
- Chamber Seals
- Slit Valve and BSVs
- Pendulum and Gate Valves
- Eseals
- Chemical Delivery

Can Greene Tweed's sealing solutions withstand aggressive cleaning and etching chemistries?

Absolutely! Chemraz® exhibits exceptional chemical resistance, making it highly compatible with aggressive cleaning and etching chemistries used in semiconductor fabrication. It remains stable even when exposed to harsh plasma environments and reactive chemicals, ensuring optimal performance and longevity.

Can Greene Tweed customize seals to suit specific semiconductor applications?

Yes, at Greene Tweed, we offer a range of sealing solutions that can be tailored to meet your specific requirements. Our engineering team works closely with semiconductor manufacturers to design custom seals that match equipment specifications and deliver optimized performance.

I want to implement Greene Tweed's latest sealing solutions in my semiconductor application. How can I start the process?

To explore the benefits of FFKM sealing solutions tailored to your semiconductor equipment, reach out to our expert team at Greene Tweed. Our engineers are ready to talk about your specifications and provide technical guidance.

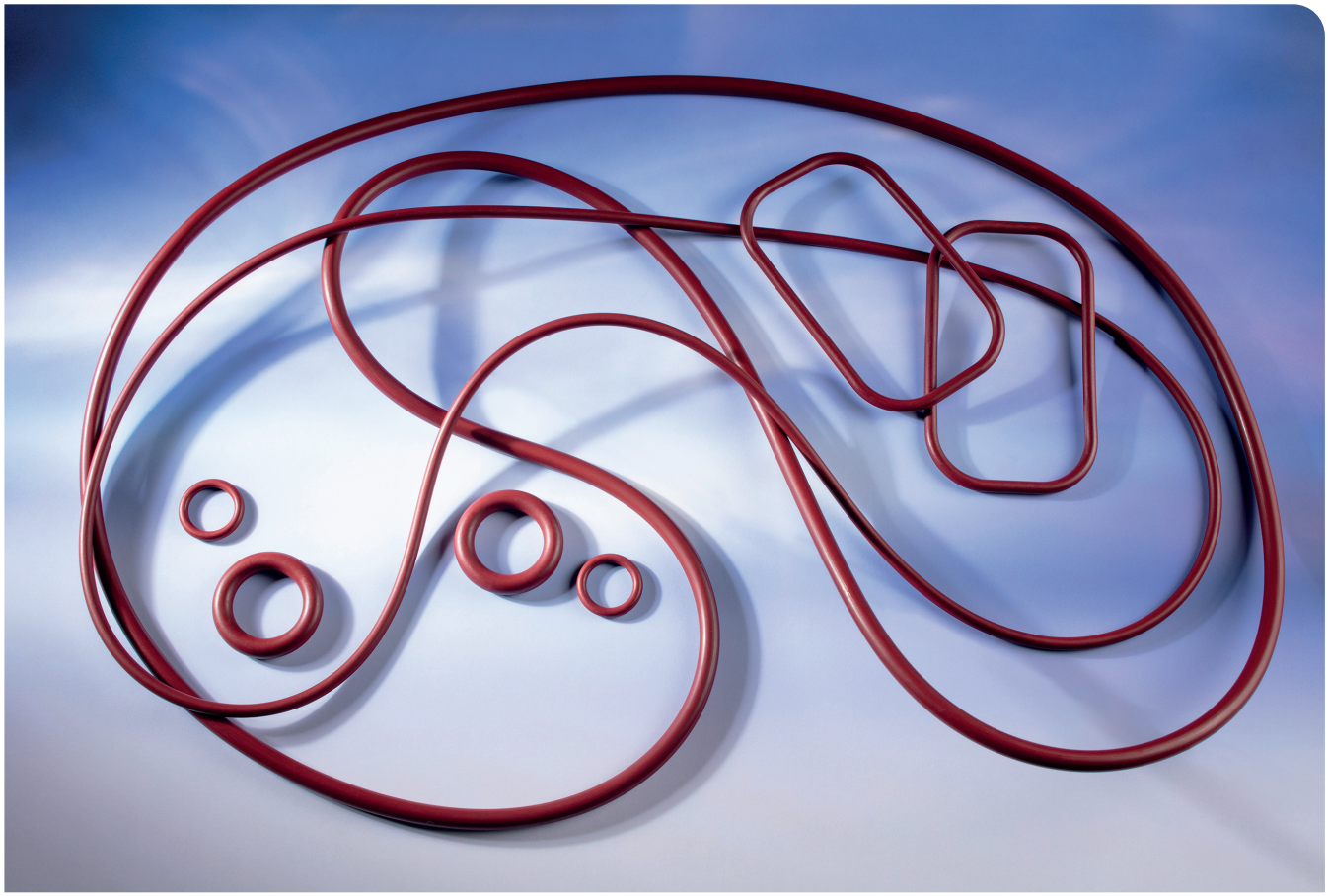
We'll keep working to iterate, improve, and deliver high-quality sealing solutions to elevate your semiconductor manufacturing process.

As a global leader in seals based on FFKM elastomers, we at Greene Tweed know that second-best seals aren't good enough in an industry as complex and challenging as semiconductor manufacturing. So, we decided to take action to minimize the impact of future disruptions on our customers' ability to manufacture chips

Where second best isn't good enough

Cut to 2023: While the semiconductor industry is currently experiencing a short-term cyclical downturn, the next year looks brighter with predictions pointing towards an upturn in the second half. These boom-and-bust cycles are bound to intensify uncertainty and create demand-supply imbalances. In these uncertain times, even a downturn cannot eliminate the potential for supply disruptions leading to tightness and a resultant surge in demand. As a global leader in seals based on FFKM elastomers, we at Greene Tweed know that second-best seals aren't good enough in an industry as complex and challenging as semiconductor manufacturing. So, we decided to take action to minimize the impact of future disruptions on our customers' ability to manufacture chips. We realize that the dynamic landscape of the semiconductor industry demands strategic planning and foresight and are proactively taking measures to create robust Business Continuity Plans (BCPs) and ensure a steady and uninterrupted supply. We began by conducting comprehensive risk assessments, identifying vulnerabilities, and developing contingency plans to mitigate potential disruptions. Following the deep exploration, Greene Tweed has rolled out four major initiatives to help us navigate this turbulent terrain, circumvent future disruptions, and secure a regular supply to help drive our semiconductor customers' continued growth and success:

- **Secure FFKM polymer supply**
  Our first step at Greene Tweed was to build strategic stockpiles of critical raw materials to prepare for the anticipated upturn. Securing raw materials is very important, but it's just one aspect of our multifaceted approach to ensure supply. Greene Tweed scientists are innovating to develop new products and reformulate existing



ones to prepare for the ever-evolving regulations and shifting market dynamics. We are proactively identifying risks from ingredients that are supply constrained and mitigating them with more readily available feedstock materials. At the same time, we are working with our supply chain partners to determine the potential impact of government reviews and supply crunch on their materials, chemicals, and production processes. Simultaneously, we are working with our customers to develop and validate alternate compounds with superior technologies and significant benefits.

- **Diversify supply chain**
  While reformulating and developing new products, we are taking proactive measures to diversify our supply chain and reduce the risk of overreliance on a single supplier or region. We realize that setting up multiple FFKM factories is too capital intensive and might not be feasible for our suppliers. That's why we are leveraging multiple suppliers to build a resilient and adaptable supply chain that is better equipped to navigate the challenges of an ever-evolving semiconductor landscape. To do this, we are developing equivalent products that serve as alternatives to the original ones. We carefully select compounds and source raw materials for two equivalent products from different suppliers located in separate countries. For example, we are augmenting our supply chain by adding Chemraz® G57 that is equivalent to Chemraz® 657 and provides excellent plasma resistance in a variety of aggressive chemical environments.

- **Expand manufacturing operations**
  We are also spreading our manufacturing footprint, strategically setting up factories in new locations across the world to help bring supply chain stability to the semiconductor customers. The latest is our upcoming manufacturing facility in Cheongju-si, Chungcheongbuk-do, Korea. Expected to be ready by mid-next year, it will initially be dedicated to our highest-performing elastomer Chemraz® product line that was specifically formulated for semiconductor applications. The state-of-the-art factory will not only increase our production capacity but also enhance flexibility and resilience in our supply chains. By decentralizing production and sourcing, we will be better equipped to manage supply crunches, overcome production bottlenecks, and maintain consistent deliveries to customers.

- **Boost operational capacity**
  In tandem with the expansion of manufacturing capacity, we have significantly stepped-up our inventory optimization by building the right inventory to meet future demand within industry leading lead times. Coupled with our new facility, this will help us grow our capacity and capability to better support the global demand for our products and bring enhanced supply chain stability to the semiconductor industry.

Our lead times: back on track

The results of building supply resiliency are already evident. We have been able to restore standard pre-disruption level lead times that our customers saw before geopolitical and regulatory events cause unprecedented supply chain issues – it's a testament to our resilience, adaptability, and customer-centric approach.

As we continue to forge ahead on this transformative journey, we are committed to keeping customer satisfaction and supply chain stability at the core of everything we do. We understand that our high-performance Chemraz® seals do what other seals can't do and timely delivery of our products is essential for our customers' success. Together with our customers and partners, we will continue to shape a resilient future that thrives on innovation and a custom collaborative approach that delivers certainty for our customers' crucial operations.

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- Based around a hot topic for your company, this 60-minute recorded, moderated ZOOM roundtable would be a platform for debate and discussion
- Moderated by an editor, Phil Alsop, this can include 3 speakers
- Questions prepared and shared in advance
- There would be an opportunity to view and edit out any unflattering bloopers

This event would be publicised for 4 weeks through all our mediums including:

- A banner on the Silicon Semiconductor homepage for 8 weeks
- 4x weekly dedicated HTMLs
- 4x news pieces which would also appear on the weekly e-newsletters
- Promoted through our social media platforms for 8 weeks (pre and post event)
- Available as an on-demand asset through all mediums
- All registered attendees' details would be made available to you

Cost: €5995

Contact: Jackie Cannon at jackie.cannon@angelbc.com

ANGEL EVENTS

New developments in underlayers and their role in advancing EUV lithography

Extreme ultraviolet (EUV) lithography is used to pattern the smallest features in advanced semiconductor devices. The demand for smaller devices with more capabilities requires industry innovation in EUV processes and materials.

By Joyce Lowes, Director, Emerging Materials Technology, Corporate Research and Development, Brewer Scientific.

ADDITIONALLY, EUV plays a critical role in the evolution of technology and enables the continuous advancement of the semiconductor roadmap, as it provides the capabilities of higher processing power while using less energy and providing higher performance. However, one of the biggest challenges facing EUV lithography is material requirements, recognizing the critical role underlayers play in the patterning of EUV lithography.

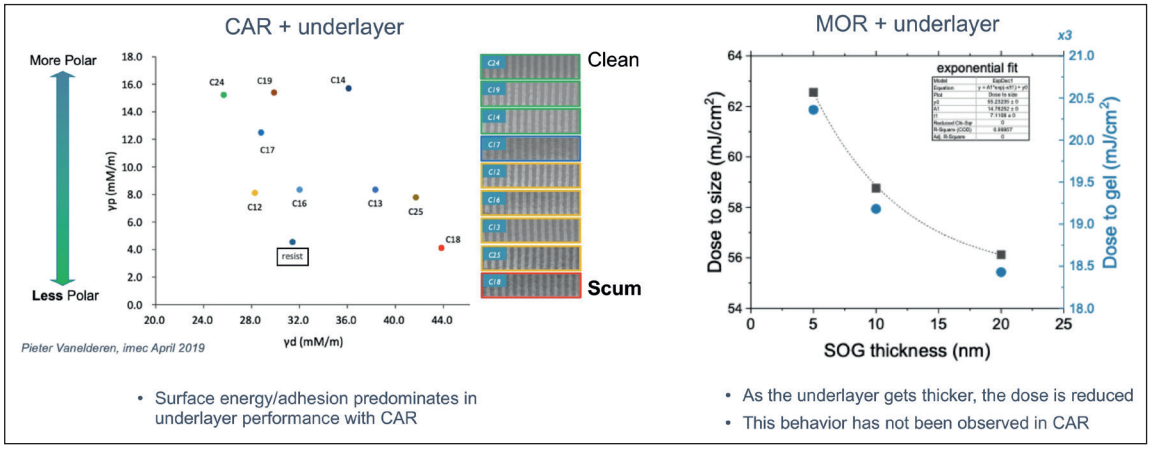
Unlike bottom antireflective coatings (BARCs), reflectivity control is no longer the driving mechanism for underlayers. Now, underlayers are necessary to support resist performance and to enable scaling of the process. Underlayers that offer optimum adhesion while ensuring minimization of pattern defects are key. Beyond just lithography performance, in cases where the underlayers also serve a dual purpose as an etch mask, they need to offer etch resistance beyond their predecessors and at a much reduced thickness.

Brewer Science introduced our first EUV underlayer material in 2010, E2Stack® AL412 material, which serves as the standard for EUV tool qualification and resist screenings. This material delivers excellent adhesion and resist compatibility for lithography. Since then, Brewer Science has introduced a variety of material approaches that offer process and defectivity improvements for traditional EUV lithography schemes. These materials demonstrate improved process window, depth of focus, and LWR/CDU, and can be used across a variety of EUV patterning applications.

Underlayer Challenges for EUV

With the adoption of EUV into more layers and the introduction of high-NA tools quickly approaching, the minimum pitch as defined in DRAM and Logic roadmaps requires photoresist thickness continue scaling down, reaching as thin as 15 nm in the next few years. As expected, the underlying film stack will need to scale as well, all while maintaining existing properties and often doing more.

The industry has already moved from traditional 30 - 80 nm deep UV (248 nm or 193 nm) BARC layers down to 5 - 20 nm EUV underlayers. This thinning-down trend will continue (likely towards 1 – 10 nm) as high NA becomes a reality. Meanwhile, to be able to print ever-shrinking defect-free EUV features



➤ Figure 1. Comparison of underlayer properties on traditional CAR and MOR.

with the lowest possible dose while maintaining reasonable process window, more functional demands are being added to the underlayer requirement list. Just to name a few, the underlayer needs to provide enough adhesion to prevent pattern collapse but not too much to cause scum, it needs to be as thin as possible but at the same time provide the required etch selectivity uniformly across a 12-inch wafer, and it is also called on to help reduce the dose but without too much chemical exchange with the resist. Overall, an optimum EUV underlayer design needs to have at least three main challenges in mind: enhancing the lithography performance with compatibility to a wide range of resist vendors and types, thickness and chemical homogeneity control to minimize both coating defects and stochastic impact to the imaging/developing process, and the perfect etch selectivity for pattern transfer demanded by different resist types and integration schemes.

Obviously, lithography performance needs to be perfect. When films are at a normal thickness, bulk properties have large influence over performance. However, with thin films, those bulk properties are less significant, since there really is no bulk left and behavior at the interface is more important. All of the desired properties need to be packed at the interface. Adhesion to and interaction with the resist at the interface needs to be optimized to get the right balance. And, unlike traditional ArF or KrF resists, each EUV resist from each vendor has its own unique chemical designs and working mechanisms, so underlayers need to be adjusted for each different resist formulation. More preferably, the underlayer needs to be "universal" to be compatible with all the resists.

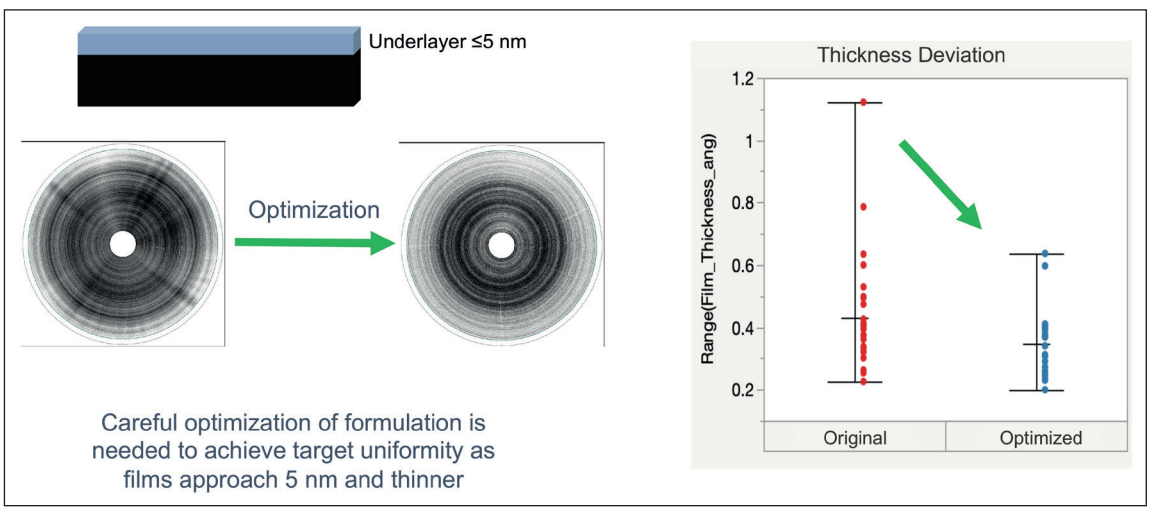
Reducing the thickness in itself is a critical challenge. At 5 nm, control of uniformity across the wafer is tricky, with the film sensitive to many factors in the tool, such as exhaust and hotplate uniformity. Compounding that as well are chemical effects, such as distribution of components and their effect on crosslinking rate. Even though the thin films are at very low solids content, defectivity reduction does not get easier. Tiny defects that were previously tolerable or even ignorable compared to the rest of the bulk film now become dominant and problematic at the interface. These defects now may start becoming larger than the thickness of film or CD of the features and so become more impactful. Traditional methods that were used to remove larger defects are running into a wall in the EUV era where everything shrinks in size and thickness, requiring more sophisticated filtration and other techniques to purify the materials, and more innovative metrologies to even detect the defects.

Lastly, there is pattern transfer. These ultrathin underlayer films will need to deliver at the same but more likely at a better level of etch selectivity than their much thicker precedents. This applies to both silicon- and carbon-based films. Depending on the integration scheme and etch setup, faster or slower etch rates are prescribed for the EUV underlayers, but sometime the underlayer needs to be both faster and slower (under different etching gases), all at a thickness as thin as 1 – 10 nm.

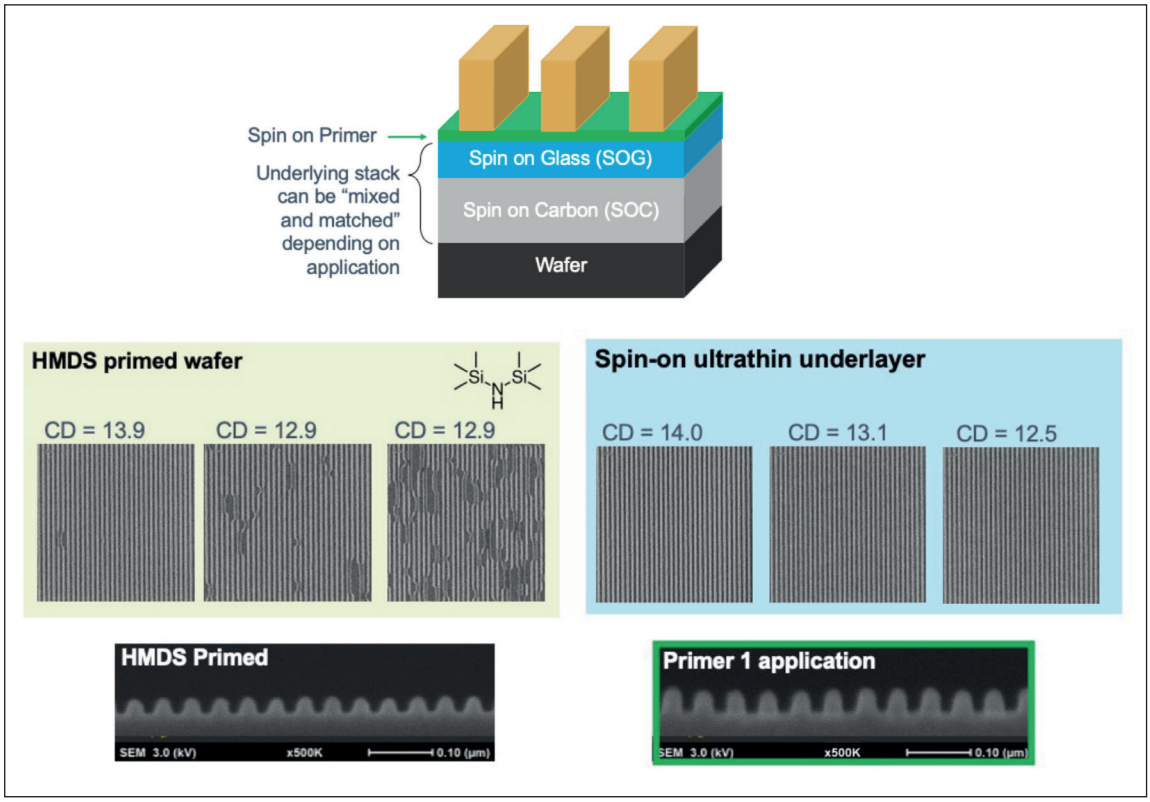
Underlayer Effects on CAR and MOR

In figure 1, two examples illustrating the role the underlayers play in EUV with a traditional chemically amplified resist (CAR) and metal oxide resist (MOR) are shown. With CAR, one factor at play for performance is surface energy. With this combination, as seen on the left, underlayers with various polarities were screened. As the underlayer became more polar, this change leads to less scumming/cleaner profiles. At lower polarity, scumming became more evident, likely due to too much interaction of the exposed resist and the underlayer. But, too much of a good thing is sometimes bad, so there needs to be a balance to avoid too little adhesion and causing collapse.

With the MOR, surface energy is important, and the collapse/adhesion trends are similar to CAR. Some impact on thickness versus dose has been seen, which was not observed with CAR. When



➤ Figure 2. Thickness uniformity studies.



➤ Figure 3. Primer concept and comparison of HMDS priming vs spin-on primer film.

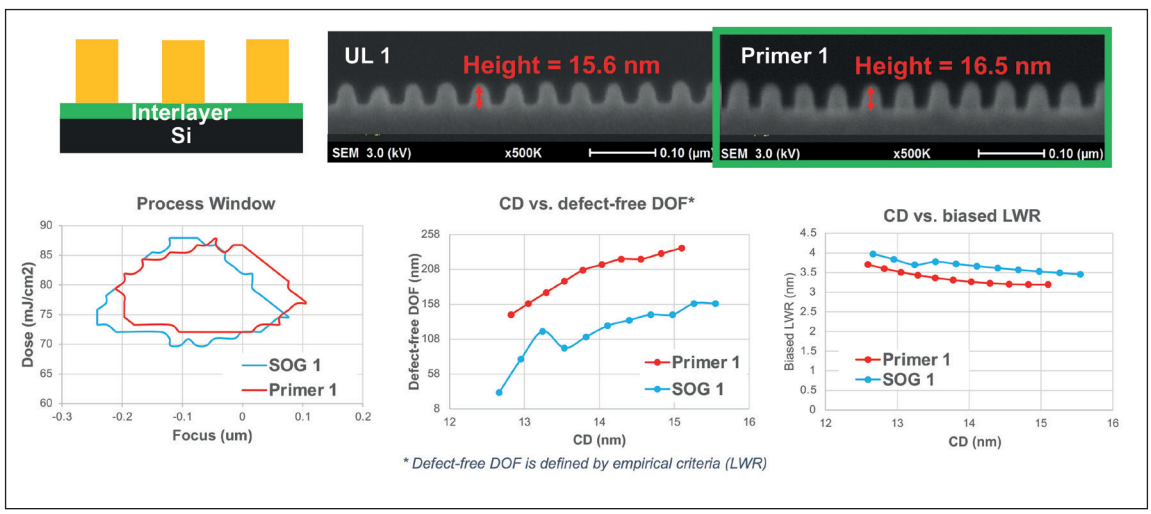
the underlayer became thinner, the resist required higher dose, which could be explained through some chemical interactions.

Tackling Thickness Issues for Extreme Uniformity

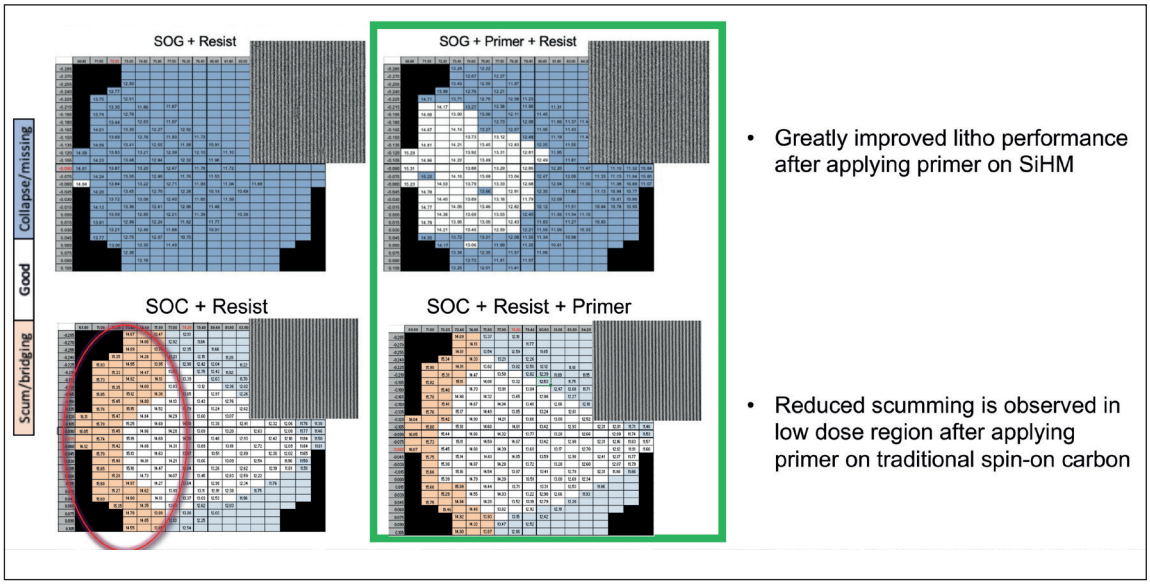
Coating uniformity at EUV dimensions requires extreme uniformity. At a normal thickness, for an ArF underlayer, thickness variation targets can be as low as 5 angstroms. At 5 nm, that same variation is still expected. Unfortunately, it's not as simple as repurposing a 30-nm film by diluting it and have it perform the same. Striations as seen in Figure 2 with the radial striations in the haze image from an SP5 on the left, and thickness deviation from center to edge are common problems that occur when the film is thinned, causing process window errors, CD mis-uniformity and other issues. To eliminate striations or to reduce thickness uniformity down to target, careful optimization of the formulation is necessary. And since all underlayers are not created equal, when the formulation changes for better adhesion, slower etch rate, or the need to replace or remove PFAS components such as surfactants, each material will need to go through another optimization step to fine tune its uniformity.

Underlayers for Adhesion – How Thin Can We Go?

As films get thinner, a question arose: how thin can a traditional spin-on film actually coat before it starts to fail? Does a spin-coated polymer film actually coat consistently across the wafer when thinned down? Is there enough polymer for adequate coverage? A



➤ Figure 4. Comparison of primer versus traditional crosslinked film.



➤ Figure 5. Primer on top of problematic underlayers.

few methods can be used to characterize the film and coverage across the wafer. Of course, thickness , but also density, roughness via AFM, contact angle and surface energy are used. Using this data, it was found that high quality films can be obtained down to 4 nm and likely even thinner.

With those same thin films, evaluation with both CAR and MOR was conducted at 28-nm pitch. With CAR, no change in dose or best focus and CD were seen as thickness was decreased. Roughness values varied a little bit, but overall performance was very similar. But again, overall, thin films were proven to work as well as their thicker counterparts.

Going Ultrathin – Spin-on Primer

So how much thinner can we go? If 4 nm works, why not 2 nm or even1 nm? One concept that has been borrowed from other areas may be a path to get the properties needed for performance but alleviate those issues seen with traditional crosslinked films. This spin-on primer concept can be used to functionalize a variety of surfaces including other spin-on films or CVD-deposited layers through just a simple grafting process. These types of materials have the ability to tune or adjust adhesive properties while allowing for truly ultrathin films.

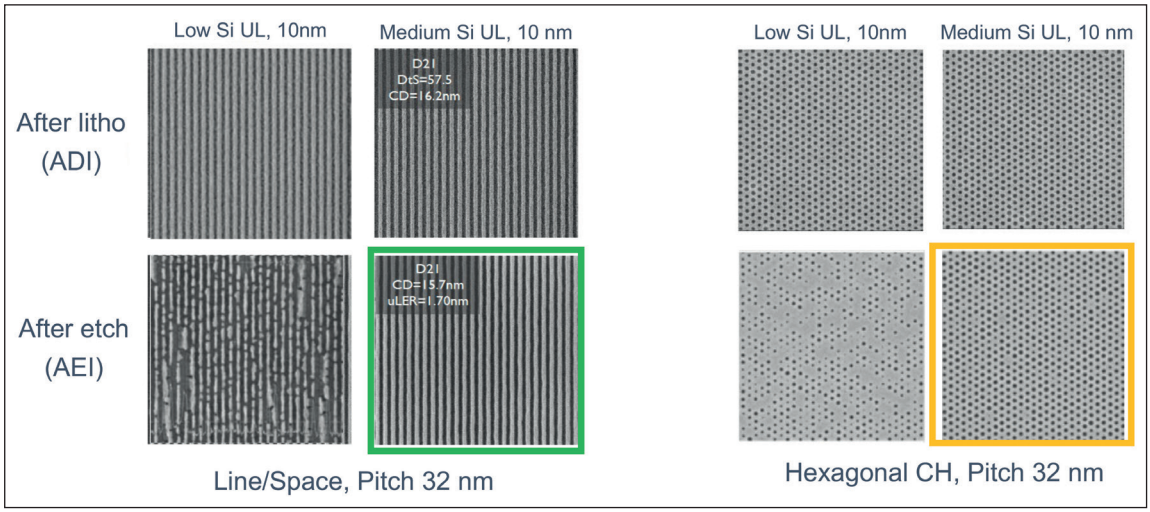
With this ultrathin film, it is important to verify that it is indeed uniform. In addition to just thickness uniformity, using those same characterization methods as before, including surface roughness and surface energy across the wafer, is is possible to ensure the film is consistent across the entire wafer surface.

Here are a few examples of how ultrathin layers will work with different film stacks. First, since this is a primer, it can be compared to the traditional HMDS primer applied on silicon. With the HMDS priming, lines will print with this resist, but adhesion is poor and collapse shows up early. Looking at cross-sections, the resist has quite a bit of top loss. With the spin-on primer applied onto silicon, no collapse is observed across dose and resist top loss is minimized.

Figure 4 demonstrates a comparison of a spin-on primer to a traditional crosslinked film at 5 nm. While the crosslinked film does perform well, replacing that layer with the thinner equivalent can lead to wider defect-free depth of focus window and better roughness. Less scumming and top loss is also observed.

And lastly, what does this layer look like when it is added on top of other layers? Can the primer be used to 'fix' an existing underlayer? In Figure 5 (top row), there is a traditional silicon hardmask that was not optimized for EUV use. Looking at the focus/exposure matrix, dose in the x-direction and focus in the y-direction, it can be seen that with this underlayer, the resist has significant collapse

This spin-on primer concept can be used to functionalize a variety of surfaces including other spin-on films or CVD-deposited layers through just a simple grafting process. These types of materials have the ability to tune or adjust adhesive properties while allowing for truly ultrathin films



➤ Figure 6. Silicon loading content studies.

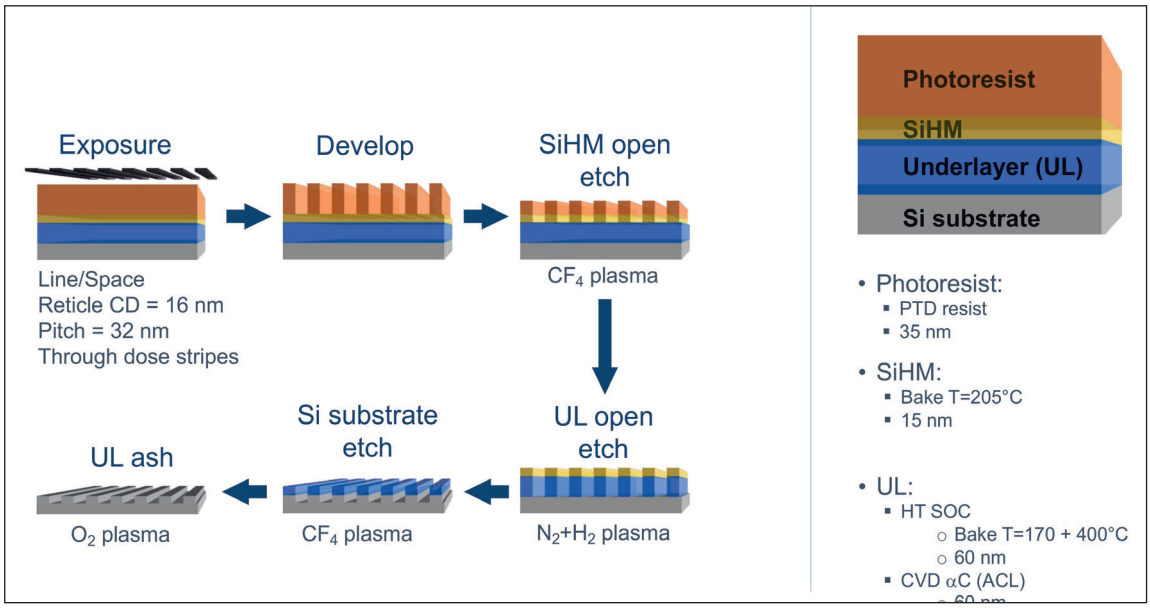
and line breaks as shown in blue, and possibly only one good die as shown in white, but it is probably questionable, too. Take that same layer, graft a spin-on primer with the right resist compatibility, and adhesion is fixed. Figure 5, (bottom row) shows what happens when a traditional spin-on carbon film is modified with the primer film. Original performance is not too bad, but there is a bit of bridging and scumming in the low dose region seen in orange. But with the spin-on primer, the bridging and subsequently the defect-free window is improved in that area.

Addressing Pattern Transfer – Silicon Hardmask

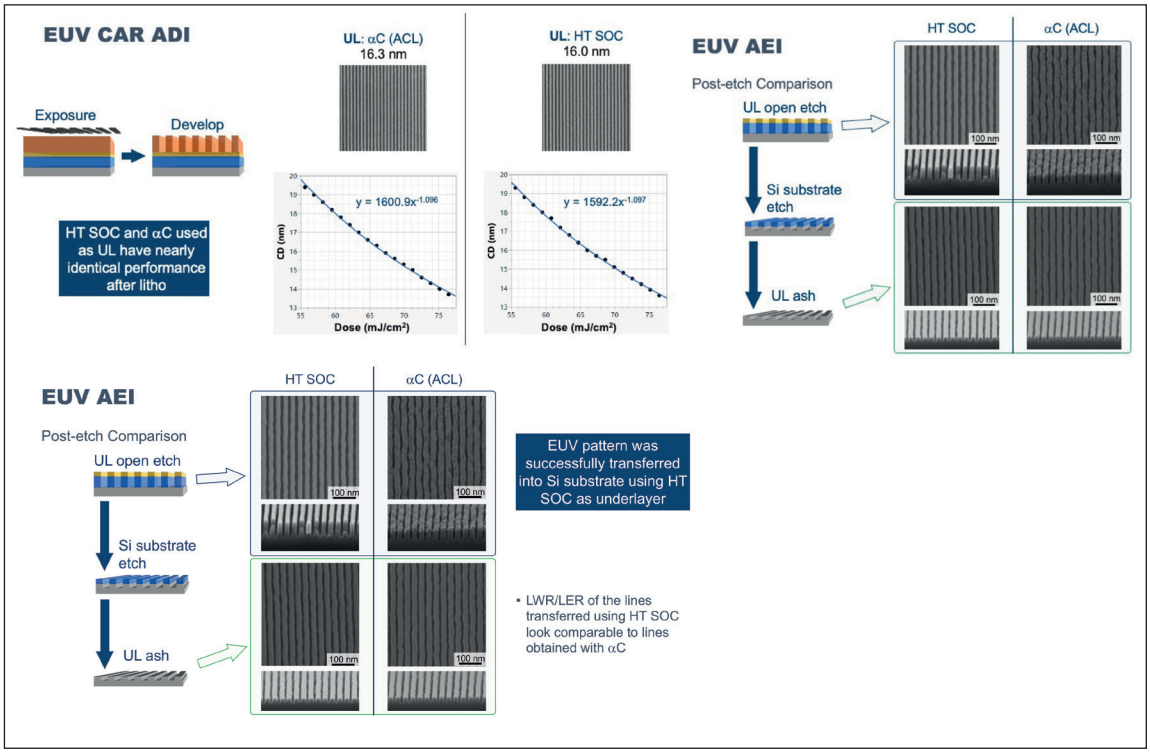
As the film stack gets thinner, maintaining adequate etch resistance is another main challenge. When films are not optimized, some familiar pattern transfer defects that crop up are missing holes, line breaks, wiggling and others. These could be caused by several things, including poor adhesion or scumming, but in this case it is important to review how inadequate etch resistance of the silicon hardmask causes problems.

How much silicon is ideal? Not all silicon hardmasks are alike and not all pattern transfer needs are the same. As seen in the line/space example in Figure 6, the low-silicon hardmask obviously fails, but a medium-silicon hardmask looks good. However, when using the same materials for contact holes, failure is seen with medium-silicon hardmask, indicating that better performance is needed.

As the move to even thinner silicon hardmasks proceeds, how much silicon is really needed, especially approaching 5-nm-thick films? The performance is all tied to etch rate. The higher the silicon, the slower the etch rate in oxygen, and consequently, the longer the hardmask lasts during the carbon etch. Traditional silicon materials typically range in the medium to high level of silicon, which would allow for use between 7-10 nm in most cases. However, getting to higher silicon has been difficult for multiple reasons, including chemistry and defectivity, but new materials are now able to get to levels that will enable 5-nm etch equivalence and maybe even beyond.



➤ Figure 7. CAR pattern transfer flow process.



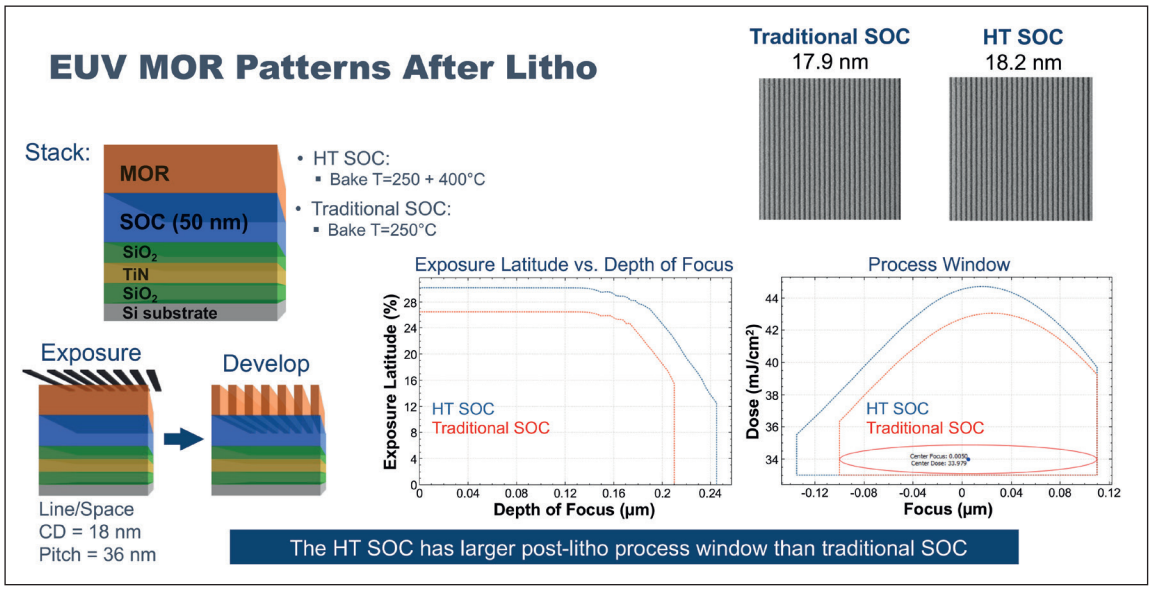
➤ Figure 8. ADI and AEI results with CAR resist and HT-SOC.

Addressing Pattern Transfer – Carbon Hardmask

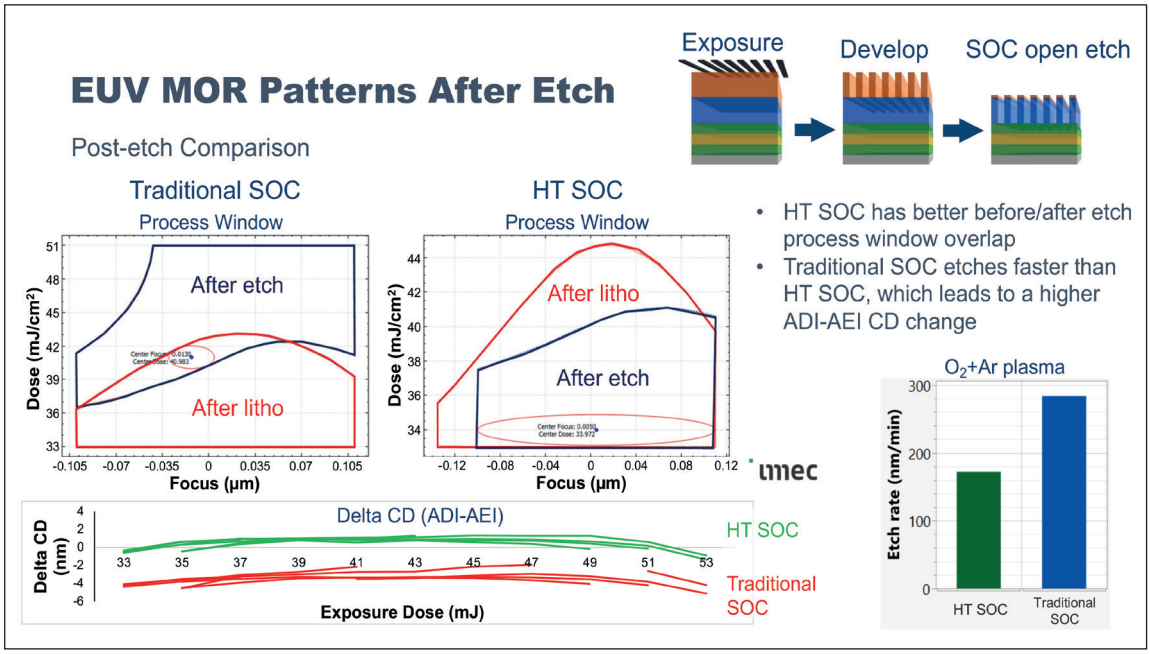
With silicon taken care of, how about the carbon hardmask? The most logical way to provide a carbon underlayer has been to use alpha carbon or other films, but in certain applications, there may be limitations to what those films can do, such as planarization, gap-fill, optimized resist adhesion, or reworkability, so the use of a spin-on option with optimized etch rates may be needed.

To check the effect of variations in the carbon layer, a standard pattern transfer flow using a CAR and EUV lithography is used. In Figure 9, a simplified stack and flow for checking the pattern transfer capability into a carbon layer using EUV patterning in shown. In this example, a standard silicon layer is coupled with different carbon films, and the lithography and etch steps are performed before checking for wiggling and other failures. After lithography, both alpha carbon and a high-temperature spin-on carbon (HT-SOC) films have good almost identical lithography performance. Dose and process window is similar. This is not unexpected since there should be minimal impact from a layer buried beneath the silicon hardmask.

Moving on to the next step, after etch is the key to checking for differences. This is where line wiggling is typically apparent. With some older generation films with lower carbon content, it can be very difficult to obtain patterns at EUV wavelengths. But, with high-temperature carbon materials, like



➤ Figure 9. Pattern transfer data (ADI) for MOR plus SOC layer.



➤ Figure 10. SOC etch rate and lithography comparison (AEI) for MOR.

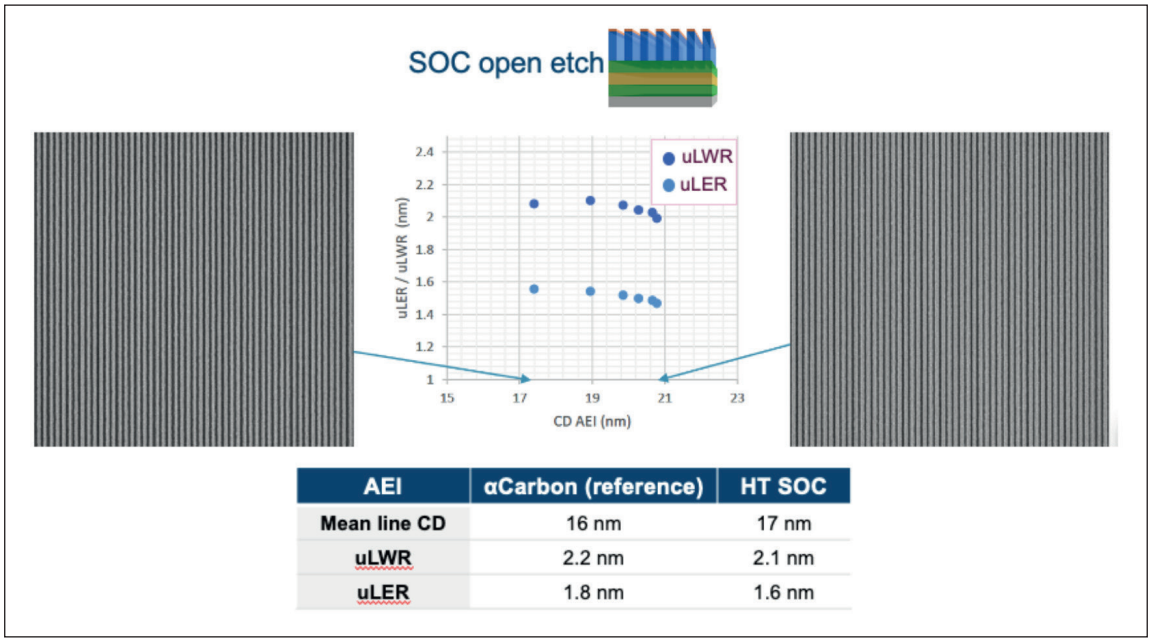
OptiStack® SOC450, that were designed with higher carbon content, there is enough etch resistance to perform similarly to an alpha carbon film, as shown in Figure 10.

Pattern transfer with CAR is well known, but MOR is different and the stacks used will vary from a typical CAR. In this example, the carbon film is directly under the resist, so planarization or other properties might not be needed, but it still serves two functions, adhesion and etch resistance. In Figure 8, a traditional spin-on carbon is compared to a high-temperature/high-carbon film. As discussed previously, litho performance is highly dependent on resist interaction, so those differences in the changes in process window and exposure latitude are apparent, but not terrible and the process can proceed to etch.

After pattern transfer, the impact of carbon film composition on performance with MOR is apparent.

In Figure 10, a comparison of etch rates shows that a traditional SOC is faster than the higher-carbon/high-temperature alternative. With that faster-etch-rate material, the CD delta changes significantly, as shown on the bottom chart in red, reducing the process window as seen on the left. With the slower material (high-temperature carbon), there is still some slight CD change, but far less and the overlapping process window is much better..

Finally, it is necessary to analyze how these materials perform for roughness and subsequent overlay. Under the MOR, LWR and LER for the high-carbon spin-on film are comparable to alpha carbon.



AEI	αCarbon (reference)	HT SOC
Mean line CD	16 nm	17 nm
uLWR	2.2 nm	2.1 nm
uLER	1.8 nm	1.6 nm

➤ Figure 11. Alpha carbon vs HT-SOC (AEI) with MOR.

All roads lead to Arizona

Arizona Commerce Authority's President and CEO, Sandra Watson, explains the long-term strategy that has led to Arizona becoming a premier location for the global semiconductor industry - with a skilled talent pipeline and ongoing supply chain development efforts, two of the key elements that have attracted global semiconductor leaders that have added to the state's over 200 semiconductor companies, with more in the pipeline.

PA: *The obvious place to start would be with a little bit of background on the Arizona Commerce Authority, how long you've been in existence, any key milestones to date - what it is you've been doing?*

SW:
The Arizona Commerce Authority was established in 2011. It was established because of the need to diversify our economy. In 2008, with the financial collapse, Arizona was facing some very serious challenges. Our economy was built on growth in construction and the service industry and we needed to ensure that we were diversifying our economy so that, with any future recessions, Arizona would not suffer from some of the challenges that we faced in 2008.

Governor Brewer chose to bring business leaders together to determine a new course of action for the state's economic development strategy. And as we assembled business leaders within Arizona, we also did substantial work and analysis, looking at best practices across the country. As a result, we recommended a new organization called the Arizona Commerce Authority, which required legislation, and Governor Brewer called a special session and within three days we had established the Arizona Commerce Authority and we began running full operations in July of 2011.

➤ Intel-Chandler's, Arizona Ocotillo Fab

PA: *In terms of the semiconductor industry specifically, I'm intrigued. Was there a base of semiconductor companies in Arizona which the Commerce Authority then thought, hey, this is a booming industry or a growing industry, let's see if we can promote it more? Or did the Commerce Authority say, hey, the semiconductor industry is where it's going to happen in the future, so let's see if we can create an industry within the state?*

SW: The Arizona Commerce Authority's mission is very focused on creating a diversified sustainable economy in Arizona. We have had strength in the semiconductor industry, aerospace and defense and other manufacturing operations throughout the state. The one area that we really wanted to focus on is building up Arizona's advanced manufacturing base. As we looked and evaluated the strengths that Arizona had and the opportunities in the future, we did zero in on the semiconductor industry. And there are several reasons why.

In 1950, Motorola began its operations here in Arizona, which really started to begin an opportunity for Arizona to grow not only its advanced manufacturing industry, but also start to attract suppliers to support Motorola's operation. In 1979, Intel launched its first fab in Arizona. So, we began to develop a strong presence of the semiconductor industry here in Arizona. And with the work that Motorola was doing in our state and Intel, we started to be able to attract suppliers to support both of those companies and began to grow an industry in Arizona that was very focused on the semiconductor industry. When we created the Arizona Commerce Authority, we wanted to build on the success of the industry and look at opportunities to grow the semiconductor industry here in Arizona.
In 2013, a few years after we established the Arizona Commerce Authority, we actually began to develop relationships with many companies outside of the state, in particular TSMC. At that

time, Governor Brewer and I visited Taiwan and began conversations with them, developed a strong relationship and continued that relationship up until their announcement in Arizona in May of 2020. We've now got over 200 direct suppliers in the semiconductor industry and thousands of other suppliers who support these industries each and every day.

PA: *And you offer various programmes for businesses – can you give us a flavour of the incentives you offer, the ways you can help businesses if they're looking to move towards Arizona?*

SW: Arizona offers a complete package when it comes to working with industry. We not only focus on Arizona's quality of life, but our friendly business environment, our light touch on regulations, our ability to attract and grow talent and really develop a modern infrastructure. We also do have some financial programmes that support these industries. We have refundable tax credits, some other tax credits that are all focused on job creation.

So, everything we offer a company from a financial standpoint, is all performance based. We work with companies to understand what their investment is, how many jobs they'll be creating in our state, and then we're able to put a package together to help support their growth and ensure that Arizona and the company that is locating in Arizona is successful moving forward.

The other factor that is, I think, incredibly important to every company out there, especially today, is workforce. It's really important for us to be working very closely with companies to ensure that we're meeting their talent needs. And by doing a complete assessment of what those needs are, we actually work very closely with our higher ed community, our universities and community colleges to ensure that they're producing the talent that is necessary for those companies to be successful.

Our universities are doing incredible work. They have developed strong programmes in engineering, and ASU, as an example, is considered the most innovative university in the country eight years running. And they have grown their engineering school from about 10,000 students enrolled, maybe ten years ago, to over 30,000 students enrolled in their engineering programmes today, and that continues to grow. UArizona is doing a tremendous amount also in increasing their engineering talent. We're also working very closely with our community colleges to ensure that the employers in our state have the technicians and the operators that they need in order to continue to realise their employment opportunities. One of the really exciting programmes that we just launched in partnership with Maricopa Community Colleges and the semiconductor industry, it started with Intel, now TSMC is a part of it as well.

And Maricopa Community Colleges have been leading this effort in creating the Semiconductor Technician Quick Start programme. In the last eight months, they've already run 600 students through that programme. And that is intended to give potential new employees an early start, a quick start into the industry, understanding what the needs are from a semiconductor standpoint. So, there's a lot of activity. We're also doing a number of new things, that we're ramping up these workforce accelerators in partnership with our community colleges and industry to ensure that we're developing very strong centres of excellence to train potential new hires through these accelerators.

PA: *I was going to ask for semiconductors, the three S's, which are skills, sustainability and supply chain. I think you've probably covered skills. So, your thoughts around sustainability and supply chain?*

SW: Absolutely. Here in Arizona, we have a very robust supply chain in place to help support the semiconductor industry. But we are always looking to identify if there are gaps within the supply chain.

Our focus is to attract companies to help support those industries. We have over 200 companies that are direct suppliers to the semiconductor fabs. In addition to those 200, we also have thousands of suppliers that are helping to support not only the semiconductor industry, but many of our advanced manufacturing companies. We have mapped out our entire supply chain to really develop a very comprehensive strategy to ensure that our companies here in Arizona have the goods and services they need to continue to grow their operations.

We have worked with over two dozen new suppliers that have just landed in Arizona within the last two years. And we have several other suppliers in our pipeline that we're currently working with. Our focus is always to work with the existing companies that are currently here in Arizona looking to see what their needs are and then either growing that opportunity here in Arizona or looking to attract

➤ Governor Katie Hobbs was joined by the Arizona Department of Occupational Safety and Health (ADOSH), Taiwan Semiconductor Manufacturing Company (TSMC), and workers to sign a Voluntary Protection Program (VPP) covering the TSMC Arizona construction project. Currently, nearly 12,000 workers support this north Phoenix project each day, and the VPP applies to all contractors on the site

➤ A vision to transform acres of state-owned desert into a global technology epicenter marked a major milestone when Governor Doug Ducey and TSMC celebrated the first piece of equipment added to one of the most technologically advanced chip factories in the world.

those companies to ensure that we have developed a very comprehensive supply chain opportunity for these companies.

PA: *And on the sustainability front, I mean we're all aware of the climate volatility - I think in Arizona at the moment, for example, the temperature you're experiencing record or near record. But do you have programmes as well to encourage the people that come to you within the state to take their sustainability responsibility seriously and you give them help to do so as well?*

SW: Yes. Our companies in Arizona are very focused on sustainability. Many of these companies have policies in place to ensure that they're using resources efficiently and effectively and working with the community. We have examples of companies like Intel, which has a goal of being water neutral by 2030. We have several companies in Arizona, including TSMC, who are building state of the art water reclaim facilities to ensure that they're using water efficiently. With new technology today

We brought in over 50 industry players from all over the country and we established a National Semiconductor Economic Roadmap Committee to develop a national strategy that would ultimately complement and support the federal legislation. As we brought industry together, we convened meetings over the course of 18 months to really understand what the needs were from industry and how we could help support them, not just here in Arizona but around the country

and with the relationships and partnerships we have throughout the state, companies are coming up with solutions to ensure that they are utilising these resources in an efficient way so that we can continue to develop a very robust economy.

PA: *In terms of the fairly recent the US Chips Act, I'm just wondering, and it may be a stupid question, but have you noticed any difference, if you like, pre the act and then after it, have you noticed any (presumably) increase in activity?*

SW: Well, it has greatly impacted the amount of activity that we are seeing here in Arizona - The CHIPS Act and the opportunity to partner with the federal government to ensure that resources are being utilised to develop new opportunities and create a leadership position here in the U.S. Not only from a production standpoint but really focused on both national and economic security. As we saw during the pandemic, there was a shortage of chips and it's very important that the U.S. continues to develop chips and the production of chips to maintain a leadership position in this industry. The CHIPS Act has really been instrumental. My gratitude to Secretary Romando, the entire Chips office, the administration and the work that our senators have done and continue to do. Senator Kelly and Senator Sinema here in Arizona have been very instrumental in ensuring that not only did the CHIPS Act pass, but that also that Arizona continued to stay very focused on how we could support this industry. As a result of the CHIPS Act and the funding, Arizona began discussions to ensure that we were developing a strategy that complemented the federal programme. And quite honestly, prior to, because the CHIPS Act was negotiated over a number of years before its passage, we began having discussions with Industry.

We brought in over 50 industry players from all over the country and we established a National Semiconductor Economic Roadmap Committee to develop a national strategy that would ultimately complement and support the federal legislation. As we brought industry together, we convened meetings over the course of 18 months to really understand what the needs were from industry and how we could help support them, not just here in Arizona but around the country. And as we began to have those conversations, when we developed the idea and the strategy to bring these industry leaders together, we really wanted to make sure that this was an industry led initiative, that ultimately industry was coming together to develop its roadmap to ensure that they had what they needed.

Along with the funding from the federal government to continue to grow the semiconductor industry here in Arizona, we had strong partnership with SIA and SEMI, both national organisations who are doing incredible work supporting the industry and really leading the charge to ensure that Arizona and the U.S. maintains a leadership position in this industry. As a result of all of that work and the partnership

with the national associations and several other states who got involved in this process with us, we were able to develop and publish a roadmap that was launched in December of 2022.

That roadmap centred around four key areas - supply chain, which is critical to the industry and we need to continue to develop a very robust supply chain to support the industry. Talent - critical in any expansion. And our focus around talent, is working with our educational institutions and thinking about apprenticeship programmes and on the job training and working with higher ed, but also looking at the high schools and elementary schools to ensure that we have and develop programmes that get kids excited about a career in the semiconductor industry. So, talent was obviously a strong topic of conversation and clearly a key focus of the roadmap. areas also equally important are infrastructure, ensuring that the U.S. has the infrastructure necessary to support the growth of this industry. So, infrastructure can be a term broadly used, where most people think of infrastructure as utilities and water and a whole host of other utility and infrastructure roads, but also research and development infrastructure in making sure that we have the research and development opportunities and institutions to help support the future advancements in this industry and looking at developing new innovative technologies to support the industry.

Infrastructure was broadly discussed largely in the R and D realm, but also with the other factors of infrastructure. And then the last piece, which is really critical, is entrepreneurship. And this industry, as you can imagine, because it's so capital intensive that it is difficult for entrepreneurs to establish themselves in this industry because the costs are so high. The barriers to entry are very high. So, the strategy was to focus on entrepreneurships and helping entrepreneurs find access to some of these research facilities. Creating a strategy to help entrepreneurs both on the capital side - access to capital, but also access to equipment and tools and opportunities to work in a collaborative way with our universities or with businesses and giving them access to some of these shared facilities. These four areas - supply chain, infrastructure, talent, and entrepreneurship - were key to develop a very strong roadmap going forward to help support and complement the federal investment that is being made.

PA: *In terms of the fruits of this strategy, you mentioned TSMC earlier, and you said you went for a visit, and then a few years later, they arrived. Clearly, there was a lot more went on, can you just give us some outline of that journey to get them to Arizona? And are you having ongoing conversations with them as to what's next?*

SW: TSMC is a global leader in the industry. In 2013, Governor Brewer and I visited Taiwan. We had our first visit with TSMC. At that time, they did not have a project that they were considering in the U.S. And our intent there was to educate them on Arizona should they have an opportunity in the future. We visited with them, we shared Arizona's story about the current semiconductor industry here at that time. In addition, we lett them know how our community has developed and our support for not only this industry, but for advanced manufacturing across the board.

We provided information on our business climate and our regulatory environment, both very friendly to businesses to ensure that they had a full understanding of what Arizona could offer should they consider an operation in the U.S. As we continued that conversation, we talked a lot about talent and the importance of talent to the industry and the great work that our universities are doing here to ensure our companies have the talent they need to grow. And the university talent, especially from an engineering standpoint, and the explosive growth that we have seen, especially with ASU's continued expansion of its engineering school.

Our intent in 2013 was to share Arizona's story and start to develop a relationship. That relationship continued over several years. In 2017, they decided to come visit Arizona. And at that time, Governor Ducey and I had an opportunity to meet with the executive team and also share additional information about Arizona, show them around and look at potential opportunities within Arizona. It was in 2020 when they made a commitment to establish their facility here. At that time, they were talking about one fab – we were excited to have them announce that in May of 2020. And then shortly thereafter, they announced fab two - for a total investment of $40 billion for both fabs and the creation of 4500 new jobs. These relationships are important, and it's important, at least from our standpoint, to share Arizona's story with companies so that they know what Arizona offers when they are making those decisions to establish an operation in the U.S.

➤ Edwards Vacuum grand opening took place in Chandler in April 2023

PA: *You've already mentioned the education part. In practice, Arizona State University and Applied Materials have fairly recently announced a Materials to Fab Centre. So again, were you instrumental in bringing those two together?*

SW: We are so excited about the announcement that was made with Applied Materials, ASU and the ACA. It was a partnership in working together to ensure that Applied Materials had the resources they needed to establish this Materials to Fab Centre of Excellence at ASU, bringing in the latest state of the art tools to begin. Obviously, a testing centre is important to Arizona and to the country. So that as we continue to grow this industry, the research and development, especially from the new tools, is going to help grow this industry. So that partnership was an exciting opportunity for Arizona because it allowed us to continue to focus on developing our research infrastructure, and having a global leader like Applied Materials as a partner was just incredibly important. We're excited about the relationship and the partnership and we're certainly looking forward to the future opportunities that that partnership brings to Arizona.

PA: *And I've also noticed that you've opened offices in both Korea and I think Taiwan. Was the main reason for this to do with the semiconductor or at least the tech industry?*

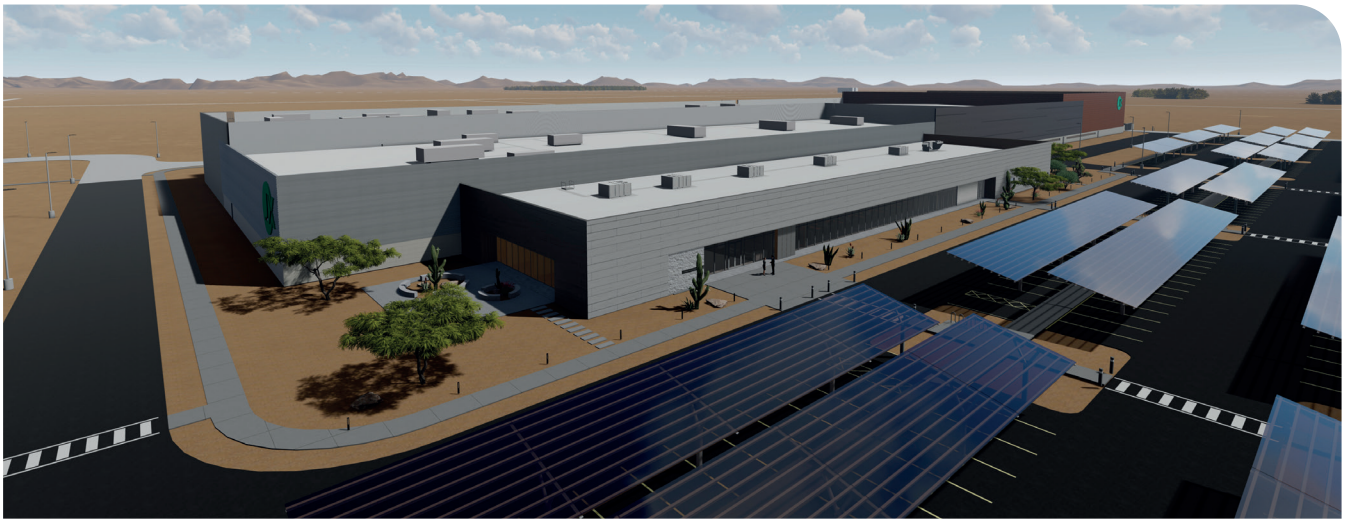
SW: We officially opened our offices in Taiwan and in Republic of Korea just this past year. And we have been developing a global strategy for many years, obviously looking at opportunities not just within the U.S., but also globally on how to grow our base of manufacturing opportunities. Taiwan and Republic of Korea are our latest offices. We have also an office in Germany, we have an office in Israel, three offices in Mexico. We've been focused on an international strategy for quite some time. The relationship with the businesses in Taiwan and the government of Taiwan was an important relationship that we had established many years ago. So that relationship was underway, but it was important for us to have someone on the ground in Taiwan and in Republic of Korea.

The opportunities in working not only with TSMC, but with other businesses within Taiwan is critical to advancing our strategy here in Arizona. The business attraction piece - we call that the FDI (foreign direct investment) opportunities - is important in our overall strategy, but just as important is the trade opportunities and making sure that Arizona companies are able to develop relationships with companies in both of those countries to ensure that we are providing a supply chain opportunity as well. Trade and investment are the two key factors and components of the programme.

PA: *And I am also intrigued to see that SEMICON West, which traditionally has had one home, has announced that they will alternate venues, with the 2025 event (and every other year after) coming to Phoenix, I believe?*

SW: We're incredibly excited that SEMICON West will be establishing a presence here in Arizona in 2025. We're looking forward to partnering with them to launch their very first conference outside of California. So, again, that partnership is critical and important. And as we began to develop these strong relationships with the national associations, SEMI has been amazing to work with and a strong leader in advancing the industry here in the U.S.

Those relationships and discussions continued and we assembled a team here in Arizona led by the city of Phoenix, Visit Phoenix, a few other organisations in Phoenix, the Greater Phoenix Economic Council and the ACA, and we collectively had discussions with SEMI to see if it was possible to have an alternating conference here in Arizona. So those conversations obviously were successful. That announcement was made and we could not be more proud and grateful to SEMI for working with



➤ JX Nippon Mining and & Metals had a groundbreaking ceremony for its facility in October 2022

As an example, these workforce accelerators, we know how important talent is and the ability to attract talent and grow talent are clearly foundational for every single company we work with. And by listening to industry and understanding what their needs are, we're able to work with our partners, universities, community colleges and other state partners who are helping to develop a strong set of programming to support these industries.

us and looking to Arizona as a partner in helping to grow the industry nationally. We believe that, with the robust activity happening here in Arizona, not only with the strong base of companies that we currently have to support the industry, but also the interest that we have from domestic and international companies to establish their operations or grow their operations in Arizona, we believe that having a partnership with SEMI and the conference here will help us grow the prominence of the industry nationally.

PA: *In terms of other companies, you've mentioned, I think it was 200 you attracted over the years. In terms of the recent ones, are there any of those that you are particularly proud of attracting for whatever reason? Or are you just delighted every time a semiconductor company arrives?*

SW: Every company that lands in Arizona is a win. We are focused on ensuring that we develop a very robust, comprehensive ecosystem to support the industry. Our focus is on working with industry to support not only the semiconductor industry, but all advanced manufacturing companies in our state. We're seeing a tremendous amount of activity in battery and electric vehicles as well, and other advanced manufacturing sectors. But the semiconductor industry is clearly one of our most important industries, along with aerospace and defence.

We've got a very strong presence here as well. But the semiconductor industry, for a whole host of reasons, is critical not only to Arizona, but to national security and the economic security of the country. Every single win, large or small, is important to us. And we don't necessarily look at a company and evaluate a preference of this larger company versus the smaller companies. We know that this value chain for the industry is so important and that we need all of the businesses together to be successful. Every single win that we have announced, we've been excited about, and we celebrate. And we've got several others in the pipeline that we hope to announce very soon.

PA: *One would almost have thought with all the activity going on, it's almost as if organic growth takes over. I'm not saying you could shut your office, but you've got to that critical mass where people go, well, if we need to establish a base or expand within the US, then Arizona is the obvious place to go. I'm sure you're not complacent, but what else are you working on? You say you've got some deals in the pipeline, are you looking to attract more fabs? Do you think that's important? And then you get all the supply around that. Just anything you can share as to future objectives?*

SW: Absolutely. Arizona's strategy is very intentional. We have developed a strong base of semiconductor companies here in Arizona, but we are also looking at the entire ecosystem, the entire industry, and we continue to reach out to companies and develop proposals to support the industry, so new companies coming in and helping Arizona-based businesses also grow their opportunities. We will continue to develop a very strong strategy to continue to bring new companies in, and support our existing industry. We also are ensuring that we're developing a strong foundation for these companies along talent, infrastructure, our business climate.

We're always looking at developing new opportunities. As an example, these workforce accelerators, we know how important talent is and the ability to attract talent and grow talent are clearly foundational for every single company we work with. And by listening to industry and understanding what their needs are, we're able to work with our partners, universities, community colleges and other state partners who are helping to develop a strong set of programming to support these industries. These workforce accelerators are critical to ensuring that these employers have the talent we need. And most of the activity we do is very centred around the needs of industry.

We listen to what industry needs are, we work with partners within the private sector and then develop these strategies – these programmes would not be successful without the partnership of the private sector. Each of our initiatives are designed around private sector partnerships and how we can work together collaboratively to ensure that they've got what they need. We also have developed a task force here in Arizona to help support the semiconductor industry. We created the Semiconductor Task Force to look not only at the federal programming and the opportunities to attract those research dollars that are part of the CHIPS Act, but also to support the existing industry.

We're always looking at ways to ensure that we're bringing industry together, understanding what their current needs are, understanding what their future needs are, and then developing solutions to help support those industries, whether they're state focused, federal focus or global issues. We're having those conversations with industry.

PA: *Finally, the semiconductor industry is going to be a $1 trillion industry by 2030? In terms of the challenges and opportunities, you've mentioned skills a few times and I think everybody in the wider It industry is aware of the problem - do you think that's the number one challenge or are there others? And the opportunities from now until 2030, for Arizona to be a crucial part in helping the industry get to that target?*

SW: Here in Arizona, we are focused on providing solutions. The shortage of talent is a global issue. And no matter where you are, whether it's the U.S. or in another country, every company is looking at ways to help develop new programmes to upgrade skills to bring in populations that aren't currently in the labour market, and looking at ways to create a variety of entry points for individuals who are interested in pursuing a career in the semiconductor industry. I will say that talent is probably the number one issue, but it is global. But here in Arizona, we have some solutions. And we've been working very closely with our industry partners, and through the great work of our universities and our community colleges and the partnerships we have with industry, we've been able to ramp up the engineering, as I mentioned, sort of the engineering schools, especially ASU, and their incredible growth in engineering and the great work that they continue to do. But we also have our community colleges engaged. And so in Arizona, you can attract talent to the state because it's this wonderful place to live. Our net immigration leads the country - there's a lot of new talent moving in on a daily basis. And we have an infrastructure in place and we are working with all our partners to grow talent and to ensure we're meeting the future needs. We focus on solutions to some of the challenges and we're very excited to be working directly with industry, understanding what their challenges are and then developing a collaborative effort to support those industries.

The last thing I will mention, because supply chain clearly is important as well, and we have established a supply chain consortium. We have called out to all of our suppliers in Arizona and also those that may be considering Arizona as a location. And we've developed a supplier consortium so that we can begin to work with our suppliers and create the same opportunities that we are doing for the semiconductor industry and all these other industries to ensure that our suppliers have what they need to meet the needs of their customers.

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Time to celebrate and accelerate diversity, equity and inclusion

Laura Silverstein, Technology Development Integration Engineer at GlobalFoundries' Essex Junction, Vermont facility, was recently recognised as GF's DEI in Inventorship Champion – awarded for hard work in creating a new and more diverse generation of inventors. Silicon Semiconductor Editor, Philip Alsop, finds out more about her career to date, her current role at the company and her thoughts on diversity, equality and inclusivity in the semiconductor industry.

PA: *Have you always wanted to work in the semiconductor industry? And the second question, which might be answered by the first, is, what did you know about the industry before you joined it?*

LS: I'll admit I knew nothing about the semiconductor industry until I got the interview and got the job! My degree is in chemical engineering, and I heard there was a fab in the Burlington, Vermont area that was hiring chemical engineers. And I was looking for a technical job after my undergraduate degree and was excited to live in Vermont. So, I met up at the career fair and hit it off and interviewed, actually in New York, and then interviewed up here and started working at this fab right out of college. But I knew nothing about computer chip manufacturing at all. I wasn't even sure if they cut up the wafers into chips, but I knew I probably shouldn't ask that at that point!

➤ (Left): One of the things that I think that I love most about the semiconductor industry is that it's so complex nobody can know it all. It's impossible. You can't possibly know every detail of every piece of equipment that's used to make every device and every level and how it's working.

PA: *Were you looking at other industries' opportunities, or was this more or less the first thing that you came across?*

LS: I was looking at some consulting jobs, also I had done internships in biomedical pharmaceutical companies, so I had been looking at that as well. Sometimes things fall into place and you're like, okay, I'm clearly meant to go in this direction. And that's kind of how my job here at the fab came about. It just fell into place much more smoothly than the other things that didn't seem to be quite as good a fit at the time.

PA: *What is your role at GlobalFoundries? Are you still doing the job that you were hired to do or have you moved on?*

LS: I started as a process engineer and was in that role for about seven years. And it was great because our process engineers have technicians that have a lot of background that they work closely with. It was nice to have that working relationship with folks who had a little bit more experience than me. And then at that point, I decided I wanted to get better at data analysis. My degree is not in electrical engineering, so I didn't have a lot of background on device performance or anything. But we were doing some CMOS image sensors in this lab and I decided, okay, I can understand if you take a picture in the dark, there's a bright spot.

Take a picture in the bright, there's a dark spot. So it was my way to make my transition into that data analysis, by getting my head around it. And it did a characterization for that for a couple of years and then worked on some other products, some of our 90 nanometer, some RF. And then about eight years ago, I moved into technology development when this fab became part of Global Foundries. And I've been in our technology development for the past eight years. And I love doing new technologies, new features, getting to run a lot of experiments. And right now I'm working on some of our GaN programme. So that's been a fun challenge here as well.

PA: *You've always worked in the semiconductor industry, and you have your college experience before that. In terms of how you found the environment - the semiconductor industry, and certainly the broader IT industry is characterised as being fairly male dominated. When you arrived, were you surprised at how few, or maybe even how many women there were in the industry? Your initial thoughts as to when you joined the industry?*

LS: In college, actually, my chemical engineering major, I think it was 16 females and 10 males. I actually came from a pretty nurturing college environment. And really my first notice of it was when I started, when you're new, you're trying to figure out what you're supposed to wear, what do other people wear to work? And I looked around and realised, oh, there's enough women to have that baseline. I guess I have some flexibility. But yeah, I would say we were pretty not always the only, but one or two or three a lot of the times in meetings through my early years.

Right now I'm actually in a department that I think is 50:50 in technology development integration that has a good, strong female representation, which is pretty exciting. But for the most part it was more of just that, oh, okay, I guess I get to be a little bit more flexible. There's not a uniform because there's a little bit more variety.

PA: *Expanding on the point, have you found any challenges in the workplace? Do you think that any were at all related to the fact that you were a woman in a male dominated environment, or has the company had, as far as you can see, a fairly enlightened and diverse approach to employees? Any experiences, thoughts you want to share on that?*

LS: Yeah, I think whenever you're a new engineer coming into an area and people are looking for your decisions and you've only been there a year, it's a little intimidating. One of the things that I remember laughing about when I was new is at one point I was working with three technicians who are all male,

➤ I've been in our technology development for the past eight years. And I love doing new technologies, new features, getting to run a lot of experiments.

who are all taller than 6ft, and I was just five three, five four. And so a couple of times I'd be walking down the hall to a meeting and it would be me with my three six foot coworkers with me. I felt like I had some pretty strong backup!

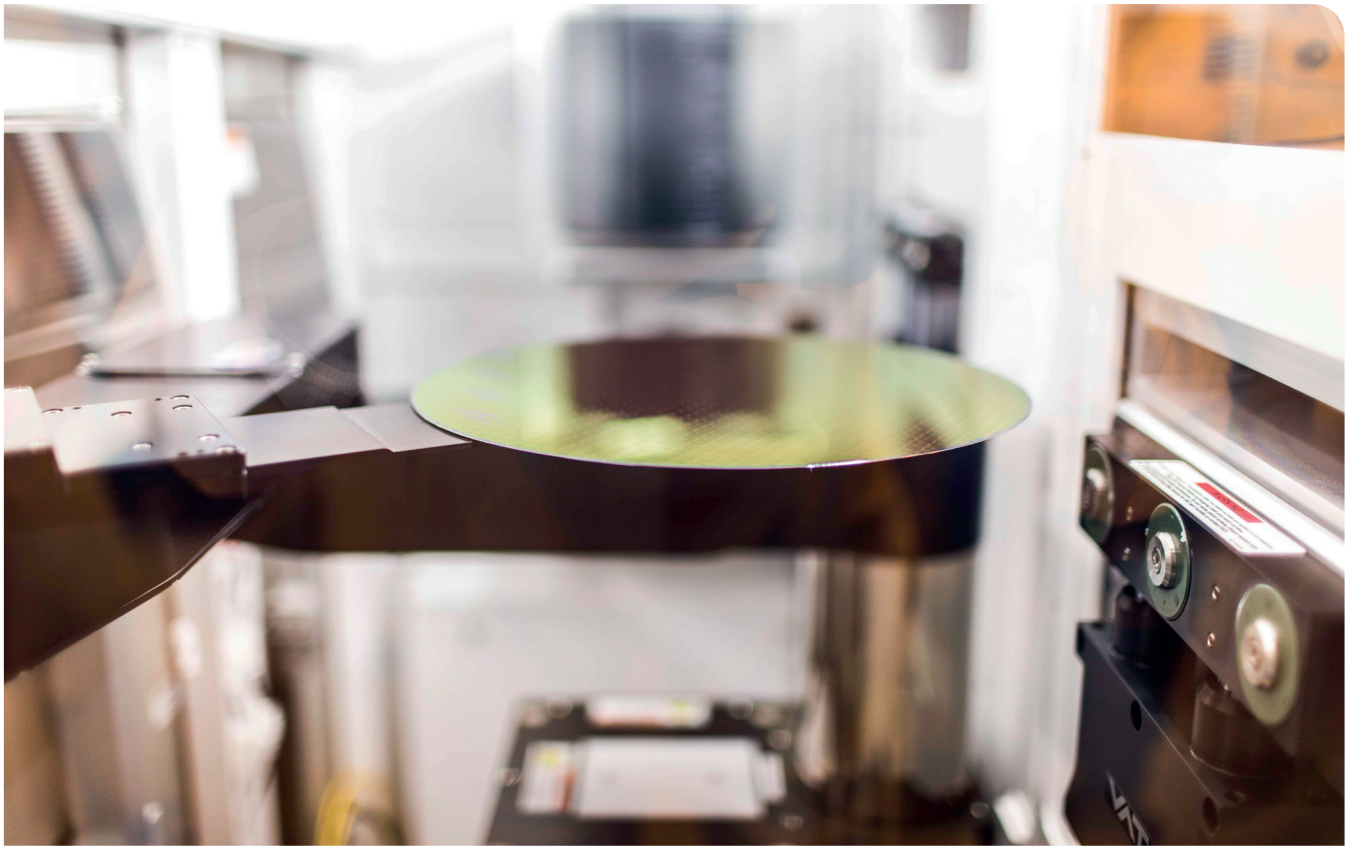
But to be honest, I think part of that has been living and working in the Northeast United States. A lot of my colleagues are supportive of their wives' careers, take time off for childcare, leave work early for school sports. So I think part of it is, from a gender perspective, being in the Northeast United States has made it very normal and has not had that much of a challenge related to gender. And certainly while it wasn't a heavily female environment, I wasn't the only one. There were plenty of other women around who've gone through maternity leave or asking for part time schedules for that and created this culture where it was normal and accepted and not that much of a challenge.

PA: *Have you noticed at all during your career, then, with GlobalFoundries any differences, any improvements? It sounds as if it was a pretty positive environment to start with, but have you noticed things have got even better from that starting point? And does the company run specific initiatives around diversity or equality?*

LS: Yeah, the biggest one for me that I'm really excited about, I had my son almost four years ago in 2019. At that point, my leave was just the standard six weeks short term disability. And then I took some time off, unpaid, under FMLA, to be home for three months before working about four days a week when I returned.

And now GlobalFoundries is up to 20 weeks maternity leave. Just huge. I mean, that's a huge change for the positive - that support and also some pretty generous paternity leave, which a lot of my colleagues have taken when they've had children in their families. So that's been a huge step forward that I'm really excited about for my colleagues, GlobalFoundries also has a great global women programme. They have regional and local conferences that have been really helpful. There was one, I think, in February of this year, and one of the things that I really liked is they talked about visualising your goals. And so one of the things I wanted to work on more was doing a better job of patenting and okay, I really need to start working with a patent group. And one of the questions they asked as they went through this goal visualisation was, okay, now who can help you with that?

And it was great because I hadn't thought about, okay, if I want to start a patent group, I don't have to reinvent the wheel. I have some colleagues who've done this, so I picked their brains about what are your best practices, how many people, how often do you meet? And it was just a good



➤ One of the things I appreciate about the semiconductor industry, especially when you're working in a 24/7 fab, is while it's important to have a good amount of your working hours while colleagues are there so you can engage with them, it's not impossible to work off hours because the fab is open.

initiative to kind of get the momentum going, to look at it in that perspective that I found really helpful. Global Women has also had a strong presence at the National SWE (Society of Women Engineers) conferences. Two years ago I attended remotely due to COVID. I didn't feel comfortable travelling at that point. My son wasn't vaccinated yet, but this past year I was able to attend in person the National SWE Conference and was a co-speaker of a session with a colleague. And GlobalFoundries was really supportive of us as we brainstormed our idea and went through that process. So I really appreciated that as well, my chance to network and meet up with other colleagues.

PA: *And in terms of where we are and where we perhaps need to end up, are there any things you can think of that you would like to see happen or need to improve or it sounds as if there's quite a lot of positivity, certainly at GlobalFoundries. So, is it just doing more of the same and just increasing that, or do you think there are any sort of step changes that still could be made in terms of changes for the better, for equality and diversity?*

LS: Well, I think that the ramifications of COVID in the workplace and that flexibility of home versus in the office are profound for families, and that increased flexibility has been great, amazing. One of the things I appreciate about the semiconductor industry, especially when you're working in a 24/7 fab, is while it's important to have a good amount of your working hours while colleagues are there so you can engage with them, it's not impossible to work off hours because the fab is open.

The FA teams, the failure analysis teams are there, working. There's folks, if you want to set up an experiment, somebody can run it for you at any time of the day. So that's an opportunity, it's a plus and a minus, but there is a positive for that flexibility to work your schedule around your time. One of the areas that's been key for me that I've really valued between my son was born until he was three, both my husband and I worked 80% time, so we each took a day off a week and it's amazing what one day a week does to get rid of that parental guilt part!

So it's fantastic. And I really felt privileged to do that and supported. But I do think there's still some room to grow the flexible work programmes. Not just the offering of them, but also the uptake and people who take advantage of that. Because for me, it was really valuable to have that time to get rid of that parental guilt stage. So those are the directions I think there's some room for growth in.

PA: *And in terms of role models, when you arrived in the industry, were there any senior women that you thought, yes, there's someone I can aspire to, or there may have been a male role model that helped you find your feet? More generally in the industry, is it fair to say that at the moment it's not obvious that there are that many female role models? Certainly, when you get beyond a certain level within an organisation, whenever you see people in the news or reported in magazines, it generally tends to be a male individual that's doing the talking because they're the CEO. What do you see as that picture for role models and perhaps what needs to change in terms of the boardroom?*

LS: That's a challenging one. For me, the places where I found the most help as a newer engineer were colleagues who were near retirement. There's something about a colleague who's near retirement that is really interested in helping new hires come up to speed, very free to speak their own mind. So, I had a lot of value from some coworkers who are all, in retrospect male, but especially those who are near that retirement stage, of really being able to lend some advice and create some good relationships with that.

And the other part that's been really powerful me is peers. For me, peer mentoring kind of sometimes doesn't get as much recognition as it deserves and when I took my job in technology development, part of the reason I did was because a coworker had started working there - a peer - and said, hey, this area is great, you should apply, there's an opening. And I think there's something to be said for that coworker peer sort of guidance, because there's a good amount of power on that, not just mentors. From a mentoring perspective, otherwise, I think GlobalFoundries actually is doing a great job of encouraging women in management roles.

I do see a lot of my peers, or even engineers who've started, say, ten years after me, making headway in that sector. One of the reasons I've tried to stay in a technical role is I haven't seen as many females advancing in that sort of technical role and there's a few that have since retired that I really did admire, but a little bit harder to find. But right now, Isabelle Ferain, I think she's leading Fab8 right now from Germany. She is fabulous. If you ever get a chance to talk to her, she's really great. And I got a chance to meet with her at the Global Women Conference two years ago and by the time I woke up the next morning she had sent me a note saying thanks to me for meeting you and she's just really fantastic. So, it is valuable to have those females out there and that the Global Women Conference has been a really valuable way for me to meet some of them within GF.

PA: *Quickly back to the education side. It sounds like on your course there was an even spread or even the women were in the majority over the men. But do you think there's more that needs to be done on the education front to convince women and diverse groups that the IT sector and the semiconductor space is for them or do you think it's happening naturally?*

LS: One of the things that I think that I love most about the semiconductor industry is that it's so

➤ GlobalFoundries also has a great global women programme. They have regional and local conferences that have been really helpful.

complex nobody can know it all. It's impossible. You can't possibly know every detail of every piece of equipment that's used to make every device and every level and how it's working. One of the things that I don't think we promote or talk about much is just how much of it is that collaboration, of people bringing their own skills to the table and collaborating and getting the right people in the room that have the different pieces of the pie.

And it's something that's hard to capture in the education system because you basically all have the same background when you're in classes together so you're not bringing different things to the table.

As I've been thinking about this question recently, I think there's a room for kind of trying to think about that cross disciplinary and that power of communication because that is, I think, a differentiator in this sort of technical world, that ability to work with people who you might not be speaking the same language with. And sometimes I think women and people from diverse backgrounds might have more experience trying to speak the language of people as opposed to always being within their same group and they can bring a lot to the table in that sort of collaboration environment.

When you're in something like this, nobody can do it alone, no one can know every detail. I don't know how to do that. But I'd really like to see that emphasised as really something to celebrate about this high-tech industry is the collaboration, the communication of technical information, but still you're bringing your piece to the table. And how do we make sure that when we're trying to talk about our different pieces that we're still kind of finding that common ground and making the right decisions at that point?

PA: *Maybe just a final question in terms of folks that might be looking to join the industry, whether they are still in college or they already started a career in a different industry. I suspect, having talked to you, you would certainly recommend that they join the industry. But any advice as to what to look out for as they're looking for an opportunity within the sector?*

LS: The big challenge with semiconductor industry is the cyclical nature. And I think that is something that can be hard to deal with as a new hire. When the industry is up, everything's great. When you go through downturns. I mean, I graduated college in 2001, so not far behind the September 11 attacks, and the semiconductor industry definitely had a downturn within six months of me starting in the industry.

One of my pieces of advice is, whatever role you take, think about what you're learning, make sure you know what you're learning and think about how you can apply that in this job or in your next job. And always make sure that you're learning. So, if you find yourself in a situation where you've been doing the same thing for five years and you're not learning anymore, then it's time to make sure you think about that next growth opportunity.

Because when you're worried if you're in a situation where you're worried about layoffs or other workforce adjustments, I don't know what they call them these days, but if you're worried about that, I think by prioritising what you're learning about in your role and how that would help you in this job or another job in the future, is a good way to help ease your mind over that stress.

And for me, that's been really helpful to think about what I'm learning in every role I work in and what do you like about it, and just be really upfront with yourself, what you like about it, what you dislike about it, and that can help make decisions easier. I think the US-based manufacturing, it's pretty exciting to work in it. It's exciting to be able to do experiments, try new things. So those are some of the reasons I really do like the industry.

PA: *And I guess, although you alluded to the ups and downs, overall, I think everyone, all the market analysts, say that it's got to expand fairly significantly if it's going to meet all these demands around AI, IoT, electric vehicles and the like. In general, it's a pretty positive place to be?*

LS: Yeah, I would agree. I think it's nice to be part of that. It's nice to be working on technology that, for the most part, is doing some really interesting things when you think about automotive these days or what we have in our cell phones. It's really exciting to know that you're part of that and have a product that you can reference, that you've been working on, that you're not just moving money or consulting, you're actually doing the work.

➤ VistaX Pro LayerScan, the Comet Yxlon computed laminography technique, is the most efficient inspection method in advanced packaging.

Advanced X-ray technology for advanced packaging

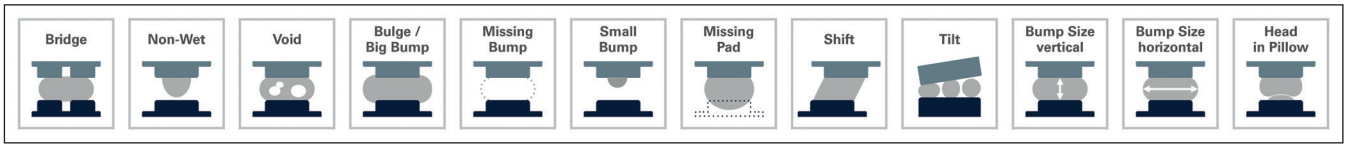
While X-ray technology in the semiconductor industry was considered too inaccurate, too slow, and too expensive a short time ago, new developments in micro-CT, sophisticated trajectories, and smart algorithms are delivering a non-destructive inspection method that is helping manufacturers with their zero-defect strategy taking their productivity and profitability to a new level.

BACK IN 2005, in an interview marking the 40th anniversary of 'Moore's Law', Moore noted that this miniaturization would soon reach its limits and would probably become physically unfeasible or simply too expensive sometime in the mid-2020s: "...the fact that materials are made of atoms is the fundamental limitation, and it's not far off...We're hitting some pretty fundamental limits, so one day we're going to have to stop making things smaller." Meanwhile, having arrived in the 2020s, we still haven't reached the end of the line.

Today, Advanced Packaging has long since moved into the nanometer range regarding electronical structures. Compared to an average human hair of 0.06 mm, i.e., 60,000 nm in diameter, think of microchips sizes of a few square millimeters and their transistors inside acting as miniature electrical switches to turn the electricity on and off. Nowadays, there are several billion transistors per chip!

Increasing amounts of dies inside of individual packages are connected in enormous networks of metal traces. Further sub-components inside fine-tuned electrical circuits are bridged via thousands of solder joints with diameter sizes between 5 to 100 µm. These solder joints (balls, C4- or micro-bumps) as well as the TSVs (Through-Silicon Vias) are risks to the product quality, generally caused by production process variations.

➤ Right: 3D-view of 60 µm micro-bumps, soldered and open.



➤ Typical defects of solder joints.

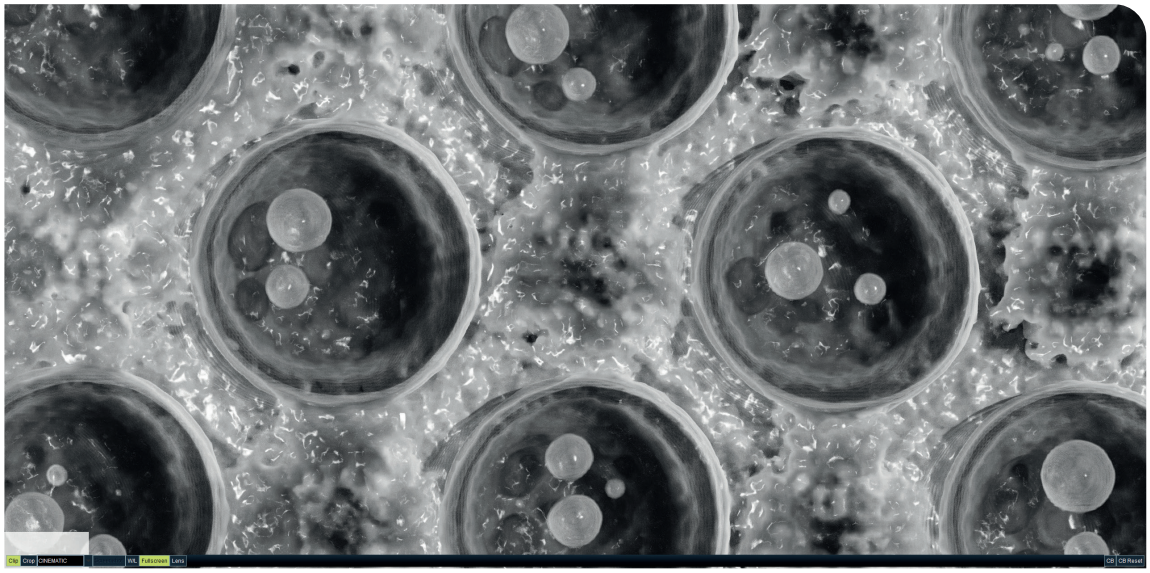
The more compact and powerful today's ICs become and the more complex their production is, the more increases their value - from one production step to the next. Every defective microchip that needs to get sorted out means high financial losses. Imagine the economic damage through a whole series of entirely packaged ICs that are unusable due to a process error not discovered at an early stage! Manufacturers in the semiconductor industry need to aim for zero-defect production defining strict tolerances. And therefore, reliable quality inspections already start in research and development and accompany the entire manufacturing process to reduce the costs of non-quality production processes.

Destructive testing methods, however precise and detailed they may be, can no longer be the solution, given the long turnaround time and high costs involved. Optical inspections on the other edge of the possible inspection technologies only detect a fraction of the critical defects. X-ray technology has received little attention as an inspection method in the semiconductor field. Although it is the only technology which can look inside a product, simple fluoroscopy cannot distinguish the overlapping layers in today's complex three-dimensional packages. Three-dimensional computed tomography (CT), which images the spatial view of an object, was long considered too slow and too cost-intensive.

Three-dimensional computed laminography (CL) has now changed the game. Unlike CT, CL does not require 360° rotation of the test part. In a special way, the component gets scanned layer by layer, achieving the required resolution and image quality to inspect the critical interconnections. Layers can get analyzed individually or reconstructed into a 3D volume. The 3D volume, in turn, can be cut at any region of interest and examined in detail. In doing so, computed laminography is much faster than, for example, FIB-SEM (Focused Ion Beam Scanning Electron Microscopy) and detailed enough to detect all critical defects. Today's CT/CL inspection systems ensure consistent image quality and stable, repeatable results even after hours of operation during batch inspection.

In addition, X-ray inspection in the semiconductor industry is becoming even more efficient by applying automated inspection processes and automatic defect recognition (ADR). Comet Yxlon's high-resolution microfocus X-ray systems, with their best-in-class imaging and latest software features, combined with Dragonfly's sophisticated deep-learning models for automatic segmentation and image evaluation, can be tailored to individual user requirements and work independently from human bias. Ramp-up processes are accelerated, resulting in significantly shorter time-to-market.

But wait, can't X-rays damage, or even destroy your sensitive products? That's no longer the case with the innovative Comet Yxlon inspection systems. Low-dose detector modes for sensitive components, dose monitoring with alarm and stop function, and additional dose reduction kits prevent possible damages through radiation and guarantee safe X-ray inspections. In addition to the proven Cheetah EVO, Cougar EVO, and FF20 CT microfocus systems, Comet Yxlon also offers the FF35 CT as a SEMI version, certified according to the high SEMI® standards, including the hazard and safety standards SEMI® S2-0818 & SEMI® S8-0218. And the developments continue at full steam.



➤ 3D-view of voids in solder bumps.

How does mass spectrometry support the demand for semiconductors?

The controlled use of various gases is an important aspect of semiconductor chip manufacturing, which helps to ensure high quality end products. Contamination at any stage in the workflow, including gas delivery, can have significant and expensive repercussions, meaning that even the smallest concentrations of impurities need to be detected and removed before the gas enters the fabrication process. Fortunately, technologies for monitoring and controlling the supply of ultra-high purity (UHP) gases have advanced, and now include atmospheric pressure ionization mass spectrometry (API-MS), which can detect impurities as low as 10 parts per trillion (ppt).

By Thermo Fisher Scientific

Market growth expedited by changes in patterns

The global semiconductor market has experienced record growth in recent years, and its value is forecast to expand to almost $803 billion by 2028. This progression can be mostly credited to the ever-growing worldwide demand for electronic devices, as well as lifestyle changes resulting from the COVID-19 pandemic, which revealed the importance of networking and communication solutions required for remote working and distance learning. Semiconductors are at the core of an ever-increasing list of products deemed essential for enriching the customer's life and helping businesses to operate smarter and more productively. This continuous innovation, combined with the emergence of new technologies – such as the internet of things, artificial intelligence, machine learning and cloud computing – are the most significant drivers of the market.

Meeting demand with UHP gas supplies

Manufacturers have had to drastically ramp up chip production in response to the heightened demand for high quality semiconductors. The need for UHP gases and chemicals has also increased, owing to the fact that silicon wafer fabrication requires a wide range of electronic specialty gases (ESGs) – including nitrogen, argon, hydrogen and helium. ESGs are produced by specialist gas and chemical companies that supply them to semiconductor fabricators to be piped in high volumes throughout the whole plant. These gases are needed at various stages of the manufacturing process to aid in the

creation of the required surface features on wafers. For example, 80,000 to 100,000 Nm3/h of nitrogen with 99.999 % purity is necessary for 3D NAND manufacturing.

Consequences of chemical contamination of wafers

Semiconductor production came to a sudden halt during the recent pandemic, and resulted in apparent shortages in both the automotive and high-tech industries. This disrupted the smooth running of businesses and prompted a major drive to speed up production. However, increasing production rates also heightens the chances of chemical contamination of wafers during fabrication, which may cause a decline in device processing and performance. The source of this problem can be in the gas supplies used during production, where undetected trace contaminants may be present. Such contaminants may penetrate the surface of the wafer through micropores and absorb into the bulk of the layers to affect their properties, causing defects and reliability issues. For example, organic contaminants such as hydrocarbons can corrupt the reliability of gate oxides, and negatively impact the thickness reproducibility of thin silicon nitride layers.

Manufacturing incidents or technical difficulties are often just the start of the multitude of downstream consequences that can follow. Wafer defects can sometimes go unnoticed until they reach the market, resulting in unexpected costs to semiconductor companies. This can also lead to reputational damage, compensation claims and loss of future revenues for such companies. Even if faulty products are identified and do not enter the market, gas contamination during production can still result in increased production waste, suspension of production lines and delays in supply. Two market leading semiconductor companies experienced such an event in 2019, and had to scrap huge amounts of wafers due to manufacturing contamination, resulting in millions to billions of dollars in revenue loss. This has led to calls for stricter procedures and quality control measures to ensure that compliant UHP gases are delivered to production lines.

Analyzing gases to determine purity

UHP gases are usually delivered to a basement or ground floor storage location of a semiconductor fabrication site, where they are analyzed for trace impurities before being piped throughout the plant. Continuous quality control systems in the quality assurance and quality control stages of semiconductor production ensure that these gases meet the required purity specifications. This is traditionally done with inline gas chromatography, thermal desorption or inductively coupled plasma analyses that have limits of detection between 100 and 500 ppt, depending on the instrument used. However, these methods are no longer considered to be sufficient by some in such a competitive industry where gas purity is critical, so such methods have recently been displaced by API-MS that allows detection of trace impurities down to 10 ppt.

API-MS has become an attractive technique to use, as the single or multiple UHP gas lines are coupled with an API-MS, for immediate and continuous analysis. API-MS involves the ionization of the gas in a reaction chamber maintained at atmospheric pressure, followed by the detection of positive or negative ions by the mass analyzer. When a measurement is conducted, sample gas is pumped into the instrument's reaction chamber, which maximizes the volume for ionization and reduces background interference to improve performance. This set-up allows the identification of impurities down to 10-50 ppt – far below the specified limits – ensuring that the gases are suitable for use in the various workflows of high quality semiconductor manufacture. Unlike chromatography, the flexibility of API-MS also allows the measurement of a considerably wider spectrum of impurities, including moisture, oxygen, carbon dioxide, carbon monoxide and methane.

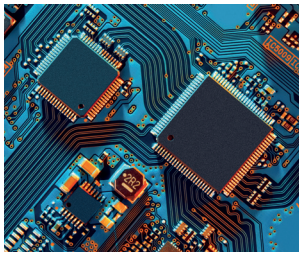
Enhanced analyzers for ultra-clean gases

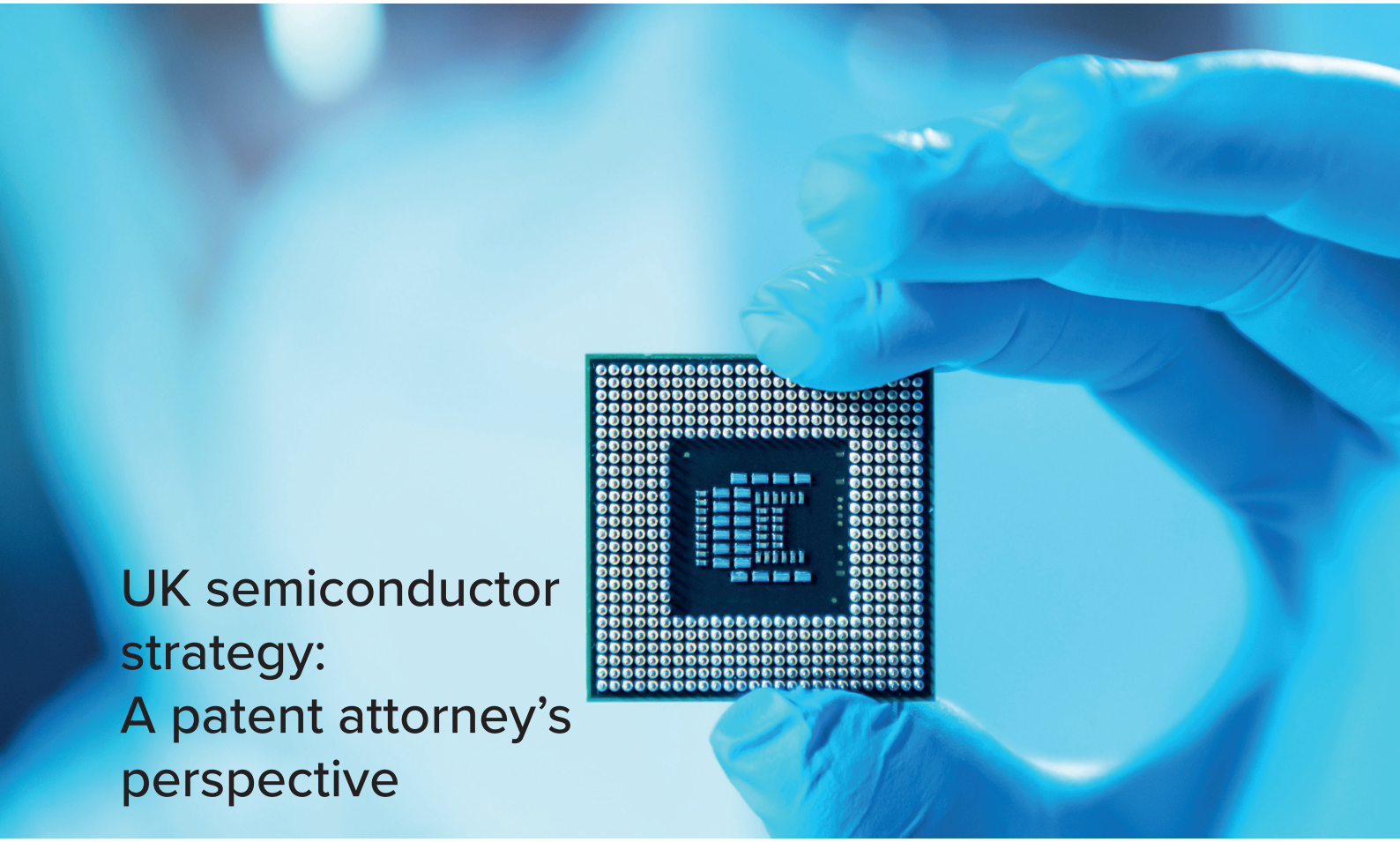
Sophisticated electronics and software have recently been integrated with the API-MS method, further improving routine continuous measurement of contaminants in bulk gases. These UHP electronic gas analyzers are designed to ensure that each bulk gas is monitored for a wide range of potential impurities, and to achieve lower detection limits than API-MS alone. However, the International Technology Roadmap (ITR) for the semiconductors industry has established gas phase contamination limits of 100 ppt per impurity. It is therefore beneficial to have UHP electronic gas analyzers that offer even lower contamination limits, and one such existing set of instruments that currently achieves this detection level is Thermo Fisher Scientific's APIX δQ & APIX Quattro process mass spectrometers.

Vision for meeting future demand

Using ultra-high sensitive, multi-component, multi-stream gas analyzers that are low maintenance, fast, easy to use and self-calibrating promises to help meet the semiconductor chip manufacturers' requirements of today and well into the future. Automating workflows is also becoming more prevalent. Integrating these features in quality control systems ensures 24/7 vigilance, offers continuous protection of UHP gas supplies and validates the performance of purification systems.

API-MS, combined with effective gas purifiers, is now commonly used in the industry for detecting, monitoring and purifying gases in applications that use nitrogen, argon, helium and hydrogen. Overall, UHP gas production supports a niche – yet absolutely crucial – part of semiconductor chip fabrication, helping businesses to not only keep up with the ever-increasing demand, but also continue to produce reliable, high quality goods.





UK semiconductor strategy: A patent attorney's perspective

The UK Government has published its National Semiconductor Strategy, announcing a 20-year initiative that seeks to establish the UK as a world-leader in semiconductor technologies. While the reaction from industry has understandably focused on the amount of financial support pledged in the strategy, as intellectual property (IP) attorneys our attention was drawn to the emphasis which the strategy places on IP as an area of UK strength. Encouraging as it is to see IP highlighted as an important factor in the semiconductor industry, in our view the authors of the strategy seem not to recognise the full potential of IP rights which arise across the semiconductor industry.

By Will Ponder, Partner and Gavin Dundas, Senior Associate, Reddie & Grose, a UK & European specialist intellectual property law firm.

Technology of Tomorrow

The strategy emphasises how excellence in semiconductor technology is key to the UK's position as a scientific powerhouse. Semiconductors are identified as one of "the five technologies of tomorrow", along with quantum, AI, engineering biology and future telecoms. The strategy even suggests that semiconductors might be the most important of all, as they will underpin advancements in telecommunications, quantum computing, AI, and net zero technology, all of which are critical to the UK's economic and national security.

Unlike many other countries, the UK Government strategy aims not to expand large-scale silicon manufacturing, focussing instead on existing strengths such as R&D, IP and chip design. There are planned investments into a number of UK semiconductor clusters that are already manufacturing compound semiconductors, albeit on a small scale, and leading UK companies ARM and Imagination Technologies are cited as assets that the UK will build on in the future.

The strategy aims to support innovation by encouraging new semiconductor start-ups and supporting existing companies to become tech unicorns. A new UK incubator programme is proposed to develop semiconductor start-ups, and the Department for Science, Innovation and

Technology (DSTI) will review pre-seed/seed funding opportunities for such companies via UK Research and Innovation (UKRI). The strategy also emphasises the importance of collaboration between universities and industry to promote the commercialisation of R&D.

Initial reaction

It is clear that the strategy has ambitious aims, but industry leaders have questioned whether these ambitious words are adequately backed up by the funding package: £200 million from 2023 to 2025, and up to £1 billion in the next decade.

This pledge of financial support compares poorly to the sums announced by other countries which also aim to become world-leaders in semiconductor technology. Sums of $50bn and €43bn have been allocated by the US and the EU respectively, both of which have declared their ambitions to boost local manufacturing.

Perhaps the UK's pledge reflects a desire to attract private sector funding and focus on smaller scale start-ups and existing companies, but the reactions from leading industry figures in the UK were less than effusive.

AI chip designer Graphcore said it was "modest" compared with countries such as Germany. Dr Simon Thomas, chief executive of Cambridge based graphene semiconductor start-up Paragraf, described the investment as "flaccid... It is a long way from addressing the needs of UK chipmakers" and "In reality the UK's capital commitment is nothing but a rounding error in this industry". It was also noted by some in the industry that the funding is lacking compared to the £2.5bn allocated to the UK's quantum computing sector earlier in the year.

We consider the published strategy to be short on detail of how the pledged money will be spent, and what the road map is for spending it. As IP attorneys, we work closely with high-tech companies of all sizes, and a commonly-held view is that in order for industry stakeholders to plan effectively for the next decade, having certainty on what support they will receive is at least as important as the amount and form of that support. The strategy suggests that more announcements will be made in Autumn 2023, so these may provide some of the missing detail.

A patent attorney's perspective

The fact that there is a strategy that references IP, and that there is some investment, is certainly encouraging for the semiconductor sector. Investment and innovation should always be accompanied by a comprehensive IP strategy. However, the strategy could be clearer about the important role of IP.

In the strategy, the UK Government has picked out IP as an area of UK strength, and so they should. But the intended meaning of the word IP in the

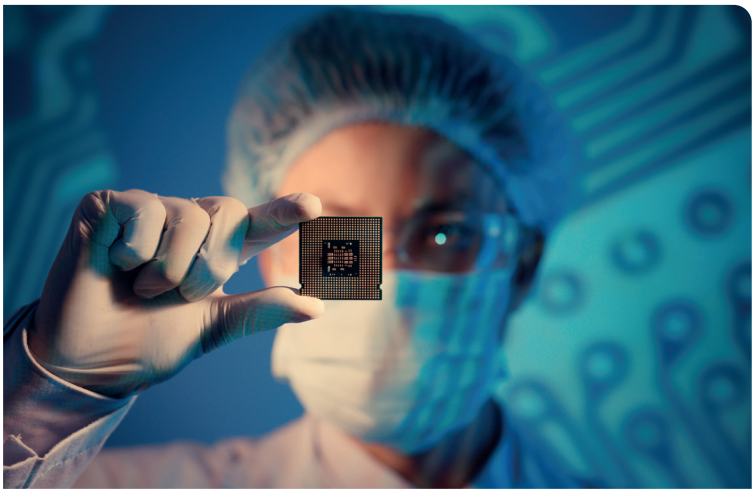
Perhaps the UK's pledge reflects a desire to attract private sector funding and focus on smaller scale start-ups and existing companies, but the reactions from leading industry figures in the UK were less than effusive

strategy is not clear to us. We think "IP" is only being referred to in a limited sense. In the context of semiconductor design, "IP" is sometimes used to refer to IP cores, which are building blocks in the overall design of a semiconductor chip. But that is not the only IP that is, and will be, important in a thriving UK semiconductor industry.

Patents will be crucial for all UK semiconductor companies seeking to secure investment and then provide a return on that investment. Any time a technical problem is solved there is a potential patent. The technical problem may be a problem in manufacture, in packaging, in chip design, in chip testing, or in the development of new materials for example. All of these are areas of potential UK strength.

As part of their decision-making process, private investors will always review the patent portfolio of any technology company that they might invest in, as well as asking questions about the IP strategy for the company more generally. So, if attracting private investment is key to the UK Government strategy, ensuring UK companies identify patentable inventions and then apply for patents will be crucial.

If the plan is that fabrication will largely be done by non-UK based companies, protecting the IP generated by UK companies is even more important as a way to generate revenue. Companies such as ARM, which are presented as a model of success, do not manufacture anything but instead generate all their revenue by licensing their IP. That requires



protecting their IP not only in the UK, but also in those jurisdictions where significant manufacturing will be taking place.

Obtaining a patent for an invention in several jurisdictions takes time, money and professional advice. In our view, if the UK Government wants to ensure success for this 20-year initiative, it cannot overlook the importance of supporting companies in identifying and protecting the IP that they generate, particularly by applying for patents in the UK and overseas. There are UK Government schemes that do encourage companies to apply for patents, such as the Patent Box scheme, which reduces the rate of corporation tax payable on profits resulting from products that include a patented invention, and Innovate UK IP audit grants. It would be helpful to make sure those schemes, and others, are joined up with the National Semiconductor Strategy so that the UK gets the best possible outcome.

Conclusion

The announcement of the National Semiconductor Strategy is surely a positive, as it is encouraging that the UK Government is committing to investing in the semiconductor industry, and recognising semiconductors as a critical sector where the UK can punch above its weight. The UK is extremely fortunate to have well-established and successful companies in the chip design space such as ARM and Imagination Technologies, as well as exciting new companies working on compound semiconductors, new materials and new devices, including Paragraf and Porotech in Cambridge alone. It is vital that companies in this area are aware of the importance of protecting their IP both at home and abroad, and that innovators recognise that the semiconductor field gives rise to IP not just in the form of IP cores, but in a huge variety of protectable inventions.

We look forward to seeing the strategy be implemented, and hope that the UK Government backs up the strategy's ambitions with clear and pragmatic support and financial backing for those companies that are working to place the UK at the very forefront of semiconductor technology.

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The need for geofencing to help improve semiconductor IP security

At the heart of large-scale semiconductor projects are intellectual property (IP) hardware or software components, essential for implementing the design, but they can be hard to manage, trace, and keep secure. In addition, global volatility, legal restrictions and geographically distributed teams create extra pressure, with risks of IP leakage, theft, fines, and loss of market reputation. The answer is to adopt comprehensive IP geofencing to protect valuable technology without slowing project velocity or hindering team collaboration.

BY SIMON BUTLER, PERFORCE

AN ORGANISATION might have tens or even hundreds of thousands of these IPs interacting with each other in highly complex situations, factors which in themselves can make them hard to track and manage. Examples of IP are hardware components such as phased locked loops (PLLs), arithmetic logic units (ALUs), and analogue transceivers, all of which are used as functional building blocks in a System on Chip (SoC). Embedded software is another form of IP that should be managed in the same platform. These IPs exist in a rapidly changing, unpredictable global environment where one nation does not want its precious IP exposed to another country.

For instance, the US has ITAR and EAR, which regulate the export of defence articles and services. The European Union has Regulation (EU) 2021/821, which controls the export of dual-use items, such as software and technology, and which can be used for both civil and military purposes. Japan has the Foreign Exchange and Foreign Trade Act (FEFTA).

In October 2022, the US Department of Commerce's Bureau of Industry and Security (BIS) announced sweeping revisions to its technology export controls. In the same year, the chief of AMSL — one of the leading European semiconductor organisations

responsible for key manufacturing technology used worldwide — spoke publicly about the risks around IP leakage and the need for the industry to manage them more effectively.

Fines and firefighting

Fines for exporting restricted technology can quickly run into the $100,000s and even millions of dollars. In the most startling case, a large multinational semiconductor company recently paid $10 million in fines under these rules.

Not only are there financial penalties for semiconductor organisations who break these rules, but violations are also hard to manage, leading to firefighting instead of focusing on the project. And the situation constantly changes: what might be permissible one month could be restricted the next.

Furthermore, semiconductor firms typically have geographically dispersed workforces, pulling in resources from different teams and seeking out the best talent across the world. Employees who became used to remote working during the pandemic may now decide to experience living in another country for a while. People are starting to travel more. The multi-geographic nature of work is accelerating.

Plus, a complex and often overworked IT infrastructure of storage, data centres, and network connectivity underpins these teams. Add these factors together – a changing world, restrictions, the changing nature of work and technology systems — and it is easy to see how keeping track and securing technologies is complicated and cumbersome.

How IP leakage occurs

Before diving into how geofencing can help, it makes sense to understand how IP leakage occurs. The average SoC has more than 100 different IPs: some may be produced internally, others are provided by external sources. While malicious attacks are always a threat to take seriously, IP leakage can happen inadvertently. Here are a couple of scenarios.

First, imagine a semiconductor engineer travelling abroad to help a local team, carry out a demo, or have face-to-face meetings. During that trip, a problem arises with the project the engineer is working on back home and needs debugging. They build a local space and export all those components from a database in their own country to the one they are visiting.

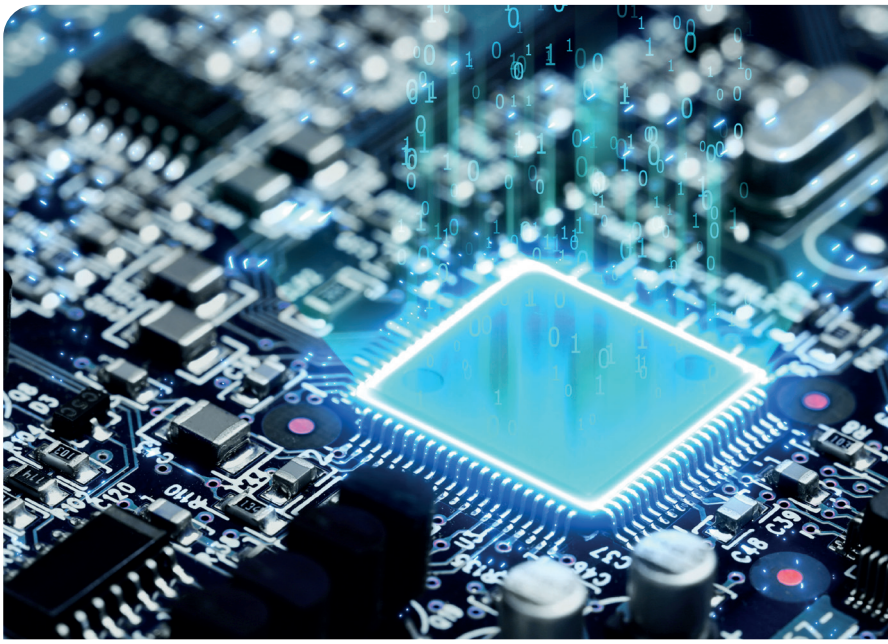
Most of those IP components are fine, except for one, which is not even the one the engineer wants, is not visible and is not flagged as restricted. But by downloading this asset, the engineer has violated a restriction, and because they have logged in to the network at a remote site, they are allocated an IP address based on that geography. In turn, that information is logged and can be used to generate warnings or alarms. If not heeded, that action could lead to their employee being fined, loss of revenue and damaged brand reputation.

Here is another scenario. A company might be headquartered in the US but has multiple offices worldwide, and to make it easier for teams to share data, they build local IP caches. Now, those caches may have restrictions in place, for instance, 'The Australian team does not have access to this IP'. However, the Australian team may see that it is available to their European counterparts, so they access the IP that way. While they have not directly exported the IP, the fact that they have acquired it is still a major problem.

This happens in real life, and it is not a criticism of those teams, who are often under considerable pressure to get a project completed and out the door. While IP leakage has to be managed, it must be done in a way that does not adversely impact people's productivity. Users are generally unaware of the fine-grained details of the content they have accessed. The IP is opaque data, often just presented as a tarball (short for 'tape archive' — a set of files packaged together into a single file, then compressed using the gzip compression program).

Better IP management

So, how can all these challenges be addressed? The first step starts with the IP itself. For decades, semiconductor projects have been built as monolithic blocks, which worked well enough in the original context. Everything existed in one environment, and previous projects were copied to the new one because reuse always makes commercial sense. However, this approach makes traceability difficult: if the technology is suddenly restricted and there is some IP buried deep with no clear distinction to say that it should not be exported.



Therefore, the first step is to move from project-centric design to IP-centric design. In practice, this means that every unit or component is always maintained as a complete IP, whether built in-house or purchased from a third party, or reused for different projects. All these IPs can be stitched together in the project lifecycle management system into a hierarchical bill of materials (BoM), thus creating the projects. Moreover, the entire BoM can be reused as the starting point for another project while maintaining complete visibility of all the pieces.

Then, apply effective permissions management, with each IP having the correct view, read, write, or owner permissions. This is implemented via a permissions hub managed by a systems administrator, but in addition, each IP carries this information within itself.

Next, apply geofencing, which is additional metadata within the IP that dictates where it can be used. For example, a semiconductor company might operate in 30 locations, and geographies can be defined in different ways, such as 'these are all our data centres in Ireland' or 'these are all our computer servers in India'.

This geographic distinction is determined by IP addresses, with IPv4 being the most logical since it is so universal, but other methods, such as IPv6, will be viable in the future. In effect, the onus is taken away from people having to work out restrictions because each IP determines whether it is allowed in a particular geography through its own metadata. Think of it as a passport accompanying that piece of IP everywhere, stopping it from entering a country when it does not have the appropriate visa. Rather than extracting IP design data from the underlying data management system into a local workspace, embedding restrictions within the IP itself ensures that geographic protection overrules user permissions. So, even if someone usually has access to specific IP, this is blocked when travelling in a restricted region. Of course, situations change, so it is crucial that restrictions can be lifted. Again, by having that information embedded within the IP itself, the removal of a geographic ban is automatically populated wherever that IP is being used, without having to go into every single design project file to make that change.

Beyond helping to prevent IP leakage, this approach also prevents modifications to IP from becoming invisible or hard to trace because each piece of IP carries all relevant information within its metadata. Hence, when it comes to compliance and regulation processes, all the required details on how that IP was used, when, and where are easily accessible while reducing the manual burden on teams. Since workspaces are built IP-by-IP, companies can confidently guarantee that an IP never goes into a restricted geo.

Enabling collaboration

However, geofencing IP must not hinder the effective collaboration of globally distributed teams. The management of project configurations should be carried out predictably and securely. For instance, numerous projects engage external contractors, making it crucial to impose certain restrictions on these contributors. This is especially pertinent to their access to high-value intellectual properties (IPs) within the project.

Another concern is the potential for IP contamination, whereby engineers working on a specific IP might inadvertently gain access to similar third-party IPs available through the IP catalogue. Even well-intentioned engineers might find it challenging to avoid inference during the design process, possibly leading to unintentional replication of the third-party design. A further risk exists around sensitive subcomponents that should remain restricted at the source level, for example, the source code implementation for a process core or the specific implementation details of a leaf memory cell in a DRAM design. In such cases, to reduce the risk, an abstraction of the IP can be provided to the project, while certain aspects of its implementation are withheld from geofenced team members and other parties.

Better bill of materials (BoM) management

A more modern approach to managing BoMs can also enhance collaboration while still protecting IPs. In older workflows, distinct user groups were typically managed using separate BoMs, revealing only the relevant IP hierarchy to each

group. However, this approach adds complexity to the process of releasing components and their corresponding hierarchies as they mature. Moreover, it necessitates the synchronisation of these disparate BoMs and their timely distribution to groups whenever updates to project releases are made.

A more effective solution involves using the same BoM across all project members, coupled with individualised permissions that filter the content delivered to each user's workspace. Commonly referred to as "partial" workspaces, these setups enable users to execute releases and updates even in the absence of specific segments within the IP hierarchy.

That said, making well-informed decisions about which version of a missing subcomponent should be included in a release necessitates a certain level of sophistication in the IP management platform. During the initial workspace creation and subsequent workspaces updates, the user should be alerted to the fact that not all the IPs in the project hierarchy were synchronised over. However, in many organisations, naming those IPs is another form of IP leakage, so just enough information should be provided to enable them to sanity-check their configuration without necessarily revealing specific components. With a single unified BoM across all IPs in the projects and contributors, there is a significantly reduced risk of inconsistencies and stale versions of the BoM being used by team members, while also increasing the robustness of the geofenced project environment.

So, is there an alternative to automated IP-led geofencing? Of course, traditional techniques could be used by throwing money and people at the problem, using spreadsheets and manual edits, but this could lead to over- or under-correction and introduce human error. Plus, as mentioned earlier, semiconductor design teams have enough workload and time pressures already, without adding IP geofencing to their daily routine. Securing semiconductor design is a multi-faceted challenge, but having an IP-centric approach that effectively makes the IP responsible for its own accessibility, should go a long way towards preventing geographic violations.

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How to get two-digit savings on the cost of semiconductor test, with device-oriented test architecture

The adoption of testing solutions that help increase throughput and lower the cost of testing is a key factor to keep competitiveness up in the semiconductor industry. While, for many years, the way to reduce the cost of test was exclusively based on increasing the multi-site factor, a new test architecture approach demonstrates to boost test performances and efficiency.

There is no argument that testing represents a large share of the overall manufacturing costs for semiconductor devices. This cost percentage is experiencing a rising trend, due to the reliability concerns in mission-critical applications like automotive and security, as well as the longer lifetime expectations for many devices.

For decades, all the efforts to reduce the cost of test have focused on increasing the multi-site capabilities of testing equipment, called to perform multiple tests on higher numbers of devices at the same time. That, in turn, paved the way for highly sophisticated and expensive test equipment, housing all the specialized instrumentation to address the requirements of the whole variety of increasingly complex technologies. The company SPEA has been on the track for more than 45 years in developing cutting-edge test solutions, being a partner to semiconductor manufacturers and continuously innovating to meet the needs of this fast-moving industry.

The company has recently inaugurated a ground-breaking approach in the test architecture design, introducing an entirely new test platform called DOT (Device-Oriented Tester).

The innovative architecture DOT testers are based on has proven on the field to bring savings on the cost of test per device that often exceed 60% (going up to 95% savings in the best cases), on several challenging applications such as BMS, SerDes, OpAmp, PMIC, MEMS and sensors, Microcontrollers, Converters.

All the test resources are enclosed in a modular and composable board

The innovation at the basis of DOT architecture resides in the tester instrumentation, which is designed around the device requirements, instead of being based on the specific function to perform. In other words, instead of having a big-iron cabinet containing specialized instruments for every specific function (analog instruments, digital instruments, power instruments, digitizers, waveform generators, and so on), a device-oriented architecture allows for a tester configuration based on modular boards that incorporate, on a single instrument, all the analog, digital and signal-processing resources needed to test the devices.

The number of channels per board is the highest on the ATE market, and it contributes to lower the cost of test, offering more channels available per chip. This high-density board can be replicated inside the machine to reach the required multi-site capability, without losing on multi-site efficiency: as every board incorporates its own CPU and memory resources, the tester's memory size and the strategy to access it efficiently do not represent a limitation. The advantages of this type of test solution are tangible at different levels.

➤ Left: The innovative DOT test platform addresses the test requirements of applications like BMS, SerDes, OpAmp, PMIC, MEMS and sensors, Microcontrollers.

Savings over industrial costs
First of all, the overall tester cost and footprint are greatly reduced, as the total number of boards required is significantly lower than that of a traditional tester. The entire tester can be docked on a wafer prober, while also the power consumption is minimized.

Simple tester use, programming, maintenance
In second place, the possibility to populate a tester with all boards of the same type makes the tester easy to use and program, speeds up the learning curve for test engineers, simplifies maintenance operations and spare parts management.

Superior performance and test efficiency
The modular channel instrument is a high-density, multi-processor, multi-function board, composed of an on-board controller, four matrix cards and up to four different channel cards that can be selected to build the required performance mix, for a total of up to 256 channels in a single instrument slot. Multi-site management is transparent, and test efficiency is practically 100% when scaling from 1 to multiple sites.

Ensure best accuracy through time, with tester self-calibration

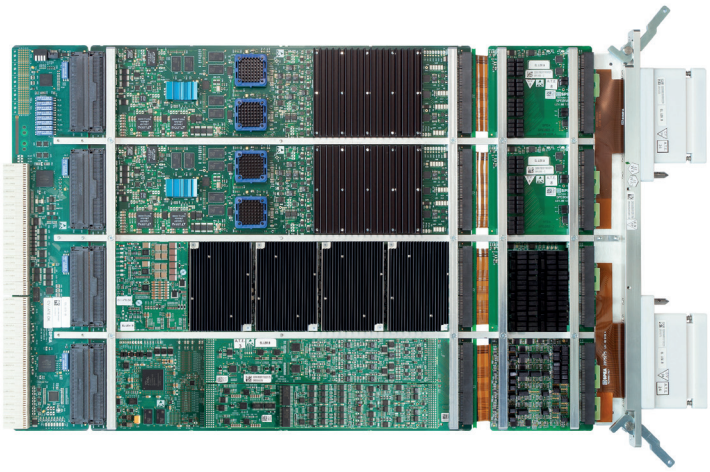
On every test floor, test equipment requires periodic calibration procedures to ensure that the test instrumentation meets the expected measurement accuracy, that is subject to deterioration through time.

Verifying the operation and functional stability of the semiconductor tester is mandatory to ensure accurate results: a tester that is out of calibration would contaminate the product yield with unreliable performance.

However, the tester calibration procedure normally implies a downtime scheduling, the stop of the tester operation for several hours, and the intervention of a qualified operator to undock the production load board, connect the tester to specific diagnostics and calibration hardware, and dock the tester again to the prober or handler at the end of the procedure.

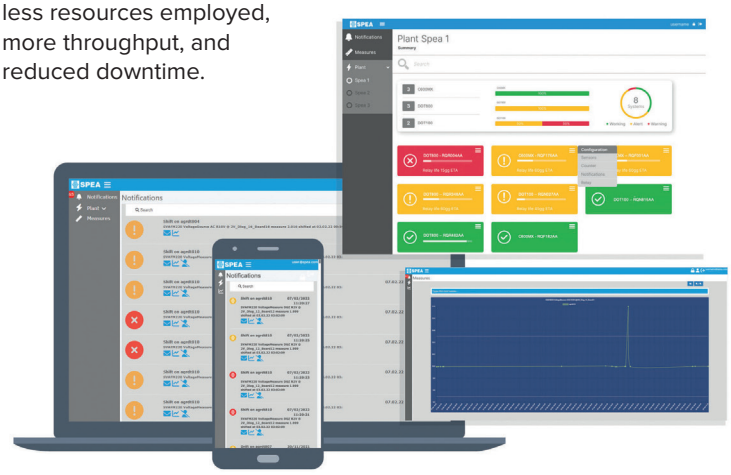
DOT test platform introduces predictive maintenance and self-calibration capabilities as strategic elements to minimize downtime and cost of ownership, while improving quality and control. The incorporation of artificial intelligence and smart sensors inside the test equipment enables the performance of automatic diagnostic procedures, self-corrections and comprehensive data analysis, without needing any scheduling, operator's intervention or specific hardware.

The tester is capable of autonomously verifying the instruments' health status, assessing the instrument measurement accuracy and detecting any trend towards out-of-specs performance, then independently adjusting the involved parameters. When a deviation from the standard occurs, the instrument calibration procedure is automatically launched and the accuracy is restored. In addition to that, key indicators - like the number of relay commutations - give information about the instrument wear, allowing for the schedule of predictive maintenance interventions. This prevents unexpected stops of the tester operations, and permits to reduce the number of interventions required. Dedicated sensors constantly monitor the operating temperature and humidity, to detect any dangerous condition. The data are stored both locally, on the instrument memory, and made available for further analysis and correlation to any anomaly in the machine performance.



➤ The channel instrument of DOT testers is a modular board, incorporating all the analog, digital, signal processing resources to test the devices.

Thanks to these features, testing equipment can become an interactive part of the production floor, in an Industry 4.0 perspective. The adoption of this solution on a fab-wide scale helps semiconductor manufacturers save on scheduled and unscheduled downtime, keeping the process quality under absolute control. Testing semiconductor devices more intelligently can bring better product quality, less resources employed, more throughput, and reduced downtime.



➤ The tester is able to self-assess its measurement accuracy, recalibrating the instrumentation when needed. Key parameters about the instrument wear status, and the operating conditions, are constantly monitored, notified, and analyzed, allowing for an effective predictive maintenance schedule.

ULVAC ENVIRO™ Plasma Ashing Systems

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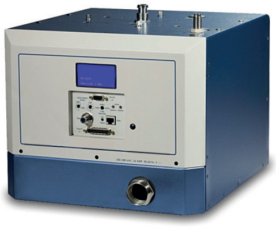
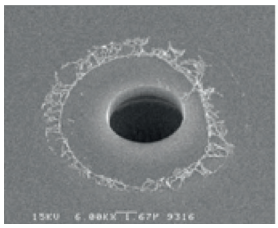
Plasma Source Options for ENVIRO

ICP Source

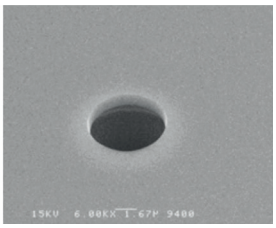
The original Optima was designed for high throughput and high reliability utilizing a compact, inductively coupled plasma (ICP) source. To meet the demands for high productivity, the process focus was on high film removal rates, MEMS applications, and high dose implant strip (HDIS).



Post Bosch Process Residue Removal



➤ After Conventional Ash Process



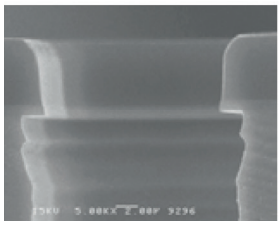
➤ After ENVIRO Ash Process

MEMS Device Descum

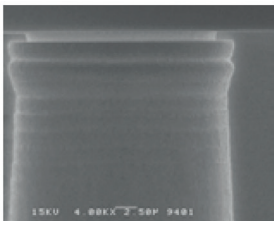
➤ Pre Descum

➤ Post Descum

Post Deep Silicon Etch Resist Removal



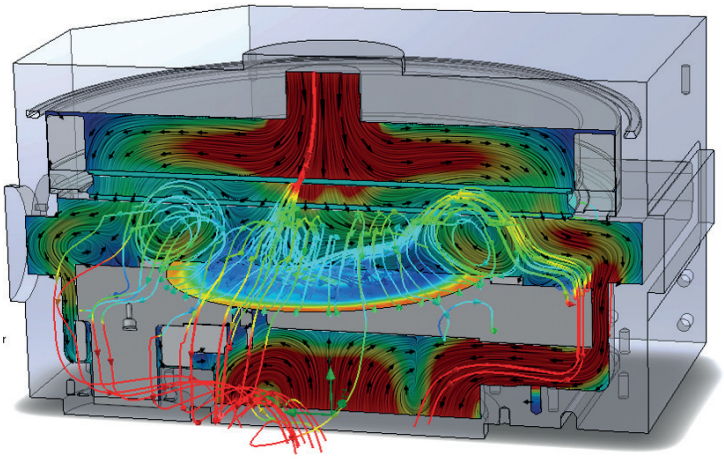
➤ Pre Ashing



➤ Post Ashing

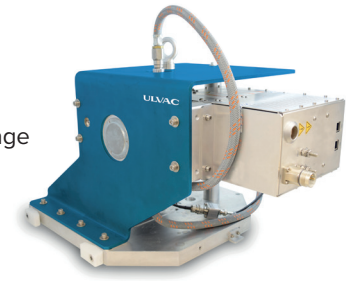
MW Source: Expanded Process Capabilities

With the addition of microwave frequency plasma source technology, the Optima can support a wider range of process chemistries to address low temperature polymer removal and low oxidation of substrate materials. The microwave energy provides low plasma induced damage with test results indicating approximately 50% reduction from the ICP source.



➤ Configured with either Microwave or ICP as downstream plasma option, and RF Bias as an independent plasma option, the Optima continues to support the needs for high volume production with its ability to replace multiple legacy systems with a single Optima tool. ULVAC customers have put into mass production one Optima system to replace from three to seven legacy dry strip systems.

- Wider range of process chemistry
- Low temperature polymer removal
- Low oxidation of substrate materials
- 50% reduction in plasma induced damage



RF Bias Source: More Expanded Process Capabilities

RF Bias source is the latest addition to Optima's plasma options, which further expands Optima's process capabilities. RF Bias plasma can act on its own, or be used in conjunction with MW or ICP downstream plasma source. Chemical and physical ashing/etching can be achieved at the same time, to address a wider range of processes:

- Carbonized skin layer removal in high dose implant strip
- Anisotropic low temperature descum
- Light etching
- High aspect ratio cleaning

ULVAC

About ULVAC Europe

ULVAC GmbH was established in 1987 as the European subsidiary of ULVAC, Inc. Headquartered in Munich, Germany. From Munich, our sales and service team serve the EMEA region. ULVAC provides a very broad portfolio of manufacturing equipment for the vacuum, materials, and thin film industries.

ULVAC's solutions diversely incorporate equipment, materials, analysis, and services for semiconductors, MEMS, flat panel displays, electronic components, PCB, TFB and other vacuum equipment.

ULVAC offers state-of-art products and technologies for semiconductor and related processes. To support MEMS, power devices, and NVM fabrication, ULVAC offers equipment for sputtering, evaporation, plasma etch, ashing, ion implanting, oxidation/POA/nitridization, and activation annealing for both R&D, pilot line, as well as high volume manufacturing. A complete line of vacuum components is also offered which includes vacuum pumps of all types, helium leak detectors, UHV systems and gauges, RGA's and thermal analysis instrumentation.

At ULVAC we pursue leadership in vacuum technology to realize innovation for our customers.

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Pfeiffer Vacuum HiPace Turbopumps Combines High Performance with Reliability

The Pfeiffer Vacuum **HiPace-I** series turbo molecular vacuum pumps have been specifically developed for ion implantation processes with the goal of increasing pump lifetime for the harshest ion implantation environments.

Problem

Today, the process of ion implantation is widely used for fabricating modern micro devices. This process requires high vacuum which can only be provided with high performance turbomolecular vacuum pumps. In the source chamber of the ion implantation tool several process gases will be introduced which causes the accumulation of many byproducts inside the turbopump. Due to the byproduct accumulation, the life expectancy of the turbopump can be negatively affected.

Solution

The Pfeiffer Vacuum **HiPace-**I series combines performance with reliability due to a new nickel-coated rotor technology. The revolutionary rotor design also provides good compression ratio for light gases such as He and H_2 without the use of a drag (Holweck) stage. The elimination of the drag stage provides a bigger gap between the rotor and the housing and greatly reduces pump failure caused by the accumulation of byproducts.

Pumping Speed Class	Implant Standard	Implant Heated
1200 l/s	HiPace 1200 I	HiPace 1200 IT
1500 l/s	HiPace 1500 I	HiPace 1500 IT
1800 l/s	HiPace 1800 I	HiPace 1800 IT
2300 l/s	HiPace 2300 I	HiPace 2300 IT
2800 l/s	HiPace 2800 I	HiPace 2800 IT

The **HiPace-I** series turbopumps can be equipped with specially developed accessories for implantation processes such as a heating jacket in combination with a temperature monitoring system (TMS) and a sealing gas monitoring system.

Applications

HiPace-I series can be used for the source and beamline chambers of the implantation tool. For use with the source chamber, a heated pump version is recommended.

Platforms

The **HiPace-I** series is available in several sizes with pumping speeds ranging from 1200 to 2800 l/s and is offered in ISO-F, ISO-K and ISO-CF flange types.

Availability

Available worldwide now.

To promote your products and services contact: **Shehzad Munshi**
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