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INSIDE

News Review, Features
News Analysis, Profiles
Research Review
and much more...

ELECTROPLATING ENABLES INDIUM BONDING

Flip-chip bonding is essential to hybridization, the process of combining die from differing technologies

FIRST SEMI-DAMASCENE MODULE

Semi-damascene integration is an attractive, cost-effective approach to extend process flows below 20nm metal pitch

SAMSUNG DEVELOP SILICON PICS FOR LIDAR

Incorporating silicon photonic integrated circuits into advanced CMOS has challenging requirements



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VIEWPOINT

BY MARK ANDREWS TECHNICAL EDITOR

Capacity-driven Fab expansions continue to fuel spending sprees

➤ The message came loud and clear: We need more chips! The 'we' in this case included major OEMs as well as consumers – practically anyone trying to buy anything that was suddenly unavailable because the product's 'brain' was sitting in a cargo ship or amongst the backlogged orders at myriad global Fabs.

The semiconductor industry has heard from many voices and it quickly became clear that demand was going to continue outstripping supply unless new Fabs were built and existing facilities expanded.

Fast-forward to the middle of 2022 and we see shovels hitting sand in 60 new Greenfield projects along with many expansions, altogether about 110 global Fab projects.

With so much capacity pending, some wondered: will there be oversupply by 2024 and beyond? Investors bank-rolling the Fab spending spree don't think so and neither do IC manufacturers.

The SEMI trade association reported recently that Fab equipment spending was expected reach \$109 billion this year, a new record and 20 percent more than last year's record that was itself 42 percent greater than 2020. As noted by Ajit Manocha, president and CEO of SEMI, "The global semiconductor equipment industry remains on track to cross the \$100 billion threshold...This historic milestone puts an exclamation point on the current run of unprecedented industry growth."



No kidding. What did not make the really big headlines was the equally fantastic fact that compared to 2019, spending on Fab equipment in 2022 will be two times greater.

As this edition of Silicon Semiconductor nears publication, industry leaders from across the globe will converge in Brussels for AngelTech 2022, investing 28-29 June to attend three co-located conferences focused on growth and opportunities in compound semiconductors, sensors, and photonic integrated circuits (PICs).

Two weeks later many of these same persons will regroup in San Francisco, California for SEMICON West, looking for insights into future silicon technologies.

In this edition of Silicon Semiconductor we explore the latest research advances by imec. We also hear from Nel Hydrogen discussing the timely way manufacturers can best access high-purity hydrogen that could also exempt them from future supply chain headaches. We also explore innovations by ClassOne Technology and MacDermid Alpha that enable the use of indium for flip-chip bonding in high performance image sensors.



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AVOID HYDROGEN SHORTAGES WITH ON-SITE GENERATION

A steady supply of high-purity hydrogen is critical to semiconductor fabrication. Recent post-pandemic supply chain interruptions have challenged manufacturers, leading to production stoppages



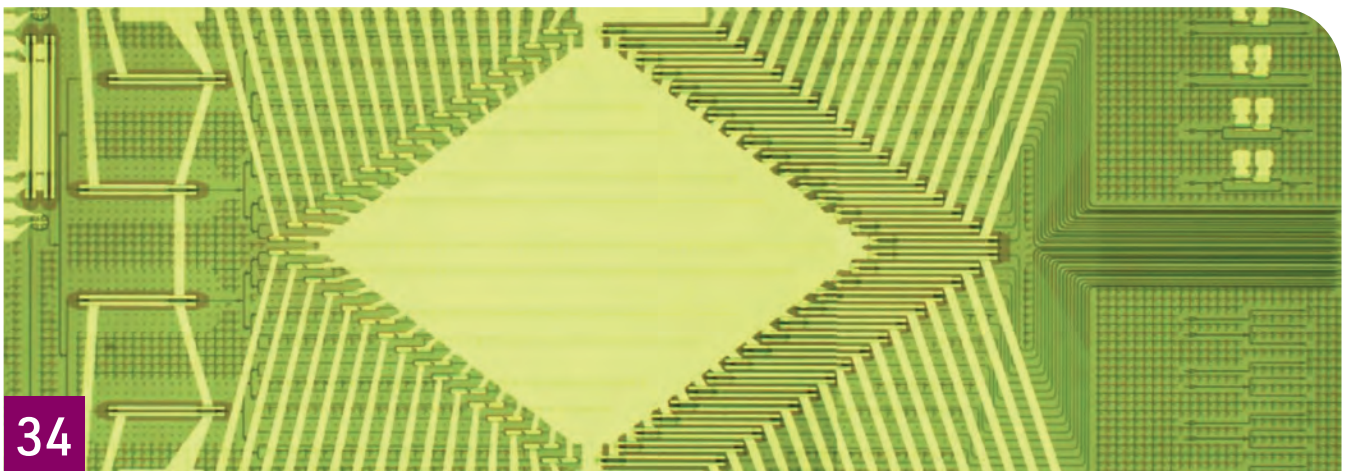
20 Electroplating innovation enables ultrafine indium bonding

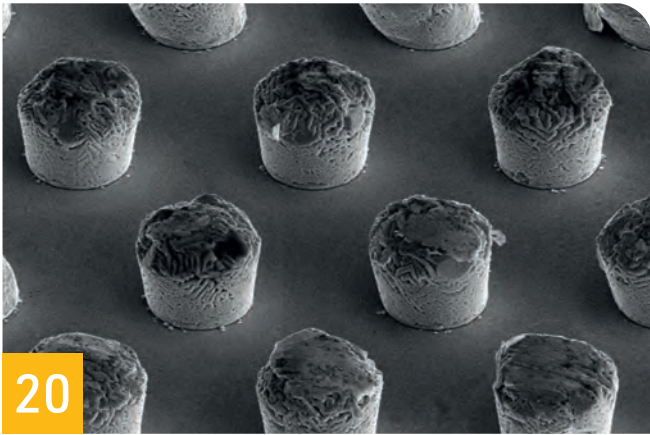
Flip-chip bonding is essential to hybridization, the process of combining die from differing technologies into a high performance module such as the hybrid pixel detectors found in LiDAR and other imaging applications

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Semi-damascene integration is an attractive, cost-effective approach to extend interconnect process flows below 20nm metal pitch

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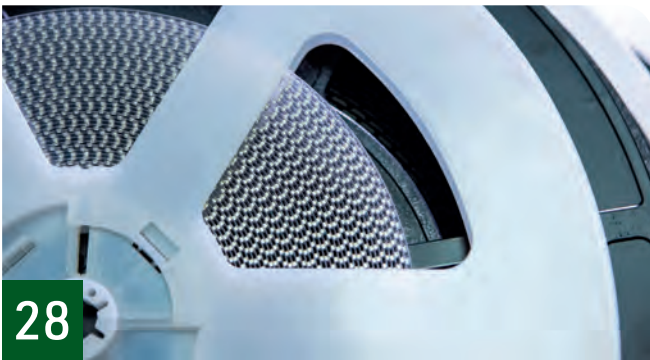
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28 New micro-textured film enables universal bare die carriers

Moving singulated die within production environments can pose many challenges. While safe transport solutions aplenty exist, all involve either tape and reel single use systems

34 Samsung progresses developing silicon photonics for LiDAR

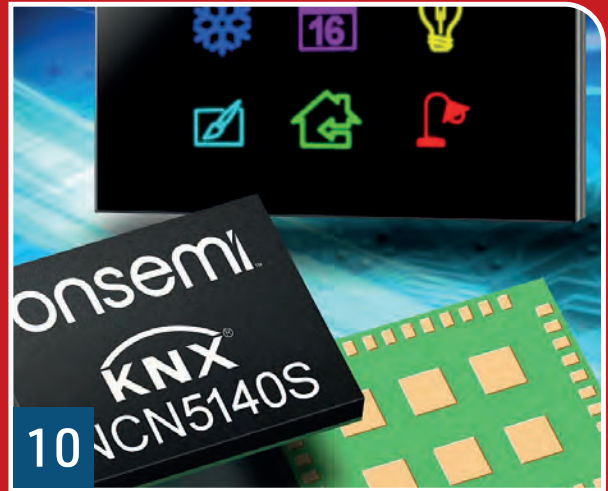
Microelectronics has revolutionized almost every aspect of life. Efforts to incorporate silicon photonic integrated circuits (PICs) into advanced CMOS ICs often center on requirements that II-VI or III-V technologies cannot solely address



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Cadence expands collaboration with Arm

CADENCE DESIGN SYSTEMS has announced it has extended its collaboration with Arm to accelerate mobile device silicon success using Cadence digital and verification tools and the new Arm Total Compute Solutions 2022 (TCS22), which includes the Arm Cortex-A715 and Cortex-X3 CPUs and the Arm Mali-G715 and Immortalis-G715 GPUs. Through the collaboration, Cadence has delivered comprehensive RTL-to-GDS digital flow Rapid Adoption Kits (RAKs) for 5nm and 7nm nodes to help customers achieve optimized power, performance, and area (PPA) goals and improved productivity. In addition, Cadence has validated mobile reference platforms for the Cortex-A715 and Cortex-X3 CPUs and the Mali-G715 and Immortalis-G715 GPUs to jumpstart customer verification flows.

Cadence Digital Flow for Arm Total Compute Solutions

The Cadence integrated digital RTL-to-GDS RAKs that have been optimized for SoC development using the latest Arm TCS22 include the Cadence Cerebrus™ Intelligent Chip Explorer, Innovus™ Implementation System, Genus™ Synthesis Solution, Modus DFT Software Solution, Quantus™ Extraction Solution, Tempus™ Timing Signoff Solution and ECO Option, Voltus™ IC Power Integrity Solution, Conformal® Equivalence Checking and Conformal Low Power.

The digital RAKs provide Cortex-A715 and Cortex-X3 CPU and Mali-G715 and Immortalis-G715 GPU users with several key features. For example, the Cadence Cerebrus AI-driven flow optimization enables quick and efficient design-specific closure with reduced engineering effort. Cadence iSpatial technology provides an integrated and predictable implementation flow for the fastest design closure.

The RAKs also include an innovative smart hierarchy flow to deliver better turnaround times on large, high-performance CPUs. The digital flow's integrated Tempus ECO technology for signoff offers accurate, final design closure based on path-based analysis.



Finally, the activity-aware power optimization engine incorporated with the Innovus Implementation System and the Genus™ Synthesis Solution significantly reduces dynamic power consumption, enabling customers to achieve low-power goals.

Cadence Verification Flow for Arm Total Compute Solutions

The verification flow includes the Cadence Xcelium™ Logic Simulation Platform, Palladium® Z1 and Z2 Enterprise Emulation Platforms, Helium™ Virtual and Hybrid Platforms, Jasper® Formal Verification Platform, vManager™ Planning and Metrics, VIP and System VIP tools and content for Arm-based designs.

The Cadence verification flow enables customers to improve verification throughput and achieve advanced software debug for SoCs containing the Cortex-A715 and Cortex-X3 CPUs and Mali-G715 and Immortalis-G715 GPUs. Furthermore, the virtual and hybrid platform reference designs include the Arm Fast Models to enable early software development and verification using the Cadence Helium and the Palladium and Protium platforms, also known as the dynamic duo.

“With the delivery of Arm TCS22, we’re enabling customers to create high-performance, high-efficiency and secure

products that provide an optimal user experience across a variety of mobile applications,” said Paul Williamson, vice president and general manager, Client Line of Business, Arm. “By continuing to collaborate with Cadence, our mutual customers can leverage our latest Armv9 CPUs and the Mali-G715 and Immortalis-G715 GPUs alongside the Cadence digital and verification flows to deliver SoCs to market faster.”

“This latest collaboration with Arm further demonstrates our commitment to empowering designers to create the world’s most advanced mobile designs that provide the best user experience,” said Dr. Chin-Chi Teng, senior vice president and general manager, Digital & Signoff Group at Cadence. “Arm has utilized the latest Cadence digital and verification flow innovations to develop Arm TCS22, and we’re jointly enabling customers to leverage these latest innovations to realize optimal power and performance results and a faster path to tapeout.”

The Cadence digital flow enables customers to achieve PPA goals, and the verification full flow provides improved verification throughput.

Both flows support the Cadence Intelligent System Design™ strategy, which enables customers to achieve SoC design excellence.

Ansys joins Intel Foundry Services Cloud Alliance

ANSYS has announced that it has joined the Intel Foundry Services (IFS) Cloud Alliance. IFS is a fully vertical, standalone foundry business announced by Intel last year. As part of the company's commitment to meet the growing demand for foundry capacity, Intel is partnering with cloud service providers and EDA suppliers to enable a secure design environment for customers on the cloud. Ansys tools, including Ansys RedHawk-SC, Ansys HFSS, Ansys Totem, Ansys® PathFinder, Ansys® VeloceRF™ and Ansys® RaptorX™, are available as part of this interoperable, cloud-enabled semiconductor design flow that will help enable current and future Intel customers to enhance their productivity.

RedHawk-SC is a next-generation system-on-chip (SoC) power noise signoff platform that is built on Ansys SeaScape, the world's first custom-

designed, big data architecture for electronic system design and simulation. Its underlying highly-scalable elastic compute architecture takes full advantage of the cloud, enabling customers to load the largest designs within seconds and quickly explore thousands of scenarios.

"We are pleased to announce the launch of the IFS Cloud Alliance to accelerate design on the cloud," said Rahul Goyal, vice president and general manager of Intel Product and Design Ecosystem Enablement. "We are excited to have Ansys as an alliance partner and look forward to continued collaboration with Ansys to enable efficient reliability and verification flows on the cloud."

The Cloud Alliance advances semiconductor design by ensuring that chip designers have a robust, interoperable EDA workflow that is

easily accessible via the cloud. The workflow allows customers to focus on creating unique product ideas, rather than operational tasks.

"Our comprehensive suite of interoperable multiphysics analysis solutions are a key part of IFS first design flow supported on the cloud," said John Lee, vice president and general manager of the semiconductor, electronics, and optics business unit at Ansys. "IFS chose Ansys as their multiphysics partner, as the Ansys platform helps enable customers to work on delivering unique new capabilities while benefiting from Ansys' gold-standard simulation accuracy within popular EDA design flows"

RedHawk-SC and other Ansys multiphysics solutions work with other Ansys tools, EDA implementation flows, and even customers' internally developed solutions.



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AEM to create over 300 additional jobs with the expansion plans

AEM, has announced its expansion plans. With a new site in Penang and the US, AEM will also expand its research and development centers ("R&D") in the aforementioned countries and Singapore, with the new facilities scheduled to start operating by the end of Q3 2022. The expansion of AEM's Penang, the US, and Singapore manufacturing sites will more than double its current manufacturing space in the three countries and create over 300 additional jobs. In particular, AEM's Penang expansion will include an R&D lab that will allow AEM to increase its R&D capabilities, with a strong focus on delivering technologies and solutions for advanced, integrated semiconductor test needs. AEM will also double its headcount in Malaysia to support the expansion, including new roles for technicians, engineers, customer support group, and supply chain management.

This expansion allows AEM to tap on the region's growth opportunities and talents and brings its operations closer to existing and potential customers. AEM's US expansion will include R&D, prototyping, and manufacturing in Arizona and California, while the expansion in Singapore will focus on R&D. "The ability to tap on a diverse talent pool and the high growth potential of Malaysia and Singapore is what makes the region an attractive location for AEM. Our expansion will allow us to better scale up our testing and handling capabilities in tandem with our customers' needs. It also further solidifies AEM's position as a hub in the region and its position as a critical node in the global semiconductor supply chain," says Juha Arola, AEM's Chief Operating Officer.

Malaysia is strategically positioned in the heart of Southeast Asia, a regional home to top semiconductor and electrical & electronics ("E&E") companies along with a large technology talent pool. The country is also a crucial player and hub in the semiconductor global supply chain, with approximately 7% of the total global semiconductor trade flowing through the nation. Additionally, the regional growth of the E&E sector is projected to increase by 15% in 2022, propelled by strong global semiconductor sales expected to grow by 13.6% in 2022.

"AEM's decision to expand its plant in Malaysia, notably in Penang highlights our attractiveness as a hub in the semiconductor industry on the world stage, driven by our well-connected and vibrant local E&E ecosystem. MIDA remains committed to growing our E&E and semiconductor industries, working hand in hand with our strategic investors such as AEM. AEM's expansion will provide new impetus to our efforts to further strengthen Malaysia's competitiveness in the global E&E value chain while also spurring socio-economic development to our local vicinities; this is indeed a "win-win" situation for both the company and our country in line with the National Investment Aspirations (NIA)," says Datuk Arham Abdul Rahman, Chief Executive Officer of the Malaysian Investment Development Authority (MIDA).



OPTIM Wafer Services is pleased to announce the installation of an automated ALPSITEC MECAPOL E550 CMP tool at its site in Greasque France.

The system will allow OPTIM to offer for following new or improved services.

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- Oxide Roughness Improvement
- Metal CMP
- Poly CMP

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- Edge Trimming
- Wafer Dicing
- Dice Before Grinding
- Wafer Cleaning
- Process development services, combining any of the above capabilities.

For detailed technical discussions please contact either Mr. Mark Wells or Mr. Georges Peyre using the contact details below or visit our website.

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onsemi accelerates building automation

SUPPORTING major building automation protocols, new, fully integrated devices shorten development of smart building control panels and connected lighting

onsemi, a supplier of intelligent power and sensing technologies, has announced the introduction of two complete system solutions supporting the most widely used building automation network protocols - Power over Ethernet (PoE) and KNX.

Easing the development of access and control panels, the NCN5140S is the first System-in-Package (SiP) certified with the KNX Association. The NCN5140S integrates all critical

and certifiable elements of a KNX device, including a digital KNX transceiver, a 32-bit Arm® Cortex®-M0+ microcontroller with a pre-certified software stack, and system power DC/DC converters, into a single package. With its high degree of integration, the NCN5140S considerably reduces material costs and allows manufacturers to develop very slim and modern designs (<5 mm total depth).

Alongside the NCN5140S, onsemi has introduced a complete solution for ethernet-powered connected lighting. Unique to any other device on the market, the NCL31010 integrates an intelligent LED driver and PoE interface into a single package. This provides support for both the lighting and power delivery needs of fully connected and managed lighting systems.

“As building automation installations continue to gain greater momentum, the industry needs solutions that incorporate necessary functionality in a simple, compact package,” said Michel De Mey, vice president of the Industrial Solutions Division, onsemi. With our pre-certified KNX SiP and new intelligent LED driver, onsemi provides manufacturers with the latest

technology and the head start they need to develop complex, full-scale automation systems in a shorter time.” KNX products must demonstrate compliance to supported protocols and profiles through the association’s certification program to ensure seamless connectivity.

Because the NCN5140S platform is pre-certified, products based on the device inherit this compliance, and KNX certification testing is not necessary. All that is needed is a KNX declaration of product modification, eliminating the time and engineering efforts of a complete certification process.

The IEEE 802.3bt compliant NCL31010 can deliver over 90 Watts via PoE. An innovative application for this device, made possible by the highly efficient buck LED driver, is called Visible Light Communication (VLC). This involves modulating data directly onto the LED light, which remains imperceptible to the human eye, allowing it to broadcast data and function as a location beacon for use in indoor positioning systems. The NCL31010 and the NCN5140S are available now through onsemi sales support and authorized distributors.



Lam Research teams up with SK hynix

LAM RESEARCH has announced that SK hynix has selected Lam’s innovative dry resist fabrication technology as a development tool of record for two key process steps in the production of advanced DRAM chips. A breakthrough technology introduced by Lam in 2020, dry resist extends the resolution, productivity, and yield of Extreme Ultraviolet (EUV) lithography, a pivotal technology used in the production of next-generation semiconductors.

Through Lam’s work with SK hynix and ongoing collaboration with ecosystem partners on dry resist technology, the company continues to take a leadership role in driving patterning innovations to remove the roadblocks associated with scaling to future memory nodes with EUV lithography. “Lam’s dry resist technology is a game-changer.

By innovating at the material level, it addresses EUV lithography’s biggest challenges, enabling cost-effective scaling for advanced memory and logic,” said Richard Wise, vice president and general manager of the dry resist product group at Lam. “We are proud to continue our long-standing collaboration with SK hynix to accelerate DRAM technology innovations.”

SK hynix intends to use Lam’s dry resist underlayer and dry development processes for advanced DRAM patterning. “As DRAM continues to scale, innovations in EUV patterning are critical for delivering the performance needed for today’s increasingly connected devices at a cost that is right for our customers,” said BK Lee, head of R&D process at SK hynix. “The dry resist technology that we are working on with

Lam enables exceptionally precise, low defect, and lower cost patterning.”

As chipmakers move to advanced technology nodes, they must resolve ever smaller and finer chip designs on the wafer. First developed by Lam in collaboration with ASML and IMEC, dry resist technology offers several advantages over conventional chemically amplified resist patterning for EUV lithography. Dry resist technology solutions significantly enhance EUV sensitivity and the resolution of each wafer pass, enabling patterns to better adhere to the wafer and improving performance and yield. In addition, Lam’s dry resist development approach offers key sustainability benefits by consuming less energy and five to ten times less raw materials than traditional chemical wet resist processes.

Imec unites partners to target net-zero emissions

AT FUTURE SUMMITS 2022, imec, a leading research and innovation center in nanoelectronics and digital technologies, has announced that its Sustainable Semiconductor Technologies and Systems (SSTS) research program succeeded in bringing together stakeholders of the semiconductor value chain, from large system companies such as Apple and Microsoft, to suppliers, including ASM, Kurita, SCREEN and Tokyo Electron.

The program was set up last year as part of imec's sustainability efforts to support the semiconductor industry reducing its carbon footprint.

The addition of these new partners enables a holistic approach, which leverages imec's expertise and knowledge to cut the industry's environmental impact.

The semiconductor industry is booming with a never-seen demand. As an integral part of our smart portable devices, IoT systems and compute infrastructure, chips are embedded in our everyday life. Semiconductor manufacturing, however, comes at a price. It requires large amounts of energy and water and creates hazardous waste.

To tackle this problem, the entire supply chain needs to commit, and an ecosystem approach will be key. While system and fabless companies are already investing in decarbonizing their supply chain and products, committing to be carbon neutral by 2030 or 2040, they typically lack accurate insight into the contribution of chip manufacturing of future technologies as there is limited life cycle analysis data available.

With its SSTS program, imec calls upon the whole semiconductor value chain to join forces to cut back on the semiconductor industry's environmental footprint.

It combines imec's strong partner ecosystem, insights in processing technology, infrastructure, and machinery to provide partners across

the semiconductor value chain insight in the environmental impact of certain choices made at the chip technology's definition and production phase.

Apple was the first public partner to join hands with imec on the SSTS program last year. Now additional major system companies like Microsoft have joined the program.

The program assesses the environmental impact of new technologies, identifies high-impact problems and defines greener semiconductor manufacturing solutions.

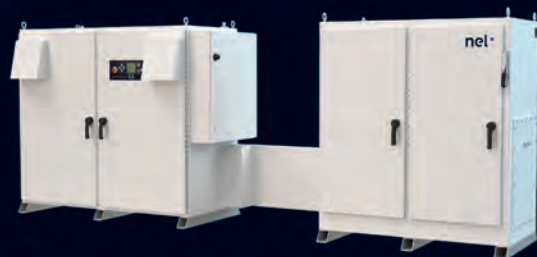
"Today there is a data gap concerning the environmental footprint of the fabrication of semiconductor integrated circuits (IC) for more advanced technologies.

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EV Group earns outstanding 10th consecutive triple crown win

EV GROUP (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets, has announced that it has once again been voted by customers as one of the 10 BEST Focused Suppliers of Chip Making Equipment and one of the 2022 THE BEST Suppliers of Fab Equipment in the 2022 TechInsights Customer Satisfaction Survey (formerly known as the VLSIresearch Customer Satisfaction Survey), increasing its score in both award segments compared to last year's listings as well as earning a 5 Star rating for the first time in both segments.

EVG also received a RANKED 1st in Specialty Fab Equipment award again this year, marking the 10th year in a row that it has received all three customer satisfaction awards.

In addition, for the sixth year in a row, EVG was recognized as one of THE BEST Suppliers of Fab Equipment to Specialty Chip Makers—increasing its score in this award category while achieving a 5 Star rating for the second time in a row.

A white paper detailing EVG's survey results issued by TechInsights is available at: https://www.techinsights.com/sites/default/files/2022-06/WP_CSS_EVG_22_06v1_0.pdf.

According to TechInsights, EVG earned its highest 10 BEST rating ever this year,

with customers rating the company best at partnering, trust in supplier, recommended supplier and technical leadership. 2022 marks the 20th consecutive year that EVG has been listed among THE BEST Suppliers of Fab Equipment, as well as the 10th year EVG has achieved the number one spot as the highest ranked wafer bonder supplier.

"Once again, EV Group outperformed most of its peers, earning its first 5 Star rating for 10 BEST Focused Chip Making Equipment Suppliers for the first time while increasing its ratings in nearly every category and improving its overall rating for the fifth consecutive year," stated G. Dan Hutcheson, vice chair of TechInsights.'

"EVG's strong focus on process knowledge is key to developing its core capabilities of wafer bonding, lithography, and metrology. At the same time, the company's Triple-i philosophy of "invent-innovate-implement" guides EVG's enthusiasm for technology, innovative strength, and internationality, which in turn helps enable its customers to successfully commercialize their new product ideas."

"Customer satisfaction is at the core of our business philosophy," stated Hermann Walzl, executive sales and customer support director at EV Group. "During the past year, EVG has continued to make significant investments, not only in our technology but also in our employees and services,

in order to bring the best possible solutions and support to our customers. For example, our recently opened state-of-the-art customer training facility, the EVG Academy, has continued to expand its offerings for both EVG employees and customers, including technical training, general introductory courses, language training and soft skills development.

"In just one year, more than 100 technical training courses have been held, with more than 1300 certificates issued. In addition, with the lifting of COVID-19 travel restrictions, EVG has experienced all-time-high demand for our product demonstrations and process development services at our NILPhotonics® Competence Center and Heterogeneous Integration Competence Center", which serve as innovation incubators to shorten development cycles and time to market on new products and applications driven by advances in nanoimprint lithography, and system integration/packaging, respectively."

EVG offers a complete portfolio of wafer-level manufacturing solutions for a wide variety of micro- and nanotechnology applications and products, addressing established as well as emerging markets. The company's field-proven equipment, combined with EVG's superior process expertise and development support, enable its global customer base to stay one step ahead of the competition.





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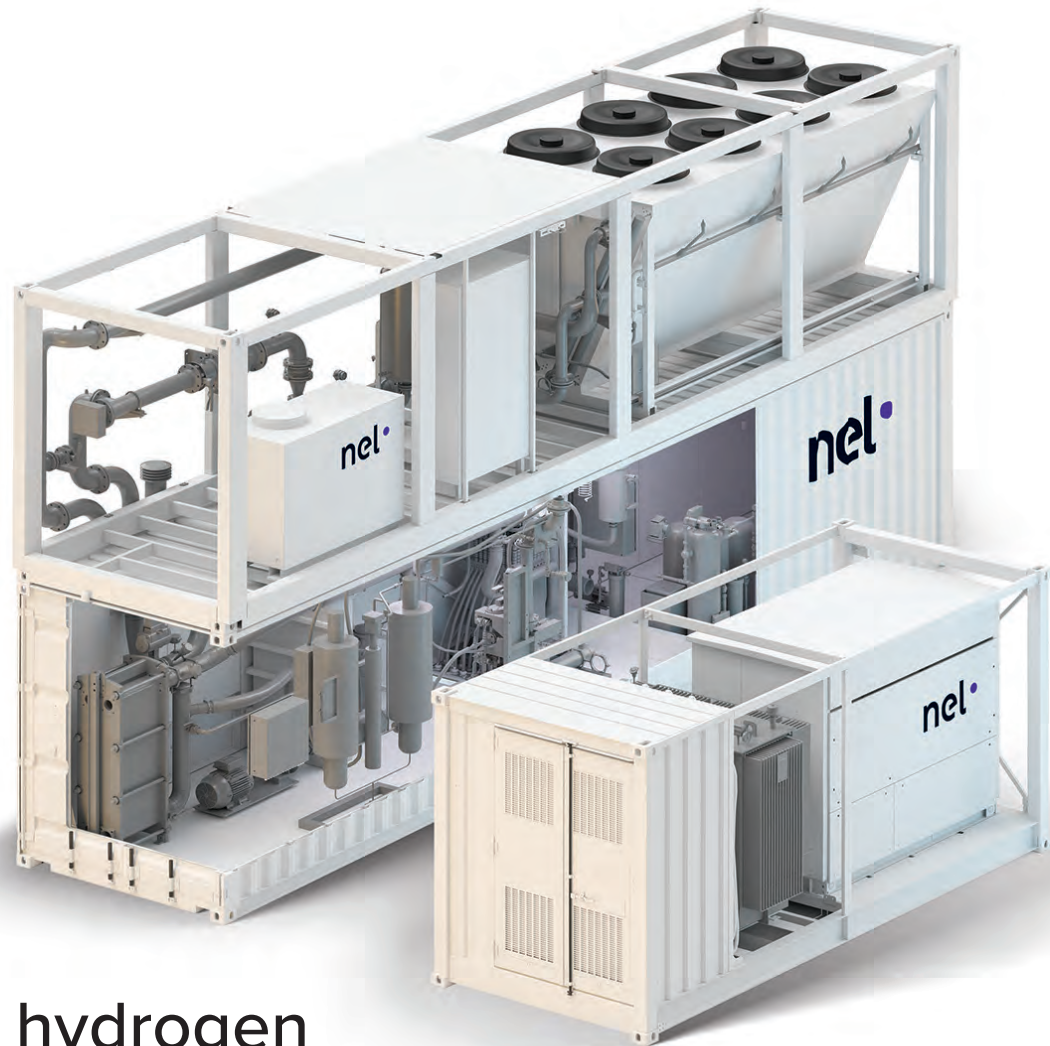
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Avoid hydrogen shortages with on-site generation

A steady supply of high-purity hydrogen is critical to semiconductor fabrication. Recent post-pandemic supply chain interruptions have challenged manufacturers, leading to production stoppages. On-site hydrogen generation offers a scalable alternative for new and existing fabs, eliminating the need for hydrogen storage, and freeing the operator from dependence on gas delivery.

BY LYNN GORMAN, **FREELANCE TECHNICAL WRITER**

READERS OF SILICON SEMICONDUCTOR understand the critical role that hydrogen plays in semiconductor fabrication. Hydrogen facilitates crystal growth, wafer annealing, acts as a carrier gas and is important in the growing use of extreme ultraviolet (EUV) lithography at 7nm nodes and below. As the need for semiconductors vastly grows across all sectors of world economies, so does the need for hydrogen. The semiconductor industry is aware that supply challenges are damaging the production rates of cars, appliances, and myriad electronic devices. Simultaneously, the hydrogen market is facing its own trials.

Besides semiconductor manufacturers, other traditional consumers of hydrogen include chemical producers, hydrogenated fats and oil manufacturers, glass makers, metal fabricators, refineries, and thermal power stations. There are also newer applications for hydrogen that are putting a strain on supply. In the last decade, fuel cell forklifts have evolved from being non-existent to becoming the world's largest single application for liquid hydrogen. Another example of hydrogen's expanding industrial role is under trial right now: the use of hydrogen to fuel 18-wheel freight haulers, making short- and long-haul truck transport potentially the next major

On-site/pipeline hydrogen options for fabs

Technology	Capacity range	Primary raw material(s)	Inherent purity	Compression requirement
Steam-methane reformer (SMR)	Medium to large	NG, water	Low	Requires NG compression
PEM electrolysis	Small to large	Water	High	No mechanical compression needed
Alkaline electrolysis	Medium to large	Water	Medium	Generally requires hydrogen compression

➤ There are three ways to generate hydrogen on site that are amenable to semiconductor operations: steam methane reforming, alkaline electrolysis, and proton exchange membrane (PEM) electrolysis.

growth area for hydrogen fuel. If the trucking sector adopts hydrogen fuel, that demand will be hundreds-fold larger than the forklift market.

As diesel fuel and gasoline rise in price and emissions laws tighten, hydrogen fuel will become increasingly attractive for transport. Even the need for hydrogen for space flight is growing with the rise of private space companies that are sending satellites into orbit at a faster rate than ever before; NASA’s ambitious planned return to manned space flight missions to the moon and beyond will only grow consumption.

“Closer to the semiconductor world, the return and expansion of semiconductor manufacturing in the United States will introduce more pressure on the liquid hydrogen supply, including the new entry of extreme UV lithography,” said David Wolff, Regional Manager at Nel Hydrogen. “The EUV trend alone will more than double the use of hydrogen in each of the largest and most sophisticated fabs.”

In addition to the disruption in global supply chains due to the pandemic along with more demand for hydrogen by multiple major consumers, there is another key reason why the production of hydrogen is taking a hit. Liquid hydrogen in the past was most often made from off-gas streams such as

byproducts from chlorine/caustic chemical plants and from petroleum refining; this source met most past needs. But the availability of off-gas hydrogen has declined considerably in recent years. To supply high quality hydrogen, industrial gas companies would typically buy excess hydrogen and then purify, liquify, and verify it for quality. They would then distribute by tanker trucks directly to customers or through terminals. Part of that hydrogen would be turned from liquid to gas for delivery in cylinders. Unfortunately, the availability of low-cost, raw gas hydrogen is dropping. Industrial scale operations producing low-cost raw gas hydrogen are starting to shut down due to environmental pressures.

In some cases, they are shifting capacity to other parts of the world with looser regulations. In other cases, the plants are closing and not being replaced because the end use applications for their primary products are disappearing permanently from the areas where they are located. A good example of this are chlorine/caustic chemical plants serving paper and PVC plastic markets.

This multi-faceted convergence of factors impacting how hydrogen is produced and in what quantities is affecting both the semiconductor market and the supply of delivered hydrogen. The confluence of increased demand and reduced supply is creating

Hydrogen supply chain can be simple or complex

	Depends on raw hydrogen third party supplier?	Depends on 15-40 year old purification and liquefaction plant?	Depends on transportation and driver availability?	Depends on on-site equipment to produce or store hydrogen for use?
Delivered liquid hydrogen	✓	✓	✓	✓
On-site generated hydrogen				✓

➤ On-site hydrogen generation offers a highly simple supply chain depending only on water and electricity at a facility.

Hydrogen supply options: delivery vs. generation

Hydrogen source	Volume range	Advantages	Drawbacks	Anticipated trend
LH ₂ delivery	Medium 300 k-3 MM scf/mon	Inherent purity Low capital investment	Contract implications Pricing volatility Supply reliability?	Shortages Reliability issues Price increases
Compressed hydrogen delivery	Low < 500 k scf/mon	Low capital investment Excellent for infrequent use	Contract Relatively high gas price Purity	Shortages Reliability issues Price increases
On-site generation	Low to High	Stable pricing Designed for specific use	Capital investment Backup	Market share increase
Pipeline third party supply	Typically, high 3+ MM scf/mon	Predictable pricing	Dependency Reliability? Backup	May be attractive when possible

➤ A multi-faceted convergence of factors is affecting the semiconductor market and the delivered hydrogen supply. Certain commodity, specialty, and compound fabs are already using on site generated hydrogen for its economy, its space efficiency, and lowering the risk factor of relying on supply disruptions affecting delivered hydrogen.

such a conundrum that generating hydrogen on-site is becoming a compelling and practical consideration at semiconductor fabs of all sizes, capacities, and specialties. Certain commodity, specialty, and compound semiconductor fabs are already using on-site generated hydrogen due to its economy, space efficiency, and as a means to lower risks associated with delivered hydrogen that is subject to supply interruptions.

Extreme UV Lithography, or EUV, more than doubles a fab’s hydrogen consumption. EUV is a critical process step in the manufacture of next-generation ICs and is already being utilized by major manufacturers to produce advanced node devices. However, EUV deployment requires significant capital investments both for the EUV equipment itself and for the support of that equipment, including consumables. That support infrastructure includes hydrogen, which maintains the extremely important optical clarity EUV requires. Fabs utilizing EUV systems must either provide hydrogen at the point of use with on-site generated hydrogen, or it will have to be piped throughout the fab to reach the EUV process tool location. EUV systems are also very large—typically requiring a fab expansion or sizeable remodeling to accommodate requirements. On-site hydrogen generators can be setup alongside EUV systems, completely eliminating the need to pipe-in hydrogen and the costly infrastructure expansion needed to support a new EUV system.

“Among on-site technologies to create hydrogen suitable for semiconductor applications, there

are three that are amenable to semiconductor operations,” said Wolff.

One way to generate hydrogen, albeit to a small degree according to Wolff, is via steam methane reforming. In steam methane reforming natural gas is stripped of its hydrogen constituents and that hydrogen is subsequently purified for semiconductor use. A steam methane reformer is most suitable for medium to large facilities. It emits large quantities of carbon dioxide (CO₂) – a major greenhouse gas, so there are emissions regulations surrounding its use. But more importantly from an IC manufacturing standpoint, steam methane reforming produces inherently low purity hydrogen that demands further processing to be pure enough for semiconductor manufacture.

The second and third ways to generate hydrogen on-site are to use alkaline electrolysis or proton exchange membrane (PEM) electrolysis. Both techniques split apart water molecules to yield hydrogen without a CO₂ byproduct. They emit only oxygen and are therefore not subject to the same emissions controls and regulations as is steam reforming. Of the two, alkaline electrolysis is the older technology and yields hydrogen of medium purity; it can be refined further until it reaches semiconductor-level purity, but this process requires an additional mechanical compression step. PEM electrolysis can provide hydrogen from the smallest to the largest semiconductor facility because the equipment is made in a wide variety of sizes and designed to be expandable as needs grow, making

expansion more cost-effective. A PEM generator uses only water and outputs hydrogen at a very high purity level without requiring subsequent mechanical compression.

At present, semiconductor manufacturers typically buy extremely pure hydrogen and then purify it even more at the point of use (POU). In the past, palladium filter purifiers were widely used, but they were expensive to buy and subject to catastrophic failure under some process conditions. Palladium purification has been augmented and to some degree replaced using selective impurity removal devices called 'getters.' One of the features of PEM electrolysis is that it provides hydrogen which is at sufficient pressure to use with any type of purification method. Systems designed by Nel Hydrogen, for example, make hydrogen at 435 PSI (30 bar) with 99.9995 or 99.9998% purity, which is at sufficient pressure to use with any point of use purification device. The PEM process delivers extremely high purity hydrogen, any measurable contaminants are readily identified by Nel's system: oxygen, nitrogen, and water. If any of these exceed the limits for a particular IC manufacturing requirement, they can be removed with dedicated getter devices.

"Practically speaking, most semiconductor fabs may take a hybrid approach to hydrogen generation," said Wolff. "For example, there may be those that already have liquid supply tanks, and hydrogen stored in those might be considered as reserves, but not necessarily for the facility's baseload supply. The day-to-day requirements for hydrogen would be generated without increasing the area required for hydrogen storage. Hydrogen storage takes up a large footprint on a company's property because of

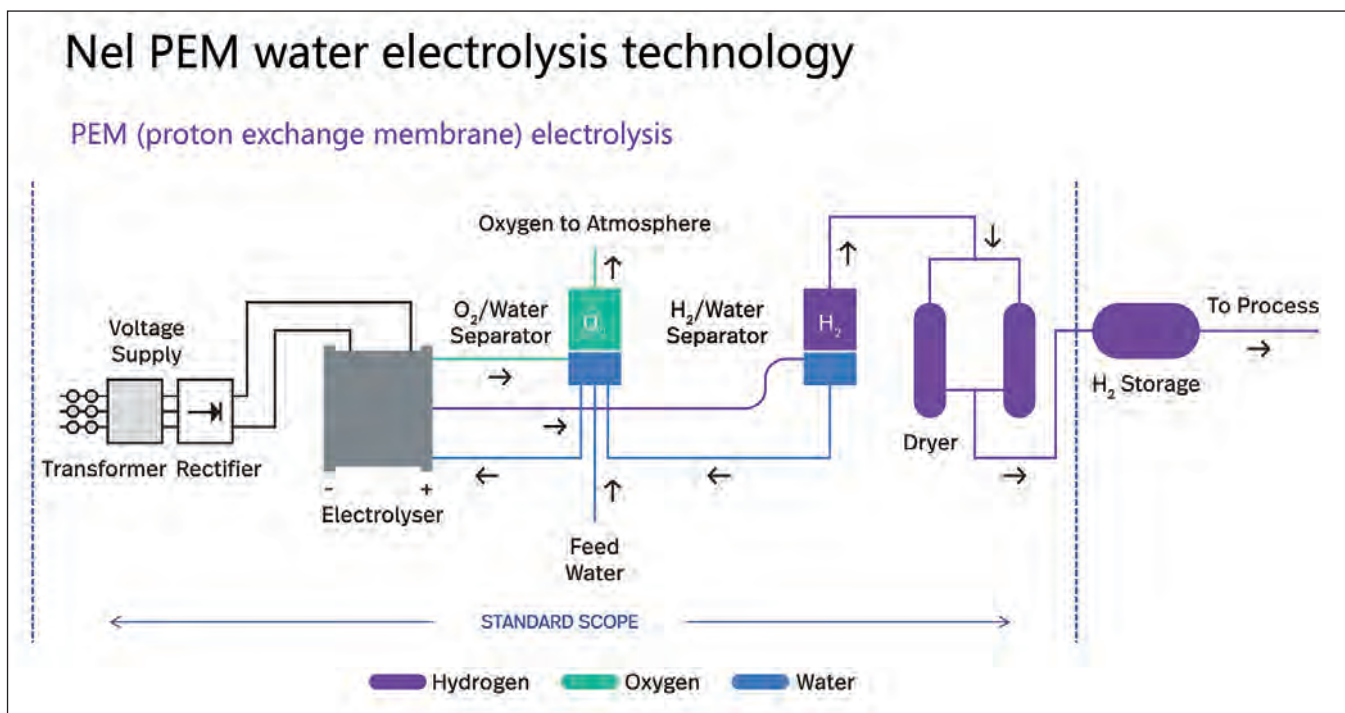
the safety clearance requirements around the highly hazardous hydrogen tanks."

Advantages that on-site PEM hydrogen generation provide for semiconductor manufacturers include no hydrogen storage; hydrogen generation that is ultra-pure and extremely dry. Having an on-site generator plant readily accommodates the ups and downs of production cycles with zero inventory. As plants expand, on-site generators also minimize new hydrogen piping and what is almost certainly a considerable disruption of plant operations needed to accommodate construction; this is especially important to new and expanding facilities. Electrolysis equipment for on-site generation is also portable; companies can take it with them if they move or reconfigure a plant's layout.

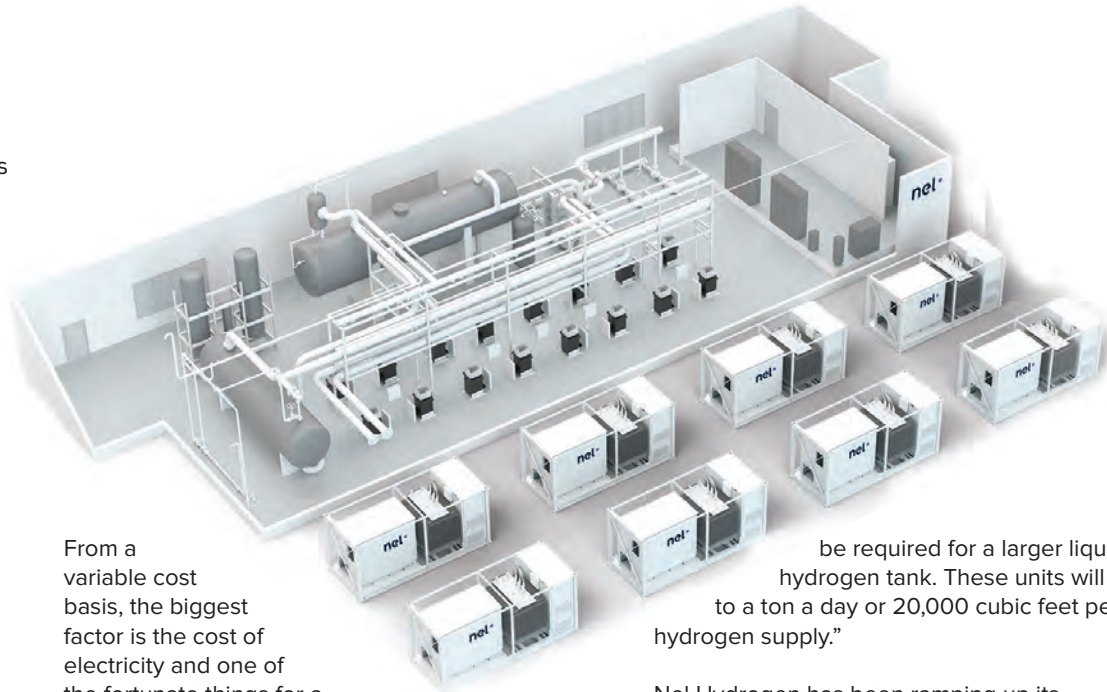
On-site hydrogen generation does require an investment of capital for the electrolyzers, but that capital may be less than other approaches to hydrogen supply. It will almost certainly be less expensive than building another gas farm. Further, typical capital equipment and construction savings can provide a quick return on the operator's investment.

"One of the attractive factors in electrolysis is its simple cost structure," explained Wolff. "Essentially the fixed cost is the cost of the hydrogen generator, and the variable costs are the electricity, the water to feed it, and a very small contribution from maintenance. Depending on the scale of the equipment, the fixed cost of hydrogen generation is anywhere from \$4 per 100 cubic feet of hydrogen supplies down to about \$1 per 100 cubic feet for the largest scale equipment. The larger the scale the greater the economy."

➤ Proton exchange membrane (PEM) electrolysis uses only water and outputs hydrogen at a very high purity level without requiring subsequent mechanical compression.



> Proton exchange membrane (PEM) Electrolysers



From a variable cost basis, the biggest factor is the cost of electricity and one of the fortunate things for a fabrication facility, especially those that are new or expanding, is that they often receive very low-cost energy arrangements that are typically underwritten by governmental agencies seeking to bring new industry to their areas. In situations where low-cost energy serves a site this can also contribute to lower cost hydrogen. In some plants around the world, green electricity is also in play. On average it takes 15 kilowatt hours to make 100 cubic feet of hydrogen. If the electricity cost is 6 cents per kilowatt hour, that means it costs 90 cents in electricity per 100 cubic feet of hydrogen produced. If there's a \$1 fixed (capital) cost per 100 cubic feet of hydrogen produced in a large semiconductor fab plus the 90 cents variable and a couple of pennies for maintenance, that equates to hydrogen costing under \$2 per 100 cubic feet, delivered at the purity and pressure that's required.

be required for a larger liquid hydrogen tank. These units will make up to a ton a day or 20,000 cubic feet per hour of hydrogen supply.”

Nel Hydrogen has been ramping up its manufacture of both alkaline and PEM electrolyser equipment, readying themselves for demand from semiconductor manufacturers and other markets. The company has been making electrolysers for nearly 100 years and has delivered over 3,500 units that are used in over 80 countries. Considering today's labor shortages, many fab managers may wonder who will operate this new hydrogen generating equipment, and what level of specialized training might be required for daily operation.

“There are a few scenarios in practice today,” reported Wolff. “Perhaps the most beneficial is the fact that electrolysers can be easily operated and maintained by current fab personnel because they take a minimal amount of attention and training. In some facilities, it's operated by the current supplier of delivered hydrogen. Some industrial gas and utility companies have field service personnel who can operate and maintain electrolysers at customer sites. There are also private companies getting established in certain geographical areas that are specializing in the operation and servicing of electrolysers, comparable to current water treatment and compressed air service company models.”

Hydrogen supply chains can be complex, or they can be simple. On-site hydrogen generation offers a highly simple supply chain depending only on water and electricity at a facility. Using PEM water electrolysis is a highly efficient means to provide semiconductor fabs with ultra-pure hydrogen to improve safety, quality, and productivity. It helps ensure production quantities of hydrogen will be available even as traditional methods of delivery are struggling to achieve pre-pandemic levels of efficiency. Further, as we can all appreciate at a time when chip shortages make daily media headlines, maximizing production uptime is more important today than ever before.

If more capacity is required, multiple unitized systems can meet growing needs so fabs can add capacity in blocks of up to 30 normal meters cubed per hour (Nm³/h) or fabs can step up to Nel's containerized systems to be installed outdoors

“If more capacity is required, multiple unitized systems can meet growing needs so fabs can add capacity in blocks of up to 30 normal meters cubed per hour (Nm³/h) or fabs can step up to Nel's containerized systems to be installed outdoors,” continued Wolff. “These start at 250 Nm³/h of ultra-pure hydrogen. Importantly, containerized systems do not require the excessive land area which would

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Electroplating innovation enables ultrafine indium bonding

Flip-chip bonding is essential to hybridization, the process of combining die from differing technologies into a high performance module such as the hybrid pixel detectors found in LiDAR and other imaging applications. The tin solders once used in flip-chip bonding are being replaced by lead-free alternatives including indium. However, creating the indium ‘bumps’ essential to forming bonds is challenging using conventional approaches. The experts at ClassOne Technology believe a new electroplating process solves the indium bump conundrum.

BY FARZANEH SHARIFI AND BRANDEN BATES, **CLASSONE TECHNOLOGY**;
ELIE NAJJAR, WENBO SHAO, PHD; ERIK YAKOBSON, PHD; AND BRIAN GOKEY,
MACDERMID ALPHA ELECTRONIC SOLUTIONS

HYBRID PIXEL DETECTORS are widely used for imaging applications ranging from high-energy physics to military, environmental and medical. Hybrid pixel detectors combine a pixel sensor chip with a readout integrated circuit (ROIC), which allows electronic access to every pixel in the detector. Pixel sensors are made of high-resistivity silicon, while low-resistivity material is required for the ROIC. Hybridization allows each one to be manufactured independently and then later coupled together through a process called flip-chip or bump bonding.

Flip-chip bonding creates a contact that provides high input/output (I/O) density and a short interconnect distance between the sensor pixel and the ROIC, enabling high device performance. During flip-chip bonding, the solder bumps are melted to form this connection. The pixels in a hybrid detector are placed in an array with less than 100-micron (mm) distance, or pitch, between them. This high connection density requires finer, more precise bumps and a very high-yield flip-chip process that ensures each pixel is connected to the IC.

Flip-chip evolution

Conventional flip-chip assembly was first achieved using lead-based solder bumps, but those materials have had to be revisited due to the worldwide banning of lead in electronic products due to its toxicity. However, lead-free alternatives such

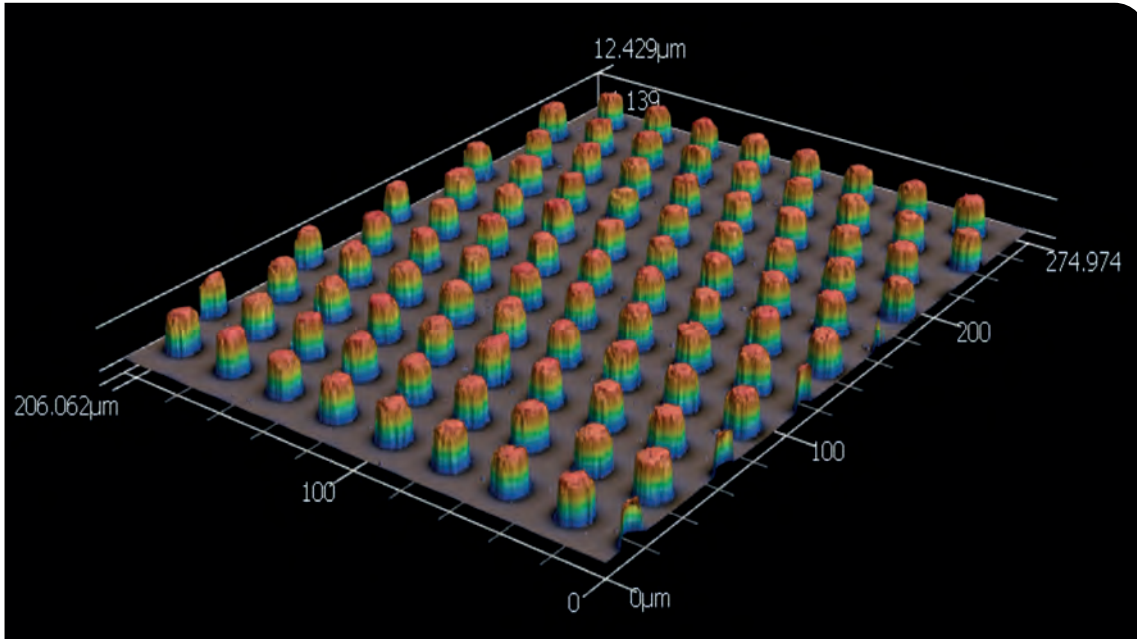
as pure tin or various tin-based lead-free alloys, e.g., SnAgCu (tin-silver-copper, or SAC), also face challenges with pixel detectors, so a viable alternative is a necessity.

Since the readout chips and sensor chips are made of different materials, a low-temperature fabrication process is necessary to reduce the thermal impact on the sensor chips due to a mismatch in coefficient of thermal expansion (CTE). Additionally, the sensors can face environmental extremes, from harsh radiation to cryogenic temperatures. Together, all these challenges require a new solder material with specific characteristics. We propose indium as one such preferred candidate.

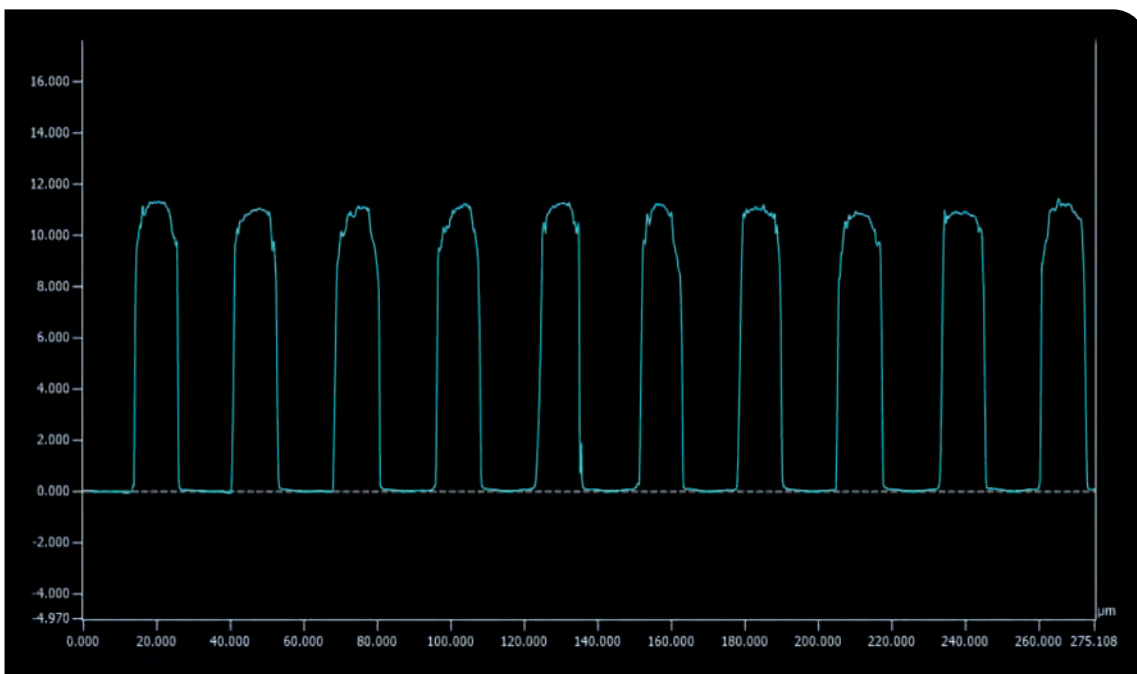
Why indium?

Indium is a soft metal (softer than lead) with a low melting point (156°C) that is highly malleable and ductile and retains these properties at very low temperatures, i.e., down to absolute zero (-273°C). This makes indium ideal for cryogenic and vacuum applications.

In terms of chemical properties, indium reacts with oxygen only at higher temperatures, doesn't dissolve in acids, has good adhesion to other metals, and has the ability to wet glass. Its good electrical conductivity, ductility, and low-temperature stability make it an excellent candidate for use in hybrid pixel detectors.



► Figure 1a & 1b: Confocal microscopy data (a) topography map of indium features (b) profilometry. The bumps were observed using a scanning electron microscope (SEM) as shown in Figure 2.



Older approaches

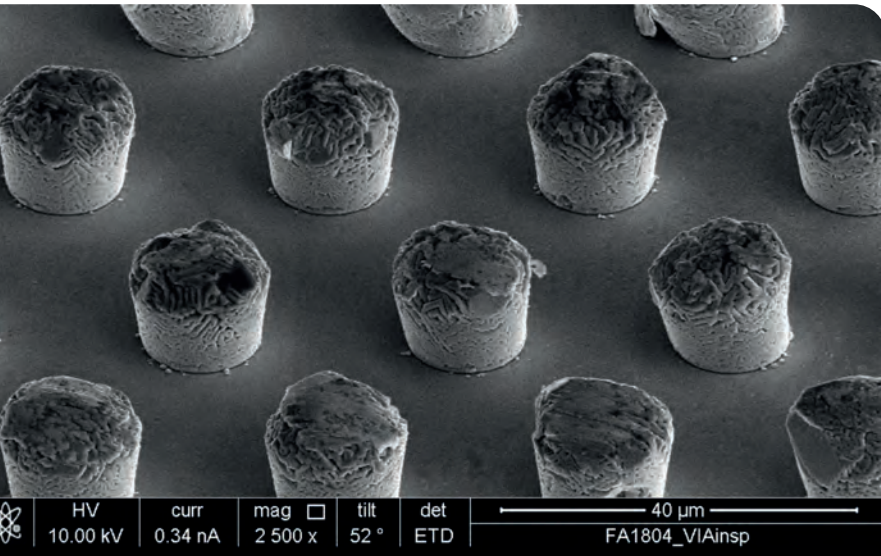
Indium bumps were previously fabricated via thermal evaporation, or sputtering, which yields highly uniform bumps with good bump structure control. However, this method cannot produce small bumps (higher aspect ratio) with a smaller pitch that's suitable for the semiconductor industry's current needs.

Moreover, indium sputtering requires expensive evaporation equipment, is limited to materials with high vapor pressure, requires a complicated fabrication process, isn't well suited to larger wafer sizes because of mask-to-wafer mismatch, is less environmentally safe as it creates more pollution, and is only viable for small-scale production.

In contrast, electroplating bumps with a high aspect ratio, at low cost, and with a simple fabrication process is achievable, especially for mass production. But conventional electroplating needs optimization, as non-uniform bumps cause failures in the fabrication process and reduce the hybrid chip's reliability. Evaporation of indium bumps for ultrafine pitch is difficult and time-consuming. Moreover, the waste of material on the photoresist mask renders the process non-cost-effective, and the smallest pitch size achievable through this approach is 30mm.

Electroplating challenges

Electroplating faces multiple challenges when utilized to create flip-chip bonding bumps: it must achieve the



► Figure 2. Scanning electron microscope images of indium bump

required uniformity and consistency of plated bumps, with ultrafine pitch, at wafer-scale and at high yield. It becomes even more challenging as the pitch shrinks and the number of bumps increases.

As wafer features shrink in size, bump sizes will decrease from 50 to 15 μm , with pitch sizes decreasing from 100 to 25 μm . Our goal was to demonstrate the capability of electroplating to generate high-density indium bumps with high quality and yield. Our work proved that electroplating smaller bump sizes with reduced pitch is achievable with the proper tool and material sets.

Process steps

Indium bumps are electroplated after under-bump metallization (UBM) is deposited on the silicon wafer. For the UBM, a barrier and adhesive layer such as titanium is needed, followed by an indium-wettable layer such as nickel or gold since nickel tends to oxidize quickly. The height of the indium balls is defined by the volume of the indium and the diameter of the wettable UBM pad. In our test, we used copper for the outer layer of the UBM. At temperatures around 125°C, some trivial amounts of indium form intermetallic phases with copper; then, for higher temperatures, a barrier metal such as nickel-gold or nickel-copper should be used.

After removing the top UBM layer (copper in our

tests), wafers are heated to a temperature at which the electroplated indium bumps form spheres due to the surface tension. The purpose of reflow is to increase bump height by reshaping the indium into a sphere and to help the flip-chip bonding alignment.

The copper seed layer is etched away with nitric acid mixed with water before reflowing. Titanium, a non-wettable material, was used to prevent the spread of indium across the surface during reflow. Indium has good adhesion to the top layer of the UBM (copper) but not the surrounding material (Ti).

Reflow must be performed in an oxygen-free environment, i.e., a controlled atmosphere in an oven; otherwise, indium oxide would form, impeding indium bump formation. In our study, the bumps were reflowed on a hot plate at a temperature of around 200°C, with nitrogen gas blowing on the surface.

Following reflow, the pixel sensor and ROIC are mated via low pressure at room temperature. In an industry application, a second reflow is performed following the flip-chip procedure to achieve self-alignment with the surface tension of the molten indium, as well as high strength.

Factors that affect the quality and yield of the bumps include uneven UBM, the etching process, reflowing temperature profile, and cleaning after reflowing. Accurate alignment of the photoresists during the lithography process is critical to achieving good-quality bumps, but not as much as in the evaporation process. Current distribution and mass transport during the electroplating process are the main factors in electroplating that determine indium deposit growth and influence the bumps' shape evolution.

Experimental approach

In this work, we attempted to electroplate ultra-fine-pitch indium bumps (features with 10 μm size and pixel pitch of 5 μm and 7.5 μm) with a very uniform height. We used a 6-inch silicon wafer as the substrate with a copper seed layer and 17 μm of thick photoresist developed to form the required pattern. Strict control of photoresist thickness is required to assure good bump profile. We used a vacuum prewet process for bubble removal and prewetting

Factors that affect the quality and yield of the bumps include uneven UBM, the etching process, reflowing temperature profile, and cleaning after reflowing. Accurate alignment of the photoresists during the lithography process is critical to achieving good-quality bumps, but not as much as in the evaporation process

small patterns, and selected a pure indium plate for the anode, assuring 100% anode efficiency.

Indium bump electroplating was carried out through direct current (DC), pulse, and pulse reverse current waveforms. The average current densities of pulse and pulse reverse current were kept the same as the DC condition to enable direct comparison.

Role of the electrolyte

Various chemistries have been used for indium plating to date. Resist damage, due to hydrogen evolution, large grains and nodules, is the primary defect resulting from conventional indium plating electrolytes. MacDermid Alpha Electronics Solutions has developed an indium electrolyte to overcome these killer defects.

Novafab IN-100 is an acid electrolyte system created for low-temperature, lead-free solder interconnect. This proprietary electrolyte was formulated to deposit indium metal at high efficiency and, unlike conventional indium plating baths, does not produce hydrogen evolution due to its innovative chemical composition.

During electroplating, the pH at the metal-solution interface is kept stable, eliminating drastic pH increases that may result in photoresist lift and damage. Thus, Novafab IN-100 is suitable for

photoresist-patterned wafer plating because of its intrinsic photoresist compatibility. It produces a fine-grained, nodule-free matte deposit with >99.5% pure Indium and exhibits superior adhesion. The solution is fully analyzable and is compatible with both soluble and insoluble anode systems.

Conclusion

The height of the plated bumps was measured by using a confocal microscope, as shown in Figure 1. To remove the effect of the non-optimized reflowing process, height measurements were taken after electroplating and before the reflow process. Among the three waveforms we used, pulse plating with a high ratio of on-time to off-time yielded the best results. Measuring the height of the bumps, we were able to get uniformity of less than 10 percent across the wafer.

An indium oxide layer did form on the surface of the bumps in our demonstration process, so we weren't able to obtain a perfectly shaped sphere after reflowing, but it was observed that the bumps began to be rounded and form a sphere.

The properties of the indium electrolyte combined with the flip-chip process performed on ClassOne's Solstice single-wafer platform illustrated a viable approach to using indium for flip-chip electroplating processes.



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Imec produces the first fully self-aligned, two-metal-level, semi-damascene module

Semi-damascene integration is an attractive, cost-effective approach to extend interconnect process flows below 20nm metal pitch. Imec proposed its approach five years ago, and now confirms the first experimental demonstration of a functional, two-metal-level semi-damascene module at 18nm pitch.

BY GAYLE MURDOCH, TECHNICAL STAFF PRINCIPAL MEMBER AND ZSOLT TOKEI, IMEC FELLOW AND PROGRAM DIRECTOR FOR NANO-INTERCONNECTS

► Figure 1: Imec's semi-damascene flow: a) Ru etch (formation of the bottom local interconnect line (Mx)); b) gap fill; c) via etch; and d) via fill and top line (Mx+1) formation (as presented at VLSI 2022).

Semi-damascene integration & the BEOL roadmap

FOR MORE THAN 20 YEARS, copper (Cu) dual-damascene has been the workhorse process flow for building reliable interconnects. But when dimensional scaling continues and metal pitches become as tight as 20nm and below, the back-end-of-line (BEOL) increasingly suffers from RC delay, which is the result of a dramatically growing resistance-capacitance (RC) product. This has forced the interconnect community to start looking for alternative integration schemes and metals, with better figures of merit at tight metal pitches.

In this article, imec researchers Gayle Murdoch and Zsolt Tokei highlight the importance of via self-

alignment at tight pitch, explain and demonstrate the key technical parameters of the module including via and line resistance as well as reliability.

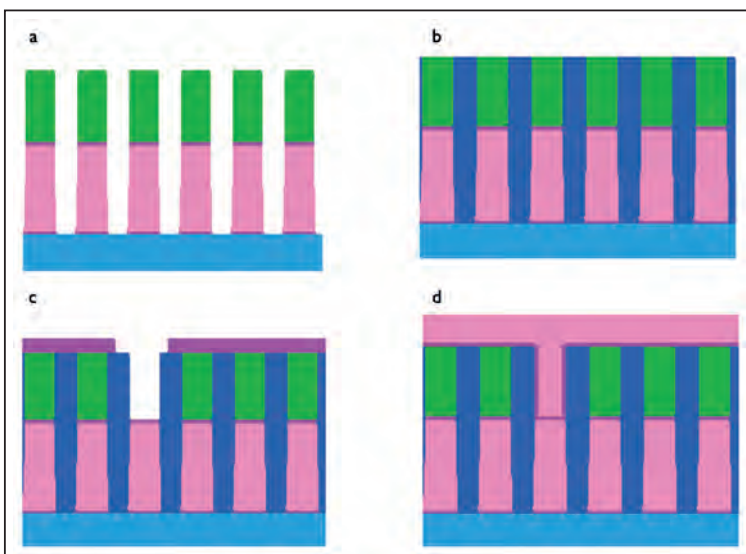
The results were presented at the 2022 IEEE VLSI Symposium on Technology and Circuits (VLSI 2022).

About five years ago, imec initially proposed semi-damascene as a viable alternative to Cu dual-damascene for integrating the most critical local (Mx) interconnect layers of the 1nm (and beyond) technology nodes.

Unlike dual-damascene, semi-damascene integration relies on the direct patterning of the interconnect metal for making the lines (referred to as subtractive metallization). No chemical mechanical polishing (CMP) of the metal is needed for completing the process flow.

The vias that connect subsequent interconnect layers are patterned in single-damascene fashion, then filled with metal and overfilled - meaning that the metal deposition continues until a layer of metal is formed over the dielectric. This layer of metal is then masked and etched to form the second interconnect layer with orthogonal lines.

After metal patterning, the gaps between the lines can be filled with a dielectric or can be used to form (partial) airgaps at the local layers. Note that in a semi-damascene flow, two layers (via and top metal) are formed in one-go, just like for conventional dual-damascene. This makes it effectively cost competitive, when benchmarked with dual-damascene (see figure 2).



Benefits of a semi-damascene integration flow

Semi-damascene promises several advantages over Cu dual-damascene at tight metal pitches according to Zsolt Tokei, imec fellow and program director for nano-interconnects. “Firstly, it allows for higher line aspect ratios while keeping capacitance under control – promising an overall RC benefit. Secondly, the absence of a metal CMP step leads to a more simplified and cost-effective integration scheme.

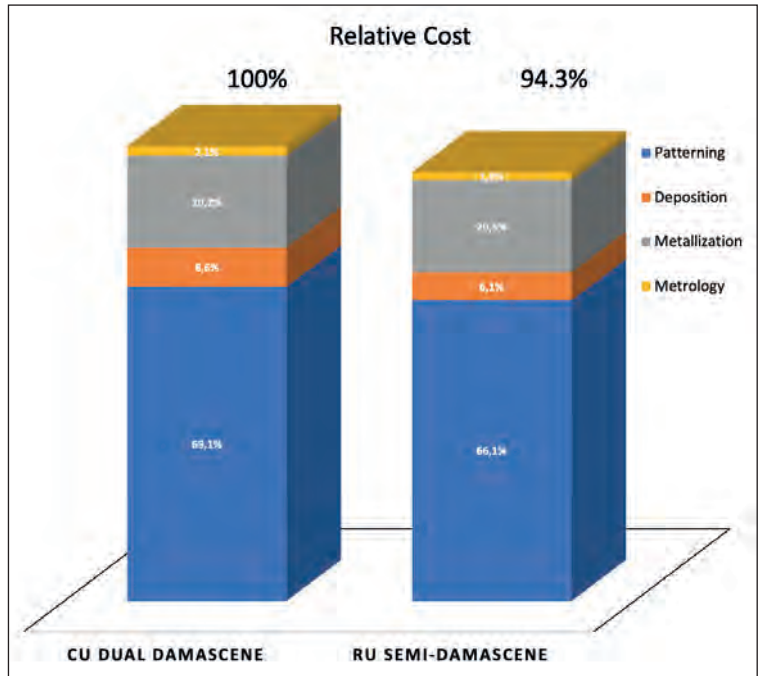
Finally, semi-damascene integration requires a barrierless, patternable metal such as tungsten (W), molybdenum (Mo) or ruthenium (Ru). By using metals that, unlike Cu, do not require a metal barrier, the precious conductive area can be fully utilized by the interconnect metal itself. This ensures competitive via resistance at scaled dimensions.”

Besides the benefits there are of course numerous challenges to tackle before such a scheme would get industrial acceptance. One step in that direction is the actual demonstration of a two-metal-level scheme. While the benefits have so far only been showed through simulation and modelling, imec has for the first time provided experimental evidence with a two-metal-level semi-damascene module.

The fully self-aligned via – a critical building block

At metal pitches as tight as 20nm, controlled via landing on top of the narrow lines is key to the successful operation of the semi-damascene integration module. When the via and the lines (at both via top and bottom) are not properly aligned, there is a risk of leakage between the via and an adjacent line. These leakage paths are the result of a too large overlay error induced by conventional patterning of the small via holes.

Gayle Murdoch, principle member of technical staff at imec said, “Finding a way for making functional, fully self-aligned vias has been a holy grail of the semi-damascene process. We achieved this



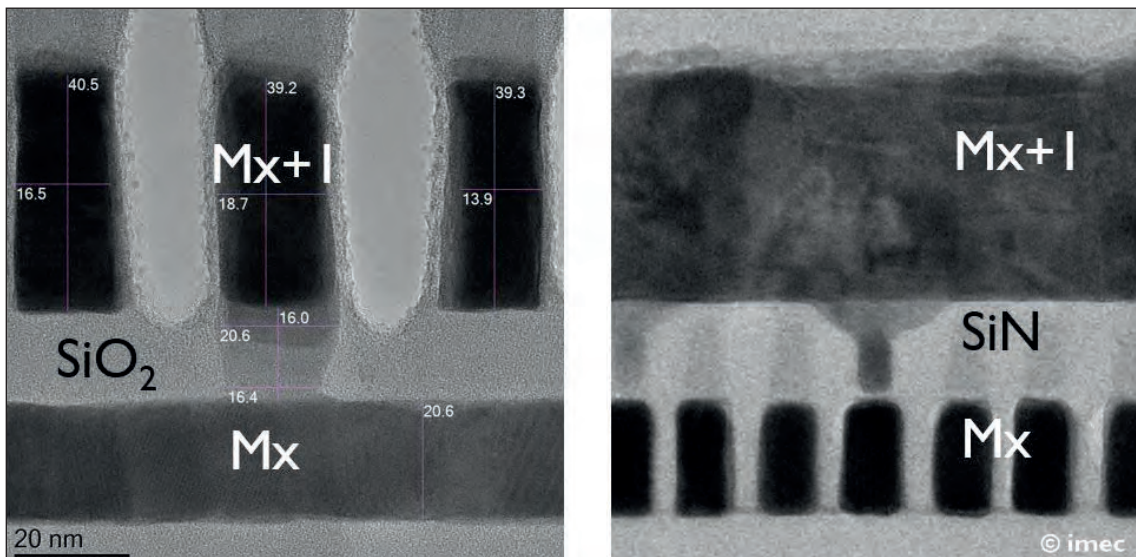
► Figure 2: Comparison of semi-damascene and dual-damascene cost at 18nm metal pitch.

milestone through intense collaboration between the integration, lithography, etch and cleaning groups at imec. With our fully-self aligned integration scheme, we were able to compensate for overlay errors up to 5nm – a key achievement.”

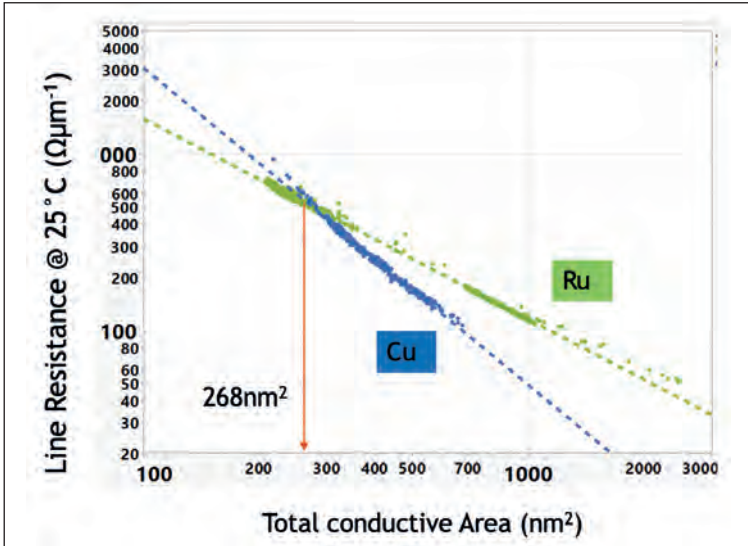
Bottom self-alignment was ensured by the selective removal of silicon nitride after gap fill, allowing the via to form on the confines of the lower metal line. The self-alignment towards the top metal layer (Ru) was achieved by the Ru over-etch step, applied after via overfill and Ru patterning.

New milestone: Good resistance and reliability at 18nm pitch

Using subtractive etch of Ru with fully self-aligned vias resulted in a functional two-metal level device



► Figure 3: Self-aligned via along Mx+I (left) and across Mx (right). The X-TEMs show self-aligned vias landing on 18 nm pitch Ru lines (as presented at VLSI 2022).



► Figure 4: Conductive area vs. line resistance for Ru and Cu lines (as presented at VLSI 2022).

at 18nm metal pitch. EUV lithography combined with self-aligned double patterning (SADP) was used for patterning the 9nm ‘wide’ Ru bottom local interconnect line (Mx), while single-exposure EUV lithography was used for printing the top line (Mx+1) and via. The top metal was combined with air gaps to counter the capacitance increase.

When benchmarking the line resistance vs. conducting area of Ru against Cu, Ru clearly outperforms Cu for the target metal pitches. Via self-alignment was confirmed both morphologically and electrically. Excellent via resistance was achieved (ranging between 40 and 60Ω for 26-18nm metal pitch), and a via-to-line breakdown field of >9MV/cm was demonstrated.

Zsolt Tokei remarked, “We have demonstrated excellent values for all the key technical parameters, including via and line resistance and reliability. This shows that semi-damascene is a worthy alternative to dual-damascene for integrating the first three local interconnect layers of the 1nm technology node and beyond. Our two-metal-level device with fully self-aligned via has proven to be a key building block.”

The researchers said that they believe further improvements are possible by increasing the aspect ratio of the lines (which reduces resistance) while keeping the air gaps (which keeps capacitance under control).

At the same time, imec has concrete ideas for implementing middle-of-line (MOL) and BEOL technology boosters using the semi-damascene technology (which allows further area reduction at standard cell level).



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New micro-textured film enables universal bare die carriers

Moving singulated die within production environments can pose many challenges. While safe transport solutions aplenty exist, all involve either tape and reel single use systems or they employ carriers that are customized for each die size, a different carrier for each and every form factor a fab produces. Delphon division Gel-Pak has a new solution that is set to change how manufacturers handle and test die in HVM settings.

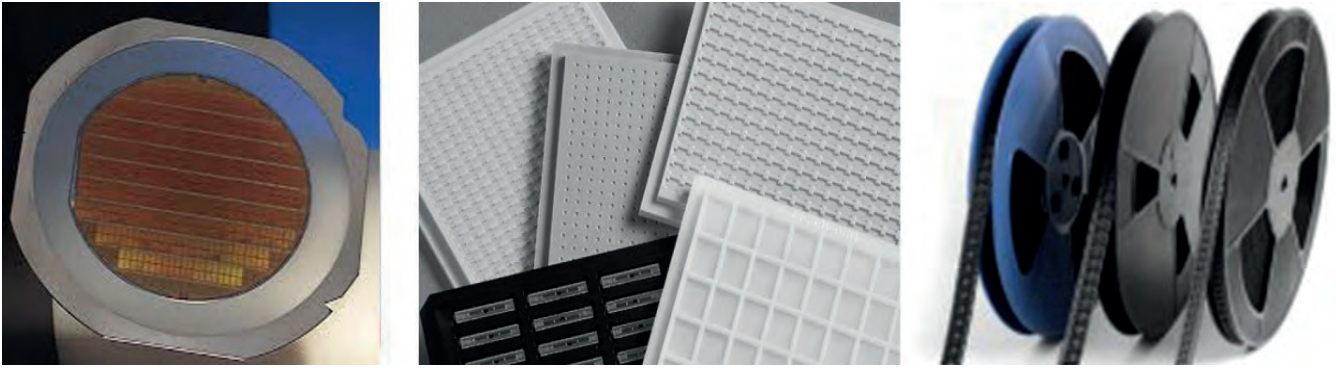
BY RAJ VARMA, CTO, DELPHON

THE EMERGING CHIPLET TREND, which calls for the disaggregation of large monolithic functionality into interconnected smaller dies, offers significant advantages over the alternative system on chip (SoC). The move toward this technology has accentuated the need for known good die (KGD) that have been fully tested prior to integration into their final packaging.

One challenge the industry faces in the test and assembly process is that conventional methods for handling chips can be problematic. A multitude of

device dimensions and the need to pick and repick components or move them between processes calls for a more simplified way of handling these chiplets.

There is a need in the industry for a universal carrier to sidestep the need for molded trays with custom-designed pockets or carrier tapes that are only suitable for one-time use. Gel-Pak fills this gap with its well-known Vacuum Release™ tray technology, and most recently with a newly developed micro-textured film that can readily grip bare die without the need for pockets.



➤ Figure 1: Dicing films, JEDEC trays, and tape and reel are the commonly used device-handling formats.

The material is inspired by the bio-based dry adhesion found in nature with geckos, lizards, beetles, spiders, and ants. This article discusses Gel-Pak’s process around developing the ideal textures, fabrication process, and geometric patterns for this novel material, as well as its efficacy as an integrated circuit (IC) carrier.

Chiplets, Known Good Die, and Singulated Die Testing (SDT)

The modern semiconductor industry has faced major hurdles with the plateau of Moore’s Law. It is no longer the case that transistor geometries decrease to allow for the transistor density to double every two years. This has made the goal of packing in more processing capability per unit area much more difficult to achieve – monolithic chips are growing in physical size with the attempt to fit more hardware blocks onto a piece of silicon.

There is, however, a limit to how much can be integrated into a single die. Chiplets involve the 2.5D and 3D stacking of interconnected smaller dies (chiplets) with a well-defined subset of functionality. Compared to the monolithic chip, the high amount of integration allows for more silicon with which to add transistors without taking up additional space.

There is one major factor to consider when assembling chiplets: the integrity of the chiplets themselves. One “bad” die would result in a malfunctioning 2.5D or 3D module, leading to a poor yield. This potential downside has accentuated the need for KGD, where individual dies are tested prior to installation into the larger design. The

employment of “good” die allows manufacturers to readily integrate these bare chips into the final package, dramatically improving the yield of these modules.

The test and assembly process for chiplet technology often requires banking and kitting of these components prior to final integration. Components are commonly moved within a facility for die level testing or processing. Changing device dimensions require component carriers that can adapt quickly to the rapid changes in form factor but still maintain the JEDEC standards to fit with existing equipment and pick-and-place (PnP) tools.

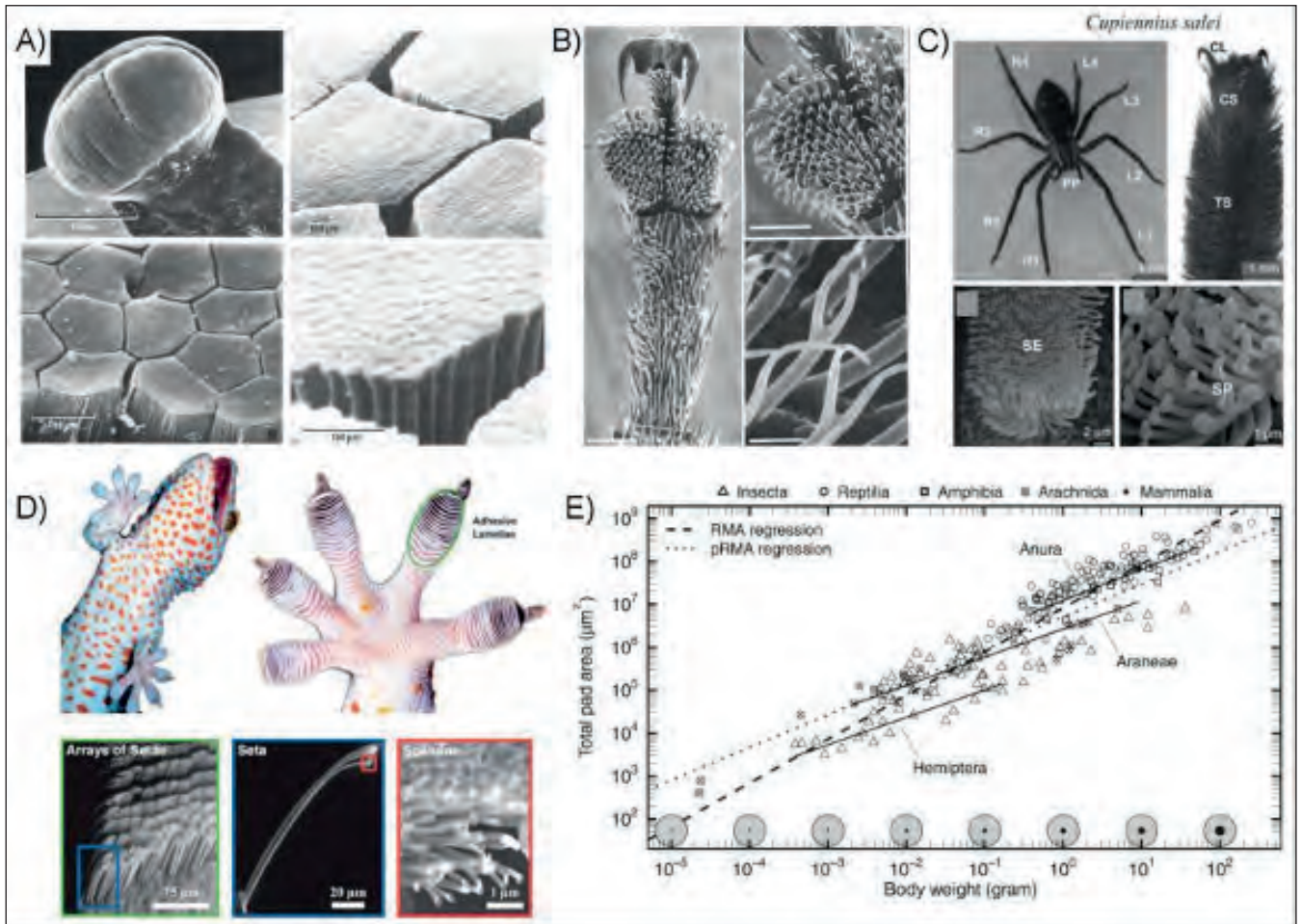
Wafer probe testing versus SDT

The conventional approach of testing individual die on a wafer is the wafer probe testing (WPT) method, or the wafer-level burn-in (WLBIn). In this method, a specialized wafer prober with thousands of probing needles makes contact with the micro bumps on the bare die. However, it’s not a full and accurate test, because the presence of the surrounding die reduces testing accuracy and militates against running certain tests, such as high-current tests. Although drain and gate leakage tests (such as IDSS and IGSS) may be performed at WPT, the measured leakage values will change after singulation. Furthermore, defects such as side-wall cracks can bring additional changes.

Singulated die testing (SDT) allows for much more accurate results, with the resulting test parameters lining up with the packaged part. With these tests there is a much more thorough assessment of the

Chip Carrier	Allows for Repick	Handles Different Chip Dimensions	Allows Access to IC Sides	Immobilizes Chip
Waffle pack	✓	×	×	×
Tape and reel	×	×	×	×
Sticky tape	×	✓	×	×

➤ Table 1



➤ Figure 2: Images of the adhesion system of various animal taxa. [Image Credit: [1]]

reliability of the bare die. This allows vendors to effectively bypass the potential hurdle of integrating “bad” die that do not match the parameters necessary to meet the performance requirements of the chiplet.

The challenges of handling bare die during SDT

Singulated die testing presents a significant challenge, as bare die can be brittle and susceptible to particle contamination, cracking, and breaking. Ideally, a bare die carrier would allow manufacturers to pick and repick chips, access its sides, handle chips of different sizes, and immobilize the chip (See Table 1).

Some common methods for handling bare die include:

- Waffle pack chip trays
- Tape and reel
- Sticky tapes (dicing tape)

Waffle pack chip trays are often used to ship and carry bare die in a series of parallel cavities or pockets that hold semiconductor chips. The width, length, and positioning of the pockets are custom-tailored for a specific IC dimension. However, waffle pack trays cannot be reused in the event that there is a redesign or the vendor desires to ship another batch of ICs in which the chip dimensions have

changed. These trays also do not allow for access to the edges of the chip, which is critical for devices with large stay-out zones. Additionally, these trays are not well-suited for the handling of thin die. There is always the potential for chips flipping in their pocket and die migration if the pockets themselves exhibit poor flatness tolerances.

Tape and reel packaging faces similar challenges; the requirement for customized pocket dimensions will not suffice for ICs that change form factor in a new design iteration. Because the pockets are sealed with a cover tape, which can only be removed once, the tape and reel packaging does not lend itself to the repick required for SDT.

Sticky tapes do not share the burden of customizing pocket dimensions to hold a particular IC as do both waffle packs and tape and reel packages. These tapes also allow access to the sides of the chip and immobilize the chip to prevent die migration. However, once a device is picked, it can never be put back to be reused, thus mitigating its utility for SDT.

Reversible adhesion in nature

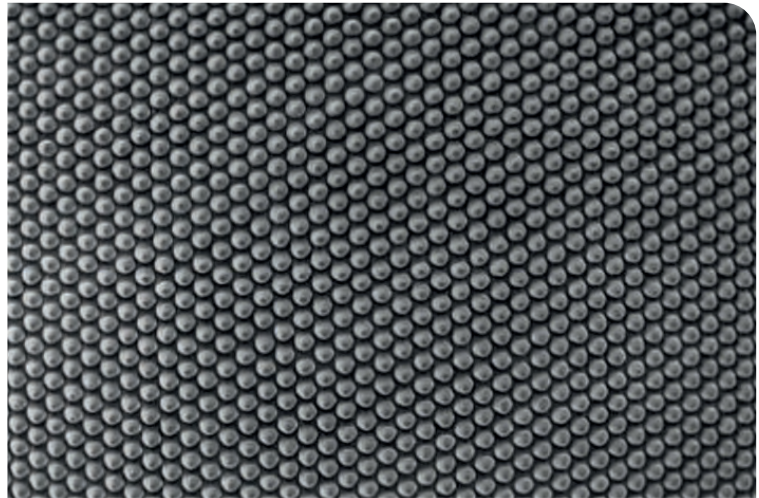
Gel-Pak noted this need for a universal chip carrier that does not require custom compartments to hold the IC in place, allows for repicking, enables access to the edges of the chip, and immobilizes the chip itself. The inspiration for this reversible adhesion

came from the dry adhesive characteristic found in nature. The ability of certain lizards, insects, and frogs to climb up walls and easily detach themselves is enabled by the micro-texturing of their toe pads. The toe pads consist of fibrillar micro- and nanostructures that conform to surface irregularities; the adhesion comes from the viscoelastic response of their outer membrane. As shown in Figure 2, each species exhibits a unique texture in which individual micro- and nanoscale fibers are adequately long and flexible to reach into the microscopic valleys of the surface they attach themselves to. In other words, these toe pads feature a dense array of microscopic contact points that demonstrate surface forces and kinetics to produce strong, controllable, and reliable adhesive contact. This interplay of surface texture and viscoelastic response of tissue materials is referred to as dry adhesive.

Developing the Novel Micro-textured Material
 In the field of pressure-sensitive adhesives, micro-texturing has led to dry adhesion that enables a strong bond with a simple and clean release. Gel-Pak utilized the same textured adhesive concept in developing carrier tray technology by carefully researching other successful adhesive developments. One main parameter to observe in this process is the pull-off force, or the amount of force required to pull the adhesive off of the surface. This inevitably varies with preload, the compressive force placed upon the adhesive prior to pull-off. It has been shown that the pull-off force generally increases with preload, regardless of which geometric pattern the tip of the fibrils takes on (e.g., spherical, flat with rounded edge, mushroom, spatula, concave, square, dimples) [2] [3].

Moreover, a larger fibril will require more preload strength to obtain adhesion — and, as a result, more pull-off force to remove the material from the surface. In other words, the more force placed upon the viscoelastic membrane, the stronger the adhesion; and the thicker the fibrils, the more force required to attach and detach the material. This is relevant to better understand whether or not a PnP machine can gently lift the bare die from the carrier tray.

Gel-Pak focused on textures that were compatible with high-volume manufacturing (HVM). In HVM, conventional plastic fabrication processes such as injection molding and extrusion are used. Typically in plastics fabrication processes, texturization is primarily used for ergonomic considerations. However, this application necessitated the engineering of tack, or adhesion. Furthermore, the injection molding of textured adhesives is not generally practiced in the industry. During the process of developing this micro-textured material, Gel-Pak innovated an injection-molding textured adhesive that allows for HVM. There is no precedent for this in the plastics manufacturing industry, and the application itself is unique. As a result, ASTM and other test standards don't have any tack

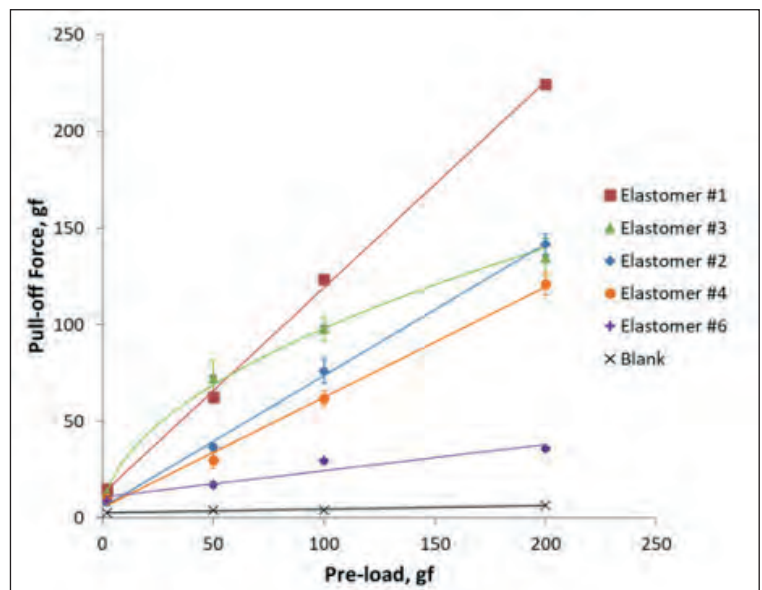


metrology for textured surfaces. With the goal to use materials best suited for such processes, Gel-Pak tried six different texture geometries and more than two dozen different adhesive formulations. Eventually, this process was narrowed down to the staggered dimple (Figure 3).

➤ Figure 3: Staggered dimple tip geometry used for the Gel-Pak's novel universal carrier.

Testing the IC tray technology

After the process of selecting the texture geometry, various elastomers were used to generate a wide range of preload force curves (Figure 4). In this research initiative, the micro-texture features were not as small as in some of the previously published works; however, a wide preload force spectrum was enveloped by leveraging different adhesive chemistries. The prototype leveraged a custom-made flat JEDEC tray with the micro-textured film laminated to the surface (Figure 5). While JEDEC trays are really leveraged for packaged components, using the JEDEC form factor allowed for tests with common PnP machines, making this a more practical solution for SDT.



➤ Figure 4: Pre-load versus pull-off force for six different elastomer chemistries.

➤ Figure 5: Image of the micro-textured film laminated to the flat JEDEC tray to allow for the adhesion and immobilization of bare die of different sizes.

Each adhesive option was screened based on the following:

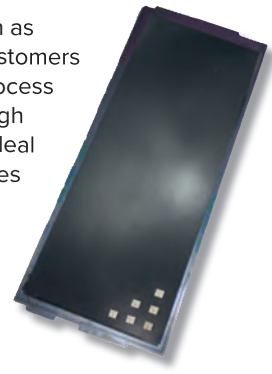
- Surviving shock/vibration/drop at -10°C, 20°C, and 50°C
- Long-term tack growth
- IC backside residue
- PnP and surface mount technology (SMT) pickability

After this testing, three different tack levels were finalized:

- Low tack
- Medium tack
- High tack

The low-tack material corresponds to elastomer 6 in Figure 4. This grade of adhesion is ideal for

in-process device handling, such as testing. The medium tack, or elastomers 2, 3, and 4, is preferred for in-process handling as well as shipment. High tack, or elastomer 5, would be ideal for more robust packaged devices such as quad-flat no-lead (QFN) packages. Finally, we tested the resulting three micro-textured materials on several different PnP machines, including the Royce, Besi, Muhlbauer, and MRSI, as well as the Juki Surface Mount Technology System. With only a few modifications to the equipment parameters, all the machines were able to successfully pick up the sample IC devices from the modified trays at moderate unit per hour (UPH) rates. The modifications allowed just enough z-axis down force to seal the vacuum cup with the device surface, pull the vacuum to an optimum threshold, and initiate the pick.



FURTHER READING

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- 2. Campo A, Geiner C, Arzt E. Contact Shape Controls Adhesion of Bioinspired Fibrillar Surfaces. *Langmuir* 2007;23:10235–10243.
- 3. He B, Chen W, Wang J. Surface Texture Effect on Friction of a Microtextured Poly(dimethylsiloxane) (PDMS). *Tribol Lett* 2008;31:187–197.

Conclusion

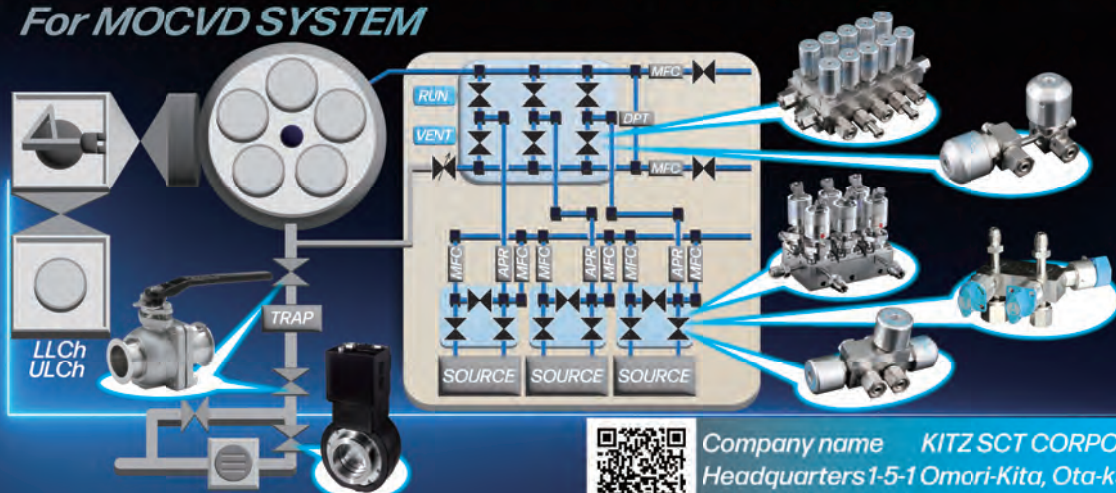
Gel-Pak’s textured universal chip carrier is built upon innovation in both material science and manufacturing technology. We explored both the bump geometry and elastomer materials to ensure that components strongly adhere to the material’s surface with minimal effort and can be easily removed via PnP and SMT machines. The carrier is best suited for singulated die tests for KGD.

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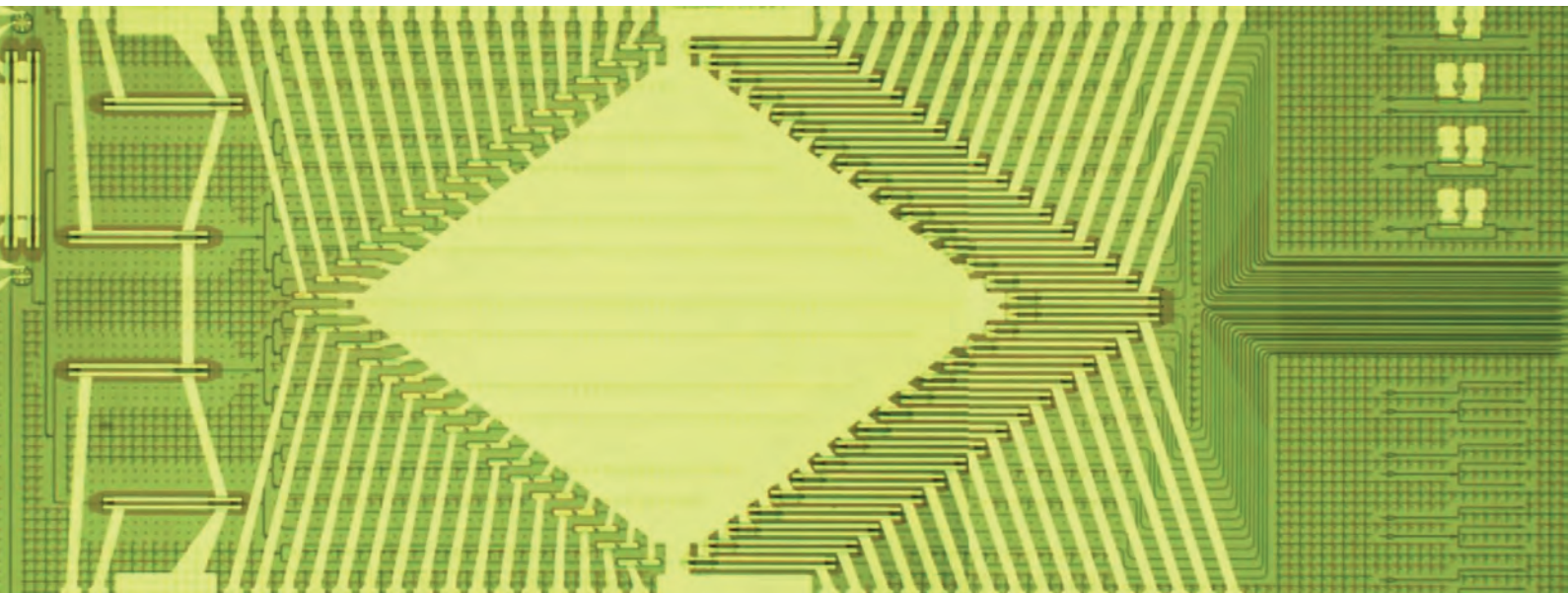
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Samsung progresses developing silicon photonics for LiDAR

Microelectronics has revolutionized almost every aspect of life. Efforts to incorporate Silicon photonic integrated circuits (PICs) into advanced CMOS ICs often center on requirements that II-VI or III-V technologies cannot solely address. Computing, automotive, wellness and myriad other applications will or are already benefitting from integrated photonic devices that leverage various silicon or hybrid technologies. LiDAR is at an inflection point where further advances to reduce size and increase performance will hinge on new approaches like those envisioned by researchers at Samsung's Advanced Institute of Technology who report on SiP advances on the road to better LiDAR PICs.

BY DONGJAE SHIN, KYOUNGHO HA, AND HYUCK CHOO, [SAMSUNG ADVANCED INSTITUTE OF TECHNOLOGY](#)

MODERN ELECTRONICS and photonics began around the middle of the 20th century with the inventions of the transistor and laser, respectively. Thanks to the continued evolution of complementary-metal-oxide-semiconductor (CMOS) technology that revolutionized transistors, microelectronics has for decades been a foundation for creating today's communications and computing systems and countless other innovations [1].

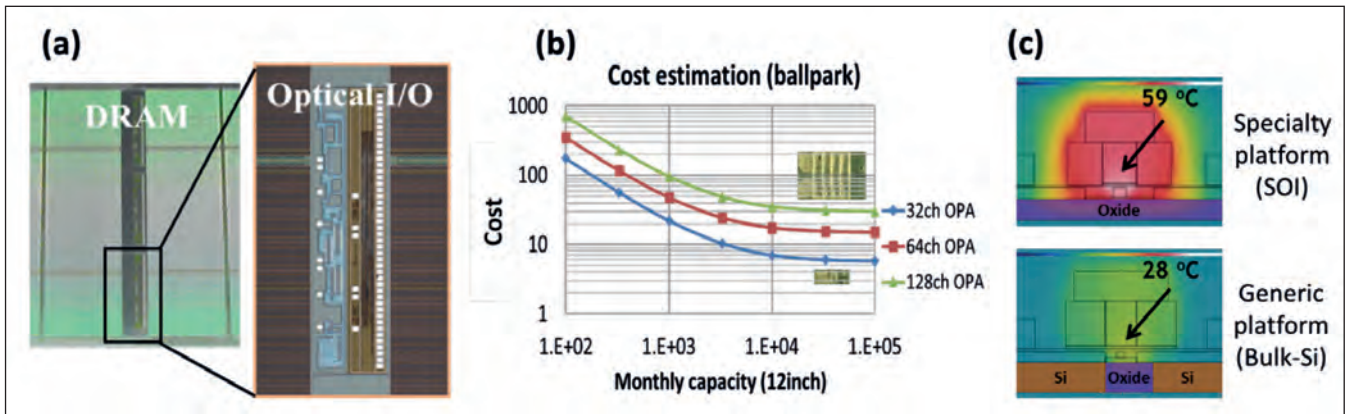
On the other hand, photonics is evolving at a relatively slower pace and is still confined, compared to microelectronics, to diverse but relatively smaller niche fields. Silicon Photonics (SiP) was born under this circumstance. Interest continues to grow as to whether Silicon Photonics can reduce the gap between the two technologies and achieve

the commoditization of photonic devices by grafting the productivity of CMOS to photonics [2].

As the CMOS industry has given more technical attention to SiP, it is important to find 'killer applications' that can bridge the gap between technologies that can become profitable business opportunities since without a profit potential any technology will not see rapid development. This article introduces recent research by the Samsung Advanced Institute of Technology (SAIT) in support of photonic integrated circuits designed for light detection and ranging (LiDAR) sensors.

Why LiDAR?

In order to explain why LiDAR presents one of the best opportunities for photonic integration among



numerous applications, a glimpse into the product development history at Samsung is helpful. One of the most representative missions of SiP has been to resolve the DRAM-CPU interconnect bottleneck, the well-known Achilles heel of classical von Neumann computing architectures. Attempts were actively made by Samsung around 2010. Considering the cost limit of DRAM, photonic interconnect feasibility between DRAM and CPU was demonstrated by directly integrating a PIC into a DRAM chip as shown in Fig. 1(a) [3][4]. Despite such a significant achievement, these attempts also revealed the huge difference in technological maturity between CMOS and photonics, and did not lead to subsequent full-scale development. One of the lessons learned from this experience was that it is very difficult to apply emerging PIC technology directly to legacy applications that have matured for a long time. Samsung therefore believes that PIC technology is most suitable for emerging applications in many instances.

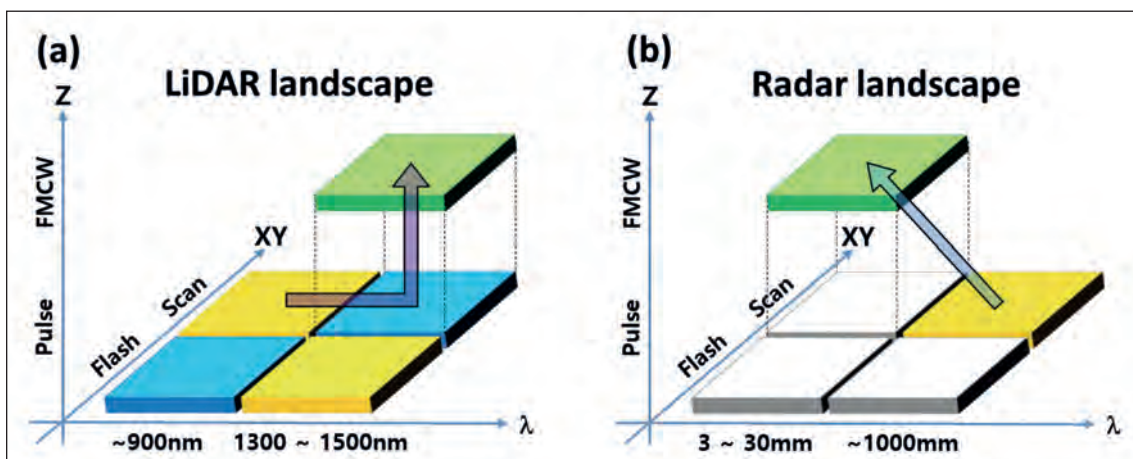
Among numerous emerging applications considered, LiDAR was chosen for three main reasons. The first reason is its possibility of high volume. Since LiDAR is (or will be) in high demand from various applications such as autonomous vehicles, robots, and smart devices, it is likely to achieve the high volume that can justify CMOS scale production. The second reason is its good

timing from the perspective of CMOS evolution as characterized by Moore's Law and its relentless march towards smaller, faster devices that use less power and cost less to fabricate. Wide deployment of LiDAR has been delayed due to its high cost, so the virtuous cycle of volume and cost reduction from CMOS-like production processes has been an urgent goal for LiDAR development as shown in Fig. 1(b). The third reason is LiDAR's good match-up with Samsung's PIC platform. While most of the Silicon Photonics industry has been developing PICs on various specialty substrate-based platforms such as SOI, Samsung has developed PICs on a generic substrate-based platform for legacy applications as shown in Fig. 1(c) [5]. Thanks to ~100X higher thermal conductivity of silicon compared to oxide, Samsung's platform provides better heat dissipation, making it well-suited for heat-sensitive laser or amplifier arrays needed for LiDAR applications. This generic platform, however, is on hold for now, and the specialty platform is used for research purposes.

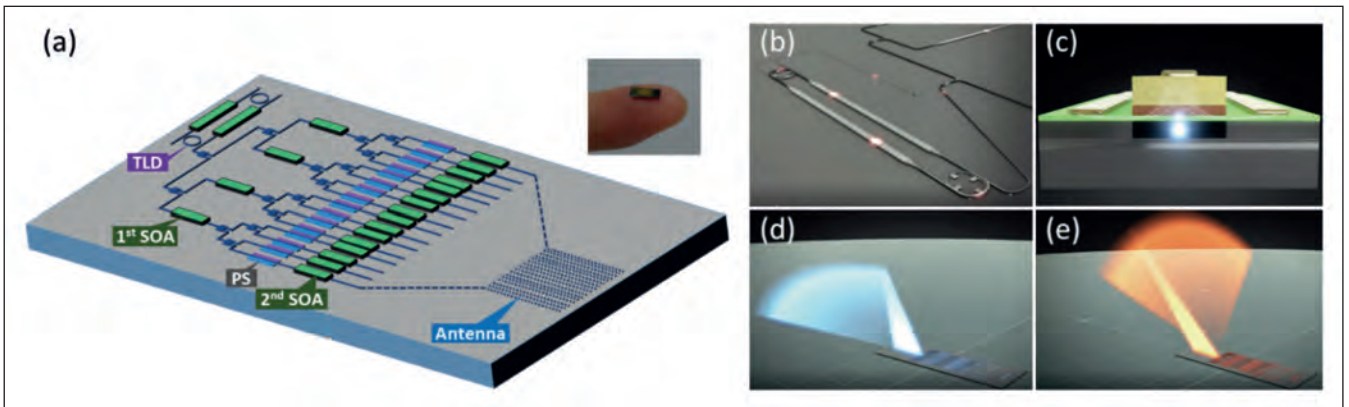
➤ Figure 1. (a) PIC embedded in 65nm DRAM. (b) Estimated volume-cost curve for LiDAR. (c) Thermal advantage of generic platform.

Technologies best suited for LiDAR

In LiDAR, various technology schemes are competing in terms of performance and cost, and the market winner is still uncertain at this point, especially for low-end applications. The rough consensus about LiDAR architectures is that solid-state solutions are most likely to win rather than mechanical systems with moving parts. Integration



➤ Figure 2. Technology landscapes of LiDAR(a) and RADAR(b).



➤ Figure 3. (a) LiDAR chip integrating TLD, SOA, PS, and antenna array. (b) TLD planar structure. (c) SOA vertical structure. (d) Horizontal beam scan in lower elevation angle with short wavelength. (e) Horizontal beam scan in higher elevation angle with long wavelength.

rather than assembly of disparate technologies will have an advantage in competition; comparative discussions are actively underway from various viewpoints.

The road to an optimized LiDAR solution typically considers three most important viewpoints: planar (XY) illumination, axial (Z) ranging, and wavelength as shown in the Fig. 2. Illumination typically employs the flash scheme, with simultaneous illumination of the entire field of view (FOV) while the scanning scheme employs sequential illumination in each direction comprising the FOV. The flash scheme has already been commercialized for short-range applications by utilizing the existing CMOS ecosystem, and the scanning scheme has been proven for a long time in long-range radio detection and ranging (RADAR) applications.

Ranging could involve various approaches such as the time of flight (TOF) scheme that transmits short light pulses while the frequency modulated continuous wave (FMCW) scheme transmits frequency modulated light. Considering that RADAR evolved from TOF to FMCW, it is believed that a

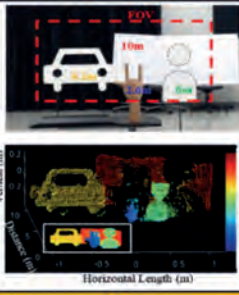
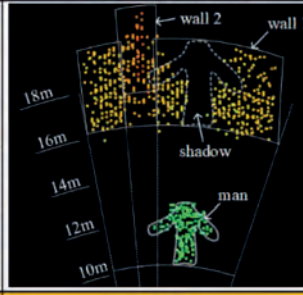
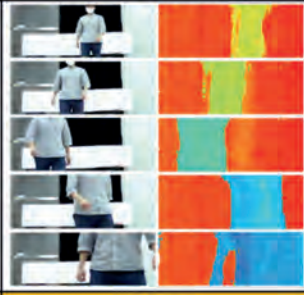

similar evolution is likely to occur in LiDAR. In wavelength, there is the silicon-compatible ~900nm band and the III/V-based 1.3~1.5um band. The ~900nm band is advantageous from the perspective of the existing industry ecosystem, but the 1.3~1.5um band is advantageous from the perspective of eye safety and resistance to ambient light noise. SAIT has been adopting the scanning scheme and the 1.3um band with more focus on long-range applications; it is preparing to evolve from TOF to FMCW.

PICs for LiDAR

As is appreciated in many photonics applications, to maximize the volume-cost virtuous cycle, it is necessary to integrate all photonic devices on a single chip. Until now, photonic devices for a LiDAR transmitter (Tx) have been integrated into a single chip first, with receiver (Rx) photonic devices integrated after clearing architectural uncertainties. The LiDAR Tx is an optical phased array (OPA) that corresponds to a photonic version of the RF phased antenna array used for RADAR. Figure 3 conceptually illustrates the OPA chip and main photonic devices such as tunable laser diode (TLD),

➤ Figure 4. LiDAR device integration progress.

	PoC1[CLEO2021]	PoC2[CLEO2020]	PoC3[IEDM2020]	PoC4[IEDM2021]	PoC5
Chip					
Platform	Si	III/V on Si	III/V on Si	III/V on Si	III/V on Si
Ch#/size	128ch, 5.7 x 5mm	32ch, 7.5 x 3mm	32ch, 7.5 x 3mm	32ch, 8.7 x 3mm	TBA
OPA	Integrated	Integrated	Integrated	Integrated	Integrated
SOA	Assembly	Integrated	Integrated	Integrated	Integrated
TLD	Assembly	Assembly	Integrated	Integrated	Integrated
PD	Assembly	Assembly	Assembly	Assembly	Integrated

	PoC1[CLEO2021]	PoC2[CLEO2020]	PoC3[IEDM2020]	PoC4[IEDM2021]
Real-time 3D data				
Range	~10m	~20m	~10m	~20m
FOV	50 x 7°	12 x 3.2°	15 x 3.5°	20 x 3.5°
Res.(H x V)	100 x 36	40 x 21	120 x 20	120 x 20
Frame rate	slow	2 fps	20 fps	20 fps

semiconductor optical amplifier (SOA), phase shifter (PS), and antenna array. The OPA amplifies the 32-way split outputs of the TLD by a total of 36 SOAs and controls the phases with 32 phase shifters, thereby reducing the diffusion angle of the optical beam from the antenna array. The optical beam is then scanned by the phase shifters in the horizontal direction and by the TLD in the vertical direction as shown in Fig. 3(d) and (e). The TLD controls the lasing wavelength by the heaters in the two ring resonators shown in Fig. 3(b).

When fabricating the OPA, silicon processes were followed by III-V on silicon bonding and III-V processes. This III-V on silicon heterogeneous integration is advantageous for low-cost manufacturing since it simplifies subsequent packaging. The III-V material used for this work is combination of four elements in the group III and V of the periodic table such as Aluminum, Gallium, Indium, and Arsenic, grown on InP substrates.

LiDAR developmental status

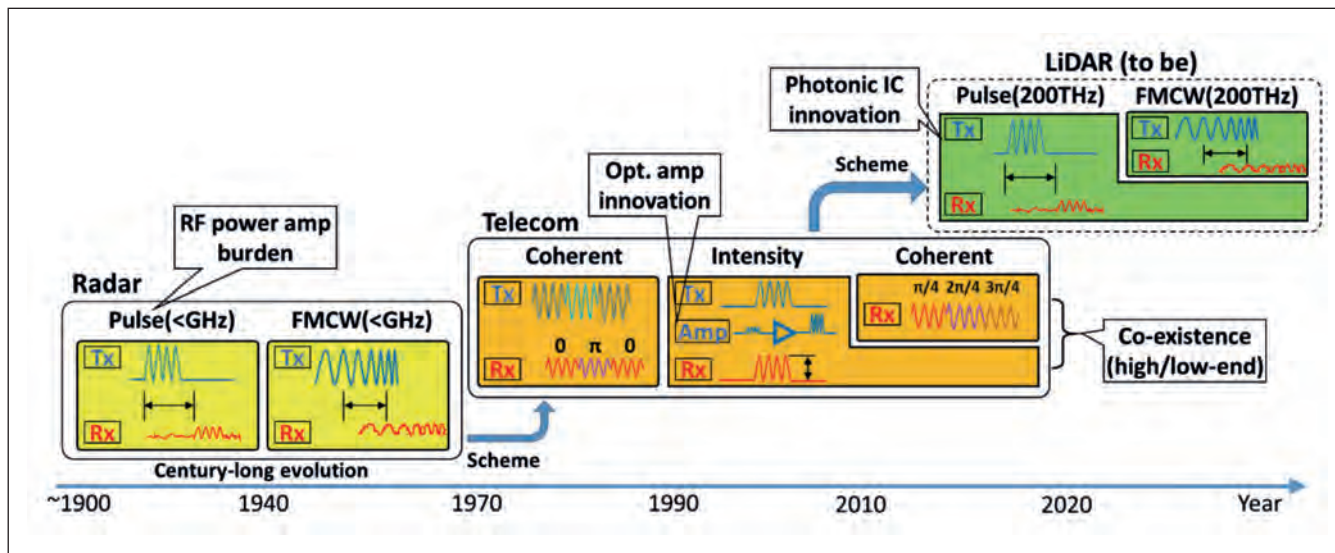
In moving toward single-chip integration, the progress of device integration so far is summarized in Fig. 4. From the PoC1 in which only the phase shifter and antenna array were integrated with a silicon-only process, to the PoC2 with additional integration of the SOA, to the PoC3 and the PoC4 groups with additional integration of TLD. These were fabricated through III-V on silicon process [6] [7]. From the PoC3 to the PoC4, the circuit layout was improved to reduce on-chip losses and thermal effects [8][9]. The PoC5 with integrated photodiodes (PDs) is also under consideration, but its integration is still ongoing due to delays related to some LiDAR architectural issues. In the PoC1, using a relatively simple silicon-only processes, an OPA with 128 antennas was fabricated, and from the PoC2 with higher III-V on silicon process challenges, OPAs with 32 antennas were fabricated due to lower device yields. The optimal antenna count is determined as part of a performance-cost trade-off, and is expected to vary according to the detection

distance required for various applications.

The success of various technology combinations designed to achieve optimal LiDAR performance is summarized in Figure 5. While the PoC1 group had decent resolution with 128 antennas, a very slow frame rate was unavoidable due to low OPA output power and slow external TLD. In the PoC2 testing, because the OPA output power was improved through the SOA integration, video recording at 2 frames per second became possible, but the resolution was lowered due to the decrease in the antenna count. In the PoC3 tests, a 20 frames per second video recording was achieved thanks to the additional integration of TLD, and the resolution was also improved by digital signal processing (DSP) and image signal processing (ISP). In the PoC4 tests, the detection range and FOV were

➤ Figure 5. LiDAR performance progress.

When fabricating the OPA, silicon processes were followed by III-V on silicon bonding and III-V processes. This III-V on silicon heterogeneous integration is advantageous for low-cost manufacturing since it simplifies subsequent packaging. The III-V material used for this work is combination of four elements in the group III and V of the periodic table such as Aluminum, Gallium, Indium, and Arsenic, grown on InP substrates.



> Figure 6. Insights from RADAR and Telecom evolution.

improved as the output power increased by the optical and thermal improvement of the OPA. Efforts to optimize performance are currently underway to reach the performance levels demanded by the market. In particular, improving the FOV is the most urgent issue as indicated in Fig. 5.

Since the FOV and range are interrelated, improvements to the FOV should be accompanied by improved range. While a TOF approach is likely to be sufficient for short-range applications, long-range utility is likely to necessitate using a FMCW approach. Therefore, it is believed that the lower cost of the relatively complex FMCW and the higher performance of the relatively simple TOF would be important to the initial segmentation of the LiDAR market.

Future outlooks

In order to anticipate the future technology evolution of LiDAR, it is necessary to look into relevant prior technologies such as those pivotal to the development of RADAR and telecommunications applications. Radar has almost the same purpose as LiDAR, and has undergone technological evolution over 100 years. Telecommunications also uses optical devices and module technology that are common to LiDAR, and has undergone evolution over 50 years. Fig. 6 concisely summarizes the major evolutionary paths of RADAR and Telecom. RADAR started in the early 20th century using a TOF approach, and has evolved into utilizing a FMCW scheme because of the challenges of high-power RF amplifiers. FMCW RADAR influenced the development of telecommunications technologies in the 1970s; interest in a FMCW-like coherent scheme was high.

However, due to the emergence of optoelectronic based systems and well-known optical fiber amplifiers, the telecommunications market has been dominated by TOF-like intensity schemes since the 1990s. Beginning in the 2010s when more performance improvement was needed, a coherent scheme was revisited for telecom/ datacom applications, and now it coexists with the intensity scheme. One important implication of this evolutionary history is that the amplifier technology has had a significant impact on the evolutionary direction of these devices and timing for development leading to market introduction, which is likely to repeat in the evolution of LiDAR technologies. That is, the timing of the TOF-FMCW transition might be determined according to the degree of success of the SOA-based distributed optical amplification technology as described in this article.

Attention is focused on how this technological uncertainty will affect the commercialization of LiDAR technology in the coming years.

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