SILICON SEMICONDUCTOR

VOLUME 46 ISSUE X 2025

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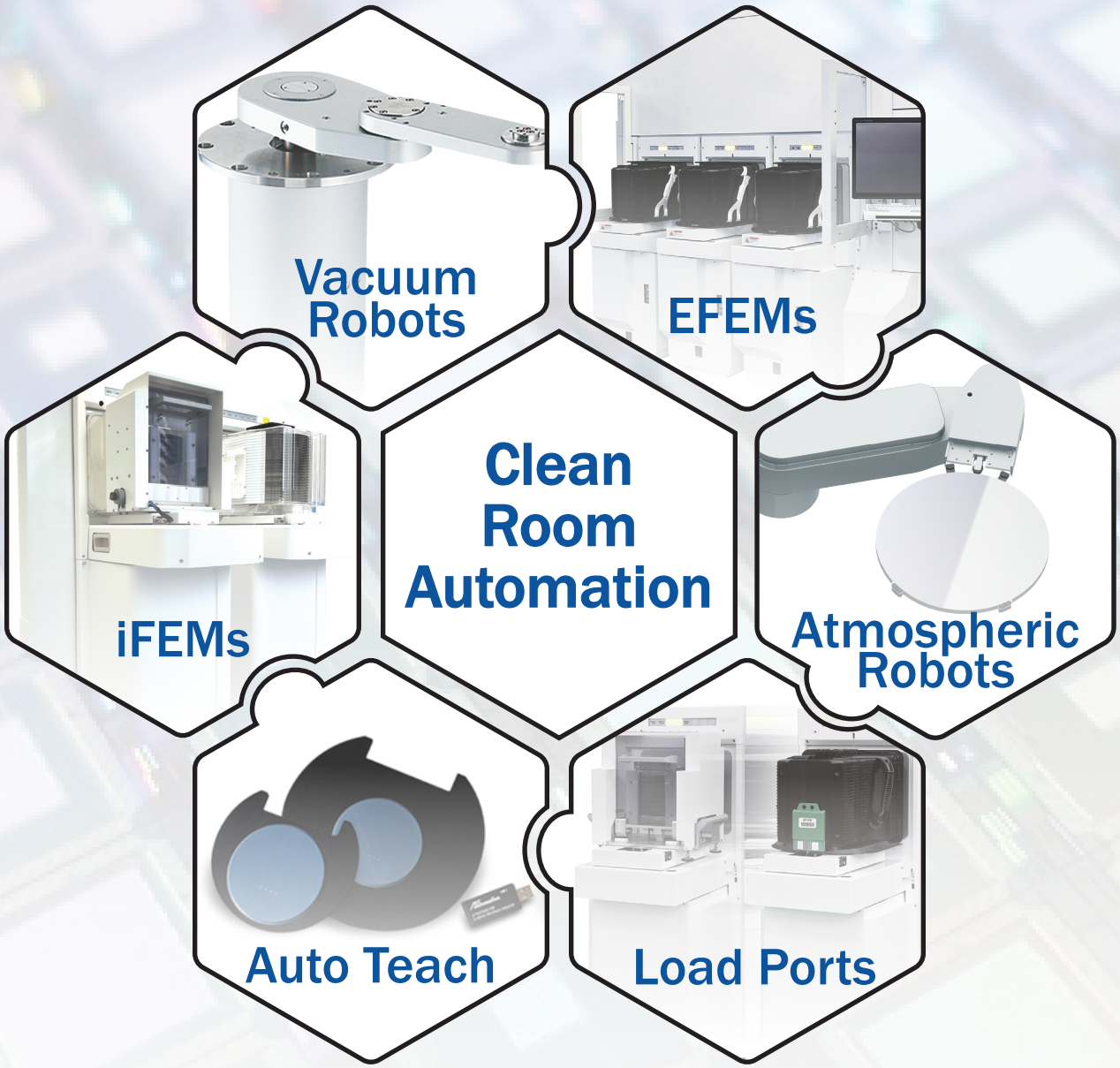

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VIEWPOINT

BY PHIL ALSOP
EDITOR

Looking ahead to 2026:

scale, skills and the shape of silicon

AS the semiconductor industry looks toward 2026, the message from the data seems unambiguous: scale is back, complexity is accelerating, and the industry's future will be shaped as much by people and policy as by process technology. SEMI's latest forecasts, projecting equipment sales of $145 billion in 2026 on the way to a record $156 billion in 2027, confirm that this cycle is structurally different from those of the past. AI is not merely another demand driver; it is redefining how and where the industry invests.

In 2026, AI-driven capital expenditure will dominate the agenda. Leading-edge logic at 2nm, aggressive HBM ramps, and sustained DRAM and NAND upgrades will keep wafer fab equipment on a strong growth trajectory. Yet the real inflection point lies beyond the front end. Advanced packaging — from chip-to-substrate thermo-compression bonding to fan-out and panel-level processing — is rapidly becoming the industry's critical enabler. Recent wins by ASMPT and ACM Research underscore a broader truth: heterogeneous integration is no longer optional. It is the only viable path to scaling performance, yield and cost in an AI-centric world.

At the same time, back-end test and inspection are emerging as strategic bottlenecks. As devices grow larger, denser and more complex, the ability to validate performance, reliability and thermal behaviour at speed will be a defining competitive advantage in 2026. Software, AI-enabled automation and advanced metrology — exemplified by innovations in 3D image analysis and fab automation — will increasingly differentiate suppliers and manufacturers alike.

Another defining theme for 2026 is energy. AI's explosive compute demand is colliding with physical and environmental limits, pushing power efficiency to the forefront of system and chip design. Silicon photonics is rapidly moving from promise to necessity. GlobalFoundries' expansion in photonics manufacturing and Europe's growing policy focus reflect a broader industry realisation: electrons alone cannot sustain AI's trajectory. Expect 2026 to be the year when photonics transitions decisively from infrastructure to integration, reshaping data centres, packaging architectures and foundry roadmaps.

Geopolitics and regionalisation will continue to influence investment patterns. China, Taiwan and Korea will remain the top equipment destinations, but Europe's role is evolving. The European Chips Act, its forthcoming 2.0 iteration, and initiatives such as Finland's 200 mm R&D upgrades signal a more determined push toward sovereignty — not just in fabs, but across materials, equipment, design and packaging. However, capital alone will not be enough.

Perhaps the most underestimated challenge heading into 2026 is talent. Europe's looming shortfall of skilled semiconductor workers highlights a global issue: advanced fabs, photonics lines and AI-driven manufacturing systems cannot run without a new generation of cross-disciplinary engineers. Skills in system design, AI-enabled hardware, cybersecurity and manufacturing automation will be as critical as lithography expertise.

Looking ahead, 2026 will not simply be about building more tools or fabs. It will be about building an ecosystem capable of sustaining unprecedented complexity — technologically, energetically and humanly.

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Preventing liquid cross-contamination in semiconductor manufacturing

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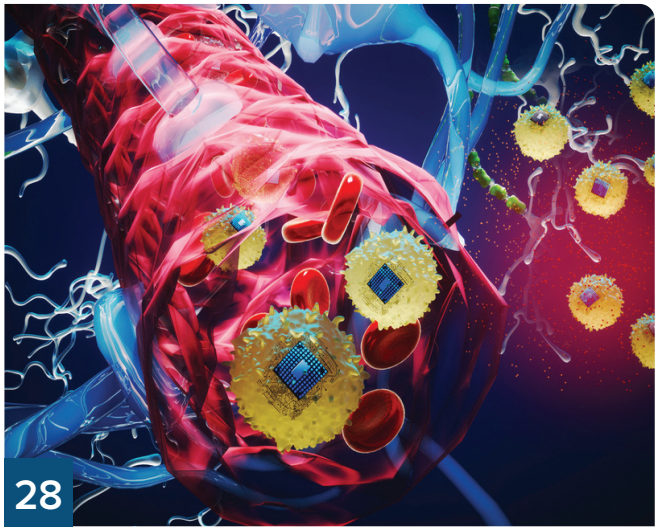

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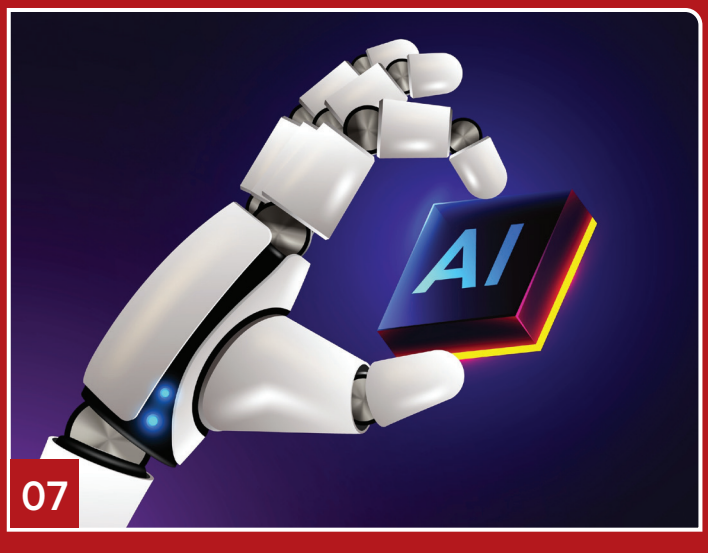

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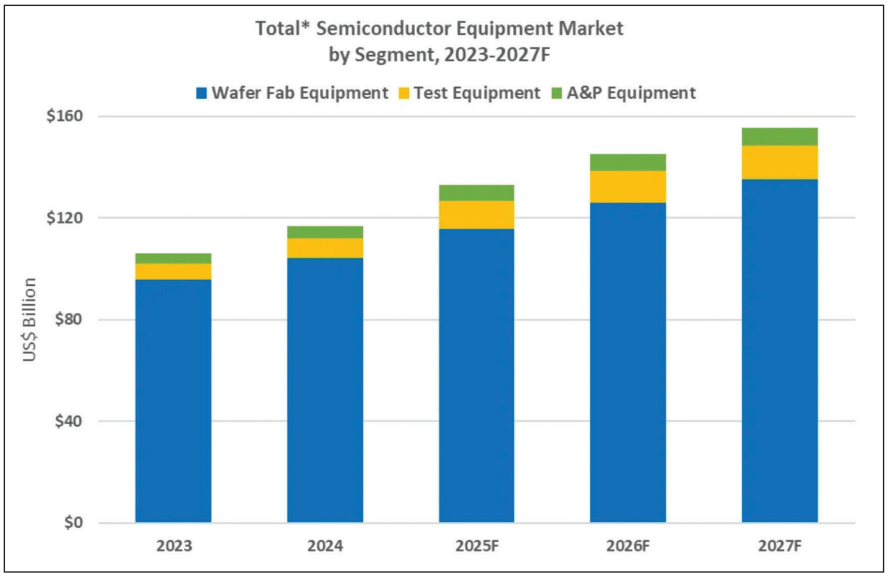
Global semiconductor equipment sales to reach $156 billion in 2027

Global sales of total semiconductor manufacturing equipment by original equipment manufacturers (OEMs) are forecast to reach a record high of $133 billion in 2025, growing 13.7% year-on-year, SEMI announced its Year-End Total Semiconductor Equipment Forecast.

GROWTH in semiconductor manufacturing equipment sales is expected to continue in the two following years of the forecast period, with projections of $145 billion in 2026 and $156 billion in 2027. This growth will be driven primarily by investments related to AI, particularly in leading-edge logic, memory, and the adoption of advanced packaging technologies. "Global semiconductor equipment sales show robust momentum, with both the front-end and back-end segments projected to see three consecutive years of growth, culminating in total sales surpassing $150 billion for the first time in 2027," said Ajit Manocha, SEMI president and CEO. "Investments to support AI demand have been stronger than anticipated since our midyear forecast, leading us to boost the outlook for all segments."



Semiconductor equipment sales by segment

After registering a record $104 billion in sales last year, the wafer fab equipment (WFE) segment, which includes wafer processing, mask/reticle, and fab facilities equipment, is projected to grow 11.0% to $115.7 billion in 2025. This represents an upward revision from the previously forecast $110.8 billion in the SEMI 2025 Mid-Year Equipment Forecast, reflecting stronger than expected investments in DRAM and high-bandwidth memory (HBM) to support AI computing. Continued capacity build-out in China is also contributing meaningfully to WFE demand. Looking ahead, WFE segment sales are projected to expand 9.0% in 2026 and 7.3% in 2027, reaching $135.2 billion as device makers increase spending on advanced logic and memory technologies.

The back-end equipment segment is anticipated to continue its strong recovery that began in 2024. Sales of semiconductor test equipment are projected to surge 48.1% to $11.2 billion in 2025, while assembly and packaging (A&P) equipment sales are projected to rise 19.6% to $6.4 billion. Back-end growth is expected to continue, with test equipment sales growing 12.0% in 2026 and 7.1% in 2027, and A&P sales are forecast to grow 9.2% in 2026 and 6.9% in 2027. This expansion is underpinned by the growing complexity of device architectures, accelerated adoption of advanced and heterogeneous packaging, and stringent performance requirements for AI and HBM semiconductors. These drivers are partly offset by ongoing softness in consumer, automotive and industrial demand, which continues to weigh on some mainstream test and packaging segments.

Wafer fab equipment sales by application

WFE sales for foundry and logic applications are expected to show robust 9.8% year-over-year growth to $66.6 billion in 2025, supported by resilient spending for advanced nodes. The segment is forecast to see 5.5% growth in 2026 and 6.9% increase to $75.2 billion in 2027 as chipmakers add capacity for AI accelerators, high-performance computing and premium mobile processors. Investments will increasingly target leading-edge technologies as the industry moves toward high-volume manufacturing at the 2nm gate-all-around (GAA) node.

Memory-related capital expenditures are projected to see significant expansion through 2027 powered by increasing demand for HBM to support AI deployment and ongoing technology migration. The NAND equipment market is expected to see growth of 45.4% to $14.0 billion in 2025 and further increase 12.7% to $15.7 billion in 2026 and 7.3% to $16.9 billion in 2027, driven by advancements in 3D NAND stacking and capacity expansion at both leading and mainstream layers. DRAM equipment sales are projected to rise 15.4% to $22.5 billion in 2025, followed by 15.1% and 7.8% year-on-year growth in 2026 and 2027, respectively, as memory suppliers ramp HBM and upgrade to more advanced process nodes to meet AI and data center requirements.

‘Only photonics’ can satisfy AI’s insatiable appetite for compute power

As artificial intelligence expands, its soaring electricity use is putting unprecedented pressure on power grids, driving up costs and threatening to slow Europe’s energy transition. But a new report shows that only light-based computing can keep AI’s ever-expanding power demands at bay without triggering a surge in emissions.

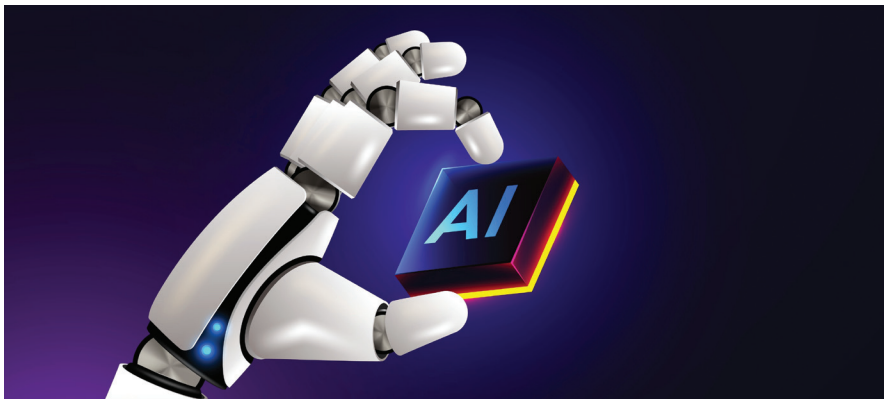
The study, published by Photonics21 and compiled by market intelligence agency TEMATYS, finds that as electricity use from AI rises sharply, and conventional silicon chips struggle to keep pace with the twin pressures of ever-larger models and expanding data centres, Europe risks undermining its clean-energy goals and increasing reliance on fossil fuels.

Entitled “AI Desperately Needs Photonics,” the report concludes that photonics, which uses light rather than electricity to move and process information, offers the only viable pathway to scale up AI computing while dramatically reducing energy consumption. The study reveals that integrating photonic technologies into data-centre and chip architectures can help AI growth remain compatible with Europe’s climate commitments.

AI is scaling faster than the world’s power grids can handle. Each new generation of larger, more complex models demands exponentially greater computing power, sending data-centre energy use soaring.

The International Energy Agency puts global consumption at roughly 415 TWh in 2024, and TEMATYS warns it could more than double by 2030 as AI workloads dominate digital infrastructure.

Sébastien Bigo, Nokia Bell Labs Fellow and Photonics21 Work Group Leader for Digital Infrastructure, said, “Photonics can provide the infrastructure that will determine whether AI becomes cleaner and more competitive or simply costlier and dirtier. Europe has the research base to lead; what it lacks is coordinated investment and industrial scale.”



The report shows that bringing photons much closer to the compute (whether through co-packaged optics or other emerging photonic integration approaches) and using light to handle increasing parts of data movement or specific acceleration tasks can considerably improve the carbon and cost profile of AI. While photonics is not a replacement for CPUs or GPUs, it can become a critical complement that eases the pressure on them. If Europe wants sovereignty in future AI hardware and to meet its climate commitments, the report stresses that Europe’s policy and investment decisions in the coming years will be decisive.

The report finds that photonics is already indispensable to the digital world. Fibre optics underpins today’s internet and data-centre infrastructure, and the next step of integrating light directly into chip architectures through co-packaged optics is already underway. These advances, however, will not be enough on their own. Even with industry claims of 3.5 times greater power efficiency, TEMATYS concludes that these gains cannot fully offset the surge in energy demand driven by AI’s rapid expansion.

The study also shows that optical computing is no longer theoretical. Laboratory breakthroughs and start-up prototypes, including MIT’s 2024 demonstration of an integrated photonic chip performing neural-network computations entirely with light, reveal a clear technical path towards fully photonic processors.

Finally, the report warns that Europe has the expertise but not yet the scale. World-class research and promising start-ups exist across the continent, but without faster investment, large-scale manufacturing, and workforce development, Europe risks surrendering this strategic market to competitors abroad.

The report urges European institutions, national governments and private investors to treat photonics as strategic infrastructure for AI. Recommended actions include: dedicated funding for pilot manufacturing, incentives to scale photonics start-ups, inclusion of photonics in Chips/AI/Green tech funding streams, and skills initiatives to build a manufacturing workforce. Without these steps, Europe risks ceding critical parts of the AI hardware value chain to overseas competitors while facing higher energy bills and emissions.

Siemens and GlobalFoundries collaborate

Strategic collaboration to enhance performance of semiconductors and other advanced industries based on both companies' AI-based capabilities.

SIEMENS and GlobalFoundries (GF) have entered a new strategic collaboration to leverage each company's complementary AI-based capabilities to enhance performance of semiconductor manufacturing and advanced industries – making operations more efficient, secure and reliable. In their latest memorandum of understanding, the companies focus on automation technologies for semiconductor fabrication (fab automation), electrification, digital solutions and software ranging from chip development to product lifecycle management.

A key element of the new strategic collaboration is deployment of advanced AI-enabled software, sensors and real-time control systems in fab automation to meet the growing demand for reliable semiconductors and autonomous platforms. Through centralized automation and predictive maintenance, GF and Siemens aim to increase equipment availability and operational efficiency in chip production while building capabilities that can be extended to other advanced industries. The companies intend to develop and deploy new solutions within their own operations to deliver enhanced offerings.

This expanded collaboration comes at a time of unprecedented demand for essential semiconductors and autonomous platforms in critical areas such as artificial intelligence, defense, energy and connectivity. By teaming up and bringing new capabilities, Siemens and GF can support accelerated growth, better security and reliability and broaden their impact across the industry.

"Our economy runs on Silicon – one wafer at a time. Chips are critical for applications like robotics or connectivity and for bringing AI into the physical world and industry. We are collaborating to make global semiconductor supply

chains more resilient and to enable efficient localized manufacturing around the world," said Cedrik Neike, Member of the Managing Board of Siemens AG and CEO Digital Industries.

"Secure, locally manufactured semiconductors are at the core of the AI transition – from cloud to the physical world, bringing intelligence into devices we use every day and enabling applications we couldn't imagine a few years ago," said Tim Breen, CEO of GlobalFoundries. "Our unique collaboration with Siemens allows us to go faster – to build the technologies that make this possible – differentiated, energy-efficient, connected and secure chips across a wide range of next-generation applications."

A key element of the new strategic collaboration is deployment of advanced AI-enabled software, sensors and real-time control systems in fab automation to meet the growing demand for reliable semiconductors and autonomous platforms

Siemens brings a comprehensive suite of industrial, energy & building automation and digitalization technologies including advanced software for chip design & manufacturing, fab automation, and product lifecycle management.

Utilizing Siemens' suite of solutions, GF and Siemens will enable seamless collaboration across the entire semiconductor lifecycle and deliver high performance and reliable semiconductor solutions at scale.

GF, together with MIPS, a GF company and global leader in RISC-V processor IP, brings unique process technology and design capabilities to accelerate the development and manufacturing of tailored solutions that support Siemens goal of enabling autonomous platforms and physical AI chips at scale. GF is one of the world's leading semiconductor foundries. The publicly listed U.S. company operates manufacturing facilities in the USA, Asia, and Europe. In Dresden, GlobalFoundries runs Europe's largest semiconductor production site with around 3,000 employees.

One step towards European excellence in microelectronics

VTT completes 200 mm silicon wafer size conversion in its cleanroom.

VTT completes the conversion of its cleanroom equipment in the Micronova cleanroom to 200 mm silicon wafer size. It has been a major project, during which the previous 150 mm semiconductor manufacturing equipment has either been converted or upgraded to support 200 mm wafers.

According to Piia Konstari, Director at VTT, the investment is part of Finland's goal to strengthen its leading role in the European specialised microelectronics ecosystem.

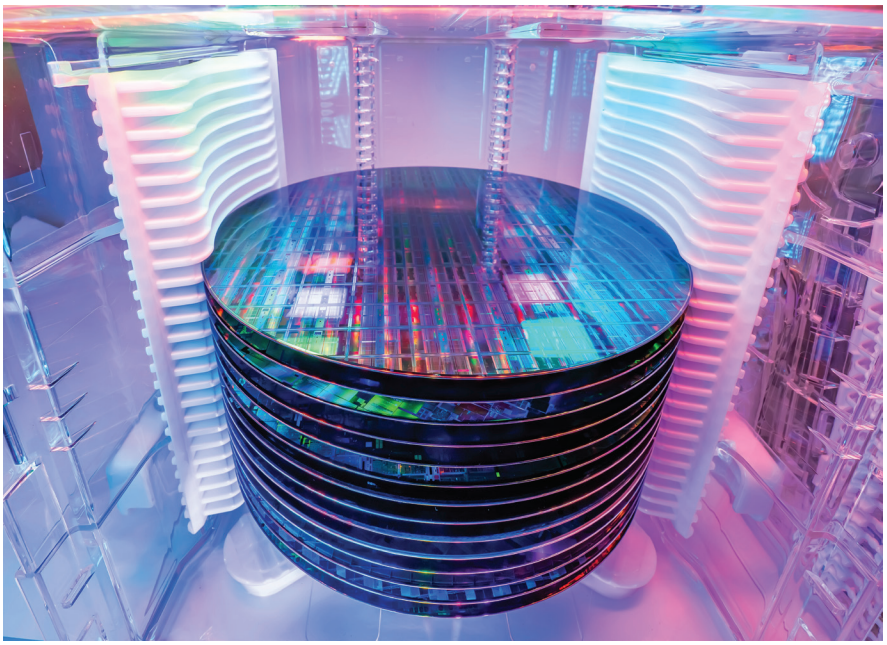
The investment strengthens Finland's position in specialised microelectronics development and supports Europe's strategic sovereignty in critical technologies. It also marks a significant step forward for Nordic semiconductor capabilities.

"This upgrade significantly enhances our toolset enabling us to efficiently process 200 mm sized wafers and benefit from the latest industrial technologies and processes.

With investments in front-end-of-line equipment as well as advanced back-end-of-line process equipment, we are strengthening our position in the forefront of microfabrication R&D and piloting," says Oliver Pabst, Head of Fab operations at VTT.

"Our goal is to build a leading European microelectronics R&D and piloting cleanroom and ecosystem, supporting research, development, innovation, piloting and industrialisation. Our customers and partners will widely benefit from VTT's new capabilities.

This investment is part of a broader strategy through which VTT and Finland strengthen their leading role in the European specialised microelectronics ecosystem," says Piia Konstari, Director, Microfabrication services at VTT.



The funding for this upgrade has come from Business Finland, the Research Council of Finland, the EU PREVAIL project, as well as VTT's own funds granted by the Ministry of Economic Affairs and Employment.

The project has spanned several years, beginning in 2019 and continuing through 2025, reflecting the scale, complexity and ambition of the transformation.

The rationale behind this conversion is rooted in the widespread adoption of 200 mm silicon wafers in the semiconductor industry and to the compatibility with other European cleanroom wafer sizes.

The 200 mm wafer size is a standard choice for fabrication in MEMS (micro-electromechanical systems), RF (radio frequency) devices, analogue integrated circuits, integrated photonic components and quantum circuits.

Transitioning to 200 mm wafers ensures seamless compatibility with key customers and research partners, including several prominent EU institutions that have already standardised their processes around this wafer size.

The availability of cutting-edge processing equipment for 200 mm wafers is rapidly expanding, while support and equipment for the older 150 mm format is on the decline.

This demonstrates that the upgrade to 200 mm wafer size is not only strategic but necessary to remain competitive and relevant in the market.

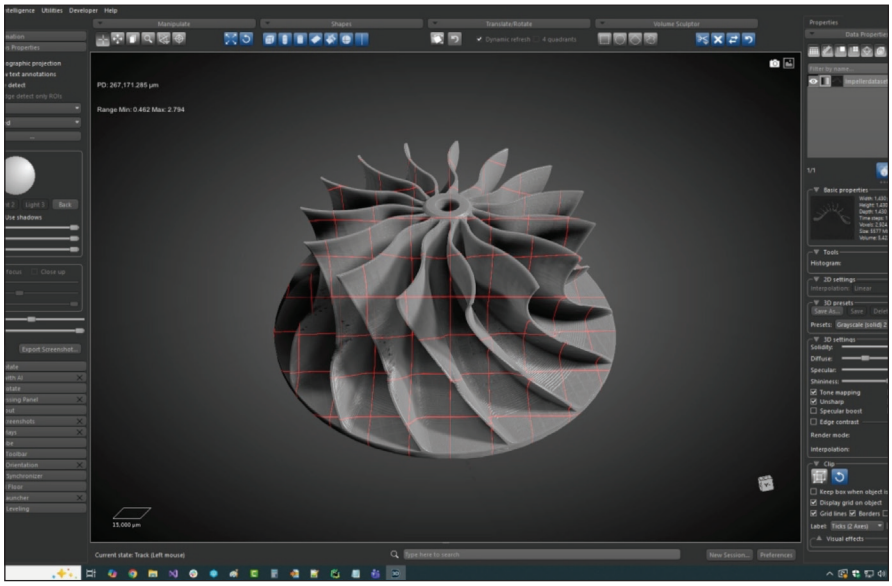
Furthermore, the 200 mm wafer size offers access to a wide range of specialised wafer types, such as Silicon-on-Insulator (SOI), enabling advanced fabrication possibilities such as monolithic integration with CMOS technology, wafer-to-wafer bonding, and chip-to-wafer assembly processes.

These new capabilities lay the ground for future innovation, allowing VTT and the Finnish ecosystem to explore more complex system architectures and integrated solutions.

Dragonfly 3D World 2025 transforms 3D image analysis

Comet Technologies Canada Inc. has launched Dragonfly 3D World 2025, a major software upgrade that redefines how scientists and engineers explore, analyze, and quantify complex 3D image data.

WITH its new high precision surface determination, faster GPU-accelerated performance, advanced one-click AI segmentation, and next-generation visualization tools, 3D World 2025 delivers a powerful combination of speed, precision, and usability for applications in materials science, life sciences, electronics, additive manufacturing, automotive, and beyond.



Smarter segmentation. deeper insight

Segmentation lies at the heart of image analysis and 3D World raises the standard once again. The newly integrated Meta AI's Segment Anything Model (SAM) brings one-click annotation to even the most complex objects, from microstructures to biological tissues. By adapting across imaging modalities, SAM enables users to identify and isolate meaningful features instantly, without manual thresholding or model training.

"This release marks a major leap forward in segmentation automation," says Joscha Malin, Director of Software Solutions at Comet. "Dragonfly 2025 helps our users spend less time preparing data and more time interpreting it — driving faster decisions and more accurate results."

Precision that Reaches Beyond the Pixel

When it comes to quantitative measurement, accuracy starts at the surface. 3D World 2025 introduces a redesigned Surface Determination engine, now capable of sub-voxel precision. This advancement enables highly accurate surface and mesh extractions - a critical step for geometric metrology, roughness analysis, and dimensional validation.

Combined with new 3D rendering modes, users can visualize internal and external structures with photorealistic clarity, making even the smallest details measurable, shareable, and ready for publication.

Accelerated workflows for modern research and manufacturing

Whether analyzing thousands of CT slices or processing terabytes of microscopy data, performance defines productivity.

3D World 2025 introduces GPU-accelerated filtering, denoising, and skeletonization that deliver a performance improvement of as much as 100x over CPU processing. For instance, a Canny filter applied to a 1024^3 USHORT dataset is completed in under 1.4 seconds on an NVIDIA GeForce RTX 4090, compared to over 55 seconds on an Intel i7-13700K CPU. Together with macro automation and upcoming Auto Executor add-ins, this release empowers users to build fully reproducible, high-throughput pipelines that scale from single-lab experiments to industrial inspection lines.
This leap in efficiency helps both research teams and manufacturers achieve faster validation cycles, improved quality control, and deeper data-driven understanding of materials and components.

Setting the standard in 2D, 3D, and 4D image analysis worldwide

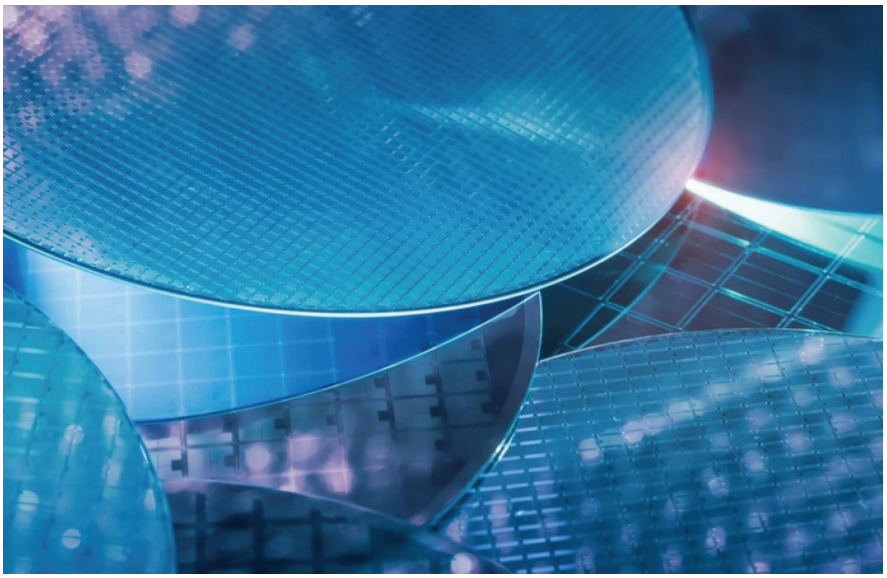
Dragonfly has long defined the benchmark for advanced image processing and quantitative analysis. Trusted by global leaders in X-ray CT and X-ray microscopy, the software is relied upon by industry innovators such as Comet Yxlon, Zeiss, Tescan, Rigaku, and Brucker, as well as by leading research institutions worldwide.

By powering inspection and visualization software for major OEMs, Dragonfly technology has become the analytical backbone of modern imaging - supporting applications in materials research, electronics, additive manufacturing, and life sciences.
With the release of 3D World 2025, Dragonfly strengthens its leadership position, delivering tools that drive faster insight, greater precision, and smarter automation across the global imaging community.

Silicon Labs partners with Rimini Street

Multi-year strategic partnership empowers Silicon Labs to maximize SAP ECC 6.0 value, accelerate transformation and avoid costly upgrades and disruption.

SILICON LABS has selected Rimini Street as its strategic partner to maximize the value of its SAP ECC 6.0 investment. This collaboration provides the U.S.-based semiconductor manufacturer with long-term SAP maintenance and professional services to accelerate modernization without costly upgrades or business disruption.



Partnership reduces technical debt and accelerates modernization

Silicon Labs first engaged Rimini Street's professional services team, Rimini Consult™, to develop a strategic ERP roadmap leading to a multi-system project to align 12 SAP environments with modern operating system and database standards.

The project reduced Silicon Labs' technical debt by improving platform stability, strengthening its security and compliance posture and delivering faster, real-time reporting capabilities to support informed executive decision-making.

"Rimini Street not only delivered outstanding results for our SAP project, but we were also able to go live ahead of schedule, working side by side with our team to ensure success from start to finish," said Radhika Chennakeshavula, CIO and vice president of Silicon Labs. "Our current SAP ECC investment continues to provide value across our operations. As part of our innovation strategy, we are accelerating new capabilities built on and around our SAP core, modernizing where needed without the cost, risk and disruption of an unwanted move to RISE with SAP. I prefer to make impactful investments of our people, time and money to harness the full power of the latest AI technology rather than a low-ROI platform upgrade".

Outstanding results lead to expanded partnership

The success of the professional services engagement with Rimini Street became the catalyst for a five-year Rimini Support™ for SAP agreement generating an immediate savings of 50% on annual support costs, along with additional solutions such as Rimini Watch™, Rimini Street's change management alternative to SAP Solution Manager, allowing Silicon Labs to move quickly in its growth strategy.

"Rimini Street is more than a service provider. They are now a trusted, long-term partner that respects our strategic direction, aligns with our vision and delivers real value," said Chennakeshavula. "Rimini Street frees up critical resources, fast-tracks innovation and provides expert support across our global operations, giving us the flexibility to modernize on our own terms and timeline." With deep confidence in Rimini Street's ERP expertise and capabilities, Silicon Labs is expanding its partnership to include new Agentic AI ERP innovations.

"We are proud to serve as a strategic partner to leading manufacturers such as Silicon Labs, helping to build a stronger, more secure operation that is agile in its ability to adopt the latest technology without lengthy migrations or replatforming," said Jeff Chenevey, Rimini Street's VP of manufacturing industry solutions. "Rimini Street's end-to-end approach means we look after the full scope of needs for our clients, expertly managing today's needs while accelerating tomorrow's capabilities."

We are proud to serve as a strategic partner to leading manufacturers such as Silicon Labs, helping to build a stronger, more secure operation that is agile in its ability to adopt the latest technology without lengthy migrations or replatforming

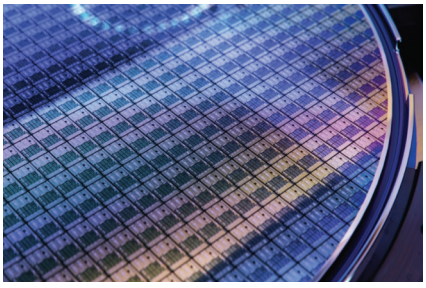
ACM Research delivers first horizontal panel electroplating tool

ACM's Ultra ECP ap-p enables next generation device performance amid accelerating market demand for advanced packaging.

ACM RESEARCH has delivered the first panel electrochemical plating tool, the Ultra ECP ap-p, to an industry-leading panel fabrication customer.

This achievement underscores ACM's advancement in panel-level electroplating technology and reflects growing market demand for scalable, cost-efficient advanced packaging solutions to meet next generation device requirements.

The Ultra ECP ap-p is the first commercial panel-level copper deposition system for the large-panel market, supporting plating steps across pillar, bump, and redistribution layer (RDL) processes. The system achieves panel-processing performance - comparable to traditional round wafer processes, enabling manufacturers to meet demanding device requirements with greater efficiency.



"We are pleased to fulfill this order for our Ultra ECP ap-p," said Dr. David Wang, ACM's President and Chief Executive Officer. "This milestone demonstrates our ability to deliver high-performance horizontal panel electroplating solutions through our differentiated technology that help customers accelerate their fan-out panel-level packaging roadmaps while strengthening our role in the advanced packaging ecosystem. As demand grows for next-generation devices, panel-level packaging offers the scalability, throughput, and cost advantages needed for high-volume production, which will achieve a seamless transition for the industry from 300-millimeter wafer packaging to panel-level packaging."

The system features ACM proprietary horizontal electroplating technology, and supports copper (Cu), nickel (Ni), tin-silver (SnAg) and a gold (Au) plating.

The Cu plating chambers incorporate high-speed plating paddles specifically designed for tall pillar applications, capable of achieving pillar heights exceeding 300 microns. The Ultra ECP ap-p features a four-sided sealing dry contact chuck for improved reliability, in-cell rinse functionality to minimize chemical cross-contamination between different plating cells, and a horizontal electroplating design synchronizing a rotating square electrical field with the rotating chuck for superior deposition uniformity.

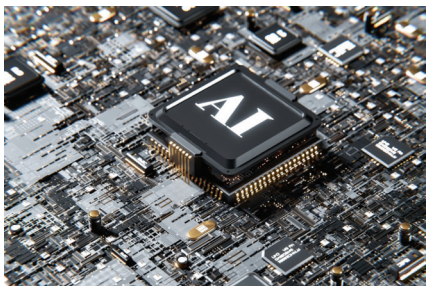
Qnity spins from DuPont

QNITY ELECTRONICS, INC. has compleeted its separation from DuPont de Nemours, Inc..

Jon Kemp has assumed the role of Chief Executive Officer of Qnity and continues as a member of Qnity's Board of Directors, as planned. Prior to this appointment, Kemp served as president of DuPont's Electronics & Industrial business, where he led major portfolio transformation and business growth.

"Today marks a pivotal milestone, built on decades of innovation, as Qnity begins its next chapter as a leading pure-play technology provider serving the semiconductor value chain," said Kemp. "Driven by strong customer partnerships, global reach, and a broad portfolio of industry-leading materials and technologies, Qnity is making tomorrow's technologies possible. This includes the transition to advanced nodes, especially for AI applications, including chip manufacturing, advanced packaging, and thermal management."

Qnity has more than 10,000 employees serving customers in more than 80 countries and regions. Facilities include 39 manufacturing sites and 17 R&D facilities around the world. Two-thirds of Qnity's portfolio is tied directly to semiconductors, giving the company a total addressable market exceeding $30 billion. The global semiconductor industry revenue is projected to surpass $1 trillion1 around the end of the decade.



At the company's Investor Day in September, Qnity's leadership outlined its financial strategy to achieve above-market growth and strong profitability through 2028.

"As a pure-play company focused on the evolving needs of the semiconductor industry, we're confident in our position to deliver sustained outperformance relative to peers and the market," said Matt Harbaugh, Chief Financial Officer of Qnity.

Powerful inspection solutions for wafer and chip level packaging.

From root cause analysis in the lab, to fast process analysis in the fab, Comet's leading 2D and 3D X-ray technology provides powerful inspection solutions for wafer and chip level packaging, enhanced with incredible AI-based software.

	Height	Diameter
TSV	105 µm	10 µm
Void	50 µm	6 µm

Visualization of 3D X-ray inspection results of TSV fills in a wafer. Wafer designed for Comet by Fraunhofer IZM_ASSID, it contains voids for illustrative purposes.

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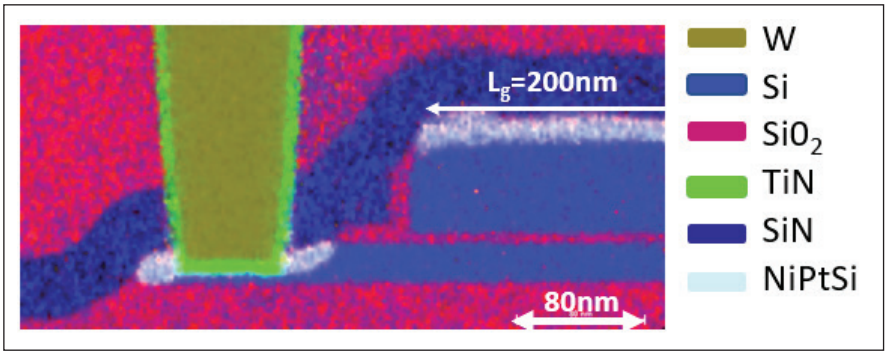
R&D advances for the FAMES Pilot Line

400 °C CMOS breakthrough opens critical doors to 3D integration goals.

CEA-LETI, the coordinator of the FAMES Pilot line, has achieved a major milestone for next-generation chip stacking: fully functional 2.5 V SOI CMOS devices fabricated at 400 °C. The devices match electrical performance of devices fabricated at standard thermal budget (>1000 °C), removing one of the last barriers to large-scale 3D sequential integration (3DSI) – a core objective of FAMES.



Enabled by advanced CEA-Leti expertise in low-temperature processes (nanosecond laser annealing (NLA) and solid-phase epitaxy regrowth (SPER)), this work offers true three-dimensional device stacking from the lab to fab. 3D sequential-integration interconnection density between tiers is the highest among 3D technologies, such as TSV and hybrid bonding. In this project, CEA-Leti demonstrated that Si CMOS is BEOL compatible, and thus can be stacked safely above BEOL, while transistor performance and maturity overtake largely the other technological options from the state-of-the-art, low-temperature solutions.

The achievement, presented today in a paper at IEDM 2025, titled, "High Performance 2.5 V n&p 400 °C SOI MOSFETs: A Breakthrough for Versatile 3D Sequential Integration," is a key breakthrough for the FAMES Pilot Line, a European Union initiative launched in 2023 in response to the EU Chips Act strategy to strengthen sovereignty and competitiveness in semiconductor technologies. By combining 3D heterogeneous and sequential integration on FD-SOI platforms, the consortium aims to enable a new generation of More-Than-Moore devices and applications.

Enabling new chip architectures

"This breakthrough is a major milestone of the FAMES project as it enables innovative new chip architectures," said Dominique Noguet, CEA-Leti vice president and coordinator of the FAMES Pilot Line. "Our low-temperature process could accelerate real-world demonstrations of multi-tier stacks combining advanced CMOS logic, with smart pixel or RF layers, to create new high-performance 3D chips."

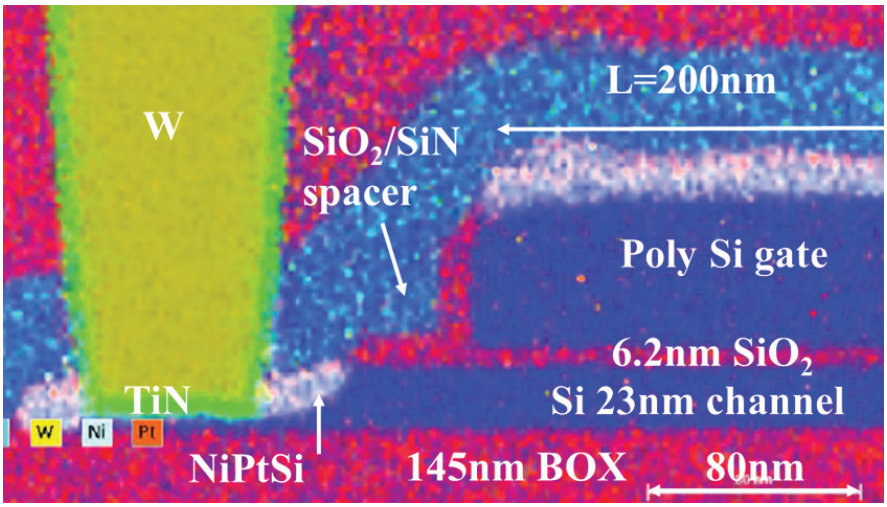
Concept of 3-tier µLED GaN pixel allowing an emissive array with strong pitch reduction thanks to 3DSI in combination with 3D hybrid bonding technology. CEA-Leti's 400 °C CMOS process enables such top-tier integration without exceeding the thermal limits of the active circuitry below. The team showed that SOI devices processed at 400 °C instead of the high temperature (>1000 °C) industry standard and high-temperature industrial reference, performed equivalent to high-temperature devices.

"The 400 °C process enables 3D sequential stacking on any bottom tier," Noguet said. "It's a huge step forward because it's far more mature—reliable and scalable – than current low-temperature solutions, such as polycrystalline films, oxide semiconductors or carbon nanotubes."

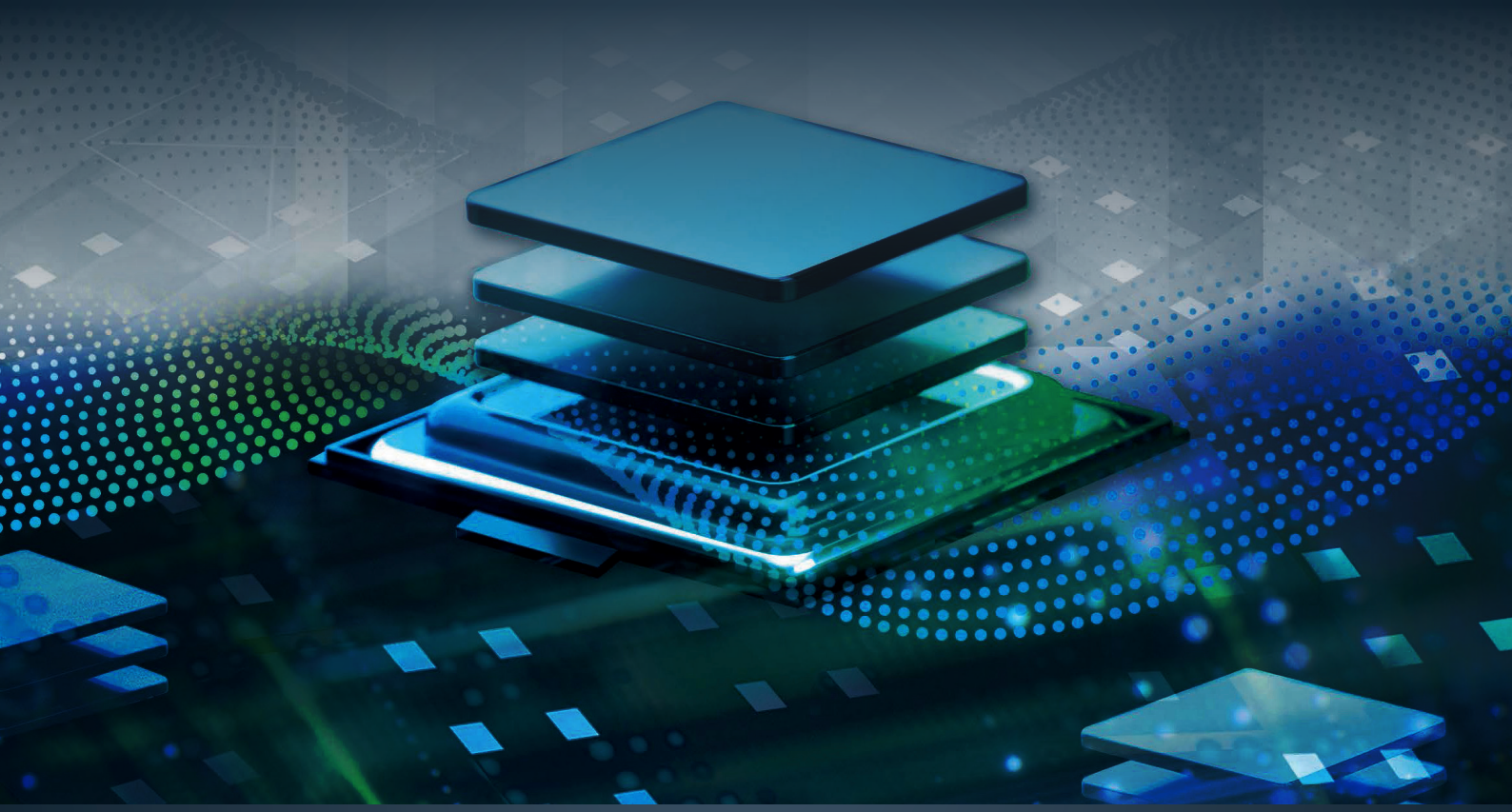
Protecting circuitry on bottom-tier layers

In their paper, CEA-Leti's team demonstrated n- and p-type transistors matching the characteristics of conventional high-temperature CMOS devices, while staying within the ≤400 °C thermal budget required to preserve active circuitry in lower layers. The process relies on an optimized 400 °C LPCVD deposition for amorphous silicon followed by NLA in the melt regime for dopant activation and diffusion – producing polycrystalline, low-resistance gates with excellent interface quality. In addition, NLA-SPER mastering enables dopant activation without diffusion leading to access resistance within specifications.

"Our strength lies in mastering the cold process – especially nanosecond laser annealing – to achieve high-mobility, high-reliability CMOS at low temperature," said Daphnée Bosch, lead author of the paper. "This laser expertise makes our approach unique."



MKS Advanced Packaging Handbook



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Explore how advanced packaging is reshaping semiconductor integration – unlocking new possibilities through heterogeneous and system-level design.

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Driving success for customers

Alan Maher, Business Development Manager, Greene Tweed, shares his thoughts on the industry's current buzz topics, as highlighted at SEMICON West, before outlining what is keeping the company busy, both now and into the future

SIS: *If we can start with your overall feedback from the recent SEMICON West event – was it a success for Greene Tweed?*

AM: Absolutely. Attendance was up significantly from last year, and you could feel the energy throughout the event. Having it in Arizona was also a nice change, especially with so many customers now based there. And locals turned up in numbers, which really helped.

Our booth was also buzzing with activity – customers, partners, analysts – it was a steady stream of meaningful conversations. The overall tone of the event, I would say, was optimistic.

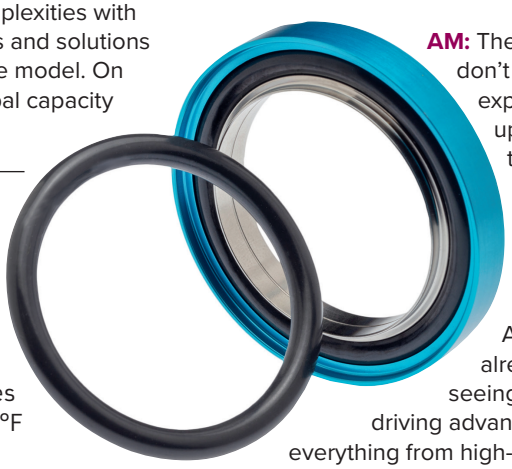
SIS: *There were a number of challenges discussed during the event – economics, supply chain and geopolitics, talent shortage and sustainability issues – what's the Greene Tweed take on these?*

AM: **Supply chain**
The semiconductor industry is inherently cyclical, and supply chain challenges will always persist. We're focused on helping our customers navigate these complexities with innovative materials and solutions with our dual source model. On top of that, our global capacity investments ensure we're ready to support the next wave of growth. Our latest being our new manufacturing facility in Korea

Talent shortage
This is a critical issue for the industry. We ourselves are addressing it by fostering innovation and efficiency and making semiconductor careers more rewarding. Collaboration with partners and a focus on automation are key. Then there are great initiatives like the UK's Women in Tech Works that are focused on attracting and retaining more women in the industry.

Sustainability
We're committed to providing materials and solutions that perform at the highest level, while being mindful of their environmental impact. It's about balancing innovation with responsibility. We have two projects in the works where sustainability is the key driver that we hope to bring to the market in the near future.

SIS: *There was also a great deal of positivity about the industry's numbers and future, with AI seen as the major opportunity right now?*



➤ Fusion® F07 FKM seal assembly used in semiconductor SubFab vacuum fittings and vacuum system lines operating up to 355°F (180°C).

AM: The numbers don't lie – AI is expected to make up nearly half of the semiconductor market by 2030.

That's huge. And we're already seeing how it's driving advancements in everything from high-performance computing to advanced packaging. Greene Tweed is partnering with customers to tackle the unique challenges AI brings to manufacturing, in areas like particulation, electrostatic discharge, and adapting to new chemistries. It's exciting to be part of shaping AI.

SIS: *Alongside the related topic of advanced packaging – 3D is here?!*

3D is a new frontier. At SEMICON West, it was clear that hybrid bonding, substrate innovation, and other advanced packaging technologies are driving the industry forward. Greene Tweed is already making an impact in this space. Our Chemraz solutions are helping customers tackle the challenges of advanced packaging, from yield improvement to process reliability.

As the industry continues to push the boundaries of 3D integration, we're excited to extend our collaborations and help drive this innovation forward.

SIS: *If not already covered, it would be great to understand Greene Tweed's role when it comes to supplying technology solutions to help the development of AI and advanced packaging technologies?*

AM: Greene Tweed aims to be at the forefront of enabling the next generation of semiconductor technologies. For AI, we're delivering solutions that address critical manufacturing challenges, ensuring our customers can meet the demands of this rapidly growing market. In advanced packaging, we partner with customers to design materials that support the precision and reliability required for cutting-edge processes,

like hybrid bonding and 3D integration.

SIS: *A couple of other takeaways from the event – the need for cost-effective innovation?*

AM: Cost-effective innovation is a cornerstone of Greene Tweed's approach. We understand that our customers need solutions that deliver exceptional performance without compromising on value.

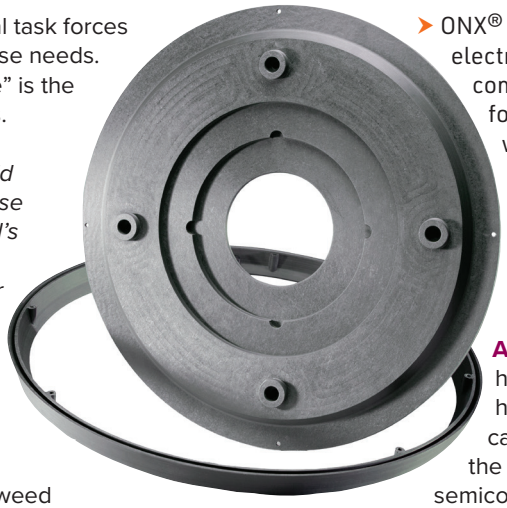
We remain committed to providing a well-balanced portfolio of options, including Chemraz, Fusion, and ONX materials, designed to strike a balance between performance and cost of ownership. For example, our Fusion F07 line exemplifies how we address specific process challenges while keeping cost-effectiveness in mind. Similar is our recently launched Chemraz G-Series range.

SIS: *And the acknowledgement that no one organisation can 'do it all' – why is collaboration important?*

AM: No single organization can tackle every challenge alone, especially in an industry as complex as the semiconductor ecosystem. To overcome the biggest hurdles, we need to work together.

Greene Tweed prioritizes close collaboration with Fabs, OEMs, and other industry leaders, as well as industry trade bodies. By working together, we co-develop innovative solutions to complex problems more effectively. I, myself, am part of a collective, grouping the critical needs of Fabs and OEMs in the USA and UK, and forming tactical task forces to address these needs. The "collective" is the key to success.

SIS: *How would you characterise Greene Tweed's profile in the semiconductor industry as of now – what have been the successes?*



AM: Greene Tweed has been a trusted partner and innovator in the industry for over 35 years. Our materials and solutions are integral to critical processes across etch, dep and now advanced packaging, and we keep pace with changing needs.

You will find us on everything from 30-year-old legacy tools to the latest, most advanced tools in the world's leading Fabs.

Our success comes from a relentless focus on quality, innovation, and collaboration. However, the main driver of our success has been providing technology-enabling solutions to our customers' problems. By staying true to that approach, I believe we will continue to lead our field for years to come.

SIS: *And how are you looking to further develop your presence in the sector – any plans you can share as to technology innovations coming down the line, different ways of working with partners and the like?*

- ONX® 600 lightweight, electrically conductive composite components for semiconductor wafer handling and cleaning systems, stable up to 260°C (500°F).

AM: Greene Tweed has invested heavily in our global capacity to support the next growth in semiconductors, as well as the research and development to create new materials and solutions for critical processes like etch, deposition, lithography, etc.

We're also strengthening our collaborations with OEM equipment providers and exploring new opportunities in advanced packaging and AI, so Greene Tweed can stay ahead of the curve and help our customers do the same.

SIS: *Greene Tweed solutions cover a great many applications within the semiconductor industry – how to build on this success?*

AM: We need to continue to innovate, deepen our partnerships with OEMs, Fabs, and academia, and deliver solutions that address our customers' evolving needs.

Whether that's through new materials or advanced manufacturing techniques, we're committed to driving success for our customers.

Preventing liquid cross-contamination in semiconductor manufacturing

Producing high-purity wafers via the CMP process is a critical application and the halting of harmful slurry-DIW cross-contamination and back-flow can be optimised with the Malema Interconnect Interlock Device.

BY JAY RAJAGOPALAN, MALEMA

CHEMICAL MECHANICAL PLANARIZATION, or CMP, also known by some of its practitioners as Chemical Mechanical Polishing, is a stage in the semiconductor-manufacturing process where the surfaces of an integrated circuit – otherwise called a "wafer" – are smoothed and flattened via chemical and mechanical forces.

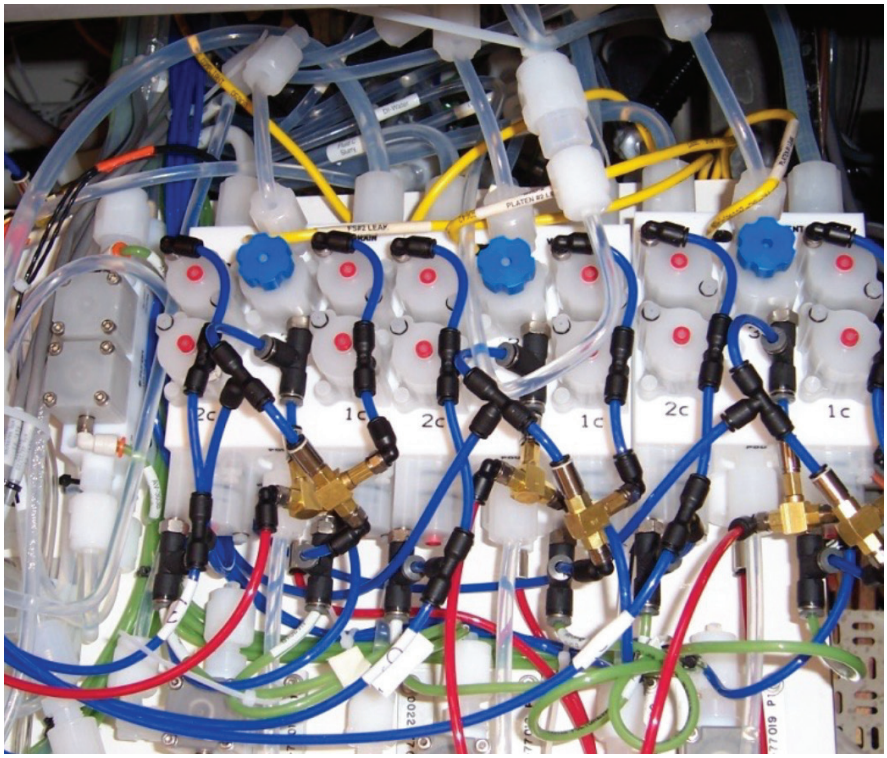
The CMP process requires the use of a colloidal chemical slurry that contains nano-sized abrasive powders. The slurry is pumped over the surface of the wafer with a polishing tool, which removes excess material and imperfections from the wafer's exterior, resulting in a uniformly smooth and ultra-flat, or planar, finish. In the final stage of the CMP process, deionized (DI) water is sent through the polishing

➤ Chemical Mechanical Planarization (CMP) is a critical stage in the manufacture of integrated circuits (wafers) for use with semiconductors. As such, it is imperative that the colloidal chemical slurry and deionized (DI) water that are used in the process do not commingle, with any cross-contamination compromising the slurry's ability to deliver the required level of smoothness to the wafer's surface. The Malema™ Interconnect Interlock Device (MIID-1000) overcomes this challenge through a design and method of operation that specifically prevent cross-contamination of the slurry and DI water, resulting in an optimized CMP process.

tool in order to wash away any remaining chemical slurry from the wafer's surface before the next wafer in the production line is treated.

To optimize the CMP process, it is imperative that the dedicated supplies of chemical slurry and DI water not be allowed to commingle; allowing this to happen will adversely affect the slurry's ability to deliver the demanded level of smoothness to the wafer's surface. However, some semiconductor manufacturers noticed slurry contamination with DI water within their CMP systems, which led to lost wafers, overall reduced yields and unwanted repair, replacement and cleanup costs.

This article will illustrate how this phenomenon was confronted and, eventually, solved through the creation of a breakthrough technology: the Malema™ Interconnect Interlock Device (MIID-1000), which has been designed to specifically prevent cross-contamination of the CMP slurry and DI water.



➤ One of the differentiating advantages of the Malema MIID-1000 is that it can be retrofitted onto existing CMP polishers as a drop-in replacement for the existing slurry-supply manifold. Malema streamlines this retrofit process by including all of the needed parts in a replacement kit with a single part number.

The challenge

As mentioned, the overarching challenge of the CMP process comes from the aggressive nature of the chemicals that are used, as well as the abrasiveness of the very-fine grinding particles found in the polishing medium. This makes the flushing away of the used chemical slurry with DI water critical to the success of the CMP operation.

At the beginning of the process, however, the chemical slurry must not be contaminated by any other type of liquid. If this occurred, its ability and effectiveness in producing the ultrasmooth and ultra-flat wafer surface would be compromised.

The prevention of this unwanted occurrence has traditionally been achieved by using a three-way diverting valve designed to alternately deliver the chemical slurry and DI water for the CMP process. Operators were discovering, though, that there were times when the polishing tool requested slurry that DI water was delivered instead and vice versa.

An investigation into what was causing this problem also revealed that DI water was diluting the chemical supply and, again, vice versa. At this point, the entire semiconductor-manufacturing system would need to be shut down for cleaning.

A thorough, top-to-bottom examination and review of the CMP system revealed that the root cause of the slurry/DI water cross-contamination was unexpected and intermittent reverse liquid back-flow or internal bypass leaks in the three-way valve that were occurring during certain operating conditions experienced by the polishing tool. Finding this hiccup in the CMP process was difficult because while the valves were indeed malfunctioning, they were not actually being damaged at the same time, so they would often times return to normal function for a period of time before malfunctioning again.

Identifying the problem was also made more problematic by the simple mechanical fact that, to some degree, all valves will leak. The job for the user is to determine what is an acceptable leak rate for the application in which the valves will be used. Further complicating the problem is the volume of slurry or DI water that was lost during back-flow or reverse bypass-leak conditions could be less than 5 milliliters per minute (0.17 ounces per minute), a miniscule amount that can be extremely difficult to detect, yet one that still possesses the ability to contaminate or dilute the CMP processes' cross-connected liquids.

This cross-contamination via back-flow and bypass leaks can be prohibitively costly for the semiconductor manufacturer since it will typically result in the cessation of the production process and long periods of downtime.

These unplanned shutdowns to repair or replace leaking components and clean up contaminated plumbing systems will both adversely affect the operation's overall financial performance and make meeting tight delivery schedules virtually impossible.

All of this meant that a solution to the problem would have to satisfy two things: 1) detect when a back-flow or a reverse-bypass leak was occurring in the three-way valve and 2) prevent these events from happening.

The solution

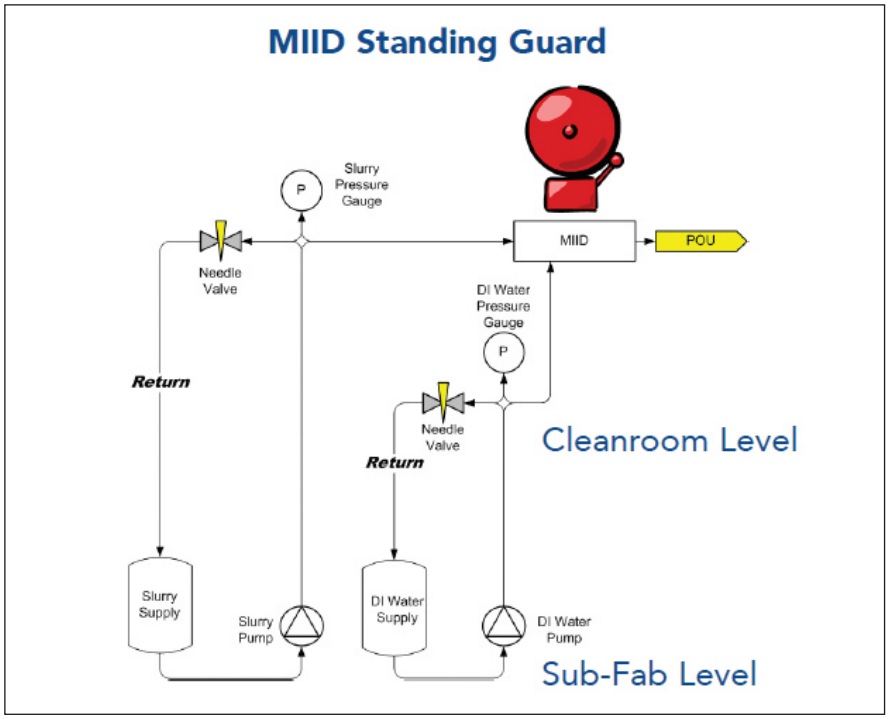
Recognizing the urgent need for a solution to the leaking three-way valve quandary, Malema, Boca Raton, FL, USA, a brand of PSG®, Oakbrook Terrace, IL, USA, a Dover company, began searching for ways to either prevent the leaks from occurring or develop a next-generation solution to the conundrum.

With over 20 years of experience supplying ultrasonic- and Coriolis-based flow measurement and control solutions to major semiconductor equipment manufacturers, the engineering team at Malema understood the industry's exacting requirements for cleanliness and reliability.

In the search for a leak-halting solution, Malema engineers tested a variety of methods that could potentially prevent the leaking-valve condition.

These included the incorporation of low-flow uni- and bi-directional flow switches, flow meters, and pH and conductivity meters. While these pieces of equipment were able to detect back-flow and bypass leaks in the three-way valves, they were only able to do so after the slurry or DI water supplies became contaminated, which compromised the CMP process.

The "eureka" moment for the Malema research team came when they determined that a "double block-and-bleed" (DB&B) valve arrangement would prevent reverse bypass leaks. DB&B is a piping configuration that anticipates leaking valves, but provides absolute protection against their precarities by placing dedicated isolation valves upstream and downstream of a third vent valve on both the CMP slurry and DI water lines.



➤ A built-in leak sensor in the Malema MIID-1000 enables it to prevent cross-contamination from occurring by sounding a warning when a potential back-flow event that will mix the CMP slurry with DI water could be imminent.

This double containment between the two liquid-supply lines ensures that no amount of back-flow or bypass leaks will bleed through to the other side of the valve block. Instead, any CMP slurry or DI water that does leak is vented out of the polishing tool before it reaches the point of use (POU). In laboratory tests where all of the valves were actually forced to leak, the DB&B configuration prevented any of the leaked liquid from working its way downstream to the POU or back upstream to the supply lines.

These features were incorporated into the patented Malema Interconnect Interlock Device (MIID-1000) By-Pass Leak Detection and Prevention System, which has been designed specifically to protect against liquid back-flow and internal bypass leaks. This capability is created via a manifold of pneumatically actuated valves that operate in a coordinated fashion in order to ensure that CMP-liquid supplies cannot be contaminated before use or during the actual CMP process.

"The "eureka" moment for the Malema research team came when they determined that a "double block-and-bleed" (DB&B) valve arrangement would prevent reverse bypass leaks. DB&B is a piping configuration that anticipates leaking valves, but provides absolute protection against their precarities by placing dedicated isolation valves upstream and downstream of a third vent valve on both the CMP slurry and DI water lines"

Key features of the MIID-1000 include:

- All wetted components are constructed of high-purity PTFE (modified) and PFA
- Non-wetted surfaces of PFA and PVDF
- Other materials used: FKM seals, ECTFE-coated stainless steel, polypropylene, nylon and acetyl
- Media-pressure range from 0 to 80 psig (0-5.5 bar)
- Pneumatic-actuation pressure range of 60 to 120 psig (4.1-8.3 bar)
- Media-temperature range of 0°F to 265°F (-17.7°C-130°C), excluding phase changes

MIID standing guard cleanroom level sub

- Ambient-temperature range from 0°F to 150°F (17.7°C-130°C), with no frozen liquids allowed • Critical Value characteristic: Cv = 0.8

- Field-configurable inlet connections – with either 1/4- or 3/8-inch flare nipples – that allow for simplified retrofit installation and reduced inventories
- Minimal had loss
- Built-in leak detection and monitoring
- Built-in optical valve-position sensing
- Valve components tested to more than 10 million cycles for DI water and more than 2 million cycles for SS-12 slurry

To simplify the incorporation of the MIID-1000 into a CMP system, Malema integrated the supply lines for the CMP slurry and DI water into a single block. This combines the leak-detection and drain-management features of two DB&Bs in one easy-to-handle and install console.

Additionally, Malema has created MIID-1000 retrofit kits – which can be installed by an experienced technician in as little as two hours – that include all components needed to upgrade an existing CMP system.
The retrofit kits place the MIID-1000 into a watertight programmable logic controller (PLC) enclosure. This allows the system's existing plumbing and pneumatic signals to be repurposed to manage the MIID-1000's functions.

Since this process makes the operation of the MIID-1000 completely transparent to the system's host-tool controller, no adjustment to the host tool's software is needed. Finally, all of the electrical connections between the MIID-1000 and the PLC are fully connected. This enables any leak-warning signals generated by the MIID-1000 PLC to be communicated to the existing user-input channels on the CMP polishing tool.

Conclusion

The use of three-way valves in CMP systems in semiconductor manufacturing had been accepted, as had the fact that, at some undetermined point, those valves would experience liquid back-flow or internal bypass-leak conditions. The problem with this habitual "cost of doing business" with three-way valves was unpredictable cross-contamination of the chemical slurry and DI water that are the lifeblood of the CMP process.

The results when this happens are not pleasant or profitable: shutdown of the semiconductor-manufacturing process; excessive downtime to rectify the problem; and the accumulation of ancillary repair, replace and cleanup costs that will have a deleterious effect on the operation's bottom line.

To put an end to this untenable situation, Malema worked to find a solution, achieving it with the creation of the Malema Interconnect Interlock Device. This innovative device allows semiconductor manufacturers to replace their OEM-supplied and mis-performing three-way valves with a DB&B-based solution that completely eliminates liquid back-flow and internal bypass leaks.

The ultimate result is optimized wafer production that can be a boon to the semiconductor-manufacturing operation's bottom line.

Safety, purity and performance in semiconductor cleanroom environments

Advanced Almatec AODD pumps play a vital role in next-generation semiconductor manufacturing

BY JESSE OWEN AND DANIEL CZEKAJ, ALMATEC

THE semiconductor industry is growing at an unprecedented pace, fueled by the demand for advanced electronics, 5G infrastructure, AI processing power and IoT integration. As chip geometries shrink and production volumes increase, even the smallest impurities or equipment failures can result in costly yield losses. This environment demands not only cutting-edge fabrication tools but also auxiliary equipment, like pumps, that can maintain strict purity, safety and uptime requirements throughout production.

Because semiconductor manufacturing continues to evolve in scale and sophistication, pump technologies must meet increasingly stringent demands. Whether it's transferring solvents, handling waste streams, or maintaining safety in environments with explosion risks, cleanroom-compatible pumping systems must deliver uncompromising performance without contaminating delicate processes.

One technology stands out for its ability to meet these challenges: air-operated double-diaphragm (AODD) pumps. Offering a unique combination of metal-free construction, chemical resistance, self-priming capability and ATEX compliance, AODD pumps are increasingly being adopted in semiconductor cleanroom environments, especially for niche applications involving aggressive or explosive fluids.

This article explores how AODD pumps, specifically those designed for conductive, solvent-handling applications, can help semiconductor manufacturers maintain safety, reliability and operational uptime while navigating the complex requirements of modern cleanroom processing.

➤ Every Almatec FUTUR Series component is repeatedly cleaned and assembled in ISO-class cleanrooms to ensure contamination-free performance.

Understanding the cleanroom pumping challenge

Cleanrooms in semiconductor facilities are tightly controlled environments. Even the most microscopic contaminants can destroy wafers or compromise yields. This puts extraordinary pressure on the materials and design of process equipment, including pumps.

In addition to purity, specific applications – such as solvent transfer, waste stream handling, or alcohol pumping – introduce an added layer of risk: flammability. In these cases, any electrostatic discharge or metal-on-metal contact within the pump could result in ignition. This is where the ability to provide explosion protection becomes vital.

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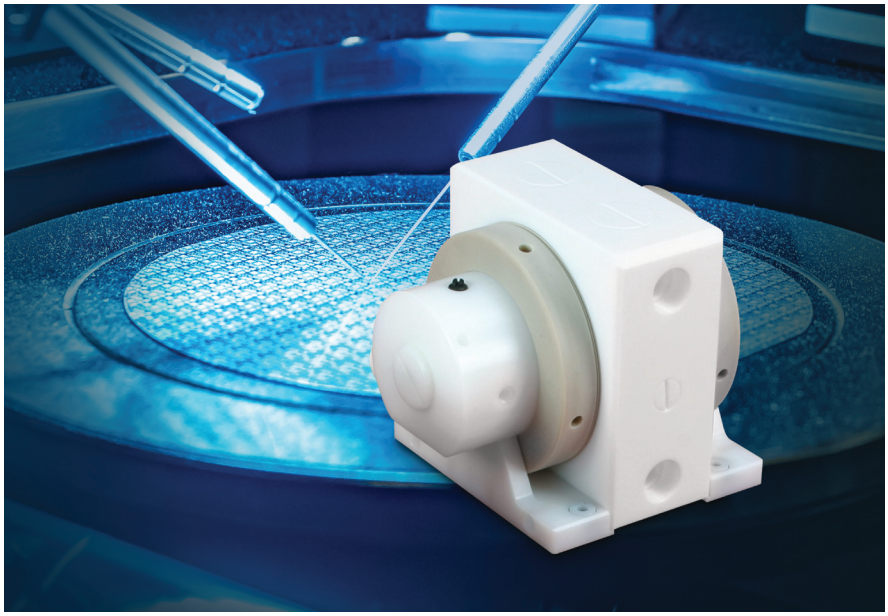
Performance without compromise

Semiconductor fabrication facilities, commonly known as fabs, are required to follow global explosion protection standards, such as ATEX (ATmosphères EXplosibles) certification, for equipment operating in potentially explosive environments. Finding pumps that can meet both the cleanroom-grade purity and explosion-proof safety standards is no easy feat – yet it's where AODD technology excels.

Moreover, the pumping systems in these settings must operate reliably under fluctuating chemical conditions and temperatures, often in confined or enclosed cabinets. Maintenance opportunities are limited, so pumps must not only be durable but also easy to inspect or service with minimal disruption. At the same time, safety cannot be compromised. This combination of factors makes it critical for semiconductor fabs to specify pump technologies that are purpose-built for the unique operational and safety demands of cleanroom environments, particularly in niche or hazardous applications.



➤ Built from high-grade, non-metallic materials, Almatec FUTUR Series pumps are engineered for ultra-pure chemical supply and circulation in semiconductor manufacturing. Designed for long-term reliability, these pumps have become a trusted standard in fabs worldwide, helping manufacturers maintain the highest levels of safety, purity and process performance.

The case for AODD pumps in semiconductor applications

AODD pumps have long been used in demanding industries due to their exceptional versatility, chemical compatibility and self-priming abilities. In semiconductor applications, AODD pumps offer a range of benefits over mechanical or centrifugal pumps:

1. **Metal-free, contamination-free operation:** Semiconductor-grade AODD pumps are often crafted entirely from high-grade plastics or PTFE-based materials. This design eliminates the risk of trace metal contamination, a crucial factor when handling ultrapure fluids or solvents in fabrication processes.

2. **Conductivity and electrostatic discharge control:** Specialized AODD pumps designed from conductive plastics, such as carbon-filled conductive ultra-high molecular weight polyethylene (UHMW-PE), enable safe fluid transfer in explosive or flammable environments. These materials allow for electrostatic dissipation while avoiding the use of metals altogether.

3. **ATEX certification:** Leading AODD pump models meet ATEX Zone 2 compliance requirements, making them suitable for solvent handling, alcohol transfer, or chemical disposal tasks in explosion-prone areas of the facility.

4. **One-piece PTFE diaphragms:** Modern AODD pump diaphragms are machined from solid PTFE for maximum durability and minimal delamination risk. These diaphragms offer a long service life and ensure that aggressive fluids don't compromise pump integrity or performance.

5. **Straight-through flow paths and minimal bends:** In some AODD designs, the liquid path is engineered for minimal bends and surfaces, reducing particle generation and improving chemical compatibility.

6. **Self-priming, low-shear and maintenance-free:** AODD pumps are self-priming and capable of dry running. They are low-shear by design, protecting sensitive fluids, and they often incorporate maintenance-free air control systems, which require no external lubrication or electronics.

7. **Cost effectiveness:** AODD pumps are often more cost-effective over the long term compared to other pump types. Their robust construction, minimal maintenance requirements and compatibility with a wide range of chemicals help reduce downtime and simplify spare parts inventory. These factors contribute to a lower total cost of ownership, making them a wise investment for fabs focused on long-term operational efficiency.

Alcohols, solvents and waste streams

While most semiconductor-grade AODD pumps are used in ultra-pure chemical loops, a specific subset of applications presents a different challenge – safely transferring potentially explosive or aggressive media in cleanroom environments.

These include:

- Alcohol transfer for cleaning and rinsing processes
- Solvent and stripper circulation in lithography and etching steps
- Chemical waste and solvent recovery systems
- Tank or cabinet venting and draining in explosive atmospheres

In many of these applications, the implementation of ATEX-compliant pumping systems is not just a safety best practice; it's a regulatory and insurance requirement. Yet, meeting these standards without compromising cleanroom compatibility can be difficult.

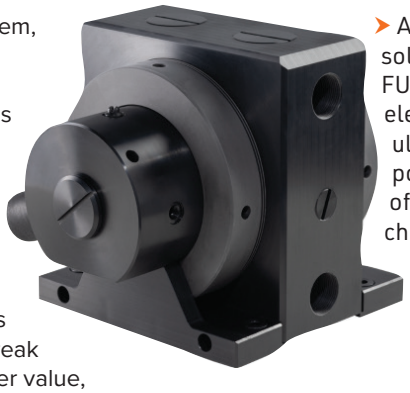
The availability of a fully non-metallic, conductive and ATEX-approved AODD

pump bridges this gap, enabling facilities to adhere to explosion protection standards without sacrificing chemical purity or uptime. FUTUR Series AODD pumps from Almatec, a product brand of PSG, a Dover company, are designed precisely for such environments.

Conductive, ATEX-certified FUTUR AODD pumps

The development of the Almatec FUTUR Series was directly driven by requests from semiconductor customers. These users wanted the proven benefits of the Almatec non-conductive FUTUR pumps, particularly the one-piece PTFE diaphragm. Still, they needed a version that could be safely deployed in ATEX-regulated environments. The result was the Almatec FUTUR: a carbon-filled pump combining cleanroom compatibility with explosion protection.

Available in different sizes, the Almatec FUTUR is one of the only pumps on the market offering the rare combination of ATEX certification, fully metal-free construction and a machined, one-piece PTFE diaphragm. This makes it particularly valuable in fab processes where contamination, sparking, or chemical degradation simply cannot be tolerated. Its conductive plastic construction eliminates the risk of static discharge without relying on any metallic components, aligning with the most stringent cleanroom safety protocols. Additionally, its straightforward installation and proven long-life design make it a reliable solution for operations that cannot afford downtime or maintenance interruptions. The Almatec PERSWING P® air control system, which requires no lubrication or maintenance, adds an extra layer of operational efficiency.



Optional accessories such as stroke counters and membrane break sensors add further value, enabling real-time monitoring and predictive maintenance capabilities that help fabs stay one step ahead of unexpected failures or costly disruptions.

As a testament to the trust that semiconductor manufacturers place in the reliability of Almatec AODD pumps, more than 400 units have already been successfully installed at companies throughout Germany's Dresden region – widely known as "Silicon Saxony." This region has emerged as Europe's leading hub for semiconductor manufacturing and microelectronics, where global players operate alongside a robust network of medium-sized companies and cutting-edge research institutes.

With its unique ecosystem of suppliers, universities and applied research centers, Dresden seamlessly blends industrial strength with scientific expertise to drive breakthroughs in chip design and production. The strong presence of Almatec in this innovation-rich environment underscores its reputation as a trusted partner for high-performance, reliable pumping technology.

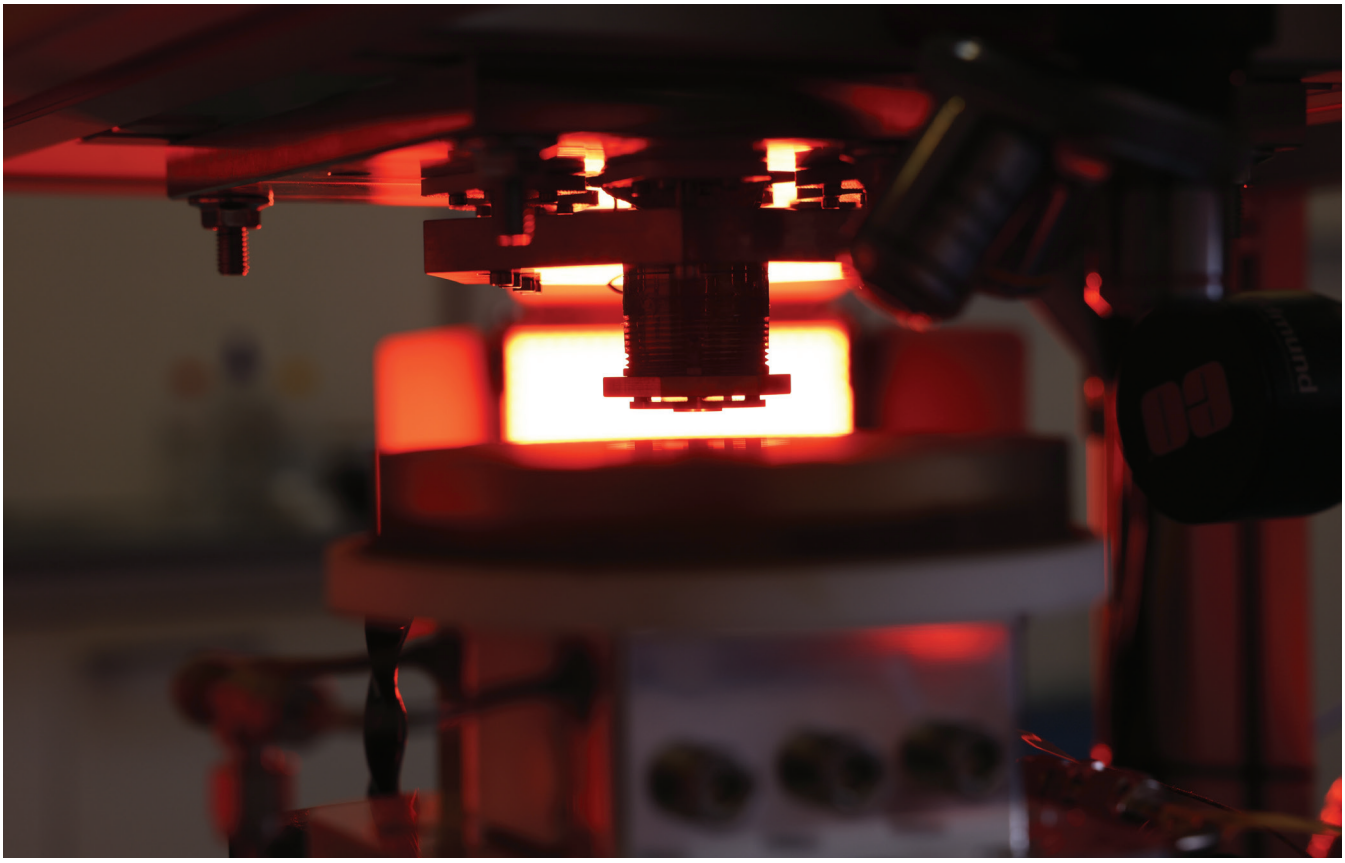
➤ Applications involving solvents, the Almatec FUTUR 100F is made from electrically conductive ultra-high molecular weight polyethylene (UHMW-PE), offering outstanding chemical resistance, abrasion resistance and conductivity.

Conclusion

In a semiconductor industry defined by precision, purity and safety, selecting the right pumping technology for niche applications is critical. AODD pumps, especially those engineered with conductive, non-metallic materials and certified to ATEX standards like Almatec FUTUR pumps, offer fabs the ability to transfer aggressive or flammable media without compromising cleanroom integrity.

As fabs strive to scale production, minimize contamination risks and comply with stringent safety standards, advanced AODD pumps are poised to become more than just a utility. They will serve as a critical enabler, driving the next generation of semiconductor manufacturing with precision and reliability.

As the industry continues to evolve, the role of versatile, safe and contamination-free pumping technologies will only grow more critical. By choosing the Almatec FUTUR today, fabs secure unmatched reliability and the confidence to meet tomorrow's technological and regulatory challenges without compromise.



Maximising advanced packaging hinges on manufacturing process optimisation

Unlocking packaging's promise will require solving upstream manufacturing process bottlenecks and rethinking global semiconductor supply chain strategies.

BY DR. MAKSYM PLAKHOTNYUK, CEO AND FOUNDER, ATLANT 3D

AI CHIP revenue is soaring, driven by breakthrough models and unprecedented demand across the GPU and ASIC segments.

This rapid growth benefits semiconductor manufacturers, as each new AI generation requires ever-larger quantities of leading-edge silicon to deliver improved cost, performance, and efficiency per operation.

To keep pace with this demand – and transcend the physical limits of classic transistor scaling—advanced packaging technologies, especially 3D stacking and chiplet architectures, have become a vital frontier. These techniques integrate multiple chips and components (such as CPUs, GPUs, memory, and high-speed interconnects) in a single heterogeneous package.

By minimizing the physical distance between elements, advanced packaging improves data transmission rates and energy efficiency, a key factor in the escalating technological rivalry between the U.S. and China.

Leading foundries and outsourced semiconductor assembly and test (OSAT) players are responding. Notably, TSMC has announced a $100 billion U.S. investment plan – including a next-generation advanced packaging facility in Arizona – while Intel recently expanded its advanced packaging operations in New Mexico, aiming for domestic supply chain resilience.

Such moves are further catalyzed by policy incentives and tariff structures designed to onshore semiconductor manufacturing capacity.

Despite these advances, challenges remain. Advanced packaging is highly complex, involving tightly integrated stacks of diverse materials and structures – such as interposers, redistribution layers (RDLs), and multiple active and passive chips.

Conventional thin-film approaches like atomic layer deposition (ALD)

offer atomic-scale precision but generally lack the throughput or process simplicity required for large-scale packaging. Direct-write additive manufacturing techniques like DALP are emerging to address some of these bottlenecks, enabling more flexible and rapid construction of advanced packages with lower material waste, fewer processing steps and the same precision as ALD.

Meanwhile, the infrastructure that houses AI chips must evolve. Next-generation AI accelerators and advanced packages require new datacenter designs – with upgraded power delivery, cutting-edge cooling, and higher rack densities – to avoid bottlenecks that would offset performance and sustainability gains from packaging improvements.

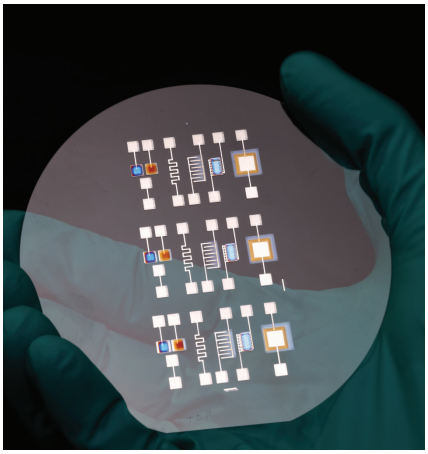
While advanced packaging reduces the energy needed for interconnects, the aggregate power draw for hyperscale AI datacenters continues to rise in line with massive computational demand.

Crucially, high-volume advanced packaging capacity in the U.S. is not expected to be available before mid-2027, and U.S.-designed chips like NVIDIA's Blackwell family continue to be routed to Taiwan for packaging.

This gap creates opportunities for other countries to accelerate local industry development, and exposes U.S. manufacturers to additional costs and potential tariffs if products must be re-imported after overseas packaging – potentially eroding domestic cost advantages.

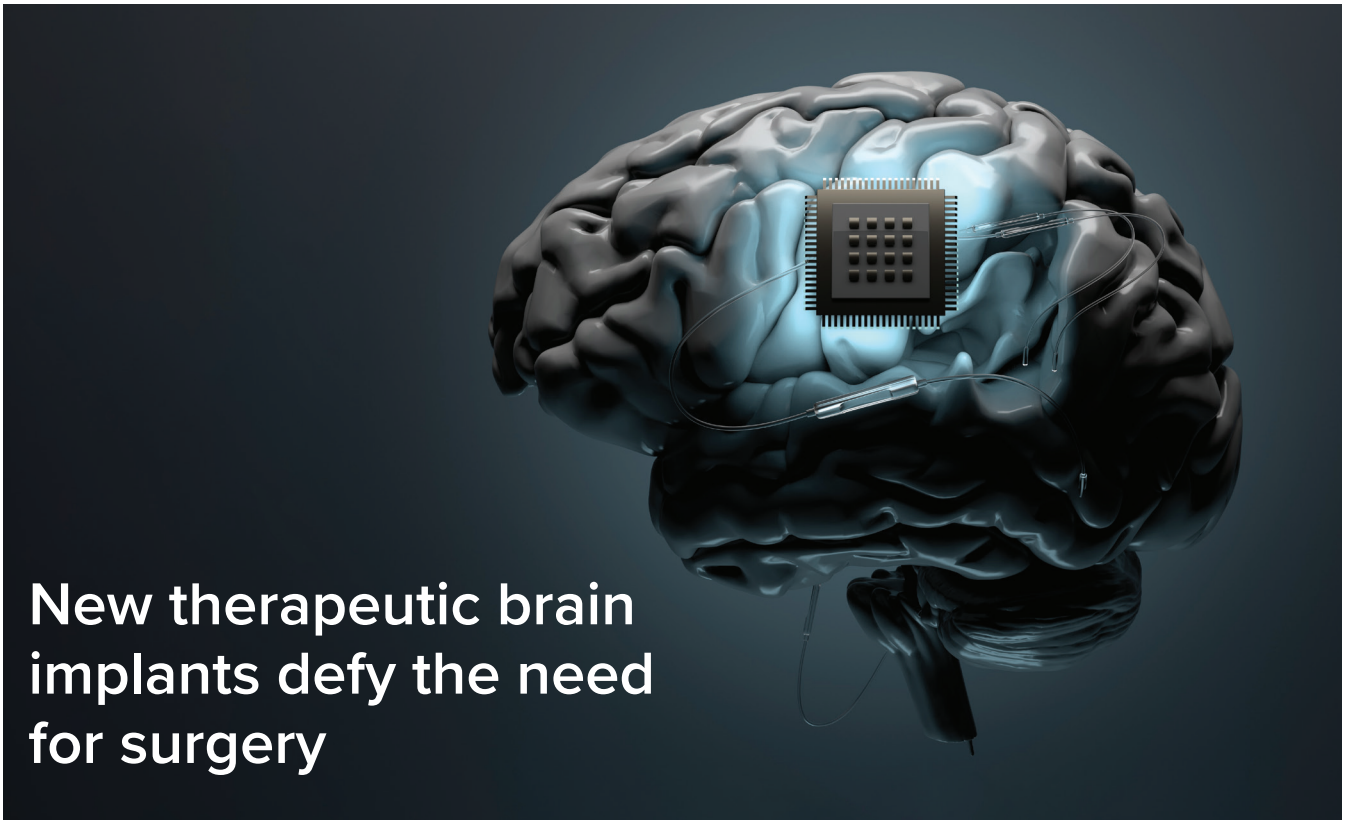
Industry consensus is forming around the idea that advanced packaging may be as critical as transistor innovation itself for the future of AI and semiconductors. As NVIDIA CEO Jensen Huang noted,

"To meet [AI's] demand, advanced packaging has become as critical as transistor design in delivering the efficiency and power our customers require." But fully unlocking packaging's promise will require solving upstream



manufacturing process bottlenecks and rethinking global semiconductor supply chain strategies.

Advanced packaging holds the potential to shift power balances not just within AI, but also in fields such as defense, biomedical engineering, and energy, provided nations and firms can adapt their supply chains, infrastructure, and manufacturing processes for a new era of integrated, high-performance computing.



New therapeutic brain implants defy the need for surgery

MIT researchers created microscopic wireless electronic devices that travel through blood and implant in target brain regions, where they provide electrical stimulation.

BY ADAM ZEWE, MIT NEWS OFFICE

WHAT IF clinicians could place tiny electronic chips in the brain that electrically stimulate a precise target, through a simple injection in the arm? This may someday help treat deadly or debilitating brain diseases, while eliminating surgery-related risks and costs.

MIT researchers have taken a major step toward making this scenario a reality. They developed microscopic, wireless bioelectronics that could travel through the body's circulatory system and autonomously self-implant in a target region of the brain, where they would provide focused treatment.

In a study on mice, the researchers show that after injection, these miniscule implants can identify and travel to a specific brain region without the need for human guidance. Once there, they can be wirelessly powered to provide electrical stimulation to the precise area. Such stimulation, known as neuromodulation, has shown promise as a way to treat brain tumors and diseases like Alzheimer's and multiple sclerosis.

Moreover, because the electronic devices are integrated with living, biological cells before being injected, they are not attacked by the body's immune system and can cross the blood-brain barrier while leaving it intact. This maintains the barrier's crucial protection of the brain.

The researchers demonstrated the use of this technology, which they call "circulatronics," to target brain inflammation, a major factor in the progression of many neurological diseases. They show that the implants can provide localized neuromodulation deep inside the brain achieving high precision, to within several microns around the target area.

In addition, the biocompatible implants do not damage surrounding neurons. While brain implants usually require hundreds of thousands of dollars in medical costs and risky surgical procedures, circulatronics technology holds the potential to make therapeutic brain implants accessible to all by eliminating the need for surgery, says Deblina Sarkar, the AT&T Career Development Associate Professor in the MIT Media Lab and MIT Center for Neurobiological Engineering, head of the Nano-Cybernetic Biotrek Lab, and senior author of a study on the work.

She is joined on the paper by lead author Shubham Yadav, an MIT graduate student; as well as others at MIT, Wellesley College, and Harvard University. The research appears today in Nature Biotechnology.

Hybrid implants

The team has been working on circulatronics for more than six years. The electronic devices, each about one-billionth the length of a grain of rice, are composed of organic semiconducting

polymer layers sandwiched between metallic layers to create an electronic heterostructure.

They are fabricated using CMOS-compatible processes in the MIT.nano facilities, and then integrated with living cells to create cell-electronics hybrids. To do this, the researchers lift the devices off the silicon wafer on which they are fabricated, so they are free-floating in a solution.

"The electronics worked perfectly when they were attached to the substrate, but when we originally lifted them off, they didn't work anymore. Solving that challenge took us more than a year," Sarkar says.

Key to their operation is the high wireless power conversion efficiency of the tiny electronics. This enables the devices to work deep inside the brain and still harness enough energy for neuromodulation.

The researchers use a chemical reaction to bond the electronic devices to cells. In the new study, they fused the electronics with a type of immune cell called monocytes, which target areas of inflammation in the body. They also applied a fluorescent dye, allowing them to trace the devices as they crossed the intact blood-brain barrier and self-implanted in the target brain region.

While they explored brain inflammation in this study, the researchers hope to use different cell types and engineer the cells to target specific regions of the brain.

"Our cell-electronics hybrid fuses the versatility of electronics with the biological transport and biochemical sensing prowess of living cells," Sarkar says. "The living cells camouflage the electronics so that they aren't attacked by the body's immune system and they can travel seamlessly through the bloodstream. This also enables them to squeeze through the intact blood-brain barrier without the need to invasively open it."

Over the course of about four years, the team tried many methods to autonomously and noninvasively cross the blood-brain barrier before they perfected this cellular integration technique.

In addition, because the circulatronics devices are so tiny, they offer much higher precision than conventional electrodes. They can self-implant, leading to millions of microscopic stimulation sites that take the exact shape of the target region.

Their small size also enables the biocompatible devices to live alongside neurons without causing harmful effects. Through a series of biocompatibility tests, the researchers found that circulatronics can safely integrate among neurons without impacting the brain processes behind cognition or motion.

After the devices have self-implanted in the target region, a clinician or researcher uses an external transmitter to provide electromagnetic waves, in the form of near-infrared light, that power the technology and enable electrical stimulation of the neurons.

Targeting deadly diseases

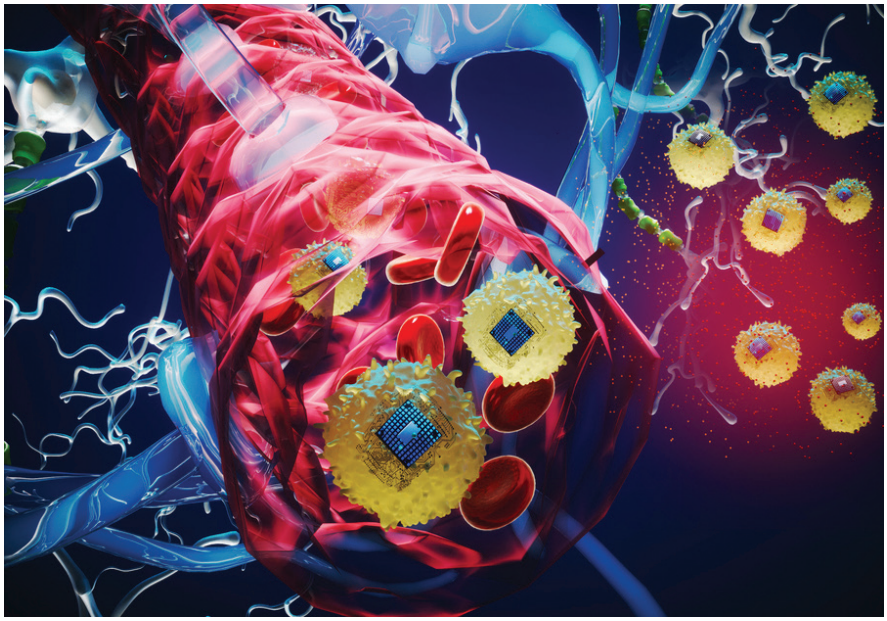
The Sarkar lab is currently working on developing their technology to treat multiple diseases including brain cancer, Alzheimer's disease, and chronic pain.

The tiny size and self-implantation capabilities of circulatronics devices could make them well-suited to treat brain cancers such as glioblastoma that cause tumors at multiple locations, some of which may be too small to identify with imaging techniques. They may also provide new avenues for treating especially deadly cancers like diffuse intrinsic pontine glioma, an aggressive type of tumor found in the brain stem that usually cannot be surgically removed.

"This is a platform technology and may be employed to treat multiple brain diseases and mental illnesses," Sarkar says. "Also, this technology is not just confined to the brain but could also be extended to other parts of the body in future."

The researchers hope to move the technology into clinical trials within three years through the recently launched startup Cahira Technologies. They are also exploring integration of additional nanoelectronic circuits into their devices to enable functionalities including sensing, feedback based on-chip data analysis, and capabilities such as creating synthetic electronic neurons.

"Our tiny electronic devices seamlessly integrate with the neurons and co-live and co-exist with the brain cells creating a unique brain-computer symbiosis. We are working dedicatedly to employ this technology for treating neural diseases, where drugs or standard therapies fail, for alleviating human suffering and envision a future where humans could transcend beyond diseases and biological limitations," says Sarkar.



Credit: Courtesy of the researchers

➤ "The living cells camouflage the electronics so that they aren't attacked by the body's immune system and they can travel seamlessly through the bloodstream," Deblina Sarkar says.

Inspiring innovations address key industry challenges

Imec has been busy in recent weeks, unveiling a tool for AI data centre design and optimization and presenting research results, including mitigating thermal bottleneck in 3D HBM-on-GPU architectures using a system-technology co-optimization approach, demonstrating the first wafer-scale fabrication of solid-state nanopores using EUV lithography, advancing 2D-material based device technology beyond state of the art and successfully integrating colloidal quantum dot photodiodes (QDPDs) on metasurfaces developed on 300mm CMOS wafers.

AT THE RECENT Super Computing 2025 event, the premier international conference and exhibition for high performance computing (HPC), imec launched imec.kelis, a cutting-edge analytical performance modeling tool designed to revolutionize the design and optimization of AI datacenters. Early adopters are already experimenting with the tool, signaling strong market interest.

The AI datacenter landscape is undergoing rapid transformation. As workloads scale to trillions of parameters and energy demands surge, system architects face mounting pressure to balance performance with sustainability and cost. Traditional simulation methods are often slow, opaque, or too narrow in scope. Imec.kelis addresses this gap by offering a fast, transparent, and validated modeling framework that enables informed decision-making across the full stack—from chip to datacenter.

It empowers teams to explore architectural trade-offs, optimize resource allocation, make informed decisions, and accelerate innovation in a field where time-to-insight is critical. Imec.kelis provides an end-to-end framework for evaluating system performance across compute, communication, and memory subsystems. It is tailored for large language model (LLM) training and inference workloads, offering fast, accurate, and generalizable predictions validated on industry-standard platforms such as Nvidia A100 and H100. The tool builds on imec's proven track record in analytical performance modeling for high-performance computing (HPC) and artificial intelligence (AI). It leverages imec's system-level modeling and performance analysis for compute, communication, and memory subsystems, especially in the context of large-scale AI datacenters and large language model (LLM) workloads, imec's hardware-software-codesign expertise, and semiconductor technology roadmap.


imec

"Imec.kelis is more than a simulator – it's a strategic enabler for the next generation of AI infrastructure," said Axel Nackaerts, imec's System Scaling lead. "By combining hardware-software-codesign, we empower system architects to make informed decisions at datacenter scale."

Key Features:

- LLM task-graph analyzer and parallelism mapper

- Hierarchical roofline model and topology-aware communication library
- Interactive dashboard for real-time design space exploration
- Validated within 12% error margin for large-scale LLM

"In a test case, we used imec.kelis to compare the performance (defined as training time for GPT3), for different GPU architectures and scaling nodes, at plotted performance against cost, showcasing the flexibility of the tool for various purposes, such as architecture exploration, future technology projection, and co-optimization. Our results show that imec.kelis enables careful validation of performance and helps identify key insights for architecture exploration and future technology projection." stated Nackaerts.

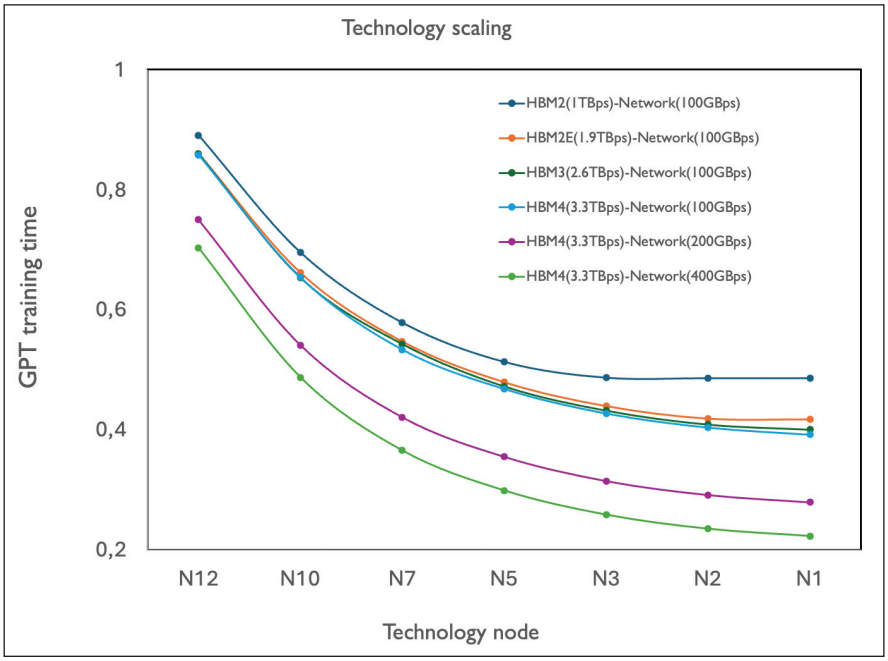
Imec.kelis v1.0 will be available for licensing starting Q1 2026. The tool has already attracted early adopters, signaling strong market interest.

NanoIC adds advanced SRAM memory macros to its N2 pathfinding PDK

Meanwhile, at SEMICON Europe, the NanoIC pilot line, a European initiative coordinated by imec and dedicated to accelerating innovation in chip technologies beyond 2nm, announced the release of the N2 P-PDK v1.0, an important update of its N2 Pathfinding Process Design Kit (P-PDK). This new version introduces several new features, including a library of 29 SRAM memory macros, allowing designers to explore and benchmark system-on-chip (SoC) designs with frontside and backside power routing. By adding the SRAM macros in the design options, the N2 P-PDK v1.0 marks an important milestone in enabling research, learning, and design exploration on advanced and future nodes.

Towards next-generation SoC designs

As chip technologies scale beyond 2nm, the ability to explore full System-on-Chip (SoC) architectures with novel technology enablers becomes increasingly important. SoCs, integrating logic, memory, and interconnect capabilities into a single chip, are the backbone of a wide variety of digital applications, from smartphones and AI accelerators to automotive controllers. However, early-stage SoC design exploration is often constrained by limited access to complete and realistic design kits that include advanced or future technology scaling boosters such as power delivery networks. This gap makes it difficult for designers to validate architectural concepts, experiment with emerging technologies, or to train the next generation of chip designers on advanced nodes.



➤ imec.kelis

NanoIC's low-barrier N2 P-PDK v1.0 aims to bridge this gap, offering instant access to a wide variety of new design features, including a portfolio of 29 ready-to-use SRAM macros with both frontside and backside power routing configurations.

This dual configuration, offered for the first time in a pathfinding PDK, enables designers to experiment with and optimize memory integration within realistic, advanced power networks.

As a result, NanoIC's N2 P-PDK v1.0 now provides the building blocks of a complete SoC as well as the architectural context to explore how those blocks interact within realistic power networks. It enables users to move beyond simple logic design and explore and validate full SoC systems that reflect the challenges and opportunities of next-generation semiconductor design.

Lowering barriers for learning and exploration

By making these advanced features freely available to academic researchers, startups, and design teams, NanoIC significantly lowers the barriers to innovation, empowering the development of next-generation applications, and strengthening Europe's position in the global semiconductor landscape.

"This v1.0 version of our N2 P-PDK enables designers to evaluate the impact of new technology features and integration options on their designs before they exist in foundry offerings. It provides a unique environment to connect technology pathfinding with practical design enablement, ensuring that breakthroughs in device research translate into system-level advances.", Marie Garcia Bardon, Department Director at imec and work package leader within the NanoIC pilot line, summarizes.

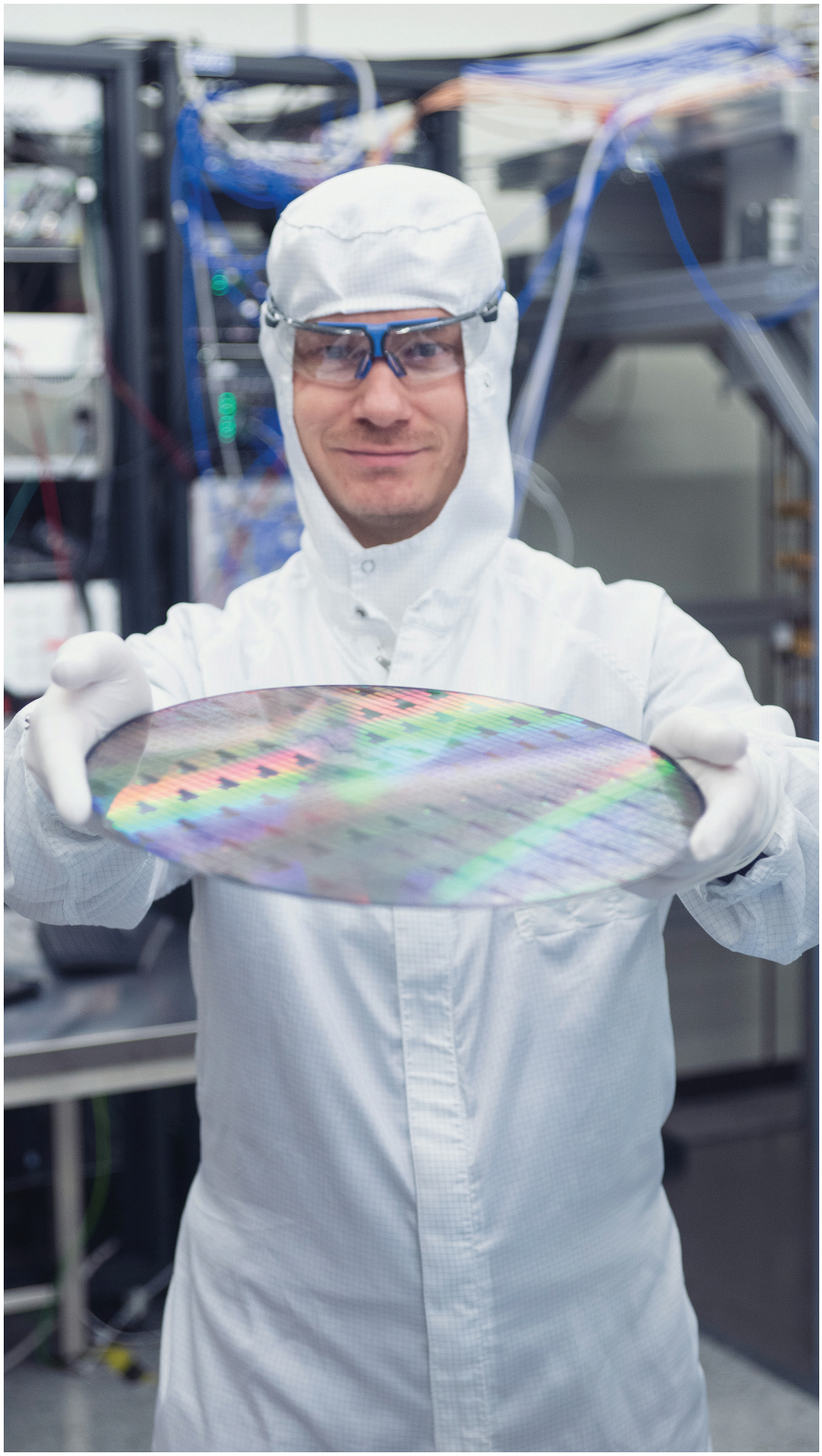
Building on the learnings from the previous N2 P-PDK, this release lays the groundwork for future PDK iterations, launching additional advanced logic, memory, and interconnect PDKs in the coming years. The roadmap includes future versions of the N2 P-PDK, as well as upcoming A14 and A7 logic P-PDKs, eDRAM and SOT memory PDKs, and advanced interconnect solutions (RDL, hybrid bonding, interposers),

empowering innovation across the full spectrum of next-generation chip technologies.

To support designers in exploring the full capabilities of the N2 P-PDK v1.0, a dedicated workshop will be organized on March 25-26, 2026. This session will offer a theoretical framework, followed by hands-on training sessions, using two different EDA tools: Cadence and Synopsys. Participants will gain insights into the SRAM memory macros, updated design rules, and system-level integration strategies. More details and registration will be made available via the NanoIC website.

Mitigating thermal bottleneck in 3D HBM-on-GPU architectures

At the 2025 IEEE International Electron Devices Meeting (IEDM), imec presented that is believed to be the first thermal system-technology co-optimization (STCO) study of 3D HBM-on-GPU (high-bandwidth memory on graphical processing unit), a promising compute architecture for next-gen AI applications. By combining technology and system-level mitigation strategies, peak GPU temperatures could be reduced from 140.7°C to 70.8°C under realistic AI training workloads – on par with current 2.5D integration options. The result demonstrates the strength of combining cross-layer optimization (i.e., co-optimizing the knobs at all the different abstraction layers) with broad technological expertise, a combination that is unique to imec.



Integrating high bandwidth memory (HBM) stacks directly on top of graphical processing units (GPUs) offers an attractive approach for building next-gen compute architectures for data-intensive AI workloads. This 3D HBM-on-GPU promises a huge leap forward in compute density (with four GPUs per package), memory per GPU, and GPU-memory bandwidth compared to current 2.5D integration options where HBM stacks are placed around (one or two) GPUs on a silicon interposer. However, the aggressive 3D integration approach is prone to thermal issues because of higher local power density and vertical thermal resistance.

At 2025 IEDM, imec presented the first comprehensive thermal simulation study of 3D HBM-on-GPU integration that not only identifies thermal bottlenecks but also proposes strategies to increase the architecture's thermal feasibility. Imec researchers show how co-optimizing technology and system-level thermal mitigation approaches can reduce peak GPU temperatures from 141.7°C to 70.8°C under realistic AI training workloads.

The model assumes four HBM stacks – each consisting of twelve hybrid-bonded DRAM dies – placed directly on top of a GPU using microbumps. Cooling is provided on top of the HBMs. Power maps derived from industry relevant power profiles are applied to identify local hotspots and compare them to a 2.5D baseline. Without thermal mitigation strategies, the 3D model yields a peak GPU temperature of 141.7°C – far too high

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for GPU and HBM operation – while the 2.5D integration benchmark peaks at a workable 69.1°C under the same cooling conditions. We used these data as a starting point to evaluate the joint impact of technology and system-level thermal mitigation strategies. Technology-level strategies include, among others, HBM stack merging and thermal silicon optimization. On the system-level side, we assessed the impact of double-sided cooling as well as GPU frequency scaling.

James Myers, System Technology Program Director at imec: "Halving the GPU core frequency brought the peak temperature from 120°C to below 100°C, achieving a key target for the memory operation. Although this step comes with a 28% workload penalty (i.e., a slowdown of AI training steps), the overall package outperforms the 2.5D baseline thanks to a higher throughput density offered by the 3D configuration. We are currently using this approach to study other GPU/HBM configurations (e.g., placing GPUs on top of HBMs), anticipating future thermal constraints."

Julien Ryckaert, Vice President Logic Technologies at imec: "This is also the first time that we demonstrate the capabilities of imec's cross-technology co-optimization (XTCO) program in building more thermally robust compute systems. XTCO was launched in 2025 to efficiently align imec's technology roadmaps with key industry system scaling challenges and is built on four critical system level pillars: compute density, power delivery, thermal, and memory density and bandwidth. It combines our STCO/DTCO mindsets with imec's broad technology expertise – a unique combination that is of great value in addressing the growth and diversification of compute system demands. We invite companies from within the entire semiconductor ecosystem, including fabless and system companies, to join our XTCO program and collaboratively resolve critical system scaling bottlenecks."

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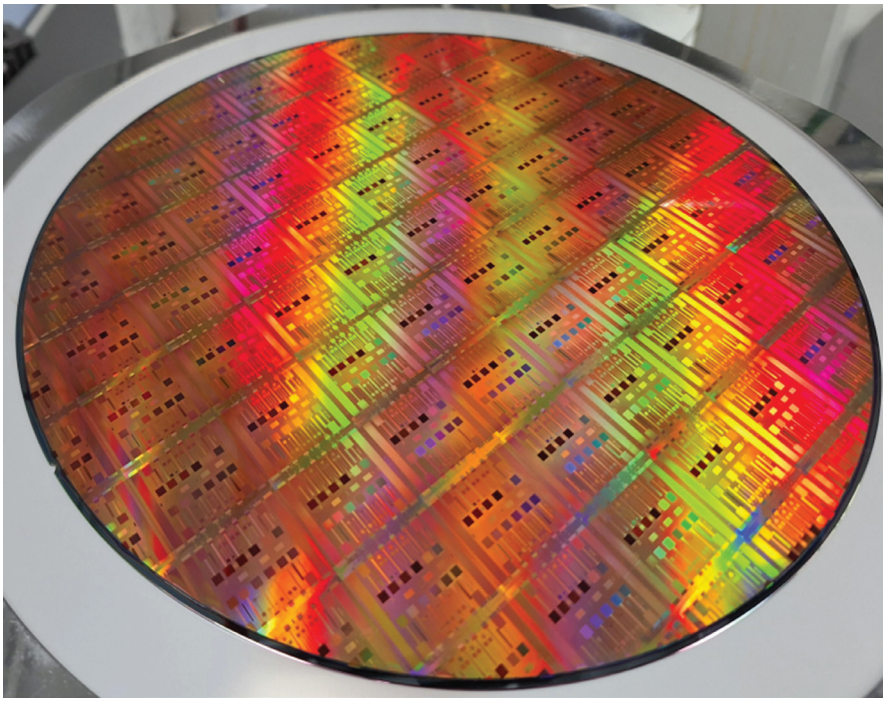
The first wafer-scale fabrication of solid-state nanopores using EUV lithography

At IEDM 2025, imec also presented the first successful wafer-scale fabrication of solid-state nanopores using extreme ultraviolet (EUV) lithography. Solid-state nanopores are emerging as powerful tools for molecular sensing but haven't been commercialized yet. This proof of concept is a crucial step towards their cost-effective (mass) production.



Solid-state nanopores are tiny holes - just a few nanometers wide - etched into Silicon Nitride membranes. When immersed in fluid and connected to electrodes, they allow individual molecules to pass through, generating electrical signals that can be analyzed in real time. Because the pore size can be easily adjusted, they offer a wide range of applications, from virus identification to DNA and protein analysis. This label-free, single-molecule detection method is key to next-generation diagnostics, proteomics, genomics, and even molecular data storage applications.

Biological nanopores, on the other hand, formed by proteins in lipid membranes, have enabled commercial sequencing platforms, but they are limited by stability and integration challenges. Solid-state nanopores overcome these limitations with robustness, tunability, and compatibility with semiconductor manufacturing, making them ideal for scalable, high-throughput sensing. But achieving nanometer-level precision and uniformity in solid-state pores across large areas remains a challenge.

Current fabrication techniques are often slow and limited to the lab, delaying their widespread use for sensing applications.

In a new paper presented at IEDM 2025, imec reports successful fabrication of highly uniform nanopores with diameters down to ~10nm across full 300mm wafers.

The team combined EUV lithography with a spacer-based etch technique to achieve nanometer-level precision and reproducibility - two long-standing challenges in nanopore technology.

The nanopores were embedded in silicon nitride membranes and electrically characterized in aqueous environments. Translocation experiments with DNA fragments also confirmed high signal-to-noise ratios and excellent wetting behavior, validating the nanopores' sensing performance with biological material.

"Imec is uniquely positioned to make this leap. We can apply EUV lithography - traditionally reserved for memory and logic - to life sciences. By leveraging our lithography infrastructure, we've shown that solid-state nanopores can be fabricated at scale with the precision needed for molecular sensing," said Ashesh Ray Chaudhuri, first author and R&D project manager at imec. "This opens the door to high-throughput biosensor arrays for healthcare and beyond."

Looking ahead, this feat can enable rapid diagnostics, personalized medicine, and molecular fingerprinting. Building upon the EUV nanopore advancements, imec is currently developing a modular readout system with scalable fluidics as a platform for application relevant chemistry development. The team invites life science tool developers to use this platform to test their concepts and requirements.

At the 2026 IEEE International Solid-State Circuits Conference (ISSCC), the paper "A 256-Channel Event-Driven Readout for Solid-State Nanopore Single-Molecule Sensing with 193 pArms Noise in a 1 MHz Bandwidth" was presented, showcasing a proof-of-concept ASIC readout developed by imec, to support next-generation custom nanopores.

Advancing 2D-material based device technology beyond state of the art

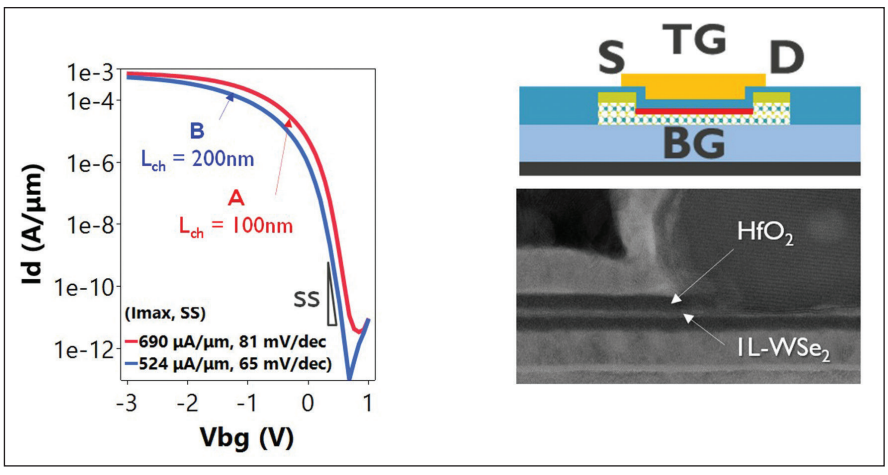
Again at the IEDM, imec also presented breakthrough performance of p-type FETs with monolayer WSe_2 channels, and improved fab-compatible modules for source/drain contact formation and gate stack integration. These results, achieved through collaborations with leading semiconductor manufacturers, mark a significant advance for 2D-material based technology, which is considered a promising long-term option for extending the logic technology roadmap.

Replacing Si conduction channels with atomically thin layers made of 2D transition metal dichalcogenides (MX_2) promises to enable ultimate gate and channel length scaling, while maintaining good electrostatic channel control and high carrier mobility. Crucial milestones to be achieved include high-quality 2D-material layer deposition, gate stack integration, low-resistance source/drain contact formation, and 300mm fab integration. Also, while most efforts focus on improving n-type devices (with channels made of WS_2 or MoS_2), more fundamental work is needed on *p*-type devices, which require different channel materials (such as WSe_2).

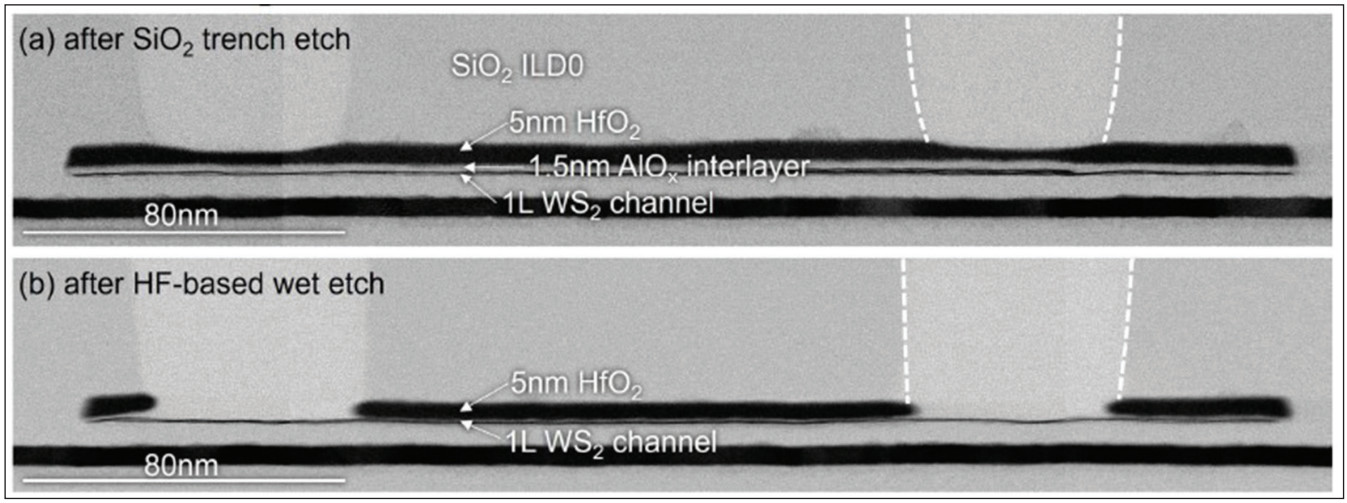
Gouri Sankar Kar, VP R&D compute and memory device technologies at imec: "At 2025 IEDM, we show in two separate presentations how in-depth collaborations with leading semiconductor manufacturers within imec's core CMOS Industrial Affiliation Program (IIAP) have enabled breakthroughs in the performance of 2D-material based devices. In both partnerships, combining high-quality 2D material layers provided by the manufacturer with imec's optimized contact and gate modules played a key role in pushing the technology beyond state of the art."

"Depositing the top-gate HfO_2 dielectric on top of a MX_2 channel requires an additional seed layer to support HfO_2 nucleation and growth", explains Gouri Sankar Kar. "For nFETs, this is solved by creating an AlO_x interfacial layer, but this approach is challenging for pFETs due to the different characteristics of the WSe_2 channel material as compared to its n-type counterparts. In partnership with TSMC, we started with a synthetic bilayer of WSe_2, which was formed by subsequently transferring two high-quality WSe_2 monolayers from TSMC on our substrates. We then oxidized the top WSe_2 monolayer, converting it into an interfacial layer that successfully supported the deposition of the HfO_2 gate oxide. This fab-compatible lab-based integration approach resulted in record performance of our dual-gated pFETs."

Another presentation highlights the collaboration between imec and Intel in developing 300mm manufacturable modules for source/drain contacts and gate stack integration, for n-type (WS_2 and MoS_2) and p-type (WSe_2) 2D-FETs. "The key innovation consists in applying a selective oxide etch process on Intel's high-quality 2D material layers, that were capped with an interfacial AlOx layer, a HfO_2 layer and a SiO_2 layer", Gouri Sankar Kar explains. "The oxide etch process allowed the formation of fab-compatible damascene-style top contacts – a world first. In addition, during the vertical contact etch process, the interfacial AlO_x layer was simultaneously etched laterally, removing AlOx from the channel region.



➤ Figure 1: Cross section and transfer curves of WSe_2 devices.



➤ Figure 2: Selective etch process resulting in AlOx interlayer lateral removal

This significantly lowered the top gate's EOT benefitting the gate's transfer characteristics."

This research was funded by the imec IIAP Exploratory Logic program, the 2D-PL pilot line project through Horizon Europe (101189797) and Horizon 2020 (952792) grant agreements.

Overcoming the cost and complexity barriers of traditional SWIR sensors

Finally at IEDM 2025, imec successfully demonstrated the integration of colloidal quantum dot photodiodes (QDPDs) on metasurfaces developed on its 300 mm CMOS pilot line. This pioneering approach enables a scalable platform for the development of compact, miniaturized shortwave infrared (SWIR) spectral sensors, setting a new standard for cost-effective and high-resolution spectral imaging solutions.

Unlocking new possibilities in SWIR sensing

Short-wave infrared (SWIR) sensors offer unique capabilities. By detecting wavelengths beyond the visible spectrum, they can reveal contrasts and features invisible to the human eye and can therefore see through certain materials such as plastics or fabrics, or challenging conditions like haze and smoke. Conventional SWIR sensors remain, however, expensive, bulky, and challenging to manufacture, restricting their use to niche applications. Quantum dot (QD) image sensors, a new class of SWIR sensors, offer a promising alternative, combining lower cost with higher resolution. So far, however, they have operated in broadband rather than in spectral mode.

Imec addresses this challenge by successfully cointegrating colloidal quantum dot photodiodes (QDPDs) with metasurfaces developed on its 300 mm CMOS pilot line. Quantum dots are nanoscale semiconductors that can be tuned to absorb specific infrared wavelengths, while metasurfaces are nano-patterned ultra-thin layers that precisely control how light interacts with the sensor. By combining these elements in a CMOS-compatible process, imec has created a scalable platform for miniaturized SWIR spectral detectors, delivering a compact, high-resolution sensor architecture that can be manufactured using standard CMOS processes.

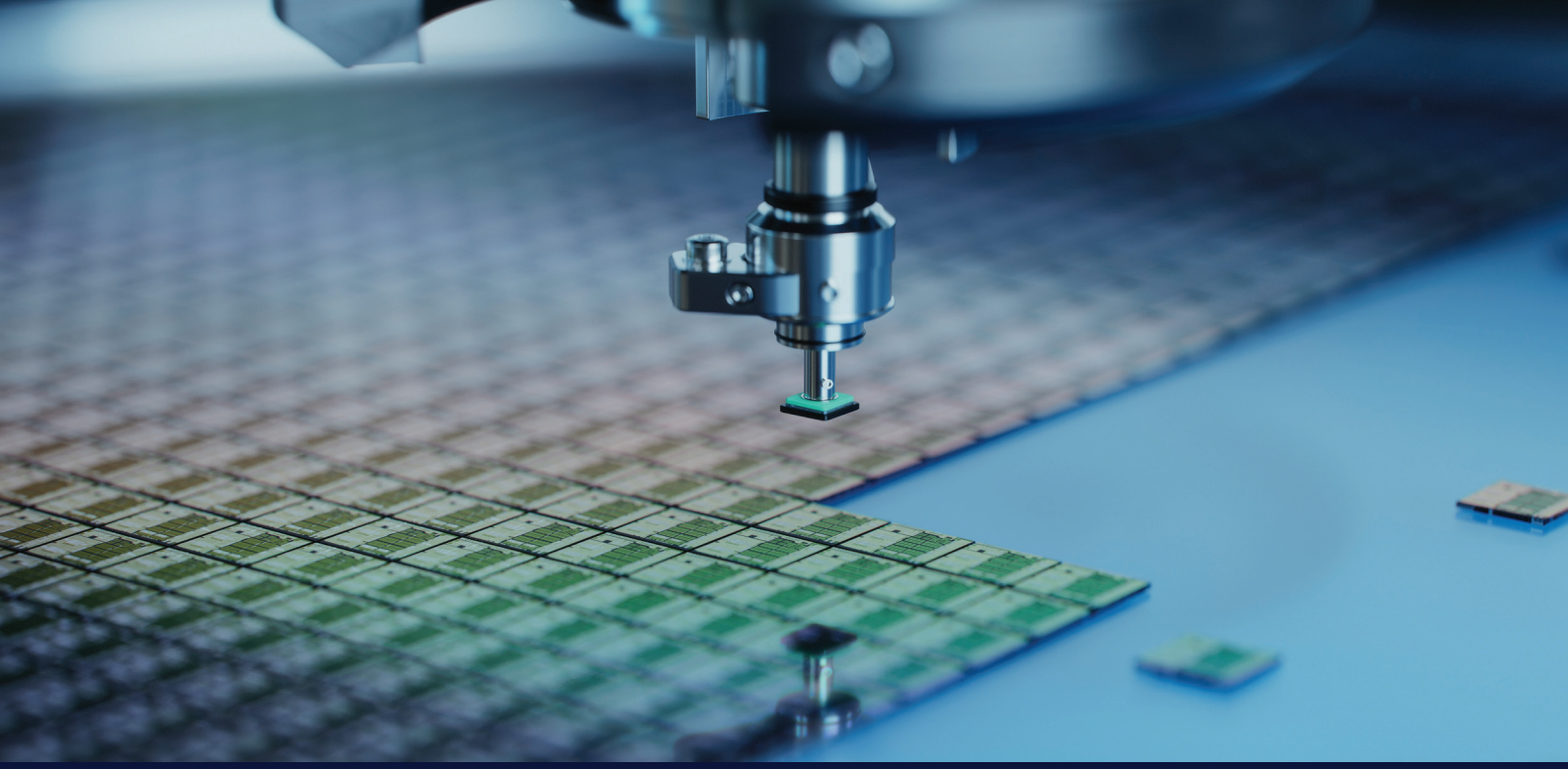
"What particularly sets this technology apart is its scalability," says Vladimir Pejovic, R&D project lead at imec. "Traditional quantum dot image sensors require redesigning complex photodiode layers for every wavelength, which makes adjustments to each application's spectrum complex and costly. Our approach shifts that complexity to the CMOS level, using metasurfaces to tune spectral response instead of altering the photodiode stack. This opens the door to easily customizable high-resolution spectral SWIR sensors and paves the way for new features in areas such as security, agriculture, automotive, aerospace, and beyond."

> Replacing Si conduction channels with atomically thin layers made of 2D transition metal dichalcogenides (MX_2) promises to enable ultimate gate and channel length scaling

Accelerating innovation through collaboration

This breakthrough is the result of a multidisciplinary effort, uniting imec's expertise in quantum dot image sensors, flat optics (metasurfaces), and spectral imaging. The next step is to scale this technology from proof of concept to low volume, and ultimately, full-scale manufacturing. To accelerate this transition, imec invites partners to collaborate.

"Our ambition is to turn this breakthrough into an industry-ready platform," Pawel Malinowski, imec portfolio manager, explains. "We want to work with partners to develop custom image sensors and integrated devices, demonstrating this technology in real-world applications. By combining imec's spectral expertise, quantum dot know-how, and advanced CMOS process capabilities with specific application domains, we aim to accelerate innovation and bring next-generation SWIR sensors from proof-of-concept to full-scale manufacturing. Imec therefore welcomes collaboration with partners to help shape the future of sensing and imaging together."



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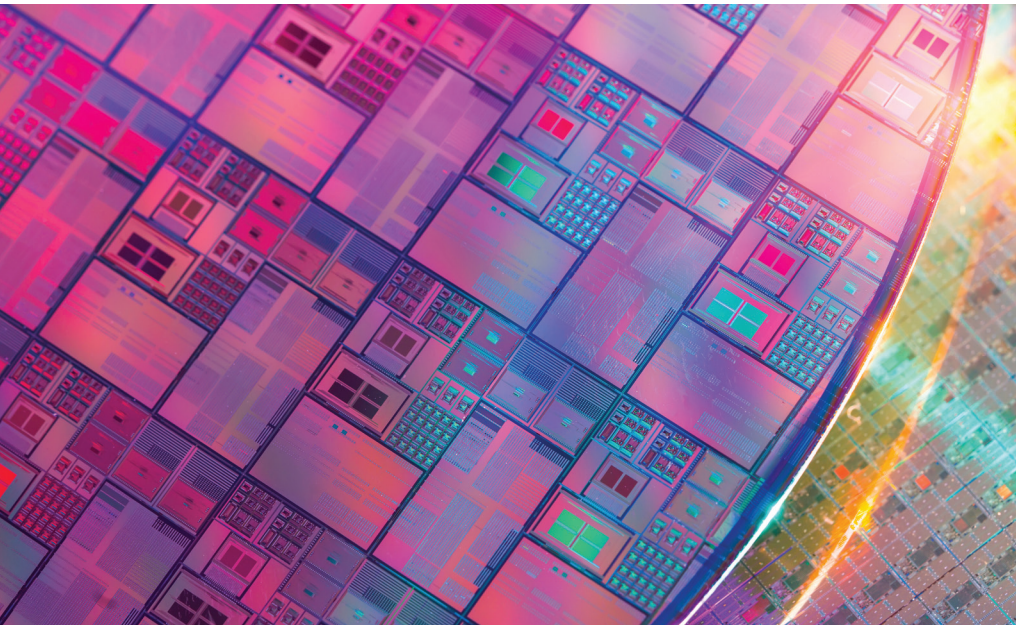
The secrets behind SCREEN's semiconductor success

Martin Hollfelder, VP for Service and Installation/Qualification and Technology at SCREEN SPE Germany, discusses the company's long track record in the semiconductor industry, evolving from its Japanese roots into a global supplier of equipment for wet cleaning/etching, lithography coat/develop, thermal annealing, inspection, metrology and advanced packaging applications. SCREEN has won a deserved reputation for both technology innovation and equipment reliability and Martin shares his excitement as to the challenges and opportunities facing the semiconductor industry into the future.

WHEN a company's history stretches back more than 150 years, its longevity alone tells a story. But in the case of SCREEN, the Japan-headquartered global equipment manufacturer, the story is less about endurance and more about an unbroken chain of reinvention.

From its origins in 1868 as a Kyoto printing venture founded by artist Ichida Yasushi, the company that would eventually evolve into today's SCREEN Semiconductor Solutions has repeatedly transformed itself to meet new markets and emerging technology waves. In doing so, it has become one of the semiconductor industry's most quietly influential powerhouses - an equipment supplier known worldwide for its innovation, precision engineering, and a reputation for reliability that chipmakers consider indispensable.

Today SCREEN stands as the global market leader in wet cleaning and wet etching systems, complemented by a deep portfolio of lithography coat/develop tools, annealing platforms, advanced packaging solutions, inspection and metrology systems. Its significance within the wider SCREEN Holdings Group is unmistakable: more than 80 percent of the group's revenue flows from semiconductor equipment. And yet, despite its scale, SCREEN often communicates with a sense of humility and technical focus rather than self-promotion.



To explore the company's evolution and its role in powering the next generation of semiconductor breakthroughs, Silicon Semiconductor spoke with Martin Hollfelder, Vice President for Service and Installation/Qualification and Technology at SCREEN SPE Germany. Approaching his third decade in the sector, Hollfelder offers a rare insider perspective on SCREEN's past, present, and the seismic changes reshaping the global chip industry.

From woodblock printing to the Angstrom Era

Although the world now knows SCREEN as a semiconductor equipment leader, its roots are unmistakably artistic. Ishida's original business focused on printing; by 1943 it had become Dainippon Screen Manufacturing. The company name may no longer include "Dainippon" - "Big Japan" - but the imprint of those early decades is still visible. SCREEN's legacy with precision machinery, imaging, and surface treatment created a natural pathway toward its entry into semiconductor technologies in 1975. This year marks the 50th anniversary of that transition - five decades of continuous engineering development and global expansion.

By 1985, SCREEN had crossed the ¥10 billion revenue threshold. It entered the global top-10 list of semiconductor equipment manufacturers in 1991, a position it has maintained ever since; in recent years it has ranked sixth or seventh worldwide. Between 1996 and 2000, the company achieved

worldwide dominance in wet cleaning systems, surpassing ¥100 billion in revenue and building its now-famous coater/developer and scrubber factory in Taga, near its central manufacturing hub in Hikone.

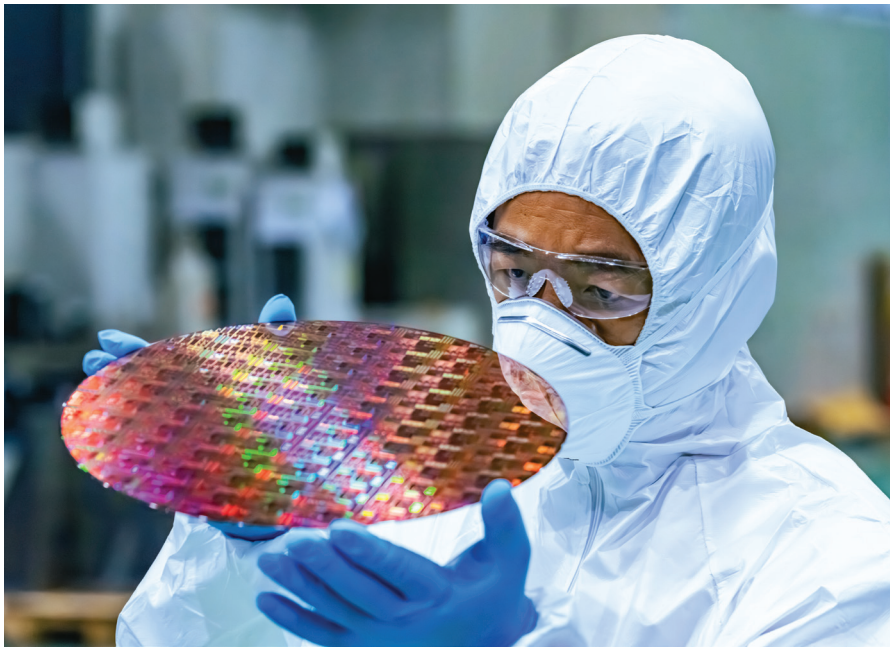
The 2000s saw the creation of its state-of-the-art S3-1 and S3-2 facilities for batch and single-wafer cleaning tools, followed by the opening of its advanced process and training centers. More recently, SCREEN has invested in automated manufacturing through its S3-3 plant in 2019 and the S3-4 and S3-5 expansions in 2023 and 2024. The growth trajectory is clear. SCREEN closed its last fiscal year at more than ¥520 billion in revenue - an all-time high and a reflection of the unprecedented global demand for chips.

A global presence aligned with the industry's needs

Despite its Kyoto roots, SCREEN today operates across every major semiconductor region. It supports 300mm leading-edge fabs producing logic, foundry, and memory devices, while also serving the 200mm and below markets tied to IoT, industrial, and automotive segments. These markets have very different requirements, and SCREEN has built a unique multi-decade competency in tailoring its tools to disparate customer needs.

For cutting-edge manufacturers, SCREEN's systems support the industry's push deep into the sub-2nm regime and toward what Hollfelder refers to as "the angstrom area of scaling." The demands at these nodes are extraordinary, involving particle control in the 10–15 nanometre range and, soon, below 10nm. Achieving this precision requires advances not only in process chemistry, but in every subtle detail - filtration, tubing materials, valves, pump technology, and the fine-tuned airflow behaviour inside tools. The company's R&D organisation makes extensive use of simulation technologies to optimise those airflow dynamics and minimise sources of contamination. This, Hollfelder notes, reflects SCREEN's broader engineering philosophy: thoroughness, durability, and continuous refinement.

Alongside contamination control, another dominant concern for leading-edge customers is pattern collapse. As



3D geometries grow taller and features narrower, the risk of physical collapse during drying or etching becomes severe. SCREEN has developed multiple approaches, including the use of surface-modifying molecules during IPA drying, polymer-based sublimation techniques, and the exploration of super-critical CO_2 technologies that provide drying without the capillary forces that lead to collapse.

The company's strength in etching spans resist stripping. To meet customer expectations, SCREEN has developed scanning and heating uniformity solutions capable of delivering highly consistent etch depth and profile control—even under low-oxygen conditions needed for backend-of-line materials.

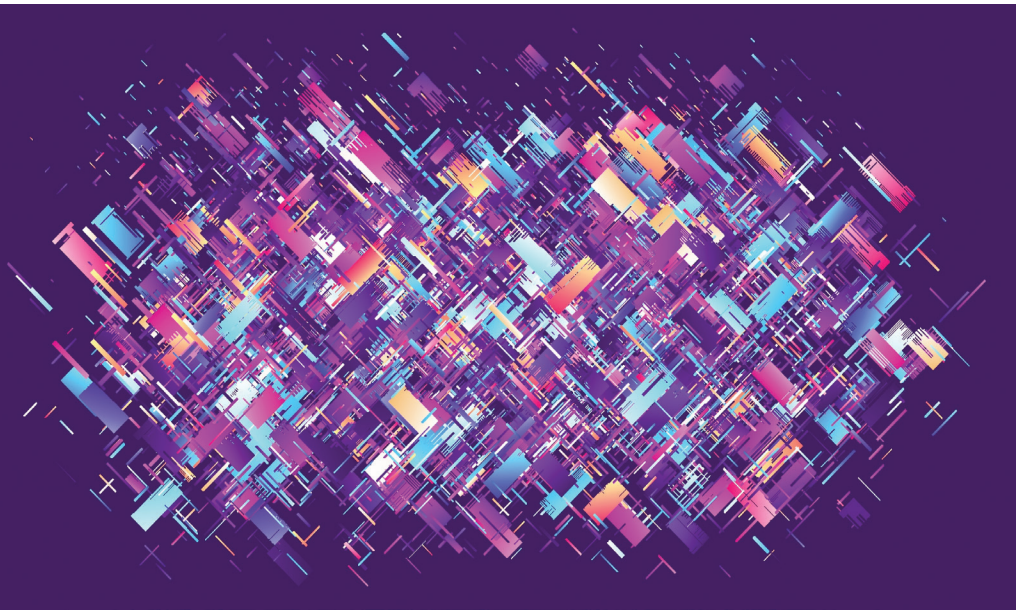
Another area of critical investment is bevel cleaning. As backside power distribution networks (BSPDN) become integral to advanced logic nodes, new materials and coatings are exposed around the wafer edge, making bevel cleaning and backside preparation essential. SCREEN now offers top-side and backside bevel etchers equipped with in-situ optical monitoring. These systems play a vital role in preventing overlay issues, focus variation, and contamination ingress into lithography tools.
Its scrubber platforms, meanwhile, are workhorses deployed across fabs for yield stabilisation - capable of nanospray processes, dual-fluid cleaning, functional water treatment, and advanced alkaline chemistries suited for defect reduction.

Lithography coat/develop systems remain another cornerstone. SCREEN's portfolio covers i-line, DUV, KrF, ArF, ArFi,, as well as direct-write platforms offering mask-less lithography for wafer-level and panel-level advanced packaging. The company's optical bake processes for underlayer materials in advanced lithography represent a new direction focused on lowering power consumption while improving stability for emerging Photoresist systems, including metal-oxide resists.

In thermal processing, SCREEN's flash-lamp anneal technology supports advanced gate-stack engineering and high-temperature processes beyond the source/drain anneals for which it has long been known. Its system versatility, including operation under different gas chemistries, makes it suitable for both planar and 3D architectures.

Beyond processing equipment, SCREEN provides inspection and metrology tools such as high-throughput macro-inspection systems down to one-micron resolution, replacing manual visual review, and thickness measurement systems based on reflectometry and ellipsometry. SCREEN has established a strong foothold in power, legacy, and specialty markets where throughput, cost effectiveness, and ease of use are paramount.

While much industry attention focuses on the bleeding edge, Hollfelder



emphasises that 200mm fabs remain vital to global supply chains, particularly for IoT, industrial, and automotive chips. These segments face intense cost pressure, exacerbated by new competitors, and depend on high-productivity, small-footprint, long-lifetime equipment.

SCREEN has responded by optimising its 200mm platforms for uptime, throughput, and cost of ownership, while maintaining particle and contamination control that meet customers' device requirements. The company continues to sell 150mm and below systems as well, recognising that not all markets move in lockstep toward larger substrates.

Advanced packaging: the industry's next great inflection

If any domain represents the coming era of semiconductor transformation, it is advanced packaging. Hollfelder describes it as 'a game changer', and the scale of current investments bears out that claim. The rise of chiplet architectures, 3D heterogeneous integration, through-silicon vias, wafer-on-wafer stacking, and photonics-in-package solutions is reshaping entire manufacturing flows. The new fabs being built for this purpose increasingly resemble front-end fabs in their contamination and particle-control requirements - areas where SCREEN's expertise is immensely valuable.

The company has long supported silicon thinning after back-grinding, etch processes, and backside cleaning for 3D integration. But the latest packaging generations require extremely thick photoresist layers for bumping, redistribution layers, and hybrid bonding interfaces. SCREEN is developing new stripping, bevel cleaning, and contamination-control methodologies specifically for these geometries.

The market inflection is driven primarily by AI. Hollfelder notes that hyperscalers' voracious appetite for AI accelerators is pushing foundries to build unprecedented amounts of capacity not only for GPUs but also for high-bandwidth memory. However, power consumption has become a limiting factor. The shift toward photonics in the package - reducing electrical I/O energy per bit - is central to making next-generation AI systems viable. The most forward-looking roadmaps envision 'systems on wafer' architectures, placing the equivalent of a supercomputer in a compact rack.

As chiplet architectures expand, the relevance of SCREEN's core competencies - cleaning, etching, drying, contamination control, and resist handling - only grows stronger. The company sees advanced packaging as a major pillar of its long-term roadmap.

Artificial Intelligence: driver of demand and tool for innovation

AI is not only generating record demand for chips; it is transforming semiconductor manufacturing itself. SCREEN is using AI to optimise silicon thinning processes by compensating for process variation through in-line measurements and closed-loop control. Future integrations will include chamber matching optimisation, excursion prevention, and enhanced image-processing algorithms.

AI is also embedded in SCREEN's digital-twin initiatives, helping the company reduce water usage and waste treatment loads inside its factories. Beyond its own operations, SCREEN expects fabs everywhere to adopt AI for predictive maintenance, workflow optimisation, and yield improvement.

Yet Hollfelder also identifies an obstacle: the industry's culture of data protection. AI thrives on shared data across partners, but semiconductor companies traditionally guard process information closely. The balance between collaboration and confidentiality will shape how fast AI can deliver its full benefits.

Sustainability and the PFAS question

Sustainability is no longer just a 'nice to have', it is a business requirement driven by customers and regulators worldwide. SCREEN is deeply involved in several initiatives, including the imec Sustainable Semiconductor Technologies and Systems (SSTS) programme and the European GENESIS project. Both focus on reducing environmental impact across semiconductor manufacturing, with a growing emphasis on PFAS-free materials.

Hollfelder explains that SCREEN's strategy spans the three "R's": reducing usage of chemicals and water, recycling them where possible, and reusing them safely. The newest SCREEN systems include recycling capabilities for phosphoric acid, sulphuric acid, ozone water, and high-temperature deionised water. The flagship SU-3400 tool is designed to operate with lower chemical and exhaust consumption, reflecting SCREEN's broader efficiency roadmap.

PFAS, widely used in semiconductor processes and tool components, is increasingly scrutinised by regulators. SCREEN is proactively developing PFAS-free resist materials and surfactants alongside imec, while redesigning tool parts to minimise PFAS exposure. Approaches include hybrid PFA tubing, in which only the fluid-contact layer uses fluorinated materials,

and emerging recycling pathways for PFA components.

The urgency of sustainability becomes more pronounced at advanced nodes. As imec research shows, every new generation of devices adds more process layers, driving up energy and resource consumption even as transistors shrink. This paradox underscores the need for aggressive innovation in green manufacturing - a domain where SCREEN intends to lead.

Partnerships for the future

SCREEN's partnership with imec spans more than two decades. As one of the world's premier semiconductor R&D hubs, imec provides a real-world proving ground for SCREEN's latest cleaning and lithography tools. The two organisations recently extended their strategic partnership for five more years, covering research areas from EUV to next-generation 1 nm CFET technologies.

A second major collaboration, announced with IBM, focuses on cleaning challenges for high-NA EUV lithography. The industry's move toward numerical apertures near 0.55 brings far tighter tolerances, and with them, a new level of sensitivity to backside particle contamination and wafer flatness. Even minute particles or scratches can create overlay drift, focus errors, or degradation inside the scanner. Through joint development, SCREEN is refining brush technologies, chemical etch sequences, and defect-removal methods capable of delivering the near-perfect wafer flatness and cleanliness high-NA tools demand.

Such partnerships exemplify the collaborative model now necessary for progress. No single company can master every detail of the advanced semiconductor stack; SCREEN's willingness to share expertise accelerates breakthroughs across the industry.

Industry challenges

Even as demand surges, the semiconductor ecosystem faces some potentially daunting obstacles. One is a global shortage of experienced technical talent. SCREEN's rapid growth requires more engineers, service specialists, and manufacturing staff across its worldwide locations, yet the talent pool remains constrained.

SCREEN's partnership with IMEC spans more than two decades. As one of the world's premier semiconductor R&D hubs, IMEC provides a real-world proving ground for SCREEN's latest cleaning and lithography tools. The two organisations recently extended their strategic partnership for five more years, covering research areas from EUV to next-generation 1 nm CFET technologies

Geopolitical tensions add another layer of complexity, affecting trade policy, equipment exports, and materials supply chains. Hollfelder notes that tariffs and geopolitical realignments place pressure on both SCREEN and its customers, complicating long-term planning.

Meanwhile, market divergence continues. The cutting-edge races toward angstrom-scale nodes and 3D integration, while legacy markets - particularly automotive and industrial - face intensifying cost competition. SCREEN's dual responsibility is to support both ends of the spectrum without compromising the reliability its brand is built on.

Despite these headwinds, the company's vision remains clear. SCREEN's credo: 'Innovation for a sustainable world', guides its strategy across R&D, operations, and customer engagement.

A roadmap toward the Angstrom Age

Looking ahead, SCREEN is preparing new platforms for both the most advanced technology nodes and the rapidly expanding advanced packaging landscape. The push into the angstrom era will require breakthroughs in contamination control, new drying and etching chemistries, more precise airflow engineering, and integration of AI-driven process optimisation.

At the same time, advanced packaging fabs are adopting front-end contamination standards, creating an entirely new market category aligned with SCREEN's foundational expertise. Hollfelder sees this as one of the company's strongest growth opportunities, as customers desperately need equipment capable of managing the strict defect-density requirements for chiplet interconnects, TSVs, and hybrid bonding.

Expansion of global offices, support teams, and manufacturing capacity will continue as SCREEN positions itself to meet surging demand, especially from the hyperscalers and megafoundries producing AI silicon.

As the semiconductor sector pushes toward the much-discussed trillion-dollar milestone by 2030, Hollfelder maintains a sense of grounded optimism. With 29 years of experience in the field, he has seen downturns and booms alike, but he still finds excitement in the technical challenges and collaborative spirit that define the industry.

"If you compare the semiconductor industry with other sectors," he reflects, "we are still in a very well-suited situation." The challenges are real - geopolitics, sustainability, skills shortages, and the sheer complexity of today's devices - but the momentum is unmistakably forward.

SCREEN's journey from a 19th-century printing workshop to a global leader in semiconductor equipment illustrates the power of reinvention and relentless engineering focus. As the world steps into the angstrom age and the era of AI-driven computing, companies like SCREEN will shape the technologies that define the next generation.

And after 50 years in semiconductors, SCREEN shows no signs of slowing. The company's future, like the industry's, is one of challenge, but also of unparalleled opportunity.

Securing the future of battery power: Precision testing challenges of next-generation BMS ICs

The rapid global transition toward electrification, driven by the booming Electric Vehicle (EV) and Energy Storage System (ESS) markets, has placed Battery Management System (BMS) Integrated Circuits (ICs) at the epicenter of system design.

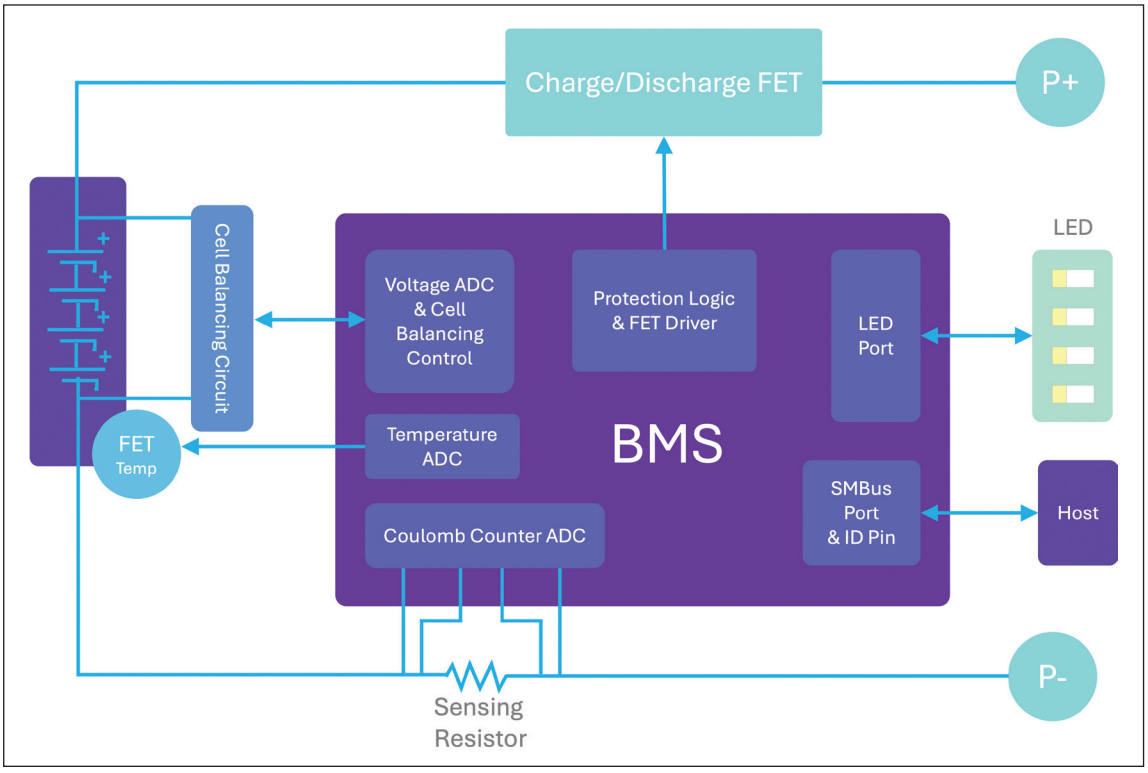
FAR from being a mere component, the BMS IC acts as the electronic brain, a critical safety and efficiency gatekeeper responsible for monitoring, balancing, and protecting thousands of battery cells within a pack. Its proper functioning is not negotiable; a failure can lead to catastrophic thermal events, drastically reduce battery lifespan, or compromise critical performance metrics like vehicle range.

As BMS IC complexity increases - with modern devices now managing up to 32 cells and operating at high-voltage, high-current extremes - the task of Automated Test Equipment (ATE) has become exponentially more challenging. Ensuring the long-term reliability and functionality of these sophisticated mixed-signal devices requires a paradigm shift in test methodology.

Manufacturers must move beyond standard ATE capabilities to embrace specialized solutions that guarantee flawless performance under real-world, high-stress conditions and meet the stringent zero-defect quality demands of the automotive sector.

The triple challenge of BMS ICtesting

Testing a modern BMS IC presents three fundamental technical hurdles that conventional mixed-signal ATE often struggles to resolve, demanding specialized instrumentation and test architectures:



➤ Figure 1: Typical BMS block diagram.

- **High-voltage cell simulation with ultra-precision:** A BMS IC must be rigorously tested against every potential battery state, including critical over-charge and deep-discharge scenarios. This demands the ATE to accurately simulate the individual voltage inputs of every cell, often requiring stable, low-noise voltage generation up to 200V. Crucially, the accuracy requirement is extremely stringent - often less than 50µV - to precisely emulate minor voltage fluctuations that trigger sophisticated cell balancing functions. The test solution must achieve this high-precision measurement while operating in a floating setup, isolating the measurement circuitry to prevent interference from ground loops, which is paramount for maintaining signal integrity in high-voltage applications.

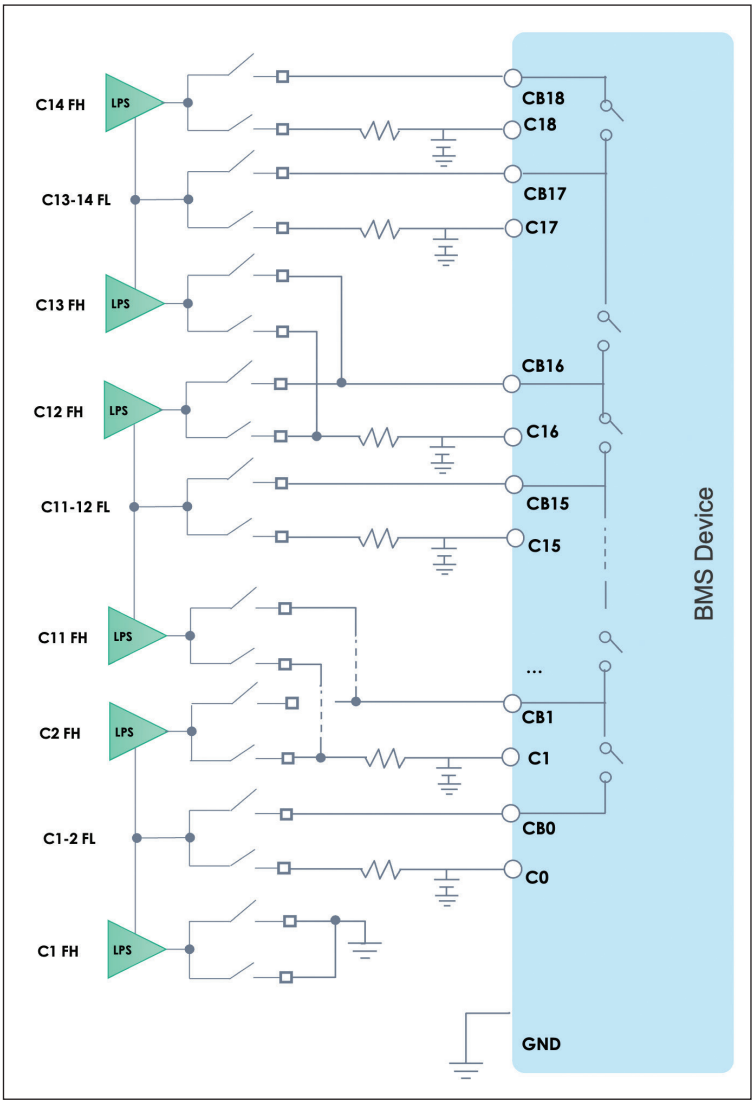
- **Sensitive measurement for longevity:** Leakage current and RDS-on: Battery longevity is directly impacted by power consumption from the BMS IC itself. Accurately measuring the minute leakage current generated by the IC is essential for verifying efficiency and preventing unnecessary battery discharge during long idle periods. If the leakage current exceeds specifications, the overall capacity and lifespan of the battery pack will be compromised. Similarly, a core function of the BMS is cell balancing via integrated MOSFET switches. The tester must precisely measure the MOSFET's on-state resistance (RDS-on). Any elevated RDS-on value translates directly into increased power dissipation and thermal issues, compromising the battery pack's long-term health. These sensitive measurements require high-resolution, high-speed data acquisition capabilities well beyond standard ATE specifications.

- **Maintaining Accuracy at Volume Production:** In mass production environments, maintaining sub-millivolt accuracy across a multitude of channels, often running 24/7, is a critical challenge. Standard ATE relies on periodic, costly calibration, which introduces significant downtime and risks accuracy drift over large production lots. Automotive standards require traceability and stability that generic testers often cannot guarantee efficiently.

The SPEA DOT800 solution: High-density floating instrumentation

To navigate these unique high-precision, high-voltage testing demands, SPEA's DOT800 Mixed Signal Tester instrumentation is engineered specifically around the unique requirements of the BMS IC, leveraging a key architectural feature: high-density floating instrumentation.

Precision through a floating architecture: Unlike less accurate resistor ladder or single-ended configurations, the DOT800 employs a floating test architecture. This superior design isolates the measurement system from ground-related noise,

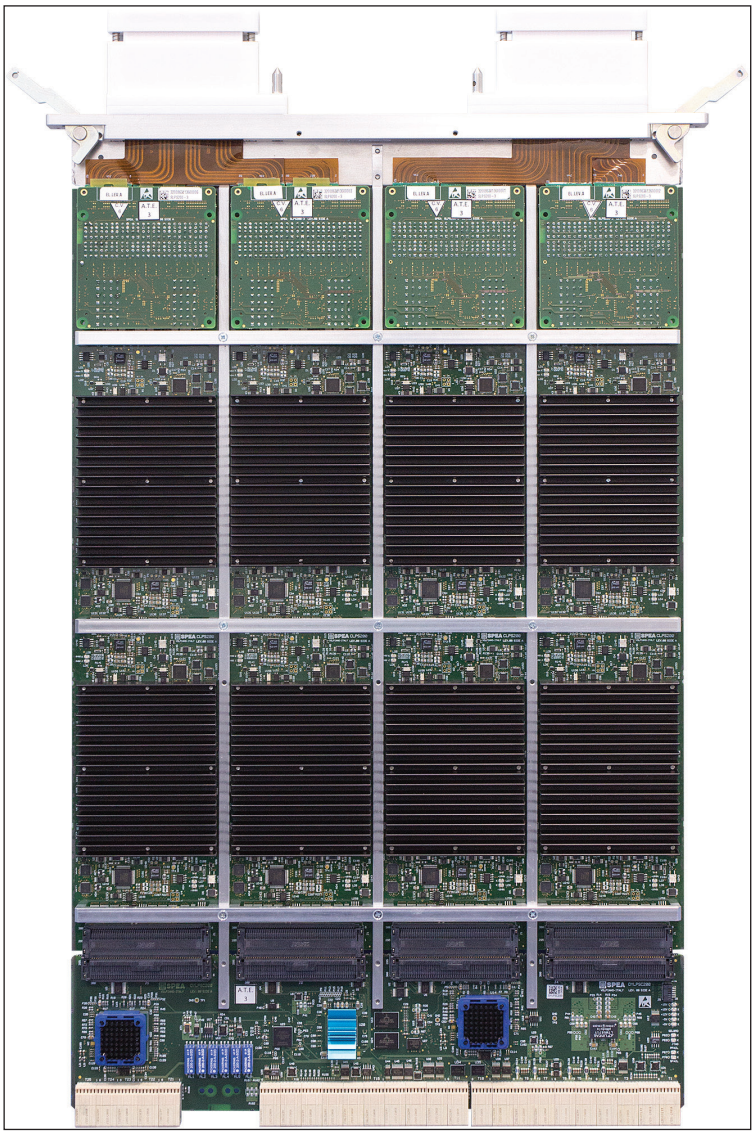


➤ Figure 2: Typical BMS test setup configuration.

enabling highly accurate voltage generation and measurement across a wide voltage range without losing resolution. This is essential for:

- **Voltage generation:** Achieving long-term stability and a remarkable accuracy of 5-100µV at high voltage levels
- **Safety and protection:** Integrating fast current clamping to instantly protect the Device Under Test (DUT) and the test system in the event of a short circuit
- **Efficiency verification:** Providing the necessary high resolution to verify leakage current performance and accurately assess RDS-on, direct indicators of long-term battery efficiency.

➤ Figure 3: SPEA DOT800 Mixed Signal Tester.



➤ Figure 4: DOT800's high density fully floating drivers with V/I digitizer are specifically designed to test ICs with multiple voltage domains, that demand for advanced isolation schemes.

The self-calibration advantage: Guaranteed accuracy per Lot

Perhaps the most significant differentiator in maintaining robust quality control for critical BMS ICs is the DOT800's unique self-calibration system, which utilizes an integrated external, high-precision multimeter with direct access to the DUT pins.

This process ensures that system accuracy surpasses even the tester's published specifications:

- **Reference measurement:** At the start of a production lot, the tester performs an internal calibration sequence. It generates the required test voltages and then uses the integrated high-precision multimeter to measure the exact voltage delivered at the DUT pins, storing this value as a highly accurate reference.

- **Total Measurement Error (TME) correction:** During production testing, the measured DUT value is constantly compared against the stored reference. This comparison effectively calculates and corrects the Total Measurement Error (TME) for each individual cell, providing consistent, reliable, and traceable results.

By leveraging the inherent stability of the SPEA architecture, this comprehensive calibration is only required once per production lot, maximizing equipment uptime and minimizing the Cost of Test (COT) while guaranteeing stable accuracy over the entire production run.

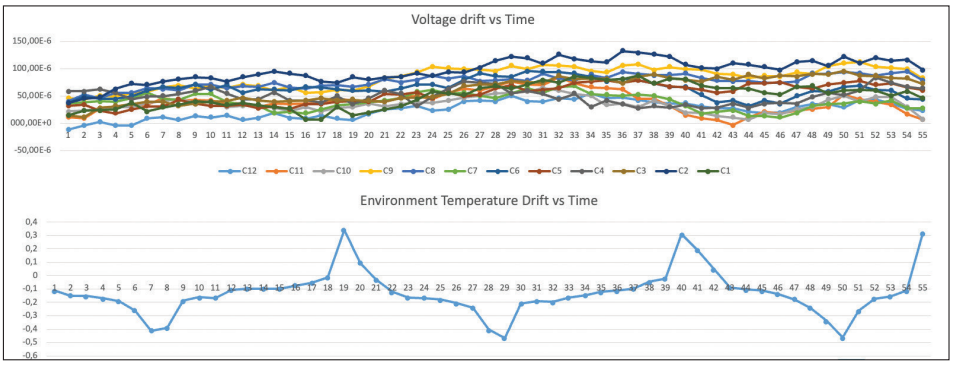
Conclusions

The exponential growth in battery-powered systems hinges on the reliability of the BMS IC. As device complexity continues to rise, the limitations of conventional ATE will become an unacceptable risk.

For manufacturers committed to battery safety, performance, and longevity, adopting specialized ATE - featuring high-voltage floating architecture, ultra-precise measurement capabilities, and unique self-calibration systems - is no longer optional.

The DOT800 provides the necessary toolset to meet the most rigorous performance standards, securing the quality and reliability of the next generation of battery-powered products.

➤ Figure 5: Very high precision drivers allow the user to strongly reduce the frequency of instrument calibrations with external multimeters. The charts show the long-term drift of SPEA's drivers: in over 50 hours of consecutive working, with spot calibration performed every hour, the maximum drift is around 50µV.



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