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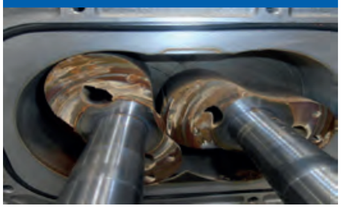
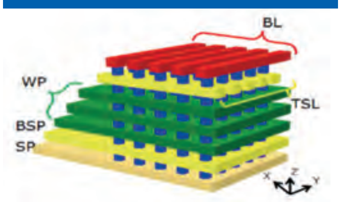
KLA steers automotive IC, power applications

Smart manufacturing in the sub-fab

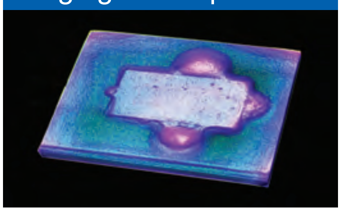


The vertical ferroelectric FET



Q&A with Mike Plisinski Onto CEO

X-ray and acoustic 3D imaging of components



Siconnex development offers great advantages in automated wafer handling

inside News Review, News Analysis, Features, Research Review, and much more...
Free Weekly E News round up go to: www.siliconsemiconductor.net

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

editor'sview

By Mark Andrews, Technical Editor

Taking stock and looking ahead in 2020 and beyond

THE NEW YEAR got off to a roaring start across global semiconductor manufacturing even as most of us did not realize that an all too old-fashioned threat was raising its head: contagion.

At a time when we typically celebrate and look forward to greater sales and innovative new products, we were instead watching news of infection tallies and WHO pronouncements. The continuing and unfolding story of Chinese and world-wide efforts to halt the Coronavirus (COVID-19) is now creating supply chain ripples even as efforts to heal the sick and end quarantines accelerate.

The human story behind the virus centers in Wuhan and greater China, but it's a story without borders. For us in technology, Wuhan is as 'close' as Birmingham or Brussels, San Jose or Singapore. We need to remember that our global colleagues affect our lives just as we affect theirs.

My family is not in Hubei, but many friends are whether they are in Wuhan, Shanghai, Shenzhen or elsewhere—the location isn't as important as the fact that those directly affected are 'us' – just in different locations.

The viral outbreak that China is battling also points to how interconnected our world has become. Our industry helped create global connectedness and our technologies will have a role in finding a cure. Support those efforts in ways that you can while looking ahead to a time when everyone will be able to say they are optimistically looking ahead, not behind.

At this point I typically offer a brief summation of the excellent articles we have written and collected to better inform your business decisions.

They are still with us and I hope that you will enjoy our fine articles chronicling advances at Edwards Vacuum, KLA Corporation, Onto Innovation, and industry-leading research from our imec colleagues.

At the same time, take a moment to support our brothers and sisters in China and anyone fighting a tough battle. We truly are an industry without borders.

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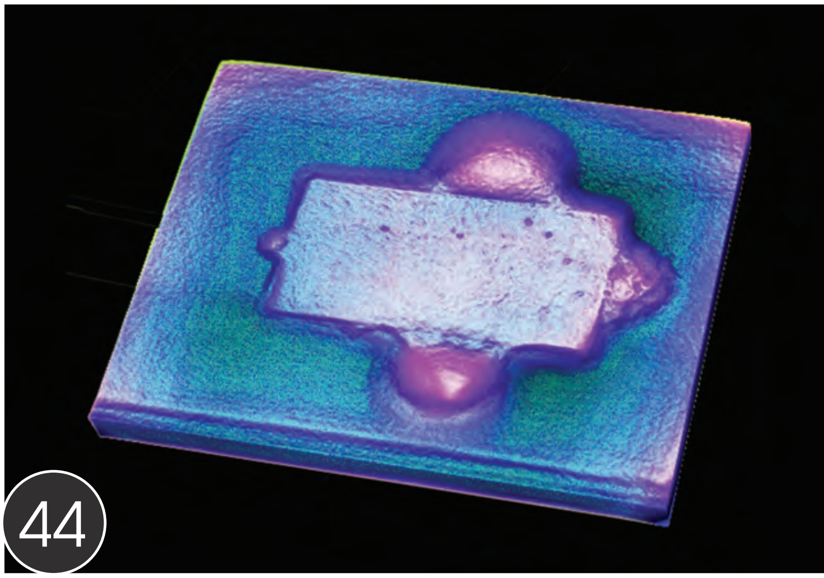

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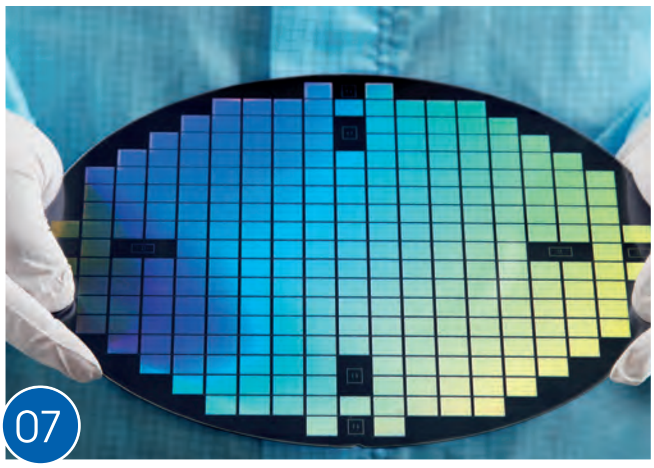


Pfeiffer Vacuum receives milestone award for vacuum technology

"PROCESS", the specialist media brand of the Vogel Communications Group, has taken its 25th anniversary as an opportunity to present some of the most important technologies from this period in a series of milestones. In this context, vacuum specialist Pfeiffer Vacuum received the milestone award for vacuum technology, one of a total of 16 award-winning categories.

The prize was awarded to companies whose developments have significantly influenced technology and continue to do so today, during an anniversary gala at the Vogel Convention Center in Würzburg.

Dr. Jörg Kempf, editor-in-chief of PROCESS, praised Pfeiffer Vacuum in his awards presentation for its customer orientation: "For more than 125 years now, the company has been living the fascination of vacuum and has distinguished itself not only through its technology, but especially through its feel for the diverse requirements of the relevant industries – from vacuum generation to leak detection."
In the process industry, Pfeiffer Vacuum's cutting-edge vacuum solutions set standards time and again, he said during the award ceremony.

"We are delighted to receive this award. We regard it as recognition of the fact that we develop tailor-made solutions together with our customers. Our aim is always to make our customers more successful," said Wolfgang Bremer, head of the Industrial Vacuum Product Group at Pfeiffer Vacuum, who accepted the award at the gala.

SEMICON China 2020 postponed

THE CHINESE GOVERNMENT has implemented strict measures in the prevention and control of the outbreak of the Novel Coronavirus (2019-nCoV), escalating it to the highest priority with an intent to protect public health and minimize further spreading of the virus.

In accordance with government guidelines and to protect the health and safety of exhibitors and guests, we regret to inform you of the postponement of SEMICON/FPD China 2020 and related events originally scheduled for March 18-20, 2020. SEMI China is actively working on a contingency plan for rescheduling of the event and will keep you informed as soon as a confirmed plan is in place. We apologize for any inconvenience caused by this change, but your safety is our top concern.

SEMICON/FPD China has become the leading semiconductor and display industry event in China and globally because of your continuous participation and contribution. Your understanding and support are particularly appreciated at this critical moment.

SEMI is evaluating the health risks the Novel Coronavirus poses at other upcoming exhibitions and conferences and will make decisions whether to hold them as planned on a case-by-case basis. We encourage everyone to remain abreast of developments on the Novel Coronavirus by visiting the World Health Organization website for updates.

Mycronic receives order for an SLX mask writer

MYCRONIC AB has received an order for the new SLX mask writer from a customer in Asia. The order value for the chosen SLX configuration is between USD 3 and 4 million. Delivery is scheduled for the fourth quarter of 2020.

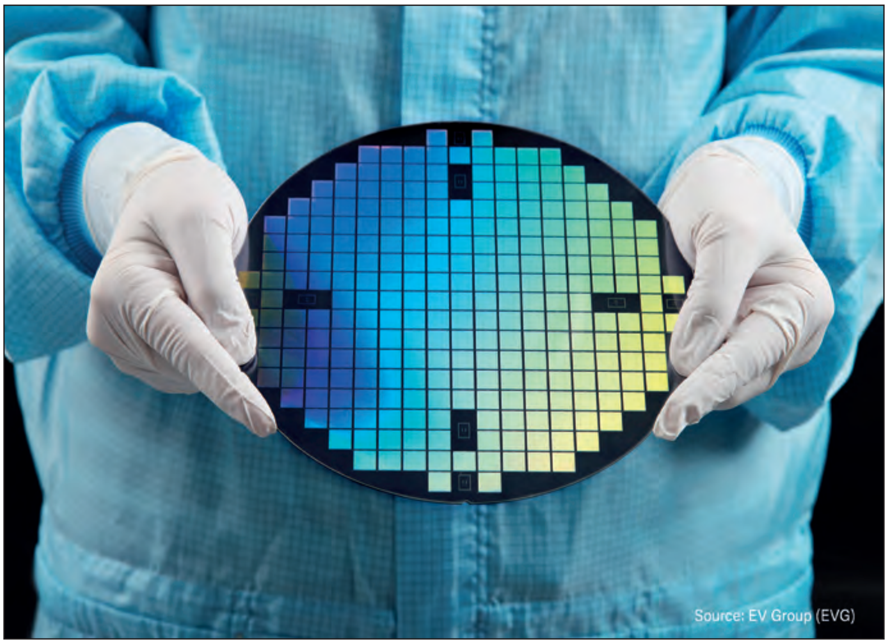
The laser-based SLX mask writer was launched at the end of October 2019 to meet a rising demand for photomasks for the semiconductor industry driven by long term trends as well as to support an upcoming replacement and modernization cycle. Photomasks produced by laser-based mask writers are very important in the production of semiconductors, accounting for 70-75% of all photomasks produced. The SLX is a new and modern mask writer based on the same technology as the display mask writers, which includes the recently launched Evo control platform.

Mycronic offers mask writers for the manufacture of photomasks within different areas of application. These are display manufacturing (TV, smartphones and tablets), semiconductor manufacturing and applications within multi-purpose, a broad segment comprising many different application areas.

EVG and Inkron partner on high refractive index materials

EV GROUP (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets, has announced that it is partnering with Inkron, a manufacturer of high and low refractive index (RI) coating materials, to provide optimized processes and matching high RI materials for the development and production of high-quality diffractive optical element (DOE) structures.

These DOE structures include waveguides for augmented/mixed/virtual reality (AR/MR/VR) devices, as well as beam splitters and diffusers for advanced optical sensing used in automotive, consumer electronic and commercial applications.


Source: EV Group (EVG)

This partnership is being carried out within EVG's NILPhotonics Competence Center at its headquarters in St. Florian, Austria. EVG's NILPhotonics Competence Center provides an open access innovation incubator for customers and partners across the NIL supply chain to collaborate to shorten development cycles and time to market for innovative photonic devices and applications.

As part of this agreement, Inkron has also purchased an EVG 7200 NIL system for use in its own research and development facility to accelerate the development and qualification of new optical materials. The EVG 7200 system leverages EVG's innovative SmartNIL technology and materials expertise to enable mass manufacturing of micro- and nanoscale structures as small as 30 nm over a large area with unmatched low-force and conformal imprinting, fast high-power exposure and smooth stamp detachment.

"Demand for wafer-based optical components and sensors across commercial and consumer markets is accelerating at a breakneck pace, driving the need for materials and processes that are optimized to meet the performance requirements and production volumes required in these markets," stated Markus Wimplinger, corporate technology development and IP director at EV Group. "Inkron has extensive know-how in optical materials and is one of the leading manufacturers of high and low RI coatings, making the company an ideal partner to work with at our NILPhotonics Competence Center.

Collaborations such as this one enable EVG to further explore and expand the applications and capabilities of our NIL technology, ensuring the availability of production-ready solutions for next-generation optical devices and end products."

The material properties of optical elements and components have a major impact on the overall performance and form factor of the packaged optical device. For example, higher refractive indices (up to 1.9x and above) enable optimized designs for improved outcoupling of the light, which can significantly increase the field of view of waveguides, providing a more immersive experience in AR/VR headsets.

Higher RI materials can also provide higher optical density and enable more efficient diffractive optics used for beam splitting (such as for facial recognition sensors), supporting further miniaturization of the optics.

Additional optimization of high RI materials can provide better contrast due to improved film transparency as well as reduced haze and scattering, while improved resin stability can address more stringent thermal requirements, such as those needed in automotive applications.

Optimizing the high RI materials for NIL processing helps ensure their implementation in volume production. NIL is a proven method for manufacturing optical elements due to its ability to provide cost-effective patterning of nanometer-scale features at high volume, while being insensitive to feature size, shape and complexity.

"We are excited to be teaming up with EV Group to accelerate the introduction of new, optimized and innovative optical material technologies that help to address critical performance roadmaps of our customers," stated Juha Rantala, CEO of Inkron.

"Our nanoimprintable high refractive index materials and matching gap filling coatings, combined with EVG's leading NIL systems, provide critical wafer-level solutions that optics manufacturers need in order to quickly scale up production on their latest products."

Evonetix collaborate with imec to scale-up chip based tech production

EVONETIX, the synthetic biology company developing a desktop platform for scalable, high-fidelity and rapid gene synthesis, today announced it has partnered with imec, a world-leading research and innovation hub active in the fields of nanoelectronics and digital technologies, to increase production of Evonetix's proprietary microelectromechanical systems (MEMS)-based silicon chips, enabling the platform to be manufactured at a commercial scale. The novel silicon chip is a key component of Evonetix's desktop DNA platform which, once fully developed, will facilitate and enable the rapidly growing field of synthetic biology.

Evonetix's technology utilises a silicon chip, made by MEMS processing, that controls the synthesis of DNA at many thousands of independently controlled reaction sites or 'pixels' on the chip surface in a highly parallel fashion. Following synthesis, strands are assembled on-chip into double-stranded DNA in a process that identifies and removes errors, enabling accuracy, scale and speed that is several orders of magnitude better than conventional approaches.

Under the terms of the collaboration, imec will work with Evonetix to scale up manufacturing of the MEMS technology on 8-inch silicon wafers, enabling Evonetix to supply customers in volume. Imec is able to leverage its experience in manufacturing silicon for life sciences applications to transfer the novel Evonetix process to their foundries and to manage further expansion in volume.

Dr Matthew Hayes, Chief Technology Officer at Evonetix, said: "With the support of imec, a world-renowned leader in microchip technology, we will be able to optimise our highly parallel desktop platform for commercial supply."

Peter Peumans, Senior vice president life science technologies at imec added: "We have extensive practical knowledge of chip design and technology, which we use to help develop innovative tools for the life sciences and pharma R&D.

Evonetix has developed an innovative approach that integrates physics and biology to enable the production of high-fidelity long DNA in a highly parallel fashion. We are eager to contribute to their success using our nanotechnology capabilities."

Miniature power supply devices for automotive electronics

INFINEON TECHNOLOGIES AG is taking the next step towards smallest power supply devices for automotive electronics. As first chipmaker, the company set up a dedicated production process for flip-chip packages that is fully aligned with the high quality requirements of the automotive market. Infineon now launches the first respective product: the linear voltage regulator OPTIREG™ TLS715B0NAV50.

With flip-chip technology, the ICs are installed upside down in the package. With the heated part of the IC facing the bottom of the package and being closer to the PCB, thermal inductance can be improved by a factor between 2 and 3. The higher power density enables a significantly smaller footprint than conventional package technologies.

The footprint of Infineon's new linear voltage regulator (TSNP-7-8 package, 2.0 mm x 2.0 mm) is more than 60 percent smaller than that of an established reference product (TSON-10 package, 3.3 mm x 3.3 mm) while the thermal resistance stays the same.

This makes the new device particularly suitable for applications with very limited board space, such as radar and cameras. The OPTIREG TLS715B0NAV50 provides 5 V with a maximum output current capability of 150 mA. Flip-chip technology has been used in consumer and industrial markets for several years. Due to increasingly strict space requirements, particularly in the growing number of radar and camera systems, also automotive electronics require smaller power supply solutions – albeit with much higher quality requirements.

In order to offer best-in-class flip-chip quality Infineon does not rely on a subsequent qualification of existing consumer and industrial products but rather on a dedicated production process for automotive devices. In the future, flip-chip technology will strengthen Infineon's overall portfolio of automotive power supply products in the OPTIREG family.

The chipmaker is planning to apply it also to its switch mode voltage regulators and power management ICs.

Dry run over IC bridge

CARS HAVE ALWAYS needed to be safe, but safety is no longer just about having robust engine and chassis. With the shift in automotive technology being from mechanical to electronic, it is the performance of the electronic components that need to be reliable.

The consequences of failure can, of course, be devastating as these component manufacturers are all too aware. One of the leading players in the automotive semiconductor sensors market is Melexis, and it has recently completed the first phase of a new project to ensure components are delivered in the same impeccable condition that they were made in.

Moisture in semiconductors is a serious issue. Trapped moisture can vaporise and expand when subjected to the temperatures of a reflow oven during assembly. While this can lead to catastrophic failure of the part during the production process – an effect called 'popcorning' – it can also introduce cracks and weaknesses in the component that could present reliability issues once the assembly is out on the market. It is an issue that is obviously taken very seriously both by the electronics assembly sector in the way that they handle and store components, and also by the semiconductor makers themselves.

What Melexis was aiming to achieve with this latest project was to provide additional assurance for the step from its semiconductor factory in Ieper, Belgium to its assembly customers. The site works round the clock to test around 40 million ICs a month principally sensors for the automotive market, though their high performance has also led to applications in consumer and industrial.

Dry Tower is the solution provided by Totech, a company that was already well-known to Melexis. "Totech solutions and tools are known and used internally and at our customers," continued Leterme, who also recognised 'Totech's support and reactivity'. This project was looking at the stage just before final packing and sending off to customers. All components will have had their final optical inspection before being taped and reeled, and then this final drying stage ensures components are completely dry before despatch. It is a stage that is standard – and defined by standards – within the industry. All components are held for a minimum of 24 hours at 1% RH (relative humidity).

Totech's standard drying cabinets were already being deployed at an earlier stage in the Melexis process. However, to use these cabinets for the final drying application would have meant a footprint of around three times that of the adopted Dry Tower solution - and floor space was one of the key considerations. After benchmarking against another main European supplier, it was considered that the Dry Tower would offer the best solution.

Swagelok launches ultra high purity valve for ALD

SWAGELOK, a US solutions provider of fluid system products, assemblies, and related services, announced the release of a new ultra high-purity (UHP) valve for high-flow applications – the ALD20.

Since introducing atomic layer deposition (ALD) valve technology to the market, Swagelok has worked with semiconductor tool manufacturers and chip fabricators to provide the performance needed to keep pace with quickly changing process requirements. The new ALD20 valve is the latest result of this collaboration, allowing forward-thinking process designers the flexibility to experiment with low-vapour pressure chemistries that may hold the key to tomorrow's competitive advantage. The ALD20's patent-pending design maximizes production process efficiency and deposition consistency by providing flow coefficients two to three times what can be achieved using today's standard ALD valve technology. It can deliver a flow rate of up to 1.2 Cv in the same footprint (1.5 in.) as existing ALD valves, allowing some users to boost throughput without retooling existing equipment or making additional process changes. The other standard version ALD20 valve with a slightly larger footprint width (1.75 in.) provides an even greater flow rate of up to 1.7 Cv. Custom set flow coefficients are also available.

Designed for peak process consistency, the ALD20 can be fully immersible in a gas box from 10degC up to 200degC, enhancing thermal stability and deposition uniformity. It also features a valve body comprised of 316L VIM-VAR stainless steel or Alloy 22 – offering enhanced corrosion resistance to withstand aggressive media—as well as a highly polished bellows with a 5 μin. Ra finish to support clean operation for long-term process integrity.

"The ALD20 is a direct response to the rapidly evolving needs of the semiconductor industry," said Garrick Joseph, director of marketing, semiconductor, for Swagelok. "Through partnership with industry leaders and application of fluid system engineering

expertise, we are pleased to launch a product that allows customers to effectively use precursor gas chemistries that previously may have been considered too challenging or too expensive to employ, but which could be crucial to the development of the next generation of chip technology."

The ALD20 is available today in modular surface-mount configurations with two or three ports, in straight configurations with tube butt weld and male or female VCR face seal fitting end connections, and in multiport valve configurations to optimise flow paths within existing or new systems. A high-temperature optical position sensor is available as an add-on component as well.

Brewer Science introduces their first permanent bonding material

BREWER SCIENCE has introduced their first material for permanent bonding from the European 3D & Systems Summit. This new material is included within the Brewer Science product family of PermaSOL materials designed to address device- and wafer-level packaging requirements. The new material addresses a range of needs identified for permanent bonding applications, which include low-temperature bonding, extreme chemical reisistance, UV or thermal curable bonding process, and no material movement after cure.

Permanent bonding materials are adhesives and dielectrics used to assemble integrated circuit (IC) logic chips, memory chips, image sensor devices, and microelectromechanical systems (MEMS) devices, which go into high-density heterogeneously integrated packages. These high-density, ultra-thin electronic packages are needed for artificial intelligence (AI) in high-performance computers, data centers, 5G, and high-end mobile products.

“This is an exciting time for the industry as we continue to develop new materials that meet our customers’ needs for next-generation technology to perform at its best,” said Kim Arnold, Executive Director – Wafer-Level Packaging Materials, at Brewer Science. “As we move forward and work closely with our customers, suppliers, and partners, we expand our ability to offer solutions into new exciting areas including permanent bonding.”

PermaSOL materials have been created to enhance and improve many key market drivers within device- and wafer-level packaging processes:

- MEMS devices, glass frit, and anodic bonding technologies in order to achieve good hermeticity to protect the MEMS sensor
- LED devices requiring metal bonding (eutectic and thermo-compression bonding) to meet higher performance in terms of light extraction
- CMOS image sensors for direct bonding & adhesive bonding
- SOI substrate manufacturing supporting the fusion bonding technology
- 3D Integration: Thermocompression bonding (TCB)

Edwards announces new liquid ring vacuum pump

EDWARDS VACUUM has developed a new range of new liquid ring pumps – the ELRi series - made for applications which are wet, humid as well as corrosive.

According to the company, the stainless steel impeller, endplates, liquid reservoir and heat exchanger makes this pump resilient against corrosion and harsh process gases. The internal injection channels reduce the risk of leakage while the horizontal motor flange arrangement saves precious time on maintenance. Use of mechanical seals also ensure reliable operation by preventing leaks as well as extending service intervals.

The technology is contained in a compact noise cancelling sturdy canopy protecting and extending lifetime of the electronic components.

The ELRi is equipped with two variable speed drives (VSD). While the main VSD matches the speed of the pump to vacuum level by adjusting its speed, the second VSD regulates the water flow through the centrifugal pump according to the operating conditions to avoid risks of cavitation. A patented algorithm maintains a perfect harmony between the two VSDs ensuring optimal performance.

In addition, it is protected against automatic seizure, so users do not have to worry about the pump failure after long periods of inactivity.

The integrated air logic controller enables the monitoring of important features and parameters of the pump and also offers the option of set-point control. This allows users to have a vacuum pump that matches the process demand saving energy. While the ECOntrol box even allows you to connect and control multiple ELRi pumps, the Icon Box enables smart monitoring and remote controlling ensures optimal servicing to get maximum uptime with your pumps. Along with this, water consumption is also reduced as the separator is only filled up when required.

The ELRi series comes in pumping capacity 750-1050m3/hr covers a wide range of applications in the central vacuum, pharmaceutical , plastics, conveying and food applications.

Megha Ajmal product manager for Rough Vacuum products commented: “While the standard range of pumps is a perfect solution of general industrial applications, our Heavy-Duty range is designed with all process wetted parts to be stainless steel.

“All pumps are also fitted with spray nozzles as standard which are particularly useful for high steam load applications allowing to pump increased capacity of gas load.The manual and automatic modes of flushing allow operation in even in the dirtiest applications with minimal downtime.”


environments
where
innovation
thrives

Siconnex BATCHSPRAY® Autoload & the patented RETAINER COMB HANDLING

This development is the next step towards meeting the requirements of our customers and the industry in future. The development of the patented Retainer Comb Handling (RCH) system provides a brand-new fully automated solution.

Patent number: AT515531 B1 2015-10-15 / DE 102015217132A1 / US 9,698,032 B2

Siconnex customized solutions GmbH (Hof bei Salzburg, Austria) has been an established and market-leading equipment manufacturer of manually loaded BATCHSPRAY® equipment for wafer processing for over 15 years.
The logical next step was to also become one of the leading suppliers of fully automated solutions for our existing customers and to use the great potential therein to gain new partners.

With our years of experience, the process chambers and all related components for BATCHSPRAY® Acid, BATCHSPRAY® Solvent & BATCHSPRAY® Clean equipment were familiar tasks. The BATCHSPRAY® Autoload, however, was a new challenge. We started with two main goals: simple design and optimum process performance. A summary of our implemented solutions from the engineer's perspective is as follows.

PROCESS PERFORMANCE "THE PROCESS ENGINEER'S VIEW":

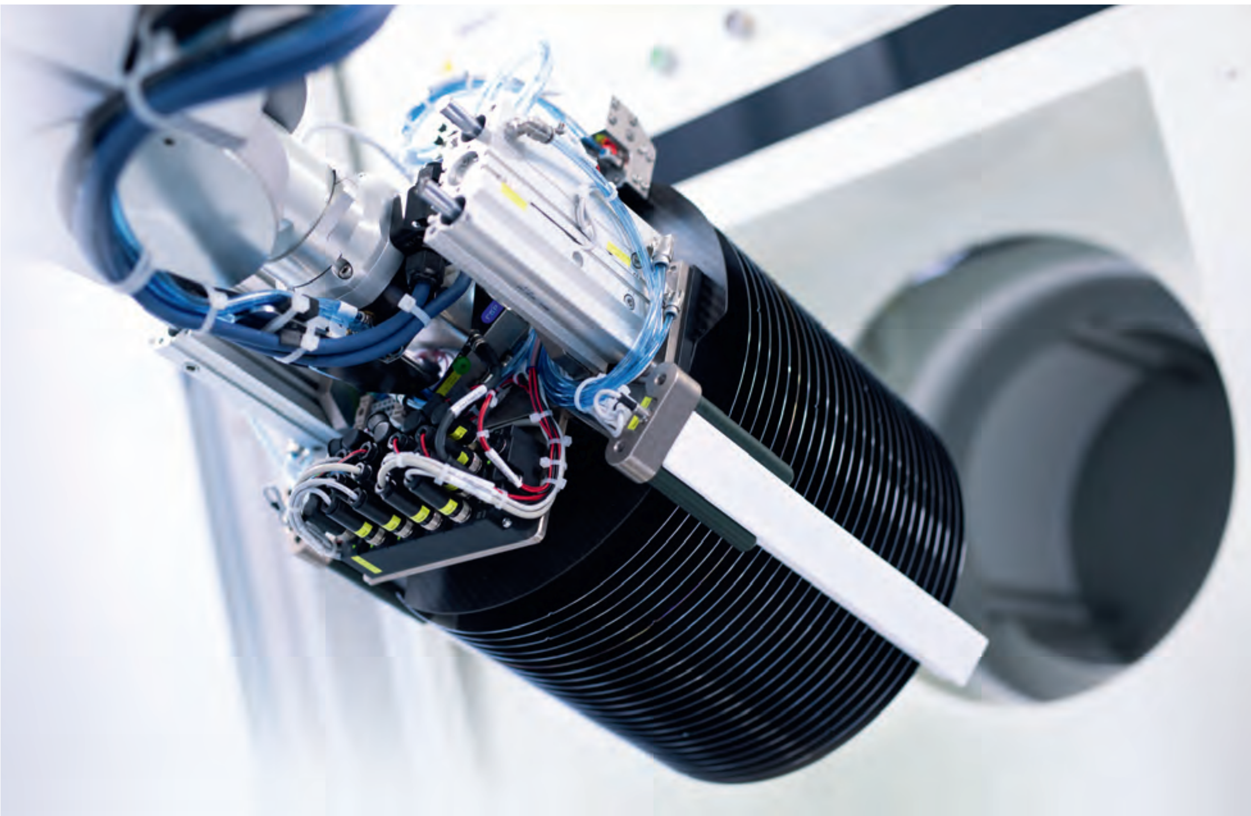
Getting the largest possible opening area is one of the key factors in getting optimum process results. Every part that interrupts the chemical spray during rotation can affect the uniformity result on the wafer. With our three independent retainer combs, we have created the best possible solution: an opening area of more than 80%. This value cannot be obtained with conventional systems.

Batches with lower quantities or empty slots are also a factor that had to be considered.

Wafers are only held by 3 retainer combs: the result is an opening area of more than 80%.

Wafers that are not shielded on the front or rear side can be affected differently by temperature or chemical exchange.
Therefore, we have the option to process the batch with shield wafers on both sides and with no empty slots between the wafers.

A compressed batch and shield wafers on both sides are beneficial for the process results.



Parts kept simple: nothing mechanical or moving in the process chamber. Replacement is quick and requires no teaching effort.

The shield wafer handling and compressing is done with the single-wafer handler included. Empty slots in the batch are filled with process wafers and the rear shield wafer is always placed in the first empty slot. Every wafer station in the BATCHSPRAY® Autoload is equipped with storage space for up to six shield wafers. In case of an endpoint detection system, a glass wafer can be used as front shield wafer.

The goal of high throughput values can only be reached when the process chambers are continuously in use. Therefore, we always have at least one empty wafer station which can be used to prepare the next batch during the running process. All preparations are finished before the process chamber is ready for unloading, and exchanging the finished batch with the newly prepared batch takes less than one minute. This can be easily achieved because we handle all process wafers in one step using the 25-wafer handler. The compressing is done with the single-wafer handler. After processing, every wafer is returned to its original slot.

SIMPLE DESIGN "THE HARDWARE ENGINEER'S VIEW":

All of the parts in the process chamber are exposed to the influences of different chemicals and temperatures. This is the reason why we kept the retainer combs as simple as possible. Each retainer comb is made of one piece and no mechanical or moving parts are necessary in the process chamber. All movements required for handling are made by the robot and the process handler.

Another reason for the wear of the retainer combs is the mechanical stress caused by the rotating wafers during processing. It is important to keep the effort required for a retainer comb change very low. With our design, the retainer combs can be changed quickly and without a teaching operation.

Every piece of equipment with rotating parts faces the same challenge with vibrations. Our three independent retainer combs allowed us to design the rotor considering the centre of mass, and the result is almost no vibration, regardless of the number of loaded wafers and the rotation speed.

The modular design that has already proven effective in our other BATCHSPRAY® equipment has also been incorporated. Assemblies like handlers or wafer stations are all built as modules, making upgrades or changes not only possible, but also faster and easier.

The BATCHSPRAY® Autoload is compatible with our BATCHSPRAY® Acid, BATCHSPRAY® Solvent & BATCHSPRAY® Clean equipment, all built in a modular design. The footprint is <11m².

TECHNICAL SUMMARY “THE FEATURES AND BENEFITS”:

- The BATCHSPRAY® Autoload is compatible with all Siconnex BATCHSPRAY® equipment.
- Retainer Comb Handling is available for 8” and 12”, both sizes with the same handling principle.
- For both diameters, the 25-wafer handler and the wafer station have been equipped with wafer detection sensors for continuous wafer tracking.
- Wafer stations always include two additional slots for shield wafers (27 slots for 12” & 52 slots for 8”) and storage slots for up to six shield wafers.
- Optionally, a second set of handlers can be included to operate either in left/right or dirty in/clean out modes.
- All common industry communication standards are supported (Gem300).
- The arrangements for fully automated fabs, hardware and software are included.
- For the six-axis robot, the best choice is a robot system provider that is well known in the industry.

These benefits, combined with the known advantages of our BATCHSPRAY® Acid, BATCHSPRAY® Solvent & BATCHSPRAY® Clean equipment, have already convinced some of the leading semiconductor manufacturers in the world, and more are sure to follow...

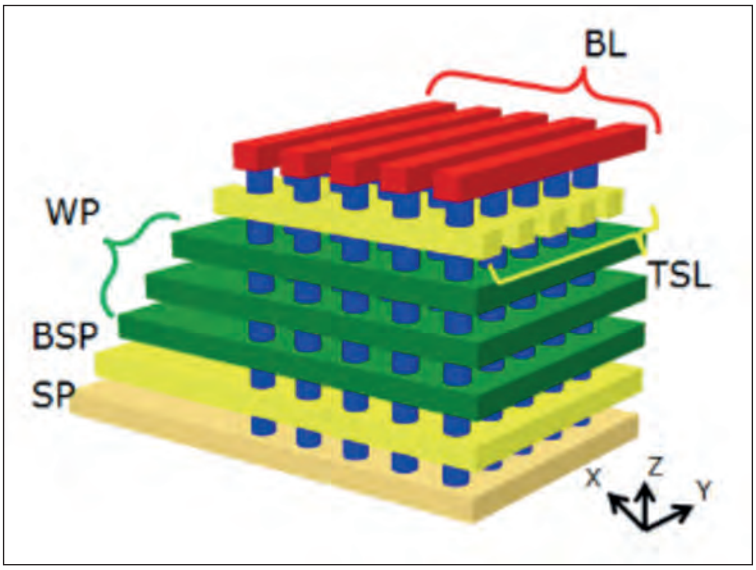
BATCHSPRAY® Autoload

The vertical ferroelectric FET: a new contender for 3D-NAND Flash memory and machine learning

Jan Van Houdt, Scientific Director at imec, explains how the FeFET works and how this exciting 'newcomer' might fit in the next-generation memory landscape.

FERROELECTRICS are a class of materials that consist of crystals exhibiting spontaneous electrical polarization. They can be in two states, which can be reversed with an external electric field. When such a field is applied, the electric dipoles formed in the crystal structure of the ferroelectric material tend to align themselves with the field direction.

After the field is removed, they retain their polarization state – giving the material its non-volatile characteristic. A ferroelectric material has a non-linear relationship between the applied electric field and the polarization charge, giving the ferroelectric polarization-voltage (P-V) characteristic the form of a hysteresis loop.



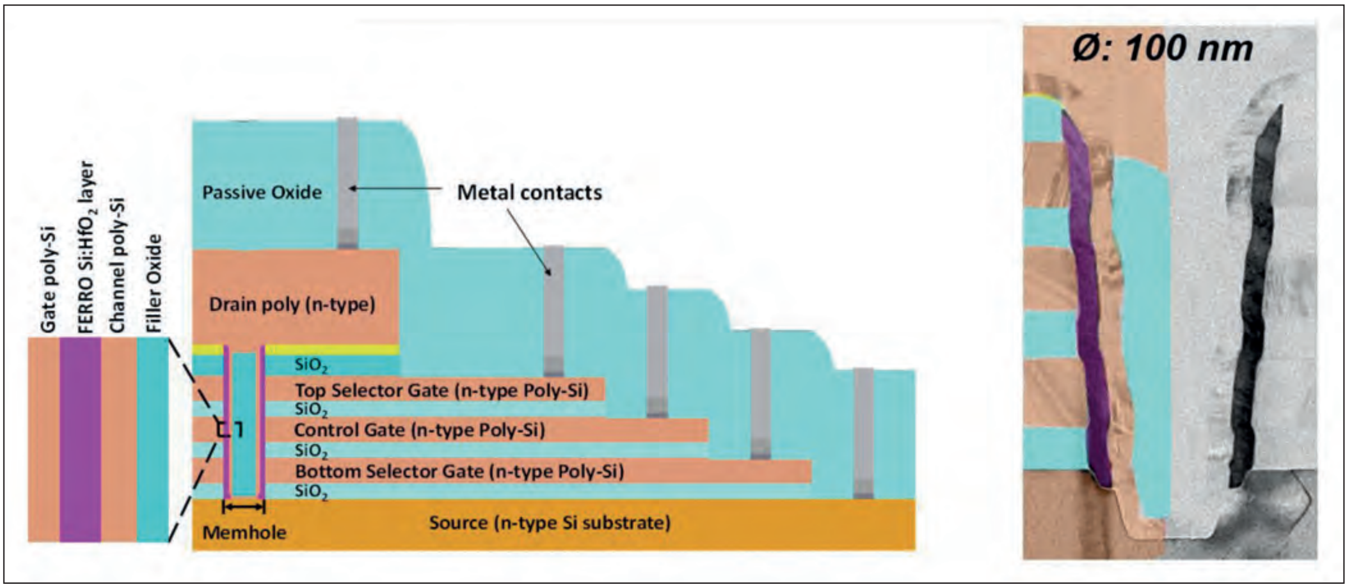
Schematic representation of a 3D-NAND Flash structure.

Ferroelectric materials are being explored for DRAM-like memory applications – with ferroelectrics implemented as the dielectric in the DRAM capacitor. But one can also think of replacing the gate dielectric of a standard high-k/metal-gate transistor with a ferroelectric and end up with a non-volatile transistor: the ferroelectric FET or FeFET. The two stable, remnant polarization states of the (now ferroelectric) gate insulator modify the transistor threshold voltage, even when the supply voltage is removed.

Accordingly, the binary states are encoded in the threshold voltage of the transistor. Writing of the memory cell can be done by applying a pulse on the transistor's gate which alters the polarization state of the ferroelectric material and impacts the threshold voltage. For example, applying a positive pulse lowers the threshold voltage and leaves the cell in an 'ON'-state. Reading is done by measuring the drain current. This type of memory operation resembles the working of a NAND Flash memory cell – where electrons are forced in and out of a floating gate, impacting the threshold voltage of the floating gate transistor in a similar way.

From dream to reality...

Discovered more than five decades ago, ferroelectric memory has always been considered ideal, due to its very low power needs, non-volatile character and high switching speed. However, issues with complex ferroelectric materials have presented significant challenges. Early attempts were based on ferroelectric



(Left) Schematic cross-section of the macaroni-type 3D FeFET with three cells in series; (right) TEM cross section (Ø: 100nm).

materials belonging to the perovskite family of lead-zirconate-titanate (PZT). But conformally depositing these materials in thin layers has proven very challenging. Also, the very high dielectric constant of these materials (in the order of 300) posed an obstacle for integrating them into a functional transistor. The recent discovery of a ferroelectric phase in hafnium-oxide (HfO_2), a well-known and less complex material, has however triggered a renewed interest in this memory concept.

Researchers discovered an orthorhombic crystal phase – the ferroelectric phase – that can be stabilized by doping HfO_2 with e.g. silicon (Si). Compared to PZT, HfO_2 has a lower dielectric constant and can be deposited in thin layers, in a conformal way. On top of that, HfO_2 is a well-understood material that has been used as the gate stack dielectric material in logic devices. By cleverly modifying this CMOS-compatible material, the logic transistor can now be turned into a non-volatile FeFET memory transistor.

... and from planar to vertical

Functional FeFETs have already been demonstrated in two-dimensional, planar architectures. But the ability to make conformal layers of HfO_2 opens the door towards vertical varieties, e.g. by depositing the ferroelectric material on a vertical 'wall' and stacking the transistors in the third dimension.

On the material side, these 3D FeFETs can solve some of the challenges imposed by 2D FeFET structures. One challenge has to do with the poly-crystalline nature of the HfO_2 dielectric. Scaling the dimensions of the HfO_2 layer significantly limits the number of crystal grains within the layer. Not all these grains have the same polarization direction, and this impacts their response on the external electric field – leading to large variabilities. By going 3D, this restriction is at least removed in the third dimension, relaxing the variability and allowing a better control of the statistics.

Vertical FeFET technology fits in a 3D-NAND-like manufacturing flow, an approach which has been actively pursued by imec. 3D-NAND Flash is today's mainstream medium for high-density data storage. 3D NAND is relatively cheap and non-volatile, but it has a complex structure and slow memory operation.

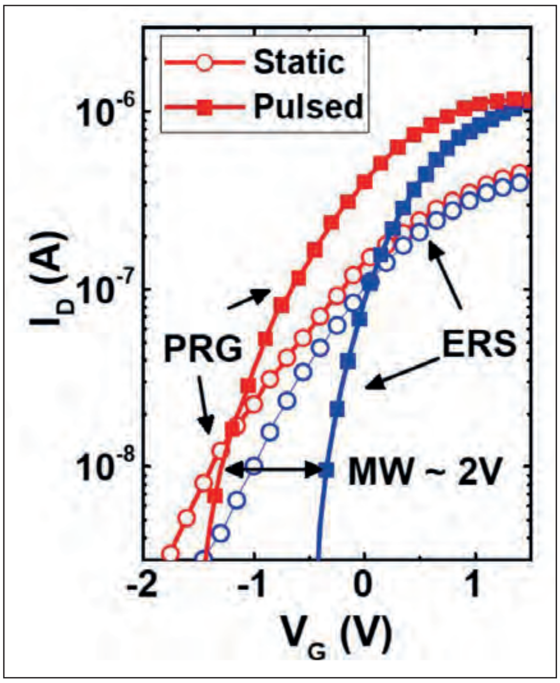
These vertical FeFETs are expected to present several advantages over complex 3D-NAND Flash memories, including more simplified processing, lower power consumption and higher speed. Compared to 3D-NAND Flash, vertical FeFETs can potentially be programmed at much lower voltages (at about 4V compared to 20V for NAND), which leads to improved reliability and scalability.

First results: 2V memory window and Flash-like endurance

Since several years, imec has been focusing on 3D-NAND-like vertical FeFETs, hereby using its longstanding experience in advanced 3D-NAND Flash technology development combined with the tools, background and vehicles developed for earlier research on PZT-based ferroelectric memories. Since 2016, imec and its partners have an industrial affiliation program running on vertical FeFETs.

In the frame of this program, the team tackles main challenges related to the processing, characterization and reliability of the 3D FeFET. For example, the imec team is building up the knowledge on how to stabilize the orthorhombic phase of HfO_2, which is the ferroelectric phase. This phase can be obtained by substitutional doping of the HfO_2 layer with silicon for example.

This generates a strain in the thin layer, bringing the crystal into the desired orthorhombic phase. Silicon is preferred as a dopant atom because of the thermal budget (i.e., to preserve the ferroelectric phase), but the team also studies alternative dopants such as



Memory characterization: up to 2V memory window was obtained after applying 100ns program (PRG)/erase (ERS) pulses.

aluminum (Al) and lanthanum (La), and investigates the use of hafnium-zirconium-oxide as an alternative ferroelectric.

Recently, imec demonstrated a first functional vertical ferroelectric HfO_2 FET based on a 3D macaroni NAND architecture. The device was fabricated based on imec's process flow for 3D-NAND Flash memories, now replacing the typical oxide-nitride-oxide (ONO) dielectric layer by an 8nm Si-doped HfO_2 layer – which is deposited using atomic layer deposition (ALD).

Poly-Si is used as the gate material, and amorphous Si for the channel. The test vehicle contains a vertical string of three gates in series (a control gate, and a bottom and top selector gate). The hole in the string is filled with oxide and then recessed, giving it a macaroni-like structure. In a real 3D-NAND-like device, the number of control gates can mount up to 64 in the vertical direction to obtain a high-density memory solution.

For this test vehicle, up to 2V memory window was obtained after applying 100ns program/erase pulses. The FeFET exhibits 85°C retention: after 100 hours at 85°C, a clear separation of states can still be observed. The team also reported Flash-like endurance of 104 cycles and has performed first reliability assessments. Charge trapping – caused by high fields over the interface – is put forward as the limiting factor for the cycling performance. A decrease of the interface layer thickness could potentially address this challenge.

3D-NAND-like applications and machine learning

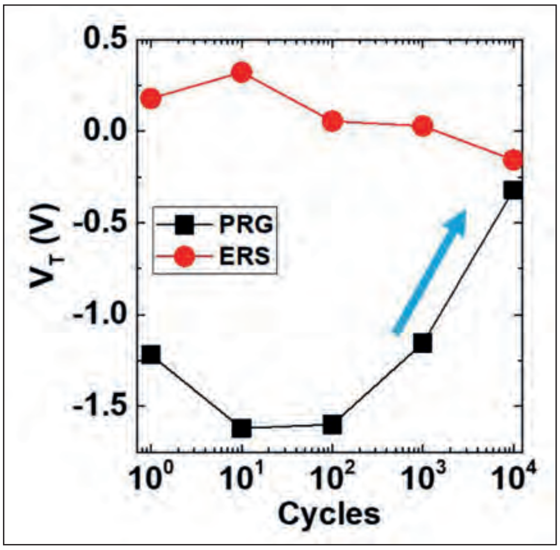
FeFETs are still in the early stages of R&D and it's too soon to say if or when they will ever make it into production. Nevertheless, this promising new memory concept has raised major interest from the industrial players. It is the role of imec to explore its full potential and offer its partners a head start in this exciting research area. They can then decide how to best fit FeFET memories in their products and chips.

As a standalone memory, FeFETs are believed to enter the family of storage class memories (SCMs) and as such help closing the gap between fast, volatile DRAM and slow, non-volatile and high-density NAND Flash memories. FeFETs are non-volatile and can offer several advantages over NAND Flash: they have faster switching speeds, are simpler to process, consume less power and can potentially operate at much lower voltages. But, although closer to DRAM in terms of speed, the limited cycling performance (104 for FeFET compared to 1012 for DRAM) will most probably push FeFETs to the NAND side of the DRAM-NAND gap.

FeFET memories have also gained interest among the logic foundries: the memory's high speed can be very advantageous for machine learning applications, which rely on in-memory computing. For this, several types of memories, including Flash, magnetic random access memory (MRAM), resistive RAM, phase change memory (PCM), static RAM (SRAM) and FeFET, are currently being explored. The non-linear characteristics and speed properties of FeFETs make the technology particularly appealing for machine learning applications that make use of deep learning convolutional neural network models. For this application, we will most probably see planar versions of FeFETs coming up.

Outlook: towards higher density FeFETs

A particular advantage of NAND-Flash technology is



Reliability characterization: Evolution of the threshold voltage VT with cycling after program and erase. Closing of the memory window is observed after 104 cycles.

As a standalone memory, FeFETs are believed to enter the family of storage class memories (SCMs) and as such help closing the gap between fast, volatile DRAM and slow, non-volatile and high-density NAND Flash memories

the ability to store up to 4 bits per cell, which gives the technology its unique high data density. In a traditional single-level cell, each cell can be in one of two binary states, storing one bit of information per cell. Industrial NAND-Flash cells have evolved from single-level cells to cells with 2, 3 and even 4 bits per cell. With 4 bits, the cells use 16 discrete charge levels in each individual transistor – requiring a sufficiently large memory window.

For FeFETs, imec sees three ways to increase the data density and make FeFETs true competitors for NAND Flash in terms of density. First, provided that the threshold voltage can be sufficiently stabilized, the 2 – 2.5V memory window of FeFETs should in principle allow programming 2 bits per cell – which requires 4 charge levels within the transistor.

Second, the cell density can be doubled by using a trench-like architecture for connecting the transistors, with two transistors on each side of the trench. In current 3D FeFET designs, such as in imec's macaroni NAND architecture, the control gate is designed in a gate-all-around (GAA) structure. This means that the gate is wrapped around the channel, limiting the number of transistors (per layer and per string) to one.

The GAA structure is needed in NAND Flash memories to improve the injection of charges into the floating gate or the nitride trapping layer but is not needed for FeFETs. Imec is currently exploring the use of an alternative trench-like structure, where the transistors are implemented at the sidewall of a trench – with two transistors now at opposite ends of the trench. This type of structure should potentially allow doubling the cell density while decreasing the variability between cells.

And third, the FeFET memory cell can potentially be scaled to much smaller physical dimensions. In a typical NAND Flash cell, the ONO dielectric layer has a thickness of about 20nm. In a FeFET cell, the HfO_2 ferroelectric layer is expected to scale down to 4nm. In addition, in the vertical direction, the lower operation voltage of the FeFET compared to NAND Flash will allow the word lines to come closer together.

In summary, these possible routes towards higher density in combination with a higher speed, non-volatile, Flash-like endurance, lower operation voltage and lower power consumption make 3D FeFETs interesting contenders for 3D NAND-like applications.

Want to know more?

The paper 'Vertical ferroelectric HfO2 FET based on 3D NAND architecture: towards dense low-power memory' by K. Florent et al. was presented at the 2018 IEDM conference, and can be requested via our contact form.

If you want more information on ferroelectric memories, you can request the following papers via our contact form: (1) 'Memory technology for the terabit era: from 2D to 3D', Symp. on VLSI Technology, Kyoto, Japan, June 2017, invited, p. T24-25; (2) '3D memories and ferroelectrics', 2017 IEEE-IMW, Monterey, CA, invited, p. 92-94.

About Jan Van Houdt

Jan Van Houdt received a Ph.D. from the KU Leuven. During his PhD work, he invented the HIMOS™ Flash memory, which he transferred to several industrial production lines. In 1999, he became responsible for Flash memory at imec and as such was the driving force behind the expansion of imec's Industrial Affiliation Program on Memory Technology. Jan has published more than 300 papers in international journals and accumulated more than 250 conference contributions (incl. ~50 invitations and 5 best paper awards). He has filed about 80 patents and served on the program and organizing committees of 10 major semiconductor conferences. In 2014, he received the title of IEEE Fellow for his contributions to Flash memory devices. In the same year, he started the Ferroelectrics program at imec and became a guest professor at the KU Leuven teaching on CMOS and memory technology. Today, he is Scientific Director at imec, active both in the memory as well as in the logic scaling programs.

Surrounding the molecule:

A comprehensive approach to gas delivery excellence

You can rarely see, smell, or sense them. And yet, they are essential to the processes that make so many innovations possible.

BY APPLIED ENERGY SYSYTEMS

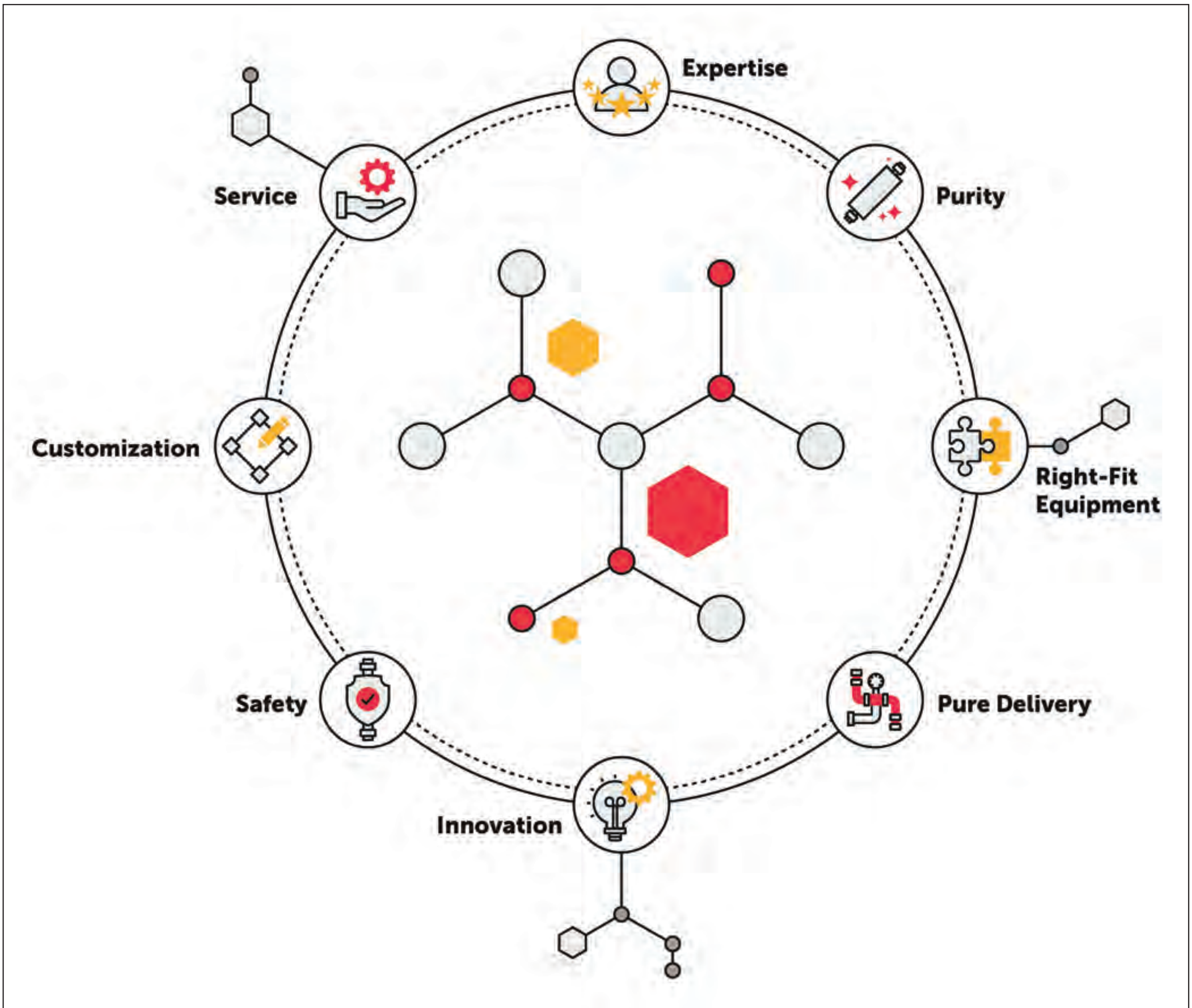
IN APPLICATIONS like semiconductor fabrication, electronics manufacturing, aerospace, laboratory research, and more, high and ultra high purity gases are central to process integrity. For the most precise applications, even a trace impurity can be detrimental to output.

At Applied Energy Systems (AES), the high and ultra high purity molecule is at the center of our work, just as it is at the center of your processes. We work diligently to "Surround the Molecule" with everything innovators need to ensure pure gas delivery for process excellence. Here's how:

Surround the molecule with expertise.

A defining element of any gas delivery system is the partner who delivers it. Specifically, a partner's expertise, commitment to excellence, and spirit of collaboration are all essential to ensuring the pure molecule is stewarded from storage to point-of-use. With more than 50 years solely focused on upholding rigorous purity standards, AES leverages an unrivaled level of expertise with every gas delivery system we engineer, whether standard or custom.
Our team is comprised of seasoned experts that understand the most intricate nuances of pure gas delivery, and we extend this knowledge on-demand to every client. Our clients view us as collaborators, focused on meeting the unique requirements of each and every molecule.

Our knowledge enables us to understand the why behind the what and, as a result, adds value to every engagement. This expertise is the first circle of protection "Surrounding the Molecule" and permeates all of the solutions and services we provide.



Surround the molecule for purity.

The next layer "Surrounding the Molecule" is purity. Yes, pure gas is by its very nature free of contaminates. But surrounding the molecule with purity means far more than that. The process gas in one application may actually be the targeted impurity in another.

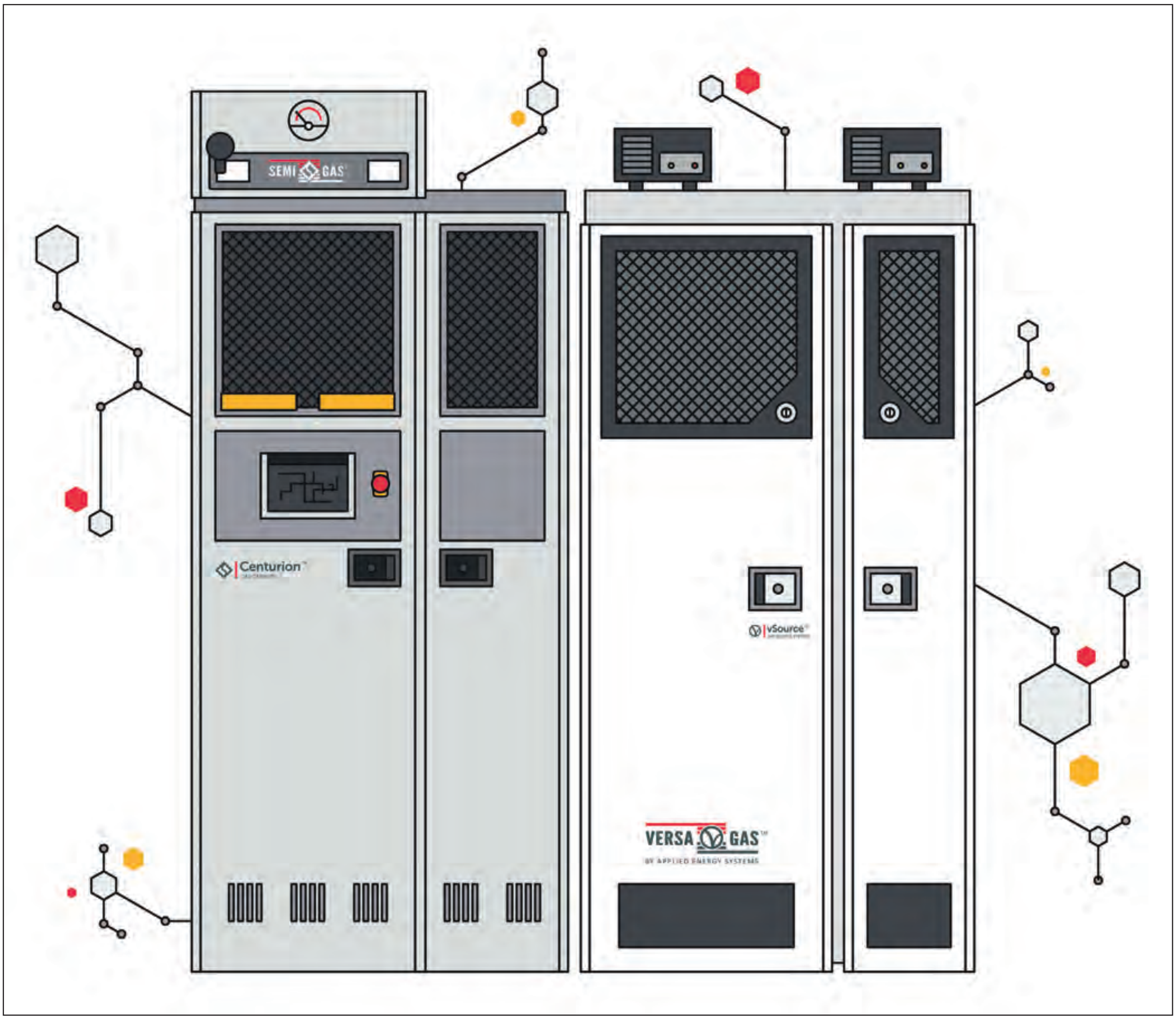
In order to truly master purity, gas delivery equipment and systems must be designed with an understanding of each application's exacting purity requirements, including process gas, potential contaminates, desired level of purity to the ppbv or pptv levels, and the kind of technology required to achieve the targeted results.

With a rigorous standard for purity and potentially dire implications should contamination occur, the application environment is no place for experimentation. That's why we replicate application conditions in our very own facility to affirm the performance of our high and ultra high purity gas delivery systems.

In addition to expert equipment evaluations and rigorous QA testing areas, our campus is home to Class 100 and Class 10,000 cleanrooms which ensure that our standard of purity matches that of our clients.

Surround the Molecule with Right-Fit Equipment. Comprised of myriad mission-critical components working in perfect harmony, gas delivery systems are among the most vital pieces of equipment in the application environment. The purity and safety standard of the system as a whole can be compromised by the shortcoming of a single component. As a result, it is not only desirable but essential that a gas delivery systems provider specialize in all parts of the system – from the cabinet, to the controller, to the purifier.

Wholly focused on gas delivery systems, AES ensures the quality and reliability of every component. Our ultra high purity SEMI-GAS® and high purity VERSA-GAS™ equipment lines have been accommodating



the complex and stringent purity requirements of AES customers for decades. Our family of controllers provides precise operator control while enabling Industry 4.0 applications.

Last, but not least, our ARM Purification division provides a robust family of Point-of-Use, Micro-Bulk, and Bulk purifiers to satisfy the full range of purification demands. From this comprehensive portfolio, customers can select the system solutions and services that best fit their process gases, requirements, and budgets – and benefit from working with a single provider for their range of gas delivery equipment needs.

Surround the molecule for pure delivery

A gas delivery system is only as good as its ability to bring pure gas to the ultimate point-of-use. The next layer around the molecule, therefore, is the ultra high purity process piping that carries mission-ready pure gas from source equipment through the application environment and to your process tools.

AES delivers high and ultra high purity process piping services that are tightly integrated with our systems-level expertise. Whether working in cleanroom, space-constrained, underground, or outdoor environments, AES installs and quality assures process gas lines, exhaust lines, tubing, and interconnecting lines with complete analytical testing.

surround the molecule with innovation

With data becoming ever-more pervasive in the manufacturing environment, it is critical that technology "Surrounds the Molecule." As application complexity rises, so too must the commitment to leveraging technology in order to more effectively maintain, monitor, and measure gas purity conditions.

With data becoming ever-more pervasive in the manufacturing environment, it is critical that technology "Surrounds the Molecule." As application complexity rises, so too must the commitment to leveraging technology in order to more effectively maintain, monitor, and measure gas purity conditions

In addition to harnessing a range of purification technologies – including getter, catalyst, and adsorber – we are also focused on delivering systems that support the connected nature of today's applications. For example, our SCADA-ready control technologies enable innovators to integrate their gas delivery systems into their Industry 4.0 facilities. With a long track record serving Tier 1 innovators, we remain committed to employing the latest technologies in order to keep our customers ahead.

Surround the molecule for safety

Along with the purity of the molecule, it is equally important to ensure the safe operation of the system. In many applications, hazardous gases have a high risk of combustion when exposed to other materials. In high pressure applications, a system compromise could result in dangerous explosions. No matter the application, safety should be a top priority.

Each of our gas delivery systems is equipped with an exhausted enclosure, a fire detection system, a sprinkler system, and both local and remote emergency shutdown protection. Furthermore, our systems include safety alerts should performance fall outside of specifically defined thresholds.

Surround the molecule with customization

While standard solutions satisfy a diverse range of requirements, rising application complexity often necessitates customization. By synergizing specialized engineering capabilities with our vast scope of product offerings, AES is able to tailor our core systems to create adapted, custom Applied Solutions that meet specific gas delivery requirements.

Our Applied Solutions process begins with an in-depth understanding of application needs, and continues through engineering design, production, in-house validation, and installation—building the solution around the unique requirements in every phase.

Surround the molecule with service

The commitment to "Surrounding the Molecule" must continue well beyond system delivery, throughout the lifecycle of the gas delivery system. Through our Applied Services division, we demonstrate our commitment to serving customers as a trusted and reliable field resource.

From analytical testing and installation, commissioning, and training, to ongoing maintenance and servicing, our full lifecycle approach to services ensures reliable access to pure molecules—today and over time.

The molecule lives at the center of our mission – it's true. But equally central to our mission is our customer. Our service-focused approach enhances responsiveness, collaboration, and ultimately, value for every customer with the need for pure process molecules.

KLA steers tech for automotive IC power applications

Silicon Semiconductor technical editor Mark Andrews speaks with Robert Cappel, Senior Director of Marketing, about advances that KLA Corporation has made to enable defect reduction and quality improvement processes for automotive applications. As chip makers go after new auto IC opportunities they face challenging reliability and performance standards up to 10 times those of consumer electronics

MA – *Auto electronic systems present unique challenges for IC manufacturers due to quality and lifetime requirements that are years longer than consumer electronic device standards. Please describe the landscape they are entering*

RC – Process control requirements for automotive electronics are extremely stringent and much greater than for business and consumer grade products like laptops and mobile phones. While an acceptable failure rate for consumer type products might be 10% within the first two years, automotive requirements are significantly tougher. As semiconductors are now a critical part of Advanced Driver Assistance Systems (ADAS) that are critical to the function and safety of the vehicle, failures cannot be tolerated. The rapid push of the automotive industry to incorporate autonomous driving features, and the eventual transition to fully autonomous driving, further drives the needs for all the semiconductor chips to work perfectly together to protect the safety of both the car's occupants and others in the surrounding environment. This is the biggest driver of a requirement for zero defects in parts per billion within the automotive semiconductor industry today and in turn has increased the emphasis on strategies to handle stronger process control requirements.

MA – *How can KLA systems help device manufacturers new to the automotive market succeed?*

RC – The bulk of automotive devices have historically been manufactured at established 200mm fabs with design rules of 65nm or above, or to a lesser degree, in mature 300mm foundries. Manufacturing processes in these fabs are well characterized and established. The move to smarter, connected and autonomous cars will require additional computational power that cannot be served by these older devices. The need for advanced technology, as well as more manufacturing capacity, will speed the migration of automotive capacity to advanced logic foundries.

Anticipating this trend, foundries are already gearing up to serve 14nm SOCs (system on a chip) in the automotive space, with even smaller automotive chip designs in preparation. These newer processes have not enjoyed the lengthy time (years) to mature compared to many of the larger design node automotive chips currently in use, and therefore, will still suffer from baseline yield challenges and excursions. Manufacturers using methods that are better suited to consumer mobile devices, where 10% failure rates from reliability issues is acceptable, will result in unsatisfactory reliability for automotive grade parts. This increased quality requirement has been creating additional pressure on fabs new to the automotive space to ramp to extremely mature yields even faster than before, with much lower defectivity levels than with advanced consumer grade parts. KLA's inspection and metrology process control systems and strategies are the enabling technology to enhance this necessary yield learning. KLA works with these new customers in a collaborative effort to help them define inspection and metrology requirements, and then develop sampling strategies to reduce overall defectivity, which in turn drives down potential reliability failures.

MA – *For established auto device IC manufacturers, what changes are coming to the market and how are market expectations changing? How does KLA address these challenges?*

RC – Automotive semiconductor manufacturers are adopting a new mentality focused on increased quality to prevent chip reliability issues in the field. For example, general continuous improvement programs reduce the random defectivity introduced by process tools, while more stringent characterization and monitoring strategies also ensure that the process tools are in top operating condition. With a Zero Defect focus, fabs can no longer settle for "good enough" or traditional yield optimization. The quality mentality will need to shift to "the best possible" – running the processes under the best possible conditions in order to achieve strict reliability goals. This quality mentality may increase fab costs in the short term but will result in long term savings from delivering the higher reliability IC chips required by automakers.

When looking at automotive semiconductor best known methods, the defect pyramid (figure 1)

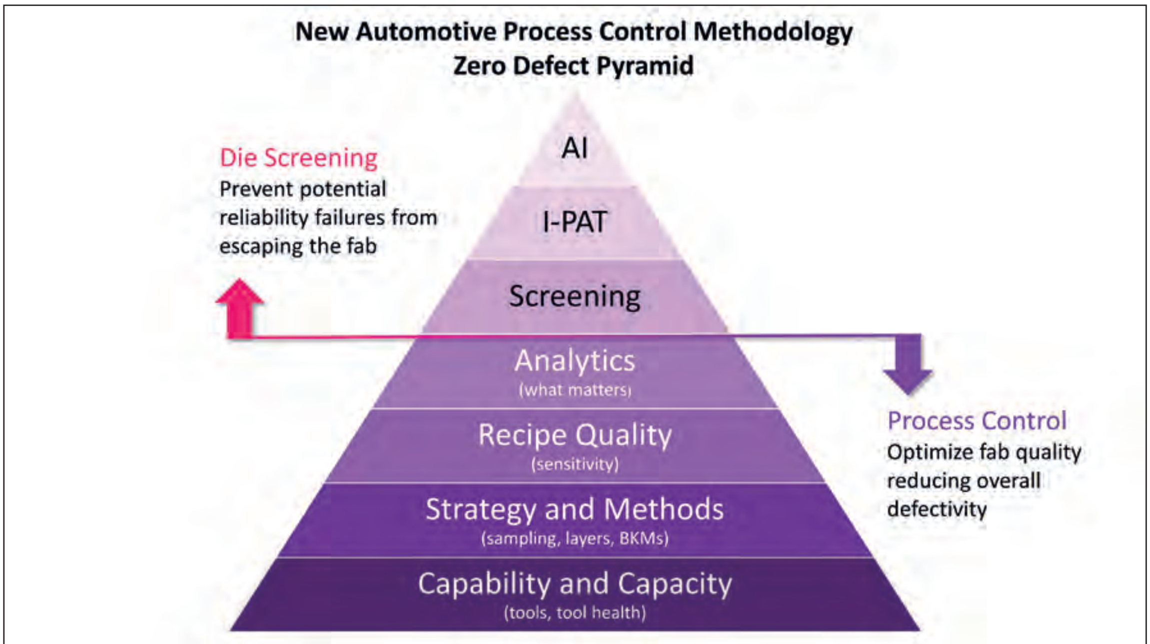


Figure 1: New automotive process control methodology Zero Defect pyramid

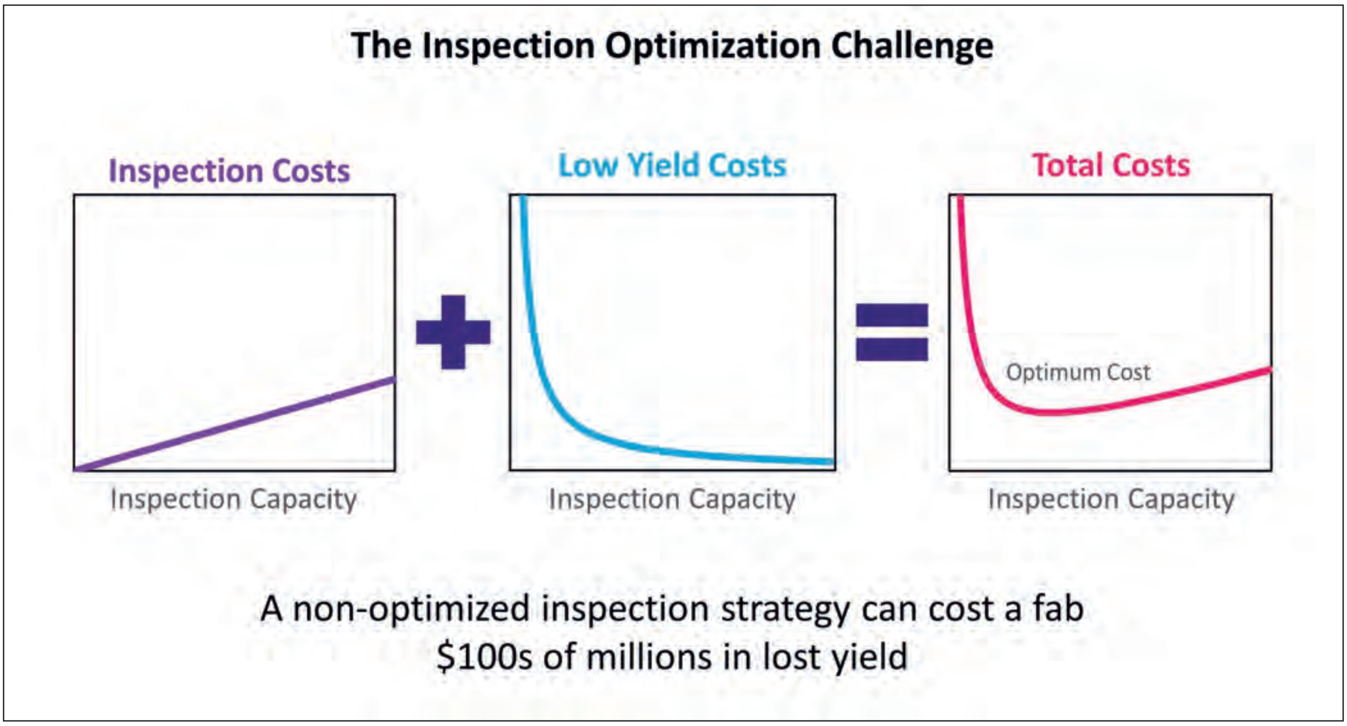
provides a blueprint for the types of strategies needed for success in producing automotive grade semiconductors.

As shown, the optimal base is to start with having the best performing process control tools in place. An effective way of finding and removing chips with latent reliability defects is to increase parametric and defectivity margins. Increasing parametric margins means requiring that the chips not only function, but also operate within a tighter parametric window. Increasing defectivity margins means setting the acceptable defect size to be smaller than what has been proven to be yield-killer defects. For a fab to find more subtle parametric variations or smaller defects, fabs need to implement higher sensitivity process control strategies – either by increasing the recipe sensitivity or by utilizing inspection and metrology systems designed to detect smaller defects or variations. With more capable process control systems, automotive fabs can detect, monitor and control the latent defects that might otherwise cause premature chip reliability failures.

The next approach is to manufacture fewer overall defects by closely controlling the process and employing continuous improvement programs that reduce the random defectivity introduced by the process tools or environment. This approach requires the fundamental baseline yield improvement techniques of tool monitoring (equipment may include Surfscan® unpatterned wafer and Puma™ patterned wafer inspection systems) and defect discovery or root-cause partitioning (equipment may include 39xx/29xx broadband plasma patterned wafer inspection systems) that fabs have utilized for years, but have now taken to a new higher standard to provide the absolute best in class tools for sensitivity, accuracy, reliability and matching. The approach also requires that the process is sampled frequently enough to provide traceability. When the inevitable process excursion happens, Zero Defect fabs know definitively where the problem started and stopped and can quarantine the affected parts until they can be effectively dispositioned or culled. The combination of the two requirements has resulted in the automotive fabs adopting process control tools at a higher rate, as well as using tools designed with sensitivity for one design rule node more advanced than they are manufacturing, so they can detect the smaller defects that may affect reliability.

Finally, a method that is receiving increased interest is to utilize inline defect information not only to control the process, but to identify die at risk for reliability problems while they are still in the fab--where the cost of correcting the problem is the lowest. Automotive fabs have long relied on "screening" where a high throughput tool inspects 100% of the die on all wafers at a handful of final layers late in the process. Die that meet the defined failure criteria (defect size/type/location) are excluded or "inked." While effective for large defects, this method is inadequate alone for smaller latent reliability defects. A new inline technique, called I-PAT™ (Inline Parts Average Testing), may be the answer. It leverages a 20-year-old automotive industry technique known as Parametric Parts Average Testing (P-PAT). This original e-test based method identifies any die whose test results lie outside of the normal distribution of the population, even if they are within the operating specifications. For a small sacrifice of 0.5-2.5% of yield, significant

Figure 2: The inspection optimization challenge



improvements in reliability are gained, with some automotive fabs seeing 20-30% improvement when the outlier die are culled. I-PAT moves this concept inline using massive data sets and artificial intelligence to identify die with outlier defect populations across the multiple steps within the manufacturing process. The outlier die are statistically more likely to contain the latent defects that the industry desperately wants to eliminate. I-PAT results could be used to cull these at risk die to improve the overall go/no-go decision for die.

Automotive quality standards are driving the combined requirements for additional sensitivity to small reliability defects. Faster yield learning cycles resulting in higher overall yield levels at advanced design rules and increased sampling for continued traceability all point to the value of process control in the automotive space. Additionally, the introduction of I-PAT will help automotive semiconductor suppliers better utilize their process control equipment to identify the latent defects that are a top priority.

MA – *Please describe KLA's specialized inspection systems for SiC substrates as well as processing within GaN-on-silicon manufacturing flows that target present and future requirements for automotive power devices?*

RC – SiC power devices pose unique yield and cost challenges in comparison to Si-based devices. Some of these challenges include:

- Much higher intrinsic material defect densities than Si-based devices
- High level of defect transference from substrate to epitaxy to device fabrication
- Variation in quality among substrate suppliers. Wafers graded and sold by dislocation density.
- Key defect issues include both crystallographic and morphological defects (carrots, surface triangles and stacking faults)
- Defect mechanisms act in the z-direction instead of x/y-plane.

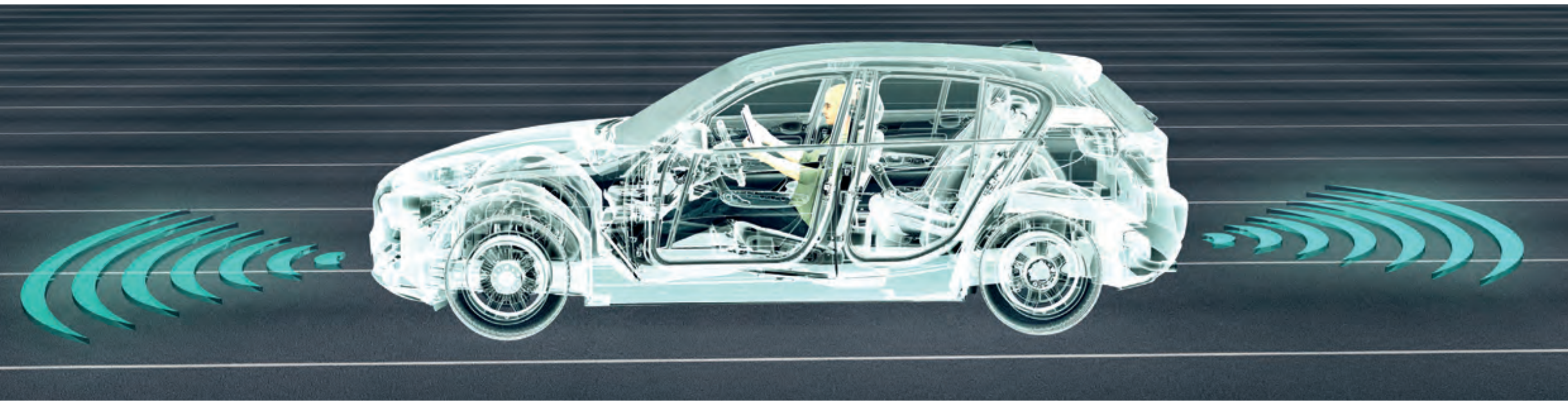
KLA's Candela 8720 compound semiconductor material surface inspection system and the 8 Series patterned wafer inspection system have been developed to address these challenges. The Candela® compound semiconductor material surface inspection system enables GaN-related materials,

GaAs substrate and epi process control with high sensitivity to critical defects for the production of power devices, communications and RF devices, and advanced LEDs (as well as upcoming micro LEDs).

With its proprietary optical design and detection technology, the Candela inspection tool utilizes signals from scatterometry, reflectometry, ellipsometry, slope and photoluminescence detectors to detect and classify yield-limiting, sub-micron defects to support production-line monitoring. The Candela 8720 system is used to monitor the substrate IQC (incoming quality control) and OQC (outgoing quality control) processes for a variety of defect types including particles, scratches, stains, pits, micropipes, stacking faults and other crystallographic defects. For the post epitaxial growth process step, the inspection system can detect and monitor process issues such as cracks, macro epi disturbances (such as droplets), epi pit, epi bump, crystal-oriented defects (such as single/bar stacking faults, BPDs, etc.), micropits and particles. Defects in the substrate and post epi growth can significantly impact end of the line yield, so detecting and correcting such process issues at the source – where cost is the lowest – is critical.

Patterned wafer inspection of SiC semiconductor devices is important for reducing defectivity and maintaining traceability, but inspection can present several unique challenges. Wafer thickness and warpage are outside typical SEMI standards. The transparent (SiC) substrate can create challenges

Automotive quality standards are driving the combined requirements for additional sensitivity to small reliability defects. Faster yield learning cycles resulting in higher overall yield levels at advanced design rules and increased sampling for continued traceability all point to the value of process control in the automotive space



for focus systems and create unwanted noise when imaging the wafer. The 8 Series patterned defect inspection tool addresses these challenges through a specialized prealignment and chuck, selectable illumination wavelengths and depth of focus for inspection, multiple inspection channels and increased wafer handling flexibility.

With simultaneous brightfield and darkfield inspection capability, it captures all types of surface defects with a multi-level defect binning solution. With optional backside inspection capability, the 8 Series system can handle and inspect both frontside and back side of 6" SiC pre- and post-grind wafers offering high precision frontside to back side correlation and die inking for process-induced killer defects on both sides of the wafer.

It is important to note that beyond some of the early SiC process steps, the many remaining steps for SiC are very similar to a standard silicon chip process, so SiC fabs will utilize similar process control strategies compared to silicon IC fabs.

MA – *Automotive ICs and packaged products can present production challenges beyond higher reliability such as the need to produce spare parts for years longer than consumer electronics. How does KLA technology help device manufactures meet these critical needs?*

RC – Automotive fabs have faced this problem for years and they do it by maintaining the process control strategies and standards that they used successfully in the past. This is shown through the defect pyramid referenced earlier. In order to help maintain these strategies along with the best performing tools, KLA works with our customers in two areas:

- KLA helps customers by making continuous improvements on the process control platforms through product upgrades.
- KLA provides an extensive service package that helps our customers ensure that the process control tools are performing at the highest levels.

In addition, KLA also offers metrology and inspection tools that enable component sorting to prevent defective devices arriving at the assembly line and to keep track records of each device. Metrology helps verify whether device dimensions are within tolerance and thus confirming the quality of packaged products; inspection verifies that there are no particles, burrs or other defects present that could impact the yield.

MA – *IC manufacturers accustomed to serving non-automotive applications focus on increased yield at lower costs; there is typically no heavy emphasis on long-term reliability. Is it possible to 'have it all' – to keep yield high at low cost while substantially improving quality and long-term reliability?*

RC – There are always going to be trade-offs when looking at scenarios where risk tolerance is the biggest factor in making these decisions. Do I sacrifice equipment capital costs or the costs of lost yield and reputation? Most choose to err on the side of caution as generally the costs of lost yield far outweigh the costs of additional process control. Lost yield or reliability failures that result from a process with lower yields cost significantly more than inspection costs as shown in figure 2. But more importantly, these failures can cost fabs critical contracts within the automotive ecosystem that typically are never regained. Auto OEM's and Tier 1 companies don't want to take on the risk of a fab that produces parts that fail.

MA – *As electric vehicles increasingly enter mainstream product lines, what special challenges are seen in the shift from traditional mechanical cars to EVs for IC manufacturers pursuing this emerging market?*

RC – As more electric vehicles are introduced into the market, a significant challenge with this transition is the move to SiC and GaN materials for power applications. This is highlighted in the previous question regarding SiC solutions. Another challenge from increased electrification and electronic content in modern vehicles is the continued growth of semiconductor content within the car. IC manufacturers that want to participate in this fast-growing market will need to meet the new stringent quality requirements.

Enabling smart manufacturing in the sub-fab

The Industry 4.0 movement is rapidly becoming the de facto means to optimize cost-effective manufacturing. The experts at Edwards Vacuum are demonstrating proven methods that can rapidly reduce costs while improving uptime by utilizing smart manufacturing techniques in a part of the fab that manufacturers don't always consider first when pursuing a healthier bottom line.

BY ALAN IFOULD, ERIK COLLART, ANTONIO SERAPIGLIA, AND MICHAEL MOONEY FROM EDWARDS VACUUM

IN THE BROADEST TERMS, smart manufacturing refers to collecting data from all aspects of the manufacturing process and by using advanced analytical and modeling capabilities, like artificial intelligence and machine learning, process performance and productivity are improved. It has been embraced by manufacturers in all industries and hailed as the fourth industrial revolution (Industrie 4.0). Semiconductor manufacturers have a long history of collecting and analyzing process data, a key smart manufacturing concept, to improve performance in the fab. Now semiconductor manufacturers are realizing the potential benefits of extending smart manufacturing technologies to the support systems housed in the sub-fab.

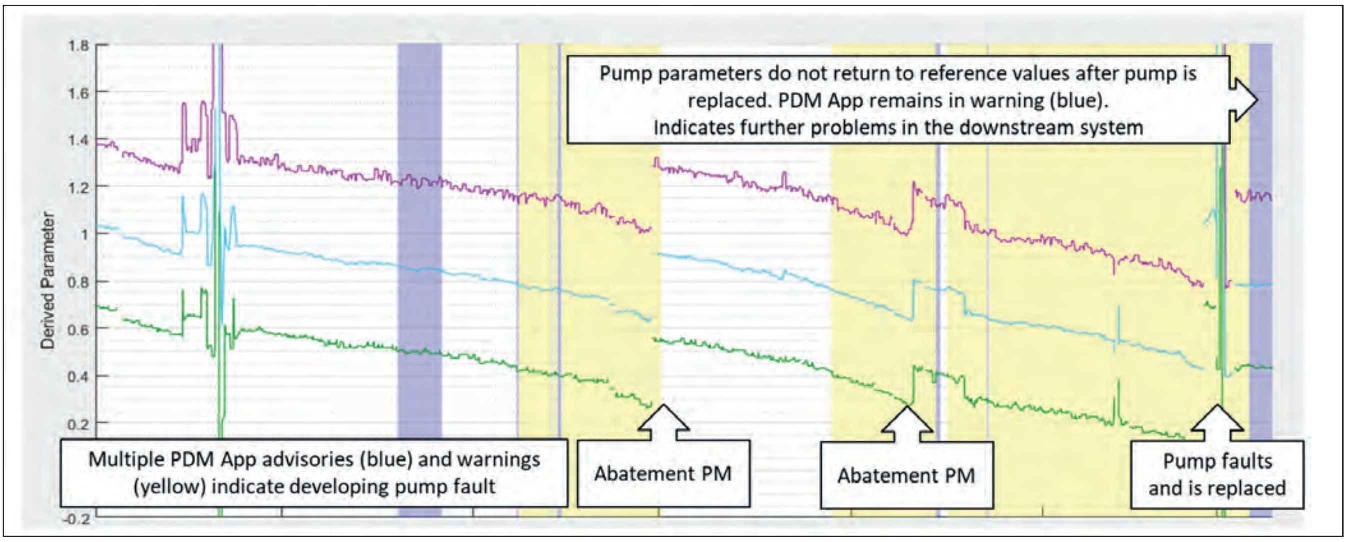


Figure 1: Output from a predictive maintenance application (PdM app) monitoring a vacuum pump

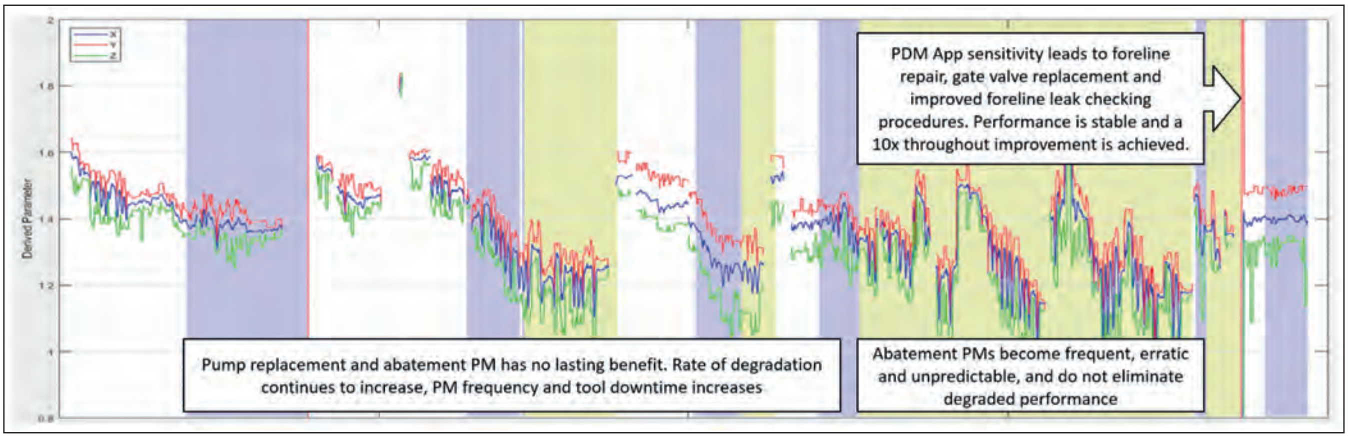


Figure 2: PdM data from a process tool in an HVM environment was delivering only 10% of the wafer throughput of other comparable tools

Driven by recent developments in the fields of sensors, data management, analytics and artificial intelligence, a new vision for manufacturing has emerged. This vision includes integrating supply chains; creating virtual factories with cyber-physical systems and digital twins; using big data techniques to interrogate tool, process, yield and facility data; and accumulating and applying critical domain knowledge.

Smart manufacturing is a broad concept that is perhaps best generally described as combining technologies and solutions to optimize operations by reducing and/or managing risk and uncertainty. In more practical terms, it is using big data infrastructure and information technology to provide advanced analytics and create a knowledge network of subject matter expertise and operational excellence models. It connects people, machines and processes in a more effective way.

Semiconductor manufacturers have been using advanced automation and statistical control techniques for a long time. As fabs have become more expensive and the cost of unexpected downtime has increased, they have enhanced their capabilities using smart manufacturing concepts. They are also extending them to the critical process support systems found in the sub-fab. The sub-fab has evolved dramatically over the years, from what was originally simply a location outside the fab in which to house supporting equipment, to an environment that is in many ways as sophisticated as the fab itself. A typical HVM fab, starting 40,000 wafer per month, may have 1,500 process tools. It's sub-fab will have 2,000 vacuum pumps and 1,000 abatement systems plus other ancillary systems. Most of the critical steps in a chip manufacturing process require high vacuum conditions and the unexpected failure of a pump can bring significant disruption to the manufacturing process, imposing heavy penalties in lost productivity and scrapped product.

Smart manufacturing in the sub-fab enhances vacuum security with comprehensive monitoring of process critical vacuum and abatement equipment. Using specifically designed models and algorithms, it can predict catastrophic failure modes related to hazardous process chemicals, high flowrates of flammable gases, ingestion of solid materials and condensation of liquids and solids. It can also deliver

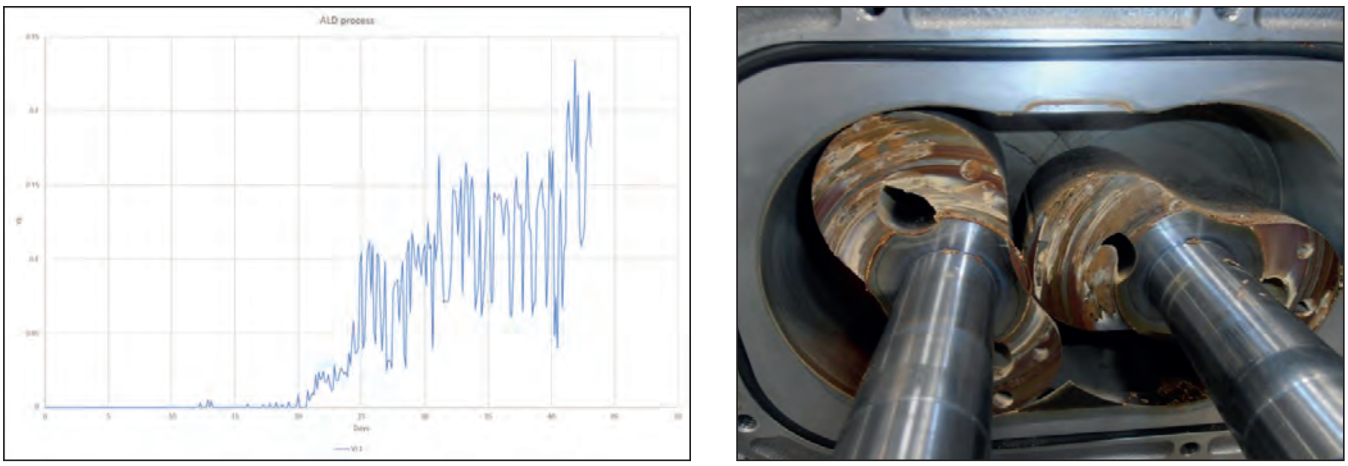


Figure 3 Vibration signal from a pump on an atomic layer deposition tool (left) and a photo of material deposited on internal components.

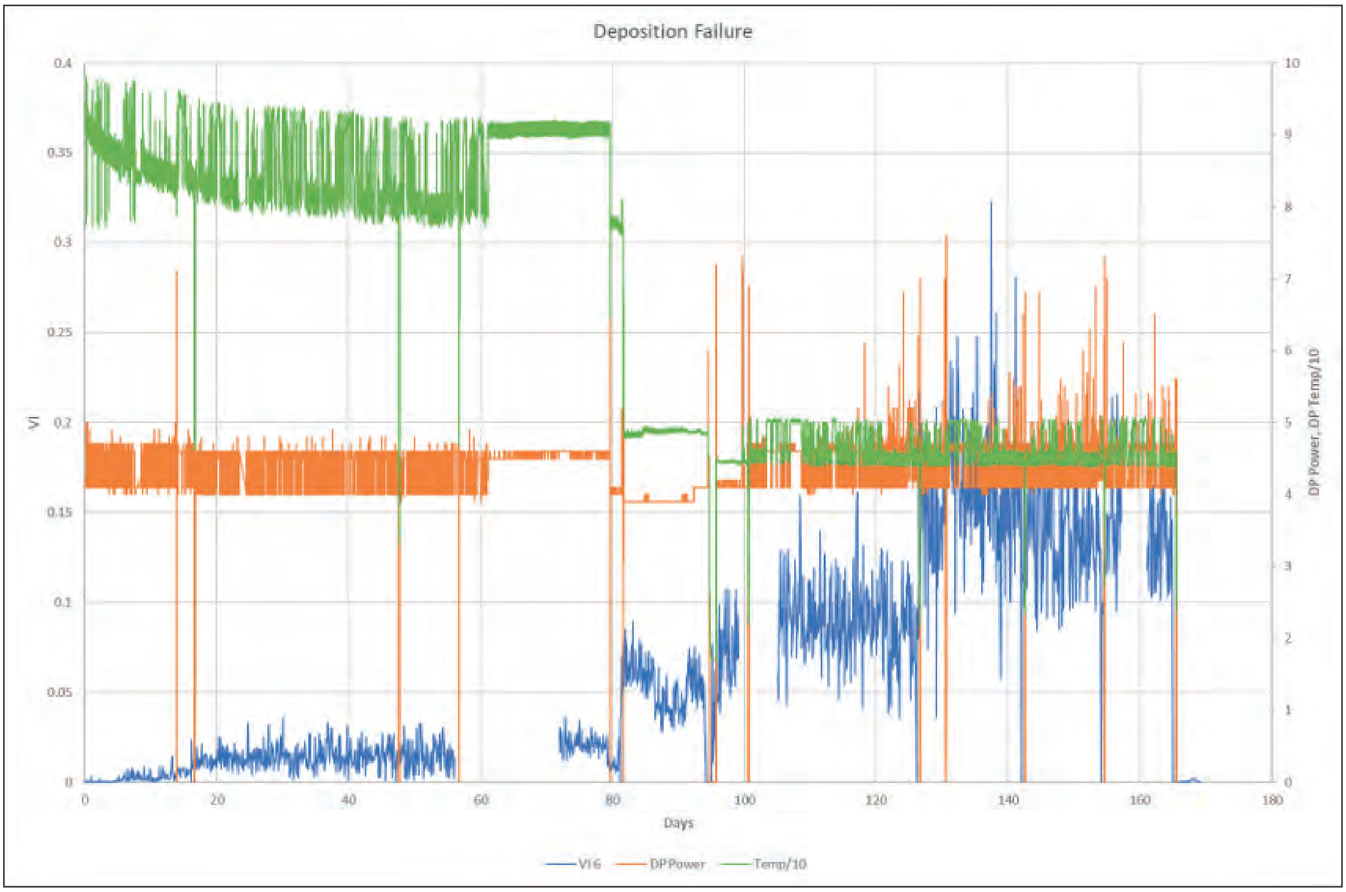


Figure 4: Dry pump power (orange) and temperature (green), and vibration data (blue) taken from a pump supporting an LP-CVD Si_3N_4 batch deposition process

rapid root cause analysis for new and harsh process steps and materials, provide real-time intelligence on critical process vacuum states, accelerate yield ramp by correlating vacuum behaviour with wafer yield, and support fast installation of new sub-fab equipment.

A systems approach to the sub-fab

There is a growing understanding that vacuum pumps and abatement systems are not isolated, self-contained pieces of equipment. They react to each other and to the wider vacuum system that includes forelines, gate valves, other vacuum components and fab process tools. Monitoring pump parameters can reveal the health of individual pumps and also the health of up- and downstream components, including forelines, gate valves, and process chambers. Data acquired at the pump or abatement system can help determine the size and location of vacuum system leaks. Algorithms based on vacuum science and thermodynamics can lead engineers to problems that, over time, can have a significant impact on yield.

Figure 1 shows output from a predictive maintenance application (PdM App) monitoring a vacuum pump in an HVM environment. The plotted parameter is derived from a multivariate analysis and is responsive to various fault types. The downward trend in this plot indicates gradual degradation, interrupted by a temporary re-setting. Comparing sub-fab maintenance records with parameter time stamps showed a one-to-one correspondence between reset events and preventive maintenance procedures performed on the abatement system for the same process tool, indicating that the degradation was connected to the state of the abatement equipment, rather than the health of the pump itself. This was corroborated by other pump parameters not part of the PdM App. The evolution over time further suggested that the abatement PM's themselves did not fully address the issue at hand: the derived parameters did not return to their default values and the downward trend resumed immediately. Ultimately, successful diagnosis of pump faults, combined with the successful segmentation of external downstream issues, resulted in reductions in unscheduled tool down time.

Figure 2 illustrates a case where a process tool in an HVM environment was delivering only 10% of the wafer throughput of other comparable tools. A multivariate PdM App was monitoring the vacuum pump health. The time-series plot of derived parameters clearly showed degradation over time, interrupted by abatement PM-driven re-sets. Initially, the degradation was not as severe and abatement

PMs re-set the pump health as indicated by the multiple step changes. But degradation resumed almost immediately after each step improvement. As time went on this degradation worsened, in spite of the increasing frequency of preventive maintenance on pumps and abatement units. Multiple PdM App alerts were issued. This and other indicators pointed to leaks in the upstream vacuum system. Ultimately a thorough review and repair of forelines and gate valves resolved the issue and resulted in an improved, integrated vacuum system leak check procedure. The wafer throughput gradually returned to match the throughput of peer systems, a 10x improvement for this particular tool.

Sensorization

One of the key requirements for smart manufacturing is the development and implementation of sensors to collect and record new signals, beyond the power and temperature sensors typically used to monitor pump health and performance. An innovative vibration sensor (EdCentra Vision, Edwards Vacuum) illustrates some of the requirements and challenges encountered in this "sensorization".

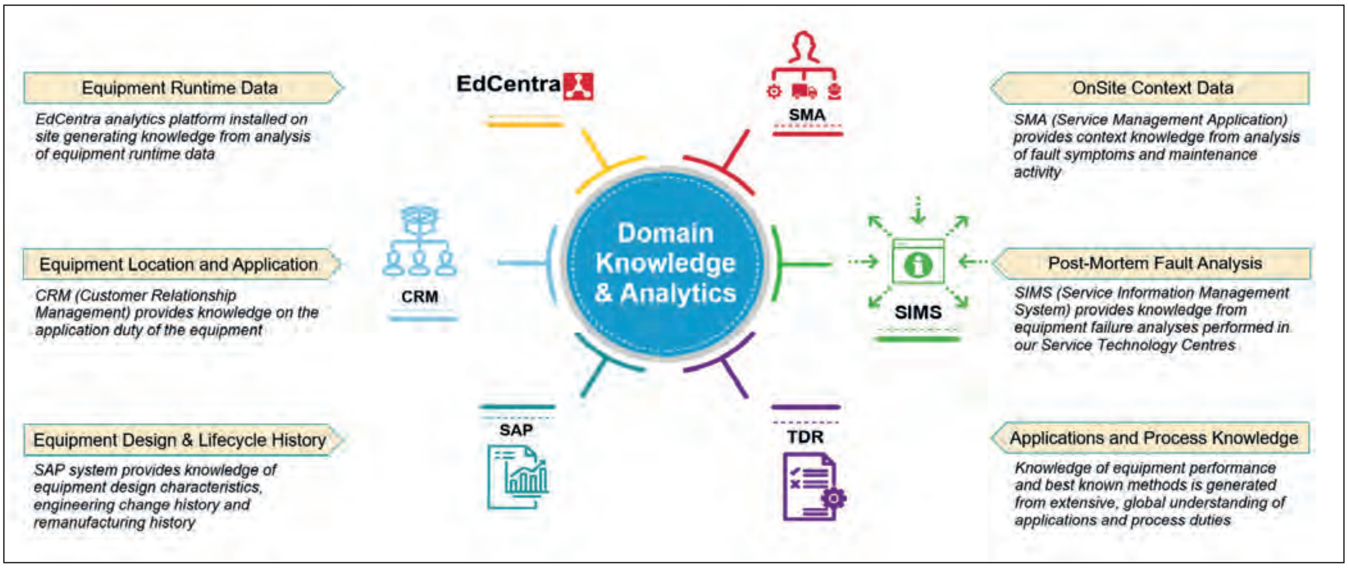
Measuring vibration to monitor the health of rotating machines has a long and successful history. Intrinsic bearings frequencies can be calculated from rotation speeds, and wear-generated perturbations of these frequencies can indicate bearings faults. However, these methods do not translate well to a semiconductor environment where process-induced failure modes are more common than wear-induced. The effects of process-induced failure modes on standard vibration spectra are largely unknown and analysis is complicated by high noise levels.

The new method unlocks key predictive information from vibration data and can detect failure modes that cannot be seen by conventional vibration detectors. It uses a retrofittable "edge" sensor module that includes both sensing and data processing capability to reduce bandwidth requirements on the communications network. Its innovative data analytics methodology translates the complex, noisy vibration signal into a single dynamic coefficient that is easy to compare with existing predictive maintenance parameters. Further vibrational sub-band analysis can provide specific failure mode identification and root-cause analysis, thus providing valuable fault classification (FC) capability.

Compared to conventional methods, the new approach increases sensitivity and provides extended, and in some cases unique, predictive maintenance capability for mechanical pump failure modes. Figure 3 shows the vibration signal from a pump on an atomic layer deposition tool. This pump was pro-actively removed from service based on the progression and value of some of the vibration parameters, even though the next calendar-based maintenance was not imminent. Other pump parameters (not shown), failed to indicate pump deterioration. A detailed analysis of the pump after removal indicated that it was very close to faulting. The picture on the right in figure 3 shows part of the internal pump mechanism with significant process deposition and confirming the vibration-based prediction. Early replacement prevented unscheduled process downtime and potential losses from wafer scrap. The data management system used to collect this data can combine it with other pump and abatement data in a multi-variate analysis to significantly enhance predictive power and accuracy.

Figure 4 demonstrates the sensitivity of vibration analysis in tandem with traditional pump parameters used historically to monitor conditions. The figure shows an example of pump parameters, dry pump power (orange) and temperature (green), and vibration data (blue). The failure mode in this case was deposition related. As shown in Figure 4, from

Figure 5: Information sources for domain knowledge



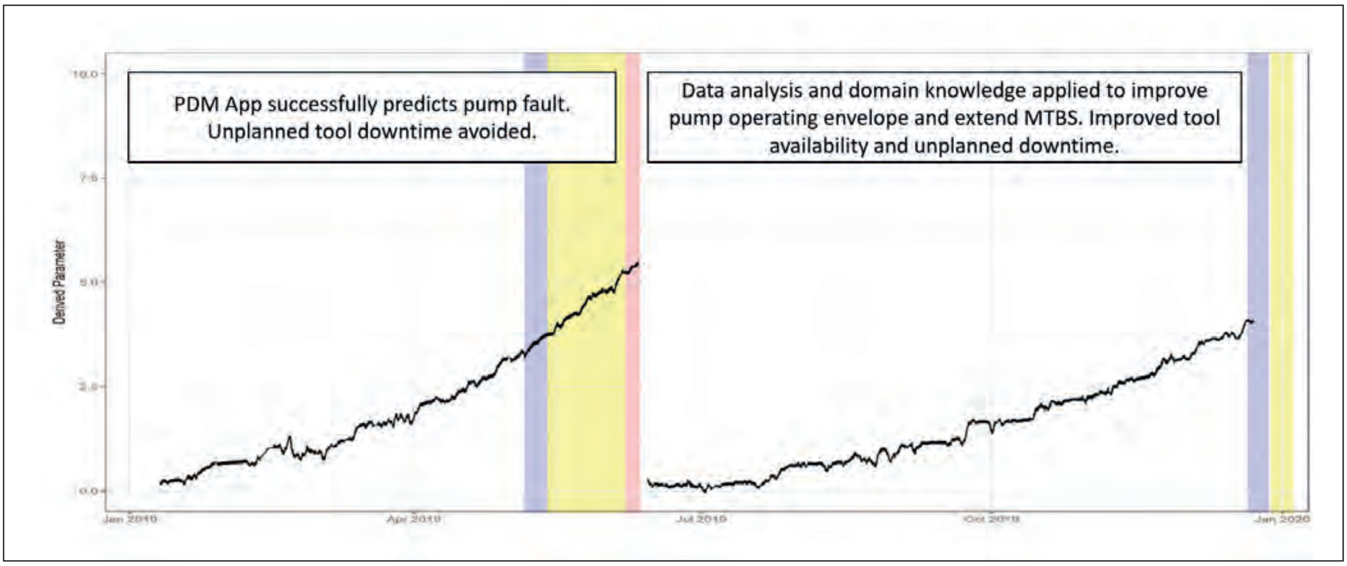


Figure 6: Application of domain knowledge improves pump operating envelop and extends MTBS

day 80 onward changing process conditions caused a step-change in temperature. The power curve shows developing patterns at around the 120-day mark, indicating a predictive time horizon of about 40 days. An important observation to make here is that the vibration data (blue curve) reacted immediately to the modal change and the increased impact of condensable process by-product adversely affecting the operation of the pump. The heightened sensitivity of vibration gave a point-of-detection time period of around 75 days, 25 days greater than traditional pump parameters. Although vibration analysis is not a new technique, the new vibration sensor detected anomalies otherwise missed by traditional monitoring techniques. Importantly, it has added considerably to the ability to detect process-induced changes to the vacuum pump. Its implementation of edge computation reduces data volume, enables real time analytics and shortens detection latency.

Safety

No discussion of smart manufacturing can be complete without considering its potential impact on safety in the sub-fab. The sub-fab is a dangerous place, and safe working practices must be maintained alongside new business processes enabled by smart manufacturing. Examples of potential benefits include: providing advance notice of required equipment interventions so that activities can be better planned, thereby reducing risk and uncertainty associated with the time pressure of urgent activities; using technology to deliver safe standard operating procedures (SOP) and best known methods (BKM) for equipment installation; and incorporating safety data and observations along with asset performance data to domain knowledge drives a holistic approach to reducing risk and uncertainty.

Domain knowledge is central

Domain knowledge and subject matter expertise are key in providing the right context for any type of machine learning and data science application within smart manufacturing. They are key for several reasons, including the complexity of the manufacturing process, the dynamic nature of day-to-day operations and the general unavailability of

Domain knowledge and subject matter expertise are key in providing the right context for any type of machine learning and data science application within smart manufacturing. They are key for several reasons, including the complexity of the manufacturing process, the dynamic nature of day-to-day operations and the general unavailability of large, unambiguous and consistent data sets

Equipment behavior is also ruled by the details of electronic sub-assemblies and mechanical construction. This specific domain knowledge is, for instance, required to distinguish between normal, instantaneous power spikes from pump-vent cycles or powder ingestion and abnormal power spikes from gradual film deposition over long periods of time

large, unambiguous and consistent data sets. People will manage, operate and optimize machines with the help of digital technologies. Processes will define the interaction of machine to machine, people to machine, and people to people. This constitutes a domain knowledge supply chain essential to enabling smart manufacturing.

For sub-fab vacuum and abatement equipment, domain knowledge encompasses multiple areas of know-how, ranging from specific knowledge of how a process or a piece of equipment works to all the ways the process interacts with the world in which it exists.

- Vacuum science and thermodynamics provide the basic laws governing critical parameters such as pressure, flow, temperature, and pumping speed. These all display linear and non-linear responses, instantaneous changes, and long-term trends that need to be considered.
- Equipment behavior is also ruled by the details of electronic sub-assemblies and mechanical construction. This specific domain knowledge is, for instance, required to distinguish between normal, instantaneous power spikes from pump-vent cycles or powder ingestion and abnormal power spikes from gradual film deposition over long periods of time.
- A third area relates to the sequence of wafer processing vs. idle and how it affects parameter behavior over time.
- The last areas of domain knowledge, measured and inferred alert states and measured degradation states, relates to quantifying and calibrating the progression of abnormal behavior against PdM alert states. Depending on process and equipment types, different parameter sets and thresholds may be needed to accurately capture this data.

Figure 6 shows a practical example of domain knowledge at work. PdM Apps, built using domain knowledge, were used to monitor the condition of the pump. The first blue/yellow band indicates a successful fault prediction that eliminated an unscheduled tool down event. Domain knowledge was then applied to change the operating envelope of the vacuum system. Note the right-hand side of the graph shows a much slower degradation of performance before a second successful fault prediction. This delivers the additional benefit of a longer MTBS and thus tool availability.

Tying it together – operational excellence

Smart manufacturing connects people, machines and processes. The full benefit of any smart manufacturing strategy is only realized once these three elements work effectively together to reduce and/or manage risk and uncertainty. Considering the examples discussed, a PdM App may provide a good indication of a fault condition, but further action is needed to eliminate the root cause of the problem and design out the cause of faults from machines or the processes that support them. New sensors provide more information than ever, but processes are needed to bring new learning to fruition. It is always worth reiterating safety: safe working practices must be maintained alongside new business processes enabled by smart manufacturing.

A strong subfab management strategy includes a strong operational excellence model to drive safe and stable operations. Operational excellence incorporates four key areas: standards and procedures; team competency and capability; operational models; and knowledge systems. This is the holistic approach required to provide the solid foundations from which data-driven decision making and improvement activities can be achieved.

Summary

Smart manufacturing in the sub-fab combines real-time data with specific domain knowledge to optimize equipment performance. Improved performance enables significant improvements in productivity and yield. A successful implementation of smart manufacturing requires that sub-fab vacuum and abatement systems be treated as a whole as well as individually. Application of big data techniques, data mining, artificial intelligence and machine learning will certainly reveal new relationships within the data, especially as the number and types of sensors grows and data is integrated across the fab, sub-fab and entire manufacturing ecosystem. Operational excellence models will provide the safe and solid foundations needed to realize the full benefits of new learning.

Rudolph Technologies and Nanometrics merge to form Onto Innovation

Silicon Semiconductor technical editor Mark Andrews recently spoke with Onto Innovation's CEO Mike Plisinski about the merger of Nanometrics and Rudolph Technologies. Plisinski explores the benefits, challenges and opportunities of forming a new semiconductor supply chain entity by combining two industry leaders.

MA – *When resources combine post-merger, each company contributes expertise, viewpoints and strategies which creates both challenges and opportunities. Looking at the merger from the perspective of each company, what are the primary near-term benefits and what might the industry expect from Onto Innovation over time?*

MP – When I think about the benefits of the merger, I put them primarily in three categories: scale, scope, and synergy. Onto Innovation is now the fourth largest (by revenue) wafer fab equipment supplier in the U.S. and among the top 15 in the world. We have over $300 million in cash, cash equivalents or marketable securities and no debt. That gives us a lot of options to invest in our future. We are one of a few companies that is an end-to-end supplier, with products and applications ranging from unpatterned wafer quality, through advanced front-end metrology and macro defect inspection to advanced packaging lithography and inspection in the back-end, with enterprise software solutions spanning the entire value chain.

The synergies between Nanometrics and Rudolph were tremendous, with the positive complementary product lines, markets and organizations with no overlapping products. Nanometrics' strengths were in the optical metrology space where the company had been quite successful with the top manufacturers in the industry. While Nanometrics' metrology sales were concentrated at relatively few customers, those customers were industry leaders in the front end, producing advanced nodes. Rudolph's strengths were in different product technologies: macro defect inspection, acoustic metrology, advanced packaging lithography and software, serving a much broader customer base. Yes, some of the same customers, but the Rudolph customer base was fairly diverse across the entire supply chain. So, by bringing these companies together, we now have a broader product portfolio to offer to a broader customer base and those products have very little to no overlap.

The two companies were built around the same core competencies in software and optics. So, R&D investments are magnified. Let's say we develop a new artificial intelligence engine for fab wide software. We can apply that to help with automatic defect classification in our inspection systems and now to optical metrology as well. The same goes for optics. If we're developing new high-speed camera technology or new illumination technology, we can apply it across a broader set of product lines. We will ultimately develop common platforms, common staging, common end effectors, robots, etc. All that provides tremendous leverage on the R&D investment.

One other point relates to the commonalities of the two companies. We share a common understanding of our products and markets. Putting two companies together that don't share that common understanding and background can be very challenging. Without it, decision making processes can easily become contentious, based on emotion and descending quickly into chaos. With it, discussions stay focused on the facts, on the merits of the case. It was an important consideration in our evaluation of the integration risk. I know it resonated strongly with both boards of directors.

With regard to longer term benefits, we expect some gains in our existing markets as well as expansion of our SAM (served available market). What we ultimately want to do is expand our TAM (total available market) by developing new products and technologies and entering new markets. With two healthy companies coming together there will be some immediate gains in efficiency, primarily from cutting out duplicate public company expenses, but we also have substantial financial resources available to invest. There are opportunities to gain share by combining technologies to open up other aspects of the optical metrology market, like planar films, that we are not serving now. We're also looking at ways to bring software onto the metrology platforms to make them even more competitive and differentiate them in ways that competitors can't match. It is the same approach that was successful for Rudolph for inspection and lithography. There are other options to consider as well, including further M&A activity to accelerate our entry into other markets and expand our SAM and TAM.

MA – *Why now? Can you point to any events or trends that made this the right time to merge?*

MP – I get that question a lot. Neither company was dying, neither company was even sick. Both had growth, both had strong operations and financial statements, etc. The better question might be why did it take so long? And I would say there is no real answer to that. Different personalities, different points of view. Finally, the viewpoints converged. The importance of software was becoming more and more clear and it's not easy to build the kind of software assets Rudolph had. I also believe that, with the consolidation in the industry, the importance of diversity became clearer and more critical to Nanometrics. I think Rudolph saw the exploding growth in the logic and memory spend and they were only partly participating in it. The two boards started to see that a merger really did make sense, that it was an enhancement more than a change in direction.

MA – *Since the two companies that have merged are well known within the industry, why not use one name or the other rather than an entirely new name, or is that the point?*

MP – That is exactly the point. A lot of investors ask that, and customers do too. Both companies had strong brand recognition and long histories – Rudolph from the 1940s and Nanometrics from the 1970s. It is not easy to walk away from such strong legacies, but we are building a company for the future and the future is changing dramatically. What each brand was known for did not really reflect the power and the focus and the potential for this new company in the future. We wanted to reflect the new world moving forward. The pace of innovation is only going to accelerate. We are constantly looking to the future. The electronics/semiconductor market is no longer just the PC/server refresh. Technology is part of every aspect of people's lives. So, Innovation, because we are always looking toward the next innovation, and Onto, because it brings a sense of movement and immediacy. We also did not want to be tied to any specific market. We want a new name that reflects the exciting potential we see.

MA – *2019 has been a tough year for many across the semiconductor industry supply chain due to the fact that two of its largest host countries (the US and China) have been in a months-long trade dispute. Is this situation creating new opportunities or challenges for Onto Innovation as 2020 begins?*

MP – China has been a source of great growth for both companies. So, of course the trade situation has impacted us, but we are still doing very well. Bringing the companies together only allows us to serve our Chinese customers better. Both companies' technologies are clearly important to the Chinese markets because both have seen great growth, and that we expect that to continue. Business in 2019 was down but I think the trade dispute was a minor consideration.

Memory and smartphone adoption were down, but the refresh cycles haven't really occurred. So, there was sort of a natural slowdown. But logic is growing, and certain advanced packaging. Even though it's slowing, memory is transitioning from wire-bonding to advanced packaging and that's an opportunity for us. One of the benefits of bringing these companies together is that it should mute some of these cycles by having more diverse platforms, portfolios and markets.

MA – *Identifying and controlling defects; eliminating potentially damaging contaminants from process flows and related tactics/strategies are all common for work at the extreme limit of CMOS scaling – Does the merger primarily benefit companies working at 7nm and below, or seen another way, what benefits could MEMS makers and others such as power device manufacturers gain from the merger?*

MP – The merger does not enhance, specifically, our ability to do something at 7-8nm. There are areas where we may leverage our software or other core technologies to enhance the value of our tools for 8nm and below. For example, we may be able to leverage acoustic technology to enhance signal generation. Advanced nodes require higher quality wafers and we have seen increasing demand for our bare wafer edge inspection technology.

We also see opportunities to go the other way, taking advanced film metrology and optical metrology from sub 8nm into other markets and specialty devices. Wafer handling requirements for a lot of these specialty devices are very different from the traditional front-end requirements. Rudolph already had the handling and it may enable us to go after specialty applications for optical metrology that Nanometrics could not pursue because developing the handling was too expensive.

MA – *Every merger brings with it good and bad prospects: economies of scale can be optimized, but this sometimes leads to job cuts. A fresh approach can benefit growth opportunities, but the challenge of melding two corporate cultures can be considerable. Can Onto Innovation delve into what they see occurring in the next few years in terms of both challenges and benefits?*

MP – Integration strategies generally fall somewhere between two extremes. Either you force an immediate integration of everything and risk creating chaos because everything changes. Or you let them run more or less independently in the hope that they will merge naturally over time.

Unfortunately, this often results in the creation of silos that grow apart rather than together. We have tried to follow a middle path that balances between silos and forced integration, trying to address integration issues in the most sensible way on a case-by-case basis. In our organization, individual business units are responsible for R&D.

We combined metrology R&D from both companies together under one leader. But R&D for the other business units is largely staying focused on what they did, so not a lot of chaos. But we did centralize each of the manufacturing, marketing, and sales organizations. In manufacturing, one leader looking across the whole company is better able to see things like supply chain opportunities. In marketing, we have all the product lines under one group, so they are better able to develop a coherent Onto Innovation strategy and message. As for staff reductions, the lack of overlap has kept them very few.

The real focus has been on driving efficiency and driving the positive synergies through organizational development. This really leads back to the commonality between the two companies' cultures that I mentioned earlier.

hat common understanding makes it easier to choose the best people for each role and balance between silos and forced integration. R&D is probably hardest to get the synergies. Supply chain, manufacturing improvements, channels to market, those are the quicker and easier places to find synergies.

We were both American companies with similar business cultures: competing on value, competing on technology, understanding the importance of the pace of innovation, emphasizing profitable growth. Shared values make it a lot easier to avoid constant fighting.

If we are considering a big R&D spend, we share a common set of criteria for the decision. We go through a disciplined process and that is engrained in our common culture. I've been very pleased by the progress we have made in only a few short months.

X-Ray and acoustic 3D imaging of components

Both x-ray and ultrasound can non-destructively image internal features in solid objects such as electronic components. Since the two methods use different forms of energy for imaging, employing both methods can greatly enhance and speed problem solving. Most images are two-dimensional, but both methods can also create three-dimensional images of internal features - again, in different ways.

BY TOM ADAMS, CONSULTANT, NORDSON SONOSCAN

AS X-RAY PROPAGATES through a given material, it is attenuated at a rate specific to that material. Although the mechanics of travel are very different for ultrasound, it is also attenuated at its own specific rate for a given material.

If both types of energy [Figure 1] are traveling through the same material and encounter the same bonding interface between two materials, the x-ray simply crosses the interface and keeps going, although its rate of attenuation will likely be different in the second material. The pulse of ultrasound, however, will be partly reflected back to the receiver and partly transmitted across the interface. The portion of each is determined by the identity of the two materials and covers a wide range. But if the second material is a gas such as air, nearly 100 percent of the pulse is reflected, and none of it crosses the interface.

Making a 3D x-ray image is quite different from making a 2-dimensional planar image. Three-dimensional images depend on viewing the object from an angle. To make the 3D image, the beam (or the object) is rotated to various angles and data collected from

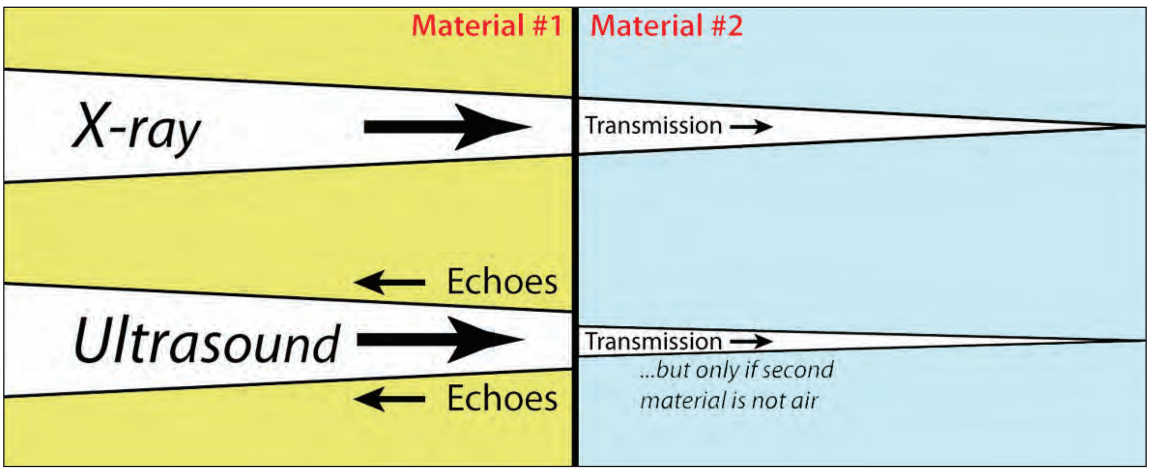


Figure 1. Reaction of an x-ray beam (top) and an ultrasonic pulse (bottom) as they encounter a material interface between two solids.

each view. Then software is used to digitally create the view desired by the operator in 3D. The process is somewhat similar to a CAT (Computer Aided Tomography) scan of a human body to obtain 3D images of bones and other internal structures. Figure 2 is the 3D x-ray image of the die region of a TO-220 device. The rectangular item at center is the die. Imaging was performed by a Nordson DAGE Quadra 7 system. Some observations:

- The die is flat, but the edges give some suggestions of its vertical dimension.
- There are two wires attached to the top surface of the die, but they are not visible at this resolution because they are very thin and, relative to the whole thickness of the encapsulated package, cause little change in attenuation of the x-ray beam.
- At all four sides of the die there is an apparent extrusion of die attach material from beneath the die. The brightness of some of the areas of extrusion does not indicate greater height or reflected visible light, but suggests that the material comprising the die attach material is less attenuating than the mold compound or the heat sink, with the result that the beam that passes through the tops of the extrusions will be less attenuated than those passing through other regions. Being less attenuated, they are imaged more brightly.
- There are about a half-dozen very small black features on the die, mostly on the right side. They represent material that is dense enough to locally attenuate the x-ray beam. They are certainly not voids, which would appear brighter than the surrounding area. Possibly they are small foreign particles, most likely above the die.

Ultrasound creates 3D images in a very different way. The ultrasonic transducer scans back and forth above the sample, sending many thousands of pulses into the sample each second. An echo reflected from an internal interface travels straight back to the receiver. However, if a surface is far from being perpendicular to the beam, the pulse can be reflected at a large angle, and the echo will be lost, thereby creating a dark area in the image.

The TO-220 shown in Figure 3 is the same TO-220 imaged in Figure 2, but imaged with ultrasound, and with the leads included at the bottom of the image. Figure 3 is a Time-of-Flight image made by a Nordson SONOSCAN C-SAM® acoustic microscope. In this imaging mode an echo arriving at the receiver is assigned a color depending upon its arrival time. In the vertical color map at the left of Figure 3, the highest features - the leads - are pink, the die is green, and the heat sink - the deepest interface - is orange.

The travel time of each echo is converted into distance. After the full 3D scan of a sample such as a TO-220, the distance from the top surface of the device to each x-y reflection site on all imaged internal interfaces is known.

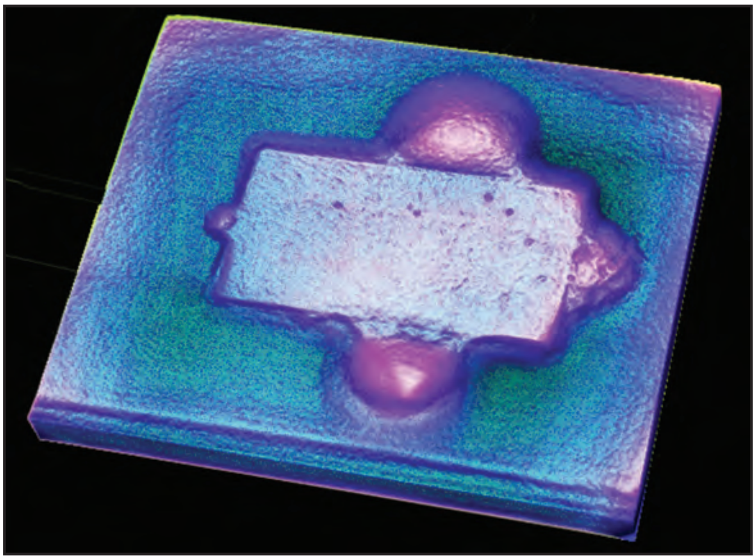


Figure 2: 3D x-ray image of the die region of a TO-220 package.

The whole component package is 6.4mm thick. The “gate” (the vertical extent from which echoes are accepted for imaging) runs from just below the top surface of the device to below the top of the heat sink. The orange surface of the heat sink is about 1mm above the bottom, the top of the die about 2mm, and the tops of the leads so high, at about 5mm, that the wires were not imaged.

If viewed from directly above, the 3D acoustic image of the TO-220 would look flat and many-colored. An observer could surmise the depth of each feature but could not see the depth directly. For that reason, acoustic 3D images are typically viewed from an oblique angle.

In Figure 3, the die at center is green (almost halfway up the color map) because it is higher than the heat sink. In this image, the die appears to be fairly thick but it is probably much thinner than it appears; 3D software exaggerates the thickness to achieve a 3D effect. In making a 3D image, ultrasound sees the top surfaces of features but cannot see the vertical sides (if any) of an object, so it creates a straight side using the same color used for the top of the feature. If the top surface is other than flat, the wall may have multiple colors.

This image shows that there are no cracks visible in the top surface of the die. The two black spots in the die are locations where wires are attached. The wires are round in cross section; when a pulse of ultrasound strikes a wire, it is reflected in many directions and has essentially no chance of being returned to the transducer where its distance will be recorded. No ultrasound travels through the wire to the die surface. What the transducer “sees” is an area having no return signals, so the area is colored black and is given colored interior walls.

Much of the area close to the die is also black - “no return signal.” These are regions where excess die

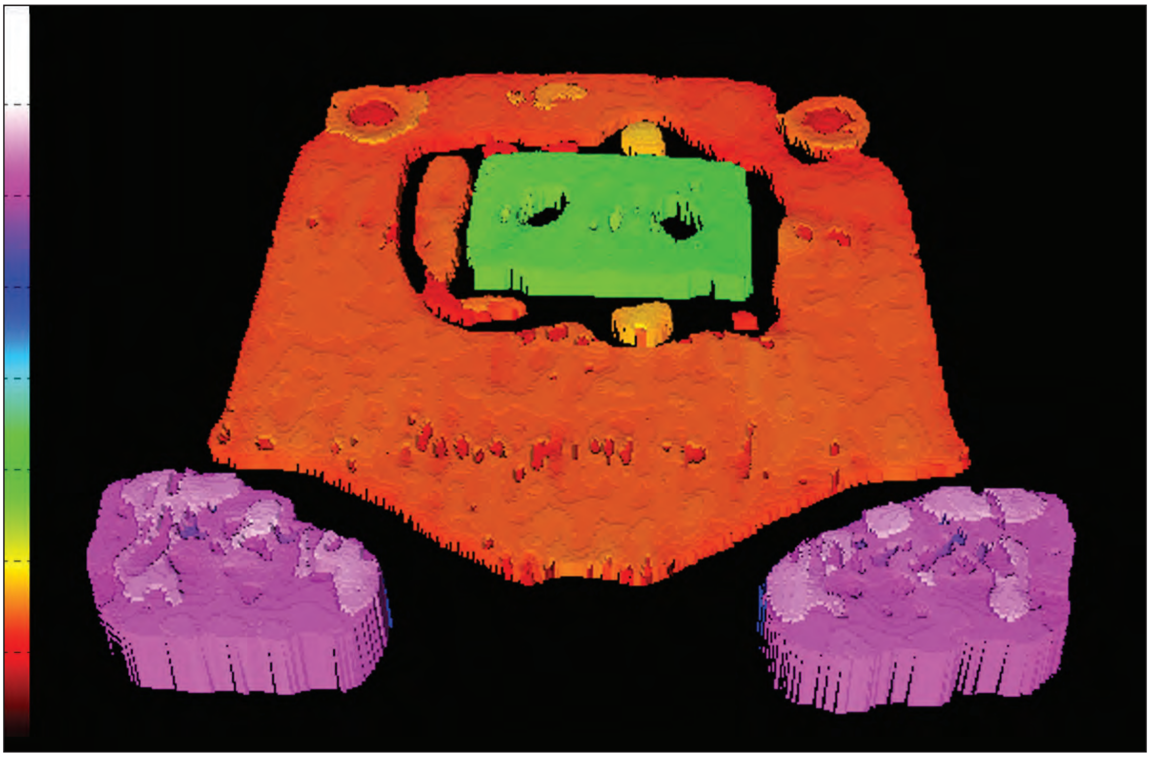


Figure 3: Acoustic image of the same package, but including the leads.

attach material has been extruded from beneath the die and formed steep mounds. Since the mounds are not flat, ultrasound from the transducer was again scattered and no signal was received. The isolated orange island to the left of the die is more or less flat and represents a delamination of the mold compound from the heat sink. A thin delamination in this location would agree with the x-ray image, which shows no feature here because a delamination would be invisible to x-ray.

At the far end of the orange heat sink are two more or less circular features that are slightly paler orange. These are mold marks in the mold compound just above the heat sink. Running horizontally across the heat sink near the pink leads is a rather straight row of small marks. Their arrangement and their small size suggest that they are not some strange type of defect in the heat sink, but are more likely the acoustic shadows of alphanumerics on (and penetrated into) the surface of the package; i.e., echoes returning from the heat sink that were slightly distorted by the alphanumerics.

The highest features in the image of this TO-220 are the two pink leads. These are the ends of the long, straight leads that extend much farther out of the component package. As with the die and other items, software has used the height-reporting color of the top surface to give the leads side walls; they are actually thinner than they appear to be here.

Taken together, the two 3D images tell a great deal about this TO-220. Ultrasound found a probable delamination; x-ray found suspicious dark features. Both ultrasound and x-ray can also image a sample in multiple progressive horizontal slices: each slice creates its own image, and the result is much like a slide show through the sample, one user-defined layer at a time. As with the 3D images shown here, the two sets of images give a very thorough picture of internal structure.

Running horizontally across the heat sink near the pink leads is a rather straight row of small marks. Their arrangement and their small size suggest that they are not some strange type of defect in the heat sink, but are more likely the acoustic shadows of alphanumerics on (and penetrated into) the surface of the package; i.e., echoes returning from the heat sink that were slightly distorted by the alphanumerics

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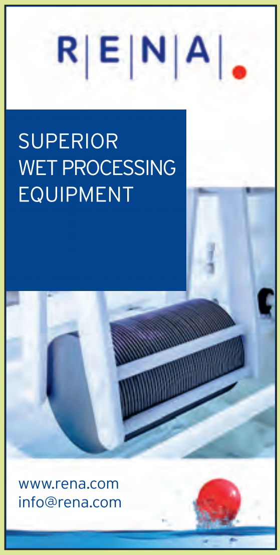

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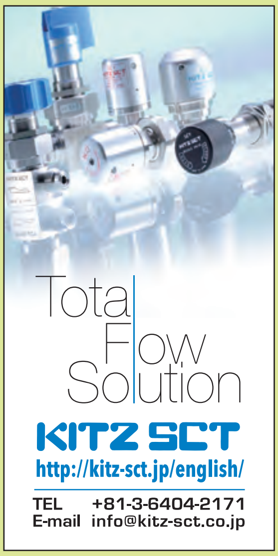

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