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Graphene Hall Effect sensors performance



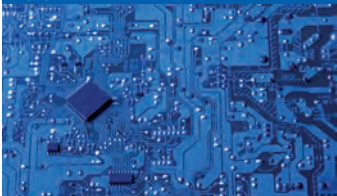
Amorepacific uses imec EEG headsets



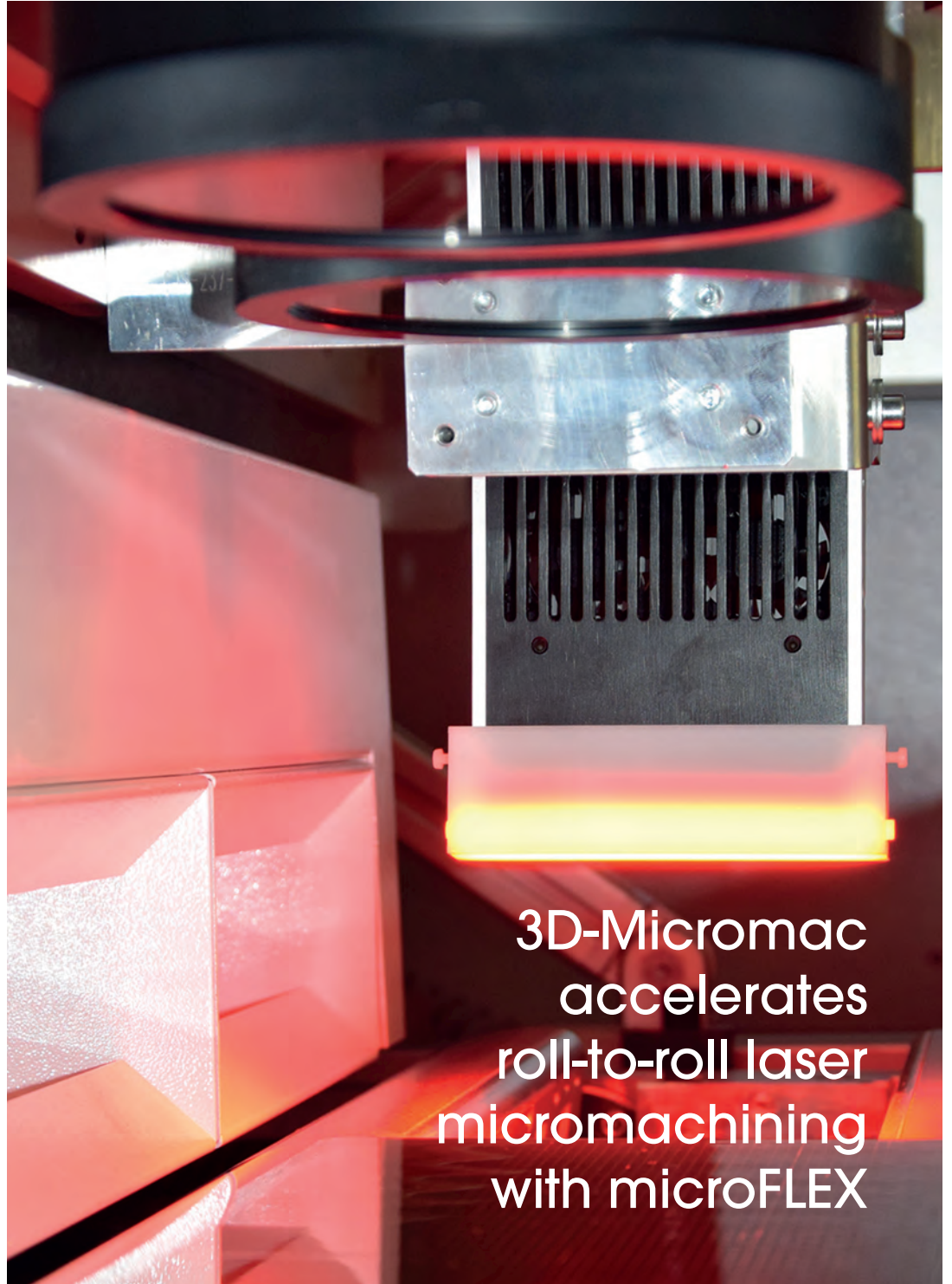
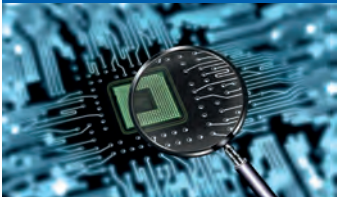
Acoustically imaging the most elusive defects



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editor's view

By Mark Andrews, Technical Editor



Stepping towards normal reveals new vistas ahead

WE HAVE ANALYZED 2020 from every business angle imaginable. What hasn't been revealed and won't be understood for a while are the ramifications of a nothing-nearly-normal 2020 that led to so much personal loss and fear – emotions now giving way to hopes for normalcy that cling to every calendar page. Have you been vaccinated? When can we de-mask? Can we plan a vacation? Can I hug my grandparents?

While some questions are too personal for these pages, answers will come with time, even though we hate not knowing about as much as we hate waiting. But as surely as each day follows another, we'll realize improvement. We frequently recognize a milestone in our rearview mirrors, but seldom can we accurately predict its coming.

In 2020 we saw how much we needed one another once the busyness of pre-pandemic life was stripped away. We worked and schooled from home. We moved our lives online. Making it through 2020 was made possible in no small part by semiconductor technologies. Look no further than achieving COVID-19 vaccines in under 12 months.

This shining moment of human accomplishment was enabled in part by our technology. 2020 business was good – so good that the SEMI trade group expects 2021 to be the third consecutive equipment sales growth year and another record-setting chip sales bonanza. But we also saw shortages; we saw how our

highly complex industry needs to add quick change artist to its repertoire; we saw our supply chain huffing, puffing and straining its way into the New Year.

This issue of Silicon Semiconductor examines the future of laser micromachining through the vision of 3D Micromac, a company that uses its highly precise laser technology to revolutionize R2R manufacturing. We also explore accelerating opportunities for graphene in electronic and photonic applications.

Sonoscan delivers an inside look at defect analysis and ways to ensure packaged device quality.

We also look at innovations from imec researchers that have demonstrated the feasibility of new transistor architectures that could be key enablers of CMOS scaling to 2nm and below while exploring the frontiers of neuromarketing through imec's investigational EEG headsets.



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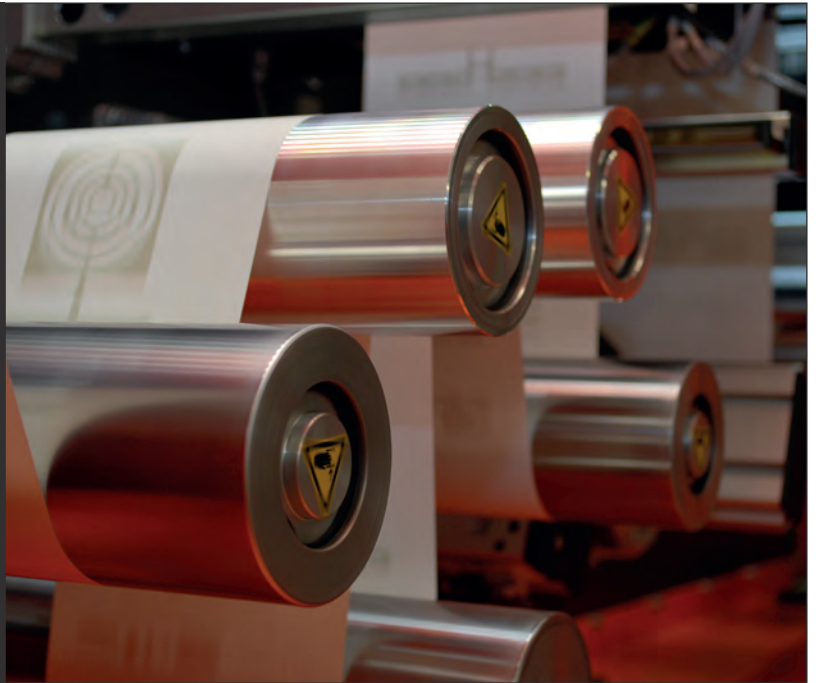
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Traditional electroencephalogram (EEG) techniques are being supplanted by new generations of headsets that can measure and assess human brainwaves outside of traditional clinical settings. This ease of use has led to a growing number of investigational programmes designed to assess whether emotional reactions to specific stimuli can be linked to neural activity.

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Most defects are easily found before assembly by ultrasound in the form of an Acoustic Micro Imaging (AMI) tool, which fires ultrasound pulses into a component and analyzes the return echoes to identify defects, but some remain elusive.

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Graphene has long tantalized electronic device developers thanks to its unique 2D capabilities. But harvesting graphene while maintaining its most sought-after properties has proved elusive, delaying adoption.

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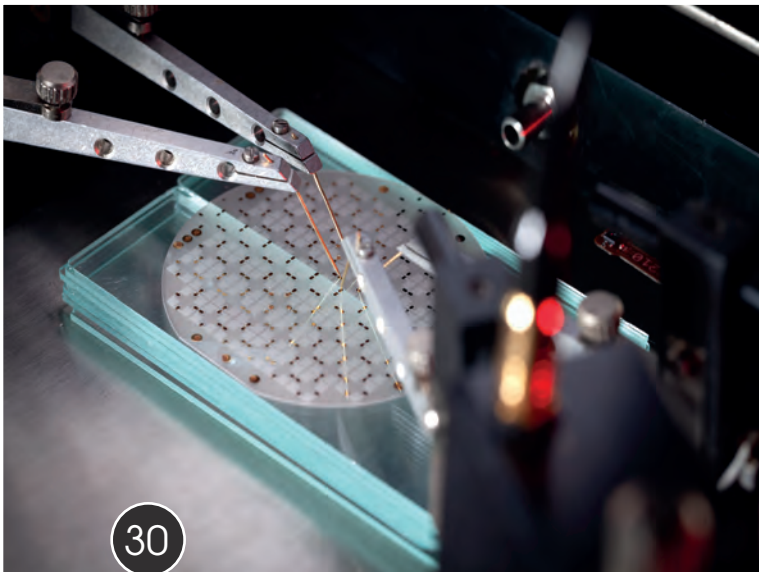
The FinFET transistor architecture is the workhorse of today's semiconductor industry. But as scaling continues, undesired short-channel effects require the introduction of new transistor architectures.



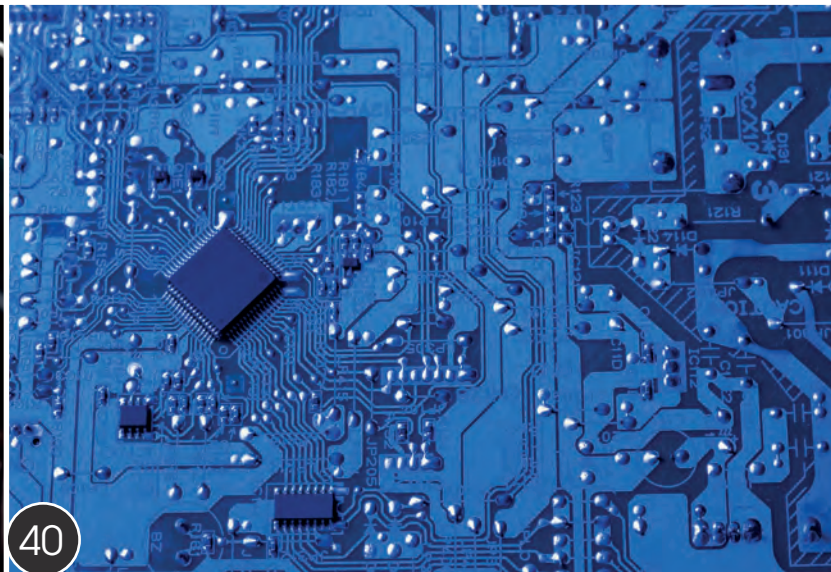
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40 Exploring emerging applications for photonic integrated circuits

Photonic integrated circuits (PICs) have emerged as key component-level enablers of next generation datacom/telecom systems that require smaller, more efficient transceivers and switches. These same qualities are opening doors across widely varied applications ranging from vehicle autonomy to quantum computing and beyond.



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EV Group establishes state-of-the-art customer training facility

EV GROUP (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology, and semiconductor markets, has announced that it has established the EVG Academy, a training facility for customers that provides technical training on all classes of EVG equipment as well as on EVG's CIM Framework software platform in an optimized environment.

Established at EVG's headquarters in Austria, the EVG Academy comprises a new 800-square-meter facility created in tandem with the recently completed Cleanroom V expansion project. By attending in-depth, tiered training classes at the EVG Academy, customers can be qualified to perform basic repairs as well as preventative maintenance on EVG equipment without the need to contact EVG customer support – providing customers with greater flexibility for tool maintenance. The new training facility also serves as the education and training hub for EVG's global organization.

The EVG Academy builds on EVG's existing training facilities at its headquarters, doubling the amount of

training space and technical trainers. It includes eight individual training areas – one for each major class of EVG equipment -- as well as four classrooms and a dedicated workshop area for electrical and mechanical training. Thanks to the additional floorspace, the EVG Academy has also expanded the number and type of tools available for training, including EVG's fully automated HVM platforms, such as the GEMINI® FB automated production wafer bonding system with SmartView® NT3 bond aligner and the BONDSCALE® automated production fusion bonding system.

"The EVG Academy was purpose-built with the goal to enable in-depth customer training on all EVG platforms utilizing the latest equipment and technologies, including our most advanced fully automated high-volume manufacturing (HVM) tools," stated Helmut Pfeifer, vice president of customer support. "EVG has made significant investments in updating our training infrastructure, and we are extremely proud of this world-class facility, which sets new standards for knowledge transfer in our industry.

The new EVG Academy will greatly enhance the learning experience for both our customers and our international customer support teams."

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The EVG Academy is now open for training. Customers interested in learning more can contact EVG at academy@evgroup.com





ITRI and DuPont partner semiconductor materials Lab

INDUSTRIAL TECHNOLOGY RESEARCH INSTITUTE (ITRI) and DuPont Electronics & Imaging have celebrated the opening of a new semiconductor materials laboratory in Hsinchu, Taiwan.

DuPont established the laboratory to stay close to the semiconductor industry in Taiwan. DuPont will conduct, in collaboration with ITRI, semiconductor material research, development and enhancement, and accelerate pilot testing and commercial viability to support DuPont's customers as they pursue the next generation of semiconductors in Taiwan.

The evolution of 5G and Artificial Intelligence (AI) has spurred development of key technologies for the next generation of semiconductors, including materials to support heterogeneous integration, advanced manufacturing processes, and high-end packaging. Taiwan plays a leading role in the semiconductor industry and has an integrated semiconductor supply chain.

Chih-I Wu, VP and general director of ITRI's Electronic and Optoelectronic System Research Laboratories, stressed that ITRI has long invested in semiconductor research and development and has a solid foundation

in the fields of electronics and optoelectronics, advanced packaging processes, chemistry and materials. With the support from AI on Chip Program of Department of Industrial Technology (DoIT),

Ministry of Economic Affairs (MOEA), ITRI will expand investment in advanced equipment and technology, heterogeneous integrated packaging experiment platforms and diversified design, manufacturing processes and prototype production services.

"Bringing together ITRI's semiconductor-related technical strength and DuPont's expertise in materials, this laboratory in ITRI's vicinity will enable closer exchanges between the two organisations to bring more innovative solutions and meet the immediate needs of Taiwan's semiconductor and IC substrate industries," he said.

"DuPont has been conducting business in Taiwan for more than 50 years



and has grown alongside Taiwan's industrial development, especially in the electronics industry.

Our investment in semiconductor technology and manufacturing centres in Taiwan serves as our hub in Asia Pacific to promote advanced semiconductor technologies globally," said Dennis Chen, DuPont Taiwan president.

"Over the years, we have made efforts in strengthening technological breakthroughs, terminal applications and supporting the strategic technology roadmap in Taiwan. The inauguration of this laboratory marks another important milestone as we continue to enhance innovation and R&D capabilities in Taiwan."

AP Memory and Ambiq partner

AP MEMORY TECHNOLOGY, supplier of ultra-low power and low pin count PSRAM (IoT RAM), and an emerging supplier of low-density LPDRAM, AI memory solutions for edge / IoT applications, together with Ambiq, a supplier of ultra-low power microcontrollers (MCU), System-on-Chips (SoC), and Real-time Clocks (RTC), have announced their partnership to enable richer experiences in next-generation battery-powered intelligent endpoint devices.

Building on the rich set of features and ultra-low power of Ambiq's Apollo4 platform, AP Memory's IoT RAM solutions are optimal for providing the additional memory needed to augment the ultimate endpoint experiences. AP Memory solutions offer low signal pin count (6 for QSPI, 11 for OPI), low power (standby from 20uA to 80uA, active from 3mA to 8mA), and high transfer rate options needed to meet the demanding power and space constraints of wearable and other battery-powered smart consumer devices. In recognition of the technical advantages of this leading-edge partnership, several large customer projects using the combination of AP Memory and Ambiq solutions are currently underway. "The market is demanding richer experiences

in intelligent endpoints, in ever more constrained form factors and stricter ultra-low power requirements. As a technology leader in ultra-low power chipsets, Ambiq is well-positioned for powering such devices. AP Memory is delighted to partner with Ambiq. Together, both companies are rising to the challenge of delivering to the market richer experiences in next-generation battery-powered intelligent endpoints." says Ivan Hong, Vice President and General Manager of IoT Business Unit of AP Memory.

"The demand for increased memory capacity in IoT endpoints is constantly growing given the need for more enhanced displays, AI/ML processing, complex audio use cases, and highly integrated sensor fusion applications. The partnership with AP Memory allows customers to take advantage of the industry-leading power consumption and features of the Apollo4 platform and address the expansive needs of those new application areas yet still maintaining a small physical form factor. The low-power products from AP Memory give our customers the flexibility to future-proof their product lines by offering more memory with longer battery life," says Dan Cermak, Vice President of Architecture and Product Planning at Ambiq.



Imec demonstrates 20nm pitch line/space resist imaging with high-NA EUV interference lithography

IMEC, leading research and innovation hub in nanoelectronics and digital technologies, reports for the first time the use of a 13.5 nm High Harmonic Generation source for the printing of 20nm pitch line/spaces using interference lithographic imaging of an Inpria metal-oxide resist under high-numerical-aperture

(high-NA) conditions. The demonstrated high-NA capability of the EUV interference lithography using this EUV source presents an important milestone of the AttoLab, a research facility initiated by imec and KMLabs to accelerate the development of the high-NA patterning ecosystem on 300 mm wafers. The interference tool will be used to explore the fundamental dynamics of photoresist imaging and provide patterned 300 mm wafers for process development before the first 0.55 high-NA EXE5000 prototype from ASML becomes available.

The high-NA exposure at 13.5nm was emulated with a coherent high-flux laser source of KMLabs in a Lloyd's-Mirror-based interference setup for coupon experiments on imec's spectroscopy beamline. This apparatus supplies critical learning for the next step, expansion to 300 mm wafer interference exposures. In this arrangement, light reflected from a mirror interferes with light directly emitted by the 13.5nm laser source, generating

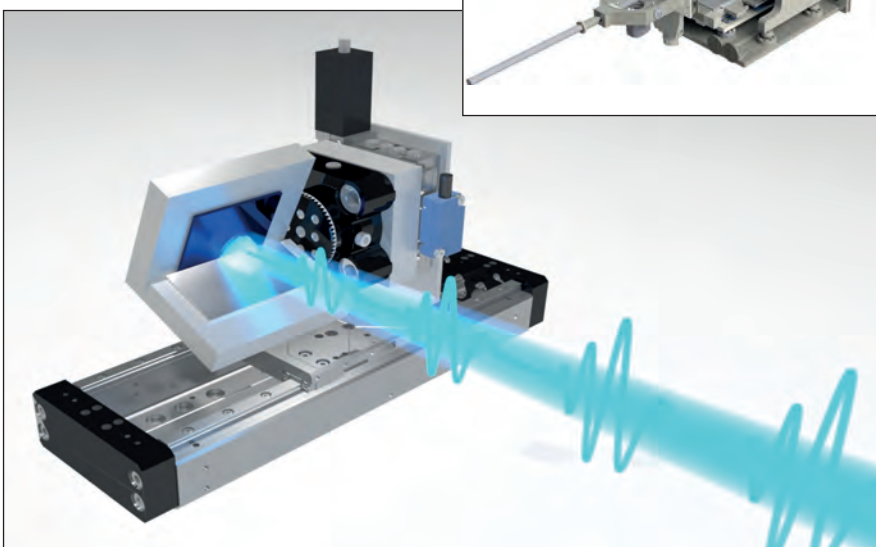
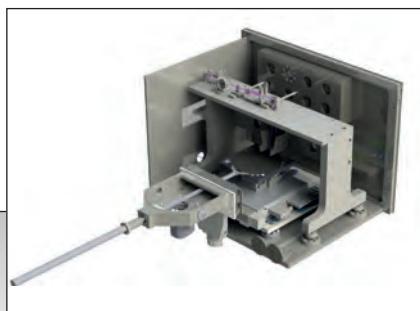
a finely detailed interference pattern suited for resist imaging. The pitch of the imaged resist pattern can be tuned by changing the angle between the interfering light beams. With this setup, 20nm line/spaces could for the first time at imec be successfully patterned in an Inpria metal-oxide resist (exposure dose range of ~54-64mJ/cm², interference angle 20°) using a single-exposure, coated on coupon samples.

"The high-flux laser source of KMLabs was used at a record small wavelength of 13.5nm, emitting a series of attosecond (10-18s) pulses that reaches the photoresist with a pulse duration that is a few femtoseconds (10-15s) in width. This imposed challenging requirements on the temporal coherence of the interfering waves," explains John Petersen, Principal Scientist at imec and SPIE Fellow. "The demonstrated capability of this setup for emulating high-NA EUV lithography exposures is an important AttoLab milestone. It demonstrates that we can synchronize femtosecond wide pulses, that we have excellent vibration control, and excellent beam pointing stability.

The 13.5nm femtosecond enveloped attosecond laser pulses allow us to study EUV photon absorption and ultrafast radiative processes that are subsequently induced in the photoresist material. For these studies, we will couple the beamline with spectroscopy techniques, such as time-resolved infrared and photoelectron spectroscopy, that we earlier installed within the laboratory facility. The fundamental learnings from this spectroscopy beamline will contribute to developing the lithographic materials required for the next-generation (i.e., 0.55 NA) EUV lithography scanners, before the first 0.55 EXE5000 proto-type becomes available."

Next up, the learnings from this first proof of concept will now be transferred to a second, 300mm-wafer-compatible EUV interference lithography beamline that is currently under installation. This beamline is designed for screening various resist materials under high-NA conditions with a few seconds per single-exposure, and for supporting the development of optimized pattern, etch and metrology technologies viable for high-NA EUV lithography. "The lab's capabilities are instrumental for fundamental investigations to accelerate material development toward high NA EUV," said Andrew Grenville, CEO of Inpria.

"We are looking forward to deeper collaboration with the AttoLab. Our interference tools are designed to go from 32nm pitch to an unprecedented 8nm pitch on 300 mm wafers, as well as smaller coupons," says John Petersen. "They will offer complementary insights in what is already gained from 0.33NA EUV lithography scanners – which are currently being pushed to their ultimate single-exposure resolution limits. In addition to patterning, many other materials research areas will benefit from this state-of-the-art AttoLab research facility. For example, the ultrafast analytic capability will accelerate materials development of the next-generation logic, memory, and quantum devices, and of the next-generation metrology and inspection techniques."





Intermolecular relocate innovation hub to San Jose

Intermolecular, Inc. (“Intermolecular”), a wholly-owned subsidiary of Merck KGaA, Darmstadt, Germany, has announced the relocation of the Silicon Valley Innovation Hub from Menlo Park to Intermolecular’s San Jose facilities, combining Merck KGaA, Darmstadt, Germany’s innovation efforts in the Bay area with Intermolecular’s services for materials and electronics, creating a unique space that empowers collaboration with startups.

The Silicon Valley Innovation Hub was established in 2017 in Menlo Park, CA. As part of the global Innovation Ecosystem of Merck KGaA, Darmstadt, Germany, it strives to identify and develop viable new businesses and technologies between the company’s existing business sectors or break new ground beyond them.

“The mission of the Silicon Valley Innovation Hub is to identify and explore untapped innovation- and business opportunities for Merck KGaA, Darmstadt, Germany. In this context, the intersection of life science and material science is becoming increasingly important and opens new areas of innovation. Having the Silicon Valley Innovation Hub and Intermolecular under one roof now will allow us and our cooperation partners to develop and test new materials for biological applications. We are very excited about these new opportunities,” states Thomas Herget, head of the Silicon Valley Innovation Hub.

Intermolecular has a unique toolset and expertise to quickly test and prove new advanced technologies and materials for semiconductor devices and electronic applications.

Having the Innovation Hub in the same building will further strengthen collaboration of the company’s businesses with startups and innovative companies in and around the Bay Area to rapidly grow their business from concept to high-volume manufacturing. The building boasts 30,000 square feet of cleanroom, chemical labs, offices, a collaboration area and event spaces. Intermolecular’s customizable services are tailored to meet a startup’s unique needs, whether it is achieving a proof-of-principle, a first prototype, or a small series production. Intermolecular assigns experts in emerging technologies and offers its manufacturing facilities, which can run experiments 24/7 to test and validate materials critical to product development. Intermolecular’s flexible methodologies and quality data help accelerate product design innovation, at any phase of a startup’s product development cycle.

“Intermolecular offers a seamless process flow that is specific and confidential to each startup, which is key to speeding time to innovation,” said Casper van Oosten, business field head and managing director for Intermolecular, Inc. “By providing startups the tools and expertise to validate their ideas, we can help them accelerate their path to new investment and speed their product introductions by giving them concrete data needed to move quickly from a research phase to full production. Having the experts from the Silicon Valley Innovation Hub now under one roof, we are looking forward to branch out into new areas and exploring collaboration opportunities that bring benefits to our customers/startups.”

“Semiconductor companies, particularly companies working on current generation and emerging memories, need to do a lot of experimentation to get the best combination of processes and materials,” said Tom Coughlin, president of Coughlin Associates. “Companies such as Intermolecular can provide efficient ways to gather and analyze the required data to make the next generations of memory possible.



WAFER ID MARKING & SORTING



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Applied Materials introduces new playbook for process control

APPLIED MATERIALS has unveiled a major innovation in process control that uses Big Data and AI technology to help semiconductor manufacturers accelerate node development, speed time to revenue and earn more profits over the life of a node.

Semiconductor technology is becoming increasingly complex and expensive, and reducing the time needed to develop and ramp advanced nodes can be worth billions of dollars to chipmakers around the world. Success is gated by the ability to detect and correct defects which is becoming increasingly difficult as line widths shrink and turn nuisance particles into yield killers. Likewise, 3D transistor formation and multiprocessing techniques introduce subtle variations that can multiply to create yield-killing defects that are vexing and time-consuming to root-cause.

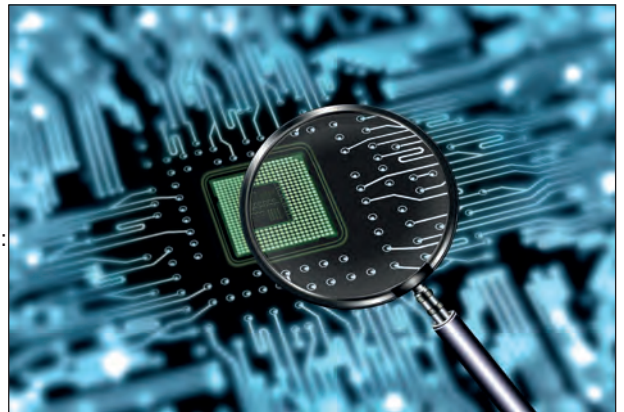
Applied Materials is solving these challenges with a new playbook for process control designed to bring the benefits of Big Data and AI technology to the core of chipmaking technology. Applied's solution consists of three elements that work together in real time to find and classify defects faster, better and more cost effectively than legacy approaches. The three elements are:

New Enlight Optical Wafer Inspection System: in development for five years, the Enlight system combines industry-leading speed with high resolution and advanced optics to collect more yield-critical data per scan. The Enlight system architecture improves the economics of optical inspection, resulting in a 3x reduction in the cost of capturing critical defects as compared to competing approaches. By dramatically improving cost, the Enlight system allows chipmakers to insert many more inspection points in the process flow. The resulting availability of Big Data enhances "line monitoring," statistical process control methods that can predict yield excursions before they occur, immediately detect excursions so that wafer processing can be halted to protect yields, and enable root-cause

traceback to accelerate corrective actions and the return to high-volume manufacturing.

New ExtractAI Technology: developed by Applied's data scientists, ExtractAI technology solves the most difficult problem of wafer inspection: the ability to quickly and accurately distinguish yield-killing defects from the millions of nuisance signals or "noise" generated by high-end optical scanners. ExtractAI is the only solution in the industry that creates a real-time connection between the Big Data generated by the optical inspection system and the eBeam review system that classifies specific yield signals so that by inference, the Enlight system resolves all of the signals on the wafer map, differentiating yield killers from noise. ExtractAI technology is incredibly efficient; it characterizes all of the potential defects on the wafer map after reviewing only 0.001% of the samples. The result is an actionable map of classified defects that accelerates semiconductor node development, ramp and yield. The AI technology is adaptive and quickly identifies new defects during high-volume production while progressively improving its performance and effectiveness as more wafers are scanned.

SEMVision eBeam Review System: the SEMVision system is the most advanced and widely used eBeam review technology in the world. With its industry-leading resolution, the SEMVision system trains the Enlight system with ExtractAI technology to classify yield-killing defects and distinguish defects from noise. By working together in real time, the Enlight system, ExtractAI technology and SEMVision system help customers identify new defects as they are introduced in the manufacturing flow, enabling higher yields and profitability. The large installed base of SEMVision G7 systems is already compatible with the new Enlight system and ExtractAI technology.



"Being able to quickly and accurately distinguish yield-killing defects from noise is something fab engineers have struggled with for more than 30 years," said Dan Hutcheson, chairman and CEO of VLSIresearch. "Applied Materials' Enlight system with ExtractAI technology is a breakthrough approach that solves this challenge and, because the AI gets smarter the more the system is used, it helps chipmakers increase their revenue per wafer over time."

"Applied's new playbook for process control combines Big Data and AI to deliver an intelligent and adaptive solution that accelerates our customers' time to maximum yield," said Keith Wells, group vice president and general manager, Imaging and Process Control at Applied Materials. "By combining our best-in-class optical inspection and eBeam review technologies, we have created the industry's only solution with the intelligence to not only detect and classify yield-critical defects but also learn and adapt to process changes in real time. This unique capability enables chipmakers to ramp new process nodes faster and maintain high capture rates of yield-critical defects over the lifetime of the process."

The new Enlight system with ExtractAI technology is the fastest-ramping inspection system in Applied's history and is already being used in production at all leading-edge foundry-logic customers worldwide. The SEMVision system has been the industry's leading eBeam review for over 20 years, with more than 1,500 systems at customer fabs around the world.



Fully Automated AFM solution for OLED, 2D encoder, photomask and more

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U.S. Department of Defense partners with GLOBALFOUNDRIES to manufacture secure chips

GLOBALFOUNDRIES (GF), leading specialty foundry, has announced a strategic partnership with the U.S. Department of Defense (DoD) to provide a secure and reliable supply of semiconductor solutions manufactured at GF's Fab 8 in Malta, New York – the company's most advanced semiconductor manufacturing facility. These semiconductor chips will be used in some of the DoD's most sensitive applications for land, air, sea, and space systems.

Under the agreement, GF will provide a supply of chips built at Fab 8 on its differentiated 45nm SOI platform. The agreement is made possible by Fab 8's compliance with U.S. International Traffic in Arms Regulations (ITAR) and highly restrictive Export Control Classification Numbers under the Export Administration Regulations (EAR). The new supply agreement builds upon the longstanding partnership between the DoD and GF to

provide chips for defense, aerospace, and other sensitive applications. GF currently supplies the DoD with chips manufactured at GF's other on-shore facilities, Fab 10 in East Fishkill, New York, and Fab 9 in Burlington, Vermont.

"GLOBALFOUNDRIES is a critical part of a domestic semiconductor manufacturing industry that is a requirement for our national security and economic competitiveness," said Senate Majority Leader Chuck Schumer, who successfully passed new federal semiconductor manufacturing incentives in last year's National Defense Authorization Act (NDAA). "I have long advocated for GLOBALFOUNDRIES as a key supplier of chips to our military and intelligence community, including pressing the new Secretary of Defense, Lloyd Austin, to further expand the Department of Defense's business with GLOBALFOUNDRIES, which will help

expand their manufacturing operations and create even more jobs in Malta." In a supporting statement from the U.S. Department of Defense, "This agreement with GLOBALFOUNDRIES is just one step the Department of Defense is taking to ensure the U.S. sustains the microelectronics manufacturing capability necessary for national and economic security. This is a pre-cursor to major efforts contemplated by the recently passed CHIPS for America Act, championed by Senator Charles Schumer, which will allow for the sustainment and on-shoring of U.S. microelectronics capability."

The first chips from this new agreement are targeted to begin delivery in 2023. GF is in ongoing discussions with the DoD regarding Trusted Accreditation for Fab 8. GF employs nearly 3,000 people at Fab 8, and has invested more than \$13 billion in the facility.

Macronix provides advanced flash memory to STMicro

Macronix International, an integrated device manufacturer in the non-volatile memory (NVM) market, has announced that STMicroelectronics (ST) is using Macronix OctaBus flash memory for several STM32 microcontroller (MCU) platforms, including the STM32H72x/73x, STM32L5 and the recently announced STM32U5. Macronix's MX25 OctaBus family is providing the high-performance memory on select STM32 Discovery Kits and Evaluation Boards.

"Finding an external memory solution that allows our STM32 devices to demonstrate the full range of their exceptional performance and features is key to the success of our industry-leading family of MCUs," said Daniel Colonna, marketing director, Microcontroller Division, STMicroelectronics. "By helping developers exploit the full capabilities of the STM32 MCUs, Macronix, with its OctaBus non-volatile memories, is a member of the ST Partner Program and a contributor to the extensive STM32 ecosystem." "We're pleased to continue our valuable

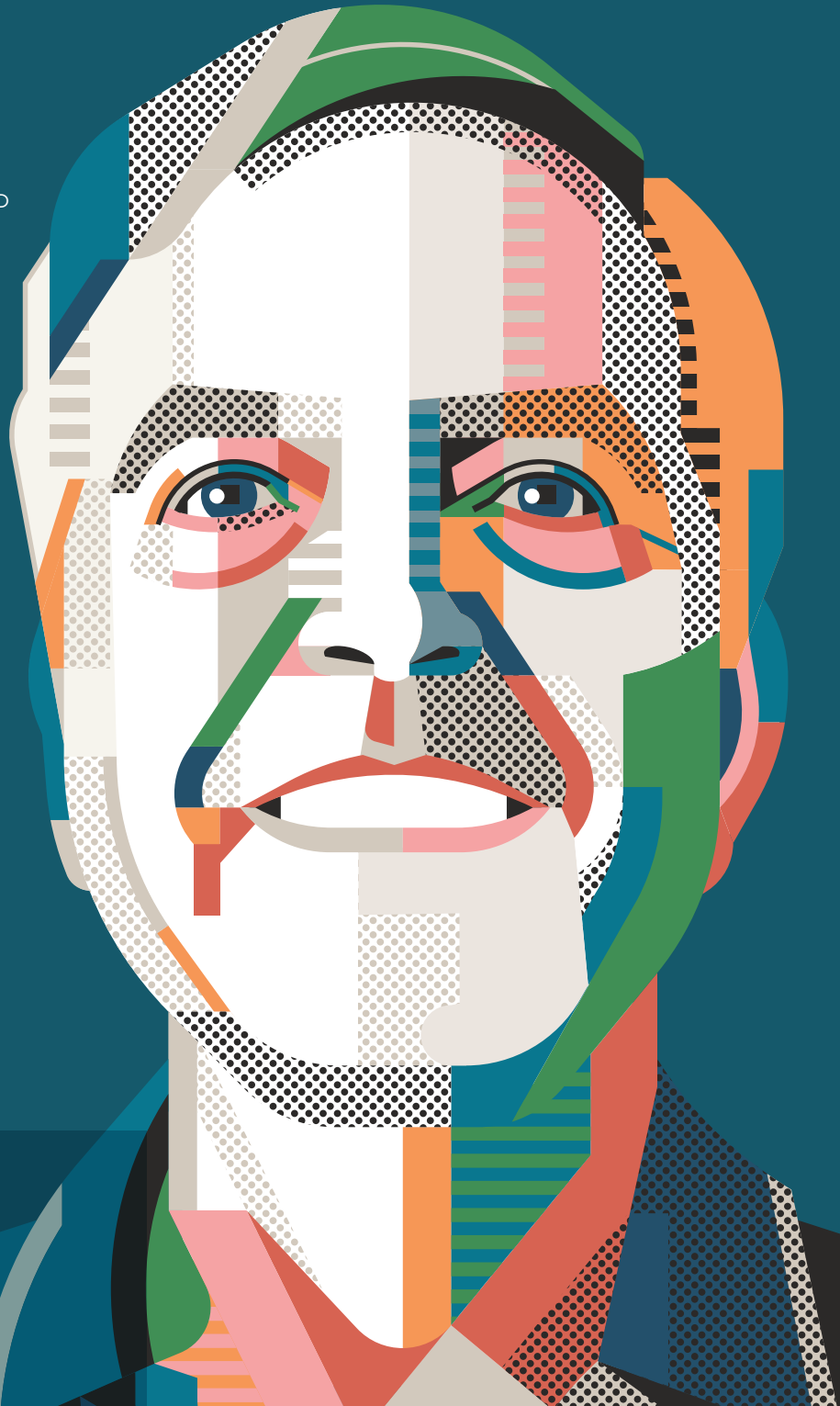
partnership with STMicroelectronics and to deliver innovative solutions that unleash the exceptional performance of the wide STM32 offering," said F.L. Ni, vice president of marketing at Macronix. "STM32 family is designed to cover the full spectrum of performance, high memory integration and power savings for smart, connected products."

The highly advanced STM32 devices embed up to two Octal SPI ports supporting the OctaBus interface, which comprises Macronix's octaflash 8 I/O NOR and OctaRAM memories. OctaBus memory devices have been designed to meet current and emerging trends of demanding applications that require extremely high performance, reliability and an enhanced user experience. The MX25LM/UM OctaBus memories meet the growing demand for "instant-on" performance and real-time system responsiveness for external memories in automotive, industrial and consumer applications. The ultra-high-performance OctaBus memory products can perform up to an operational frequency of

250MHz with 500MB/s read throughput, which is the industry's fastest. The OctaBus memory devices enable system architects to meet customers' demanding expectations for systems with a rich graphical user interface and achieve ultra-fast response times.

The MX25LW/UW OctaBus memory family has exceptional features for efficient management of over-the-air (OTA) software updates and data logging. Those features of the MX25LW/UW family are also a natural extension as execute-in-place (XIP) memory for STM32 MCUs. OctaBus memory offered in densities up to 2Gb can support the most advanced graphical user interfaces. The STM32 family of 32-bit microcontrollers, based on the Arm Cortex-M processor, is designed to offer new degrees of freedom to MCU users. It offers products combining very high performance, real-time capabilities, digital signal processing, low-power / low-voltage operation, and connectivity, while maintaining full integration and ease of development.

Dennis Ralston
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3D-Micromac accelerates roll-to-roll laser micromachining with microFLEX

Lasers are versatile industrial tools that today are mainstays within many semiconductor and photovoltaic manufacturing processes. The accuracy, repeatability, speed and cost-effectiveness of laser micromachining was largely absent from roll-to-roll (R2R) thin-film manufacturing until 3D-Micromac brought its innovative microFLEX system from the lab to fabs across the globe.

BY MARK ANDREWS, TECHNICAL EDITOR, SILICON SEMICONDUCTOR

ADVANCED TECHNOLOGIES often share a common heritage. The development of drones and quadcopters for example would likely not have occurred when it did were it not for the miniaturized gyroscopes, accelerometers, and microphones first developed for smartphones.

One technology frequently gives rise to another, so in a sense it is not surprising that the roll-to-roll (R2R) technology first developed for web printing was foundational to thin-film manufacturing utilizing a wide range of flexible substrate materials. Thanks to this genesis, products built utilizing flexible electronics and batteries are now enabling wearable medical diagnostic tools, fitness trackers and photovoltaic (PV) cells to name but a few of the most widely recognized applications.

According to Christian Scholz, 3D-Micromac Team Leader for R2R Processing, initial work on the system that would evolve into microFLEX began as a project with the Technical University of Chemnitz (Germany.) An early goal was incorporating a laser module into a R2R printing system. While those first systems brought high accuracy and repeatability to printing, achieving the next step – R2R manufacturing using flexible substrates and laser micromachining – was still years away.

“The Technical University of Chemnitz is very strong in printing technology and they were venturing into printed functionalities – printing simple circuits and things like that in the early 2000s. And they quickly realized that with standard printing technology, you cannot achieve such small feature sizes as would be needed for a printed circuit,” Scholz noted. “Standard graphic printing doesn’t need an accuracy in the range of a few microns since the human eye cannot see those very fine details. But if you want to print electronics, especially if you have multiple layers, then you need to precisely align your first printing step to the next one and the next. Also, the laser has to be very precise to machine at the very right position.”

The potential of manufacturing flexible device components at high speed with extreme precision was tantalizing even as researchers quickly realized that toolsets optimized for paper printing were not accurate enough for manufacturing at micrometer scale. Once 3D-Micromac successfully created a laser micromachining module for print, could the

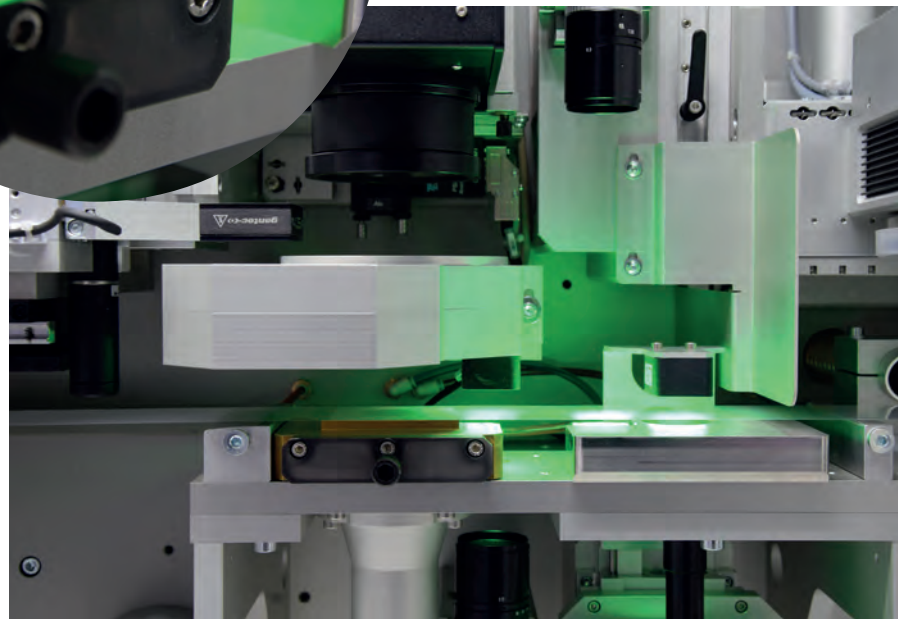
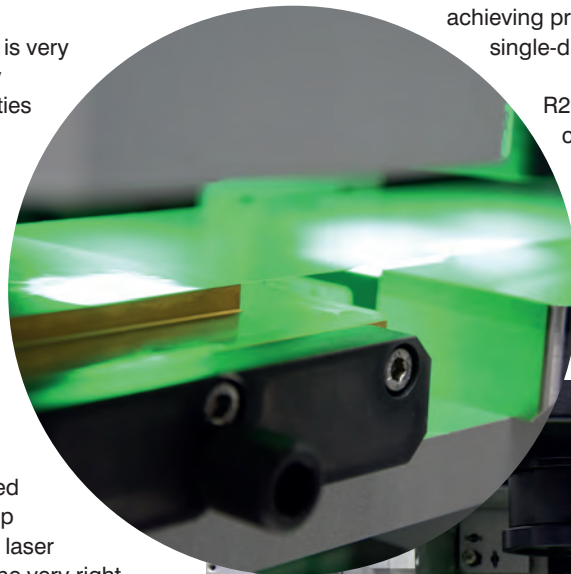
technology be adapted, optimized and transferred to thin-film R2R manufacturing? The answer ultimately proved to be ‘yes,’ but as is often seen in developmental work, adapting technologies frequently involves creating new approaches and machines to work with very different materials, especially at high speeds while retaining micrometer accuracy. 3D-Micromac achieved its goal by creating microFLEX: a cost-effective, reconfigurable laser micromachining system that supports myriad R2R applications for a global customer base.

Today’s R2R machining refers to a family of manufacturing technologies and processes that involve the continuous processing of a flexible substrate that is moving between two moving rolls of rotating material. The speed at which the films are processed depends in part on the width of the material, its thickness, and the processes involved, such as ablation, structuring of flexible solar cells, and so forth.

Advancements in the R2R field have made it an important class of substrate-based manufacturing processes in which subtractive and additive techniques are used to build structures in a consistent manner. High degrees of accuracy are possible, with 3D-Micromac systems often achieving precision within single-digit micron ranges.

R2R processes comprise many techniques that, when brought together, help produce rolls of finished material in a highly efficient

As laser processing is forceless and contactless, microFLEX guarantees a very selective machining of material stacks and extremely thin layers



Left: The microFLEX roll-to-roll laser micromachining system provides continuous on-the-fly processing for high machining speeds up to 50 m/minute



The modular machine concept of microFLEX allows the system design to be easily adapted to customers' requests

and economical manner. Chief benefits amongst many are high speed, high volume production. Comparatively low cost and high throughput are the key differentiators of R2R manufacturing compared to conventional techniques such as batch processing, which involves more steps. In comparing different approaches to the manufacture of solar cells, a thin-film R2R process producing CIGS PV cells is four times faster than other techniques, according to the US National Energy Research Laboratory (NERL).

Speed is a key cost driver in manufacturing, and faster throughput at high yield is a sizeable advantage in R2R processes. As noted, the actual speed of producing a range of products depends largely on the type of machining work that is needed, substrate thickness and width, and the number of passes that are needed to complete the entire manufacturing process.

When manufacturing thin-film medical devices, web speed is often 50 m/minute and throughput is 600,000 m²/a. The complexity of printed organic solar cells will typically 'slow' the process to 5 m/minute; the throughput drops to 500,000 m²/a. But as the 'flex' in microFLEX implies, the system is not only designed to work with bendable/soft substrates, it is by design a flexible, modularized system that can be grown or reduced in complexity to meet almost any micromachining need.

The microFLEX system supports R&D programmes requiring frequent retooling and reconfiguration to test new technologies. It also supports complex, high volume production environments in which configuration tends to be kept the same so that high speed, pinpoint accuracy and repeatability are achieved. But if one were to take customization to its practical limit, speeds could approach 80 m/second. Because the microFLEX modules use standardized

interfaces and data communication protocols, quality control and myriad process details can be easily checked and optimized. Additionally, several technologies can be integrated into one module. Today's investment can be built upon and either grown, reduced or reconfigured as customer needs change over time.

Additional benefits of laser micromachining include the fact that it is forceless and contactless, which is unlike mechanically punching through a material to achieve a desired shape. Laser machining thus frees manufactured products of burred edges, bulging and material residues. In on-the-fly laser ablation, material that is removed, such as aluminum, is fully recyclable. Unlike other manufacturing processes, laser micromachining involves no liquid chemicals, so when compared to liquid etchants, dry laser processing can be up to 10 times faster and there is no need to carefully store, handle or dispose of waste acids. The contactless quality of laser machining is especially beneficial when producing medical devices or other electronic components that need to be as free of microscopic debris as possible. In a microFLEX system, accuracy up to +/- 1.1µm at 1 m/minute is possible; the system also fully supports the use of biocompatible materials in single layers or multiple stacks.

The wide-ranging adaptability of microFLEX has led to its global adoption; microFLEX now comprises roughly 25 percent of 3D-Micromac sales. The majority of the company's micromachining systems are sold today across Asia, North America and Europe. The modularity of microFLEX has proved popular, with most customers highly customizing the systems now on their production floors. Although one might imagine that microFLEX would be adopted by contract manufacturers that would leverage its flexibility to switch between products as needed, Marketing Director Mandy Gebhardt said the systems they typically install are very purpose built. While researchers desire flexibility within a small configuration of modules, commercial manufacturers are interested in cost-effective, high volume throughput – their processes typically do not change once optimized. When change is needed, manufacturers either retool their system, or they add modules to support new goals and requirements.

Gebhardt added that the adaptable nature of microFLEX has spurred the company to build a system within its Chemnitz headquarters for on-going product development that also enables customers to see its potential on-site. This system is also used for localized contract manufacturing. At present, European customers are using the Chemnitz system to manufacture RFID



The microFLEX solution from 3D-Micromac brings new dimensions of substrate material choices, exactness, cost efficiency and sustainability. The laser technology enables extreme accuracy, smaller and repeatable patterns and provides for a production speed up to ten times faster than that of chemical etching processes

antennas and related components, medical devices, and flexible PCB for use in manufacturing LED/OLED lighting components.

“All the systems we have sold so far are customized to the requirements of the end user. In some cases, we first sold a more flexible system for product development. And some years later after finalization of the product, we sold a few specialized systems (cost-efficient, with high throughput) to the same customer. Every customer buys a special machine configuration for his special product, so they maximize cost efficiency and high throughput,” she remarked.

The microFLEX system offers a level of utility, speed and accuracy that customers appreciate as an ‘edge’ in winning their fight for international market share.

“The microFLEX solution from 3D-Micromac brings new dimensions of substrate material choices, exactness, cost efficiency and sustainability.

The laser technology enables extreme accuracy, smaller and repeatable patterns and provides for a production speed up to ten times faster than that of chemical etching processes,” said a European-based customer of flexible electronics and IoT applications.

The microFLEX system has grown into a unique application of laser micromachining technology that continues to find new homes across multiple industries. “An advantage for us now is that we have been developing and working on this system for 15 years now. We took all we knew about laser machining and applied it in R2R situations. We know the issues and we know what the customers need, and value,” observed Scholz.

Considering the evolution of microFLEX, Gebhardt noted that her company expects more development within thin-film photovoltaic cell manufacturing,



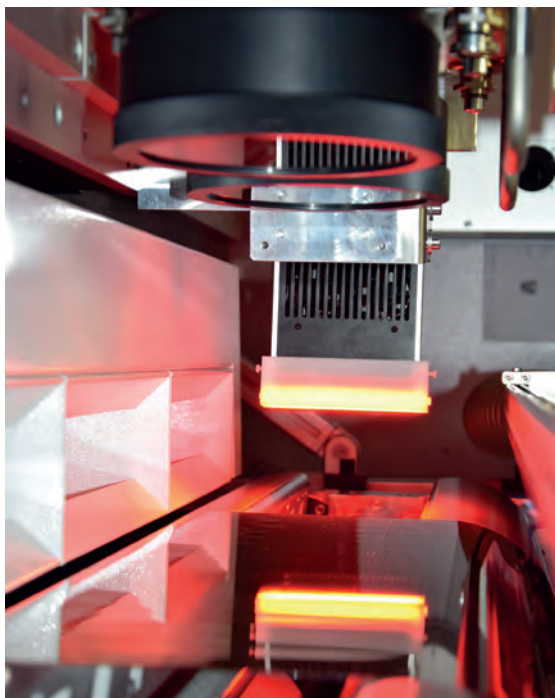


3D-Micromac offers R2R process development and contract manufacturing services for its customers

electronics such as OLED, and new types of various sensors, as well as support for the evolution of flexible circuit boards.

“I believe a few things have emerged over the years as we developed this technology that point to the future. First is the customer need – we support our

customers, and future customers, in optimizing their laser processes. For some, this is doing what they are doing now, but at higher volume. Often times, it involves processes the customer developed beforehand; he has a rough idea of what’s going on at a small scale, but often not roll-to-roll. They created a process using small sheets, and now they need to upscale it, and we are very good at helping with this. Sometimes a process needs to grow from small sheets onto one meter wide rolls – there’s a big difference.”



The processing of flexible thin-film photovoltaics has high process stability, reproducibility, and throughput requirements

“Technologically, we are seeing laser sources with hundreds of watts of power and very high repetition rates – in theory, they offer very high processing rates. But then there is the issue of precisely moving the laser over the materials surface and you have to do this with very high speed and with increasing repetition rates and increasing power at the same time that the machining rate is increased. We see the industry moving from galvanometric to polygonal scanners – six years ago this wasn’t as necessary, but in the future I can imagine the practice will be more widespread, and this is kind of a science in and of itself. There are challenges all along the way, and that is what we are constantly investigating. We have integrated the first polygonal scanners into our machines and it is working phenomenally. I believe there are many more things to come and the customer should always choose a partner that they can depend on for helping them take advantage of the best new technologies available,” Scholz concluded.

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Amorepacific uses imec EEG headsets for neuromarketing research

Traditional electroencephalogram (EEG) techniques are being supplanted by new generations of headsets that can measure and assess human brainwaves outside of traditional clinical settings. This ease of use has led to a growing number of investigational programmes designed to assess whether emotional reactions to specific stimuli can be linked to neural activity. This emerging science is giving rise to neuromarketing initiatives like those pursued by Korean cosmetic and health care giant Amorepacific that uses imec's investigational EEG headsets to research emotional reactions to fragrances. If successful, the approach may redefine how companies assess new products and refine marketing efforts in a way never before possible.

AN ELECTROENCEPHALOGRAPH is a test that detects electrical activity in the brain using small electrodes attached to the scalp. Traditionally, these tests were done in dedicated hospital labs where trained personnel attached the electrodes – one by one – and connected them to a large computer. EEGs done this way are accurate, but are also expensive, time consuming and limited to clinical facilities.

Thanks to chip and dry electrode technology, the days of traditional EEGs may soon be history. Leveraging years of technology development in the EEG field, electroencephalogram acquisition systems are now wearable and take few seconds to be installed, even by an untrained user. This makes wireless EEG headsets useful in wider therapeutic contexts, adding VR-based cognitive treatments, cognitive skill improvement and rehabilitation in addition to the more traditional applications such as epilepsy or sleep disorder research. And now, EEG tests are also being used outside of medical applications. With 'neuromarketing', more and more companies are

using unique EEG tools to better understand their customers.

Neuromarketing: understanding the customer without asking questions

The neuromarketing trend is gaining ground in many companies as technologies are emerging to link brain activity to human emotions and reactions. According to industry surveys, about 53% of the marketing industry already uses some form of neuromarketing in their everyday work to develop advertising campaigns and optimize websites; neuromarketing can also be used to develop concepts, innovate new products and package design as well as assess the 'shelf impact' of products in-store.

The term neuromarketing was coined some 20 years ago by Dutch professor Ale Smidts. The professor defined Marketing 1.0 as product-centered; Marketing 2.0 is consumer-centered, while Marketing 3.0 focuses on human values. Smidts said the best way to unlock these human values and emotions is by



using neuroscience and studying brain and biometric responses to better understand how consumers feel, think and act.

The reason why neuromarketing is so valuable is because people cannot in most instances accurately articulate their preferences and emotional reactions; humans seldom make choices rationally 100 percent of the time. As the famous marketer David Ogilvy said: “Consumers don’t think how they feel. They don’t say what they think, and they don’t do what they say.”

Do you remember how you felt when watching a commercial yesterday? How would your response to a questionnaire about this commercial differ from the actual reaction you had while watching it live? Neuromarketing and neurotechnology tools (like fMRI and EEG) do not rely on post-rationalization and memory. In this way, they tackle some of the greatest shortcomings of traditional research methods like surveys and interviews.

Amorepacific’s innovative journey towards a more beautiful world

The South Korean cosmetics firm Amorepacific is very interested in neuromarketing and EEG recordings. The company was founded in 1945 with a clear mission to present its unique perception of beauty – what it calls ‘Asian Beauty’ – to the world. With its world-class products represented in more than 20 cosmetics, personal care, and health care brand names, Amorepacific is acclaimed for the innovative ways in which it is transforming global beauty trends.

The company’s success and marketplace appeal relies greatly on the high-quality products based on innovative technology and natural ingredients. About ten years after its foundation, Amorepacific set up its very own R&D center, among the largest of any cosmetics company in the world. With a strong focus on research, innovation, and technological

advancement, Amorepacific today employs about 550 researchers to develop new materials for cosmetics and health to study the biology of skin health and aging and to find the optimal formulations for their products.

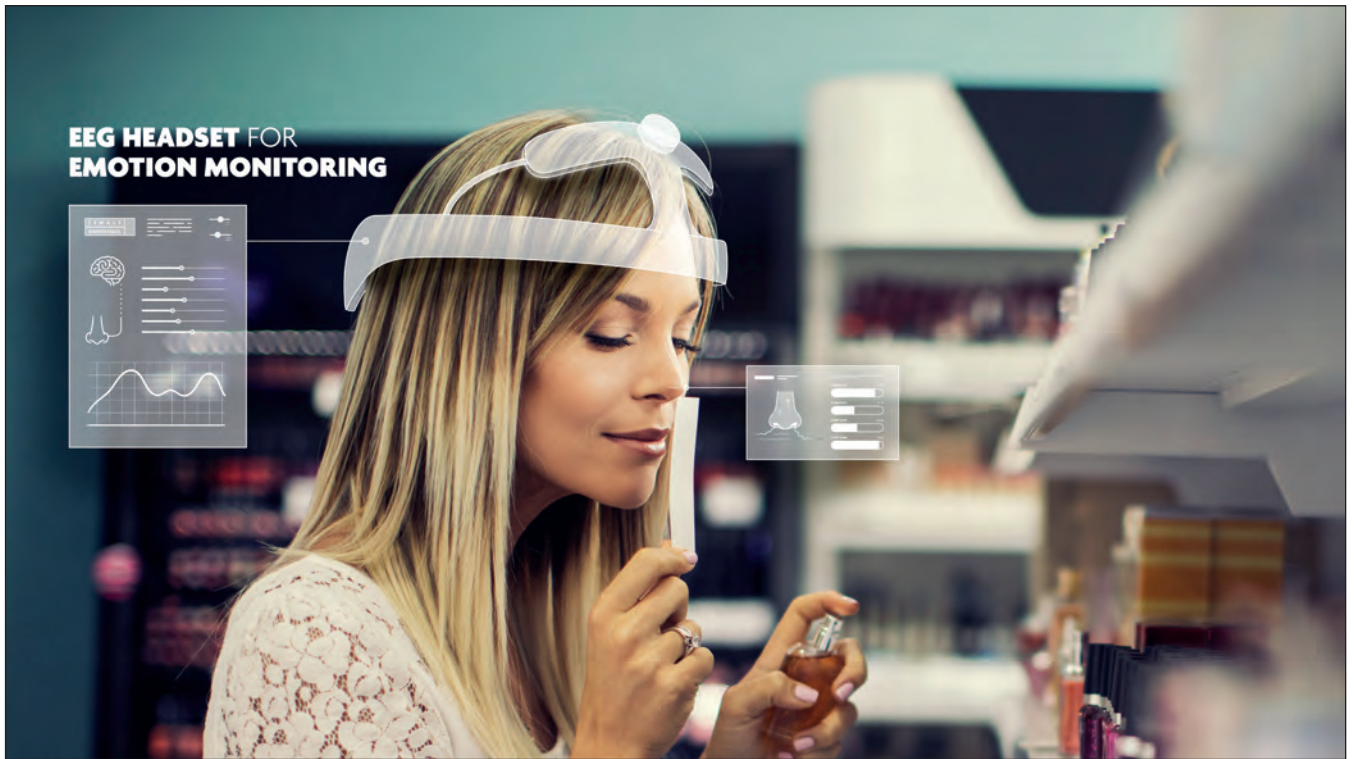
Measuring brain waves and emotions

Gusang Kwon is a researcher from the Amorepacific Consumer Insight & Innovation Lab. With a background in biology, psychology, neuroscience and neuromarketing, he started working at the company in 2016. His goal is to develop new tools for researching consumer behavior. During work on his PhD, Gusang gained a lot of expertise in using and interpreting EEG. Now he wants to deploy this brain research tool to gain more insights in the unconscious feelings and sensations of Amorepacific’s customers. According to Kwon, the company chose imec headset prototypes because of their user-friendliness, light weight, high number of EEG channels and imec’s assistance in developing dedicated algorithms for real-time emotion

Two of imec’s EEG headsets: the one from the press release in 2018 and the one developed for Amorepacific to be used as an investigational device for fragrance studies.



Right: Imec’s non-contact sensor solutions were demonstrated in this car seat prototype



EEG HEADSET FOR EMOTION MONITORING

A future vision of a brain-monitoring headsets that may one day help customers choose their favorite perfume by unlocking their unconscious feelings

monitoring. He explained that the company’s ultimate goal is to develop a unique customer experience for people shopping for their perfect perfume.

“As a researcher, I spend a lot of time going through papers and publications to learn about the latest technological developments in neuroscience. Back in 2019, I came across imec’s press release about an EEG headset for emotion detection. I was already experimenting for some time with commercial headsets to gain insights in the unconscious reactions and emotions of test persons while they use samples of our products. None of them satisfied my needs, especially in terms of the number of electrodes,” Kwon said.

A complementary tool for customer surveys

Navid Shahriari, project manager at imec in The Netherlands, briefly outlined how the collaboration began: “It was our business development manager Jiaqi Shen who introduced me to Gusang. First, we did a short feasibility study with Amorepacific in which we studied EEG measurements with our headset investigational device.”

“In 2020, we set up a second 10-month project to adapt our EEG headset to their needs and to combine these recordings with galvanic-skin-response measurements from our Chill+ wristband prototype. We made it more adjustable to fit different head shapes and sizes. Together, we will now train and tune our algorithms to estimate the fragrance response of test persons.”

“Our current design features digital active electrodes (DAE) that use imec’s latest chip design achieving a

low noise level, high input impedance (that allows us to work with the dry electrodes), higher dynamic range and amplification and digitization at the electrode. Continuous electrode-tissue impedance monitoring in the DAE chip provides information about electrode contact quality that could provide more insight about motion artefacts. Additionally we use Softpulse dry electrodes from Datwyler in our headsets, which provide comfort and signal quality without the need of gel,” Shahriari explained.

Gusang Kwon: “In our research with test panels, both smell and touch are important sensations. Think of people trying out different perfumes or skin-care products for example. Smells trigger very powerful emotions and are therefore a good starting point for our EEG studies. Traditionally, we use surveys to do market research. Our hope is to complement this with EEG recordings to better understand the unconscious emotional response to scent.”

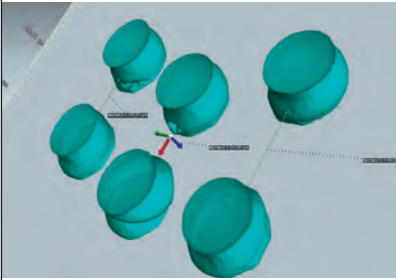
The future of the cosmetics industry: more technology and personalization

Gusang Kwon: “With imec’s EEG headset, we hope to develop a valuable tool for our research, our company and our customers. It could help to offer our customers a perfectly tailored solution, fitted to their conscious and subconscious needs. One day, we could even use neuroscience technology to help them choose the perfume that suits them best and give them insight into the emotions it triggers inside them.”

Amorepacific’s research highlights a trend towards more personalization that is growing in the cosmetics industry. As further example, Amorepacific introduced

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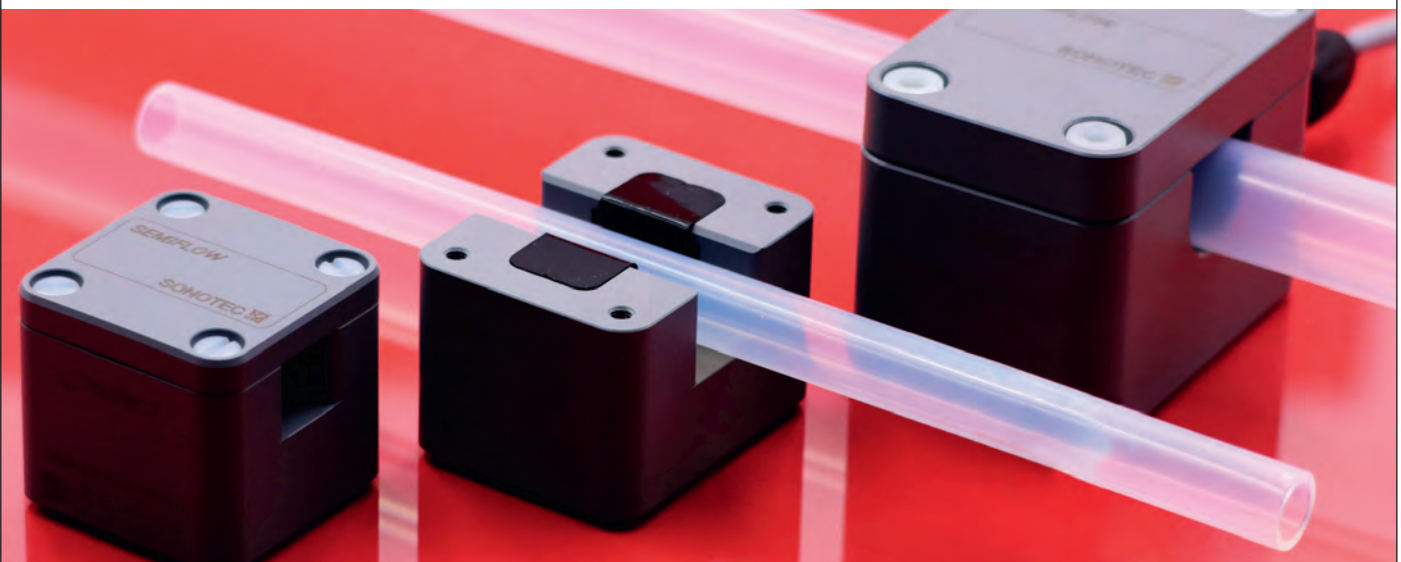
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its innovative technology called 'The Tailored Mask Pack 3D Printing System' at the 2020 Consumer Electronics Show. With this technology, users can print a personalized hydrogel mask pack that caters to individual facial features and skin conditions.

Gusang Kwon: "For sure, the cosmetics industry will integrate more technology in future products. Another important (capability), in my opinion, is non-contact sensing. Imagine one of our customers sitting in a smart chair at a shop that can measure emotions and biometric responses to assist in choosing the right perfume."

Navid Shahriari: "Indeed, imec also believes in the power of non-contact sensing. In a car, on a toilet seat, and why not – in a chair at a perfume shop. We are developing robust sensors and smart algorithms to make these kinds of measurements reliable. Of course, these sensors are aimed at measuring heart rate, breathing, etc. It's unclear whether we can do such a thing for brain waves."

Gusang Kwon: "I will certainly keep an eye on all new developments of imec. And I would highly recommend a collaboration with imec to other companies too. For me, working with imec exceeded my expectations in terms of quality of the prototype, help with the algorithm development and trial setup, as well as the

broad range of expertise that is present in the team. As a neuroscientist working in the cosmetics industry, it is great to be backed up by the wonderful team at imec, who can support me both on the technology and on the data interpretation. This for sure will help me to extend this neuromarketing activity in the company in the near future."

About Gusang Kwon

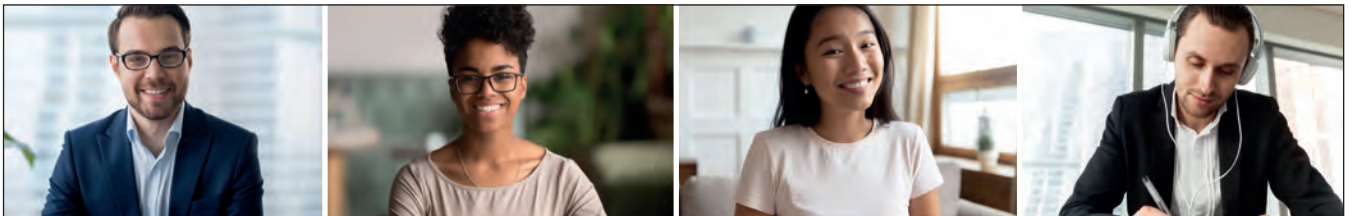


Gusang Kwon joined the R&D center of AMOREPACIFIC in 2016. Gusang majored in Cognitive Neuroscience and holds a Ph.D. degree from the Samsung Advanced Institute for Health Sciences & Technology, Sungkyun Kwan University, Korea. With over 15 years of experience in consumer tests, he is expanding his expertise in the field of neuromarketing and consumer neuroscience.

About Navid Shahriari



Navid Shahriari joined imec in 2017; he is a Project Manager within the Solutions Department. Navid holds an M.Sc. degree in Artificial Intelligence and Robotics from the Sapienza University of Rome, Italy, and a Ph.D. degree in Surgical Robotics from the University of Groningen, the Netherlands.



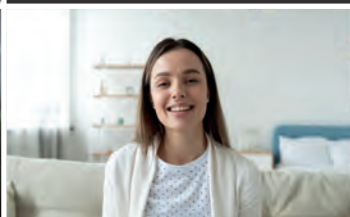
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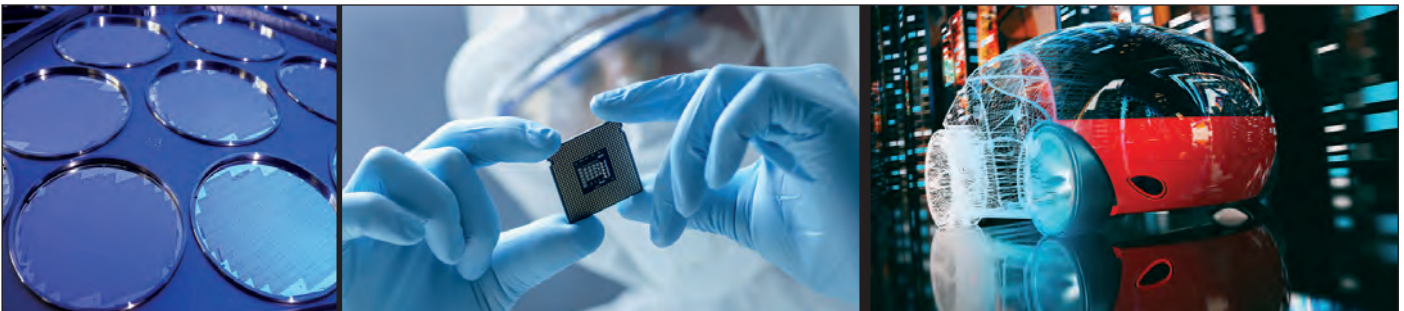
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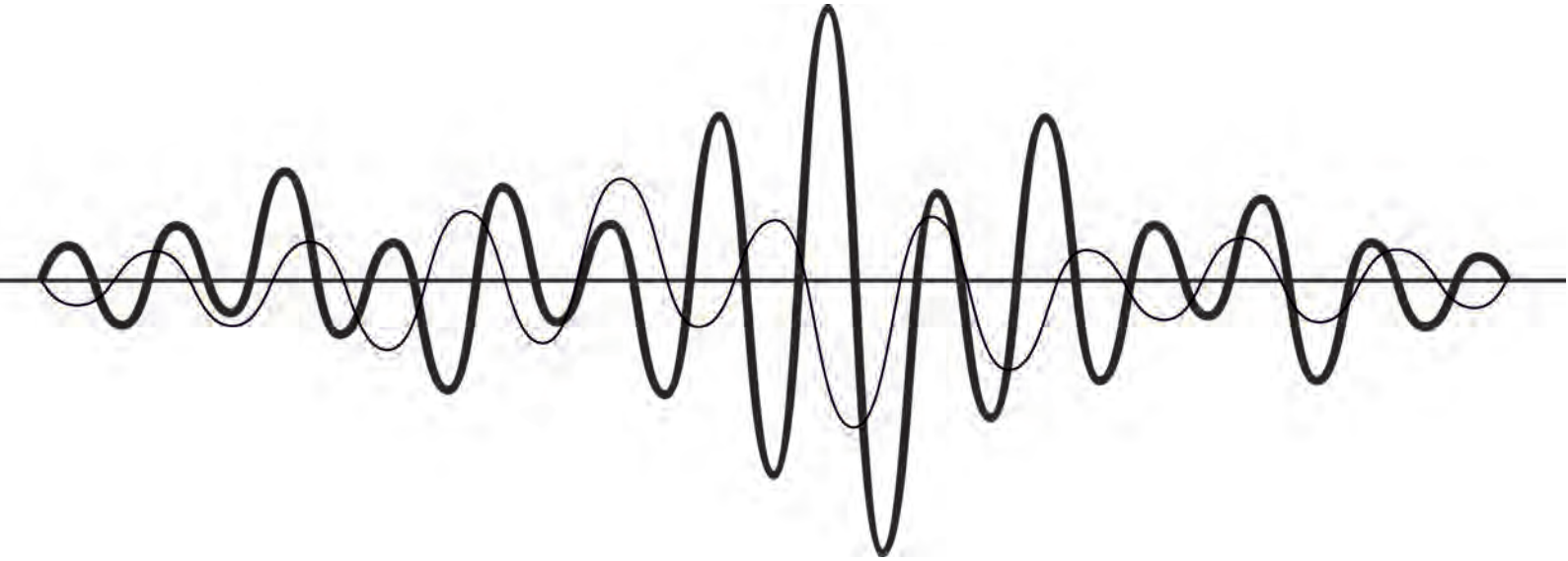
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Acoustically imaging the most **elusive defects**

Most defects are easily found before assembly by ultrasound in the form of an Acoustic Micro Imaging (AMI) tool, which fires ultrasound pulses into a component and analyzes the return echoes to identify defects, but some remain elusive.

BY TOM ADAMS, CONSULTANT, NORDSON SONOSCAN

CRACKS, delaminations, non-bonds and voids are among the names used for internal gap-type structural defects that may occur in electronic packages. They may, in service, react to thermal and mechanical forces in a manner that breaks electrical connections.

Most such defects are easily found before assembly by ultrasound in the form of an Acoustic Micro Imaging (AMI) tool, which fires ultrasound pulses into a component and analyzes the return echoes to identify defects. Components having defects are removed from production.

As the tool's scanning transducer moves along above an electronic component, it fires tens of thousands of pulses per second into the component. Each pulse is launched at a specific x-y location, and will send back

echoes from internal material interfaces, such as mold compound to silicon, that it encounters. The echoes are rich in information, and each one determines the color or grey shade of a pixel in the acoustic image.

The component being scanned may contain two types of internal interfaces:

- Bonded interfaces between two solids such as mold compound and silicon. Solid-to-solid interfaces reflect part of the pulse and transmit the rest deeper into the component.
- Interfaces between a solid and air. The air may have been incorporated into the device during fabrication. Solid-to-air interfaces reflect virtually all of the ultrasound back to the transducer. None travels into or through the air.

The solid-to-air interfaces are the top surfaces of voids, cracks and other internal structural defects containing air. Thermal or mechanical stresses may cause such a gap to expand and break electrical connections within the component. There are also internal anomalies that do not contain air. They are solid features that may be tilted, warped, or in the wrong place.

Most air-gap defects are easily detected and imaged by the AMI tool. The scanning transducer sends out tens of thousands of pulses per second as it scans at high speed over the component's surface. Each pulse is aimed at a specific x-y location on the component's surface and travels into the component. The transducer collects the echoes from internal interfaces from one location before it arrives at the next x-y location and launches the next pulse. In many of the imaging modes developed for the Nordson SONOSCAN C-SAM® tools, the highest-amplitude ("loudest") return echo at a given x-y location determines the color of the pixel at that location.

If a high-resolution 230 MHz transducer is being used, it is actually firing pulses with frequency content ranging from about 160 MHz to about 300 MHz. An outgoing pulse contains all of the frequencies in this range. The return echo can be differently distributed among the various frequencies depending on the nature of the interface. Typically, when the return echo arrives at the transducer, its amplitude is used to determine the pixel color for that x-y location. This is the sequence in what is called the Time Domain mode, in which other aspects of the echo (frequency, arrival time, polarity) are ignored.

The pulse-echo sequence is demonstrated in detail in Figure 1. The length and width of the arrow representing each pulse or echo approximates its amplitude.

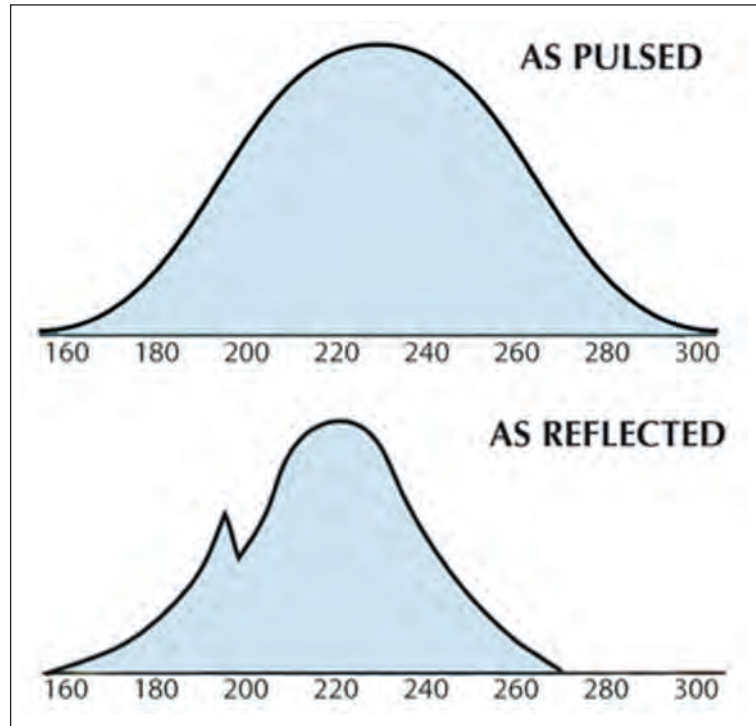
At left in Frame 1, the scanning transducer has fired a pulse into the top of a component. It travels through the first layer of material and strikes the interface between the first and second material layers. A portion of its energy is reflected upward toward the transducer.

In Frame 2, the remainder of the pulse encounters no anomalies. At the interface it crosses into the third layer, while a portion of its energy is again sent back to the transducer.

In Frame 3, the now much smaller pulse strikes the interface, and an even smaller echo is returned to the transducer.

In the right half of the diagram - in Frame 1, the events are essentially the same as in the left half.

But the portion of the pulse that enters Frame 2 finds not a solid-to-solid interface, but the top surface



of a void - in other words, a solid-to-air interface. Essentially all of the pulse's energy is returned to the transducer as a high-energy echo. Note that the size of the reflected echo is the same as that of the arriving pulse. No energy remains to enter the third material. At the x-y location of the echo, no interfaces directly below this point will be imaged.

But in some cases, an air-filled defect remains invisible to ultrasound. How does this happen?

As noted earlier, a 230 MHz pulse contains all frequencies from about 160 MHz to about 300 MHz. The frequency content in an echo created by this pulse will cover the same range, but possibly with a different distribution of frequencies.

But some solid-to-air interfaces may not be microscopically smooth, meaning that they can scatter the reflected ultrasound in various directions. The echo that returns to the transducer may have a unique frequency distribution. Air-gap defects of this type may be invisible to standard Time Domain imaging.

Each pulse striking the solid-to-air interface sends back an echo that includes all of the frequencies in the pulse, but a short range within those frequencies can be reflected at higher amplitude. In most modes, such as Time Domain imaging, the transducer selects the highest amplitude among all the echoes arriving at an x-y location to assign a color for each x-y location. In this situation it is possible for the smaller echoes and frequency-sensitive reflections to escape detection.

Figure 2 shows a small area of a large chip suspected of having a defect that had escaped detection by Time

Figure 1. Echo reflection (1) from solid-to-solid interfaces, and (2) from a solid-to-air interface.



Figure 2. Acoustically bright defect at right was not found by standard imaging.

Domain imaging. At left is the standard high-resolution 230 MHz Time Domain image, which shows no bright white areas that would indicate air gaps. Time Domain is an imaging mode that makes images based on the amplitude of the echo arriving from each of thousands of x-y locations within a specified time gate. The system typically selects the highest amplitude echo arriving at a given x- y location to determine the pixel color.

The image at left shows no bright areas that would indicate air gaps. Intent on finding a defect if one was present, researchers decided to use another resource: the Virtual Rescanning Module, or VRM. This mode first scans the component and in the process acquires the echo's amplitude, frequency and travel time from the interface to the component's surface.

VRM produces a matrix file containing all of the echoes from the entire volume of the component. The user can employ the matrix file to rapidly generate one image of the component at any of the frequencies between 160 and 300 MHz. Scanning of this 'slide show' can be done with either Time Domain or Frequency Domain imaging. At some point the user may find an image with a feature or features that did not show up in Time Domain imaging. In Figure 2, the frequency range in which the bright white defect appeared is in the range from 195 to 201 MHz.

The Frequency Domain scanned the VRM echoes of the area that had originally been scanned by the Time Domain. Scanning produced a single-frequency image of the area at each frequency generated by the 230 MHz transducer - that is, from 160 MHz to 300 MHz. Of these numerous images, only those in the 195-201 MHz range revealed the air gap near the right edge as a bright feature, seen in the right side of Figure 2.

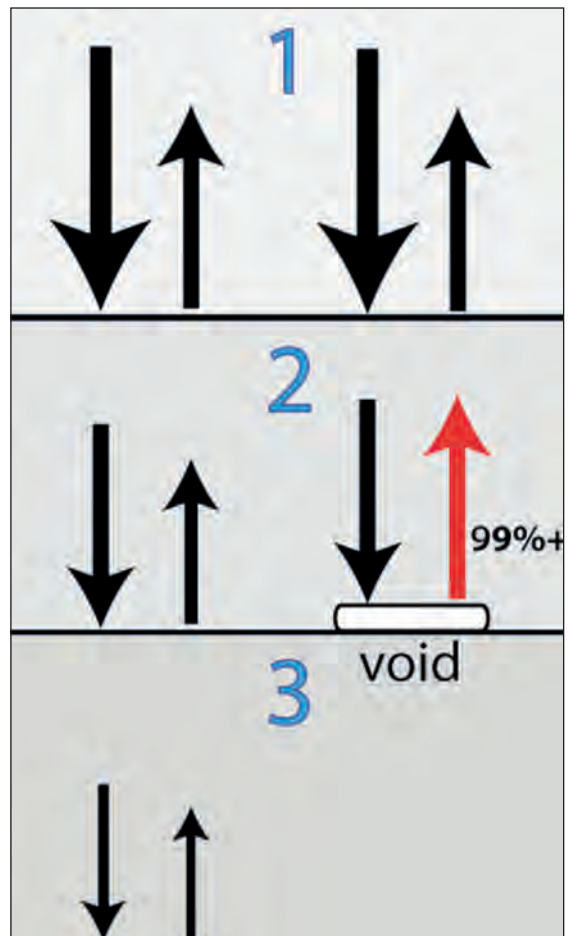
All the other frequencies lacked the image of the air gap and looked much like the Time Domain image at left. Conclusion: the bright white feature in the Frequency Domain image is an air gap and could

Figure 3. A defect may alter the range of frequency content of an echo.

easily have caused an electrical failure. But the air gap could only be revealed by going beyond the imaging modes customarily used for high-volume screening.

Figure 3 shows what can happen at the solid-to-air interface to cause the air gap to become harder to detect with Time Domain imaging. In the top diagram, the incoming pulse from the transducer shows the orderly distribution of the wide range of frequencies as they are traveling through the component, and before they strike a material interface that will reflect them. If the interface has no irregularities, the return echo will have the same distribution of ultrasonic frequencies as the pulse. But if an interface is not smooth, or if the air gap is not clean and unbroken, the distribution of frequencies changes, as seen in the hypothetical lower diagram in Figure 3.

The V-shaped irregularity in the bottom diagram marks the distribution of the 195-201 MHz reflection from each x-y location at the solid-to-air interface. Each echo from this interface will produce a bright white pixel, while locations outside the defect will produce darker pixels. The user is now free to use the Frequency Mode as part of high-throughput screening to mark for rejection any component in which this defect occurs.



angel tech VIRTUAL III

12.04.2021

Main Event:

Monday 12 April
10am BST
(British Standard Time)

China Taiwan Time

Recorded Event:

Wednesday 14 April
10am CTT, (BST +8 hrs)

Pacific Standard Time

Recorded Event:

Friday 16 April
10am PST, (BST -8 hrs)

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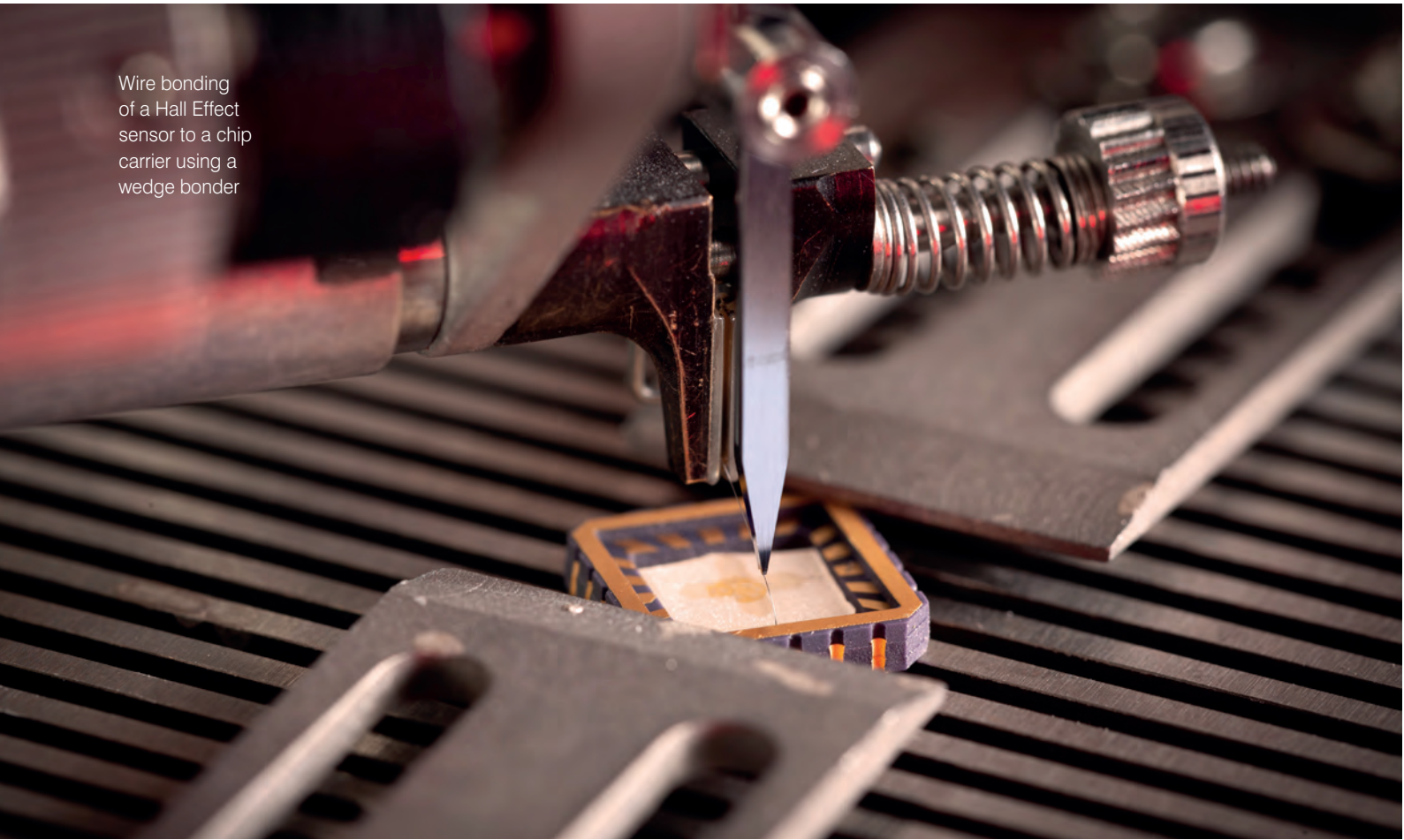
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Wire bonding of a Hall Effect sensor to a chip carrier using a wedge bonder



New graphene hall effect sensors deliver high performance

Graphene has long tantalized electronic device developers thanks to its unique 2D capabilities. But harvesting graphene while maintaining its most sought-after properties has proved elusive, delaying adoption. UK-based Paragraf and CEO Dr. Simon Thomas say the company is poised to disrupt the status quo with unique products including robust Hall Effect sensors; key to its success is Paragraf's new method of manufacturing graphene at scale to support commercialisation in electronic applications.

THERE HAS, for a long time now, been a buzz around graphene, the one-atom-thick allotrope of carbon that boasts some extraordinary properties around thinness, flexibility, robustness and electrical conductivity. The hyperbole has seen graphene grandiosely described as a 'wonder material' that is going to find transformative applications across the electronics sector.

However, living up to that heightened sense of expectation has not proved easy. To date, graphene as a material has largely failed to deliver on its potential in electronic device applications, primarily because of how it is manufactured and processed. With that in mind, a pertinent question needs to be asked: will graphene ever deliver on the hype?

To find an answer to that, we need to take a step back and look at some of the challenges of manufacturing graphene for use in the electronics sector. Most commercially produced graphene is either created by exfoliating graphite or forming the graphene onto a metal substrate – most commonly a copper foil. While exfoliating graphite produces good quality graphene, the graphene produced is typically very small in area, multi-layered, non-homogeneous and non-customizable; therefore, it is not suitable for electronic devices other than at the R&D level.

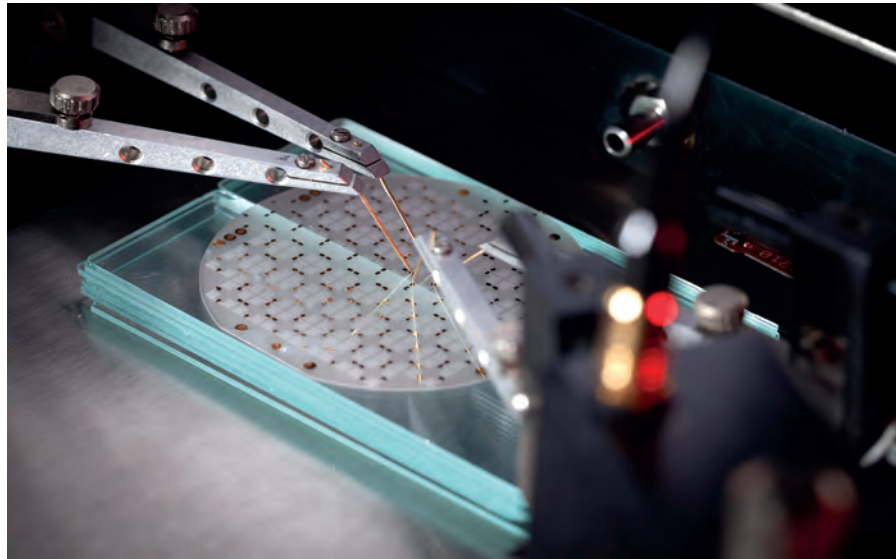
Graphene grown on copper foil, meanwhile, needs to be transferred onto an electronics compatible substrate after being synthesised, involving various wet and dry transfer processes that can affect how the graphene functions in an electronic device. It is also contaminated by the copper. These challenges mean there has been a lack of contamination-free, transfer-free, large-area graphene available in the market, and adoption in mass-market electronics remains slow. New solutions are clearly required if graphene is to make its mark in the electronics sector.

Novel technique holds real promise

Step forward Paragraf, who have caused quite a stir by developing an innovative method of producing graphene at scale. The excitement relates to a scalable and patented technology that uses processes to allow the manufacturing of large-area, high-quality graphene (currently up to 8" diameter).

The approach uses a modified deposition method that removes the need for the transfer processes commonly applied in most large area graphene synthesis methods. Therefore, the graphene can be produced in a uniform, single layer directly on a wide range of substrates, including silicon, silicon carbide, sapphire, gallium nitride, and other semiconductor-compatible substrates. It is also free from metallic contamination.

On the face of it, then, this scalable approach overcomes many of the challenges for developing graphene for electronics applications. The next step is to make the most of these advances by identifying suitable applications and bringing commercially viable products to market.



This process has already begun, with Paragraf's scientists and engineers developing a new graphene-based Hall Effect sensor. Existing Hall Effect devices, made from silicon, are primarily used for magnetic sensing. However, they have limitations in terms of sensitivity, accuracy and magnetic field range. Paragraf believes its graphene device will overcome many of these performance inhibiting parameters.

Electrical measurements of a Hall Effect sensor on wafer

So, let's look at those claims in a bit more detail, starting with the specifics of why graphene, as a material, is so suitable for use in a Hall Effect sensor. Crucially, graphene has a property called sheet carrier concentration: essentially the number of electrons available to move through the material carrying charge, which is very low. When configuring the material to interact with other electrical or magnetic fields, such as in a Hall Effect sensor, this property directly translates to a very high level of sensitivity in the device. In real terms this can be 30 to 50 times more sensitive than a standard semiconductor such as silicon.

Also, importantly, graphene is a two-dimensional material, meaning it does not exhibit the same directional properties as thicker, or bulk materials. For Hall Effect sensors this is particularly useful: one of the issues with traditional devices is the thickness

Graphene has a property called sheet carrier concentration: essentially the number of electrons available to move through the material carrying charge, which is very low. When configuring the material to interact with other electrical or magnetic fields, such as in a Hall Effect sensor, this property directly translates to a very high level of sensitivity in the device



Paragraf scientists performing electrical measurements of packaged devices

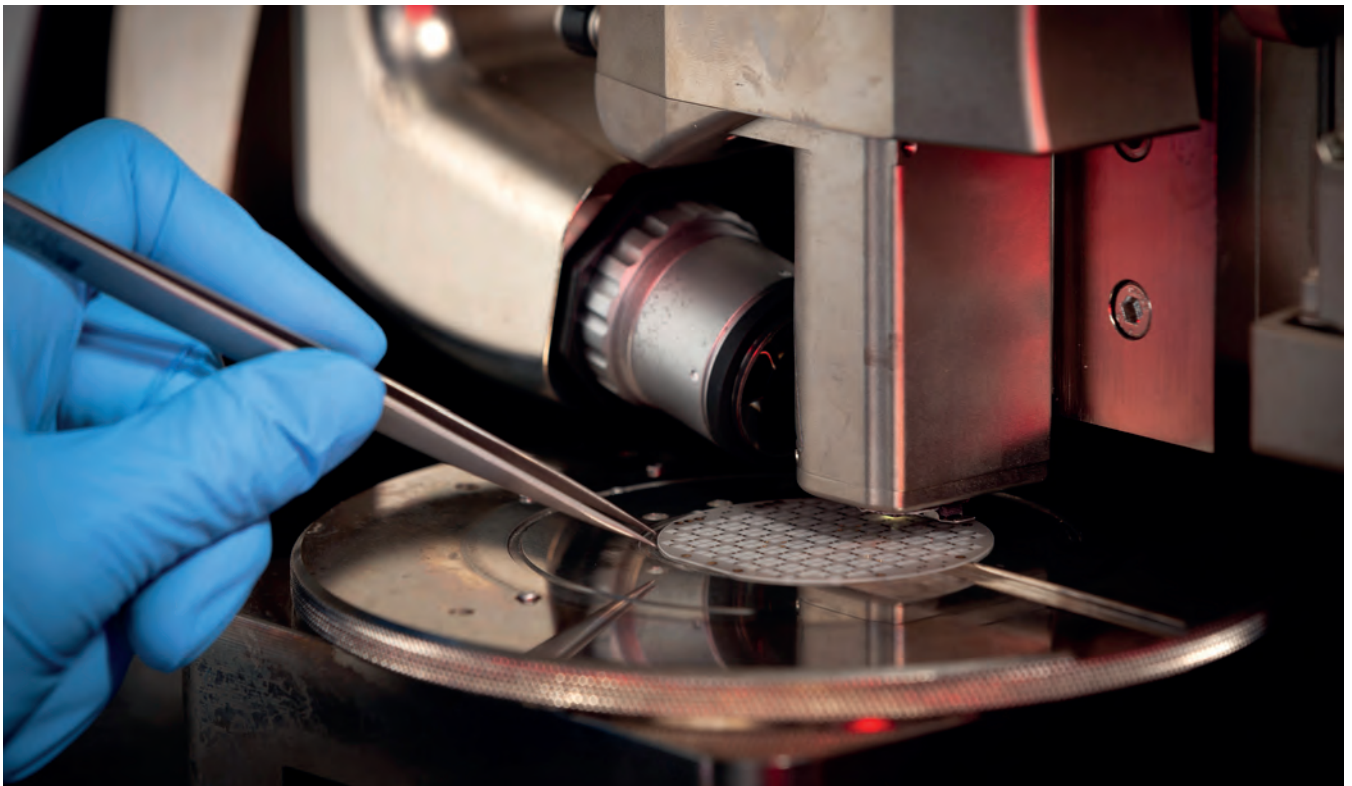
of the sensing material, which causes the sensing layer to be three-dimensional. This causes field components that are not perpendicular to the sensing direction to also be sensed, and as a result, false signals are produced. This is known as the planar Hall effect. The lack of a planar Hall Effect in Paragraf sensors is due to the inherent thinness of monolayer graphene, so these errors are removed, allowing for higher precision mapping of magnetic fields.

Also, graphene is very robust and does not suffer from the thermal impacts common with conventional

semiconductor devices. This allows the sensor to work at more extreme temperatures, much higher and much lower than standard silicon semiconductor devices. They can be used in extreme cryogenic temperatures at conditions of less than -271°C (1.8 K) and currently up to 80°C (353 K), meaning they can be used in superconducting environments while remaining highly sensitive.

As well as being resistant to thermal shock, no electrostatic discharge protection is required, so the sensors can be plugged straight into the mains (220V) without any adverse effects occurring. This makes the sensors easier to handle in industrial environments. The graphene-based Hall Effect sensors also have very low power dissipation – of the order of picowatts (pW) with nanoamperes (nA) drive current – so they will not heat cryogenic environments and will save energy compared to other Hall Effect sensors. These superior performance properties mean the Paragraf sensor provides the answer in a broad range of applications and technologies, without the restrictions of existing devices, says Dr Simon Thomas, Paragraf CEO.

“The resolution, combined with the lack of planar Hall Effect, gives it a very high accuracy capability, way beyond what is possible with any other Hall sensor on the market. Then, considering this comes in a small package which is robust in extreme conditions, you end up with a very attractive device which offers comparable performance levels to fluxgate sensors and NMR probes,” he explained.



Analysis of devices on wafer utilizing an atomic force microscope

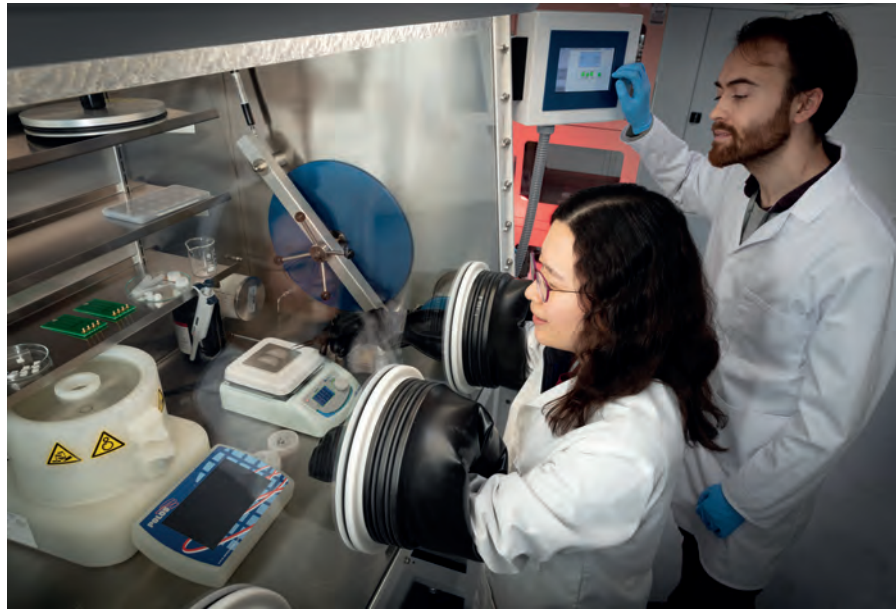
Field testing provides validation

The technical characteristics of the Paragraf sensor have been proven during field tests with several partners. For instance, Paragraf is working with the Magnetic Measurement Laboratory of the European Organization for Nuclear Research (CERN), which has tested sensors to see if they could accurately map the magnetic fields in electromagnets used within CERN's unique set up.

The field tests show definitively that Paragraf's sensor has a negligible planar Hall Effect and therefore only measures field components along the desired axis of measurement. CERN is looking to build a stacked mapping system of Hall Effect sensors that can provide very accurate magnetic field measurements using Paragraf's devices.

Paragraf has also been working with the UK's National Physical Laboratory to investigate the suitability of sensors in extremely harsh environments and with Queen Mary University of London to study the potential of graphene to replace Indium Tin Oxide in electronic devices.

"The Hall Effect sensor has demonstrated its versatility in a range of magnetic field measurement applications, and this is set to continue in the coming years. The operating temperature range and high sensitivity of the sensor open up application areas not previously possible," added Thomas.



"One example is the aerospace industry where they could be embedded into aircraft engines for the continuous monitoring of faults in real-time.

Also, once the testing work with the NPL is complete, and the sensor is shown to be capable of operating in harsh radiation environments, applications could include use as positional sensors within nuclear-decommissioning robots and space satellites," he concluded.

Paragraf scientists performing experiments on devices inside a glovebox

EC-funded Graphene Flagship develops new transfer technology

THE ENTICING PROMISES of utilizing 2D graphene to manufacture advanced photonic and electronic devices has fueled billion-euro investments across industry and academia. But bringing graphene into practical, widespread use has proved elusive. A significant stumbling block has been transferring 2D materials from growth media to target substrates. Conventional approaches are typically not compatible with high-volume manufacturing or significantly degrade the 2D material.

Enabling the full potential of graphene for European manufacturers is a central goal of the EU's Graphene Flagship. On 10 February Graphene Flagship researchers announced a new method to transfer graphene into conventional manufacturing. Researchers in Sweden and Germany initially reported their methodology in a recent 'Nature Communications' article.

"There's always this critical step of transferring (graphene) from a special growth substrate to the final substrate on which you build sensors or components," remarked Arne Quellmalz, a researcher at KTH Royal Institute of Technology and the article's lead author. "You might want to combine a graphene photodetector with silicon read-out electronics, but

the growth temperatures of those materials is too high, so you cannot do this directly on the device substrate." According to Flagship researchers, the appeal of their solution lies in using existing semiconductor manufacturing toolkits: combining a standard dielectric material, bisbenzocyclobutene (BCB), with conventional wafer bonding equipment.

"We basically glue the two wafers together with a resin made of BCB," explained Quellmalz. "We heat the resin until it becomes viscous, like honey, and press the 2D material against it." At room temperature, the resin becomes solid and forms a stable connection between the 2D material and the wafer, Quellmalz said. "To stack materials, we repeat the steps of heating and pressing. This work is an important step ... although many further challenges remain, the range of potential applications is large. The integration of 2D materials could be a real game-changer for the European high-tech industry," concluded Prof. Max Lemme of Graphene Flagship partners AMO GmbH and RWTH Aachen University.

The new Graphene Flagship 2D material transfer process differs from proprietary approaches of UK based Paragraf, which is already using its process to manufacture commercial devices including sensors.

Scaling CMOS beyond FinFETs:

From nanosheets and forksheets to CFETs

The FinFET transistor architecture is the workhorse of today's semiconductor industry. But as scaling continues, undesired short-channel effects require the introduction of new transistor architectures. In this article, Julien Ryckaert, program director of 3D hybrid scaling at imec, sketches out an evolutionary path towards 2nm and beyond technology nodes. Part of these insights were presented at the 2019 IEEE International Electron Devices Meeting (IEDM).



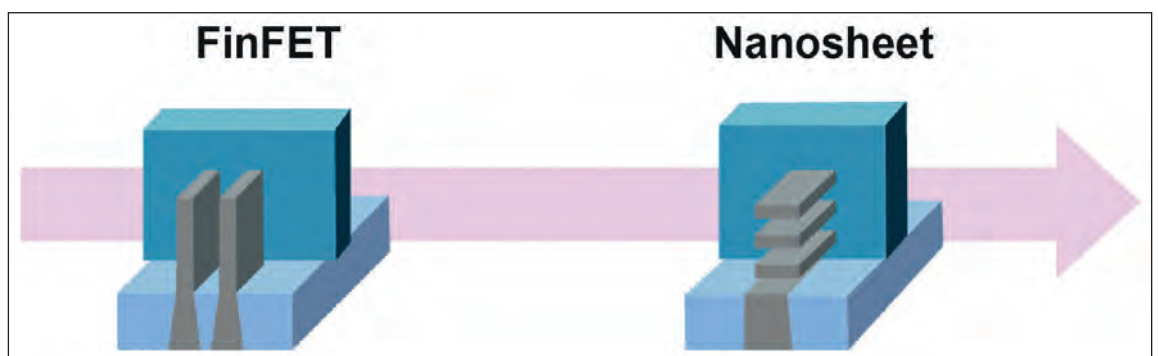
The FinFET: today's leading-edge transistor

At every new technology generation, chipmakers have been able to scale transistor specs by 0.7x, delivering a 15% performance boost, a 50% area gain, a 40% power reduction as well as a 35% cost decrease at device level. Several years ago, the industry made the transition from 'good old' planar MOSFET to FinFET transistor architectures in order to maintain this scaling path. In a FinFET, the channel between source and drain terminals is in the form of a fin. The gate wraps around this 3D channel, providing control from 3 sides of the channel. This multi-gate structure was designed to eliminate short-channel effects, which starts to degrade the transistor's performance at reduced gate lengths.

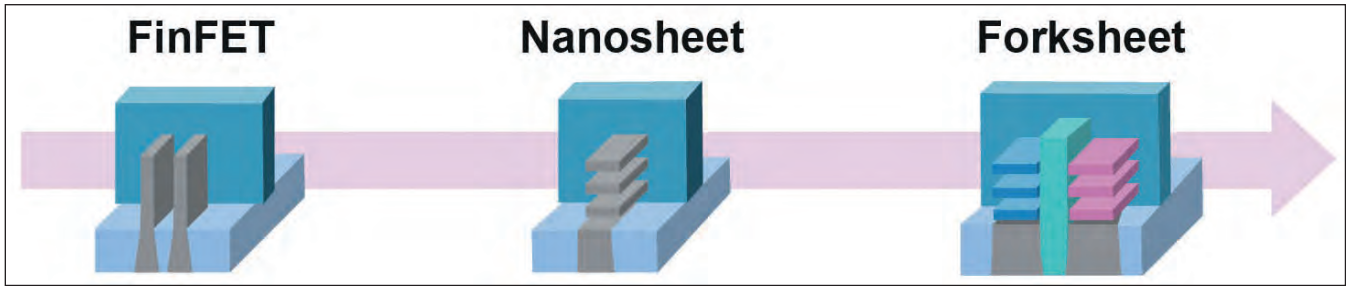
Superior short-channel control is crucial since it sets the foundations of device scaling – allowing shorter channel lengths and lower operating voltages.

The first commercial 22nm FinFETs were introduced in 2012. Since then, FinFET architectures have been improved for enhanced performance and reduced area. For example, the 3D nature of the FinFET allowed an increase in fin height to obtain a higher device drive current within the same footprint. Today, industry is ramping up production of 10nm/7nm chips with FinFETs 'inside.' At the cell level of the most advanced nodes, standard cells with a track height of 6T (which is a measure of the cell area) feature down to 2 fins per device.

Vertically stacked nanosheets: an evolutionary step
But as scaling is pushed beyond 5nm, the FinFET is expected to run out of steam. At reduced gate length, the FinFET structure in turn fails to provide enough electrostatic control. FinFETs cannot be reduced in size beyond a certain point if the goal is improved performance as well as reduced area. On top of



Natural evolution from FinFET to nanosheet



that, the evolution to lower track height in standard cells requires a transition to single-fin devices, which cannot provide enough drive current even if fin height is further increased.

With changing technology nodes, the semiconductor industry is however not eager to switch to other transistor architectures. Changing architectures can prove costly if the design is not manufacturable at high yield or desired performance is not achieved. Some manufacturers might even decide to stay at certain nodes longer. But still, there are applications – such as machine learning, big data analysis and data center servers – that will require the latest ‘universal’ CMOS solutions. With such a universal CMOS solution, one and the same transistor architecture in one and the same technology node can be used to perform all functionalities on the chip.

Here, vertically stacked nanosheet transistors can come to the rescue. They can be considered a natural evolution of the FinFET device. Just imagine placing a FinFET on its side, and dividing it into separate horizontal sheets, which make up the channels. A gate now fully wraps around the channel. This gate-all-around nature of the nanosheet provides superior channel control compared to the multi-gate FinFET. At the same time, the more optimal distribution of the channel cross-section in the 3D volume optimizes the effective drive per footprint.

The need for scaling boosters

The migration to nanosheet devices becomes optimal at low cell track heights of 6T and 5T, where fin depopulation would degrade drive current in traditional FinFET-based cells.

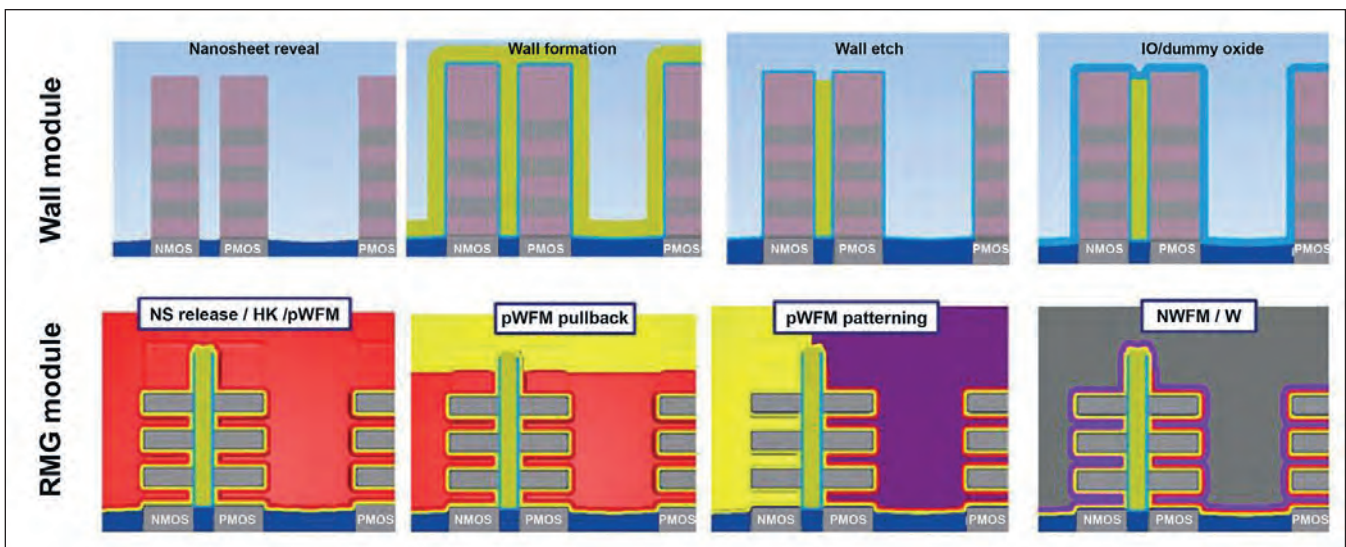
Natural evolution from FinFET to nanosheet, and to forksheet

But reducing track heights (and hence, cell area) from 6T to 5T cannot happen without introducing structural scaling boosters such as buried power rails and wrap-around contacts.

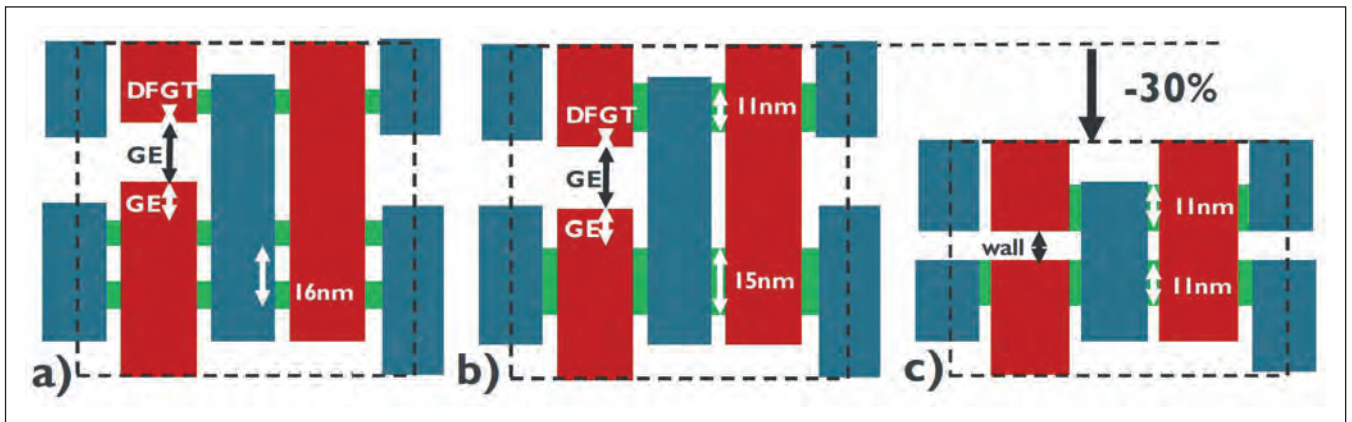
Power rails provide power to the different components of the chip and are traditionally implemented as metal lines in the chip’s BEOL (i.e., the Mint and M1 layers). There, however, they occupy considerable space. In a buried power rail construct, the power rails are buried in the chip’s front-end-of-line to help free up routing resources for the interconnects. Moreover, they provide a lower resistive local distribution of the current to a technology that suffers from increasing BEOL resistance with pitch scaling. By removing the power rails from the back-end-of-line, the standard cell height can be further reduced from 6T to 5T.

The next step: reducing the spacing between p and n

As the journey to smaller track heights continues, a further reduction of cell height will require a much tighter spacing between nFET and pFET devices within the cell. However, for both FinFET and



Key steps in the forksheet process flow, showing the wall formation step after active patterning



Layout of SRAM half cells for a) FinFET, b) gate-all-around nanosheet and c) forksheet. The forksheet can provide up to 30% scaling of the bit cell height as the p-n space is not governed by gate extension (GE), gate cut (GE) or dummy fin gate tuck (DFGT).

nanosheet devices, process limitations pose a limit to how close these n and p devices can be brought together. In FinFET architectures, for example, 2 dummy fin spacings are typically required between n and p, consuming up to 40-50% of the total available space.

To extend the scalability of these devices, imec has recently proposed an innovative alternative architecture, called the forksheet device. The forksheet can be considered a natural extension of the nanosheet device.

There are important differences between nanosheet and forksheet device architectures. Unlike a nanosheet device, forksheets are controlled by a forked gate structure, realized by introducing a dielectric wall in between the p- and nMOS devices before gate patterning. This wall physically isolates the p-gate trench from the n-gate trench, allowing a much tighter n-to-p spacing.

The process flow used for making forksheet devices is similar to the flow used to make nanosheet devices, with only a few additional process steps. The dielectric

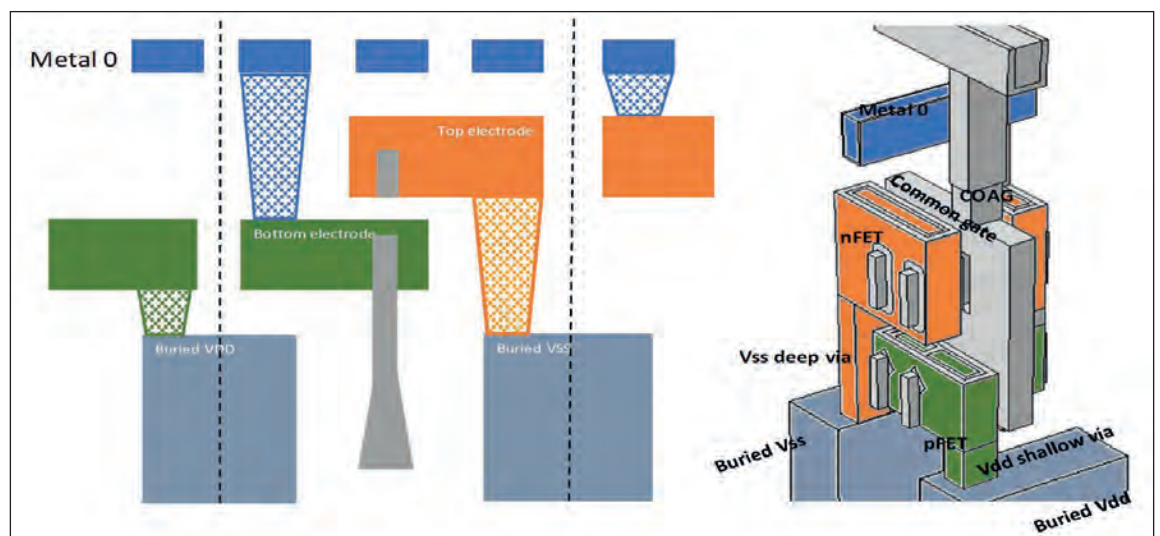
isolation between n and p even holds a few process advantages, including, for example, a more simplified process for filling the work function metal. On top of this process window enhancement, the forksheet is expected to have superior area and performance scalability due to the large reduction in n-to-p separation.

The forksheet device: improved performance and area

Researchers at imec have recently used TCAD simulations to quantify the expected power-performance-area (PPA) potential of the forksheet device architecture. The device under study targets imec's 2nm technology node, using a contacted gate pitch of 42nm and a 5T standard cell library with a metal pitch of 16nm. The proposed design includes scaling boosters such as buried power rails and wrap around contacts.

Compared to a nanosheet device, a 10% speed gain (at constant power) and a 24% power reduction (at constant speed) has been calculated. This performance boost can be partly explained by a

The CFET architecture forming a stacked p-n CMOS primitive structure with 2-level local interconnects



1000



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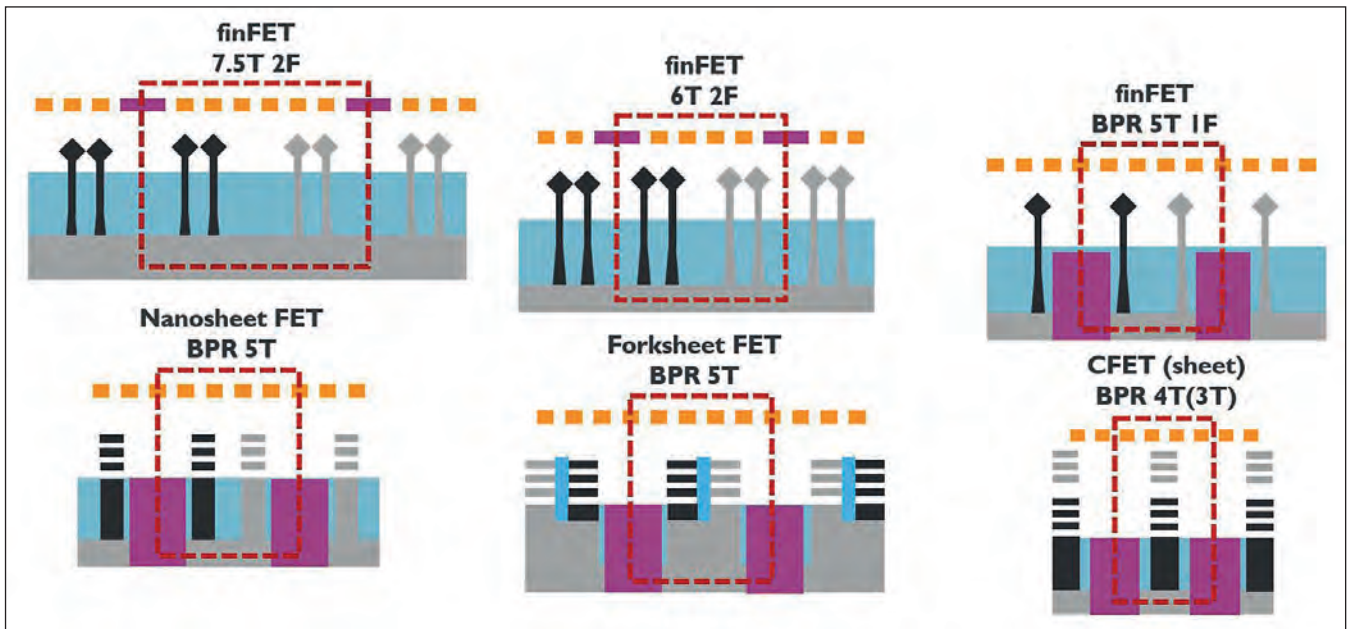
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From FinFET to nanosheet, to forksheet and to CFET

reduced (parasitic) Miller capacitance, resulting from a smaller gate-drain overlap. The available space can also be used to increase the sheet width, and as such enhance the drive current. Finally, the n-to-p separation reduction can be exploited for shrinking the track height from 5T to 4.3T – resulting in a 20% cell area reduction. When implemented in an SRAM design, the simulations reveal a combined cell area scaling and performance increase of 30%, for 8nm p-n spacing.

The forksheet can be considered a next step in the natural evolution from planar to FinFET and then to vertically stacked nanosheets. The above characteristics demonstrate its potential as an ultimate logic ‘universal’ CMOS device for the 2nm technology node. In further research, the process challenges to fully bring these devices into manufacturing need to be resolved.

CFET: the road towards 3T logic standard

cells

Beyond 5T, a further reduction of the cell height is now mainly limited by routability issues – which should be evaluated at the logic block level. Optimizing routability brings us to the CFET or complementary FET device – pushing the horizon for Moore’s Law further out. The concept of CFET consists in ‘folding’ the nFET on top of the pFET (either fin-on-fin or sheet-on-sheet) – as such fully exploiting the possibilities of device scaling in 3D.

By its stacked nature, the CFET exhibits 2 levels of local interconnects – providing more freedom for internal cell routing and for reducing cell area. Routing between cells can also be largely improved.

First assessments have shown that a FinFET-based 4T CFET can match and even surpass the standard cell power-performance metrics of a 5T ‘standard’ FinFET device. It can also yield standard cells and SRAM cells with 25% smaller layout area. A nanosheet-based CFET could offer an extra performance boost and be necessary for scaling down to a 3T logic standard cell.

Conclusion

In this article, imec has mapped out an evolutionary path towards ultimately scaled logic devices for 2nm and beyond technology nodes. After today’s mainstream FinFET comes the nanosheet device, offering superior channel control with limited additional process complexity. When complemented with scaling boosters, standard cells with 5T track height come within reach. As a next step, the forksheet may enter the scene, offering a path to 4.3T cells due to a reduced n-to-p spacing. First simulations confirm its potential for the 2nm technology node. The CFET completes the roadmap as the ultimate compact CMOS structure, holding promise for 3T logic standard cells.

About Julien Ryckaert



Julien Ryckaert received a M.Sc. degree in electrical engineering from the University of Brussels (ULB), Belgium, in 2000 and his PhD degree from the Vrije Universiteit Brussel (VUB) in 2007. He joined imec as a mixed-signal designer in 2000 specializing in RF transceivers, ultra-low power circuit techniques and analog-to-digital converters. In 2010 he joined the process

technology division in charge of design enablement for 3DIC technology. Since 2013, he has been in charge of imec’s design-technology co-optimization (DTCO) platform for advanced CMOS technology nodes. He is now program director, with a focus on scaling beyond the 3nm technology node as well as 3D scaling extensions of CMOS.

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Exploring emerging applications for photonic integrated circuits

Photonic integrated circuits (PICs) have emerged as key component-level enablers of next generation datacom/telecom systems that require smaller, more efficient transceivers and switches. These same qualities are opening doors across widely varied applications ranging from vehicle autonomy to quantum computing and beyond.

BY ANA GONZALEZ, R&D MANAGER AT EPIC



MINIATURIZATION, higher performance, vibration immunity, reduced footprint and low heat generation are some of the clear benefits of adopting photonic integrated circuit (PIC) technologies for developing new photonic products. PIC technology meets the requirements for the development of new, exciting applications such as point-of-care devices, miniaturized LiDAR, quantum computing, structural monitoring and wearables for healthcare. In this article, we explore some of these emerging applications together with the companies at different levels of the PIC supply chain that can provide the technology required for the design, fabrication, packaging and scaling up volumes for PIC-based modules.

Although PICs have been used extensively in datacom and telecom, there are other application fields in which this technology is attracting increasing attention. An example is the automotive market, as a result of increasing demand for safety and advanced driver-assistance as well as autonomous driving systems, some companies such as Omnitron Sensors, Fastree 3D, Mouro Labs, Beamagine and LuxC are pushing the development of new LiDAR systems. LiDAR based on PIC technologies is potentially cheaper, lighter, more compact and more reliable—PIC based LiDARs have no moving parts.

To meet the increasing demand for automotive LiDAR systems, a growing number of companies have moved into the development of PIC-based LiDAR systems and components. Lumentum is one such company; for short-range LiDAR (10-50 m) and in-cabin monitoring, Lumentum provides high-power 940

nm VCSEL array illuminators. For long-range (200 m), they offer 1550 nm narrow-linewidth DBR diode lasers for long-range frequency-modulated continuous-wave (FMCW) coherent LiDAR. Both of these devices are designed to be time-of-flight (ToF) light sources for flash systems and are really intended to provide more power. To reach much higher power levels, longer distance, higher resolution and the performance required by automotive LiDAR, Lumentum have developed two innovative solutions: multi-junction addressable VCSEL arrays and bottom emitting devices.

MULTI-JUNCTION VCSEL ARRAYS:

By increasing the number of junctions, the number of photons emitted can be also increased with the same type of overall wall plug efficiency. This allows the low currents, typically used in two or three junctions, to produce higher levels of power and faster applications.

BOTTOM EMITTING DEVICES:

These allow fabrication of devices with no external optics and the ability to modify the beam profile. Basically, an external lens is put on the back of the device and the chip is flipped upside down and then mounted top down onto the sub-mount. This allows integration of multi-junction adjustable arrays and optics to create new and novel gallium arsenide patterns, which will be required for the next generation of detector devices (see Figure 1).

There are other companies providing VCSEL arrays for LiDAR, such as Array photonics, Bandwidth10 and Astrum. Different types of lasers can be also

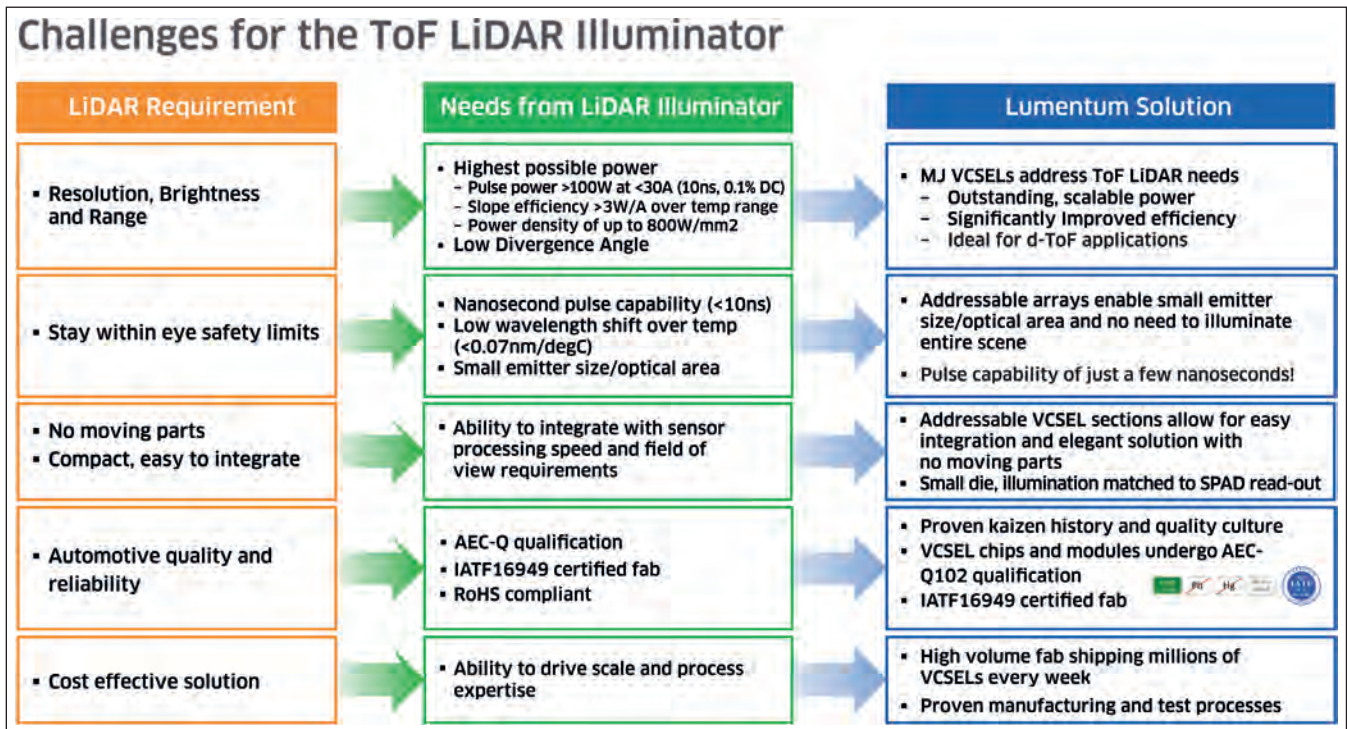


Figure 1. Bottom Emitting Integrated Optics Configurations (courtesy by Lumentum)

employed for LIDAR, such as the ones provided by companies including Lumibird, Bright solutions, Eblana photonics, BKtel and RIO.

Another company working on a cost-effective solution for improving vehicle perception is SCANTINEL PHOTONICS, a spin off from Carl Zeiss AG, that uses coherent Frequency-Modulated Continuous Wave (FMCW) ranging to achieve longer distance by using a 1550 nm integrated swept source with a narrow bandwidth and high linearity (see Figure 2). This enables the system to generate reliable, high range three-dimensional images of the environment required for autonomous navigation.

Coherent ranging allows the photonic integration of the lasers, detectors, and a large part of the optical components on a silicon wafer platform, which eliminates error-prone assembly and calibration steps. The core concept of the system is its scalability to high pixel rates through efficient multiplexing, which is achieved by using a high parallelization of different FMCW channels.

Using PICs to create an optical enhanced array (OEA), enables high integration of the system, low power, and solid-state scanning up to a range of 300 meters as well as the option to scale up to high volumes at very competitive price points. SCANTINEL collaborates with partners such as imec, a leading European research centre in the field of

silicon photonics with whom they are working on solid state beam steering, and PHIX, a packaging company for large-volume photonics manufacturing.

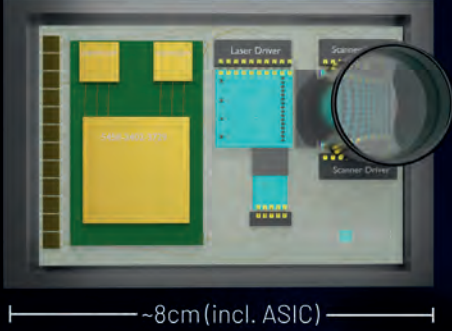
Fabricating proof of concept chips or taking proven designs to initial prototype stages is a costly process, so a number of European foundries offer multiproject wafer (MPF) services including:

- **Silicon Nitride (SiN):** CNM, imec, Lionix and LIGENTEC
- **Indium Phosphide (InP):** Smart Photonics, Fraunhofer HHI, 3-5 labs
- **Silicon Photonics (SiP):** VTT, imec, ihp and Cornerstone

Multi project wafer foundries fabricate different chips in the same wafer to reduce costs in the prototyping phase. Another option is the JePPIX Pilot Line that was launched in 2019. JePPIX aims to provide companies with direct access to state-of-the-art manufacturing InP chips from proof of concept to industrial prototyping and pre-production. Applications include fibre-optic communication, biomedical devices, next generation mobile and portable devices, astrobiology, and quantum computing. Foundries also offer Process Design Kits (PDKs) for circuit simulation and mask design to aid in the process of turning concepts into chips. The PDKs can be implemented in different software packages offered through Synopsys, VPI Photonics, Lucedra, Lumerical, Nazca and PhotonDesign.

Scantinel's approach is a 1550nm Solid-state FMCW LiDAR

Our Product:



~8cm (incl. ASIC)

Our Approach:

- Coherent FMCW ranging
- 1550nm integrated swept source with narrow bandwidth and high linearity
- Combination of photonic integrated chip and optical collimator for scanning (Optical Enhanced Array - OEA™)
- Silicon photonics to enable a full solid-state solution for high volume scalability
- Parallelization of multiple FMCW channels to achieve high MP/s data rate

EPIC Online Technology Meeting on Exploring Emerging Applications for Photonic Integrated Circuits.
Scantinel Photonics GmbH, Davide Canavesi

www.scantinel.com

Figure 2. Scantinel's 1550 nm FMCW LiDAR approach (courtesy by SCANTINEL PHOTONICS)

Luceda Photonics, based in Belgium, provides software and services for an integrated approach, enabling photonics IC engineers to enjoy the same first-time-right design experience as electronic IC designers. To this end, they have their IPKISS integrated photonics design platform based on Python. This platform is a scripting environment that covers the complete photonic IC design flow up to measurement feedback for true component characterization and validation. The components rely on a single, centrally defined model for a smooth transition between the different design stages such as layout, physical and circuit simulation. This makes the design flow robust, reduces design errors and saves considerable design time.

The IPKISS platform is modular and can be extended to integrate with EDA design flows via their IPKISS.eda module. This module can be plugged into the IPKISS platform to allow parametric cells to be exported to EDA tools, thereby enabling PIC designers to enjoy the benefits of a professional EDA environment and the ability to exercise good control over the details of complex components. It affords automation and control across all levels from the component to the circuits - a feature particularly attractive for both LiDAR and quantum computing applications.

Another company working in the field of simulation software is VPI Photonics. They have participated in a number of industry-leading research projects, the most recent of which is PlasmoniAC, an EU-funded project that aims to develop a radically new

circuit-technology for neuromorphic computing based on plasmons. The idea is to create high-speed neuromorphic chips that are low-cost, energy-efficient, and compact with the aim of strengthening the competitiveness of the European photonics industry to play a greater role in the global neuromorphic and deep learning market. The project basically leverages the energy and size efficiency of plasmonic circuits and applies them to neuromorphic computing architecture. VPI's contribution is to develop an add-on model library for plasmonic devices for use in conjunction with their photonic integrated circuit models to allow their customers to build and simulate neuromorphic circuits as well as evaluate their performance.

PICs are envisioned as a key technology in the near-term deployment of metropolitan quantum-key-distribution-based secure systems that leverage the fact that entangled photons can be individually generated, modulated and routed on the PIC. Companies such as QuSide Technologies and Quix develop PIC based devices for random number generation.

Another application is the development of quantum computing being pursued by companies such as XANADU, a quantum photonics computer company with a mission to build quantum computers that are useful and available to people everywhere. They currently have three cloud machines available, which are based on silicon nitride PIC systems that generate gaussian process sampling for near-

term applications. The advantage of silicon nitride is that the machines can operate primarily at room temperature and the system easily integrates into existing telecommunication infrastructure.

Personal health and agri-food applications are under development at OnePlanet Research Center, which was established in 2019 to initiate fundamental and applied research into applications to improve health and access to healthy and sustainable food. The centre focus on three main areas: sensing, including non-invasive, electrochemical, imaging techniques; digitizing and data analysis; and various applications as diverse as wearables, nitrogen sensor boxes and AI models. As shown in Figure 3, the photonics sensor technology is based on silicon nitride and is being developed by imec.

Health applications include devices to detect early markers in urine samples that could point to potential health issues and to provide insights into changes that occur in a certain timeframe; wearables for measuring mental well-being and stress; and digital techniques to measure how individuals absorb food and to detect problems in the gastrointestinal system.

Agri-food applications aim to use sensor and digital technology to make food production and processing more sustainable. Specifically, to enable farmers to monitor every tree, plant and animal individually so they can respond quickly and precisely at the right place and time. The aim is save time and use resources more effectively and efficiently while protecting the environment as much as possible. In

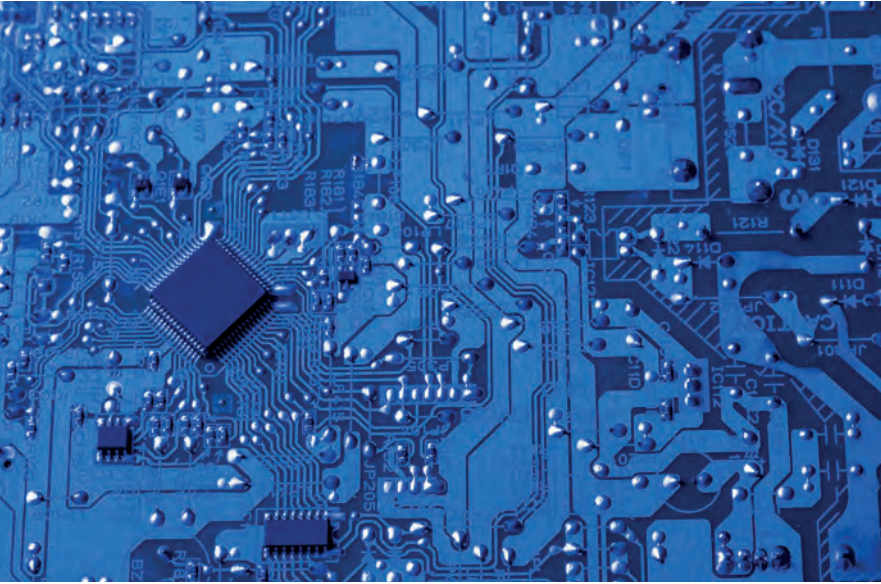
this way, it may be possible to grow crops in places where the soil is less fertile, which has in turn led to food shortages.

Related to healthcare and environmental applications, the MIRPHAB Pilot Line was launched to scale up products based on miniaturized Mid-IR spectroscopic sensors, including PICs acting as the spectrometer by using arrayed waveguide gratings (AWG). Mid-IR light in the 3- 12 μm wavelength band interacts strongly with molecular vibrations that present unique adsorption spectrums that give superior detection capabilities and unambiguous detection of chemicals in gas and liquids, enabling high sensitivity and real-time detection, qualities that present interesting applications for the development of wearables, breath analysers, point-of-care applications and detection of chemicals for industry.

Optics11 offers high-end optical sensing systems for both industrial and life science applications. Their main focus is on developing high-end tuneable laser-based fiber Bragg grating (FBG) integrators for optical sensing systems that incorporate a high-end optical acoustic emission system called Optima, which can sample up to megahertz rates. The FBG integrators have high accuracy and high precision. The Optics11 FAZ 14 series integrators can sample up to kilohertz rates. The technology also features a broad portfolio of FP and FBG based to sensors to measure strain, acceleration, temperature, and pressure. The company has experience in a wide range of applications and is currently engaged in research for the next generation of PIC based interrogators for low-



Figure3. OnePlanet Research Center focus on silicon nitride sensor technology (courtesy of OnePlanet)



cost, high volume applications, while maintaining high performance.

Optics11's technology is used in real-time structural health monitoring applications, for example, in bridges, caves and wind turbines to detect displacements and the need for repairs. Other industrial applications include acoustic emission for detecting partial discharge in high voltage applications and also road traffic monitoring, which involves installing fibre FBG arrays under the road surface to monitor the flow, speed and weight of traffic.

For life science, Optics11 technology is used in organ-on-a-chip and cell/tissue indentation applications that are able to simultaneously measure the mechanical properties of up to 92 samples of organ and tissue cells. This requires a platform and high-speed measurement system that can simultaneously integrate all the samples.

The MedPhab Pilot Line was created to ramp up the manufacture of devices for a particular application field, namely, medical diagnostics including fibre optics, microfluidics, surface functionalisation, instrumentation, opto-electronic integration, miniaturisation for micromodules and wearables applications. The MedPhab Pilot Line utilizes PIC technologies and other non-PIC advanced resources.

After designing and fabricating PICs, the next challenges include test, assembly and packaging. The PIXAPP Pilot Line provides a range of standardised photonic packaging technologies that can be scaled to high volumes; PIXAPP also provides training in optical, electrical, and mechanical packaging technologies. PIXAPP offers a menu of packaging processes in the form of building blocks to allow standardised manufacturing processes to be used across the entire supply chain for the production of PICs in the major photonic platforms (InP, SOI, SiN),

with standard designs for electro-optical I/O ports and packaging assembly steps.

Companies and organizations such as Bay Photonics, PHIX, AEMtec, AMETEK, Chip Integration Technology Center (CITC), Catapult, Cordon Electronics, Focuz, Fraunhofer IZM, Hisense Broadband, Icon Photonics, INPHOTEC Foundation, PakPIC, Photonics42, Technobis group and VTT offer services for packaging PIC modules. Micro-optics is also a fundamental aspect when talking about packaging of PICs, PHABULOUS is a Pilot Line created to help mature manufacturing processes and increase manufacturing readiness of free-form micro-optical structures and functionalities.

PIC testing is now a hot topic in the photonic scene. There are a number of challenges in PIC testing, particularly in relation to speed, dynamic range, and accuracy, and also from the instrument perspective, the requirement for integration, flexibility, and a degree of automation. EXFO, a Quebec based company, has been involved in test measurement since 1985, and in the past five years, they have developed a line of products particularly for PICs.

The testing of PIC-based passive components, i.e. those that guide light, is challenging due to the high port count of some components like arrayed waveguide grating (AWG) or the large number of components to test on a single die. For passive components, EXFO provide a CTP10 component test platform, which is a multiport detection system that works in conjunction with their T100S-HP swept tuneable laser to measure optical insertion loss, return loss and polarization-dependent loss across the telecom spectral range, facilitating integration as part of an automated PIC testing setup, increasing PIC testing throughput while reducing test time.

Conclusion

Over the next few years, the increase in demand for PIC based systems for LiDAR, personal health, agri-food, life science, structural monitoring, and industrial applications present clear opportunities for PIC-based technology reaching beyond datacom/telecom. In this article, we have looked at some of the ground-breaking PIC technologies being developed for these application fields and the corresponding supply chain providing support services for PIC design and testing.

In addition to these important contributions, EU pilot lines are making great strides in helping European SMEs develop the tools and processes to scale up the manufacture of innovative PIC-based components by providing services for chip fabrication and standardised photonic packaging technologies.

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Dr. Ana González is currently R&D Manager at EPIC (European Photonics Industry Consortium). Her role is to understand the technology developed by EPIC members and to identify potential collaboration between them. She also participates in different EC initiatives such the Pilot Lines in Photonics in which she is involved in business development and marketing strategy. Her expertise lies in the development of optical systems and the investigation of applications such as Sensing and Datacom. She received her bachelor's degree in Chemistry from the University Autonomous of Barcelona (UAB) and her PhD degree from the Catalan Institute of Nanoscience and Nanotechnology (ICN2).

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PIXAPP is the world's first open-access Photonic Integrated Circuit (PIC) Assembly and Packaging Pilot Line.

Developing multiple standardized packaging and packaging building blocks, the PIXAPP pilot line aims to help leading companies and SMEs to exploit PIC technologies for improving their current products and/or to transfer their PIC-related research(es) into PIC-based products. PIXAPP has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 731954. (www.pixapp.eu)



JePPIX Pilot Line democratizes access to industrial prototyping and pre-

production of high-performance InP photonic integrated circuits (PIC). The JePPIX Pilot Line is enabled by the InPulse project. InPulse has the ambition to transform business practices from vertical integration – where design, fabrication and product development are all in-house and inaccessible to new entrants, to horizontal where fabless and lab less businesses share the same manufacturing infrastructure. InPulse provides a low entry barrier access to low and medium production volumes of InP PICs. InPulse has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 824980. (www.inpulse.jeppix.eu)



MedPhab is Europe's first Pilot Line dedicated to manufacturing, testing, validation, and up-scaling of new photonics technologies for medical

applications ranging from diagnostics to surgical tools and therapeutics. The purpose of MedPhab pilot production line is to accelerate the commercialisation of diagnostic devices and instruments for treatment based on photonics, and to reduce the R&D costs. The chosen areas are devices intended for hospital use (assist doctors), home care devices (monitoring patient) and equipment for chemical diagnostics (based on use of serum, saliva, or urine sample). MedPhab will also

provide seamless transition from pilot line production to up-scaled production without a need for changing service providers. Use-case companies have been selected for the validation of the pilot line services covering both in-vivo and in-vitro domains. This project has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 871345. (<https://medphab.eu/>)



MIRPHAB is a Pilot Line for prototyping and production of Mid-IR chemical sensing devices able to

operate in both gas and liquid mediums. MIRPHAB provides a platform to ensure the bridging between technology and component development and the commercial availability of such component avoiding the risks associated with the introduction of new disruptive technologies. The aim of MIRPHAB is to become a commercially available prototyping line in 2020. The focus of the Pilot Line is to deploy your Mid-IR prototype swiftly in the market at a minimum of capital investment. MIRPHAB has received funding from the European Union's Horizon 2020 research and innovation programme under grant agreement No 688265. (<https://mirphab.eu/>)



PHABULOuS is to strengthen Europe's leading position as a

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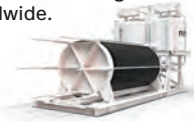
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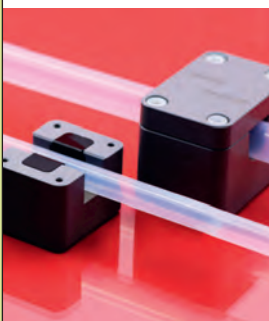


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