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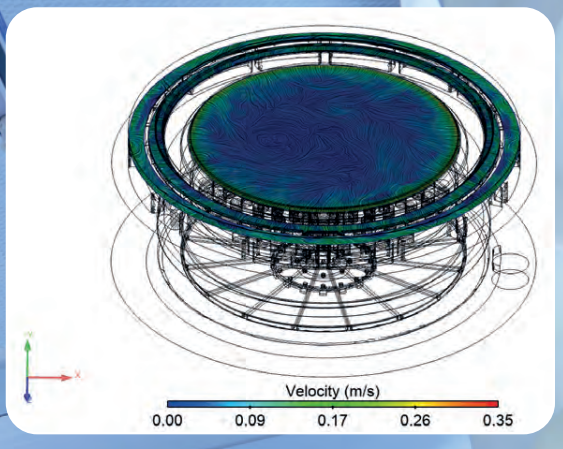

ClassOne simplifies metallization while improving On-Wafer performance

ClassOne TECHNOLOGY

VOLUME 43 ISSUE I 2022
AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION
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INSIDE

SUB-FAB SEALS AND COMPLEX CHEMISTRIES

The quest for higher performance has steadily increased the complexity of semiconductor manufacturing

UTILIZING BACKSIDE 3D SOC INTERCONNECTS

Significant performance gains are possible by utilizing new backside interconnects in 3D SOC circuits

IMPROVE DESIGN FLOW THROUGH IP MANAGEMENT

IP reuse has become a necessity since circuits and systems are almost always built on content from preceding generations

picosun SPRINTER

Perfect ALD

Fast batch manufacturing for 300 mm wafers

A REVOLUTION IN ALD MASS PRODUCTION FOR 300 MM WAFER MARKETS

The PICOSUN® Sprinter ALD system is designed to disrupt batch ALD production on 300 mm manufacturing lines in the semiconductor (emerging memory, transistor, capacitor), display, and IoT component industries. Barrier, high-*k* oxide, and conductive films are deposited in the PICOSUN® Sprinter with perfect ALD in mass production volumes.

SINGLE-WAFER FILM QUALITY SCALED TO HIGH VOLUME, WITH PERFECT ALD

Fully automated, SEMI S2/S8-certified PICOSUN® Sprinter combines the leading single-wafer film quality and uniformity with fast processing, high throughput, and uncompromising reliability.

Fast process times make Sprinter's thermal budget lower than typical vertical furnace reactors commonly used in batch ALD manufacturing. Fully laminar precursor flows in the reaction chamber guarantee perfect ALD deposition without unwanted CVD growth, minimizing the need for system maintenance.

Sprinter operates fully automated with Picosun's own, proprietary, SEMI-compliant PicoOS™ operating system and process control software. PicoOS™ combines individual ALD process module, wafer handling and transfer system, and instrumentation control under one common HMI for easy, intuitive and user-friendly operating of the whole Sprinter cluster.

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VIEWPOINT

By Mark Andrews Technical Editor

Strong 2021 semiconductor sales set pace for 2022 growth

Looking back at 2021 we see a year that underscored the vital role semiconductor manufacturing plays in geopolitics and a universe of end-use products. In a January report, IC Insights said 2021 chip sales grew 25 percent; researchers forecast sales in 2022 will likely drop to a 'meager' 11 percent, which would have been considered 'outstanding' five years ago.

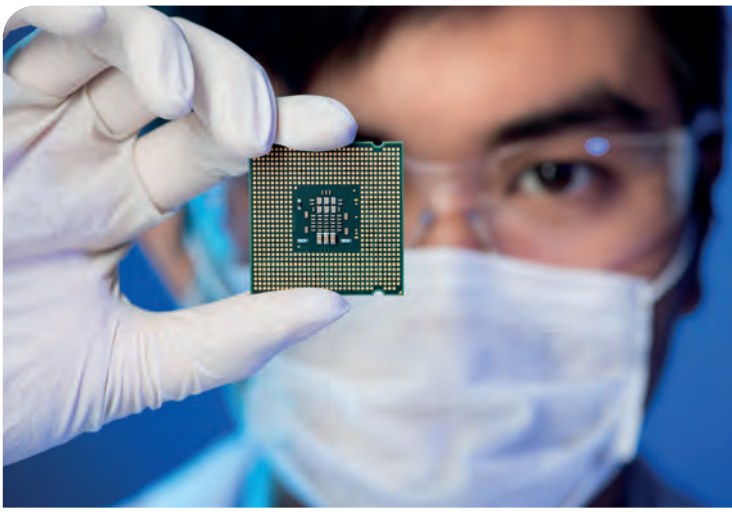
How is 2022 progressing? The Semiconductor Industry Association (SIA) reported in March that global IC sales increased 26.8 percent year-on-year this January, the second highest first quarter start in history.

While the global supply chain is still a tangled mess, there are signs that a gradual return to normal is unfolding. But as we have seen since 2020, what is predicted one month is not always realized the next.

When auto industry and consumer electronics manufacturing executives assembled in January for the JP Morgan Tech/Auto Forum, opinions about achieving a 'new normal' varied. For Nvidia Corporation, chips are still hard to find, with sales falling short largely due to unavailable key components, delivery delays and other headwinds; CFO Colette Kress said she expects constraints to ease mid-year.

Like many OEMs looking to balance demand, supply and internal post pandemic challenges, company after company has reported 2021 profits were held back by a slowly recovering global economy. Apple joined the chorus, reporting it could not realize up to $6 billion in sales thanks to component shortages.

Sales outlooks for the balance of 2022 remain positive. Although the world is anxiously watching the war in



Ukraine that began when Russia invaded, it is too soon to tell how the conflict may affect the region or Europe as a whole.

In this edition of Silicon Semiconductor we explore a unique new approach to electroplating courtesy of ClassOne Technology. The company's new Solstice GoldPro system can dramatically simplify metallization, benefitting manufacturers pursuing a 'More than More' strategy for enhancing performance.

We also look at major industrial trends that characterized 2021; the latest in technology for ensuring the integrity of vacuum and abatement seals from Greene Tweed; research updates from imec and tactics for managing IP resources by Perforce Software.

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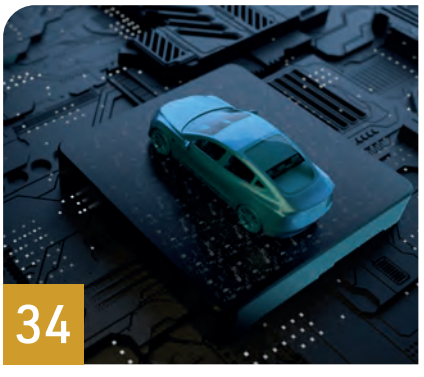

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Surging automotive semiconductor industry to grow

THE AUTOMOTIVE SEMICONDUCTOR industry is set to surge at a compound annual growth rate (CAGR) of 12.3% through 2025 on the heels of a strong comeback from the pandemic, according to a new report from Omdia.

Semiconductor content in automobiles has been increasing steadily for the past decade, but several recent trendlines have combined to accelerate automotive semiconductor revenues, Omdia notes in its new report Automotive Semiconductor Market Tracker – 2H21 Analysis. Those trends include rising sales of battery electric vehicles (BEVs) and growing demand for advanced driver assist systems (ADAS) and infotainment & telematics (I&T) systems, according to Sang Oh, Senior Research Analyst for automotive semiconductors at Omdia and author of the market tracker report.

"The average BEV creates 2.9 times more semiconductor revenue than a vehicle with a traditional internal combustion engine," Oh said. "In addition, ADAS applications like camera modules for park assistance and collision warning, plus I&T applications like the transition from analog or hybrid instrument clusters to digital clusters, are also driving increased semiconductor content."

Bouncing back from pandemic

COVID-19 dealt a significant blow to the global automotive semiconductor industry in the first half of 2020 as global vehicle production ground to a halt during the early days of the pandemic. But the industry posted a strong rebound beginning in 3Q20.

The sector's recovery accelerated in 2021, with total annual revenues hitting a projected $51.6 billion, up 28.6% from the prior year.

This came at a time when the automotive supply chain overall continued to experience disruption, and global vehicle production grew a relatively small 2.5% in 2021 against the prior year.

"The much stronger recovery in the automotive semiconductor market than we see in the industry as a whole can be attributed to the dramatic increase in average selling prices for auto semis as supplies became constrained, as well as the trend for electronics manufacturers to pre-order and increase their inventories and safety stocks," explained Oh.

The Automotive Semiconductor Market Tracker summarizes the auto semis industry and provides information to help industry players better understand and forecast upcoming trends.

The report covers 30 separate semiconductor device types used across more than 49 different primary vehicle electronic applications. The tracker is built using vehicle production and electronic module fitment projections.

Lam Research introduces suite of selective etch tools

LAM RESEARCH has announced a new suite of selective etch products that apply breakthrough wafer fabrication techniques and novel chemistries to support chipmakers in the development of gate-all-around (GAA) transistor structures. Composed of three new products – Argos®, Prevos™ and Selis® – Lam's selective etch portfolio provides a powerful advantage in the design and manufacture of advanced logic and memory semiconductor solutions.

As modern technologies and devices continue to evolve, the need for greater device density for improved performance and efficiency increases. To keep pace with Moore's Law, chipmakers are now developing transistor structures vertically – an exceptionally complex process that requires ultra-high selectivity, precision etching and uniform isotropic removal of material without modifying or causing damage to other critical material layers.

Lam's selective etch solutions provide the ultra-high, tunable selectivity and damage-free material removal required to support advanced logic nanosheet or nanowire formation, enabling chipmakers to make the next evolutionary leap from planar to three-dimensional structures for DRAM as it reaches its planar scaling limit.

Developed in collaboration with the world's most innovative logic and foundry chipmakers, Lam's selective etch products are already being used in the fabs of industry leaders like Samsung Electronics to support nearly a dozen critical steps in the advanced logic wafer development process.

"The semiconductor industry is continuously driven toward more powerful and faster device capability. As the density and complexity of the devices have been increasing significantly, selective etch technology is critical to manufacturing our most advanced logic device," said Dr. Keun Hee Bai, Master of Semiconductor R&D Center at Samsung. The Lam selective etch portfolio is composed of three new tools:

- Argos, with revolutionary MARS™ (Metastable Activated Radical Source) technology, selectively modifies and decontaminates wafer surfaces. Its groundbreaking treatment and conditioning capabilities enable chipmakers to treat wafer surfaces precisely, optimizing them for peak performance.
- Prevos enables atomic layer precision, ultra-high selectivity etching for oxide, silicon, and metal by combining novel chemistries and innovative vapor technology with agile temperature control. Prevos leverages a new proprietary chemical technology solution developed by Lam; additional chemistries can be added to support chipmakers' production needs.
- Selis uniquely employs both radical and thermal etch capabilities to enable ultra-high selective etching with uniform top to bottom process control without causing damage to the wafer structure.
- Prevos and Selis can also be delivered as a single, integrated tool to provide unique multi-layer selective etching, improved queue-time control, and maximum production flexibility.

Infineon names Rutger Wijburg as new COO

Rutger Wijburg will join Infineon's management board as new chief operations officer in April 2022. He will succeed Jochen Hanebeck, who will take over from Reinhard Ploss as the new CEO, according to plan.

"We are very pleased that Rutger Wijburg, an internationally experienced industry expert with intimate knowledge of both semiconductor manufacturing and the silicon foundry world is joining the Management Board team," says Wolfgang Eder, chairman of the supervisory board of Infineon. "He will bring valuable additional perspectives to the board as the chief operations officer."

"Electrification and digitalisation are major trends of the coming decade. Infineon is investing decisively in its manufacturing capacities in order to satisfy the long-term demand for semiconductor solutions," says Jochen Hanebeck, current COO at Infineon. "Rutger Wijburg has both the knowledge and the vision to develop Infineon's operations in the years to come.."

"Based on our structural growth drivers, Infineon is ready to invest in its manufacturing capacity and to extend partnerships in order to deliver to our customers what they need, when they need it," says Rutger Wijburg. "Infineon creates a competitive advantage through quality, innovation and cost performance. It will be my priority to further expand our lead over the competition by harnessing our technological leadership, while always keeping an eye on profitable growth."

Wijburg joined Infineon in 2018. As MD of Infineon Dresden, he was responsible for the successful ramp-up of highly automated 300-millimeter production. After taking over as head of frontend in the beginning of 2021, Wijburg has focused on expanding wide bandgap capacities and was instrumental in establishing the concept of the 300-millimeter "One Virtual Fab" cluster. He has more than 30 years of international experience in the semiconductor industry.

Corning Laser Technologies announces new technology for glass wafer dicing

CORNING INCORPORATED today announced the launch of a dicing technology that will allow the company's Corning Laser Technologies (CLT) business to enter the semiconductor application space to further focus on microfabrication processes.

CLT advanced its patented nanoPerforation process and paired it with a well-established breaking technology from Dynatex International, an industry leader in mechanical breaking of crystalline wafers, to create a new glass wafer dicing technology.

The new technology will allow customers to drive lower cost through significantly higher throughput as well as achieve lower, near-zero kerf loss and high edge strength through an inherently clean process that will eliminate subsequent cleaning steps. Additionally, the glass wafer dicing technology for up to 300 mm diameter glass wafers achieves superior results on yield, enabling unprecedented die aspect ratios and a side-wall quality that meets the highest demands of the semiconductor industry. The innovation was developed for use in industries such as micro-fluidics and micro-optics. It can also be applied for meta-surfaces on glass and other glass wafer-based semiconductor applications, as well as dicing of other brittle and transparent materials.

"We are looking forward to leveraging our 20-plus years of experience in precision laser machining along with Dynatex's expertise in breaking tools and supporting equipment," said Michael Mueller, business director, Precision Glass Solutions and Corning Laser Technologies. "This novel wafer dicing method will help Corning continue to grow in the semiconductor industry and innovate to meet current and future demands."

With decreasing die sizes and increasing wafer diameters, material utilization becomes significantly more important for high-yield semiconductor applications. When comparing to a kerf-removing technology such as blade dicing (calculated with a kerf loss of 0.2 mm), CLT's new laser dicing method can increase utilization of a wafer with small dies of 5x5 mm by 8% and even smaller dies of 2x2 mm by 17%. Enabled by the near-zero kerf loss, a fully populated 300 mm diameter and 0.7 mm thick wafer can provide a wafer utilization of 96% calculated with an edge exclusion of 5 mm.

Small dies on large glass wafers require a high-quality and high-speed dicing process. With the die size of 5x5 mm, a 300 mm wafer can be fully diced in less than 10 minutes – significantly faster than classical blade dicing, which requires multiple hours to cut.

Additionally, when using Corning® HPFS® Fused Silica (HPFS), a semiconductor-ready wafer material known for its high transparency, results demonstrate the exceptional performance for chipping and edge quality. HPFS wafers allow for low chipping that is better than 50 µm with very precise edges and die corners.

Income and revenue up for Veeco

VEECO INSTRUMENTS has announced financial results for its fourth quarter and fiscal year ended December 31, 2021. Revenues were $153.0 million, compared with $138.9 million in the same period last year. GAAP net income was $8.2 million, or $0.15 per diluted share, compared with a net loss of $0.1 million, or $(0.00) per diluted share in the same period last year. Non-GAAP net income was $22.6 million, or $0.43 per diluted share, compared with $15.0 million, or $0.30 per diluted share in the same period last year.

For the full year, Veeco reports revenues of $583.3 million, compared with $454.2 million last year. GAAP net income was $26.0 million, or $0.49 per diluted share, compared with a net loss of $8.4 million, or $(0.17) per diluted share last year. Non-GAAP net income of $73.6 million, or $1.43 per diluted share, compared with $42.3 million, or $0.86 per diluted share last year.

"I am proud of our many accomplishments in 2021," commented Bill Miller, Veeco's CEO. "We successfully advanced our product innovation and penetrated new customers, enhanced our service capabilities, increased our manufacturing capacity, improved our capital structure, solidified our governance and commitment to corporate responsibility, and strengthened the Veeco United culture. In September, we announced long-term financial targets and made immediate progress toward those targets with significant revenue and EPS growth in 2021." We had solid results in the fourth quarter with revenue and EPS exceeding the midpoint of our guidance," continued Miller. "Demand in our semiconductor and compound semiconductor markets is exceptionally strong and we exited 2021 with order momentum, increased backlog and exciting opportunities that will support our growth strategy."

Veeco has given the following guidance for the first quarter 2022.

Revenue is expected in the range of $145 million to $165 million, GAAP diluted earnings per share are expected in the range of $0.15 to $0.32, and non-GAAP diluted earnings per share are expected in the range of $0.28 to $0.44. The guidance takes into account the impact of the adoption of ASU 2020-06, effective January 1, 2022.

Picosun delivers powder MEMS platform

FRAUNHOFER INSTITUTE for Silicon Technology (ISIT) has taken PICOSUN P-300B ALD system into use as their powder MEMS technology platform.

Fraunhofer ISIT PowderMEMS is a new innovative technology for creating three-dimensional microstructures from a multitude of materials on wafer level.

The technology is based on bonding together µm-sized powder particles in a cavity with Atomic Layer Deposition (ALD). It has many advantages compared to other manufacturing techniques as it allows using much lower process temperatures compared to a traditional sintering process.

The bonded porous structures are thermally and chemically resistant thus enabling their extensive post-processing in a clean room.

“The technology can be used for various applications, such as microelectronics, MEMS sensors, MEMS actuators and microfluidics.

For example, it enables the integration of porous and magnetic 3D microstructures on wafer level”, explains Dr. Björn Gojdka, Group Leader at Fraunhofer ISIT.

“We were looking for a solution for conformal high surface area coating of powder located in trenches. Picosun solution is a perfect fit for this need as we are also looking into scaling up the technology. We are especially happy about the tool’s hot wall reactor, versatile precursor sources and its easy maintenance”, states Dr. Thomas Lisec, Chief Scientist at Fraunhofer ISIT.

“We are excited over this new technology coming to life and all the opportunities it will bring. I am especially impressed by the potential applications for the Fraunhofer ISIT PowderMEMS as they are exceptionally diverse. I’m looking forward to continuing working closely with Fraunhofer ISIT on bringing the technology up to industrial production”, says Dr. Christoph Hossbach, General Manager of Picosun Europe GmbH.

Siemens joins Intel Foundry Services' EDA Alliance program

SIEMENS Digital Industries Software has announced it has become a charter member of the Intel Foundry Services (IFS) Accelerator - EDA Alliance, a program committed to establishing an ecosystem for the design and fabrication of next generation System-on-Chip (SoCs) manufactured on IFS' leading-edge process technologies.

The initiative promotes collaboration between IFS and its ecosystem partners, with a focus on reducing risk and tackling design barriers while accelerating time-to-market for mutual customers' products. IFS Accelerator - EDA Alliance partners receive early access to Intel process and packaging technologies, allowing them to co-optimize and enhance tools and flows to best realize Intel's technology capabilities.

"We are excited to announce the IFS Ecosystem Alliance as a major step forward for Intel's foundry ambitions," said Rahul Goyal, vice president and general manager for Intel Product & Design Ecosystem Enablement. "We are pleased that Siemens EDA has joined the program. The combination of Siemens' world-class EDA offerings and IFS' leading-edge process technologies will provide design teams across the industry with the solutions needed to deliver in today's competitive IC markets."

As part of the alliance, Siemens plans to collaborate closely with IFS to optimize best-in-class IC design tools, flows and methodologies for Intel's world-class processes. The initial Siemens EDA product lines certified by IFS include the industry-leading Calibre® nm platform, as well as the Analog FastSPICE (AFS) platform for leading-edge circuit verification targeting nanometer analog, radio frequency (RF), mixed-signal, memory and custom digital circuits. "With the increasing importance of semiconductors in the global economy, Intel's commitment to the foundry market through IFS is an important new source of innovative capacity for advanced products," said Joe Sawicki, executive vice president, IC-EDA for Siemens Digital Industries Software. "Siemens is proud to collaborate with IFS to help provide software solutions that are tuned to allow mutual customers to get the most out of Intel process and packaging technologies."

EV Group and Teramount collaborate

EV Group (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets, and Teramount, a supplier of scalable solutions for connecting optical fibers to silicon chips, announce a collaboration on implementing wafer-level optics to solve a major obstacle of silicon photonics, namely fiber chip packaging. The collaboration will leverage EVG's nanoimprint lithography (NIL) technology, expertise and services with Teramount's PhotonicPlug technology.

Under this collaboration, standard CMOS wafers that implement silicon photonics chips will be post processed using EVG's NIL technology to implement optical elements such as mirrors and lenses for Teramount's unique "self-aligning optics". This enables flexible beam extraction from the chips and easy connection to a large number of optical fibers. Furthermore, it enables wafer-level optical inspection capabilities for enhancing silicon photonics wafer manufacturing.

The collaboration is being carried out within EVG's NILPhotonics Competence Center at its headquarters in St. Florian, Austria. The NILPhotonics Competence Center provides an open access innovation incubator for customers and partners across the NIL supply chain to collaborate to shorten development cycles and time to market for innovative photonic devices and applications. Through the collaboration with Teramount, EVG provides process development and production services, as well as expertise in both CMOS and photonics manufacturing, thus accelerating the commercialization of Teramount's PhotonicPlug technology.

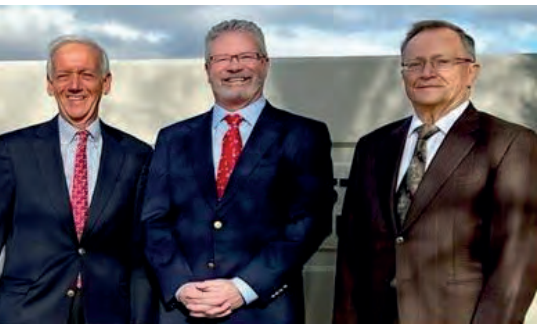
The need for high-speed data transfers in data centers, telecom networks, sensors and emerging applications in advanced computing for artificial intelligence (AI) is growing exponentially. This in turn is driving the importance of developing solutions that can cost-effectively scale up production of silicon photonics, which enable ultra-high bandwidth performance. The collaboration between EVG and Teramount aims to solve this problem.

"Our joint work with EVG has been very successful in producing this innovative synergy between wafer-level optics and silicon photonics wafer manufacturing," said Hesham Taha, CEO of Teramount. "By offering this capability to the industry, Teramount solves one of the major hurdles to further adoption of optical connectivity, which is critical for so many applications that require high-speed data transfers and low power consumption. Teramount's PhotonicPlug silicon photonics packaging technology is a truly novel approach to improving optical performance, and we are excited to be a partner in helping to bring it to the market," stated Markus Wimplinger, Corporate Technology Development and IP Director at EV Group.

Particle measuring systems celebrates 50 years

PARTICLE MEASURING SYSTEMS (PMS) has celebrated the 50th Anniversary of its inception. Started in 1972 as a cloud microphysics company, PMS has grown into a solutions and thought leader for contamination monitoring and control within clean manufacturing facilities at facilities around the globe.

PMS was founded in 1972 in Boulder, Colorado, USA by Dr. Robert G. Knollenberg who invented the laser particle counter to count and measure the sizes of particles in air. In 1978 PMS sent the first particle spectrometer into space on the Pioneer Venus Probe. In 1985 it incorporated its portfolio of particle monitors into full Facility Monitoring Systems. In 1996 PMS was acquired by Spectris, whose focus is to equip their customers with the ability to reduce time to market, improve processes, quality and yield.



Particle Measuring Systems Presidents (Lto R) Paul Kelly, John Mitchell, Dr Robert Knollenberg (founder), the late Dr Don Veal (not pictured)

PMS has since developed into the industry leader in monitoring sensitivity and is the only complete contamination monitoring solution provider. PMS delivers not only micro contamination instruments, but also expert consultants, data management software, and training and education to our global customers.

As thought leaders and industry experts, the PMS teams have trained contamination monitoring professionals around the world using their in-house “Particle College” curriculum. PMS employees are recognized as authorities in the field and are frequently asked to present at industry events and write technical papers for publications. PMS maintains an extensive knowledge center to educate and support contamination control specialists.

“It has been gratifying to see this business, that started with me designing and building instruments in my basement while juggling my full-time work in academia, grow into the industry leader for contamination monitoring in controlled environments”, said Dr. Robert Knollenberg, founder, Particle Measuring Systems. This sentiment was supported by John Mitchell, 4th President of PMS, who followed, “The key to our success is having employees who embrace our values of Aim High, Be True, and Own It. I’m immensely proud to have been part of this growth while being a company with a purpose: making the world cleaner, healthier, and more productive. I look forward to what we will accomplish for our customers, employees, and the world far into the future.”

Edwards invests in New Arizona facility

Edwards, supplier of vacuum and abatement services and solutions to the semiconductor industry, has announced its investment in a new state-of-the-art manufacturing facility in Chandler, Arizona, North America.

The new 200,000-square-foot facility will use the latest manufacturing and digital technologies to support the fast-growing North American semiconductor market with services and solutions for the efficient and environmentally sustainable production of chips.

“Unprecedented growth in the semiconductor market to meet the world’s growing consumer demand has resulted in extraordinary growth in demand for Edwards’ products and services,” said Troy Metcalf, president of Edwards Semiconductor Service. “Looking ahead, this growth is set to continue, with our customers in the USA investing billions of dollars in additional manufacturing capacity. At Edwards, we have a long tradition of supporting our customers with local service and manufacturing capabilities, and our investment in the Chandler facility continues that tradition. With the utilisation of the latest in smart manufacturing techniques and advanced automation, this new facility will be instrumental in supporting the safe, productive and environmentally sustainable manufacturing of semiconductors in North America.”

The Chandler facility will also feature warehousing facilities, factory areas, meeting rooms, and a dedicated training centre. It is anticipated that the new facility will create approximately 200 new jobs in the local area, with scope to grow along with the market.

Construction of the new site in Chandler is underway and from the third quarter of this year, the facility will commence the remanufacturing and assembly of equipment essential to meet the demand for new semiconductor fab requirements. It will use advanced automation and data solutions to disassemble, clean, inspect, repair, replace and reassemble vacuum pumps. Reduced transportation through close customer proximity, along with water recycling and the use of renewable energy will all contribute to more sustainable manufacturing operations.

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Imec, KU Leuven and PragmatIC Semiconductor demonstrate fast 8-bit flexible microprocessor

AT THE 2022 International Solid-State Circuits Conference (2022 ISSCC), imec, a research and innovation hub in nanoelectronics and digital technologies, KU Leuven, and PragmatIC Semiconductor, presented the fastest 8-bit microprocessor in 0.8 µm metal-oxide flexible technology capable of running real-time complex assembly code.

The microprocessor was implemented with a unique digital design flow that allowed the creation of a new standard cell library for metal-oxide thin-film technologies – relevant for designing a broad range of IoT applications.

The robust thin-film technology offered by imec's foundry partner PragmatIC Semiconductor was key to integrate the approximately ~16,000 metal-oxide thin-film transistors on a 24.9mm2 flexible chip.

Flexible electronics based on thin-film transistor technology is preferred over Si CMOS-based electronics for applications requiring low-cost, thin, flexible and/or conformable devices. The technology already made inroads in, e.g., health-patch sensors and RFID labels, and as a driver for flat panel displays. The missing piece is a flexible microprocessor to perform more complex signal processing calculations – as such adding compute functionality to a broad range of IoT applications.

Imec has designed a flexible 8-bit microprocessor in 0.8 µm indium-gallium-zinc-oxide (IGZO)-transistor technology, able to perform such complex computations. Kris Myny, Principal Scientist at imec:

"Our flexible microprocessor shows excellent characteristics for IoT applications, including high speed (71.4kHz max operating speed), low power consumption (11.6 mW when running at 10kHz, 134.9 mW at max operating speed), and high transistor integration density (~16,000 transistors with 0,8 µm gate length in a 24.9mm2 chip).

"Moreover, at ISSCC 2022, we will showcase real-time correct operation of our circuit by running the complex assembly code of the popular Snake game."

With the new microprocessor, imec addressed major challenges related to the design of unipolar systems. Kris Myny: "Metal-oxide thin-film transistors based on IGZO are inherently n-type.

This results in circuits with a higher (static) power consumption compared to complementary technologies. To address this, we created our own design flow starting from the open-source file of the MOS6502 microprocessor – one of the most influential microprocessors ever designed.

We engineered the number of cells and logic gates to obtain the most optimal design for our flexible6502 microprocessor in terms of area, power, and speed – using pseudo-CMOS as our logic family. This unique design flow allowed us to create a new standard cell library for metal-oxide thin-film technology that can be used to innovate applications based on metal-oxide thin-film technology. As such, this work nicely wraps up my ERC Starting Grant which aimed at opening up new horizons in the field of thin-film transistor technology."

To fabricate the flexible microprocessor, imec teamed up with foundry partner PragmatIC, whose unique FlexIC Foundry offers rapid prototyping and high-yield volume manufacturing of flexible integrated circuits. Brian Cobb, VP Product Development at PragmatIC: "Until recently, there was no mature and robust technology available for integrating such a large number of thin-film transistors with sufficient yield.

Our pioneering FlexLogIC fab now enables the rapid turnaround of such complex new designs at an ultra-low cost, delivering ICs on thin and flexible wafers. Our FlexIC Foundry service continues to be instrumental in enabling design teams like the one at imec to expand the range of design and use cases for flexible electronics."

This research was performed in the framework of the ERC starting grant FLICs under grant agreement No 716426 under the European Union's Horizon 2020 research and innovation programme.

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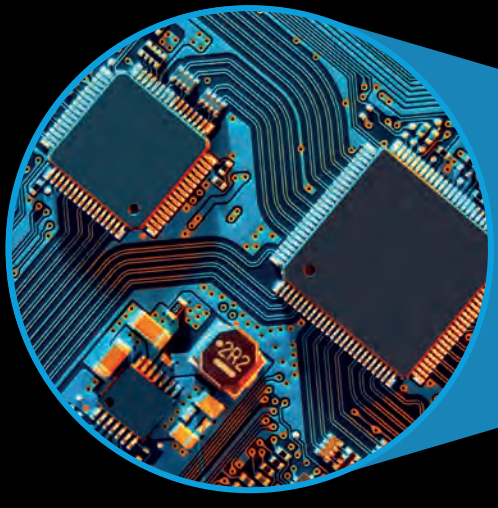

Creating and strengthening links between chipmakers and network builders

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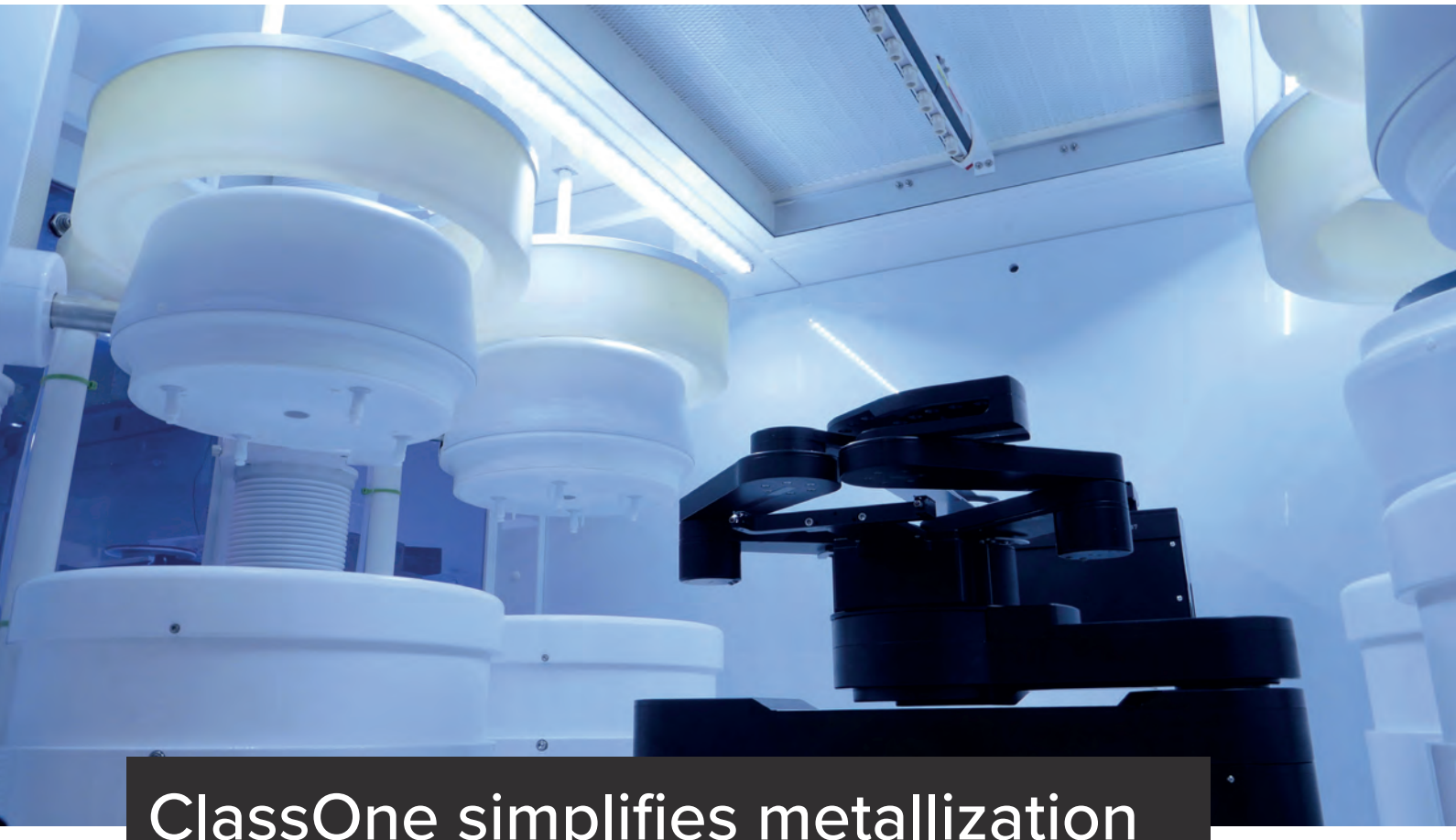


ClassOne simplifies metallization while improving On-Wafer performance

Reducing transistor size to increase performance has driven semiconductor manufacturing since Moore's Law was first articulated. Only a handful of companies still pursue this; many others look to new device types and architectures that do not depend on shrinking transistors or increasingly complex and expensive equipment. ClassOne Technology is a leader in the anti-complexity revolution that champions high performance and cost-effective throughput.

BY JOHN GHEKIERE, VICE PRESIDENT, PRODUCT AND TECHNOLOGY, AND CODY CARTER, PRODUCT ENGINEER, CLASSONE TECHNOLOGY

THE WITHERING MARCH of relentless device scaling described by Moore's Law has left a mere handful of device manufacturers in that race, with TSMC clearly in the technology lead. When the cost per transistor inflected to become more expensive with each generation, somewhere between 26 and 22 nm nodes, it drove even many of the larger and more powerful manufacturers to alternate paths of innovation and new means of bringing value; GlobalFoundries pivoted boldly into FD-SOI; STMicroelectronics into SiC. The broad expansion of new device types - in short, the ubiquitous adoption of microelectronic devices into almost every aspect of our daily lives - has brought about the More Than

Moore era, where feature scaling is no longer the sole means of device innovation.

This sea change in device innovations has essentially occurred in the wake of feature scaling, in a space of free-mindedness around device architecture and the applicability of manufacturing steps defined by that ceaseless grind. The industry, in a sense, has been able to take a breath, and we now see clearly, perhaps surprisingly, that the pace of Moore drove into unit processes and capital equipment certain complexities that may add little or no value. Whereas More Moore brought an almost exponential increase in complexity to unit processes, More Than Moore, while retaining expectations around on-wafer performance, has kicked wide the door to reducing complexity.

The shift is not only timely; it is critically necessary in very practical ways. As the global race for semiconductor leadership continues to escalate, thousands of new semiconductor jobs are being opened with thousands more to come. It is an expansion not previously seen and its impact is the rapid dilution of experience in the workforce. Now, the complexities of setting up, operating and optimizing unit process equipment becomes a costly, and for many More Than Moore manufacturers, a debilitating challenge. Device manufacturers need the same performance from their equipment, but they need it to be simpler to use.

The truth of the impacts of Moore on complexity was made clear to me, in a previous role, during a visit to a major advanced memory manufacturer to discuss process equipment technology. I had traveled to share some recent development results, aiming to place equipment within a new R&D location within the fab. The senior technology director was pressing me on a particularly nuanced capability that our competitor had and we did not. Adding the capability meant introducing a complicated mechanical system submerged in a concentrated wet chemistry. From an engineering perspective, such a system was not only expensive, but it introduced a dozen new potential failure modes. I explained to him that we had studied that function and its effects in depth and could find no indication of any kind that it provided any benefit. I asked for clarity of its on-wafer benefit. He said, “John, you don’t understand. If I can measure it, then you must control it.”

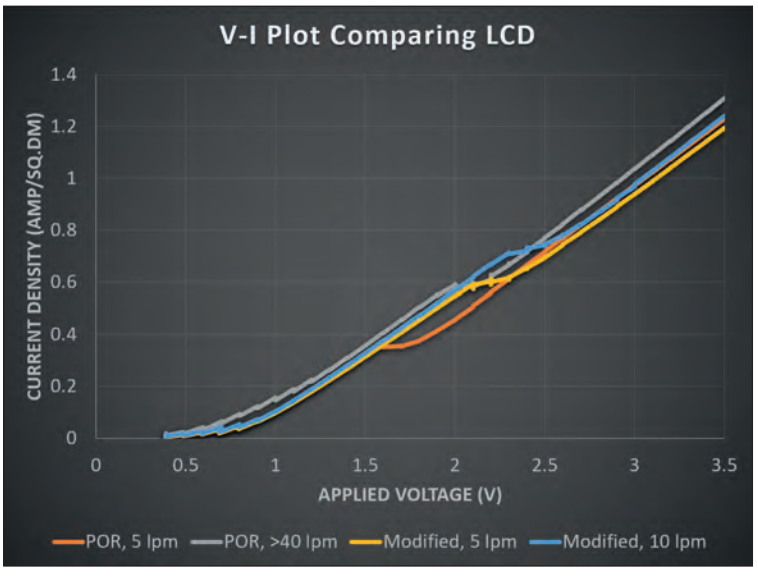
It became clear. The pace of Moore means that there is simply not sufficient time to investigate everything to complete understanding. Perception of risk is risk, thus, complexity is driven in, even if, in certain cases, that complexity serves as largely an insurance policy against factors that may or may not be important. Better to have the complexity (and cost) than the question.

The More Than Moore crowd are rising in the wake of Moore, where heightened complexity no longer offers assurances. It offers higher cost and more unwieldy process steps; and if it doesn’t bring measurable benefit, then it simply isn’t needed. The opportunities are fruitful. This article will focus on the simplification of electrochemical deposition (we’ll simply say plating), which when compared to the entirety of semiconductor unit processes, already lies somewhere in the middle in terms of complexity. Plating is also broadly and deeply captured by a great host of patents. As a basic technology, plating is already more than 200 years old; yet, as we will show, even its fundamentals are ripe for innovations that simplify operation while not only maintaining on-wafer performance, but improving it.

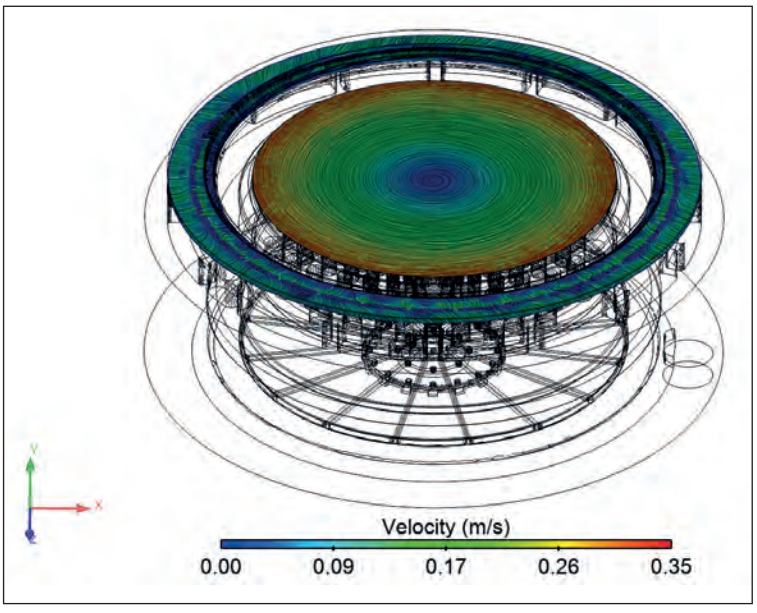
Plating remains an enabling, cost effective and highly-flexible option for metallization. The means of producing high quality plating and excellent on-wafer results are well established. The principles behind great performance are no longer the domain of one or two providers.

Uniform deposition by plating requires careful sculpting of two key factors: the electric field profile and the fluid motion profile.

As it turns out, the electric field is actually the easier of the two to perfect. Computational Fluid Dynamic modeling (CFD) provides an exceptionally accurate and predictive model around the electric field and its ultimate effects on on-wafer performance, namely film deposition rate. The need here is to deliver a zero-gradient potential at the wafer surface. The electric field wants to be zero-gradient so this aspect of reactor engineering has a lot to do with developing hardware that “stays out of the way.” In terms of the actual state of reactor hardware in the industry, however, the scaling race resulted in over-engineering of plating chambers for most More Than Moore applications and, arguably, many



➤ Figure 1: V-I plot comparing LCD of POR condition against modified condition



➤ Figure 2: CFD image of electrolyte at wafer surface

applications at >32nm node.

Anode elevators, mechanically actuated irises and multiple independently controlled anodes provide very clever and interesting control knobs (as an engineer who worked extensively with such systems, I also found them extremely fun to play with). But these features add complexity and hardware costs that provide little to no benefit except in the most extreme use cases. For example, multiple independently controlled anodes do allow for radial tuning of the electric field. But so do physical diffusers made of natural polypropylene. The difference is not in the ability to deposit uniformly - both do. The difference lies in the need (or lack thereof) to adjust dynamically insitu.

Electric field dynamic tuning is very cool. But patently unnecessary for seed thickness above about 100A. A careful reader of this article will note that a uniform potential at the wafer surface does not necessarily mean a uniform current density across that surface. However, looking more closely at the reality of the situation, we find that until scaling drives a sufficiently thin seed material, one that results in a significant potential gradient across the wafer itself, a uniform potential does result in a uniform current density. The multiple independent anodes, as well as mechanically actuated irises, really only find their use in the dynamic condition where a very thin and resistive seed rapidly, typical of the most advanced logic and memory devices, thickens with plating, changing the curve to a flat one. The vast majority of MtM applications, as well as damascene applications at 32nm and above, are applied to wafers with a flat potential profile. It's notable, if you believe the patent landscape, that only one major plating manufacturer engineered multiple anodes into its system, and more notably that the provider with the larger market share was not that one.

So we see that shaping the electric field is readily done and without complexities that bring challenging setup procedures as well as expanding modes of potential failure.

The more challenging factor is the fluid motion profile. The fluid motion profile relates entirely to cation availability. Plating processes result in beautiful, shiny high purity metal films in large part because those processes are run in an "electron-poor" regime. This regime is crippled when the concentration of target cations available at the surface of the wafer is drawn down to become similar to the "concentration" of electrons. In such areas on the wafer where this depletion occurs, the resistance rises, and since the plating system is driving a potential while tuning by an ammeter, the localized current density is lowered and plating slows locally.

The key to ensuring abundant cation supply is to make uniform the time required, at each location, for the target cation to cross the diffusion layer. This can be done by simply slowing the process. But, as a rule, device manufacturers do not like to slow down processes. Again, the inherently risk-averse drive of Moore resulted in a large number of complexities aimed to eliminate questions of cation availability with brute force as opposed to system efficiency.

There is an interesting difference between e-field and fluid motion profile in that the e-field reaches the wafer and "sinks in". The fluid motion profile, by contrast, has to get out of its own way. The fluid that reaches the wafer must turn and go away from the wafer, and it must move past other fluid in order to do so. The challenge here, in terms of supporting the highest possible plating rates, is to sculpt the fluid motion profile in such a way that no bias of motion is produced. A bias in fluid motion vector creates localized and stable differences in diffusion layer thickness, which translate to slightly different times for cations to diffuse. As the current density is increased in order to drive the fastest possible process, so is the consumption of those precious cations.

The limitation is reached wherever that supply becomes sparse and starts to impose higher potential, thus lower current density, thus slower localized plating, and an impact to uniformity.
The most prevalent solution to combat this in the industry has been the inclusion of a submerged paddle. While simple in concept, paddles do add to complexity of a chamber. They introduce more moving parts and therefore things that require setup and which have certain modes of failure. They also, obviously, add to the cost of building the reactor, both in terms of materials, machining steps and labor of assembly. In cases where a technician needs to access the interior of the chamber, for whatever reason, there is now the need to get the paddle out of the way of hands and tools. In short, chambers must be disassembled for even relatively

minor maintenance tasks.

Interestingly, as noted earlier in this article, whereas we said that forming the profile of the electric field was easy and amounted to setting it up and then staying out of the way, with paddles, there is something literally placed in its way.

In actuality, the electric field is not manipulated by the motion of the electrolyte. But it is manipulated by the hardware that produces the motion of the electrolyte. Put another way, one can independently model the electric field and the fluid motion profile. And the results of the models accurately predict on-wafer behavior. The two factors really do function independently from one another. This means, in theory, it should be possible to tune them separately. And yet, reactor designs historically bind the two together. After all, the fluid passes through and across the same hardware that the electric field does. The result has been the proliferation of highly complicated reactors driven by the dual constraint of field sculpting and fluid motion formation. Theoretically then, if one can fully segregate optimization of the electric field from optimization of the fluid motion profile, then both can be tuned to best possible state without "getting in the way". And this, it turns out, can be done with a reduction in complexity as opposed to an increase.

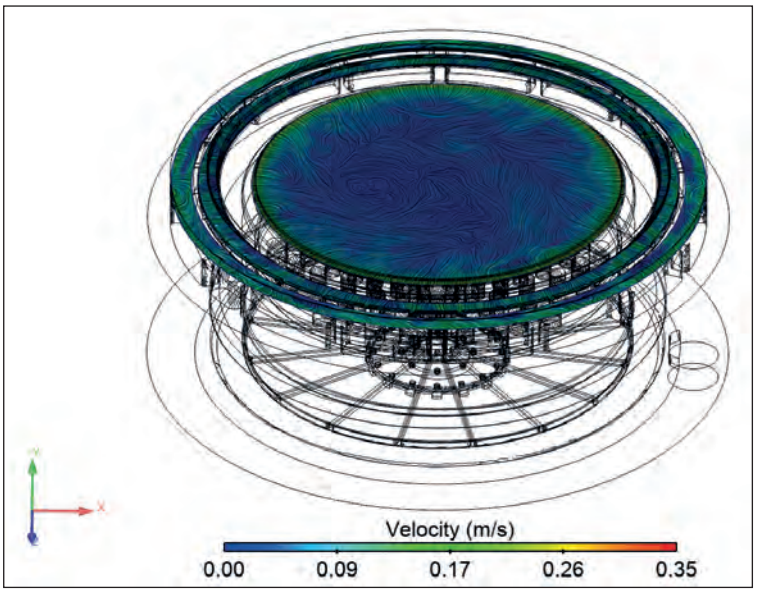
The thickness of the diffusion layer cannot be directly measured of course. But a very descriptive proxy is available by use of an V-I graph, which plots voltage as an input and current as the output. Ohm's Law of course states that, for an electrical circuit with a given resistance, current rises linearly with voltage. This is true of electrochemical systems as well, yet with one notable influence. Electrochemical cells involve electrochemical reactions, meaning the electrons are "consumed" in the formation of reaction products, namely deposited metal. When cations begin to become scarce, the resistance of the system begins to rise and the curve starts to flatten out, as shown in Figure 1. This flat region is called the Limiting Current Density (LCD) and it serves as a practical limitation to how fast one can drive a plating system. Approaching this region leads to poor uniformity and ultimately poor deposition.

The LCD of a given system thus serves as a means to compare cation availability between systems. If a modification of a given system results in the LCD being moved to a higher potential, that means the supply of cations has been improved. It further means that the system can be run at a higher current density while still depositing high-quality films.

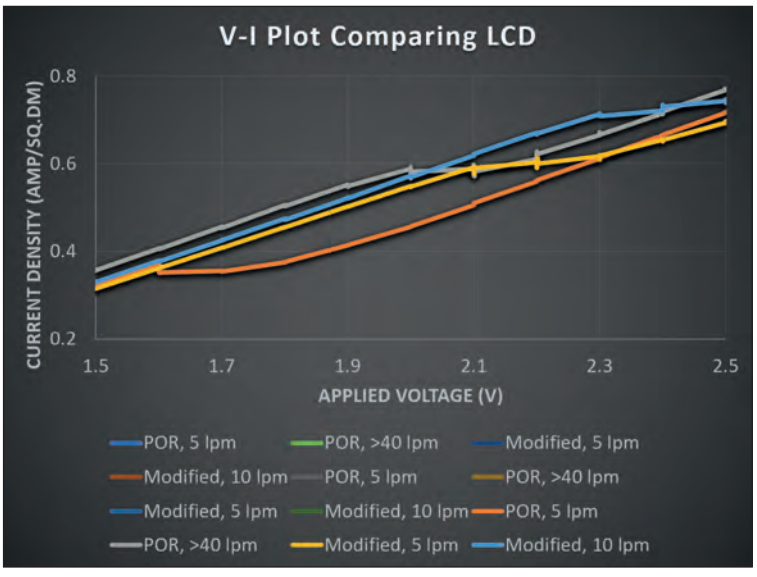
ClassOne Technology, with MtM manufacturers as its target customer base, has adhered since inception to a design ethic whereby no complexity is added to its Solstice plating system unless actual value is realized. And even having started from this mission of design elegance, continues to uncover new means of advancing on-wafer results while maintaining or even reducing complexity.
In revisiting the principles summarized above, we understood that our paddle-free GoldPro reactor, which already competes with all major plating systems globally for on-wafer performance and feature uniformity, could be improved further in terms of the simplicity in delivering perfectly uniform features across the entire wafer.

Typical adjustments that raise LCD include increasing agitation or increasing temperature. Typically, increasing electrolyte temperature causes certain undesirable side effects and is not a practical option. This leaves agitation and also explains the reason that paddles have been so prevalent in reactor design. Other means of enhancing agitation involve higher wafer rotation rates and higher fluid flow rates. Wafer rotation rate is constrained by two factors: one, it produces radial effects in terms of localized variations in cation availability, thus there is going to be an optimal rotational speed above which uniformity becomes worse again. Secondly, a too-high wafer rotation can establish stable and directional fluid motion, i.e. bias, that results in localized non-uniform plating and lopsided features. Thus wafer rotation rate is not really a viable process knob for substantially increased plating rates.

Sheer fluid flow rate is viable as a process parameter though it bears practical limitations related to pump size as well as fluid evacuation (remember, the fluid has to get out of its own way). If the aim is simplification, which it is, then inclusion of a paddle is not taking things the preferred direction. All of this apparently leaving few options for raising LCD and making room for higher plating rates. ClassOne, through a focused effort aided by CFD modeling, investigated certain passive means of fluid manipulation within its reactor, aimed at producing ample fluid motion in a non-directional



➤ Figure 3: CFD image of electrolyte <1mm from wafer surface showing randomized motion



➤ Figure 4: V-I plot zoomed in to highlight increase in LCD using modified condition

manner. Considered more closely, our aim was to transform the observed motion of fluid from the circular motion of liquid attached to the spinning wafer to a random pattern, and to do so as close to the wafer as possible. CFD modeling of various reactor concepts directed the design team to a specific concept that manipulates fluid motion in a passive way (i.e. no paddles or moving parts).

As the model shows, the electrolyte at the wafer surface (d=0) is clearly attached and moving rotationally with the wafer. Yet at a distance much less than a millimeter, the fluid motion is already largely random, leaving no effective bias. (See Fig 2 and 3) Further, the concept increases cation availability, as evidenced by a significant shift upward of the LCD. The LCD is found by initiating a plating sequence in voltage control mode and then periodically raising the voltage setting while recording the current that results.

Using this method, the LCD was found for POR condition which uses a flow rate of >40 lpm. Combined with a specific wafer rotation rate, this POR produces cross-wafer uniformity in gold of <2.5% 3-sigma and a feature uniformity of <1% (max-min / max+min). We then used the same method to find LCD at lower flow rates, including as low as 5 lpm through the system. The lower flow rate on the standard system produces a very low LCD, so low as to be debilitating. In short, this is a process of very low productivity.

Next, by implementing some targeted changes to fluid motion through the reactor, still employing a passive system, we determined that the LCD at 5 lpm flow rate, could be raised again to the level of LCD for the POR at >40 lpm. The conclusion is that, with the targeted modifications to the reactor, we are able to maintain very high cation availability at the wafer surface while decreasing the flow rate by more than 87%! This opens the process window significantly without high flow rates. As a last confirmation of the new approach, we then increased flow to 10 lpm (still a quite low flow rate) and we see that the LCD is actually improved to a value higher than the original POR. (See Figure 4) The conclusion is that greater performance is achieved using a simpler process.

The specifics of this design, while they cannot be disclosed in this publication, also ensure that the manipulation of the fluid motion profile does not interfere at all with the formation and shaping of the electric field. The chamber stays out of its own way. Taking altogether, we confirmed that exceptionally high cation availability is possible at significantly low flow rate using a passive means of fluid motion control, i.e. no paddle or other submerged moving parts. Further, we demonstrated we were able to achieve this profile without interference to the electric field distribution.

The work shows that there is ample room, particularly among More Than Moore device manufacturers, to not only maintain competitive on-wafer performance, but to improve on it, while simultaneously eliminating complexities in the process system. This results in lower costs on equipment, lower costs on maintenance, and a far simpler system to operate at a time when the industry is experiencing rapid dilution of experienced workforce.

And this is just the beginning.

For additional information, please visit: https://classone.com/reactor-and-platform-innovations-advancing-our-plating-technology/#GoldPro

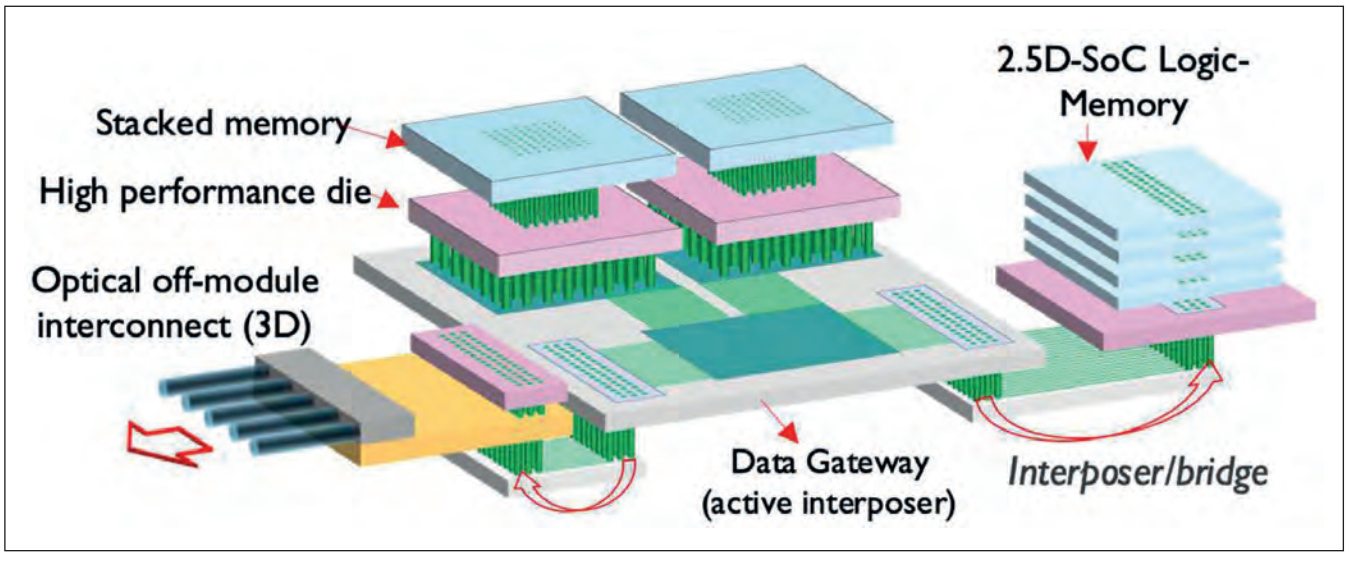
Imec demonstrates significant performance gains utilizing backside 3D SOC interconnects

Principal researchers at imec, working with Cadence EDA programmers, have demonstrated significant performance gains are possible by utilizing new backside interconnects in 3D SOC circuits.

BY DRAGOMIR MILOJEVIC, GEERT VAN DER PLAS AND ERIC BEYNE, IMEC

IMEC RESEARCHERS Dragomir Milojevic, Geert Van der Plas and Eric Beyne delve into highlights of their work to improve SOC performance through a novel approach utilizing backside interconnects. According to imec, researchers have shown the following key results with the promising approaches studied so far:

- 3D system-on-chip (3D SOC), enabled by electronic design automation (EDA) and 3D process technologies, is an attractive heterogeneous integration approach for addressing the memory wall in high-performance systems.
- Further performance gains at the system level can be achieved when the backside of one of the integrated wafers is exploited for either power delivery, signal routing or both.
- The benefits of 3D-SOC design and of backside interconnects in specific circuits are highlighted in two papers presented at the 2021 IEEE International Electron Devices Meeting (IEDM).



➤ Figure 1: Abstracted view of a possible future high-performance system. High-performance die with 3D-SOC stacked memory are implemented on an active interposer chip which acts as a data gateway and connects in a '2.5' fashion with local high bandwidth memories and optical transceiver modules (as presented at 2021 IEDM).

Promises of a 3D-SOC design approach

Data-intensive high-performance systems intended for advanced computation, data server or deep-learning applications increasingly suffer from the so-called 'memory wall' – the challenge of accessing data quickly enough. An interesting approach to tear down this memory wall is 3D system-on-chip (3D SOC) integration. Following this heterogeneous integration approach, the system is automatically partitioned into separate chips that are concurrently designed and interconnected in the third dimension.

In their invited 2021 IEDM paper '3D-SOC integration, beyond 2.5D chiplets', the authors explain how this 3D-SOC concept goes beyond today's popular chiplet approaches for realizing multi-chip heterogeneous system integration. Eric Beyne, senior fellow, VP R&D and program director 3D system integration at imec said, "Chiplets involve separately designed and processed chiplet dies.

A well-known example are high-bandwidth memories (HBMs) – stacks of dynamic random access memory (DRAM) chips. This memory stack connects to a processor chip through interface buses, which limit their use to latency-tolerant applications. As such, the chiplet concept will never allow for fast access between logic and fast, first and intermediate level cache memories."

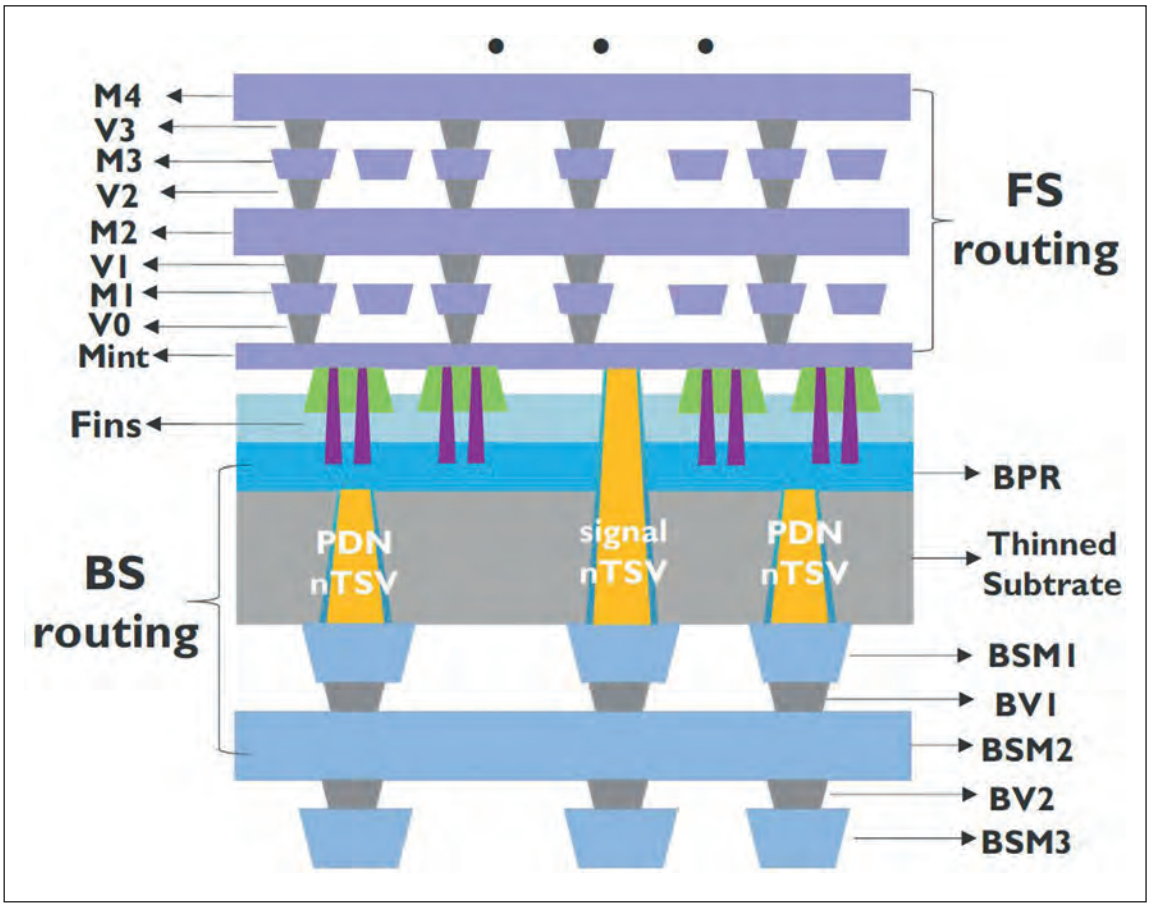
With 3D-SOC integration, memory-logic partitions can be realized using direct and shorter interconnects - resulting in significant performance improvements. In their invited paper, the authors showed an optimized implementation of a 3D-SOC design with memory macros in the top die and remaining logic in the bottom die – resulting in a 40 percent higher operating frequency compared to a 2D design.

The authors also discuss the key challenges of realizing fully functional 3D SOCs. Dragomir Milojevic, principal scientist at imec and professor at Université libre de Bruxelles remarked, "On the design side, a 3D-SOC co-design strategy is needed for both logic and memory partitions. This requires dedicated electronic design automation (EDA) tools that can handle both designs simultaneously, using automated tools for system partitioning and 3D critical path optimization during place-and-route. Through our collaboration with Cadence, we have access to these highly advanced tools." On the technology side, progress in wafer-to-wafer hybrid bonding solutions will allow for very high chip-to-chip interconnect densities, mandatory for partitioning of first and intermediate level cache memories.

The next step: exploiting the wafer's backside

A possible partitioning of high-performance 3D-SOC systems involves some or all memory

➤ Figure 2: Wafer-to-wafer hybrid bonding at 700nm pitch (as presented at 2021 IEDM).



➤ Figure 3: Schematic of conventional frontside (FS) BEOL and backside (BS) metals for PDN and signal routing. The BS metals for PDN routing use nTSVs to connect BS metals to buried power rail while BS metals for signal routing use nTSVs to connect BS metals to FS metals (as presented at 2021 IEDM).

Dragomir Milojevic

Geert Van der Plas

Eric Beyne

macros to be placed in the top die, while the logic is placed in the bottom die. On the technology side, this can be realized by bonding the active frontside of the 'logic wafer' to the active frontside of the 'memory wafer' by using a low-temperature wafer-to-wafer bonding technique. In this configuration, the original backsides of both wafers now reside on the outside of the 3D-SOC system.

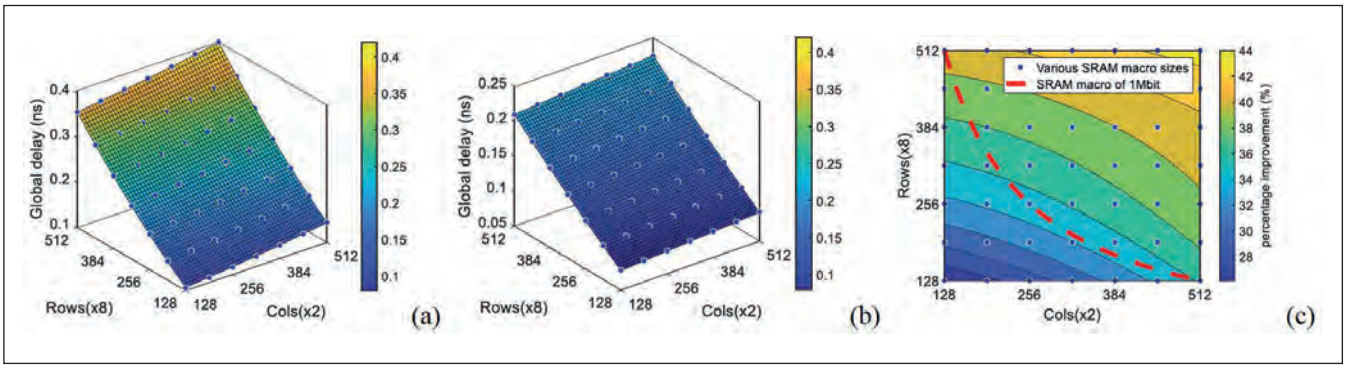
Eric Beyne said, "We can now think of exploiting the 'free' backside of these wafers for signal routing or for directly powering the transistors in the 'logic wafer'. Traditionally, signal routing and power delivery happens in the wafer's frontside, where they compete for space in a complex scheme of back-end-of-line interconnects. In these designs, the wafer's backside only serves as a carrier.

In 2019, simulations by Arm for the first time showed the beneficial impact of using a backside power delivery network (BSPDN) in the design of a central processing unit (CPU) that implemented a 3nm process as developed by imec. In this design, the interconnect metals residing in the wafer's thinned backside connected to 3nm transistors in the wafer's frontside using through-silicon vias (TSVs) landing on buried power rails. Simulations revealed that this BSPDN was seven times more efficient than the traditional frontside PDN."
Additional performance gains can therefore be expected when BSPDNs are implemented to supply the power-hungry core logic circuits that reside in the bottom of a 'memory-on-logic' 3D-SOC. One could also think of alternative 3D-SOC partitions where part of the memory tiles (e.g. the L1-level caches static random access memory (SRAM)) reside in the bottom die as well, also powered from the backside.

Besides extending the possibilities for 3D-SOC designs, BSPDNs have also been proposed for monolithic single-chip logic and SRAM systems-on-chip (SOC), where they can assist further device and IC scaling. Geert Van der Plas, program manager at imec said, "Moving the power delivery network to the chip's backside has proven an interesting approach to address the back-end-of-line (BEOL) routing congestion challenge and reduce the IR-drop. A main difference with the 3D-SOC approach is that a dummy wafer is now bonded to the target wafer to allow for backside wafer thinning and metallization." One of imec's partners recently announced to implement such a BSPDN concept in one of its future node chips.

Backside interconnects to further improve SRAM macro and logic performance

While the benefits of a BSPDN could already be demonstrated in specific designs, additional gains can be expected from using the wafer's backside for global signal routing. Imec, in collaboration with Cadence, has for the first time assessed and optimized SRAM macro and logic circuit designs that



➤ Figure 4: Global routing delay (read access) of SRAM macro at various macro rows and columns. (a) FS; (b) BS and (c) from FS to BS improvement. The macro size ranges from 128*128*16=256kbit to 515*512*16=4Mbit (as presented at 2021 IEDM).

are partly routed from the backside. An SRAM macro not only involves the memory bit cell arrays but also the peripheral circuitry (like address decoders, control block, etc.) that are relevant for processor design.

For both SRAM macro and logic, up to three backside metal layers were used for signal routing, while nano-TSVs (nTSVs) connect the backside metallization to the frontside. The SRAM macros implemented 2nm nanosheet transistors in their design. In these macros, only the global routings for the peripheral circuit were designed with backside metallization.

For logic, a ring oscillator framework was used to assess the impact of backside signal routing. The design implemented forksheets of the 2nm technology node in the logic standard cells. A physical implementation of a 64-bit ARMTM CPU using the same 2nm forksheet process design kit (PDK) is used to ensure the meaningfulness of the ring oscillator simulation results.

Geert Van der Plas said, "Compared to frontside routing, backside routing turned out significantly more beneficial in improving delay and power efficiency for long interconnect signal routing. For the SRAM macros, we demonstrated up to 44 percent performance improvement and up to 30 percent power efficiency improvement compared to frontside routing. For logic cells, backside routing enabled 2.5x speed improvement and 60 percent energy efficiency increase." The results are described in the 2021 IEDM paper 'Design and optimization of SRAM macro and logic using backside interconnects at 2nm node' by R. Chen et al.

Assessment of the circuits' performance and power efficiency was enabled through a combination of experiments and modelling. Dragomir Milojevic explained the process: "Experiments involved an optimization of nTSV processing in terms of capacitance and resistance to ensure a good electrical connection between the frontside and the backside metals. These parameters were fed into a model, used to perform the simulations.

Finally, our team performed a design-technology co-optimization (DTCO)-driven routing optimization which showed a path for further improvements. We demonstrated an additional 20 percent performance improvement by reducing the capacitance of the backside metals."

Conclusion

The heterogeneous 3D-SOC approach – enabled by system architecture re-design and 3D integration technologies – has proven an attractive way of improving system performance. Additional performance gains can be achieved by exploiting the backside of the bottom wafer for power delivery and/or signal routing. Imec has for the first time shown the beneficial impact of using backside interconnects in SRAM macros and logic circuits. These backside interconnects can bring performance improvements for high-performance 3D-SOCs as well as for monolithic single-chip SOCs.

FURTHER READING

- 'Imec demonstrates critical building blocks for a backside power delivery network', imec reading room;
- 'Cadence accelerates system innovation with breakthrough integrity 3D-IC platform', press release;
- 'Next-gen chips will be powered from below', IEEE Spectrum, August 2021.

More details can be found in the 2021 IEDM papers:

- '3D SOC integration, beyond 2.5D chiplets', invited paper by Eric Beyne et al.
- 'Design and optimization of SRAM macro and logic using backside interconnects at 2nm node' by R. Chen et al.

Top semiconductor manufacturers improve design flow through IP management

Intellectual property (IP) is used and reused as semiconductor designs evolve from one generation to the next. IP reuse has become a necessity since complex circuits and systems are almost always built on content from preceding generations. IP management tools are the most efficient way to track origins and changes, which translates into far less time spent researching IP. Perforce Software explains how IP management tools are already shortening design cycles while helping ensure security.

BY SIMON BUTLER, GENERAL MANAGER, METHODICS BUSINESS UNIT, PERFORCE SOFTWARE

AS IS SEEN EACH DAY, the semiconductor industry is going through a period of rapid evolution, with growing demand being counter-balanced by some considerable challenges. At the end of 2021, Perforce Software asked close to 100 industry professionals worldwide about current concerns, working methodologies, and emerging trends around design and development. While Perforce does not claim this to be an exhaustive list, the results provide valuable insight into some of the main factors shaping semiconductor design and development right now.

The largest categories of respondents were engineering management and design engineering (approximately a third each), followed by CAD management, executive management, and others. Company size ranged from under $500 million annual revenue to over $5 billion. While these organizations do vary, there are some strong areas of commonality.

The biggest industry issues

When asked about design imperatives, responding organizations' two most important issues were time-to-market (55%) and IP reuse (45%). These point out that semiconductors are becoming commoditized, with fierce competition and slim margins in most categories. Keep in mind that even when considering more expensive application specific integrated circuits (ASICs), these designs almost always reuse at least some IP just like their commoditized cousins. Reusing some components from of a previous design — also known as IP reuse — has become a priority for many.

Respondents said the following two issues were highly important after market timing and IP reuse:

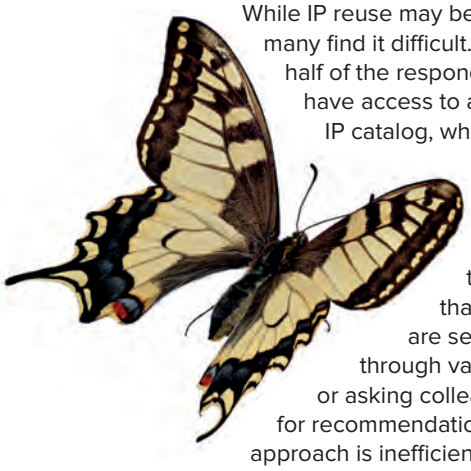
functional safety (35%) and IP security (23%). In a sense this comes as no surprise, given that chips are often used in safety-critical, sensitive or highly regulated environments. Over 70% of respondents are required to meet compliance or functional safety standards, such as ISO 26262, ITAR and others, yet 70% are still using manual processes for compliance management. This may be fine for smaller teams, but this can become untenable as organizations scale. However, almost half of respondents also have some element of automated compliance management, even if it is not being used for everything.

A majority of the survey's global respondents (76%) were also concerned about the drop in the US share of global manufacturing capacity. The hope is that the US government's efforts to find new ways to drive more in-country manufacturing and gain more control over the semiconductor supply chain will work.

Key trends

Nearly two-thirds of respondents develop embedded software as part of their product portfolios, reflecting that the global embedded system market is predicted to grow 6.3% to $137.31 billion by 2027, according to a report published by Fior Markets[1]. Bundling hardware and software together creates new challenges; designs become more complex, creating a greater need for developers and designers to collaborate and manage design lifecycles in a coherent, unified way. Perforce also asked about analog designs for SoCs, and almost half stated that there is 40% or more custom-IC design on a die in a typical chip in their organizations. In addition, 76% of respondents said that more than half of their jobs requires IP integration. The survey also found that 2.5D (interposer) designs are being considered or implemented by 36%. While that number may sound low, it does indicate that 2.5D is no longer being used only for expensive, high-end chips. Importantly, usage is trending upwards.

IP reuse and management are hard



While IP reuse may be a priority, many find it difficult. More than half of the respondees do not have access to a centralized IP catalog, which inhibits the design reuse discovery process. In practice, this means that people are searching through various projects or asking colleagues for recommendations. This approach is inefficient: nearly 40% report that discovering candidate IP for their designs is time-consuming and burdensome.

Furthermore, for more than a third reported that trying to determine the status of IPs after making an initial discovery is a challenge, and nearly 75% reported difficulty in determining the context of an IP and its quality.

Clearly, with IP-centric design and IP reuse continuing to grow, these issues need to be addressed. Understanding the context of IPs for reuse has historically required advocates from the original project. Having a better process for identifying IP for inclusion in a project helps companies make better use of their existing assets and avoid reinventing the wheel for each new project.

Bundling hardware and software together creates new challenges; designs become more complex, creating a greater need for developers and designers to collaborate and manage design lifecycles in a coherent, unified way

Software tools can assist with these and other challenges. Perforce asked industry professionals what they were using. Over half are not using commercial IP management tools: 30% use manual tools such as Microsoft Excel, and 22% are not using any tools at all. This demonstrates that while most companies have embraced IP-centric design practices, using dedicated IP lifecycle management tools is still in its relative infancy.

However, 83% use version control software, which enables configuration management at the file level. This is a prerequisite for traceability but does not provide the necessary IP level context for component-based traceability. Component-based bills of materials (BoMs) and lifecycle management tools facilitate version control of the IP hierarchy at the individual component and system level, with dependent properties memorialized on the IP versions in the hierarchy. This allows a much richer meta-model for tracking design components and subsystems through the design lifecycle.

Requirements management tools are used by 76% of respondents. Finally, almost two-thirds use static code analysis tools, which inspect code during the development process. Both requirements management tools and static code analysis are great candidates for sourcing component level meta-data and giving IPs the context to aid reuse.

While not the majority, more of the organizations Perforce surveyed are moving to the cloud and cited reasons include optimization of capital expenditure, better pricing, support and maintenance, and control over operating costs as well as reducing the cost of expanding infrastructure. Respondents also said using the cloud helps them manage demand for peak-time computing more efficiently; it was also found to be beneficial in terms of its ease of use and access, including spinning up teams quickly and as a means to better involve home-based workers.

The big picture

Collectively, survey results paint a picture of the state of semiconductor design and development right now while offering good indicators to overcome some of the challenges that industry faces. Some things are clear: alongside ensuring IP security and compliance, dealing with the difficulties of IP management, discovery and reuse must be addressed.

As SoC designs become more prevalent with increasing amounts of the target system being developed in-house by systems companies, semiconductor development needs to take a more IP-centric approach to get ahead. The initial set of components/IPs will need to be discovered/designed, but once the base architecture is in place, good IP reuse aids design so it can become an iterative process to leverage/reuse those IPs to reduce costs and improve performance for a given system design. This partly means that finding the right platforms and tools to manage and deploy IP more effectively is key, including a common view aggregated across multiple dimensions. An IP lifecycle management (IPLM) tool can deliver significant efficiencies to the design process. It can manage many variants across different product skews, with different hardware IP and embedded software IP versions, all via a hierarchical bill of materials (BoM) overlaid with metadata to track state and quality.

Creating the right culture around IP management is equally important: as is always the case, people's buy-in and the right processes matter as much as the supporting technology. Therefore, communicating to users the need for IP-centric design and educating them around the tools and processes required is also advised.

Worldwide, semiconductor design and development faces multiple hurdles, but likewise, there are some significant opportunities out there. The survey results underscore some of the substantial challenges and positive signs of how many organisations are focusing on IP reuse to continue thriving in this fast-changing industry.

REFERENCE

➤ 'Global Embedded System Market Forecast, 2020-2027', Fior Markets, May 2020.

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Sub-fab seals critical in handling complex chemistries at higher temperatures

The quest for higher performance has steadily increased the complexity of semiconductor manufacturing. Corrosive, exotic and highly reactive gases combined with new metallization chemistries have increasingly challenged sub-fab vacuum and abatement systems, requiring advanced seals to help ensure more uptime. Greene Tweed explains the latest solutions for handling the toughest chemical compositions.

BY SEEMA GANGATIRKAR, GREENE TWEED, INC.

In recent years, as the Semiconductor industry embraced FinFET and 3D NAND technologies, manufacturing processes came to require the utilization of more exotic gases at higher temperatures. The combination of new gases and higher temperatures drove the development of new sub-fab sealing solutions that perform reliably under these harsh conditions.

Sub-fab sealing applications

The sub-fab is critical to maintaining the operational effectiveness of the cleanroom environment above it. As wafers undergo a variety of processes including etch and deposition, effluent gases like flammables, oxidizers, and corrosives are shuttled through exhaust lines into the SubFab for safe disposal.

Gases flowing into the SubFab condense within system exhaust lines, causing particle deposition which can lead to premature equipment failure. To keep gas molecules moving, thermal management systems are utilized to increase temperatures within the exhaust lines. The use of these higher temperatures heightens the need for reliable seals in pumps, abatement units, and valves.

Seal material selection considerations include temperature and chemical resistance to highly reactive gases and radical species. Selecting or installing the wrong material into a SubFab application could compromise the integrity of the seal and possibly lead to safety hazards and other unplanned maintenance events that impact production in the cleanroom above.

Elastomer seals

Within the SubFab, elastomers are often chosen as the seal material because they are flexible,

durable, easy to install, and conform well against many different surfaces. An elastomer or rubber is a polymer chain with viscoelasticity, meaning that it can be stretched and retracted. Elastomers make excellent sealing materials due to their self-energizing property which provides a sealing force response when compressed.

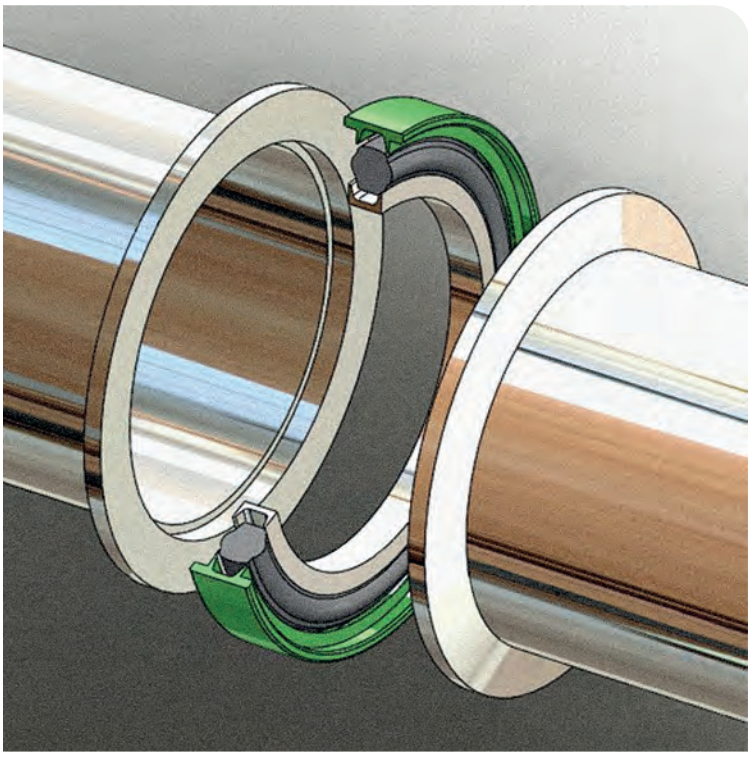
Elastomers are often molded into shapes such as o-rings or gaskets. Compared to other sealing solutions such as metal or plastic, elastomeric seals are more effective in mitigating leakage because they are generally more forgiving and conform well to most surfaces and thereby establish a tighter, more reliable seal; as an added benefit, they are also easier to install correctly.

Resistance to plasma

Choosing the optimal elastomer material usually comes down to application requirements. These are driven by a variety of factors that include compatibility with fluids and operating temperatures. Fluoroelastomers, including FKMs and FFKMs, are often selected as sealing materials for the sub-fab. As high-performance materials, FKMs and FFKMs are chosen for applications requiring a high degree of temperature resistance, chemical compatibility or both. FKMs have excellent compression set resistance, are resistant to a broad range of chemicals, and can operate in temperatures up to 450^{0}F. FFKMs are resistant to nearly all chemicals, including plasma, and can operate in temperatures up to 615^{0}F.

As fab process chamber and reactor conditions have grown more aggressive, it has effectively limited the reliability of general purpose FKMs in the sub-fab. Semiconductor manufacturing processes produce plasma gas, which is extremely damaging to most conventional seals. Even FKM polymers, which are known for their broad chemical resistance against many aggressive chemicals such as acids and solvents, are attacked by plasma.

When traditional FKMs are attacked by plasma, they will break down, crack, or fail prematurely. The higher the level of plasma exposure, the more quickly seals fail. Historically, sub-fab processes had very minor exposure to plasma and traditional FKM seals were acceptable. But as fabrication processes use more aggressive forms of plasma and higher temperatures, traditional FKMs are breaking down. Greene Tweed's high-performance Fusion® F10 was



designed by industry leading material scientists specifically to resist the moderate levels of plasma exposure seen in semiconductor processes. Fusion F10 contains higher amounts of fluorine than general purpose FKM materials, contributing to its exceptional chemical resistance to plasma when compared to chemical makeup of other FKMs.

Resistance to reactive chemistries

Emerging reactive chemistries, such as those found in ALD and epi SiGe processes, have a higher probability of condensation and require thermal management systems that increase temperatures in the forelines and exhaust lines to keep gases from depositing particles on equipment. As temperatures within these lines rise, many leading device manufacturers have switched to FFKMs, such as Chemraz® SFX, to ensure safety and tool uptime.

As Chemraz® SFX boasts higher operating temperatures up to 300°C/572°F and broader chemical resistance than FKMs, adoption of Chemraz® SFX seals helps ensure forward compatibility. Documented field experience has demonstrated chemical resistance to an array of

FKMs have excellent compression set resistance, are resistant to a broad range of chemicals, and can operate in temperatures up to 450^{0}F

sub-fab effluents in these temperature ranges, and internal Greene Tweed analysis has shown that SFX offers extra protection from in-line chemical interaction by limiting inclusion of moisture and oxygen.

Lab testing for permeation resistance using nitrogen and helium gases has shown that Chemraz SFX outperforms when compared to competitive materials. Materials that typically show good results in resisting permeation by nitrogen also demonstrate similar results against water and oxygen. This performance is attributable to SFX's unique filler and polymer backbone.

Innovative seal design

Ensuring the right o-ring is properly installed into the KF fitting assembly minimizes the chance of a premature failure. Unlike other commonly used materials in the SubFab which are typically black in color, Chemraz® SFX is grey and F10 is cream colored, making them easier to distinguish from other elastomers and lessening the chance that the wrong material is installed.

Furthermore, Chemraz® SFX's performance advantage in harsh conditions also benefits from its innovative seal design. Greene Tweed's custom engineered assembly overcomes the mechanical limitations of KF fittings in extreme process environments and improves seal performance. The custom assembly is available in different materials including stainless steel, aluminum and PTFE. Chemraz® SFX solutions are offered in a green-colored assembly as an additional safeguard to ensure the proper material and seal is being used.

Greene Tweed has specific expertise in seal design. Through FEA analysis, company engineers were able to understand how a standard o-ring installed in a KF fitting performs in application, and where potential failure points due to gland overfill may occur. Taking that knowledge, Greene Tweed re-engineered its elastomeric component of the KF fitting to a new custom cross-section that now accounts for gland overfill, thus limiting the possibility of premature failure. The inner and outer rings are also engineered to account for the custom geometry.

Backed by a broad portfolio of elastomeric materials, including general purpose and high-performance compounds paired with expertise in the semiconductor industry, Greene Tweed engineers evaluate each application carefully and recommend the material best suited to it, thus ensuring superior cost of ownership.

The company's wide range of seals guarantees that semiconductor sub-fab requirements can be met including the needs of vacuum and abatement systems tied to processes utilizing highly corrosive and reactive chemistries.

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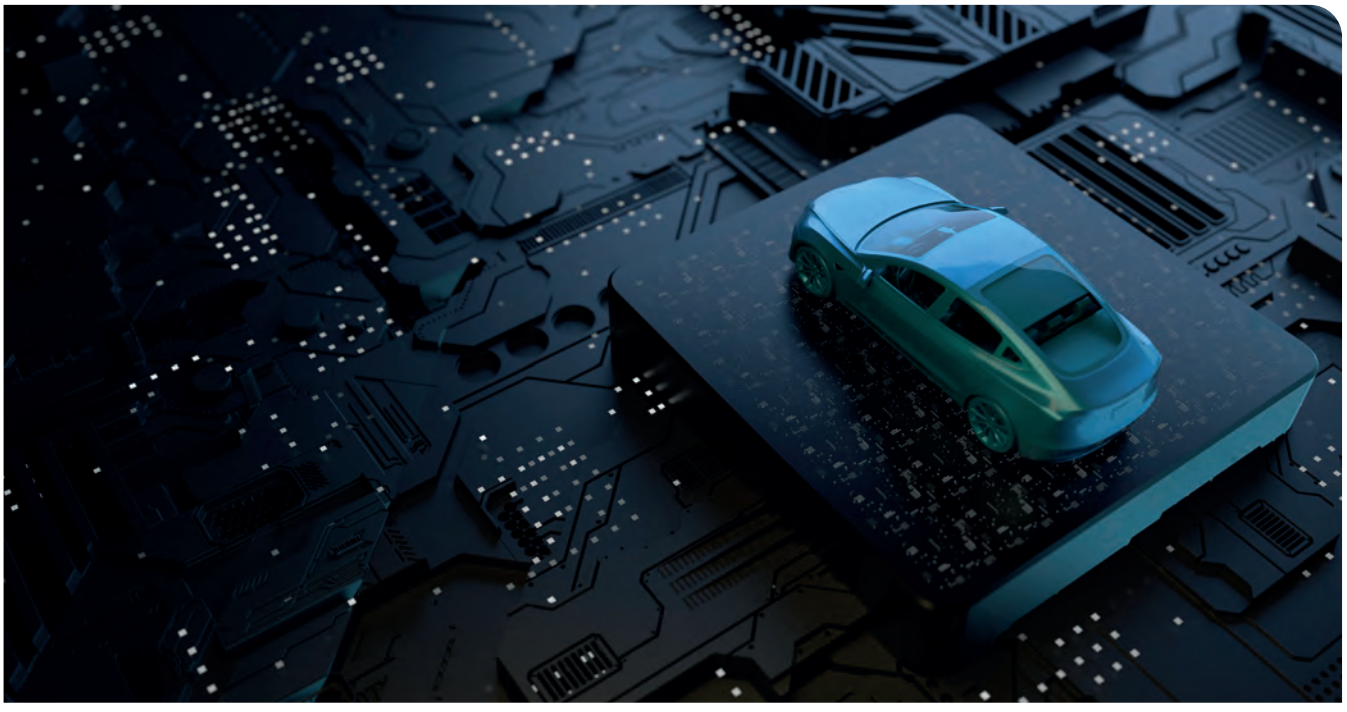

Pandemic lessons learned will shape IC manufacturing well beyond 2022

From the first days of the pandemic to the recovery now taking hold, the semiconductor industry has retained its role as both a pain point and as a balm to speed a much needed global economic reset. One quarter into the New Year, we examine common assumptions, the facts, and strategies for achieving sustainable growth amidst challenging times.

AN ANALYSIS BY MARK ANDREWS, TECHNICAL EDITOR, SILICON SEMICONDUCTOR

BUSINESS UNUSUAL is how many have described the semiconductor industry throughout the past two years. This description persists as manufacturers work their way out of varying pandemic-induced crises towards sustainable growth.

If the pandemic can be credited for any changes in semiconductor manufacture it is an important new understanding across different industries that a full recovery is going to require increased production of semiconductors from the most simple power controllers to the most advanced ASICs. What isn't clear is how to find the best road for meeting demand amidst continuing supply chain woes and the reality of a world that continues to grow ever more dependent on advanced technology. While digitization was already well underway in 2019, the pandemic transformed evolution into revolution. And as we can all appreciate now more than ever, revolution by nature forces a disruption of the status quo.

It doesn't take an in-depth market study or a survey of the world's top manufacturers and suppliers to know that the IC business is booming and will stay that way for the foreseeable future. But since technology is in a sense 'all about the numbers,' let us take a look at one recent study released in January by IC Insights that showed 2021 chip sales grew 25 percent. This came on the heels of records set in 2020 despite the challenges of manufacturing amidst the worst global pandemic in a hundred

years. While 2022 is expected to be another growth year, IC Insights believes that a long anticipated return to more typical business growth will result in a comparatively 'modest' growth rate of 11 percent this year. Keep in mind that 11 percent growth in virtually any of the 10 years preceding 2020 would have sent champagne corks popping across the globe.

In an industry as large as global semiconductor manufacturing, it is best to have as many insights as is practical before closing the books. The Semiconductor Industry Association (SIA), in a March 2022 report, said it expects 2022 may hold some additional surprises in the form of growth that could surpass the IC Insights forecast. The SIA stated that global IC sales increased 26.8 percent year-on-year as of January – this figure is the second highest first quarter start in history. Bear in mind that January sales are typically well off those of the previous year's fourth quarter since in January of a typical year, the ICs going into holiday gifts around the world have largely been built, sold, and shipped to OEMs; slight seasonal peaks and valleys typically appear in the quarters that follow, but first quarter is usually a time to restock, resupply and plan how to achieve success throughout the ensuing months. Not so much in January 2022 – this year, January was all about filling orders and reducing backlog.

The lack of advanced ICs and semiconductors of all types has been widely discussed as reasons for some OEMs to report smaller than expected sales. Indeed, some were held back, like Apple that reported it 'lost' up to $6 billion in sales due to its inability to complete product builds. Over at Nvidia Corporation, CFO Colette Kress echoed that refrain, saying her company did not realize a substantial amount of sales it believes it could have achieved had all key components been delivered as originally expected. Kress forecast supply constraints to ease by mid-year. But her forecast needs to be considered in two contexts that have great potential to upset the applecart: first, manufacture and delivery may continue to improve if there is no major surge in COVID-19 infections due to new variants emerging. Secondly, while Kress did not attempt to offer insights about other business influencers beyond the pandemic, it is clear that no one can accurately predict how the conflict in Ukraine begun by Russia weeks ago may eventually affect global markets including semiconductors.

While every product that needs to move from one distant point to another has been impacted by pandemic related shipping and distribution challenges, automobile manufacturing is often cited as a heavy industry bellwether. While this is very likely true within regions dependent on a particular auto makers' health, understanding the true cause and effect at the national and global level isn't as simple as accounting for a single variable. Like most complex manufacturing processes, the success of vehicle production and sales can't be tied solely to one commodity. In fact, recent studies appear to reveal that some of the assumptions around the impact of IC shortages on new car sales may have been over stated. While contributing to empty sales lots and higher prices, was the lack of some semiconductors the ultimate culprit?

In a recent IC Insights study, researchers took an in-depth look at the automotive device market as part of the organization's January Semiconductor Industry Flash Report; look to the IC Insights February quarterly update for in-depth auto IC sales numbers and forecasts.

This is the point where previous 'conventional wisdom' departs from the facts that are now available. According to a sizeable majority of auto related headlines, supply and demand imbalances can be traced to ways that the semiconductor device shortage that began in late 2020, grew in 2021, and persists into 2022 has dramatically impacted both the availability and cost of new vehicles. Further, that the lack of new vehicle production has led to escalating used car prices and a general lack of replacement vehicles for anxious buyers.

The commonly accepted rationale for what led to auto makers' woes goes a bit like this: In March of 2020, just as the first shut-downs signaled the onset of the COVID-19 pandemic, auto demand plunged worldwide. Auto makers reacted to this and began to shut down plants and halt semiconductor orders from suppliers. Like many manufacturers, the relatively cheap and fast ability to move goods around the pre-pandemic world led auto makers to depend on a 'just-in-time' inventory strategy that helped reduce costs of warehousing months' worth of parts at the expense of flexibility should vital parts suddenly become unavailable. Just-in-time as a

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business strategy works so long as the supply chain is functioning according to established performance metrics. The strategy falls flat on its face when container ships can't load or unload, and vendor factories are idled for protracted periods of time.

While auto makers were putting the brakes on their usual inventory restocking practices, there was a global surge in demand for cellphones, televisions, computers and monitors, games, and home appliances from a global population that was sheltering in place. As the pandemic grew in mid-2020, what began as sheltering in place turned into a tsunami of work-from-home paradigm shifts that are only now beginning to reverse in substantial numbers. As conventional wisdom holds, semiconductor manufacturers and suppliers switched production capacity away from automotive devices to the commoditized components and ASICs needed to build electronic systems now suddenly in much higher demand compared to purchasing in typical years.

When auto makers wanted to reopen factories in 2020, the story goes than many if not most found that semiconductor suppliers had shifted production capacity away from automotive applications to meet greater than usual demand for consumer electronics. IC manufacturers could not meet a renewed demand for automotive products, so a serious shortage ensued. This shortage drove up the price of new cars and light trucks while transforming pre-owned cars into driveway goldmines.

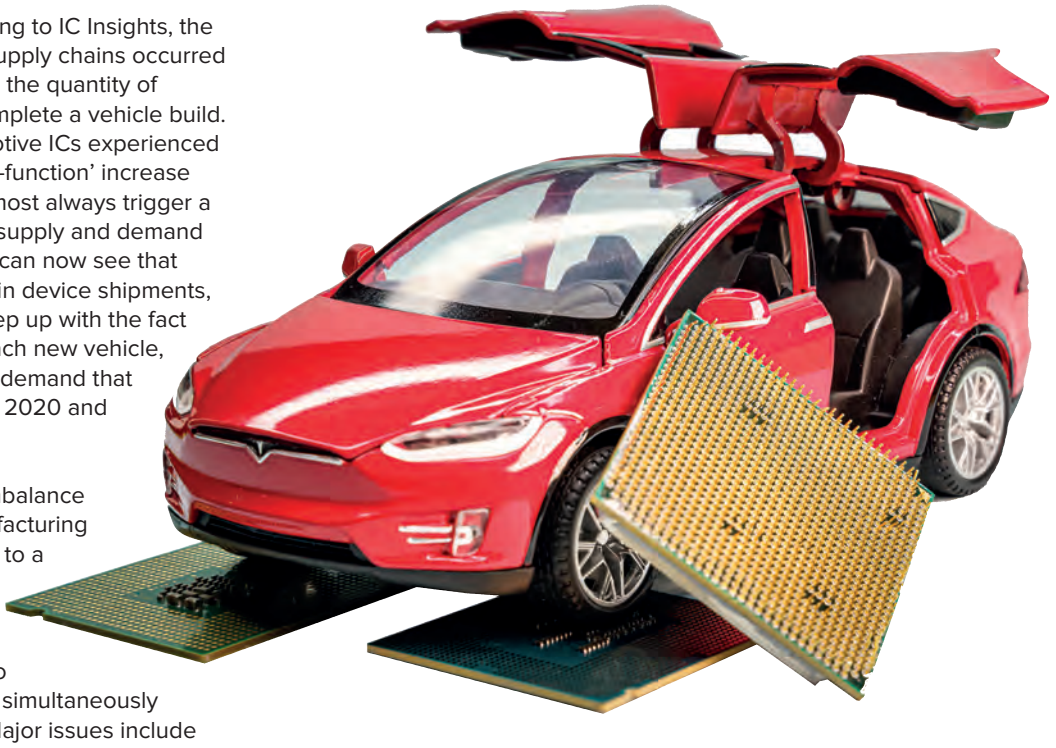
IC Insights has said that it believes that the commonly accepted scenario described above is not the complete story behind automotive industry production shortfalls. In the opinion of IC Insights' researchers, the real reason behind the automotive IC shortage lies in a combination of factors: first, the surge in demand for automotive ICs in 2021 was to blame, not the inability of semiconductor manufacturers to increase production. Automotive ICs are increasingly vital in each succeeding generation of new cars and light trucks thanks to their role in advanced driver assistance and safety (ADAS) systems, greater vehicle autonomy, the shift from conventional internal combustion engines and drive trains to electric vehicles, and more in-vehicle entertainment and internet connectivity. Essentially: supply was falling short due to a combination of pent-up demand in 2020 and the fact that more ICs were needed per vehicle. (See Figure 1)

According to the researchers, IC manufacturers actually shipped 30 percent more devices to the automotive industry in 2021 as compared to 2020, which was substantially greater than the 22 percent increase in total worldwide IC unit shipments recorded in 2020. What is especially revealing is that the growth of IC units shipped to auto makers in 2021 was substantially greater than pre-pandemic 2019. Further, the response by manufacturers' to their auto manufacturer customers' needs represented the greatest increase in shipments since 2011. The most recent substantial jump in IC shipments to auto makers occurred between 2016 and 2017 when shipments increased 20 percent. The 2017 growth spurt was considered record-setting at the time.

So where does the mismatch come between the shipments we can see vs. the commonly held public perception that semiconductor manufacturers did not 'step-up' when needed? A lot hinges on the subjective nature of perception and the complicated entanglement of influencers that affect outcomes

Figure 1.

across global markets. According to IC Insights, the pandemic's impact on global supply chains occurred at a time of continual growth in the quantity of semiconductors needed to complete a vehicle build. Essentially, demand for automotive ICs experienced what is generally called a 'step-function' increase in 2021. Such increases will almost always trigger a temporary mismatch between supply and demand regardless the product. So we can now see that despite a 30 percent increase in device shipments, IC manufacturers could not keep up with the fact that more ICs are needed in each new vehicle, paired with unexpectedly high demand that grew during the second half of 2020 and throughout 2021.



The pandemic-driven global imbalance between semiconductor manufacturing and OEM consumption has led to a substantial reevaluation of where the most advanced chips are manufactured and how industry might work to restore balanced growth while simultaneously addressing long term needs. Major issues include the concentration of chip manufacturing in the Asia-Pacific region; impacts of More's Law-driven device architectures changing into 'More than Moore' paradigms; and the implications still being assessed of talent shortages now seen globally as today's most senior engineers, researchers and technicians retire or for other reasons decide to leave the industry.

Even before the pandemic, alarm bells were ringing when manufacturing advanced ICs had substantially moved out of North America and Europe in favor of lower labor cost locations across the Asia-Pacific region, most notably to Taiwan, Korea and China. Perhaps one of the most striking indicators is a look at the share of worldwide semiconductor manufacturing in the United States in 2020 compared to 1990. According to an analysis by Brookings Metro published earlier this year, despite its incumbency role in developing the semiconductor industry, US-based IC manufacturing has fallen steadily in the last 30 years from a 37 percent share to about 12 percent in 2020. According to experts at Employ America, this transformation has many implications, but the two most worrisome is the loss in production leadership and also what they describe as the 'learn by doing' processes that go hand-in-hand with manufacturing.

Ask any production manager or engineer how they honed their fab expertise and grew within their fields. Most will attribute success to a combination of continuing education and the hands-on work experience that gives seasoned employees an edge. From a company's least experienced new hire to a company's most senior researchers and chief technologists, experience counts not only in terms of production efficiency but also because of its unique ability to drive innovation. It may sound obvious, but many of the best ideas manufacturers develop are outgrowths of hands-on work with the product and the machines, processes and materials required to make said products. Essentially, building advanced devices concentrates the experience needed to build next-generation devices in the location where the manufacturing takes place. Studies by Employ America have shown that not just in the US, but in any location that hosts advanced manufacturing, it is the presence of manufacturing facilities alongside research and academia that enables constant product and process improvement, which elevates competitiveness.

In the United States and across the European Union, the importance of having advanced semiconductor manufacturing in-country is key to continuing leadership within a given field. This has led to a number of legislative initiatives in both the United States and the EU to foster 'home grown' manufacturing. The United States has its America COMPETES Act along with the CHIPS for America Fund now being debated in Congress. The EU has developed and supported its counterpart, the European Chips Act, which ambitiously calls for quadrupling Europe's production capacity by 2030 while also attempting to create systems designed to avoid future supply chain disruptions. Both US and EU initiatives are designed to counter the subsidies, government ownership and tax advantages found in other countries including China and Taiwan that underwrite the development and expansion of semiconductor manufacturing within their borders.

Governmental actions in North America and Europe have not gone unnoticed as evidenced by new rules and tax incentives to support and safeguard local semiconductor industry recently passed by

South Korea's National Assembly. In China, 15 local semiconductor funds have been established in an effort to supply 70 percent of its own chip needs by 2025.

Not finding a sought-after consumer electronics product, or paying substantially more for it, is certain to catch the eye of any frustrated shopper. But what does not make mainstream media headlines is the titanic shift underway that is already changing the way chips are designed and manufactured.

While Gordon Moore's 'Law' drove the pace and essential rules for competitive semiconductor architectures through the early 2000s, it has become more and more apparent that transistor shrink can no longer meet the needs for greater performance, reduced size and lower power consumption that have enabled widespread use of semiconductors across multiple product categories. The 'More than Moore' (MTM) movement has many permutations, but to condense this into digestible bites, think of MTM innovations as design approaches that depend upon new electronic materials science, new device structures and even whole new underlying technologies as a means to achieve performance, cost and power consumption goals rather than conventional Dennard scaling.

As outlined in an article in this edition of Silicon Semiconductor, ClassOne Technology Vice President John Ghekiere points to ways that he has seen companies outside the exclusive club of 'Uber Foundries' still pursuing transistor shrink are instead charting new courses to achieve their goals without the complexities and expense driven into Moore-style transistor shrink. These are innovative companies working to develop top-performance devices, yet they eschew coughing up the price for EUV lithography systems or other exorbitantly expensive technologies designed to enable transistor features scaled to and below 3nm.

"The withering march of relentless device scaling described by Moore's Law has left a mere handful of device manufacturers in that race, with TSMC clearly in the technology lead. When the cost per transistor inflected to become more expensive with each generation, somewhere between 26 and 22 nanomater nodes, it drove even many of the larger and more powerful manufacturers to alternate paths of innovation and new means of bringing value; GlobalFoundries pivoted boldly into FD-SOI; STMicroelectronics into SiC. The broad expansion of new device types - in short, the ubiquitous adoption of microelectronic devices into almost every aspect of our daily lives - has brought about the More Than Moore era, where feature scaling is no longer the sole means of device innovation," he said.

The headlong pursuit of More Than Moore strategies at the time other manufacturers are seeking to build 3nm devices, plus the simultaneous need for more semiconductors for more applications is creating a unique combination of challenges and opportunities for the industry. This is perhaps best appreciated when one considers that third and fourth quarter 2021 saw one of the largest employment sea changes since the Great Recession of 2008. In the United States alone, 4 million persons changed jobs, retired before age 65, or left the workforce across a multitude of professional roles for a variety of reasons.

The SEMI trade association reported results of its latest industry survey on 28 February 2022 that points to the greatest concerns amongst its international membership. More than 400 US member companies replied, offering insights into perspectives about the importance of enhancing competitiveness through targeted public and private investments aimed at developing the industry's manufacturing capacity, infrastructure and workforce. SEMI conducted the survey in partnership with MITRE Engenuity, the technology foundation for public good launched by MITRE two years ago.

The survey indicated US manufacturers and key suppliers see needs and challenges in three primary areas:

- A need for investment across the entire semiconductor ecosystem
- Investment by private firms as well as publicly-funded entities to counter the governmental incentives provided in current centers of IC manufacturing in Asia-Pacific
- Investment in multi-generational workforce initiatives including STEM incentives, apprenticeship programmes, and similar efforts built around creating interest in careers that pay well but may be perceived as unreachable goals

While governments and major semiconductor manufacturers agree hybrid investment strategies are key to increasing competitiveness and to ensuring continual growth in the global chip supply, it was somewhat surprising to see the importance placed on growing the talent pool of engineers, technicians, researchers and scientists focused on developing and manufacturing advanced ICs. Respondents in the SEMI survey were essentially saying that building new fabs in Europe, the United States and elsewhere are critical to expanding global semiconductor capacity while supporting the 'on-shoring' of IC manufacture, but that shiny new infrastructure will come to naught if those facilities cannot be staffed by a highly educated, well trained workforce.

The combination of senior technical staff reaching retirement age and plans to dramatically increase manufacturing in North America and Europe are at odds – factors that will play an increasingly important role to correcting the supply/demand imbalance while ensuring that there is a steady supply of semiconductors from a diversified global manufacturing base.

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- Combining EVG's world-class wafer bonding, thin-wafer handling and maskless, optical and nanoimprint lithography products and expertise, as well as pilot-line production facilities and services

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