SILICON SEMICONDUCTOR

Connecting the Silicon Semiconductor Community

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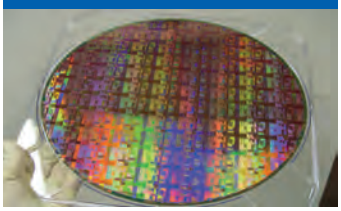
Auto makers must find memory 'sweet spot'

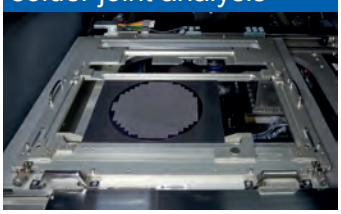
Ultrahigh purity valves help thin film deposition

From wearables to 'careables'

Stacking GaN on silicon transistors



3D semiconductor solder joint analysis



Brewer Science

Materials are Key to Next-Generation Flip-Chip FOWLP

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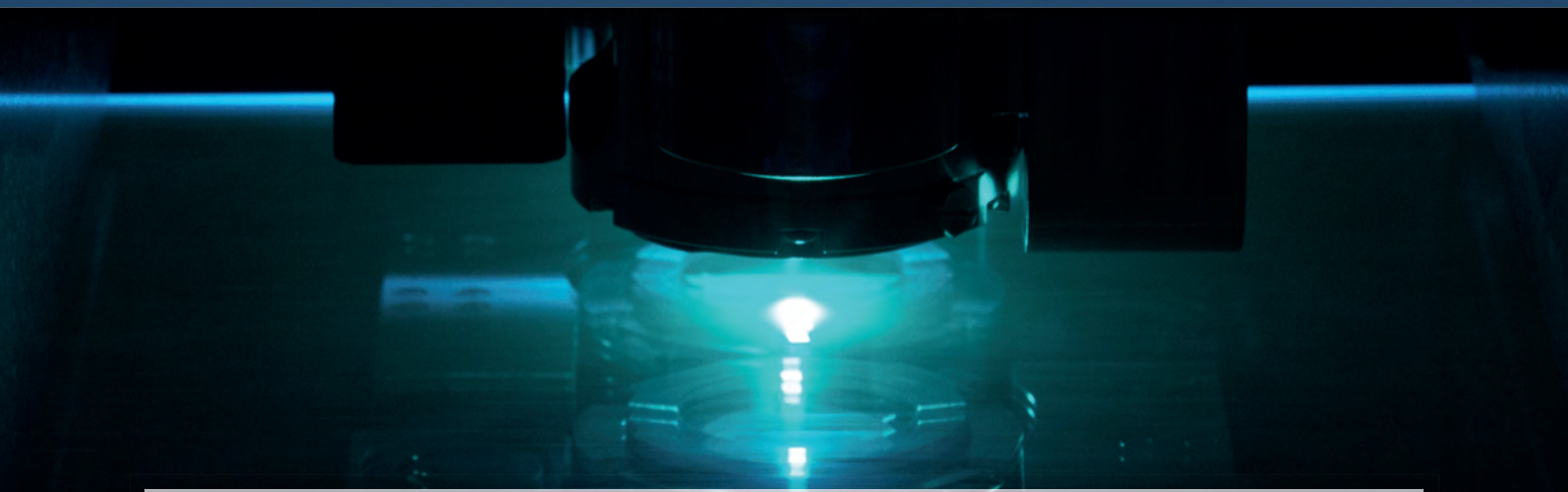

- Featuring next-generation digital lithography technology for high-volume manufacturing
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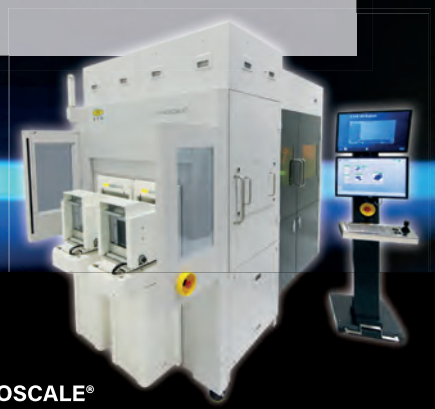

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editor's view

By Mark Andrews, Technical Editor

The year we didn't expect continues to amaze

AS WE ENTER fourth quarter 2020 – a time of reflection on what was, and speculation on what will be – no one across industry can say 2020 wasn't a year of surprises. Some good. Some bad. Some very bad. Five years from now, what will the Year of the Pandemic look like in our review mirrors?

Firstly, when the world realized a new, potentially fatal virus was going to impact every corner of the earth, we reacted with fear, denial, stalwart preparation, confusion and dread – And then we got on to deal with it even while life around us changed in ways we could not have anticipated nine months ago.

Secondly, while some industries have 'cratered' and remain in dire straits, the semiconductor supply chain has managed to grow despite typhoon-like headwinds. Industry conferences have been cancelled and rescheduled by the score even as companies have had to reinvent themselves in a business-unusual year driven by COVID-19 fears.

Lastly, some have prospered throughout this pandemic despite not having a direct connection to medical treatment or other sectors that tend to grow when infectious disease captures headlines. Cases in point: on 8th September the SEMI trade group reported, "…Soaring pandemic-inspired demand for chips … will drive an 8% increase in global fab equipment spending in 2020 and a 13% increase in 2021. SEMI cited, "… rising demand for semiconductors for datacenter infrastructures and server storage …" plus a buildup of stock in case US-China trade tensions reintensify. At the same time, world-class luxury automotive brands like Daimler-Benz announced new vehicles

in hopes of reviving sales that plummeted in 2020; analysts say the pandemic will keep new car demand at record lows for up to five years.

In this edition of Silicon Semiconductor we look at important trends and innovations that are driving success. Brewer Science, in concert with imec, describes how its latest bonding material innovations are enabling zero die shift (ZDS) in fan-out wafer-level packaging (FOWLP). We also hear from the experts at Rambus discussing memory requirements for higher levels of vehicle autonomy. We also delve into new generations of medical diagnostic and treatment tools powered by new sensors, AI and machine learning that imec describes as the future of 'Careables' – critical links to ways that medical professionals will soon care for all of us.

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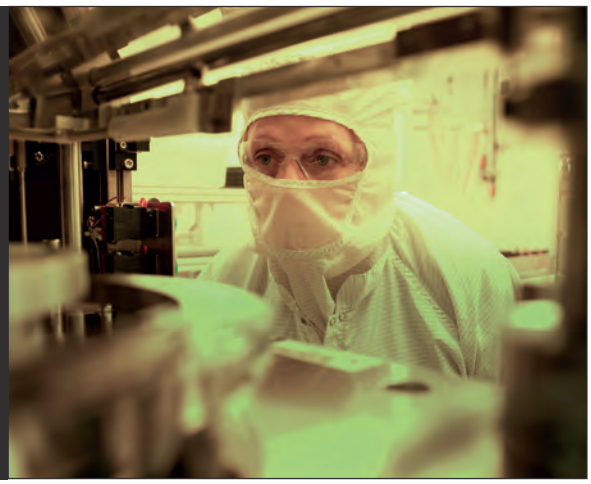

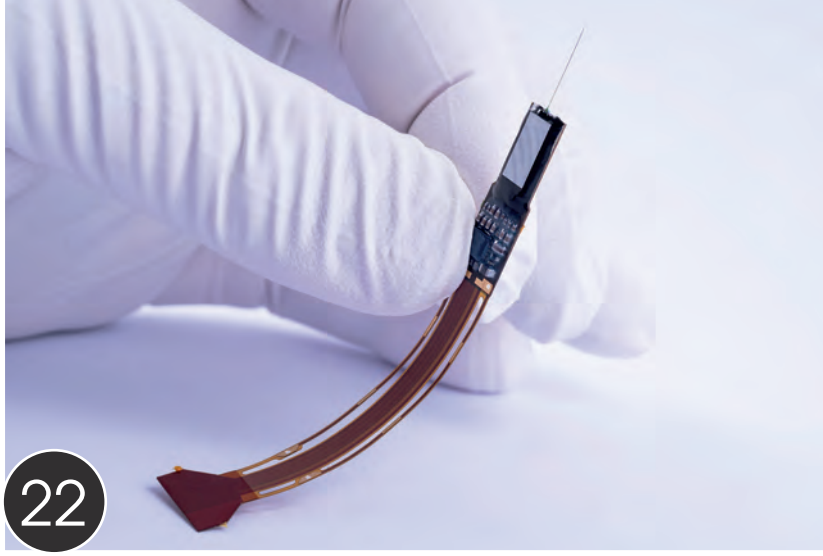

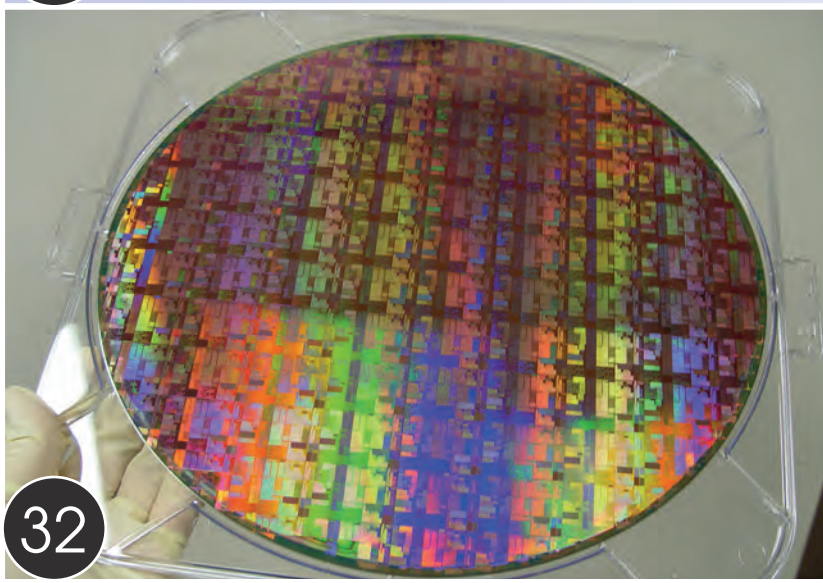

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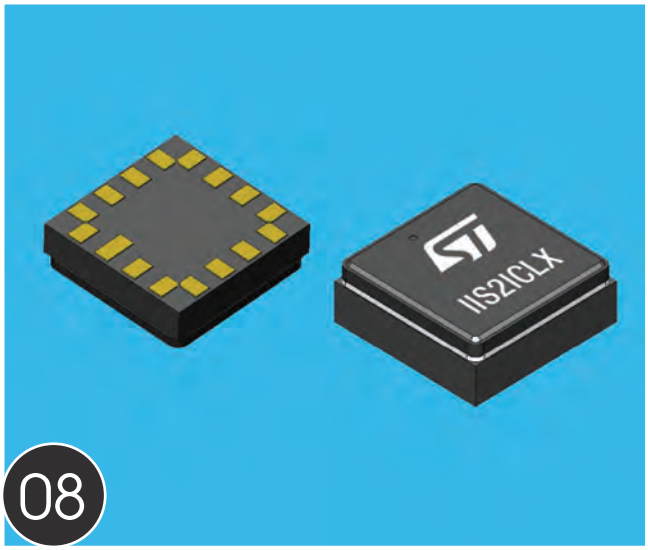


Scientech and Trymax partner to distribute resist ashing and UV products in Taiwan

TRYMAX SEMICONDUCTOR EQUIPMENT BV, a supplier of semiconductor plasma technology, and Scientech, have entered into a distribution agreement for Taiwan. The agreement gives Scientech Corporation the right to distribute all of Trymax's NEO ashing, etching products and their latest UV curing and charge erase products.

This agreement with Trymax will assist Scientech in expanding its business in the segment of high speed communication, 3D sensing including ToF, high frequency power devices and related device markets. Scientech offers extensive experience in introducing the highest quality equipment from around the world and will provide world-class technical and field support for Trymax products after system delivery.

"A partnership with Scientech is a critical component for our expansion strategy in Taiwan" stated Ludo Vandenberk, Executive Vice President of Trymax Semiconductor Equipment. "By combining forces with Scientech, we are able to better serve the front-end, MEMS and back-end manufacturers with solutions that span the ashing, descum and lite etch process steps as well as the UV curing and charge erase applications. We are eager to get started serving our customers with the competitive advantages that our technologies can offer.'With Trymax's expertise and cost-effective solution, we are very grateful to cooperate with Trymax to support the customers in the semiconductor field, which is not only to enhance our coverage of front-end production but also to strengthen our customers' competition in the arena." commented Peter Kuo, Vice President Representative Div. II at Scientech Corporation.

Trymax's NEO products for ashing, etching and descum serve the semiconductor industry for 150mm, 200mm and 300mm substrates. Our bridge tools are fully flexible for processing multiple different substrates types like Si, GaAs, SiC, LiN, LiT, eWLB and Taiko wafers from R&D to high volume production."

"We offer optimized solutions based on the best cost of ownership in combination with the maximum flexibility. All Trymax platforms are configured with a fully digital onboard communication system with up to 5 different process chamber technologies selectable. The UV curing and charge erase equipment from Trymax is used for a wide range of applications that includeing photo-stabilization of the resist prior implantation or etch, for small CD, or to erase charge built-up during the IC manufacturing process. The NEO 2000UV has been designed taking advantage of the reliable NEO platforms developed by Trymax for plasma ashing, descum, and etching applications. The NEO 2000UV is implementing state-of-the-art robotics, components, the latest digital technologies and software, and is CE compliant. NEO 2000UV can accommodate cassettes or SMIFs.

Global semiconductor sales increase 4.9 percent

The Semiconductor Industry Association (SIA) has announced worldwide sales of semiconductors were $35.2 billion in July 2020, 4.9 percent more than the July 2019 total of $33.5 billion and 2.1 percent greater than the June 2020 total of $34.5 billion.

Monthly sales are compiled by the World Semiconductor Trade Statistics (WSTS) organization and represent a three-month moving average. SIA represents 95 percent of the U.S. semiconductor industry by revenue and nearly two-thirds of non-U.S. chip firms.

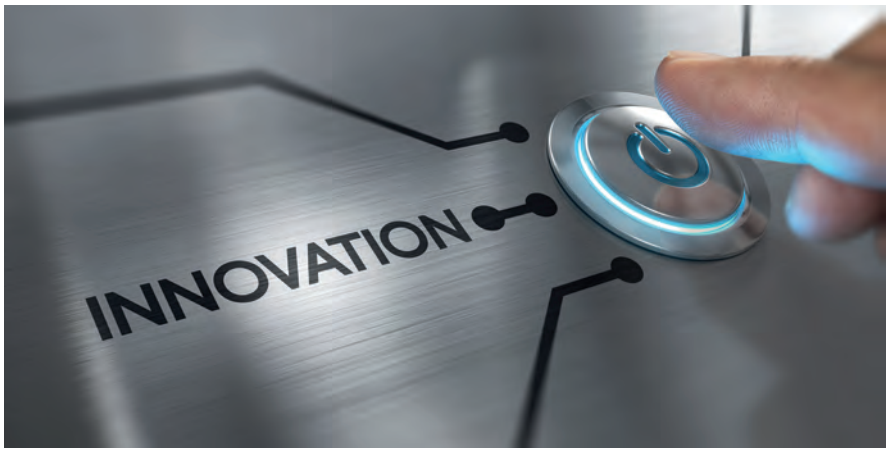
"The global semiconductor market has so far remained largely resistant to global macroeconomic headwinds through the first seven months of the year, with sales in July increasing on both a year-to-year and month-to-month basis, but substantial market uncertainty remains for the rest of the year," said John Neuffer, SIA president and CEO.

"Sales into the Americas remained strong in July, increasing 26 percent year-to-year, and year-to-year sales were up globally among both memory and non-memory products."

Regionally, sales increased on a year-to-year basis in the Americas (26.3 percent), China (3.5 percent), and Asia Pacific/All Other (1.4 percent), but decreased in Japan (-0.4 percent) and Europe (-14.7 percent). On a month-to-month basis, sales increased across all regions: Asia Pacific/All Other (4.5 percent), Japan (3.4 percent), Europe (3.2 percent), the Americas (0.9 percent), and China (0.5 percent).

Onto Innovation announces new metrology systems

ONTO INNOVATION INC. announced the availability of a suite of process control metrology solutions for advanced device manufacturing. The suite of optical metrology solutions was developed for next generation semiconductor devices to enable high precision, high accuracy, and high productivity solutions for Gen6, 3D NAND, leading 5nm/3nm logic and advanced 1alpha DRAM devices. This new metrology suite represents the first exciting results from Onto Innovation's enhanced R&D team to create a comprehensive solution set that capitalizes on its extensive leadership in optical metrology and enhancements in a new machine learning engine software for all of these applications.



Kevin Heidrich, senior vice president of marketing, commented, "We are very excited by our customers' early responses to the performance and value of these new systems. Our measurement data analysis from advanced logic and memory devices has been found to be highly correlated to our customers' metrology lab standards such as CD-SEM and TEM, which means they can continue to use high-speed optical metrology systems without the need to use significantly slower, and more costly, X-ray technology."

He continued, "For the most advanced 3D NAND devices, the challenges to measure the very high aspect ratio channel holes and word lines, with aspect ratios much greater than 80:1, are forcing customers to consider slower X-ray tools and other destructive measurement techniques. Similarly, for the most advanced DRAM and logic devices, complex transistor structures and new materials at the 5nm and 3nm nodes have customers looking at new methods of metrology for the critical gate-all-around/nano-sheet processing steps. Onto Innovation has developed platforms that drive optical technology to the next level enabling the advantages of both high sensitivity and high productivity, providing customers information at the rate and quality that is needed for process development and high-volume manufacturing."

3D NAND / DRAM / Logic Metrology

The new Atlas V metrology system is designed to measure several key steps that include buried features, not visible by CD-SEM and other techniques.

The sensitivity of Atlas V metrology enables these critical dimensions to be measured with high accuracy and sensitivity, extending the capability of optical solutions for generations of devices and eliminating the need for other slower process control techniques.

Atlas V technology now enables the performance needed for customers' development of gate-all-around devices and is over 100 times faster than X-ray solutions for these structures. Onto Innovation's customers that have validated this new OCD technology and have already seen the speed and resolution that was once thought to be beyond the limits of optical technology.

The IMPULSE V system, built on a history of industry leading reliability, enables higher productivity and higher performance for next generation integrated metrology. The system is designed to work seamlessly with chemical mechanical polishing (CMP) systems to provide high throughput run-to-run control for critical process steps.

The IMPULSE V system enables recipe inter-operability with the Atlas V system for uninterrupted production recipe setup and optimization. Utilizing the latest machine learning technology, the IMPULSE V technology supports on-device metrology enabling broad flexibility and high process coverage enabling higher productivity with broader process recipe coverage.

3D NAND Advanced Metrology

The new Aspect metrology system is a revolutionary optical platform that is designed for the current and future challenges of advanced 3D NAND devices. Memory density increases with both layer-pair scaling and tier stacking for memory stacks well over 200 pairs. The Aspect technology was designed with these future architectures and scaling strategies in mind. Aspect metrology is demonstrating performance superior to X-ray systems across multiple customer devices through a revolutionary infrared optical system providing full profiling capability to enable critical etch and deposition control, with the speed and process coverage that customers require.

All Products Powered by AI-Diffract Modelling Technology

AI-Diffract Technology is the key component of the new solution suite. It is the software analysis engine powering all of these leading metrology systems. This new product now provides up to 90% faster time to solution using the AI-Diffract engine which extends the industry leading NanoDiffract® software by leveraging extensive machine learning capabilities along with high fidelity modeling. The result is a simultaneous improvement in metrology performance along with a significant time to solution reduction.

All products are shipping to select customers this quarter, with broad availability by the fourth quarter. The company expects revenue to begin in the fourth quarter and ramp in the first half of 2021.

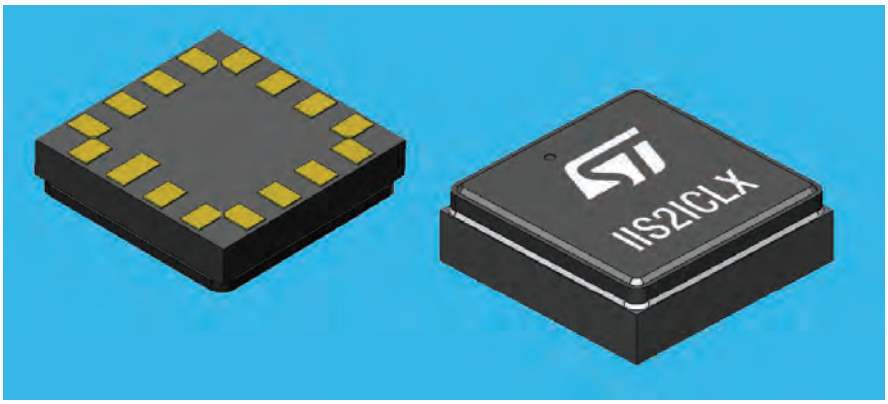
STMicroelectronics launches inclinometer with learning core

THE IIS2ICLX from STMicroelectronics is a high-accuracy, low-power, 2-axis digital inclinometer for use in applications such as industrial automation and structural-health monitoring. It features a programmable machine-learning core and 16 independent programmable finite state machines that help edge devices save power and reduce data transfers to the cloud.

With its advanced embedded functions, the IIS2ICLX lowers system-level power consumption to extend the operation of battery-powered nodes. The sensor's inherent characteristics simplify integration into high-performing products, while minimizing the effort and cost of calibration. Using MEMS accelerometer technology, the IIS2ICLX inclinometer has a selectable full scale of ±0.5/±1/±2/±3g and provides outputs over an I2C or SPI digital interface. Embedded compensation maintains stability over temperature to within 0.075mg/°C, ensuring high accuracy and repeatability even when ambient temperatures undergo extreme fluctuations. Its ultra-low noise density of 15μg/√Hz enables high-resolution tilt sensing as well as sensing of low-level, low-frequency vibration, as required in structural-health monitoring.

The combination of high stability and repeatability, high accuracy, and high resolution make the IIS2ICLX particularly suited to industrial applications such as antenna pointing and monitoring, platform leveling, forklift and construction machines, leveling instruments, equipment installation and monitoring, and installation and sun tracking for solar panels, as well as Industry 4.0 applications such as robots and autonomous guided vehicles (AGVs). In structural-health monitoring, accurately measuring inclination and vibration with the IIS2ICLX can help assess the integrity of structures such as tall towers and infrastructure like bridges or tunnels. Affordable, battery-powered MEMS tilt sensors containing the IIS2ICLX enable many more structures to be monitored for safety than has been economically viable using earlier, more expensive technologies. Whereas many high-accuracy inclinometers are single-axis devices, the 2-axis IIS2ICLX accelerometer can sense the tilt with respect to a horizontal plane along two axes (pitch and roll) or, by combining the two axes, can measure the tilt with high and repeatable accuracy and resolution with respect to a single direction of the horizontal plane over a range of ±180°. The digital output simplifies system design and reduces Bill-of-Materials (BOM) cost by saving external digital-to-analog conversion or filtering.

To ease the adoption of the IIS2ICLX and accelerate application development, ST also provides specific software libraries to support sensor calibration and real-time computation of tilt angle. Such software libraries are part of the X-CUBE-MEMS1 expansion software package for STM32Cub. The IIS2ICLX is housed in a high-performance ceramic-cavity LGA package measuring 5mm x 5mm x 1.7mm, with an operating temperature range of -40°C to +105°C. It is available now in sample quantities. The devices are in volume production now, with a web price of $15.00.



Watlow acquires CRC

WATLOW, an industry provider in the design and manufacture of complete thermal systems, is pleased to announce that it has acquired CRC (Component Re-engineering Company, Inc.) of Santa Clara, California. The terms of the transaction were not disclosed.

Since 2002, CRC has designed, built and serviced wafer pedestals used in semiconductor manufacturing facilities all over the world. CRC's unique high-temperature bonding and refurbishment technologies enable advanced ceramic pedestal and in-chamber solutions that complement the industry-leading thermal technologies developed by Watlow. Integrating CRC into Watlow's business advances the company's wafer pedestal solutions, which are essential for achieving the technological advances in the memory and logic segments of the semiconductor industry. Watlow will now have a full suite of wafer pedestal solutions from low to high temperatures and ranging from a single zone to 80 zones of control and beyond.

"Watlow is excited to invest in this innovative product portfolio and team," said Peter Desloge, Watlow's chairman and CEO. "We believe we are uniquely positioned to leverage CRC's capabilities and through our collective efforts will continue to unlock high-performance solutions that will bring added value to our customers."

"Watlow is investing aggressively right now, and it is our plan to continue," added Rob Gilmore, chief operating officer. "While continuing to scan for good partners and acquisitions, we are also expanding our investments in Europe and Asia to ensure we can support and respond to our customers and markets globally."
"We are very pleased to be joining the Watlow team," said Brent Elliot, CRC CEO and cofounder. "Watlow is a known leader in the industry, and we have worked with them for many years. I believe that combining our strengths will open new opportunities and create value for our customers."

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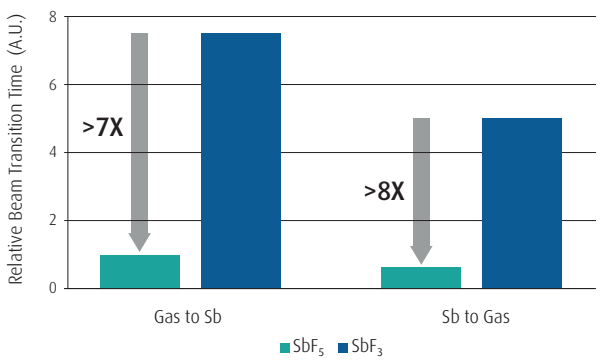
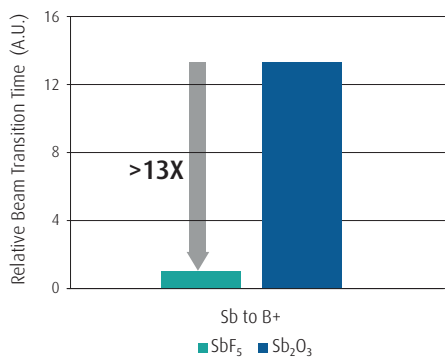
US Patent numbers:
10,597,773 10,711,343

1. High beam current
2. Longer source life
3. Fast beam switching
4. Easy handling & transport

Relative transition times comparison SbF_5 vs SbF_3



Antimony to Boron beam transition SbF_5 vs Sb_2O_3



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Mentor helps SimpleMachines speed development of first AI processor

MENTOR, a Siemens business, announced that artificial intelligence (AI) silicon startup SimpleMachines (SMI) successfully developed its first-generation product using Mentor's Enterprise Verification Platform including the Questa simulation platform and Veloce Strato emulation hardware, as well as Mentor Consulting's cloud-based Emulation-as-a-Service (EaaS) offering.

SMI's new AI processor, based on composable computing technology, features a "software-first" approach that is designed to enable extreme power efficiency and enhanced utilization of its powerful onboard deep learning algorithms. The device boosts total system software performance with a novel hardware design that reconfigures instantaneously to accommodate dynamic software workloads. To verify and validate the device, SMI used a Mentor flow featuring the Questa simulation platform and Questa Verification IP for PCIe and HBM2, together with Mentor's third-generation, data-center friendly Veloce Strato emulation platform. SMI accessed the Veloce Strato emulation platform via Mentor Consulting and its cloud based EaaS offering.

"We needed a cycle-accurate model of our hardware very early in the design and development phases of our first-generation device," said Karu Sankaralingam, CEO for SMI. "We turned to Mentor Consulting's exceptional simulation/emulation flow, together with the sound expertise of Mentor's consultancy services, which allowed us to port our neural network software to the underlying hardware much faster than we expected. Mentor's EaaS played a critical role in enabling us to rapidly develop and differentiate our AI system software a full year before initial availability of first silicon."

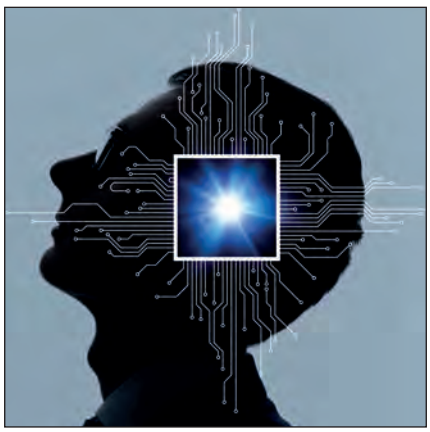
Mentor's EaaS provides customers with secure and reliable access to the cloud-hosted Veloce emulation hardware platform without requiring ownership or management of an emulator and associated infrastructure. The offering also includes expert consulting, which SMI selected to fully optimize the cost- and time-efficiency advantages of cloud-hosted, Veloce emulation hardware technology.

ventureLAB and Silicon Catalyst partner to expand silicon ecosystem

ventureLAB has announced that it has partnered with Silicon Catalyst to expand its reach for the Hardware Catalyst Initiative (HCI), Canada's first hardware and silicon lab and incubator. Silicon Catalyst is the world's only incubator focused exclusively on accelerating solutions in silicon, offering a coalition of in-kind and strategic partners to dramatically reduce the cost and complexity of development.

With a world-class network of mentors to advise startups, Silicon Catalyst is helping new semiconductor companies address the challenges in moving from idea to realization. The incubator/accelerator supplies startups with a path to design tools and silicon devices, as well as offering networking opportunities and access to funding, banking and marketing acumen to successfully launch and grow their companies' novel technology solutions.

According to the Semiconductor Industry Association, the global semiconductor industry generates $7 trillion in economic activity, creates 4.89 indirect new jobs for every one semiconductor job, and enables the development of breakthrough products like smart energy,



autonomous vehicles, and innovative healthcare solutions. Canada is a leader for creating and scaling IP-rich semiconductor and hardware companies and a magnet for home-grown and global talent.

The new partnership will expand the HCI's expert network to support hardware and silicon start-ups and scale-ups building and commercializing transformative solutions in healthcare, telecommunications, advanced computing, connected transportation and smart energy. This expanded support will also help the HCI deliver its mission to accelerate commercialization and reduce cost of development for emerging hardware and silicon leaders who are Built-to-Scale from Canada and go global.

"We are delighted to partner with Silicon Catalyst as the reach of the Hardware Catalyst Initiative expands coast-to-coast and around the world," said Melissa Chee, President and CEO, ventureLAB. "Canada is a recognized leader for creating and scaling IP-rich semiconductor and hardware-based companies and a magnet for home-grown and global talent. We are excited to collaborate with Silicon Catalyst in our collective bold vision to enable Canada's pioneering tech founders scale in the global innovation economy."

"Our mission is to provide early-stage entrepreneurial teams with the strongest possible foundation for business growth," stated Rick Lazansky, co-founder and Chairman of Silicon Catalyst. "Through our collaboration with the ventureLAB technology hub and it's Hardware Catalyst Initiative, these startups will gain access to critically important tools, services and in-depth semiconductor industry expertise uniquely available from our ecosystem."

ClassOne's Solstice LT Plating System selected by Jenoptik

SEMICONDUCTOR equipment manufacturer ClassOne Technology announced the sale of its Solstice LT electroplating system to Jenoptik for manufacturing semiconductor material for high-power diode lasers at its semiconductor production facility in Berlin-Adlershof, Germany.

High-power diode lasers play an important role in optical pumping of solid-state lasers as well as in direct use applications such as material processing, sensing as well as in healthcare & life science. The dual-chambered Solstice LT is specially configured for high-performance gold processing. The announcement was made jointly by ClassOne CEO, Byron Exarcos, and Dr. Juergen Sebastian, plant manager of the Jenoptik facility in Berlin.

"The new Solstice LT will replace a manual plating wet bench," explained Dr. Sebastian. "This will significantly improve process stability, plating quality as well as reduce our metallization step costs. That's important because at Jenoptik, we build all the semiconductors that go into our diode lasers in-house. The new Solstice LT electroplating system thus ensures very high quality, performance and service life of our end products. Moreover, the new system also promotes Jenoptik's policy of sustainability thanks to the new electrolyte technology."

"The Solstice LT for Jenoptik is specially configured with our GoldPro™ processing chamber," said Exarcos. "GoldPro can deliver unprecedented levels of repeatability – wafer-to-wafer, die-to-die, within-die, and within-feature. The bottom line is exceptional uniformity and reproducibility, along with reduced cost of ownership."

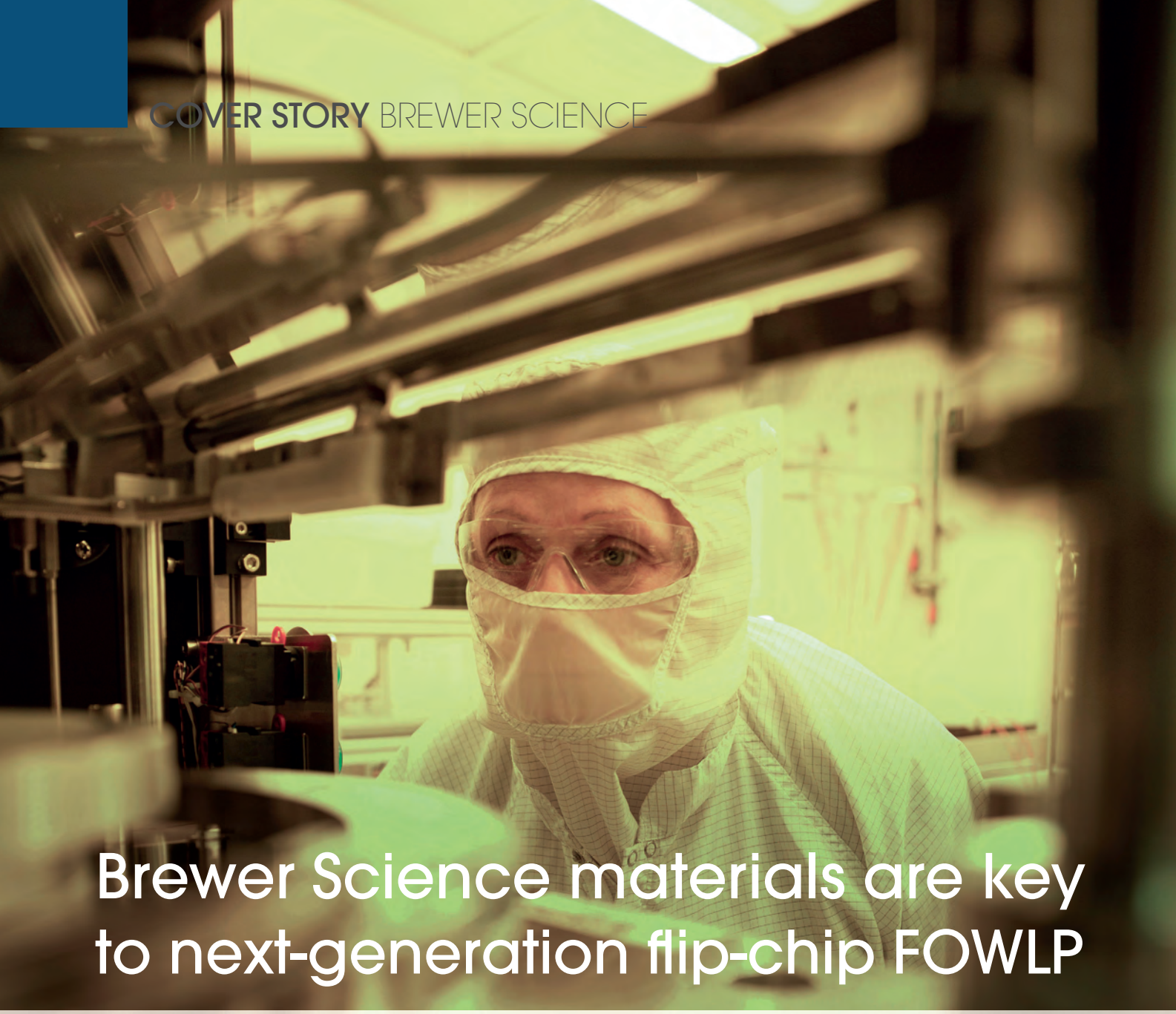
With the new electroplating system, Jenoptik is now able to process different GaAs wafers sizes to accommodate different customer requirements. Another reason for selecting Solstice was the flexibility of its design, which readily allows the handling of multiple wafer sizes on the same tool.

"We're proud to be on the Jenoptik team because their semiconductor lasers are industry leaders," said Exarcos.

"Their quality is based on advanced manufacturing, with strict quality controls and state-of-the-art process technologies. It's an environment in which Solstice can play an integral role, and we're looking forward to the next generations of Jenoptik diode lasers!"

ClassOne Solstice systems provide high-performance electroplating specifically for ≤200mm wafer processing. The Solstice series includes fully-automated 8-chamber and 4-chamber systems with up to 75-wph throughput as well as a 2-chamber semiautomated configuration that can be used both for process development and production.

In addition to electroplating, the unique Plating-Plus™ capabilities of the Solstice platform enable it to handle many other important functions, such as wafer cleaning, high-pressure metal lift-off, resist strip, UBM etch, and more. Solstice's class-leading performance and flexibility consistently make it the tool of choice for ≤200mm plating.



Brewer Science materials are key to next-generation flip-chip FOWLP

Temporary bonding and debonding solutions in many ways enabled the ascendency of 3D structures within silicon semiconductors and are essential to fan-out wafer-level packaging (FOWLP). Stacked dies, utilizing a combination of through-silicon vias (TSVs), microbumps and flip-chip technologies, provide essential connections within die stacks. Advancing FOWLP technologies offer new benefits yet also pose new challenges that are being addressed through innovative materials from Brewer Science.

THE DEVELOPMENT of FOWLP with a greater I/O density, more functionality, smaller form factors and continuing cost reductions is being actively pursued by growing numbers of researchers and manufacturers. But while FOWLP offers many compelling advantages, working with reconstructed wafers and assembling extremely thin dies presents unique challenges including warpage and alignment mismatch that can make further wafer processing a costly challenge. If FOWLP challenges are not addressed at the proper assembly point, yield can plummet and manufacturers can find that the technology they saw as a benefit could instead become a costly miscalculation.

To better appreciate the challenges of FOWLP it is worthwhile to consider some key processing steps, and within that context, to explore the advantages

of next-generation bonding materials that help ensure cost-effectiveness, productivity and higher performance.

With FOWLP, a redistribution layer (RDL) is created to direct I/O connections to the desired die location on the top of the device surface, typically a bump that connects to another die. RDLs can be created either before or after wafer over-molding steps that typically employ an epoxy molding compound (EMC) that has several key roles. The EMC keeps individual components in precise alignment, provides die protection, and enables the integration of dies of different functions and sizes into one wafer.

Assembling and processing dies for FOWLP presents many challenges due to the wide range of temperatures typically utilized, which in turn creates new challenges for temporary bonding materials. One of the main challenges is maintaining device positioning in all three dimensions (X, Y and Z) while at the same time mitigating stress that occurs during the many processing steps required to create a final product.

Temporary bonding materials must deal with high amounts of stress and widely varying process temperatures, all while maintaining wafer geometry, which means reducing bow and warp so it falls within small tolerance ranges.

According to Kimberly Yess, Executive Director within the Brewer Science WLP Materials Division, it was clear that for FOWLP technologies to advance, there was a need for more capable bonding solutions. New approaches were needed to maximize performance, simplify processes and help ensure minimal die shift.

In partnership with imec, a nanotechnology and advanced process research group headquartered in Leuven, Belgium, Brewer Science developed a new generation of temporary bonding solutions that significantly addressed the key objectives. The materials Brewer Science developed in concert with imec provide a range of previously unobtainable benefits, including nearly zero die shift (ZDS), all of which can be achieved using industry-standard equipment.

“The value of new materials in the ZDS process is that it allows for controlled die placement and less adaption of RDL alignment after mold. With correct placement and locking the dies in place, the manufacturing process is more flexible and forgiving to the stresses induced by the EMC. It also allows you to be able to extend the equipment used at the BEOL because of its reduced warp, making it compatible with tools already available,” Yess explained. She noted that when other materials are used to create FOWLP devices, warp and bow can be so pronounced that special BEOL tool sets have been needed to handle wafers that were distorted to the point that malformation could be seen, unaided, by the human eye.

When Brewer Science and imec set out to identify new materials and processing techniques and to test them using standard CMOS-compatible processing equipment, the key challenge was to mitigate the effects of over-molding assembled dies. Researchers are targeting an extremely high interconnect density and believe a 20-μm pitch is now achievable. The technology is highly attractive for mobile device applications since it enables cost-effective memory-to-logic high-density interconnects in a very small form factor. This paves the way for heterogeneous integration that targets high-performance applications.

Flip-chip on FOWLP typically utilizes a mold-first approach in which dies are first assembled on a temporary carrier that is followed by wafer over-molding. In the final step, the RDL is created and connections are made. Expanding on this approach, imec and Brewer Science have shown multi-stacking of chips are efficiently linked using silicon bridges

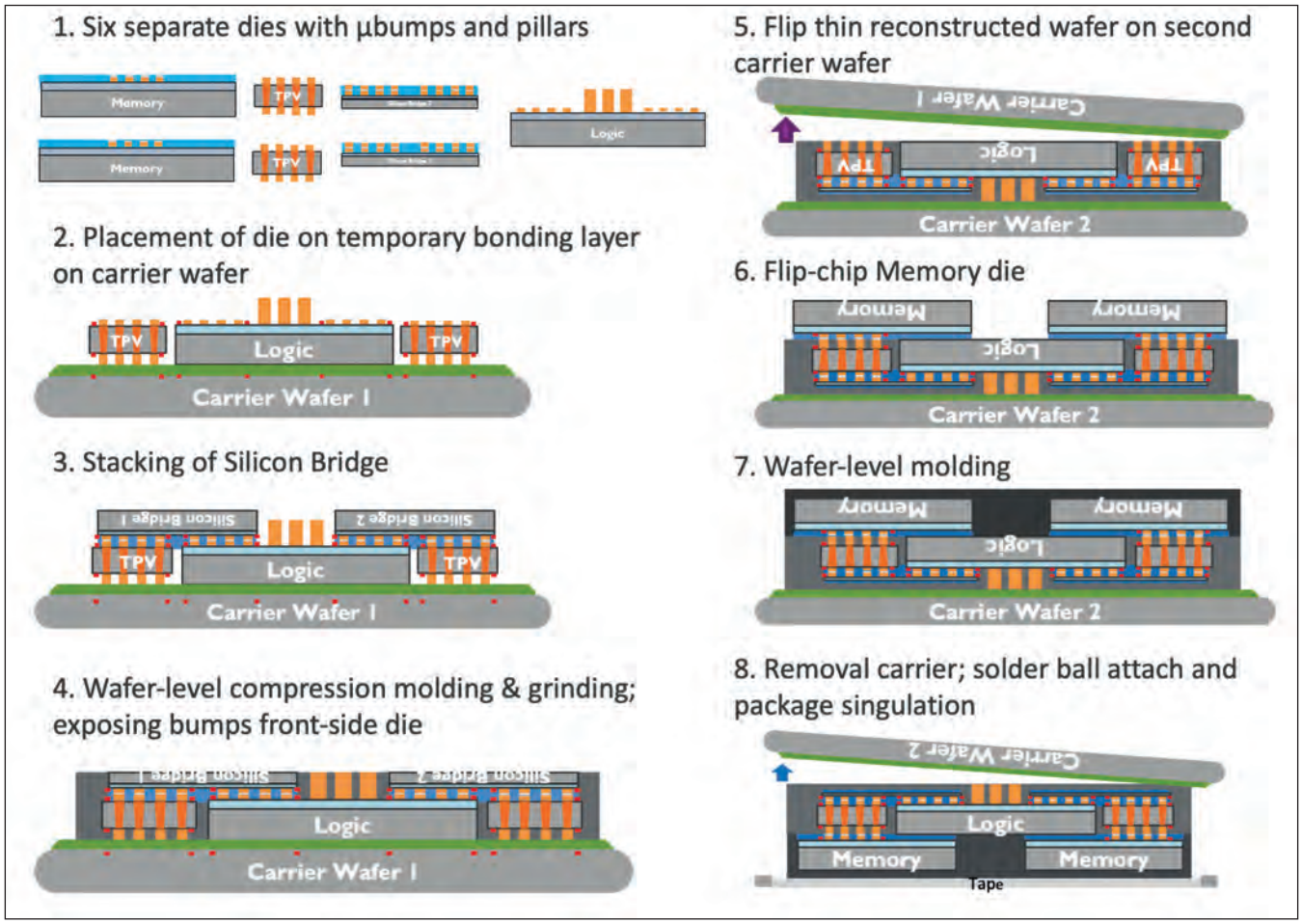


Figure 1: Process Flow Diagram

and through package vias (TPVs) in a two-step molding flow. The feasibility of this approach was first demonstrated using dummy components and is being validated with 'active' dies in subsequent experiments. (See Figure 1: Process Flow Diagram, which illustrates key research goals and findings described in: "Novel Temporary Bonding and Debonding Solutions Enabling an Ultrahigh Interconnect Density FOWLP Structure Assembly with Quasi-Zero Die Shift", Podpod, et al., 68th ECTC, 2018)

The concept that is being developed at imec has multiple steps. The first step is to coat a carrier wafer with a temporary bonding layer (BrewerBOND® C1301 material) and then place the through-package via and logic dies on top. Next, the silicon bridge is attached using thermocompression bonding (TCB). The wafer is subsequently over-molded with an epoxy mold compound.

Following this step the copper pillars are exposed by grinding the mold. After flipping the reconstructed wafer to a second carrier, the first carrier is removed and the memory dies are assembled using a flip-chip technology. A second, wafer-level molding follows; the removal of the second carrier completes this phase of the process flow. The resulting complete package is 300-400 µm thick (excluding solder balls.)

From a materials perspective, it is worth noting that throughout this assembly and processing flow, two temporary carrier substrates are utilized. Success of the entire process is greatly determined by the specific characteristics of the materials coated on the carriers, chiefly: the temporary bonding materials and the release material needed for efficient debonding.

The principal role of the first carrier is to assemble chips with extremely high inter-die alignment: +/- 3 µm, which is needed to allow for the 20-µm bump pitches. To achieve such high accuracy, alignment marks are used in both the carrier and the dies. For these marks to be useful in achieving tight alignment, they have to be visible, which means the first adhesive material must be sufficiently transparent so that precise, automated alignment can occur.

Another key requirement is that the various dies comprising the assembly need to be placed at room temperature, and for a very important reason: limiting or sharply curtailing thermal expansion. Limiting thermal expansion helps enable much more precise die-to-carrier alignment. However, the adhesive also needs to withstand high temperatures during subsequent TCB die-to-wafer bonding steps.

The material must also be able to maintain highly

accurate die placement during the wafer over-molding step that involves heat and force. Finally, to further raise the bar, the adhesive should also allow debonding from the first carrier and be effectively cleaned to reveal the embedded dies for the following process steps.

The second carrier's chief purpose is to enable the removal of the first carrier system without adversely damaging the thinned mold and embedded dies. When it is removed, the front side of the devices can be accessed for testing and further processing by TCB and over-mold.

A major requirement for the second carrier is to enable selective removal of the first carrier without creating die shift, damaging the reconstructed wafer or increasing overall warpage. The adhesive in this case must have very good adhesion to mold and the second carrier while maintaining the ability to debond at the final steps.

The 'enemies' of successful flip-chip FOWLP are die shift, wafer warp and bow. The degree to which dies might move or a wafer could be deformed can also be influenced by the mold material and over-molding techniques that a manufacturer might employ. The initial over-molding takes place after the silicon bridge is placed; the second occurs after the memory dies are attached by flip-chipping them into place. The right choice of temporary bonding and mold materials (and the processes used to apply them) are key to avoiding die shift or wafer distortion after molding.

Imec constructed a number of experiments to evaluate different carrier systems, temporary bonding agents and mold materials. On test blanket wafers, researchers noted that dies maintained their placement accuracy with less than 2 μm shift for both granular and liquid materials. This was true even after exposure to temperatures of 200° C for two hours. Researchers also noted that extremely low warpage of less than 200 μm was achieved across the entire 300-mm wafer.

These experiments demonstrated warpage values far below those reported in literature. For example, warp is typically on the order of millimeters to centimeters - you can measure it with a ruler. However, with advanced bonding materials and advanced mold materials, warp is reported on the micron scale.

Just as temporary bonding materials and over-molding materials are essential to successful flip-chip FOWLP processing, so is efficient debonding for carrier systems. In the case of carrier one, it was found that mechanical debonding was most successful and did not impact the second bonding process. A laser-assisted debonding process was found to be most effective for successfully debonding the second carrier since it aided selective debonding.

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Conclusion

Imec's development of an innovative new approach to flip-chip FOWLP technology shows a path forward to reducing warp and bow in high density interconnect packaging that also demonstrates a way to help ensure dramatically reduced die shift. The Brewer Science temporary bonding adhesive, Brewer Bond® C1301 material, plays an essential role as a key enabler of these advances. The fact that the process, paired with essential new materials science, has produced very low warpage is key to processing over-molded substrates in standard manufacturing equipment.

The need for specialized process tools designed to handle reconstructed wafers that exhibit significant warpage can be eliminated. The fact the temporary bonding agent is designed for application at room temperature while still being able to sustain stability at temperatures up to 200° C for two hours is a significant milestone. Fine pitch RDLs in combination with a chip-first will pave the way for a wide range of applications, especially those in which the end goal is high density I/Os.

Ultrahigh purity valves can help optimize thin film deposition

As the semiconductor industry continues to change rapidly, tool manufacturers must keep pace as well. To help optimize thin film processes, new ultrahigh purity (UHP) atomic layer deposition (ALD) valves can enable total thermal immersibility and much higher flow rates than current valves. According to the experts at Swagelok Company, these qualities can enhance chip manufacturing efficiency and reliability while also enabling new process and media innovation.

BY MATT FERRARO, PRODUCT MANAGER, SEMICONDUCTOR, SWAGELOK

PRESSURE to keep up with competitors and rapidly advancing technology requirements means that chip fabricators do not have much room for mistakes in their manufacturing processes. After all, manufacturing wafers that ultimately become highly advanced chips requires perfect precision in intricate and involved processes using expensive materials, corrosive gases, and extreme temperatures. In short, it is not an easy business.

As a result, the market is equally complex for companies that supply chip fabricators with the components and tools they need to produce advanced semiconductors. Like their customers, suppliers are pushed to upgrade their products consistently to enable greater precision and efficiencies. Chip fabricators are demanding tools that allow them to produce more product in less time without adversely affecting quality. In addition, suppliers are expected to see into the future and develop technologies that will help fabricators optimize their processes and experiment with different inputs (such as new precursor gases) as they develop the next generation in chip technology.

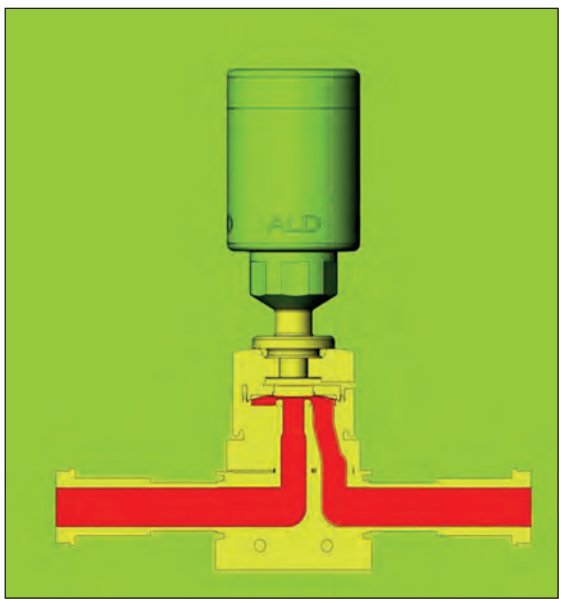


Figure 1. Thermal isolation in traditional ALD valves can cause temperature discrepancies – represented by color variations here – between different valve components. Transmitted gases may therefore cool, leading to unexpected variables that may impact the process.

"Semiconductor chip fabricators tell the tool original equipment manufacturers (OEMs) what they want to achieve as far as chip performance and what production processes that will likely require," says Carl White, an industry analyst and principal engineering consultant at C.L. White Engineering Services, LLC. "This collaboration is critical if semiconductor companies are going to keep up with the speed of innovation, as it helps OEMs receive the components they need today, and it helps the component manufacturers anticipate the future needs of the industry."

Since semiconductor manufacturers have put a premium on atomic layer deposition (ALD) processes, ultrahigh purity (UHP) valves are equally vital. ALD UHP valves enable precise dosing of gases during the semiconductor wafer manufacturing deposition process. Although relatively small components, the valves have an outsized effect on the successful creation of chips.

UHP valves for ALD processes are state-of-the-art, offering levels of precision and cycle life as high as just about any valve. But recently, fabricators have been searching for even higher performing valves

with greater thermal stability and flow capacities to enhance current manufacturing capabilities and pursue new processes. If the semiconductor industry wants to keep innovation and productivity moving forward, it is clear ALD valves need to evolve in three ways:

1. Thermal Stability
In the ALD process, UHP valves are sometimes heated to elevated temperatures to prevent low-vapor-pressure gases from solidifying before reaching the wafer. To maintain their proper function, actuators on current UHP diaphragm valves must be thermally isolated by not being fully immersed in the high-temperature environment. Unfortunately, this results in a temperature difference between components in the valve itself. As seen in Figure 1 (with different colors representing varying temperatures), this means transmitted gases can cool.

2. Flow Rate
Flow capacity presents another significant challenge for semiconductor tool OEMs and fabricators. Currently, UHP valves used in ALD processes have limited flow capacities because the rates plummet when the valves are heated, and the required footprint does not allow the valve to increase significantly in size. Improving flow capacities of UHP valves could also accelerate the rate at which fabricators can manufacture semiconductor wafers or at least give them a greater ability to ensure precursor gas stability. Such improvements could also increase revenues for fabricators.

3. Ability to Experiment
Semiconductor manufacturing is not a static process. Challenges abound, so manufacturers must be allowed to try new processes and media to maintain competitive advantages well into the future.

A single solution to three challenges

Addressing emerging industry needs, a new generation of ALD valves – such as the recently released Swagelok® ALD20 UHP valve (Figure 2) – has come to the market, promising to outshine previous iterations and provide a bright future for chip fabrication. The new valves address all three evolutionary needs:

1. Total Thermal Immersibility
Since consistency is critical in chip manufacturing, the new valves provide a lower risk of buildup or deposition variations than their older ALD counterparts. The new ALD valve design no longer requires the actuator to be isolated to maintain its integrity or dosing precision, permitting the entire valve to tolerate heat up to 200˚C (392˚F). As a result, chip fabricators can be assured that precursor gas temperature variability will be reduced or eliminated entirely. Figure 3 shows what an ideal state of thermal stability looks like, as opposed to Figure 1 with its varied temperatures.

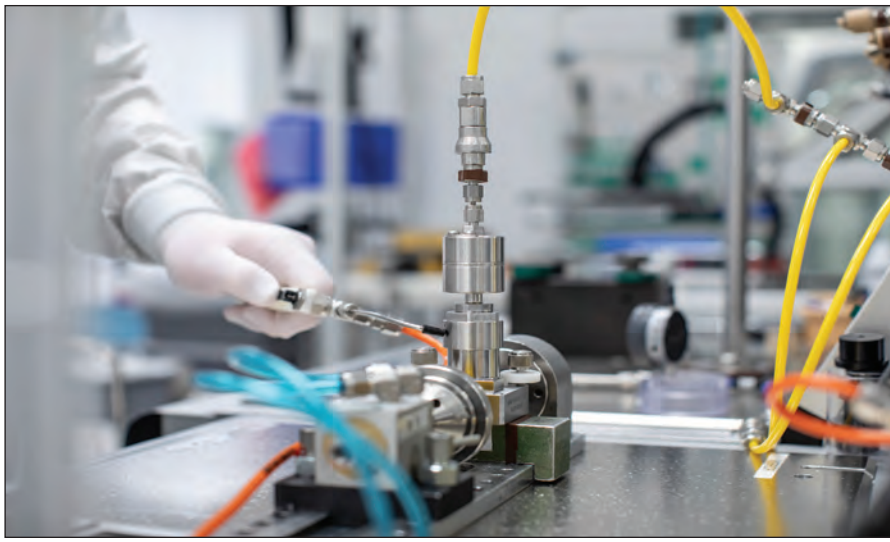


Figure 2. Advanced UHP ALD valve designs like that found in the Swagelok ALD20 UHP valve are enabling greater thermal stability, higher flow rates, and increased innovation in semiconductor wafer manufacturing.

2. Much higher flow rates
In addition to delivering better thermal stability, new valves can provide chip fabricators with the ability to increase flow rates without negatively affecting cleanliness or component longevity. Current valves might provide a 0.6 Cv flow coefficient, but a new valve like the ALD20 can offer double that at 1.2 Cv – without increasing the size of the valve from its normal 1.5-inch footprint. This higher flow rate means tool manufacturers can increase output without retooling or significantly changing their processes. To further increase flow rates, a chip manufacturer also has the option to use new ALD valves with a slightly larger footprint of 1.75 inches. The larger valves enable manufacturers to achieve flow coefficients up to 1.7 Cv, which is nearly triple that of today's common ALD valves.

The reason for these significant flow rate advances is that this new type of ALD valve features a bellows

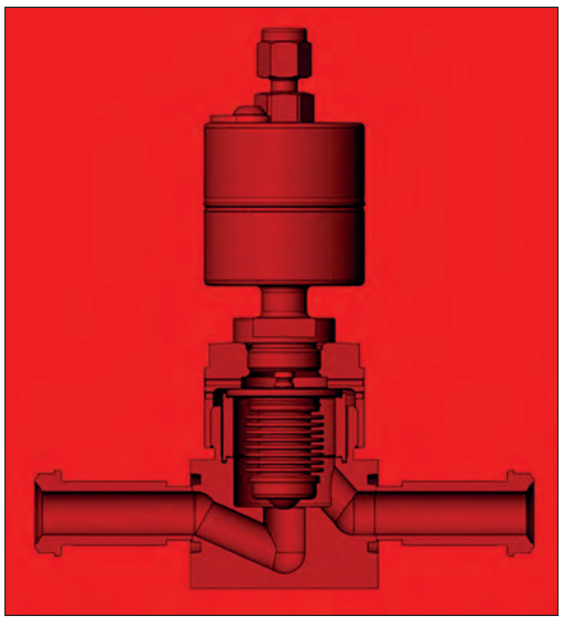


Figure 3. This setup shows an ideal state of thermal stability, as compared to the varied temperatures that may occur in the Figure 1 design.

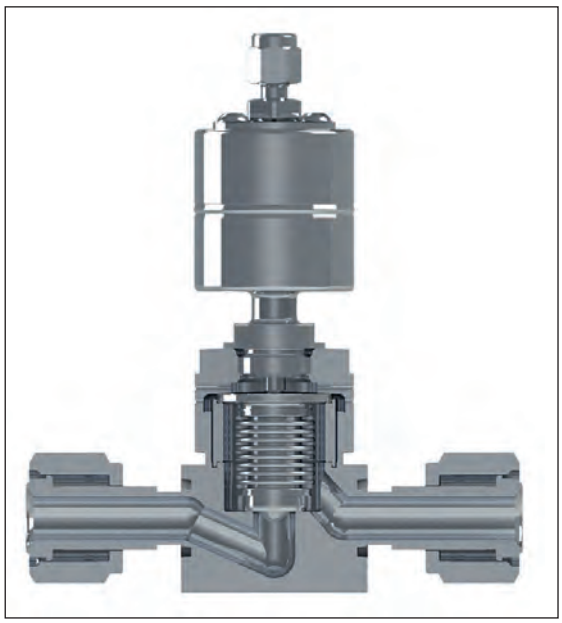


Figure 4. The bellows design of this UHP ALD valve enables higher flow rates to accelerate chip production.

design (see the center of the valve in Figure 4) instead of a traditional diaphragm design. Bellows valves are naturally capable of higher flow rates. The bellows inside the new ALD20 valve is polished to a 5 μin Ra finish, allowing the valve to mirror the UHP performance that chip fabricators expect from the current diaphragm valves. These new designs have revolutionized the industry by providing the best features of both valve technologies in one UHP valve that has an ultrahigh cycle life.

"Now, we are seeing the benefit of the high flow capacity that comes from a bellows valve that still offers the ultrahigh purity performance needed in modern semiconductor manufacturing," said White. "This was made possible in part because manufacturing techniques have improved over time, and because we also have access to enhanced materials – high-quality VIM-VAR steel and corrosion-resistant alloys, for example. There are also better finishing techniques being employed, like electropolishing and passivation, as well as better testing before product launches than there used to be."

3. Enhanced Innovation Opportunities

Practically speaking, these advances in ALD valve technology mean chip fabricators will no longer be hampered when they try to innovate. For example, new ALD valves combine the performance and durability necessary for manufacturers to experiment with new areas of the periodic table by using low vapor pressure precursor gases. This development could lead to breakthroughs in use of better-performing inputs than what are currently used in ALD processes. In addition to keeping temperatures consistent and enabling higher flow rates, new ALD valves are available in highly corrosion-resistant materials like Alloy 22. Such materials allow manufacturers to use more aggressive chemistries without worrying about problematic pitting or crevice corrosion.

Meeting new industry demands

The latest ALD UHP valves could revolutionize the market because they provide chip fabricators with the ability to ensure high-quality depositions with enhanced process efficiency and new experimentation capabilities. While these advances are significant, they will not change the fact that the semiconductor industry will remain subject to rapidly shifting demands within a competitive environment. Component manufacturers will need to continue to stand up to these emerging challenges with high-quality manufacturing of their own.

Virtual Customer Service in the Time of COVID-19

SWAGELOK believes the best way to prepare for any business challenge is to consistently anticipate better ways of identifying and meeting customer needs. The company recognized that its ability to responsively deploy technical expertise remotely is critically important to its semiconductor customers around the world. The global pandemic presented an opportunity to sharpen these types of capabilities to solve technical issues virtually rather than on-site. The result is added efficiency, agility, and collaboration through virtual customer connectivity.

The Swagelok virtual customer services offering has already been deployed to fluid system customers in key industry segments such as Oil & Gas and Chemical & Refining in countries around the globe. The company is expanding this virtual customer service offering to the semiconductor segment, delivering field services that include remote evaluation and advice, as well as fluid system troubleshooting and commissioning at their facilities.

The benefits of virtual customer service visits include:

- Real-time collaboration with a complete, cross-functional team of Swagelok fluid system experts
- Increased agility and responsiveness to issues
- Enhanced safety
- Reduced time and travel costs

Swagelok provides customers with headsets that enable two-way video and audio sharing. Since the Microsoft Teams-enabled system is hands-free and voice-controlled, customers can easily navigate their facility on-site, take notes, and continue to work throughout the virtual visit. Finally, virtual customer service allows Swagelok to provide remote assistance from an expert team, enabling better overall problem-solving capabilities for quicker evaluations and solutions.

Industry counts on SEMI standards.

SEMI is the global industry association serving the product design and manufacturing chain for the electronics industry.

Check out our new standards on SMT & PCB Manufacturing Equipment Communication, Panel Level Packaging & Energetic Materials at:

www.semi.org/collaborate/standards

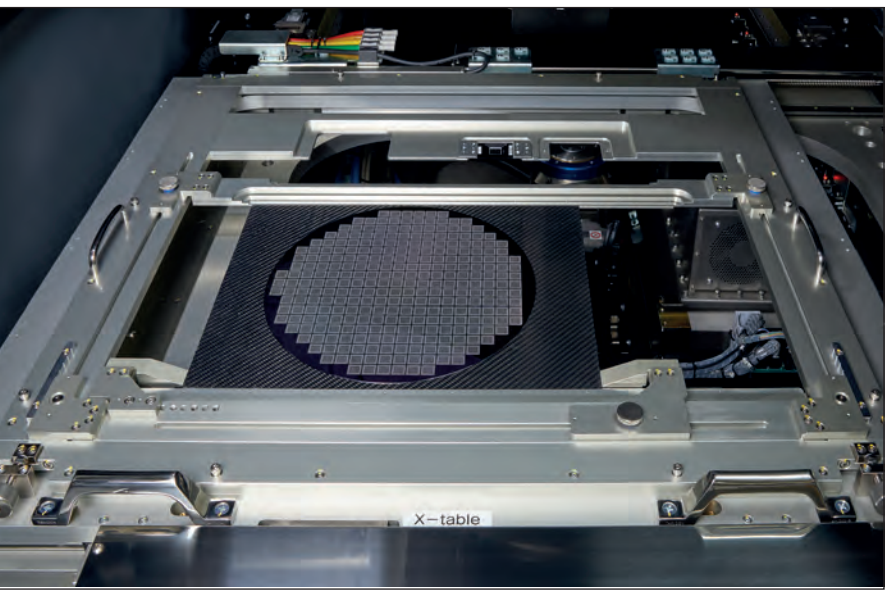
YXLON

The perfect solution for high-volume, automated and reliable 3D semiconductor solder joint analysis

Semiconductor manufacturing requires automated, high-quality, reliable, fast, and non-destructive inspection and analysis for an optimum production since defects can be found on the wafer, on a substrate, on a strip, or in the subassembly of a final device.

THE NEW X-RAY inspection system YXLON FF65 CL has especially been designed to provide the best automatic analysis of the smallest and most demanding features within the 3D IC, MEMS, and sensors. The result: impressively precise and reproducible test and inspection excellence.

The FF65 CL uses 2D and 3D x-ray techniques that are based on the proven open nano-focus x-ray sources with high-power targets, the latest generation of optimized high-resolution x-ray detectors, and a high-precision, fully automated manipulation system. Collectively, these leading-edge components make the FF65 CL the perfect solution for the automatic analysis of bumps, flat solder connections, and filled vias to easily and reproducibly find non-wetted bumps, voiding, and misalignments.



The YXLON FF65 CL distinguishes itself by its large inspection area of 510 x 610 mm and the detectability of < 300 nm, making it ideal for automatically and non-destructively analyzing solder bumps and filled vias such as through-silicon vias (TSV) in 3D ICs, flip chips, and wafers. The innovative vacuum mechanism of the system manipulator holds the sample securely and precisely during analysis and counteracts the effects of sample warpages.

The FF65 CL provides 2D (top-down) radioscopy with a high-performance flat-panel detector and 3D (CL – Computed Laminography) automated analysis using a high-resolution image intensifier within a special manipulation assembly for its inclined rotations. The latest generation of nano-focus x-ray tubes creates 2D and 3D images that can reveal and measure the smallest voids and features, allowing the YXLON FF65 CL to analyze the most demanding advanced semiconductor challenges.

A user-friendly and intuitive graphical user interface (GUI) allows the easy creation of automated, multi-point, and multi-functional analysis inspection programs. Measurement repeatability over time is ensured by automatic, continuously monitoring background calibration tests over all aspects of the system.

As the market leader for digital radioscopy (DR), computed laminography (CL), and computed tomography (CT) inspection systems in the electronics industry, Yxlon is continuously innovating and providing solutions precisely where they are needed. The YXLON FF65 CL pursues this tradition to ensure that the Semiconductor industry is completely supported for today's and tomorrow's manufacturing challenges. Our global, interlinked, service network

with seven regional service centers and more than 50 local partners is prepared to quickly and efficiently support and help our customers to ensure the highest quality and minimum downtimes.

Yxlon's roots go back to the discovery of x-rays in 1895 by W.C. Röntgen and the production of the first x-ray tube in 1896 by C.H.F. Müller. Founded in 1998, our name stands for the non-destructive quality assurance of electrical and electronic components and assemblies, all types of castings and different materials, additive manufacturing, wheels and tires, welds, and much more in production, research, and development.

Our microfocus x-ray (DR) and CT systems meet the individual requirements for safe, reliable, and cost-saving testing of electronic, microelectronic, and electromechanical products, both in the SMT and semiconductor area.

X-ray is the most reliable technology for detecting cracks, open solder joints or cavities, measuring pores, and evaluating their distribution. Inspections can be performed manually, semi-automatically, or fully automatically and provide valuable information about the manufacturing process. As an additional sensor and through the transfer of extensive data sets, x-ray systems are considered an important part of the modern Smart Factory.

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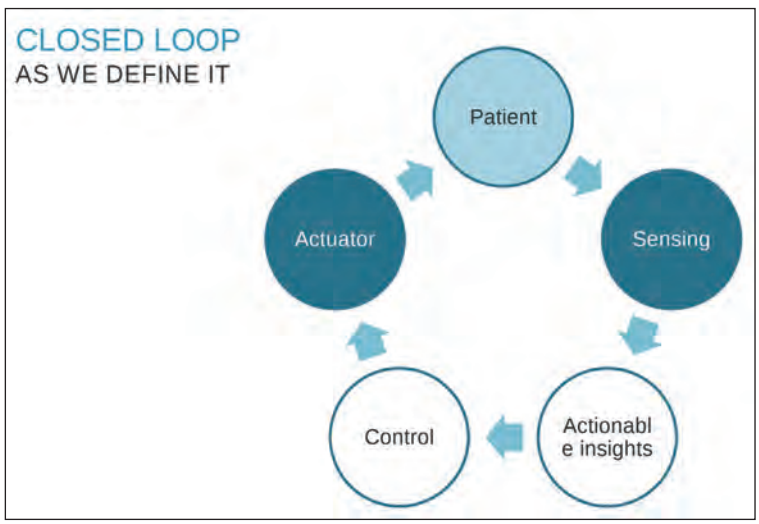
From wearables to 'careables': Closing the loop in connected health

What if we could combine vital sign sensing capabilities with smart algorithms and actuation features in order to not only diagnose but also 'fix' a problem in the body? Just like a pacemaker does today, a multitude of closed-loop systems will help us in the future. **Vojkan Mihajlovic, senior researcher, and Evelien Hermeling, principal scientist at imec**, share their vision on how closed-loop systems, consisting of wearables, implantables, invisibles and smart algorithms, will transform healthcare.

THE BEST-KNOWN EXAMPLE of an autonomous and closed-loop therapy device is a pacemaker. Second in line, although not yet commercially available, are intelligent insulin pumps. With artificial intelligence, and miniaturized sensors and actuators, the ingredients are there to shape a future with a multitude of closed-loop systems for remote, preventive and curative healthcare.

Think of medical-grade wearables measuring blood pressure and assisting in finding the right dose of blood pressure-regulating medicine. Think of small implants that stimulate specific nerves based on biomarkers for migraine sensed in real time. Or think of invisibly integrated sensors in (car) seats and office chairs to access the breathing capacity of lung patients and advise them on their fitness program.



Key building blocks of a closed-loop therapy system. The dark blue circles are typically hardware components, while the white-colored blocks are mainly software modules.

From pacemakers to anesthesia

If you Google 'closed loop in healthcare' you immediately get thousands of hits on the artificial pancreas. **Evelien Hermeling:** "In fact, the evolution of diabetes care is ideal to illustrate what a closed-loop therapy system is. Patients moved from finger pricks and insulin pens to glucose monitors on their abdomen or upper arm that measure continuously and send alarms to their cellphones."

"More advanced systems today (such as the Minimed 670G Insulin Pump System of Medtronic) go one step further and add a small wearable computer to the continuous glucose monitor. That computer captures the data, calculates how much insulin is needed and sends this info to the insulin pump that is also attached to the patient's abdomen. In this way, blood sugar remains steady day and night, automatically. That vision is pursued for other diseases as well to make the lives of patients healthier and more comfortable. The artificial kidney for dialysis patients is another typical example, although still far in the future. Imec, together with leading research organizations in the field, has and will continue to work on a roadmap to make such an artificial kidney a reality."

It is also forecasted that for other chronic or acute conditions, next-generation treatments will no longer

be restricted to chemical medications alone. Doctors might soon be able to prescribe drug treatments in combination with devices that monitor the effect of the drug or suggest changes in its dosage (medically known as titration process). These kinds of treatments are known as drug-device combinations.

Vojkan Mihajlovic: "Also for doctors, closed-loop systems are there to make life easier. Think of a closed-loop system for anesthesia: the anesthesiologist sets a target blood pressure and the system automatically maintains this target by dosing the appropriate medication. This allows specialists to focus on the patient and relieves them from repetitive, automatable tasks."

Compose your future closed-loop therapy system

With the advent of miniaturized, wireless, reliable sensor and actuator systems, and artificial intelligence for interpretation of the data, the time has come to fully invest – both money and brains – in new systems that are smarter and more autonomous when it comes to keeping an eye on patient's health.

Evelien Hermeling: "A typical closed-loop system is made up of different key parts, each with its specific requirements. The sensing part measures one or more parameters of the patient's body, such as heart rate, ECG, blood pressure etc. Sensors must be accurate, small, and able to wirelessly transmit their data to the cloud or a device in the patient's vicinity."

"Next, a small processing unit is needed, executing algorithms that can interpret these sensor data into actionable insights. Depending on the use cases, time constraints need to be considered. For example, a heartbeat needs to be acted upon immediately (as with a pacemaker), while blood pressure is known to take time to change and here it is more important to watch a trend over a few hours or even days. Also, personalization is key. 50 beats/minute may be a normal resting heart rate for one person and an abnormally low heart rate for someone else. Algorithms need to add this kind of intelligence to the system so that useful and accurate actionable insights can be deducted from the sensor data. Next to time constraints and personalization, contextual and environmental parameters also need to be considered. Blood-pressure-lowering drugs, optimally titrated to a person for an average day, might cause the blood pressure to drop during hot weather. This can be a dangerous situation that needs to be corrected. Algorithms would be able to adjust the doses, taking such contextual and environmental parameters into account."

"A third building block is the control algorithm that translates the insights into a control action. For example, too much fluid buildup in the body can result in an increased medication dosage for a patient. Again, personalization and time constraints

Closed-loop therapy devices can take on many forms. Think for example of medical-grade wearables measuring blood pressure and assisting in finding the right dose of blood pressure-regulating medicine.

are key here. Imagine you are dealing with diuretics (pills to help increase urine volume), then the control algorithm should accommodate that the body needs some time to get rid of the excessive fluids. Delivering a medicine in the bloodstream will not immediately change the fluid status."

"And the last part is the actuator hardware, e.g. the micropump delivering a drug into the blood stream, based on the instructions it received from the control algorithm. A small form factor, and accurate and timely operation are the most important features of this building block."

These closed-loop therapy systems can have many different form factors: wearables, implantables, invisibles. As **Vojkan Mihajlovic** notes: "Invisibles are sensors that are seamlessly integrated into the patient's environment. Think of sensors in a (car) seat, a car's dashboard, a mattress or even a toilet seat. While wearables and implantables measure continuously, invisibles only measure occasionally, which is sufficient for certain types of measurements. Think for example of a daily check of blood pressure, urine composition or lung capacity."

Imec has all the building blocks in-house

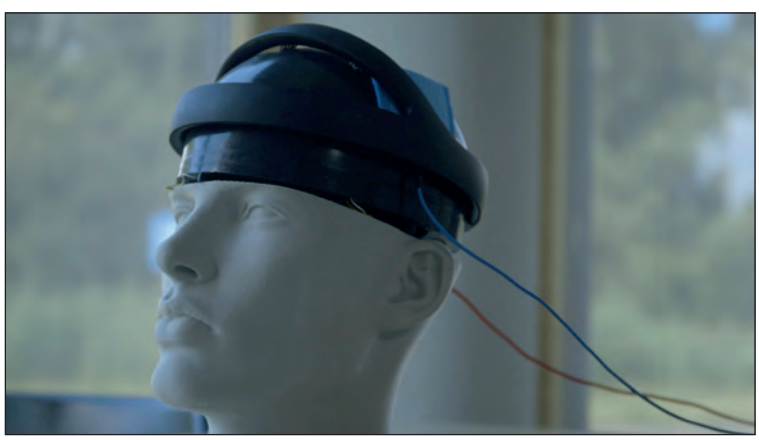
Imec is known for its work on miniaturization of electronics, which is researched in state-of-the-art cleanrooms. **Evelien Hermeling:** "Some 15 years ago, work started on making sensing systems for vital sign monitoring. This work resulted in collaborations with industry leaders such as Samsung and Biotelemetry, in a large study on stress monitoring

Imec's EEG headset research platform with optical and electrical modalities to both measure and stimulate brain activity. Possible applications are treatment of depression, migraine, and epilepsy. Imec looks for partners to work out a system for specific applications.

in real-life conditions, and in different prototype devices for measuring brain waves, eye movements, gait, sleep patterns, respiration, pain and stress, and general health parameters."

"The focus has been on making very compact, low-power and wireless sensor systems, with efficient data acquisition, using different modalities (activities of the heart, lungs, muscles or nerves) and integrating them in different form factors (watch, patch, headset, ...) We are now working towards expanding the efficient acquisition portion, with smart algorithms to provide actionable insights, and actuation principles to close the loop."

"We invest a lot of work into algorithm development for good interpretation of the collected sensor data and to ensure reliable data quality in real-life conditions and in uncontrolled environments. Also, algorithms allow the fusion of all available sensor data, from different kinds of sensors, in order to draw even more reliable conclusions." In another imec article, "Inhale the future: bringing respiratory monitoring to the 21st century" the use of algorithms (signal-level, digital-biomarker level and application-level) is further explained.



Imec's phantom head. It can be used in the development of closed-loop EEG and tCS applications, before doing trials on humans.

Vojkan Mihajlovic: "In the domain of actuation and stimulation, imec explores the possibilities of non-invasive brain stimulation (with its EEG headset) and electrical stimulation of nerves with small implantable nodes. Also, we are developing a general-purpose software framework that facilitates multimodal data acquisition, signal interpretation and specification of control rules required for optimal actuation. This framework links all these ingredients into a true closed-loop system. The development currently focuses on timing requirements and feedback/actuation modalities. Of course, imec looks for partners and users to complement this expertise, especially from the application side."

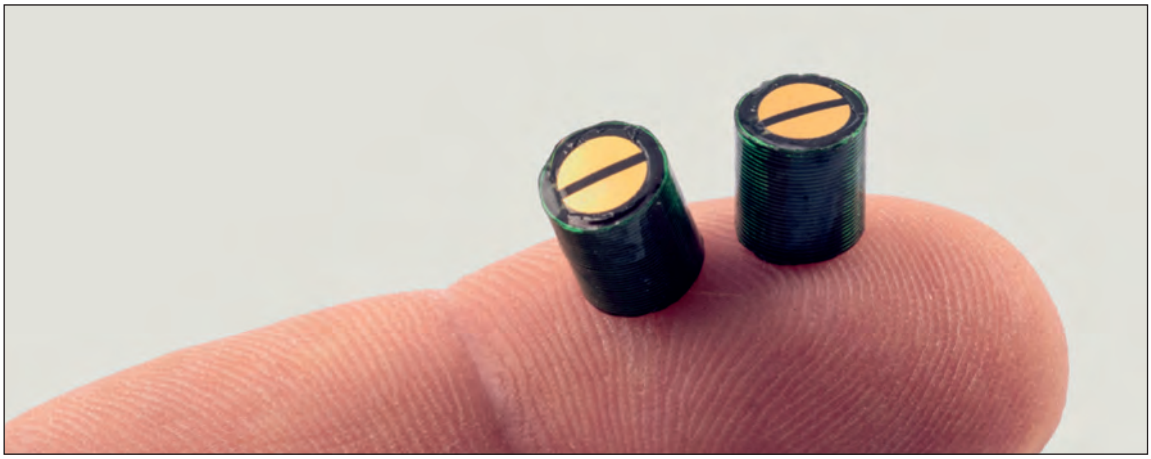
Below are 3 examples of work that imec has done over the years related to closed-loop systems. As said previously, closed-loop feedback systems can be embodied in multiple form factors, such as wearables, implantables and (non-contact) invisibles or combinations of these. For each of these form factors, we highlight one example. At imec, we specialize in using our knowledge and experience to solve customer-specific challenges, hence the following examples are meant as a source of inspiration. Each application requires different building blocks used in different manners.

A headset that combats depressions, migraines and more

Transcranial current stimulation (tCS) relies on injecting currents (a few mA) over the human scalp in order to modulate ongoing brain activity.
Vojkan Mihajlovic: "The applications for tCS are numerous, ranging from treatment of depression and migraine to epilepsy and anxiety disorders. In a closed-loop system, it is important to measure the brain waves while and after applying stimuli, such that the stimuli can be adapted to facilitate personalized treatment."

"Traditionally, the method involved two large electrodes placed at different locations on the scalp with current going from one electrode to the other. The electrodes were made of conductive polymer enclosed in a sponge-like housing, soaked in a saline solution. More recent approaches of tCS rely on a larger number of smaller (1 cm^2) electrodes. Imec developed EEG monitoring headsets with small dry electrodes (together with Datwyler). They are very easy to use and deliver high-quality measurements. Currently, such dry electrodes are being adapted for tCS.

For this application, imec also plans to extend the headset's capabilities with digital active electrodes, with both electrical and optical features. By using



Examples of implantable node sensors

two different modalities, it becomes possible to simultaneously measure and stimulate without interferences (e.g. electrical stimulation, optical sensing and vice versa).

Imec developed a phantom head to facilitate the exploration of safety aspects and the impact of tCS on head tissue. Also, it allows to optimize closed-loop brain monitoring and stimulation. This phantom head is the electrical equivalent of a human head consisting of different head tissue layers. It enables probing the current paths at different surface locations and tissue depths. Tests done using brain monitoring and tCS systems applied on the phantom head, along with simulated EEG signals (generated by using signal generators), are a steppingstone to closed-loop EEG & tCS trials in humans.

Small implantable nodes that tickle your nerves

Next to wearables, implanted devices can also do sensing and actuation of vital sign parameters as part of a closed-loop therapy system. **Vojkan Mihajlovic:** "An important field, with an enormous potential, is bioelectronic medicine, in which the central or peripheral nervous system is electrically stimulated. Stimulation can be done in the brain region, the spinal cord, or the Vagus, hypoglossal, phrenic, sacral or tibial nerves."

"In the brain, microneedles are the preferred form factor whereas tiny stimulation nodes placed next to nerves or miniaturized cuff electrodes wrapped around the nerve bundles, can be used in the rest of the body. Imec develops both neuroprobes and small stimulation nodes. With both form factors, the focus is on miniaturization and wireless powering and communication."

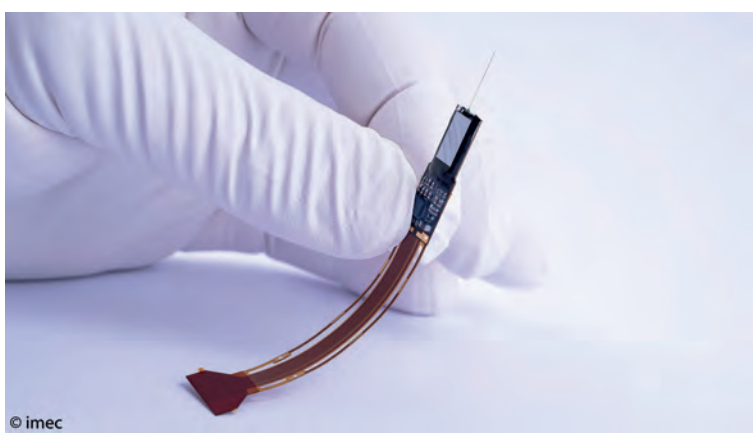
An important milestone in 2018 was the release of a neural microneedle probe, Neuropixels, to the global neuroscience research community. The probes were developed through an international collaboration funded by the Howard Hughes Medical Institute (HHMI), Wellcome Trust, Gatsby Charitable Foundation and Allen Institute for Brain Science and designed, developed and fabricated at imec, in collaboration with HHMI Janelia Research Campus, Allen Institute for Brain Science, and University College London.

The probes have almost a thousand electrodes and 384 recording channels on a single shank, providing an unprecedented resolution for mapping brain activity. Now, first steps are being taken in extending the Neuropixel platform towards stimulation.

Vojkan Mihajlovic: "Another example, with a different form factor, are the implantable stimulation and sensing nodes that we developed and that allow the stimulation of human tissue and at the same time capture impedance and temperature. They are powered and communicate using wireless protocols, hence they can be deployed in the human body for an extremely long time. You could also combine implantable nodes with wearable devices. Think, for example, of an external wearable sensor that measures heart rhythm, respiration or digestive activity from the skin surface. This would then communicate with the implanted neurostimulators that counteract any sensed abnormality."

Use the patient's environment to monitor vital signs

Next to, or in combination with wearables and implantables, one can also use sensors in the



Imec develops both microneedles and implantable nodes for electrical sensing and stimulation of nerve cells.

Capacitive sensors can be incorporated into an armchair, bed, office chair or car seat. Imec has developed a system that can support up to 64 sensors. If you want to use capacitive sensors to record respiration rates, it is important in practical applications to make a record of the reliability of the readings as well.

environment to monitor patient's vital signs, at specific moments of the day. Miniaturized sensors can be integrated in chairs, car seats, beds, toilets etc.

Evelien Hermeling: "Imec explores capacitive, optical and radar technology to do vital sign monitoring 'from a distance.' For example, in a car one could build sensors into the driver's seat, steering wheel and dashboard to measure respiration rate, blood pressure, heart rate and cardiac activity."

"As a demonstrator, we integrated capacitive sensors in an office chair and a car seat to carry out ECG readings and detect respiration rates through clothing. This principle is not new, but the technology has not been used before in practical applications because the quality of the readings was poor due to movements of the person in the chair."

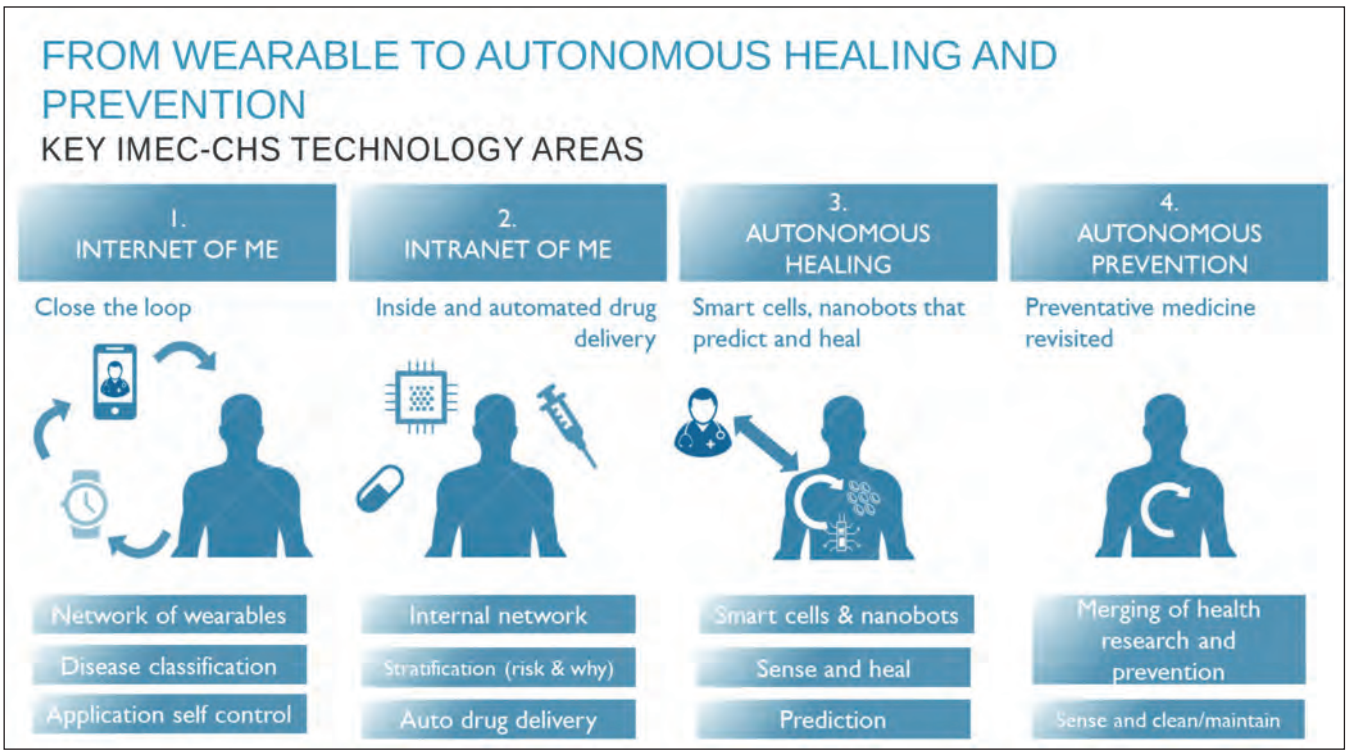
"The solution lies in the use of smart algorithms. First, algorithms can compensate for variations when movements and artifacts are detected, which makes the readings more reliable. Second, algorithms can make the system adaptive. This means that, in good conditions, an (ECG) signal of medical quality can be recorded. When conditions are not so good, the sensors switch to robust mode and take more general readings. For example, although you can still record the heart rate, obtaining an accurate ECG graph is not possible. This variable quality is factored into the readings and passed on as such – together with the results recorded."

Such sensing information could for instance be used as input to dynamically and automatically adapt the driving conditions and the level of self-steering of the car, or to generate actionable alarms. **Vojkan Mihajlovic:** "It's also possible to use wearables to capture how our senses react to different stimuli in the environment and use this info to adapt the environment. For example, we are collaborating with one of the largest South Korean cosmetics companies, Amorepacific, on capturing user reactions to different fragrances.

Based on this, a real-time selection of preferred fragrances is performed. Also, we are setting up a European project in which an avatar adapts its interaction with a real-life person to this person's emotional state. The possibilities are enormous."

Future vision: closing the loop with nanobots

Evelien Hermeling: "These are indeed some of the possible future applications of closed-loop therapy. At imec, we have a vision on how these closed-loop systems could evolve (see figure below). In the near future, we foresee a multitude of closed-loop therapy examples using wearables or sensors in the environment, communicating with (e.g. one's smartphone and doctor,) resulting in an action to be taken by the person (being monitored.) Image your smartwatch measuring your blood pressure and alerting you via your smartphone to take one extra pill."



Imec's future vision on the evolution of closed-loop therapy systems.

"In a next phase, the sensors and actuators could be implanted in the body, so the closed-loop system would be an integral part of the patient, regulating blood pressure, etc. We could think of 'nanobots' inside the body detecting certain abnormalities (e.g. atherosclerotic plaques inside blood vessels) and a doctor injecting some form of a smart cell to fix the problem. Or could this one day be executed in a completely autonomous way, giving a whole new meaning to preventive medicine? At imec, we like to think big, and lay out truly visionary roadmaps to inspire our researchers and to fuel the discussions with our partners."

Conclusion

Thanks to the miniaturization of sensors and actuators, and thanks to the enormous progress made in artificial intelligence and deep-learning algorithms, it becomes possible to close the loop on health: not only sensing vital signs but also interpreting the data, getting actionable insights, and triggering some action.

This leads the way to artificial organs, drug-device combinations, the targeted treatment of depression and chronic pain, and many other applications. Every closed-loop therapy system will look different and will rely on (a combination of) different form factors (wearable, implantable, invisible) and building blocks to find the perfect fit for a specific application.

Imec researches and develops the key building blocks for such a closed-loop therapy system of the future. Together with application and research partners, this technology can be translated into a tailored solution for specific patient conditions. Partner with us to shape this future!

About Vojkan Mihajlovic

Vojkan Mihajlovic is a senior researcher at imec. He received his PhD degree from the University of Twente, Enschede, The Netherlands and has worked as a senior scientist at Philips Research from 2006 to 2012. Since 2012 he has been working on system level and biomedical algorithms at imec. He has extensive experience and leads research activities in the area of wearable brain monitoring and noninvasive neuromodulation. He is also coordinating connected health solution innovation activities.

About Evelien Hermeling

Evelien Hermeling received her PhD degree in 2009 at the Maastricht University, the Netherlands. After a few years of post-doc at Maastricht University, she started as senior researcher at imec in 2015 and became principal scientist in 2019. Her drive is to bridge the gap between hardware, software, biomedical engineers and medical doctors. She is leading the competence team focused on biomedical algorithms and models within imec-Netherlands.

Auto makers must find memory technology's 'sweet spot' to deliver full vehicle autonomy

Auto makers and the driving public are pursuing greater levels of vehicle autonomy for wide-ranging safety and convenience issues. While many of today's vehicles offer one or more ADAS systems, memory capacity and speed will need to dramatically increase to enable full autonomy according to the experts at Rambus.

BY FRANK FERRO, SENIOR DIRECTOR OF PRODUCT MARKETING FOR MEMORY INTERFACE IP AT RAMBUS

THE MARKET for connected and autonomous vehicle (CAV) technologies is proving to be significant for the electronics sector. The UK's Centre for Connected & Autonomous vehicles estimates that by 2035, the global CAV technology market will be worth £63 billion. This research solely assessed the potential for the higher levels of driver assistance and automation, described as Advanced Driver Assistance Systems (ADAS) level 3 and above, which are not commonly found in vehicles at present.

What are ADAS Levels?

The automotive industry, regulators, and insurers have together adopted categories to classify the capabilities

of the different levels of driver assistance and automation. From level 0, where the vehicle is being driven by a human with no assistance, to level 5, where no human attention or intervention is required. In the current market, most vehicles operate at level 2 or below. Tesla's cars, widely lauded for their level of automation, and in many cases equipped with hardware to enable higher ADAS levels, typically operate at level 2 currently, or with enhanced features, at what is known as level 2+.

The 2018 Audi A8 is one of the few vehicles on the market with level 3 capabilities. When on roads with a central barrier, and operating at speeds below 60Km/h, its 'Traffic Jam Pilot' mode can take control. Level 4 systems that are not yet in the market can handle complex driving situations, such as road works, without driver intervention.

The system will take over driving and monitoring the entire driving environment. Looking further ahead to level 5, full driving automation, every human is a passenger. These vehicles will not need a steering wheel, nor brake or accelerator pedals.

Delivering fully autonomous vehicles is often linked to the roll-out of 5G technology, due to the huge bandwidth promised and the potential for low latency connectivity. While there will be many applications for 5G in Vehicle to Vehicle (V2V) and Vehicle to Everything (V2E) communication (for example: to manage traffic and share information on road conditions), driving functions such as steering and collision avoidance will have to be in-vehicle.

The real response required for driving safely will mean that even 5G latency levels would have risks attached if safety-critical driving functions were not in-vehicle, and with human lives at stake, network failure cannot be tolerated. On a lighter note, it would also be unacceptable for owners of autonomous vehicles to find that they cannot travel when there is no 5G signal. Hence, true autonomy must be independent of the need for connectivity.

If connectivity is not material to autonomy, what is?

The industry leaders running prototype autonomous vehicle trials are amassing real world data for refining control models. The work they have completed so far has illustrated that a key technical obstacle to achieving full autonomy is delivering the ability to rapidly process enough data, both for machine learning (ML) training and, once that training is done, for in-vehicle inference. With the length of vehicle design cycles, solving this bandwidth challenge is a real-world issue for automotive systems engineers today.

Dealing with ADAS complexity

There are complexities to accelerating both AI/ML training and inference for ADAS. In training, data centre-based systems must scale dramatically to provide the necessary bandwidth and capacity required by the exponential growth in the size and complexity of training models. For the embedded systems used for in-vehicle inference, scaling of capability has to happen within additional constraints of cost, size, and long-term reliability.

The size and complexity of embedded inference models grows significantly with each ADAS level, increasing the memory bandwidth required. A current level 2 ADAS system will process around 60 Gigabytes per second (GB/s). Moving to level 3 ADAS, with inputs from a sophisticated sensor suite, the system

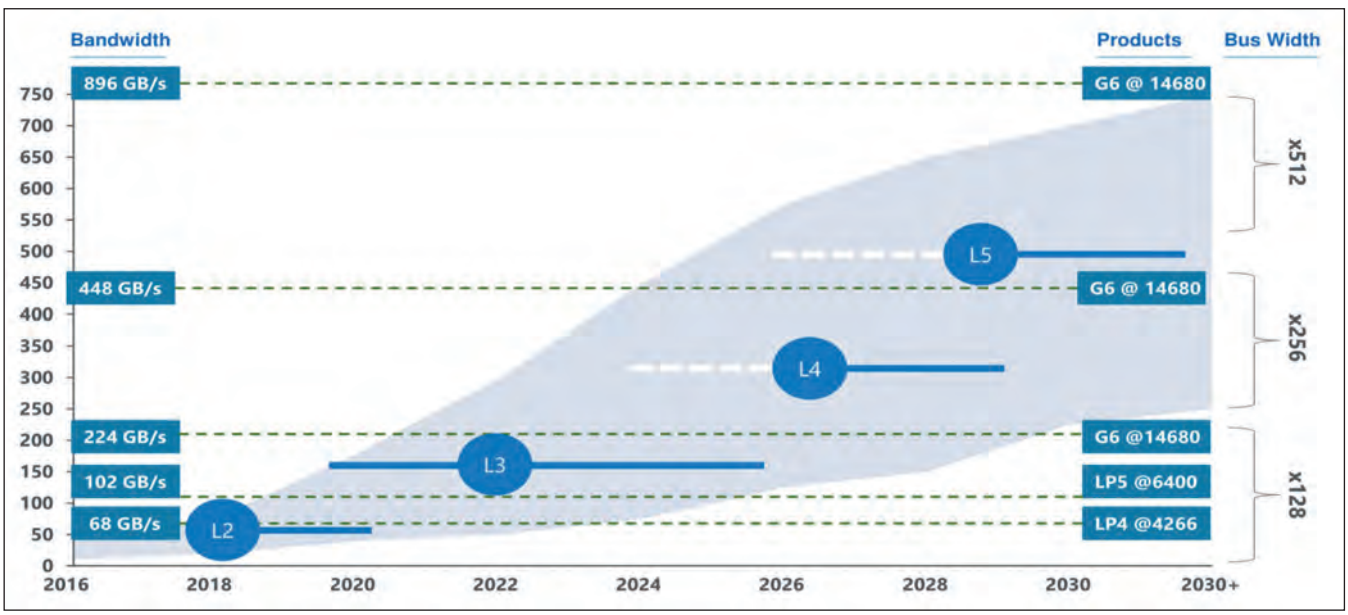


Figure 1 shows how predicted bandwidth demands rise significantly as ADAS capabilities increase.

Parameter	LPDDR4x	LPDDR5	DDR4	GDDR6
Bandwidth (GB/s) per device	Low-Medium (17)	Medium (25.6)	Medium (25.6)	High (64)
Data Rate (Gbps)	4.266	6.4	3.2	16
Interface width (bits)	32	32	64	32
Board Area / System design	Large/Medium	Large/Medium	Large/Easy	Medium/Medium
Efficiency (mW/Gbps)	High (3)	High (3)	Moderate (10)	Moderate (10)
Cost ($)	Medium	Medium	Low	Medium
Reliability / Yield	Good	Good	Good	Good

Table 1: Each memory architecture described in the table has its pros and cons. Source: Rambus

realistically needs memory bandwidth of at least 200 GB/s.

Below we explore memory options for meeting the requirements of level 3 ADAS. Delivering the real-time inference needed for level 5 autonomy will require complete optimisation of the memory-processor interfacing to maintain the necessary data throughput.

Memory choices

ADAS may be the ultimate ''IoT'' AI-inference application – after all, it is a system responsible for human safety and comfort. This has led designers to lean heavily on tried and tested memory architectures such as DDR4 – which over the years have successfully been used in laptops and desktop systems, as well as LPDDR, which has supported billions of mobile phone deployments, and also GDDR6, which has been deployed in hundreds of millions of graphics cards and game consoles.

Memory implementation at L3 ADAS, and beyond

Figure 2 provides options for memory system configurations capable of delivering level 3 ADAS implementation. Each implementation delivers 224 GB/s, meeting the level 3 requirement of 200 GB/s. With LPDDR4, 13 DRAM devices would be required, therefore demanding a large board and die area that poses practical challenges.

Selecting LPDDR5 simplifies the system; it requires nine DRAM devices to deliver 224 GB/s - making it potentially a pragmatic choice for low-end L3 ADAS. DDR4 with a 32-bit wide bus, which is not shown, would require double the number of devices as LPDDR5. GDDR6, with the highest per device bandwidth among these alternatives, delivers the required bandwidth using only four devices.

For level 4 ADAS, bandwidth requirements rise to 300 GB/s. In this case, an LPDDR5 design running at 6.4

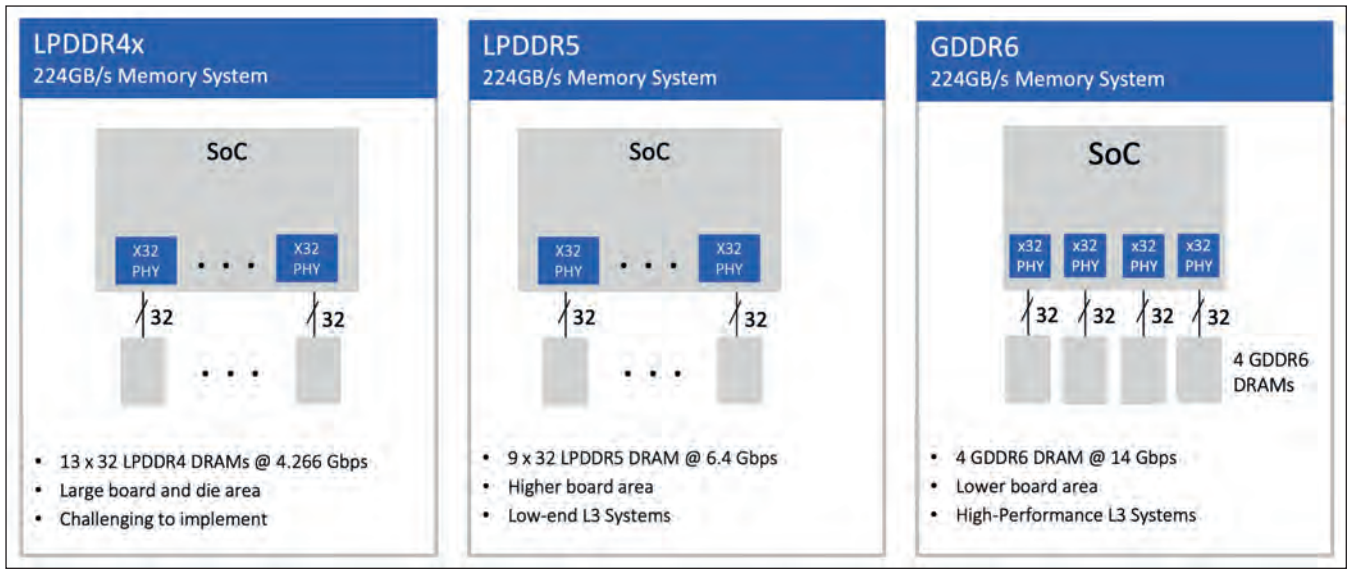


Figure 2: L3 ADAS Memory System Implementation Examples. Source: Rambus

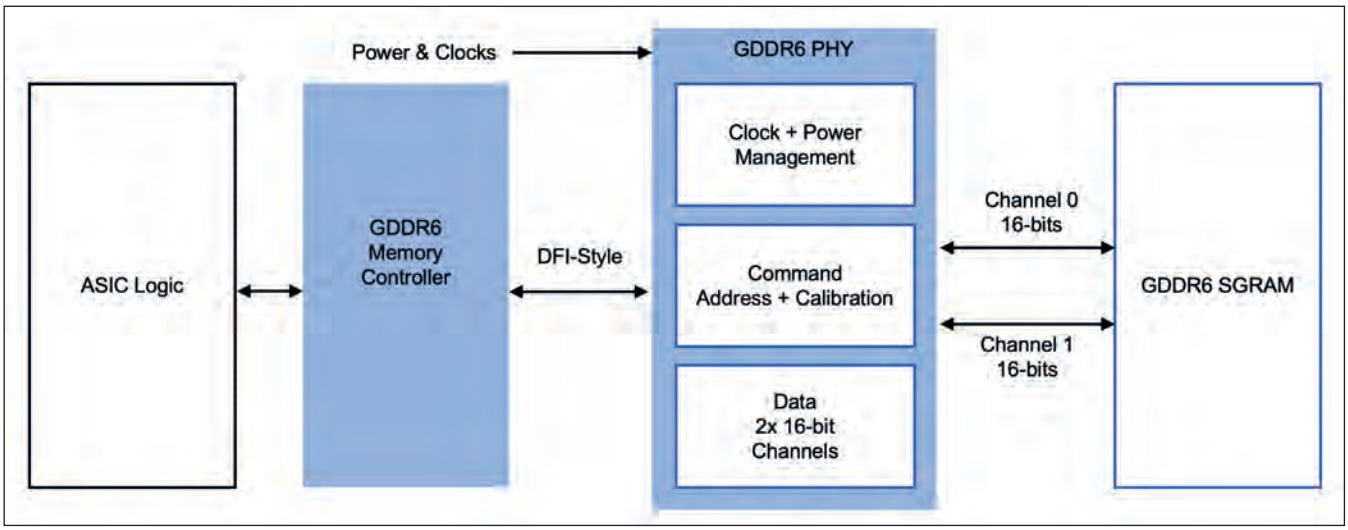


Figure 3: GDDR6 Memory Interface Subsystem Example. Source: Rambus

Gbps would require 12 DRAM devices. At this point the 'beachfront' of the SoC die would be dominated by memory interfaces, complicating the logic layout of the SoC and likely rendering both chip and board design impractical.

As bandwidth requirements increase to meet the inference demands of higher ADAS autonomy levels, GDDR6 becomes the optimal choice. GDDR6 running at 16 Gbps can supply over 300 GB/s of bandwidth using just five DRAM devices and with eight DRAM extends to deliver greater than 500 GB/s needed for level 5 autonomy. As well as excellent performance, GDDR6 is field-proven in volume, using standard manufacturing flows which makes it a great choice for in-vehicle AI inference.

Designing with GDDR6

The strength of GDDR6, which is its speed, is at the root of one of the key challenges in designing GDDR6 into SoCs for ADAS. Maintaining adequate signal integrity (SI) at 16 Gbps with a 1.35V operating voltage, in the mixed signal environment of the memory interface, requires expertise. The memory interface, package, and board require careful co-design to optimize the interactions between the different elements of the system to guarantee maximum system performance. The good news is that GDDR6 is an established technology with several suppliers of high-quality DRAM. These are complemented by a small pool of vendors offering 'off the shelf' memory subsystem designs. Rambus' silicon-proven memory subsystem for GDDR6 is rooted in decades of memory interface expertise, including for LPDDR4 and LDDR5. It can readily support the high bandwidth, low-latency requirements of ADAS inferencing, and is complete, comprising a fully co-verified GDDR6 PHY and memory controller, together with the engineering support to optimize the system-wide signal and power integrity (SI/PI) and the ASIC layout.

Having access to off the shelf intellectual property for memory processor interfacing has been demonstrated to significantly reduce time to market and design risk.

In conclusion, GDDR6 is currently the optimal fit for ADAS applications for present and future designs. It offers a sweet spot where bandwidth, capacity, power efficiency, reliability, and price-performance converge. In the key requirement of bandwidth, GDDR6 has the power to enable designers to reach ADAS level 5.

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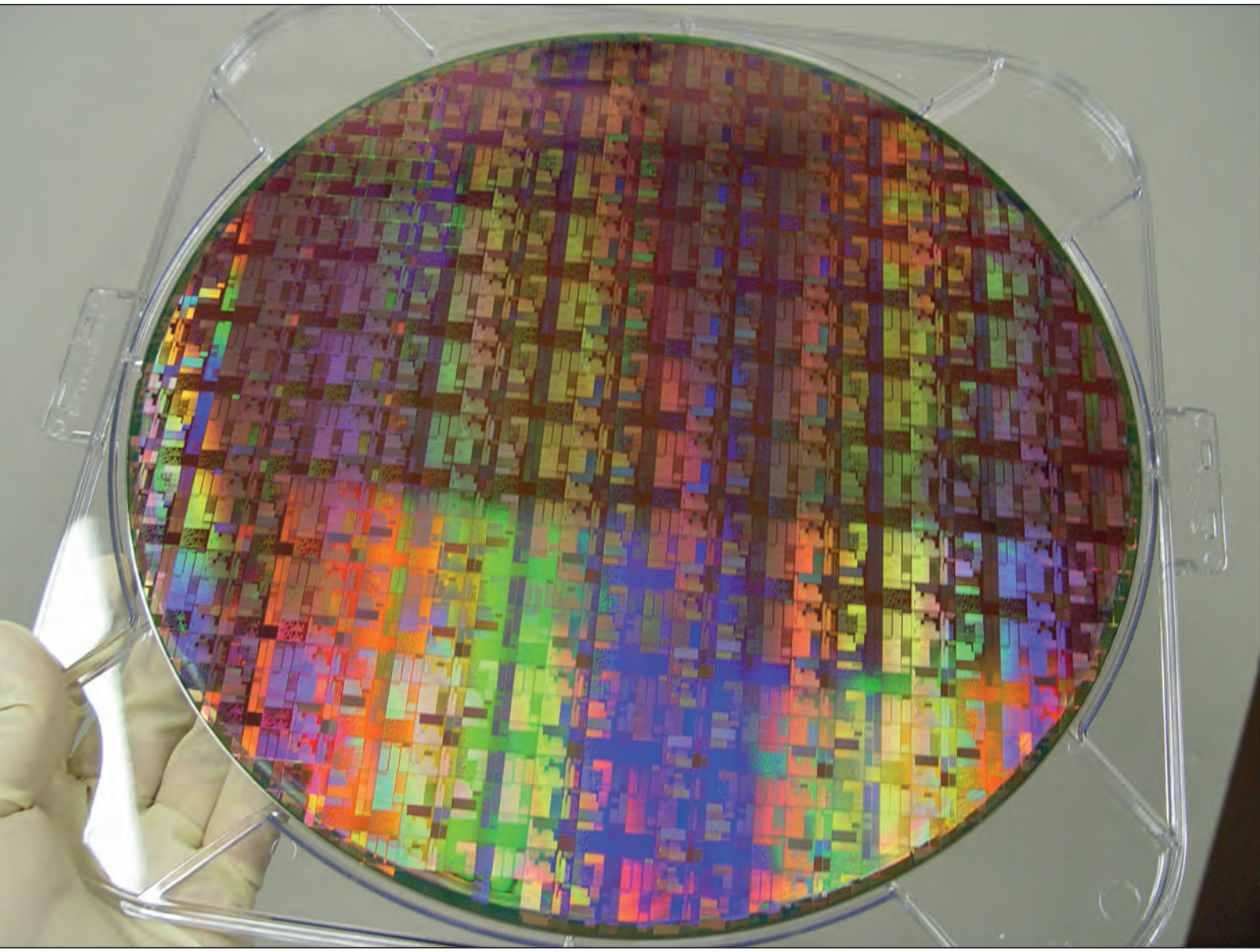

Stacking GaN and silicon transistors on 300 mm silicon

Next-generation mobile devices, data infrastructure and communication networks could be aided by three-dimensional, monolithic integration of GaN and silicon CMOS on 300 mm wafers

BY HAN WUI THEN FROM INTEL CORPORATION

THE TRANSITION to 5G and beyond is tipped to drive an exponential increase in the number of connected mobile devices. The integrated circuits that power them will need to provide greater energy efficiency, in a smaller form factor. Consequetly, there is much demand for more capable transistors and the integration of ever-larger numbers of components on the microchip.

Fulfilling these requirements is far from easy, as none of today's transistor technologies are capable of meeting the diverse needs associated with power delivery and RF front-end design. Due to this issue, circuit designers are combining many distinct, separate chips. This is not great, as it results in a bulky package.

To tackle this problem, our team at Intel's Components Research division in the Technology Development Group of Oregon has developed the first monolithic, three-dimensional GaN and silicon transistor stacking technology. It delivers best-in-class performance and efficiency, while allowing diverse functionalities to be integrated on a single chip.

Combining silicon and GaN is an attractive proposition. Silicon is today's workhorse for power electronics and RF switches, but it struggles to deliver high-frequency, high-power performance, so it is not a good choice for RF power amplification (see Figure 1). For that particular task, GaAs HBTs, GaAs HEMTs and GaN HEMTs are the front runners. However, these technologies are not ideal for making efficient power electronics: depletion mode GaAs HEMTs and GaN HEMTs are not favoured, due to their always-on nature; and the GaAs HBT is unsuitable, being current-driven rather than field-driven.

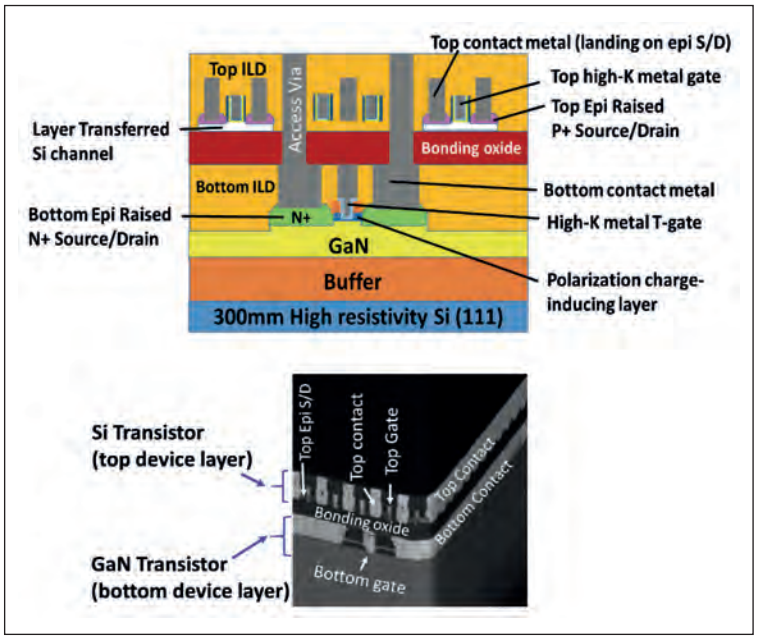

Figure 2. Intel has produced the first GaN transistors on a 300 mm silicon (111) wafer in one of its leading CMOS fabs. Its researchers have employed a new technique of three-dimensional monolithic integration by layer transfer to stack silicon PMOS transistors on top of GaN NMOS transistors to enable CMOS functionalities, for the first time in industry.

Fortunately, there is a transistor that excels on all fronts: the enhancement-mode (e-mode) GaN transistor. Recently, we have shown that when this class of device is equipped with high-κ dielectric metal gate technology, it can deliver best-in-class performance, in both power delivery and RF front-end functionalities. We have built on this success by using three-dimensional monolithic integration to unite GaN power and RF transistor technology with silicon

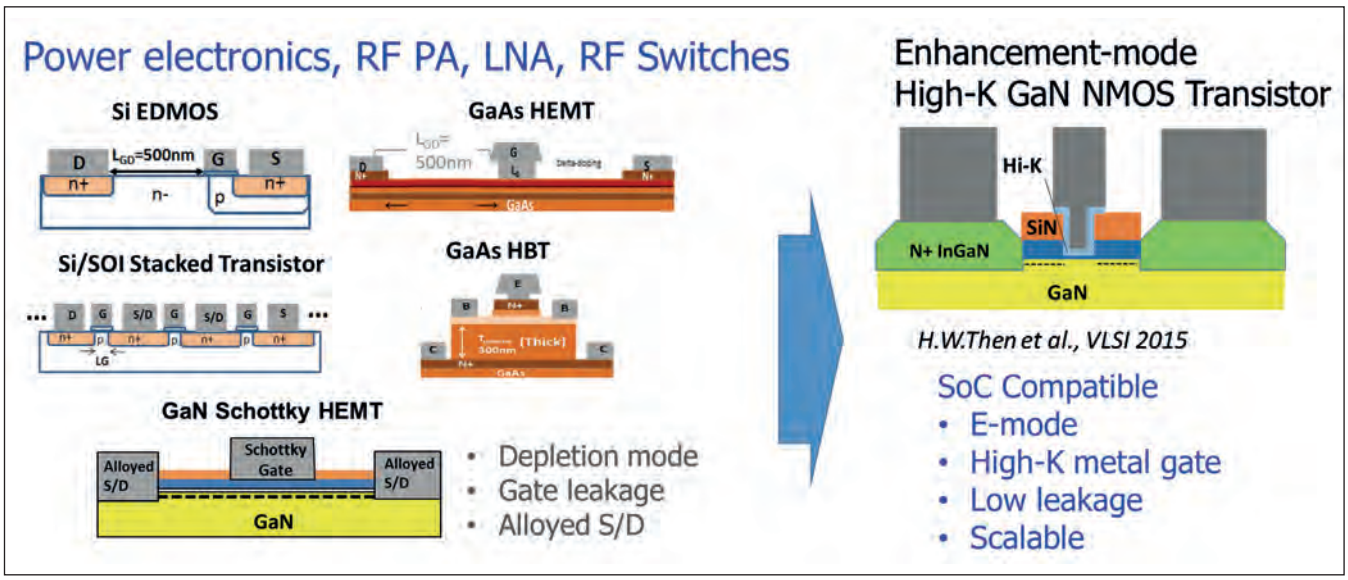

Figure 1. In today's power delivery and RF front-end solutions, dissimilar technologies come in multiple distinct and separate chips that have to be made to work together in a bulky package. Enhancement mode GaN transistors enabled by high-κ dielectric and metal gate technology can enable, for the first time, all these functionalities to be integrated on a single chip, realising a system-on-chip (SoC).

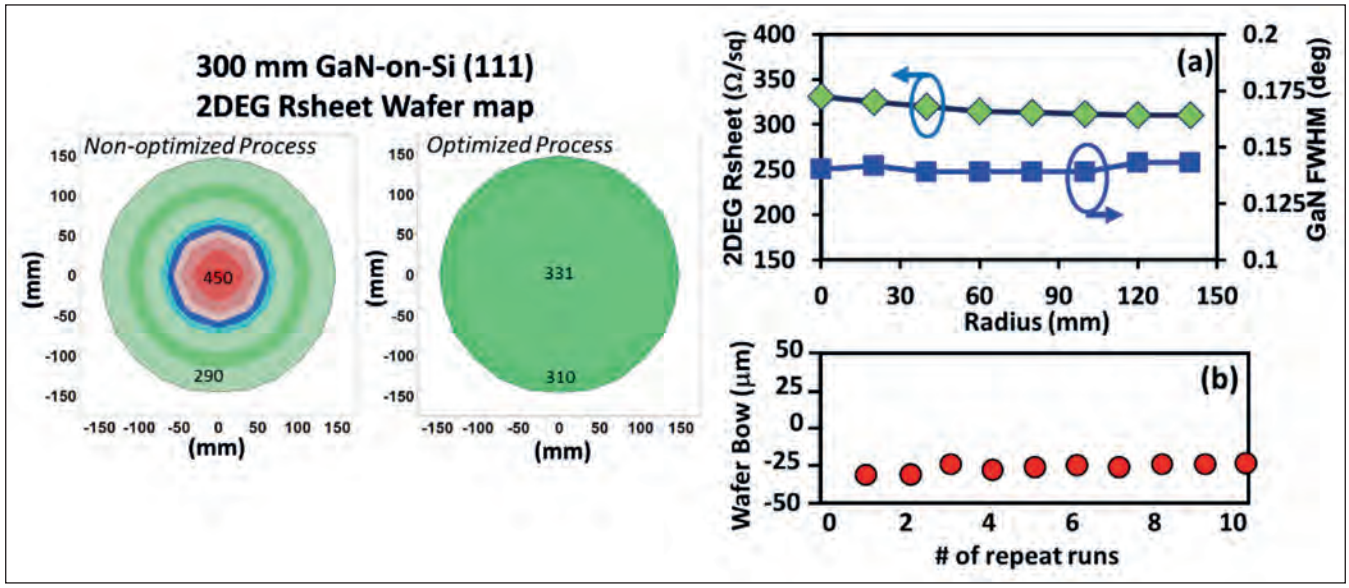

Figure 3. Optimised and uniform data from a manufacturable 300 mm GaN epitaxy process at Intel. Data distributions shown include: two-dimensional electron gas sheet resistance; GaN crystal quality, evaluated in terms of the the x-ray diffraction peak's full width at half-maximum (FWHM); and 300 mm wafer bow.

PMOS on 300 mm silicon substrates. Thanks to this, all functionalities can be integrated on a single chip to yield a system-on-chip for the very first time.

One of the successes that has come from our efforts is the fabrication of the first high-performance GaN transistors on 300 mm silicon (111) wafers (see Figure 2). We make these transistors with a 300 mm process technology that is compatible with leading CMOS fabs.

Another accomplishment is our use of a new technique of three-dimensional monolithic integration, based on layer transfer. With this approach we are breaking new ground by stacking silicon PMOS transistors on top of GaN NMOS transistors to enable CMOS functionalities. This new technology significantly expands the universe of solutions that can be implemented and integrated in an efficient, tiny system-on-chip.

Using one of our leading CMOS fabs for processing our GaN transistors on 300 mm silicon reaps an additional reward – it opens the door to all the latest process innovations. They include high-κ technology, three-dimensional layer transfer, chemical-mechanical polishing, lithographic techniques and copper interconnects. In addition, we benefit from the significant reduction in cost associated with cheaper 300 mm silicon substrates and high-volume production.

Leveraging larger wafers

Due to the lack of native substrates, nearly all GaN is

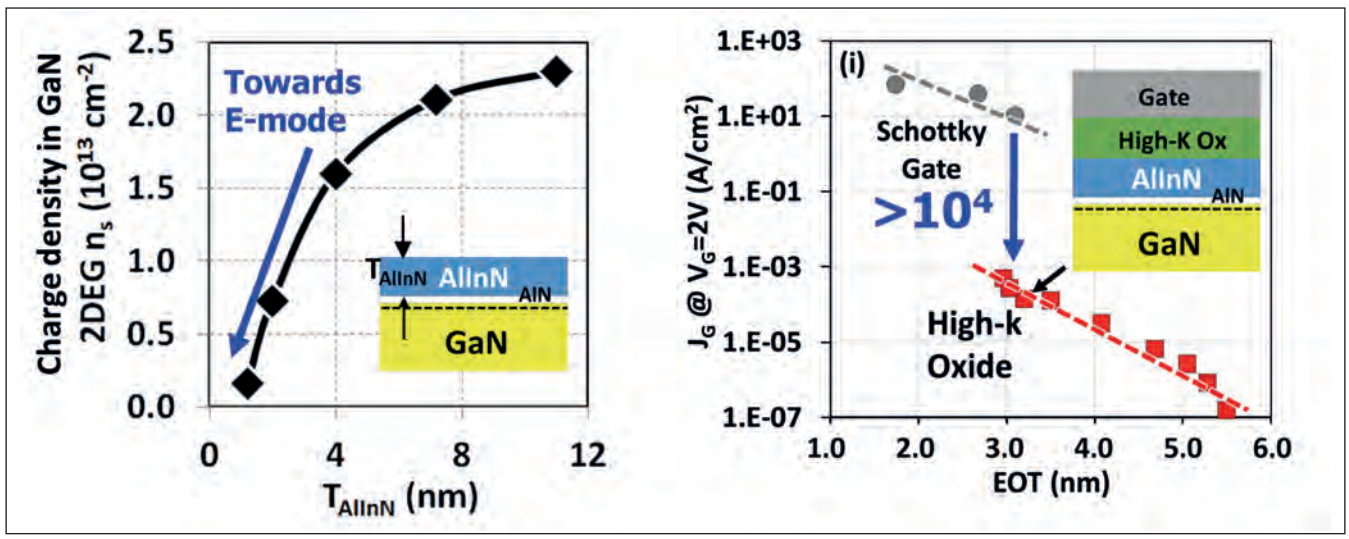

Figure 4. A high-κ gate dielectric reduces gate leakage by more than four orders of magnitude at scaled equivalent oxide thickness (EOT) for higher performance.

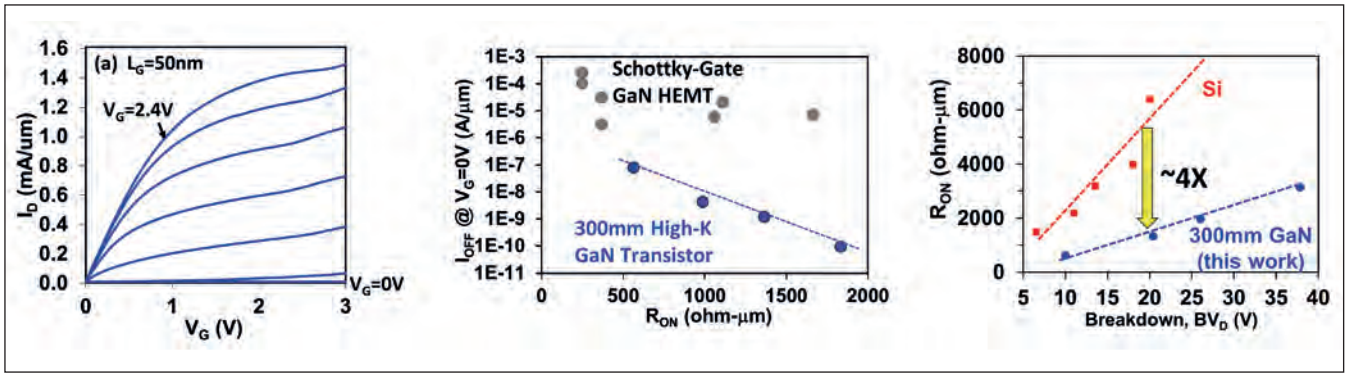

Figure 5. The I_D-V_D characteristics of Intel's e-mode high-κ dielectric GaN NMOS transistor on a 300 mm silicon wafer showing a high drive drain current that is approaching 1.5 mA/μm, a low knee voltage (it is below 1 V), and an on-resistance, R_{ON}, of just 610 Ω-μm. Low drain leakage, with I_{OFF} as low as 100 pA/μm at 5 V drain voltage, and excellent R_{ON} can be achieved simultaneously. The high-κ e-mode GaN NMOS transistors are about four times better than silicon transistors used for power delivery.

grown on foreign substrates, such as sapphire, SiC and silicon. The most popular platforms are 3-inch and 4-inch SiC, which are both relatively expensive, and 4-inch, 6-inch and 8-inch silicon (111). In contrast, we are using cost-effective 300 mm silicon (111) substrates (see Figure 3). On this platform we marry GaN with the most advanced high-κ dielectric metal gate technology in our 300 mm fab. This enables enhancement-mode operation and gate-stack scaling, and it ultimately realises high performance and low leakage, the keys to higher efficiencies. Note that this reduction in leakage is significant – it can exceed four orders of magnitude (see Figure 4) better than a Schottky gate GaN HEMT.

Another virtue of enhancement-mode, GaN transistor technology is that it simplifies the circuit architecture. As the enhancement mode transistor is normally-off, it does not require a negative power supply. Instead, this device can be driven directly from a battery, saving precious real estate on the microchip.

Measurements on our high-κ dielectric enhancement-mode GaN NMOS transistors on 300 mm silicon reveal excellent electrical characteristics and best-in-class performance for power delivery and RF. The devices have low drain leakages, high drive drain currents, low knee voltages and low on-resistances. Such characteristics show that high-κ dielectric technology enables a GaN transistor to combine a low leakage with excellent performance – it is about four times better than industry-standard silicon transistors for power delivery (see Figure 5).

Our devices also deliver excellent RF performance. Our high-κ GaN NMOS transistor significantly outperforms those based on GaAs and silicon/SOI transistors in power-added efficiency across a wide frequency range that spans 1 GHz to 30 GHz (see Figure 6). Due to the excellent knee voltage and on-resistance, efficient power amplifier (PA) operation is realised at drain voltages as low as 1 V (see Figure 7).

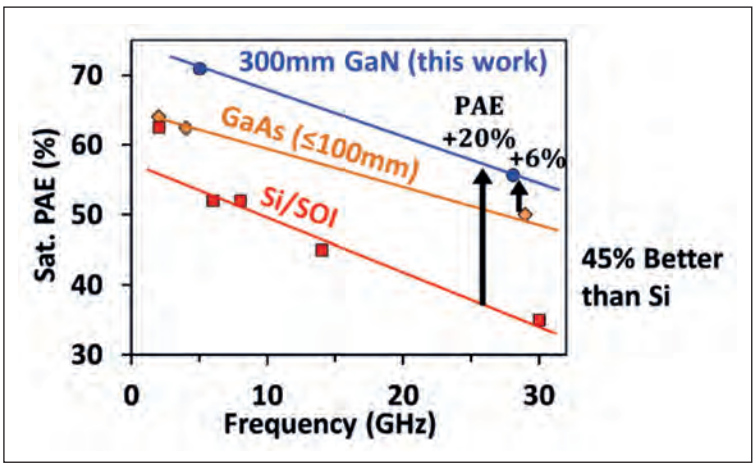

Figure 6. Intel's high-κ e-mode GaN NMOS transistor significantly outperforms GaAs and silicon/SOI across a frequency range spanning 1 GHz to 30 GHz.

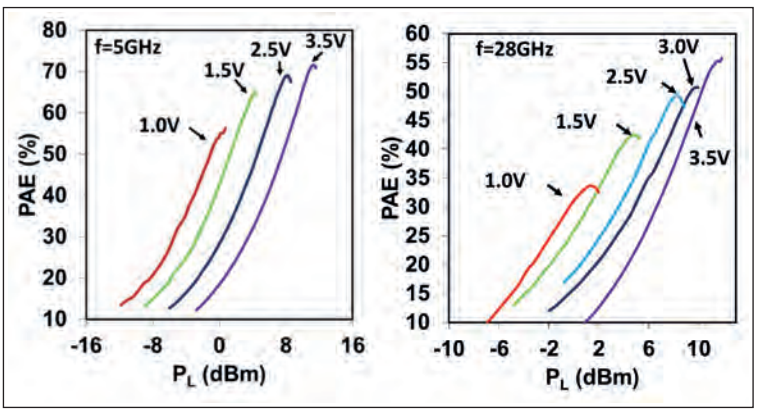

Figure 7. High power-added efficiencies are demonstrated with supply voltages from 3.5 V to as low as 1 V. Efficient PA operation well below 2 V surpasses the minimum cut-off supply voltage achievable by typical GaAs HBTs and highlights the potential of Intel's high-κ GaN transistor to extend battery life, and to realise efficient envelope-tracking RF PA.

The merits of GaN

Thanks to its wide bandgap, GaN has vastly superior Johnson and Baliga figure-of-merits when compared with GaAs and silicon (see Table 1). These virtues enable GaN to operate at high frequencies and high power.

An additional strength of GaN stems from the spontaneous and piezoelectric polarization effects associated with this family of materials. Due to this, a two-dimensional electron gas is produced in the GaN channel at the interface of GaN and a related ternary alloy, without the need for impurity doping. The resulting GaN heterostructure has a high carrier concentration, and also a high electron mobility, due to the low effective mass of the electrons and the absence of impurity scattering.

Yet another strength of GaN is that, due to its wide bandgap, it has a critical breakdown field that is at least ten times that for GaAs and silicon. This allows GaN transistors to be scaled to smaller lengths, leading to a higher performance. For example, for a supply voltage of 3.7 V, which is that provided by a lithium-ion battery, GaN transistors can be shorter, have a lower resistance and provide a higher drive current. Strengths such as these have made GaN the best semiconductor technology in production today for power and RF performance.

	Si	GaAs	GaN
Bandgap (eV)	1.1	1.42	3.4
Critical breakdown field, E_{crit} (MV/cm)	0.3	0.4	3.3
Electron Mobility, μ ($cm^2/V/s$)	1350	8500	2000
Peak velocity, v_{peak} (10^7 cm/s)	1	2	2.5
N-channel Baliga FOM$\propto\mu E_{crit}^2$ (normalized to Si)	1	11	179
N-channel Johnson FOM$\propto v_{peak}E_{crit}$ (normalized to Si)	1	2.7	27.5
Hole Mobility ($cm^2/V/s$)	<450	<400	<50
Active p-doping ($/cm^3$)	~10^{21}	~10^{19}	~10^{17}

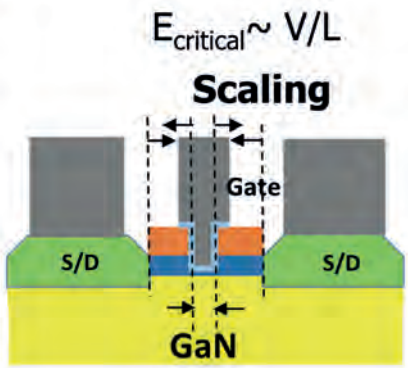

Table 1. Intrinsic semiconductor properties and figure-of-merits (FOM) for silicon, GaAs and GaN. N-channel GaN has the highest Baliga and Johnson FOMs, but P-channel GaN remains challenging due to low active *p*-doping and low hole mobility. The silicon PMOS transistor has a proven complementary P-channel with high hole mobility and high active *p*-doping.

This value is well below the minimum cut-off supply voltage for a typical GaAs HBT, highlighting the potential of the high-κ GaN NMOS transistor to significantly extend battery life while providing unrivalled efficiencies using the envelope-tracking RF PA architecture. High-κ GaN NMOS transistors also make excellent RF switches and low-noise amplifiers. For example, they have an excellent figure-of-merit for the switch, with a product of on-resistance and off-capacitance of just 110 fs. The minimum noise figure is only 0.4 dB at 5 GHz and 1.36 dB at 28 GHz (see Figure 8).

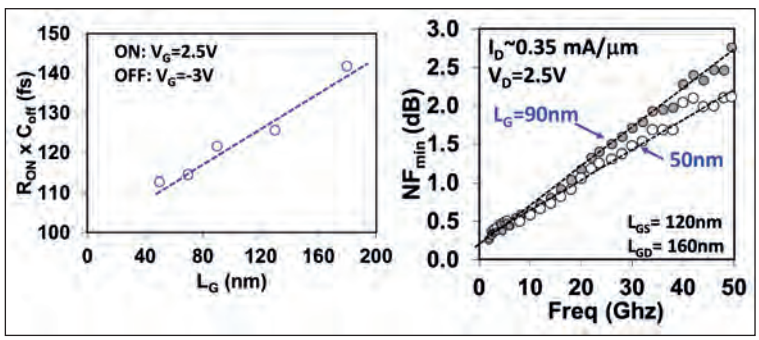

Figure 8. The excellent switch figure-of-merit, R_{ON} x C_{OFF}, and noise performance, NF_{min}, of the high-κ e-mode GaN NMOS.

The combination of the great performance as a power amplifier, a low-noise amplifier, an RF switch and a power transistor enables the enhancement-mode high-κ GaN NMOS transistor technology to boost the efficiency and performance of RF front-end and power delivery systems beyond what is capable today with GaAs and silicon technology. But that's not all – by turning to high-κ GaN NMOS transistor technology, we realise compact integration of multiple functionalities on a single chip, saving space and achieving unmatched small form factors.

Three-dimensional integration

A selling point in today's marketplace is tight on-chip integration of CMOS analog and digital logic/control functionalities, along with CMOS memory. These types of CMOS chips are currently built as standalone units, but as functionality and complexity increases, monolithic system-on-chip solutions will be needed to provide higher efficiency, lower cost and a higher integration density (see Figure 9).

However, it is extremely challenging to implement a design based on monolithic complementary GaN CMOS, due to the low hole mobility in GaN, and the difficulty in realising high *p*-type doping in this material.

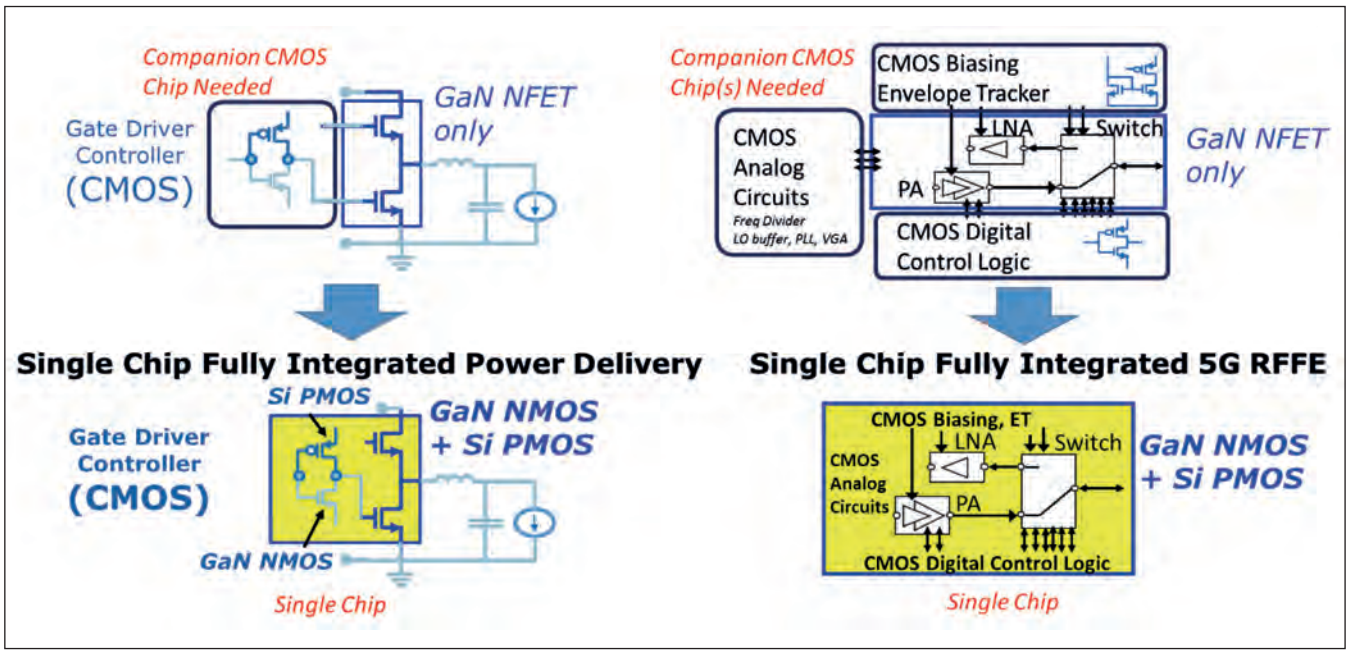

Figure 9. Single-chip fully integrated power delivery and RF front-end units can be realised with Intel's three-dimensional monolithically integrated silicon PMOS stacked on GaN NMOS transistor technology.

The good news is that progress is being made by a partnership between our team and research groups at Cornell and MIT. This effort hopes to fulfil the promise of wide bandgap, high-voltage operation of GaN PMOS. While this work is in its infancy, the hope is that standard high-κ metal gate silicon PMOS can step in to provide an excellent complementary p-channel technology to GaN NMOS, due to its high hole mobility and possibility to realise a very high *p*-doping for source-drain contacts.

To monolithically integrate multiple dissimilar semiconductor materials on a single silicon substrate, we have turned to layer transfer techniques. This enables us to monolithically stack silicon PMOS transistors on top of GaN NMOS transistors.

Drawing on this form of three-dimensional monolithic integration has much merit, as it allows each constituent transistor technology to be built and optimised separately to offer the best performance and cost.

We begin our three-dimensional layer transfer process by oxide fusion-bonding a standard 300 mm crystalline silicon (100) donor wafer to a completed 300 mm GaN-on-silicon (111) wafer. After this, we remove the bulk donor wafer and fabricate silicon PMOS transistors (see Figure 10). We ensure high-performance silicon PMOS by aligning the finfet in an orientation that boosts hole mobility. This is accomplished by having the transistor channel on the

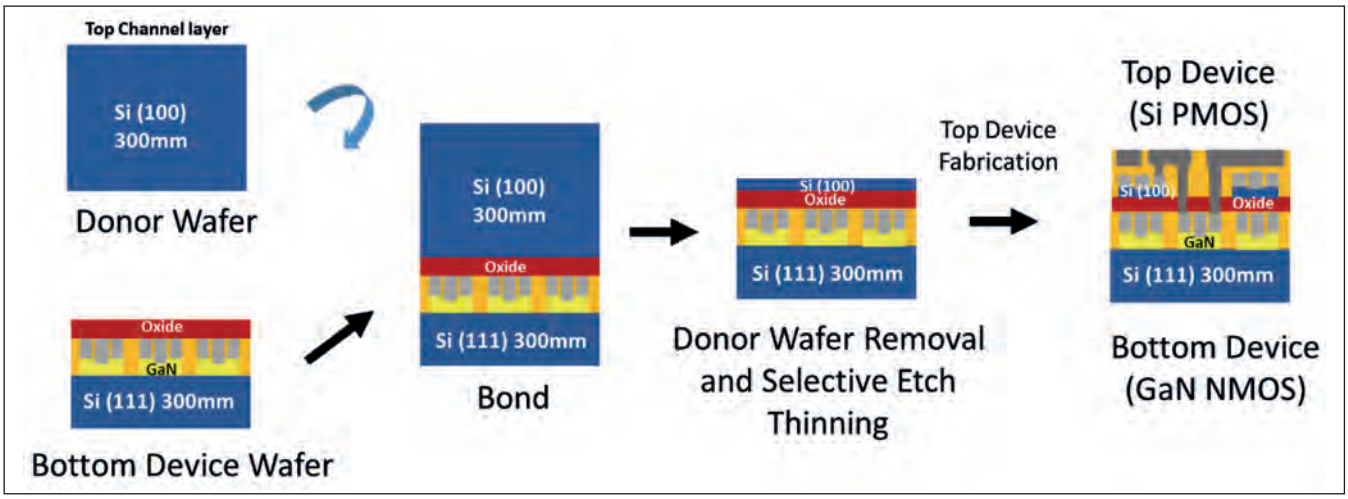

Figure 10. Intel's monolithic three-dimensional layer transfer process flow involves the transfer of a layer of single crystalline silicon from a 300 mm silicon (100) donor wafer onto a completed 300 mm GaN-on-silicon (111) wafer, prior to fabrication of the top silicon PMOS transistors.

sidewalls orientated in a particular crystal plane and current-carrying direction (see Figure 11). There is much freedom with our approach. The silicon PMOS transistor design and architecture can be made independently of the choices for the bottom GaN transistors. For example, by selecting the appropriate channel orientation for the silicon PMOS and the channel length for the GaN NMOS, the drive current and the off-state leakage can be matched for both channels (see Figure 12).

Our monolithic three-dimensional stacking of GaN NMOS and silicon PMOS transistors provides a powerful way to integrate two dissimilar best-in-class semiconductor technologies on the same wafer and deliver the best performance, increased density, and greater functionality.

This technology has tremendous promise as it could enable entirely new classes of products with game-changing capabilities. Many exciting opportunities lie ahead, including the full integration of efficient, high-performance RF and power delivery with standard silicon-based processors. Such a technology has the potential to meet the demands of next-generation mobile devices, data infrastructure and communication networks for 5G and beyond.

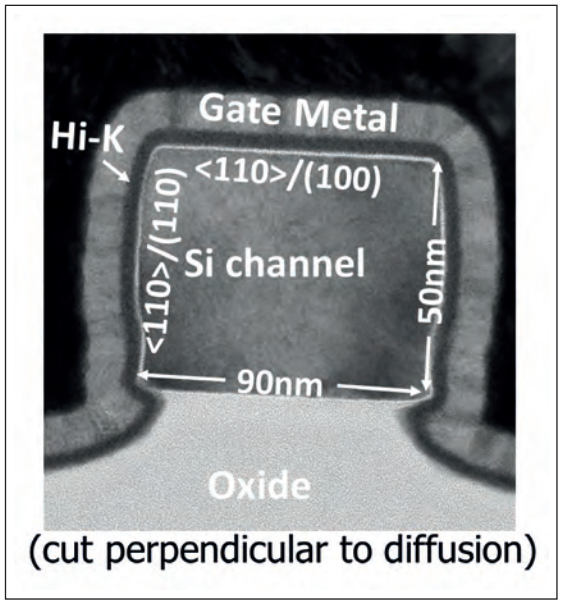

Figure 11. The cross-section of the top silicon PMOS transistor showing its finfet architecture, crystal orientation and current-carrying direction to boost hole mobility and performance. These silicon transistor design and architectural choices can be made independent of the choices made for the bottom GaN transistors.

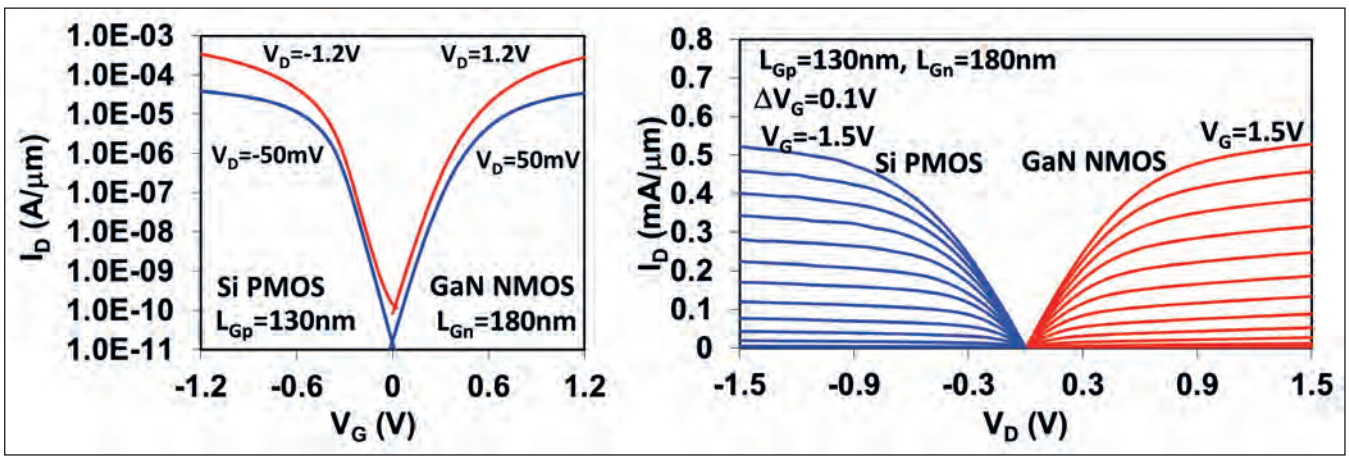

Figure 12. Current-voltage characteristics of the top layer channel length (L_G is 130 nm) silicon PMOS transistor and the bottom channel length (L_G 180 nm) GaN NMOS transistors. Dimensions have been chosen independently, to match drive current strengths and off-state leakages.

Further reading

H. W. Then *et al.* "3D heterogeneous integration of high performance high-κ metal gate GaN NMOS and Si PMOS transistors on 300mm high-resistivity Si substrate for energy-efficient and compact power delivery, RF (5G and beyond) and SoC applications", IEDM, 2019.

H. W. Then *et al.* ""High-Performance Low-Leakage Enhancement-Mode High-κ Dielectric GaN MOS-HEMTs for Energy-Efficient, Compact Voltage Regulators and RF Power Amplifiers for Low-Power Mobile SoCs", VLSI Technology Symposium, 2015.

S. Bader *et al.* "GaN/AlN Schottky-gate *p*-channel HFETs with InGaN contacts and 100mA/mm on-current", IEDM, 2019.

N. Chowdhury *et al.* "First Demonstration of a Self-Aligned GaN *p*-FET", IEDM, 2019.

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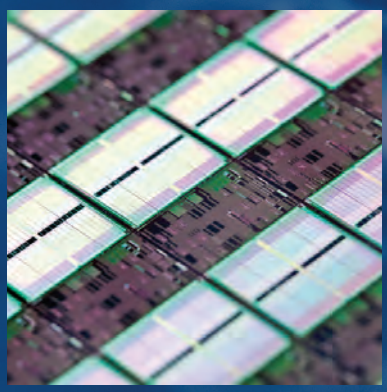

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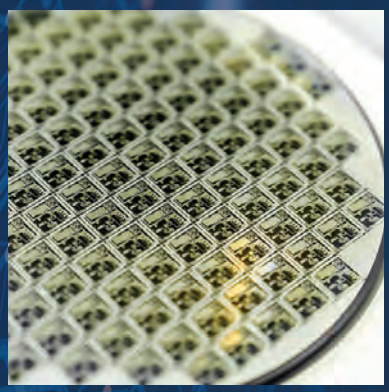

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