SILICON SEMICONDUCTOR

Connecting the Silicon Semiconductor Community

Volume 42 ISSUE II 2021 @siliconsemi www.siliconsemiconductor.net

Non-destructive testing of metals & materials

Fab lifecycle and subfab service maturity model

Benefits of plasma dicing technology

For die in a package, it's always about the bond

Paradigm shift for device manufacturers

Meeting demanding customer requirements through revolutionary materials science

MERCK

inside News Review, News Analysis, Features, Research Review, and much more...

Free Weekly E News round up go to: www.siliconsemiconductor.net

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

www.EVGroup.com

ACCELERATING HETEROGENEOUS INTEGRATION

- EV Group establishes Heterogeneous Integration Competence Center™ to accelerate new product development and process integration efforts
- Wafer-to-Wafer (W2W) and Die-to-Wafer (D2W) hybrid bonding processes ready for sample test, product development and qualification
- Open access innovation incubator for EVG customers and partners across the microelectronics supply chain, guaranteeing the highest IP protection standards
- Combining EVG's world-class wafer bonding, thin-wafer handling and maskless, optical and nanoimprint lithography products and expertise, as well as pilot-line production facilities and services

GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com

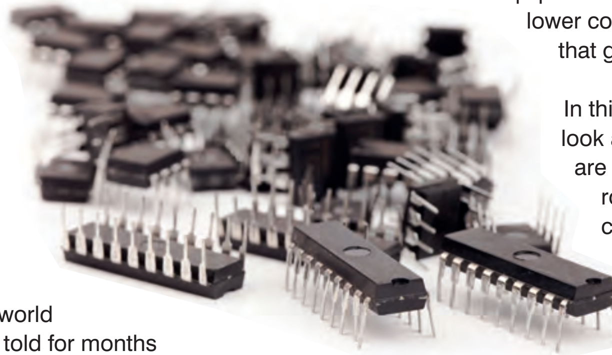
editor's view

By Mark Andrews, Technical Editor

Post-COVID IC manufacturing sees surging wafer, materials & equipment sales

EVEN AS THE WORLD STRUGGLES to regain its pre-pandemic footing, leading semiconductor indicators point towards a strong post-COVID economy driven by a thirst for tech-enabled products and services. Shortages persist across many IC categories while stronger demand affecting nearly every supply chain sector has fueled concerns that consumer spending may also drive inflation.

Consumers are paying more for just about everything in these post-pandemic times. Anyone who has recently shopped for pantry staples, consumer electronics, vehicles, or even a home, the chances are that prices seen today are higher than three months ago. Answering the 'why' question is straightforward — demand continues to outstrip supply. In a world where almost everyone has been told for months to stay at home, avoid crowds, mask, and be vaccinated, factory output is lagging behind the spending of consumers anxious to trade the 'new normal' of 2020 for a taste of pre-pandemic freedoms.



The SEMI trade group reported that as of May, first quarter silicon wafer shipments easily surged past historic 1Q seasonal benchmarks. Materials makers are also enjoying robust sales as digitization (in part pandemic driven,) continues to surge more deeply into daily life. SEMI also attributes the rise in materials sales to an outgrowth of 5G buildouts and new interest in this supply chain sector by global investors. Unsurprisingly, semiconductor equipment makers are also on track for another bonanza year, so much so that legacy gear (process tools for wafers under 300mm) is enjoying a resurgence. Refurbished equipment sales are also climbing thanks to lower costs and an experienced workforce that got its start with 200mm tech.

In this edition of Silicon Semiconductor we look at how advanced electronic materials are playing an increasingly important role in IC manufacturing. Merck KGaA continues to expand its capabilities with materials that help reduce defects while offering the ability to assess performance in unique ways, providing customers a new competitive edge.

We also look at new bonding solutions from Palomar Technologies that put a fresh spin on 'multi-tasking' and Edwards Vacuum's continuing evolution of sub-fab maintenance designed to ensure uptime while lowering overall costs.

Publisher & Editor Jackie Cannon	jackie.cannon@angelbc.com	+44 (0)1923 690205
Technical Editor Mark Andrews	mark.andrews@angelbc.com	
Sales & Marketing Manager Shehzad Munshi	shehzad.munshi@angelbc.com	+44 (0)1923 690215
USA Representatives Tom Brun Brun Media	tbrun@brunmedia.com	+001 724 539-2404
Janice Jenkins	jjenkins@brunmedia.com	+001 724-929-3550
Director of Logistics Sharon Cowley	sharon.cowley@angelbc.com	+44 (0)1923 690200
Design & Production Manager Mitch Gaynor	mitch.gaynor@angelbc.com	+44 (0)1923 690214
Circulation Director Scott Adams	scott.adams@angelbc.com	+44 (0)2476 718970
Chairman Stephen Whitehurst	stephen.whitehurst@angelbc.com	+44 (0)2476 718970
Chief Executive Officer Sukhi Bhadal	sukhi.bhadal@angelbc.com	+44 (0)2476 718970
Chief Technical Officer Scott Adams	scott.adams@angelbc.com	+44 (0)2476 718970
Directors Jackie Cannon, Sharon Cowley		

Published by Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. T: +44 (0)2476 718 970 F: +44 (0)2476 718 971 E: info@angelbc.com

Silicon Semiconductor is published four times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £50.00/e60.00 pa (UK & Europe), £70.00 pa (air mail), $90.00 pa (USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher. Every effort has been made to obtain copyright permission for the material contained in this publication. Angel Business Communications Ltd will be happy to acknowledge any copyright oversights in a subsequent issue of the publication. Angel Business Communications Ltd © Copyright 2021. All rights reserved. Contents may not be reproduced in whole or part without the written consent of the publishers. The paper used within this magazine is produced by chain of custody certified manufacturers, guaranteeing sustainable sourcing. US mailing information: Silicon Semiconductor, ISSN 1096-598X, is published 4 times a year, Jan/Feb, March, April/May, June, July, August/September, October, November/ December by Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Rd, Coventry CV5 6SP. UK. The 2021 US annual subscription price is $90.00. Airfreight and mailing in the USA by agent named World Container Inc, 150-15, 183rd Street, Jamaica, NY 11413, USA. Periodicals postage paid at Brooklyn, NY 11256. US Postmaster: Send address changes to Compound Semiconductor, Air Business Ltd, c/o WN Shipping USA, 156-15, 146th Avenue, 2nd Floor, Jamaica, NY 11434, USA. Printed by: The Manson Group. ISSN 2050-7798 (Print) ISSN 2050-7801 (Online) © Copyright 2021.

We strive for accuracy in all we publish; readers and contributors are encouraged to contact us if they recognise an error or omission. Once a magazine edition is published [online, in print or both], we do not update previously published articles to align old company names, branding, marketing efforts, taglines, mission statements or other promotional verbiage, im-ages, or logos to newly created or updated names, images, typographic renderings, logos (or similar) when such references/images were accurately stated, rendered or displayed at the time of the original publication. When companies change their names or the images/text used to represent the company, we invite organizations to provide Angel Business Communications with a news release detailing their new business objectives and/or other changes that could impact how customers/prospects might recognise the company, contact the organisa-tion, or engage with them for future commercial enterprise.

VOLUME 42 ISSUE II 2021

CONTENTS

12 COVER STORY

Merck meets demanding customer requirements through revolutionary materials science

The continuing evolution of semiconductor devices has challenged materials suppliers to take a more active role in defect elimination and yield enhancement as IC manufacturing grows increasingly complex

16 For die in a package it's always about the bond

Manufacturers constantly seek to reduce costs and improve performance. As advanced node devices continually shrink, process complexity, cost and risk also multiply.

20 Ensuring the reliability of electronic devices

Non-destructive advanced scanning acoustic microscopy detects flaws in specialty metals, materials, and packaging of semiconductor devices.

22 Benefits of plasma dicing technology

Plasma dicing addresses the challenges of dicing smaller and thinner dies; enables higher throughput and increased yield per wafer.

30 System level test enables a paradigm shift

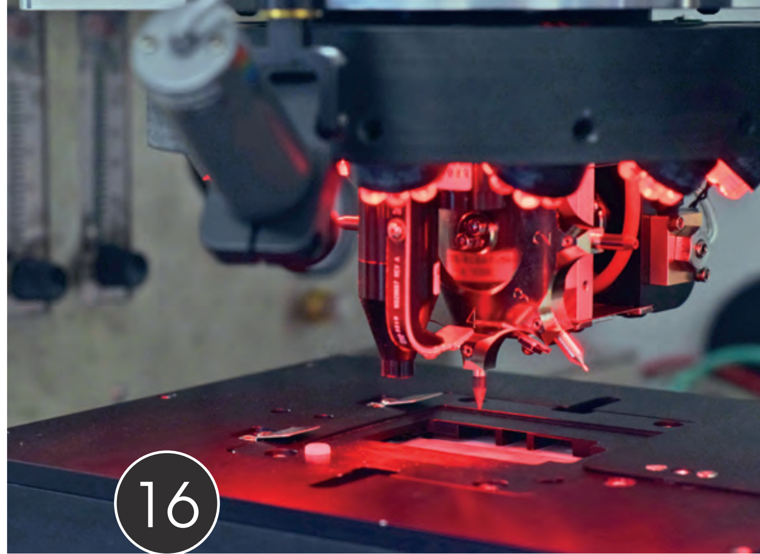
Research conducted by AEM Singapore says the semiconductor industry needs continuous improved faults coverage while reducing the overall costs of test and measurement operations.

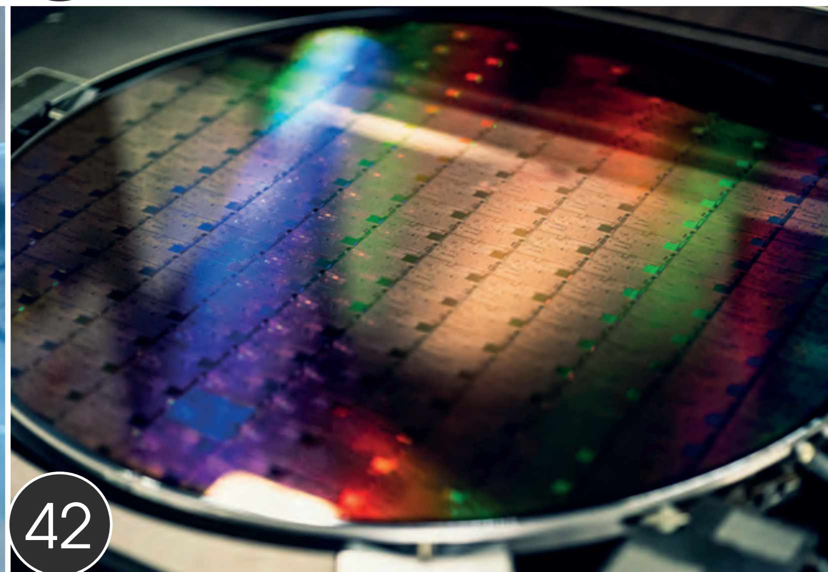
34 Evaluating the Fab Lifecycle and SubFab service maturity model

Many plant managers view subfab maintenance as an unavoidable cost rather than an opportunity to lower overall expenses while increasing uptime.

42 2D transistors to extend the logic roadmap

Development of WS2 2D transistors in a 300 mm CMOS fab provides a promising pathway for scaling the transistor





news

06 Quantum Computing breakthrough shows blueprint for scalable future

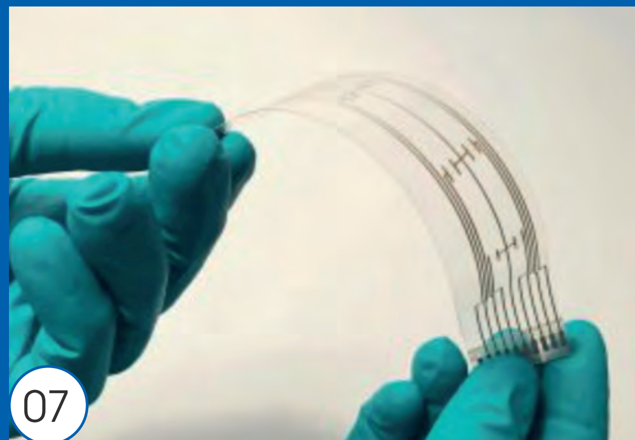
07 Brewer Science expands capabilities

08 EU Project to mimic multi-timescale processing of Biological Neural Systems

09 Park Systems hits 1 Trillion KRW mark at KOSDAQ

10 Reno launches Series of integrated RF power systems at 7nm or below

11 TESCAN new delayering capability for unattended, automated failure analysis



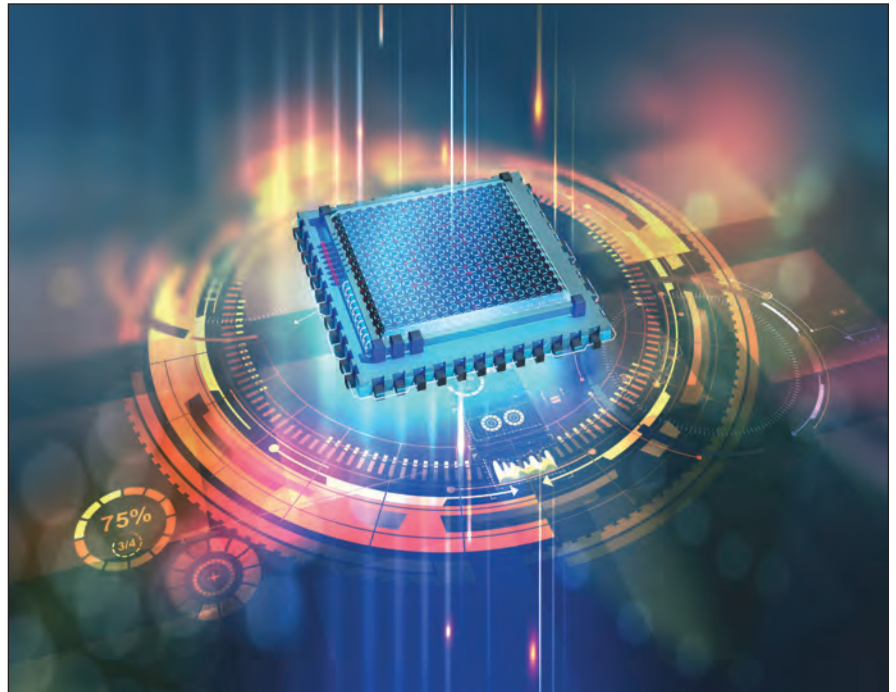
Quantum Computing breakthrough shows blueprint for scalable future

QUANTUM MOTION, a UK-based quantum computing startup led by academics from UCL and Oxford University, has made a breakthrough that radically advances the viability and production of quantum computers. Quantum Motion has been able to demonstrate state of the art quantum capabilities using industrial-grade silicon chips,helping to set a blueprint for how quantum chips can be manufactured at scale using existing manufacturing processes. The discovery has been peer reviewed in the scientific journal PRX Quantum.

The discovery changes the dynamics in the development of quantum computing, showing that it is possible to build devices at scale using established processes and fabrication plants. This contrasts with other industry approaches that are looking at totally new manufacturing processes or even newly discovered particles. This potentially makes quantum computing development quicker and more cost effective.

A quantum computer harnesses some of the deepest laws of physics, normally seen only at the atomic and subatomic level, giving it unique powers to model the natural world. Quantum computers could be more powerful than today's super computers and capable of performing complex calculations that are otherwise practically impossible. While the applications of quantum computing differ from traditional computers, they will enable us to be more accurate and faster in hugely challenging areas such as drug development and tackling climate change, as well as more everyday problems that have huge numbers of variables – just as in nature – such as transport and logistics.

"We're hacking the process of creating qubits, so the same kind of technology that makes the chip in a smartphone can be used to build quantum computers," said John Morton, Professor of Nanoelectronics at UCL and co-founder of Quantum Motion. "It has taken 70 years for transistor development to reach where we are today in computing and we can't spend another 70 years trying to invent new manufacturing processes to build quantum computers. We need millions of qubits and an ultra-scalable architecture for building them, our discovery gives us the blueprint to shortcut our way to industrial scale quantum chip production."



The peer reviewed paper demonstrates that Quantum Motion has been able to isolate and measure the quantum state of a single electron for a period of nine seconds on a CMOS chip. The chips were manufactured at CEA Leti, a large microelectronics facility in Grenoble, France. Qubits, the building blocks of quantum computers, are often realised using exotic technologies such as superconductors or individually trapped atoms. The big breakthrough is the proof that it is possible to create a stable qubit on a standard silicon chip, like those found in any smartphone, rather than one specially created in a lab environment. Combined this creates the potential for stable and scalable quantum computing.

The experiments were performed by Virginia Ciriano Tejel, a PhD student working in a low-temperature laboratory at UCL, and co-workers. During operation, the chips are kept in a refrigerated state, cooled to a fraction of a degree above absolute zero (−273 degrees Celsius).

Virginia described the eureka moment, "Every physics student learns in textbooks that electrons behave like tiny magnets with weird quantum properties, but nothing prepares you for the feeling of wonder in the lab, being able to watch this 'spin' of a single electron with your own eyes, sometimes pointing up, sometimes down. It's thrilling to be a scientist trying to understand the world and at the same time be part of the development of quantum computers."

Quantum Motion was founded in 2017 and has raised £8million in series A funding, led by INKEF capital, a Dutch based venture capital company. The round was supported by new investors Octopus Ventures and the National Security Strategic Investment Fund (NSSIF) as well as existing investors Oxford Sciences Innovation, Parkwalk Advisors and IP Group plc.

Brewer Science expands capabilities: smart devices & printed electronics foundry

BREWER SCIENCE has announced that its division formerly known as "Printed Electronics" has expanded and is now its "Smart Devices & Printed Electronics Foundry." Brewer Science combines materials science expertise, printed flexible electronics technology, and firmware development capabilities to deliver flexible hybrid electronic (FHE) products that deliver actionable data required for today's sophisticated IIoT environments.

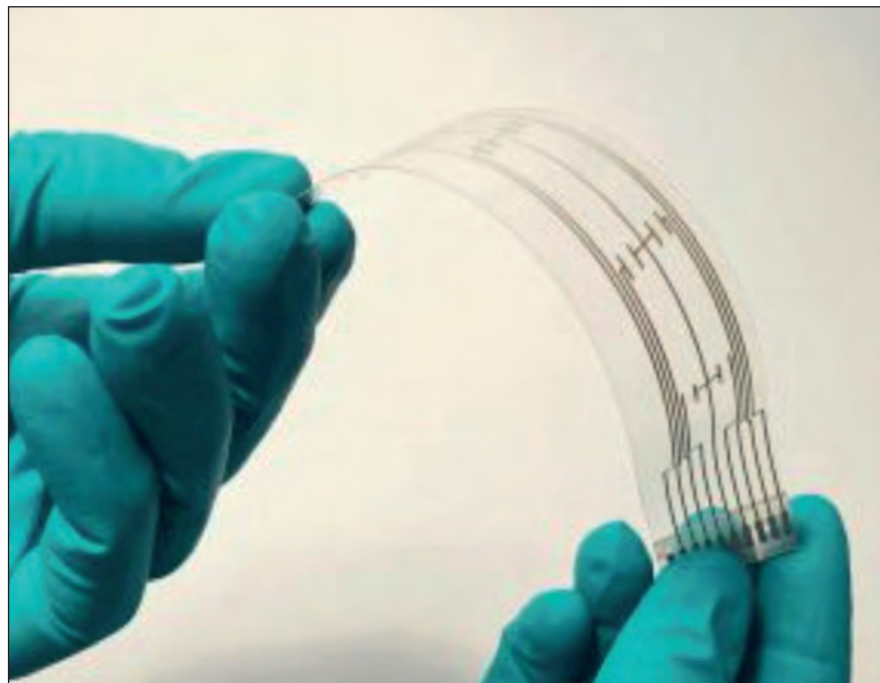
The expanded Smart Devices & Printed Electronics Foundry now offers a full range of electronics platforms, including sensors and systems, that are easily integrated into existing processes and products, such as foundry services, printed temperature sensors, water quality sensors, and condition-monitoring sensors.

The complete end-to-end services range from small-scale prototyping and sensor manufacturing to user interface design, security protocols, as well as data-to-cloud capabilities.

"Brewer Science continues to push the boundaries of what is possible. Cutting-edge materials science and innovative process development are at the core of the company's 40-year history.

By expanding into smart devices and printed electronics, we are leveraging our knowledge and experience in microelectronics to deliver smart sensor systems and real-time data to our customers," said Dr. Adam Scotch, Director of R&D, Smart Devices and PE Foundry.

Showcasing its cutting-edge technology, Brewer Science exhibited its FHE capabilities at the FLEX 2021 Virtual Conference February 22 through 26, and will exhibit at the LOPEC International tradeshow in Messe Munchen, Germany, 23 - 25 March. Ryan Moss, Director of New Business Development at Brewer Science, and Jonathan Fury, Director of Printed Electronics at Brewer Science, will be presenting their research, "Enabling IIOT Applications in Water Sensing."



PICOSUN Sprinter demonstrates record-breaking batch film quality

PICOSUN GROUP has further optimized its PICOSUN Sprinter ALD system processes successfully for semiconductor, display and IoT component manufacturing lines. PICOSUN Sprinter ALD system Al2O3 process results showed excellent thickness uniformity even at low 90 °C deposition temperature.

At 300 °C temperature the results were at record-breaking level (<0.2% 1sigma) when measured within wafer. Furthermore, the team has continued to improve also other parts of the process performance. The production capacity has more than doubled in the last two months when the process cycle time has been reduced to 8 seconds, without any uniformity degradations.

Other examples include the SiO2 process results, which showed uniform films for backend-of-the-line compatible thermal SiO2 ALD process at 300-390 °C.

More information on these and other process improvements are available on request. Al2O3 is one of the most common deposited films for applications such as moisture barrier for image sensors and displays. SiO2 thin film is widely used in the manufacturing process of for example logic chips as spacer or multipattern applications. Sensitive substrates can require low deposition temperature or low thermal budget without compromising the film quality, which is one of the challenges the company wanted to address with PICOSUN Sprinter.

EU Project to mimic multi-timescale processing of Biological Neural Systems

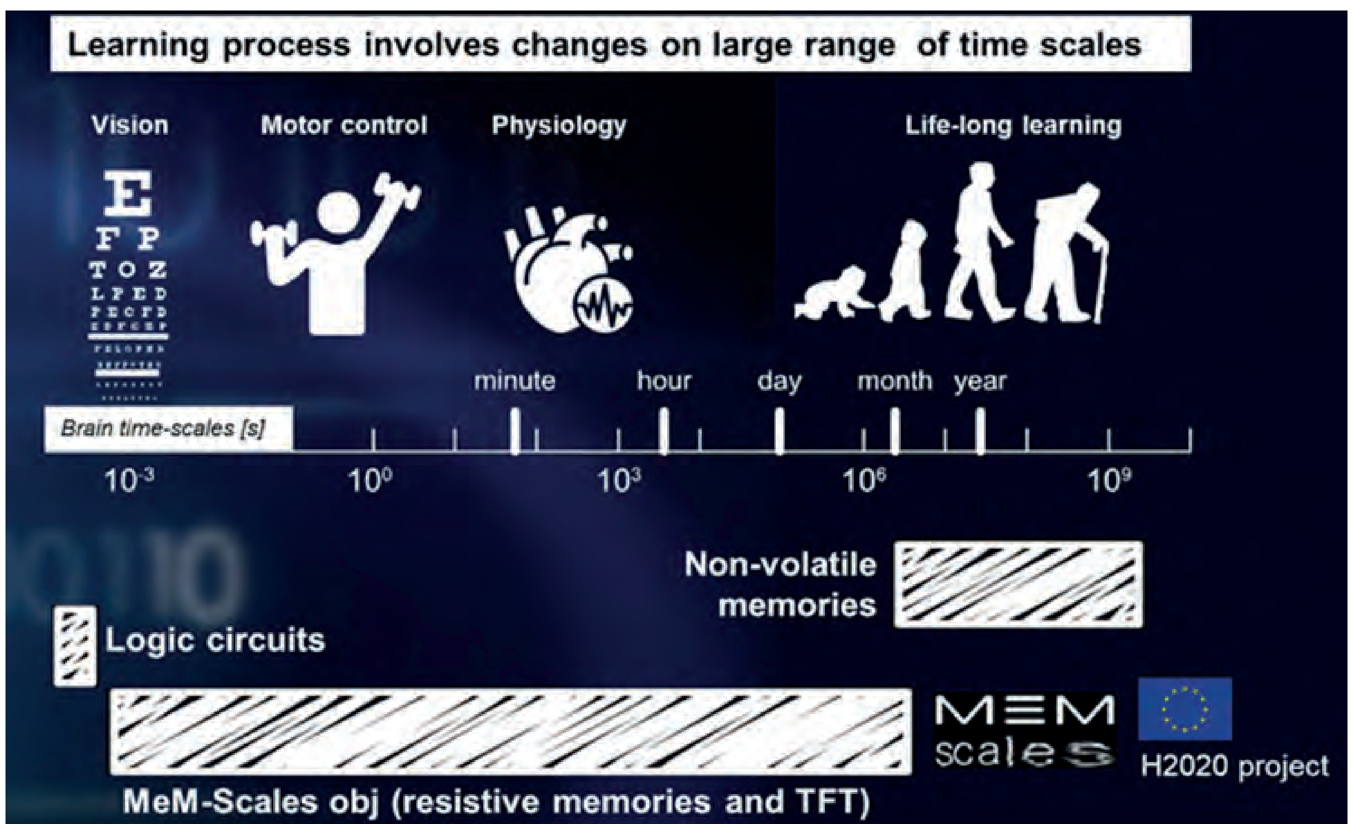
CEA-LETI has announced the launch of an EU project to develop a novel class of algorithms, devices and circuits that reproduce multi-timescale processing of biological neural systems. The results will be used to build neuromorphic computing systems that can process efficiently real-world sensory signals and natural time-series data in real-time and to demonstrate this with a practical laboratory prototype.

The technology developed in the MeM-Scales project will enable novel solutions for the Internet of Things (IoT). In the future IoT, much computing volume will be offloaded from central servers and delegated to small controllers and intelligent sensors directly where their services are needed. These IoT systems must be able to work reliably, without interruptions and with very low energy demands. The project also will develop edge-computing processing systems for applications that do not require connectivity to the cloud. Multi-timescale processing is inspired by neural processing in the nervous system, which occurs naturally over time scales ranging from milliseconds (axonal transmission) to seconds (spoken phrases) and much longer intervals (motor learning).

“The MeM-Scales project aims at lifting neuromorphic computing in analog spiking microprocessors to an entirely new level of performance,” said Elisa Vianello, manager of CEA-Leti’s AI program and the coordinator of the MeM-Scales project. “Our work is based on a dedicated commitment that novel hardware and novel computational concepts must co-evolve in a close interaction between nano-electronic device engineering, circuit-and-microprocessor design, fabrication technology and computing science: machine learning and nonlinear modeling.”

For physical substrates, novel memory and device technologies will be fabricated to support on-chip learning over multiple timescales for both synapses and neurons. Multi-timescale resistive memory technologies as well as thin-film transistor (TFT) technology will be used to enable timescales spanning up to nine orders of magnitude. On the side of computational theory, autonomous learning algorithms and architectures supporting computation over this wide range of timescales will be developed. These computational methods will be specifically tailored to cope with the low numerical precision, parameter drift, stochasticity and device mismatch that are inherent in analog nanoscale devices.

The project brings together European specialists in neuromorphic engineering, an emerging interdisciplinary field that takes inspiration from biology, physics, mathematics, computer science, and engineering to design hardware/physical models of neural and sensory systems. The project’s name is short for Memory technologies with Multi-Scale time constants for neuromorphic architectures.



Park Systems hits 1 Trillion KRW mark at KOSDAQ

PARK SYSTEMS, manufacturer of Atomic Force Microscopes announced the company stock valuation exceeded 1 Trillion KRW (almost $1 Billion USD) at the end of KOSDAQ on April 20, 2021. Park Systems issued 1 million shares for its initial public offering on December 17th, 2015 at KOSDAQ, a NASDAQ equivalent in Korea. Since the IPO, the company has progressed as a global leader in Atomic Force Microscopy, with a commanding lead in semiconductor advanced automated AFM systems and bringing AFM technology into the mainstream as the premier tool for nanoscale metrology.

"Park Systems has received successive purchase orders by all the world's top semiconductor and data storage manufacturers," states Dr. Sang-il Park, CEO and founder of Park Systems, who worked as an integral part of the group at Stanford University that first developed AFM technology, and created the first commercial AFM in 1988. "We have continued to grow at an accelerated rate of over 20% compounded growth, even during the turbulent pandemic year." The valuation at KOSDAQ, close to $1 Billion USD brought attention from foreign investors who have made active purchases, increasing the company's holding from 11% (Jan) to 18% (March). Recently Park was recognized by Forbes Asia Best Under a Billion list for 2020, received the KOSDAQ Grand Prize, and listed on the FTSE small-cap index.

In 2020, Park Systems signed a joint development project with IMEC to address the current metrological challenges of continuously downscaling the geometrical dimensions of devices and 3D stacking assembly. Earlier this year, Park Systems made an equity investment in Molecular Vista, that produces tools to probe and understand matter at the molecular level through quantitative visualization using InfraRed Photo-induced Force Microscopy. Park Systems is headquartered in Suwon, South Korea. With its rapid global expansion, it has become the premier supplier of Atomic Force Microscopy (AFM) tools for industrial, research and academic nanoscale research. Research at the extensive Park Applications Technology locations worldwide have led to the development of many leading AFM technologies including True Non-Contact™ technology, SmartScan™ operating software, PinPoint™ mode, which can be applied for nano-mechanical analysis and electrical modes; and most recently, the Smart Litho™ for nanoscale lithography. Park Systems was the first company to revolutionize AFM technology with its flexure-based scanner system that brought new levels of accuracy, resolution, and sample handling to the technology. In 2024, Park Systems will move into a new expanded headquarters, and later this year, it will introduce a new fully automated AFM with AI and robotic intelligence for both scientific and industry labs.

OPTIM Wafer Services is pleased to announce the installation of an automated ALPSITEC MECAPOL E550 CMP tool at its site in Greasque France.

The system will allow OPTIM to offer for following new or improved services.

- **Oxide CMP Planarisation**
- **Oxide Roughness Improvement**
- **Metal CMP**
- **Poly CMP**

This additional capability enhances OPTIM's already large portfolio of services that include:

- **Wafer thinning by grinding**
- **Individual Die thinning**
- **Taiko Grinding**
- **Single/Double side Polishing**
- **SOI Processing**
- **Edge Trimming**
- **Wafer Dicing**
- **Dice Before Grinding**
- **Wafer Cleaning**
- **Process development services, combining any of the above capabilities.**

For detailed technical discussions please contact either Mr. Mark Wells or Mr. Georges Peyre using the contact details below or visit our website.

www.Optimwaferservices.com

Mark Wells
Tel - +44 1743 891 820
Email – MWells@optimws.com

Georges Peyre
Tel - +33 442 126 158
Email – GPeyre@optimws.com

Reno launches Series of integrated RF power systems at 7nm or below

RENO SUB-SYSTEMS (Reno), a developer of high performance radio frequency (RF) matching networks for nanoscale semiconductor manufacturing, has introduced its new GenMatch Series that integrates the company's proven solid-state Electronic Variable Capacitor (EVC) RF match and Precis generator technologies into a single unit. The systems have a footprint similar to a match alone, saving space on the process tool, and are faster, more repeatable and more reliable, with lower cost of ownership. GenMatch systems are ideal for leading-edge etch and deposition applications in semiconductor manufacturing, where level-to-level pulsing and short RF on-times are critical to meet performance requirements at the most advanced nodes.

"Reno has a strong track record of bringing novel RF match technology to market, and the GenMatch™ is no exception," said John Voltz, senior vice president of business development at Reno. "The high reliability of our EVC all-solid-state match equals RF generator reliability, making it now economical to put both in the same package. The GenMatch is a true RF power system that delivers plug-and-play performance, a first for plasma processing in advanced semiconductor manufacturing."

The GenMatch platform covers powers from 500W to 10kW and frequencies from 400kHz to 60MHz. The generator supports level-to-level pulsing, while the RF matching network matches impedance on each pulse, meaning every wafer sees the same frequency, unlike frequency sweep. AI and machine learning using the matching network's extensive sensor and sampling capability further enhance system performance.

Benefits offered by the GenMatch Series include:

- Detection of fast transients at the output of the RF matching network. These transients may represent micro-arcing in the plasma chamber that the etch or deposition tool would never identify. Reno's RF generator can then control the power to the chamber to eliminate the micro-arcing.
- The option to fully tune the plasma impedance, compared to standard frequency tuning approaches that can only tune limited plasma impedances, and then only the reactive part of the plasma impedance.
- The ability to provide additional tuning options, such as sequential tuning, where the frequency tuning and EVCTM tuning are done sequentially for faster, repeatable and more stable tuning of the plasma impedance.
- The generator can be set to sweep the frequency to tune the reactive portion of the plasma impedance, for which the EVCTM-based matching network adjusts the capacitance values to tune the resistive portion of the plasma impedance.
- Proprietary, dual-stage heterodyne circuitry that enables a faster slew rate response from the detector stages of the control circuit. This provides a considerably more accurate measurement of pulsed RF signals.

With match and generator about the same size as Reno match alone, the combined unit saves valuable space on the process tool. Additional cost savings are achieved, as only one location is required to facilitize power, water, etc. All-digital units allow for multiple communication protocols, Ethernet, EtherCAT and DeviceNet.

Brewer Science recognized as certified B corporation

BREWER SCIENCE, a global technology company has announced it is now a Certified B Corporation. As a B Corp, Brewer Science is committed to achieving the highest standards of corporate, social, and environmental performance, along with transparency and accountability.

The rigorous certification process recognizes for-profit companies who utilize business as a force for good through exacting standards for social and environmental performance. Brewer Science is the first company in the semiconductor industry to earn this certification and the seventh in the state of Missouri. Brewer Science joins a worldwide network of almost 4,000 Certified B Corps to date, from more than 60,000 applicants across 150 different industries and 74 countries, with one unifying goal: to redefine business success.

Brewer Science completed a meticulous assessment process conducted by B Lab, the governing body of B Corps, which examined over 170 factors while reviewing Brewer Science's customers and vendors, record of inclusion, community involvement, corporate governance and environmental impact. Key elements such as average employee tenure, charitable giving, energy savings plan, recycling policies, employee volunteer service and employee upward mobility are also analyzed. Brewer Science will hold B Corp certification for three years before submitting to a renewal process.

Environmental impact is one of the highest factors Brewer Science scored, valuing the company's efforts in its environmentally innovative manufacturing processes. "Brewer Science remains committed to protecting the environment, conserving resources, and providing a healthy, safe and secure workplace. Environmental responsibility is an ongoing priority at Brewer Science and we are targeting a carbon-neutral footprint by 2030," said Dan Brewer, Chief Resources Officer at Brewer Science.

TESCAN new delayering capability for unattended, automated failure analysis

TESCAN ORSAY HOLDING a.s. has announced the release of the new TESCAN Delayering Module that enables automated gas-assisted top-down delayering using TESCAN SOLARIS X and AMBER X Plasma focused ion beam (FIB) instruments. TESCAN Delayering supports physical failure analysis through the combination of inert Xe plasma FIB ions and unique, proprietary gas chemistries that have been developed specifically for today's advanced technology nodes, creating artifact-free, site-specific trenches—with maximum planarity and homogeneity and without altering a device's electrical properties—for rapid access to deeply buried features or defects.

"Efficiently delayering today's devices requires solutions that are different from the standard gas chemistries or traditional gallium (Ga) FIB technologies that have been used in the past for this application," states Lukáš Hladík, product manager for FIB-SEM in TESCAN's Semiconductor market segment. "With TESCAN Delayering, we have developed a state-of-the-art solution for technology nodes below 10nm, and which also provide the ability for users to customize parameters for their own devices. Predictable, automated and unattended delayering can help with allocating and deploying lab resources. Users can be confident that the delayering process will terminate at the designated layer so they don't need to spend a lot of time monitoring the process."

TESCAN Delayering uses a step-by-step guided wizard to set-up the required delayering process. Factory-defined templates assure consistent application of all delayering parameters. The templates also can provide the starting point for users to develop their own recipes customized to their specific devices. Once the job is set-up, the TESCAN Delayering module executes the process automatically, with the plasma FIB providing rapid material removal, without Ga implantation or beam damage. At any time during the delayering process, users may monitor the progress by using signal peak recognition in the end-point-detection curve. TESCAN Delayering module is supported by a team of skilled applications scientists who can assist with process development and customizations for users who want to further streamline their delayering processes.

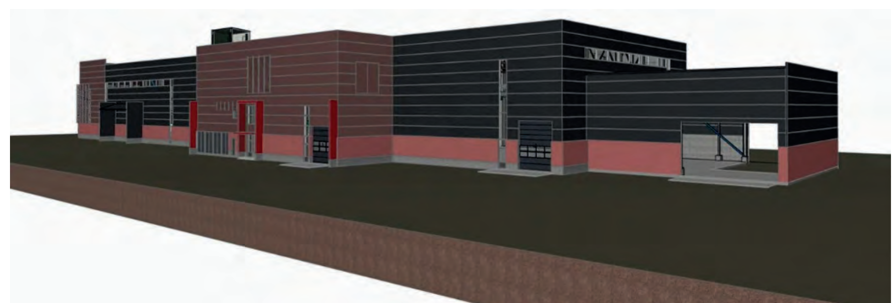
Luvata announces €34M investment in Finland hot extrusion line

LUVATA in Pori, Finland has announced a €34M investment in a new hot extrusion line and facility on its premises in the Pori Copper Industrial Complex. This new 5237-square metre facility will be home to a 130-metre long by 30-metre wide, 55 meganewton (MN) hot extrusion press that includes the latest in robotics and automation.

Construction of the new building includes over 1000 concrete and steel piles to support the 1000-ton hot extrusion press, roughly 5X the weight of a Boeing 747. The building's infrastructure and equipment will enable improved efficiencies in terms of productivity, quality, safety and energy efficiency. The complex installation involves components from Germany, Spain, Czech Republic, and Italy coming to Finland in over twenty truckloads at prescribed times and in designated sequences. "This extremely complex project reflects the technical competence and confidence we have in our employees and suppliers," indicates Jyrki Rantanen, Managing Director of Luvata Pori Oy. "It also reflects Luvata's long-term commitment in meeting the growing needs of our customers."

Luvata Pori Oy produces a wide variety of oxygen-free high-conductivity copper and copper-alloy products including hollow conductors, tubes, wires, strip and other specialty profiles that serve the automotive, electronics, healthcare, mining, power generation and distribution and renewable energy markets. The new extrusion press will double Pori's current capacity and expand available billet sizes, wire sizes and alloys to meet the company's growing demand for high-quality copper-alloy products and solutions.

Construction of the new building is now underway with production estimated to begin in Q2 2022. The new extrusion press will eventually replace Pori's nearly 60-year old 25-meganewton press currently in operation.



Merck meets demanding customer requirements through revolutionary materials science

The continuing evolution of semiconductor devices has challenged materials suppliers to take a more active role in defect elimination and yield enhancement as IC manufacturing grows increasingly complex. **MERCK,** a science and technology company headquartered in Darmstadt, Germany, offers insights into how the company has redefined material science to speed up production, increase yields and provide customers a competitive edge.

DEMANDING PRODUCTION requirements for advanced node semiconductors continue to make the world's most complex manufacturing processes all the more challenging. Flaws that were inconsequential two or three device generations ago today are 'killer' defects in devices at 10nm and below.

As a consequence of ever more stringent process requirements, manufactures and their supporting supply chain members are seeking ways to make the production of advanced node devices as fool-proof as possible. One way to minimize defects requires greater materials purity and precisely controlled formulations that essentially create materials with carefully documented 'fingerprints' for each compound so that batches can be more readily sourced, stored, and tracked from the point that they enter the manufacturing process stream to the very last back end of line steps.

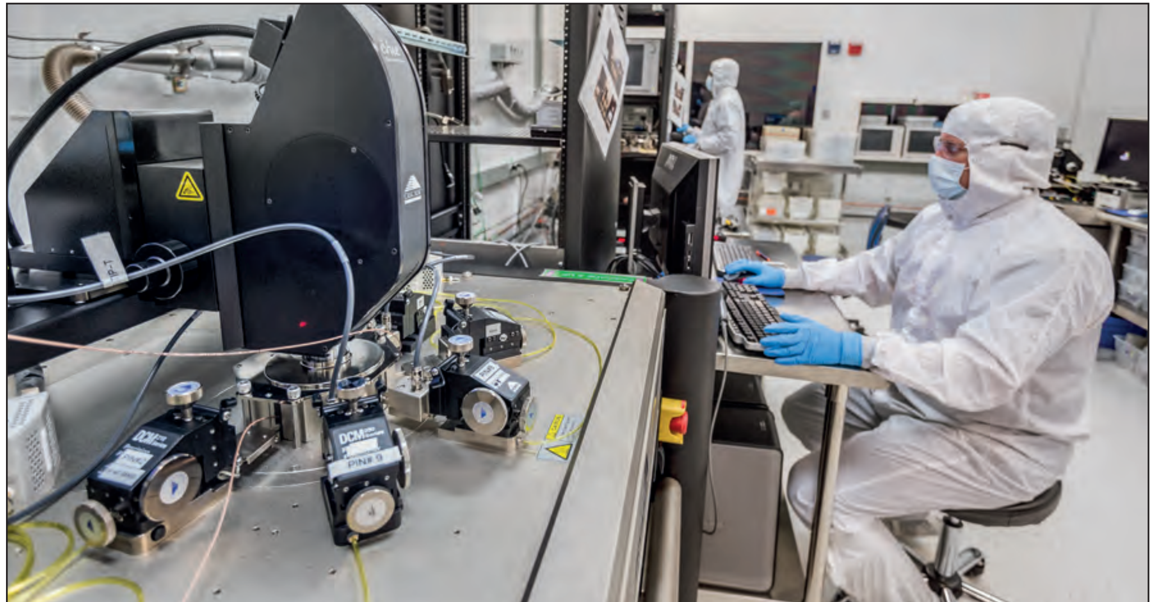
No compound is exempt from constantly improving quality control demands since manufacturers appreciate that the more control they exert over every aspect of a material's composition, the less likely it is that one of those materials might accidentally inject defect-inducing qualities. At stake is billions of euros in microelectronic devices and trillions in end-use products that will succeed or fail based on their semiconductor content.

The continual advancement of materials science has created unique opportunities for suppliers and process chemical manufacturers that already have stringent standards and exemplary quality controls. Such companies are ideally positioned to meet the growing needs of semiconductor device makers. Somewhat like semiconductor manufacturing, the development and formulation of pharmaceutical and life science products require extreme precision and rigorous quality control. So it should come as no surprise that a company known for quality and advanced technology such as Merck would continually invest in its advanced electronics materials division.

Today, Merck has emerged as one of the largest international players supplying high-purity/high-quality semiconductor process chemical formulations to a growing list of global IC manufacturers.

Merck isn't satisfied to rest on its laurels or expect its more than 300 years of industrial excellence to meet every requirement in an ever-changing 21st-century global marketplace. Since 2007, Merck has made acquisitions and divestments totaling around €40 billion – in the process, Merck has transformed itself into a leading science and technology company supporting semiconductor manufacturers in addition to its prominence in healthcare and life science industries.

Recent acquisitions by Merck include bringing Versum Materials into its family of companies in October 2019. In September that same year, Merck completed



its acquisition of Intermolecular, a California-based company focused on advanced materials innovation. Both acquisitions added products, processes, and a wealth of experience to Merck's already deep well of high-performance materials expertise.

Following completion of the Versum acquisition, former Chairman of the Executive Board and former CEO of Merck, Stefan Oschmann remarked, "By acquiring Versum, we will be optimally positioned to capitalize on long-term growth trends in the electronic materials industry. At the same time, we are broadening our commitment to electronic materials, balancing our portfolio with three strong business sectors and sharpening our strategic focus on innovation-driven technologies."

Echoing those remarks, Kai Beckmann, Executive Board member of Merck and CEO of Electronics said, "We are very pleased to welcome Versum to our team. After the most recent acquisition of Intermolecular, this closing marks another major milestone on our Bright Future transformation journey to become a leading player in the electronic materials market. The expertise of our combined business will enable us to offer customers in the electronics industry cutting-edge technology innovations."

In all its acquisitions, Merck has sought to add strategic advantages that complement its existing global portfolio. Amongst key benefits of its 2019 acquisition of Intermolecular was an opportunity to relocate the Merck Silicon Valley Innovation Hub team in Menlo Park to Intermolecular's 150,000 square foot facility located in San Jose, California. Much more than just a consolidation, the move to San Jose allowed Merck to take advantage of Intermolecular's 30,000 square feet of cleanroom, chemical laboratories, offices, meeting and event spaces in a way that not only benefitted Merck, but also created a unique space to empower collaboration with startup companies focused on advanced materials and support services for semiconductor manufacturing.

"The mission of the Silicon Valley Innovation Hub is to identify and explore untapped innovation and business opportunities for Merck. In this context, the intersection of life science and material science is becoming increasingly important and opens new areas of innovation. Having the Silicon Valley Innovation Hub and Intermolecular under one roof now will allow us and our cooperation partners to develop and test new materials for biological applications. We are very excited about these new opportunities," stated Thomas Herget, head of the Silicon Valley Innovation Hub, on the occasion of the move by Merck staffers to San Jose in March 2021.

Materials science can and does play a decisive role in the fabrication of next-generation semiconductors. Products and processes that may have previously been considered secondary to the success of a new wafer production step have now proven critical. Equally important is the need for manufacturers to understand and appreciate exactly what constitutes a successful new material or process compared to legacy approaches.

One area in which Merck continues to excel and set new standards involves delivering superior materials as well as better performance data compared to competing approaches. A ready example can be found in the chemical mechanical planarization (CMP) technologies that are utilized throughout the transformation of a bare silicon wafer into a substrate bearing finished devices at high yield with high performance. Amongst its many functionalities in device manufacturing, CMP plays a critical role in producing finished copper interconnects. In production, sheet resistance (Rs) of copper interconnects are measured after the barrier layer is removed by copper/barrier CMP.

But generally speaking, this analysis is not available in the laboratories of consumable CMP suppliers.

A combination approach to measuring the effectiveness of CMP on copper interconnects is to examine dishing and erosion following planarization completion. Ordinarily, only dishing is analyzed in part due to the challenges of measuring both qualities.

Merck has found that as feature sizes become even smaller, traditional CMP metrology becomes more time consuming, noisy and challenging. Hence, electrical testing provides the most comprehensive, accurate, and reliable dataset. Merck performs back end of line (BEOL) copper and copper-barrier CMP slurry testing on an electrically capable test vehicle. The test vehicle is then sent to the company's in-house electrical characterization laboratory.

An automated high-throughput program can be used to probe the test vehicle. For example, 16 features across 32 dies can be measured in four hours, whereas by physical methods (AFM, profilometer), only 11 features across three dies can be measured, which typically takes double the time, (i.e., 8 hours.)

Merck can provide such data to customers upon their request; other CMP suppliers do not have access to such electrical characterization, and typically lack expertise in electrical data analysis. Merck's approach was developed in concert with customers to ensure that the data made available is not only useful, but provides the manufacturer with an 'edge' compared to other approaches to characterizing post-CMP effectiveness.

One company that has partnered with Merck is UMC Fab12i (Singapore.) Fab Director Steven Hsiao shared his opinion that the accelerated success of a recent wafer run could be tied not only to the support of his internal engineering team and production technicians, but also the direct support of Merck in assessing the performance of their CMP copper planarization processes. "We believe that anything is possible if we work together, and we look forward to working with Merck again on our next project," said Hsiao.

For BEOL copper bulk slurries, Merck products offer the following advantages:

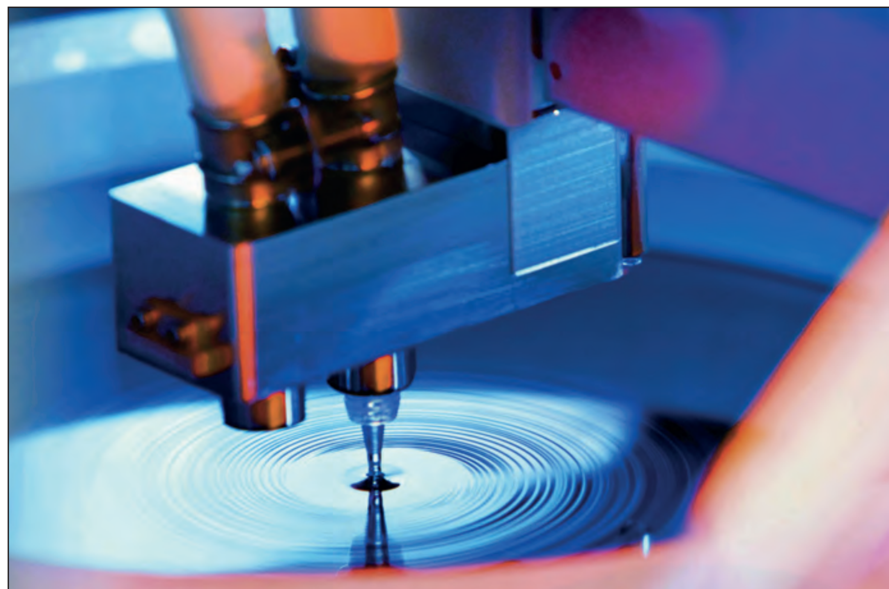
- Residue-free & 100 percent copper clearing due to low additives
- Tunable profile and dishing to meet customer's technical requirements, low step-height to large step-height
- Low abrasives to provide low defects
- No pad stains
- High selectivity
- Slurry in corrosion-free regime of the Pourbaix diagram
- Newtonian and Prestonian behavior for predictability across consumable sets

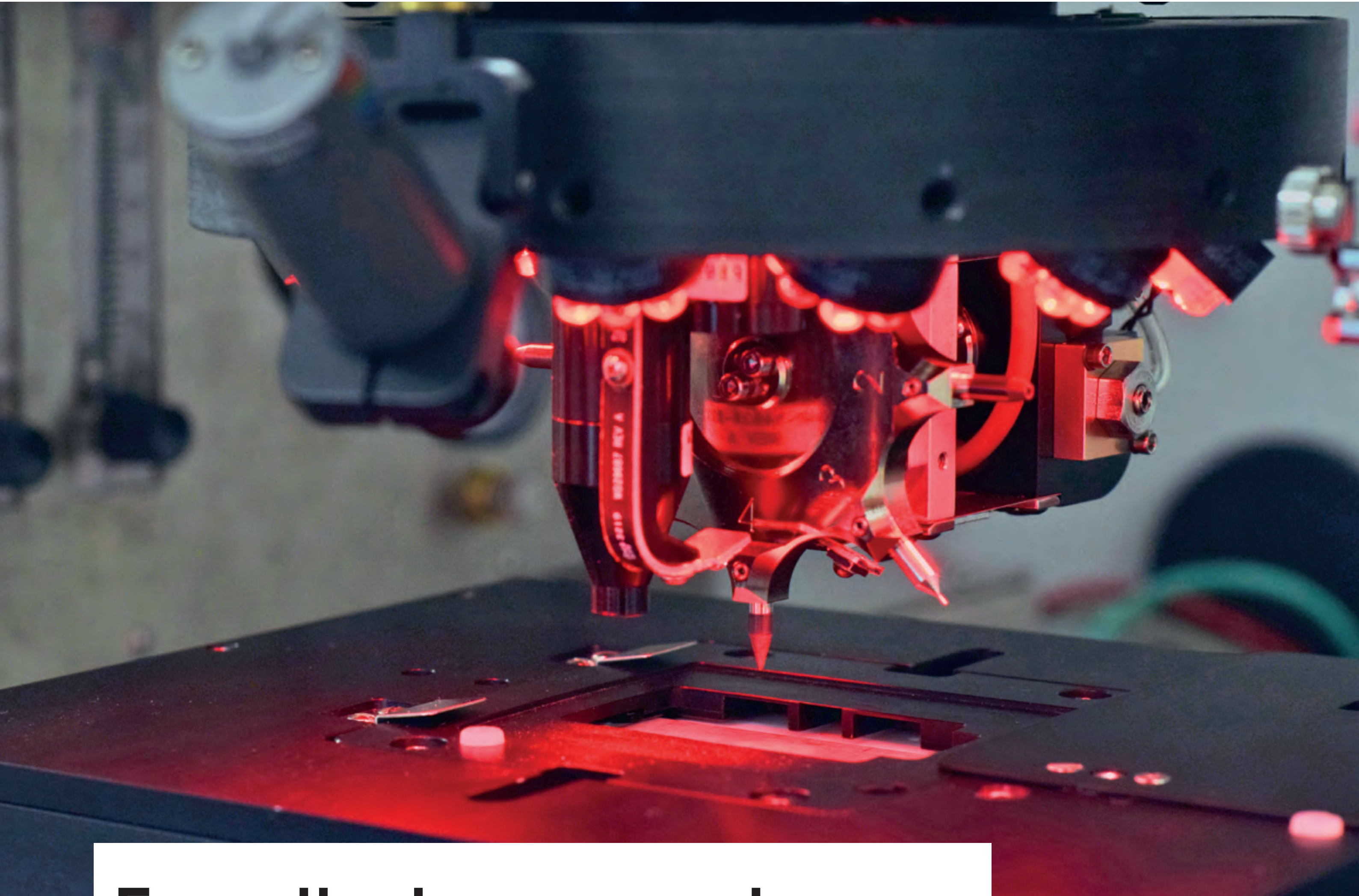
For BEOL copper barrier slurries, Merck products offer the following advantages:

- Customized tunable selectivity, working with customer-specific requirements
- Low defectivity
- Superb topography control
- More concentrated formulations
- Compatible with novel liner schemes

"Merck is pushing boundaries to create next-generation CMP slurries which revolutionize the semiconductor industry. The integration of Merck and Intermolecular provides more value to customers and enables us to partner with customers to solve current and future integration challenges. For example, Merck developed its new, innovative CMP slurries and can provide dishing/erosion (physical) data of materials as well as electrical data to measure CMP slurry performance. This preview of electrical data minimizes risk, maximizes yield and shortens cycle time for our customers, which also demonstrates Merck to be a total solutions provider. At Merck, we are striving to respond quickly to industry challenges. We aim to deliver the total solution, and strive to be the preferred partner for our customer's future needs," said Laura Matz, the Chief Science and Technology Officer at Merck.

In an effort to continually improve its already industry-leading approach to combining high-performance materials with actionable performance data, Merck is also examining the development of novel abrasives and the ability to modify the surface of abrasive constituents so that materials are effectively customized to a manufacturer's unique needs and requirements. This is a key element of topography and defect control that will continue to grow in importance as the industry moves from one device generation to the next. Merck has set its sights on leading the semiconductor materials industry; Merck is well down the road to accomplishing its goal.





For die in a package
it's always about the bond

Semiconductor production is so complex that manufacturers constantly seek to reduce costs and improve performance. As advanced node devices continually shrink, process complexity, cost and risk also multiply. Silicon Semiconductor spoke with the experts at Palomar Technologies to learn how die bonding continues to evolve and play a central role in II-VI, III-V, photonic and hybrid module manufacturing.

THE UNIVERSALITY of some semiconductor processes points to their essential nature across technological platforms. Even as device form factors, lithographic innovations, defect management and performance enhancement techniques come and go, there remain some steps that are always needed including the requirement to place finished die inside a receptacle that will protect it and enable its functionality.

As nodes advance to smaller feature dimensions, manufacturers are keenly aware of the growing importance of finely tuning process steps and material formulations to aid in defect elimination and quality

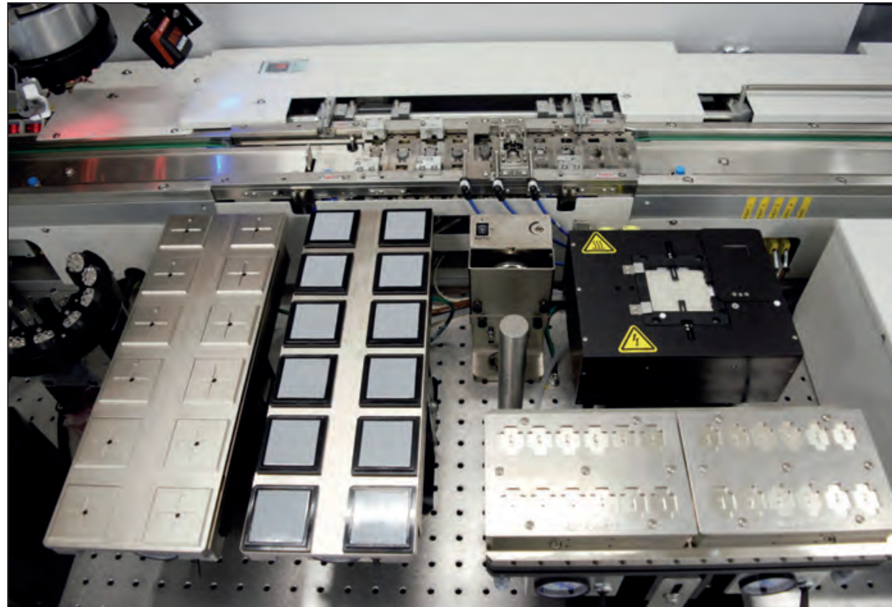
control while improving product lifetimes / adding value. This attention to details pays dividends that include enhanced profit margins, faster time to market and reduced cost, not to mention overall customer satisfaction.

Die bonding is a prime example of how a technology that has been a part of semiconductor production predating the advent of widespread automation has continued to evolve and bring value to complex manufacturing systems. In a recent conversation with Palomar Technologies' Kyle Schaefer, product marketing manager, Silicon Semiconductor technical editor Mark Andrews spoke about ways that die bonding has evolved, and how advances in the field can contribute to balancing the need for high throughput along with process control. This versatility benefits very diverse products that can range from filters to power amplifiers to photonic assemblies.

Schaefer noted that one measure of how die bonding continues to evolve can be found in the RF power amplifier market, which is expected to increase substantially in the next five years. This expectation is rooted in the need to support 5G service rollouts that depend heavily on new power amplifier assemblies in base stations. The estimated CAGR for the general RF power amplifier market is 5-6 percent from 2020-2025. This anticipated demand translates into a need for manufacturers to increase their production capacity. But unlike previous generations, 5G technology is different than the more evolutionary transitions seen as 2G became 3G, which begat 4G; a simple production ramp will not address all 5G needs since volumetric growth carries with it new challenges as well as new processes that need to be developed and refined.

5G vendors must simultaneously churn out considerably more devices while dealing with design, material, and process faults. There is also a great deal at stake in terms of long-term supply chain relationships—5G technology is the foundation of new, wide-ranging commercial initiatives including the opportunity to use wireless networks to fill gaps in wireline networks or supplant fixed broadband access. In the mix are new amplifier designs at higher frequencies and new technologies along with all the usual pressures to ramp-up volumes. A misstep during the early stages of a build-out expected to take a decade or more could freeze-out a manufacturer from future business. Poor execution in terms of yield, quality, or product reliability could indeed prove quite costly if future business tenders fail to convert into design wins.

RF power amplifiers are worth examining in the context of die bonding due to the mixed technologies being utilized. While not as different as requirements for photonic assemblies, there are substantial differences between amplifier types, principally divided between die utilizing LDMOS technology and



components based upon newer technologies such as gallium nitride (GaN) on silicon carbide (SiC). While LDMOS is considered mature, GaN on SiC has been a mainstream product for a fraction of the LDMOS tenure. GaN-based amplifiers also serve a substantially different frequency range (3.5 GHz and above), and due to its significantly greater power density, the most important metric for assessing a successful bond for GaN amplifier die comes down to thermal management.

"Ensuring high thermal conductivity of the bond between the chips and the transistor package is paramount to the longevity and performance of the device. Beyond that, the build requirements vary based on assembly approach and materials used," Schaefer noted. In addition to the thermal management requirements, GaN devices are also more fragile and come at a higher cost than similarly sized LDMOS devices. Due to their fragility and susceptibility to surface damage, pick-place-bond sequences for GaN die need greater care during handling and bonding.

In addition to very significant differences between LDMOS and GaN that affect handling and die attach methodologies, the second most important division concerns the actual assembly and die attach material options. There are a host of choices available, each designed to deliver voidless bonds with high strength and longevity appropriate to the underlying die technology. An important related aspect of die bonding is the vision system used to not only ensure highly accurate and consistent placement, but also help maintain quality while collecting data to ensure damage-free placement of each die. Using Palomar Technologies 3880 Die Bonder as a reference, Schaefer explained ways that industry's latest bonding systems deliver performance that was previously not possible.

Often a simple active process control step consisting of a single reference can be enough to prevent repeated misplacement or consecutive component damage

"For preventing component damage in general, or even simply just monitoring die placement, the die bonder vision system can be used to great effect. Often a simple active process control step consisting of a single reference can be enough to prevent repeated misplacement or consecutive component damage. This can be achieved by using a unique feature of the VisionPilot® referencing system referred to as the ability to 'score clutter'. Essentially, the pattern recognition algorithms can use excess data (i.e. clutter) which comes from debris, chips, and scratches, to lower the given 'score' for a reference. This allows rejection of die based on damage or cleanliness."

"Using this technique before beginning any assembly allows for die sorting during the actual build process to prevent any waste of material. It is also possible to use this same 'chip damage check' after placement to avoid any instances where damage was done through any debris collected on the vacuum tool – a situation that, when left unchecked, could result in consecutive device destruction until noticed much later down the line. This control step can also simultaneously check for die placement repeatability in terms of X, Y, and Theta, further adding to the complete control options available," Schaefer explained.

While some process tools come and go depending on the die generation, others evolve since the need to perform a given function like wafer manipulation remain even as wafer diameters change, die grow smaller, or substrate materials vary in crystalline structure, thickness and fragility. Yet the underlying need to move wafers along a processing line remains even as other factors change. The same could be said with die bonding, hence the favored approach of building a process tool that evolves rather than enters production with only a limited lifetime.

The idea of flexible evolution was central to the development of Palomar Technologies 3880 Die Bonder. Schaefer explained some of the highlights of the system's enduring and wide-ranging appeal.

"Flexibility is key to providing a strong ROI across many business models from academia, SME's, CM's, to full scale manufacturing giants like Lumentum & II-VI. Typically, Palomar customers keep Palomar bonders for many years, so longevity of support and the ease of reconfiguration as products and processes mature and change is a major consideration for engineers and procurement professionals when investing in bonding solutions."

"Specifically, flexibility is one of the core design philosophies of the Palomar 3880. The flexibility of the system is unique in that it offers the capability to easily change from one process or configuration to another while also remaining effective in its performance for all potential applications."

"It is not just the 8-position, bi-directional tool turret, which only takes 250ms to change tools on the fly, that makes the 3880 extremely flexible. It is the extra-large work envelop where many configurations of bonding hardware, material presentation options and automation options can be utilized. In addition, the changeover is rapid and effortless which supports any company's need for high mix."

"Essentially, the robust abilities of the software and hardware are the core functionality that make the flexibility of the 3880 so impactful, in that it is not just great in one area and good in many others, but it is great in all areas. The 3880 is an R&D, NPI and volume production machine all in one," Schaefer stated.

As semiconductor processes and manufacturing goals change with succeeding device generations, some needs remain constant, like the requirement to pick and place die, then create a permanent, robust bond between the device and its package. The Palomar 3880 remains a centerpiece of both research and all manner of production environments. Sometimes, the best products just keep getting better.

Micromachining Excellence

New: Laser Contract Manufacturing

Whether standard system or special solution:

High-Performance & Reliable
Laser Micromachining Solutions for

» Roll-to-roll laser processing of flexible substrates
» Laser drilling, cutting, structuring, modification, ...
» Almost any application and substrate

Contact us now!

3D-Micromac AG
Tel: +49 371 40043-222
sales@3d-micromac.com

WWW.3D-MICROMAC.COM

Ensuring the reliability of electronic devices through non-destructive testing of specialty metals & materials

Non-destructive advanced scanning acoustic microscopy detects flaws in specialty metals, materials, and packaging of semiconductor devices.

MANUFACTURERS of high-end semiconductor electronic products used in consumer, industrial, and military applications have long relied on precise testing methodologies to identify the location of defects such as voids, cracks, and the delamination of different layers within a microelectronic device, also known as a Chip.

Manufacturers employ a range of other techniques: scanning acoustic microscopy (SAM), a non-invasive and non-destructive ultrasonic testing method, has become an industry standard to detect and analyze flaws during various chip production steps and in the final quality inspection after packaging.

In addition, SAM is often utilized as a Failure Analysis method when needed to identify a specific root cause failure mechanism when a device fails during use.

Beyond semiconductor components themselves, today's electronics products contain various specialty metals, alloys, plastics, and glass components. All semiconductor components need to be enclosed and packaged in consumer usable formfactors. As a result, SAM equipment has evolved and is now being used to detect subsurface flaws, dis-bonds, cracks, and other irregularities in these types of materials that constitute "packaging" of semiconductor components.

With the same rigor of failure analysis and quality testing used for semiconductors now being applied to metals and alloys, both the production yield and overall reliability of electronic devices have improved significantly. In doing so, projects are completed in less time while eliminating potential points of failure in the field.

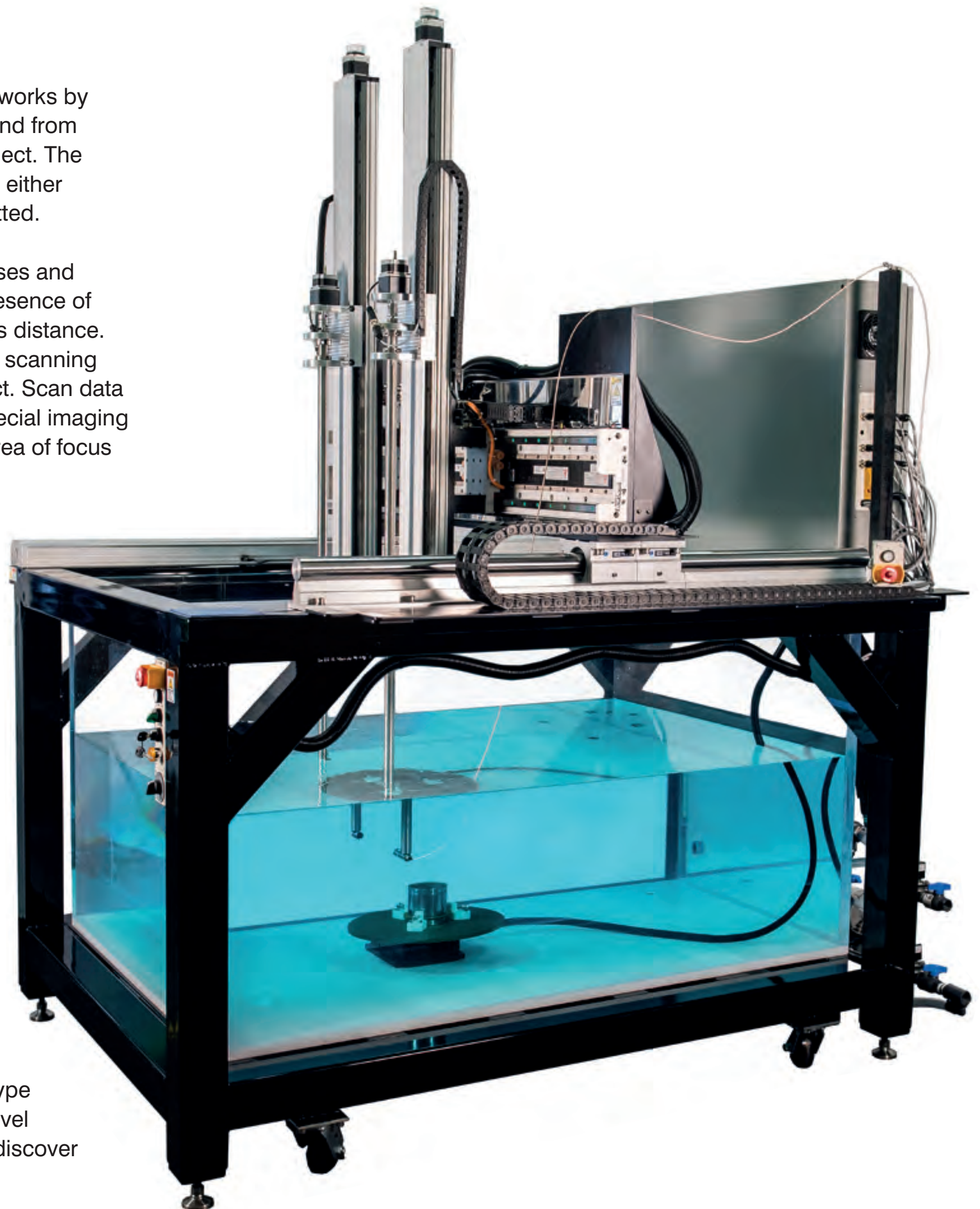
"The reality is that a failure in an electronic product package or a non-semiconductor component can be just as catastrophic as a failure with the semiconductor," said Hari Polu, President of OKOS, a Virginia-based manufacturer of SAM and industrial ultrasonic non-destructive (NDT) systems. The company serves the electronics manufacturing, aerospace, and metal/alloy/composite manufacturers, and end-user markets.

Detecting Flaws with SAM

SAM is a powerful non-invasive and non-destructive method for inspecting internal structures in optically opaque materials. Depth-specific information can be extracted and applied to create two- and three-dimensional images without the need for time-consuming tomographic scan

procedures and more costly X-rays. SAM works by directing focused ultrahigh frequency sound from a transducer at a tiny point on a target object. The sound as it passes through the material is either scattered, absorbed, reflected, or transmitted.

Detection of the direction of scattered pulses and measuring the TOF "time of flight," the presence of a boundary or object is determined and its distance. Three-dimensional images are created by scanning point by point and line by line on an object. Scan data is digitally captured and processed by special imaging software and filters to resolve a specific area of focus in either single or multiple layers.



According to Polu, the industrial sector has traditionally utilized other methods considered inferior compared to what is being used in today's semiconductor industry. However, with SAM equipment, specialty materials manufacturers can achieve the same level of failure testing to the companies that make metals, alloys, composites, and titanium plates used in electronic devices.

"OKOS has leveraged the lessons and the tight specifications from the semiconductor world and adapted our SAM scanning systems for various form factors and provide unique solutions for specialty crystalline, metals, and other material for our customers in the industrial markets," said Polu. "With this type of testing, we can inspect materials at a level one to two orders of magnitude better to discover flaws that were previously undetected."

Today, much of the SAM equipment can inspect various items with unique product geometries or sizes, from crystal ingots, wafers, and electronics packages to miniature physical packaging, metal bar/rods/ billets, turbine blades, etc. However, as important as the physical and mechanical aspects of conducting a scan, the software is the key to analyzing the information to produce detailed scans.

For this reason, "OKOS decided early on to deliver a software-driven, ecosystem-based solution," said Polu. The company's ODIS Acoustic Microscopy software supports a wide range of transducer frequencies from 2.25 to 230 MHz.
Multi-axis scan options enable A, B, and C-scans, contour following, off-line analysis, and virtual rescanning for composites, metals, and alloys, which result in highly accurate internal and external inspection for defects and thickness measurement via the inspection software.

Polu estimates that their software-driven model enables them to drive down the costs of SAM testing while delivering the same quality of inspection results. As a result, this type of equipment is well within reach of even modest testing labs, R&D centers, and material research groups.

"Every company will eventually move towards this level of failure analysis because of the level of detection and precision required for specialty metals and materials," says Polu. "The cost advantages and time savings of Industrial SAM equipment make this possible."

SAM systems have an integral role in semiconductor device manufacturing based on their precision, usability, and time-saving advantages compared to other NDT options. Extending this testing methodology beyond semiconductor components to specialty metals and materials throughout a semiconductor device can provide more robust failure detection capability for manufacturers of consumer, industrial and military electronic devices.

Benefits of plasma dicing technology

Plasma dicing addresses the challenges of dicing smaller and thinner dies; enables higher throughput and increased yield per wafer.

BY SHOGO OKITA, NORIYUKI MATSUBARA, ATSUSHI HARIKAI, AND JAMES WEBER, PANASONIC CORPORATION

IT COULD BE ARGUED that the defining feature of the Electronics Industry is the ability to miniaturize. Every person with a passing interest in electronics has heard of Moore's Law: the processing power of affordable CPUs – or the number of transistors on a chip - will roughly double every two years. It is credit to both Gordon Moore's foresight, and the technical and engineering teams around the world who continue to innovate, that the 'Law' is still even being discussed today. Part of the reason for chip size reduction lies in the shrinking of technology nodes (process geometries). Currently the smallest node that is being manufactured in mass volume is 7nm, and even the smaller size is under development in the industry. The increase in processing power and speed and the miniaturisation and integration of electronic functions that continue to result from such technological advances lie at the heart of the pervasiveness of electronics in our everyday lives: the smart phones that we rely on; the uptake of artificial intelligence in smart homes and cities; driverless vehicles; remote medical home diagnostics – there is not one aspect of life that electronic products and systems have not penetrated.

APX300 Plasma Dicer

But for this to continue, it is not only in the area of photolithographic processing that technology needs to keep innovating. Once a wafer has been created it must be singulated into individual dies, and as dies are becoming smaller and thinner, many products are facing difficulties caused by the singulation or dicing process. New challenges include: increasing material loss due to the width of the dicing street; mechanical damage such as chipping; and increasing processing time. Now, Panasonic has developed a plasma dicing process that in certain circumstances can replace mechanical dicing, which addresses these issues.

Types of Dicing Process

Traditionally, two dicing technologies have been used: scribing and breaking, and mechanical cutting using a dicing saw ("blade dicing"). Scribing and breaking causes stresses on the wafer and die and results in chipping and yield inefficiencies. Blade dicing also introduces stresses and contaminants which are more problematic as the die size and process geometries shrink. Laser dicing is another method which is faster than using a saw, but can also cause cracking and damage to the chip.

Now, a new dicing process has been introduced which uses a plasma chemical etching process, where all the 'cuts' are achieved in a single batch process, with no die stressing, no contamination, and an increase in wafer dicing throughput. Also, more chips can be designed onto the wafer as narrower dicing 'streets' can be used due to mask patterning. In addition, the

mask pattern enables flexibility in the choice of chip sizes, shapes, positioning. The two approaches are shown in Figure 1.

Figure 2 shows Panasonic's plasma dicing process which uses a dicing mask. The plasma process etches the streets by chemical reaction. Plasma dicing uses pulsed or time-multiplexed etching, with the process cycling repeatedly between two phases: a near-isotropic plasma etch where ions attack the wafer in a near-vertical direction; followed by the deposition of a chemically inert passivation layer which protects the entire substrate from further chemical attack. During etching, the vertically-directed ions attack the passivation layer only at the bottom of the trench (not along the walls), exposing the substrate to the chemical etch. This two-phase process results in side-walls that increase and decrease with an amplitude of between 100 and 500nm. The cycle time is adjustable: short cycles yield smooth walls; longer cycles yield a higher etch rate.

Advantages of the plasma process over mechanical dicing

The action of the saw blade during the dicing process causes mechanical damage and affects inner layers of the die. Figure 3 demonstrates damage and chipping at the edge and of the inner layers. By contrast, the micro-photographs show no damage when the individual dies are separated using the plasma dicing process. Also, unlike blade dicing which causes micro particles of the wafer (e.g. silicon) to be freed up, potentially causing devices to fail, by using plasma etching, no contaminating particles are released.

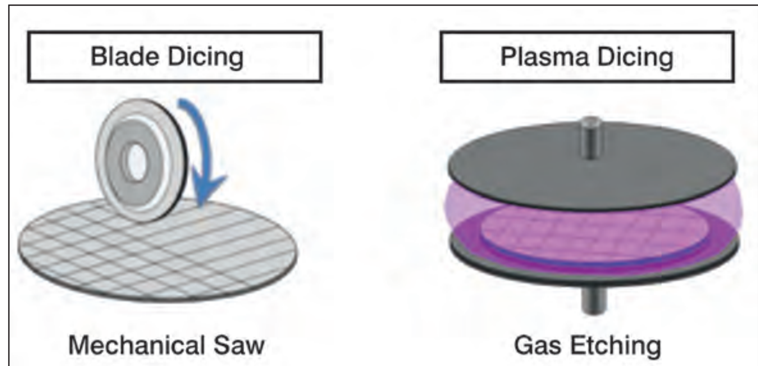


Figure 1. Blade Dicing & Plasma Dicing Processing

Greater chip strength

Chip breakage tests show the typical range of fracture strength for silicon chips to be in the range of 100MPa up to 3000MPa. Dies from several positions on a 150μm thick wafer were sampled and a Weibull plot was used to compare the statistical data for chip strengths of lots using blade and plasma dicing preparation methods. Figure 4 shows that the plasma dicing process results in chips that are about five times stronger than those which underwent blade dicing. With a fracture stress pressure of 600MPa, all samples of chips that had been processed using blade dicing broke due to internal micro-cracks, whereas all of the plasma diced chips shattered at a pressure close to the breaking-strength of silicon.

Figure 2. Panasonic's chemical etch dicing process

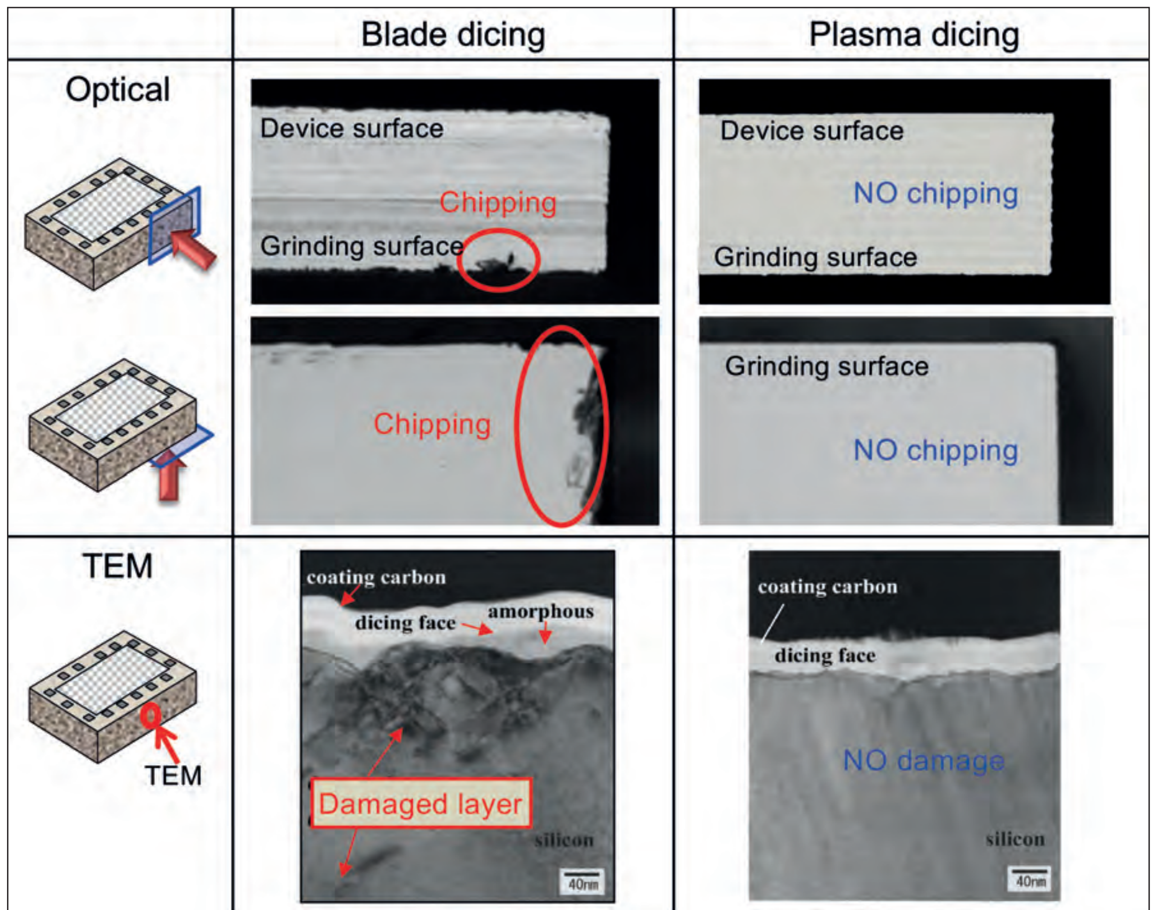


Figure 3. Damage evident on chip samples using blade dicing (left); none present when plasma dicing is used

Therefore the plasma dicing process is proven to result in dramatically higher chip strength, especially if thin wafers are being processed.

Higher throughput and yield

The processing time of blade dicing depends on the number of dicing lines. If the die size is small, longer dicing processing time is required and throughput is reduced. However, with the plasma dicing process, etching is performed across the whole wafer in one pass, so throughput remains constant, no matter how many dicing streets are required (see Figure 5).

In addition, the plasma dicing process uses a narrower dicing street design. With blade dicing, there is always a minimum cutting street width, due to the thickness of the blade. A simulation prepared by Panasonic shows that for a 0.5mm² chip size, reducing the dicing street width from 60µm to 5 µm, yield will be increased by 23% using the new plasma process. (See Figure 6).

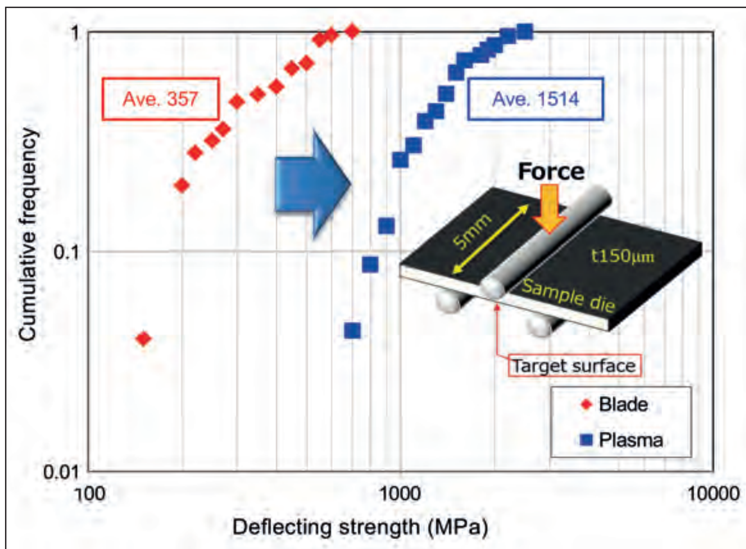


Figure 4. Strength tests prove the benefits of plasma dicing

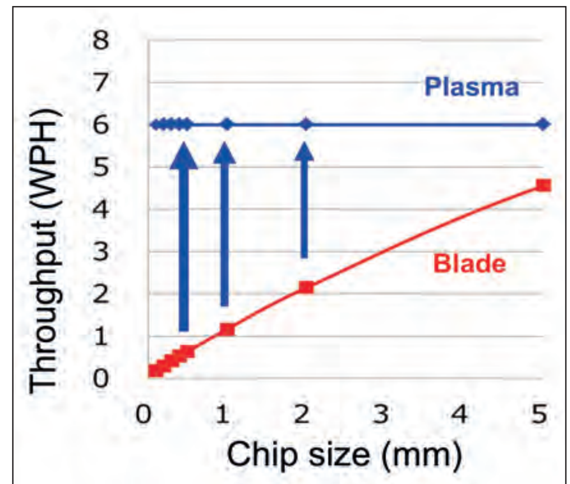


Figure 5. Productivity curves show increasing benefits with smaller chip areas

Dennis Ralston
Sr. Director –
Government Relations and Cooperative R&D
KLA

YOU HAVE
A VOICE.

WE MAKE
SURE POLICY
MAKERS
HEAR IT.

Learn how SEMI Advocacy represents the industry with governments worldwide.

We amplify the voices of individual members and transform them into policy positions. To explore the ways we advance the health and prosperity of the global electronics design and manufacturing supply chain, visit **semi.org/semiismore**.

SEMI IS MORE

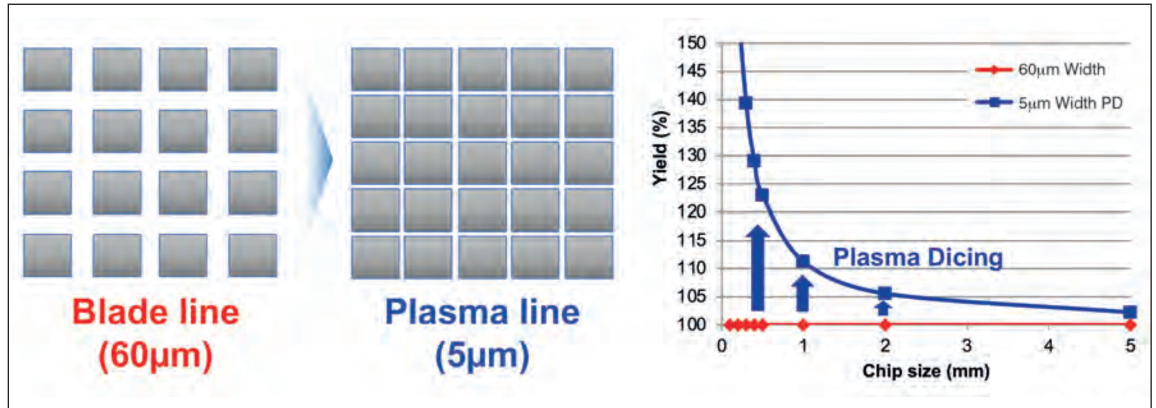


Figure 6. reduced street widths result in more chips/ wafer

But how to avoid chips to contact others when handling wafer with 5 um dicing street width needs to be considered.

Suitability for different wafer processes

The Panasonic plasma dicing process can be applied to wafer dicing with mask patterning either performed by photolithography or laser patterning methods. The appropriate process flow should be selected to fit the wafer design (Figure 7).

Plasma dicing is a high quality innovation which offers different benefits depending on the end application, as shown in Figure 8. In small chips, for example, RF ID tags, IoT devices or MEMS sensors, the ability to obtain a higher number of chips per wafer, plus the reduction in process time is paramount. For devices such as image sensors, the elimination of contaminating particles is essential, and the smoother, damage-free sidewalls, with no heat-affected zones or cracking, allows an increase in the active area. For makers of memory ICs, the elimination of damage is most significant.

Panasonic Demo Centre

In order to demonstrate the plasma dicing process, Panasonic has built a customer demonstration centre in Osaka, Japan. This Class 1000 facility is capable of processing 200mm and 300mm diameter wafers with a minimum thickness of 25μm. It is fully-equipped including two APX300 plasma dicing machines, laser patterning equipment, polish grinder, lithography and measurement equipment, enabling customers to quickly and thoroughly evaluate different products and materials.

Two processes cover target applications

Application	Chip size	Wafer Structure	Process: Mask formation		Process: Dicing
IoT Small Chip	Small (~3mm)	Mask, Si → Plasma Dicing, Si	Photolithography: Coat/Expo.	Liquid: Develop.	Plasma: Dicing
Image sensor / Memory /Logic	Large (3mm~)	Mask, Laser Patterning, Metal/ Low-k, Si → Plasma Dicing, Si	Mask Coating: Resist, Spin or spray coating	Laser: Cut mask & Metal layer	Plasma: Dicing

Figure 7. Panasonic plasma dicing process Applications

SILICON SEMICONDUCTOR

Connecting the Silicon Semiconductor Community

ONLINE ROUNDTABLE

- Based around a hot topic for your company, this 60-minute recorded, moderated zoom roundtable would be a platform for debate and discussion
- Moderated by an editor, this can include 3 speakers
- Questions would be prepared and shared in advance
- There would be an opportunity to view and edit out any unflattering bloopers

This event would be publicised for 4 weeks through all our mediums including:

- A banner on the Silicon Semiconductor homepage for 8 weeks 4x weekly dedicated HTMLs
- 4x news pieces which would also appear on the weekly e-newsletters
- Promoted through our social media platforms for 8 weeks (pre and post event)
- Available as an on-demand asset through all mediums
- All registered attendees' details would be made available to you

Cost: £4995

Contact: Jackie Cannon
jackie.cannon@angelbc.com

Target Application	Blade Dicing Issues	Benefits of using Plasma Dicing	
IoT Small chip ·RF-ID tag ·Chip component ·MEMS etc.. (0.1 mm, 0.2mm)	Wider dicing lane (W 60µm)	Narrower lane (W 5µm) → More chips from a wafer	Blade (60µm) → Plasma (5µm)
	Longer process time in smaller dies	Shorter process time →lower COO	Line-by-line → Whole wafer
Image Sensor	Particle from blading, less yield	Particle free →improve yield	Blade (NG chip) → Plasma
Memory (Memory, CPU, 25µm)	Chipping/die breakage due to damage	Damage free chip obtained →new value for end user	Blade: Damage → Plasma: No damage

Figure 8. Benefits of Plasma Dicing

Conclusion

Panasonic's plasma dicing process achieves damage-free and particle-free dicing, resulting in inherently stronger chips and increased yield. Throughput is increased and production costs reduced. Figure 9 summarises the different dicing processes and the advantages of the plasma dicing process.

All the data in this white paper have been verified in Panasonic's Plasma Dicing Demo Centre in the company's Smart Factory Solutions facility in Osaka, Japan, using the APX300 plasma dicer. Panasonic are continuing to develop the plasma dicing process for other materials such as silicon carbide, gallium arsenide and gallium nitride as well as silicon dioxide.

Product Information

Panasonic can provide a plasma dicing total solution to achieve a damage-free, particle free, higher throughput and lower overall cost of production.

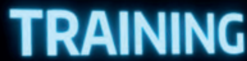
Panasonic Industry Europe GmbH
Caroline-Herschel-Strasse 100
85521 Ottobrunn, Germany

Tel. +49 89 45354-1000

microelectronics.sales@eu.panasonic.com
http://pfse.panasonic.eu

	Blade	Laser	Plasma
Dicing method			
Processing time (8"wafer, t 100µm, □1mm)	✗ (32 min / wafer)	✓ (13 min / wafer)	✓ Shortest (7 min / wafer)
Chip strength	✗ (Mechanical damage)	✓ (Mechanical damage)	✓ Highest (Damage-free)
Low-k etching	✗ (Wet process)	✓ (Dry process)	✓ (Dry process)

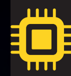
Figure 9. Summary comparison of dicing processes



Angel
BUSINESS COMMUNICATIONS

Specialists with 30 year+ pedigree and in-depth knowledge in these overlapping sectors:

Expertise: Moderators, Markets, 30 Years + Pedigree
Reach: Specialist vertical databases
Branding: Message delivery to high level influencers via various in house established magazines, web sites, events and social media


Semiconductor (Silicon/Compound)
Publications include: Compound Semiconductor, Silicon Semiconductor, CS China, SiS China

Power Electronics
Publications include: Power Electronics World

Future Mobility
Publications include: TaaS Technology, TaaS News

Data Centres
Publications include: DCS Europe, DCS UK, SNS International

SmartSolar UK & Ireland
Publications include: Solar and Power Management, Solar UK and Ireland

Sensors
Publications include: Sensor Solutions Magazine, Sensor Solutions International

Digitalisation
Publications include: Digitalisation World, Information Security Solutions, Managed Services

Photonics
Publications include: PIC Magazine, PIC Conference

Expert Moderators

Dedicated technical and time-served experts/editors

MARK ANDREWS
Mark Andrews is technical editor of Silicon Semiconductor, PIC Magazine, Solar+Power Management, and Power Electronics World. His experience focuses on RF and photonic solutions for infrastructure, mobile device, aerospace, aviation and defence industries

PHIL ALSOP
Journalist and editor in the business to business publishing sector for more than 30 years currently focusing on intelligent automation, DevOps, Big Data and analytics, alongside the IT staples of computing, networks and storage

JACKIE CANNON
Director of Solar/IC Publishing, with over 15 years experience of Solar, Silicon and Power Electronics, Jackie can help moderate your webinar, field questions and make the overal experience very professional

DR RICHARD STEVENSON
Dr Richard Stevenson is a seasoned science and technology journalist with valuable experience in industry and academia. For almost a decade, he has been the editor of Compound Semiconductor magazine, as well as the programme manager for the CS International Conference

For more information contact:

Jackie Cannon **T:** 01923 690205 **E:** jackie@angelwebinar.co.uk **W:** www.angelwebinar.co.uk
6 Bow Court, Burnsall Road, Coventry, CV5 6SP. UK
T: +44(0)2476 718 970 **E:** info@angelbc.com **W:** www.angelbc.com

System level test enables a paradigm shift for device manufacturers

According to research conducted by AEM Singapore, the semiconductor industry needs continuously improved faults coverage while reducing the overall costs of test and measurement operations to enable better, more efficient defects detection while improving quality and overall yield. **BY STUART PEARCE, AEM HOLDINGS, SINGAPORE**

FAULTS COVERAGE is becoming more problematic as systems are getting more complex, heterogeneous and applications are more demanding. Applications such as self-driving cars, cloud servers, AI, industrial IOT or medical devices are now mission critical to many end use sectors, driving the need for low parts per billion (PPB) defect levels.

Advanced Driver Assistance Systems (ADAS) and infotainment applications

Semiconductors continue to follow Moore's Law regarding the doubling of transistors at every process node. While these leaps occurred previously in 18-24 month periods, the complexity of advanced nodes has made progress more challenging and time between nodes greater. As these new process nodes come to market, higher numbers of smaller transistors will

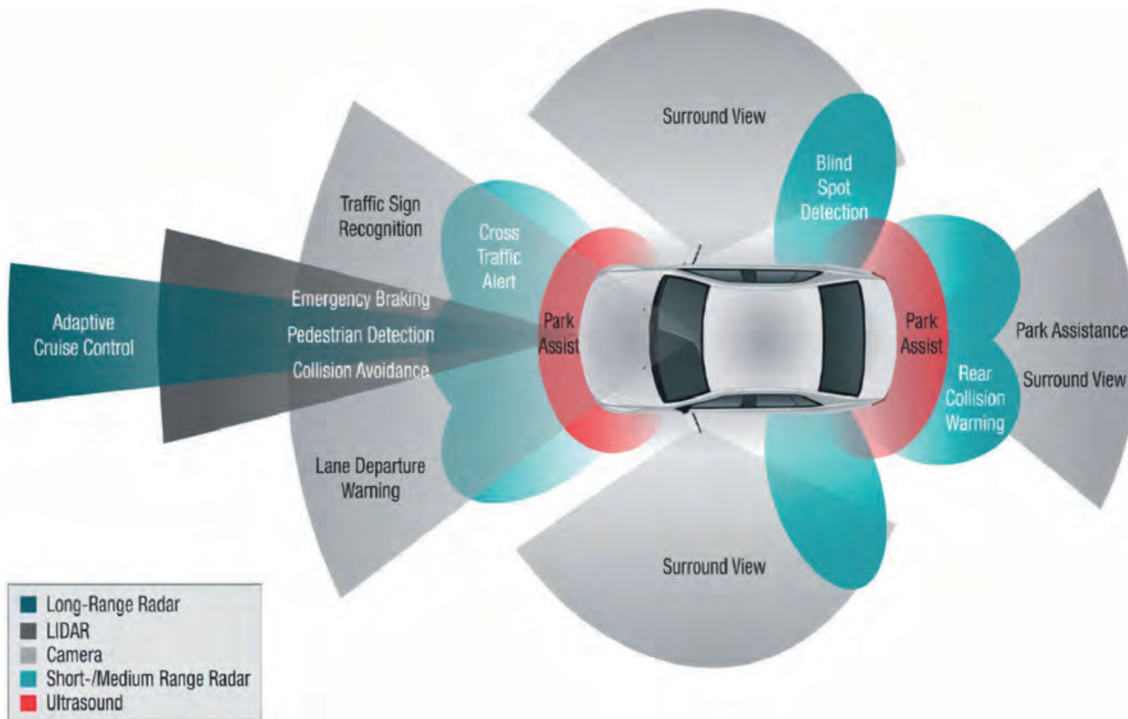


Figure 1: As on-board automotive systems rely more heavily on semiconductor based system, the requirement for fast, accurate and cost-effective testing increases

make it more difficult to catch defects, and will make test coverage more demanding.

For example, test coverage of 99.4% of an advanced node 300mm wafer still leaves 15 million transistors untested on a 2.5 billion transistor device. Time to market and time to revenue drives the need for shorter cycle time with increased faults coverage. System level test in the customer application environment provides the ability to solve these challenges while providing an opportunity to significantly reduce overall cost of test.

A New System Level Test Solution (AMPS)

AEM Singapore has developed a new system level test solution (AMPS) that leverages the knowledge

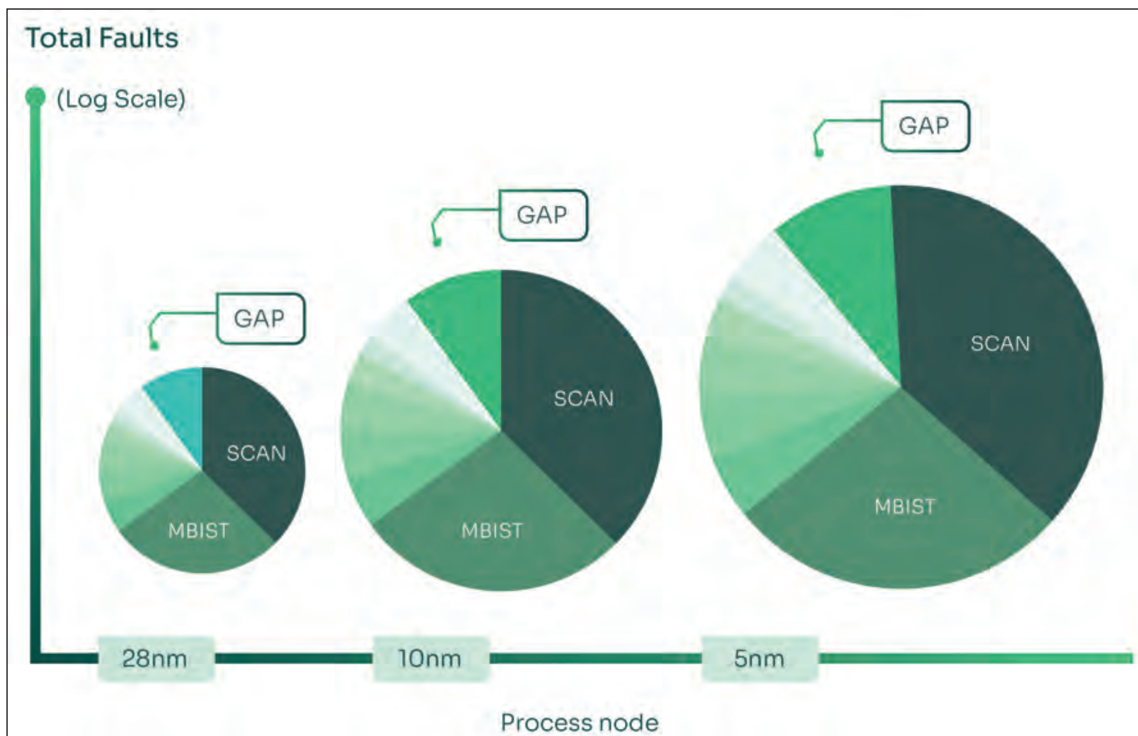


Figure 2: As transistor sizes decrease, more devices are squeezed into each wafer, creating complex test environments. Source: Qualcomm Mike Campbell

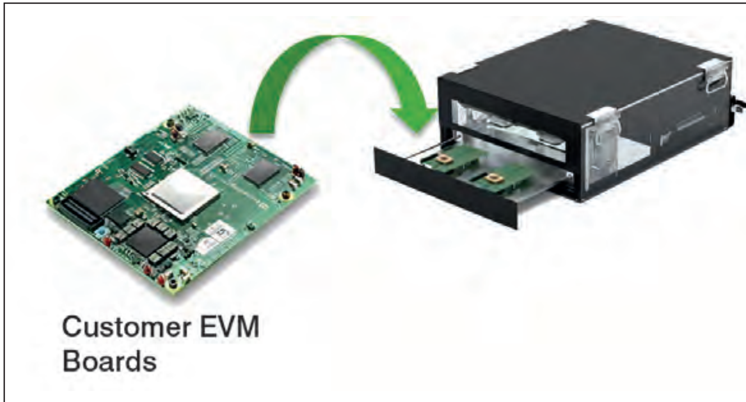


Figure 3: Example of a testing scenario

and experience gained over the last decade in system level device handling for leading semiconductor companies. AMPS stands for Asynchronous, Modular Parallel and Smart as key parameters for system level testing.

System level testers need to be modular and also be easily customized and reconfigured as required for specific device applications. Working with customers to integrate their modified application evaluation module into a system test handling solution leverages the existing test development.

Providing a modular approach that can be replicated and scaled enables the same system to be used in engineering debug environments with the key advantage being that the system a development team initially worked with can be ramped in production. Such production oriented solutions need to be completely asynchronous in operation to enable each system evaluation board to be essentially 'stand-alone' in operation. This facilitates the ability to reconfigure systems without taking a line down and enables individual smart device test flows.

Modularity by re-using the same components enables scalability for massively parallel test handlers, which can reduce the overall cost of ownership.
The AEM System Tester (AMPS) is scalable to the point that it can handle individual devices for engineering debug up to 480 parallel sites. It offers individual device ATC thermal control from -40C up to 150C, supporting burn-in and stress test within the same system. Adding optional system level functional test capability (SLT+) enables BIST, MBIST and functional testing within the same system. This provides the ability to configure a system for multiple different devices or modules to be tested at the same time supporting applications with a higher mix of products such as those frequently offered by OSAT manufacturers

Test flow with system level test

Collecting system level test data enables correlation back to both functional test and wafer test results. By accessing stored data, analytic systems can enable smart knowledge based adaptive test decisions to be made between wafer, functional and system level test (SLT), which can further reduce the overall cost of test.

Adding optional functional test modules at the system level further enables adaptability within the same system.

Advances in data analytics, machine learning and massive parallel test handling systems are now enabling a shift in testing paradigm. System level testing is not a new concept, but is now proven and ready to help increase faults coverage while reducing the overall cost of test.

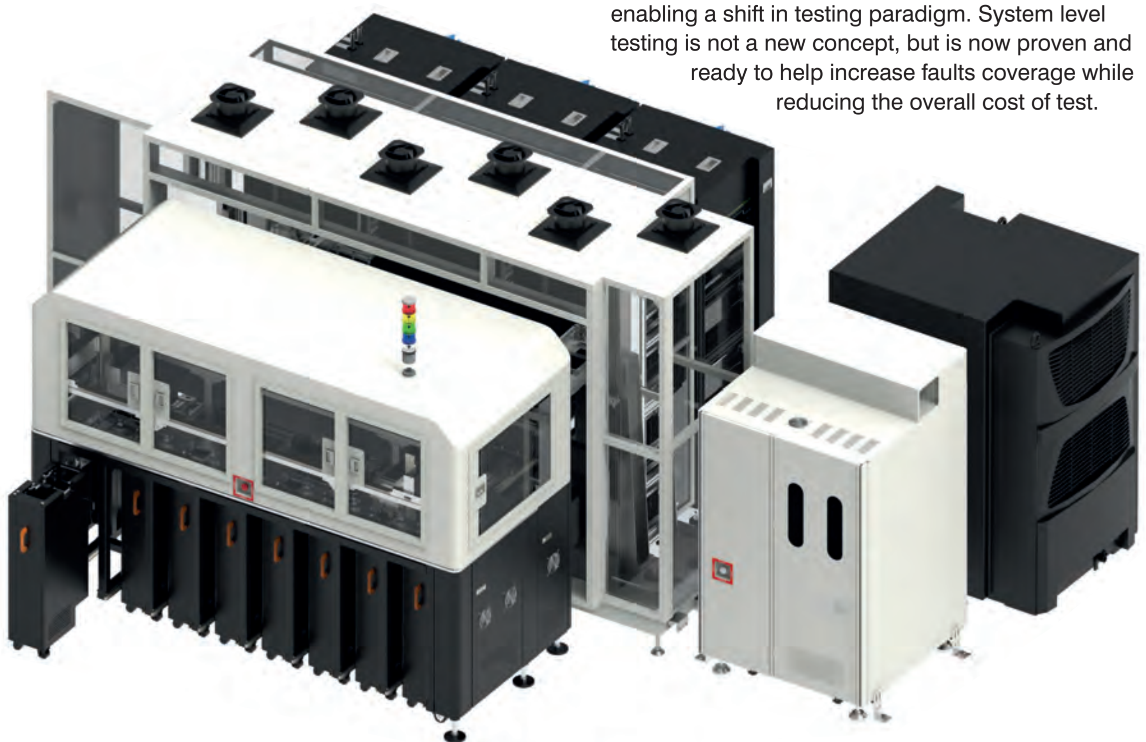
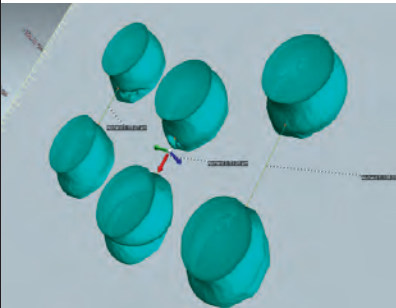


Figure 4: The AEM System Tester (AMPS)

YXLON

YXLON FF65 CL

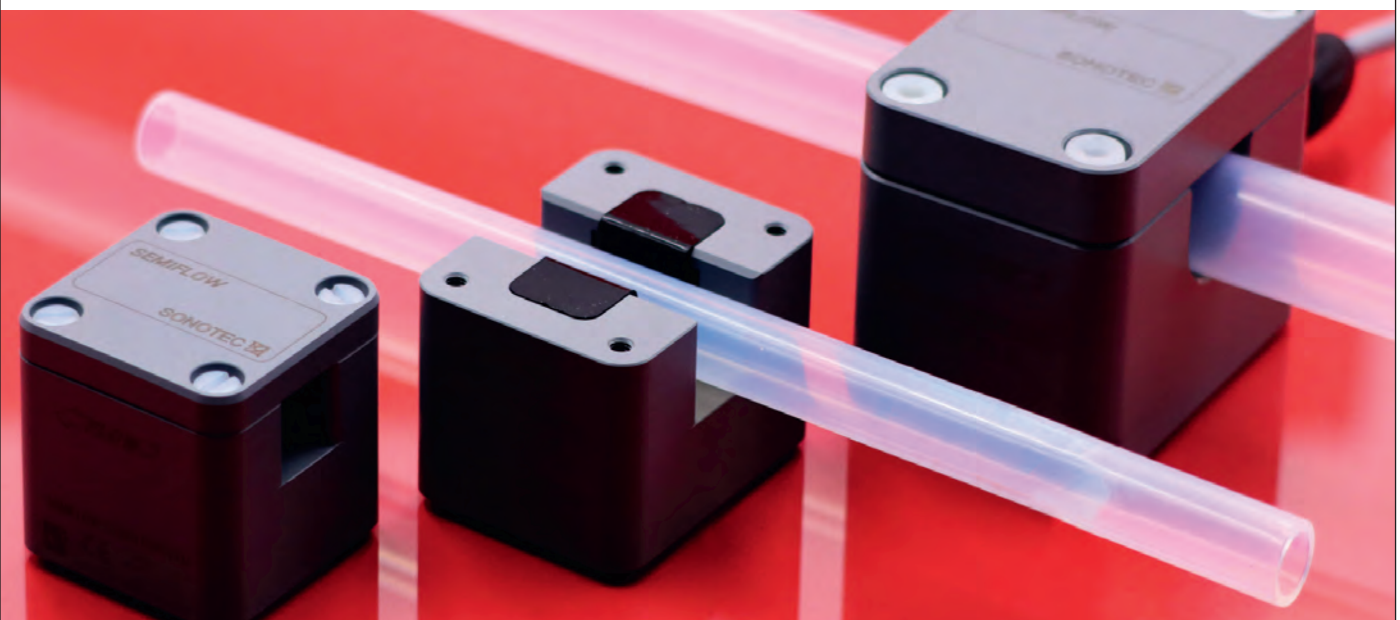


World's Best Resolution 3D X-Ray Inspection System for Fully Automated Verification of IC Packaging Defects

- High-speed 3D AXI
- Most precise measurements of defect dimensions
- Reliable check of process conditions
- Fully automated inspection solution with measurement results

www.yxlon.com

Non-contact Liquid Flow Measurement on Rigid Plastic Tubes & Pipes



SONOTEC GmbH
sonotec@sonotec.de | www.sonotec.eu

SONOTEC

Evaluating the Fab Lifecycle and SubFab service maturity model:

Is there more to gain?

Semiconductor manufacturers appreciate that maximizing fab profits requires high subfab functionality. Nevertheless, many plant managers view subfab maintenance as an unavoidable cost rather than an opportunity to lower overall expenses while increasing uptime. The experts at Edwards Vacuum delve into this dilemma, sharing insights for achieving balanced, optimized outcomes.

BY MATT MCDONALD, GLOBAL PROGRAM MANAGER, AND JOHN DALZIEL, TECHNICAL PROGRAM MANAGER, EDWARDS VACUUM

THE VACUUM and abatement systems that support semiconductor manufacturing processes in the fab are critical – if they are down, so too are the process tools they support. By the very nature of their function – to remove and render harmless process exhaust while maintaining the vacuum conditions required for the process to operate – they are exposed to harsh process chemicals and by-products that make regular service or replacement unavoidable.

Even more costly than planned maintenance is unexpected failure, which can impose additional costs for product losses and repairs to process equipment. Improving the management of vacuum and abatement systems offers significant productivity gains by minimizing both planned and unplanned downtime.

Smart Manufacturing tools and Industrie 4.0 principles are becoming more accessible to manufacturers, where data-driven optimization of maintenance scheduling, namely predictive and proactive approaches, offer the benefit of minimizing downtime and risk of failures. For these approaches to achieve the desired results, differing levels of collaboration and domain expertise are required. The service maturity model helps to visualize progress towards this goal as movement up a maturity hierarchy. This progress must be considered in the context of the fab lifecycle, and, at a more granular level, individual product and process lifecycles. The service strategy must be agile enough to accommodate shifting priorities throughout lifecycles. A critical ingredient, and often the most significant contributor to successfully implementing a smarter approach, is the level of collaboration needed to enable the free flow of critical data. At the highest level, maintenance is transformed from a support cost to be minimized to a value-adding investment that increases productivity.

Service Maturity Model

The mechanization of manufacturing, using machines to multiply the productivity of humans, was the basis of the first industrial revolution – Industrie 1.0 if you will. Ever since, as the role of machines has grown and evolved, and now as the industry embraces Industrie 4.0 and Smart Manufacturing, the methods and approaches to supporting and maintaining those machines have also evolved. The service maturity model (figure 1) classifies approaches to service in a hierarchy of five levels and visualizes the evolution as progression up the hierarchy. The lowest level is to do nothing – worry about it later. The next is reactive maintenance – run-to-fail and fix it when it breaks. At this level, maintenance costs are viewed as a non-

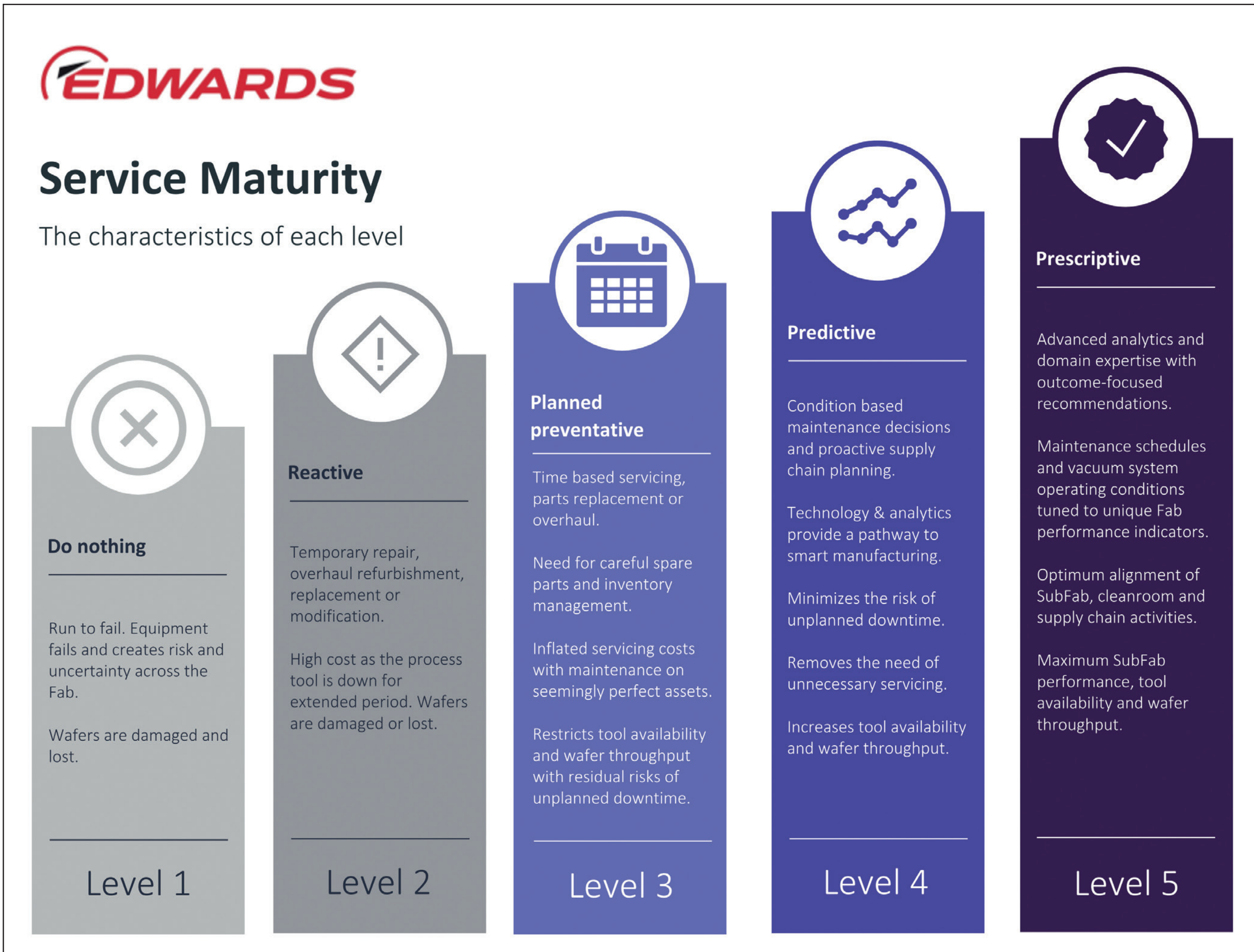


Figure 1. A service maturity model defines a hierarchy of services philosophies.

productive expense and the focus is on minimizing that cost. The next level up is planned/preventive maintenance. Here manufacturers begin looking at the value added by maintenance through improvements in efficiency and performance.

Maintenance is scheduled periodically to occur before the equipment is likely to fail. Essential components of this approach are determining the optimal service interval, standardizing performance and procedures, and finding opportunities for improvement. Predictive maintenance, the next level, is condition-based and relies on increased monitoring of operational parameters to predict imminent failures. It seeks to maximize the time between interventions while avoiding unplanned failures. The highest level in the progression is prescriptive, in which close collaboration between the user and the provider and a shared commitment to continuous improvement promotes a prescriptive approach to maintenance with adjustments to machine operation that optimize outcomes to achieve the user's goals.

The progression described in the service maturity model allows service providers and consumers to understand their position in the hierarchy and align their programs to achieve desired outcomes. Service is not a one-size-fits-all proposition. Different customers and providers will find themselves at different levels. Indeed, the same customer may be at different levels in different parts of an overall manufacturing operation. For example, some Edwards on-chamber vacuum solutions run under a predictive model while many SubFab solutions are still managed with a run-to-fail approach. The service maturity model is most useful as a framework for determining the best next step in the continuous effort to improve user outcomes.

Challenges

The greatest challenges posed by the maturity progression are related to the increasing collaboration required at each level. Every higher level requires greater understanding of the user's environment and process. At each level, the solutions must be more customized to reflect differences in processes. Each level requires more information to flow in both directions to characterize the state of the equipment, then assess and apply the required domain knowledge to enable continuous improvement. The barriers are not always technical; for instance,

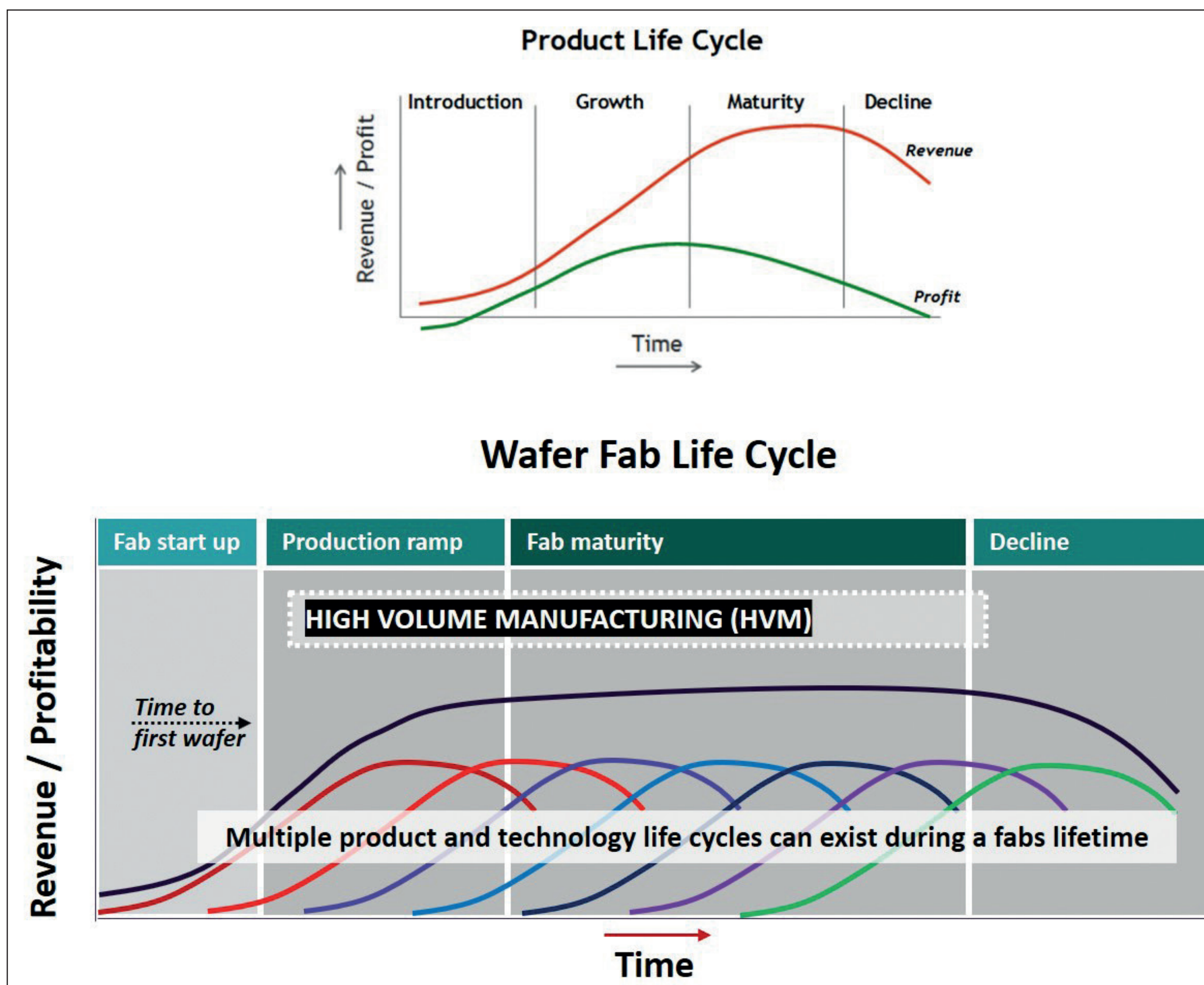


Figure 2. Service requirements change as fabs go through a lifecycle.

they may be driven by organizational concerns about confidentiality and data security. Each level requires a broader view of the operational context and an increased understanding of other equipment and environmental variables that may affect performance and efficiency.

Some of these needs can be addressed by technical innovation in the design of the equipment, such as adding sensors to monitor relevant performance parameters or cloud storage of data to offer faster access to a larger data set. Others are cultural, such as overcoming historic industry biases against data sharing and suspicions about cloud storage security. Some technical innovations are still in the early stages of their own evolution. Machine learning, in which machines analyze their own performance and self-correct, is only beginning to take hold. Artificial intelligence may someday rival human intelligence in its ability to solve complex problems and implement goal-oriented solutions, but it is not there yet. These and other advanced technologies are still at a point where their recommendations require human review. Even the most mature service approaches still rely on the creativity of humans for innovative solutions. At a minimum, these advanced technologies offer significant value by reducing the amount of data review, alerting operators of suspect conditions. They are tireless monitors that never need to eat or sleep.

Fab Lifecycle

A wafer fab life cycle (figure 2) is very much like the life cycle of the silicon chips the fab produces. Productivity and profitability follow a familiar curve from slow start through accelerating growth, peak performance and eventual decline.

- **Start-up –** The initial stage includes building the fab, installing the first equipment, and recruiting and training the staff required to run and maintain the equipment and processes. All focus is on producing “first silicon”, those all-important initial yielding wafers. Any delay is costly and service expenditures are minor relative to the overall investment at risk.
- **Ramp –** The growth stage in a wafer fab, the “production ramp”, is all about improving capacity, yield, and economies of scale to reduce costs and increase income.

- **Mature –** The focus is on maximizing profit. Here the fab life cycle differs from the product life cycle as new products and technologies can be introduced to extend the fab's life expectancy.
- **Decline –** Even with the constant upgrades of equipment and process there comes a time when a fab becomes unprofitable. This stage may be greatly extended by transitioning to products that do not require advanced technologies.

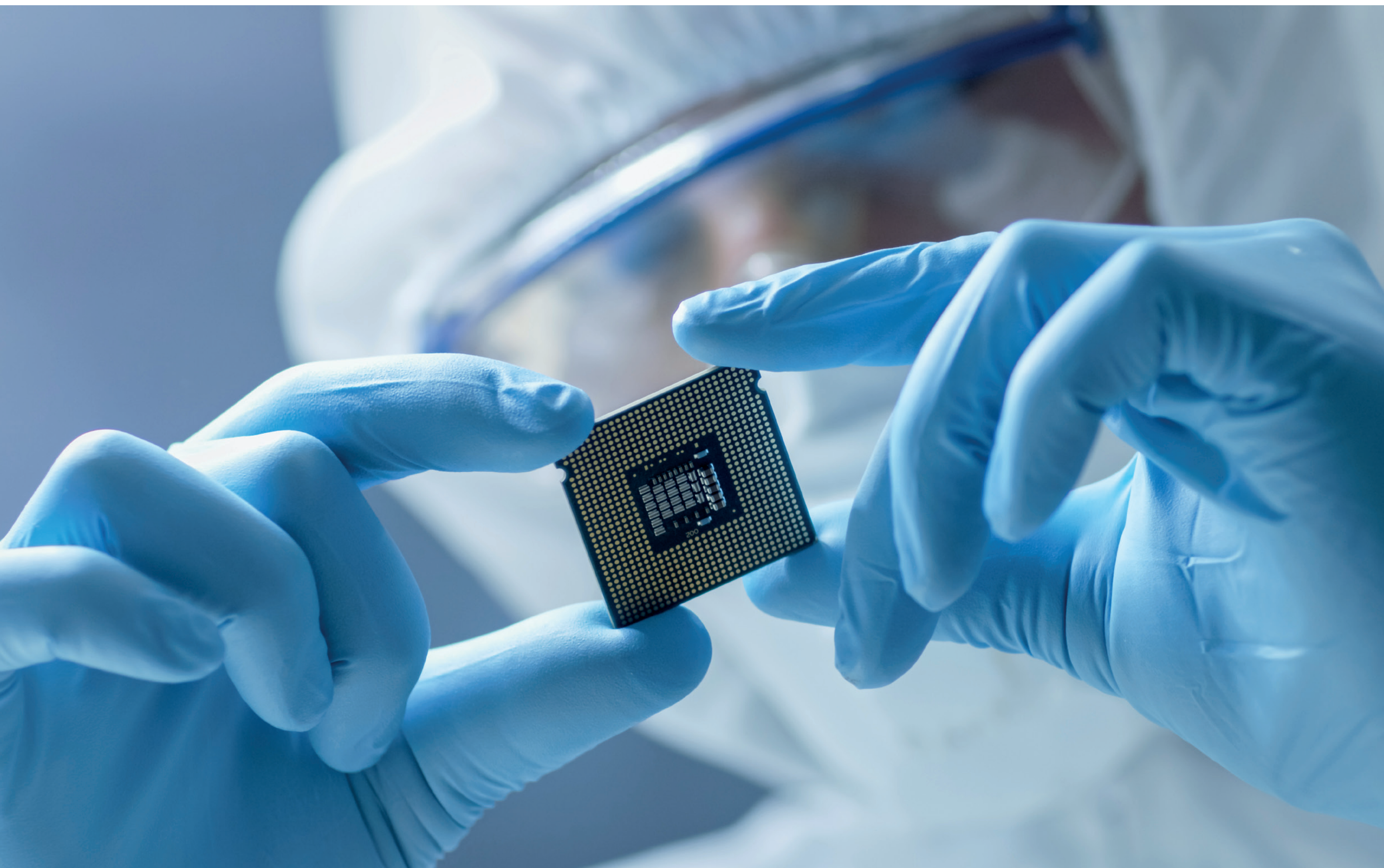
During each phase of the fab's life cycle different priorities drive the need for different skill sets and maintenance approaches.

Start-up is about project management: delivering, installing, commissioning, and setting up the equipment in a fast and effective manner. Most of these activities are carried out by the equipment manufacturers. Maintenance is lower down the food chain as the equipment is new and should perform. Preventive maintenance is likely to be the best approach during this phase. This is when equipment manufacturers need to study performance data, apply and modify domain knowledge, and determine a base-line performance for maintenance scheduling, while their customers focus on first silicon, staffing, and training.

The ramp phase can be especially challenging - it is critically important to avoid any surprises. A preventative approach may deliver best results as more equipment is coming online and first silicon is out the door. Pressure is intense to ramp volume and minimize any negative impact of maintenance. This requires skill sets and resources that are different from initial equipment installation. Growing pains are common as head counts grow for both user and service provider.

Providers must focus on how their equipment is behaving, optimizing maintenance schedules, refining parts inventories, and applying standard work practices. The user's focus now shifts to increasing output, uptime, and yield, while they continue to grow the workforce in numbers and experience. Installs and maintenance are in most cases still performed by equipment manufacturers, but a transition begins as users start to take more ownership of maintenance activities.

A mature fab never really stands still as products and technology continually change and there is pressure to maximise output. New equipment and processes are introduced, which can change the way support equipment reacts. Equipment manufacturers must



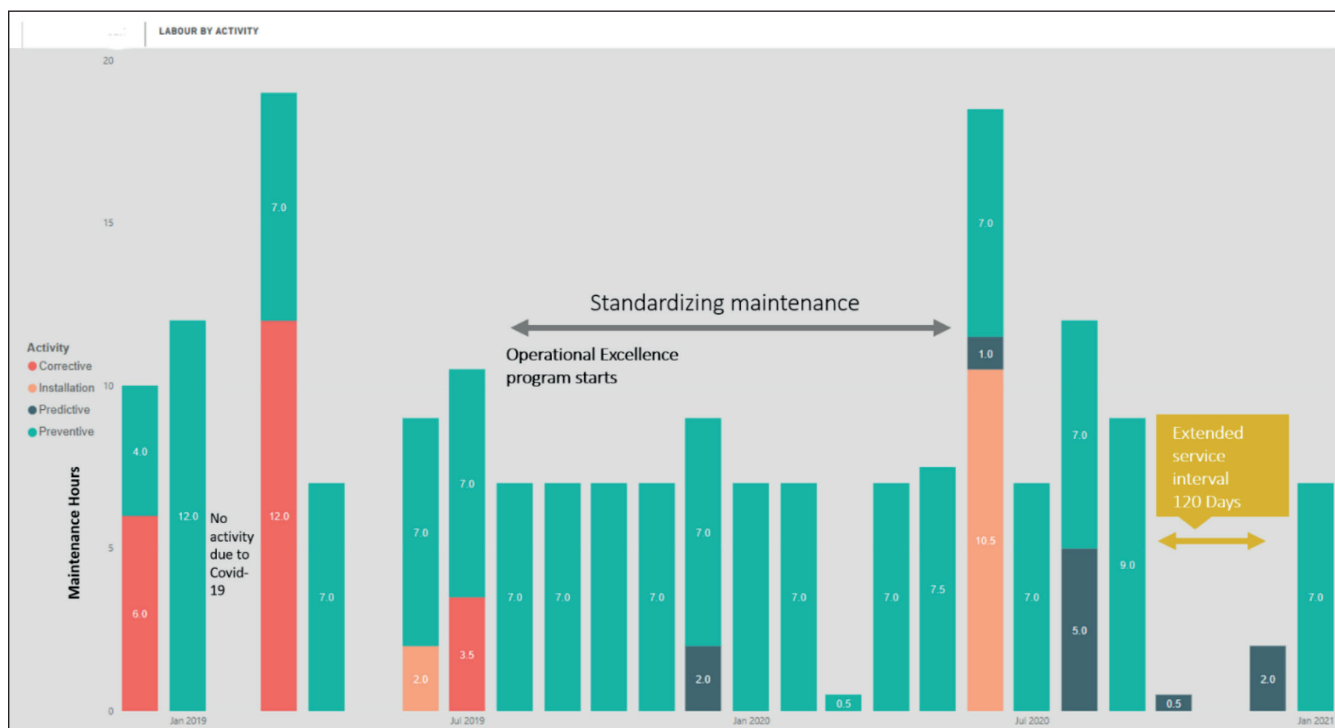


Fig 3. Results of program to enhance uptime – see text for explanation.

constantly review how their equipment is behaving and adjust maintenance activities accordingly, an ideal setting for a prescriptive maintenance approach. At this stage the fab is fully staffed. Fab personnel are trained and have gained enough experience to begin looking for ways to reduce maintenance costs and increase profitability. This is usually the time when fabs consider shifting away from reliance on equipment manufacturers to perform maintenance. The incentive grows to bring maintenance in-house to reduce costs. If equipment manufacturers wish to play a continuing role in maintaining a mature fab's equipment, they must demonstrate the value added by their domain knowledge and expertise. This requires a critical shift for both user and provider. Each must understand and accommodate shifting priorities as the fab matures. Providers must emphasize the unique contributions their knowledge and expertise allow them to make. Users must move from a model that views service as a cost to be avoided, to a model viewing service as an investment that yields returns from increased productivity. Mechanisms to achieve these goals include continuing improvement programs and predictive, adaptive, data-based interventions.

Providers must clearly demonstrate how their unique, knowledge-based value can make contributions to the user's bottom line that exceed any cost savings the user might realize from a lower hourly rate offered by a third-party provider or in-house personnel.

A "declining fab" is in survival mode; cost reduction is the name of the game as it fights to prolong its life and the jobs of the work force. Still, there is an opportunity for smart service management to support the goals of fab management and personnel. A fab at this stage has been running for a long time. The behavior and performance of its tools and the supporting equipment in the SubFab should be well understood. Based on data gathered over a lifetime of supporting, repairing, and refurbishing their systems, equipment manufacturers are in the best position to understand the maintenance requirements of the declining fab. With this unique knowledge, they can design a program that shares risks to reduce cost but still provides reliable performance to the user and reasonable compensation to the provider.

Collaboration

One trend that runs consistently from bottom to top, through all levels of the service maturity model, is the need for increasing collaboration between user and provider. Field service engineers comment frequently on its importance: close collaboration over time builds shared commitment to continuous improvement and the intimate understanding of the user's process and goals.

At the highest level of the service maturity model, users and providers can structure service programs that share risks and benefits, such as outcome-based contracts. This is the other end of the spectrum from time and materials billing. To work, the user must allow access to relevant context information and the provider must be open about process impacts on equipment performance. Ultimately, user and provider agree on the optimal outcome. The user benefits from known, stable maintenance costs and guaranteed performance. The provider is free to deliver that performance in the most efficient and profitable way. Each must trust the other's ability and commitment to make the program work.

Panasonic
INDUSTRY

Plasma Dicing

Plasma Dicing addresses the challenges of dicing smaller and thinner dies

> Particle-Free
> Damage-Free
> Higher Chip Strength
> Increased Yield / Active Area

Consider Plasma Dicing to achieve higher throughput, increased yield and lower costs per wafer.

Industry.panasonic.eu

A service maturity model is one way to evaluate the smartness of various approaches. It allows consumers and providers to consider maintenance requirements within a maturity hierarchy

Example

The customer in this example is a major semiconductor manufacturer and the fab is mature and producing at high volume. Much of the day-to-day maintenance was being performed by in-house personnel using a time-based periodic maintenance program. All such programs are inherently inefficient. If the maintenance interval is chosen to be short enough to ensure service before failure, it will almost always be performed before it is needed. On the other hand, if the interval is extended, the risk of unplanned failure increases and the potential costs of repairing a failed system, plus consequential costs from lost product and damage to process tools, far outweigh the cost of preventive maintenance.

The fab was under increasing pressure to meet growth and performance targets. Operators were aware of the inefficiencies of time-based maintenance, but did not have the full visibility of equipment failures and their causes that might have allowed them to safely increase service intervals. The additional time required to restart and requalify tools after unexpected downtime events was estimated to be 6-7 hours per tool, per year. When this is applied to hundreds of process tools in just one fab alone, the potential loss in productivity can equate to millions of dollars in revenue each year. Other costs, in addition to risks of lost product and damage to production tools, included a large spare parts inventory and morale-busting, unexpected demands on support personnel. Frustration between the fab and SubFab teams was growing, leading to inconsistent communication and a lack of data sharing.

Edwards worked closely with on-site personnel to understand the problem and identify possible solutions. A key factor in the program was the use of a central service management application that allowed field service engineers to enter information about every maintenance interaction across the entire SubFab abatement fleet in (nearly) real time. Information was stored securely in the cloud where it could be conveniently analyzed by factory experts. The project proceeded in several phases (figure 3). Data from the first half of 2019 show the inconsistencies of the pre-existing maintenance program. Preventive maintenances (PM) procedures (blue) were irregularly performed and were compounded with frequent corrective maintenance (red).

The new program begins in July 2019 with standardizing PMs and establishing base-line performance. (The absence of a PM in March 2020 was COVID-19 related.) During this phase engineers collected data on root causes of failures and all relevant aspects of maintenance and processes.

The data revealed a common cause of many failures, inlet blockage, and factory product engineers developed a solution. In July 2020, the solution was installed. PMs and monitoring (predictive maintenance – PdM) over the next 3 months confirmed the efficacy of the solution and allowed engineers to confidently extend the service interval from 30 to 120 days.

By monitoring the equipment service cycle, the SubFab team was able to understand the root causes of faults and develop trusting relationships with the fab team. Subsequent collaboration allowed them to synchronize maintenance of vacuum and abatement systems in the SubFab with scheduled maintenance of critical “bottleneck” tools in the fab, providing additional gains in productivity. With this smarter maintenance approach, the total service hours decreased from 10,002 in 2019 to 8,565 in 2020, providing 1,437 hours of additional uptime.

Summary

In conclusion, smart management can increase fab productivity. A service maturity model is one way to evaluate the smartness of various approaches. It allows service consumers and providers to consider maintenance requirements within a maturity hierarchy.

In practice the maturity scale is convoluted with fab, product and process lifecycles. Though this makes service requirements situationally specific, the maturity hierarchy still defines a preferred direction for improving service efficiency and outcomes.

Collaboration and information flow characterize successively high levels in the hierarchy and should be essential considerations in any effort to move up. Smarter, more mature service approaches benefit both consumer and provider through higher efficiency, increased productivity, and reduced risk.

The Edwards Services Maturity Model can be accessed here: https://hubs.la/H0LMZK00

Park SYSTEMS
www.parksystems.com

Fully Automated AFM solution

for OLED, 2D encoder, photomask and more

Gen 8+
Flat panel display glass

Park NX-TSH

The automated Atomic Force Microscopy (AFM) system for ultra large and heavy flat panel displays at nanoscale

As the demand for Atomic Force Metrology for larger flat panel displays increases, Park NX-Tip Scan Head overcomes nanometrology challenges for samples over 300mm. The Tip Scanning Head and gantry style air-bearing stage allows Park NX-TSH to accurately image roughness measurement, step height measurement, critical dimension measurement. Learn more about how to get reliable, high resolution AFM images on your large sample size OLEDs, LCDs, photomasks using Park NX-TSH by watching our video at **parksystems.com/tsh/video**

www.parksystems.com/nx-tsh

inquiry@parksystems.com

2D transistors look to extend the logic roadmap

Development of WS2 2D transistors in a 300 mm CMOS fab provides a promising pathway for scaling the transistor

BY INGE ASSELBERGHS AND IULIANA RADU FROM IMEC

THE ERA OF 'happy scaling', driven by Moore's Law and played out by the semiconductor community, has faced severe challenges since 2005. Up until then progress came relatively easily, with shrinking of the silicon transistors delivering multiple benefits, including a lower power consumption, increased performance, and a reduction in the fabrication cost per transistor. A new, more powerful generation of technology launched roughly every two years – denoted by a new node size – to double the number of transistors packed into an identical-sized chip.

The first sign that the benefits of scaling would not go on forever appeared when the node-to-node performance improvements at a fixed power – referred to as Dennard scaling – started slowing down. Applying the brakes were short-channel effects. Leakage currents started shooting up, even when not applying a voltage to the gate, due to significant reductions in gate length and a shortening of the conduction channel. Scaling also caused source and drain contacts to begin to have a dramatic impact on the channel region.

To compensate for this slow-down in device improvement and allow integrated circuits to continue to advance, much effort has been directed at developing new transistor technologies. Many directions have been pursued, including new channel materials, new transistor architectures and co-optimisation of the chip's design and its technology.

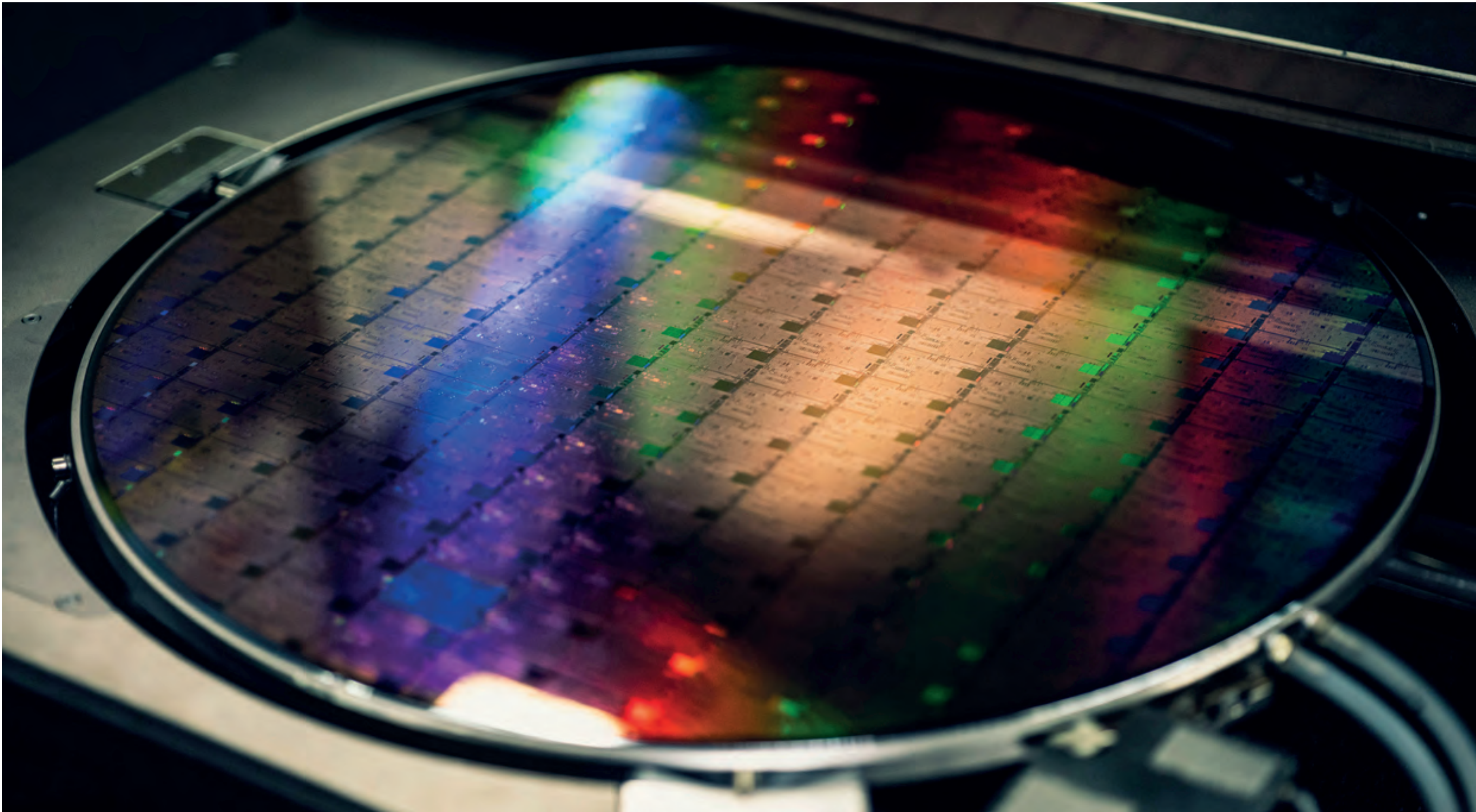
A significant architectural improvement has been the replacement of the planar MOSFET with the FinFET – the latter is now the incumbent design in mainstream chip production processes. In a FinFET, the channel takes the form of a very thin fin, positioned between source and drain terminals. Wrapping around this three-dimensional channel is a gate that provides control from three sides and combats short-channel effects. It is an architecture that has been crucial to scaling over the last decade, but will fail to provide enough electrostatic control beyond the 5 nm or 3 nm node.

Building on this approach is the vertically stacked, gate-all-around nanosheet transistor. It provides superior channel control, thanks to a gate that fully wraps around and in between the channels. At imec of Leuven, Belgium, this architecture is on our roadmap, followed by the forksheet transistor – that is a design that uses a forked gate structure to control nanosheets, and allows a far tighter n-to-p spacing than that possible with FinFET and nanosheet devices. Another candidate for well into the future is a stack of multiple channels, which could effectively extend scaling with silicon or SiGe semiconductors.

Running in parallel to this evolution, the research community has been investigating gains provided by enhancing carrier mobility. Options for the channel include strain engineering and migrating to high-mobility semiconductors, such as germanium and the III-Vs. Note that there is much interest in InGaAs: as it transports charge much faster than silicon, it promises faster speeds and lower power consumption. Innovative processes have already been developed to incorporate foreign channels with silicon CMOS, using conventional manufacturing techniques. However, just like silicon, it is unlikely that these high-mobility materials will enable sufficient gate length scaling at the very advanced nodes that lie ahead. It seems that III/V-material-based devices will find a more natural adoption in high-frequency applications – as required for (beyond-) 5G applications – that allow their high-speed properties to reach their full potential.

The promise of 2D semiconductors

To realise further gate length reduction, thinner semiconductor channels are needed to keep short channel effects under control. Migrating to thinner channels restricts the pathway for current to flow, and



this limits the opportunity for charge carriers to leak when the device is turned off.

Offering much promise in this regard is a class of materials known as two-dimensional semiconductors. They include transition metal dichalcogenides, such as WS_2 and MoS_2. In these semiconductors atoms are arranged in layered crystals, with a single layer thickness of typically just 7 Å – small enough to make these materials a great choice for ensuring very thin channels. Results from theoretical studies highlight their potential, indicating that they maintain a relatively high carrier mobility, independent of channel thickness. It's an attribute that should enable engineers to scale gate lengths below 10 nm without having to worry about short-channel effects.

Working within the Design-Technology Co-Optimization framework, our team at imec has recently highlighted the potential for transistors with a 2D semiconductor channel to further extend the logic scaling roadmap. We anticipate that these 2D-FETs, which will most probably find their insertion point in a stacked-nanosheet-like architecture, will extend the roadmap by providing at least two technology generations. Our circuit-level evaluation of power, performance and area at a node with 36 nm gate pitch revealed that transition metal dichalcogenides in a stacked 2D-nanosheet configuration outperform silicon-based counterparts while having a reduced footprint. Note that this model employed realistic assumptions, drawing on as much experimental data as possible. The global effort at developing transition metal dichalcogenides has led to the exploration of a variety of materials, and the identification of some of the main challenges for improving device performance. To date, most work has involved semiconductor channels made of MoS_2. Devices based on this material are the most mature, with the best experimental values for mobility getting close to the theoretical value of 200 $cm^2 V^{-1} s^{-1}$.

Recently, promising results have been reported for WS_2-based FETs. According to theoretical work, these devices have the potential to deliver an even higher performance than their MoS_2 cousins. Experimental results are also encouraging. For example, back in 2019, research reported by a TSMC-led collaboration showed that electrical characteristics, such as the on/off ratio and the sub-threshold swing, are comparable to the best recently published values for MoS_2 n-FETs. In its turn, imec has demonstrated functional 2D-FETs with a 30 nm-long channel just 1-2 monolayers thick.

With this class of devices a dual-gated device structure improves electrostatic control. Unlike traditional FETs, which just have a gate at the top, dual-gated siblings have a top and a bottom gate – when connected, this increases electrostatic control over the channel. Measurements on our 2D-FETs with connected top and back gates reveal that they outperform single-gated counterparts in drive current (I_{on}), transconductance and sub-threshold swing,

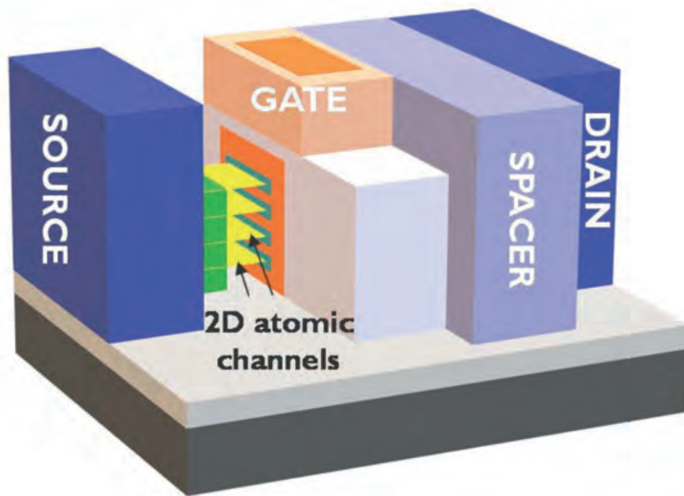


Figure 1. Design-Technology Co-Optimization (DTCO) analysis suggests that stacked 2D materials with side contacts are needed to compete with silicon nanosheets.

three key metrics for evaluating short-channel effects. Another encouraging aspect of the dual-gate structure is that it shows promise for CMOS operation. While these results suggest that a great future lies ahead for the WS2-based FET, there is much work still to do, given that the devices we've just described were fabricated on relatively small coupons with patches of synthetic transition metal dichalcogenide material. To build on these hero results from lab-based devices and prepare a pathway for commercial success, an approach must be found that enables their adoption in a 300 mm integration flow.

A 300 mm platform

Several years ago, our team started working towards 300 mm integration of the family of transition metal dichalcogenide 2D semiconductors. This created a unique 300 mm test vehicle for 2D-FETs, allowing fabrication of functioning devices with gate lengths down to 18 nm. We have used the flow to study the impact of various processing conditions, such as channel deposition technology and gate stack formation. Based on these insights, we are developing improved process steps to enhance device performance.

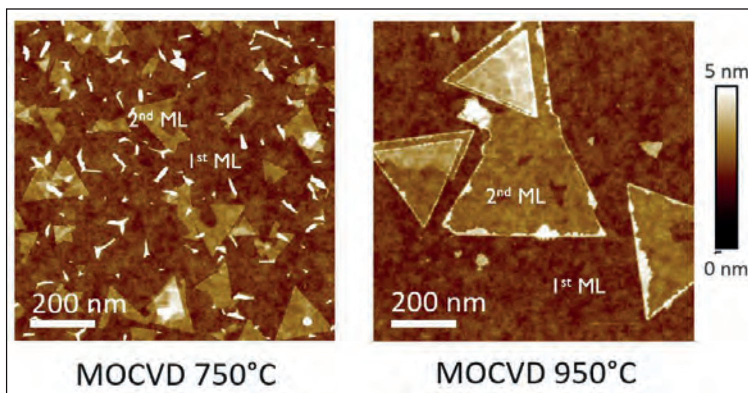


Figure 2. Atomic force microscopy of films of WS2 grown by MOCVD at (left) 750 °C and (right) 950 °C (as presented at the 2020 IEDM conference).

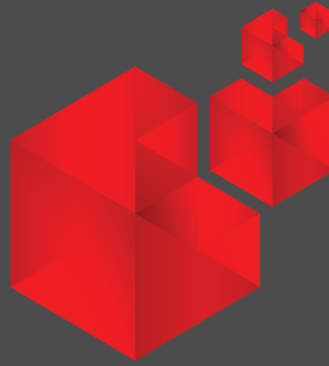
Our first foray into the formation of integrated transistors on the 300 mm platform pointed to high-temperature MOCVD as the best option for depositing high-quality channels, critical to realising high-performance devices. This growth technology offers thickness control of the 2D semiconductor down to a single monolayer. However, there are small multi-layer spots over the full 300 mm wafer.

We have found that the growth temperature impacts material quality. This conclusion came from the growth and characterisation of a layer of WS2 deposited at 750 °C and 950 °C, using W(CO)6 and H2S sources. Using atomic force microscopy, we compared films grown on 300 mm silicon/SiO2 substrates, produced using a growth time of 170 minutes, and found that a higher deposition temperature increased the size of the WS2 grains. The higher temperature also improved crystallinity and reduced the defectivity of the WS2 layer, according to photoluminescence and Raman measurements. It is possible that larger crystal sizes could be obtained at lower temperatures using different precursors or other deposition techniques – this is a topic of further research.

One of the challenges associated with producing WS2 is that it is not easy to deposit insulating materials on top of the 2D surface and form a gate dielectric. An intrinsically passivated process is to blame. When traditional ALD processes are adopted, relying on nucleation of surface dangling bonds, growth only occurs at defect sites. Since the MOCVD-grown WS2 has relatively few defect sites, this hinders direct oxide deposition.

To tackle this issue, we are investigating novel approaches for oxide deposition. They include making use of a nucleation layer of silicon seeds, deposited by a molecular beam. Another problem we shall have to consider is the low adhesion of the WS2 to most oxides, resulting from self-passivation. This poses challenges for typical patterning schemes using hard masks.

Results on our devices formed on 300 mm wafers reveal that their performance is an order of magnitude lower than it is for reported lab devices. For example, on-current is typically just 10 μA/μm. To understand why these devices are inferior, we have considered the integrated flow. Our characterisation of dual-gated devices with source/drain side contacts suggests that channel material crystallinity is the biggest challenge to improving device performance. Success requires further breakthroughs in material growth and processing. We also have room for improvement in the processes used to form gates, dope material and add contacts.



Industry counts on SEMI standards.

SEMI is the global industry association serving the product design and manufacturing chain for the electronics industry.

Check out our new standards on SMT & PCB Manufacturing Equipment Communication, Panel Level Packaging & Energetic Materials at:

www.semi.org/collaborate/standards

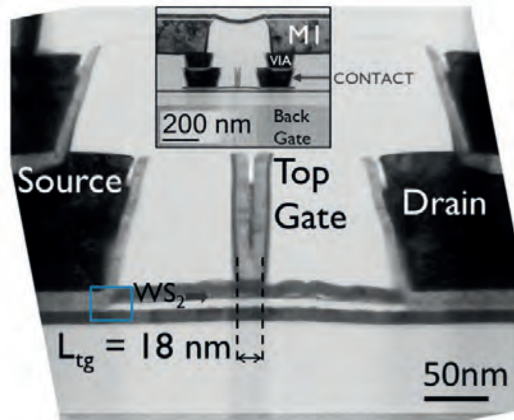


Figure 3. Transmission electron microscopy (TEM) image of a 2D device fabricated with 300 mm processes (as presented at the 2020 IEDM conference).

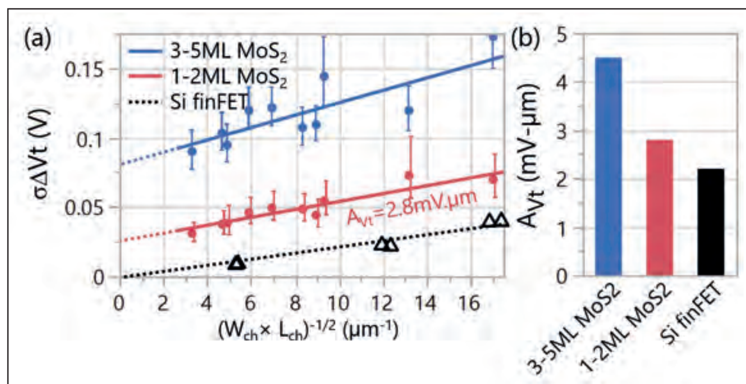


Figure 4. 1-2 monolayer MoS2 FETs (with an equivalent oxide thickness (EOT) of 2.6nm) have higher threshold-voltage variability, but their slope approaches the silicon FinFET reference (EOT=0.8nm) (as presented at the 2020 IEDM conference).

As 2D semiconductor-based FETs are most likely to be introduced in stacked nanosheet-like architectures, we have used the 300 mm-compatible flow to identify and overcome challenges associated with building these advanced device architectures. The creation of a stacked nanosheet requires formation of a superlattice structure, containing alternating layers of a channel material and either silicon or SiGe. Once this is formed, nanosheets could be released by selectively etching away the silicon or SiGe layers. Looking further ahead, there may come a time when 2D semiconductors are integrated in a complementary FET-like architecture, using n-type 2D-FETs on top of p-type 2D-FETs.

While MOCVD is the preferred technique for depositing high-quality 2D semiconductor channels, the high temperatures that are used threaten to exceed the thermal budget. Options to prevent this from happening include introducing different precursors and switching to alternative deposition technologies. There is also the more radical, complex approach of using a transfer process to move the 2D channel to a pre-patterned 300 mm silicon wafer.

Evaluating variability

Efforts at imec have not been limited to just developing and integrating 2D-based transistors. We have also undertaken the first-ever variability study of a large set of nanoscale lab-based 2D-FET devices, using transistors with a channel width of 115 nm and lengths of 100 nm and below. This investigation considered various sources of variability – including the thickness of the 2D-channel; the presence of bilayer islands, such as grains; and the 2D growth template – and the respective impact on electrical performance, with a focus on the sub-threshold regime.

Within this study, there have been simulations, along with the construction of devices that have a median sub-threshold slope of 80 mV/dec and maximum on-current in excess of 100 μA/μm. This research uncovered a strongly reduced sub-threshold slope and threshold-voltage variability when thinning the 2D material from three monolayers to one. This is an encouraging result, indicating that very thin channels are needed for further transistor scaling. For atom-thick channels, this work shows that the intrinsic variability is low, and comparable with silicon FinFETs. To make further progress in driving down device variability, so that it is suitable for future nodes, there needs to be better control of key process steps, like cleaning and contacts.

Worldwide progress with 2D-FETs is positioning this class of transistor as a prime candidate for extending the logic device scaling roadmap. At imec, work by our team and our colleagues has started to lay the groundwork for introducing 2D semiconductors into a 300 mm integration flow – a key requirement for industrial adoption. We have already taken significant steps by improving device performance and developing a fundamental understanding of this form of FET.

This work is the result of a collaborative effort of a broad imec team working on exploratory logic.

Further reading

Z. Ahmed et al. ‘Introducing 2D-FETs in device scaling roadmap using DTCO’ IEDM 2020.
K.K.H. Smithe et al. ‘Intrinsic electrical transport and performance projections of synthetic monolayer MoS2 devices’2D Materials 4 011009 (2017)
C-C Cheng et al. ‘First demonstration of 40nm channel length top-gate WS2 pFET using channel area-selective CVD growth directly on SiOx/Si substrate’ 2019 Symposium on VLSI Technology Digest of Technical Papers.
D. Lin et al. ‘Dual gate synthetic WS2 MOSFETs with 120μS/μm Gm 2.7μF/cm2 capacitance and ambipolar channel’, IEDM 2020.
I. Asselberghs et al. ‘Wafer-scale integration of double gated WS2-transistors in 300mm Si CMOS fab’, IEDM 2020.
Q. Smets et al. ‘Sources of variability in scaled MoS2 FETs’, IEDM 2020.

To promote your products and services contact:
Shehzad Munshi
T: +44 (0)1923 690 215
E: shehzad.munshi@angelbc.com

green pages directory

Chillers

CO2 CHILLER for SEMICONDUCTOR

-20°C to 70°C temperature control
2kW cooling capacity @ -10°C
GWP= 1 with CO_2 compressor

More info@atschiller.com
Advanced Thermal Sciences
www.atschiller.com

Flow Measurement

NON-CONTACT LIQUID FLOW MEASUREMENT
ON RIGID PLASTIC TUBES & PIPES

SONOTEC
SONOTEC GmbH | sonotec@sonotec.de | www.sonotec.eu

Gas Purifiers

ARM PURIFICATION
BY APPLIED ENERGY SYSTEMS

SO MUCH MORE THAN A COMPONENT.

Advanced point-of-use, micro-bulk and bulk gas purifier solutions

www.appliedenergysystems.com/pure

Materials

Electronics starts with us

From prototype to packaging, and every step in between, our semiconductor materials are designed to enable the future of electronics in a data-driven world.

www.merckgroup.com

Clean Rooms

airfiltrera
Fan Filter Unit Specialists

We supply a range of Envirco FFUs and control systems for a diverse range of cleanroom applications.

Our MAC10 units are ideal for soft/hard-wall, plenum design cleanrooms/LAF benches.

Envirco Fan Filters can be used as part of a simple installation inside a custom-made clean bench or as a full ceiling FFU to aid specifications for the removal of contaminants.

We also offer a range of Trion electro static precipitators, which are suitable for cleaning air in kitchen, industrial and commercial environments.

Over 50 years clean room experience

Web: www.airfiltrera.co.uk
Email: sales@airfiltrera.co.uk

Flow Solutions

Total Flow Solution

KITZ SCT
http://kitz-sct.jp/english/
TEL +81-3-6404-2171
E-mail info@kitz-sct.co.jp

Hydrogen Generators

nel®

Nel Hydrogen is the recognized industry leader of Alkaline and PEM water electrolysis. We provide solutions that meet global hydrogen requirements for semiconductor and thin film manufacturing worldwide.

+1.203.949.8697
info@nelhydrogen.com
www.nelhydrogen.com

Plasma Technology

Trymax®
PLASMA TECHNOLOGY SOLUTIONS

When plasma matters

www.trymax-semiconductor.com

Etch

Dry Etching for Compound Semiconductors

NE-5700 multi chamber etching system for high volume production for GaN and SiC offers excellent cost/performance.

ULVAC
ULVAC GmbH
+49 – 89 – 96 09 09 0
ulvac@ulvac.de | www.ulvac.eu

Gas Delivery Systems

APPLIED ENERGY SYSTEMS

Your world of discovery, powered by our delivery.

Ultra high purity gas delivery solutions for rigorous purity and precision needs.

www.appliedenergysystems.com

Inspection Systems

INNOVATION IS KEY TO EVOLUTION
EMPOWERS YOU

The next level of x-ray and CT inspection systems.

YXLON
www.yxlon.com/en/evolution

Vacuum Equipment

PFEIFFER VACUUM

Vacuum Solutions from a Single Source

T: +001 800.248.8254 or
E: contact@pfeiffer-vacuum.com

MERCK

WE ARE ELECTRONICS

We are the company behind the companies advancing digital living. Our product and service portfolio has been designed to enable the future of electronics in a data-driven world.

OUR OFFER TO CUSTOMERS:

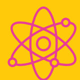
Semiconductor Materials
are at the heart of electronics and enable the transformation of communications, mobility and healthcare. We unlock the potential for smaller, faster, and more energy-efficient devices.

Delivery Systems & Services
safely guards the molecule of semiconductor and display materials. We provide high-quality delivery and storage of specialty chemicals and gases.

Display Solutions
offers next-generation material, equipment systems and services that revolutionize Electronics. We help to connect the intelligence inside devices with human experience.

Surface Solutions
helps redefine the use of color in modern living. Our broad portfolio of pigments and active ingredients continue to drive value in the automotive, cosmetic and industrial industries.

OUR EXPERTISE:



Innovation to keep you ahead:
Leading R&D investment and execution

Quality and Reliability:
Safety and consistency in purity across our product portfolio

Over 350 years of Commitment:
Enabling award-winning collaboration with industry leaders

Depth and Breadth:
Global supply chain and one of the broadest portfolios across the semiconductor, display and pigments industries

People and Purpose:
A leading team of experts at key locations

ELECTRONICS STARTS WITH US.

For more information, please visit us at bit.ly/SemiconductorMaterials

The Electronics business of Merck operates as EMD Electronics in the U.S. and Canada.