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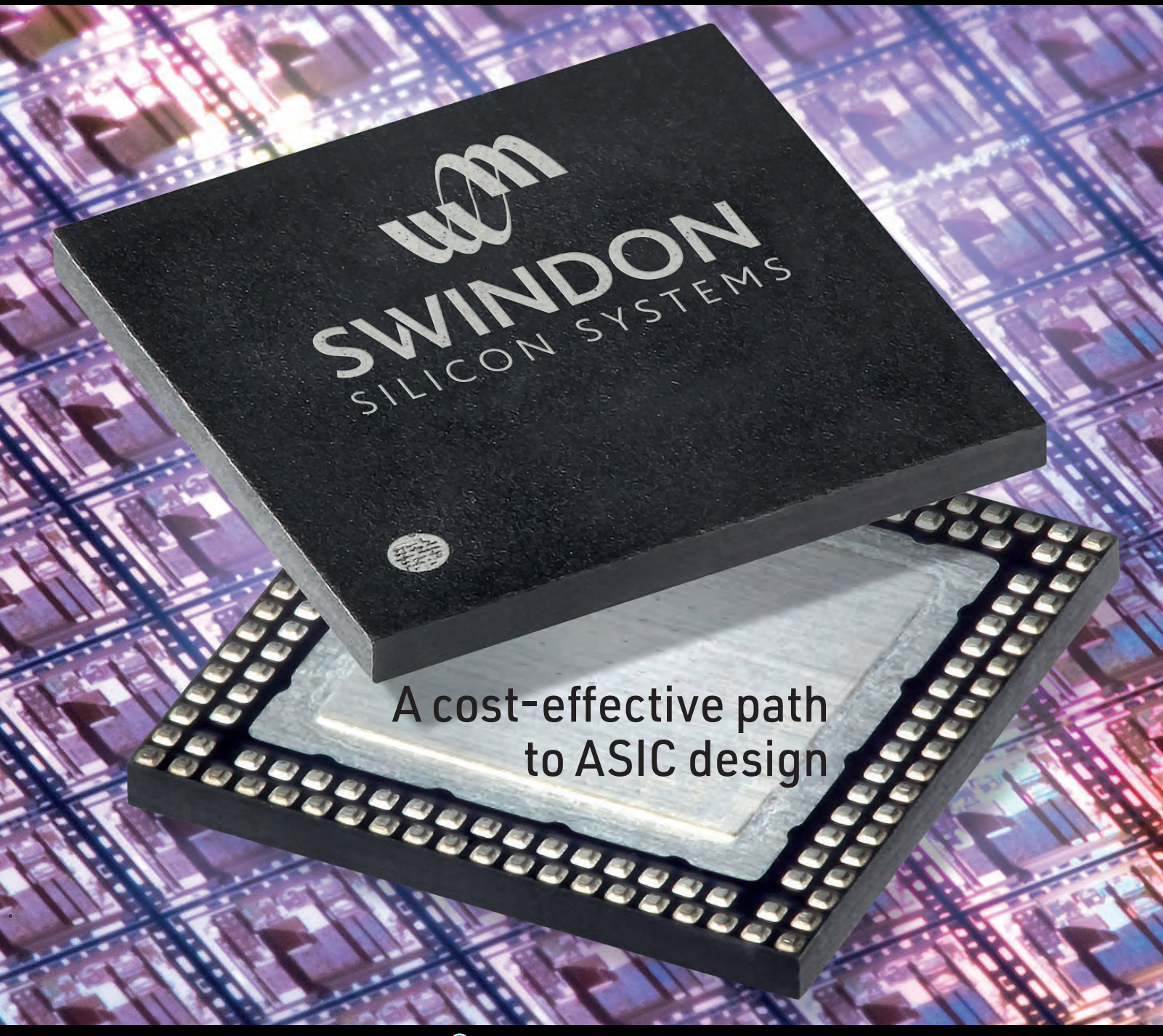

A cost-effective path to ASIC design

VOLUME 43 ISSUE II 2022
AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION
SILICONSEMICONDUCTOR.NET

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VIEWPOINT

By Mark Andrews Technical Editor

Sales records shattered as the pace in 2022 quickens

UNLESS your industry tenure predates the floppy disc it is unlikely that you recall so many reports of everything silicon setting double-digit sales records only to see those records outdone by the next quarter's figures. As we near the mid-point in 2022, records are again being overthrown; the pace is set for even more amazing growth in 2022.

When the SEMI trade group reported that electronic materials set a new $64 billion sales record in first quarter, it seemed almost 'normal' that three weeks later SEMI would report that 200mm fab capacity is set to surge 21 percent as manufacturers seek to satisfy continuing demand. This news was followed a day later by SEMI reporting that overall manufacturing equipment sales surged 44 percent – yet another industry record. Pick almost any category and the story repeats: record set/record falls/demand still outpaces supply.

By now we have all heard about market conditions prompting so many sales records. Pent-up demand, plus supply chain disruptions, plus on-going manufacturing stoppages in China and elsewhere equals record sales and record prices. The supply chain continues to right itself, yet the issues are so daunting that seeking solutions is the subject of multiple international conferences including SEMI's Industry Strategy Symposium (ISS) Europe. Supply chain headaches sit alongside achieving sustainability and tackling the need for more skilled workers, engineers, and researchers to build our silicon future.

In this issue of Silicon Semiconductor we delve into ways that key stakeholders are dealing with materials shortages, speeding the development of new devices and are taking new fab-level approaches to improving

efficiency while cutting costs. The digitization experts at Critical Manufacturing explain how they have converted multiple legacy ERP and production management systems over to their Industry 4.0 MES system, a process that is already streamlining production for Vishay.

We also explore the latest engineering simulation innovations by Ansys that demonstrate what highly accurate simulation and modeling can do to speed designs from development to production. We also look at ways new ASICs can be developed more rapidly and cost-effectively when partnering with a long-tenured design house like Swindon Silicon Systems.

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VOL 43 ISSUE II 2022

SILICON SEMICONDUCTOR
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Imec unites partners to target net-zero emissions

AT FUTURE SUMMITS 2022, imec, a leading research and innovation center in nanoelectronics and digital technologies, has announced that its Sustainable Semiconductor Technologies and Systems (SSTS) research program succeeded in bringing together stakeholders of the semiconductor value chain, from large system companies such as Apple and Microsoft, to suppliers, including ASM, Kurita, SCREEN and Tokyo Electron.

The program was set up last year as part of imec's sustainability efforts to support the semiconductor industry reducing its carbon footprint. The addition of these new partners enables a holistic approach, which leverages imec's expertise and knowledge to cut the industry's environmental impact.

The semiconductor industry is booming with a never-seen demand. As an integral part of our smart portable devices, IoT systems and compute infrastructure, chips are embedded in our everyday life. Semiconductor manufacturing, however, comes at a price. It requires large amounts of energy and water and creates hazardous waste.

To tackle this problem, the entire supply chain needs to commit, and an ecosystem approach will be key. While system and fabless companies are already investing in decarbonizing their supply chain and products, committing to be carbon neutral by 2030 or 2040, they typically lack accurate insight into the contribution of chip manufacturing of future technologies as there is limited life cycle analysis data available.

With its SSTS program, imec calls upon the whole semiconductor value chain to join forces to cut back on the semiconductor industry's environmental footprint. It combines imec's strong partner ecosystem, insights in processing technology, infrastructure, and machinery to provide partners across the semiconductor value chain insight in the environmental impact of certain choices made at the chip technology's definition and production phase. Apple was the first public partner to join hands with imec on the SSTS program last year. Now additional major system companies like Microsoft have joined the program.

The program assesses the environmental impact of new technologies, identifies high-impact problems and defines greener semiconductor manufacturing solutions. "Today there is a data gap concerning the environmental footprint of the fabrication of semiconductor integrated circuits (IC) for more advanced technologies. That's why we're assessing the environmental impact in a first step so we can make informed choices when we move to the next technology generations.

Equipment, material and tool suppliers are key in the early phase plans; they can for example create more environmentally friendly processes and tools to solve high-impact problems in these future technologies. We are also talking to foundries to help verify and benchmark the results.

By engaging with the entire semiconductor value chain in this way, our SSTS program can maximize its impact," states Lars-Åke Ragnarsson, Program Director SSTS.

Infineon revenue up in Q2 FY 2022

INFINEON TECHNOLOGIES AG is reporting results for the second quarter of its 2022 fiscal year (period ended 31 March 2022). Q2 FY 2022: Revenue €3.298 billion, up 4 percent on preceding quarter and 22 percent year on year; Segment Result €761 million; Segment Result Margin 23.1 percent; Free Cash Flow €120 million

Outlook for Q3 FY 2022: Based on an assumed exchange rate of US$1.10 to the euro, revenue of around €3.4 billion predicted. On this basis, Segment Result Margin expected at around 21 percent. Outlook for FY 2022: Based on an assumed exchange rate of US$1.10 to the euro (previously US$1.15), revenue of €13.5 billion plus or minus €500 million (previously €13.0 billion) now forecast for 2022 fiscal year. At mid-point of guided revenue range, Segment Result Margin above 22 percent predicted (previously about 22 percent). Investments at around €2.4 billion still planned. Free Cash Flow expected to reach about €1.1 billion (previously about €1.0 billion)

"Infineon continues to perform well within an increasingly challenging environment. Revenue and Segment Result both went up again in the second quarter. Global uncertainties, in particular the war in Ukraine and the further course of the coronavirus pandemic, are placing stress on supply chains. At the same time, demand for our products and solutions continues to exceed supply significantly," said Jochen Hanebeck, CEO of Infineon. "Decarbonization and digitalization will profoundly change the world we live in over the next decade. We are actively driving this change, while at the same time seizing these opportunities to generate profitable growth."

Renesas invest and restart operation of Kofu plant

RENESAS ELECTRONICS, a supplier of advanced semiconductor solutions, has announced that it will conduct a 90-billion-yen worth investment in its Kofu Factory, located in Kai City, Yamanashi Prefecture, Japan. While the Factory was closed in October 2014, Renesas intends to reopen the fab in 2024 as a 300-mm wafer fab capable of manufacturing power semiconductors.

As the momentum for carbon neutrality grows, demand for highly efficient power semiconductors, which supply and manage electricity, is expected to dramatically increase globally over the years. Renesas especially anticipates rapid growth in demand for electric vehicles (EVs), and therefore plans to enhance its production capacity for power semiconductors such as IGBTs, in order to contribute toward decarbonization. Once the Kofu Factory reaches its mass production, the total production capacity of Renesas' power semiconductors will double.
The Kofu Factory of Renesas Semiconductor Manufacturing Co., Ltd., a wholly-owned subsidiary of Renesas, previously operated both 150mm and 200mm wafer fabrication lines. To boost its production capacity, Renesas decided to utilize a remaining building of the factory and revive it as a 300mm wafer fab dedicated to power semiconductors.

"Sustainability is at our heart and with 'To Make Our Lives Easier' as our Purpose, we want to build a sustainable future where our semiconductor technology and solutions help make our lives easier," said Hidetoshi Shibata, President and CEO of Renesas.

"This investment enables us to have our largest wafer fabrication line dedicated to power semiconductors, which are key to realizing decarbonization. We will continue to conduct necessary investments to enhance our in-house production capability while further strengthening ties with outsource partners. To address the mid to longer

term demand growth, Renesas remains committed to ensuring security of supply in order to provide our customers with the best possible support."

With the Japanese Ministry of Economy, Trade and Industry's Strategy for Semiconductors in consideration, Renesas plans to conduct its investment within the year of 2022, while closely coordinating with the Ministry. While this investment will not have a material impact on Renesas' performance for the year of 2022, an announcement will be promptly issued if, following this investment, any material impact is made.

Electronics supply chain challenges are getting worse

SUPPLYFRAME has unveiled the results of its latest Commodity IQ Report that provides an overview of market dynamics (pricing, lead time, demand...) in the electronics industry. Geopolitical uncertainty and wide-ranging impacts from the armed conflict in Ukraine, alongside global inflation, and recurring COVID-19 outbreaks are compounding the situation and testing beleaguered industry supply chains.

The second quarter of 2022 began much the same as the first quarter concluded, with nearly half of all Supplyframe Commodity IQ dimensions characterized as worsening, and we saw a continuation of strong demand, production at capacity, extended lead times, and rising prices plaguing most devices. Looking ahead, for the next four quarters, the active components market remains stubborn and hostile. From analog power to standard logic to ASICs and sensors, it is a sea of red indicators. Passive component dynamics are not as constrained as their active counterparts, as evidenced by the higher number of yellow dimension forecasts for most sub-commodities except frequency devices and resistors.

Between Q4 2021 and Q1 2022, most of the components saw a modest increase in numbers when looking at design and production. Capacitors (-18%), PLDs (-13%), sensors (-8%), oscillators (-2%) and signal devices (-1%) are the exceptions who saw their design metrics drop. On the other hand, demand continued to rise for the vast majority of components, with MCUs & MPUs recording the strongest increase (+11%), followed by relays (+10%).

Between Q1 2022 and Q2 2022, in terms of design and production, most of the components saw their capacity improve, with standard logic devices recording an increase of 12%. The only components who face a decrease in design in the same timeframe are connectors (-15%), relays (-4%), oscillators (-2%) and signal devices (-1%).

As for demand, it's still trending upwards over the two quarters but more steadily than what we saw in previous editions of Commodity IQ. It's still worth noting that the components facing the biggest increase in demand in the Q1 22-Q2 22 timeframe are signal devices (+30%), capacitors (+15%), and circuit protection devices (+15%).

The situation is not getting any better. Commodity IQ paints a pessimistic picture, with supply chain challenges that will continue through 2023. The electronics supply chain can expect growing challenges into next year. Through the first quarter of 2023, more than 70% of lead times are forecast to increase. During that time frame, analog, complex semiconductor (ASICs, MCUs, MPUs, PLDs), flash memory, non-ceramic capacitor, resistor and standard logic devices are forecast to rise in price (+85%) with very limited exceptions. Most of the same devices will also remain at or exceed already elevated lead times (+83%).

Critical manufacturing releases V9 of MES platform

CRITICAL MANUFACTURING, a provider of Manufacturing Execution Systems (MES) for Smart Manufacturing and Industry 4.0, has announced the release of version nine (V9) of its successful Manufacturing Execution System (MES). The platform, which provides manufacturers with a powerful and flexible pathway to Industry 4.0 (I4.0) manufacturing, is proven to deliver increased efficiency, enhanced quality and yield, and a way to deal with fast-paced, constantly changing markets and customer demands. The new version supports continually changing market landscapes with more flexible deployment architectures, faster revision handling, powerful data management tools, and robust security.

The latest version of Critical Manufacturing's MES uses manufacturing-specific DevOps Center to enable software to be reliably deployed to multiple plants located anywhere in the world, not only ensuring easy implementation, but also providing a single, enterprise-wide platform that can be readily and continuously improved.

Francisco Almada Lobo, Chief Executive Officer and co-founder at Critical Manufacturing, says, "Version 9 of our MES delivers the rich functionality and flexibility needed for sophisticated and complex manufacturing environments along with modern software configuration management tools. Cloud support, containerization and streamlined remote deployments are all integrated to ensure enterprise-wide operations are controlled and can be continually and easily updated to meet new market demands."

Critical Manufacturing MES V9 uses the DevOps Center and containers technology to enable MES deployment within a matter of minutes in the cloud, on-premises or across hybrid infrastructures. It enables users to manage product variations using a unique combination of versions, revisions and context resolutions flexibly and efficiently. It provides a new level of agility to effectively manage market uncertainties, support continued market competitiveness, and foster innovation.

Supporting I4.0 implementation, Critical Manufacturing's MES using decentralized logic to enable dynamic production with smart products and materials automatically interacting with intelligent machines to ensure optimized production efficiencies. It incorporates an IoT Data Platform for fully scalable, real-time data processing and a Connect IoT module that accelerates the integration of devices and equipment into the platform

The MES provides a complete digital twin of the shop floor to ensure total visibility of operations and performance against key performance indicators (KPIs). Designed for easy 3D modelling of the plant, it further supports augmented reality (AR) scenarios. Critical Manufacturing's experts will be hosting a webinar on June 8th to facilitate the launch of the new V9. To learn more about the new V9's features and full capabilities, register for the webinar by clicking here.

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Okmetic invests €400 million euros to build new fab in Finland

SILICON WAFER manufacturer Okmetic will build a new production facility next to its current silicon wafer fab in Vantaa, Finland. The investment is to more than double the company's production capacity and business and create over 500 new jobs. Construction will commence in early 2023, at the latest, and the fab is planned to be in production use during 2025. With silicon wafer demand surging due to the proliferation of electronic components, the investment helps the company meet the growing demand of customers.

Okmetic supplies advanced, customized silicon wafers for the manufacture of MEMS, sensor, RF and power devices. This investment to a new production facility totaling nearly 400 million euros will more than double the company's business. It is the largest investment in Okmetic's history. Over the last five years, the company has invested over 100 million euros in increasing the production capacity of its Vantaa fab, and the new production fab is yet another chapter in the company's growth story as a provider of high value-added silicon wafers in a rapidly growing and developing industry.

We have experienced strong growth for several years now, and market forecasts suggest the positive development will continue in the semiconductor industry. The new fab will strengthen the company's position in the market and lay the foundation for the future development of our business. In a bigger picture, the investment can also be seen as part of the European push towards more self-sufficiency in the global semiconductor value chain. However, overall focus will be on global markets, says Okmetic President and CEO Kai Seikku.

The investment is one of NSIG's commitments to expedite Okmetic's further growth with greater business scale and stronger market position, leveraging on Okmetic's strength on specialty technologies, says Dr. Chiu Tzu-Yin, NSIG President and Okmetic chairman. It will also enable NSIG – the parent company of Okmetic – to play a more prominent role in the global semiconductor silicon wafers supply chain.

The new production fab of over 40,000 m² (clean room area – 6,000 m²) will be built next to the current fab, maximizing synergy between them. Production in the new fab will mainly focus on current products and markets. SOI production (Silicon-On-Insulator) will be centralized in the current fab, with 200mm DSP (Double Side Polished) wafer and SSP (Single Side Polished) wafer production and crystal growing expanded to the new fab.

The overall production capacity of the fabs will more than double the current capacity. Planning for the production fab has already begun, and the construction is set to begin in early 2023, at the latest. Following equipment installation, the new fab is expected to be in full operation in 2025. The new fab will feature state-of-the-art equipment and production lines and attention will also be paid to improved energy efficiency and complying with tightening ESG standards.

Okmetic currently employs approximately 600 people, and the investment will enable the hiring of more than 500 new employees. Recruitment will commence right away and gradually continue until the launch of the new production fab. New vacancies will include both white-collar and production work positions.

In 2022, the semiconductor market is expected to continue to grow and surpass 600 billion dollars for the first time. The growth has been driven by key technologies such as 5G, AI, IoT and autonomous vehicles. With the high growth rate, component shortage has posed a challenge for the entire industry. Following this investment, Okmetic can better respond to increasing customer demand.

Okmetic supplies silicon wafers for the manufacture of MEMS, sensor, RF and power devices, markets where growth is expected to continue and where the 200mm diameter silicon wafers are predicted to retain their position as the primary platform. The company has extensive 150 to 200mm silicon wafer portfolio comprising of comprehensive lines of SOI wafers and High Resistivity RFSi® wafers as well as Patterned wafers, Single Side Polished and Double Side Polished wafers, TSV wafers and Wafers for Power devices.

Okmetic is actively involved in different kinds of collaborative semiconductor research and EU projects aiming to develop groundbreaking microelectromechanical systems. The company also is an integral part of the wide-scale MEMS cluster in Finland.

Manufacturers are adopting MES to increase productivity, cut costs

Leading semiconductor makers were among the first to use manufacturing execution systems (MES) to achieve Industry 4.0 efficiencies. Small and medium-sized companies are also considering this as a means to automate manual processes, eliminate disparate legacy systems and make data collection actionable. The MES experts at Critical Manufacturing describe how the process benefitted IC manufacturer Vishay Passives that expects to replicate its success at a US plant across many global locations

VISHAY is a leading global manufacturer of passive components and semiconductors. The company was seeing increasing demand in volume and diversity in its product line-up, so it made the decision to accelerate its move towards Industry 4.0. After deploying the Critical Manufacturing MES at a pilot site in Yankton, South Dakota (USA), Vishay is already seeing the benefits of its initial steps towards a smart manufacturing future.

The production of semiconductors (both actives and passives) involves the most complex manufacturing processes anywhere. The rising costs of bringing new chips to market, increasingly complex customer requirements and demands for higher quality, lower cost products are creating challenging times for the industry. Disconnected sites and siloed information make it difficult for companies

to implement continuous process improvements, reach efficiency targets and maintain increasing demands for higher quality. Indeed, increasing the production of semiconductors of all types has become an international priority. Supply chain disruptions resulting from the COVID-19 pandemic and manufacturing inefficiencies all point to a tremendous need to rethink how these vital devices are made.

Vishay manufactures one of the world's largest portfolios of discrete semiconductors and passive electronic components. While this portfolio breadth delivers benefits to its customers, it also brings enormous diversity and complexity in the manufacturing IT landscape, production processes, and ways of working.

Vishay Passives has over 30 plants located throughout the world with more than 50 legacy manufacturing systems. Alongside the need to reduce the incredible IT support overhead needed to maintain these systems, Vishay's decision to standardize and harmonize information systems across these sites was based on its need to increase automation and intelligence, reduce costs, handle increasingly complex products and processes, increase production efficiency, and enhance the company's business agility to respond to changing customer demands.

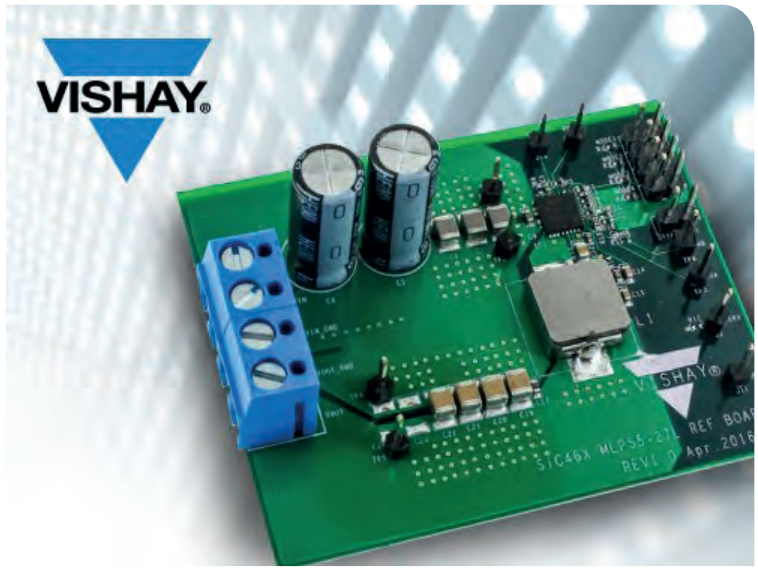
The primary requirements Vishay had while selecting the vendor for its new MES included suitability for complex electronics / discrete manufacturing, ease of multi-site installation, scalability, ease of use, flexibility, and configurability without the need for IT support for day-to-day changes over the long term.

Following an in-depth selection process which began at the start of 2017, the first of the new MES systems at Yankton is now fully operational and being hailed a huge success.

About Vishay Yankton

Yankton is one of Vishay's mid-size plants, employing around 300 people. It has four distinct product lines and processing styles covering standard inductors, medical inductors, custom magnetics, and connectors; it also produces its own powders for standard product housings. Its shop floor needs to handle a remarkable diversity of products ranging from new innovations to the support of products with a 50-year history.

The site at Yankton had a 'home-grown' legacy system and its plan to roll out Critical Manufacturing's MES involved a gradual replacement of this system's functionality with a new digital backbone provided by the Industry 4.0-ready MES. One key factor that made the conversion process more challenging than most instances was a requirement that system deployment could not stop production for more than a few days; the pilot



system was installed with only a minor, temporary impact on productivity.

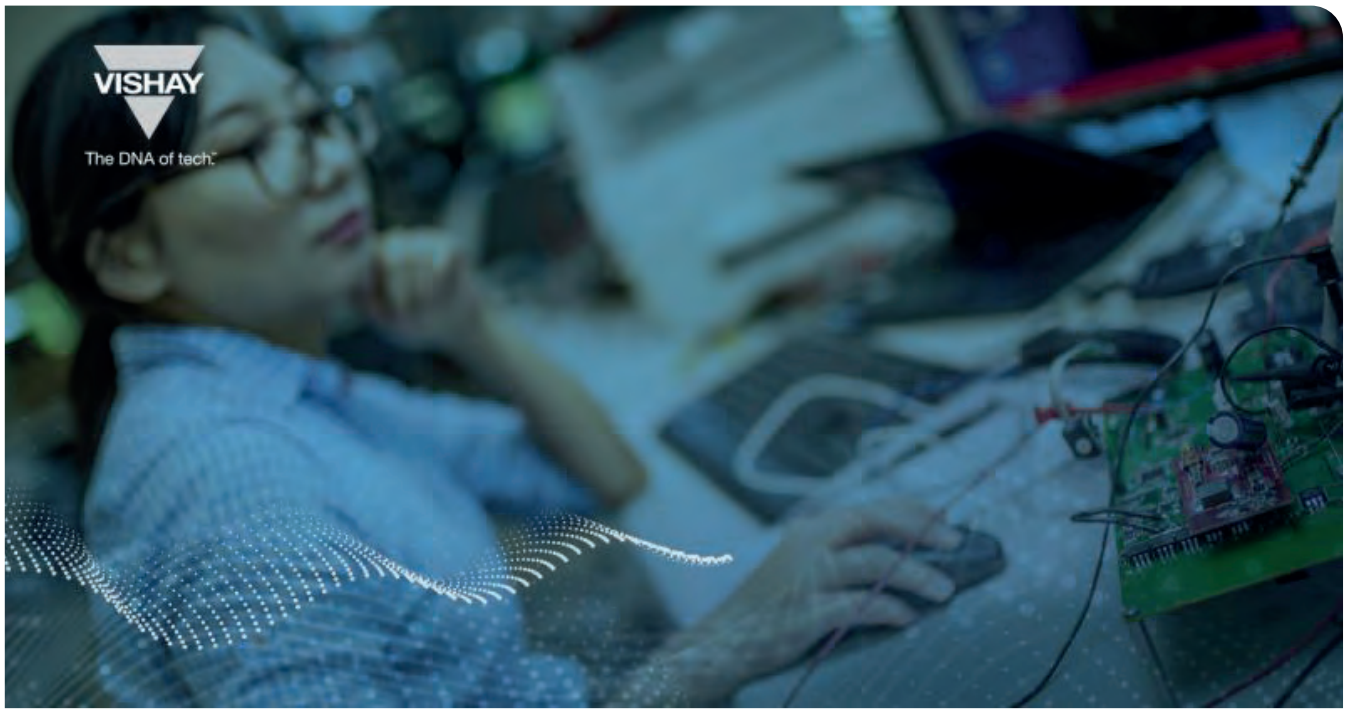
While completely replacing a complex manufacturing plant's entire core IT systems would no doubt have been a daunting prospect 10 or 15 years ago, Critical Manufacturing's CEO, Francisco Almada Lobo, said the rapid conversion with little to no down-time is feasible today for MES vendors that work extensively with complex infrastructure such as Critical Manufacturing.

"This is becoming more mainstream. Companies realize the need for more aggressive digital transformation programs, and the need to map physical and business processes as granularly as possible (creating digital twins) is essential to be able to monitor and control these processes, beyond using the data generated for traceability and for creating value-added insights. When corporations have multiple plants, then such a program reaches a completely different order of magnitude. It is necessary to account for the differences between the plants and to create templates that can be applied across the different plants – otherwise the transformation program could easily take decades to do," said Lobo.

Adam Schilousky, Vishay's Senior Director, Global Operations, Inductors Division, Custom Products, said, "We never had an instance where we shut production down or could not get something resolved within a day."

Using agile project management methodology, Critical Manufacturing supported the entire system set up at Yankton with 36, two-week agile sprints to completely implement the system across four distinct areas of production at the facility, each with their own processing style.

"Technology has evolved a lot and it's possible today to introduce automation and processes step



by step to replace existing systems or introduce them where they don't exist yet. This doesn't require massive teams, and actually the key is to involve the persons being impacted by the introduction of the system. This is critical because although there's no impact from the perspective of bringing the factory down, there is impact in terms of processes. If a company operates in a manual mode using less optimized processes, just connecting them to a new software programme is a digitization (aka paper on glass), but that alone is not a digitalization or a digital transformation, which requires transforming the processes to become more efficient or to gather data to allow better business decisions," Lobo observed.

From the 'Stone Age' to the 21st century

Commenting about the immediate impact of the MES, Schilousky said, "It has created a profound change in our operations and a radically new way of working. It affects many areas in the value stream, including planning, purchasing, accounting, production, inventory control, quality, and engineering. The difference is so dramatic, it would have been difficult to calculate a true ROI."

Vishay has already seen multiple benefits of the new MES. The system provides them with complete data transparency for divisional operations and an effective solution for raw material quality inspection, something that was not available before. Controllers and planners have visibility of all work in process (WIP) materials and products as well as the production status of each running order.
The new MES further reports consumption of person-hours back to the enterprise resource planning (ERP) system at each production step, providing detailed and accurate data for product costing management. Further, tracking and tracing the yield of each production step, as well as for the total line has many purposes, including improving customer satisfaction in highly regulated industries. Vishay reports that the automatic archiving of all data greatly streamlines audits; the smooth material flows from incoming quality checks to production release has eliminated job delays and plant stoppages completely.

The MES handles incoming material quality disposition and only releases an order when all material is available. This greatly increases overall equipment efficiency (OEE) and has eradicated the delays because of material shortages.

Advanced integration

Based on decentralized logic, the future-ready MES enables communication between intelligent machines and products. By connecting systems, materials, and products together, manufacturing efficiency is enhanced, and capability added to enable the rapid production of highly customized products. The MES provides the vertical integration needed to ensure corporate processes are enforced and the horizontal integration to provide complete visibility across production processes throughout multiple factories, wherever they are located. Vishay's new MES not only integrates machines and processes, but it is also tightly integrated with Vishay's ERP platform and the time and attendance portion of the old legacy system. All material movement data is sent to the ERP, which owns the bill of materials (BOM).

Next steps

The successful deployment of the MES at the Yankton site has been followed by installations at two other Vishay Passive divisions in a new plant

in China, where the system has been successfully installed; it has gone partially live and is in the final phase of roll out.

Dr. Thomas Amrein, VP Planning & Systems Passives, is responsible for the global MES implementation program at Vishay Passives; he said, "As a new greenfield site, the new plant in China is more highly automated. As a result, this will test the automation layer of the MES more completely. As we expand to all our plants around the world, we will see how quickly we can complete installations using the same template and with more and more standardized processes. In addition, we will increase the number of features we use in the MES, like machine maintenance or planning and scheduling."

The modularity and configurability of the new MES means it is inherently flexible and adaptable to individual site requirements and changing business needs. It will provide Vishay with much more data, insight and analysis about its products and processes to support strategic decision making. Vishay expects to measure improvements once the system has been operational at Yankton and other sites for at least a year.

What makes a digital transformation successful as a useful investment for a manufacturer? This of course depends on individual goals and how the new hardware and software components work together to meet the customers' needs, according to Lobo. "A true digital transformation might include converting both software and hardware. From a purely equipment standpoint, it is important that it captures essential data, requiring different levels of sensorization, as well as the ability to provide such data to software solutions.

From the computer hardware standpoint, the evolution is going into a mix of edge solutions, running closer to the machines to ensure low latency and short feedback loops, and centralized data storage solutions, which could be public or private clouds, or even shared data centres. From a data standpoint, once central solutions are used, this data is much more easily mined and learned from, creating true value-added insights," Lobo remarked.

Summary

With its new MES backbone, Vishay is on the path towards Industry 4.0. Ultimately, the new system will replace over 50 legacy systems and, as well as giving greater visibility and tighter process control, will free an enormous amount of IT resource to innovate and concentrate on value-add activity.

Only time will tell how quickly Vishay will realize its full ROI, but it is already seeing huge benefits. Indeed, the excitement about the potential of the new solution means its other sites around the world are vying for position as to which one will be next in the global rollout.

Automotive and consumer applications are benefitting from silicon photonics technologies

Silicon Photonics (SiP) has benefitted from strong pull by the communications sector. By leveraging the industry's vast storehouse of CMOS and related high volume Silicon processes, materials and packaging expertise, SiP is growing beyond telecom & datacom to bring the economies and performance of Silicon manufacturing to automotive and biotech applications.

BY ERIC HIGHAM, DIRECTOR – ADVANCED SEMICONDUCTOR APPLICATIONS/ADVANCED DEFENSE APPLICATIONS, STRATEGY ANALYTICS

AS GLOBAL ECONOMIES continue to recover from COVID and the pace of events around the world quickens, the importance of broadband connectivity is clear. Countries are expanding their broadband footprints and users are clamoring for higher data rates to accommodate their growing video and application appetites. The result has been an explosion of data traffic over the past decade. The curves in Figure 1 show an extrapolation of Cisco network data for the next decade and the conclusion is inescapable; data traffic is large and growing quickly.

The red curve shows IP (Internet Protocol) data traffic and this represents any bit of transmitted data, whether that data is on a wireless or wireline network. This data extrapolation predicts traffic to increase by a factor of 125 times over the forecast period. Even more impressive is the magnitude of data shown by the blue line. This curve represents expected data traffic in data centers. This short-

reach data traffic runs between five and six times the magnitude of the IP data and it reflects the increasing importance of data communications as we have become more comfortable with the cloud and the home becomes the center of many of our interactions with the world.

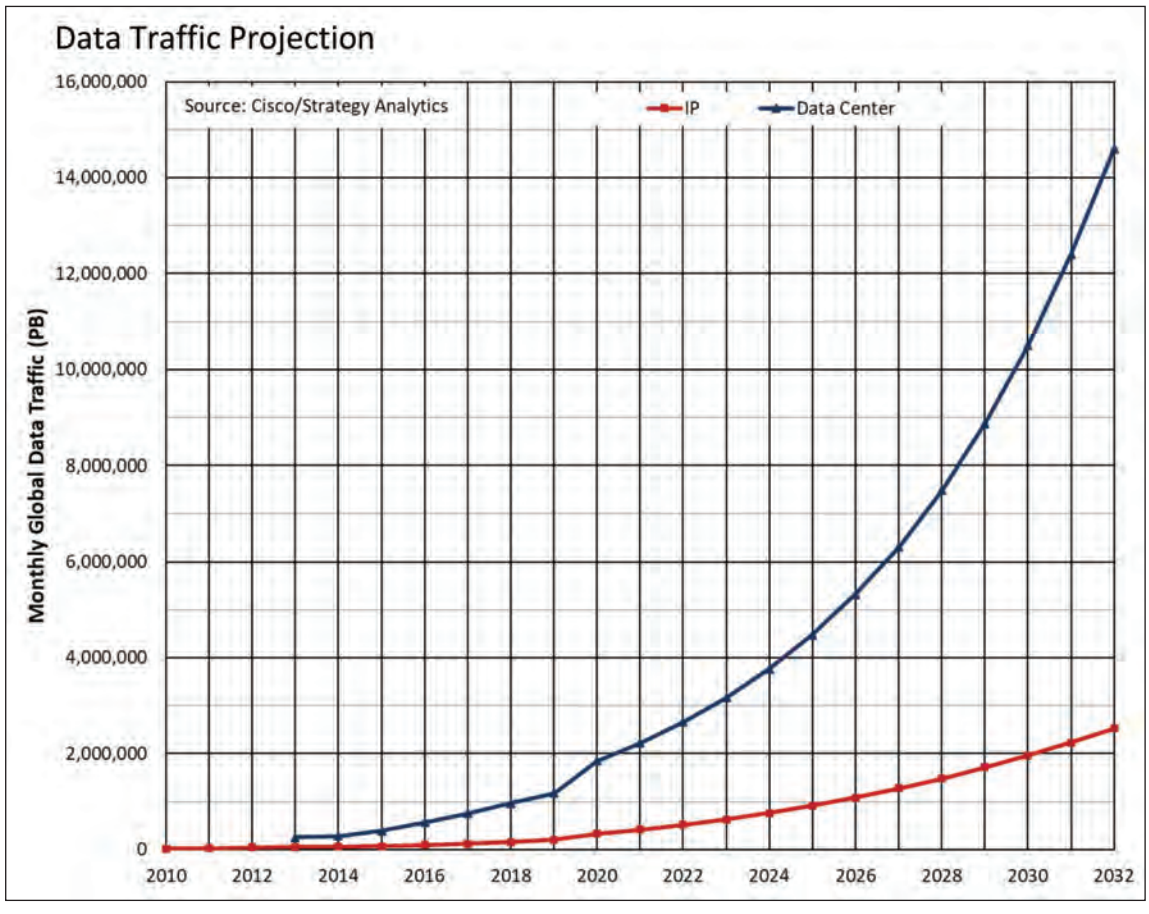
The magnitude of this communications activity is becoming clearer. The emerging 5G wireless standard will drive the entire electronics market with cellular terminals exceeding 1 billion units. There are reports of total optical transceiver shipments reaching 1 billion in the next 5 years and yearly data center port shipments exceeding 60 million in the next couple of years.

This communications opportunity, along with the technical requirements have been instrumental in the development and maturation of silicon photonics and the broader photonics integrated circuits (PIC) ecosystem. While communications opportunities currently drive the optical market, the industry is looking at other fast growth, high volume applications that could benefit from more optical content in devices and networks.

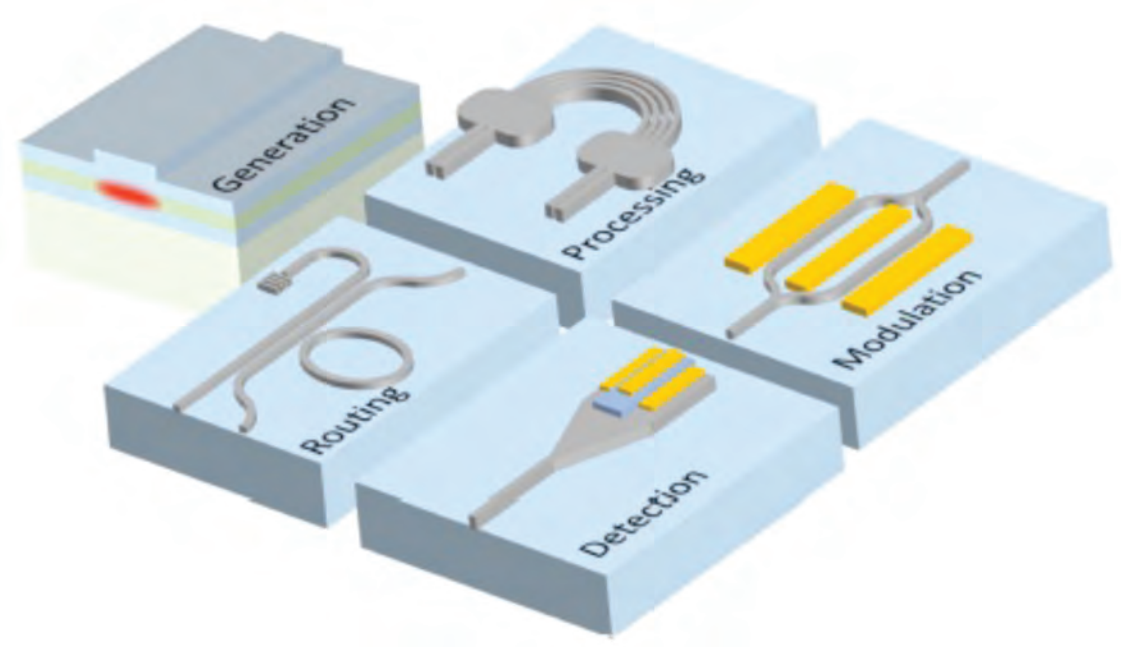
Silicon Photonics

Photonics devices face the same pressures as electronic devices to be smaller and less expensive, with better performance to enable more capabilities. The response to these challenges from optical component manufactures has been more integration. Photonic integrated circuit design and manufacturing techniques have gained traction as the component roadmap evolves to include more electrical and optical functions in an optical module. These modules are a mix of direct and coherent detection schemes and that means a variety of compound semiconductors to optimize the linear functions, along with an increasing amount of digital silicon to increase performance characteristics.

Figure 2 shows a conceptual block diagram of the functions that a photonic integrated circuit must address. As digital processing and control capabilities become more important in optical applications, silicon becomes the natural choice for an integration medium. This allows for relatively low volume opportunities to take advantage of the massive processing and manufacturing infrastructure in place for silicon technologies. Manufacturers are using existing silicon CMOS-based processes for all the functions shown in Figure 2, except for the generation function. Silicon is an indirect bandgap material, so it will not emit photons meaning that the generation function requires another technology. The silicon photonics device becomes a subset of a photonics integrated circuit, with a silicon integrated circuit accomplishing all the required functions except for the laser.



➤ Figure 1: Data Traffic Projection



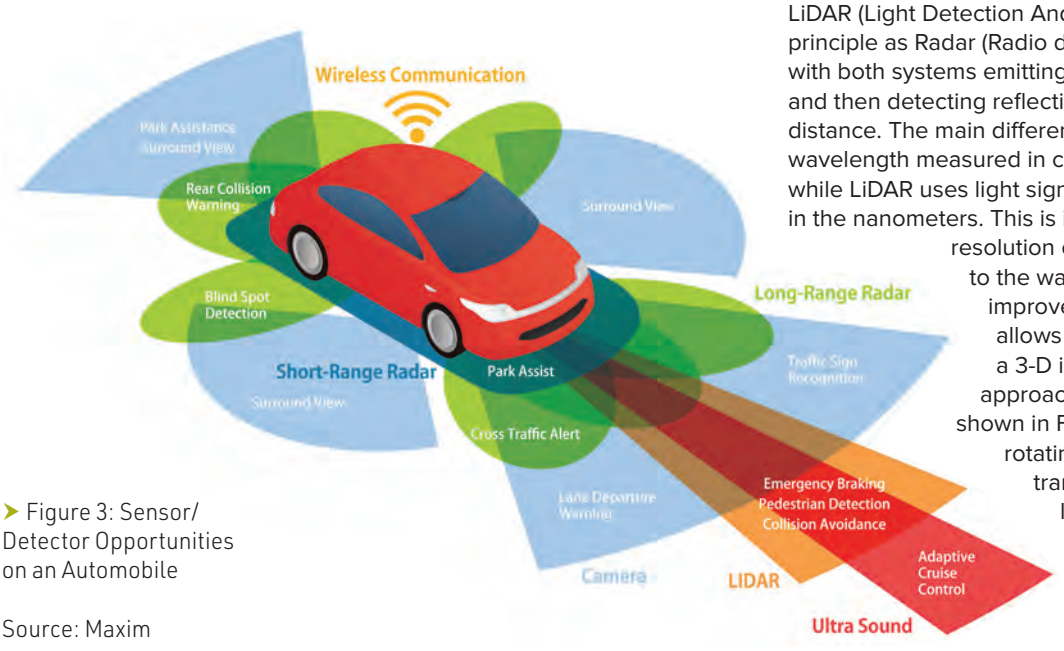
➤ Figure 2: Photonic Integrated Circuit Conceptual Block Diagram

Source: S. Y. Siew, et al, Review of Silicon Photonics Technology and Platform Development, Journal of Lightwave Technology, 2021

New Market Applications

Broadly, the optical industry is becoming extremely excited about the potential in sensing applications. Automotive platforms are generating significant interest as that industry evolves toward more electric vehicles, more sophisticated ADAS (Advanced Driver Assistance Systems) capabilities and full autonomation. After being hard hit by COVID, the automotive industry is trending toward global sales of 100 million vehicles per year and as Figure 3 shows, sensing and detection opportunities in automobiles are increasing and becoming very sophisticated. Vehicle platforms of assorted sizes and purposes are becoming webs of sensor inputs.

The term "sensor" encompasses many distinct functions and technologies. Sensors became increasingly important in automotive applications as vehicles began to incorporate more computerized functions. As semiconductor detection and processing capabilities have improved, the scope of driver assistance has increased. A thorough discussion of the full range of sensor applications and technologies is outside the scope of this discussion, but most vehicles sold today use a combination of cameras, ultrasonic sensors and radar at different frequencies to enable features like adaptive cruise control, parking assistance, automatic emergency braking, and blind spot monitoring. These technologies have advantages and disadvantages and the photonics industry is particularly interested in building on early successes with LiDAR systems to help enable the automotive industry's evolution to full automation.



➤ Figure 3: Sensor/ Detector Opportunities on an Automobile

Source: Maxim

LiDAR (Light Detection And Ranging) uses the same principle as Radar (Radio detection and ranging), with both systems emitting an electronic signal and then detecting reflections from objects in the distance. The main difference is a radar signal has a wavelength measured in centimeters, or millimeters, while LiDAR uses light signals with wavelengths in the nanometers. This is important because the resolution of either system is related to the wavelength. The resulting improvement in resolution allows LiDAR systems to map a 3-D image that begins to approach the actual image as shown in Figure 4. By using a rotating transceiver, or multiple transceivers strategically located, the system can create a 360-degree, 3-D image of the vehicle's surroundings. Of course, there are

challenges to LiDAR technology and this is where the silicon photonics industry believes it can add value.

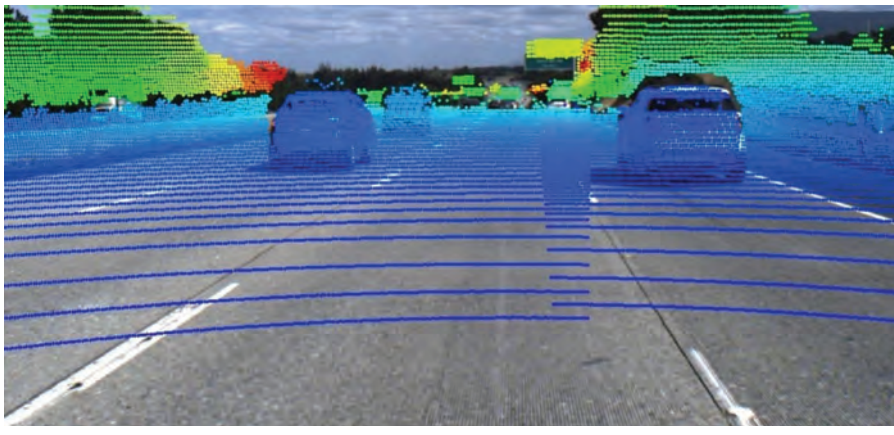
The first challenge is the appropriate system wavelength. The reflected photons received by the LiDAR system must compete with the ambient lighting to be identified as a signal. Solar irradiance in the 850nm-940nm wavelength range is about three times higher than levels at 1500nm, another popular wavelength. This added solar irradiance translates to system noise, but there is substantial development activity at 850nm and this starts to give us insight into the advantage and opportunity for silicon photonics.

The ability to detect that reflected signal depends on the material characteristics of the sensor. Silicon is responsive at wavelengths up to about 1000nm, but detection at longer wavelengths requires a compound semiconductor material. Detectors for LiDAR systems have evolved from PIN diodes to avalanche photodiodes to single photon avalanche diodes (SPAD) and silicon photomultipliers (SiPM), with the latter two methods capable of being fabricated into arrays with more capabilities. Despite the challenge posed by higher solar irradiance, wavelengths that can be detected and processed by silicon semiconductors provide cost and performance advantages.

Earlier, we mentioned achieving 360-degree coverage by rotating a LiDAR system and while early versions use this approach, the goal of LiDAR manufacturers is to develop an array approach to steer light beams in azimuth and elevation. MEMS and mirrors, along with liquid crystal metasurfaces, are array components under development, but the photonics industry is trying to develop an optical phased array (OPA). Like its RF counterparts, the OPA requires a transmit path that includes a chirped or pulsed laser source, isolators, amplifiers, modulators and splitters, along with a receive path including combiners and a detector. Both paths would also need transmission, filtering and other passive structures and that detected signal would undergo substantial processing to generate a detailed rendering like we see in Figure 4.

Except for the laser, all the necessary functional building blocks exist in process design kits (PDK) at silicon foundries currently doing optical work. The need for a discrete laser using a non-silicon technology is a challenge, but emerging silicon photonics opportunities are already embracing and optimizing this impediment. It represents an acceptable concession to access the large and well-capitalized silicon foundry and packaging industry.

Some observers believe that LiDAR deployment has been slowed by technology limitations. Words like clunky and costly are used to explain this slower than hoped adoption. The solution



➤ Figure 4: LiDAR-Generated Point Cloud Representation. Source: JD Power

to these challenges is miniaturizing circuits and footprints through integration and tapping into more cost-effective fabrication and manufacturing technologies. The emerging silicon photonics components industry is addressing all these issues as the ecosystem matures and grows. Those features, coupled with more digital processing power in shrinking silicon nodes makes silicon the likely technology choice to unlock the potential of LiDAR in automotive applications.

LiDAR has also found its way into other commercial applications. Apple includes this feature on a range of its latest devices. The LiDAR feature improves resolution and depth for more lifelike pictures. The capability is becoming important as augmented and virtual reality devices become more popular. LiDAR

The emerging silicon photonics components industry is addressing all these issues as the ecosystem matures and grows. Those features, coupled with more digital processing power in shrinking silicon nodes makes silicon the likely technology choice to unlock the potential of LiDAR in automotive applications

allows spaces to be mapped before 3-D elements are overlaid. Drones and robots use the technology for more accurate mapping and positioning.

On a broader scale, the ability of silicon to detect at wavelengths less than 1000nm (visible and near-infrared spectrum) makes this an excellent choice for biosensors. This opens a whole host of health applications such as glucose monitoring, early detection of cancer or other infectious diseases, with companies currently developing PIC-based biosensors to develop rapid testing for COVID-19. There is discussion of incorporating these capabilities into smart watches to provide medical telemetry data on a real-time basis. Other applications of the biosensor technology include detecting pollutants in the environment and chemical residues and infectious diseases in the food industry.

Conclusions

As consumers and businesses embrace more sophisticated digital capabilities, data traffic is increasing dramatically. Enabling the magnitude of this traffic explosion means that networks and devices are increasingly turning to optical transmission with that technology's enormous bandwidth capability. Like any electronics capability, as quantity and capabilities grow, size, weight, cost and performance become increasingly important.

For the optical market, this has meant a growing dependence on photonic integrated circuits that use multiple technologies and a hybrid assembly approach, along with emerging silicon photonics devices that integrate all the required functions except the laser into silicon CMOS technology. The silicon photonics ecosystem is relatively new, but it is maturing quickly and it taps into the large, established CMOS manufacturing infrastructure. While the silicon photonics solution is new, the communications and connectivity applications are not and the size of these market opportunities is a big growth engine for silicon photonics revenue.

The strong pull from communications opportunities has allowed the photonics industry to look at adjacent applications that will benefit from the advantages of silicon photonics and photonic integrated circuits. LiDAR in automotive applications is becoming one of the more exciting adjacent applications for photonics as that industry evolves toward more autonomous content and capability. Automotive volume is large and while there are still challenges to address, the silicon photonics ecosystem is interested and they are developing compelling solutions to these challenges. This combination of a strong growth engine, along with new and emerging automotive and sensor opportunities underpins our bullish outlook for the photonics market.

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IC supply crunch? Engineering simulation helps ease the pain

Increasing the semiconductor supply is a recurring theme as the world struggles to reset itself after two years battling the COVID-19 pandemic. But as viral variants continue to emerge, lockdowns persist in major Chinese manufacturing centers, and the supply chain struggles to right itself, Silicon Semiconductor asked engineering simulation leader Ansys whether multiphysics simulation can speed IC development. Ansys Director of Business Strategy Christophe Bianchi shares his insights.

BY MARK ANDREWS, TECHNICAL EDITOR, SILICON SEMICONDUCTOR

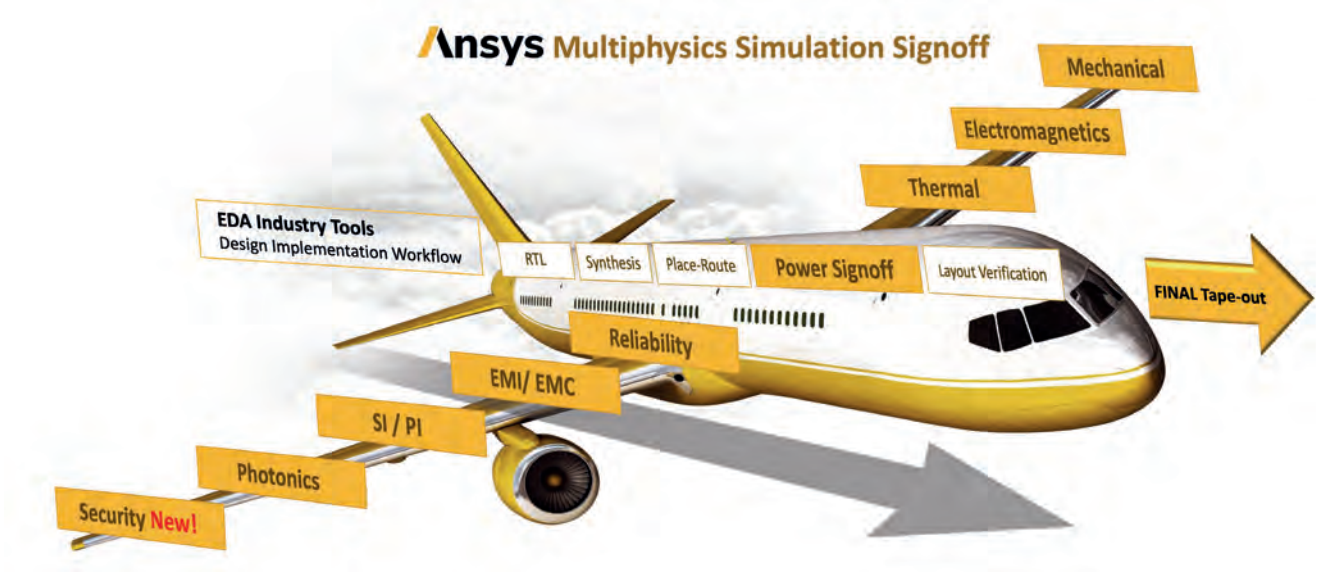
➤ Ansys multiphysics simulation can speed the design process across device types while enabling faster review and approval cycles between team members

THE CHIPS for America Act. The European Chips Act. Initiatives by GlobalFoundries, Intel, Samsung, TSMC, and more – All are efforts by governments and manufacturers to grow semiconductor supplies when a lack of ICs of every type has dogged a global recovery following the calamitous years spent fighting COVID-19.

How are we doing? According to most measures, the semiconductor shortages faced by automotive, consumer electronics and commercial manufacturers are likely to continue through 2022 and into the first quarters of 2023. Shortages persist despite the fact that SEMI, the SIA and other global trade groups report that there are 60 semiconductor fabs under construction and that manufacturers have already increased production.

The what's and why's behind a persistent shortage of semiconductors have already been explored in this business magazine and many others. Essentially, getting more devices into the hands of global OEMs and contract manufacturers is going to take time. Even though the extra capacity coming online later in 2022 through 2024 will no doubt ease the crunch, can anything be done now that has not already been tried?

One place *Silicon Semiconductor* sought answers was with the engineering simulation experts at Ansys, a leader in the field that is constantly expanding its portfolio of simulation services that embraces not just the ICs that fabs manufacture, but also the in-plant processes of multiple industries.



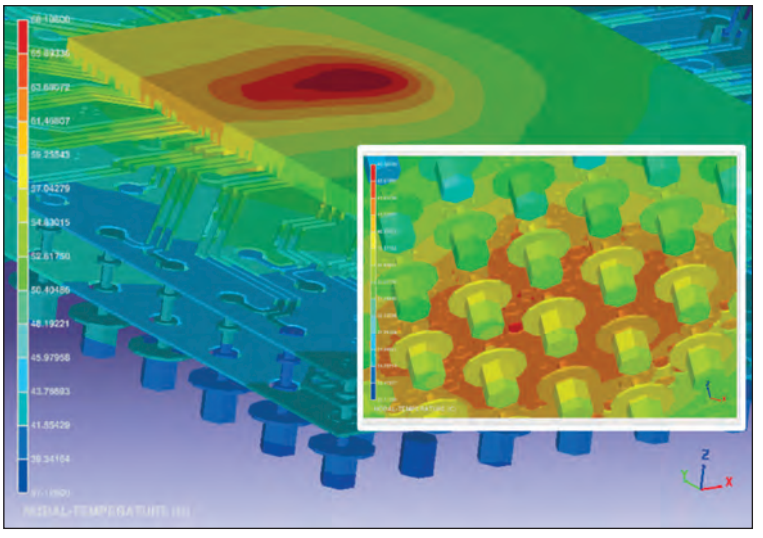
Engineering simulation has come a long ways since Ansys helped create the field 50 years ago. Today, engineering simulation offers the chance to test components in a virtual environment across thousands of scenarios that will materially affect device functionality, lifetime and adherence to specifications, amongst many parameters. Ansys reports that H3C Semiconductor, for example, uses the company's multiphysics platform to engineer an advanced processor chip for cybersecurity, AI and 5G backhaul applications, effectively improving product sign-off efficiency and accelerating product development. Through simulation, it is possible to ensure that, once in service, the chips meet the reliability, performance, and longevity requirements of their respective applications, Ansys stated. According to Ansys Director of Business Strategy, Christophe Bianchi, engineering simulation is already at work to improve quality and speed production by guiding designers away from likely-to-fail scenarios while speeding design by automatically applying years' worth of computational experience to test and verify myriad design options, materials parameters and other key metrics.

MA: *Is highly accurate engineering simulation best suited for the design phase of a new product, or can it benefit other key aspects of IC manufacturing to help close the gap between supply and demand?*

CB: Engineering simulation is pervasive across the entire engineering practice. Of course, the design phase is where trade-offs are made based on complex simulation, for example, thermal, mechanical, electromagnetic or Infrared. But simulation is also used to develop and optimise manufacturing processes, such as the Chemical-Mechanical Polishing (CMP) process, or tuning the performance of wafer handling in the fab. What we see becoming a critical use of simulation, combined with AI/ML technology, is the advent of digital twins of various manufacturing equipment (such as UV lithography tools). Here, the twin, running in the cloud or on the edge, provides invaluable information to pilot predictive maintenance and therefore optimise both performance and yield of these complex manufacturing processes.

MA: *How do today's most advanced engineering simulation programmes differ from previous generations?*

CB: Although performance and capacity remain two critical development threads in engineering simulation, for which the advent of distributed computing has provided a boost in productivity, there are two major paradigm shifts that new generations of engineering simulation impact design methodologies and product developments: Firstly, the multiphysics aspect of simulation becomes even more critical at advanced semiconductor nodes. With design margins shrinking even further, and complexity of products reaching new heights, it is now impossible to treat each phenomenon independently. The combined and interdependent effects of thermal, electromagnetic, radiation, mechanical stress, and power distribution variability must be assessed jointly in a true multiphysics way.

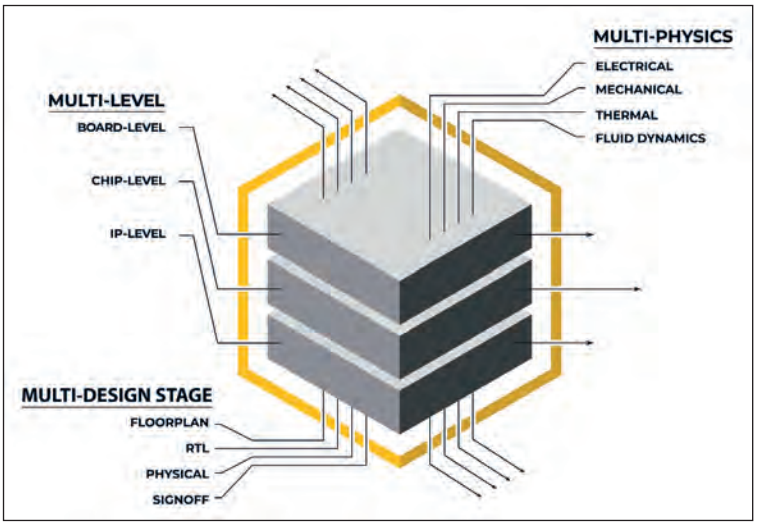


➤ Ansys multiphysics simulation can speed the design process across device types while enabling faster review and approval cycles between team members

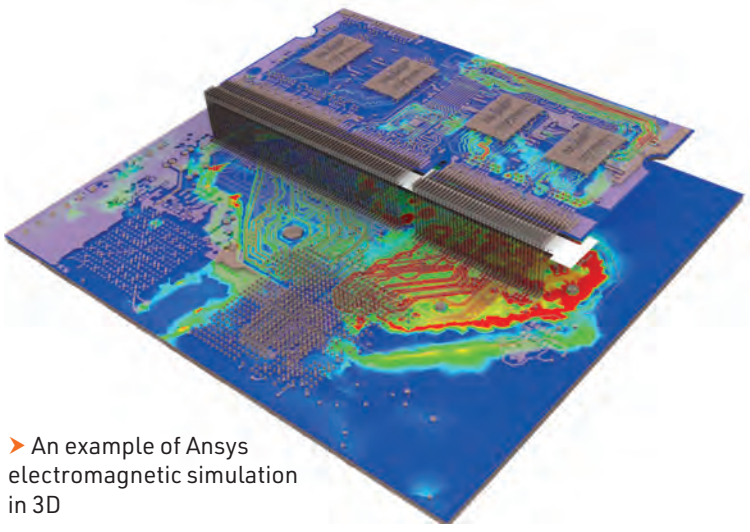
Another major shift is the advent of AI/ML methods assisting the designers and developers throughout their engineering tasks. With the increased complexity of today's most advanced engineering simulations, designers must explore much more complex solution spaces, and the help provided by AI/ML facilitates those efforts by assessing parameter sensibility, and design space optimisation using automatically trained reduced-order models for faster convergence.

MA: *Is it possible to estimate, if looking at a hypothetical product, how much time engineering simulation could save compared to developing said product without it or with outmoded tools?*

CB: I don't think it is a question of saving time when the alternative to simulation is prototyping. It is not



➤ Ansys simulation programmes can handle a wide variety of engineering requirements including IP validation and sign-off protocols



➤ An example of Ansys electromagnetic simulation in 3D

just the exorbitant cost of prototyping (reaching above $1 million in advanced semiconductor nodes), but the sheer fact that the chances of silicon success without simulation is close to zero, and that is what makes engineering simulation an essential part of the design cycle. I cannot think of a situation where a design team would risk developing a product without simulation for the sake of development time.

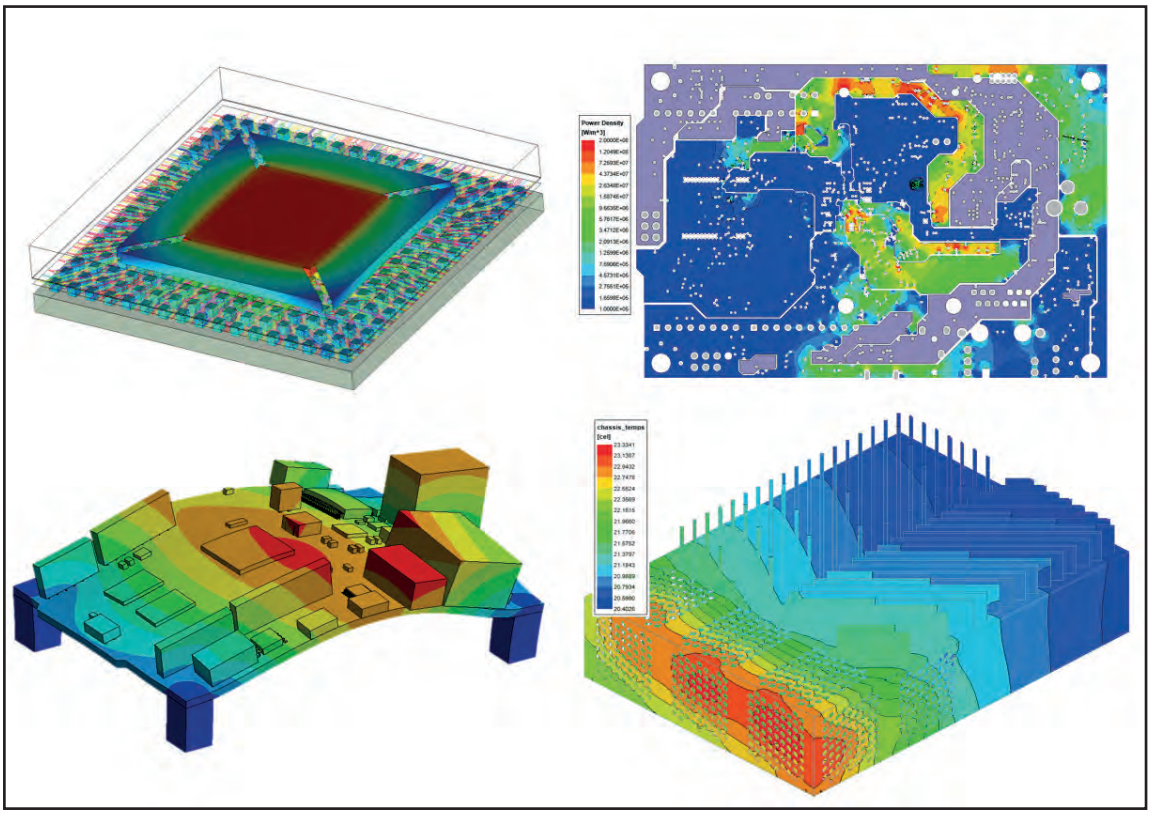
MA: *One challenge semiconductor manufacturers faced during 2020-21 that persists is addressing demand in a more agile fashion, such as rapidly changing what is being manufactured. Can engineering simulation help manufacturers rapidly retool?*

CB: The IC supply crisis the semiconductor industry is currently facing is more a capacity than an agility problem. As the most affected industry by this problem, the automotive sector did not foresee the impact of "just in time" inventory practices when facing fierce competition from computing and communication for the same manufacturing capacity. These industries rebounded faster during the pandemic and secured the wafer supplies, leaving no room for peak demand from auto Tier 1s and OEMs. Running at (or slightly above) full capacity, further agility would not really solve the IC shortage crisis.

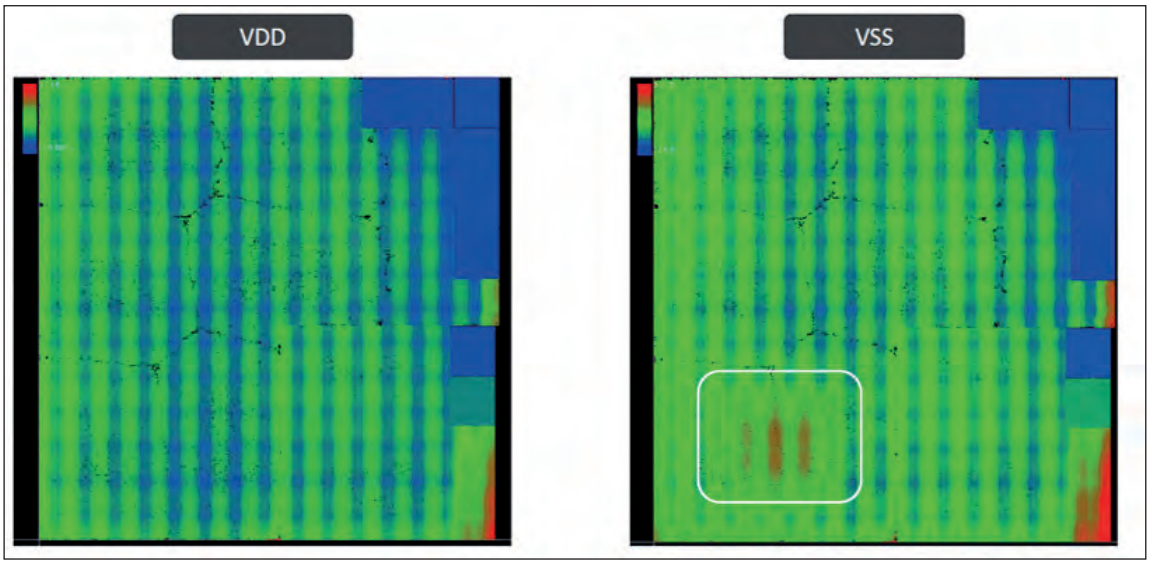
On the other hand, leveraging engineering simulation to tune and improve manufacturing yield has the potential to increase production throughout, without the delay and investment required for additional capacity. This is an area where several initiatives have been launched since the beginning of the crisis, ranging from modelling and simulation of process variability to digital twins of complete manufacturing toolchains.

MA: *If better engineering simulation can indeed shorten lead times in some circumstances, are there other factors manufacturers ought to consider to address rapidly changing customer needs?*

CB: In the automotive sector, the shortage of devices resulting from a combination of ultrafast demand change and a "just in time" inventory



➤ A sampling of various multiphysics simulations at differing scales



➤ The Ansys Redhawk SC Security application assesses build quality metrics (BQM) and in this example detects a weakness in the VSS grid

strategy have been exaggerated by the extremely large number of different components required to equip today's cars. Calls for more standardisation and a move towards software-defined systems (using less and more standardised programmable devices) are two of the ways we are seeing improvements. But developing such multi-purpose devices brings an order of magnitude in the design complexity and requires significantly more simulation in the development and design phase.

MA: *Engineering simulation has grown more sophisticated and capable. Can you please describe key breakthroughs or developmental milestones that enabled this progress?*

CB: Ansys has been refining the art of engineering simulation for the past 50 years and is not planning on stopping. Our history of acquisitions demonstrates the will to combine more and more laws of nature in our multi-physics solutions: for instance, we recently added photonics and optical simulation.

The main research and development axes that have increased the capabilities and sophistication of our solutions range from continuous research in numerical methods (For example, iterative solver methods, explicit/implicit/hybrid/bayesian computational model) to AI/ML improvement of the parametrisation of our solvers, high performance computing (task-based, shared memory, message passing, fine grain (GPU) and the future use of exascale and quantum computing) as well as platforms, workflows and data management - all targeting a more pervasive use of the cloud.

MA: *Can better engineering simulation enable a reduction in the number of prototypes a manufacturer needs en route to rolling out a new product?*

CB: Physical prototyping, in the development of semiconductor devices, is an extremely costly and time-consuming effort. A 7nm mask set costs about $15 million (3x the cost of 16/14nm node) and prices almost double when moving down to 5nm. But this cost remains small in comparison with the total development cost of the chip. (An advanced-node large SoC development is estimated to cost around $200-$300 million). Due to the large number of parameters (and physics) that can impact a chip's behaviour, performance and quality, simulation can provide a guarantee of convergence of the design effort, whilst solely prototyping would lead to an uncontrolled number of iterations.

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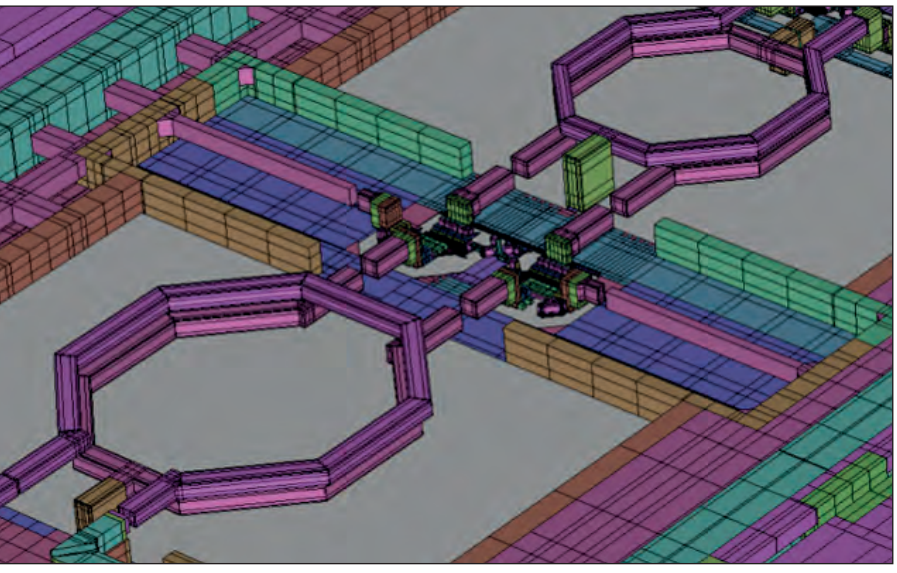

➤ A depiction of an RF coil simulation designed to detect potential flaws in the device makeup

MA: *Could you please describe some key ways developing a new device today is assisted by Ansys software compared to development with little to no engineering simulation?*

CB: Using engineering simulation enables the integration of physics constraints early in the design cycle. By taking into account the electromagnetic and Infrared effects at the planning level, designers can optimise PDNs (Power Distribution Networks) for higher performance (less DvD impact on timing), higher reliability (less fatigue and electromigration) and lower cost (optimised power grid).

What was a signoff, late-stage process in former design methods becomes a mandatory component of design planning and convergence for more complex advanced 3D ICs where multiple elements must be co-simulated in a true Chip-Package-System (CPS) view of the IR/EM/Mechanical and Thermal phenomenon impacting performance and reliability.

MA: *Many of today's advanced devices are developed by multiple engineering teams working on different aspects of the same project. How can engineering simulation aid dispersed design teams?*

CB: The physics impacting a chip's behaviour are not limited to the sub-system or component being developed by an individual contributor. These effects cross the system's hierarchy; creating physics-true bloc and chip models (power, electrothermal, etc.,) is essential to manage parallel engineering efforts. Let's consider, as an example, a 3D IC project that consists of 2 silicon dies in a complex package. These projects are usually split between 3 different teams (Die 1, Die 2 and Package). The computing and exchange of CPMs (Chip Power Models) of the two dies between the separate design teams is critical to avoid specific integration and EM/IR problems on each chip. This also reduces drastically the amount of data required to run the validation of each die (CPMs are compact models and replaced hundreds of Test Vectors). This issue is even more relevant when thermal analysis is to be performed as it is impossible, without using CPMs, to decouple heat emitters (dies) from the heat dissipater (package).

MA: *Developing future ASIC generations often begins with what worked in a previous generation. How can engineering simulation support faster, more accurate generational evolution?*

CB: The use of AI/ML to increase productivity and performance of design teams requires large amounts of data. When transitioning from Generation A to Generation B of a line of ASIC products, all the simulation and design data created in the previous generation is an extremely valuable dataset to train ML algorithms that will guide the designers in their new development. This data-driven method is becoming an essential component of the new design methodologies and must be combined with intelligent Simulation Data Management solutions to enable breakthrough productivity gains.

MA: *How can engineering simulation programmes benefit the development of entirely new devices?*

CB: Engineering simulation is as important in the case of a totally new product. And if historical data is lacking, our learning algorithms can automatically create the various configurations and parameter sets required to launch the simulations that will produce the data needed to build physics-informed optimisation solutions for the new design. Whether totally new or incrementally constructed, an ASIC is governed by the laws of physics and therefore must be modelled and entirely simulated, taking into account a large set of parameters (thermal, Infrared, electromagnetic, mechanical, etc.,) in order to guarantee first-silicon success.

MA: *Does engineering simulation aid in IP management and sourcing?*

CB: This is a very relevant question: what we are witnessing and supporting is the move towards stronger demand from IP users to IP suppliers for accurate, "true to physics" models for the IPs. These models are critical to the validation of the full system and the absence of such models can force an IP user to switch supplier. When moving from one technology node to another, even if the IP functionality remains the same, all these models have to be recreated as the physics (EM, IR, Thermal, etc.,) are highly process-node dependent.

MA: *Cybersecurity is a well-established concept, but device level security design adaptations are relatively new. Can engineering simulation help designers create ICs less susceptible to corruption?*

CB: In the emerging Internet-of-Things (IoT) market, data security and privacy are essential concerns for

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communication between a large number of ubiquitous edge devices and the internet backbone. While modern cryptography is heavily used in IoT devices to assure information security, it can be compromised by exploiting vulnerabilities in the physical implementation of underlying integrated circuits. Side-channel leakage analysis (SCLA) is a technique to extract sensitive information from sub-optimally protected hardware by probing a variety of physical phenomena, such as power consumption, electromagnetic radiation, and thermal emissions. As ICs cannot be altered in the field, it is essential to verify side-channel countermeasures in the pre-silicon design stage.

At the end of 2021, Ansys released a breakthrough technology (Ansys Redhawk SC Security) leveraging its multiphysics simulation platform that enables system-on-chip (SoC) design teams without hardware security background to predict and quantify design vulnerabilities to side-channel analysis and assess the effectiveness of their design.

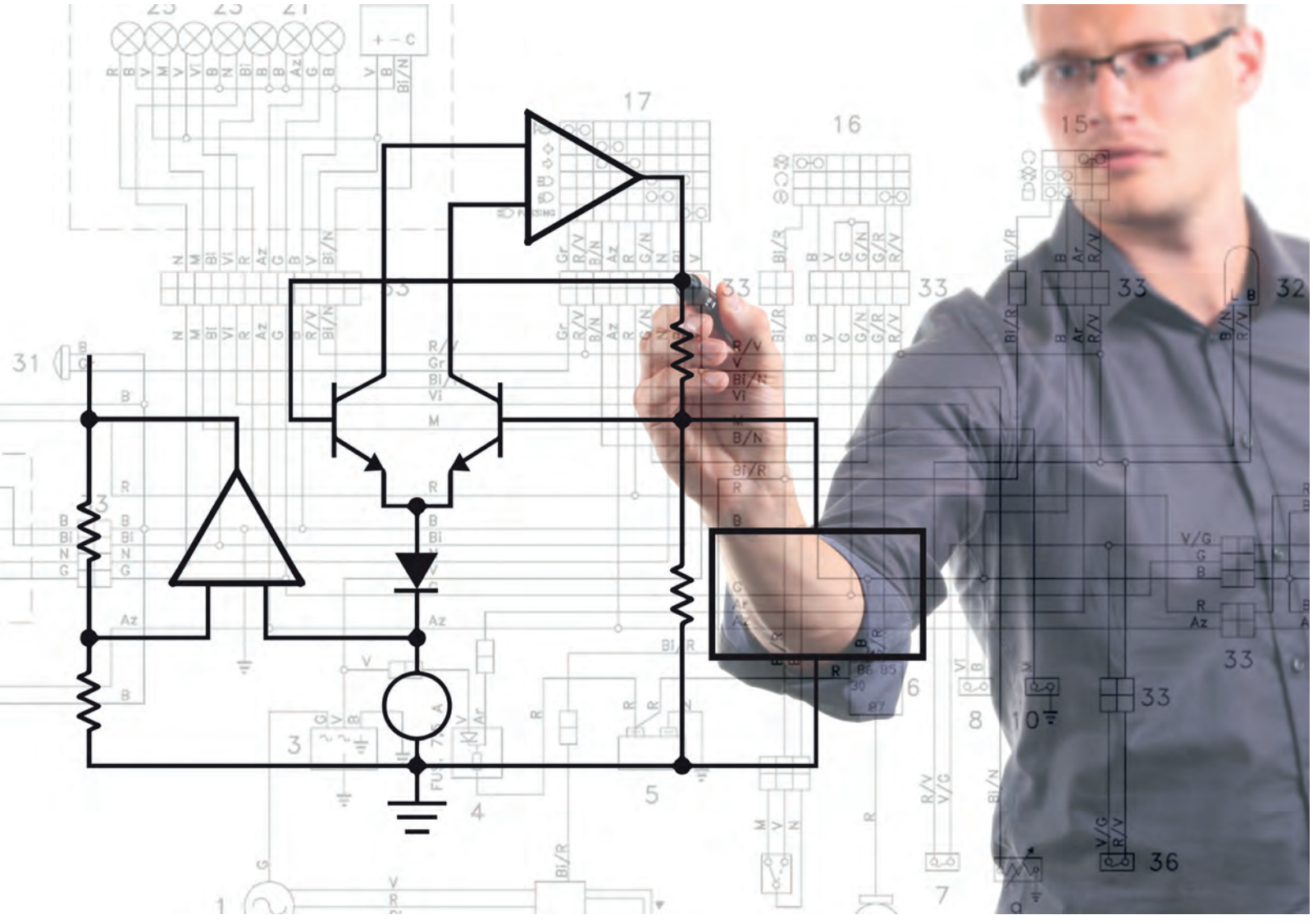
But security is also a system-level concern and, across the entire electronics architecture, we are using additional technologies (named Ansys medini analyse for Cybersecurity) that carry out system-oriented cybersecurity analysis strategy to quickly identify vulnerabilities and design weaknesses, and address them to mitigate any real-world threats by implementing key security analysis methods (TOE modelling, Attack Trees, Threat Analysis and Risk Assessment (TARA), Vulnerability Analysis, etc.) in one integrated tool.

MA: *Engineering simulation is rapidly evolving. Could you please consider what the future of this technology may hold for the semiconductor industry?*

CB: Engineering simulation will continue to broaden its scope to all industries as we are already seeing in fields such as Healthcare (with simulation assisted surgery and, on digital twins of human organs) and agriculture (with simulation-driven crop planning and autonomous farming machines)

From an underlying technology standpoint, we will continue to leverage the innovations in high-performance computing for on-the-cloud and on-the-edge deployment of simulation, along with continuous development of data-driven physics-informed machine learning methods. The pervasiveness of simulation is also opening new avenues for Ansys with the structuration of a developers ecosystems around the pyAnsys Framework: a community for python developers wanting to embed our true-physics solvers into their project/market specific applications for further adoption of engineering simulation.

More physics will continue to challenge our engineering minds and engineering simulation will continue to bring the necessary proof points and validation to enable more innovative products. As such, we are already deploying, with our most advanced users, simulation solutions for quantum physics, enabling what is believed to be the next revolution with quantum computing.



A cost-effective path to ASIC design

Application specific integrated circuits (ASICs) are microelectronic rock stars of unique functionality. Not even the sky limits ASICs; deep space probes routinely hoist II-VI and III-V engineering feats to the planets and beyond. But does ASIC design by nature require massive capital outlays? The experts at Swindon Silicon delve into the processes, pitfalls and promise of ASIC design along an easier yet effective pathway.

ELECTRONICS MANUFACTURERS turn to application-specific integrated circuits (ASICs) to optimise their products for higher volume production, reducing their size and hiding their circuit techniques from view. There is a common misconception that ASICs are unjustifiably expensive, or take prohibitively long to design. In reality, ASIC developers have tricks up their sleeves that can make an ASIC solution convenient and widely accessible, as explained by Dr Mike Coulson, Analogue Design Manager at mixed signal ASIC company Swindon Silicon Systems.

The role of an ASIC

An ASIC is a chip designed and optimised for a particular application. It combines numerous separate analogue and digital components into a single, compact package, allowing an electronic product to assume an otherwise impossibly small form factor. It allows the specifications of each

aspect to be rigorously optimised against cost, delivering differentiating performance whilst freeing the Bill of Materials (BoM) from over-specified off-the-shelf parts. It also hides any potentially novel circuit techniques from prying eyes: an ASIC is far more difficult to reverse-engineer than a printed circuit board (PCB) where the components are marked and wired together in plain sight.

Despite the potential benefits, many companies shy away from considering a bespoke ASIC due to the perceived investment and/or timescales required. They perhaps believe that bespoke means starting from scratch: a ground-up design of every aspect of the ASIC. There is a place for this in some designs, namely the highest volume parts where silicon area and fabrication costs must be absolutely minimised, and where the upfront investment is justified. But in all other cases, an experienced ASIC design company can employ various techniques to minimise non-recurring engineering (NRE) costs and hugely accelerate time to market.

Co-packaging off-the-shelf die

A typical ASIC project is to integrate the analogue and digital electronics of a customer's sensor or actuator product. When the product already exists as a prototype, or as a first production version, it will likely be built from off-the-shelf ICs. The analogue part is often quite custom, involving many separate chips and supporting passives (capacitors and resistors), while the digital aspects are often provided by an off-the-shelf microcontroller unit (MCU).

It is always wise to consider whether the MCU is being fully occupied, as standard parts are designed with versatility in mind, and are commonly over-specified for their ultimate role. But if the MCU is offering value for money, it may be possible to source the 'bare die' in a cost-effective fashion. This means purchasing the MCU chips before they are encapsulated in the black plastic 'packages' that we are used to seeing on the PCB. The bare MCU die can then be 'co-packaged' with any custom-designed die, so that they sit side-by-side or even on top of one another inside the custom package. The die are connected together internally, for example by microscopically thin bond-wires.

A key advantage of co-packaging is design scope minimisation — it allows the ASIC designer to focus on the unique aspects of the design, or those where cost can most readily be optimised. This is often the analogue componentry, due to the sheer number of discrete components it can involve. By narrowing the scope of the custom-designed die, the NRE and time to market can be significantly reduced, while returning the same improvements in form factor.

IP reuse

Swindon are well placed to employ another cost and time-saving technique, which is open to longer-established ASIC companies. This technique is intellectual property (IP) reuse. With 50 years' experience of delivering custom ICs, especially into automotive and industrial applications, there comes an abundance of acquired circuit block IP. Most of this IP is proven in the field, working right now in billions of chips and operating in some of the harshest imaginable environments. These ready-made circuit blocks can be deployed into a new project with few or no changes, and shortcut much of the design and verification time.

In addition to the circuit designs themselves, there is also less tangible yet highly valuable knowhow that an experienced team offers. For example, a design team that has specified and created numerous different analogue-to-digital convertors will quickly recognise the architecture most suited to a particular specification. This experience jump-starts the early design process, ensuring rapid progression from initial engagement to a costed ASIC proposition.

IP purchase

When in-house IP is not available, there is an alternative way to accelerate timescales and reduce NRE. Instead, designers can license IP blocks from specialist vendors and incorporate them onto the custom-designed silicon. This can work well for complex yet orthodox IP blocks — like radio transceivers supporting particular standards. IP obtained in this way can often be tweaked in-house, allowing it to meet customer-specific requirements. This kind of flexibility means that extremely complex systems can be monolithically integrated in far shorter timescales than when starting from scratch. This approach also brings with it peace of mind since licensed IP has also been exhaustively field tested through its use in many products across industries.

The ASIC design process

If you are wondering whether an ASIC might benefit your product, approach a reputable ASIC supplier

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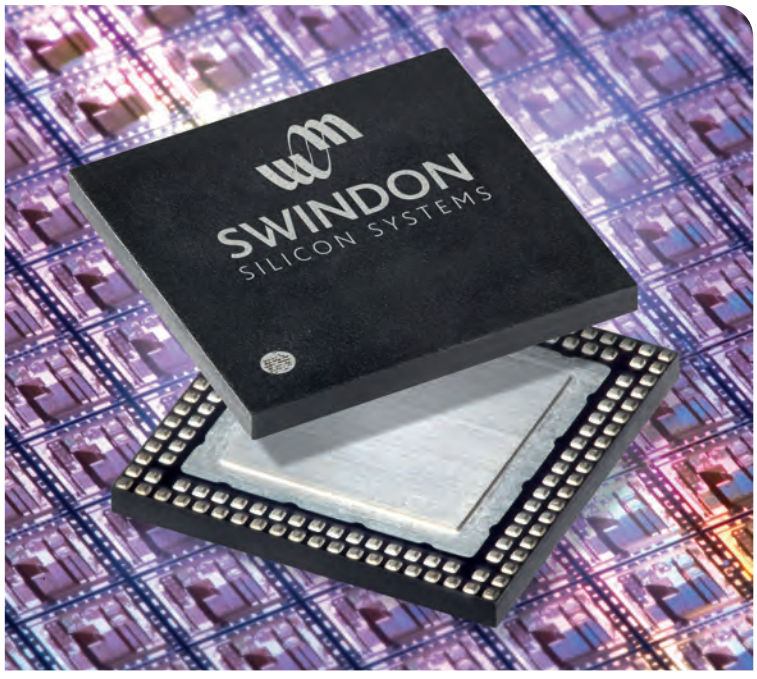

for advice. Companies serving these needs should have wide-ranging skills supporting every aspect of the circuit's design from concept through the prototype stage; the best consulting companies will be willing to work with their customers through initial production. Further, they should offer the ability to continue working with customers on subsequent design iterations, reusing circuit IP as needed to accelerate production cycles. When Swindon receives a new enquiry, company experts serve as consultants, working to understand customer ambitions and their wider system. This allows our experts to recommend the best partitioning of the system between the actual ASIC and external components, as well as the best partitioning of ASIC electronics. Swindon then produces a costed proposition before developing the ASIC's formal requirements that are based on customer input and Swindon's own expertise. Working from these requirements, an architecture is developed with individually-specified sub-blocks; the sub-blocks are passed to a team of designers for implementation. The timescale for developing an ASIC, from initial requirements to production-tested devices, will vary according to the complexity of the design. But in all cases it is essential to work with a full turnkey supplier, who can take responsibility for all aspects of the project, from initial consultancy, through packaging and qualification, to production test and supply.

A bespoke ASIC can secure the competitive edge for your product. An experienced supplier will provide an optimised solution for your application, and will know all the techniques to deliver your custom chip as rapidly and efficiently as possible. This allows them to ensure the greatest and soonest possible return on your investment.

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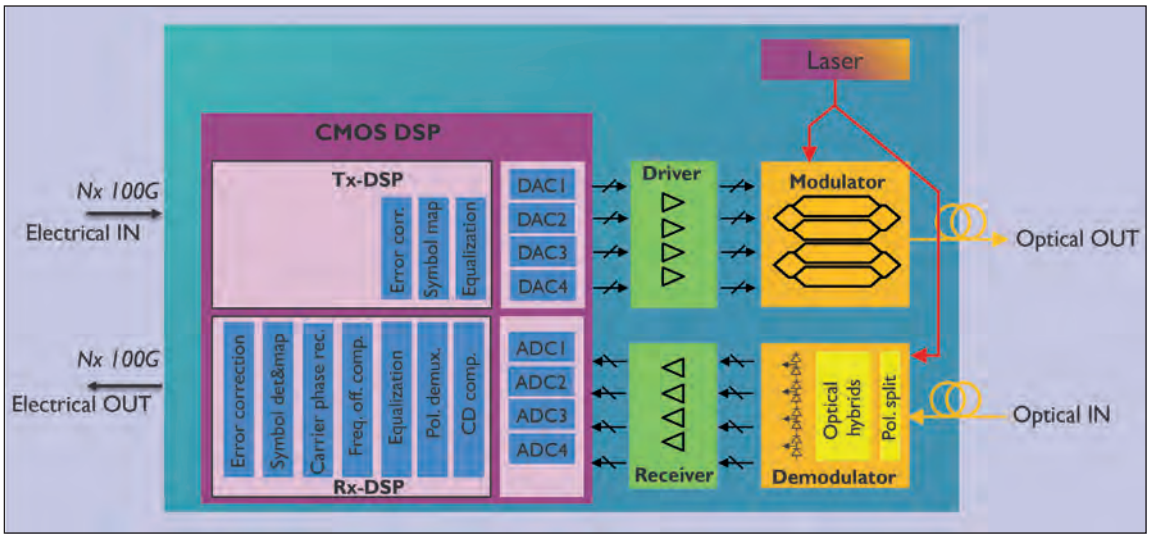
Design and integration of photonic and electronic integrated circuits for high-speed wireline transceivers

With the exploding data-rate needs of current and future digital applications, ever higher requirements are being set on the wireline transceivers for inter and intra data center traffic. The focus is on increasing the capacity of these optical transceivers, while simultaneously increasing the integration density and energy efficiency with each new generation. By Peter Ossieur, Program manager high-speed transceivers.

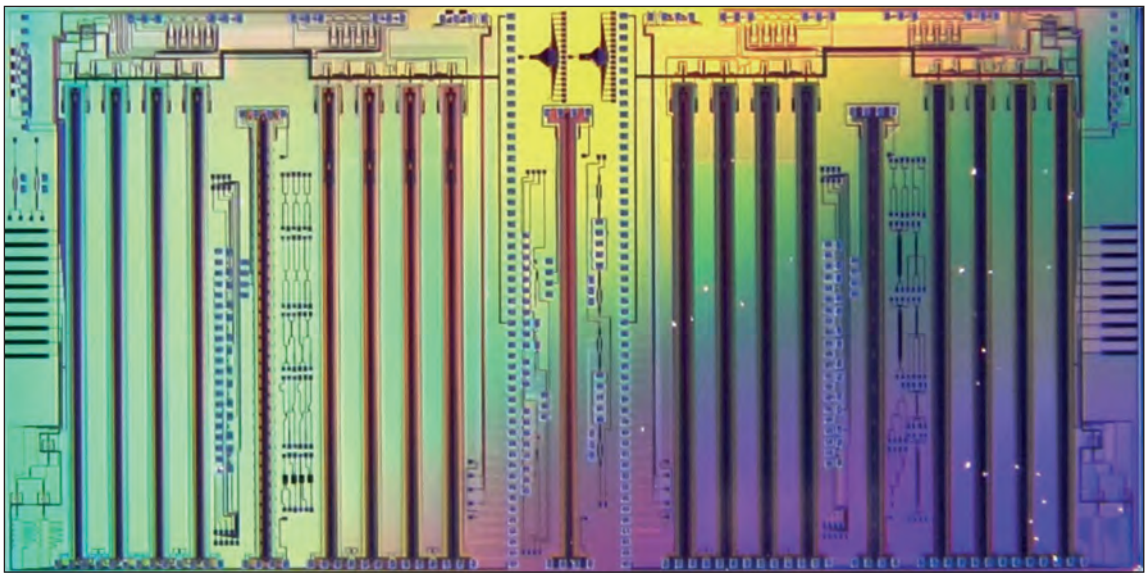
RESEARCHERS AT imec are taking on this double challenge by developing high-speed electronic and photonic integrated circuits for 100 to 130Gbaud transceivers, both for intensity-modulated direct-detect (IMDD) and for coherent optical transceivers. For a coherent transceiver, the specifications and functionality for the optics and electronics are much more demanding. The receiver DSP is also significantly more complex (compared to IMDD).

Scheme of an optoelectronic transceiver

For the optics, 100 to 130Gbaud operation requires at least 50 to 60GHz opto-electronic frontend bandwidth, both at the transmitter (modulator) and receiver (photodetector) side. Such bandwidths have been demonstrated with Indium Phosphate (InP)-based integrated optics, as well as with silicon photonics. Imec develops several silicon photonics platforms that include all the devices that are necessary for modulating and detecting optical signals. The same platform can also be used to realize passive devices such as silicon WDM filters and complex waveguide circuits. One component that until now was missing were electro-absorption modulators for the O-band. These are very compact



➤ Scheme of an optoelectronic transceiver



➤ Silicon Photonic transmitter and receiver test structures processed on iSiPP200

modulators that don't need any additional heater power unlike ring resonators. Relying on the quantum-confined stark effect, imec demonstrated such components, that could be modulated all the way up to 60Gb/s. Further work is ongoing to integrate these devices in the full platform.

To scale the bandwidth even higher e.g. towards 200Gbaud operation, compound semiconductors such as Indium Phosphate can be integrated onto Silicon photonic or Silicon Nitride wafers. Another alternative is Barium Titanate (BTO). This is a very promising electro-optic material that can push the performance of modulators even further. Imec is looking at integrating BTO-based modulators into its 200mm platform. An important focus is to adapt the BTO deposition techniques to volume scaling. Unlike other material systems such as LiNbO3, BTO can be brought into CMOS foundries, a critical advantage for manufacturing at scale.

In analog components such as drivers and receivers, electronics that can generate signals above 100Gbaud used to be the domain of compound semiconductors such as InP. Imec focusses on various circuit techniques to achieve these speeds using mainstream SiGe BiCMOS, which offers advantages in terms of the complexity of functionality that can be integrated and manufacturing throughput.

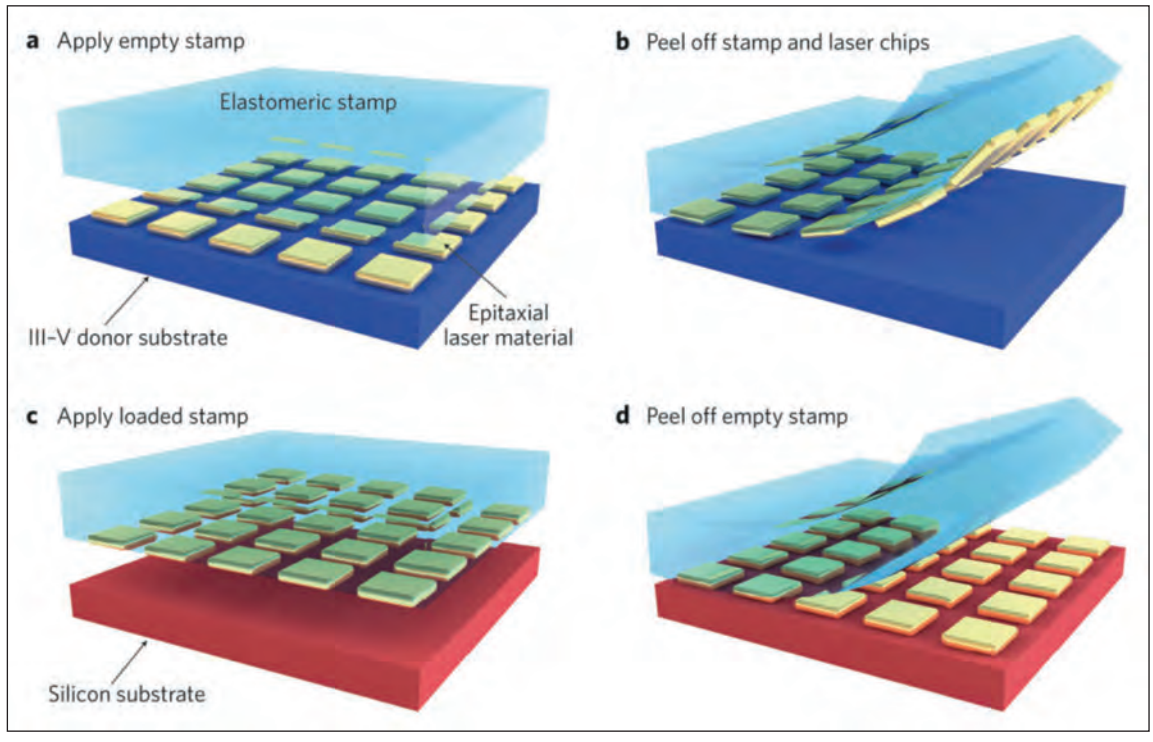
Silicon Photonic transmitter and receiver test structures processed on iSiPP200

As an example, imec researchers made a 4-channel linear Mach-Zehnder modulator driver array in which they used traveling wave amplifier circuits to achieve very high bandwidths (around 90GHz). It was codesigned with a silicon photonic dual-polarization, IQ modulator. Another example is a 4-channel linear transimpedance amplifier array, also using traveling wave amplifier techniques, and achieving bandwidths as high as 60GHz. The amplifier was codesigned with the balanced Ge photodetectors, integrated on the Silicon photonic platform.

Just as for the opto-electronic frontend, also for the DACs and ADCs at least 60GHz bandwidth is needed for 100 to 130Gbaud operation. Such ultra-high-speed ADCs and DACS can be realized using scaled CMOS such as 5- and 3nm. Next to the bandwidth, also a low power consumption and area are key. Imec is currently focussing on novel approaches for such high-speed wireline ADCs and DACs that overcome limitations in existing state-of-the-art. Designs of prototypes using 5nm CMOS are on-going to validate the new concepts in the lab.

On the receiver side, research towards energy-efficient 100Gbaud PAM-4 clock and data recovery circuitry compatible with the new ADC approach is on-going. Fractional oversampling is used in an effort to reduce the ADC sampling rate requirements. Feedforward and decision feedback equalization can be included to overcome impairments from the channel or bandwidth limitations on the optics.

To achieve the challenging specifications of next-generation high-speed transceivers, integration will obviously be key. This concerns both integration of chips and wafers from different material systems, each selected to provide optimum performance for the desired functionality, as well as integration to achieve the very high bandwidths necessary for beyond 100Gbaud operation. Heterogeneous integration is a key enabler to extend the functionality of imec's silicon platform to integrate e.g. optical amplifiers and lasers. In collaboration with Sivers Photonics and ASM AMICRA, imec demonstrated the use of ultra-high precision alignment flip-chip processes to integrate InP optical amplifiers and lasers on its Silicon Photonic wafers.



➤ Micro-transfer printing technique

The alignment accuracy was better than 500nm and resulted in beyond 10mW waveguide coupled basic power.

Micro-transfer printing is another approach to realize heterogeneous integration. It allows to integrate small components from almost any source material to almost any target substrate. It uses MEMS etch techniques to almost fully separate small chiplets from the donor substrate. Then, an elastomeric stamp with small posts is used to break the chiplets free from the donor substrate. Next, the stamp is used to deposit the chiplets onto the target substrate. Both of these operations require careful selection of the movement speed of the stamp. With this technique it is possible to deposit thousands of devices in a single step. In the H2020 Caladan project, this technique is further developed and used to realize GaAs quantum dot lasers and high-speed SiGe BiCMOS electronics.

Micro-transfer printing technique

Scaling far beyond 100Gbaud, e.g. towards 200Gbaud, may require innovative approaches beyond conventional transceivers, in which the functionality of electronics is shifted further into the optical domain. One example of such a device recently demonstrated by imec is an optical equalizer. This device can be understood by viewing a Mach-Zehnder modulator as an FIR (finite impulse response) or tapped delay line filter in the electrical input, optical phase output domain. The weight of each tap is related to the length (and drive voltage) of a particular section of the Mach-Zehnder modulator, while the FIR filter's delays correspond to delays from the optical waveguides.

Both of these can be readily manipulated: for example introducing a broadband time delay can be easily realized using a piece of optical waveguide. Even sign inversion (to realize more complex filter responses) is possibly using waveguide crossings. This approach can be used to trade for example drive voltage of the modulator for improved bandwidth or can be tailored to introduce particular peaking in the electro-optic frequency response.

ABOUT THE AUTHOR

PETER OSSIEUR received an M.Sc. Engineering degree in applied electronics and a Ph.D. in electrical engineering from Ghent University, Belgium, in 2000 and 2005, respectively. From 2005 to 2008, he was a Postdoctoral Fellow of the Fund of Scientific Research, Ghent University. During that time, his research was focused on 10Gbit/s burst-mode receivers and optoelectronics for automotive applications. In 2008, he became a part-time Professor of High-Frequency Electronics at the Faculty of Engineering, Ghent University.

In 2009, he joined the Photonic Systems Group, Tyndall National Institute and the Department of Physics, University College Cork, Cork, Ireland, where he became Senior Staff Researcher in April 2013. In this position he established an IC design group focusing on opto-electronic applications. In October 2017 he joined IDLab, an imec research group at Ghent Unviersity, as Senior Researcher and is currently Program Manager High-Speed Transceivers. He leads research activity focused on the development of high-speed analog and mixed-signal integrated circuits for photonic applications. He has (co-) authored 120 peer-reviewed papers, and holds several patents in the aforementioned research areas.

Contamination management solutions from Pfeiffer Vacuum

Pfeiffer Vacuum's many years of experience as a provider of vacuum technology have shaped our know-how and understanding of the processes, equipment and environment of production systems. Based on this knowledge, we have developed solutions to identify and minimize contamination and increase the yield at each step of the process.

SOLUTIONS for contamination management from Pfeiffer Vacuum improve the yield in the individual process steps of sensitive devices production. Innovative solutions from Pfeiffer Vacuum In-order-to-ensure the quality and a high yield in production, knowledge about the contaminants in the packaging of devices and their direct environment is important.

In the semiconductor industry, continuous analysis within the process cycle is possible with the APA 302. The fully automated process of the ADPC 302 localizes and counts particles on the inner surfaces of transportation carriers. The APR 4300 even goes a step further. The AMPC is the ideal solution for clean room and equipment front end modules monitoring (EFEM).

APA 302 - Pod Analyzer

The APA 302 is a unique in-line monitoring tool for advanced chip manufacturing in a clean room environment. This innovative equipment measures the airborne molecular contamination (AMC) in a FOUP and in the surrounding environment. The measurement occurs in real-time with a high sensitivity in the ppbv-range.

ADPC 302 - Dry Particle Counter

The ADPC 302 is a unique in-process contamination management system for particle contamination monitoring in the semiconductor industry.

Efficient particle monitoring

The ADPC 302 measures the number of particles in wafer transport carriers (Front Opening Unified Pod, FOUP, and Front Opening Shipping Box, FOSB).

The fully automated patented process localizes and counts particles from the carrier surfaces, including the door. Qualified by leading fabs, this system can be used for both the serial production as well as R&D analysis. The main applications are the carrier characterization, cleaning strategy optimization and cleaning quality check.

Advantages

The dry process (Dry Particle Counter) of the ADPC shows clear benefits compared to the traditional wet method (Liquid Particle Counter). The main advantage of the dry process is that the particle measurement is completely automated. It is integrated in the production process and therefore does not require time outside the production period. The fully automated measurement process does not require an additional operator. The test time is only seven minutes, meaning that the ADPC 302 is four times as fast as traditional systems. It is possible to test eight transport boxes in one hour.

APR 4300 - Pod Regenerator

The APR is a system for the decontamination of wafers and the protection during queue time.

➤ The Pod Analyzer APA 302 is a unique in-line monitoring tool for advanced chip manufacturing in a clean room environment.

Airborne Molecular Contamination (AMC) lowers the yield and quality in the semiconductor production. The APR effectively prevents the adsorption of contaminated organic or inorganic molecules on the surface of a wafer and the transport box. Through the evacuation of chambers in the APR, the adsorption probability is reduced dramatically. The yield of a fab can be increased significantly in this way and the queue times between the individual process steps can be optimized.

AMPC - Ambient Multi Port Controlling

Airborne molecular contamination (AMC) in IC fabs is known as the major factor of yield loss. To control and understand where contamination comes from, Pfeiffer Vacuum offers a unique solution to the semiconductor market to monitor clean rooms as well as EFEM (Equipment Front End Module).

Customer benefits

- Real-time compound measurement (acids, bases, organic compounds)
- Innovative software to manage sampling lines priority, quality check (QC) and alarms
- 96 samplings lines gathered onto one tool (up to eight analyzers)
- High throughput (analyzing and cleaning within three minutes)
- No cross-contamination from one sampling line to another

Systems for contamination management are our newest developments, specifically for the semiconductor and pharmaceutical industry.

How does contamination occur?

In the semiconductor industry, wafers emit reaction by-products during transport and waiting times. Moisture and molecular contaminants borne by air currents (Airborne Molecular Contamination, in short AMC), such as hydrogen fluoride (HF) react in the tight interstices of the transport boxes (pod systems) with oxidants from the ambient air (H_2O and O_2). During these reactions, undesired crystal growth on structured wafers is triggered which leads to a decline in quality and a decreased production yield.
Sub-micrometer particles can cause defects that may lead to considerable yield loss. Even the smallest particles measuring 0.1 µm may damage the structure of semiconductor chips.

The APR 4300 decontaminates 300 mm wafers and their transport boxes (FOUPs) on a molecular level and protects them during queue time. Reliable decontamination and protection from contamination

How does APR work?

The FOUP can be delivered either manually or through overhead hoist transportation (OHT) on the two load ports. The APR is a system with four stacked vacuum chambers for the decontamination of wafers and FOUPs, which is served from a reliable robot. All chambers are equipped with a vacuum pumping station, a gas box, an operating panel and a control with power supply. The chambers can be operated individually. After loading the chamber with a FOUP containing wafers, the pressure in the chamber is reduced to 0.1 mbar. Then the decontamination process is applied. After this, the chamber is purged with clean nitrogen and returned to atmospheric pressure. The wafers and the transport box are now protected from contamination for more than one day.

The AMPC is the ideal solution for clean room and equipment front end modules monitoring (EFEM).

The AMPC gathers the most advanced analyzers to detect and quantify acids, bases and organic compounds in up to 96 locations in a fab due to an innovative and integrated valves design. AMPC range includes two tools: AMPC S and AMPC L where external dimensions, number of lines and options are different. Additionally, the AMPC Extension Frame provides 39 U of space for extra analyzers. It can be used for upgrades of existing AMPC units or added to new AMPC S and AMPC L units.

Data management and fab communication

The tool software allows the end users to set various alarms when the levels of contamination exceed defined thresholds. All measurement results and tool parameters are stored in a database that can be transmitted to fabs' communication protocols to provide customers with a real-time picture of the fab's contamination levels. The customer is also able to remotely access the tool to modify tool parameters if necessary.

➤ The Dry Particle Counter ADPC 302 is a unique in-process contamination management system for particle contamination monitoring in the semiconductor industry.

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