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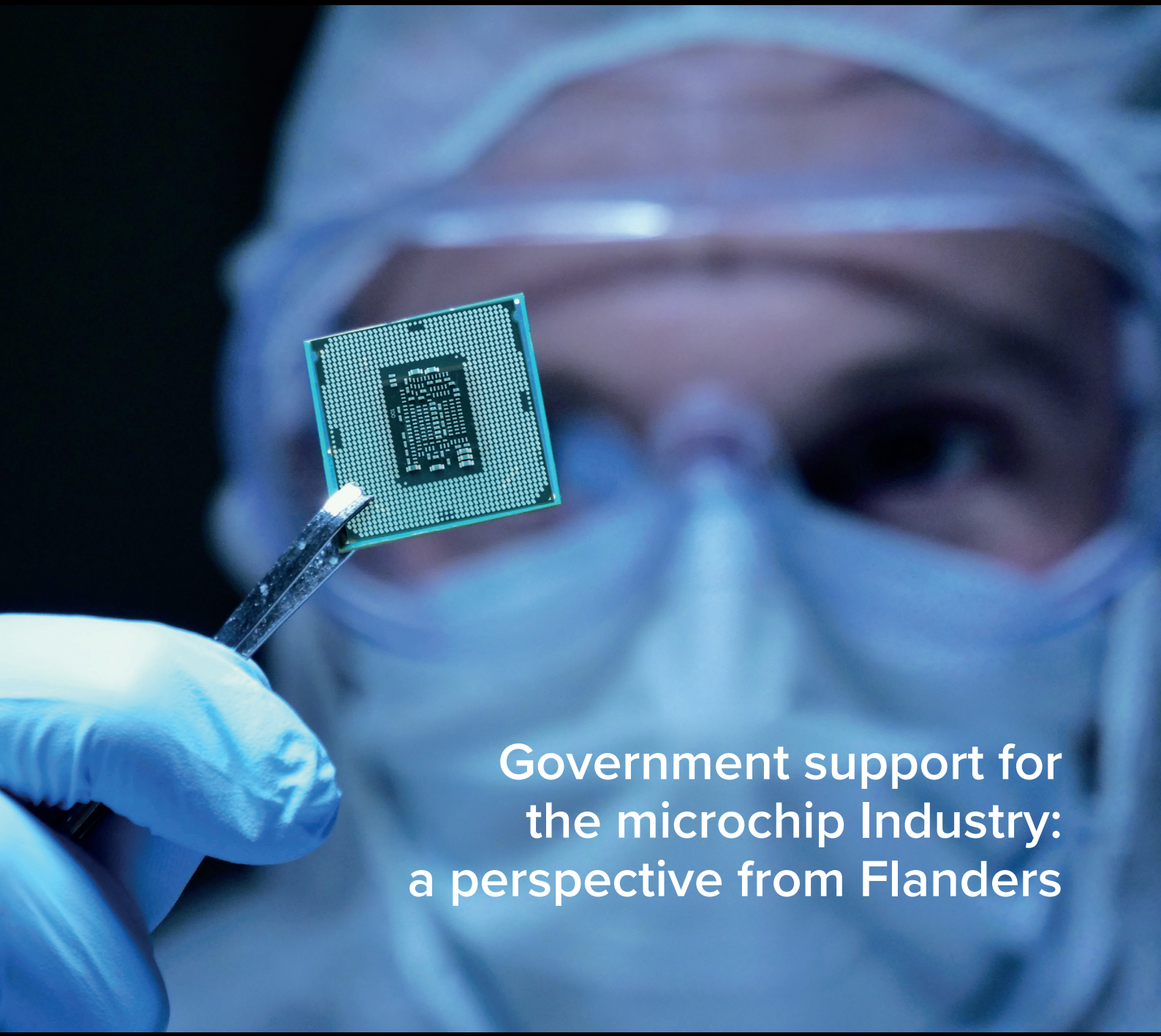

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VIEWPOINT

By Phil Alsop, Editor

Short term pain, long term gain?

FOLLOWING ON from the optimism contained within the KPMG LLP and Global Semiconductor Alliance 19th annual global semiconductor industry survey, which I commented on in the last issue, we have a slightly less cheerful market assessment, courtesy of Gartner, which predicts an 11% decline in worldwide semiconductor revenue this year. In actual figures, this means that 2022's virtually $600 billion USD total will shrink to $532 billion in 2023. However, according to Gartner, 2024 promises to be quite some year revenue-wise, with a predicted 18.5% rise to a high of $630.9 billion.

The cause of this revenue volatility? Chip over-supply resulting in price declines and, as Gartner puts it: "The past decades of high volume, high-dollar content market drivers are coming to an end, notably in the PC, tablet and smartphone markets where technology innovation is lacking."

Oh, and there's the small issue of techno nationalism to be addressed. Most obviously, this is manifested in the ongoing tension between China and the US, but plenty of countries (and the whole EU region) across the globe have decided that the business of semiconductors (and many other key manufacturing activities) is too important to be outsourced, hence the current major onshoring focus.

Whether or not the semiconductor supply chain is quite so enamoured of the geopolitics which puts pressure on who they can or cannot supply or what technology they may or may not supply, is less certain. After all, individual and even company to company relations tend to exist beneath the nationalist radar.

On the plus side, the need for the semiconductor supply chain to be much more flexible and responsive to changing market conditions means that, come 2024, it should be in a good place to meet what Gartner believes will be the twin positives of revenue recovery in the memory sector and growth in a whole range of smaller (compared to the PC, tablet and smartphone one) end markets. These include the automotive, industrial, IoT and military and aerospace sectors. No mention is made of the quantum computing opportunity, but one presumes that this will begin to make an impact over the next few years.

Richard Gordon, Practice Vice President at Gartner, concludes: "End-market demand will be less exposed to consumer discretionary spending and more exposed to business capital spending. Supply chains will be more complex with many more intermediaries involved and varied channels to market, and to satisfy different end-market requirements, different types of capacity will be required."

In the same way that a small, but significant, pandemic silver lining was the way in which many businesses accelerated their digital transformation journeys, and the flexible, hybrid workplace became a reality (and a benefit) for many, so it just might be that the current semiconductor industry volatility and uncertainty leads to the emergence of a leaner, fitter, more flexible sector over the next few years.

I'll leave you with my favourite quote:
"In Italy for thirty years under the Borgias, they had warfare, terror, murder, and bloodshed, but they produced Michelangelo, Leonardo da Vinci, and the Renaissance. In Switzerland, they had brotherly love, they had five hundred years of democracy and peace, and what did that produce? The cuckoo clock."

(To be fair to the Swiss, they also produced a banking industry of some note!).

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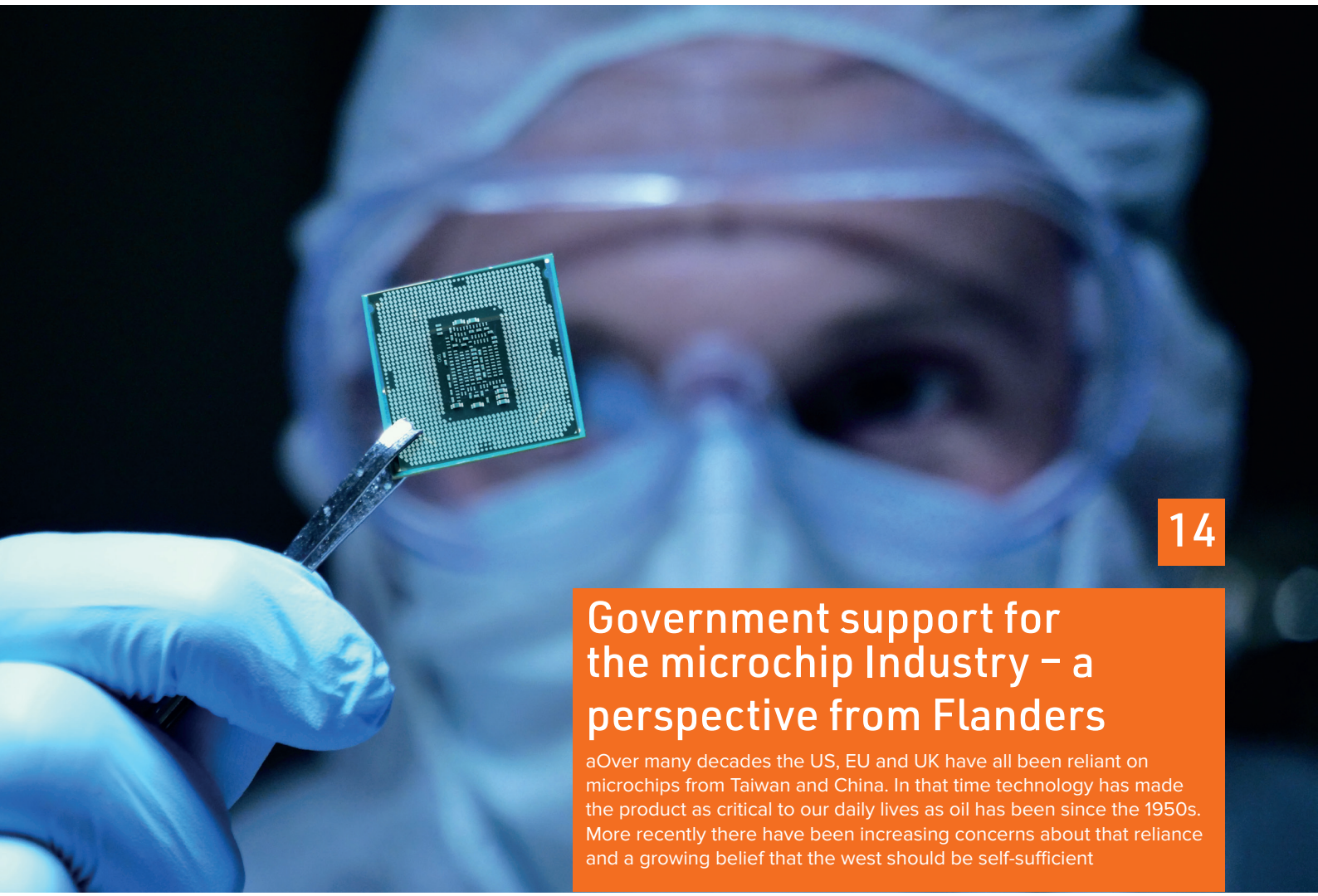

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Hybrid approach best for chip innovation?

A ground-breaking Lam study featured in the journal Nature proves a human-machine hybrid model can cut the cost of process development by 50 percent and accelerate time-to-market

IN A NEW STUDY, Lam Research Corp. examined the potential for the use of artificial intelligence (AI) in process development for chip fabrication, today a human-driven step that is essential for the mass production of every new advanced semiconductor in the world.

As the semiconductor market progresses towards $1 trillion in annual revenue by 20301 according to experts, the study, recently published in the journal Nature, identifies an opportunity to address two grand challenges facing the industry: reducing development costs and accelerating the pace of innovation to meet the increasing demand for next-generation chips. The study found that a "human first, computer last" approach can reach process engineering targets dramatically faster and at half the cost compared to today's approach.

"New approaches in innovation are needed to enable the industry to scale fast enough to meet the data-driven world's evolving demand for next-generation chips," said Tim Archer, president and chief executive officer at Lam Research. "The opportunity for greater collaboration between talented engineers and machines in process engineering highlighted in Lam's study in Nature is a potential game-changer for our customers and our industry at large. This research is a testament to Lam's more than 40-year heritage of industry leadership and semiconductor manufacturing innovation. I congratulate the Lam team on this exciting work."

The rising complexity of next-generation chips continues to drive process development to be more challenging and expensive. Seeking a more efficient approach, researchers at Lam put talented process engineers head-to-head against AI-enabled computer algorithms in the study. To manufacture every chip or transistor designed, experienced and skilled engineers must first create a

specialized recipe that outlines the specific parameters and permutations needed for each process step.

Hundreds of steps are required to build these nanometer-sized devices on a silicon wafer. Process steps typically include multiple instances of depositing thin layers of materials onto silicon wafers and etching away excess material with atomic-scale precision. This essential phase of semiconductor development is currently done by human engineers, largely using their intuition and a "trial and error" approach. With every recipe unique to the chip design and more than 100 trillion possible options to incorporate, process development can be laborious, time-intensive, and costly – increasingly slowing down the time needed to achieve the next technology breakthrough.

In the Lam study, machine and human participants competed to create a targeted process development recipe at the lowest cost, weighing a variety of factors associated with test batches, metrology and overhead expenses. The study concluded that while humans excelled in solving challenging and out-of-the-box problems, a hybrid human first, computer last strategy can help address the tedious aspects of process development and, ultimately, speed up process engineering innovation.

"Although critical to the creation of each and every chip produced, the plasma physics of process engineering has been for decades rooted in the same scientific approach that Thomas Edison used: trial and error," said Rick Gottscho, executive vice president and strategic advisor to the CEO – Innovation Ecosystem at Lam Research and co-author of the study. "Our research showed that while engineering talent remains essential to innovation, process engineering costs can be reduced by 50 percent by integrating AI at the right stage and with the right data. The study provides a prescriptive approach for bringing together the best of human-led engineering and the best of what data science and machines offer to create a combination that performs better than either one alone. If realized, this hybrid approach can lead to significant savings in both dollars and engineering time for the industry."

Lam is currently incorporating the key learnings from the study into its development operations. The Lam study provides initial guidance on how to successfully integrate human knowledge, skill and experience with AI's ability to rapidly assess numerous possible combinations in process engineering.

Gordon Moore, Intel Co-Founder, dies at 94

Moore, who set the course for the future of the semiconductor industry, devoted his later years to philanthropy

INTEL and the Gordon and Betty Moore Foundation have announced that company co-founder Gordon Moore has passed away at the age of 94.
The foundation reported he died peacefully on Friday, March 24, 2023, surrounded by family at his home in Hawaii.

Moore and his longtime colleague Robert Noyce founded Intel in July 1968. Moore initially served as executive vice president until 1975, when he became president. In 1979, Moore was named chairman of the board and chief executive officer, posts he held until 1987, when he gave up the CEO position and continued as chairman. In 1997, Moore became chairman emeritus, stepping down in 2006.

During his lifetime, Moore also dedicated his focus and energy to philanthropy, particularly environmental conservation, science and patient care improvements. Along with his wife of 72 years, he established the Gordon and Betty Moore Foundation, which has donated more than $5.1 billion to charitable causes since its founding in 2000.

“Those of us who have met and worked with Gordon will forever be inspired by his wisdom, humility and generosity,” reflected foundation president Harvey Fineberg. “Though he never aspired to be a household name, Gordon’s vision and his life’s work enabled the phenomenal innovation and technological developments that shape our everyday lives. Yet those historic achievements are only part of his legacy. His and Betty’s generosity as philanthropists will shape the world for generations to come.”

Pat Gelsinger, Intel CEO, said, “Gordon Moore defined the technology industry through his insight and vision. He was instrumental in revealing the power of transistors, and inspired technologists

and entrepreneurs across the decades. We at Intel remain inspired by Moore’s Law, and intend to pursue it until the periodic table is exhausted. Gordon’s vision lives on as our true north as we use the power of technology to improve the lives of every person on Earth. My career and much of my life took shape within the possibilities fueled by Gordon’s leadership at the helm of Intel, and I am humbled by the honor and responsibility to carry his legacy forward.”

Frank D. Yeary, chairman of Intel’s board of directors, said, “Gordon was a brilliant scientist and one of America’s leading entrepreneurs and business leaders. It is impossible to imagine the world we live in today, with computing so essential to our lives, without the contributions of Gordon Moore. He will always be an inspiration to our Intel family and his thinking at the core of our innovation culture.”

Andy Bryant, former chairman of Intel’s board of directors, said, “I will remember Gordon as a brilliant scientist, a straight-talker and an astute businessperson who sought to make the world better and always do the right thing. It was a privilege to know him, and I am grateful that his legacy lives on in the culture of the company he helped to create.”

Prior to establishing Intel, Moore and Noyce participated in the founding of Fairchild Semiconductor, where they played central roles in the first commercial production of diffused silicon transistors and later the world’s first commercially viable integrated circuits.

The two had previously worked together under William Shockley, the co-inventor of the transistor and founder of Shockley Semiconductor, which was the first semiconductor company established in what would become Silicon Valley. Upon striking out on their own, Moore and Noyce hired future Intel CEO Andy Grove as the third employee, and the three of them built Intel into one of the world’s great companies. Together they became known as the “Intel Trinity,” and their legacy continues today.

In addition to Moore’s seminal role in founding two of the world’s pioneering technology companies, he famously forecast in 1965 that the number of transistors on an integrated circuit would double every year – a prediction that came to be known as Moore’s Law. “All I was trying to do was get that message across, that by putting more and more stuff on a chip we were going to make all electronics cheaper,” Moore said in a 2008 interview.

With his 1965 prediction proven correct, in 1975 Moore revised his estimate to the doubling of transistors on an integrated circuit every two years for the next 10 years. Regardless, the idea of chip technology growing at an exponential rate, continually making electronics faster, smaller and cheaper, became the driving force behind the semiconductor industry and paved the way for the ubiquitous use of chips in millions of everyday products.

Top 10 foundry revenue falls by 4.7%

According to TrendForce's latest survey of the global foundry market, electronics brands began adjusting their inventories in 2Q22, but foundries were unable to rapidly adapt to this development because they reside in the more upper portion of the supply chain

MOREOVER, revising procurement quantities of long-term foundry contracts takes time as well. Hence, only some tier-2 and -3 foundries were able to immediately respond to the changes in their clients' demand. Also, among them, 8-inch wafer foundries made a more pronounced reduction in their capacity utilization rates.

As for the remaining foundries, the downward corrections that they made to their capacity utilization rates did not become noticeable until 4Q22. Hence, in 4Q22, the quarterly total revenue of the global top 10 foundries registered a QoQ decline for the first time after 13 consecutive quarters of positive growth. The quarterly total revenue of the top 10 foundries came to US$33,530 million, reflecting a drop of 4.7% from 3Q22. Moving into 1Q23, TrendForce projects that the quarterly total revenue of the top 10 will show an even steeper drop on account of seasonality and the uncertain macroeconomic situation.

Although TSMC and GlobalFoundries actually managed to raise revenue market share in 4q22, top five foundries all inevitably faced massive reduction in orders.

In 4Q22, foundries' revenues were affected by an underwhelming peak season and their customers' inventory corrections. Even with stock-up activities related to new iPhones and Android smartphones, TSMC still posted a QoQ drop of 1.0% in revenue to reach US$19,962 million. However, TSMC's revenue market share climbed to almost 60% mainly because tier-2 and -3 foundries took a heavier hit with respect to customers' inventory corrections. Competitors' weaker performances thus allowed TSMC to gain market share. Regarding the revenues from TSMC's process technologies, the decline in the revenues from the 7/6nm nodes was mostly offset by the rise in the revenues from the 5/4nm nodes. The share of the ≤7nm nodes in TSMC's overall revenue remained stable at 54%.

Turning to Samsung, it experienced a drop in orders for advanced processes and a general demand contraction as its customers were concentrating on inventory reduction. However, the demand drop associated with these factors was marginally offset by stock-up activities related to the components for the new iPhones and Android smartphones. All in all, Samsung posted a QoQ drop of 3.5% in foundry revenue to reach US$5,391 million for 4Q22. TrendForce also points out that Samsung has lost a significant amount of demand for its ≤7nm nodes as Qualcomm and NVIDIA made the decision to reallocate orders for chips used in flagship hardware products.

Currently, there are no new major customers that can effectively address the idling production capacity caused by the order reallocation. Therefore, the utilization rates of Samsung's advanced processes are projected to remain at a low level of around 60% through 2023. In sum, Samsung lacks the momentum to achieve a positive YoY revenue growth for this year.

Regarding other the major foundries, UMC saw a drop in both capacity utilization rate and wafer shipments in 4Q22, so its revenue fell by 12.7% QoQ to US$2,165 million. In the aspect of wafer size and process technology, UMC saw a QoQ revenue decline for both 12- and 8-inch wafer foundry services, and its 0.35/0.25μm nodes had the worse revenue performance with a QoQ decline coming to 47%. Conversely, in the case of GlobalFoundries, its revenue actually rose by 1.3% QoQ to US$2,101 million thanks to the optimization in its ASP and product mixes, as well as an increase in revenue from its non-wafer business. GlobalFoundries was the only one among the top 10 to record a positive QoQ growth, and its revenue market share also climbed to 6.2%. Turning to SMIC, it also saw a drop in both wafer shipments and wafer ASP. As a result, its revenue slid by 15.0% QoQ to US$1,621 million. Looking at SMIC's revenue by application or production category, the sharpest drops were experienced by chips related to smart home and consumer electronics. To get its customers to raise wafer input, SMIC has been offering price concessions.

However, this aggressive pricing strategy has not been particularly effective as customers are concerned about the risks associated with the US-China trade dispute. Therefore, SMIC's capacity utilization rate and revenue are expected to shrink further in 1Q23.

TrendForce notes that the extent of the impact from order cuts varied for individual foundries in 4Q22. Consequently, there were two notable changes in the quarterly revenue ranking from sixth to 10th place. First, Nexchip fell out of the top 10 group and will unlikely return in the short term. DB Hitek filled in the 10th place vacated by Nexchip in 4Q22. However, its capacity utilization rate dropped to 80-85% due to the recent market downturn. DB Hitek posted a QoQ drop of around 12.4% in revenue to reach US$292 million. Second, Tower, which was in ninth place in the 3Q22 ranking, benefited from the stable demand for chips based on specialty process technologies and a relatively steady flow of orders from European clients during 4Q22.

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UMC circular economy & recycling innovation center breaks ground

The first R&D center for waste recycling in the Southern Taiwan Science Park

UNITED MICROELECTRONICS CORPORATION recently held a groundbreaking ceremony for its Circular Economy & Recycling Innovation Center, which will be established at its Fab 12A in Tainan, Taiwan.

The NT$1.8 billion (US$58.8 million) facility will be the first waste recycling R&D center in the Southern Taiwan Science Park, serving as an important contributor for sustainable circular economy in Taiwan. After the center begins operating in 2025, it is expected to reduce 15,000 metric tons of semiconductor manufacturing waste annually.

"UMC has invested in Taiwan for more than four decades, including in our flagship Fab 12A, the manufacturing and R&D hub for our specialty process technologies. While we have continued to pursue capacity expansions and enhance our R&D capabilities, UMC is also deeply committed to our corporate sustainability goals. The Circular Economy & Recycling Innovation Center will serve as the center of our efforts to maximize resource recovery and minimize waste," said SC Chien, UMC's Co-President and Chief Sustainability Officer. "Working hand in hand with our value chain partners, we believe we can raise the bar for circularity in Taiwan, and enhance our industry's competitiveness through sustainable practices."

In the first phase, UMC's Circular Economy & Recycling Innovation Center will process waste produced during IC manufacturing processes into products that can be reused or sold, such as turning liquid waste and sludge into industrial-grade products. As for waste solvents that cannot be purified, the thermal cracking process will be applied to produce fuel gas to be reused within the facility. In the second phase, the Center will further develop thermal cracking technology that can directly convert waste solvents and plastics into energy supply.

Once operational, the facility is expected to reduce waste from UMC's Taiwan fabs by one-third, and create around NT$100 million worth of value-added products.

UMC has invested in a number of circular economy initiatives over the years, such as decreasing outsourced waste disposal by promoting resource reuse within its fabs.

Estimated to lower carbon emissions by around 5,000 tons per year, this program reduces the need for waste transportation and raw material mining, while also mitigating the risks of transporting waste to external facilities.

In addition, Fab 12A has introduced an electrolysis process to convert copper sulfate liquid waste into copper tubes with re-sale value, expected to generate more than NT$13 million of revenue per year. Anther initiative in progress is the recycling of used photomasks, which are cleaned on-site to remove patterning and resold as quartz substrates for optical products.

With a total floor area of around 9,000 square meters, the Circular Economy & Recycling Innovation Center is designed in compliance with green building codes, and will also act as an education center to promote circular economy and environmental protection to the young generation.

Using this center as a base, UMC will work closely with waste management service providers and raw material suppliers to develop innovative recycling methods and projects, contributing to a better, more sustainable future through collaborations together with value chain partners.

Signs of price stability and improved availability

Complexity, uncertainty, and unevenness persist, driving need for the power of intelligence

SUPPLYFRAME'S latest Commodity IQ insights reveal positive signs for a normalized supply-demand balance and reduced pricing and availability challenges as we advance into the new year. Excluding memory devices, 85% of semiconductor pricing dimensions will be stable and the remainder will move squarely in favor of buyers for the second half of 2023. But Supplyframe Commodity IQ indicates that extended lead times for semiconductors, including programmable logic devices and passive components like automotive-specific resistors, will continue into the second half of the year.

"New Commodity IQ insights, the resilience of world economies to inflation and threats of recession, and China's reopening economy in the second half suggest there is reason to be optimistic. Commodity IQ indicates that component availability has largely improved, and prices across many commodities and sub-commodities have stabilized," said Supplyframe CEO and founder Steve Flagg. "But electronic component lead times remain longer than historical norms. Component lead times are improving faster than prices as demand in some markets deteriorates. And in this age of macroeconomic uncertainty, where it is becoming increasingly difficult to forecast demand amid mixed end-market signals, further intensification of the Russia-Ukraine war, continuing COVID-19 challenges in China or any number of other disruptions could emerge."

Supplyframe Commodity IQ is a transformed approach to electronics supply chain sourcing and analysis that provides unique, predictive, and prescriptive intelligence for electronic components, systems, and associated commodities based on operational analytics. This always-on software-as-a-service solution from Supplyframe pairs expert analysis and context with global electronics design, demand, pricing, lead time, and inventory indices to help companies connect the dots.

For the first quarter of 2023, Commodity IQ forecasts indicate the global market will experience an 8% decline in the number of rising lead times and commodities with part allocations for active and passive components. According to the Commodity IQ Price Index for Q1, the number of component pricing dimensions will decrease by 14%. And global electronic component demand and sourcing activities quarter-on-quarter in the first quarter of this year are expected to be down by 2%, while engineering design will be off by 20% – further evidence of demand erosion.

While there are bloated inventories for components like memory and small case-size ceramic capacitors, automotive-grade microcontrollers, and FPGAs remain far below the Commodity IQ Inventory Index baseline. And analog integrated circuits (ICs), microcontrollers, and discrete ICs (especially power MOSFETs) will remain constrained and costly in the first quarter and beyond.

In the third quarter of 2023, global lead times for all electronic components will ebb dramatically as compared to the third quarter of 2022. Commodity IQ projects that nearly 60% of lead time dimensions will decrease in the third quarter versus 1% in the third quarter of 2022, with none expected to increase in the third quarter compared to a massive 73% in the same quarter of 2022. But Commodity IQ expects extended lead times to endure into the second half for semiconductors, including programmable logic devices and passive components like automotive-specific resistors.

Despite inventory reductions that will likely be complete by the end of the first half, IC orders, wafer starts, and capacity utilization will begin to rise and memory pricing will reach its bottom in the second half of this year. The company forecasts that DRAM prices will commence recovery in the third quarter, and NAND pricing will follow in the fourth quarter or early in 2024.

Following seasonal trends, global demand activities increased by 7% month-over-month in January, with all regions rising except Asia, which declined by 14% from December to January on general economic weakness and the Chinese Lunar Holiday. In the Europe/Middle East/Africa region, growth was driven by significant sourcing action increases in Germany (44%), France (37%), Italy (32%), Israel (15%), and the United Kingdom (55%). Month-over-month through January in these countries, transistors, including constrained IGBTs, rose sharply by 68%, microcontrollers and microprocessors climbed by 34%, capacitors expanded by 30%, and diodes were up by nearly 40%.

The Commodity IQ global electronic component demand forecast is for a weaker first half in 2023, compared to 2022, with Q1 anticipated to grow just 1% versus Q4 2022. Given automotive and industrial component order optimism and a resilient macroeconomic outlook, Supplyframe projects an overall demand rebound commencing in the second half of the year.

Industry hits record sales

Worldwide sales of semiconductor manufacturing equipment increased 5% from $102.6 billion in 2021 to an all-time record of $107.6 billion last year, SEMI has reported. The data is now available in the Worldwide Semiconductor Equipment Market Statistics (WWSEMS) Report.

FOR THE THIRD consecutive year, China remained the largest semiconductor equipment market in 2022 despite a 5% slowdown in the pace of investments in the region year over year, accounting for $28.3 billion in billings. Taiwan, the second-largest destination for equipment spending, recorded an increase of 8% to $26.8 billion, marking the fourth straight year of growth for the region. Equipment sales to Korea contracted 14% to $21.5 billion.

Annual semiconductor equipment investments in Europe surged 93%, while North America logged a 38% increase. Sales to the Rest of World and Japan increased 34% and 7% year over year, respectively.

"The record high for semiconductor manufacturing equipment sales in 2022 stems from the industry's drive to add the fab capacity required to support long-term growth and innovations in key end markets including high-performance computing and automotive," said Ajit Manocha, SEMI president and CEO. "Additionally, the results reflect investments and determination across regions to avoid future semiconductor supply chain constraints like those that surfaced during the pandemic."

Global sales of wafer processing equipment rose 8% in 2022, while other front-end segment billings grew 11%. After robust growth in 2021, assembly and packaging equipment sales decreased 19% last year while total test equipment billings contracted 4% year over year.

Compiled from data submitted by members of SEMI and the Semiconductor Equipment Association of Japan (SEAJ), the WWSEMS Report is a summary of the monthly billings figures for the global semiconductor equipment industry.

Fab equipment spending on track for 2024 recovery

Global fab equipment spending for front-end facilities is expected to decrease 22% year-over-year (YoY) to US$76 billion in 2023 from a record high of US$98 billion in 2022 before rising 21% YoY to US$92 billion in 2024 to reclaim lost ground, SEMI announced in its latest quarterly World Fab Forecast report.

The 2023 decline will stem from weakening chip demand and higher inventory of consumer and mobile devices. Next year's fab equipment spending recovery will be driven in part by the end of the semiconductor inventory correction in 2023 and strengthening demand for semiconductors in the high-performance computing (HPC) and automotive segments.

"This quarter's SEMI World Fab Forecast update offers our first look ahead to 2024, highlighting the steady global expansion of fab capacity to support future semiconductor industry growth driven by the automotive and computing segments and a host of emerging applications," said Ajit Manocha, SEMI president and CEO. "The report points to a healthy 21% uptick in equipment investment next year."

Taiwan is expected to retain the global lead in fab equipment spending in 2024 with US$24.9 billion in investments, a 4.2% YoY increase, followed by Korea at US$21 billion, a YoY 41.5% jump. While China is forecast to place third in equipment spending worldwide in 2024, U.S. export controls are expected to limit the region's spending to US$16 billion, comparable to the region's investments in 2023. The Americas is expected to remain the fourth largest region in spending with a record US$11 billion in investments in 2024, a 23.9% YoY increase. Europe & Mideast is also forecast to log record investments next year, increasing spending by 36% to US$8.2 billion. Fab equipment spending in Japan and Southeast Asia is expected to increase to US$7.0 billion and US$3.0 billion, respectively, in 2024.

Foundry Segment Continues to Lead Semiconductor Industry Expansion

Covering 2022 to 2024, the SEMI World Fab Forecast report shows the global semiconductor industry increasing capacity by 4.8% this year after a 7.2% rise in 2022. Capacity growth is expected to continue in 2024, rising 5.6%.

With more suppliers providing foundry services to increase global capacity, the foundry segment is expected to lead the semiconductor expansion in 2023 with US$43.4 billion in investments, a 12.1% YoY decline, and US$48.8 billion, a 12.4% increase, in 2024. Memory is forecast to place second in global spending in 2023 despite a 44.4% YoY decline to US$17.1 billion, with investments rising to US$28.2 billion next year.

Unlike other segments, analog and power will see a steady expansion with a forecast spending increase of 1.3% to US$9.7 billion in 2023 on the strength of stable growth in the automotive market. Investments by the segment are expected to remain flat next year.

The latest update of the SEMI World Fab Forecast report, published in March, lists 1,470 facilities and lines globally, including 142 volume facilities and lines with various probabilities that are expected to start production in 2023 or later.

Annual Billings by Region in Billions of U.S. Dollars with Year-Over-Year Change Rates

Region	2022	2021	% Change
China	28.27	29.62	-5%
Taiwan	26.82	24.94	8%
Korea	21.51	24.98	-14%
North America	10.48	7.61	38%
Japan	8.35	7.80	7%
Europe	6.28	3.25	93%
Rest of World	5.95	4.44	34%
Total	**107.64**	**102.64**	**5%**

Sources: SEMI (www.semi.org) and SEAJ (www.seaj.or.jp), April 2023

Note: Summed subtotals may not equal the total due to rounding.

SEMI wins skills funding

SEMI Europe, as the lead of a new 18-partner consortium, has won up to €4 million in funding to develop the European Chips Skills Academy, an initiative to help tackle the skills and talent shortages in Europe's electronics industry and propel its long-term growth.

The initiative is backed by more than 30 partner research organizations, vocational and education training providers, certification agencies and industry stakeholders.

The European Chips Skills Academy will expand on the Microelectronics Pact for Skills and the EU Chips Act to support the microelectronics ecosystem in Europe to attract new talent. The academy will deliver targeted European-wide training in key microelectronics fields such as automotive and additive manufacturing.

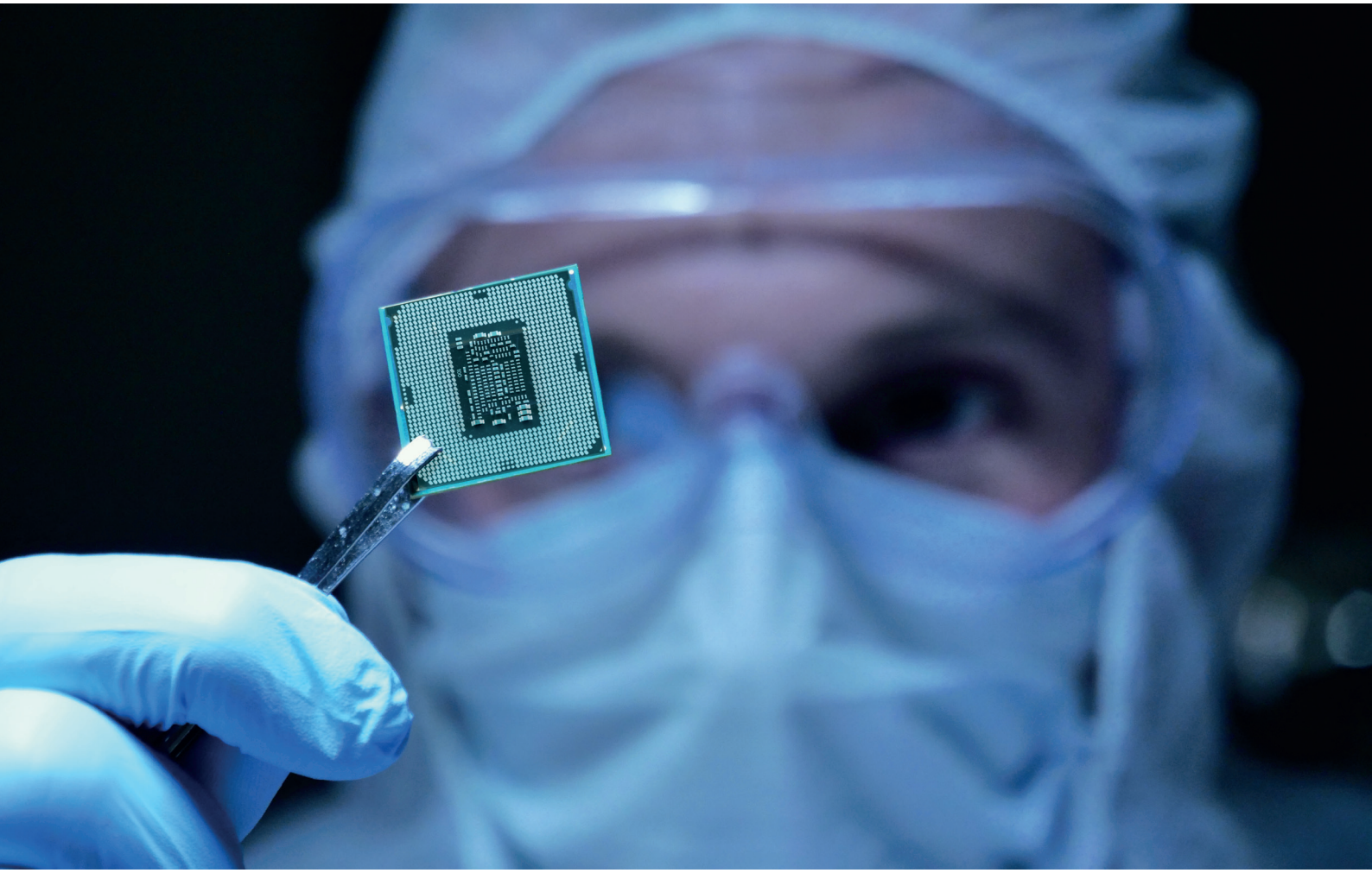
The grant, provided by the European Commission's Erasmus+ Programme, will fund the academy for four years. The European Chips Skills Academy is the second phase of the Microelectronics Training, Industry and Skills (METIS) consortium. Both initiatives are designed to foster microelectronics industry collaboration with key education, training and certification providers to address the skills shortage and European competitiveness.

"The pan-European alliance guiding the European Chips Skills Academy will leverage the diverse and considerable strengths of its many partners from across the microelectronics' ecosystem and industrial value chain," said Ajit Manocha, president and CEO of SEMI. "The project aims to bring greater strategic foresight to the evolution of professions and skills in the industry by applying evidence-based, data-driven success metrics to workforce development."

"Rapid semiconductor industry growth in Europe and around the globe in the years ahead necessitates that we quickly scale up the region's training efforts and drive greater cohesion of skills strategies across Europe to meet demand for the qualified workers required to sustain innovation and growth," said Laith Altimime, president of SEMI Europe. "The European Chips Skills Academy will be the first decentralized microelectronics skills provider in Europe to help overcome this critical workforce development challenge."

Expected to begin work in autumn 2023, the European Chips Skills Academy consortium consists of the following organizations:

- Asociación Nacional de Centros con Certificados de Profesionalidad (ANCCP) - Spain
- Association for European NanoElectronics Activities (AENEAS) - France
- Budapest University of Technology & Economics (BME) - Hungary
- DECISION Etudes & Conseil - France
- Dresden University of Technology (TU Dresden) - Germany
- Graz University of Technology (TU Graz) - Austria
- Infineon Technologies - Austria
- Information Centre on Academic Mobility and Equivalence (CIMEA) - Italy
- Innovazione Apprendimento Lavoro Friuli Venezia Giulia (IAL-FVG) - Italy
- Interuniversity Microelectronics Centre (imec) – Belgium
- Knolyx - Romania
- Melexis - Belgium
- Okmetic - Finland
- Platform Talent voor Technologie (PTVT) / European STEM coalition - Netherlands
- SEMI Europe - Germany
- Silicon Saxony - Germany
- Technical University of Ostrava (VSB) - Czechia
- Tyndall National Institute - Ireland.



Government support for the microchip industry – a perspective from Flanders

Over many decades the US, EU and UK have all been reliant on microchips from Taiwan and China. In that time technology has made the product as critical to our daily lives as oil has been since the 1950s. More recently there have been increasing concerns about that reliance and a growing belief that the west should be self-sufficient.

BY JAN WAUTERS, SCIENCE AND TECHNOLOGY COUNSELOR AT FLANDERS INVESTMENT & TRADE (AN OFFICIAL BODY OF THE GOVERNMENT OF FLANDERS).

IN RESPONSE, the U.S. and EU have announced multibillion-dollar packages aimed at boosting domestic chip production, but that's not happening in the UK. Many in the industry are pleading with the Government for subsidies amid fears that some chip firms will be forced to move overseas due to the innate lack of competitiveness of the UK industry. Do subsidies work? What is the long-term impact of subsidies? What other factors influence their success?

Flanders is a leading destination for the development of next-generation semiconductors. The region is home to three major strategic research centres and a further five research institutes with dedicated microelectronics, nanotech and semiconductors departments. The region is cultivating a vibrant ecosystem supporting semiconductor innovation. On the private innovation side, four semiconductor startups have raised six rounds of investment between them in the last 18 months.

This is underpinned by a substantial public budget for research and innovation. Of all EU member states, Belgium gives the highest net subsidies to support the business world in terms of innovation, employment and more. The Flemish government made an initial investment of €62m to help found Imec in 1984 and continues to support research centres to this day. Imec has since become a global leader in R&D, and in the translation of that innovation into industry. How has that happened? What has been the role of the public subsidies in this?

Background – The history

It is useful to first explain the context to how and why Flanders made the decisions they did. In the 1980s, Belgium introduced major constitutional reforms which gave Flanders, the northern region, far greater autonomy and with it the ability to promote itself as an industrial, entrepreneurial, and technological powerhouse.

The Flemish government took this opportunity to develop a clear vision, which became known as the 'DIRV' program or Third Industrial Revolution. The aim was for Flanders to be a pioneer in the European knowledge society and economy. A key part of the strategy was to boost the region's ability to innovate, develop its knowledge base and focus on its strengths. It made major strategic investments in a number of key sectors with a focus on renewal and re-enforcement of industrial ecosystems in new materials and micro-electronics.

One unique aspect of this is that, despite many changes of government in the last 40 years, the focus has never changed. The grants have been reviewed every five years, and each time the funding has been maintained. In 2022 the Government of Flanders committed to putting innovation at the centre of its strategy for recovery following the pandemic and allocated an additional €100 million from the recovery provision for companies' R&D projects. An additional €60 million from the recovery provision will be used to strengthen the research field and accelerate R&D.

R&D in Flanders – An overview

Gross domestic expenditure on R&D is comparatively high in Flanders. The equivalent of 3.3% of the region's GDP is invested in R&D (2019), which makes the region an outlier in the EU and a reputed knowledge hub in Europe.

In 1984, the University of Leuven (KU Leuven), wanted to launch a microelectronics research and development (R&D) 'superlab' in order to enter, what was then, a new chip-based industrial revolution. However, the funding required to pay for the advanced equipment needed was challenging for the university to manage alone. They needed significant investment. That came from the Flemish Government. In 1984, as part of their new vision, the Government made an initial investment of €62m to help found imec, as a spin-off from KU Leuven.

Imec brought R&D in advanced microelectronics technologies into one center, creating a central hub, where the level of investment needed for state-of-the-art cleanrooms could be concentrated.

Imec is now Europe's largest independent research and training centre and boasts highly-specialised expertise in microelectronics and nanotechnology for applications in the ICT, automotive, health, food and materials sectors – and beyond. Its nanotech R&D activities include:

- nano-CMOS and novel devices for nanoelectronics, micro- and nanoelectromechanical systems (MEMS and NEMS);
- nanomaterials and nanopatterning;
- nanoprobes, surface functionalization and self-assembly;
- molecular interconnects for molecular electronics and bioelectronic circuits.

120 unique spin-offs have been established from imec. A recent example is Azalea Vision, which has produced a smart artificial lens for the human eye. In addition to the creation of imec, we also have the Strategic Research Center for Life Sciences and Biotechnology (VIB), with headquarters in Ghent. VIB works closely with Flanders' universities to unite the strengths of various research teams into a single institute for life sciences and biotechnology. VIB and imec set up the Neuro-Electronics Convergence laboratory together. Located at imec, this unique R&D facility is home to multidisciplinary tools for:

- semiconductor processing;
- nanotechnologies;
- biosensor fabrication;
- cell culture;
- molecular biology;
- electrophysiology;
- and more.

Between 1984 and 1999, international technology fairs were organised by the newly established Flanders Technology. The aim of these fairs was to position Flanders as a national and international innovation hub. They promoted innovation, entrepreneurship and economic growth by supporting the development and commercialisation of new technologies. Flanders also has a minority stake in imec.xpand, the independently managed investment fund of approx. €117 million that takes participations in promising nanotech companies. The Flemish Government committed €30 million in capital to a second xpand fund.

The ecosystem

Flanders leveraged imec and maximized the economic development benefits coming from its research by creating an ecosystem that fosters collaboration between academia, industry, and government. This has been done through initiatives such as:

- **Spin-off companies:** imec has created numerous

spin-off companies that are commercialising the research and technology developed at the center. They have created a dynamic ecosystem in Leuven and Flanders together with universities (Leuven, Ghent, Antwerp and Hasselt) that thrives on talent, serial entrepreneurs, mentors, venture capitalists, etc.

- **Industry platform:** imec's model is largely based on joint R&D programmes, with the industry, that deliver new pre-competitive technologies to be used in future generations of semiconductor products. This joint collaboration model accelerates innovation, by pooling resources and alleviating the ever-increasing development costs of new technologies. Today, imec is one of the largest R&D industry platforms of its kind in the world.
- **Incubation and acceleration programmes:** Flanders established incubation and acceleration programs to support start-ups and young companies, leveraging the knowledge and technology generated by imec. E.g. Over the years, imec has created a fund, imec.xpand, to invest in spinoffs and other startups/scaleups to increase the fabric of high-tech in the region. It is based on imec's unique semiconductor expertise and infrastructure. The business accelerator imec.istart, another example, targets promising startups and supports them in their growth process.
- **Concentration of research infrastructure and talent:** The government has invested in research infrastructure and provided funding for imec's research programs, helping to create a supportive environment for innovation and entrepreneurship.
- **Attracting foreign direct investment:** Flanders Investment & Trade has been very successful in leveraging the reputation of the Flemish research centers, such as imec and VIB, and its world-leading universities, to attract foreign investment, particularly in the fields of nanoelectronics and life sciences. imec is a key partner for many foreign companies to develop new technologies.
- **Collaboration with universities:** Partnerships have been established between imec, universities and research centers, promoting collaboration between researchers and students and increasing the transfer of knowledge between academia and industry. imec has collaboration agreements with over 200 universities worldwide, and many more that involve non-formal collaborations through a network of scientists, engineers and PhD students. One of the legacies of this is that Universities in Flanders consistently score well in the international rankings: Thomson-Reuters has ranked KU Leuven as Europe's most innovative university several years in a row.

Beyond subsidies

Flanders has taken a comprehensive and integrated approach to creating a knowledge-based innovation ecosystem. However, government subsidies alone would not have delivered the results we've seen in Flanders. There are many other crucial factors that are key to the success. The top two are:

- **Tax incentives:** The Government of Flanders actively supports business innovation through R&D tax incentives. Flanders gives an 85% corporation tax saving on profits that are the result of a company's own innovations. This is one of the most advantageous in Europe. This allows companies to recover part of their innovation investments.
- Longstanding joint efforts by knowledge institutions, companies and governmental organizations. It is rare for successive governments to maintain the consistency of focus that has been experienced in Flanders. The European Innovation Scoreboard (EIS), released by the European Commission, ranks Flanders/Belgium among the 5 innovation leaders.

There are a number of unique factors that have substantially contributed to delivering the original vision, some within the control of policy makers and some are cultural. These include:

- The concentration - in a very small territory - of top scientists and engineers (both from Flanders and international companies) and R&D centers, and the availability of state-of-the-art infrastructure
- A focus on interdisciplinary research in sectors at the interface of new technologies, such as nanotech and biotech. There have been a number of cross-disciplinary initiatives, such as NERF (Neuro-Electronics Research Flanders), which is a collaboration between Imec, VIB and KU Leuven.
- An open and international mindset, written in our DNA.
- **Talent attraction and retention:** Flanders works hard to attract and retain talented individuals through programmes such as internships, research fellowships, and entrepreneurship support. This helps to build a pool of skilled professionals that can contribute to the growth of the innovation ecosystem.
- **Open innovation:** Flanders has adopted an "open innovation" approach, encouraging collaboration between different stakeholders and promoting the sharing of ideas and knowledge between businesses, academia, and government.
- **Focus on key industries:** The region has focused its efforts on key industries such as life sciences, clean technology, and microelectronics, helping to create a strong ecosystem in these areas and attract investment.
- **International partnerships:** Flanders has established partnerships with other regions and countries, promoting the exchange of knowledge and ideas and providing opportunities for collaboration on research projects and technology development.
- High levels of success in attracting foreign investment, led by Flanders Investment & Trade. This was partly due to factors such as proximity

to other markets and the strength of our transport infrastructure, including our world famous ports. Building on the success of foreign investments and exports, Flanders Investment & Trade substantially enlarged its foreign network with 10 Science & Technology Offices (New York, Palo Alto, Paris, London, Copenhagen, Munich, Mumbai, Singapore, Guangzhou and Tokyo), focussing on Digital Tech, Health Tech and/or Climate Tech).

- Extensive study work and analysis in place to boost the opportunities for growth in Flanders' technology niches.

The impact

Over the last 40 years, Flanders has become a global leader in R&D, and in the translation of that innovation into industry. Through its support of its strategic R&D centers such as Imec and VIB, the Government of Flanders ensures that the long-term IP needs of industry are met across the key sectors first identified in the 1980s.

Imec has become one of the world's most important independent electronics R&D centres. Thousands of world leading researchers are based there, and its pilot production line is home to around €4bn complex semiconductor-making equipment. Imec is at the centre of an ecosystem of companies that, over the years, have leveraged their partnership with the centre to develop world-leading technologies. They include ASML, the only company in the world that owns the technology to produce microchips out of silicon wafers. Their machines are used by every major advanced semiconductor producer.

Imec's business and financing model means that it is able to be a non-commercial, or neutral, provider of R&D services in the semiconductor industry which is recognised as intensely competitive.

Financial support from the Government of Flanders initially accounted for the majority of imec's budget. Today the annual government grant, though increased, accounts for less than 15% of its budget. Most of imec's income now comes from local and international contract research with industry. According to the most recent figures, companies, governmental organisations and knowledge institutions in Flanders collectively spent 3.60% of the region's GDP on R&D. This is more than any other region in Europe. FDI (secured by Flanders Investment & Trade) also plays a major role in enriching the ecosystem in Flanders. 1 in 4 new jobs created through FDI in 2022 is related to R&D. Government support has been crucial to the success of the original vision. Imec would not have been established without that support. And without imec Flanders would not have been able to establish itself in the way it has and delivered on its strategic objectives.

What next?

In October 2022, the Government of Flanders launched a new project and a promotional campaign called "Flanders Technology & Innovation". It was inspired by the success of "Flanders Technology". The initiative breathes new life into the concept of technology fairs, which are to be held in 2024. Through "Flanders Technology & Innovation", the region will present itself as a world leading technology laboratory.

In 2019 76% of R&D in Flanders was funded by the business enterprise sector (BERD of 2.40%). However, innovation efforts are still largely concentrated in certain industrial sectors and large companies. Industry does not typically invest in long-term foundation IP for pre-competitive enabling technologies. It is challenging to convince Finance Directors and shareholders of the benefits. Through its continued financial support of imec, the Government of Flanders ensures that the long-term IP needs of industry are met and it enables imec to:

- Carry out groundbreaking technology research in joint R&D programs with industrial partners and
- Keep its position as the world's most advanced independent nanoelectronics R&D platform for industry, with state-of-the art infrastructure.

Virtual fab focuses on real carbon footprint reductions

EMILY GALLAGHER, A PRINCIPAL MEMBER OF THE TECHNICAL STAFF AT IMEC, discusses with Philip Alsop, SiS Editor, the sustainability challenge facing the semiconductor industry and explains how imec's recently launched Virtual Fab is playing an important role in helping to improve both the understanding and development of environmentally friendly, patterning-related process solutions.

PA: *CO_2 emissions associated with integrated circuit manufacturing, I think they're expected to quadruple over the next decade. Why is that? Simply because of the massive explosion in digital infrastructure, an explosion that is not sustainable?*

EG: There are two factors to that quadrupling number. It's really sort of doubling twice. One time, because of complexity, so going to more advanced nodes, having more process steps involved, that creates a growth. And then the other thing that creates a growth is the volume, so the market itself is getting larger. So those two things together add to the quadrupling. And I agree it's not sustainable. There are some low hanging fruit things we can do. One of them is move to greener energy and another one is improved abatement. Those are in the works, planned, but even with those two, we still are about two and a half x off where we need to be to meet the Paris agreement - reducing by 50% over the next decade.

PA: *I think the semiconductor industry, or certainly the majority of companies, have committed to the carbon neutral and net zero targets by. It's debatable how much activity is maybe being done right now to get there. But I know in this context, Imec has launched the Sustainable Semiconductor Technology and System programme. The idea behind this is, I think, to help the supply chain with these changes?*

EG: First, on the horizon for the targets, there are some companies who are more aggressive and they

have net zero goals for more like 2030. The problem for these companies is very real and one of the big gaps in the industry was, well, how do we measure, how do we measure over a full process what the emissions impact is?

And that's where Imec netzero was launched to provide a way of measuring the impact of creating fabricating an IC device from cradle to grave. We work on the fabrication piece so that obviously there's a whole value stream, but everyone in that value stream is going to have to become involved. But our main focus, at least initially, has been on the fabrication piece. So, from the silicon coming in, to a chip leaving.

PA: *And expanding on what you just said, I think that you're taking a bottom-up approach. You're looking to provide insight, actual data in terms of environmental impact assessment and that's to do with what you call the process flow. So, that's before people even start the manufacturing process, it's to understand the impact of what they're planning to do, is that correct?*

EG: The application can be used either way. Either you could really just have a methodology for assessing what's already done today, or you could look towards the future and say, I know I have these process steps, calibrated, I know what an etch step costs environmentally, I know the same for a resist. Apply step costs, and you can basically string them together with a different process, flow forward, looking into the future, and make decisions based on minimising the emissions for those future processes.

I think it can be used multiple ways, really, with this bottom-up approach. It's like putting lego together - you have your building blocks, which are the process steps. You can link them however you want to assess a given semiconductor flow.

PA: *In terms of that already, if I understand correctly, you have a physical fab where you can explore the idea behind various environmentally friendly process solutions. What's being done with this, is it just available for hire, or do you do your own research and then also offer it to semiconductor vendors - how does that work?*

EG: We have a lot of fab space, over 12,000 metres squared of fab space, and it's 200 millimetre, 300 millimetre, and also some specialty fabrication areas. And those are used multiple ways, but it is a functioning fab.

One of the ways that Imec netzero is used is we can run a process flow, identify what the big contributors to emissions are and then specifically target what we like to call improve projects on those sectors. For example, if it's a fluorinated gas etch, we can specifically target projects that look at replacing the fluorinated gases (with their high global warming potential) for less impactful options. So that's one of the tangible ways Imec netzero plays with the fab space we have at Imec.

PA: *And you use that for your internal research, or do you also have outside organisations ask to use it and you work with them on anything they're looking at?*

EG: Both. I mean, Imec is a research institute and there are a huge number of partners as part of our ecosystem. So it's definitely both some internally owned systems and projects, but a lot of them are collaborative because ultimately our mission isn't just to identify a solution and keep it to ourselves. Our goal is to identify a solution and propagate it throughout the industry so that we can all reduce our emissions.

PA: *One of the main reasons we're having this discussion is that you've fairly recently developed a virtual fab as part of your Imec netzero modelling platform. It would be good to understand where that idea came from and what is the objective?*

Either you could really just have a methodology for assessing what's already done today, or you could look towards the future and say, I know I have these process steps, calibrated, I know what an etch step costs environmentally, I know the same for a resist

EG: That is the netzero virtual fab. You can almost use them interchangeably, so it's really just a question of how you put the software together. I mean, it all relies on these calibrated models with a combination of supplier input and measured input to identify the emissions associated with a certain process step, and then strung together, they become part of a whole fab. In the virtual fab, of course, we have to add things like timing, idle time yield, a lot of complexity can get added on, and the software is pretty flexible in terms of being able to choose what you include or don't include, even abatement options. There are different ways that people deal with emission output from tools like gases and those models can be changed. Also, there's a lot of flexibility within this system so that if we have a partner as part of the programme, who wants to run their own use case, they know certain things about their yield and die size fab timing, they can modify it at as they choose.

PA: *And using this modelling platform/virtual fab tool, IMEC and partners have been able to quantify the 'environmental impact of patterning-related*

process steps for various logic technology nodes'? Or is there more to it than that?

EG: There are logic nodes, but we can do NAND, we can do DRAM, you can do multiple different types of devices, so it's not just logic. A lot of the same background is there if you think about it, it's a virtual fab that can make different things and you just have to modify the flows in order to get there.

PA: *In terms of what you've been able to do with the virtual fab tool so far, what have you discovered, for example, to do with lithography and etch carbon footprint? You've got some interesting results, is that right?*

EG: Yeah. So I'm from the patterning area, that's my technical background most recently. I am part of the sustainability team but definitely targeting to improve different processes within patterning. If for example we focus on a future node, you can see that I think for an N3 Wafer, it's almost 40% of the influence comes from just patterning alone.

So, etch and lithography. We really targeted that area. In terms of lithography, the types of things you can do, we wanted to know. For example, if you go from DPV multiple patterning approaches to introducing EUV, which if you look and just compare DPV tool and an EUV tool, the EUV tool uses a tremendous amount of energy. It's a complex source with relatively low efficiency to get the EUV light. And there was a lot of concern about introduction of EUV and manufacturing and what that would do with two emissions. So we did that comparison. But what we find is, for example, if you use N7 with and without EUV, the version with EUV eliminates a lot of extra process steps that are related to using multiple patterning approaches. So yes, you introduce this really high emission system but you eliminate a lot of etch steps, a lot of clean steps, a lot of deposition steps and in the end you actually have a lower emission fabrication process.

So that was one good example. We'll be doing that sort of activity again when we talk about moving towards High-NA, which is even a different throughput model and something else we'll have to look at for etch, there are other things to look at. For example, what can we do to optimise the etch stack in order to minimise the etch processes or to optimise there's a lot of detailed process work that can be done on etch. And it was really helpful for us to identify it as a big contributor. Especially the high GWP gases are something that needs to be addressed in order to get the etch impact lowered.

PA: *You described there the overall net benefit of the EUV process. But I think you've also done some fab experiments around lowering the dose of EUV as well. What results have you got with that?*

EG: Yeah, so for example, you can just run a curve that shows what the impact of changing dose does. And there are a lot of different ways to address dose. And reducing dose also reduces cost. You have a certain tool with a given throughput and if you just lower the dose your throughput during the process time is going to increase linearly with that. So it's a pretty obvious knob to work on and one that helps cost as well as emissions very easily. But it's not so simple to get equal performance at a lower dose point. So some of the kinds of things you can do is use different resists, different bakes. So we look at all of those things and what we're doing now is we basically have a calculator that we can apply to different projects just to see what the benefit is when you change dose, for example.

PA: *Okay, so the ultimate there, you'll produce, as you say, some kind of table or best practises so people can understand all the variables. Obviously, you need to produce a product - that's important, but also you want to minimise or optimise your environmental footprint. So, it's helping people understand the consequences of what they do or don't do during the manufactured process?*

EG: Right. So for a long time we've talked about PPAC, right. Power, performance, area, and cost, those have been things the whole industry has optimised around. What we'd like to do is add E for environment to that. So PPACE, and just like you said, just being sure that during the development phase we're optimising for emissions as well as everything else. It's an innovative industry, we can do this, but we have to know what we're measuring.

PA: *And in terms of the partners, I believe you're able to share, for example, you've been doing some work with Edwards, so it'd be good to understand how you've been working with them and what sort of area helping them, collaborating with them?*

EG: Yeah. Edwards is a great example of sort of an improved project. One of the consumables on the scanner for the EUV scanner is hydrogen. It's used as a gas to keep the source clean, to keep the reticle environment, mini environment (RME) clean because it keeps carbon build up so that your mirror

If you really look critically at an etch recipe, there a lot of knobs that can be turned to minimise either the power consumption or what's more important for etching is what we call the scope one emissions that are associated with the GWP gases

reflection stays as high as you need it to. So again, helping throughput. It also keeps particles away from critical areas in the source. So there's really a tremendous flow of hydrogen through the system. And what Edwards has developed, they're a vacuum and abatement company, and they have developed a system that actually reuses the hydrogen.

So rather than just consume it and then abate it with a common way suchas burning with methane, which is a high GWP gas and a pretty consumptive process, instead they're recovering. And we had the first demonstration of that system in fourth quarter of last year at Imec and demonstrated a 70% recycling of the hydrogen. And going forward, we anticipate as much as 80%. Some changes are being made now to look at that. So, a really nice example of an abatement improvement that can really reduce the emissions associated with using EUV.

PA: *Is there anything to add on the load? Because I know you are doing lots of work on the low dose solutions for EUV Lithography. Again, is that with partners or is that more of your internal research?*

EG: A lot of the dose reduction projects are actually together with ASML. They're one of our big partners there, but then almost every resist supplier is aware of this challenge and there are different formulations looking at that. So, I would say a lot of those dose reduction work is together with partners, various kinds.

PA: *And I also believe the work you've been doing, you've identified etch directions for improved sustainability. Can you explain how that works as well?*

EG: Yeah, so I think I touched on a few of them, but maybe just to say them all at the same time. So you can do things like optimise your recipe for having less power, more efficiency in terms of the use of the gases that you use, optimising stabilisation steps. If you really look critically at an etch recipe, there a lot of knobs that can be turned to minimise either the power consumption or what's more important for etching is what we call the scope one emissions that are associated with the GWP gases. Those are, I guess, the biggest things.

One of our big thrusts this year is working on various ways to have what we call reducing the fluorinated content of the gases that are used in etch. So that's basically reducing the GWP. There's an output side of that which is working on abatement too. And that'll obviously be considered with any etch process that we change. Etch is complicated, so there are a lot of pieces that come into it. And of course, we need to maintain performance at the same time as making all these other changes. But there are some good examples of effective work in the industry and we're trying to bring more of those, optimise them and bring them to people's attention. But we're not alone in working on this. There are a lot of companies both material suppliers and edge tool suppliers that are also working in this area, which is good because it's a high impact area.

PA: *To characterise it, is it very much trial and error? You tinker with a certain parameter, do you then anticipate a result and it tends to come as you expected, or is it often unexpected? So, it is very much you're a bit in the dark, trying bit by bit all these different recipes, if you like, or do you have a fairly good idea of what you think will work and then you use the virtual lab to just say, yes, what you thought was indeed correct?*

EG: The virtual lab is helpful to a point here, but we do need to make measurements as well, because the input gases, you could understand right away what the embodied carbon of making a certain type of gas is and how much it leaks and guess at what the output would be after etch. But in fact, you really need to measure. So this is one of those cases where you might have a relatively good idea, but measuring the by-products after etch are really important because some processes are very efficient consumers of the greenhouse gases.

And if that's the case, it's much, much less of a problem than if they're actually being released into the atmosphere. And also, I should mention, my background was not etch until recently. I've been focusing on it more because of the sustainability work. So to me, plasmas are a little bit of a black box. I think that's the way most people look at them. But perhaps if you had someone who grew up in plasmas, they wouldn't think about it quite that way.

PA: *And the overall objective is that you can get to the point where you can produce a semiconductor process flow with the sustainability angle, very much part of it. Do you have a time frame for that and how is your work going towards that overall goal?*

EG: Our initial goal was to create this virtual fab or Imec netzero platform, so that you could actually

measure and assess where you are today and then work from that. On terms of being able to move the needle of HVM manufacturing that relies on adoption and changes within the industry.

So our big goal there is really just to collaborate and partner as much as we can. For example, we are part of some larger organisations as well, such as SEMI's SCC, the Semiconductor Climate Consortium. We're heavily involved there and with other groups like IRDS, because I think climate is one of those things, no one's going to be able to do it alone. And what we can do is try and look for the biggest gaps in the industry and try and fill them and sort of act as a way to propel everybody to a state where we're using less and emitting less. But Imec could have a perfect process and if it's only at Imec, it doesn't help anybody.

PA: *Just to restate, the fundamental issue is you're trying to maintain and develop patterning processes for the industry moving forward, but at the same time reducing CO_2. So to a certain extent they might appear, on the face of it, sort of incompatible goals. But your idea is obviously to make sure that the industry progresses, but it also reduces its carbon footprint – achieves much more in terms of sustainability.*

EG: Exactly. I don't think the industry would accept a process that wasn't at a high level. They wouldn't accept, for example, higher line edge roughness or lower EPE just because you reduced emissions. They want everything. But I think if we do this at the early stages, that's possible.

PA: *More generally, in terms of the industry's outlook on sustainability - I think we covered earlier on the fact that, although 2050 is where most of the world's headed, you say that some organisations are working to a much tighter deadline. A lot of industries, they started paying by lip service, a bit of green washing and then at some stage they actually started getting really serious about sustainability. Is that the same with the semiconductor industry? And do you think they've now fully understood their sustainability obligations or is there still a bit of a mixed picture as to companies that are at the forefront of it and others that are perhaps dragging their heels a little bit? Because it's obviously, as we've discussed, a complicated process to understand how you can become green at the same time as carry on doing what you've always done in terms of the manufacturing?*

EG: I think when you think about most companies, there has been a shift in that, in order to meet these net zero targets on a realistic timescale, it's not just what the company itself does, their scope one and scope two emissions, it's also scope three - what comes into them and what leaves them. That's also going to be part of the equation and for that to happen they need to push on everybody throughout the supply chain. So now you have this pressure that's coming from companies who have made these very public commitments, who have pressures from their communities to do it and from their customers. It's becoming a lever on costs or getting business to actually have a green portfolio.

I think just lately there has been a shift in this way and that making the low emissions decision is also going to be good for business. I think when that happens you're going to see an accelerated rate of change and I do see it already that some companies have been working on, for example, greenhouse gas replacements for ten years and now all of a sudden everybody wants to talk to them.
I do think change takes time, but I think the pressure is there to change more quickly now.

PA: *And when it comes to achieving that, are you optimistic that the industry can improve and continue to meet the increased demand for the product as the digital world explodes and also meet every sustainability type?*

EG: I guess I'm hopeful. I am worried about greenwashing. It is something like how do you make

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sure that we report? But I think that's one place that standards from larger groups can come in and help, perhaps. And I do think it's possible that we'll have to compromise at some point. But I do see the pace accelerating, I think we're moving in the right direction.

PA: *Finally, when it comes to the external pressure, you say obviously big corporations sign up to ESG goals and they push down on the supply chain. But do you think it's inevitable that there will be the need for government legislation or do you think the whole industry can collaborate better and more quickly to make sure that they try and stay ahead of what government might be asking? Or do you think there will be a bit of a crunch time when legislation comes in, everyone looks at each other and goes, heck, what are we going to do? How are we going to meet that?*

EG: Well, I think the interesting thing about the global industry that we're in is that different governments have come in at different times on different pieces.

For example, PFAS legislation has been a little bit faster in the US with 3M, so we haven't talked about PFAS because it's not directly emissions related, but it's the forever chemical. And there you can see what the impact of legislation has on not just the US companies, but all companies.

I do think that it helps add this fear of legislation coming and we need a solution in place and we're going to have to ask for exceptions and it might not be granted and then what will we do? So I think it's helpful. I think the more we can have government legislation,

in addition to the corporate pressures that already exist to be green because of consumers and customers, I think that's all going to help. So I guess I think it's both. I think sometimes companies can act a little more quickly than governments, but when a government speaks, it carries a lot of weight.

PA: *And just on that point, do you think there will be overall a fairly level playing field or, as history shows us, a lot of manufacturing sectors have been quite agile. To put it bluntly, they've moved where they can perhaps escape certain regulations and carry on doing certain things. Do you think there will be any hiding places for the industry should they wish it? Or do you think there'll be pretty comprehensive, globally agreed legislation that will mean that they can't run away from their obligations?*

EG: I have trouble imagining that all of the governments will agree to putting in place the same legislation at the same time. I like to think that customers will not welcome companies hiding from emissions regulation, but I don't feel equipped to say that it won't happen.

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Fab scheduling is now so complex that it needs next-generation intelligent software

There are literally billions of possible ways to schedule all the work through a fab, so finding the best way is an immense challenge. This is a multidimensional problem that current heuristic scheduling software just cannot handle. A new approach to the complexities of scheduling, developed by Flexciton, is already making a significant impact in the semiconductor industry.

BY JAMIE POTTER, CO-FOUNDER AND CEO, FLEXCITON

GLOBAL MEGATRENDS such as autonomous cars, AI and high performance computing are driving technological advancements and the need for ever more sophisticated chips and smaller process nodes. As a result, the wafer fabrication process is becoming even more complicated, with certain types of products requiring wafers to go through thousands of process steps and taking several months to manufacture. In addition to the challenge of complexity, there is an expectation for wafer fabrication to become more sustainable and energy efficient while increasing productivity and keeping the cost per wafer low.

The level of complexity in the production process is only expected to increase and unless fabs adopt new methods to simplify and streamline management, the challenge will become overwhelming. Chip companies must improve their performance and output by addressing the sophistication of their products. The current common approach of fabs to deal with complexity involves breaking down a big problem into smaller, more manageable ones, with specific teams assigned to tackle each challenge. In principle, this approach seems the right one, however, in practice it has significant drawbacks. Different teams within the fab often have different priorities and KPIs, which leads them to work in isolation. As individual teams strive to maximise their own KPIs, conflicts can arise as the KPIs of one area may be in opposition to those of another, negatively affecting the overarching fab objectives.

For example, while process engineers prioritise yield, industrial engineers are focused on reducing cycle time and increasing throughput, and manufacturing operators seek to maximise the number of moves per day. As an illustration, the objective of maximising the yield can impede the increase in throughput. Conversely, altering the recipe to enhance yield can impact throughput and cycle times, particularly if the changes require optimization over time.

Using scheduling to conquer complexity

Let's dive deeper into the issue of complexity and how it impacts the scheduling of wafer production in

particular. The process involves various stages such as; metrology, photolithography, diffusion furnace, epitaxy and more, each with its own unique set of guidelines and tools. The most common approach to scheduling is utilising rules-based software that dictates the sequence in which wafers are processed.

However, the sheer number of rules per area can be overwhelming, and industrial engineers often resort to simplifications and shortcuts to manage and control each stage's parameters. Again, these 'shortcuts' may lead to suboptimal decisions made by the scheduler, with a negative impact on performance. Another problem with this approach is that it requires a huge amount of manual input from skilled industrial engineers to write and maintain the rules in an attempt to keep pace with a fab's dynamic nature. In a fully operational fab, things are constantly evolving, which requires constant human intervention to ensure that scheduling rules are proactively monitored and updated. This is necessary to accommodate any changes that may occur and to create new rules in situations when new tools, recipes, or product mix are added. As the complexity of chips increases, so does the complexity of their production, necessitating frequent updates and additions to the rule set.

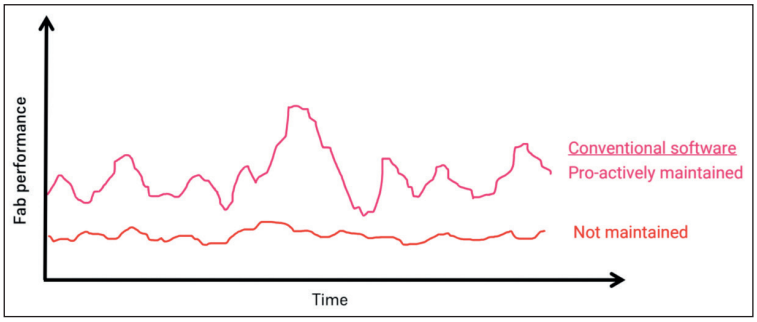
As shown in Figure 1, these constant changes have an impact on the performance of the rules-based scheduling. Sometimes it can make good decisions, but other times – due to the lack of intelligent algorithms – it can make decisions that are not optimal. It has significant peaks and troughs due to the time lags between introducing a change in a fab and, subsequently, new rules. In order to sustain performance, It does require proactive rules maintenance and full-time industrial engineering resources to work on it. This is currently a problem in itself. The industry is suffering from a skilled labour shortage and industrial engineers are particularly in high demand. Attracting a new generation of IEs to work in a wafer fab, often built in remote locations, is proving to be a challenge. If a huge amount of their capacity is taken up by tweaking a rules-based scheduling system, we are only making this challenge harder.

Working smarter, not harder

How can we effectively manage production complexity without compromising its potential? Attempting to simplify data is not the solution, as its complexity is what makes it a potent tool. Instead, by fully embracing smart manufacturing technologies that allow us to fully utilise the abundance of data, we can achieve a more complete and accurate understanding of a fab's operations. Rather than simplifying the data, the focus should be on streamlining the process.

How does Flexciton software work?

There are literally billions of possible ways to schedule all the work through a fab so finding the best way is an immense challenge. This is a multidimensional problem that current heuristic scheduling software just cannot handle.



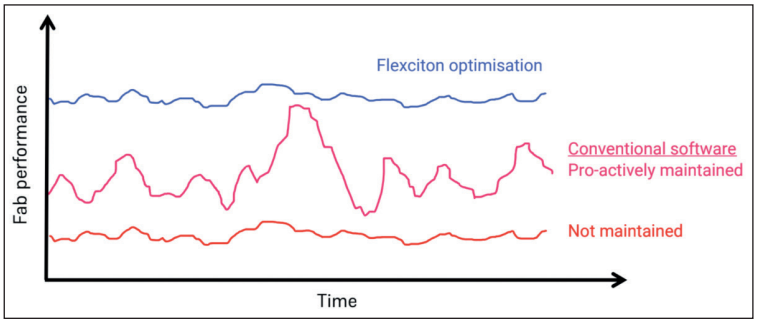
➤ Figure 1: Rules-based scheduling requires proactive and time-consuming rules maintenance to sustain performance.

Flexciton's next generation scheduling software is the only solution on the market that is able to solve this. It pairs powerful mathematical optimisation technology with smart decomposition techniques to work out solutions with complete autonomy. This advanced, intelligent software has the ability to generate an optimised production schedule within a few minutes by searching through billions of scenarios and honing in on the best possible one that achieves the overall KPIs. This repeating, iterative process ensures that it is continually updating the schedule to allow for any changes in fab conditions or business objectives (Figure 2).

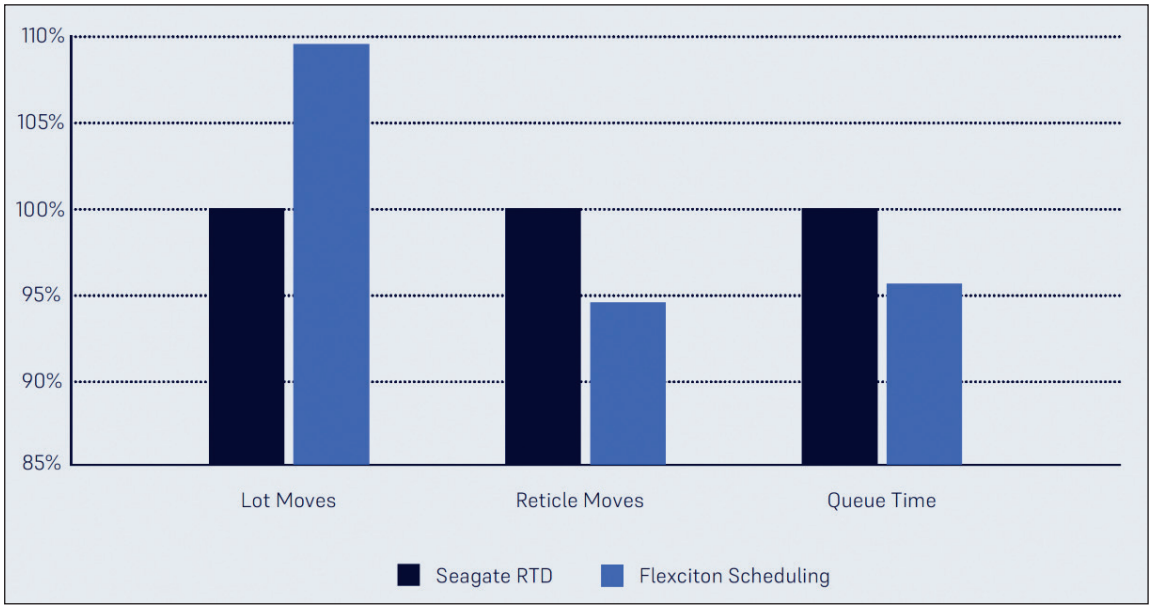
Importantly, the software does not need a skilled industrial engineer to create an initial set of rules and to be modifying or creating new rules all the time. The intelligent software is learning all the time how to optimise the running of the fab to meet the given KPIs. If the objectives change, then it looks through the myriad of possible scenarios to find the one that meets the new objectives which is why it does not need any rules to guide it. This makes it the first and only, goal-centric and self-adapting scheduling solution.

How Flexciton eliminates bottlenecks

The scheduling software looks at how the queueing changes over time for each toolset. The Flexciton scheduling application has a heatmap that illustrates any considerable queuing in front of a toolset in red and then going to green for toolsets with



➤ Figure 2: When compared with conventional rules-based software, Flexciton's software is able to maintain optimal performance with greater autonomy.



➤ Figure 3: The results gathered from live deployment onto a Seagate photo-lithography toolset, with 9.4% increase in throughput despite reducing reticle moves by 5.3% and queue time by 4.3%.

little or no queuing. The software then focuses on each red section and tries many different possible adjustments to the scheduling to balance the load across all toolsets and reduce bottlenecks. Because the software has the vital insight of future activities, it can see how a single change can have a knock-on effect not only on the timeline of the toolset in question but also the timeline of all the other toolsets.

Seagate case study

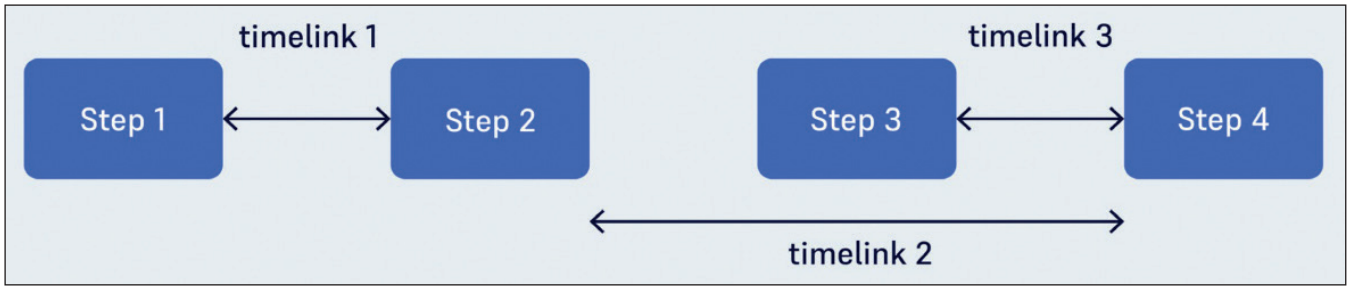
The photolithography area has a long and highly reentrant process with 1,600 steps and is the core of the fab so it is critical to have an optimised schedule. The results below are from one toolset in a live production environment, with an internal reticle library, where reticles can be moved individually between tools and cabinets.

Renesas case study

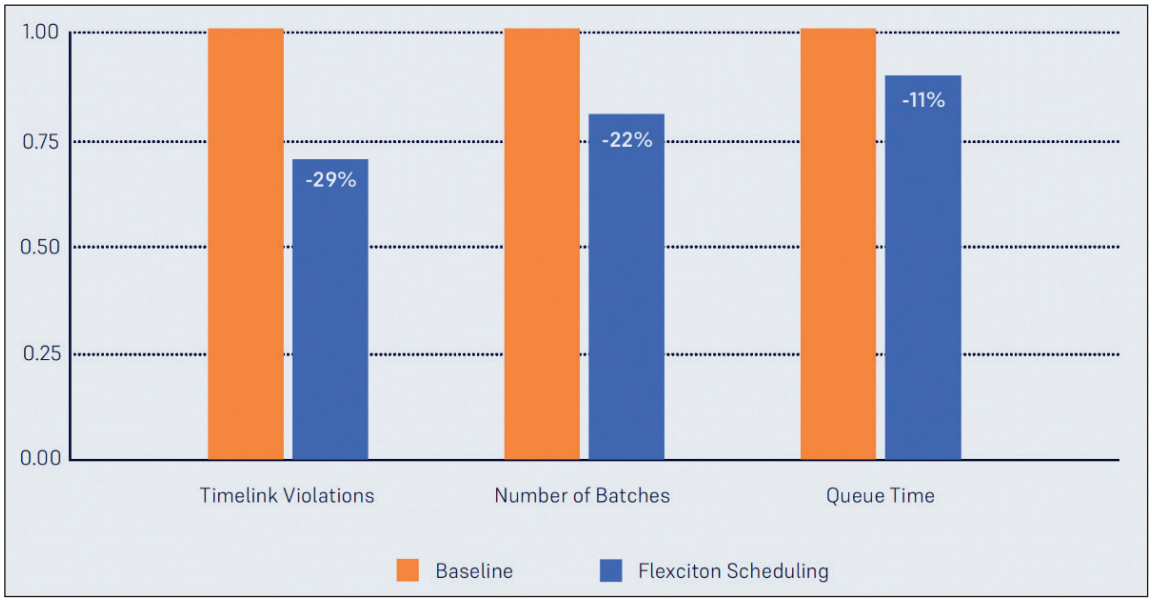
Timelink constraints are one of the most complex issues to handle in fab scheduling. They define the maximum allowed time between steps in the production of a wafer. Correct scheduling of timelinks is critical to helping minimise the risks of oxidation or contamination. This can happen when a wafer is queuing outside of a tool for too long, resulting in scrappage or rework that damages profitability. Renesas Electronics asked Flexciton to see if its intelligent scheduling software could improve this aspect of scheduling in the diffusion area of its wafer fab.

What makes timelink constraints very hard to schedule is their interdependence. For example, by moving from step one to step two, the wafer enters the first timelink. When moving from step two, the wafer enters a second timelink which lasts until step 4. However, there can also be a third timelink constraint – known as a nested timelink – between step three and step four which overlaps the second timelink constraint (see Fig. 4). Therefore, step three has to be scheduled in a way that allows for both the second and third timelink constraints to be adhered. This example discussed is just for a few steps but, in reality, there could be hundreds of steps and many overlapping time constraints that need to be continually considered. This creates one of the most complex scheduling problems seen in a wafer fab, and any violation of the timelinks has a negative financial impact.

The software was run in a simulation environment that replicated the way that Flexciton's scheduler would have run live at the Renesas fab. The results showed that a significant improvement in reducing



➤ Figure 4: This diagram shows an example timelink system between four consecutive steps. The overlapping timelinks mean that after completing step 3, the lot begins a new timelink (3) whilst still transitioning an existing timelink (2).



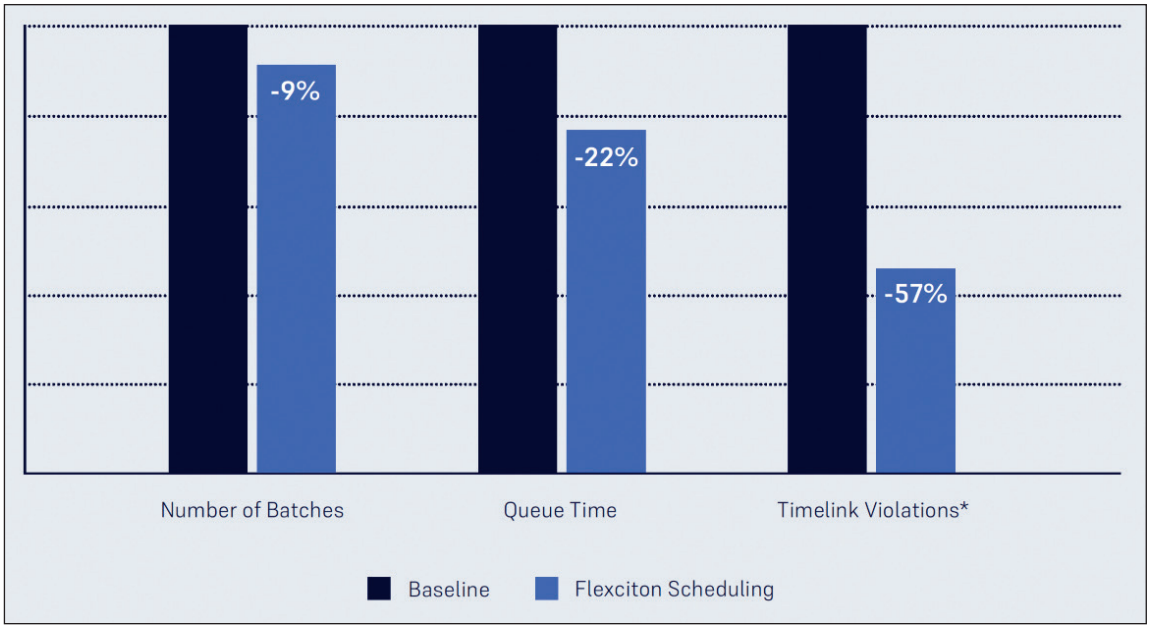
➤ Figure 5: The KPI improvements for timelink violations, number of batches, and queue time against the baseline results at Renesas Electronics.

timelink violations of 29% could be achieved. Additional improvements would be possible of a 22% reduction in the number of batches and an 11% reduction in queue time despite these two KPIs being conflicting (see Fig. 5). This is because decreasing the number of batches naturally means increasing the number of wafers in each batch, but this increases the queue times for each batch as operators wait for new wafers to arrive at the tool before processing them together. Currently, most fabs have no knowledge of the arrival times for future lots so operators can sometimes wait unnecessarily to maximise a batch size, causing more wafers to queue and damaging productivity. Uniquely, the Flexciton scheduler can see how lots are moving in time and can thus optimise the trade-off between number of batches and queue time to achieve the impressive gains seen on these conflicted KPIs.

Case study: a wafer fab in the EU

The fab was struggling to achieve efficiencies at clean and furnace due to complex timelink constraints. A similar off-line approach of a simulation environment was used to run Flexciton's scheduling software. The customer was so impressed that the software is now on live deployment in the fab.

Jamie Potter, Flexciton's Co-Founder and CEO, explains, "The key differentiator of our approach is that our software has the intelligence to predict what may happen in the future based on the current state of a fab (or WIP in a fab). It searches for the best solution amongst billions of possible solutions to continuously keep finding the optimal schedule that meets the KPIs to maximise a fab's productivity and profitability. Humans and heuristics just can't do that."



➤ Figure 6: The results gathered across the clean and furnace area at a fab in Europe.

New centre for semiconductor research in Dresden

With the establishment of the Center for Advanced CMOS & Heterointegration Saxony, the Fraunhofer Institute for Photonic Microsystems IPMS and the "All Silicon System Integration Dresden - ASSID " branch of Fraunhofer IZM are pooling their expertise in semiconductor research.

BY MARTIN LANDGRAF, BUSINESS DEVELOPMENT, KONRAD SEIDEL, GROUP LEADER EMERGING MEMORIES, AND ROBERT KRAUSE, PROJECT MANAGER AND PROCESS ENGINEER, AT FRAUNHOFER IPMS.

IN THE FUTURE, they will offer the complete value chain in 300 mm microelectronics and thus the prerequisite for high-tech research in future technologies with international reach. The 300 mm wafer industry standard is crucial in this context, because on the one hand it is the only way to ensure a rapid transfer of research results to the semiconductor industry in Saxony, nationwide and also worldwide. On the other hand, this wafer standard is a basic requirement to be able to successfully participate in new technology developments in the near-frontend sub-100 nm range. The center offers customers the opportunity to develop and test new manufacturing processes, as the stringent workflows in high-volume fabs such as Infineon, Globalfoundries or Bosch offer little scope for such test phases.

Among the persons (flnr): Prof. Harald Schenk (Director of the Fraunhofer IPMS), Sebastian Gemkow (Saxon State Minister for Science), Dr. Manuela Junghähnel (Site Manager of the new Center), Prof. Reimund Neugebauer (President of the Fraunhofer-Gesellschaft), Prof. Hubert Lakner (Institute Director of the Fraunhofer IPMS), Dr. Wenke Weinreich (Site Manager of the new Center), Dr. Manfred Horstmann (Vice President of the Fraunhofer-Gesellschaft). Hubert Lakner (Director of the Fraunhofer IPMS), Dr. Wenke Weinreich (Site Manager of the new Center), Dr. Manfred Horstmann (Vice President Globalfoundries Dresden), Prof. Martin Schneider-Ramelow (Director of the Fraunhofer IZM), Dirk Hilbert (Mayor of Dresden)

➤ Figure 1: Symbolic wafer handover for the ceremonial opening act of the "Center for Advanced CMOS & Heterointegration Saxony" in Dresden on June 7, 2022. © Schneider-Bröcker

Introduction

With the Center Nanoelectronic Technologies CNT division of the Fraunhofer IPMS and the ASSID branch of the Fraunhofer Institute for Reliability and Microintegration IZM, two research facilities in the field of microelectronics that are unique in Germany are located in Saxony. Today, they are the only two German research centers for applied microelectronics research based on 300 mm wafer industry standard equipment. The core of the concept for the foundation of a joint center was to combine the scientific and technical competences of IZM-ASSID and IPMS-CNT with regard to research and development (R&D) in 300 mm front-end and back-end processes. On the one hand, this will increase efficiency and complete the value chain, while at the same time opening up new fields of research.

Semiconductor material screening and evaluation services

An important prerequisite for cooperations with industrial partners is the industry-compatible clean room of the new center, which houses an R&D technology platform with a plant procurement value of more than 120 million euros on an area

of approx. 3,000m?. Crucially, in addition to the process equipment, the associated logistics (such as stockers and sorters) and all the measurement and analytical equipment are based on the 300mm industry standard. The IPMS-CNT conducts applied research in the front end of CMOS manufacturing. Fraunhofer IZM-ASSID complements this expertise with innovative packaging and heterointegration technologies.

The new center provides semiconductor manufacturers and suppliers with screening and evaluation services for materials, processes, chemicals and consumables from laboratory to production scale. Services include consumable benchmarking, process development, ultra large scale integration (ULSI), pilot production and equipment evaluation. Independent evaluation and test control with ISO 9001 certification is performed in a production-like environment with standard industrial equipment. This includes direct exchange of wafers with production lines (short loops) and professional contamination management. Pre- and post-processing of individual process steps are optimized to enable rapid scaling from laboratory scale to operational capability in a high volume fab. The center can draw on more than 10 years of experience in introducing new materials into production and thus offers customers savings in resources, equipment investments, personnel and time (time-to-market).

Insight into semiconductor research and manufacturing

Individual process development

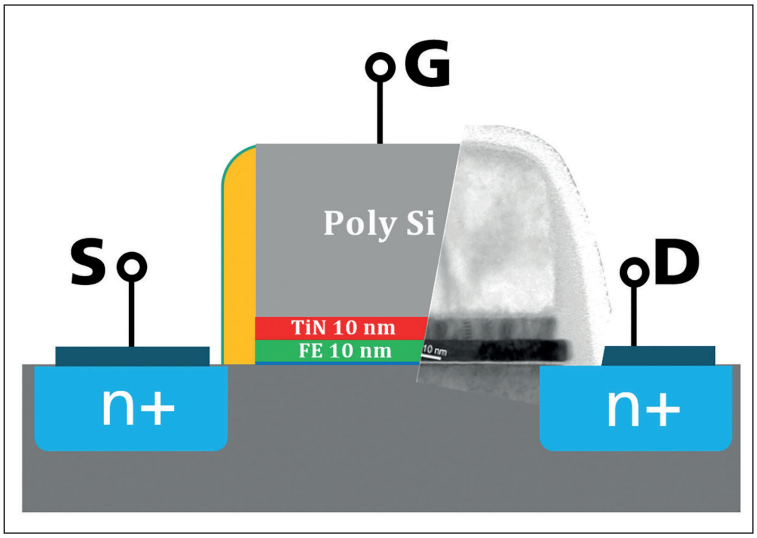
An important core task of the center is the development, optimization and transfer of process and integration concepts with industrial partners. One example of this is the development of novel memory technologies for, among others, the long-standing industry partner Globalfoundries. The research on innovative processes carried out by Fraunhofer IPMS in the clean room and laboratories forms the basis for new reliable memory concepts as applied in embedded memory blocks as well as future neuromorphic computing concepts.

The ferroelectric hafnium oxide researched at Fraunhofer IPMS offers much potential for use in future chip generations for a wide range of applications. Due to the appreciable polarization property of the ferroelectric crystal structures, this material can be used for non-volatile data storage. Such concepts have been in use for many years. However, conventional ferroelectric memories are often based on lead-containing materials, such as PZT, which on the one hand require special precautions for processing in the clean room and on the other hand are less scalable.

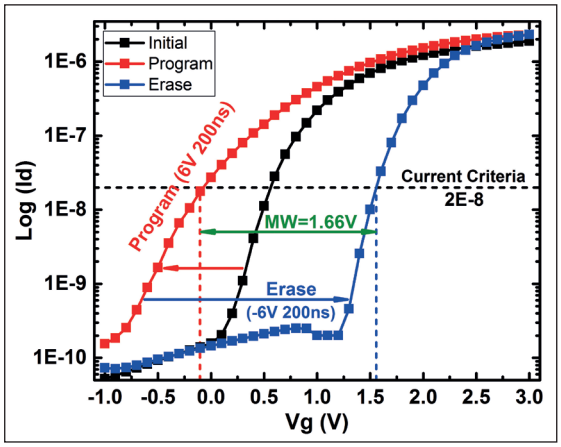
In contrast, hafnium oxide is an established gate dielectric in newer transistor generations, which can be provided with ferroelectric properties by selective doping with e.g. silicon. Embedding this ferroelectric material in field-effect transistors results in FeFET memory transistors (Fig. 3), which can be scaled very well due to the very thin ferroelectric layer and can also be switched with low voltages. By applying electric fields, the polarization of the ferroelectric dipoles can be switched. With the field effect of these dipoles, the operating point of the FeFETs can be shifted and thus the stored information can be read out non-destructively (Fig.4a). In addition to the very high switching speed and low energy consumption, another major advantage is the ease of integration into existing semiconductor technologies.

➤ Figure 2: View into the clean room of the new center on the 300 mm industry standard equipment. ©Fraunhofer IPMS

As part of a research project, new approaches for the ferroelectric material stack in FeFET transistors were explored by process trials at Fraunhofer IPMS for the industrial partner Globalfoundries. Using a FeFET technology platform established in the clean room and wafer exchange with Globalfoundries, innovative process variants for optimizing the reliability and switching behavior of ferroelectric transistors were developed and tested. For example,



➤ Figure 3: Schematic of an FeFET memory transistor of the IPMS technology platform. ©Fraunhofer IPMS



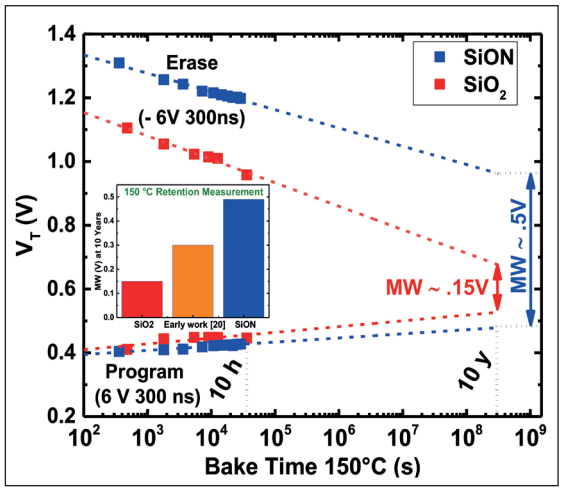
➤ Figure 4a: Current-voltage characteristics of an FeFET memory transistor for the two memory states programmed (red) and erased (blue) (Publication T. Ali et al. TED, 2018). ©Fraunhofer IPMS

a silicon nitride-based interface significantly increased the data retention of the memory cells (Fig. 4b). This process optimization was established at Globalfoundries and successfully demonstrated on scaled memory cells in the megabit range.

Screening and evaluation services

In addition to individual process development and process optimization, the CNT of Fraunhofer IPMS also offers screening and evaluation services for materials, processes, chemicals and consumables that are required and used in semiconductor fabs. For example, a long-standing cooperation agreement has existed between the CNT and BASF SE since 2014, which intends to jointly develop innovative solutions for the semiconductor industry. In this context, new chemicals for semiconductor processes such as plating and bonding are tested for BASF and process optimizations are carried out. In this context, BASF has installed a corresponding process plant of a renowned manufacturer at the CNT. This modern plating process plant for the electrodeposition of copper layers on 300 mm wafer scale is operated by the researchers of the Fraunhofer Center.

The technologies used in the screening include dual damascene plating processes for very small technology nodes down to less than 20 nm, as well as packaging technologies for chip wiring, in which trace materials are produced using RDL, TSV, pillar and bump plating for wafer level packaging applications.



➤ Figure 4b: Comparison of data storage for two interface variants. With the nitride interface, a significant improvement in data retention was achieved in experiments. (Publication T. Ali et al. TED, 2018). ©Fraunhofer IPMS

The Fraunhofer Center's work under the cooperation agreement includes research and development. In the area of electroplating, newly developed products from BASF are tested and ramp-ups to industrial scale are carried out. This includes the screening of chemicals, electrolytes and bath additives to deposit high-purity metal layers that will later be used in wiring structures in chip production. The Fraunhofer Center uses the system to test whether, for example, the deposition with new electrolytes currently under development is low-particle and produces a homogeneous layer on the wafer. The focus is also on investigating the properties of the deposited layers, such as grain size and orientation.

The second work area comprises demonstration and test trials. The facility is used to test BASF's latest technologies and innovative chemicals on test wafers or short-loop wafers and to generate process data tailored to customers' needs. In addition, parameter optimizations are carried out on production processes in order to further develop them and adapt them to new chip designs. The target parameter values to be achieved in the tests for metallization for wiring structures include good structure filling without voids and homogeneous structure and wafer surfaces. Since Fraunhofer is using the same equipment technology as is used by BASF's customers, this enables significant cost and time savings for the chemical manufacturer. With the completion of the pilot tests at the Fraunhofer Center, customers can thus immediately use the ready-to-use processes for the production of advanced electronic materials. The further development of materials and processes makes it possible to meet the constantly increasing demands on microchips in terms of functionality, speed and energy efficiency.

Wafer characterization in the clean room and laboratory area

The physical and electrical characterization of wafers in the clean room and in the specialized analysis laboratories plays an important role. In order to be able to evaluate the processes and components of nanotechnology research with regard to their application properties and reliability, a broad portfolio of highly sensitive electrical and physical measurement technology exists at the Fraunhofer Center in Dresden.

So-called inline measurements during the processing of wafers in the clean room can already provide initial insights into the functionality and electrical parameters of the manufactured structures in a non-destructive manner. This enables fast reaction times with regard to process adjustments and insights into the individual intermediate steps. After completion and ejection of the wafers, they can be analyzed with more in-depth analysis

methods using highly specialized electrical and physical measurement technology.

The wafers produced are then loaded into wafer probers in the electrical test laboratory, either as a whole or as a single sample, and the components on them are electrically contacted by means of micrometer-fine probe needles. Using the connected measurement technology, it is then possible, for example, to characterize characteristic fields of integrated transistors, the frequency behavior of capacitors and high-frequency structures, the switching behavior of memory cells, or leakage currents of dielectrics up into the femtoampere range, to name just a few.
An important role is also played by the high degree of automation of the measurement procedures, which makes it possible to determine the electrical properties over entire wafers by means of statistical measurements in order to be able to draw conclusions about the uniformity of the wafer processes in the clean room.

This consistent automation of the electrical measurement technology, combined with the wide temperature range of the wafer probers from -55°C to 300°C, also enables complex, lengthy measurements at various test temperatures without manual intervention and thus scientific research into physical processes in materials as well as the consideration of reliability in real application scenarios such as those found in industry and automotive engineering. As already mentioned, an important focus in the electrical test lab at the Fraunhofer Center is the characterization of non-volatile data storage devices. Here, individual memory elements or even complex memory blocks can be statistically examined on a gigabit scale with regard to performance, data retention and other reliability parameters.

Extensive tests and measurements are being carried out for the mixed-signal foundry X-FAB to improve its chips. In this context, memories of the nvSRAM technology are analyzed in a joint research project. An nvSRAM combines the advantages of a very fast but volatile SRAM memory with the properties of a non-volatile memory by integrating

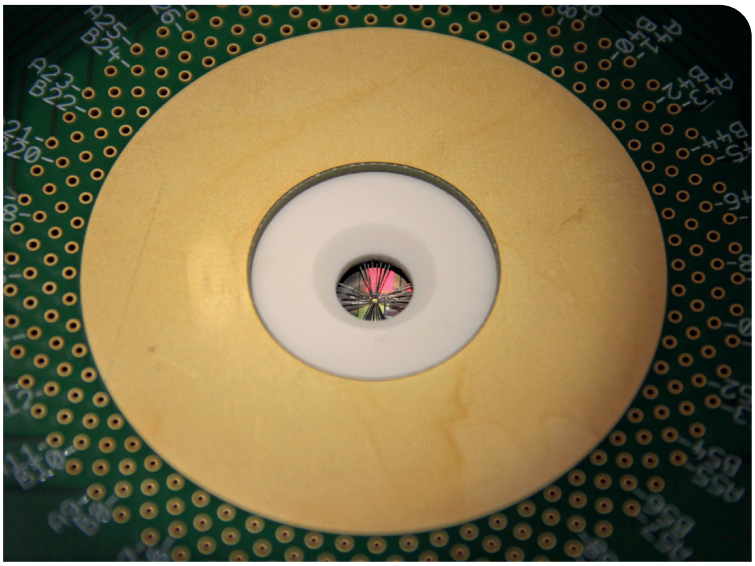
➤ Figure 5: Process control of development wafers at the Fraunhofer Center for Advanced CMOS & Heterointegration Saxony. ©Fraunhofer IPMS

corresponding memory cells into the SRAM circuits. Thus, in the event of a power failure in the system, the contents of the SRAM can be backed up within a few milliseconds, thus preventing data loss. At the Fraunhofer Center, larger nvSRAM memory blocks from X-FAB are being tested using fast mixed-signal test systems (24 analog and 96 digital channels) with regard to their switching characteristics, error rate and reliability under automotive conditions. The measurement results can be used to optimize memory technology and circuit design.

Cooperations of the Center

The implementation of joint research projects and cooperations with industrial companies is a core task of Fraunhofer. For example, the CNT division of Fraunhofer IPMS has already implemented projects with more than 100 customers. About a quarter of the industrial revenues come from Saxony, half from Germany (excluding Saxony). The largest customers include Globalfoundries, Infineon, BASF, X-FAB and Sony. In addition to orders from the major Saxon semiconductor manufacturers, there are numerous cooperations with smaller Saxon companies which, for example, do not have access to semiconductor foundries due to low volumes or specific material

➤ Figure 6: Electrical measurement technology at the Fraunhofer Center (left: automatic wafer prober, middle: semi-automatic wafer prober, right: semiconductor parameter analyzer). ©Fraunhofer IPMS



➤ Figure 7: Test structure contacted with test needles. ©Fraunhofer IPMS

requirements. The CNT is also an important partner for the semiconductor supplier industry. For example, a novel environmentally friendly wafer cleaning technology developed by a Leipzig-based startup (Intelligent Fluids) was tested for the first time under industrial conditions at the CNT. Based on the project results, the technology is now being used directly by semiconductor manufacturers worldwide. The long-standing cooperation with BASF to test and further develop chemicals for chip production is another example of successful collaboration.

Further cooperations exist with Saxon universities, especially the TU Dresden, as well as with non-university research (e.g. HZDR, IFW). An example of this is the cooperation with the Max Plack Institute for Structural Physics in Halle, where a new promising research cooperation in the field of magnetic storage is currently being realized.
At the European level, there is close networking between the Fraunhofer Group for Microelectronics, the CEA-LETI in Grenoble (France) and the IMEC in Leuven (Belgium). The three leading European Research & Technology Organizations (RTOs) in the field of microelectronics are increasingly coordinating their R&D activities. For the current European Research Framework Program (HorizonEurope), for example, joint research priorities were coordinated according to the “Smart Specialization” approach and implemented, for example, through a joint application to create a European “Testing and Experimentation Facility (TEF) for Edge AI”.

The CNT, together with the IZM-ASSID, plays a key role for Germany in this European cooperation in the field of industry-related 300mm research. Without these two research sites, Germany would not be able to play an adequate partner role in this field in the European semiconductor research triangle Grenoble - Leuven - Dresden. Internationally, Fraunhofer IZM-ASSID is also closely intertwined with working groups in the field of wafer level integration, including Heterogeneous Integration Roadmap - HTA, CPMT- IEEE, Sematech.

➤ From top to bottom: Martin Landgraf, Konrad Seidel and Robert Krause

Conclusion and outlook

The chips of the future should be three-dimensional, energy- and chemical-saving, environmentally friendly and inexpensive. The even more closely interlinked joint work of the Fraunhofer colleagues in the new Center for Advanced CMOS & Heterointegration Saxony will provide the best conditions for important impulses and research results to come from Saxony in future technologies.

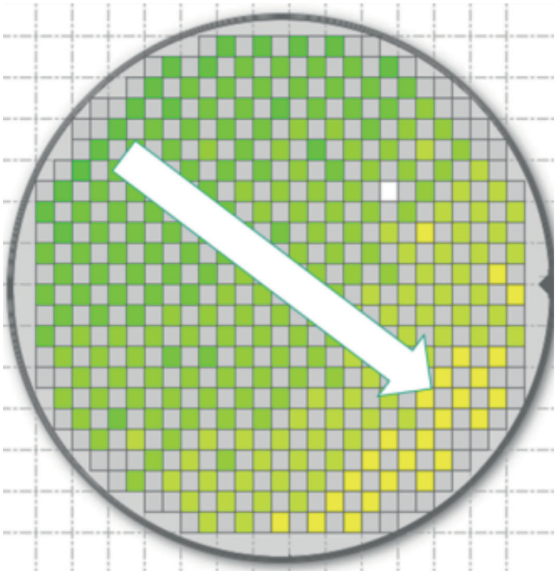
For example, the Center’s scientists are working together in the field of quantum computing to ensure that quantum production will be CMOS-compatible and thus more scalable in the future.

The Center represents an important link and bridging function between basic research and industrial application. In the area of neuromorphic computing, researchers are working on new memory devices and accelerators on in-memory computing solutions for particularly energy-efficient AI solutions (Edge AI).

Services

In addition to direct contract research for companies and R&D collaboration in publicly funded projects, the Center offers numerous services, such as:

- Nanopatterning by e-beam lithography for various substrates (e.g. Si glass) and sizes
- Processing of wafers (up to 300mm) with customer-specific layer structure
- Test Wafer Evaluation
- Studies on individual process steps such as CMP, ALD, DRIE, Cu Plating
- Wafer cleaning
- Screening and optimization of new chemicals and processes up to the 2x nm node
- Qualification of equipment and components for high-volume semiconductor manufacturing under standard industrial conditions



➤ Figure 8: Statistical measurement with check erboard wafer map and wafer signature

Why 'silicon proven' is not what you think

Agile Analog's approach to analog IP design and quality.

BY CHRIS MORRISON, DIRECTOR OF PRODUCT MARKETING AT AGILE ANALOG.

THE COMPLEXITY of integrated circuit design has expanded a billion-fold since the invention of the first transistor, guided by the famous "Moore's Law" of semiconductor manufacturing. An important factor to this ever-growing expansion is the development of the digital design flow. A modern digital design consists of several steps, a simplified flow chart is shown below:

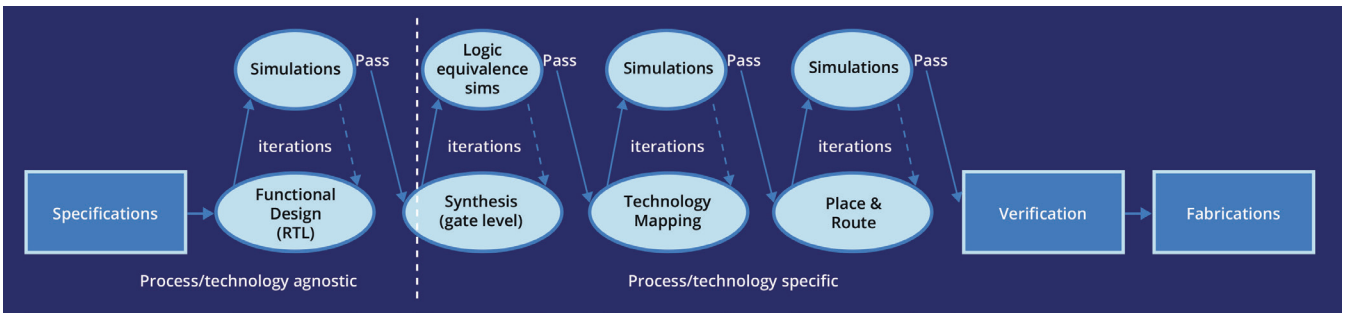
Digital design is initially done in a largely process agnostic way, guided mostly by the likely logic depth and its impact on the achievable performance. This enables excellent design portability between process nodes, without impacting verification quality. A comprehensive design tool flow and verification methodology to check consistency and compliance at each stage of the flow has enabled a huge growth in designer productivity as the level of design capture abstraction has increased. Along with the improved verification and signoff tools, it has enabled the automation of the digital design process to generate complex, high quality, right-first-time ICs that no longer rely on silicon validation for proof.

Although the digital design is process independent, the implementation of the design from synthesis through place and route takes full consideration of the target process node through the various models and signoff processes. Indeed, the same design can be implemented in a very different way and optimized to take advantage of the specific process features.

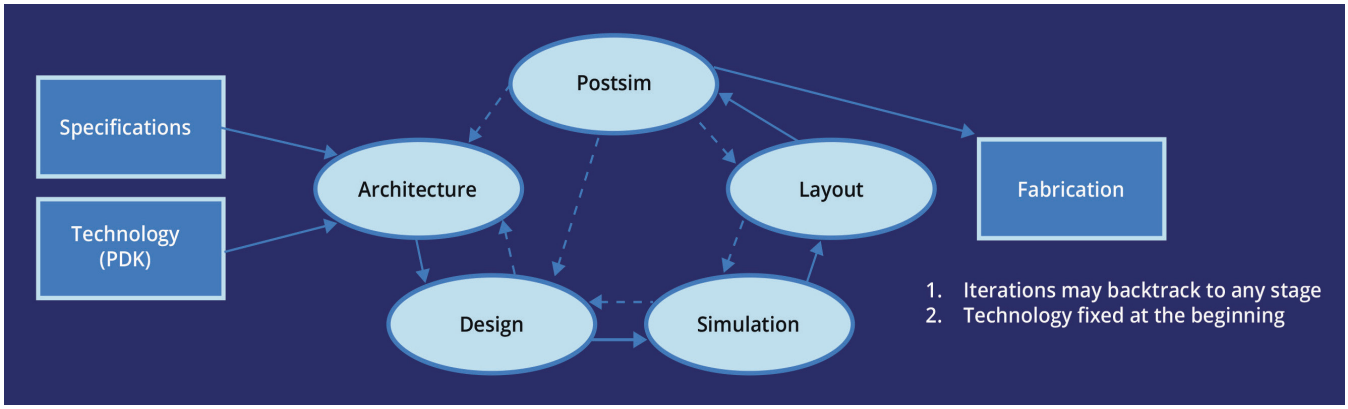
The process agnostic digital design allows full IP reuse across projects and product generations within a company. This it is a key reason why the digital IP business model has continuously grown and thrived over the years. The digital implementation process flow is process-specific and allows companies to reuse digital designs while keeping up with the newest generation of semiconductor manufacturing technology. Over the past three decades, digital design flow has been proven, improved and optimized, such that a first-cut design success is expected, even in the most advanced technology nodes.

On the other hand, the analog design flow is very different

While there are analogies between the analog design flow and digital design flow, for example the "architecture" in analog flow is akin to the "functional design" in digital flow, and "layout" in



➤ Simplified flow chart of a modern digital design.



➤ Flow chart of an analog design.

analog flow to "place and route" in digital flow, there are distinguishing differences between the two.

First, the analog design flow is a circular iteration of several cycles, which as different from the "linear" digital design flow. Depending on the complexity of the analog circuit block, experience of the circuit designer, expertise in the technology node, and many other factors, the design flow will iterate several times in the analog design flow loop, often between layout and postsim steps. In some cases, the architecture chosen cannot fulfill the circuit specifications in the physical level, resulting in a restart from the first step. Simply speaking, the time and effort needed to complete an analog circuit are approximations, and the uncertainty increases as the complexity increases or there are changes in technology.

Second, the technology or process node of an analog IP is decided at the beginning of the design, the available devices for architecture exploration and design, model cards for simulation, layout rules, and the metal R-C models are all process specific. If a project manager decided to change the process node, or even modify the process options available for use, the whole analog design often must start from square one. Finally, there is very little CAD automation in each step of the analog design process. While there are excellent EDA tools for each design step, the different analog blocks have different design methods, simulations are circuit, process, and application dependent, and layout is fully custom.

The below table summarizes the key differences between analog and digital design methods, and these differences are the reasons why analog design takes more time, is not easily scalable, and is exclusive compared to digital designs.

What makes a good analog IP? More specifically, what is needed to create a good analog IP?

First, we need to choose a good circuit architecture that is stable, robust, and suitable for mass production. Up-to-date PDKs (Process Development Kit) from foundries provide front-end (transistors, varactors, diodes, etc.) and back-end (resistors, capacitors, metals, etc.) models for simulation, various command files for DRC, LVS, and parasitic extraction.

PDKs nowadays from major foundries have very good correlation between model and physical silicon. A proper PDK installation and choosing the process option is all that needs to be done.

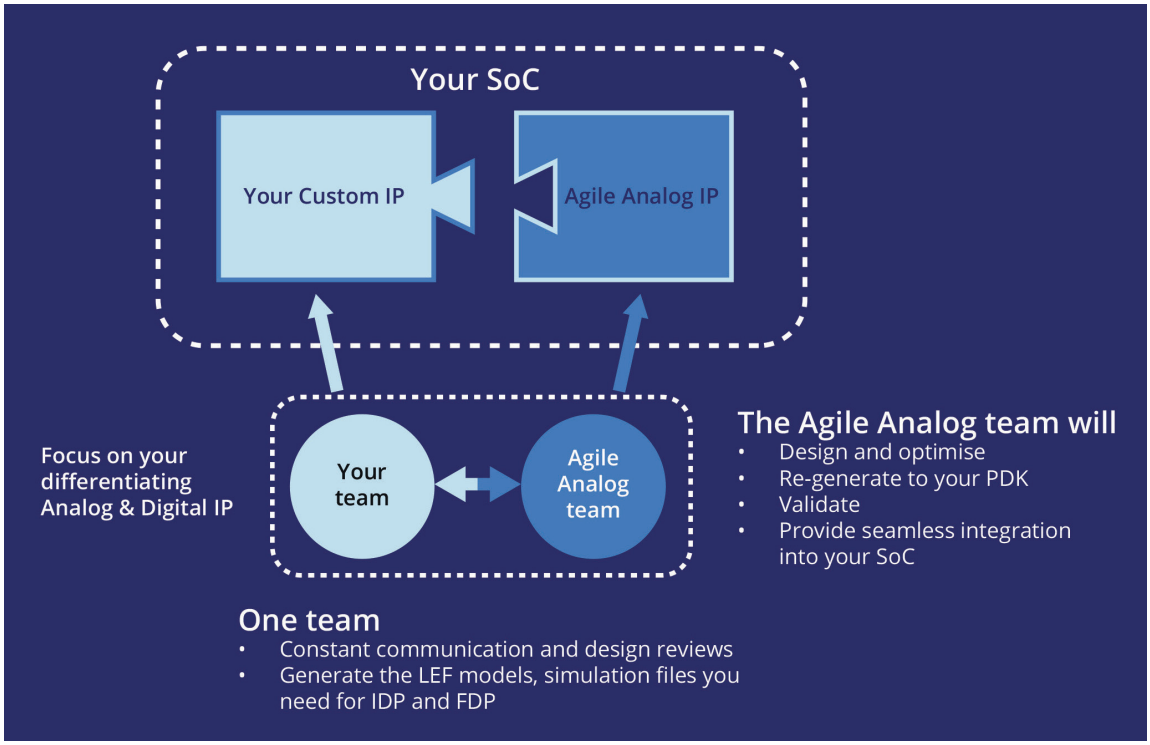
Thorough behavior simulation and detailed circuit simulations at the required PVT (process, voltage, and temperature) corners will assure that the circuit will operate as expected. Circuit layout requires knowledge of the circuit of design, knowledge of process effects to analog performance, and meticulous attention to the details of every single trace.

The work above requires a seasoned team of experienced circuit designers and layout engineers with multiple-domain knowledge. For example, an analog circuit designer needs to have a working knowledge of layout rules and placement guidelines as well as the main process effects to the circuit performance, and a layout engineer need be able to identify the key requirements for each trace, whether a trace is for power, general signal, or sensitive signal.

With a good circuit architecture, accurate PDK, thorough simulations, detailed layout and an experienced team to execute through the analog design flow, a high-quality analog IP will be delivered with minimum rounds of iterations through the design flow.

Good analog design teams are scarce and hard to come by and high-quality analog IPs are rare and are quite valuable in the market as well. This often leads to the question from IC design companies whether a particular analog IP is "silicon proven" or requiring an analog IP to be "silicon proven" to be qualified for use. Hence, we come to the fundamental questions -- "what is silicon proven?" and "is silicon-proven proof of IP quality?"

The general definition of a "silicon-proven" IP is an IP that has been manufactured on silicon and its functionality bench-test measured, hence



verified "on-silicon". Once an IP is "silicon-proven", it gains credibility that it will work as expected on a production chip, with the identical layout on the same process technology. However, such a silicon proof is only a single-point (or several points) validation of the design, usually based on pre-defined parameters and measured at specific voltage and temperature points; in other words, a "sample" of the IP's capabilities. Whether this "silicon proven" IP is "production quality" is determined before the manufacturing of this IP: the architecture chosen, the comprehensive simulations and design corners covered, the diligence put in the layout, and the effort in verification during development. In other words, an IP that is "silicon-proven" is merely a sanity check, only proving that the IP development flow "seems" to be "okay." This does not seem to be a sufficient proof of quality.

Some "silicon-proven" IPs are IPs extracted from production chips, or used by other licensees in successful production, which have endured real-world, high-volume tests under all sorts of conditions. These IPs certainly have credibility in its quality. However, these IPs are designed specifically for a particular product in a particular process node. For a project in a different node, process-porting is required thus nullifying its "silicon-proven" status. In the case where a new project is using the exact node as the silicon verified IP, the IP may not match your need in terms of performance or area. For example, the PMOS driving device consists of over 50% of the entire LDO area, a "silicon-proven" LDO is often over-designed for one's need, costing more silicon area than necessary. The dimensions are also fixed, so the other components need to fit the dimensions of the IP. Modifications to these silicon-proven IPs are possible, but the additional cost in money ($xxx k) and time (6 months to a year) for each instance is quite often too high to bear. Modifications also invalidates the "silicon-proven" status of the original IP.

Process choice, process option, design parameters over corners, functions are all factors determining the "silicon-proven" validity of the IP. Shown in table form, it is clear that "silicon-proven" is very rare in IP reuse.

In summary, "silicon-proven" IPs are tied to certain processes with defined performances and validated at specific points of the design parameters. They may not match one's need and modifications to the IPs most likely invalidate their "silicon-proven" statuses. The quality of an analog IP is still based on the criteria addressed in the previous section, namely: good architecture, accurate PDK, thorough simulations, experienced design team, and a rigorous design flow to connect all these qualities together. At Agile Analog, we have an experienced analog design team, with decades of experience

	Design Flow	Process	CAD Automation
Digital Design Flow	Linear	Fairly Independent	High
Analog Design Flow	Circular	Highly Independent	Low

➤ Table summarising the key differences between analog and digital design methods.

➤ Shown in table form, it is clear that "silicon-proven" is very rare in IP reuse.

Reuse Risk	Low → High					
Process Choice	Identical	Identical	Identical	Identical	Identical	Different
Process Options (e.g. metal stack)	Identical	Different	Identical	Identical	Different	Different
Design Parameters	Identical	Identical	Different	Identical	Different	Identical
Functions	Identical	Identical	Identical	Different	Different	Identical
Silicon Proven?	Yes	NO	NO	NO	NO	NO

➤ Agile Analog's ability to repeatedly generate fundamental IPs allows customers to focus their team and experts on their differentiating analog and mixed mode designs

with all sorts of analog and mixed-mode IPs. Our designers have designed and delivered analog IPs across standard CMOS processes, in both mature and advanced nodes, as well as specialty CMOS processes such as SOI and BCD processes.

In addition, Agile Analog's core technology is a "formal-flow" to the so-called "art" of analog circuit design. By applying software automation via rules-based AI to the generation of the IP and to the design flow, we are developing and delivering analog IPs in a revolutionary way. Our method not only defines the schematic, the "what" of the IP, but also the intent and the essence of the design, which is the "why" and the "how" an IP works. This allows us to develop and generate an IP in any process node, and the automated, comprehensive verification flow assures the performance and quality of the IP for every delivery.

Taking advantage of Agile Analog's IP generation engine, we can deliver analog IPs tailored to the specific needs of each customer. The specifications are "exactly to spec," optimized for area and performance. For the "front-end" portion of the project, Agile Analog's initial deliverables include behavior models for system simulations. The behavior models are process-independent, which means that analog IPs can be introduced early in the system design flow, allowing customers to plan and simulate the system including the analog IPs early in product development. For the "back-end" portion of the project, in the case of a PDK update from the foundry, regeneration or re-verification of the IP can be quickly done. It is also possible to evaluate IP performance across different process nodes or device options.

Fundamental analog IPs such as power management (PMU), sensors, and data processing (ADC & DAC) are essential blocks in every SoC, but, due to its repetitiveness, maturity in design and domain knowledge, these tasks are often mundane and unexciting to an analog expert. Agile Analog's ability to repeatedly generate these fundamental IPs allows customers to focus their team and experts on their differentiating analog and mixed mode designs, i.e., the "added-value" portion or "secret sauce" of their product. A customer's product lineup usually consists of several chips of varying features and configurations, which Agile Analog can sufficiently support by generating an assortment of analog IPs to meet each chip's specific requirements. In addition, Agile Analog can also generate IPs in any process node of customer's choice, as a customer migrates to newer process nodes, Agile Analog's IP delivery can follow customer's development roadmap. Our automation technology brings consistency to our IP generation and delivery across technologies.

Automation also applies to our quality checks, meaning less sensitive to human interference, and continuous improvement as new rules and features are added to our flow. Gone are the days of finding new analog IP vendors every time one migrates to a new technology node, Agile Analog can do it all.

Good architecture, thorough design and simulation, quality layout, and following a formal and automated design flow that ensure the above criteria are met at every step are the essential elements to developing high-quality analog IPs. Agile Analog's experienced design team and our IP generation engine assures that our deliverables will meet the quality and performance that our customers and the IC industry demands. Through our formal flow and automation, Agile Analog can deliver high quality analog IPs for all process nodes and optimized to customer's individual needs in a repeatable and timely manner.

Agile Analog's customer can kick-off a project with the assurance that the fundamental analog IPs are available and will meet the project's specifications, without the need to shop around. Our approach to analog IP development can grow and evolve along with the customer, either horizontally across the product line, or vertically to newer technologies and process nodes. Following the footsteps of the leaders in IC industry, Agile Analog is committed to bring success to our customers.

Many thanks to Pete Hutton, Mike Hulse, Robert McCubbin, and Graham Woods for their valuable comments and contributions to this paper.

The perfect partner for wet process equipment?

TOBIAS BAUSCH, CMO & CTO AT AP&S INTERNATIONAL, discusses with Philip Alsop, Silicon Semiconductor Editor, the company's batch processing, single wafer processing and support equipment technologies, with the emphasis very much on continuous innovation to deliver cost-saving, operationally-optimised and sustainable customer solutions. The conversation also covers some of the current industry challenges, including ongoing supply chain issues and skills shortages, as well as the opportunities offered by new and emerging markets.

PA: *The obvious place to start would be if you can give me a little bit of background on the company, the history and some of the key milestones.*

TB: The company itself, AP&S started in 2003, but the history starts in 1995. The current shareholder, Horst Hall, started the business in 1995. Then, from 2001 to 2003, we were part of the SEZ Group and we were called SEZ Germany. The batch part during this time was that SEZ Austria had a single wafer portfolio and in 2003, Alexandra (Laufer-Müller) and Horst, the current shareholders of the company, did a management buyout and founded the company AP&S. So, as I've tried to explain the history is much longer than 2003. Which means this year we have the 20 year anniversary. In July we celebrate this with the company employees and the partners. And yes, over the last 20 years we developed several tool platforms, mainly in the wet process sector. So all our machines are used in the wet departments of our customers. And during this time, sure, we have several milestones - we invested in an in-house lab where we can run demonstrations for customers, the demonstration lab starting in

2012. And as I said, over this time we have a lot of redesigns or redevelopments of machines, new developments of existing machines or new machines.

PA: *And it would be good then to move the actual technology solutions you provide. If you can run us through the batch processing solutions - one of your main sort of strengths?*

TB: We have the existing three platforms, it's the batch, the single wafer and the production supporting equipment or facility logistics as we call it. And the batch is this one where we've grown up. Since 2003 we're starting with the batch tools. We have there several platforms, semi-automated and fully automated platforms. The smallest platform is a two-tank solution where customers can have etching and the cleaning application in one equipment. And mostly this tool will be used by customers who coming from manual operations - where the operator handled the wafers manually and they want to go to some kind of automated production.

And the next platform is a tool which is called multi or giga step. It's a bridge tool. It was developed in the 2009-2010 years and we have the possibility to run in these platforms very easily, six and eight inch in a bridge combination without any kind of modification between the wafer sizes. So at the moment this will be very requested related to the Silicon Carbide issues and the Gallium Nitride request. And this tool platform itself is very modular and flexible.

So the customers could also decide by today to go with a tool configuration for a cleaning application and, in the future when their needs change, the product is changing or whatever, we could reconfigure easily, by adapting the modules or insert or disassemble modules or insert new models, the tool configuration. So that's one of the key benefits of this platform.

And then we have a high throughput platform, a new development - it's called Nexus Step. It's up to 12,000 wafs per day, mostly for cleaning applications. We run in this case with 100 wafer batch per load. And therefore we have this year within the year, by end of the year, let's say we will have the market launch of the Nexus Step, which is a new development. But I think we discuss later on about developments more in detail.

And last but not least is a very special tool. It's eless metalization equipment for underbump metalization, we call it Volcano. We start this development in 2009. And I think by today we are at most of the customers in Europe. The process of record for this eless metalization, where we can have nickel, palladium, gold metalization on copper or aluminium pads and, yeah, this tool platform was one of the biggest success stories in the history of AP&S. Our target is to have a clear enlargement of the bath lifetime, because the eless chemistries are quite expensive compared to standard chemicals in the semiconductor industry and we want to ensure that the customer can run on a higher throughput base on a better total cost of ownership.

PA: *We can perhaps go on to the single wave of processing technology - if you can just outline what it is you do in that area.*

TB: The single wafer equipment we developed in the early 2010-2011 years. And as I said, we also decide very fast to go with the single wafer in a demo application to show the customers the possibilities to run demonstrations. And in the meantime, we run not only demonstrations, we also run R&D activities in the lab.

The tool itself is a very small equipment. We can start with one chamber. It's called a single chamber. We could adapt it with a robotic module to have automated loading of the wafers or the masks and up to a double chamber. So, the biggest enlargement of the tool configurations are two chambers, a double chamber solution. But in the chamber itself, we are not limited. So, we could run up to twelve inch on the wafer base and up to nine inch on the mask size. And, during the development of the machine, we decided to give the machine the name of the processes. So, for example we have a spin mask which, as the name suggests, that's the equipment for the mask cleaning a spin lift off. It was designed for metal lift off applications or spin RCA spin scrubber for typical cleaning applications or spin metal or spin edge for etching applications.

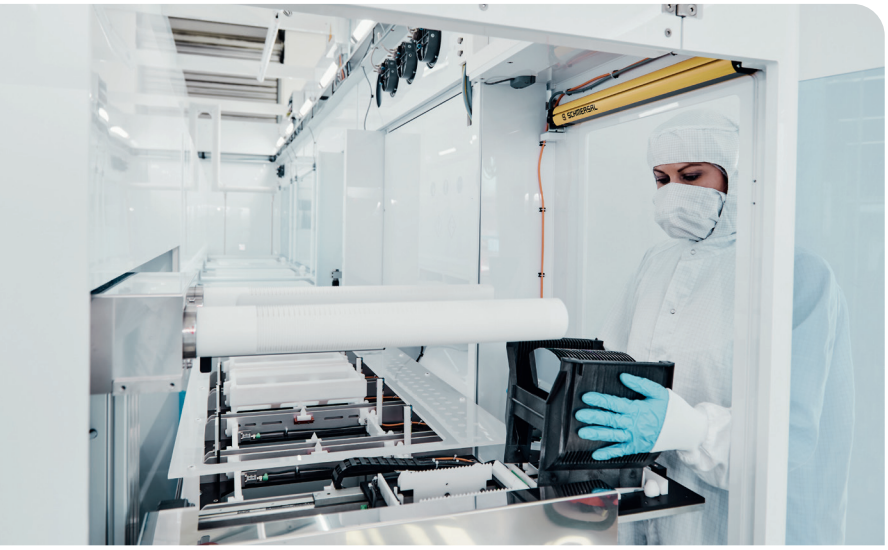
And each of them has specialties and different features related to the processes. For example, the spin metal, we developed for a metal etch application, an endpoint detection system which is included inside of the process chamber. And therefore we had in this case, one example we had developed with a customer realised for three metal layers, so they had a metal layer of silver, nickel and titanium. And with this endpoint detection we could realise a very fast step, very fast process steps. We can reduce clearly the undercut and the over etch and especially we can compensate any kind

of chemical concentrations, temperature variations in the chemistries, over the time of the chemistry usage, dilution or degradations. So, all these things were compensated even if we take a look on the etching endpoint. And this was, for example, one of the benefits we could include in these single wafer chambers. As I said, there are a variety of features related to each dedicated process step.

PA: *It sounds what you described there, that you collaborate quite closely with customers. So, I guess you produce what we call a standard range of equipment solutions, but then you will work with individual customers to customise them for their specific needs?*

TB: Especially single wafer or even on the batch. I forgot previously to mention that we also include in this demo centre four years ago a batch demonstration equipment. And this is what we see. So, as I said, we do a lot of R&D activities with the customers. So they come to us. They have a dedicated problem. Sometimes they could not solve it in their own facility, related to contamination issues because they are not allowed to run different tests on production equipment or at the moment, for sure they are all fully loaded, so they don't have the time to do a lot of R&D activities in their own production lines. And then they came to us with the wafers, with the issues and we do together the R&D activities in our lab, find the best set up, or even find a new set up with new features like ozone, like megasonic, supporting whatever. And then at the next step we try to implement it on the existing machine of our customer site. Or if for sure needed, we will develop a new machine for the customer itself and we build it. During the manufacturing phase we try and we go ahead in the lab to bring the process as close as possible to a production running parameter set up.

PA: *Okay. And you mentioned as well at the start that you make a range of support equipment. So again, it would be good to understand support equipment - what does that actually mean?*



TB: So, the supporting equipment or we change it to the new definition in the near future. Fab logistic equipment is the third pillar of our product portfolio. In this case it includes also cleaning equipment, but especially for carrier boxes, SMIFs and FOUPs in this case, or parts or tube cleaning equipment for parts made of quartz parts and chemical delivery systems. So, I think this is the basics. Every fabrication needed to run their production and especially on the carrier box or SMIF or FOUP cleaning, we see in the last years a very increasing demand for sure, the ramping of every customer is ongoing. And if you have more wafers in the facility or you're producing more wafers, you need more boxes. And these boxes have to be cleaned. Therefore it's clear that the customers need more cleaning equipment. Also we could generate and provide to the customers a clear benefit if they go back to in-house cleaning. In the industry in the last ten to 15 years, several of the customers don't want or don't do this in-house. So, they outsourced their boxes, their FOUPs, their SMIFs to external cleaning centres.

But, at the moment, we see the benefits bringing it back in-house. You have faster reaction time, you have a higher flexibility when you have to clean boxes or FOUPs immediately. You could reduce logistic costs, you don't have to send it out to an external provider, get it back and so on. You lower the number of parts which you have to have in the loop for the cleaning and at the end for sure, reduction of the cleaning cost, something which can be calculated and visualised. And I think what will be more important in the next years, the carbon footprint could be much better because you don't have to send parts on a longer logistic way to the external partner. As I said, you can reduce the logistic cost, but you also can improve your carbon footprint.

PA: *And in terms of the applications, I think you referenced the main ones. You're focused on a number of application areas, cleaning and etching would be the main ones. Were they there others as well? What are the focuses exactly?*

TB: Yeah, so these two are, I think the typical ones, which we are coming from and which the company history was grounded on - typically cleaning machines in the front end production for pre-diffusion cleans or post CMP cleans, whatever, on the etching equipment for the typical front end steps for oxide edge, nitride edge, silicon edge and so on. So, this is the basis where we found our tool base, where we found our process know how and so on and over the last year are several things coming add on. So, especially solvent applications was very important over the last years and I think AP&S was one of a few worldwide which include solvent applications in machines where we have a tool configuration in parallel also with acid steps or cleaning steps. So especially these things, solvents and so on. You have to know what you have to do related to the security issues and so

on. But that's one of the additional focuses and applications we do. The metal etch I explained previously on the single wafer, in the meantime where we had developed this single wafer metal etch with the endpoint we also go ahead and do this development on a batch platform.

It's on our multistep and gigastep tool platform to upgrade or enlarge the throughput capability on the batch tool. Everybody is clear on the batch tool. You will have a higher throughput application possibility compared to a single wafer. Both types of equipment have their benefits and pros and cons. But especially the metal etch was growing over the last year. And yeah, as I said previously, the eless metalization, this is one of the most popular applications we focus on at the moment. This is also coming for sure from the mega trends we have at the moment with the decarbonization, green energy, electrical cars, loading stations and so on. At the end everybody needs power devices. On the power devices you need a good metal stacks for the UBM, for the under bump metalization. And we see also here that these metal layers where we can realise with the eless process steps are very good in the terms of quality, temperature and so on for these new technologies here.

PA: *As you've been answering, you've alluded to a lot of the technology solutions and clearly some innovations along the way, but are you able to summarise some of the recent innovations or at least highlight some of the most important ones as far as you're concerned, what you've been developing recently?*

TB: I think I can summarise, let's say, three of the main innovations we do at the moment, or we have done in the last two years. We hve a very huge in-house software department. The company has 250 people, but the in-house software group is compared to this number, a huge group. And we do this with a clear strategy to have it in our own hands, to have the development of the software in our own hands, because we also see that software features, interfaces to customer interfaces, handling solutions and so on would be the key in the future. So, we speak about AI, we speak about predictive maintenance and so on. All these things are related at the end to a software feature so that the tool can control itself, measure itself, do the diagnostics itself to see if a part, even a pump, a heat or whatever is coming to a failure and so on. All these things are related in the software, in the software code and therefore we do there, let's say a lot of investigations and innovations.

Also what is clearly focused, but that's nothing new that's in the industry since it's been happening for quite a while, is the quest to increase and optimise the throughput of the machines so you can even lower the cost in the production - if you can optimise this throughput you can reduce process times, can save chemistry costs or in this case also it would be in term of a green footprint of the company a good feature to save chemistry volumes and costs. So, this is something we take account of in the software.

we do this with a clear strategy to have it in our own hands, to have the development of the software in our own hands, because we also see that software features, interfaces to customer interfaces, handling solutions and so on would be the key in the future

The second is the next step where we are in the development phase of actually building a new machine currently. This will be the machine especially designed also for a high throughput eight inch application. We will have inside of the machine a unit to stock up to 44 transport carrier or boxes. And it allows us to have a very flexible handling of it in terms of recipe control and throughput control. And it allows a customer also to stock carrier boxes and so on inside the equipment and can bring it to the equipment in a time when the time is available and we use it, we stock it and we give it back to the fab when the production or the recipe is finished. And this is a tool, as I said, with additional process features. We're reducing some process activities like for only one example, reduce the rinsing time to save time and to save also money and to save at the end DI water which also be good for the whole environment on the customer side.

And the third is our cleanser. It's the equipment we developed over the last two years. It's a new cleaning equipment for fab logistics and especially for cleaning off FOUP. The equipment is able to run twelve FOUPs per run. And we see that we have time or a recipe reduction from approximately ten minutes to benchmark equipment. So we also could increase here the process sequence and enlarge the throughput at the end. And this equipment is developed with the implementation of automated loading system. So, especially on high automated twelve inch fabrications, we see that the demand to load the machine not by an operator, so to load the machine by overhead transport system is also coming in the path cleaning area. And this is something we focus on. And the development of this fully automated loading system is ongoing. And I think we will come out with the market launch in the next one and a half years.

PA: *A lot of your success is clearly based on the people and the skills you have within your organisation. And I know you pride yourselves on*

your recruitment and skills development. It's very important to the company. So particularly, I guess at the moment where all sectors are maybe struggling a bit, but the technology sector, we constantly hear of skill shortages. So, what sort of initiatives do you have in terms of both identifying suitable people to join yourselves and also then once they're in the company, how do you help them to develop?

TB: Yeah, so in the south of Germany, when we are located close to the Swiss border and to Lake Constance, we have for a good location for employees. We have a lot of strong companies and all of these are looking for high qualified and good people. So, for the company itself, as you said, it's quite difficult to find the right people. We could say that in the last three years, during the pandemic situation on the R&D sector, we find very good people. I think there was the situation that a lot of people from the universities who were finished with their study were looking for new jobs and not everybody was hiring new people at that time. We decided decide early on that we would use this situation and get a lot of students into in the company. So, on the R&D sector we have a better situation compared to the manufacturing area. In the manufacturing area it's quite difficult to find the people to produce the machines and therefore I think it would be the biggest challenge over the next years to find there the right people and the people with the good skills and the right skills.

We also try to hire people who come from industries closer to the semiconductor industry, to the machine manufacturing industry. We have a lot of machine manufacturers around of us which are in the metal sector.

Internal study and training is one of the biggest things we do. So, we have in several departments, trainees and most of them, or let's say all of them, will be after their training time and after the study time, part of the AP&S team. We do this very carefully and I think we have at the end, if they are finished with their study, we have several options.

They could start in an R&D area or in sales or marketing, and if their technical skills are quite good, they also can start in the manufacturing sector.

PA: *Do you think the industry has more or less recovered from the impact of the pandemic? And if so, or whatever the current state is, what sort of opportunities are there, and are there still any sort of challenges off the back of it? Everyone's calling it where we are now?*

TB: Yeah, that's a difficult question because I think over the last three years nobody was able to say what happens next. So I think at the beginning, 2020, everybody was afraid and nobody know what's coming soon and then I think especially the semiconductor industry was at the mid tp end of 2020, very fast in a way and since this time everybody is growing and ramping up. If it's going back to normal, I don't know. At the moment we see that the parts we need out of our own industry, plc controller, motor controller, whatever, still have a lead time of 50 weeks, so approximately one year. On other parts we see the lead time was also in the past close to 52 weeks and they're going back to 44, 42. So there we see a reduction but especially on the electronic parts we doesn't see a clear reduction. Therefore, I don't know if we are back on a normal level. We see that the demand for semiconductors also relates to a higher demand of equipment, which was for us measurable in the order entry we have had over the last two or three years and for sure also this is also related to several megatrends.

We have the emobility, decarbonization trends and so on. And if you take a look at all this market research it seems to be that it's going on this way, especially the power industry, power semiconductors will grow more than others - but what is the new normal? I don't know.

I think at the moment, especially industries and ecosystems like Europe, like Germany, like other European countries. We see that the globalisation, which we have prior the pandemic was very good and great and it was not a problem to have a supply chain which is around the world. I think in the semiconductor industry the supply chain was typically around the world and it is clear for everybody. And then we have this pandemic situation and this crisis, and then everybody sees, okay, the supply chain was cut. And at the moment, for the European people, it's interesting and great to see that we have a lot of new projects. A lot of new, growing fabs, even internal, coming to Germany. Infineon decides to expand, TSMC, was in discussion to have a new fab in Germany or in Europe.

And I think it's great, but I don't know if this would be the first step to have towards the decentralisation - to the external production coming back to internal production on each continent. If we are back to

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a new normal. I don't know. I think we will have also a lot of movement in the market and let's see what happens in the next three years. So we had now three years Pandemic time and I think it takes minimum the same time to see what is the new normal.

PA: *Are you able to analyse what sustainability means for the industry and particularly the supply chain and anything around the sort of geopolitics as well?*

TB: In terms of geopolitics, I'm not a politician, so the geopolitics situation is quite difficult and two years ago nobody believed that we will have a war in Europe now we have it so what happens in the next three years? I think it's quite difficult to underline this.

It is important in the semi industry to have a strong network and also to know and have scenarios, backfall scenarios - what happens when such situations came or what happens when such situations don't come about.

On the sustainability view, the resources we have are not endless. So, if we take care about the materials if we take care about raw materials or especially on the employees and the technologies we have to find ways to improve what we do, so to handle the resources we have. Even if we speak about water, which I believe will happen in the next years, one of the most important resources around the world, I think it will be difficult in the next years around the world to have it in the right volume and in the right quality.

And our industry is one of the industries which need a lot of them. And I think this should be the target to focus on activities, to save these resources - raw materials, water, whatever. And this will be also the success in the future. These companies which find a way to handle these resources in a good way, which are going on a sustainability strategy will be successful.

PA: *Are you noticing that your customers are more interested in sustainability? When they're talking to you do they ask about your sustainability initiatives and your supply chain?*

TB: We're getting these questions more and more. We are part of several sustainability projects. Even if you have at the moment we have customers which have fabrications which are 20-25 years old, and for sure they will run these fabs for more than the next 20 or 25 years. They have clear communicated sustainability strategies. And for us, it's clear as a supplier of this industry to go ahead in these strategies, to find ideas and ways to come in close to the targets which the customers have and find our own way, our own ideas to fulfil this sustainability request from the customer sites.

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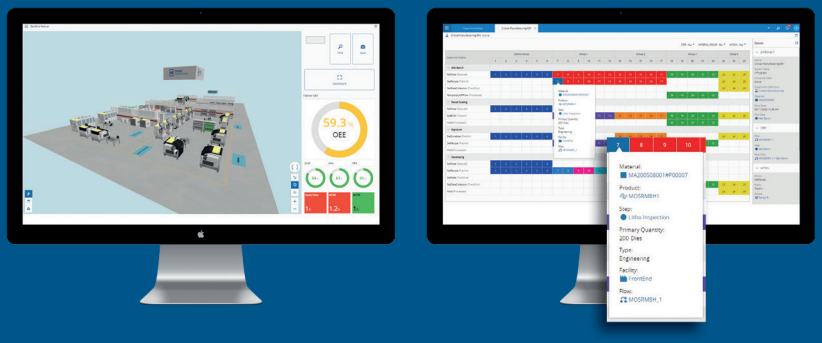

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