SILICON SEMICONDUCTOR

VOLUME 46 ISSUE II 2025

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

SILICONSEMICONDUCTOR.NET

EUROPE'S SEMICONDUCTOR INDUSTRY FOCUSES ON SUSTAINABLE GROWTH

EVG®

invent
innovate
implement

www.EVGroup.com

FUSION AND HYBRID BONDING FOR HETEROGENEOUS INTEGRATION

- Enabling advanced 3D device stacking and chiplet integration for CMOS image sensors, memory and 3D system-on-chip (SoC)
- High-volume production equipment and process technology for Wafer-to-Wafer (W2W) and Die-to-Wafer (D2W) hybrid bonding
- GEMINI® FB Automated Production Wafer Bonding System delivers industry leading alignment accuracy and bonding performance
- Heterogeneous Integration Competence Center™ serving as leading-edge innovation incubator for EVG customers and partners

GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com

VIEWPOINT

BY PHIL ALSOP
EDITOR

The race for resilience

WITH ELON MUSK at his side, one imagines that the US president is all too aware that the current focus on AI chips is nothing to do with his favourite fast-food choices, and everything to do with the ongoing geopolitical tension whereby China looms large over Taiwan. In a recent podcast, Musk spelt out the threat quite simply – if China were to invade Taiwan, the rest of the world would be cut off from advanced AI chips, as 100% of advanced AI chips are currently made in Taiwan.

With my storage and data centre hats on, where resilience and business continuity and disaster recovery (BC/DR) plans are so crucial, I might ask how such a situation has been allowed to occur within the semiconductor industry. Hindsight is a wonderful thing of course. Until fairly recently, the concentration of AI chip manufacturing in Taiwan made complete commercial sense. Ah, but even then, did no one even think of the risks of concentrating this manufacturing activity in one location?

In the storage and data centre industries, offsite backups, mirroring, disaster recovery sites and the like are all taken for granted. Even more so, as cybersecurity threats have heightened the awareness of the imperative of cyber resilience. Of course, every organisation makes its own decisions around the cost of such resilience – hence BC/DR plans can vary greatly – with the main decision being the relative cost of protecting crucial business assets (data, infrastructure etc.) versus the possible cost of doing nothing – anything from minor disruption through to the business shutting down.

For the semiconductor industry, the billions involved in building and operating fabs means that the idea of having some empty fabs in a different geographical location sitting idle against the day when they might be needed is a non-starter. Nevertheless, the 'putting all of your eggs in one basket' approach that seems to have been adopted when it comes to AI chips was maybe less smart than it might once have appeared.

To use another cliché – there's no use crying over spilt milk. As the business folks like to say: 'We are where we are'. Hence, not before time, countries and regions far away from Taiwan are looking to ensure that some level of resilience is now being built into the semiconductor supply chain, from the construction of new fabs onwards.

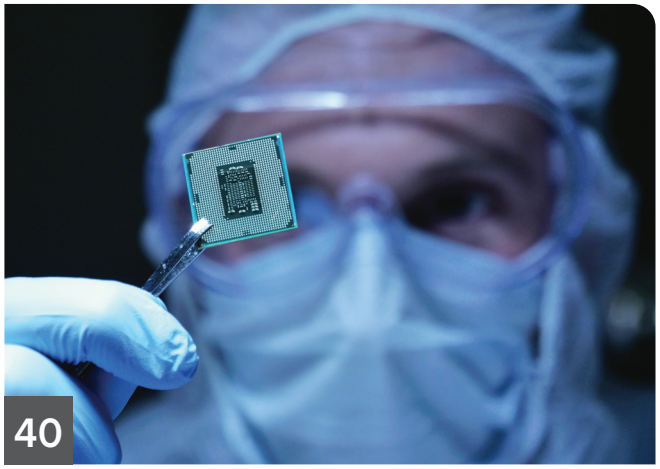
Regrettably, what has yet to play out is just how local and insular these supply chains need to be. Not only do we have the uncertainty over Taiwan's future, but we are also faced with an absence of any certainties when it comes to whether or not the rest of the world can continue to operate as one unified, all be it competitive, supply chain, or whether geopolitics will mean further fragmentation is likely.

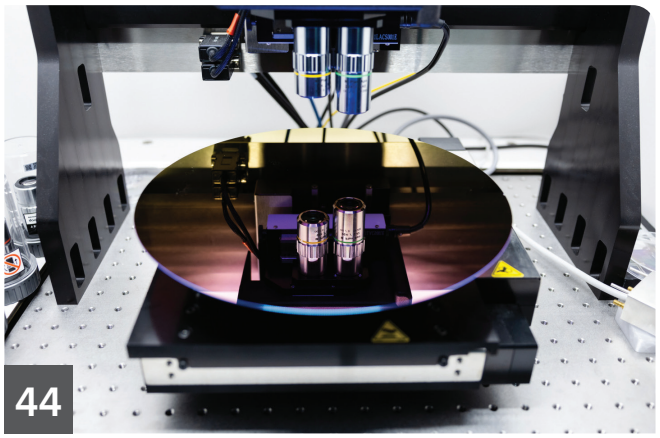
Historically, there's always been a balance to be struck between the success of individual country economies and more collaborative, mutual economic success across multiple countries and regions. It will be fascinating to see how such different points of view do, or do not, impact the semiconductor industry into the future.

CONTENTS

VOL 46 ISSUE II 2025

SILICON SEMICONDUCTOR





NEWS

Publisher Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Editor Phil Alsop phil.alsop@angelbc.com
Sales & Marketing Manager Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215
Marketing & Logistics Executive Eve O'Sullivan eve.osullivan@angelbc.com +44 (0)2476 823123
USA Representatives Tom Brun Brun Media tbrun@brunmedia.com +001 724 539-2404
Janice Jenkins jjenkins@brunmedia.com +001 724-929-3550
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214

Chief Executive Officer Sukhi Bhadal sukhi.bhadal@angelbc.com +44 (0)2476 718970
Chief Technical Officer Scott Adams scott.adams@angelbc.com +44 (0)2476 718970
Directors Jackie Cannon, Sharon Cowley

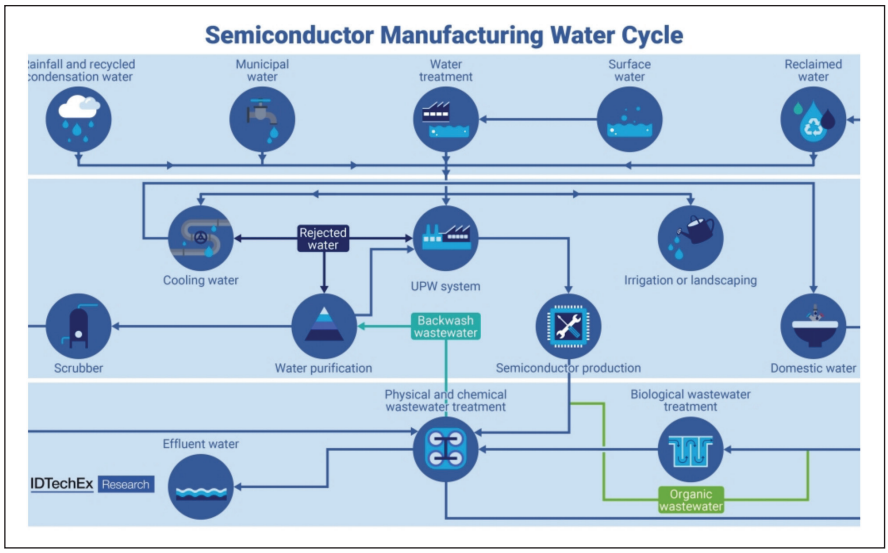
Published by Angel Business Communications Ltd,
6 Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970 E: info@angelbc.com

Printed by: The Manson Group. ISSN 2050-7798 (Print) ISSN 2050-7801 (Online) © Copyright 2024.

Water usage in semiconductor manufacturing to double by 2035

Not only does semiconductor manufacturing require large volumes of energy, chemicals, and silicon wafers, it also requires vast volumes of water.

IDTECHEX'S latest report, *"Sustainable Electronics and Semiconductor Manufacturing 2025-2035: Players, Markets, Forecasts"*, (courtesy of Thomas Bithell, Technology Analyst at IDTechEx) forecasts water usage across semiconductor manufacturing to double by 2035, as demand for integrated circuits continues to rise. In 2023 alone, semiconductor giant TSMC reported consumption of a staggering 101 million m3 of water, highlighting the scale of thirst in this fast-growing sector.



Furthermore, as node technology advances, so do the number of manufacturing process steps, and the usage of single wafer tools instead of batch tools, making the task of reducing water usage both challenging and even more critical. With many semiconductor fabs located in areas of high-water scarcity, such as Taiwan and Arizona, it is vital that semiconductor manufacturers take action to mitigate this huge consumption as part of the wider search for sustainable electronics. Water management for semiconductor manufacturers is complex, propagated by the extreme purity requirements for the water used in manufacturing, giving it the name Ultra-Pure Water (UPW). However, water management techniques being implemented have the potential to mitigate water scarcity fears whilst also reducing operational costs.

Increasing volumes of reused water

Most semiconductor manufacturers now recycle or reuse water in some capacity, with annual targets to increase current levels of water reuse and combat increasing water withdrawal rates. Many companies such as NXP, Onsemi, and TI now reuse wastewater in their cooling towers. Reprocessing wastewater back into UPW is more difficult, but implementing new water treatment systems will be necessary to achieve sustainability in water use in semiconductor manufacturing. SK Hynix increased its volume of reused water by 51% between 2020 and 2023, partly motivated by water stress classification of 3 fabs as 'High' or 'Medium-high'. This is expected to also reduce operational costs through reduced municipal water consumption.

Efficiency of water use

Process optimization can also reduce water usage. Many semiconductor manufacturers have cited a reduction in water per wafer as a key target for sustainability and to negate the risk of water shortages. This has been an issue for some, as the increased demand and complexity of wafers required has increased water use per wafer for companies such as SMIC. Reducing consumption per wafer becomes increasingly difficult with advancing node technologies, which often require increasing numbers of process steps.

However, simply reducing rinse times can result in large savings. GlobalFoundries reduced their rinse time from 10 minutes to 5 minutes after etching, resulting in an annual water saving of 10,000 m^3, and there are many more examples in the report.

Diversification of water sources

Negation of water scarcity risk can come through diversification of water sources. Installing facilities such as rainwater collection may reduce operational costs due to a decreased requirement for municipal water.

Tower Semiconductor has utilized the dehumidification of air required for the dry indoor environment in their factory in Texas. SMIC have also utilized condensate from air conditioning alongside rainwater collection to reduce municipal water consumption and associated costs.

These techniques may only recover a small fraction of total water usage but could still be invaluable. Larger usage could be obtained from seawater, with desalination employed in the Hsinchu TSMC plant. Where fabs are located close to the coast, utilization of onsite desalination could solve many fears surrounding sustainable water usage, although this would require high energy consumption.

3D Semiconductor packaging market to reach US$ 43.6 billion by 2034

According to Fact.MR, a market research and competitive intelligence provider, the 3D Semiconductor Packaging Market is valued at US$ 10 billion in 2024 and is expected to grow at a CAGR of 15.9% during the forecast period of (2024 to 2034).

PRESENT market trends show that the rising demand for compact, quicker, and more efficient electronic devices drives the expansion of 3D semiconductor packaging. This technology stacks and integrates multiple chips in one package to enhance performance while reducing latency and power consumption. Fan-out wafer-level packaging development and through-silicon via are also aiding in delivering high performance interconnects and signal integrity. As the semiconductor industry proceeds with development, 3D packaging has become one of the major enablers for innovating autonomous driving, 5G connectivity, and next-generation consumer electronics that are further driving market growth.

Key takeaways from 3D semiconductor packaging market study

The global 3D semiconductor packaging market is projected to grow at 15.9% CAGR and reach US$ 43.6 billion by 2034 The market created an absolute $ opportunity of US$ 33.6 billion growing at a CAGR of 15.9% between 2024 to 2034.

North America is a prominent region that is estimated to hold a market share of 30.5% in 2034. Predominating market players include TSMC (Taiwan Semiconductor Manufacturing Company), Amkor Technology, GlobalFoundries, Infineon Technologies, Qualcomm Incorporated, among others. Through-Silicon Via (TSV) under technology are estimated to grow at a CAGR of 16.9% creating an absolute $ opportunity of US$ 7.9 billion between 2024 and 2034. North America and East Asia are expected to create an absolute $ opportunity of US$ 29.5 billion collectively.

“North America and Asia Will Drive The 3D Semiconductor Packaging Market Due To Strong Demand from Technology, Automotive and AI-Driven Sectors” says Fact.MR analyst.

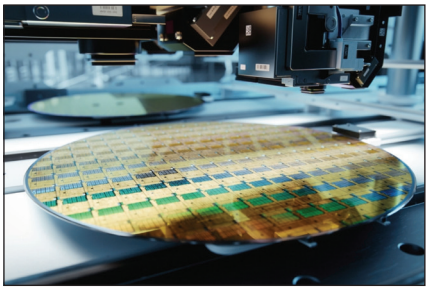
Leading players driving innovation in the 3D semiconductor packaging market

The Key Players in the Infant 3D Semiconductor Packaging Industry include Amkor Technology; ASE Group (Advanced Semiconductor Engineering); Broadcom Inc.; GlobalFoundries; Infineon Technologies; Intel Corporation; Jiangsu Changjiang Electronics Technology Co.; Lattice Semiconductor Corporation; Marvell Technology Group; Micron Technology; NXP Semiconductors; ON Semiconductor; Qualcomm Incorporated; Renesas Electronics Corporation; Samsung Electronics; Siliconware Precision Industries Co., Ltd. (SPIL); Sony Corporation; STMicroelectronics; Texas Instruments; TSMC (Taiwan Semiconductor Manufacturing Company); Other Market Players.

Country-wise insights:

Why is the US one of North America’s top markets for 3D semiconductor packaging?

The US market is expected to reach US$2 billion in 2024 and grow at a compound annual growth rate (CAGR) of 16% until 2034. From 2024 to 2034, this market is expected to create an absolute potential worth US$6.7 billion. Advanced electronic equipment, like as sensors, artificial intelligence (AI) processors, and potent computers, are essential to an autonomous car and require tiny, high-performance chips. Multiple chips can be stacked vertically thanks to 3D semiconductor packaging, which boosts processing power while taking up less physical space in these devices. 3D packaging is essential for integrating many functionalities, increasing energy efficiency, and



speeding up data transfer rates as AV technology advances and demands smaller sizes and more processing power.

This partnership between 3D semiconductor packaging and autonomous vehicle integration strengthens the US market’s position as a leader by meeting the growing demand for reliable yet small solutions that are necessary for cutting-edge autonomous driving advancements.

What is the current state of demand in China for 3D semiconductor packaging?

At a compound annual growth rate (CAGR) of 16.2%, the Chinese market is projected to reach US$ 11.4 billion in 2034. From 2024 to 2034, this market is expected to create an absolute potential worth US$ 8.9 billion.

China’s rapid adoption of 5G technology and drive to provide ultra-fast internet connections are driving increasing demand for 3D semiconductor packaging in the nation. Building up 5G networks is part of this expansion of digital infrastructure, and China has been actively working to meet the demand for faster data rates and more processing power with the use of 3D semiconductor packaging.

As cloud computing, smart cities, and the Internet of Things become more integrated, 3D packaging helps data-intensive applications that require low latency and high-speed communication.

Commission approves €920 million German State aid measure to support Infineon

The European Commission has approved, under EU State aid rules, a €920 million German aid measure for the construction of a new semiconductor manufacturing plant in Dresden.

THE MEASURE will allow Infineon to complete the MEGAFAB-DD project which will be able to produce a wide range of different types of chips. This new manufacturing plant will bring flexible production capacity to the EU and thereby strengthen Europe's security of supply, resilience and technological autonomy in semiconductor technologies, in line with the objectives set out in the European Chips Act Communication and the Political Guidelines for the European Commission 2024-2029.

The German measure

Germany notified the Commission of its plan to support Infineon's project to set up a new semiconductor manufacturing facility in Dresden, Germany. The plant will produce two technology families: (i) discrete power technologies used for power switching, management and control in electronic systems, and (ii) analog/mixed-signal integrated circuits that are crucial for bridging the gap between the analog and digital worlds. The produced semiconductors will be used in industrial, automotive and consumer applications.

The new facility will be the first one in Europe that will be able to rapidly switch its production between the two technology families while maintaining its high output capacity. It will be a front-end facility, covering wafer processing, testing and separation. The plant will reach its full capacity in 2031.

The aid will take the form of a direct grant of up to €920 million to Infineon to support its investment amounting to €3.5 billion. Under the measure, Infineon agreed to:

ensure that the project will bring wider positive effects to the EU semiconductor value chain;
invest in the research and development of the next generation of chips in Europe;
contribute to crisis preparedness by committing to implement priority-rated orders in the case of a supply shortage in line with the European Chips Act Regulation; and
provide access to its new facility to SMEs and research organisations for testing and prototyping.

The Commission assessment

The Commission assessed the German measure under EU State aid rules, in particular Article 107(3)(c) of the Treaty on the Functioning of the EU ('TFEU'), which enables Member States to grant aid to facilitate the development of certain economic activities subject to certain conditions, and based on the principles set out in the European Chips Act Communication.

The Commission found that:
The measure facilitates the development of certain economic activities, by enabling the establishment of a new semiconductor manufacturing facility in Europe.

The facility is a first-of-a-kind in Europe, as there is currently no semiconductor manufacturing facility that would be able to flexibly change its output between discrete power and analog-mixed signal technologies in a comparable manner.

The aid has an 'incentive effect', as the beneficiary would not carry out this investment in Europe without public support. The measure has a limited impact on competition and trade within the EU. The measure is necessary and appropriate to ensure the resilience of Europe's semiconductor supply chain. In addition, the aid is proportionate and limited to the minimum necessary based on a proven funding gap (i.e. the aid amount necessary to attract the investment that otherwise would not take place in Europe). Infineon has agreed to share with Germany potential additional profits going beyond current expectations.

The measure has wider positive effects for the European semiconductor ecosystem and contributes to strengthening Europe's security of supply. The Commission also took note that Infineon will apply to be recognised as an integrated production facility under the EU Chips Act Regulation and will comply with all obligations linked to this status. On this basis, the Commission approved the German measure under EU State aid rules.

EU funding boosts Europe's semiconductor production

The Public Authorities Board of the Chips Joint Undertaking (EU Chips Act) has awarded funding to the APECS pilot line project.

THE PROJECT is part of a major effort to develop European semiconductor production. The project focuses on developing and providing new packaging and integration solutions for the industry. VTT is also involved in the following pilot line projects aiming at semiconductor production: FAMES, NanoIC and PIXEurope.

The APECS (Advanced Packaging and Heterogeneous Integration for Electronic Components and Systems) pilot line, as part of the EU Chips Act programme, will promote European semiconductor manufacturing capability and chip innovation. The pilot line will focus on the development of reliable packaging solutions for microchips and innovative combinations of semiconductor materials and technologies, as well as chiplet integration. As its name suggests, the APECS pilot line will provide technologies to help others develop technology and innovation and will be coordinated by Fraunhofer.

"In the APECS project, VTT will focus in particular on the radio frequency technologies required for the 6G network and on the development and demonstration of optical microsystems and chip packaging methods," says Tauno Vähä-Heikkilä, Vice President, Microelectronics and Quantum Technologies at VTT.

VTT is involved in other European pilot projects: The FAMES and NanoIC pilot lines are run by CEA-Leti of France and imec of Belgium. In October, we published news about our collaboration on the EU-funded CEA-Let and imec FAMES and NanoIC pilot projects. Through the pilot lines, Finland is strongly involved in the European semiconductor ecosystem. The pilot lines provide services to companies to develop products and scale them up for production. Technologies under development include the latest transistor and RF technologies, new memory technologies and packaging technologies.

VTT's activities in the European APECS, FAMES and NanoIC pilot lines will be located in Kvanttinova for which the Finnish government has granted EUR 79 million in funding to build shared pilot lines. Kvanttinova is an RDI Hub in microelectronics and quantum technology, jointly developed by VTT, Aalto University and the City of Espoo.

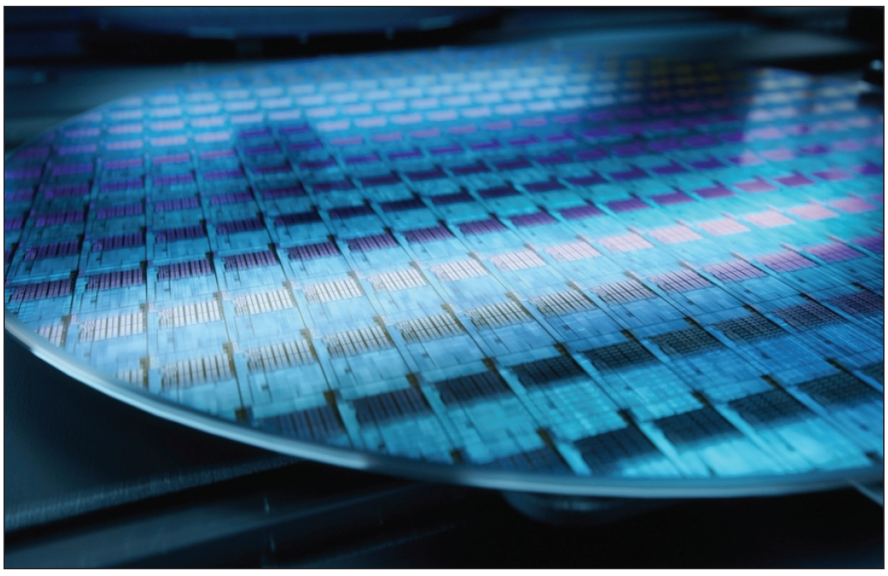
VTT's shared-use cleanroom enables domestic companies to develop and pilot microelectronics components, systems and innovation and scale them up for production. The first semiconductor processes in Finland will start up towards the end of 2026.

Furthermore, the European Commission has announced the creation of PIXEurope, a new pilot line for photonic chips. It is coordinated by ICFO, the Institute of Photonic Sciences in Barcelona. VTT is among the participants of the PIXEurope consortium. Financial and technical negotiations are currently underway. VTT develops low-loss thick-SOI integrated photonics for the pilot line's offering.

The EUR 29 million funding from the EU and the Finnish government for the APECS pilot line will focus on VTT's shared-use cleanroom facilities and the development of semiconductor manufacturing processes.

"Taken together, these four pilot lines, APECS, FAMES, NanoIC and PIXEurope, will support the growth of the Finnish and European semiconductor industry and help Finnish industry to connect to European value chains," says VTT's Research Manager Pekka Pursula.

The recent funding decisions made through the Chips Act and the equipment acquisitions enabled by them will support the strong areas of expertise of the Finnish semiconductor industry, in particular new materials, ALD technology for memory applications and RF technology.



Worldwide semiconductor revenue grew 18% in 2024

Worldwide semiconductor revenue in 2024 totalled $626 billion, an increase of 18.1% from 2024, according to preliminary results by Gartner, Inc. Revenue is projected to total $705 billion in 2025.

"GRAPHICS PROCESSING units (GPUs) and AI processors used in data centre applications (servers and accelerator cards) were the key drivers for the chip sector in 2024," said George Brocklehurst, VP Analyst at Gartner. "The rising demand for AI and generative AI (GenAI) workloads led data centres to become the second-largest market for semiconductors in 2024, behind smartphones. Data centre semiconductor revenue totalled $112 billion in 2024, up from $64.8 billion in 2023."

The positive performance of the overall market impacted the ranking of several semiconductor vendors. Eleven vendors experienced double-digit growth and only 8 of the top 25 semiconductor vendors posted revenue decline in 2024.

Samsung Electronics Regained No. 1 Spot in 2024

With 9 out of the top 10 semiconductor vendors recording revenue growth in 2024, the ranking of the top 10 semiconductor vendors changed year-over-year.

Samsung Electronics reclaimed the No.1 spot from Intel and extended its lead over the company in 2024 driven by a strong rebound in memory device prices. Samsung Electronics revenue totalled $66.5 billion in 2024.

Intel moved to the No. 2 position as its product set — AI PCs and the Core Ultra chipset — was insufficient to offset the limited success of its AI accelerator offering and the modest growth in its x86 business. Intel's semiconductor revenue was flat at 0.1% growth in 2024.

Nvidia continued to perform exceptionally well, increasing its semiconductor revenue by 84% in 2024, to total $46 billion. It moved up two spots to secure the No. 3 position thanks to the strength of its AI business.

HBM to Represent 19.2% of DRAM Revenue in 2025, Up from 13.6% in 2024

Memory revenue recorded 71.8% revenue growth in 2024. Memory's share as a percentage of total semiconductor sales increased to 25.2% in 2024. DRAM revenue improved 75.4% in 2024 while NAND revenue increased 75.7% year-over-year. High-bandwidth memory (HBM) production contributed significantly to the revenue for DRAM vendors. HBM revenue represented 13.6% of total DRAM revenue in 2024.

NVIDIA continues to dominate the global semiconductor sector

Brand Finance data reveals strong growth for world's top semiconductor companies despite ongoing supply chain challenges and geopolitical tensions.

NVIDIA has retained its position as the world's most valuable semiconductor brand, according to a new report from Brand Finance, the world's leading brand valuation consultancy. With a 98% increase in brand value to USD87.9 billion, NVIDIA's brand value is now more than two and a half times that of TSMC, the second-most valuable brand in the sector.

This growth propelled NVIDIA into the top 10 most valuable global brands list for the first time since it was valued in 2014, when it ranked 424th in the US 500. Last year, NVIDIA was the fastest growing brand in the world.

With a Brand Strength Index (BSI) score of 88.9 out of 100, NVIDIA has also become the world's strongest semiconductor brand in 2025. This puts NVIDIA more than seven points ahead of Intel, whose BSI now stands at 81.4 out of 100 – a notable shift from Intel's former position as the sector's strongest brand in 2024.

Lorenzo Coruzzi, Valuation Director at Brand Finance, commented, "Artificial intelligence remains a hotbed of controversy, investment, and innovation, drawing significant interest from VCs and big tech firms.

This AI-driven momentum continues to bolster semiconductor brand equity, with Brand Finance research confirming NVIDIA's dominance. Brand Finance data also highlights NVIDIA's strong 'positive contribution' score, reflecting widespread consumer trust and a strong market reputation. This enduring brand strength not only cements NVIDIA's leadership in the semiconductor industry but also positions it for sustained growth in an increasingly competitive market.

Looking ahead, a key question for the industry is sustainability—whether brands can maintain their value over time amid rapid advancements, including the recent launch of Deepseek."

NVIDIA CEO Jensen Huang also retains his position as the third-ranked CEO globally in the 2025 Brand Guardianship Index, securing the top spot in the semiconductor sector. Under Huang's visionary leadership, NVIDIA has not only advanced in AI but has also made significant strides in digital biology, climate science, autonomous vehicles, and robotics—sectors poised to reshape the future. According to Brand Finance data, Huang excels in familiarity, reputation, and is also recognised for his exceptional 'strategy and vision.'

The Brand Finance Semiconductors 2025 ranking has expanded from 20 to 30 brands, reflecting the intensifying competition and rising influence of emerging players in the semiconductor industry, particularly in Europe. This expansion highlights the sector's dynamic evolution, with new entrants such as UK-based Arm (brand value USD1.5 billion) and Dutch brand ASM (brand value USD837 million) making their mark.

"Artificial intelligence remains a hotbed of controversy, investment, and innovation, drawing significant interest from VCs and big tech firms. This AI-driven momentum continues to bolster semiconductor brand equity, with Brand Finance research confirming NVIDIA's dominance"

ASML and imec sign strategic partnership agreement

ASML Holding N.V. and imec have signed a new strategic partnership agreement, focusing on research and sustainability.

THE AGREEMENT has a duration of five years and aims to deliver valuable solutions in two areas by bringing together ASML's and imec's respective knowledge and expertise. First, to develop solutions that advance the semiconductor industry and second, to develop initiatives focused on sustainable innovation.

The collaboration incorporates ASML's whole product portfolio, with a focus on developing high-end nodes, using ASML systems including 0.55 NA EUV, 0.33 NA EUV, DUV immersion, YieldStar optical metrology and HMI single- and multi-beam technologies. These tools will be installed in imec's state-of-the-art pilot line and incorporated in the EU- and Flemish-funded NanoIC pilot line, providing the most advanced infrastructure for sub-2nm R&D to the international semiconductor ecosystem. Focus areas for R&D will also include silicon photonics, memory and advanced packaging, offering full stack innovation for future semiconductor-based AI applications in diverse markets.

A new area in the collaboration consists of a significant contribution to fund innovative ideas and activities in imec's research funnel that bring environmental and societal benefits. ASML's president and CEO Christophe Fouquet comments: "This agreement marks the next step in the longstanding co-operation between ASML and imec. It signals our joint ambitions to develop solutions for the semiconductor industry and fits our strategy of investing in technology and innovation that will benefit society at large."

"We are excited to continue our longstanding unique partnership with ASML, offering the industry access to the most advanced patterning solutions for over 30 years," states Luc Van den

hove, President and CEO at imec, "The inclusion of ASML's full product portfolio will allow us to expand and further mature the capabilities of our pilot line, providing the entire semiconductor ecosystem with the most advanced R&D to tackle the challenges of AI-driven technological advancements. Since imec has a strong focus on sustainable innovation, having this explicitly included in our partnership is a great addition."

The ASML investment in the partnership is complemented with funding made available by the Chips Joint Undertaking and the Flemish government (for the realization of the EU Chips Act NanoIC pilot line), and by the Dutch government (as an Important Project of Common European Interest). The acquisition and operation of the NanoIC pilot line are jointly funded by the Chips Joint Undertaking, through the European Union's Digital Europe (101183266) and Horizon Europe programs (101183277), as well as by the participating states Belgium (Flanders), France, Germany, Finland, Ireland and Romania. For more information, visit nanoic-project.eu.

Making 0.55 NA technology available at imec was part of the Next Gen-7A project (IPCEI22201) funded by the Dutch government as an Important Project for Common European Interest (IPCEI).

> "The inclusion of ASML's full product portfolio will allow us to expand and further mature the capabilities of our pilot line, providing the entire semiconductor ecosystem with the most advanced R&D to tackle the challenges of AI-driven technological advancements. Since imec has a strong focus on sustainable innovation"

Don't carry defects through your processes.

Find systematic yield issues fabulously fast.

With our new smart 3D X-ray solution for the fab.

comet yxlon

yxlon.comet.tech

Smarter by design: how AI is reshaping manufacturing in 2025

AI is at the heart of the manufacturing revolution, driving efficiency, sustainability, and precision as we head into 2025.

BY DIGANT SHAH, CHIEF REVENUE OFFICER (CRO) BOSCH SDS

ACCORDING TO a recent PwC report, AI adoption in manufacturing is expected to contribute $4.6 trillion to the global economy by 2030, illustrating its huge potential. As CES 2025 prepares to spotlight the latest AI innovations, it's clear that AI-driven tools like robotics, predictive analytics, and digital twins are no longer optional but essential ingredients to the industry's future.

But integrating the technology isn't without its hurdles. AI-powered solutions that tackle critical challenges - from minimising waste to optimising energy consumption and enhancing decision-making - require significant levels of operationalisation to achieve their goals.

AI on the assembly line

The manufacturing sector is witnessing a revolution on the factory floor, driven by the integration of AI and robotics.

A McKinsey study highlights that AI can boost manufacturing productivity by up to 20% by improving processes and reducing downtime. Predictive maintenance plays a pivotal role here. By analysing real-time machine data, AI tools can anticipate equipment failures before they occur, enabling proactive repairs that save both time and money while keeping production lines running smoothly.

It's no surprise, then, that the impact of robotics automation is accelerating. The market is projected to grow at a 10% compound annual growth rate (CAGR) through 2025.

Assembly lines, once defined by manual labour, are one area in particular which is benefiting from the precision and efficiency of AI-powered robotics. These advancements are not only boosting speed and accuracy but also reducing the likelihood of costly errors.

As these technologies advance, assembly lines are evolving into centres of innovation, setting new benchmarks for precision, speed, and competitiveness in production. But they're not the only area in which innovation is accelerating.

AI & Digital twins – doubling down on smarter decisions

Digital twins—digital replicas of physical

objects—are experiencing rapid adoption. In the manufacturing sector, 89% of organisations adopting digital twin technology have done so within the past two years, with 19% adopting it within the past six months.

Digital twins are being used to simulate and optimise factory workflows in real time, allowing manufacturers to test scenarios and refine operations before implementing changes on the ground. AI-based data analysis has also helped reduce cycle times during production ramp-ups by 15%, while new algorithms have streamlined component-testing processes, significantly enhancing efficiency. These advancements demonstrate how AI models and digital twins mirroring production lines can reduce energy usage and enhance production outputs without overextending resources.

By combining advanced simulations with real-time insights, digital twins are not only improving operational performance but also laying the groundwork for more sustainable manufacturing practices.

Efficiency meets responsibility

Sustainability remains a key priority for manufacturers, with the industry responsible for one-fifth of the world's carbon emissions.

AI can help manufacturers track and optimise energy consumption across every area of operation. By identifying inefficiencies and suggesting AI-driven adjustments, manufacturers can significantly cut emissions and costs.

Supply chain sustainability is another huge focus area. AI-powered tools enable predictive inventory management, reducing overproduction and minimising waste. A recent Capgemini report found that AI could cut supply chain emissions by 5-10%, in line with growing corporate ESG commitments.

As such, AI is enabling manufacturers to create leaner, greener supply chains, reducing waste and helping meet ambitious ESG targets without compromising operational performance.

Filling the (skills) gap

It's no secret that the manufacturing sector faces a widening skills gap, with over 2.1 million jobs expected to go unfilled by 2030, according to Deloitte. This shortfall not only threatens productivity but also risks slowing innovation in an industry that is rapidly evolving with the adoption of advanced technologies.

One solution lies in leveraging AI-enabled workforce strategies. By automating repetitive or routine tasks, manufacturers can free up human workers to focus on more complex, value-added roles. Beyond automation, AI also supports upskilling initiatives, helping employees adapt to new technologies and work collaboratively with AI systems. This dual approach empowers workers, enhances efficiency, and builds a future-ready workforce.

Keeping AI in check

Ethical AI implementation is equally critical to manufacturing's future. Transparency, privacy, and worker safety must remain at the core of any AI strategy.

Crucially, the building blocks for Ethical AI in manufacturing hinges on five key things. Transparency, fairness, privacy, accountability and human oversight. Bosch SDS prioritises these principles, ensuring AI adoption respects ethical standards and aligns with initiatives like the World Economic Forum's advocacy for "ethical AI governance."

We use our Sure.AI framework, which merges AI innovation with ethical governance standards. We also use Computer Vision based solutions to ensure worker safety and these algorithms are tested continuously to ensure that there are no biases developed over time. Such efforts not only mitigate potential risks but also build trust among employees and stakeholders, fostering greater acceptance of AI in manufacturing.

AI: the blueprint for smarter manufacturing

To begin integrating AI and driving smarter, more sustainable operations, manufacturers should launch small pilot projects to test their solutions before scaling up. Investing in employee training also ensures teams are equipped to collaborate effectively with AI systems. AI-literate employees who can leverage real-time insights are the key to agile, data-driven decision-making that enhances efficiency.

As we approach 2025, the opportunity to transform operations for the better is at hand. By embracing AI and building partnerships with technology providers, manufacturers can streamline processes, improve decision-making, and drive sustainability—paving the way for a smarter, greener, and more efficient future.

Biometric ID drives semiconductor manufacturing security and efficiency

The wrist-worn Nymi Band using biometric ID is expediting secure, hands-free authentication across semiconductor fabs, dramatically increasing productivity.

BY ARISTA BIOMETRICS

SEMICONDUCTOR manufacturers have traditionally been hindered by the need to authenticate operator identity across a complex patchwork of access points, workstations, and tools. Using badges, passwords, and other means of authentication has been slow, requiring the use of gloved hands, and could always be utilized independent of the intended operator, an inherent security flaw.

Wafer fabrication is a highly intricate process that demands precise execution, stringent control, and strong security protocols to safeguard intellectual property, protect sensitive information, and adhere to industry regulations. Conventional authentication approaches, such as passwords and hardware tokens, are often inadequate, inefficient, and insecure, particularly for deskless workers. This challenge is especially pronounced in semiconductor fabs, where employees are required to wear gloves and full-body suits while working in cleanroom conditions.

➤ Mobile workstations are now available with an optional NFC reader that can be used throughout semiconductor manufacturing facilities with biometric wearables and other forms of identification.

In response, semiconductor manufacturers are increasingly turning to wearable biometric ID products like wrist-worn Nymi Bands to securely speed authentication in a hands-free manner.

These innovative, wearable wristbands blend biometrics, security, and privacy, digitally empowering employees with passwordless, contactless workflow across applications, systems, and networks.

Employees simply wear their Nymi Band, authenticate as little as once per day, and work until they want to disconnect, according to the OEM's solutions brief "Connected Workers in a Passwordless World."

When used to facilitate employee entry to access points, tools, and equipment, wearable biometric identity products are significantly increasing security and productivity.

Now, computing solutions providers are providing scanners that can instantly read biometric wearables such as bands. When used with equipment such as mobile workstations, the combination is enabling seamless identification and authentication of authorized users throughout semiconductor fabs, further enhancing safety and efficiency.

"Using unique biometric ID wearables like Nymi bands is not only more secure than utilizing credentials [such as passwords] that can be compromised, but also enables much faster access to a wide range of tools. When utilized with equipment such as mobile workstations or handheld devices that require authorization to use, the combination unlocks greater productivity," says Paul Shu of ARISTA Corporation, a leading provider of computing platforms and visualization display products for semiconductor manufacturing environments.

"Ultimately, the wearable bands provide much greater security to semiconductor fabs. Employees cannot take someone else's band and log into a computer since each band corresponds with the operator's specific biometric data," adds Shu.

Streamlining connectivity

Semiconductor fabs often consist of hundreds of systems and applications that require proper user identification to access and use. Traditionally, the burden of providing and managing separate identification credentials has fallen on the employee, which has resulted in increased stress and decreased productivity.

The wafer fabrication process in semiconductor manufacturing takes place in an ultraclean environment where high-precision equipment is used, necessitating strict trackability and traceability.

Deskless operators in these facilities move between multiple machines, systems, and terminals throughout their shifts. Depending on the task, they may use devices such as desktop computers, tablets, or human-machine interfaces (HMIs). This frequent movement, coupled with the need to switch between various systems, makes conventional authentication methods like password entry or USB keys inconvenient, prone to errors, and inefficient.

Additionally, the use of PPE garments designed to minimize contamination from the operator further complicates traditional authentication processes like typing passwords or using hardware tokens.

Today, a new approach is enabling identity to be authenticated once per person while allowing the platform to facilitate connections to the required systems. Employees no longer assume the burden of manually authenticating their identity at each access point.

An example of this more streamlined, integrated approach to identification and access is the increased adoption of the Nymi Band at semiconductor fabs. The biometric wristband works in conjunction with the Nymi Connected Worker Platform, which creates an intermediary layer between employees and their employer's complicated IT infrastructure. The Platform establishes the biometric security and privacy of its users and allows them to inter-operate between disparate technologies.

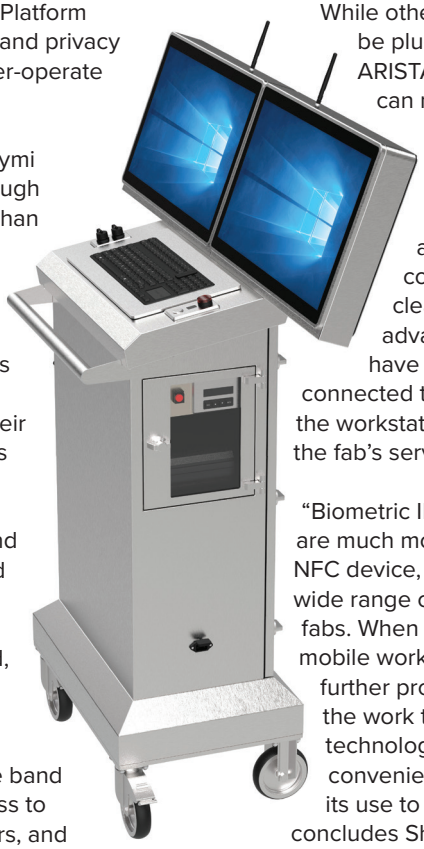
Employees authenticate to their Nymi Band as little as once per day through their fingerprint, which takes less than a second. The device's on-body detection capability enables an assigned employee to use it continually throughout all of their integrated applications. Employees simply take off their Nymi Band to deactivate and disconnect from their workplace, according to the OEM's solutions brief.

To enhance security, the Nymi Band is authenticated via fingerprint and verified against a mathematical template created at enrollment. Biometric images are never stored, and templates are secured locally in the band.

Employees can use their wearable band to efficiently gain hands-free access to terminals, email, applications, doors, and elevators throughout a facility, as required for their official duties. Access can be custom set according to the user's role, to appropriately protect sensitive information and areas.

> "Biometric ID wearables like Nymi Bands are much more secure than any other NFC device, so are ideal for logging into a wide range of devices at semiconductor fabs. When used with equipment such as mobile workstations, the combination can further promote productivity, allowing the work to occur where needed"

Paul Shu of ARISTA Corporation notes that biometric wearables pair with short-range wireless Near Field Communication (NFC) technology to expedite identification, authorized access, and communication. This is the case, for example, with ARISTA's mobile workstations, which are now available with an optional NFC reader that can be used throughout semiconductor fabs with biometric wearables and other forms of identification. NFC readers and related technologies are widely employed across industries for tasks such as asset management, inventory control, equipment monitoring, and enhancing security.



While other mobile workstations must be plugged into the wall to function, ARISTA's Mobile Operator Workstation can move from place to place while in operation free of wires due to its powerful lithium-ion battery. Wi-Fi capability is built into the workstation to allow for uninterrupted wireless communication in all corners of the cleanroom and fab. In addition, most advanced semiconductor fabs today have Wi-Fi-based system backbones connected to legacy subsystems, meaning the workstation can communicate directly with the fab's server.

"Biometric ID wearables like Nymi Bands are much more secure than any other NFC device, so are ideal for logging into a wide range of devices at semiconductor fabs. When used with equipment such as mobile workstations, the combination can further promote productivity, allowing the work to occur where needed. The technology provides greater security, convenience, and efficiency, so we expect its use to grow in the industry and beyond," concludes Shu.

➤ Mobile workstations with NFC readers enable biometric wearables to provide seamless identification and authentication of authorized users throughout semiconductor fabs.

The geopolitics of the semiconductor industry: navigating a global power struggle

Nations are racing to control the semiconductor technologies that power everything from consumer gadgets to defence systems. With supply chain issues, national security concerns, and economic goals all at play, the competition to lead this sector has never been more intense.

BY DUNSTAN POWER, DIRECTOR OF EMBEDDED DESIGN CONSULTANCY BYTESNAP DESIGN

HERE we explore the dynamics shaping the semiconductor industry, from the intensifying US-China rivalry and Taiwan's pivotal role to the global push for supply chain resilience, the rise of AI and EVs, and the challenges faced by regions like Europe and India in carving out a foothold in the sector.

US-China tensions and the semiconductor race

At the centre of semiconductor geopolitics lies the rivalry between the United States and China. While Washington seeks to maintain its technical and economic dominance, Beijing is rapidly growing its semiconductor capabilities. Allegations of intellectual property theft and questionable practices are further fuelling tensions. While US sanctions, which block China's access to advanced manufacturing equipment, have slowed its progress, they have not dented its long-term goal of becoming a global leader in chip production.

Despite its efforts, China remains 5–10 years behind in the most advanced semiconductor technologies. The gap between its global market share in semiconductor equipment supply (3.2%) and its share of demand (34.4%) further underscores the significant challenge it faces in achieving self-sufficiency.

To counter China's semiconductor ambitions, the US enacted the CHIPS Act, a key initiative aimed at boosting domestic production and restricting China's access to advanced manufacturing equipment. However, the future of the legislation is uncertain following President Donald Trump's sharp criticism during his campaign, which has raised doubts about the continuity of projects funded by the Act. This includes a £6.29 billion grant finalised by the Biden administration for Intel's semiconductor plant in Ohio, which some GOP lawmakers are keen to protect despite broader Republican support for cost-cutting measures.

Taiwan plays a pivotal role in the semiconductor industry, with TSMC producing over 50% of the world's chips. This dominance has raised concerns from governments and businesses like Apple about geopolitical risks from potential conflict with China. In response, TSMC is diversifying its operations by constructing new fabs in Arizona and Japan, though these facilities will contribute only about 10% of its total silicon output. Despite these initiatives, the majority of production will remain in Taiwan, highlighting the challenges of reducing reliance on a single region – a process that will take years to fully materialise.

The Netherlands has also been drawn into this geopolitical struggle, with its leading lithography equipment company, ASML, facing pressure to limit exports to China. These lithography machines, especially those using extreme ultraviolet (EUV) technology, are critical to advanced chip production and represent a linchpin in the semiconductor ecosystem. Although the Dutch government has taken steps to align with US sanctions, questions remain about the extent of its compliance.

Supply chain challenges and the road to recovery
The COVID-19 pandemic laid bare the fragility of global semiconductor supply chains. A surge in demand for electronics and automotive components created an acute shortage, with lead times stretching beyond a year. During this crisis, China absorbed a significant share of global demand. However, as the pandemic's supply chain pressures eased in early 2023, the industry faced a new problem: overproduction and excess inventories. Companies, having overordered during the crisis, found themselves saddled with surplus chips, dampening innovation and creating market instability.

Despite the challenges, the semiconductor industry is rebounding, largely driven by the surging demand for artificial intelligence (AI) applications. AI-specific chips, such as those produced by Nvidia, have experienced explosive growth, marking a significant shift in market priorities. The AI chip market, valued at £49.1 billion in 2023, is projected to grow at a compound annual rate of 29.4%, reaching £496.9 billion by 2032.

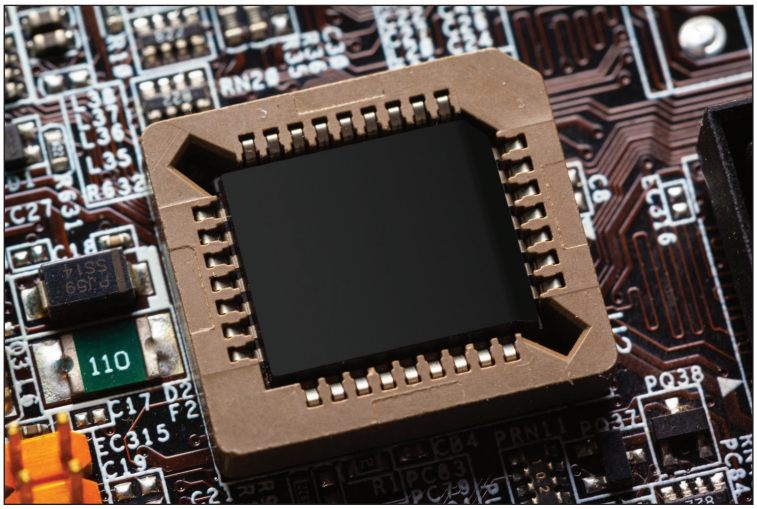
Another key driver is the rising integration of semiconductors in electric vehicles (EVs). Globally, 15.2 million EVs were sold in 2024, reflecting a 25% year-to-date increase, according to Rho Motion. China leads the charge, setting a record with 1.3 million units sold in November 2024 alone, almost entirely from battery electric vehicles (BEVs). Brands like Geely, Tesla, and Changan were among the top sellers, further cementing China's dominance in the EV market.

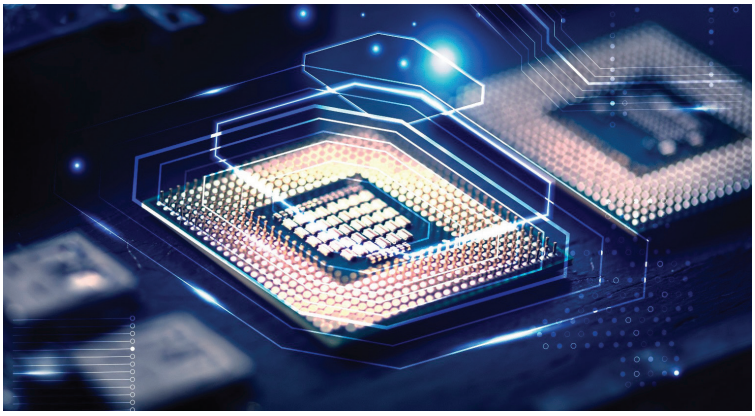
China's high EV sales have profound geopolitical implications for the semiconductor industry, as EVs rely heavily on advanced chips for critical systems. By leading global EV adoption, China is solidifying its influence in the semiconductor sector, even as it remains dependent on foreign technology. This dynamic heightens competition with the US and Europe, driving their efforts to secure supply chains and reduce reliance on Taiwan for chips and China for EV technologies. At the same time, China's integration of domestic semiconductor development into its booming EV industry strengthens its position in the global tech race, making semiconductors a focal point of both economic strategy and geopolitical power conflicts.

Europe's struggles in the semiconductor landscape
Europe, while home to significant players like NXP and STMicroelectronics, has long been overshadowed by its US and Asian counterparts. The region faces several challenges, including a lack of large-scale investment and a struggling automotive sector. Germany, the largest electronics market in Europe, exemplifies these difficulties, with its car manufacturers grappling with the transition to EVs. Meanwhile, China is taking the lead in EV technology, putting further pressure on Europe's traditional industries.

In response, the European Union has pledged billions in subsidies to bolster its semiconductor sector. For instance, Germany recently announced a €2 billion investment aimed at strengthening chip manufacturing. While this is a step in the right direction, the scale of investment pales in comparison to the costs of building state-of-the-art fabs. There is, however, a need for greater financial commitments to reduce reliance on non-European manufacturers and foster more innovation. Europe's progress is, however, hampered by bureaucratic red tape and political vacillation.

Unlike the US, which has adopted a more aggressive approach to reshoring manufacturing, Europe appears to be on the sidelines of this global competition. The UK, in particular, has little influence, with limited government investment and a reliance on allies for strategic direction. Efforts to block Chinese acquisitions, such as the attempted purchase of a fab in Wales, highlight the UK's





defensive posture but do little to address its lack of domestic manufacturing capability.

Global trends reshaping the semiconductor industry
The semiconductor industry is navigating a critical period of transformation. Diversification of manufacturing, while necessary to mitigate risks tied to Taiwan's dominance, highlights the sheer complexity and cost of redistributing global supply chains. The strategic investments in fabs across the US, Japan, and Europe signal progress, but achieving meaningful independence will require years of sustained effort and collaboration.

AI and electric vehicles are reshaping semiconductor design and production, driving demand for specialised chips that power these transformative technologies. This shift creates opportunities for regions like India, with its £12 billion investment in chip-packaging plants and its first modern chip fab, and Europe to carve out niches. However, realising this potential will also require solutions to critical talent shortages. The expertise required for semiconductor design and manufacturing is concentrated in regions like Taiwan and South Korea, where decades of focused development have cultivated a highly skilled workforce. New entrants to the industry, such as India, face significant challenges in building this specialised talent pool, with red tape and bureaucratic hurdles adding further delays. Even with AI assisting in aspects of chip design, the deep, specialised knowledge needed for tasks such as coding, placement, and fabrication remains irreplaceable by automation.

At the heart of these trends is a renewed emphasis on resilience. Nations and corporations are beginning to view semiconductors as strategic assets, integral to both economic stability and national security. This recalibration is fostering an ecosystem where long-term innovation and cross-border collaboration may ultimately outweigh competition. If governments and industries align their priorities effectively, the semiconductor sector could emerge not only stronger but also more decentralised and inclusive, offering a more secure foundation for future technological growth.

semi™

Connecting Semiconductors and Electronics

About SEMI:
SEMI connects more than 2,500 member companies and 1.3 million professionals worldwide to advance the technology and business of electronics design and manufacturing. The breadth and depth of our events, programs and services help members accelerate innovation and collaboration on the toughest challenges to growth.

ESDA Electronic System Design Alliance

FlexTech

FOA Fab Owners Alliance

MEMS & SENSORS INDUSTRY GROUP®

SOI Industry Consortium

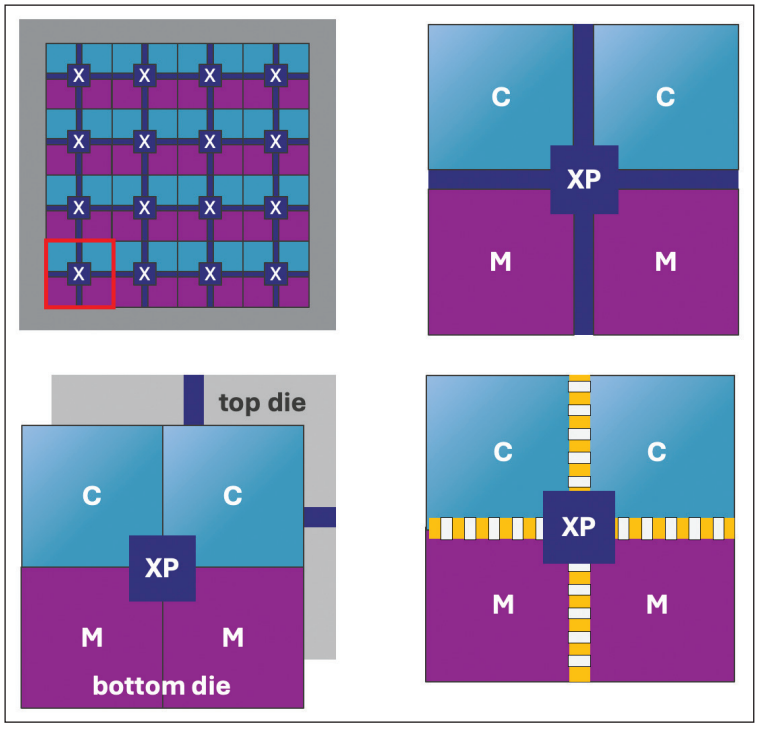
Innovative approaches to scaling network-on-chip architectures

The evolution of cloud computing has sparked a pressing need for advanced solutions that maximize computational efficiency while minimizing physical and energy constraints. Modern data centers depend heavily on multi-core processors, often packing over 100 cores into a single chip.

BY MORITZ BRUNION, RESEARCHER DESIGN-TECHNOLOGY CO-OPTIMIZATION AND JAMES MYERS, PROGRAM DIRECTOR SYSTEM TECHNOLOGY CO-OPTIMIZATION, BOTH AT IMEC.

THESE PROCESSORS are designed to handle the growing demands of cloud-based applications by sharing network, memory, and storage resources, transforming each core into a rentable unit of processing power.

However, as processors grow more powerful, the network-on-chip (NoC) has emerged as a critical bottleneck in scaling. The NoC, tasked with routing data among CPU cores and memory, relies on metal interconnects that present unique challenges when scaled down. Higher resistance in these interconnects increases power consumption and necessitates additional signal repeaters to maintain performance over long distances.



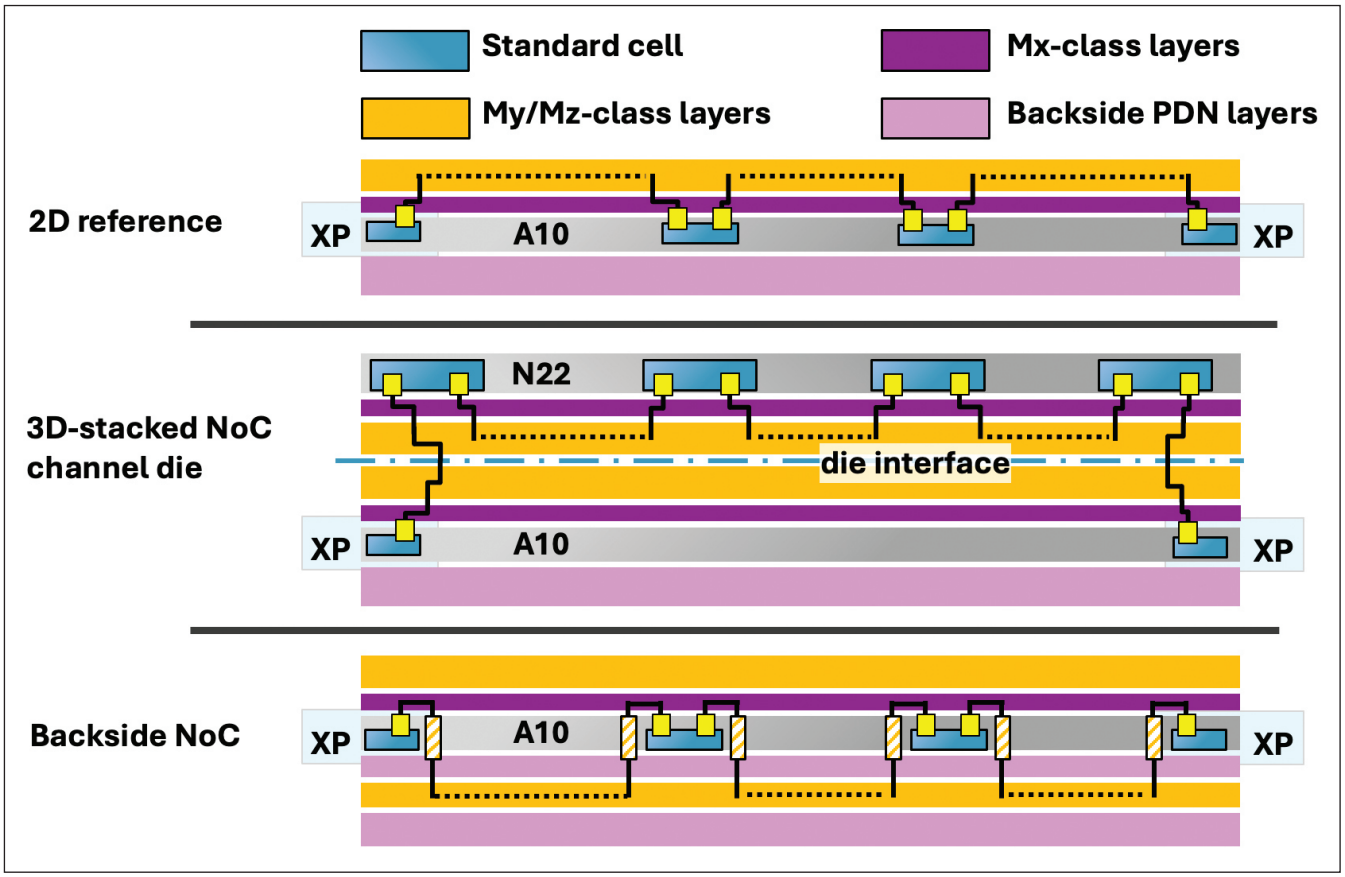
➤ Figure 1. 2D reference system (top left) and tile (top right) with NoC channel routes and logic within a single FEOL and BEOL stack. In the bottom are the two new approaches depicted: (left) 3D stacking design, showing the separation of NoC channel routes into a dedicated routing die bonded to the A10 logic die, and (right) the backside integration approach, showing NoC channel routes integrated into the backside metal layers of the BSPDN.

Adding to this, the increasing core count and HD logic scaling, while maintaining the same NoC dimensions, drive a significant rise in NoC area. These factors add complexity and compromises the goal of achieving smaller and more efficient designs.

Addressing these challenges has led to a variety of innovative solutions, though none without trade-offs. 2D mesh topologies, while straightforward and scalable, struggle with communication latency as the number of cores increases.

Other approaches, such as routerless configurations or workload-specific optimizations, can improve performance but are often impractical for general-purpose systems like those used in cloud computing. While scaling the NoC link throughput by an increase in the number of signals per channel can increase the throughput, it often results in higher costs and resource demands, further complicating the NoC landscape.

In response to these constraints, imec researchers have pioneered two transformative approaches: relocating NoC channels to a dedicated die and integrating them with the backside power delivery network (BSPDN). These strategies, guided by system-technology co-optimization (STCO) principles, aim to overcome scaling limitations while balancing cost and performance. Of these, the co-integration of NoC channels with the BSPDN offers particularly promising results for future design of such high core-count systems.



➤ Figure 2. (Top) The technology stack cross-section for the 2D reference shows both NoC channels and crosspoints (XP) in the A10 logic frontend. (Middle) The NoC routing is entirely offloaded to a dedicated die freeing up placement and routing resources on the main logic die. In this case, channels in the separate die are manufactured in older technology while the crosspoints reside in the A10 logic. (Bottom) The NoC channels sharing routing resources with the power delivery network and repeaters located on the logic die front-end. NoC buffer islands occupy 1-2% of a high-performance CPU core (compared to up to 10% of the silicon area being dedicated to the NoC in the 2D reference), with the addition of two dedicated backside metal layers for NoC channels.

Dedicated NoC routing on a separate die

One novel approach proposed by imec involves offloading the NoC channel routes to a dedicated die, independent of the main logic layers. Using wafer-to-wafer face-to-face hybrid bonding, this architecture can leverage the high-bandwidth data transfer in the vertical direction with minimal energy usage per bit. The NoC die can be fabricated using a less advanced manufacturing process, such as N22, significantly reducing production costs.

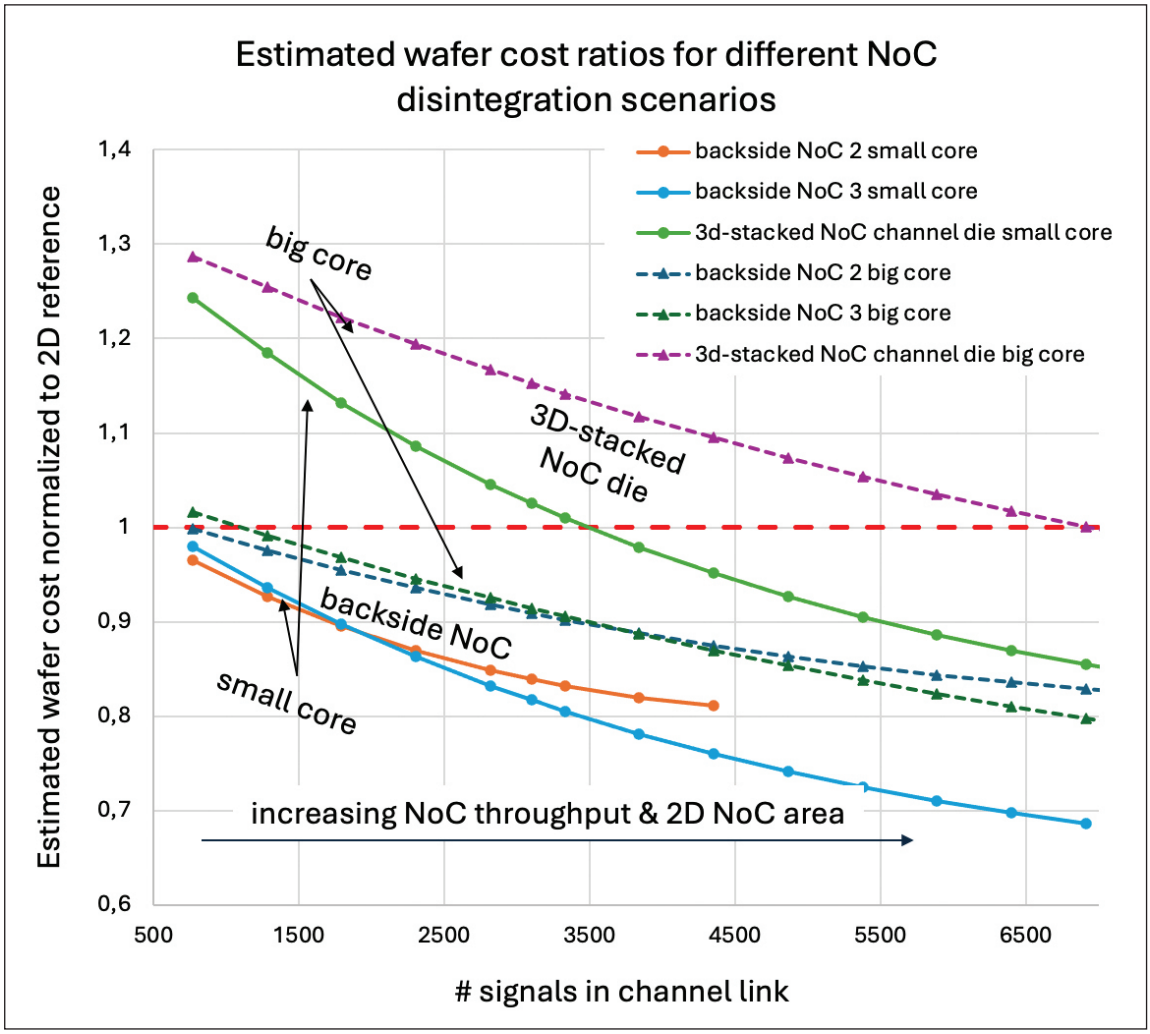
This design also simplifies the back-end-of-line (BEOL) configuration by using fewer metal layers, thereby optimizing functional integration efficiency. The NoC routers, which make real-time routing decisions, remain on the main logic die, ensuring that latency is kept to a minimum.

This design, however, is not without its challenges. Power distribution becomes more complicated, as the additional die requires its own power infrastructure. Physical design experiments also revealed an 8% increase in propagation delay and a 15% rise in energy per bit transferred across a channel link compared to conventional 2D NoC systems.

Backside integration with the BSPDN

A second solution involves co-integrating NoC channels with the BSPDN on the backside of the wafer. The BSPDN's existing metal layers, optimized for power delivery with wider pitches and lower resistance, provide an ideal foundation for routing NoC channels over long distances at high clock speeds. This integration takes advantage of the relaxed design constraints of backside interconnects to achieve efficient signal transmission.

To implement this approach, the researchers made several design adjustments. First, they devised a bidirectional wiring scheme, enabling both horizontal and vertical NoC channels to share the same metal layer. This reduces the total number of required layers, lowering both costs and the overall chip footprint. Second, since BSPDN currently doesn't support active devices on the backside, signal repeaters were placed as compact "islands"



➤ Figure 3. Estimated wafer cost ratios of different NoC integration schemes, normalized to the 2D baseline. As the width of the NoC channel increases, the cost advantage of backside integration becomes more evident.

on the main logic die. These repeaters ensure robust signal strength at a small area overhead, while freeing up the channel routing footprint in the main logic die for other logic components. Finally, integrating NoC channels with the BSPDN required addressing the shared routing resources between data and power delivery, which increases the risk of IR drop and can affect performance. To mitigate these challenges, the researchers traded-off the PDN pitches and IR drop against the area overhead of the repeater islands, maintaining the benefits of the BSPDN and ensuring stable voltage levels, while also supporting reliable data transmission across the NoC.

Cost-benefit analysis favours NoC backside integration

When comparing the two approaches, not only their technical trade-offs but also cost-effectiveness is important to identify the best solution for growing demands. The dedicated die method offers greater flexibility and customization options but incurs higher manufacturing costs due to the need for an additional fully processed wafer. By contrast, integrating NoC channels with the BSPDN reuses existing infrastructure, adding only a few extra metal layers. This significantly reduces costs and optimizes the use of front-side silicon, making it an attractive option for applications requiring high core densities, such as cloud server CPUs.

Backside integration also excels in scalability. As core counts per processor continue to rise, the demand for wider NoC channels increases. By leveraging the backside metal layers, this approach minimizes congestion and enables higher data throughput without substantially increasing the silicon footprint. These attributes make it a compelling solution for next-generation chip architectures.

To mitigate these challenges, the researchers traded-off the PDN pitches and IR drop against the area overhead of the repeater islands, maintaining the benefits of the BSPDN and ensuring stable voltage levels

Broader implications and future directions

While backside NoC integration is highly applicable for cloud server CPUs, its relevance to other applications, such as GPUs and accelerators with coarse-grained, regular topologies, is still being explored. However, widespread adoption of this technology depends on advancements in Electronic Design Automation (EDA) tools. Currently, implementing backside NoC channels requires specialized workflows, which can be labor-intensive and costly. As EDA tools evolve, they are expected to streamline the design process, making backside integration more accessible and practical for a variety of use cases.

In conclusion, the integration of NoC channels with the BSPDN represents a significant breakthrough in chip design. By addressing routing and power delivery challenges simultaneously, this approach exemplifies the power of STCO principles. As the demand for scalable, high-performance architectures continues to grow, innovations like backside NoC integration will play a pivotal role in shaping the future of semiconductor technology and driving the next wave of computational advancements.

Moritz Brunion

Researcher Design-Technology Co-optimization

Moritz Brunion received the M.Sc. degree in electrical and computer engineering from the University of Bremen, Germany, in 2022. He is currently a researcher at imec, Leuven, Belgium, and his research focuses on design-technology co-optimization for fine-grained 3D systems.

James Myers

Program Director System Technology Co-optimisation

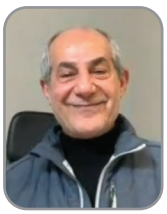
James Myers holds a MEng degree in Electrical and Electronic Engineering from Imperial College in London. He spent 15 years at Arm, leading research from low power circuits and systems, through printed electronics, to DTCO activities. He joined imec in 2022 to lead the System Technology Co-optimisation program, with the aim of building upon established DTCO practices to overcome the numerous scaling challenges foreseen for future systems. James holds 60 US patents, has taped out 20 SoCs, has presented at ISSCC and VLSI Symposium, and has published in IEDM and Nature.

Europe's semiconductor industry focuses on sustainable growth

Laith Altimime, President of SEMI Europe, discusses the challenges and opportunities facing the European semiconductor industry. Laith talks sustainability, collaboration, technology innovation, skills and geopolitics, sharing his excitement for the industry's future as it underpins the ongoing development of our digital world.

SIS: *The theme of last year's Semicon Europa, towards the end of 2024, was, innovation collaboration, powering sustainable and exponential growth. It would be good to understand what was the thinking behind this focus, as well as how did the event go?*

LA: Th event went exceedingly well. I think the feedback was tremendously positive. Semicon Europa is and will always be a pivotal event, and an exciting opportunity for the European semiconductor ecosystem, providing a platform for collaboration, innovation, and knowledge sharing.



The focus on innovation and collaboration is powering sustainable, exponential growth. It's very much the statement of the industry, which is the goal for a holistic, forward-thinking approach. And it recognises that the pace and scope of growth required to meet the global demands cannot be achieved through isolated efforts. It very much calls for leveraging cutting edge technologies alongside collaborative efforts across industries, borders, and across sectors to create sustainable, scalable digital future.

Ultimately, the thinking behind the theme underscores that the future must be built on technological advancement, cooperation, collaboration, and sustainability, all working together to generate exponential progress in a way that respects both the planet and humanity, which is really the key contribution of the semiconductor industry.

SIS: *Perhaps we can drill down into a little more detail, starting with sustainability. It's clearly a major focus for the industry. And it'd be good to understand how you would perhaps characterise the work that's been done so far, and maybe contrasting it with what more remains to be done?*

LA: Sustainability is part of the industry's exponential growth, the target to reach or even exceed $1 trillion global industry revenue by 2030. Sustainability has become a critical focus across industries, particularly in the semiconductor and tech sectors, as they play a central role in global carbon emissions, resource consumption, and electronic waste.
It's key to state that that the semiconductor industry has made substantial strides towards sustainability, particularly in the areas like energy efficiency,

material recycling, and renewable energy adoptions. These are fundamental, you know, in terms of enabling the industry to transition and to contribute. However, achieving Net Zero, requires the addressing of the broader environmental impacts associated with the entire supply chain, e-waste, carbon emissions from the semiconductor manufacturing and product usage. Ultimately, the semiconductor industry's path to Net Zero will depend very much on continued innovation and collaboration and a willingness to adopt circular economy principles, from design and manufacturing to end of life disposal.

Although this journey is complex, with really concentrated efforts, the industry can play a pivotal role in a sustainable Net Zero future.

SIS: *Collaboration has been mentioned a couple of times - there does seem to be a growing, even a final recognition that, in many cases, the challenges and the opportunities for the sector are just too complex, sizeable and expensive to be tackled by individual organisations. There is a growing need for collaborative partnerships, whether that's research to commercial or commercial organisations working each other. How would you characterise this necessity and how it is working in practise?*

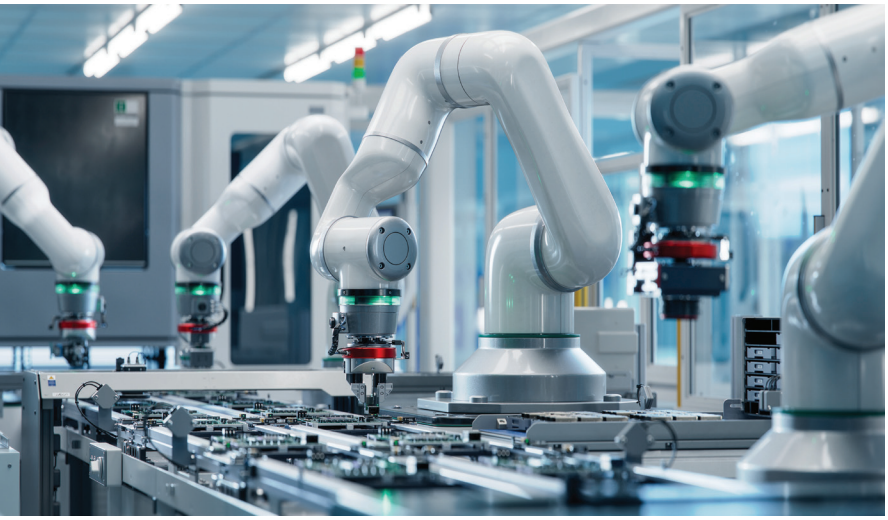
LA: Yes. You you're absolutely right. The semiconductor sector, like many other high-tech and industrial sectors, is facing challenges and opportunities that are increasingly too complex as the industry continues to growth. And one needs to keep in mind that the industry growth or doubling by 2030 is basically doubling what it has taken to reach today's figure – just over $600 billion over five decades.

Within the next five to seven years, the challenges of complexity and the speed of innovation required cannot be tackled by a single CEO, single country or single company. There needs to be a global collaborative effort, and SEMI has provided these platforms. They've grown in recognition that collaborative partnerships, whether between commercial organisations, research institutions, or even public/private entities are key for tackling the complex, large scale, unprecedented challenges of the semiconductor industry. The demand for innovation in areas like AI, quantum computing and sustainability is vast.

By leveraging collective expertise, shared resources, and joint development - collaboration - the semiconductor industry can address these unprecedented challenges. SEMI has the necessary global footprint and has launched the SEMI International Policy Summit, to bring together the industry, academia, and the policy makers to educate all on generating the new policies required to help the industry advance towards the 2030 target.

SIS: *Slightly opposed to this collaboration, or at least not necessarily fully in line, there is this growing trend towards reshoring or onshoring. Do you think that is specifically anti-collaboration? And what impact is it having on the industry overall – is it weakening or strengthening it?*

LA: It's right to highlight the growing trends towards reshoring and onshoring, it's very much in the spotlight today. It's driven by several factors, including geopolitical tensions. This is really very high on the agenda today. Along with the supply chain, which can also experience geopolitically induced disruptions. National security concerns are



very high on the agenda. There is a desire to reduce dependence on foreign sources.

The solution it to think global, act regional - by integrating into a broader strategy of collaboration, both within Europe and globally, we can achieve the best of both worlds - stronger regional capabilities while still participating in global ecosystems when it comes to innovation, research, commerce. It's key to keep in mind that the industry's future hinges on this delicate balancing act, with geopolitical tensions the overriding issue.

SIS: *In terms of innovation within the industry, advanced packaging and fab production management are near the top of the industry's priority list. It would be good to understand how excited you are about work in this area and any other innovations that you might want to highlight?*

LA: The semiconductor industry today is, in my opinion, the most exciting industry to work in because of all the opportunities, collaboration, global perspectives. Advanced packaging and fab management are incredibly exciting areas because they offer the opportunity to push the boundaries of what semiconductors can do. And also to optimise performance, and, at the same time, to drive innovation across virtually every sector of the entire value chain.

Advanced packaging maximises the performance potential because of the amount of data generated and the need for a much wider bandwidth, as with individual chips. In the end, it's really at system level that we talk about energy performance cost. This needs to be addressed at system level, and advanced packaging can be instrumental in enabling this. As the semiconductor industry continues to innovate in these areas, we're likely to see breakthroughs that enable the next generation of computing, communication, sustainable technology - helping power the industry's exponential growth is AI, the AI driven world of the future.

This is a major part of digital transformation. Everything is AI underpinned, AI driven, on enabling basically, like, everything. When we talk about smart cities, quantum computing, autonomous driving, and the need for cloud, edge computing and all the other different forms of computing to be able to handle the explosion amount of data as connectivity continues to grow. The progress being made in here promises to reshape industries and societies alike.

There will be a paradigm shift that will definitely drive the industry's exponential growth, and we'll be transitioning towards a very sustainable digital future.

SIS: *There's an insatiable demand for AI chips, which is not going to slow down anytime soon. And then there are AI applications within the industry - AI can be used by the industry to help improve production, design, and the like?*

LA: AI is really underpinning the projected exponential growth of the industry by 2030. AI is feeding sustainable demand - for specialised semiconductor hardware, examples such as AI accelerators, AI specific chips. At the same time, AI technologies are being used to customise everything from chip design and manufacturing processes to supply chain management and quality control.

We're using AI to accelerate the learning, from across the entire semiconductor value chain. The relation between AI and the semiconductor industry is one of the most dynamic and mutually reinforcing aspects of technological innovation today. It is also key also to keep in mind that there is a synergy between these two forces will which will be a key driver of technological progress in the years to come. This will help to power everything from AI driven health care, autonomous vehicles, smart cities, and beyond. Basically, accelerating the digital transformation into a sustainable digital era.

SIS: *Moving on to Europe specifically, with your remit, it would be good to understand how you see the European semiconductor industry, maybe comparing and contrasting it with the US and the Asian markets, outlining what you think that Europe can offer in terms of the strengths it has within the industry. And if there are any areas you think where, if it's not weak, it could at least develop more of a presence?*

LA: The European semiconductor industry has a clear opportunity to carve out a very competitive edge by leveraging its existing strengths, its world class R&D powerhouses, material science, automotive, and AI research, while in parallel simultaneously addressing the need for, as we have already mentioned, advanced packaging, advanced manufacturing capacity, and also global supply chain resilience. So, I wouldn't say independent sovereignty independent, but it's key to have supply chain resilience to make sure that we will not have the same thing that happened to the automotive industry during COVID.

As supply chain resilience is of paramount importance, this means we need to look at what we're strong at, compete, maintain that competitive advantage, but also continue to invest in the areas whereby it provides Europe the supply chain resilience, to maintain its global strategic positioning in the global semiconductor value chain. We have powerhouses in Europe - from equipment, the likes of ASML, from manufacturing, Infineon, NXP, ST, the Bosch. They are powerhouses, so they need to continue to invest in them to make sure that we maintain our competitive advantage while continuing to invest in innovation – for example, the most recent three pilot lines investments under the European Chips act.

SIS: *In terms of your own organization's sort of role within the industry more generally, it would be good to have an understanding of some of your key activities and achievements from the last year. And then looking ahead for this year, what's on the horizon?*

LA: SEMI Europe is very close to my heart and we play a pivotal role in driving innovation, advocacy, and collaboration across the continent.

Over the course of 2024 and into 2025, SEMI Europe activities have been largely focused on addressing the critical challenges and opportunities facing the European semiconductor ecosystem. This ranges from skills development, policy advocacy to supply chain resilience, as well as sustainability.

We continue our pivotal work in strengthening semiconductor ecosystems. This is through skills development, policy advocacy, industry collaboration and technology innovation. Workforce development is crucial and we need to continue our focus is on the talent pipeline. The skills shortage remains a critical challenge and Europe is committed to driving education and training initiatives. And we continue to generate new initiatives year on year, which is very much supported by our industry and our SEMI European advisory board to ensure Europe has the talent necessary to meet the demands of an increasingly AI-driven and digitally connected world. This means that upskilling and reskilling, as well as diversity inclusion, equity.

SIS: *Following up on the skills side, everyone talks about the impending skills shortage, but no one seems to be panicking. Famously, TSMC postponed opening a a fab in Arizona, citing a workforce skills shortage. How worried are you that, if there isn't enough new blood and skills coming into the industry, that there will be significant delays within the supply chain?*

LA: We recognise this is a key challenge, in order to enable the growth. And there are examples where things did not happen because of the talent required. But one cannot sit back and say everything will be alright. We are doing everything we can at SEMI Europe to help provide our global holistic workforce development programmes and implementation in Europe.

> The semiconductor industry today is, in my opinion, the most exciting industry to work in because of all the opportunities, collaboration, global perspectives. Advanced packaging and fab management are incredibly exciting areas because they offer the opportunity to push the boundaries of what semiconductors can do.

SIS: *Finally, if we can talk about geopolitics. Are you at all worried that various geopolitical might, if not jeopardise the industry, at least change its direction of travel, particularly with regard to sustainability. Are you at all worried that the industry might sort of have to change its focus whether it wants to or not?*

LA: Geopolitics has been taken to another level. Because we are a collaborative industry, we need to make sure that this collaboration continues. But it's a great question and one that speaks to the very heart of the industry, as evolving in a complex, but also often turbulent global environment. The intersection of geopolitics, technology and sustainability is particularly charged right now.

If you look at the investments such as the European Chips Act, the US Chips Act and other initiatives since the COVID this has taken the semiconductor industry collaboration to the next level, a very clear paradigm shift.

This needs to continue. It's imperative this continues. And I think the rest of this decade will be crucial for determining whether geopolitical tensions derail industry progress or whether global collaboration, particularly in areas like AI and sustainability, can overcome these challenges.

SIS: *Finally, are we trying to fool ourselves that we can have an equally digital and sustainable world? Does there have to be some compromise one way or the other, or do you think there is a genuine opportunity to give everyone the digital devices and access that we all demand and also do it in a sustainable way? Or do we just have to accept that if we all want to consume vast amounts of data, that will have an impact on the planet, and we just have to live with it?*

LA: I think it's important they go in parallel because one needs to consider not only the economic impact, but also societal impact. This is of paramount importance. They need to go hand in hand.

Fiber computer allows apparel to run apps and "understand" the wearer

MIT researchers developed a fiber computer and networked several of them into a garment that learns to identify physical activities.

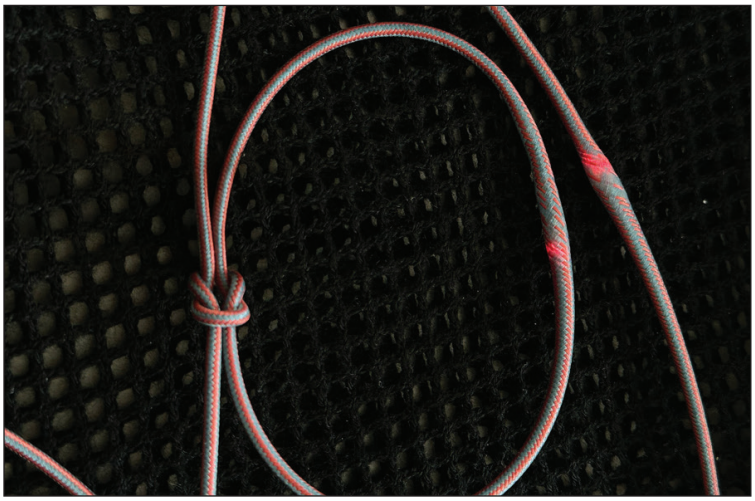
BY ADAM ZEWE, MIT NEWS

What if the clothes you wear could care for your health?

MIT RESEARCHERS have developed an autonomous programmable computer in the form of an elastic fiber, which could monitor health conditions and physical activity, alerting the wearer to potential health risks in real-time. Clothing containing the fiber computer was comfortable and machine washable, and the fibers were nearly imperceptible to the wearer, the researchers report.

Unlike on-body monitoring systems known as "wearables," which are located at a single point like the chest, wrist, or finger, fabrics and apparel have an advantage of being in contact with large areas of the body close to vital organs. As such, they present a unique opportunity to measure and understand human physiology and health.

The fiber computer contains a series of microdevices, including sensors, a microcontroller, digital memory, bluetooth modules, optical communications, and a battery, making up all the necessary components of a computer in a single elastic fiber.



➤ This single, elastic fiber contains a series of microdevices, including sensors, a microcontroller, digital memory, bluetooth modules, optical communications, and a battery, making up all the necessary components of a computer. Credit: Yoel Fink, edited by MIT News

The researchers added four fiber computers to a top and a pair of leggings, with the fibers running along each limb. In their experiments, each independently programmable fiber computer operated a machine-learning model that was trained to autonomously recognize exercises performed by the wearer, resulting in an average accuracy of about 70 percent.

Surprisingly, once the researchers allowed the individual fiber computers to communicate among themselves, their collective accuracy increased to nearly 95 percent.

"Our bodies broadcast gigabytes of data through the skin every second in the form of heat, sound, biochemicals, electrical potentials, and light, all of which carry information about our activities, emotions, and health. Unfortunately, most if not all of it gets absorbed and then lost in the clothes we wear.

Wouldn't it be great if we could teach clothes to capture, analyze, store, and communicate this important information in the form of valuable health and activity insights?" says Yoel Fink, a professor of materials science and engineering at MIT, a principal investigator in the Research Laboratory of Electronics (RLE) and the Institute for Soldier Nanotechnologies (ISN), and senior author of a paper on the research, which will appear in Nature. The use of the fiber computer to understand health conditions and help prevent injury will soon undergo a significant real-world test as well. U.S. Army and Navy service members will be conducting a month-long winter research mission to the Arctic, covering 1,000 kilometers in average temperatures of -40 degrees Fahrenheit. Dozens of base layer merino mesh shirts with fiber computers will be providing real-time information on the health and activity of the individuals participating on this mission, called Musk Ox II.

"In the not-too-distant future, fiber computers will allow us to run apps and get valuable health care and safety services from simple everyday apparel. We are excited to see glimpses of this future in the upcoming Arctic mission through our

partners in the U.S. Army, Navy, and DARPA. Helping to keep our service members safe in the harshest environments is a honor and privilege," Fink says. He is joined on the paper by co-lead authors Nikhil Gupta, a materials science and engineering graduate student; Henry Cheung MEng '23; and Syamantak Payra '22, currently a graduate student at Stanford University; John Joannopoulos, the Francis Wright Professor of Physics and director of the Institute for Soldier Nanotechnologies; as well as others at MIT, Rhode Island School of Design, and Brown University.

Fiber focus

The fiber computer builds on more than a decade of work in the Fibers@MIT lab at the RLE and was supported primarily by ISN. In previous papers, the researchers demonstrated methods for incorporating semiconductor devices, optical diodes, memory units, elastic electrical contacts, and sensors into fibers that could be formed into fabrics and garments.

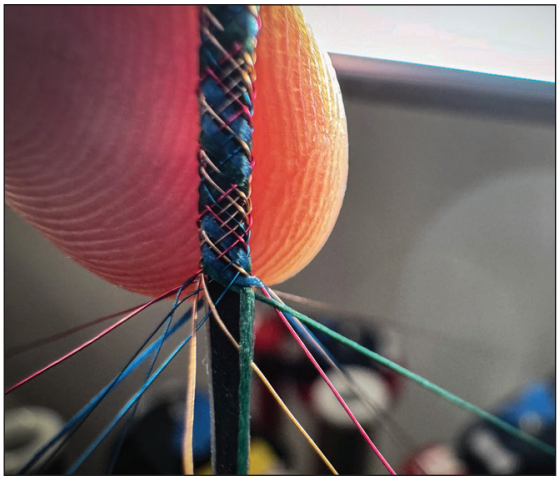
"But we hit a wall in terms of the complexity of the devices we could incorporate into the fiber because of how we were making it. We had to rethink the whole process. At the same time, we wanted to make it elastic and flexible so it would match the properties of traditional fabrics," says Gupta.

One of the challenges that researchers surmounted is the geometric mismatch between a cylindrical fiber and a planar chip. Connecting wires to small, conductive areas, known as pads, on the outside of each planar microdevice proved to be difficult and prone to failure because complex microdevices have many pads, making it increasingly difficult to find room to attach each wire reliably.

In this new design, the researchers map the 2D pad alignment of each microdevice to a 3D layout using a flexible circuit board called an interposer, which they wrapped into a cylinder. They call this the "maki" design. Then, they attach four separate wires to the sides of the "maki" roll and connected all the components together.

"This advance was crucial for us in terms of being able to incorporate higher functionality computing elements, like the microcontroller and Bluetooth sensor, into the fiber," says Gupta. This versatile folding technique could be used with a variety of microelectronic devices, enabling them to incorporate additional functionality. In addition, the researchers fabricated the new fiber computer using a type of thermoplastic elastomer that is several times more flexible than the thermoplastics they used previously. This material enabled them to form a machine-washable, elastic fiber that can stretch more than 60 percent without failure.

They fabricate the fiber computer using a thermal draw process that the Fibers@MIT group pioneered in the early 2000s. The process involves creating a



➤ Researchers braid a computer fiber with a combination of metal and textile yarns. Covering the fiber computer with traditional yarns enables it to be easily integrated into fabrics and textiles. Credit: Hamilton Osoy, IFM

macroscopic version of the fiber computer, called a preform, that contains each connected microdevice. This preform is hung in a furnace, melted, and pulled down to form a fiber, which also contains embedded lithium-ion batteries so it can power itself.

"A former group member, Juliette Marion, figured out how to create elastic conductors, so even when you stretch the fiber, the conductors don't break. We can maintain functionality while stretching it, which is crucial for processes like knitting, but also for clothes in general," Gupta says.

Bring out the vote

Once the fiber computer is fabricated, the researchers use a braiding technique to cover the fiber with traditional yarns, such as polyester, merino wool, nylon, and even silk. In addition to gathering data on the human body using sensors, each fiber computer incorporates LEDs and light sensors that enable multiple fibers in one garment to communicate, creating a textile network that can perform computation
Each fiber computer also includes a Bluetooth communication system to send data wirelessly to a device like a smartphone, which can be read by a user.

The researchers leveraged these communication systems to create a textile network by sewing four fiber computers into a garment, one in each sleeve. Each fiber ran an independent neural network that was trained to identify exercises like squats, planks, arm circles, and lunges.

"What we found is that the ability of a fiber computer to identify human activity was only about 70 percent accurate when located on a single limb, the arms or legs. However, when we allowed the fibers sitting on all four limbs to 'vote,' they collectively reached nearly 95 percent accuracy, demonstrating the importance of residing on multiple body areas and forming a network between autonomous fiber computers that does not need wires and interconnects," Fink says. Moving forward, the researchers want to use the interposer technique to incorporate additional microdevices.

➤ An operating fiber computer shown knotted (left) and hanging with a 1-kilogram weight attached (right). Credit: Nikhil Gupta/Fink Lab MIT

Arctic insights

In February, a multinational team equipped with computing fabrics will travel for 30 days and 1,000 kilometers in the Arctic. The fabrics will help keep the team safe, and set the stage for future physiological "digital twinning" models.

"As a leader with more than a decade of Arctic operational experience, one of my main concerns is how to keep my team safe from debilitating cold weather injuries — a primary threat to operators in the extreme cold. Conventional systems just don't provide me with a complete picture. We will be wearing the base layer computing fabrics on us 24/7 to help us better understand the body's response to extreme cold and ultimately predict and prevent injury," says U.S. Army Major Hefner, the commander of Musk Ox II.

Karl Friedl, U.S. Army senior research scientist of performance physiology, noted that the MIT programmable computing fabric technology may become a "gamechanger for everyday lives." "Imagine near-term fiber computers in fabrics and apparel that sense and respond to the environment and to the physiological status of the individual, increasing comfort and performance, providing real-time health monitoring and providing protection against external threats. Soldiers will be the early adopters and beneficiaries of this new technology, integrated with AI systems using predictive physiological models and mission-relevant tools to enhance survivability in austere environments," Friedl says.

"The convergence of classical fibers and fabrics with computation and machine learning has only begun. We are exploring this exciting future not only through research and field testing, but importantly in an MIT Department of Materials Science and Engineering course 'Computing Fabrics,' taught with Professor Anais Missakian from the Rhode Island School of Design," adds Fink. This research was supported, in part, by the U.S. Army Research Office Institute for Soldier Nanotechnology (ISN), the U.S. Defense Threat Reduction Agency, the U.S. National Science Foundation, the Fannie and John Hertz Foundation Fellowship, the Paul and Daisy Soros Foundation Fellowship for New Americans, the Stanford-Knight Hennessy Scholars Program, and the Astronaut Scholarship Foundation.

Paper: *A single-fibre computer enables textile networks and distributed inference*
https://www.nature.com/articles/s41586-024-08568-6

Photonic processor could enable ultrafast AI computations with extreme energy efficiency

The deep neural network models that power today's most demanding machine-learning applications have grown so large and complex that they are pushing the limits of traditional electronic computing hardware. Photonic hardware, which can perform machine-learning computations with light, offers a faster and more energy-efficient alternative. However, there are some types of neural network computations that a photonic device can't perform, requiring the use of off-chip electronics or other techniques that hamper speed and efficiency.

Building on a decade of research, scientists from MIT and elsewhere have developed a new photonic chip that overcomes these roadblocks. They demonstrated a fully integrated photonic processor that can perform all the key computations of a deep neural network optically on the chip.

The optical device was able to complete the key computations for a machine-learning classification task in less than half a nanosecond while achieving more than 92 percent accuracy — performance that is on par with traditional hardware.

The chip, composed of interconnected modules that form an optical neural network, is fabricated using commercial foundry processes, which could enable the scaling of the technology and its integration into electronics. In the long run, the photonic processor could lead to faster and more energy-efficient deep learning for computationally demanding applications like lidar, scientific research in astronomy and particle physics, or high-speed telecommunications.

"There are a lot of cases where how well the model performs isn't the only thing that matters, but also how fast you can get an answer. Now that we have an end-to-end system that can run a neural network in optics, at a nanosecond time scale, we can start thinking at a higher level about applications and algorithms," says Saumil Bandyopadhyay '17, MEng '18, PhD '23, a visiting scientist in the Quantum Photonics and AI Group within the Research Laboratory of Electronics (RLE) and a postdoc at NTT Research, Inc., who is the lead author of a paper on the new chip.

Bandyopadhyay is joined on the paper by Alexander Sludds '18, MEng '19, PhD '23, Nicholas Harris PhD '17, and Darius Bunandar PhD '19; Stefan Krastanov, a former RLE research scientist who is now an assistant professor at the University of Massachusetts at Amherst; Ryan Hamerly, a visiting scientist at RLE and senior scientist at NTT Research; Matthew Streshinsky, a former silicon photonics lead at Nokia who is now co-

founder and CEO of Enosemi; Michael Hochberg, president of Periplous, LLC; and senior author Dirk Englund, a professor in the Department of Electrical Engineering and Computer Science, principal investigator of the Quantum Photonics and Artificial Intelligence Group and of RLE. The research appears in Nature Photonics.

Machine learning with light

Deep neural networks are composed of many interconnected layers of nodes, or neurons, that operate on input data to produce an output. One key operation in a deep neural network involves the use of linear algebra to perform matrix multiplication, which transforms data as it is passed from layer to layer. But in addition to these linear operations, deep neural networks perform nonlinear operations that help the model learn more intricate patterns. Nonlinear operations, like activation functions, give deep neural networks the power to solve complex problems.

In 2017, Englund's group, along with researchers in the lab of Marin Soljačić, the Cecil and Ida Green Professor of Physics, demonstrated an optical neural network on a single photonic chip that could perform matrix multiplication with light.

But at the time, the device couldn't perform nonlinear operations on the chip. Optical data had to be converted into electrical signals and sent to a digital processor to perform nonlinear operations. "Nonlinearity in optics is quite challenging because photons don't interact with each other very easily. That makes it very power consuming to trigger optical nonlinearities, so it becomes challenging to build a system that can do it in a scalable way," Bandyopadhyay explains. They overcame that challenge by designing devices called nonlinear optical function units (NOFUs), which combine electronics and optics to implement nonlinear operations on the chip.

The researchers built an optical deep neural network on a photonic chip using three layers of devices that perform linear and nonlinear operations.

A fully-integrated network

At the outset, their system encodes the parameters of a deep neural network into light. Then, an array of programmable beamsplitters, which was demonstrated in the 2017 paper, performs matrix multiplication on those inputs. The data then pass to programmable NOFUs, which implement nonlinear functions by siphoning off a small amount of light to photodiodes that convert optical signals to electric current. This process, which eliminates the need for an external amplifier, consumes very little energy.

"We stay in the optical domain the whole time, until the end when we want to read out the answer. This enables us to achieve ultra-low latency," Bandyopadhyay says. Achieving such low latency enabled them to efficiently train a deep neural network on the chip, a process known as in situ training that typically consumes a huge amount of energy in digital hardware.

"This is especially useful for systems where you are doing in-domain processing of optical signals, like navigation or telecommunications, but also in systems that you want to learn in real time," he says. The photonic system achieved more than 96 percent accuracy during training tests and more than 92 percent accuracy during inference, which is comparable to traditional hardware. In addition, the chip performs key computations in less than half a nanosecond.

"This work demonstrates that computing — at its essence, the mapping of inputs to outputs — can be compiled onto new architectures of linear and nonlinear physics that enable a fundamentally different scaling law of computation versus effort needed," says Englund. The entire circuit was fabricated using the same infrastructure and foundry processes that produce CMOS computer chips. This could enable the chip to be manufactured at scale, using tried-and-true techniques that introduce very little error into the fabrication process.

Scaling up their device and integrating it with real-world electronics like cameras or telecommunications systems will be a major focus of future work, Bandyopadhyay says. In addition, the researchers want to explore algorithms that can leverage the advantages of optics to train systems faster and with better energy efficiency. This research was funded, in part, by the National Science Foundation, the Air Force Office of Scientific Research, and NTT Research.

Paper: *"Single-chip photonic deep neural network with forward-only training"*
https://www.nature.com/articles/s41566-024-01567-z

➤ Tim Dunn and Doug Jones of the U.S. Naval Health Research Center and International Fabric Machines personnel wear computing base layer garments in the Canadian Arctic in support of Operation Musk Ox II, a monthlong winter research mission covering 1,000 kilometers. Credit: Courtesy of the researchers

Vacuum systems: a guide to turnkey projects

When it comes to implementing vacuum systems in industrial settings, the route you take can significantly impact the efficiency, cost, and success of your project. Turnkey projects offer a streamlined solution, with a single company managing the entire process from conception to completion.

BY BUSCH

WHILE THERE are numerous advantages, it is important to also consider potential drawbacks and how to mitigate them. This guide explores how to enhance the benefits of a turnkey vacuum system project whilst mitigating potential drawbacks.

Benefits of turnkey projects

One-stop shop

Turnkey projects provide convenience by allowing customers to work with a single company, avoiding the need to coordinate with multiple suppliers and contractors. This saves time, reduces confusion, and streamlines the project process. Your supplier should serve as the single point of contact during a turnkey project, ensuring a cohesive and seamless experience from start to finish.

Reduced costs

Turnkey projects often result in lower costs because solution providers typically have strong supplier relationships and greater buying power, allowing them to negotiate better prices. Additionally, fixed-cost turnkey projects help mitigate financial uncertainties. Look for a supplier that can offer cost-effective solutions by handling all aspects of the project for a fixed fee.

➤ Turnkey vacuum systems from conception to completion offer a practical and efficient approach for businesses seeking to optimize their operations. Source: Busch Group.

Reduced lead time
Turnkey projects are usually faster to complete because design, procurement, and construction can occur concurrently. This allows customers to benefit from their investment sooner. A supplier with comprehensive project management capabilities will help to reduce project timelines, delivering results efficiently.

Improved quality
Turnkey projects often result in improved quality because the responsible company has control over both design and construction, minimizing the misunderstandings or mistakes that often arise when multiple providers are involved. With this comprehensive control, the final system consistently meets and frequently surpasses customer expectations, delivering a vacuum system of exceptional quality.

Single point of responsibility
A single company being responsible for the finished product reduces the risk of finger-pointing or blame-shifting. Your supplier should take full accountability for project results, providing customers with peace of mind and a reliable point of contact for any issues that arise.

Common concerns and misconceptions about turnkey projects

Limited control
Customers might feel they have limited control over the design and construction process in turnkey projects. A competent supplier should address this by including a detailed consultation and analysis to ensure all needs are understood, followed by a collaborative design process where local engineers design the solution in close cooperation with the customer.

Reduced flexibility
Turnkey projects can be less flexible, making changes difficult once the project is underway. To mitigate this, look for a supplier with a project philosophy that prioritizes flexibility, provides prompt feedback, and presents options for any change requests to keep the project moving efficiently.

Dependence on turnkey solution provider
Customers depend on the turnkey provider for a high-quality, reliable solution. If the provider fails to deliver, they may face subpar results or need to restart the project entirely. To ensure optimal vacuum system performance, choose a supplier with highly skilled experts, advanced sizing tools, and a proven track record of successful installations for the customer's application and industry. This ensures both reliability and peace of mind throughout the process.

Value for money of subcontracting project management
While handling projects internally may seem cost-effective, it's important to consider the hidden costs of doing so. Opting to manage key projects in house may divert employees from their core activities, potentially reducing productivity in essential business areas. Moreover, in-house teams may lack the specialized skills, experience and resources needed to handle complex vacuum system projects efficiently. Subcontracting project management to an experienced supplier allows businesses to leverage expert knowledge, tools, and industry-specific experience, ultimately leading to a more streamlined project process and fewer unforeseen issues.

Difficulties achieving the ideal project scope
Turnkey projects can limit scope options if a supplier is reluctant to customize solutions. A collaborative approach ensures that customers have control over defining the project scope, optimizing value, and tailoring solutions to specific needs. Additionally, customers can often find selecting the best solution for their needs challenging. Consider choosing a supplier that can demonstrate the value of any options presented through return-on-investment calculations, showcasing the efficiency and effectiveness of each.

Lack of transparency during design and construction
Turnkey projects can sometimes lack transparency, making it difficult for customers to understand progress. A collaborative approach to projects includes clear communication and regular updates throughout all stages, particularly during the design and build process.

Conclusion
In conclusion, turnkey vacuum systems offer a practical and efficient approach for businesses seeking to optimize their operations. By streamlining processes, reducing costs, and providing a single point of accountability, turnkey solutions address many of the challenges associated with complex industrial projects. However, the success of a turnkey project depends significantly on choosing a partner that balances efficiency with flexibility, collaboration, and a commitment to quality.

As a leader in turnkey vacuum solutions, the global Busch Group is uniquely positioned to deliver on these promises. Busch has a comprehensive approach that encompasses the full project lifecycle, from initial design consultation through to installation and beyond, ensuring that every detail aligns with client needs and industry standards. With extensive experience, advanced engineering tools, and a global track record of successful implementations, Busch ensures high-quality outcomes that meet clients' operational demands and exceed expectations. By choosing the Busch Group – comprising the portfolio of its three brands Busch Vacuum Solutions, Pfeiffer Vacuum+Fab Solutions and centrotherm clean solutions – customers gain not only a turnkey solution but also a dedicated partner, capable of maximizing the efficiency, reliability, and overall value of their vacuum system projects.

Drip by drip: semiconductor water management innovations

IDTechEx forecasts water usage in semiconductor manufacturing to double by 2035

BY THOMAS BITHELL, TECHNOLOGY ANALYST AT IDTECHEX

NOT ONLY does semiconductor manufacturing require large volumes of energy, chemicals, and silicon wafers, it also requires vast volumes of water. IDTechEx's latest report, "Sustainable Electronics and Semiconductor Manufacturing 2025-2035: Players, Markets, Forecasts", forecasts water usage across semiconductor manufacturing to double by 2035, as demand for integrated circuits continues to rise. In 2023 alone, semiconductor giant TSMC reported consumption of a staggering 101 million m3 of water, highlighting the scale of thirst in this fast-growing sector.

Furthermore, as node technology advances, so do the number of manufacturing process steps, and the usage of single wafer tools instead of batch tools, making the task of reducing water usage both challenging and even more critical. With many semiconductor fabs located in areas of high-water scarcity, such as Taiwan and Arizona, it is vital that semiconductor manufacturers take action to mitigate this huge consumption as part of the wider search for sustainable electronics.

Water management for semiconductor manufacturers is complex, propagated by the extreme purity requirements for the water used in manufacturing, giving it the name Ultra-Pure Water (UPW). However, water management techniques being implemented have the potential to mitigate water scarcity fears whilst also reducing operational costs.

Increasing volumes of reused water

Most semiconductor manufacturers now recycle or reuse water in some capacity, with annual targets to increase current levels of water reuse and combat increasing water withdrawal rates. Many companies such as NXP, Onsemi, and TI now reuse wastewater in their cooling towers. Reprocessing wastewater back into UPW is more difficult, but implementing new water treatment systems will be necessary to achieve sustainability in water use in semiconductor manufacturing. SK Hynix increased its volume of reused water by 51% between 2020 and 2023, partly motivated by water stress classification of 3 fabs as 'High' or 'Medium-high'. This is expected to also reduce operational costs through reduced municipal water consumption.

Efficiency of water use

Process optimization can also reduce water usage. Many semiconductor manufacturers have cited a reduction in water per wafer as a key target

for sustainability and to negate the risk of water shortages. This has been an issue for some, as the increased demand and complexity of wafers required has increased water use per wafer for companies such as SMIC. Reducing consumption per wafer becomes increasingly difficult with advancing node technologies, which often require increasing numbers of process steps.

However, simply reducing rinse times can result in large savings. GlobalFoundries reduced their rinse time from 10 minutes to 5 minutes after etching, resulting in an annual water saving of 10,000 m3, and there are many more examples in the report.

Diversification of water sources

Negation of water scarcity risk can come through diversification of water sources. Installing facilities such as rainwater collection may reduce operational costs due to a decreased requirement for municipal water. Tower Semiconductor has utilized the dehumidification of air required for the dry indoor environment in their factory in Texas. SMIC have also utilized condensate from air conditioning alongside rainwater collection to reduce municipal water consumption and associated costs.

These techniques may only recover a small fraction of total water usage but could still be invaluable. Larger usage could be obtained from seawater, with desalination employed in the Hsinchu TSMC plant. Where fabs are located close to the coast, utilization of onsite desalination could solve many fears surrounding sustainable water usage, although this would require high energy consumption.

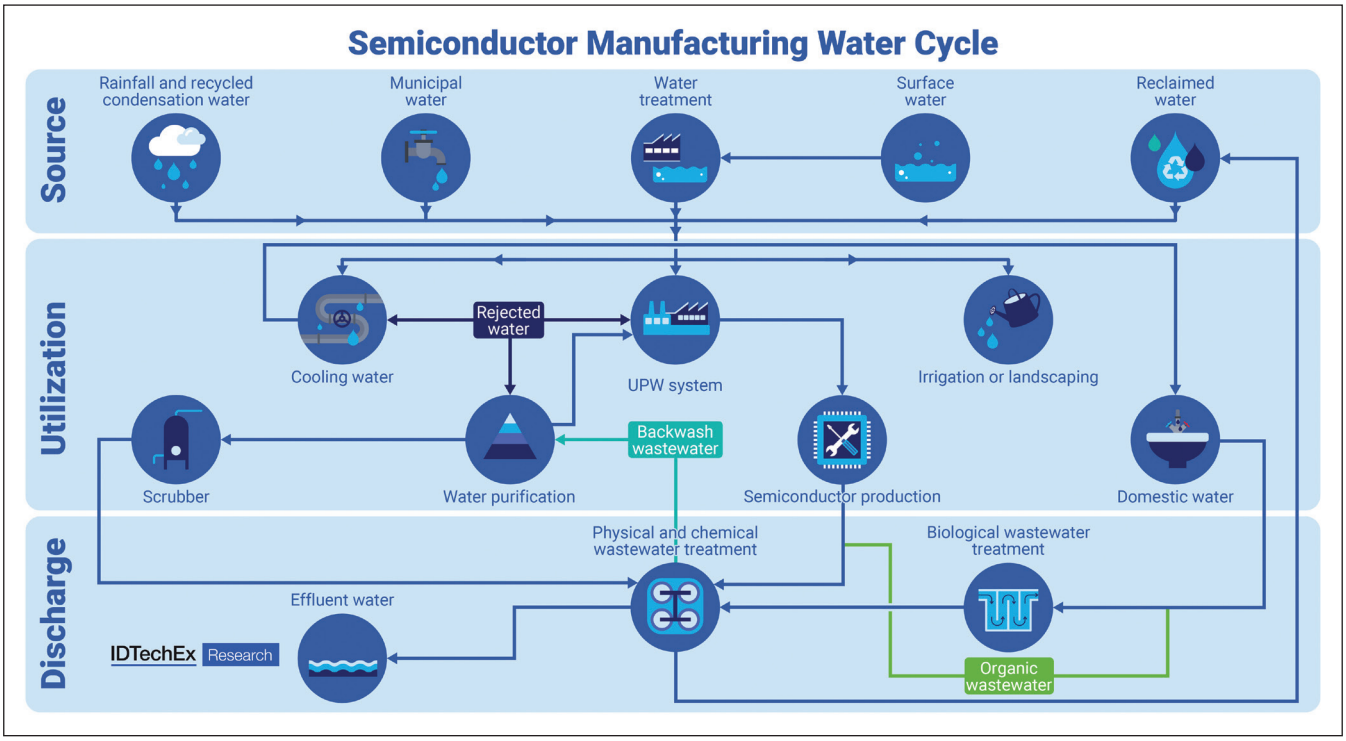
Categorisation of wastewater

Categorisation and separation of wastewater can lead indirectly to increased water reuse. This is because it enables much more efficient treatment processes. Many processes may introduce specific contaminants to the water, which can be treated with simpler water treatment. Wet processing tool provider SCREEN can now implement drain segregation within its machines to enable the categorisation of wastewater. Winbond uses 20 different pipelines to ensure no cross-contamination and allows for individual treatment of contaminants. This could also give the potential for recycling the contaminants contained within the wastewater, which could also be beneficial economically.

Categorisation and separation of wastewater can lead indirectly to increased water reuse. This is because it enables much more efficient treatment processes. Many processes may introduce specific contaminants to the water, which can be treated with simpler water treatment

Further sustainable semiconductor manufacturing insights

All of the strategies described above have the potential to benefit both the environment and the profit of the manufacturer through reduced water consumption. In many cases, reduced consumption of energy, chemicals and materials can be desirable on multiple fronts for electronics manufacturers seeking to improve sustainability and reduce operational costs.



➤ A simplified illustration of the water system implemented during semiconductor manufacture. Source: IDTechEx

From lab to fab

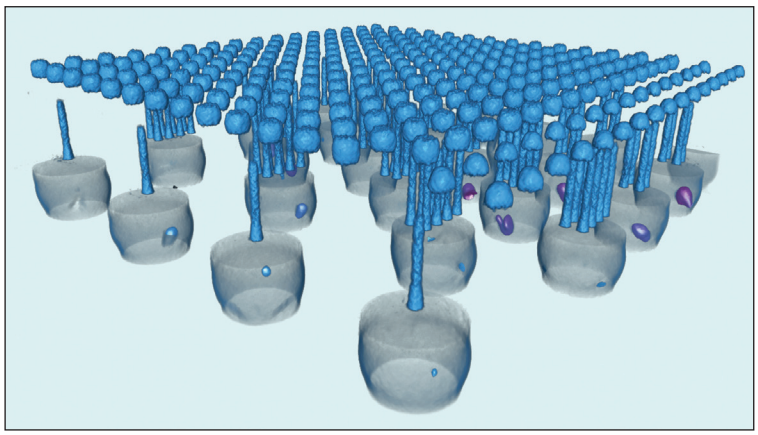
Solving systematic yield issues with next generation 3D X-ray

With the increasing adoption of 2.5D and 3D ICs in semiconductor manufacturing, the sophistication of packaging design is on the rise, highlighting the importance of robust quality assurance practices in bringing these complex architectures to market.

BY COMET YXLON

WITH TRENDS such as miniaturization, or the ever-growing hype around AI, driving demand for increased performance, the next generation of chips are pushing the boundaries of functionality within increasingly compact volumes. This shift raises a host of new challenges for manufacturers, not just in the speed required to stay ahead in a competitive market, but also in managing the higher manufacturing and material costs associated with more complex structures. To tackle this, manufacturers must adopt comprehensive inspection strategies to maintain a competitive edge. Prompt identification and resolution of issues throughout the design and manufacturing phases are crucial for efficient production scaling, improved yield, and faster market entry.

Historically, non-destructive testing methods, such as 2D X-ray, have lacked both the speed and resolution to find defects within the highly specialized parameters of advanced packaging, particularly for applications that are production-ready, however, with the new generation of 3D X-ray, supported by AI-powered defect recognition, this is about to change.



➤ Figure 1. A rendering of a commercially available CPU showcasing C4 bumps (diameter: 65µm) with visible voids, TSVs and microbumps (diameter: 20µm). All image property rights remain with Comet Yxlon and images are not to be copied or distributed.

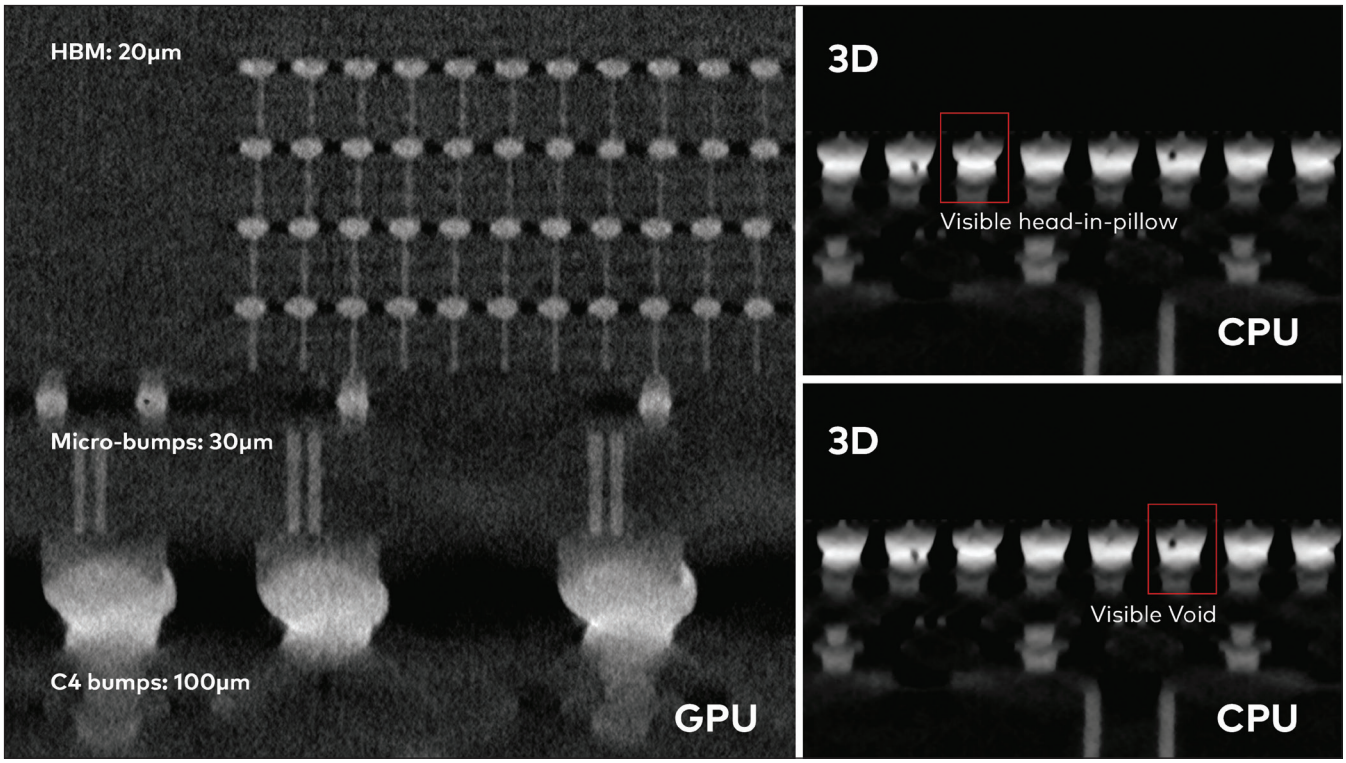
3D X-ray and AI Powered Defect Recognition: A dynamic duo

Advancements in 3D X-ray technology, and in the supporting software, such as those shown in the Comet Yxlon CA20, have the promise to revolutionize the inspection process for 3D ICs. The ability to detect even the smallest defects with precision and speed provides manufacturers with valuable insights to improve yield and quality, without sacrificing time on the production line. The detailed information extracted from captured images goes far beyond visual inspection, allowing for informed decision-making and enabling manufacturers to address systemic issues, such as voids in solder bumps or “head-in-pillow” defects, before they take hold.

The below example of a CPU captured with Comet Yxlon’s CA20 showcases the capability of modern 3D X-ray technology to reveal intricate details, including defects as small as 10 microns in diameter. The speed at which these scans can be performed highlights the efficiency of the technology in providing rapid and accurate results.

Moreover, the ability to generate “virtual slices” from reconstructed 3D volumes of multi-layered chips such as GPUs allows users to visualize cross-sections of the different layers within, such as C4 bumps, interposer bumps, and high-bandwidth memory (HBM) bumps. This level of detail would be challenging to achieve with traditional optical inspection or 2D X-ray methods due to the stacked nature of the layers obscuring underlying features.

Although capturing high-resolution images is important, the real strength of today’s 3D X-ray technology lies in its AI-powered software capabilities. Software tools like Comet Yxlon’s CoS Insights package can quickly identify and assess



➤ Figure 2: Left, virtual slice of a reconstructed X-ray scan of a commercially available GPU with 100µm C4 bumps, 30µm microbumps and 20µm high bandwidth memory bumps. Right, virtual slice of a reconstructed X-ray scan of a commercially available CPU with ca 65µm C4 bumps. All image property rights remain with Comet Yxlon and images are not to be copied or distributed

defects, such as solder bump misalignments and head-in-pillow issues, analyzing their size and severity. By evaluating critical parameters such as bump shift, die tilt, and the probability of defect occurrence, this technology offers a thorough assessment of the component's status.

Integrating 3D X-ray into the Fab environment

All of this highly detailed information can provide incredible insight into a chip's potential performance, however, in the context of a new product introduction (NPI), even small optimizations early in the process can have a significant effect on yield further down the line. It is therefore crucial that any insights into product quality can be directly fed back into the production process to improve.

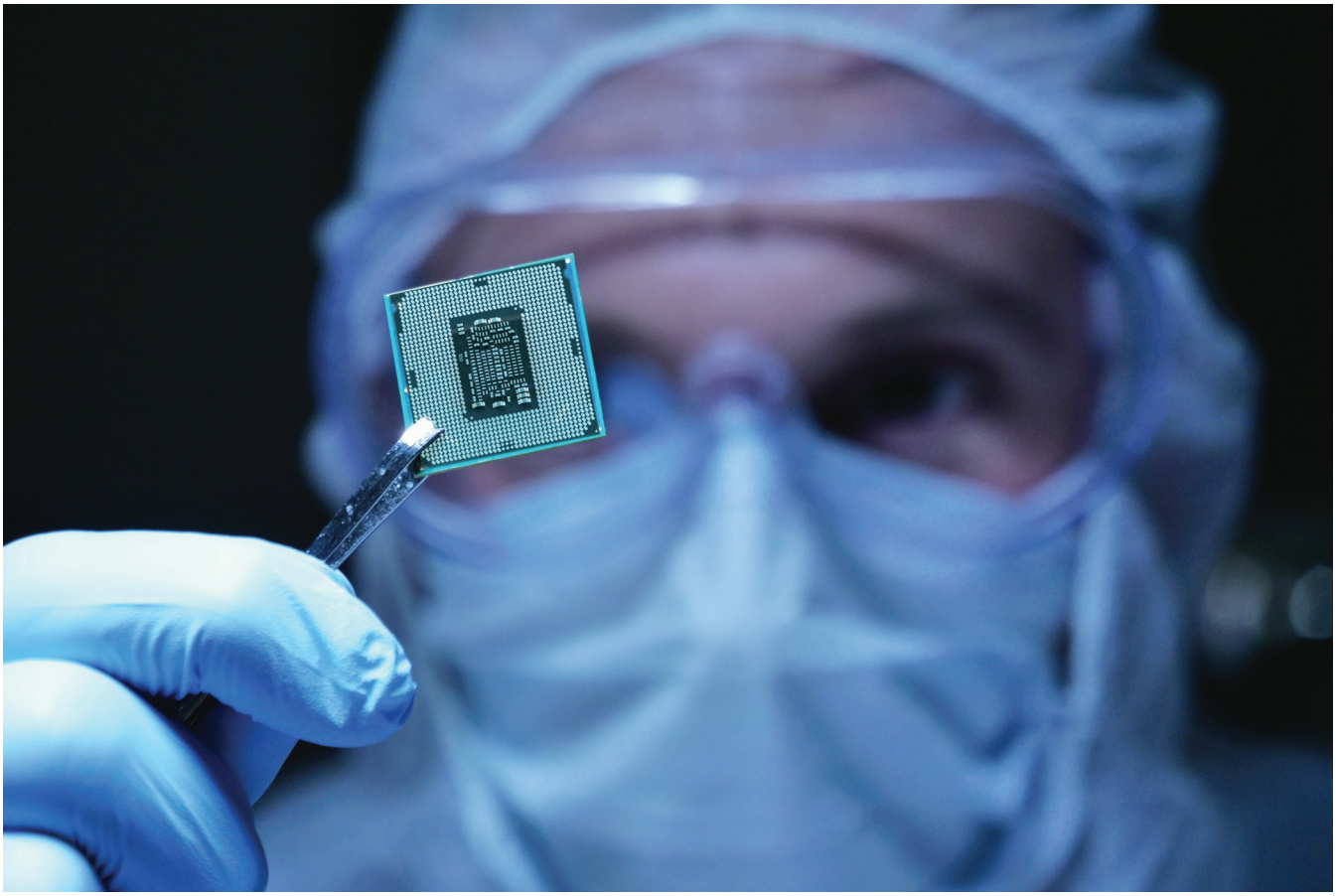
That is where the next generation Comet Yxlon CA20 comes in. Now updated with automatic loading and unloading capabilities with an integrated EFEM loader, the CA20 ensures a smooth and continuous operation without the need for manual intervention. By seamlessly integrating into the Fab production line, the CA20 offers manufacturers real-time monitoring of production quality, identifying trends and potential issues early on, allowing manufacturers to take proactive measures and ensure consistent product quality.

With wizard-guided functions and automated inspection workflows, including one-click operation, operators can quickly learn how to use the system effectively. At the same time, the advanced hardware ensures reliable measurements are given, even at the shortest scan times, delivering results in a machine-readable format for easy data analysis and interpretation. These results are then analyzed for key defect parameters automatically using powerful AI-based software in compliance with SECS/GEM standards, ensuring consistency and accuracy in defect identification and reporting.

And there are further software innovations too. Alongside defect recognition, the CA20 comes equipped with smart tools such as our Batch Manager package, which enables the scanning of multiple chips at once, flexibly organizing scan results by part IDs, while the Dose Manager package continuously monitors and tracks the X-ray dose that the sample is subjected to, taking into account the tube power and the distance to the sample to avoid damage to sensitive components.

Main takeaways

Maintaining competitiveness, managing costs, and accelerating time-to-market within today's complex chip world relies on a comprehensive inspection strategy. By including advanced technologies like 3D X-ray inspection, especially coupled with AI-powered defect recognition, manufacturers can enhance yield, quality, and efficiency not just throughout the design and research phase, but even within on the production line.



Synopsys teams up with SEMI Foundation

Synopsys, Inc. and the SEMI Foundation have signed a Memorandum of Understanding (MoU) at Synopsys' corporate headquarters in Sunnyvale, Califrnia to advance workforce development within the semiconductor chip design sector.

IT'S PREDICTED the global industry will need to fill over one million additional semiconductor jobs by 2030, equivalent to 100,000 jobs annually highlighting the crucial need for workforce development programs. Collaborations like this one are essential to bridging the chip design talent gap and shaping the innovators of tomorrow.

Together, Synopsys and SEMI Foundation will engage in opportunities to collaborate on education and training programs with academic institutions and industry experts to enhance chip design workforce development both in the United States and internationally. The two organizations will also jointly develop specialized education and training programs designed for K-12 students, academic institutions, and military veterans, providing support and resources across the talent development spectrum.

As a global silicon to systems design leader, Synopsys, through its SARA (Synopsys Academic & Research Alliances) program, has been an active participant in workforce development activities worldwide. SARA empowers the workforce of tomorrow by enabling access to cutting-edge technologies, developing shared programs, and partnering on advanced collaborations to support universities in building a diverse semiconductor workforce ready to invent the technology of the future. This collaboration with the SEMI Foundation will strengthen the pipeline of skilled talent to benefit the global semiconductor ecosystem and align with Synopsys' goal to be the preferred technology partner-of-choice for workforce development.

"I have been honored to be a part of the SEMI Foundation Board of Trustees for over five years. This partnership has been instrumental in driving forward a shared vision for a diverse and skilled workforce in the microelectronics sector. By leveraging our combined expertise and resources, we aim to make a tangible impact on the industry's ability to attract, develop, retain, and advance an inclusive and skilled workforce," said Katy Crist, Director of Workforce Development at Synopsys and SEMI Foundation Board of Trustees Member.

"Workforce development is critical for driving the semiconductor industry's continued growth and innovation," said Shari Liss, Vice President, Global Workforce Development & Initiatives at SEMI. "We are excited to announce our strategic partnership with Synopsys to advance education and training initiatives that engage, inform, and inspire the next generation of high-tech talent in the United States and abroad. Launching in 2025, our first program will focus on training students, educators, and military service members transitioning to civilian careers to expand participation in the chip design sector. Through this collaboration, the SEMI Foundation will further its mission to foster economic opportunity and equip semiconductor companies with the skilled talent they need to succeed."

SEMI Energy Collaborative releases Singapore recommendations

The SEMI Energy Collaborative today publicly released its analysis and report: Challenges and Potential Solutions for Acceleration of Low-Carbon Energy Deployment in Singapore. Now available for download, the report combines input from SEMI and its Energy Collaborative sponsors and suggests solutions for policymakers, low-carbon energy (LCE) developers, and semiconductor industry companies to further increase the pace and scale of access.

The report references the International Energy Agency, noting that as global tech giants and other companies set net-zero emission targets for their growing operations and supply chains, Singapore needs to expand its access to LCE to meet environmental needs and maintain the global competitiveness of its export industries. Singapore's semiconductor industry contributes more than 9% of the nation's GDP and 11% of the global chip output. By 2035, Singaporean companies aim to adopt 21 to 26 TWh of LCE annually, approximately 30% of the country's total power consumption. However, it is difficult for companies to source the LCE they need, and future projections indicate challenges.
The Energy Collaborative has identified six key areas of LCE policy-related actions for Singapore. Each recommendation is supported by detailed analysis of current and historical market conditions. In summary, the EC recommends the following strategies for scaling up LCE adoption:

- Signing an energy import declaration with neighboring countries
- Expanding the role of Singapore's transmission system operator (TSO) to include ownership of electricity import infrastructure
- Establishing a "one-stop shop" for import plan permits
- Leveraging the Future Energy Fund to support the adoption of low-carbon alternatives
- Maximizing Singapore's solar potential and providing outlook certainty
- Developing a robust ASEAN green hydrogen ecosystem to satisfy the long-term clean energy needs for Singapore

"SEMI and our Energy Collaborative sponsors recently presented our recommendations to the Singapore Ministry of Trade & Industry, as well as the Energy Market Authority, and engaged in very productive discussions," said Dr. Mousumi Bhat, Vice President, SEMI Global Sustainability. "Alongside key members of the semiconductor value-chain, we will continue to hold regular dialogues to explore progress and new opportunities to expand LCE in the Republic of Singapore."

The Energy Collaborative aims to reduce global semiconductor ecosystem carbon emissions as well as understand and clear regulatory and market-based roadblocks that hinder installing and procuring low-carbon energy sources in the Asia-Pacific region. The Energy Collaborative partners with civil society and other organizations which share similar objectives to leverage expertise and strengthen the voices calling for expanded access to LCE.

Singapore is the fourth market report released and follows South Korea, Japan and Taiwan.

Worldwide silicon wafer shipments and revenue start recovery

In the second half of 2024, worldwide silicon wafer demand started to recover from the industry downcycle seen in 2023, the SEMI Silicon Manufacturers Group (SMG) reported in its year-end analysis of the silicon wafer industry. Worldwide silicon wafer shipments in 2024 decreased 2.7% to 12,266 million square inches while wafer revenue

Annual Silicon* Industry Trends

	2020	2021	2022	2023	2024
Area Shipments (MSI)	12,407	14,165	14,713	12,602	12,266
Revenues ($Billion)	11.2	12.6	13.8	12.3	11.5

Source: SEMI (www.semi.org), February 2025

**Data cited in this release include polished silicon wafers, including those used as virgin test wafers, as well as epitaxial silicon wafers, and non-polished silicon wafers shipped by the wafer manufacturers to end users. Shipments are for semiconductor applications only and do not include solar applications.*

contracted 6.5% to $11.5 billion over the same period. In 2024, a broad-based inventory correction was slower due to the weak end demand from the higher volume segments impacting fab utilization rates and wafer shipments to specific applications. The recovery is expected to continue into 2025 with stronger improvements toward the second half of the year.

"Generative AI and new data-center construction has been a driver for the most advanced foundry and memory devices such as High Bandwidth Memory (HBM), but most other end markets are still recovering from excess inventory," said Lee Chungwei (???), Chairman of SEMI SMG and Vice President and Chief Auditor at GlobalWafers. "As noted by many customers in their earnings statements, the industrial semiconductor market is still in a strong inventory correction, and this has impacted silicon wafer shipments worldwide."

Silicon wafers are the fundamental building material for the majority of semiconductors, which are vital components of all electronic devices. The highly engineered thin disks, produced in diameters of up to 300 mm, serve as the substrate material on which most semiconductor devices, or chips, are fabricated.

The SMG is a sub-committee of the SEMI Electronic Materials Group (EMG) and is open to SEMI members involved in manufacturing polycrystalline silicon, monocrystalline silicon or silicon wafers (e.g., as cut, polished, epi). The SMG facilitates collective efforts on issues related to the silicon industry including the development of market information and statistics about the silicon industry and the semiconductor market.

Global manufacturing industry reports solid Q4 2024

The global semiconductor manufacturing industry closed 2024 with strong fourth quarter results and solid year-on-year (YoY) growth across most of the key industry segments, SEMI announced today in its Q4 2024 publication of the Semiconductor Manufacturing Monitor (SMM) Report, prepared in partnership with TechInsights. The industry outlook is cautiously optimistic at the start of 2025 as seasonality and macroeconomic uncertainty may impede near-term growth despite momentum from strong investments related to AI applications.

After declining in the first half of 2024, electronics sales bounced back later in the year resulting in a 2% annual increase. Electronics sales grew 4% YoY in Q4 2024 and are expected to see a 1% YoY increase in Q1 2025 impacted by seasonality.

Integrated circuit (IC) sales rose by 29% YoY in Q4 2024 and continued growth is expected in Q1 2025 with a 23% increase YoY as AI-fueled demand continues boosting shipments of high-performance computing (HPC) and datacenter memory chips.

Similar to electronics sales, semiconductor capital expenditures (CapEx) decreased in the first half of 2024 but saw a strong rebound, particularly in the fourth quarter, resulting in 3% annual growth by the end of 2024. Memory-related CapEx continued to lead the growth surging 53% quarter-on-quarter (QoQ) and 56% YoY in Q4 2024. Non-memory CapEx also edged up in Q4 2024 showing 19% QoQ and 17% YoY improvement. Total CapEx is expected to remain strong in Q1 2025, growing 16% relative to the same period of the previous year on the strength of investments to support high bandwidth memory (HBM) capacity additions for AI deployment.

The semiconductor capital equipment segment remained resilient primarily due to increased investments into expanding leading-edge logic, advanced packaging and HBM capacity. Wafer fab equipment (WFE) spending increased 14% YoY and 8% QoQ in Q4 2024. Quarterly WFE billings are expected to be around $26 billion in Q1 2025. China's investment continues to play a significant role in the WFE market but started to subside by end of the year. Additionally, back-end equipment showed strong increases in Q4 2024 with the Test segment logging 5% QoQ growth and an impressive 55% YoY increase for the quarter, while the Assembly and Packaging segment experienced a YoY increase of 15%. Both segments are expected to show similar QoQ growth between 6-8% in Q1 2025.

In Q4 2024, installed wafer fab capacity surpassed a record 42 million wafers per quarter worldwide (in 300mm wafer equivalent), and capacity is projected to reach nearly 42.7 million in Q1 2025. Foundry and Logic-related capacity continues to show stronger increases, growing 2.3% QoQ in Q4 2024, and the segment is projected to rise 2.1% in Q1 2025 driven by capacity expansion for advanced nodes. Memory capacity increased 1.1% in Q4 2024 and is forecasted to remain at the same level in Q1 2025 driven by strong demand for HBM.

"Despite seasonality and the challenges of macroeconomic uncertainty, momentum in AI-driven investments continues to fuel expansion across key segments, including memory, capital expenditures, and wafer fab equipment," said Clark Tseng, Senior Director of Market Intelligence at SEMI. "Looking forward for 2025, the industry remains cautiously optimistic, with robust growth prospects driven by ongoing demand for high-performance computing and data center buildout."

"As we begin the year, our expectation is for stronger performance in the second half, with semiconductor sales anticipated to remain flat sequentially in the first half, followed by a notable double-digit increase in the latter half," said Boris Metodiev, Director of Market Analysis at TechInsights. "Inventory challenges persist for discrete, analog, and optoelectronic manufacturers, which will need to be addressed before we can expect widespread growth to resume."

Dedicated webinars for the silicon semiconductor industry

Using our 30+ years' experience in B2B vertical technical markets, and as the publisher of Silicon Semiconductor, we offer effective webinars, ZOOM interview and virtual events. We help you get your message, to your desired audience, by marketing to over 55,000 silicon semiconductor professionals.

In addition to organising and managing your webinar, we can also market your webinar to our specialist databases.

In a dedicated 6 week program we will promote through our magazine, newsletters, LinkedIn group and website.

We can also provide the webinar moderator, from our team of highly respected editors.

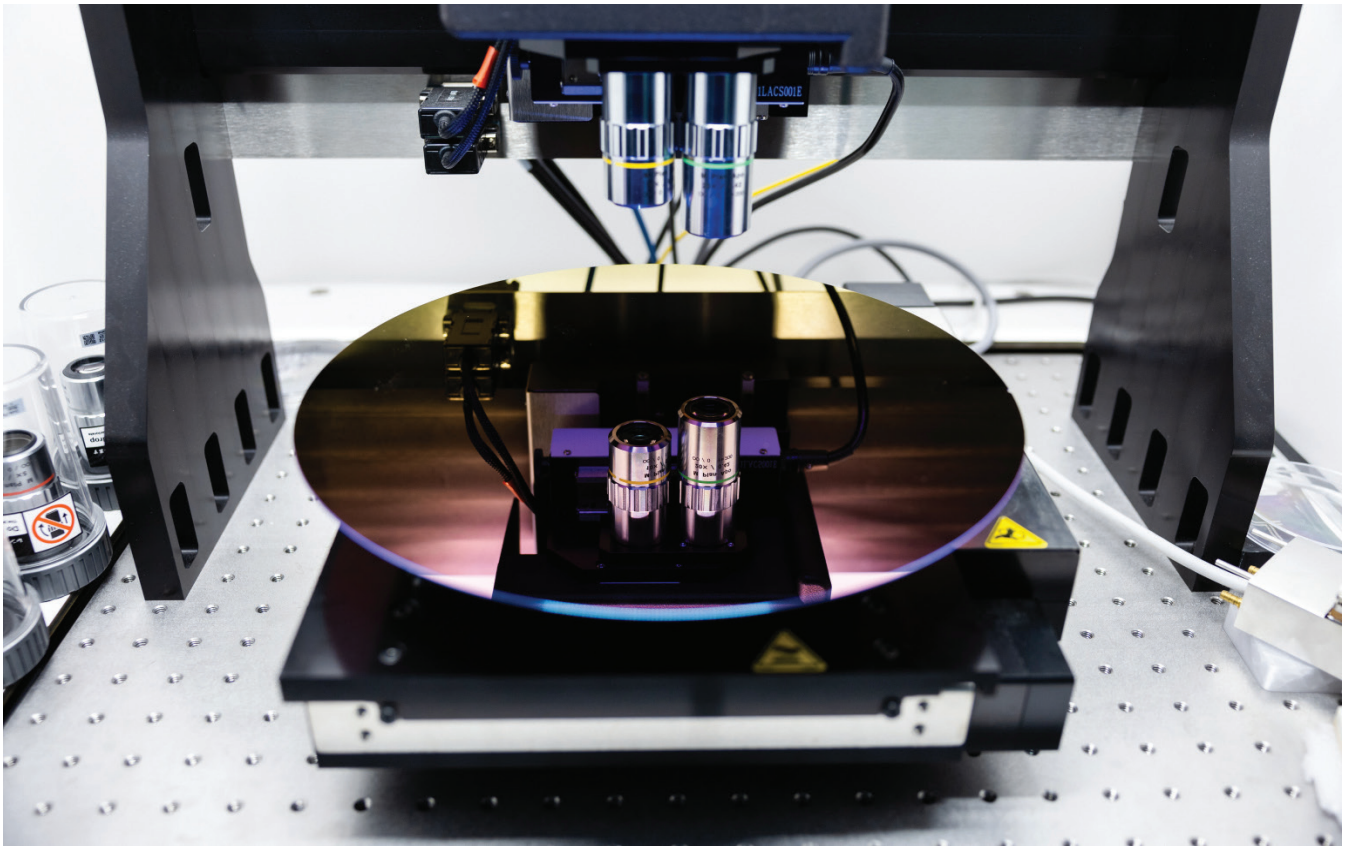
Let our editors work with you and help you with the content.

Reach Educate Influence

- **Brand Awareness**
  Increase global awareness by running sponsored webinars, Zoom interviews and virtual events
- **Lead Generation**
  Generate and mature leads through the use of online events.
- **Thought Leadership**
  Become the voice of knowledge by generating compelling content via online events

SILICON SEMICONDUCTOR

Find out how Angel Webinars can help you organise and run a webinar within the silicon semiconductor industry.
Contact: Jackie Cannon
jackie.cannon@angelbc.com
+44 (0)1923 690205



Thin film thermal metrology and its implications for electronic devices

How a new technology addresses the limitations of traditional measurement methods.

BY LASER THERMAL

SEMICONDUCTOR MANUFACTURING is an industry defined by ever-increasing demand and a constant quest for higher yield and throughput, and more fine-tuned testing processes play an important role in improving the yield and efficiency of the manufacturing process. The earlier and more precisely that defective chips or sub-standard materials can be identified, the more time and money can be saved. Once identified, defective chips can be excluded from subsequent processing that costs equipment capacity, money, and labor time. The key is identifying these defective materials, processes, and chips as early and as far upstream in the manufacturing process as possible.

In this context, our experience suggests that enhanced thermal testing capabilities for the thin film materials used in many semiconductor devices represent a valuable avenue for improvement. Furthermore, accurately measuring the thermal properties of thin films is essential for eliminating deleterious temperature rises, understanding operating limits, and designing cooling systems capable of maintaining performance while avoiding both thermal failure and costly over-specification. Understanding the thermal properties of thin film materials is crucial to maximizing performance, reliability, and manufacturing yield.

Accurately measuring the thermal properties of nanoscale thin films, however, is a substantial metrology challenge. Due to demands on throughput, a thermal resistance measurement technique must be amenable to rapid material screening along with integration into semiconductor manufacturing cycles to achieve maximal impact.

However, most traditional thermal testing methodologies cannot dependably provide exact measurements of thermal resistances on the length scales needed for semiconductor chips, nor meet the integration and throughput constraints necessary for integration into the semiconductor testing market.

In this article, we explore how a new optical measurement technique (Steady-State Thermoreflectance in Fiber Optics) can directly address the limitations of traditional thin film thermal measurement techniques.

Limitations of Traditional Thin Film Thermal Metrology Methods

Sustained thermal stress can drive a variety of different failure modes in thin film materials, which must be carefully engineered to operate within specified thermal limitations. To limit failures and accurately assess the reliability of components, semiconductor manufacturers institute rigorous procedures to test for thermal resistances. Potential modes of failure include:

- Oxide-layer faults
- Metallization defects
- Die-substrate attachment issues
- Seal failures
- Different materials with mismatched thermal expansion coefficients
- Packaging defects

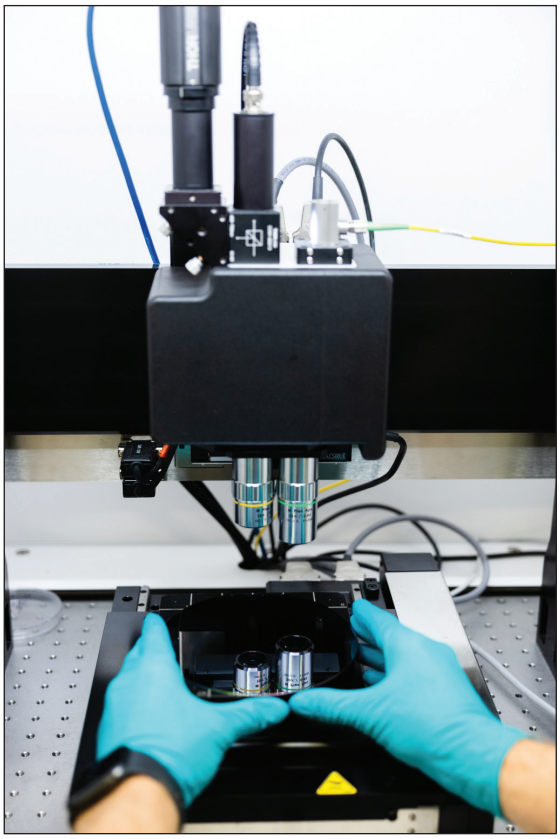
While stress screening can help establish operating limits and filter out defective devices, it does not generate precise data on how a component can dissipate heat from electrical loads. Doing so requires measuring crucial properties such as thermal resistances, but measuring these properties in the nanoscale thin films used in semiconductor devices is a substantial metrology challenge requiring specialized equipment.

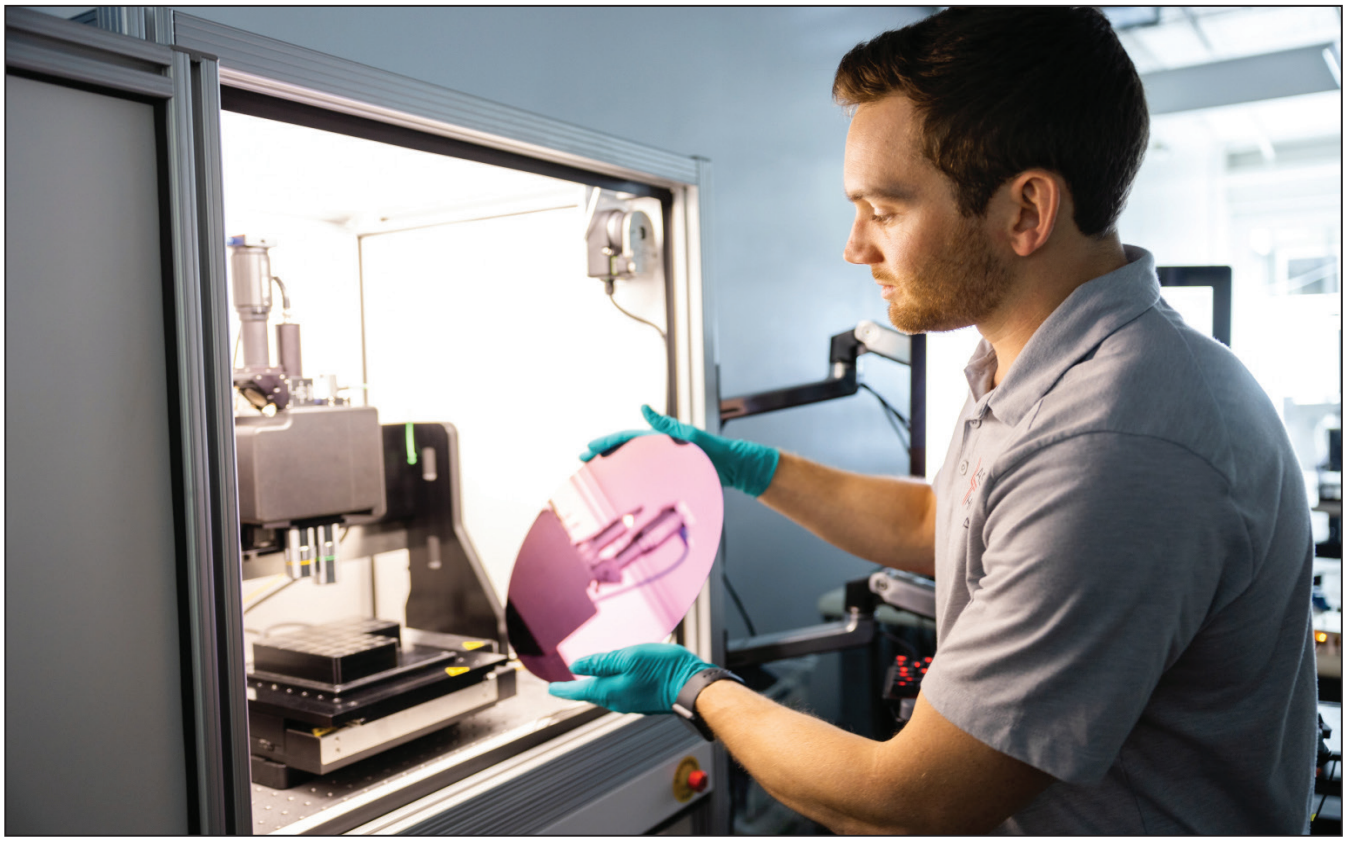
Ranging from several micrometers to less than a single nanometer in thickness, thin films create unique challenges for measuring basic thermal properties like thermal conductivity. In short, these materials are simply too thin to rely on traditional thermal measurement techniques. To make matters even worse, the thermal conductivity of thin films is strongly dependent on the film thickness and processing conditions, meaning one cannot simply “look up” the thermal conductivity of thin films in the back of a textbook. In thin films, defects and interfaces may arise during growth and heterogeneous integration that change the electron and phonon scattering events, resulting in drastically lower thermal conductivities in materials relative to their bulk counterparts. Therefore, to truly understand the thermal conductivity of a thin film in a device, one must measure the thermal conductivity of a film of the same thickness, grown under the same conditions.

In most traditional applications, sensors such as thermocouples or resistive thermometers can be used to capture measurements of the temperature gradients or changing heat flux that result as heat is applied to a material (measurements which can be directly related to thermal conductivity via Fourier’s law or the heat equation). Thin film materials, however, are often substantially thinner than the dimensions of the heaters and sensors used to induce the temperature gradients and capture temperature changes, respectively. This fact renders these measurement platforms unsuitable for these applications. Furthermore, the physical testing probes used in traditional measurement techniques are not amenable to the high-throughput screening techniques necessary in today’s semiconductor fabrication facilities.

> Accurately measuring the thermal properties of nanoscale thin films, however, is a substantial metrology challenge. Due to demands on throughput, a thermal resistance measurement technique must be amenable to rapid material screening along with integration into semiconductor manufacturing cycles to achieve maximal impact

For example, the material in the thermal sensor itself will contribute more to the recorded thermal resistances and temperature changes than the thin film of interest! The accurate measurement of thermal resistance and thermal conductivity of thin films requires a different approach to thermal metrology, which must achieve the substantially higher temporal/spatial resolutions demanded by these nano-meter scale materials.





With substantial margins for error on traditional thin film thermal resistance measurements, semiconductor manufacturers have traditionally resorted to derating (operating a device at less than its maximum rated power dissipation) to establish an additional margin of safety. Consequently, more accurate, precise thermal resistance measurements can directly enable semiconductor device designs that are higher performing, reliable, and more predictable.

Steady-state thermoreflectance in fiber optics: A novel approach to measuring thermal properties of thin films

Optical measurement techniques can directly address these key limitations of traditional thin film thermal metrology techniques. For example, Laser Thermal's products and testing services are anchored in Steady-State Thermoreflectance in Fiber Optics (SSTR-F), a non-contact, laser-based pump-probe technique.

This approach works by utilizing a laser to create a nano-to-microscale heating event on the surface of a sample, resulting in a steady-state temperature gradient in the sample. A secondary probe laser is then used to measure the temperature on the surface of the sample, which is altered by incrementally increasing pump powers to induce incremental temperature rises. The spot laser used in this process can be tuned to be as small as a few microns 1/e2 diameter, which, given the nanoscale localized absorption of the laser, enables SSTR-F to be used effectively to measure in-plane and through-plane (cross-plane) thermal resistances and thermal conductivities– even for nanometer-scale thin films and atomically thin interfaces. Defects, stresses, compositional differences, and changes in density and microstructure that occur during film growth and alter the subsequent thermal properties can be easily and rapidly identified via SSTR-F.

SSTR-F can provide accurate, repeatable (+/- 1.0 %) and reproducible (+/- 2.0 %) thermal conductivity measurements. This approach is also capable of fully automated, high-throughput measurements, which are crucial for the large volumes of testing required by the ever-growing semiconductor industry. Our automated, high throughput, turnkey implementation of SSTR-F can measure the thermal conductivity of materials with values ranging from 0.05 to 3,000 W/m/K. And high-throughput SSTR-F testing of multiple samples facilitates, for example, screening the thermal conductivity of different thin films processed under different conditions. Thermal mapping of planar devices can be performed to look at the spatially varying thermal resistance of chip level structures.

Looking forward, we expect that enhanced thermal metrology capabilities will only become more critical for semiconductor manufacturers. As System-on-Chip's become more tightly integrated and less repairable, pressure will only mount to improve reliability wherever possible. To keep up with global demand, new measurement techniques must be amenable to automated, high-throughput manufacturing operations. SSTR-F is strongly suited to this challenge, and plays a valuable role in helping semiconductor manufacturers continue to push engineering boundaries.

CLEAN AIR

CLEAN ROOMS

COMPONENTS

ETCH

FLOW MEASUREMENT

GAS DELIVERY SYSTEMS

GAS PURIFIERS

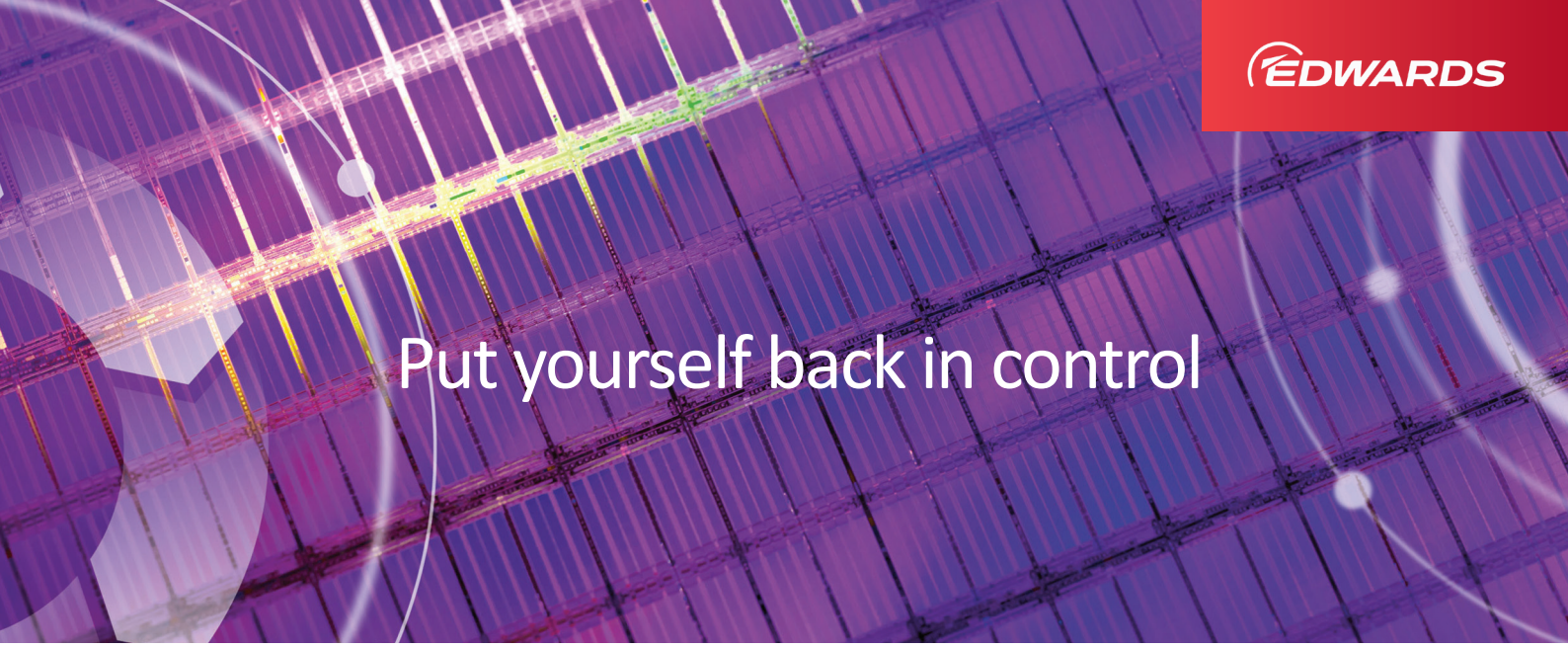
HYDROGEN GENERATORS

FLUID SYSTEMS

PLASMA TECHNOLOGY

TEST

VACUUM EQUIPMENT



Put yourself back in control

Are unplanned dowtimes dragging down your productivity? Is your Fab efficiency and TCoO being damaged by avoidable stoppages? Avoidable? How? By working with us to implement one of our core service plans you can take back control of your throughput and manage equipment with a planned service regime. Talk to us today and head towards a more productive future.

Care Spare parts plan	Maintain Parts and labour for standard maintenance	Perform Standard maintenance with upgrades included
One single purchase order and monthly billing	One single purchase order and monthly billing	One single purchase order and monthly billing
Fixed supply of parts for standard maintenance used on site annually	Preventative and routine maintenance activities, including parts and labour required for each activity	Preventative and routine maintenance activities, including parts and labour required for each activity
Basic operational support provided by our team of experts	Maintenance performed on site by our field service team for Abatement, or at our Service Technology Centres for Dry, Turbo, and Cryogenic Pumps	Maintenance performed on site by our field service team for Abatement, or at our Service Technology Centres for Dry, Turbo, and Cryogenic Pumps
The plan can be enhanced with chargeable options at additional cost, including training and troubleshooting by our service teams	Troubleshooting and operational support provided by our team of experts	Troubleshooting and operational support provided by our team of experts
	The plan can be enhanced with chargeable options at additional cost, including service exchange, upgrades, and inventory management	Can include specific upgrades or improvement components according to the contract.
		Possible to customise the plan with additional options

Edwards semiconductor *Intelligent* service

View our range of service plans at www.edwardsvacuum.com