Packaging as the last mile of semiconductor manufacturing

VOLUME 42 ISSUE III 2021

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INSIDE

News Review, Features, News Analysis, Profiles, Research Review and much more...

ENSURING IP SECURITY

Design and manufacture of today's most advanced semiconductors is increasingly complex and expensive

OMNIVISION IMAGING FRONT ROW SEATS

Digital imaging and machine vision, from a consumer perspective

LOGICAL SWITCH TO THE VERTICAL DIRECTION

Surging sales of wearable devices will drive a new era for the IC

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VIEWPOINT

By Mark Andrews Technical Editor

Shortages, solutions & surges are making mid-2021 headlines

Is the chip shortage continuing or cresting? Answers depend largely on whom one asks. Some analysts see the shortage easing already, with an end expected by late fourth quarter. Others believe relief won't arrive until early 2023. Who is correct? A lot depends on the process node, application and whether the world continues to see surges of COVID-19.

According to trade association analysts, independent researchers and major companies commenting on chip shortages, aligning supply with demand depends mostly on wafer size, node maturity, application specific requirements, and consumer demand. Answering 'when' also depends on how quickly fabs under construction come online and whether governments supporting homegrown chip making dive more deeply into new fab spending sprees.

'Spending spree' is indeed one way to characterize the capacity Gold Rush. According to the SEMI trade group, global manufacturing equipment spending will surpass (USD) $100 billion in 2022 – a new high. SEMI expects a 34 percent increase in 2021 (to $95 billion,) which follows 2020's record-setting $71.1 billion.

Some researchers are noting that the depth and widespread nature of chip undersupply is best understood by realizing that out-sized and uneven, hard-to-forecast device purchasing that began with the pandemic is continuing. While 'shortage' was first used to describe supply/demand imbalances for advanced node ICs (<10nm devices,) the gap has spread to mature nodes. Supplies of semiconductors made using mature processes (>10nm devices) are now also in shorter supply, affecting nearly every electronic product including appliances, cars, computers, industrial equipment, smartphones and TVs. Shortages once expected to ease by mid-to-late 2021 are now expected through 2022 or early 2023.

In this edition of Silicon Semiconductor we explore the importance of packaging as a means to help ensure safe deliveries of delicate microelectronic devices at a time when making certain each device reaches its intended recipient takes on ever more significance.

We also delve into digital imaging and machine vision through the expertise of OmniVision. We examine new ways to protect semiconductor IP while encouraging global collaborations from the experts at Perforce and take a look at advances Mitsubishi is making to seamlessly share data for optimized Industry 4.0 automation.

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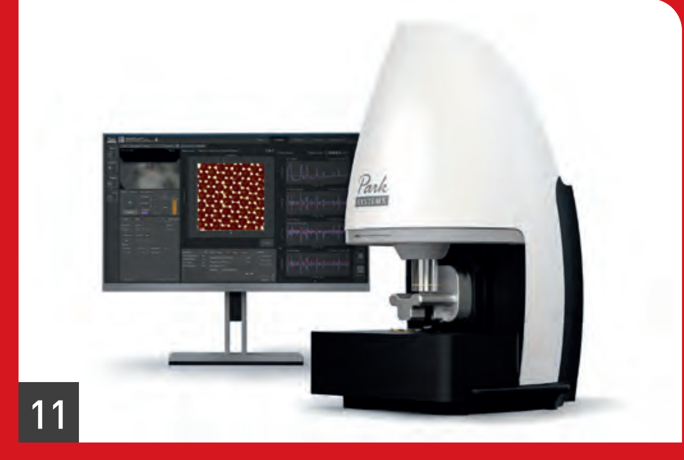

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Semiconductor IP market to reach USD $7 billion by 2027

THE GLOBAL semiconductor intellectual property (IP) market was valued at US$ 4,111.0 Million in 2019 and is expected to surpass US$ 7,103.0 Million by 2027, registering a CAGR of 8.9% during the forecast period (2020-2027), as highlighted in a report published by Coherent Market Insights.

The automotive sector is focusing on continuous innovation and the semiconductor intellectual property will continue to play a major role in the advancement of this industry. As the automotiveindustry continues to develop self-driving technology, automotive electronics are expected to play an integral role in enabling these capabilities. The safety features in today's automotive SoCs (systems-on-chip) requiressemiconductor IPs.

The growth of semiconductor intellectual property in theautomotive industry is due to increasing application of microcontroller units (MCUs), microprocessor units (MPUs), sensors, interfaces, analog integratedcircuits (ICs), and memory products in autonomous and premium cars. All major vehicle manufacturers such as Mitsubishi Motors Corporation, Renault, and Tata Motors are focusing on providing safety components in a vehicle such as high-tech sensors, cameras, advanced driver-assistance systems (ADAS), and other parts that mitigate accidents. Therefore, with launch of modern cars equipped with various features and more to come in driverless cars, semiconductor intellectual property will play a major role in facilitating further innovation.

Growing adoption of modern system on chip(SOC) designs is expected to drive the market growth during the forecast period. Semiconductor IP cores are combined with the system on-chip (SoCs) and application specific integrated circuit (ASICs) products. Such products arethen used for the production of chips, which are then installed in automobiles, MP3 players, televisions, smartphones, and others. In addition, there is rise in the demand for smart and power efficient devices, which propels demand for the SoCs. This, in turn, is projected to drive growth of the semiconductor IP market. For instance, in June 2020, Qualcomm Technologies, Inc. launched its new product 'Snapdragon 690 System-on-chip,' to support its Snapdragon 6-series processors. The Snapdragon 690 is specifically designed for 5G connectivity and supports both standalone (SA) and non-standalone (NSA) modes.

Semiconductor Intellectual Property (IP) Market - Impact of Coronavirus (Covid-19) Pandemic

COVID-19 has significantly disrupted almost all the industries including, infrastructure, automotive, manufacturing, and others. To combat COVID-19 pandemic, most of the countries have implementedlockdowns and are now easing it phase-wise and industry-wise. This has significantly impacted the manufacturing sector as the facilities across the globe were temporarily shut down. The slowdown in production by automotive OEMs due to COVID-19 crisis has resulted in demand variation for semiconductor chips. Furthermore, demand for PC/server, wired communication, and consumerproducts has dropped. Thus, consequently impacting the semiconductor intellectual property (IP) market growth. However, the demand for wireless communication has increased. Accelerated demand for cloud infrastructure tosupport distributed workforce will have a positive impact on the global semiconductor intellectual property (IP) market in the long term.

Key Trends and Analysis of the Global Semiconductor Intellectual Property (IP) Market:

- Asia-Pacific held dominant position in the global semiconductor intellectual property (IP) market in 2019 and is expected to retain its dominance throughout this period.
- North America is expected to show significant growth over the forecast period, owing to high presence of fabless companies in the US.
- Among design IP, the processor IP segment held a dominant position in the market in 2019 and is expected to retain its dominance during this period.
- Major players operating in the global semiconductor intellectual property (IP) market include Arm Holdings, Synopsys, Cadence Design Systems, Imagination Technologies, Lattice Semiconductor Corporation, CEVA, Rambus Incorporated, Silvaco, Intel Corporation, eMemory Technology, Dream Chip Technologies GmbH (Goodix Technology), VeriSilicon Microelectronics (Shanghai), Achronix Semiconductor Corporation, Open-Silicon, Dolphin Design SAS, Faraday Technology Corporation, Xilinx, Mentor, a Siemens Business, Semiconductor Manufacturing International Corp. (SMIC), Cobham Gaisler AB, Arasan Chip Systems, HDL Design House, Mixel, and TDK Corporation (InvenSense).

Park Systems announces autonomous AFM with built-in intelligence

PARK SYSTEMS, the manufacturer of Atomic Force Microscopes (AFM) just announced Park FX40, a groundbreaking autonomous atomic force microscope, infused with innovative robotics, intelligent learning features, safety features, software and specialized add-ons. Park FX40 Atomic Force Microscope is the first AFM to automate all up-front set up and scanning processes, putting the intelligent Park FX40 in a groundbreaking new class of atomic force microscope.

The new Park FX40 Atomic Force Microscope is more than just dozens of new features and upgrades – it's an overhaul in functionality while retaining the same basic design elements, enabling AFM's to think and perform essential functions completely on their own. This will allow untrained researchers to achieve a number of formerly training-intensive tasks, and trained researchers to focus on what they're best at in their specialized fields, while the menial tasks like choosing and loading the correct probes, to automatically aligning the X, Y and Z beams along the axis, take care of themselves.

"Park FX 40 features significant enhancements that are completely new tech, never before seen on an AFM," adds Yoo. Furthermore, Park FX40 has drastically upgraded many of the AFM's key aspects, including electromechanics for much reduced mechanical noise, smaller beam spot size, improved optical vision and multi snap-in sample chuck. Park FX 40 Atomic Force Microscopes are now located at key locations worldwide and will are now available for purchase.

"We are thrilled to be the first AFM user in North America to experience the Park FX40 Atomic Force Microscope, states James Hone, Professor of Mechanical Engineering at Columbia University. "As long-time users of Park AFMs, we are excited about the new features and increased capabilities in this new generation. In particular, the breakthroughs in automation of AFMs using artificial intelligence and robotics technology will dramatically boost our productivity and drive innovation across the field of nanometrology."

Park FX built in intelligence even allows users to place several samples at the onset (of the same or different types) and it will image them autonomously according to your requirements. The result is better research by obtaining publishable data easily and timely and acceleration of the research cycle for ultimate scientific and engineering success. Park FX40's unique environmental sensing self-diagnostics and head crash avoidance system ensures that Park FX40 is continuously operating at its optimum performance.

In collaboration with the expert scientists at Park's growing network of nanotechnology research centers worldwide, the product marketing team diligently worked on the design of Park FX over the last year. Our ultimate goal with developing Park FX with autonomous features is to make the researcher's job easier as they open new doors in scientific discovery."

Known for their commanding lead in semiconductor advanced automated AFM systems and bringing AFM technology into the mainstream as the premier tool for nanoscale metrology, this latest development is part of a natural progression for Park Systems as they continue to lead the world in AFM innovation.

Blaize announce $71 million Series D financing

BLAIZE, the AI computing edge and automotive computing solutions, has announced the close of a $71 million Series D round of funding. Franklin Templeton, a new investor, and Temasek, an existing investor, led the round, along with participation from DENSO and other new and existing investors.

"Blaize has demonstrated the capability to enable value creation for organizations tapping the power of AI for edge computing," said JP Scandalios, senior vice president and portfolio manager, Franklin Templeton. "We are excited to invest as Blaize leadership takes strides to realize their vision.

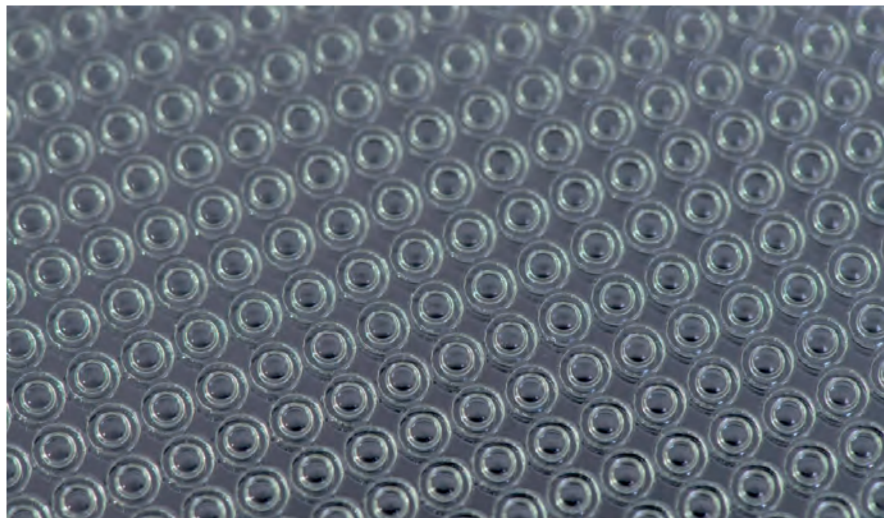
"Automotive, and numerous edge AI markets, such as retail and metro, hold tremendous potential for Blaize to expand on their early market position as the adoption of AI at the edge accelerates, creating a new wave of industrial systems. Today Blaize is delivering to customers a distinct fusion of AI hardware and AI Studio end-to- end software platform that leads the industry in productization of high-value knowledge-driven edge computing solutions."

The funding will support acceleration of the product roadmap to meet growing demand for higher performance, lower power, lower cost AI hardware and transformational AI software solutions in automotive, smart retail, smart city and industrial markets.

In 2020, Blaize successfully released and built a multi-year pipeline for the first generation Blaize AI edge computing hardware products based on the ground breaking Blaize GSP architecture, and the Blaize AI Studio end-to-end application lifecycle software platform.

EV Group launches first step and repeat mastering services for nanoimprint lithography

EV GROUP (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology, and semiconductor markets, today announced that it has established the EVG Step-and-Repeat (S&R) Mastering Shop, a new service offering to help customers accelerate the deployment of nanoimprint lithography (NIL) in high-volume manufacturing. The EVG S&R Mastering Shop™ uses EVG's own equipment and cleanroom facilities to provide contract manufacturing of large-area master templates and stamps, which are used to produce working stamps for wafer-level and panel-level NIL processing.



By eliminating the capital costs associated with owning dedicated S&R systems for master stamp fabrication, customers can more easily integrate NIL technology in their new product designs. Devices and applications benefiting from EVG's S&R NIL solutions include augmented reality waveguides, advanced micro-optics for optical sensors, micro-lenses, nanophotonics and silicon photonics. The EVG S&R Mastering Shop is a key addition to EVG's NILPhotonics® Competence Center framework, located at EVG's corporate headquarters in Austria.

Using S&R mastering, a large-area master stamp can be produced from a single-die "hard master". This S&R master can then be used to replicate tens or hundreds of working stamps, which are used to imprint the functional structures on substrates.

This replication method minimizes wear-out and risk of introducing defects to the expensive master. The ability to replicate larger master molds over ever-larger substrates -- including 300-mm wafers, panel-sized substrates and inserts for roll-to-roll (R2R) manufacturing -- allows more devices to be produced simultaneously as well as allows for the production scaling of larger individual devices without stitching. EVG is the only company to offer the complete breadth of products, services and expertise for S&R mastering and wafer-level NIL processing that enable rapid and cost-effective scaling of NIL-enabled products from R&D to high-volume production.

"EVG has pioneered the development and maturation of nanoimprint lithography with more than 20 years of experience in this innovative technology," stated Markus Wimplinger, corporate technology development & IP director at EV Group. "This year marks even more developments in NIL for EVG. Earlier this month, for example, we introduced our next-generation EVG®770NT step-and-repeat NIL system, which paved the way for large-scale master stamp fabrication for NIL volume production applications.

Now with our new S&R mastering services, EVG is eliminating even more barriers to NIL adoption for our customers by providing a one-stop shop for structured masters within a flexible and cost-effective service model. We are pleased to achieve yet another new NIL milestone by being the first company to offer S&R NIL mastering services for wafer-level and panel-level production applications."

EVG's S&R solutions offer significant yield and cost advantages compared to conventional mastering methods, such as diamond drilling, laser direct writing and electron-beam writing, which are difficult to scale up to larger substrates due to their low throughput and high cost of implementation. Incorporating the S&R process enables the use of best-performing dies and the ability to efficiently bring these high-quality patterns into production lines.

As part of EVG's new S&R mastering services offering, the company has added a new cleanroom area with dedicated S&R and metrology systems for contract services. The EVG S&R Mastering Shop utilizes EVG's newly introduced EVG770 NT step-and-repeat NIL systems, which enable large-area master stamp fabrication on substrate sizes up to 300-mm wafers and Gen-2 (370mm x 470mm) panels with industry-leading overlay accuracy and resolution. All core infrastructure is located in an access-controlled environment and operated by a dedicated team to maintain protection of customer IP.

In addition to producing master stamps, EVG also offers the ability to produce working stamps and original hard masters for customers.

Furthermore, within the framework of its NILPhotonics Competence Center, EVG also offers imprint process development, materials qualification and optimization, as well as device prototyping and pilot-line manufacturing -- all with the highest levels of confidentiality and IP protection.

Brewer Science achieves ISO 45001:2018

BREWER SCIENCE, in developing and manufacturing next-generation materials and processes for the microelectronics and optoelectronics industries, is pleased to announce the achievement of ISO 45001:2018 Occupational Health & Safety Management Systems Certification. Brewer Science is now certified in three different ISO Standards, including ISO 9001:2015 Quality, ISO 14001:2015 Environmental and now ISO 45001:2018 Occupational Health and Safety.

ISO 45001:2018 is a globally recognized occupational health and safety standard developed and published by the International Organization of Standardization (ISO). ISO developed this standard to help organizations improve employee safety, reduce workplace risks and create safer working conditions.

"Achieving ISO 45001:2018 certification exemplifies our commitment to our employees, community and customers, by continuously evaluating and improving our safety processes to ensure we exceed the highest standards in the world," said Terry Brewer, CEO and Founder of Brewer Science. "Brewer Science owes this recognition to our employees. They are the ones who continue to push the company forward, with their participation, dedication and commitment. It's evident that they want to see Brewer Science not only be a world class manufacturer, but an industry role model, advocating for innovation in safety, sustainability and quality."

Brewer Science's ISO 45001:2018 certification became effective on May 12, 2021, and was issued by Bureau Veritas Certification Holding SAS, a highly respected registrar providing certification services for Quality, Environmental and Safety Management Systems.

Brewer Science's ISO 45001:2018, ISO 9001:2015, and ISO 14001:2015 certifications require comprehensive audits by our internal teams and validation by a third-party certifying body to ensure conformance with the standard. You can view Brewer Science's certifications, registration and quality data sheets by visiting Quality, Environmental and Safety Initiatives.

Programs developed within the company, such as the Green Chemistry program launched in 2019, help ensure Brewer Science exceeds our customers' expectations. The Green Chemistry program screens chemicals for potential safety and environmental risks and identifies safer and more sustainable alternatives – both a direct component of the new ISO 45001:2018, and the renewed standard Brewer Science initially achieved in 1998, ISO 14001:2015, which focuses on environmental impact. Learn more about other sustainability programs at Brewer Science by visiting Going Green.

"Brewer Science remains committed to protecting the environment, conserving resources, and providing a healthy, safe and secure workplace. Environmental responsibility is an ongoing priority at Brewer Science, as we continue to reduce our carbon footprint and partner with our customers, suppliers, employees and the community to find new ways to have a positive impact on the environment," said Matt Beard, Director of Integrated Management Systems at Brewer Science.

FormFactor introduces automated cryogenic wafer probe system

FORMFACTOR collaborating with Northrop Grumman has announced the availability of a fully automated cryogenic wafer probe system operating at 4 Kelvin and below to accelerate the development of superconducting compute applications.

Following unique design specifications, FormFactor's HPD cryogenic systems group worked closely with Northrop Grumman scientists and engineers from concept to construction.

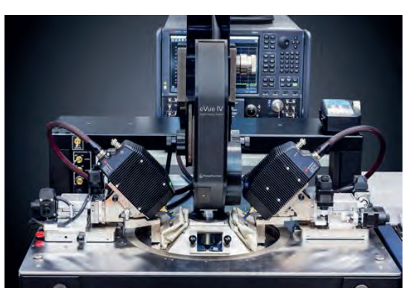
The team produced multiple units of fully automated cryogenic wafer probers capable of meeting the challenging test requirements of superconducting circuits.

Researchers at Northrop Grumman are at the leading edge in developing superconducting technologies including a Reciprocal Quantum Logic (RQL) processor, which delivers exponential improvements in computing power and reduction in energy consumption compared to traditional CMOS processors.

These characteristics are vitally important requirements for data center applications, where rapid growth in data traffic consumes an ever-increasing amount of electricity and real estate.

Other applications range from artificial intelligence to pharmaceutical and chemistry developments, to cybersecurity, financial and weather modelling and more.

The RQL processor leverages well established semiconductor circuit design and fabrication process, enabling faster time to market. Like other superconducting technologies, the processor must operate at temperatures close to absolute zero, and cryogenic test and measurement instruments are essential to device development.



"The ability to conduct testing at or below 4 Kelvin is critical to the development of superconducting circuits," said Vern Boyle, vice president, advanced processing solutions at Northrop Grumman. "Performing these tests at the wafer-level provides a significant increase in production throughput at scale."

"It's rewarding to work closely with pioneers like Northrop Grumman engineers and scientists who are expanding the frontiers of computing technology," said Amy Leong, General Manager of the Emerging Growth Business Unit at FormFactor.

"We're pleased with the part our team has been able to play in this development. We look forward to continued engagement with the Northrop Grumman team and ultimately, the beneficial applications these new technologies may make possible."

Among its portfolio of essential test technologies, FormFactor is a leading supplier of products enabling cryogenic test and measurement. Its 'lab-to-fab' array of cryogenic products provides a wide range of capabilities to accelerate time-to-market for quantum computing research and commercialization, including sub-100 millikelvin cryostats, cryogenic chip-scale and wafer-scale probers for operation at both
77 Kelvin as well as 4 Kelvin and below, engineering probes and probe cards, and scanning SQUID technology.

Nordson ships first SELECT unit from new global manufacturing facility

NORDSON ELECTRONICS SOLUTIONS, a division of Nordson Corporation, in selective soldering systems, is pleased to announce the first SELECT unit shipped May 21 from their new manufacturing facility in Carlsbad, California, USA, co-located with other Nordson Electronics Solutions production facilities. The Carlsbad campus employs hundreds of experienced engineering, manufacturing, and service personnel to provide industry-leading customer experience.

The move from Liberty Lake, Washington, USA further expands capabilities, offering scalable production, strong continuous improvement culture, and skilled manufacturing teams, while serving customers throughout Asia, Europe, and the Americas. In addition, SELECT products are supported globally by more sales managers and technical service staff who cover other Nordson Electronics Solutions products.

"We believe these changes to be meaningful in support of our customers and their continued long-term success," explained Florian Strohmayer, Product Line Manager, SELECT Products. "Our team has worked hard to relocate the operations and to ensure that the expanded field sales and services teams are ready to provide support."

SiTime MEMS oscillators support square point-of-sale products

SiTime has announced that Square, the software, payments, and hardware solution for businesses of all sizes, is using the SiTime SiT8008 low-power, programmable MEMS oscillator for its Square Terminal and Square Register point-of-sale (POS) products. The SiT8008 is one of SiTime's most popular devices and is used in over 50 applications across the enterprise, industrial, mobile, and consumer markets.

The stability of the timing subsystem plays a critical role in ensuring the accuracy of POS products. System vendors do have a choice for timing. They can use a SiTime oscillator, which is an external, standalone timing device, or they can use an on-chip oscillator on their microprocessor/SoC.

An external oscillator like the SiT8008 will consistently deliver 10-100 times better clock stability because of superior MEMS and analog technology and SiTime's systems expertise. Additionally, the programmable architecture of the SiT8008 provides excellent configurability to the user and ensures fast delivery.

"Our goal is to provide sellers with POS solutions that operate with exceptional reliability and accuracy at all times," said Thomas Templeton, General Manager for Hardware at Square. "SiTime's timing solutions are a good match for our Square Terminal and Register products because they help us to deliver an accurate, reliable product to our customers."

The SiTime SiT8008 programmable oscillator features a wide frequency range, low power consumption, small size, and excellent temperature stability over a wide temperature range. The SiT8008 family is programmable, enabling quicker sampling and shorter overall lead times. Continuous 1.8 V to 3.3 V supply voltage enables inventory consolidation and minimizes qualification time.

The oscillators support any frequency between 1 and 110 MHz while providing stability from ±20 ppm to ±50 ppm. SiT8008 oscillators are available in small packages for all frequencies, voltages, and stabilities, enabling board space savings for space-constrained designs without compromising performance and availability.

OPTIM Wafer Services is pleased to announce the installation of an automated ALPSITEC MECAPOL E550 CMP tool at its site in Greasque France.

The system will allow OPTIM to offer for following new or improved services.

- **Oxide CMP Planarisation**
- **Oxide Roughness Improvement**
- **Metal CMP**
- **Poly CMP**

This additional capability enhances OPTIM's already large portfolio of services that include:

- **Wafer thinning by grinding**
- **Individual Die thinning**
- **Taiko Grinding**
- **Single/Double side Polishing**
- **SOI Processing**
- **Edge Trimming**
- **Wafer Dicing**
- **Dice Before Grinding**
- **Wafer Cleaning**
- **Process development services, combining any of the above capabilities.**

For detailed technical discussions please contact either Mr. Mark Wells or Mr. Georges Peyre using the contact details below or visit our website.

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Smart Eye and OmniVision announce end-to-end interior sensing solution

SMART EYE AB, and OmniVision Technologies have jointly announced a full Interior sensing solution for automotive OEMs that enables complete driver and cabin monitoring with videoconferencing applications from a single RGB-IR sensor. The solution is the first integrated video processing chain, which combines innovative features based on the OmniVision OV2312 RGB-IR sensor, supporting exceptional day and night performance.

"Interior Sensing AI is crucial for the automotive industry. Not only is this technology improving automotive safety – saving human lives around the world – it is also enabling automakers to provide differentiated mobility experiences that enhance wellness, comfort and entertainment," says Martin Krantz, Founder and CEO of Smart Eye. "By partnering with OmniVision, we are delivering on this vision: providing an end-to-end, highly advanced Interior Sensing system that meets the demands of automotive OEMs, at a price point that makes it viable for the mass market."

"Empowered by our OmniPixel®3-GS pixel technology, the OV2312 is a 2.1MP, RGB-IR, global shutter image sensor that was designed specifically for interior applications, and it strikes a balance with MTF, NIR QE, and power consumption. We are proud to partner with Smart Eye to enable this accurate full interior sensing solution," says Brian Pluckebaum, automotive product marketing manager at OmniVision.

Smart Eye's AI-based eye, mouth and head tracking technology provides EuroNCAP performance linked with full cabin monitoring and driver monitoring, featuring distraction, drowsiness and incapacitated driver detection, combined with driver identification and spoof-proof processing. The cabin monitoring also includes occupancy detection for all seats, combined with out of position, seat belt status and forgotten baby detection.

The action detection allows an understanding of occupant actions like driver hands on steering wheel, interaction with mobile device, calling, drinking, and eating. These actions may have an impact on the interaction between the vehicle and the occupant and will be a pre-requisite for higher levels of vehicle autonomy.

ASM AMICRA unveils three new manufacturing systems

ASM AMICRA Microtechnologies GmbH ("ASM AMICRA") has announced three new manufacturing systems that combine X-Celeprint's Micro-Transfer Printing (MTP) and ASM AMICRA's high precision die bonding technology to introduce the complete system to enable high volume heterogeneous integration of ultra-thin dies onto up to 300mm base wafers.

X-Celeprint's MTP process stacks ultra-thin dies known as 'x-chips', which can be extremely varied[1] and made using very different process nodes and technologies[2], to create virtually monolithic 3D ICs that improve power, performance, area, cost, time-to-market and security for a wide array of applications including high-performance computing, communications, mobile, automotive, industrial, medical, or defense systems. ASM AMICRA has been perfecting ultra-high precision placement technology for almost 20 years, and has now incorporated X-Celeprint's MTP technology into three different manufacturing systems. These are:

The Nova+ MTP system, which serves high throughput needs with a fully automatic ISO 4 clean room class system using a 50x50mm MTP stamp enabling massively parallel pick-and-place of x-chips. Placement accuracy is +/- 1.5-microns with a 40-second cycle time.

The NANO MTP system, which serves markets such as photonics that require more precise placement accuracy (plus-or-minus 0.3-microns). The AFC+ MTP system, which serves R&D and low volume manufacturing markets. Placement accuracy is plus-or-minus 1.0-microns with a 50-second cycle time. X-Celeprint and ASM AMICRA are facilitating the adoption of MTP technology through development support, including design consultation with assistance in optimizing design and processes and prototyping services to ensure successful product launches. An extensive network of suppliers, manufacturers, and researchers are available to support customer project needs, including licensing programs.

"This agreement with X-Celeprint brings revolutionary technology to market for photonics and 3D heterogeneous integration," said Dr. Johann Weinhändler, Managing Director, ASM AMICRA Microtechnologies GmbH. "MTP technology offers efficient handling of high volumes of large arrays of ultra-thin, brittle dies, as well as the ability to integrate dies from several different source wafers. MTP technology will provide semiconductor manufacturers with a critical, additional 'tool in the toolbox' that supplements conventional and advanced packaging technology."

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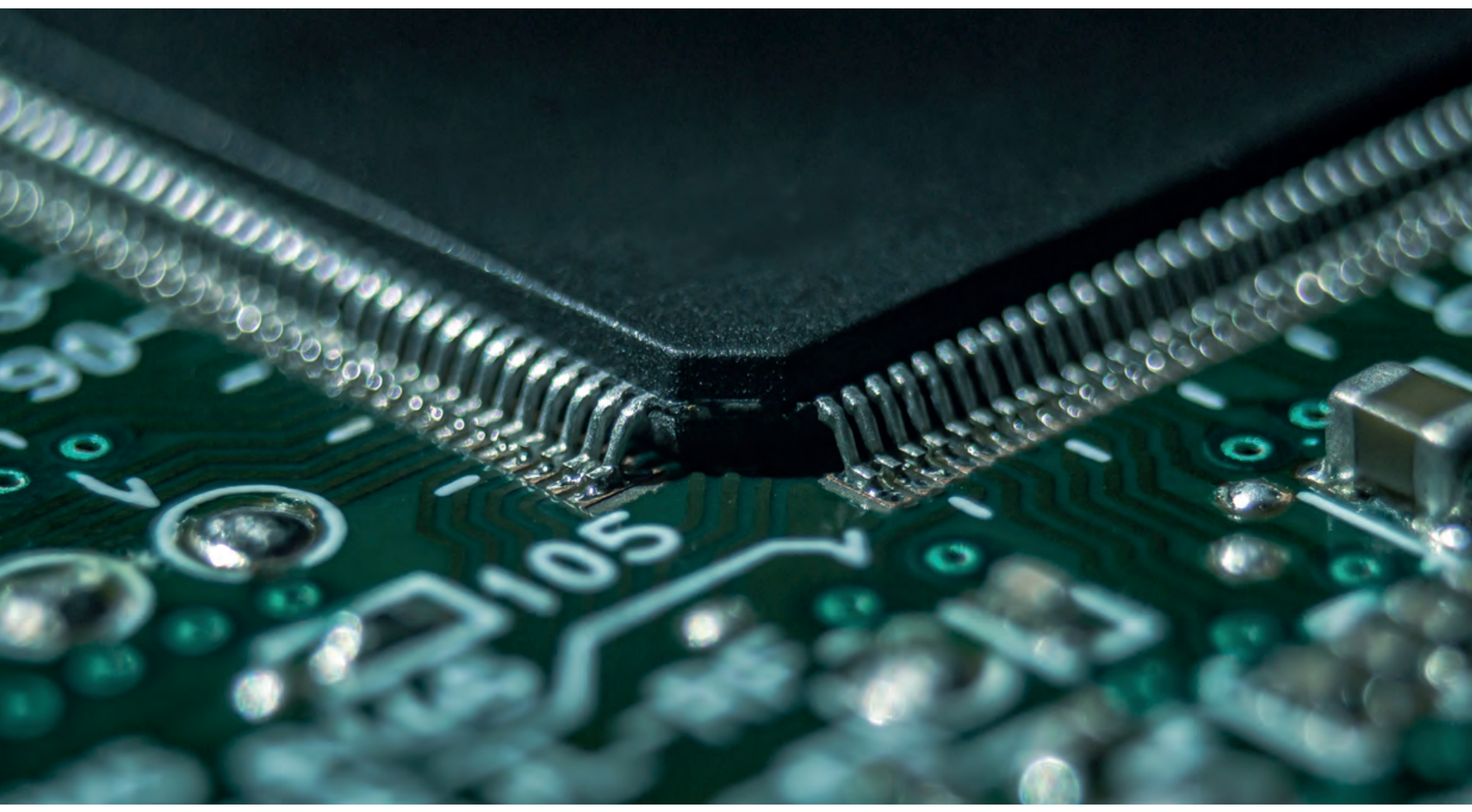


Packaging as the last mile of semiconductor manufacturing

The last step in back end of line (BEOL) device production is often considered packaging, typically including die encapsulation, WLP or FO-WLP. Packaging ends there in most minds. But what about the 'other' packaging? Manufacturers are reconsidering the humble but vital task of boxing and transporting devices to end users as a means to add value, reduce losses and deliver customer satisfaction.

ANALYSIS BY SILICON SEMICONDUCTOR TECHNICAL EDITOR, MARK ANDREWS

A CHALLENGE many might not consider when buying products that include semiconductors is the way in which those vital microelectronic devices are packaged to make their way safely from the fab to end-use customers. Microelectronic devices are small in size, so in theory, they should be easy enough to ship. However, because they are intricate, fragile and highly technical pieces of ESD sensitive equipment they need solid packaging to protect them throughout their journey to the consumer. Whether shipped as processed wafers, singulated die or fully packaged components/modules, all semiconductors have special transport requirements since they could easily become damaged without the right packaging.

As semiconductor manufacturers seek to eliminate every yield risk, and ultimately, all challenges to bottom line profitability, incorrect packaging that leads

to damaged goods can be even more costly than many realize. Packaging mistakes and miscalculations are in fact a risk the industry needs to consider more closely. According to research by Marketplace, packages are dropped an average of 17 times, a likely consequence of the numerous touchpoints they go through to reach their destinations. While the obvious solution is to add additional padding protection to the package to ensure that its contents arrive safely, this is not always the most sustainable option for businesses in every situation.

Simply adding padding will increase the size of the parcel being sent, and therefore greater costs will be absorbed by both the shipper and recipient, ultimately driving up the costs for the same item to be sent. The alternative is to take the risk with minimal padding, or making due with a one-size-fits-all approach that doesn't typically balance packaging and shipping costs against the direct and indirect costs of make-right requirements that arise whenever devices arrive broken, electrically defective or worse still, simply go missing.

PMMI informs the supply chain that replacing a damaged product can cost a business more in the long run than it does to ship it safely the first time. It is estimated that a damaged product can cost businesses within the eCommerce space 17 times more than the original cost of its shipping. With the current global shortage of semiconductor chips, this is a risk manufacturers cannot afford. The ongoing supply/demand imbalance highlights the especially acute need for safe and reliable shipping. As noted in a recent 'Taipei Times' report examining chip supply forecasts, the leaders of a major Taiwanese manufacturer, United Microelectronics Corporation, stated their belief that the shortage could continue longer than expected due to the complicated and intricate nature of global IC manufacturing.

According to UMC Co-President Chien Shan-chieh, the current global semiconductor shortage may last until 2023 as the COVID-19 pandemic boosts demand for chips supporting everything from automobiles to smart home devices. UMC's Chien said on 7th July at the company's annual meeting in Hsinchu, Taiwan, that while the COVID-19 pandemic has had an adverse impact on the global economy and populations in many areas, it also accelerated the digital transformation of daily life, affecting practically everything most people do from how and where they work to how children are educated. Regardless of the pain inflicted by the pandemic, digital transformation has accelerated, and so too has the demand for semiconductors that enable every electronic end product. He concluded that chip supply would continue to fall short of demand and is expected to only worsen in the short term.

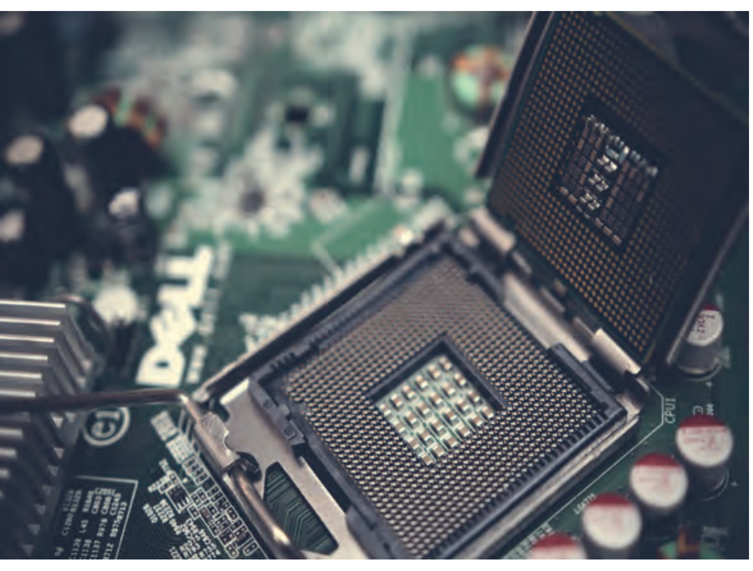
While chip shortages are being addressed by manufacturers of differing device types in different ways, most industry observers expect supply and demand imbalances through 2021 and at least partly into 2022. Whether shortages last another 6-18 months or even longer as UMC suggests, ongoing supply chain issues highlight the need to ensure that every device arrives safely at its intended destination. Global semiconductor market sales grew from $34.85 billion in February 2021 to $41.05 billion in March 2021, according to Statista. This continued growth in chip need is being frustrated by supply chain issues and manufacturing difficulties, meaning that the current global shortage of semiconductors could extend well beyond 2021, according to Richard Palmer, Chief Financial Officer at Stellantis.

Adapting to Changing Demands

The global pandemic has had a huge impact on every industry. Even though the demand for semiconductors continues to grow, every manufacturer appreciates that as device backlogs grow, while boding well for future business, a company can only generate revenue today through what it can actually build and ship. The 10 major fabs under construction worldwide will not come online until late 2022, 2023 or later, underscoring the idea that every realistic option for increasing net productivity needs to be explored until capacity effectively addresses demand.

Manufacturers of all types have had to radically alter their typical production processes to accommodate pandemic affects and aftereffects; most have had to space out workers to allow for social distancing and safer working environments; factories have had to reduce the number of staff working at any one time, which reduces the output of crucial parts. They are simultaneously dealing with supply shortages, delivery delays and related consequences; consumers have experienced similar 'domino effects' which effectively spread the problems encountered in one area of the supply chain to many other points across global markets.

In one major industry – automobile manufacturing – car makers initially pushed-out their IC orders in early 2020, fearing slower sales due to the pandemic. But to the contrary, the COVID-19 pandemic actually



accelerated demand, leaving auto makers in a quandary after calling back workers to factories faster than they initially had anticipated. These call-backs set the stage for a frustrating cycle. Back when automobile IC sales initially slowed last year, semiconductor makers shifted to manufacturing other devices suited to consumer electronic products that were suddenly in higher than expected demand—laptop sales shot up in double digits in 2020, something that hasn't happened as fast and as quickly in more than a decade. This in turn left auto-related orders unfilled due to the time it takes to shift production from one device type to another. The 'seesaw' nature of product demand has left IC makers looking for ways to increase capacity; until this can be achieved, ensuring the safe shipment of all their finished components takes on new, more pressing priorities.

The Importance of Packaging

The way that semiconductors are packaged is now more important than ever in order to reduce the number of products damaged in transport and the consequential return of goods proven faulty due to defects traced back to improper packaging and/or handling. With significant shortages across the supply chain coupled with increased demand, manufacturers must think carefully about the most effective way to package and transport microelectronics.

The process of packaging components along with the often specialized materials that are fabricated specifically to ship ICs are key elements in the electronic transportation supply chain. Packaging of delicate devices shipped by the tens of millions is far more challenging that simply picking the right-sized box, ordering enough and popping them into crates like boxes of ready-mix cake. Semiconductor packaging must be designed to ensure not only breakage-free transport but also protection from ESD and other environmental hazards. The industry is also challenged now more than ever before to consider the environmental impact of materials used to pack and transport semiconductors; poor choices and cost cutting are typically responsible for many integrity issues that occur in transit.

Testing and research can substantially reduce risk and increase the safety of the semiconductor shipping process. The International Safe Transit Association (ISTA) has test and measurement procedures designed to simulate a product being shipped regardless of the transit methodology. Owing to the unique requirements of shipping semiconductors, manufacturing have long adapted their methodologies and practices. But for smaller companies, or startups, the logistical challenges can seem daunting. One resources is the ISTA systematic approach to determining whether shipping containers protect the product and transport it safely. Another critical aspect to consider is the materials that come into direct contact with wafers, die and finished devices; there are tests that can help ensure a decrease in chemical damage, as well as insulation from ESD, heat, humidity and even rough handling. The key in preventing integrity issues is maintaining control over the materials used to create packaging media and to use packaging that has been specifically designed to protect the integrity of finished wafers, singulated die and packaged components.

The sustained international awareness of climate change-inducing manufacturing processes has led to growing efforts ensuring that the materials going into package construction and processes with potential environmental concerns that directly impact packing and shipping can be viewed as a necessary evil needing a solution. Or, as many are starting to see, it can also be seen as a potential means for a manufacturer to add real and perceived value, which can go directly to the bottom line. For example: recycling and disposing of packing/shipping materials can be costly and time consuming, thus creating opportunities for packaging materials manufacturers that operate with minimal carbon footprints while ensuring a package's biodegradability can create a market advantage for itself and its customers.

Especially for smaller manufactures, utilizing cost-effective packaging can be more of a challenge than most think it should be thanks to environmental restrictions that vary by region. This can make it increasingly difficult for smaller manufacturers to handle pack & ship on their own. Outsourcing is one option to consider once critical thresholds related to time and direct costs are reached, making it worth a manufacturer's time to fully investigate the sourcing of their packaging materials; how their shipment practices function and ways that packaging and shipping materials along with adherence to best known practices can contribute to overall customer satisfaction and sustained profitability.

Properly designed packaging media is essential in eliminating excess materials consumption while making certain that the materials that are used meet not only the need to protect shipped devices, but to further reduce unnecessary packaging and ease the need for an ever-increasing amount of packaging media that needs recycling or other types of disposal. By choosing a packaging materials provider wisely, and building these resources within the organization as it grows, semiconductor manufacturers can ensure that one of the most recognizable elements of their products – the packages that carry them safely to the customer – can also save the manufacturer time, offset costs, and reduce the supply chain's global carbon footprint.

EDITOR'S NOTE

➤ ***Silicon Semiconductor** thanks **DPack**, a leading UK packaging and postal supplier, for its assistance in suggesting this article and supplying content including factual references. DPack has a passion for making packaging simple, offering a wide range of packaging materials across the UK for local and international shipping.*

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Ensuring semiconductor IP security in a globalized manufacturing economy

The design and manufacture of today's most advanced semiconductors is increasingly complex and expensive. Securing access to valuable intellectual property (IP) while encouraging collaboration is no easy task. The experts at Perforce share their insights about securing IP resources at a time when misuse or loss can occur all too easily.

BY MICHAEL MUNSEY, PERFORCE

GIVEN THE CRITICAL ROLE of Intellectual Property (IP) used in system-on-chip (SoC) design, companies place an increasingly high value on the management, integration, and sharing of IP. However, the increasing complexity of chip design environments, distributed teams, and involvement of third parties make visibility and control of IP challenging. This, in turn, introduces risk or unnecessary reproduction or purchasing of IP that a company already has.

This is why a more IP-centric view of design is becoming so important, putting IP design and management— whether hardware or software – at the forefront of any project, not an afterthought. Getting it right is easier said than done, but once the challenges are understood and addressed, some proven techniques can be applied.

To understand the bigger picture, it is worth briefly revisiting the evolution of IP in semiconductor design.

As we all know, once upon a time, everything was created from scratch. But then it became apparent that many of the pieces of functionality within a design could be reused – or at least tweaked – from one generation to another. Then, as transistor densities increased, along came system-on-chip (SoC) with everything on the same die. This accelerated the idea of calling functional blocks IP and then reusing them. A further driver was the explosion of consumer devices, where the sheer cadence and volume of chip designs required that starting from the ground up every time was not viable in short time-to-market windows. Not only did reuse of IP within an organisation grow, so did acquiring IP from third parties to speed up the whole process.

Challenges

While the appreciation of IP design and its reuse is endemic, it is something that many companies still struggle to do well, and for a few reasons. First is the cultural resistance of packaging up of IP and its verification environment by engineering teams so that it can be easily dropped into a future design. The situation is made harder by the acquisition-led nature of the industry, with many design teams in theory brought together, but in reality, still operating and thinking as siloes. Often, a reuse methodology does not exist, or at least not efficiently, lacking updated IP catalogues and making it easy for colleagues to discover what already exists. These practices waste effort and money: companies often redesign or buy third-party IP time and time again.

In addition to IP file use practices and their verification is a third, very important aspect of IP design: metadata, which I call the six Ws: the Who, What, Where, When, Why and hoW. Metadata covers aspects such as: who created the IP, who else is using the IP, what version of that IP is current, when was the IP introduced into the design (and what version of that IP), and so on. Here is an example of why traceability of metadata matters: if a bug is found, not only does that bug need to be fixed, it needs to be communicated to anyone else using that IP. Additionally, everything – IP files, verification information, metadata - needs to be visible with other processes, such as bug tracking.

Many organisations have been trying to get by with fragmented approaches that include using manually-created but labour-intensive and often outdated Excel spreadsheets in an attempt to track everything. They knew the problems – the wasted effort, unnecessary time lost, risk of errors – but it felt too hard to address.

Pandemic a catalyst for change

Then along came the COVID-19 pandemic and not only did it highlight the scale of the issues, but it made it clear that they could no longer be ignored. Suddenly, not only were there siloed teams, but individuals working from home became siloes themselves, essentially proving that the infrastructure to communicate and collaborate effectively across an organisation had become necessary. How well organisations have overcome the hurdles involved varies, but some 'best practice' approaches have become apparent and increasingly are being widely adopted.

To overcome these hurdles, there needed to be a cultural change within the organisation. Unfortunately, an already difficult process was made more difficult by having design teams working remotely, trying to

Many organisations have been trying to get by with fragmented approaches that include using manually-created but labour-intensive and often outdated Excel spreadsheets in an attempt to track everything. They knew the problems – the wasted effort, unnecessary time lost, risk of errors – but it felt too hard to address

design and assemble a very complex system. The key to overcoming all the challenges is integrating a system into the existing methodology in a way that does not change how design teams work and certainly does not add any complexity to the process.

Automation is critical, and keeping track of the six Ws needs to happen without any effort or manual intervention of the design teams. IP catalogues need to be created and maintained based on real-time data from the existing design process that are not dependent on the fulfilment of yet another task delegated to the design team.

A methodology around version control is required for design files so that they are visible to all contributors, with checking in of files, checking out of files, editing them, checking them back in, and communicating all of those changes. The most common tools used are version control management systems. There are many available, many of which initially stemmed from asset-centric markets such as gaming and enterprise IT, but are now widely used in markets where IP components are also involved.

Organisations also face the challenge of managing all the metadata around IP files including such needs as: the test and verification environments; where IP has been and is being used; what is the latest version; who is editing it; any associated bugs as well as the inter-relation between different metadata. That is impossible to manage efficiently on an Excel spreadsheet; a database approach is essential. Plus, it must link with other systems such as bug tracking, continuous integration, design, verification, PLM, scheduling, resource planning, and more.

Once that framework has been established, this information can be published and made available to other people. Manually-driven catalogues and IP datasheets using word processing and presentation software packages take effort and can become quickly outdated. Therefore, real-time versions of these resources are required so that users can see what an IP does and where it is in its design lifecycle: what is needed, in other words, is sometimes referred to as a ‘single source of truth.’

Again, version control tools are used for this purpose, with a choice of both commercial and open-source programmes. However, what really matters is making sure that the selection meets the right criteria, such as how well enterprise-wide collaboration is supported, particularly across remote and geographically dispersed teams. Another consideration is whether it supports all the file formats involved, and these days the variety can be wide, including multiple binary file content. Also, can the system scale to meet demand or change? Also, look for tools that automate processes to reduce workload, errors, and time-to-market.

Ideally, the level of automation will be driven from users’ workspaces and capturing all of the metadata that goes into design intent and use. Coupling this with managing the design files through a version control system will allow for that single source of truth represented by a design bill of materials (BoM).

This BoM could represent the entire design or an IP under development because such a system and methodology would treat the combination of design and metadata as an IP, whether it is a whole design or a piece of the design. This also streamlines the process of packaging up IP for reuse within an organisation.

The ultimate goal in IP-centric chip design is a means to achieve comprehensive traceability across design teams and projects, both current and historic. Once that is established, extracting more value from IP by putting it at the heart of new design projects, organisations can expect to save costs, eliminate unnecessary duplicated effort, reduce risk, and ultimately go to market faster.

ABOUT PERFORCE

➤ Founded in 1995, Perforce Software is a leading provider of highly scalable developmental and operational solutions designed to protect and secure intellectual property while enabling collaboration without boundaries. Perforce Software partners with organizations that must accelerate time to market and reduce risk in environments where the cost of failure is high.

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➤ The latest PLCs, machine controllers and industrial PCs built for IIoT applications can be used for Edge computing while also supporting high-speed data logging to the Cloud.
[Source: Mitsubishi Electric Europe B.V.]

Manufacturers need to leverage the power of data to be competitive

Many manufacturers agree that boosting responsiveness, productivity and flexibility on the factory floor are important keys to enhanced competitiveness. Silicon Semiconductor invited **JEREMY SHINTON, PRODUCT MANAGER FOR EDGE COMPUTING TECHNOLOGIES AT MITSUBISHI ELECTRIC,** to delve into the ways that controllers designed to manage the convergence of information technology (IT) with operational technology (OT) can help ensure optimal data management and connectivity for a competitive edge

EFFICIENT DATA MANAGEMENT using the Industrial Internet of Things (IIoT) is increasingly important in extending communication beyond the production cell and ensuring the successful deployment of new and updated automation systems across manufacturing environments.

Key to bridging the gap between automation systems processing large volumes of data and the ability to turn this into intelligence that is shared with higher level enterprise systems is a new class of controller. The latest PLCs, machine controllers and industrial PCs built for IIoT applications can be used for edge computing while also supporting high-speed data logging to the cloud.

Reaching out beyond the factory floor

At the core of highly effective, futureproof production facilities is the Industrial Internet of Things. This is a network of connected devices and systems, from the factory floor all the way up to higher enterprise levels that generates and shares large volumes of data. The goal is to create unique,

actionable manufacturing intelligence to improve production and plant activities resulting in increased productivity, uptime and flexibility. Businesses that leverage the power of data can therefore considerably enhance their competitive edge in a fast-changing market.

The creation of a successful IIoT application requires automation systems built on controllers with cutting-edge processing power and capacity, allowing data to be analysed closer to where it is generated. State-of-the-art PLCs, such as Mitsubishi Electric's MELSEC iQ-R series, address these needs by featuring powerful processors and large data handling capabilities.

IIoT-ready controllers like these support advanced connectivity options, playing their part in continuously delivering data-driven information. The ability to connect to the cloud using common protocols directly on the PLC is a growing trend. The 'connect everything' idea means that controllers can be anywhere in the world and act as a 'data pump' to higher level cloud platforms. Commonly used operating systems, such as Linux, can now be hosted on PLC modules.

This enables the platform to utilise an open source and secure functionality that can easily be installed into these environments. It puts the already highly connected plant level PLC into areas using new language terminology phrases, such as JSON, REST API, MQTT, Python and the rest of the buzz words and acronyms that fill this space. These new PLC capabilities open the door to IIoT applications in all industries.

Whilst these elements are crucial to the creation of information technology (IT) driven actionable insight to improve production operations, businesses will need solutions to continuously bridge the divide between the IT world and operational technology (OT). This represents the next step in ensuring highly productive, flexible and responsive plants.

Automation that works at the Edge

To achieve this, solutions need to be implemented that can support data analysis for time-critical operational tasks and production-based analytics as well as for non-urgent but more processing-intensive data mining. These help to build an in-depth understanding of plant operations and develop actions to improve them.

Mitsubishi Electric's latest MELIPC edge computing solution offers an ideal IT/OT merger that supports both on- and off-site data analytics functions. It features advanced analytical and artificial intelligence functionality to process data locally in real-time, utilising shop floor know-how with diagnostics and predictive maintenance feedback. As a result, the device can drive a production system's decisions based on key data. MELIPC also pre-processes and aggregates data for higher-level insights. Thanks to OPC UA standard connectivity, the information is then shared to different platforms to improve plant operations.

A clear benefit of this hybrid solution over conventional cloud-based systems is a particularly secure as well as reliable connection and ecosystem. Highly regulated industries, such as the pharmaceutical sector, can therefore benefit from innovative data mining capabilities while still meeting regulatory compliance.

CASE STUDY: Automation in advanced process environment

LOTTE, a leading producer of confectionery, wanted to optimise the production of its popular Yukimi Daifuku product line. The manufacturing processes involved are complex and can be influenced by a number of factors. With this in mind, Mitsubishi Electric developed a data-driven solution to help deliver consistent product quality.

"When wrapping, the hardness of the product used to vary depending on the temperature and water content. Some operations were dependent on people, and losses arose out of the need to finely adjust the machine parameters," explains Hiroshi Sugimoto, Manager of the Facilities Department, Urawa Plant, LOTTE Co., Ltd.

"The e-F@ctory IIoT system allows us to conduct improvement activities such as enhancing the operating rate, stabilising quality, and optimising staffing for production activities. The extendibility of the system, depending on what we want to do, was also appealing," Sugimoto added.

PLCs installed in the production lines collect data on product and machine status in each process. This ranges from hopper vibration data to data from the conveying inverters. All the information can be visualised in real-time through the overall SCADA monitoring system, which is installed in the control room and also through on-site computer displays. By centralising the gathered data, Mitsubishi Electric's MELIPC could be used to analyse and conduct data diagnostics in real-time. The results of this help to improve product quality and provide the opportunity to optimise production activities in the plant.

"In the course of daily production, machines do not operate in the same condition every day. Previously experienced staff members checked and adjusted the settings of the machines," said Takayuki Manako, Executive Director & Plant Manager of Urawa Plant, LOTTE Co., Ltd. "but with e-F@ctory we can visualise the condition of machines and the machines themselves can issue instructions to make adjustments." Manako added, "We aim to horizontally deploy this system and construct a smart plant in which ´symptom management´ and ´operating rate improvement´ are implemented on numerous lines. Stable plant operation and manpower savings will eventually make a major contribution in terms of costs and so on. If we consider LOTTE as a whole, our goal is to further evolve this technology and extend it to other plants."

On-board with IIoT controllers

The future of manufacturing is here and it is based on an interconnected IIoT framework. Key technology solutions to realise this are already at hand. By setting up an IIoT system that leverages advanced controllers and industrial PCs with high-speed, powerful processing capabilities and connectivity features, companies can truly enhance manufacturing operations. This will lead to data-driven applications that can generate and share a comprehensive understanding of plant and production activities, supporting their continuous improvement.

OmniVision is giving digital imaging a front row seat

Digital imaging and machine vision, from a consumer perspective, is mostly about the visible: smartphone cameras, surveillance systems or pocket-sized DSLRs. But industrial applications of digital imaging deliver data from across many spectral bands, enabling Industry 4.0 and many new levels of manufacturing automation in addition to consumer products. Silicon Semiconductor technical editor Mark Andrews recently spoke with **OMNIVISION'S DIRECTOR OF AUTOMOTIVE MARKETING, ANDY HANVEY,** about the expanding market for machine vision and its future across multiple applications.

Sensor technologies continue to expand their reach across commercial and consumer markets thanks to a combination of increasing quality, advancing technology and the introduction of AI or neuromorphic computing. Technology continues to transform how we collect, utilize and analyze sensory data. Chip quality has skyrocketed while prices have decreased across most applications, meaning that whether someone is driving with the aid of a heads-up display, avoiding injury thanks to the latest ADAS system or any other myriad applications, digital imaging and machine vision is found in so many applications it has become a growing market force.

OmniVision Technologies is a leading developer of advanced digital imaging solutions. Like the market itself that has grown from relatively simple sensors to advanced, miniaturized imaging devices, so has the

Smart Eye's interior sensing system provides complete driver and cabin monitoring, tracking eye gaze, body key points, activities and objects in a vehicle, seat occupancy and more

OmniVision product portfolio, which embraces needs across mobile phones; security and surveillance; automotive; tablets, notebooks, webcams and entertainment devices, as well as medical, AR/VR, drone and robotics imaging systems.

As the sophistication of digital imaging has grown, so too have its applications. One market that is witnessing a transformation thanks to digital imaging is the automotive sector; each year, manufacturers add imaging sensors and digital cameras along with radar and other sensory systems to increase safety, add passenger benefits, and continually increase a vehicle's ability to support a transition to greater levels of autonomy. Advanced imaging is also getting a boost from companies that share complementary technologies and partner to offer new services that deliver benchmark capabilities.

In July, OmniVision and Smart Eye AB, a global leader in interior sensing AI, teamed up to provide the automotive industry with what the companies believe is a ground-breaking, end-to-end interior sensing solution. By combining two leading technologies, the new solution enables complete in-cabin monitoring that can locate and identify each passenger along with detecting movement that could suggest inattentive driving or incapacity. The technology can also alert a driver if a passenger (such as an infant or child) is left unattended in the vehicle. The companies stated in their announcement that the new solution supports next generation, higher level vehicle autonomy, nighttime sensing, even in-vehicle video conferencing.

The two companies described their new product solution is the first integrated video processing chain combining innovative features based on the OmniVision OV2312 RGB-IR sensor with Smart Eye's advanced interior sensing artificial intelligence.

"Interior sensing AI is crucial for the automotive industry. Not only is this technology improving automotive safety – saving human lives around the world – it is also enabling automakers to provide differentiated mobility experiences that enhance wellness, comfort and entertainment," says Martin Krantz, Founder and CEO of Smart Eye. "By partnering with OmniVision, we are delivering on this vision: providing an end-to-end, highly advanced interior sensing system that meets the demands of automotive OEMs, at a price point that makes it viable for the mass market."

"Empowered by our OmniPixel 3-GS pixel technology, the OV2312 is a 2.1MP, RGB-IR, global shutter image sensor that was designed specifically for interior applications, and it strikes a balance with MTF, NIR QE, and power consumption. We are proud to partner with Smart Eye to enable this accurate full interior sensing solution," said Brian Pluckebaum, OmniVision's automotive product marketing manager.

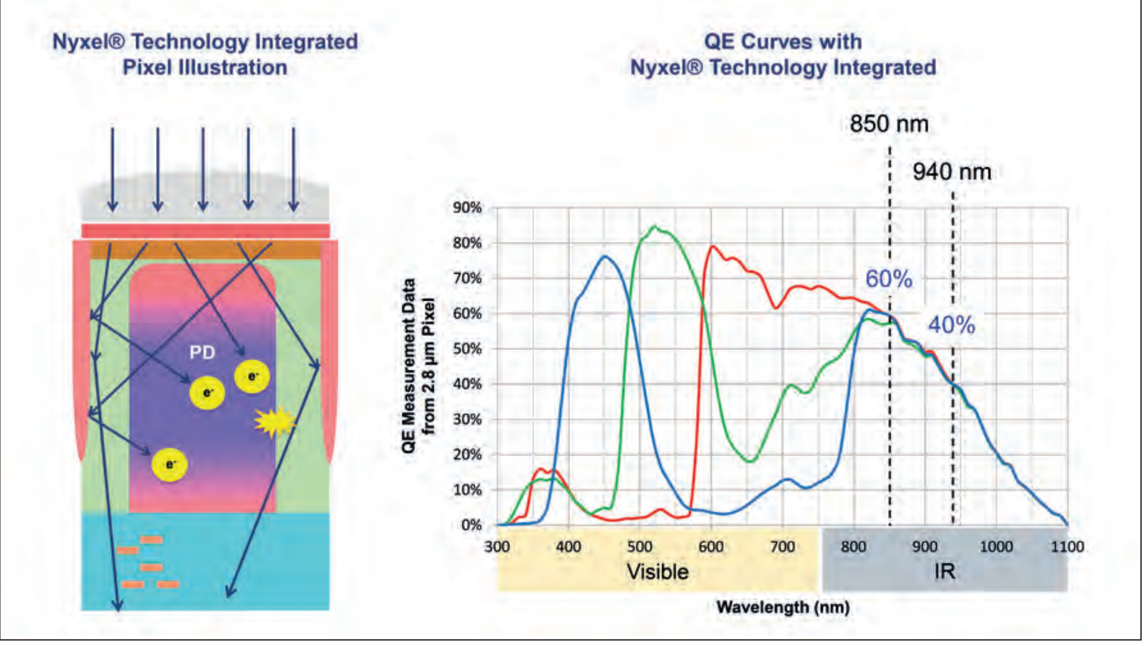
The ability to track driver and passenger movements in-vehicle can deliver immediate safety benefits, and

Interior sensing AI is crucial for the automotive industry. Not only is this technology improving automotive safety – saving human lives around the world – it is also enabling automakers to provide differentiated mobility experiences that enhance wellness, comfort and entertainment

it is believed that the ability to track in-vehicle motion, such as a driver's movement to activate a vehicle system, will be an important key to achieving higher levels of vehicle autonomy. This latest achievement comes after years of noteworthy digital imaging advances. OmviVision's automotive products marketing director, Andy Hanvey, shared company milestones that have led to some of today's state of the art accomplishments.

"One of the most significant historically was development of the OV60A, the world's first 0.6µm pixel, 4K image sensor for mobile applications. The OV60A is the world's first 0.61 micron pixel high resolution CMOS image sensor that revolutionizes the capabilities of next-generation mobile phone cameras," he said. "The OV60A offers 60 megapixel resolution with the smallest pixel size in its class at .61µm. The OV60A can fit into a 1/2.8 inch optical format, supporting either 3:4 or 16:9 aspect ratio configurations. To achieve this increase in resolution, along with a smaller pixel size and optical format, the OV60A is built on OmniVision's PureCel Plus-S stacked die technology. It is 24 percent smaller in area than the previous generation 0.7µm pixel solution, yet it can achieve higher quantum efficiency (QE) with better crosstalk and angular response than the 0.7µm generation."

Hanvey said OmniVision also developed the OH0TA; smaller than the world's smallest medical imager and CameraCubeChip, it is 0.55mm x 0.55mm with a 400 x 400 resolution. And it is the new generation of the company's Guinness World Record holder 'world's smallest image sensor' (OV6948), and wafer level module (OVM6948 with OV6948 embedded). The significance here is its record-setting size allows designers to add ultra-compact visualization to single-use and reusable endoscopes, as well as catheters and guidewires, with a small outer diameter of 1-2mm. The OH0TA's increased resolution allows higher quality color images to be captured from within the



Nyxel technology provides superior near infrared (NIR) quantum efficiency.

body's smallest organs, enabling medical devices to reach deeper into the body. Additionally, the sensor's lower power consumption reduces 'chip on tip' camera heat for greater patient comfort and longer procedure durations, while also reducing noise for crisper images.

Another highlight according to OmniVision is the company's OAX8000, the world's 1st dedicated driver monitoring system (DMS) ASIC with an integrated AI neural processing unit, image signal processor and DDR3 memory. Hanvey said that most DMS processors on the market today are not dedicated to this application, requiring added circuitry to perform other system functions that consumes more power, occupies more board space and doesn't allow room for on-chip SDRAM. By focusing the design of the OAX8000 ASIC on entry-level DMS, OmniVision was able to create the automotive industry's most optimized solution, he explained.

The OmniVision Nyxel series of digital imaging technology adds near infrared (NIR) capability that improves resolution and contrast compared to conventional CMOS chips.

To give an idea of how pervasive digital imaging has become across so many applications, Hanvey noted that another of OmniVision's noteworthy accomplishments is recently reaching the milestone of 12 billion devices shipped since the company was founded in 1995. They believe the quantity of their products, and sizeable market pull for machine vision, demonstrates a trending growth pace and a bright future for companies that meet the exacting standards.

A final milestone Hanvey mentioned was the company's launch of its Nyxel near infrared (NIR) imaging technology that OmniVision believes offers the world's best NIR imaging quantum efficiency. This is significant because competing mass-produced CMOS image sensors are still failing to achieve comparable NIR performance. With a 2.8µm pixel pitch, Nyxel provides 60 percent QE in barely visible 850nm NIR light spectrum and 40 percent at the invisible 940nm NIR wavelength, which are 5 and 3 times (respectively) more than the standard pixel structure.

Since advances in machine vision have accelerated to support manufacturer requirements and to enable future system level advances, it's natural to wonder: how are changes in machine vision technology going to enable future automotive systems?

"This is a good question, many things could be impacted including enhanced nighttime safety, improved heads-up displays, ADAS-related improvements, imaging of vehicle surroundings and many others. The use of machine vision will be found in automotive use cases more and more, not limited to just ADAS. For example, a camera which would be used today for SVS, in the future could be used for SVS and machine vision. In addition, we have multiple

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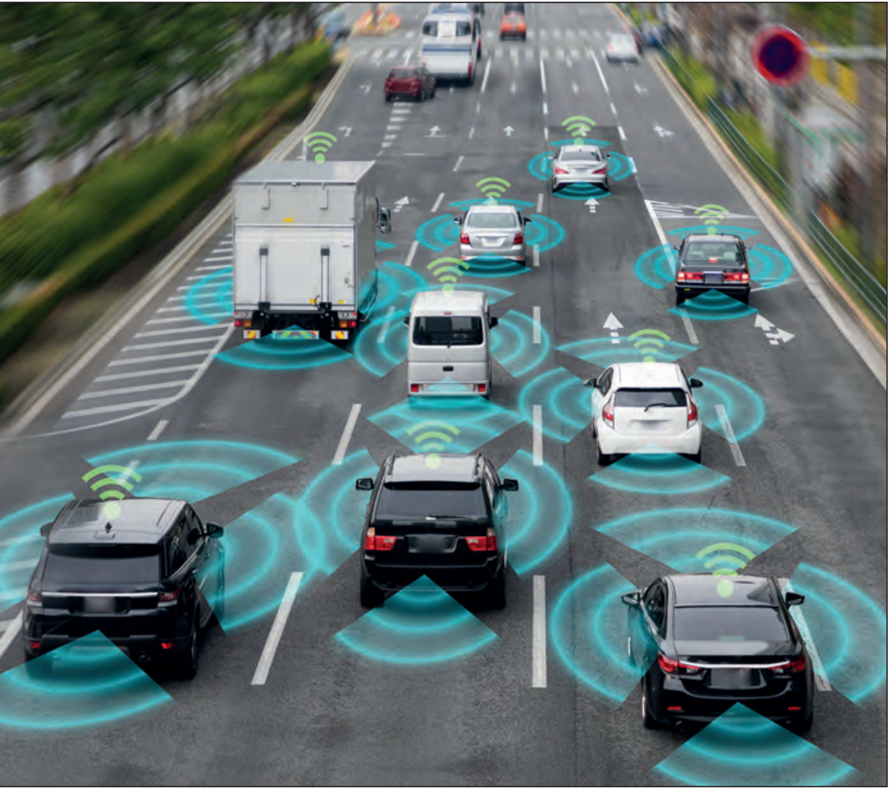

cameras inside the car – these would be used today for DMS. This is an application that looks at the drivers face/eyes, and based on an algorithm, can interpret a level of distraction. In the early days of in-vehicle monitoring, this was known as 'drowsy driver' monitoring, but distracted driving can include many activities including eating, looking at a mobile phone, texting, or talking to passengers," he explained.

Looking ahead into the future of automotive design and the role that digital imaging will play across multiple applications, Hanvey noted that as systems multiply, power consumption as well as electromagnetic interference (EMI) becomes more of a challenge, so device designers need to stay ahead of requirements while anticipating future challenges.

"Within automotive applications, there is a trend that we see where the camera is required for more than one function; for example, human viewing and machine vision. At the image sensor level this could mean adding support for specific CFA (color filter array) patterns or having advanced features such as dual output. On the processing side, having an ISP that can process multiple CFAs also helps achieve dual-use functionality, which can be found in the OAX4000," he said.

"OmniVision strives hard to future-proof designs and we can discuss a number of options. The first is providing a platform of sensors which are P2P (pin to pin) compatible. This means a design can have an upgrade path for a different feature set. Providing a wide range of functionality is exemplified by the OAX4000, so customers today can design their system with RGGB based cameras, but in 2-3 years, they may perform an upgrade to RCCB. This would be a change at the camera level (along with some software updates for the OAX4000 in the ECU), which is more efficient that starting from scratch."

"As vehicle functionalities increase, OEMs are also concerned with EMI, system power consumption, functional safety and cybersecurity. OmniVision's designs are based on system level thinking, evolving around problem solving and helping designers achieve optimal results. For instance, we have been continuously working on meeting the EMI requirement changes customers specify. In another approach, we are optimizing the process technology and pixel technology, which enables us to refine the image sensor QE, which in turn helps OEM designers reduce system power consumption.

"Currently, OmniVision's automotive products are at least ASIL B qualified, with some of the latest products meeting ASIL C compliance. Observing the high demand trend for cybersecurity, OmniVision is addressing this in our product design; we are continuously looking for more ways to enhance cybersecurity in our products," Hanvey said.

Commercial and consumer expectations for digital imaging/machine vision are constantly evolving, and Hanvey sees OmniVision's products also evolving along two primary, parallel paths.

"For automobile and vehicle manufacturers, we expect the need for more high performance products to achieve OEM KPI, along with small size, broader light spectrum, unprecedented flexibility and low power consumption. This allows the OEMs to have faster time to market, smaller system design, more use case possibilities, and the ability to hide the camera(s) out of sight. For consumer applications, we see the need to provide the functionally for today and tomorrow with future-proof technologies that deliver smaller pixel size, more visual possibility for challenging lighting conditions that include the near infrared spectrum, higher resolution, better image quality, further object detection range and less power consumption. As a result, OmniVision enables smaller, lighter devices, broader imaging applications, higher image quality and better end-user safety."

ANDY HANVEY

> Andy Hanvey joined OmniVision Technologies, Inc. in October 2016 and is currently Director of Automotive Marketing. Prior to OmniVision, he worked at Andor Technology, Aptina Imaging and most recently with Imagination Technologies. He has more than 25 years' experience in the semiconductor industry in engineering, applications and marketing. Hanvey has an MSc degree in optoelectronics from Queens University, Belfast.

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5G is a game-changer for semiconductors

Upholding the high purity & precision necessary for next-generation wafer fabrication

BY AUTHOR FROM APPLIED ENERGY SYSTEMS

5G, THE FIFTH-GENERATION of wireless technology for digital cellular, is driving tremendous potential for high-tech companies developing connected devices and smart products, as well as the semiconductor fabs producing the chips utilized in these devices.

The rollout of 5G, which rose to prevalence as recently as 2019, is deemed the gateway to Internet of Things (IoT) connectivity, automation, and edge technologies. New devices utilized in this smarter standard will require fabs to produce higher performing wafers with even greater capacity for memory and storage. This demands that the manufacturing equipment and gas delivery systems utilized in fabs are built for greater complexity, ensuring higher levels of precision are achieved and process integrity is upheld.

The Origins of 5G

5G emerged as a response to the need to handle greater volumes of data than earlier generations of cellular mobile commutations could handle. Prior to 5G, almost all cellular mobile communications took place in sub 3 GHz bands, but as the number of users and data on networks has increased, there was a need to look beyond 3 GHz bands.

5G operates at a frequency of 10mm to 1mm, offering higher speeds and improved capacity over 4G. More importantly for high-tech innovators, however, is 5G's extreme reliability and ultra-low latency. This allows IoT applications like machine to machine (M2M) communications to handle the large volumes of data needed to operate mission-critical control

applications. For semiconductor companies, meeting the demands of emerging technologies that can run on 5G will mean increasing chips' baseline memory to process far more data and handle more specific applications. It will also necessitate generating a higher volume of chips in a shorter period of time as innovators race to capitalize on the new potential unlocked by 5G.

Smartphones and the future of 5G devices

Smartphones, in particular, are driving the 5G revolution, with Gartner projecting 5G smartphones will account for 71% of smartphones by 2024. Specifically, chip volume and radio frequency frontend modules for 5G is expected to double in premium smartphones. This will have major implications for 5G semiconductor revenue, which is projected to increase from nearly zero in 2018 to $31.5 billion by 2023.

New industries and applications – from autonomous vehicles to asset tracking and smart city management – are also experiencing the benefits of 5G. For semiconductor companies, this requires fabricating more complex chips for advanced applications. To do so, fabs demand equipment and systems, like the gas delivery cabinet, to meet ultra high purity process demands.

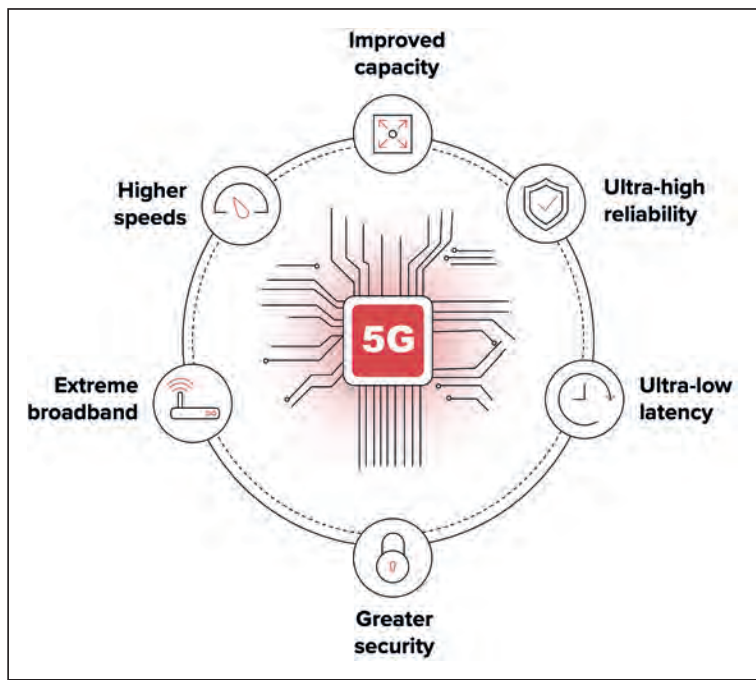
High purity gas delivery equipment powering high-tech innovation

As chip complexity becomes more advanced, only leading-edge semiconductors can be utilized. These wafers require a high level of precision to fabricate patterns with widths of around 10 nanometers – or the width of a human hair sliced 10,000 times.

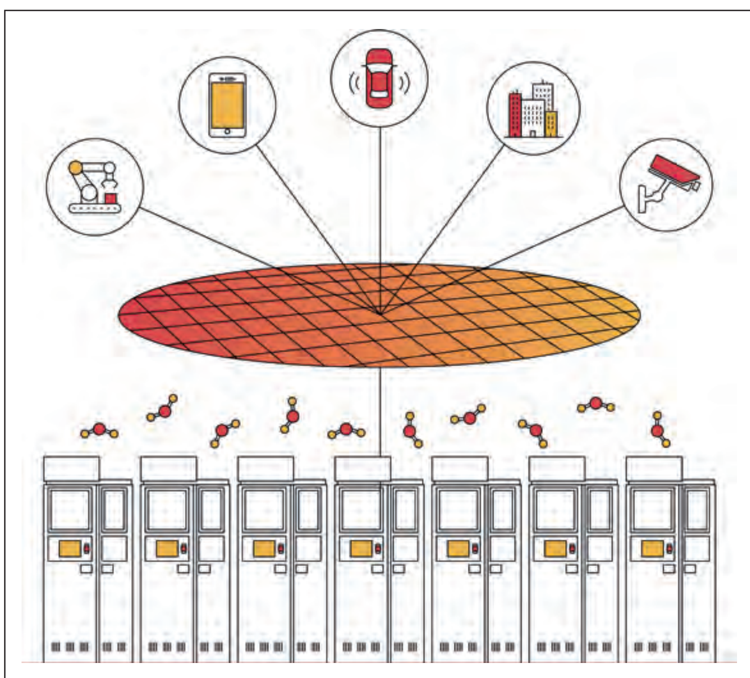
Ultra high levels of purity must be maintained during fabrication, as the slightest contaminate could render semiconductors useless. Gas purification technology, such as ARM Purification purifiers, can remove contaminates down to the parts per trillion (PPT) level to ensure impurities do not impact production. Equally important is the gas delivery equipment utilized to uphold the highest standards of precision and purity. For over 40 years, Applied Energy Systems SEMI-GAS® SEMI S2 compliant ultra high purity gas delivery systems have been the equipment of choice of Tier 1 semiconductor leaders to power next-generation innovation.

Embracing the 5G Revolution

The future of 5G is bright, with reports predicting the global 5G value chain will enable $13.2 trillion in economic output by 2035. The investment in 5G will have a downstream effect on semiconductor sales, with fabs producing a higher volume of chips for both emerging and existing markets, as well as increase the demand for reliable gas delivery systems for fabrication.

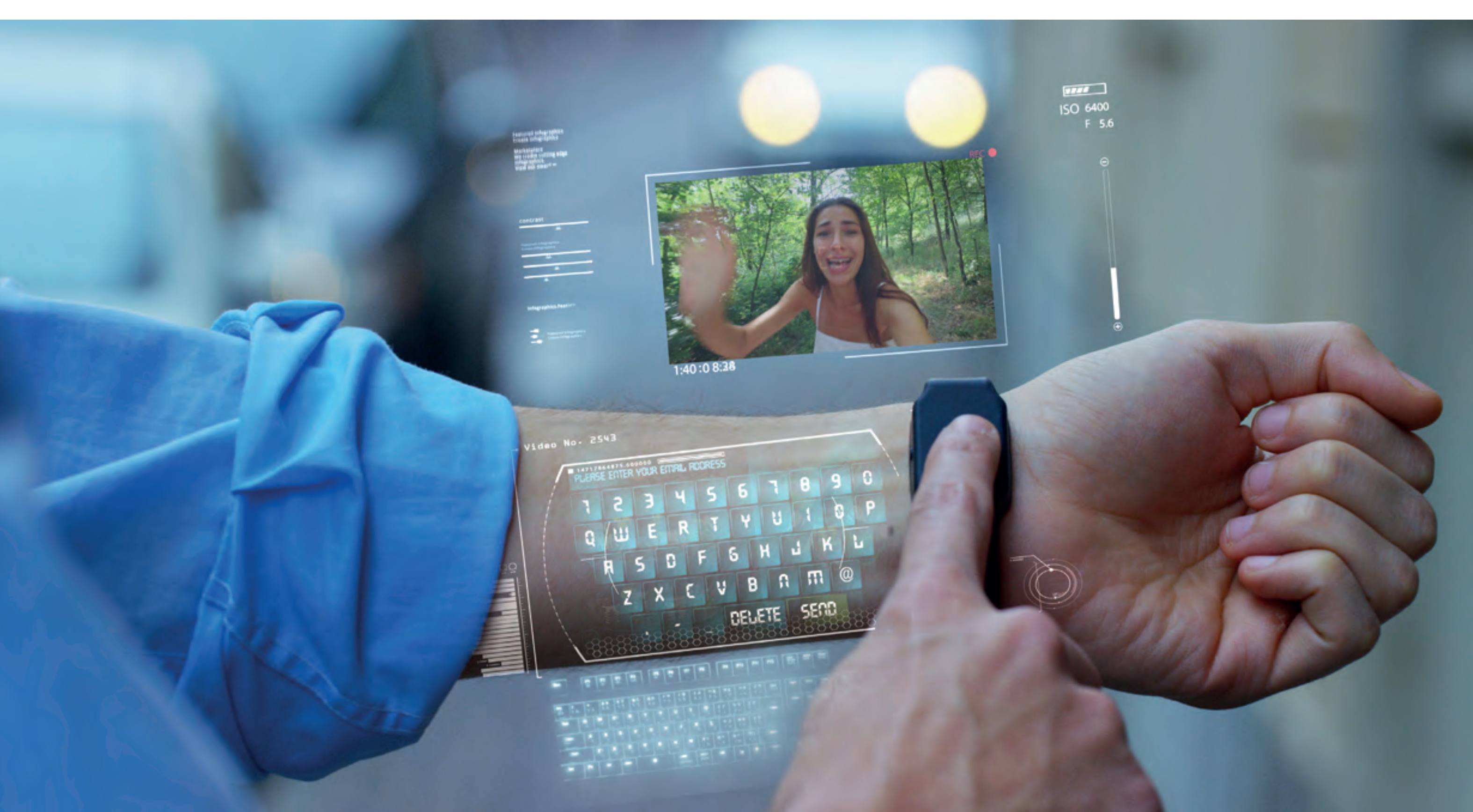


➤ By utilizing millimeter waves, 5G offers greater speed, capacity, and reliability over prior generations of cellular mobile communications to support high tech innovations. Semiconductors will be critical for supporting these new applications.



➤ Ultra high purity gas delivery systems will be required to fabricate wafers with greater baseline memory to support IoT applications, such as M2M communications, smart cities, and remote operations, that run on mmW 5G networks.

To learn more about the future of semiconductors in 5G and the role of high purity gas delivery equipment in fabricating chips for innovative applications, contact us at **https://www.appliedenergysystems.com/contact-us/**



A logical switch to the vertical direction

Surging sales of wearable devices will drive a new era for the IC, with planar FETs replaced with vertical gate-all-around transistors

BY KATSUHIRO TOMIOKA FROM HOKKAIDO UNIVERSITY

WHEN COMMERCIALIZATION of the IC began back in the 1960s microprocessors would feature a dozen or so transistors, each with dimensions of tens of microns. In the intervening years we've come an awfully long way. Progressing at rates described by Moore's Law and Dennard Scaling, we have been on an exponential trajectory. While its not been easy at times, requiring the likes of the introduction of a high-κ gate oxide, metal gates, strained silicon and multi-gate architectures to keep up the pace, continued advances have ensured that the world's leading fabs are now churning out ICs with 50 billion FETs. The big question is this: given the exceptional miniaturization of the FET, how will researchers extend LSI from now on?

While these researchers ponder this, they must consider how the pandemic has changed the way we use electronic devices, and how electronics are developed. We now live in a world where there are fewer physical spaces and cyber spaces are on the rise. This has meant that working remotely is now the norm in many sectors, and socialising on-line is commonplace. There is also more interest in wearable augmented-reality devices. The likes of smart glasses, earphones, wrist bands and rings, previously thought of as gadgets of the distant future, are now the technologies we want to soon inhabit our world.

Getting there requires addressing concerns over wearable devices. Compared to smartphones and other forms of portable electronics, they have limited functionality. It also challenging to make them small enough, so that they are not cumbersome. Success on both fronts demands a new generation of high-performance LSIs to serve in a post-5G era.

Our team at Hokkaido University, Japan, is tackling this challenge by developing a number of promising technologies. We have considered performance per unit volume, finding that when the system performance is represented by memory bytes, this plummets with the miniaturization of the device size (see Table 1). Due to this trend, we are convinced that wearable devices of the post-5G era need to contain a high-performance computing system.

What will the transistor technology look like in such a system? Consequences of miniaturisation indicate that it can't be based on planar integration, the mainstream architecture since the 1960s. We can also rule out the stacking of LSI chips – the so-called 3D integration or chiplets – due to serious thermal management problems. So a new integration schemes is needed, delivering much denser devices in a smaller footprint than modern LSI. This approach demands alternative switches, used to create small, high-performance architectures with ultra-low thermal dissipation.

Four ways forward

We are investigating four different approaches for producing modern FETs that could fulfil these requirements: an alternative FET structure, different channel materials, a new switching mechanism and a refined integration scheme (all are outlined in Figure 1).

One simple approach to decreasing the FET's power consumption is to lower its supply voltage. That's because the active power of an IC is proportional to the square of the supply voltage; and the stand-by power of an IC is proportional to the supply voltage, and the off-state leakage current.

An option for decreasing the off-state leakage current is to shift to a gate-all-around architecture. With this design, the gate metal wraps all around the channel to provide the best electrostatic control of the gate.

When it comes to replacing the channel material, there are several strong candidates for taking the place of silicon. Contenders include III-Vs, germanium, and two-dimensional transition-metal dichalcogenides. All promise to provide a high on-state current under low bias, thanks to their high carrier mobility and low electron/hole effective mass. However, the latter is actually a mixed blessing, as the small effective mass also results in a high tunnelling leakage current. So,

	Typical Volume (mm^3)	Weight (g)	CPU (GHz) RAM (GB)	Performance/ Volume (GB/mm^3)	Performance Ratio
Smart Phone	7.84×10^4 (160 x 70 x 7)	180	2.8-3.0 6	7.0×10^{-5}	1
Smart Glass	4.9×10^6 (200 x 350 x 70)	566	2.96 4	0.8×10^{-6}	1.1×10^{-2}
Smart Watch	3×10^4 (116 x 45 x 6)	30	1.2 1	3.0×10^{-5}	0.4
Smart Wrist Band	3×10^4 (144 x 18 x 12)	12	– 0.5 MB	1.6×10^{-8}	2.2×10^{-4}
Earphone	7×10^3 (19 x 17 x 22)	6	– < 0.5 MB	$< 7 \times 10^{-8}$	$< 1.0 \times 10^{-3}$
Smart Ring	6×10^3 (200 x 10 x 3)	4	0.12 0.6 MB	1.0×10^{-7}	1.0×10^{-3}

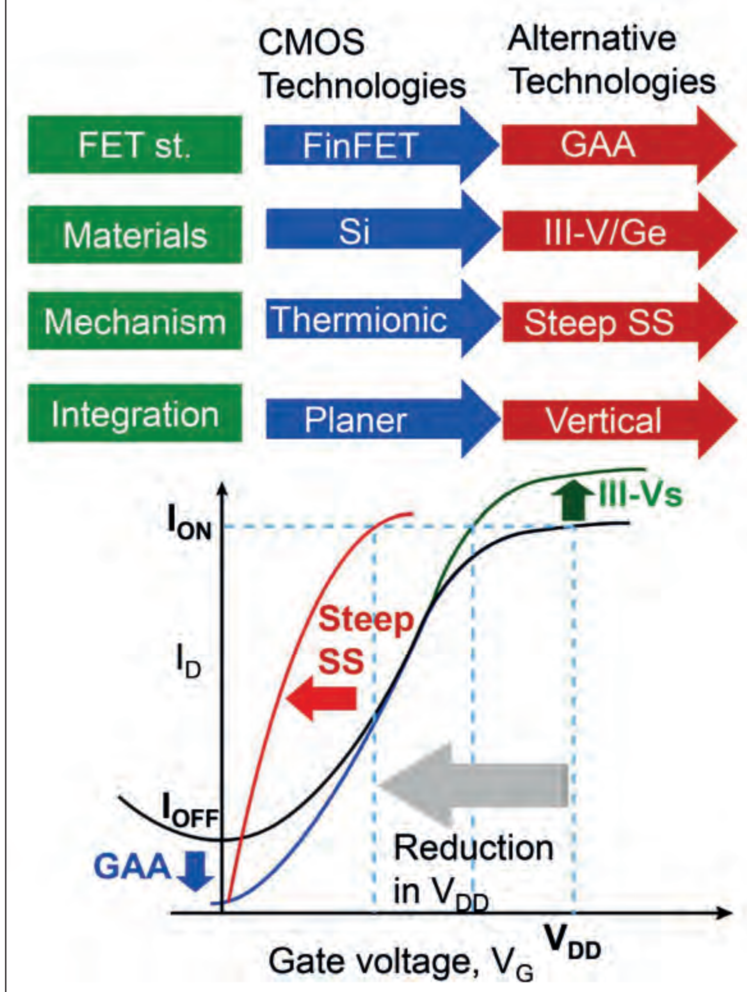
➤ Table 1. Comparison of conventional wearable devices. The device performance and functionality refers to values of RAM memory. Performance per volume rapidly decreases. The performance ratio is the fraction of the performance per volume compared with that of a smartphone.

when these alternatives to silicon are deployed in a multi-gate architecture, efforts must be directed at driving down the leakage current.

Another issue that can arise when using higher mobility materials is that there is an inherent mobility mismatch between the *n*- and *p*-channels – this is a problem in CMOS architectures. It may not seem a big issue, given that designers of LSI can adjust the device area to ensure current matching between *n*-channel and *p*-channel FETs. However, this is not possible when there is an extreme mobility difference, such as that found in some III-V/germanium materials. In these cases, more success might result from expanding the device area out of the plane, since faster channels are restricted to the vertical gate-all-around architecture.

When considering all the options for the choice of material and architecture, high on the wish list is a steep subthreshold slope, because this enables substantial reductions in the supply voltage and the power consumption. With modern LSI, there are inherent issues associated with increases in power consumption, and they are exacerbated as transistor density increases. The underlying cause is that electrons and holes follow the Boltzmann distribution. This physical law dictates that the minimum value for the sub-threshold slope, which determines the supply voltage for the FETs, is about 60 mV/decade at room temperature (the sub-threshold slope is equal to 2.3 $k_B T/q$, where k_B is the Boltzmann constant, T is the temperature, and q the elementary charge). With the lower limit for the sub-threshold slope pegged at 60 mV/decade, the power consumption for the ICs has to increase as the integration density increases.

Fortunately, there is a way to overcome this limitation. What's needed is to switch to a device that operates on non-thermionic processes, as they are not governed by the Boltzmann distribution of carriers. Operation of such devices may be based on quantum tunnelling, impact ionization, negative-capacitance, or mechanical vibrations. With any of these switching mechanisms the sub-threshold slope can be far steeper than 60 mV/decade.



➤ Figure 1. There are alternative technologies for conventional CMOS; FET structures, channel materials, switching mechanisms, and integration schemes. Included is an illustration of switching curves by introducing alternative technologies.

A history lesson

Back in the late 1980s, Japanese engineer Fujio Masouka and his co-workers, working at Toshiba, invented the first vertical gate-all-around FET. Masouka, incidentally also the inventor of NAND flash memory, referred to this device as the surrounding-gate transistor. Whatever its name, it is a device that that will change the integration paradigm. Right now, all electronics devices used in our daily lives are based on the electronics of the 1960s. While deviating from this is certainly challenging, it has to happen, with a shift to the designs shown in Table 1. It is a change that is certainly feasible, since flash memory already uses a type of vertical gate-all-around architecture.

Our view is that all the alternative technologies overviewed in Figure 1 need to be mutually developed to realize a wearable, augmented-reality device with a high-performance computing system. We expect that heterogeneous direct integration of III-V nanowires on silicon and vertical gate-all-around tunnel FETs will both play an important role in this development, because nanowires with a tunnel III-V/silicon junction can include all of the technologies shown in Figure 1. A key attribute of TFETs that comprise all these technologies is that they have a much lower sub-threshold swing, allowing the supply voltage to plummet to just 0.2 V.

For TFETs, the steepness of the sub-threshold slope strongly depends on the bias condition. Apply a high internal electrical field to the tunnel junction and the addition of a smaller bias realises a steep sub-threshold slope. Thus, by taking care of the series resistance in the TFET, a steep sub-threshold slope may be realised. Alternatively, this can be engineered by combining a moderate tunnel junction with materials with precisely controlled doping and gate

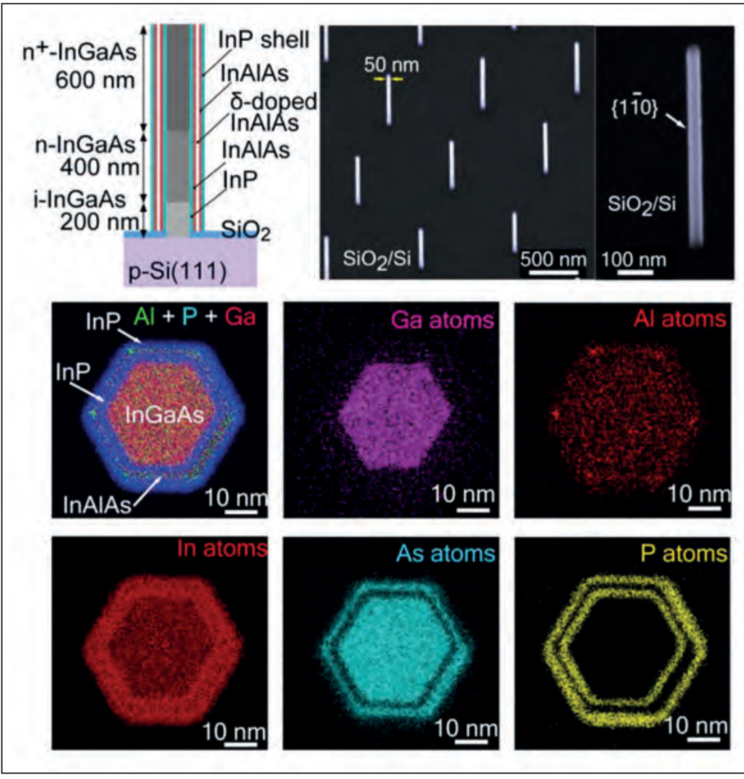
stacking technology. The latter approach is the one we have pursued.

One of the challenges with the TFET is ensuring a high enough on-current. As its value is determined by the tunnelling probability, this current depends on junction material characteristics, such as energy gap, effective mass and screening tunnelling length.

We have targeted a high on-current and a low sub-threshold slope when developing our devices. The design that we have trailblazed is a vertical gate-all-around TFET with a vertical InGaAs nanowire/silicon heterojunction and modulation-doped, core-multishell nanowire heterostructure. Selective-area growth is used to form this transistor.

There is much merit with our design. There is a staggered type-II band discontinuity at the *n*-InGaAs nanowire/*p*-silicon junction that aids TFET operation. What's more, the vertical gate-all-around structure of the grown nanowire channels only modulates the potential of the InGaAs nanowire-edge – degeneration of the *p*-silicon is neglected, resulting in potentially good electrostatic gate control, key to obtaining a steep sub-threshold swing. Yet another asset of our architecture is that the two-dimensional electron gas that is generated by our core-multishell structure increases carrier concentration and tunnelling probability at the nanowire/silicon junction, and ultimately boosts our on-current.

A representative growth by our team results in vertically integrated nanowires on silicon, based on InGaAs/InP/InAlAs/δ-doped InAlAs/InAlAs/InP core-multishell layers (see Figure 2). Within these structures, there is a core $In_{0.8}Ga_{0.2}As$ nanowire-channel with a: 200 nm-long, nearly intrinsic a zinc-pulsed doped layer; a 400 nm-long part with a silicon-doped layer; and a 600 nm-long part, heavily doped with tin. We use this axial junction to adjust the series resistance in the nanowire-channel, and to induce a large internal electric field under low bias. The thicknesses of the InP, InAlAs, δ-doped InAlAs, InAlAs, and InP capping layers are about 2.5 nm, 1.0 nm, 1.0 nm, 1.0 nm and 3.0 nm, respectively. Those values indicate that in these heterostructures fine 3D nanostructures can be precisely controlled on the atomic layer scale by selective-area growth. Critical to device performance is the inclusion of the



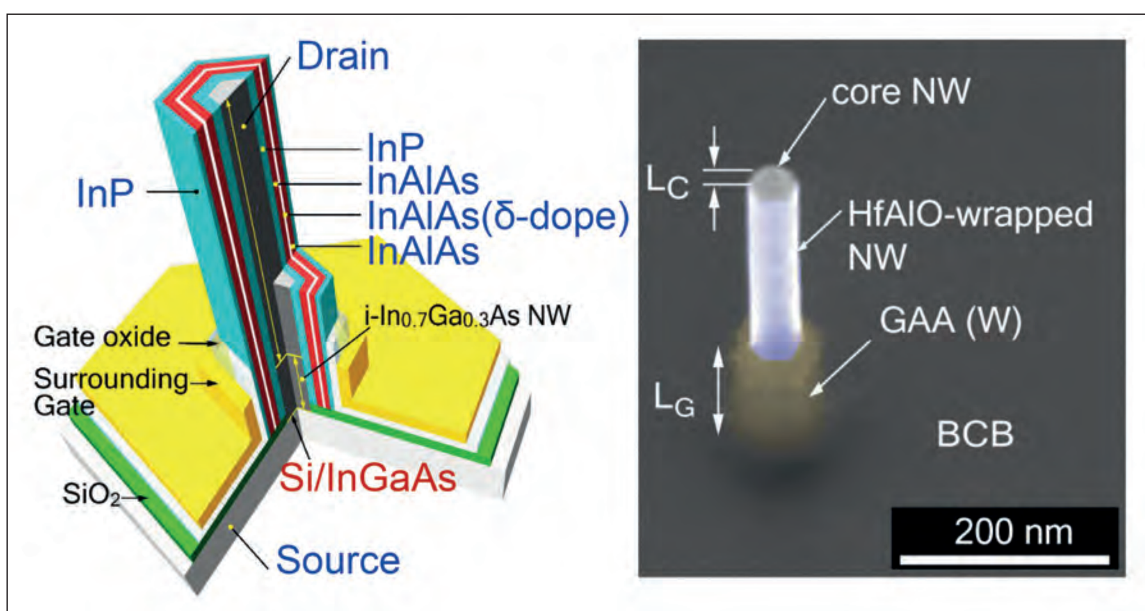
➤ Figure 2. (top left) The structure of vertical III-V nanowires on silicon, formed by direct growth. (middle and bottom) Energy-dispersive X-ray microscopy elemental mapping of nanowires composed of an InGaAs/InP/InAlAs/InP core-multishell structure.

inner InP shell layer, which facilitates the combination of a two-dimensional electron gas and quantum tunnelling.

The structure of our vertical gate-all-around TFET has been fabricated with a 3D device process flow, using a low-κ polymer resin, known as BCB (see Figure 3). Wrapping around the sidewalls of the nanowire-channel are a gate oxide, HfAlO composite oxide and tungsten gate metal, all added by atomic layer deposition. We have imaged this structure with scanning electron microscopy, after the reactive-ion process, and can see the core InGaAs nanowire on top of the nanowire channel.

The next step in our fabrication process is to form a Ni-InGaAs alloy contact with a small contact resistance

We have targeted a high on-current and a low sub-threshold slope when developing our devices. The design that we have trailblazed is a vertical gate-all-around TFET with a vertical InGaAs nanowire/silicon heterojunction and modulation-doped, core-multishell nanowire heterostructure



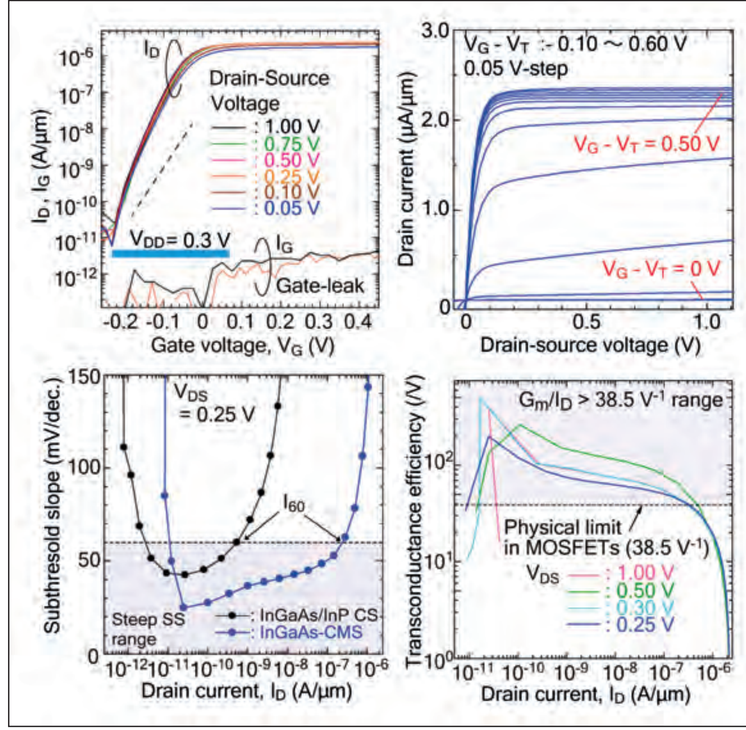
➤ Figure 3. The vertical gate-all-around TFET structure has a core-multishell and a modulation-doping structure. A scanning-electron microscopy image shows the representative device structure formed using a 3D device process.

to the core tin-doped InGaAs nanowire. After forming the Ni-InGaAs alloy layer, we deposit a drain of Ti/Au on top of the nanowire channel.

Delivering the promises

To assess the performance of our transistors, we have used a standard setup – a Keysight B1500A or 4156C, with a SMU cable – in a shielded box. Values reported for the current are normalized by the outer perimeter of the core nanowire, which is around 100 nm.

Measurements on our TFETs reveal a steep sub-threshold slope, with a minimum value of just 21 mV/decade (see Figure 4). The gate voltage window for the digital switch is 0.3 V, which is about one third of that of a modern FET. The current region where there is a steep sub-threshold slope extends over around four decades, while the average value for this key characteristic is 40 mV/decade.



The currents produced by our devices are very encouraging. At a 0.5 V supply voltage, the on-current reaches 2.4 mA/μm – that's a hundred times higher than that for a InGaAs/InP core-shell nanowire/silicon-based vertical gate-all-around TFET. With that design, the core-shell nanowire induces strain inside the core InGaAs nanowire, leading to a slight increase in on-current. Our core-multishell nanowire has the same strain effect, but a far larger current enhancement, thanks to the two-dimensional electron gas in the nanowire channel. The current at a sub-threshold slope of 60 mV/decade is 0.24 μA/mm, which is a thousand times higher than that of the core-shell nanowire/silicon-based vertical gate-all-around TFET.

Plotting the output properties of our devices reveals a unique curve, with a saturation region at a drain-source voltage of around 0.10 V. Insertion of an intrinsically doped InGaAs nanowire segment leads to an absence of the negative-differential resistance, sometimes observed in TFETs, when our device is operated under a negative drain-source voltage (that is a forward bias against *p*-silicon/*i*-InGaAs nanowire/*n*-

➤ Figure 4 (left). Device performance of the vertical gate-all-around TFET. I_D-V_G curve shows a steep sub-threshold slope (the minimum sub-threshold slope is 21 mV/dec.) and high I_{ON}. The blue bar in this graph is V_{DD} = ~0.30 V. The I_D-V_D curve exhibits unique output properties. The sub-threshold slope vs I_D indicates a steep sub-threshold slope region in the range of about four decades, and a high I60. Transconductance efficiency is much higher than the physical limitation of conventional MOSFETs.

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Mark Andrews is technical editor of Silicon Semiconductor, PIC Magazine, Solar+Power Management, and Power Electronics World. His experience focuses on RF and photonic solutions for infrastructure, mobile device, aerospace, aviation and defence industries

JACKIE CANNON
Director of Solar/IC Publishing, with over 15 years experience of Solar, Silicon and Power Electronics, Jackie can help moderate your webinar, field questions and make the overal experience very professional

PHIL ALSOP
Journalist and editor in the business to business publishing sector for more than 30 years currently focusing on intelligent automation, DevOps, Big Data and analytics, alongside the IT staples of computing, networks and storage

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Dr Richard Stevenson is a seasoned science and technology journalist with valuable experience in industry and academia. For almost a decade, he has been the editor of Compound Semiconductor magazine, as well as the programme manager for the CS International Conference

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InGaAs nanowire). A Kane model's plot shows that the dominant transport mechanism is based on tunnelling. Another strength of our TFETs is their exceptional transconductance efficiency, which is defined as the transconductance, divided by the drive current. This metric is a measure of the efficiency of the current drive in the ICs. For our devices, its value exceeds the physical limitation of the MOSFET, which is restricted to no more than 38.5 /V. For conventional FETs, this efficiency is virtually zero in the low-current region, while our vertical gate-all-around TFET exceeds this limitation over a wide current range. Transconductance efficiency peaks at around 520 /V at a drain source voltage of 0.25 V.

Note that it is not important that the maximum efficiency is high. Instead, what matters is that this efficiency exceeds the limits of the silicon FET over a wide range of low-current levels. When vertical gate-all-around TFETs are configured with a sufficiently high level of parallelism, there is no longer the need to pursue planar integration of the silicon FETs to try and improve performance as volume decreases (the requirement discussed in Table 1). The vertical gate-all-around TFET is also far better at thermal dissipation.

One other attribute of our TFETs is that, without a change in configuration, they can show *p*-channel behaviour with a steep sub-threshold swing. We need to look into this device mechanism in more detail, but preliminary investigations show that inverting the ground terminal results in a *p*-channel switch. The encouraging implication is that by simply aligning the vertical nanowires, a CMOS architecture can be constructed by forming interconnections for the ground terminals.

We have developed the integration of devices based on vertical III-V nanowires on silicon step by step; we began with nanowire HEMTs, nearly a decade ago, and now we have moved on to TFETs with a vertical gate-all-around architecture. We view these technologies as a continuation of Masuoka's invention that will lead to the next true 3D integration scheme, taking us away from today's planar integration devices, which have their roots in the 1960s. The vertical III-V architectures that we are pioneering accommodates co-integration and hybrid integration schemes. We are standing on the edge of a technology that will open up a new era, lasting for possibly the next 60 years.

FURTHER READING

- XK. Tomioka *et al*. Nature **488** 189 (2012)
  K. Tomioka *et al* IEEE IEDM Tech. Dig. **429** (2020)

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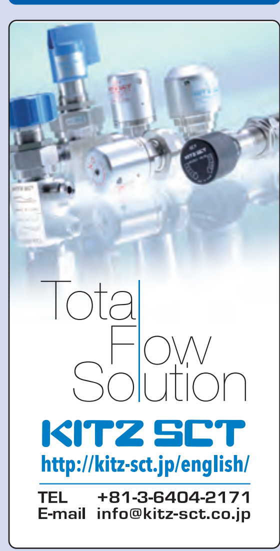

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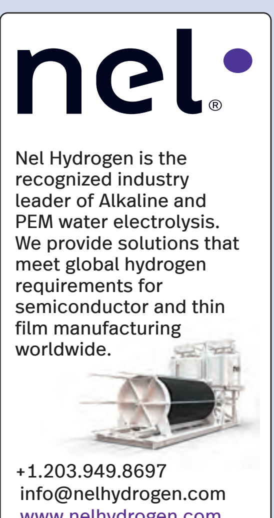

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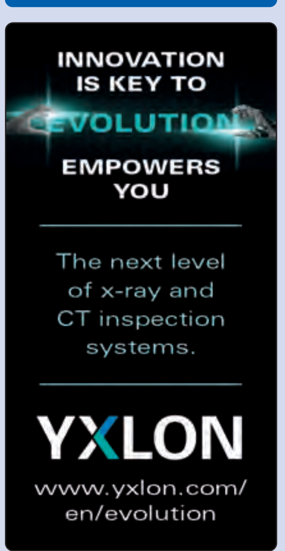

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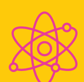
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