SILICON SEMICONDUCTOR
CONNECTING THE SILICON SEMICONDUCTOR COMMUNITY

THE CHALLENGE OF DECARBONISING THE SEMICONDUCTOR INDUSTRY AND FULFILLING CHIP DEMAND

VOLUME 45 ISSUE III 2024
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INSIDE

Wafer-level integration of ALD for 2D Materials

Meeting the challenges of advanced process development for the integration of ALD grown 2D materials at wafer level

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From the geopolitical sparring of China and the US to the global supply chain upon which we all depend

Lasers: a sustainable wafer heating solution

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VIEWPOINT

By Phil Alsop, Editor

Collaboration – the way forward

IN PREPARING the potential news stories for this issue of SiS, I was struck by the sheer quantity of stories on our website which highlight some of the many initiatives which individual countries, and both smaller and wider regions, are undertaking in pursuit of what seems to be the major focus on onshoring or reshoring.

In no particular order, I read stories referencing EU, Swiss, Japanese, Indian, German, UK and US projects, designed to increase the semiconductor industry footprint in each location.

So, much more local activity, but on a global scale.

I guess the major choice facing any local, national or regional government is what is possible, practical and, ultimately, affordable, in terms of encouraging the development of a semiconductor industry 'closer to home'. Key to making this decision is a good understanding of who is doing what, where and how. In other words, there are several options which can be pursued when it comes to playing in this space.

At the highest level, there's the possibility to create a complete, large scale, end-to-end semiconductor manufacturing supply chain. Such a strategy comes with an incredibly high price tag, but maybe one worth paying in terms of the security it provides, as well as the potential commercial return over the medium to long term. For most locations, the investment required for such an approach is prohibitive. This then leaves the decision of what area(s) in which to specialise and/or how to collaborate with other like-minded and nearby locations to develop a semiconductor focus which promises to deliver a level of specialist knowledge and expertise which can compete with the end-to-end approach in one or more part of the semiconductor industry supply chain.

It's fascinating to hear and read about all of the many partnerships and initiatives which are a part of the industry's evolution right now. Theoretically, there's room for everyone to share in the industry's predicted expansion and success, heading towards the $1 trillion/2030 objective. And sharing would seem to be the name of the game. Working with others – government at all levels, academic bodies, other vendors and, importantly, potential and actual customers – gives the best possible chance of success. I look forward to more and more examples of industry collaboration bringing huge benefits to many over the coming months.

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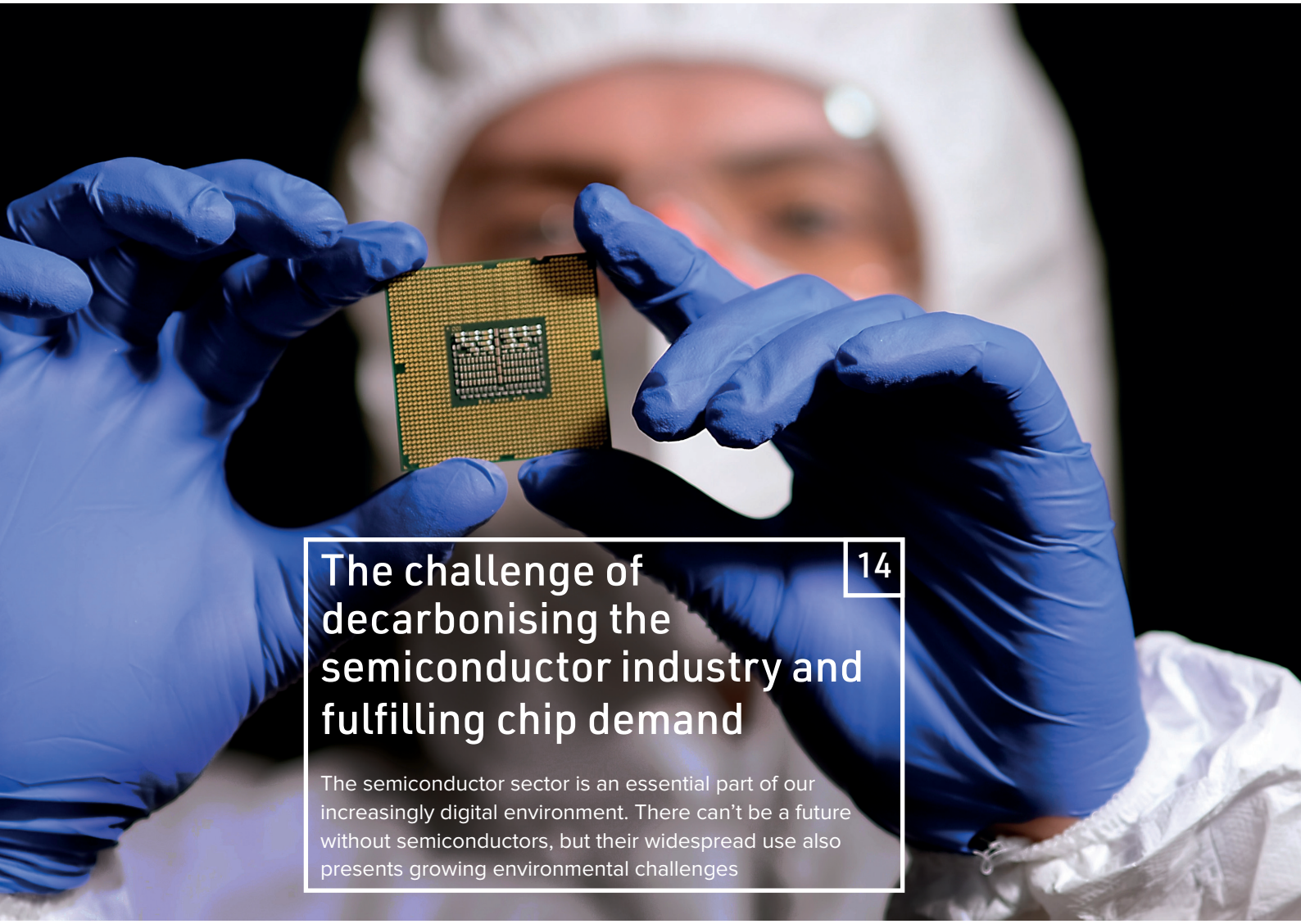

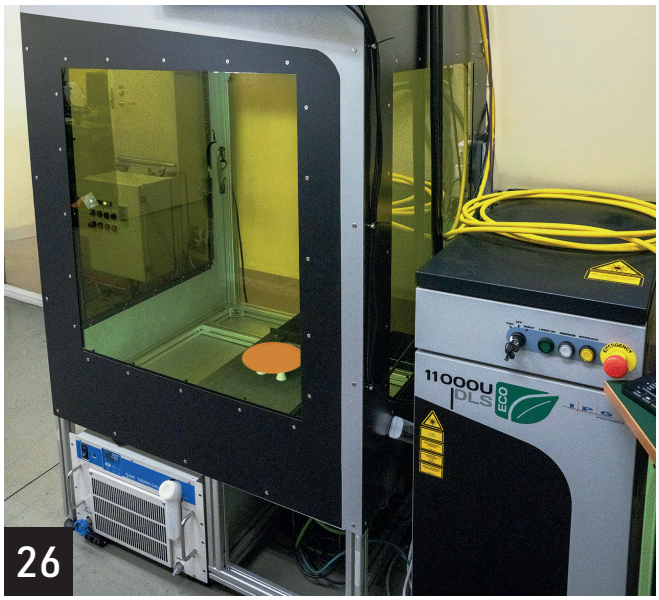

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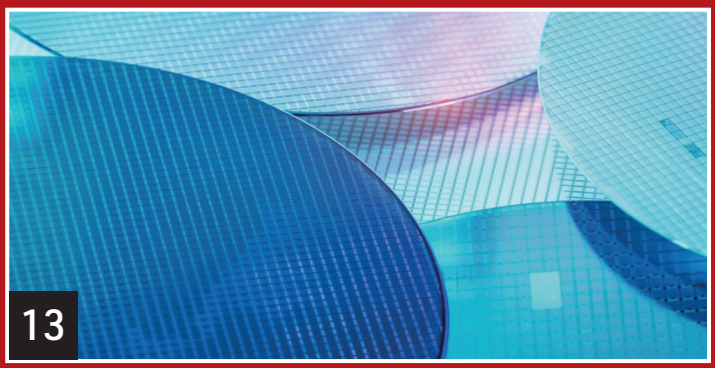
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EU Consortium accepting Edge-AI design proposals

A new European Union consortium created to accelerate the development of next-generation, edge-AI technologies is installing cleanroom tools and gearing up to design, evaluate, test and fabricate new circuits from across Europe.

COORDINATED by the EU's four leading research and technology organizations (RTOs), France's CEA-Leti, Germany's Fraunhofer-Gesellschaft, Belgium-headquartered imec and Finland's VTT, the PREVAIL project is a networked, multi-hub platform providing prototype chip fabrication capability in advanced artificial technology to EU stakeholders. In most cases, the technology offer will be based on commercial foundry processes, and advanced technology modules will be enhanced in the cleanrooms of the project partners.

"The PREVAIL project's ultimate goal is to position Europe with an easy-access, advanced manufacturing infrastructure enabling users to make early research samples of innovative and trustworthy products and accelerate their commercialization," said Sergio Nicoletti, CEA-Leti business development manager and PREVAIL project manager. "And while bringing their cutting-edge technologies to a higher maturity level and giving users the possibility to fabricate and test AI prototypes based on these technologies, the RTOs are reaping the benefits of technological cross-fertilization."

"In addition to providing high-performance, low-power edge components and technologies to support the massive data-processing requirements of AI, the project will help energize the EU's digital transformation, a precursor to the goals of the European Chips Act," he said.

Launched at the end of 2022, the project is leveraging the RTOs' advanced 300 mm fabrication, design and test facilities and related expertise to create the Testing and Experimentation Facility for Edge-AI Hardware (TEF Edge AI HW). This

network will validate new high-performance, low-power, edge-AI components and support an infrastructure capable of fabricating early research prototype samples for testing in innovative edge-AI applications.

Nicoletti said the consortium is working with selected SMEs, the RTOs' industrial partners and academic labs to prepare early designs that will be used to test fabrication equipment in the RTOs' facilities. The project plans to open access widely for EU designers by May 2026.

While 80 percent of the project's budget targets equipment suited for design, testing and fabrication of edge-AI devices, the project also will dramatically reinforce the readiness of the RTOs to equip their new pilot lines for developing 3D technologies, which also are envisioned in the chips act.

Key project components

In addition to fabricating advanced edge-AI applications and creating the platform's TEF Edge AI HW, the consortium will provide process design kits (PDKs) compatible with standard commercial CAD tools and all the elements necessary for full chip design. A user-interface team will manage relationships among the developers of next-generation, edge-AI solutions and the consortium.

PREVAIL is the EU's first step to link the RTO's different infrastructures and synchronize and coordinate their investments to minimize duplication, and to jointly increase the technology readiness levels (TRLs) of tools in development. The nearly €156 million ($169.3 million) cost of the 42-month project will be shared by the RTOs' countries and the European Commission. Approximately 80 percent of this funding is CAPEX invested in new tools suited for edge-AI devices.

PREVAIL's founding members

CEA
CEA-Leti
Fraunhofer-Gesellschaft
Imec
VTT Technical Research Centre of Finland Ltd

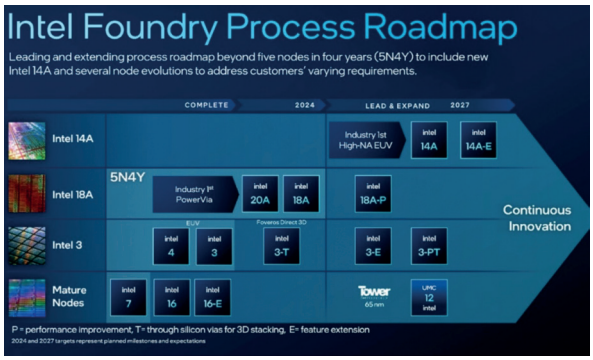
Intel launches new foundry designed for the AI era

Intel announces expanded process roadmap, customers and ecosystem partners to deliver on ambition to be the No. 2 foundry by 2030.

INTEL has launched Intel Foundry as a more sustainable systems foundry business designed for the AI era and announced an expanded process roadmap designed to establish leadership into the latter part of this decade. The company also highlighted customer momentum and support from ecosystem partners – including Synopsys, Cadence, Siemens and Ansys – who outlined their readiness to accelerate Intel Foundry customers' chip designs with tools, design flows and IP portfolios validated for Intel's advanced packaging and Intel 18A process technologies.

The announcements were made at Intel's first foundry event, Intel Foundry Direct Connect, where the company gathered customers, ecosystem companies and leaders from across the industry. Among the participants and speakers were U.S. Secretary of Commerce Gina Raimondo, Arm CEO Rene Haas, Microsoft CEO Satya Nadella, OpenAI CEO Sam Altman and others.

An Intel factory employee holds a wafer with 3D stacked Foveros technology at an Intel fab in Hillsboro, Oregon, in December 2023. In February 2024, Intel Corporation launched Intel Foundry as the world's first systems foundry for the AI era, delivering leadership in technology, resiliency and sustainability. (Credit: Intel Corporation)
"AI is profoundly transforming the world and how we think about technology and the silicon that powers it," said Intel CEO Pat Gelsinger. "This is creating an unprecedented opportunity for the world's most innovative chip designers and for Intel Foundry, the world's first systems foundry for the AI era. Together, we can create new markets and revolutionize how the world uses technology to improve people's lives."



Process roadmap expands beyond 5N4Y

Intel's extended process technology roadmap adds Intel 14A to the company's leading-edge node plan, in addition to several specialized node evolutions. Intel also affirmed that its ambitious five-nodes-in-four-years (5N4Y) process roadmap remains on track and will deliver the industry's first backside power solution. Company leaders expect Intel will regain process leadership with Intel 18A in 2025.

The new roadmap includes evolutions for Intel 3, Intel 18A and Intel 14A process technologies. It includes Intel 3-T, which is optimized with through-silicon vias for 3D advanced packaging designs and will soon reach manufacturing readiness.
Also highlighted are mature process nodes, including new 12 nanometer nodes expected through the joint development with UMC announced last month. These evolutions are designed to enable customers to develop and deliver products tailored to their specific needs. Intel Foundry plans a new node every two years and node evolutions along the way, giving customers a path to continuously evolve their offerings on Intel's leading process technology.

Intel also announced the addition of Intel Foundry FCBGA 2D+ to its comprehensive suite of ASAT offerings, which already include FCBGA 2D, EMIB, Foveros and Foveros Direct.

Microsoft design on Intel 18A headlines customer momentum

Customers are supporting Intel's long-term systems foundry approach. During Pat Gelsinger's keynote, Microsoft Chairman and CEO Satya Nadella stated that Microsoft has chosen a chip design it plans to produce on the Intel 18A process.

"We are in the midst of a very exciting platform shift that will fundamentally transform productivity for every individual organization and the entire industry," Nadella said. "To achieve this vision, we need a reliable supply of the most advanced, high-performance and high-quality semiconductors. That's why we are so excited to work with Intel Foundry, and why we have chosen a chip design that we plan to produce on Intel 18A process."

Intel Foundry has design wins across foundry process generations, including Intel 18A, Intel 16 and Intel 3, along with significant customer volume on Intel Foundry ASAT capabilities, including advanced packaging.

In total, across wafer and advanced packaging, Intel Foundry's expected lifetime deal value is greater than $15 billion.

IP and EDA vendors declare readiness for Intel process and packaging designs

Intellectual property and electronic design automation (EDA) partners Synopsys, Cadence, Siemens, Ansys, Lorentz and Keysight disclosed tool qualification and IP readiness to enable foundry customers to accelerate advanced chip designs on Intel 18A, which offers the foundry industry's first backside power solution. These companies also affirmed EDA and IP enablement across Intel node families.

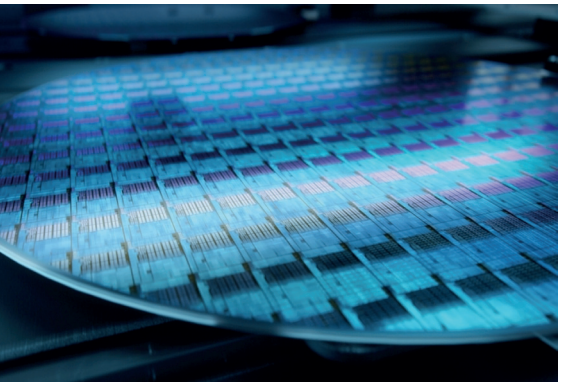
Saxony-Anhalt embraces change as an opportunity

Billions invested in key transformation industries.

THE LARGEST investment project not only in Saxony-Anhalt but in all of Europe is Intel's establishment in Magdeburg. Approximately 30 billion euros are set to be invested in the construction of multiple chip factories. The company has initiated collaborations with six universities in Saxony-Anhalt and is actively recruiting its initial workforce. Approval processes commenced in February, paving the way for the production of the world's most advanced chips in the two factories starting from 2027.

Saxony-Anhalt – HERE is the place for big plans

In addition to Intel, numerous other semiconductor companies are also making substantial investments. Sioux Technologies, a globally recognized technology accelerator with around 1,100 employees, is developing strategic high-tech solutions for various markets such as semiconductors, laboratory and medical technology, mechatronics, imaging, mobility, and clean energy. In Barleben, Sioux plans to invest around 20 million euros in a research and development center, gradually creating three hundred highly qualified permanent jobs.



Meanwhile, in Bernburg, a large high-performance distribution center for semiconductors and electronic components is taking shape. The topping-out ceremony for Avnet's Electronics Distribution Center was celebrated in November 2023, with an investment volume exceeding 225 million euros. Over the next eight years, around 700 jobs are expected to be created in Bernburg.

Sven Schulze, Minister for Economic Affairs, Tourism, Agriculture, and Forestry of the State of Saxony-Anhalt, emphasizes the economic dynamism of the region against the backdrop of these examples: "Saxony-Anhalt is on the fast track. High-profile fast-track approvals, a central location in Europe, close collaboration with educational institutions, and attractive conditions such as affordable rents and sufficient childcare spaces make investments and living here exceptionally appealing."
Life Sciences Take Pioneering Role in Saxony-Anhalt's Future

Saxony-Anhalt is establishing itself as a leader in the field of Life Sciences, showcasing the state's future resilience. The mRNA Center in Halle (Saale) is taking shape, with the Wacker Chemie AG demonstrating serious ambitions in this cutting-edge technology through a substantial investment exceeding 100 million euros. The new facility is expected to host around 200 employees. Additionally, the Magdeburg-based medical technology company Neoscan Solutions recently secured a contract to build the world's most powerful 14 Tesla MRI magnet for human examinations.

Chemical parks in Saxony-Anhalt are undergoing expansion and sustainable transformation, with Germany's largest Chemical Park Leuna, being one of the nation's largest construction sites. Over 100 companies from eleven nations are investing 1.3 billion euros in research and green chemistry. The expansion is set to create up to 250 direct and 750 indirect jobs, primarily in the sustainable chemistry sector. AMG Lithium has chosen the Chemical Park Bitterfeld-Wolfen for a 140-million-euro investment to purify lithium hydroxide, transforming it into a battery-grade raw material – a unique endeavor in Europe.

Innovations in renewables and storage technologies

NexWafe, a US-based company, is investing 30 million euros in Bitterfeld-Wolfen to establish a factory for producing solar wafers, a crucial material for the photovoltaic industry. In Bitterfeld, the German company Silicon Products, in collaboration with a French partner, aims to produce high-purity silicon carbide, a vital resource for nearly all semiconductor manufacturers.

TESVOLT AG, a leading technology company in commercial and industrial energy storage, plans to construct a new Gigafactory in Lutherstadt Wittenberg, investing around 60 million euros. The long-term goal is to create over 400 new jobs, particularly in research and development.

The automotive and logistics sectors are also experiencing rapid development from international players. LMG Manufacturing, an aluminum die-casting specialist, inaugurated its new manufacturing hall in Hoym/Seeland after just ten months of construction.

Daimler Truck's largest logistics project commenced with the official groundbreaking in Halberstadt in September 2023. The Global Parts Center in Halberstadt/Harz aims to deliver spare parts worldwide starting in 2025, generating approximately 450 jobs with an investment of nearly 500 million euros.

Dr. Robert Franke, Managing Director of the Investment and Marketing Corporation Saxony-Anhalt mbH, emphasizes, "Saxony-Anhalt is an attractive and sought-after location for settlement. We are witnessing significant investments not only in the chip industry but also in various other sectors such as pharmaceuticals, medical technology, and the automotive industry. This underscores why Saxony-Anhalt has gained considerable international visibility."

Taalas emerges from stealth

$50 million in funding and a 'groundbreaking' silicon AI technology.

TAALAS INC., an innovator in AI and silicon, has exited stealth mode and raised $50 million dollars over two rounds of funding led by Pierre Lamond and Quiet Capital.

Over the last year, AI has undergone a large scale productization and has already begun reshaping the world. Concurrently, deep learning models have become the world's most demanding computational workload, unsustainably capital intensive, power hungry, and GPU constrained.

"Artificial intelligence is like electrical power – an essential good that will need to be made available to all.

Commoditizing AI requires a 1000x improvement in computational power and efficiency, a goal that is unattainable via the current incremental approaches.

The path forward is to realize that we should not be simulating intelligence on general purpose computers, but casting intelligence directly into silicon. Implementing deep learning models in silicon is the straightest path to sustainable AI," said Ljubisa Bajic, Taalas' CEO.

Taalas is developing an automated flow for rapidly implementing all types of deep learning models (Transformers, SSMs, Diffusers, MoEs, etc.) in silicon.

Proprietary innovations enable one of its chips to hold an entire large AI model without requiring external memory. The efficiency of hard-wired computation enables a single chip to outperform a small GPU data center, opening the way to a 1000x improvement in the cost of AI.

"We believe the Taalas 'direct-to-silicon' foundry unlocks three fundamental breakthroughs: dramatically resetting the cost structure of AI today, viably enabling the next 10-100x growth in model size, and efficiently running powerful models locally on any consumer device.

This is perhaps the most important mission in computing today for the future scalability of AI. And we are proud to support this remarkable n-of-1 team as they do it," said Matt Humphrey, Partner at Quiet Capital.

Rolls-Royce supplies mtu Kinetic PowerPacks for semiconductor manufacturer X-FAB Sarawak

Four uninterruptible power supply units secure critical power load for semiconductor operations in Malaysia.

ROLLS-ROYCE has supplied and commissioned four of its mtu Kinetic PowerPacks to X-FAB Sarawak, the Malaysian division of X-FAB, the world's leading foundry group for specialty semiconductor applications.

The dynamic uninterruptible power supply (DUPS) units secure the critical power load for operations at the company's manufacturing site located in Kuching, Sarawak, Malaysia.

mtu Kinetic PowerPacks are engineered to perform seamlessly under the most demanding power supply challenges. They provide immediate, high-quality power through the use of kinetic energy. The units eliminate the need for batteries as in a standard UPS configuration, offer a much smaller footprint and are environmentally-friendly due to their 20+ year equipment life and their ability to run on sustainable fuels such as HVO.

Bryan Foo, Project Manager, Rolls-Royce Solutions Asia Pte. Ltd. said: "Being secure in the knowledge that your power supply is reliable and of the highest quality, even during times of grid instability or interruption, is important for any business but is especially vital for a company such as X-FAB Sarawak that has a consistent, high-level output of critical products and that supports many employees and corporate functions."

The X-FAB site in Kuching manufactures semiconductor wafers for automotive, industrial and medical applications and has more than 1,400 employees and a wide array of operations such as finance and procurement.

The four installed mtu Kinetic PowerPacks feature a medium voltage, parallel system configuration offering 2000 kVA (1600kW). They replace older, existing DUPS units from a different manufacturer that were experiencing ongoing issues with dropping critical load from the mains. In normal operation, when the public power supply is working, the mtu Kinetic PowerPacks use a choke - a heavy, rotating electromagnetic coil - to compensate for short-term current and voltage fluctuations in the power grid. The Kinetic PowerPacks also come with an mtu ValueCare service agreement, which provides preventative maintenance at regular intervals and technical support to ensure maximum performance.

Elvenrey Rios, Project Engineer, Rolls-Royce Solutions Asia Pte. Ltd. said: "Our project team upheld X-FAB's strong safety culture, product quality and user-friendly equipment during the entire process. The reliable critical load support provided by the current mtu Kinetic PowerPacks has also resulted in the customer engaging Rolls-Royce for an additional unit."

Kioxia and Western Digital's Joint venture

THE SUBSIDY will be granted under a designated government program aimed at facilitating corporate investment in cutting-edge semiconductor production facilities and securing stable production of semiconductors in Japan. This marks the second time that Kioxia's and Western Digital's joint venture manufacturing facilities are receiving this subsidy from the Japanese government.

Previously, the joint venture manufacturing facility at Yokkaichi was approved to receive up to 92.9 billion yen subsidy from the Japanese government in 2022.

Leveraging an over 20-year joint venture partnership, Kioxia and Western Digital will continue to enhance the development and production capabilities of cutting-edge flash memory at the Yokkaichi and Kitakami plants in Japan. In addition, the two companies will contribut e to the development of semiconductor-related industries and talent.

"We appreciate the support of the Japanese government and will continue to produce cutting-edge flash memory, which is indispensable for technologies that underpin the expanding digital transformation of society. With this subsidy, we will continue to contribute to the advancement of the semiconductor industry and the development of local and domestic economies," said Nobuo Hayasaka, President and CEO of Kioxia.

David Goeckeler, CEO of Western Digital said, "We thank the Japanese government for their ongoing and unwavering commitment to our joint venture flash memory manufacturing facilities in Japan and our long track record of innovations in the NAND flash industry."

SemiQon ships silicon-based quantum chip and transistors

Research groups around the world are now using these first-generation silicon-based chips helping the industry step faster to the million qubit level of quantum computing.

SEMIQON, a Finland-based startup specializing in silicon-based quantum processors, has successfully manufactured and pre-tested a 4-qubit quantum dot array from the first production run at its manufacturing facility in Espoo, Finland. The new chips are now shipping to strategic partners around the world as a toolkit for further research and development. The aim is to help make building stable logical qubits easier and faster to accelerate the use of quantum computing for complex problems.

First-generation quantum computers have already achieved impressive computational feats. However, solving highly specific problems related to pharmaceuticals, logistics, space, and material design will require increased computational power. As researchers, ecosystems, and companies around the globe lay out their ambitious visions for quantum computing, the computing power must still be scaled efficiently to address these challenges. Current methods do not make this possible. "We are gradually moving towards the million qubit era and the contribution of hardware is becoming more and more essential," says Dr. Himadri Majumdar, CEO and Co-founder of SemiQon. "Our solution builds on the technological development and know-how of semiconductors and benefits from existing infrastructure and industry. Utilizing such infrastructure effectively and efficiently has allowed us to accomplish one of our first goals within a short period of time. The challenge is getting to quantum supremacy in a sustainable, scalable, and affordable manner. These new chips are our first step in a long journey to making quantum dreams a reality."

SemiQon's strategic path of combining classical and quantum elements at cryogenic temperatures also took a big

leap forward through the demonstration of very low noise and better control over the channel using record low sub-threshold swing in the manufactured fully-depleted silicon-on-insulator metal-on-semiconductor (FDSOI-MOS) transistors. These transistors will be the backbone of realizing a cryogenic integrated circuit (IC), ultimately leading to quantum IC for scalable, efficient, and affordable quantum computers. The results will be communicated through a peer-reviewed international scientific article, which is currently under review.

SwissChips Initiative to boost Swiss chip industry

BY FOSTERING collaboration between academia and industry, the initiative aims to drive innovation and economic growth.

The SwissChips Initiative is a collaborative effort launched by CSEM, EPFL, and ETH Zurich, with support from various Swiss and European research entities, semiconductor associations, and industrial partners. This initiative is supported by the Swiss State Secretariat for Education, Research and Innovation (SERI).

Inspired by the US and European Chips Acts, this act aims to enhance the Swiss semiconductor sector by promoting cutting-edge research in integrated circuit (IC) design. The initiative covers a wide range of domains such as: Computing System on Chips (SoCs), 6G Communications, Space Electronics and Photonics, SoCs for Autonomous IoT Devices, Chips for EDGE AI, Biomedical Circuits and Systems, and Devices and Sensors. ETH Zurich coordinates the program, with all three founding institutions taking leading roles in their respective research areas.

These efforts are designed to bolster microelectronics and IC design research, innovation, development, and businesses, ensuring Swiss academic institutions have access to cutting-edge manufacturing and design technologies. Additionally, the initiative aims to foster the Swiss semiconductor, microelectronics, and IC design ecosystem, developing robust synergies among research institutions.

Enhance the semiconductor sector in Switzerland

The program involves PhD and Postdoc researchers, as well as the existing engineering and research staff of the participating institutions, who will push the boundaries of IC design. This concerted effort will not only enhance Switzerland's influence in the semiconductor industry during the post-Global Chip Shortage era of 2020-2023 but also ensure the development of infrastructure and technologies that benefit all scientific domains.

This includes making advancements accessible to Swiss universities and universities of applied sciences, thereby nurturing a holistic growth in the semiconductor, microelectronics, and IC design sectors.

Tata Group to build India's first indigenous facility in Assam

INR 27,000 crore investment in a greenfield facility in Assam for assembly and testing of semiconductor chips for applications across automotive, mobile devices, artificial intelligence (AI), and other key segments to serve customers globally.

IN A SIGNIFICANT step towards creating an end-to-end semiconductor manufacturing ecosystem in India, Government of India has approved a proposal by Tata Electronics to build a state-of-the-art, greenfield semiconductor assembly and test facility in Jagiroad, Assam. The facility will be built with an investment outlay of INR 27,000 crore and is expected to generate over 27,000 direct and indirect jobs in the region.

Tata Electronics Pvt Ltd (wholly owned subsidiary of Tata Sons Pvt Ltd) will build this facility focusing on three key platform technologies - Wire Bond, Flip Chip, and a differentiated offering called Integrated Systems Packaging (ISP), with plans of expanding the roadmap to advanced packaging technologies in the future. These technologies are extremely critical for key applications in India – like automotive (especially electric vehicles), communications, network infrastructure and others.

Tata Electronics has already made significant investments in indigenous technology development for all these platforms and has put together a very credible team with over 1,000+ years of global domain experience to drive this project. The proposed facility will serve the growing global demands across key market segments like AI, industrial, and consumer electronics.

The construction of the facility is scheduled to start this year with the first phase of the facility becoming operational by mid-2025 and will provide an immense boost to industrialization in North-East India. The project is envisioned under the Government of India's Semiconductor policy being driven by the India Semiconductor Mission and the Government of Assam's Electronics policy.
Semiconductor assembly and test is a critical part of the semiconductor value chain where wafers manufactured by semiconductor fabs are assembled or packaged and then tested before they are finally used in the desired product. Innovations in semiconductor assembly and test are driving increased performance, reduced form factor, and reduced costs of semiconductor chips.

Commenting on the announcement, N Chandrasekaran, Chairman, Tata Sons said, "We are in a unique time for the electronics manufacturing market globally and the world is seeking a more secure and resilient electronics supply chain. With our announcement of the semiconductor fab and this strategic project in semiconductor assembly and test, we will be enabling our global customers to base a key part of their semiconductor value chain in India. Alongside mitigating global supply chain risks, I am confident that this project will have a transformational impact towards technology led industrialization and job creation in the Northeast in particular.

Under the decisive leadership of Hon'ble Prime Minister Shri Narendra Modi, the Government of India has developed a comprehensive central and state semiconductor policy. This along with support from Ministry of Electronics and Information Technology, India Semiconductor Mission and the Government of Assam has made this announcement possible."

Dr Randhir Thakur, CEO & MD, Tata Electronics said, "The strategy of serving across the semiconductor value chain is our differentiator and will enable Tata Electronics to deliver complete system offerings to customers. We have a critical window of opportunity where we see tremendous customer pull from global players for manufacturing in India and we

plan to capitalize on this opportunity and leapfrog through technology innovation. This investment will go a long way in putting India on the map of global semiconductor manufacturing and in spurring a complete domestic ecosystem for high technology manufacturing while being an enabler for the indigenous product ecosystem."

The proposed facility in Jagiroad is strategically located with access to abundant water and green power – a key sustainability consideration for the Tata group and its customers globally. Assam is also closer to the current semiconductor packaging & test hubs in countries like Taiwan, Malaysia, Vietnam, and Singapore. Assam has technical and engineering workforce available from the entire North-East India, providing a stable talent pool for this project as well as the ecosystem development that this project will seed.

This new initiative from Tata Electronics will bring to India a portfolio of cutting-edge semiconductor technologies, advanced skill set and talent, and a network of semiconductor manufacturing suppliers and ecosystem partners, resulting in foundational development of indigenous semiconductor ecosystem in India.

This Assembly & Test facility will be able to directly ship semiconductor chips to end-users and OEMs (Original Equipment Manufacturers) in India and the world.

£35m boost for British semiconductor scientists and businesses

Semiconductor sector to benefit from up to £35m, plus European funds, in a boost to British leadership in research of cutting-edge chip technology.

BRITISH SEMICONDUCTOR researchers and businesses now have enhanced access to research funding backed by the UK Government and Horizon Europe, now the UK has joined the EU's 'Chips Joint Undertaking'.

The move provides the UK semiconductor sector enhanced access to a €1.3 billion pot of funds set aside from Horizon Europe to support research in semiconductor technologies up to 2027. Access to the one of the Chips Joint Undertaking's funds is being backed by an initial £5 million this year from the Department for Science, Innovation and Technology, and delivered by Innovate UK. An additional £30 million is due to support UK participation in further research between 2025 and 2027.

By joining the fund and contributing in the same way as all other countries who take part, the UK sector has enhanced access to bid for funding support from the €1.3 billion pot, funded by Horizon Europe. Announcing the move at a conference of global semiconductor leaders in London, Technology Minister Saqib Bhatti said: "Our membership of the Chips Joint Undertaking will boost Britain's strengths in semiconductor science and research to secure our position in the global chip supply chain.

"This underscores our unwavering commitment to pushing the boundaries of technology and cements our important role in shaping the future of semiconductor technologies around the world."

This follows the UK joining Horizon Europe through a bespoke new agreement with the EU last year. The programme is giving UK companies and research institutions unrivalled opportunities to lead global work to develop new technologies and research

projects, in areas from health to AI. Tens of thousands of UK companies are now eligible for Horizon Europe grants, which are worth £450,000 to a business on average. UK firms already benefitting from Horizon funding include Nova Innovation, whose consortium won over £17 million to develop tidal energy in Orkney, and South Yorkshire tech firm The Floow who are part of a project awarded just under £3 million, looking into road safety.

Jari Kinaret, Chips JU Executive Director, said: "We are very happy to welcome the UK to the Chips Joint Undertaking as a participating state. We are looking forward to working with the UK partners to develop the European industrial ecosystem in microelectronics and its applications, contributing to the continent's scientific excellence and innovation leadership in semiconductor technologies and related fields."

This year, the Chips Joint Undertaking fund is well aligned to UK research expertise. In 2024, it includes two focussed calls for funding bids on semiconductors for cars and other vehicles as well as RISC-V, an open-source architecture that aims to accelerate semiconductor innovation by lowering the cost of chip design. It also provides more open opportunities for scientists and firms to bid for research support. Sean Redmond, Managing Partner at SiliconCatalyst, added: "UK Semiconductor startups have a rich history of collaboration with the European Union. Our semiconductor research base is the fourth largest in the world.

"Commercialising these inventions with the help of the EU Chips Joint Undertaking will significantly increase their probability of success, mitigating risks by local collaborations that provide a clear path from lab to fab."

Jalal Bagherli, Chairman, PTSL, Chair, Williams Advanced Engineering and Co-Chair of UK Semiconductor Advisory Panel, commented: "As the UK Semiconductor Strategy ramps up its implementation phase in support of a thriving industry, I believe this initiative is the next major step enabling engagement with our global partners to advance the state of the art in chip development and innovative packaging technologies in the UK".

The UK has joined the initiative as a "Participating State", allowing the country to collaborate more closely with European partners on semiconductor innovation. As a Participating State, the UK will have a role in setting research priorities and funding decisions as the fund evolves in the years ahead. This includes the opportunity for the UK to be a part of a new funding opportunity with the Republic of Korea to research ways to combine semiconductor chips to improve performance through advanced packaging – which the UK-Republic of Korea Semiconductor Framework, signed in November last year.

British research has elsewhere led global efforts to push semiconductor technology forward in fields like "silicon photonics", which creates faster chips by using light instead of electricity, and compound semiconductors, which enable improved performance over silicon in key applications such as power transmission and radiofrequency communications.

The challenge of decarbonising the semiconductor industry and fulfilling chip demand

The semiconductor sector is an essential part of our increasingly digital environment. Its technologies, which include cell phones and computers we use for communication, the vehicles and aircraft that allow us to transport, the medical equipment that aids in disease diagnosis and treatment, and the grid systems that power our cities, are essential to everyday life. There can't be a future without semiconductors, but their widespread use also presents growing environmental challenges.

BY HENRI BERTHE, SEMICONDUCTOR VICE PRESIDENT, SCHNEIDER ELECTRIC

THE ENVIRONMENTAL COST of semiconductors
To meet demand, semiconductor players are building new fabrication plants (FABS), which can use as much as 100 megawatt-hours of power each hour—more than many automotive plants or oil refinery. This massive amount of electricity consumption will result in significant waste generation, greenhouse gas emissions and large carbon footprint In 2020, the industry emitted an astounding 41 million tonnes[VT2] of CO_2, the equivalent of 5 million houses› annual emissions. And by 2030, semiconductor manufacturing is projected to consume 237 TWh of electricity globally, around equal to Australia's total 2021 electrical consumption.

As electronics grow in importance, manufacturers must navigate concerns around energy consumption and sustainability. Recent McKinsey research finds that major semiconductor companies' latest

commitments are still falling short of what is required under the 2016 Paris Agreement. As a result, businesses that fail to make their operations more environmentally friendly may face stronger restrictions and sanctions from future governments, as well as decreasing orders from increasingly environmentally sensitive customers.

Conversely, those who optimise their energy efficiency early will unlock considerable resource savings and huge opportunities for growth.

To protect their businesses' futures, it is essential for manufacturers to start establishing sustainable practices today.

Upholding sustainability with resilience

Aside from environmental problems, many manufacturers are still dealing with the fallout from the global semiconductor crisis. A 'perfect storm' of global events almost brought production to a standstill throughout the pandemic: COVID-19's lockdowns both accelerated demand for consumer electronics and closed the factories producing the required components. Meanwhile, the China–United States trade war, Russia–Ukraine war, severe weather events, production facility fires, and a general reliance on semiconductor imports, rather than domestic manufacturing, also contributed to the sustained scarcity.

At the height of the chip shortage, research indicated that up to 169 businesses were affected globally. The consumer electronics and automotive industries took the brunt of the damage. PlayStation 5 consoles became akin to gold dust and Apple slashed its iPhone manufacturing targets, while Toyota reduced car manufacturing by 40% and General Motors paused vehicle production across North American plants.

Overall, the shortage cost the auto industry as much as $210 billion in revenue in 2021. And though manufacturers have now adapted to a constrained supply, increasingly complex products, such as electric vehicles with advanced safety and autonomy systems, will continue to accelerate semiconductor demand and spark a significant change in the manufacturing landscape.

As semiconductor production has been concentrated in Asia for the past 10 years, organisations and countries are now looking to create more diverse, resilient supply chains. In October 2022, the US government administered export control rules to constrain China's production of the world's most advanced chips.

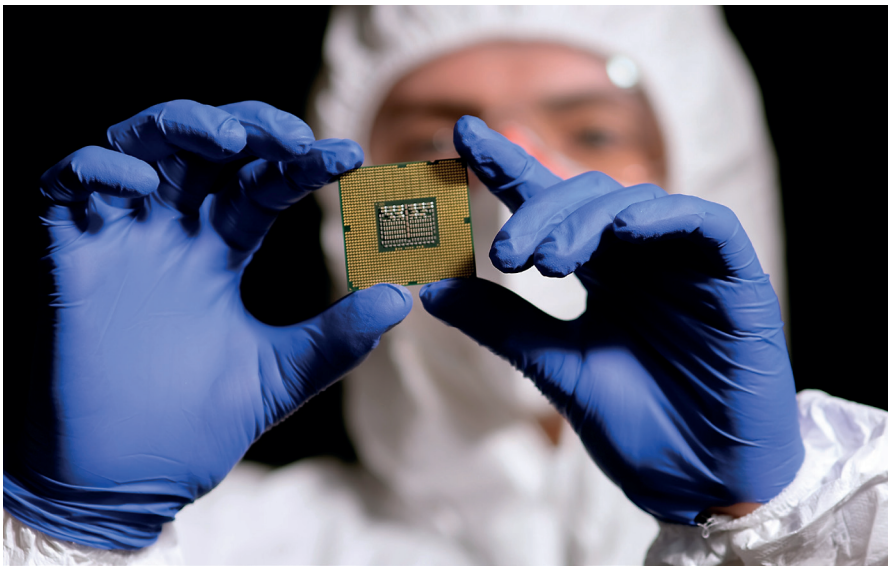
Meanwhile, the EU also intends to become a significant player through the European Chips Act. As investments shift from APAC to North America and Europe, manufacturers must be ready to offer low-carbon services to stand out from their competitors.

The three-step plan for resilience and sustainability

Determining an environmental baseline is a 'must' when decarbonizing the chip industry. At Schneider Electric, we've identified three key steps that help semiconductor organizations of all types and sizes to turn sustainable, net-zero ambitions into action. The first step, called 'Strategize', involves measuring a manufacturer's current energy performance and carbon footprint, and then crafting a net-zero plan that delivers tangible results. In reality, this involves establishing a baseline for carbon emissions, examining digital technologies to identify gaps and inform future roadmaps, assessing technical and economic feasibility to prioritize actions, and modelling building retrofit scenarios to develop a roadmap and timeline. The use of electrical digital twins when designing and simulating new FABS power systems in particular will improve their designs and optimise the network to meet local requirements and standards.

The second step is 'Digitize'. This means creating a digital hub that can monitor and visualize a semiconductor organization's energy and resource usage, enabling leaders to make data-driven sustainability decisions and report on progress towards set goals. This single source of truth aids in the tracking of embedded carbon, including building information modelling, as well as the measurement of energy and carbon, including centralizing energy supply and utility data and implementing cloud-based, AI-powered analysis.

Finally, the third step is 'Decarbonize'. This is where the true action takes place, in which semiconductor manufacturers must leverage insights from their Strategize and Decarbonize steps to make genuine sustainability improvements. Exact upgrades will depend on their findings, but examples include the electrification of fleet vehicles, the installation of renewable energy generators, the purchase of low or no-carbon products, and the use of AI to optimize on-site energy consumption in real-time.



Collaborating with dependable advisors and specialised partners

Alongside the three-step Strategize, Digitize, Decarbonize process, collaboration and partnerships are pivotal to achieving sustainability success in the semiconductor industry. With long-term sustainability requiring disparate areas of specialization and support, manufacturers must realize that no single company can accomplish it alone. Instead, semiconductor producers and vendors must work together and leverage external expertise and technology.

Schneider Electric has long been instrumental in assisting semiconductor companies in addressing sustainability and decarbonization challenges. For example, it recently partnered with Intel, one of the world's leading semiconductor design and manufacturing companies, and Applied Materials, Inc., the world's largest semiconductor and display equipment company, to launch Catalyze: a new partnership program aimed at accelerating access to renewable energy across the global semiconductor value chain. With the assistance of the Catalyze program, semiconductor leaders will be able to achieve a number of sustainability and resilience goals, including:

- Combine energy purchasing power across the semiconductor value chain to accelerate the deployment of renewable energy projects
- Participate in the market for utility-scale power purchase agreements (PPAs)
- Develop operational models to be used in supply chain programs to close net-zero ambition gaps
- Increase awareness of the availability of renewable energy in specific global regions where the semiconductor value chain is operational
- Lead the way for the industry to drive definitive next steps

Sustainable power in the manufacturing of semiconductors

Ultimately, embracing sustainability measures not only aligns with global environmental goals, but also makes sense for semiconductor fabrication plants' bottom lines.

Studies indicate that implementing sustainability strategies can reduce costs and positively impact operating profit by up to 60%. Moreover, adopting sustainability practices mitigates long-term risks and opens opportunities in new markets. Now that we've seemingly progressed from the semiconductor crisis , manufacturers have potential for enormous growth through long-term improvements. They can produce large savings as well as unlock enormous untouched energy efficiency possibilities. And the best part? The tools to achieve this are right in front of us.

With the help of a knowledgeable network of partners, organisations must learn to decarbonize, digitize, and strategize today.

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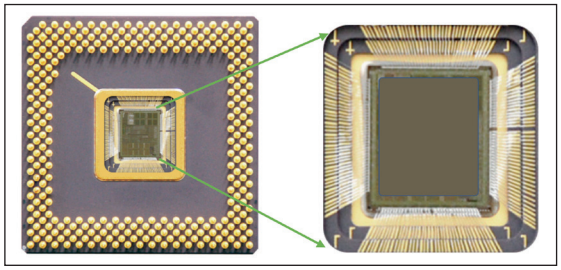
Effective hermetic sealing for next-generation microelectronic packaging

A perfectly sealed electronic package can fulfill its intended function without disruption, error or a significant reduction in performance for decades. However, design and field engineers can only achieve this level of performance by applying the right materials and sealants, and employing the correct tools, equipment and process steps to build semiconductor-driven electronic packages for the next generation. The confidence engendered by a well-sealed package inevitably leads to the development of better chips with more features.

BY RAMESH KOTHANDAPANI, TECHNICAL DIRECTOR, MICROELECTRONIC PACKAGING, MATERION CORPORATION

HERMETIC SEALING is an important process for packaging semiconductor chips. The word "hermetic," in this case, suggests leak-safe sealing. A semiconductor chip goes through several process steps, starting as a wafer before being cut into individual chips and eventually ending up in a discrete package. Such chips are strongly bonded to die pads with a die-attach epoxy or eutectic solders. They are then electrically connected to the ceramic package bond pads with very fine wires.

The ceramic package – in effect a "chip carrier" – is generally multi-layered with electrical feedthroughs within its ceramic body. These layers are internally connected to the bottom or sides of the package to be mounted onto printed circuit boards along with other electrical components. An array of packages is available for chip bonding, including leaded chip carrier (LCC); ceramic, quad, flatpack (CQFP), and quad-flat package (QFP), among others.



➤ The ceramic package with semiconductor chip attached via bonding materials. The image on the right shows the fine wire bonds to the bond pads. Each bond pad is internally connected to the pins surrounding the package.

The ceramic package containing the chip with wire bonds must eventually be hermetically sealed to prevent the entry of contaminants such as moisture or loose particles.

The hermetic sealing process is vital to determining the viability of the assembly in operation. Illustration 1 shows the semiconductor chip and its hundreds of very fine wire bonds. These chips range in size from a few millimeters to tens of millimeters. Smaller chips may have fewer wire bonds, while larger chips can have hundreds. These bonds are thinner than a human hair, with diameters as small as 0.0007 inch (17.78 microns).

Discrete chips contain micro-electromechanical systems (MEMS) with super-fine gears, clocks and moving actuators that cannot be seen with the naked eye. Any particles that deposit on these chips are likely to interfere with their performance. Equally, with the bonded fine wires so close to each other, conductive particles or moisture between the wires could cause a malfunction. This makes proper hermetic sealing of the assembled packages even more important.

Before focusing on the sealing process, it's important to know about materials which are used for sealings, its limitations, the design guidelines, storage, and handling processes.

There are, for example, several types of ceramic packages:

- Surface mount ceramic packages
- Ceramic pin grid array packages
- Ceramic quad flat packages
- Ceramic hybrid packages
- Fiber-optic communication packages
- The bonding materials or solders
- The components which have to be attached to the package such as dies, die attach materials, wires and etc.

Depending on the level of hermeticity required, packages undergo one or two sealing processes: seam-sealed with a metal lid, or solder-sealed with a plated metal lid.

SEAM-SEALED WITH METAL LID:
This is a reliable hermetic sealing process in which a pair of round electrodes run around the edge of the lid, melting and fusing it to the package's seal ring area. Seam sealing is useful when:

- The semiconductor chip cannot accept high levels of heat. Seam seal offers localized edge heating.
- The user may not have oven reflow capability.
- The end application is RF-related with a low level of hermeticity required (i.e., RF packaging).

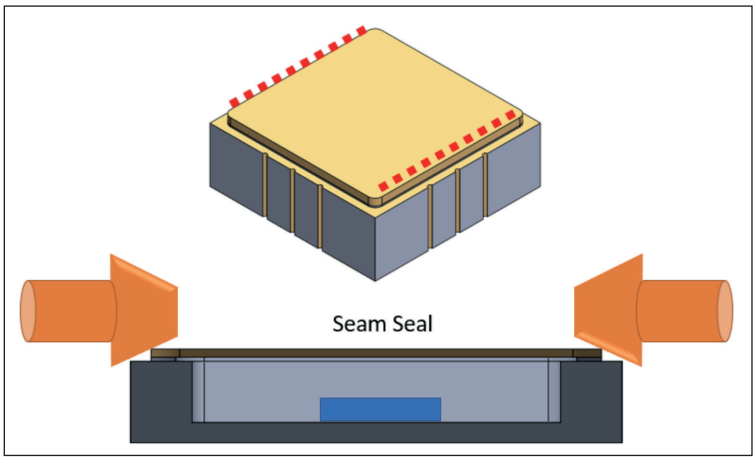
SOLDER-SEALED WITH PLATED METAL LID:
This process can also achieve high levels of reliable, airtight sealing. Several post-seal tests are available to confirm its effectiveness.

Some factors are common to all package types, including the use of die-bond pads, wire bond pads and seal rings. Illustration 3 shows some key features of the ceramic package.

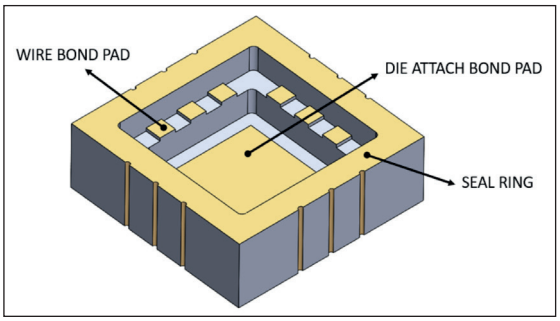
DIE-ATTACH PAD: This is the area where the semiconductor chip is attached with the aid of eutectic solder alloy or epoxy materials. Epoxy-based die-attach adhesives typically comprise a resin and a hardener, which must be well mixed before being applied to the die pad. The chip is then put into place and scrubbed with pressure to initiate wetting and release any trapped gasses in the bonding materials. The assembly is cured at high temperatures to harden it, a potentially tricky process that must be properly controlled.

Both 88Au12Ge and 80Au20Sn can be used as eutectic bonding materials. They melt at 361°C and 280°C, respectively. After considering the heat loss into the fixtures and other components, the set temperature is usually higher. Both types of eutectic solders are pure alloys without any binders or bonding agents.

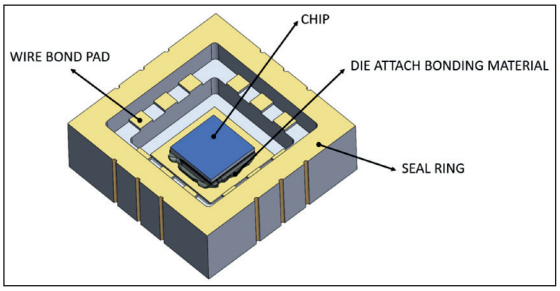
The selection of the die-attachment bonding material is subject to the coefficient of thermal expansion (CTE) of the chip and other neighboring materials with which the bonding agent may come



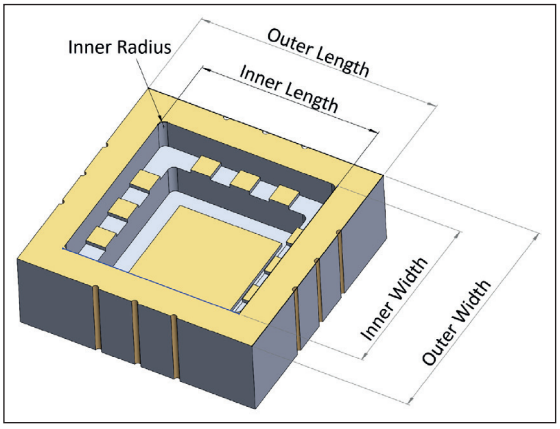
➤ The ceramic package is seam-sealed with two electrodes running parallel to melt the lid and seal it to the ceramic or metal package.



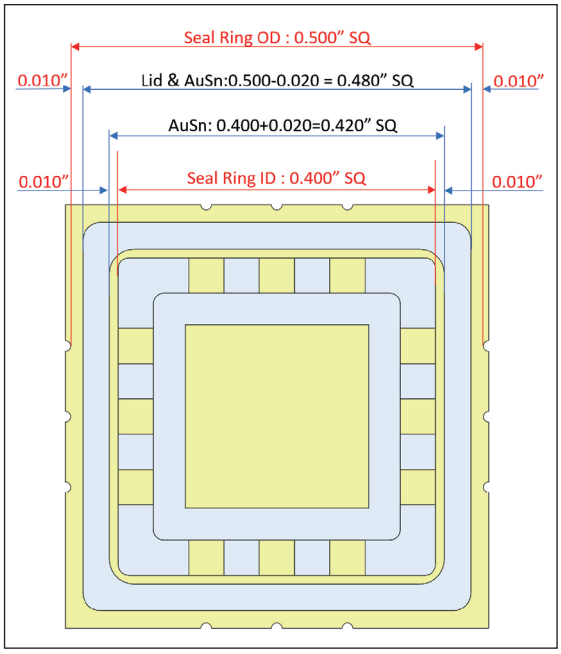
➤ The ceramic package with seal ring and wire and die-bond pads.



➤ The ceramic package with chip attachment.



➤ Ceramic package with seal ring dimensions.



➤ Design guidelines for package lid and solder.

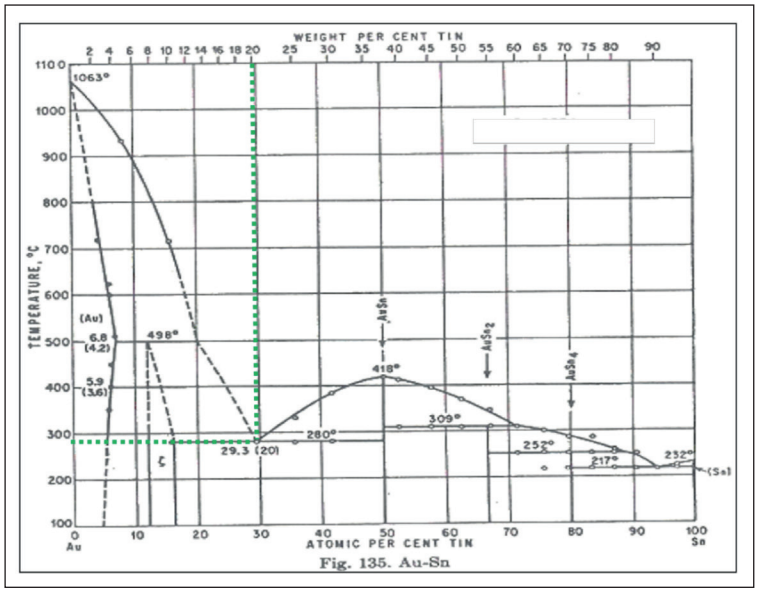
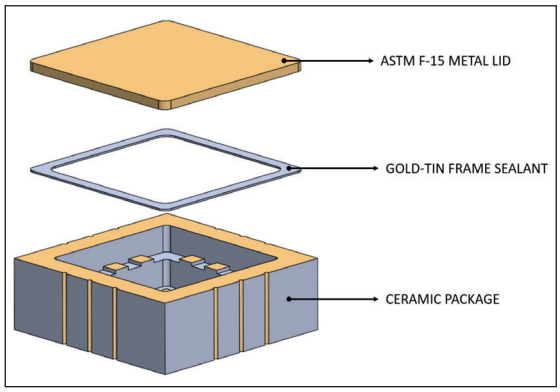


Fig. 135. Au-Sn

➤ Gold-Tin phase diagram.



➤ Exploded view of ceramic package, solder frame and plated metal lid.

into contact. Melting and curing temperatures and conditions must also be determined.

CHIP ATTACH POST-SEAL CONDITIONS:

It is important to validate secure bonding and ensure the release of trapped gasses. Suppliers will generally provide curing instructions and process steps to remove organics and binders. Otherwise, hydrogen-saturated hydrocarbons or moisture could release during the solder hermetic sealing process. Trapped gases within the package will negatively affect its overall electrical performance and lifespan.

Consequently, a well-controlled die-attach process is important for achieving void-free bonding. Unfortunately, post-seal validation can be costly and may produce irregular or misleading results. Close attention must be paid, then, to storage conditions, expiry date, mixing ratio, duration of use, and volume required per unit per shift. There is also the looming possibility of moisture absorbed from the environment.

SEAL RING:

This is one of the most important components in the ceramic package when it comes to hermetic sealing. As is the case with die and wire bond pads, nearly the full surface of the seal ring is used in the soldering process. The seal ring surface is generally porous and plated with nickel and gold, which could lead to nickel migration to the seal ring at elevated temperatures. This in turn may result in pin holes and solder voids. Thus, careful handling and temperature control are essential.

Effective hermetic sealing: Step-by-step

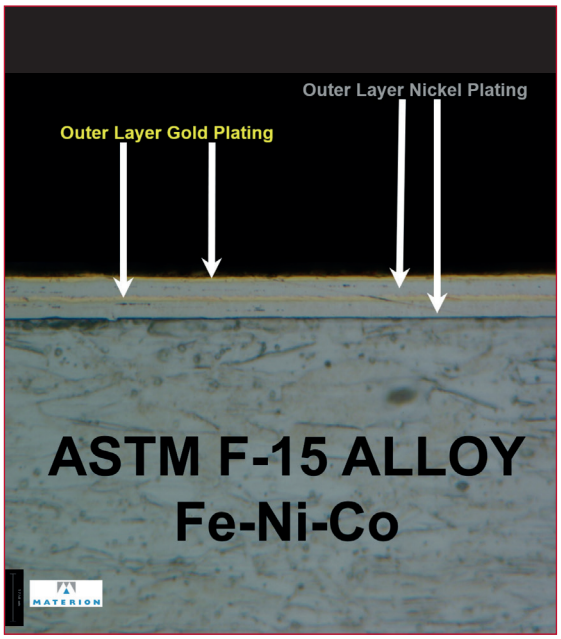
Successful hermetic sealing is dependent upon several factors, including:

- Design guidelines for the package seal ring
- Sealant and lid material selection
- Sealing methods and process controls
- Post-hermetic sealing tests and troubleshooting
- Next-generation packaging material options

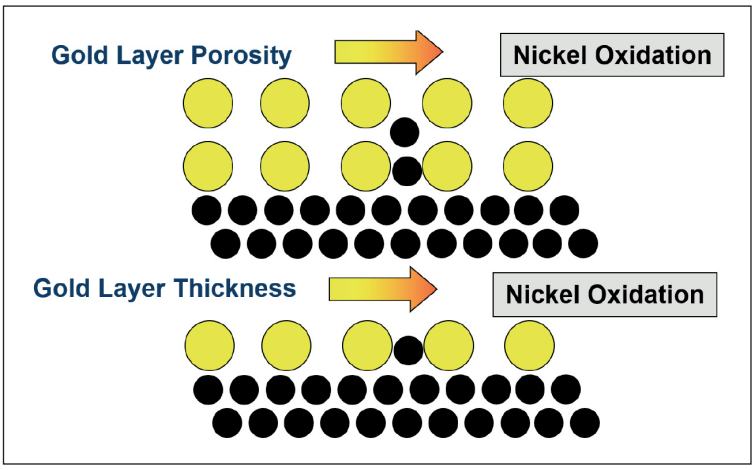
DESIGN GUIDELINES OF THE PACKAGE SEAL RING:

Consider the size of the hermetic cover lid and its solder. The outer seal ring, the metal lid, and the gold-tin frame are key design elements. For example, if the package seal ring outer length and width is 0.500” square, the lid should 0.500 inch - 0.010” - 0.010”, or 0.480” square.

Next is to determine the gold-tin solder inner dimensions. For this, both inner and outer dimensions must be considered. If the seal ring inner dimensions are 0.400” square, then the gold-tin solder inner dimensions should be 0.400” + 0.010” + 0.010”, or 0.420” square. The inner and outer radii are also important for the overall design, as is the thickness of the solder and lid. These dimensions will be based upon the size of the final package.

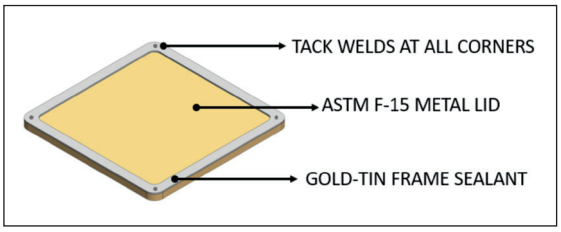


➤ Cross section image of four layers plated sequentially with nickel and gold.



➤ Nickel migration process.

The 0.010” clearance relies on the availability of space for the seal ring. It can be as low as 0.002” for the outer gap, and almost as low for the inner seal ring if the ring is narrow.

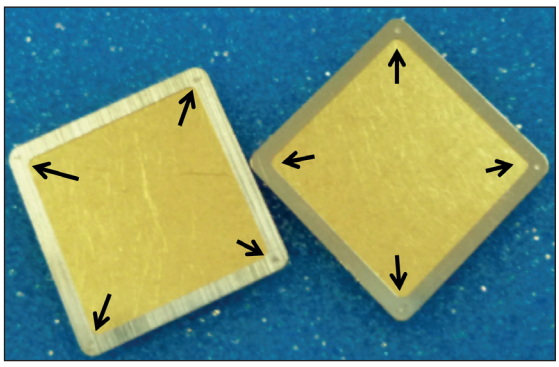


➤ Frame lid assembly.

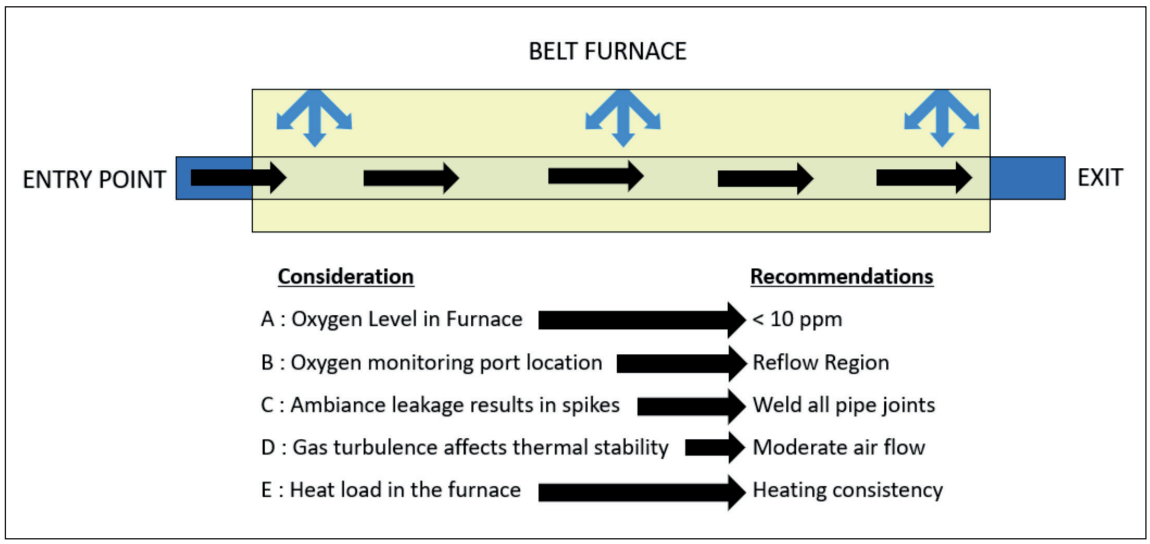
SEALANT MATERIAL SELECTION:

There is a variety of suitable solder alloys and eutectic solders for leak-safe hermetic joints. Gold-tin has been proven particularly effective for bonding metal lids to ceramic or metal packages. The 80% gold/20% tin solder melts at 280°C and holds up well when subjected to temperature cycle testing.

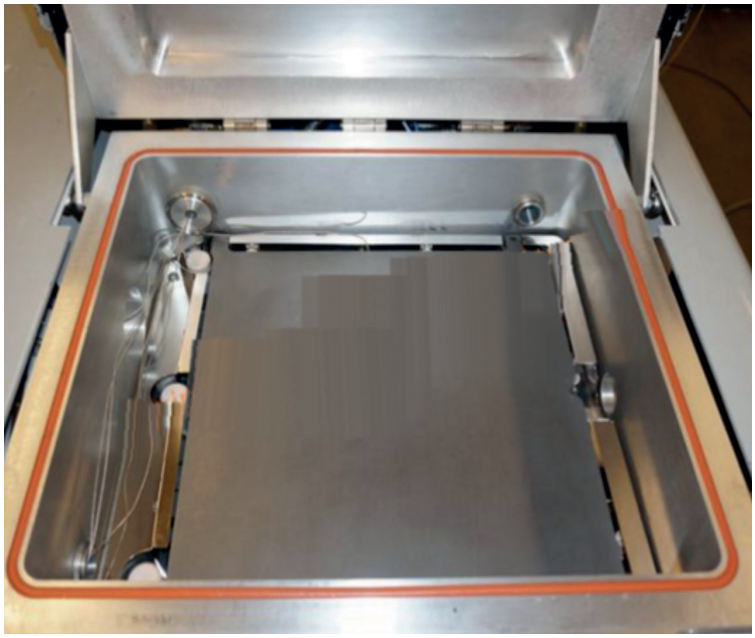
The 80% gold/20% tin alloy must be manufactured with very few impurities and must be within its nominal weight percentage to achieve a good bond.



➤ Tack weld points at corners.



➤ Critical parameter controls and recommendations for effective hermetic sealing using a belt furnace.



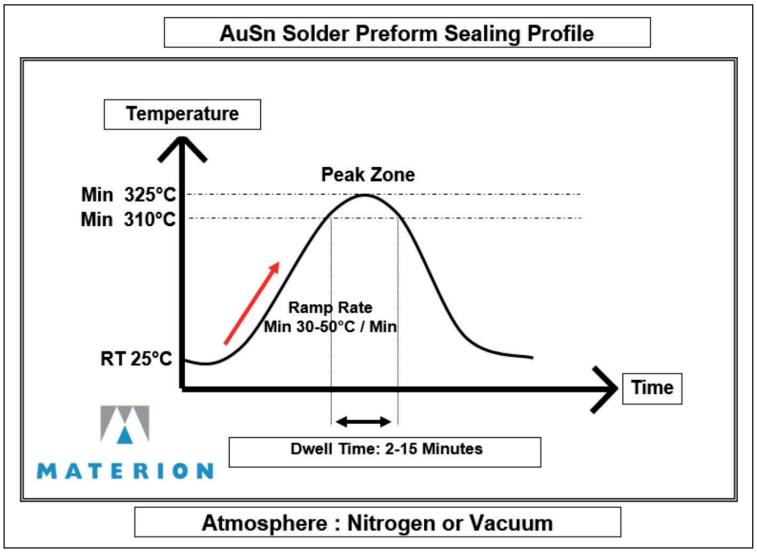
Vacuum furnace inner chamber.

- **Gold-tin purity:** Decrease in heat conductivity
- **Gold-tin contamination:** Oxides, organics
- **Gold-tin interfacial contact area**

COVER LID MATERIAL SELECTION:

The metal lid is an alloy of iron, nickel and cobalt, also known as ASTM F-15. In order for the gold-tin solder to bond well with the package, the metal lid must be well prepared. A lid composed of more than 50% iron (Fe) elements could oxidize over time. A bare lid will not allow gold-tin solder wetting. Reliable gold plating is therefore essential.

The lid is electroplated with 100 to 350 microinches of nickel, followed by gold at a thickness of 50 microinches. Additional nickel and gold are plated for high-reliability applications, though the sum of both nickel films cannot exceed 450 microinches, while the sum of the gold-plated films must be at least 50 microinches. The idea is to prevent excess build-up at the edges. which could eventually have a negative effect on the hermetic seal. The following illustration shows a cross-section of the four-layer plated lid.



Gold-tin reflow profile.

EFFECTIVE PLATING:

The plating process is extremely critical. Edge build-up, for example, must be avoided. The electroplate bath and chemistry maintenance are both important. It should be noted that this plating is not cosmetic in nature, but is rather designed for high-quality hermetic sealing, which also entails good solder bonding. Poor maintenance plating could trap unwanted gases.

Post-plate tests are available to check the quality of the plating, particularly to quantify hydrogen content in the plated films.

Plating bath maintenance and bath chemistry checks should be performed periodically for preventative reasons. Post-plate bakeouts are also sometimes performed following last-stage plating at lower temperatures (between 120°C to 150°C) for 8 to 12 hours.

High-temperature bakeouts for longer durations could cause the inner layer of nickel to migrate to the gold layer and interfere with solder wetting. The gold-tin solder alloy will not wet with nickel. Nickel migration may also occur if the plated layer is too thin or demonstrates high porosity on the plated surface.

Sealing methods and process controls

- **Tack Welding or Spot Welding:** The gold-tin solder must be attached to the plated lid by spot or tack welding. This process is crucial to avoiding misalignment and other defects that could eventually affect seal yield. It also creates additional benefits for end users who must assemble the frame and lid as a single component before final sealing. Tack welding requires very small portions of the eutectic gold-tin solder at all four corners to melt and adhere to the plated lid.

- **Reflow equipment and process controls:** It's important to select the proper reflow equipment prior to sealing. Hermetic sealing with gold-tin or other solders requires an inert environment; otherwise, oxidation might affect the integrity of the seal. If a belt furnace is used, the maintenance and seal profiles must be well monitored. Oxygen content within the reflow chamber should be tracked and controlled. Similar monitoring is required if a vacuum seal furnace is chosen, with the additional benefit of removing unwanted gasses. In both cases, equipment performance will ultimately determine the quality of the hermetic seal.

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- **Fast processes**
  through high process temperature of up to 170°C
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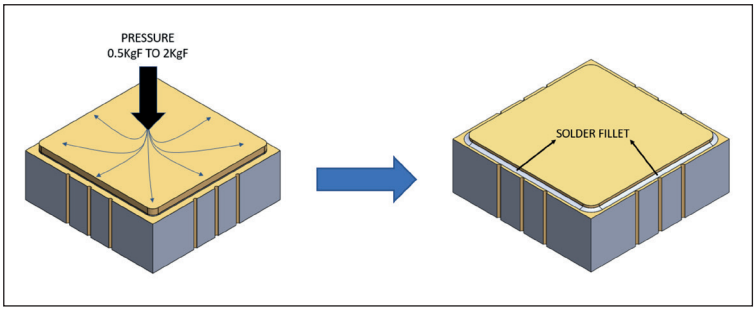


➤ llustration 16: Left, assembly with pressure applied. Right, post-seal with solder fillet.

- **The gold-tin seal profile:** Following are key considerations for the gold-tin seal profile:

- **Rise rate:** The rise rate must be gradual and slow. This helps to release gasses from the various components without promoting nickel migration. Such migration may result from a quicker ramp-up, especially with porous-plated layers. Vacuum furnaces will evacuate any outgasses, while a belt furnace with nitrogen pressure should do the same.

- **Peak temperature:** Eutectic gold-tin solder melting temperature is 280°C. In addition to the sealing components, fixtures, clips and other materials can also pull in heat. Once the solder and lid reach peak temperature, the goal should be the complete removal of gases, complete solder flowing, solder fillet formation, and the elimination of pin holes or void removal. Duration of exposure to peak temperature is very subjective and depends on product size, ssembly tools and conditions. Reducing this duration while critical processes are in progress can uncover failure modes, which can be observed visually, through leak tests or under X-ray.
- **Ramp down from peak zone:** Product cooling must also be done gradually, as sudden cooling or ejection of the product from the oven can be quite harmful.

- Adequate pressure should be applied to gold-tin solder to achieve a good hermetic joint. Interestingly, though, only about 0.5 to 4 kilogram-force is required. In all cases the pressure is transferred from the lid down to the gold-tin sealant (see Illustration 16). As mentioned, this pressure is very helpful during the peak temperature phase to press the lids and squeeze out molten solder to form a fillet.

SEAL CLIPS:

There are many different types of readily procurable clips. Depending on the type of package and production volume, pressure clips can be customized and fabricated. The aligning fixture should also be considered if increased production volume is desired.

POST-SEAL RELIABILITY TEST:

Post-seal reliability tests validate process and material selection. Several different levels of tests are performed one after another. Details of all listed tests can be found in standard Mil-883 guidebooks.

NEXT-GENERAL PACKAGING MATERIAL OPTIONS:

These tests are intended to confirm successful hermetic sealing. Similarly, an effective packaging process can significantly prolong the life of the package in field.

Many applications, such as a board-level module installed in a satellite or space vehicle, are not reachable for replacement or repair. Thus, they are made to last even in the most adverse conditions.

A variety of new materials and processes are coming into the market. For next-generation hermetic sealing applications, for example, a range of innovative cover lids are now available. These include hermetic covers or Visi-Lids for optical communications, non-magnetic Combo Lids for electromagnetic nose controls, and Getter Combo Lids to contain the release of hydrogen from the package.

No	Reliability Tests	Purpose
1	Gross leak test or die penetrate test	Hermeticity, identify leaks
2	Fine leak test (with helium bombing)	Hermeticity, identify leaks
3	Optical leak test	Hermeticity, identify leaks (mass scale)
4	Krypton leak test	Hermeticity, Identify leaks (quicker than helium)
5	Electrical test	Assembled unit performance
6	Temperature cycle test	Accelerated test for field performance
7	X-ray imaging	Solder joint integrity
8	Salt Atmospheric Test (SAT)	Accelerated test for field performance
9	PIND Test	Sealed unit internal particle identification
10	Visual inspection	Visual assurance of sealed unit, solder flow, etc.

➤ Various reliability tests.

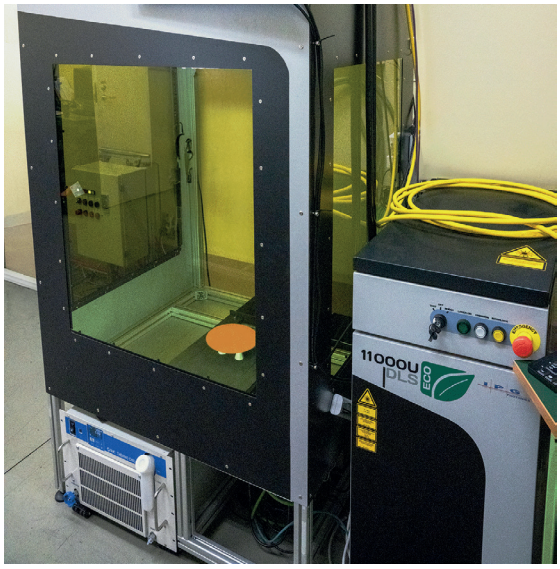
Lasers: a sustainable wafer heating solution

Lasers, in particular diode lasers, are an attractive and sustainable option for future chipmaking needs.

BY IURII MARKUSHOV, KAZUNARI MIYATA AND HARLON O. NEUMANN AND TOBY STRITE, IPG PHOTONICS CORPORATION

THE JOURNEY to a sustainable fab requires closer examination of how silicon wafers are heated during chip making. Elevated wafer temperature is required for annealing, epitaxial and etch processes. A sustainable heating solution must minimize energy consumption and consumables, while providing excellent temperature uniformity and competitive thermal rise time. Heating by infrared laser has proven itself in other industries to be just such a silver bullet. Here we describe heating experiments on a 200 mm silicon wafer utilizing a commercially available 975 nm diode laser. An empirical thermal model enables extrapolation to 300 mm wafer heating scenarios. The experimental and theoretical findings coupled with the mature state of diode laser technology suggest that heating silicon wafers by laser is an attractive path forward.

Our experimental apparatus (Figure 1) projects an 11kW near infrared (975 nm) diode laser over a thermally isolated 200 mm polished silicon wafer in regular atmosphere. The projection optics uniformly illuminate a ~213 mm square fully covering the wafer surface with minimal energy overspill onto the heatsink beneath. Wafer temperature is measured using a Chino model IP-CZP0JL pyrometer



➤ Figure 1. Experimental configuration showing the 11kW laser (right) and experimental chamber (left)

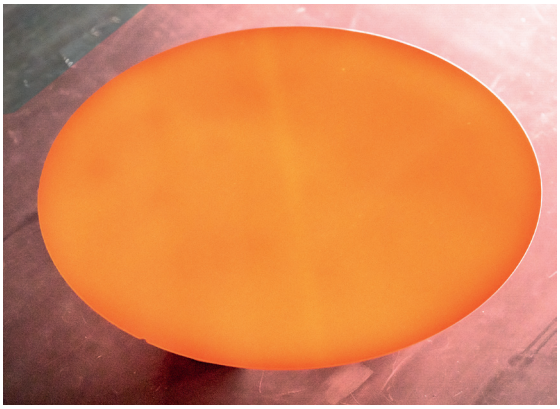
positioned about one meter above the wafer. Our experiments operate the laser at constant output power until steady state temperature is reached. After laser power is shut off, the cooling curve is also recorded.

Maximum available 11 kW laser power heats the wafer quickly. Our experiment achieves 800°C in below 9 seconds. Steady state laser power of ~8.1 kW is sufficient to maintain that temperature. Figure 2 shows the heated wafer at 800°C. The color attests to the uniform nature of the laser heating across the wafer diameter.

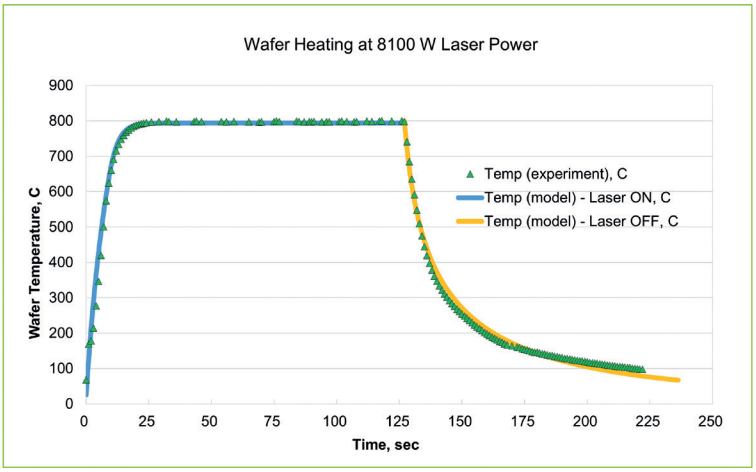
Data were collected at six laser settings ranging from 0.86 kW to 8.1 kW constant power, enabling us to develop an empirical model covering a wide range of energy input, temperature and wafer diameters. The thermodynamic model incorporates absorptive heating from the laser, the wafer's radiative and convective losses, and the heat capacity of silicon, each as a function of temperature.

Figure 3 shows an example of fitting curves (blue – heating rise and steady-state and yellow - cooling) which accurately match experimental observations at 8.1 kW laser power. Similarly excellent fits were generated at the five other settings to create our temperature dependent empirical model.

Discussions with prospective customers suggest both the short rise times and low steady state power requirements demonstrated by the laser heater are highly attractive compared with infrared lamp alternatives. Fast rise times increase tool throughput. These are possible because up to 80% of the laser optical energy is absorbed by the silicon wafer. Low overall power requirements are a byproduct of the strong absorption, along with the high directivity of laser, meaning little energy is wasted heating the chamber atmosphere or enclosure. In contrast, infrared lamps operate hot, emit energy in all directions, and produce significant energy output at longer wavelengths where silicon is not highly absorbing.



➤ Figure 2. Visible light image of 200 mm silicon wafer heated to 800°C by laser. Click here to view a video clip



➤ Figure 3. Experimental (triangles) and modeled (blue and yellow) curves for 200 mm wafer heated by 8.1 kW of laser power

Figure 4 shows the calculated laser requirements to heat 300 mm silicon wafers to a variety of temperatures. The calculated values are modeled using a regular hexagonal illumination pattern such that 91.5% of the laser output hits the wafer surface. The first column provides the laser power required to heat the wafer to target temperature within a 10 second rise time constraint. Less power is required to hold a 300 mm wafer at the target temperature. The range of values required for steady state is given in the second column. The empirical model incorporates a temperature dependent absorption coefficient for silicon to match experimental data. At 400°C, we observe 62% of the laser energy is absorbed by the wafer, while at 800°C the absorbed percentage rises to 80%.

Commercially available diode lasers, such as the DLS-ECO series from IPG Photonics Corporation, are attractive options for the sustainable wafer fab. Silicon is absorptive at 975 nm, so up to 80% of the laser optical energy contributes to wafer heating. A diode laser converts 55+% of electrical power input to usable optical energy. Laser output is homogenized for uniform energy distribution, while its shape is tailored to match the wafer dimensions. Little energy is wasted heating the susceptor, chamber atmosphere or enclosure.

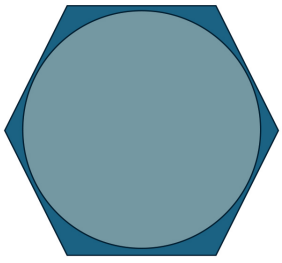
High component redundancy ensures diode lasers provide uninterrupted, service-free operation over seven years without any consumables. Fiber delivery cables 15 meters or longer enable laser light to be conveniently delivered to the tool, while all heat dissipation and electrical utilities remain outside the clean room. Because the laser operates at a single mid-infrared wavelength, pyrometry is effective in the absence of heater source interference.

While a laser is a higher up-front capital investment when compared to incumbent infrared lamp or inductive heaters, the premium is recoverable through reduced operational expense when we consider the unique combination of reliable, maintenance and consumable-free operation, low energy consumption and greenhouse gas footprint, along with the possibility to manage waste heat outside of the cleanroom. Lasers, in particular diode lasers, are an attractive and sustainable option for future chipmaking needs.

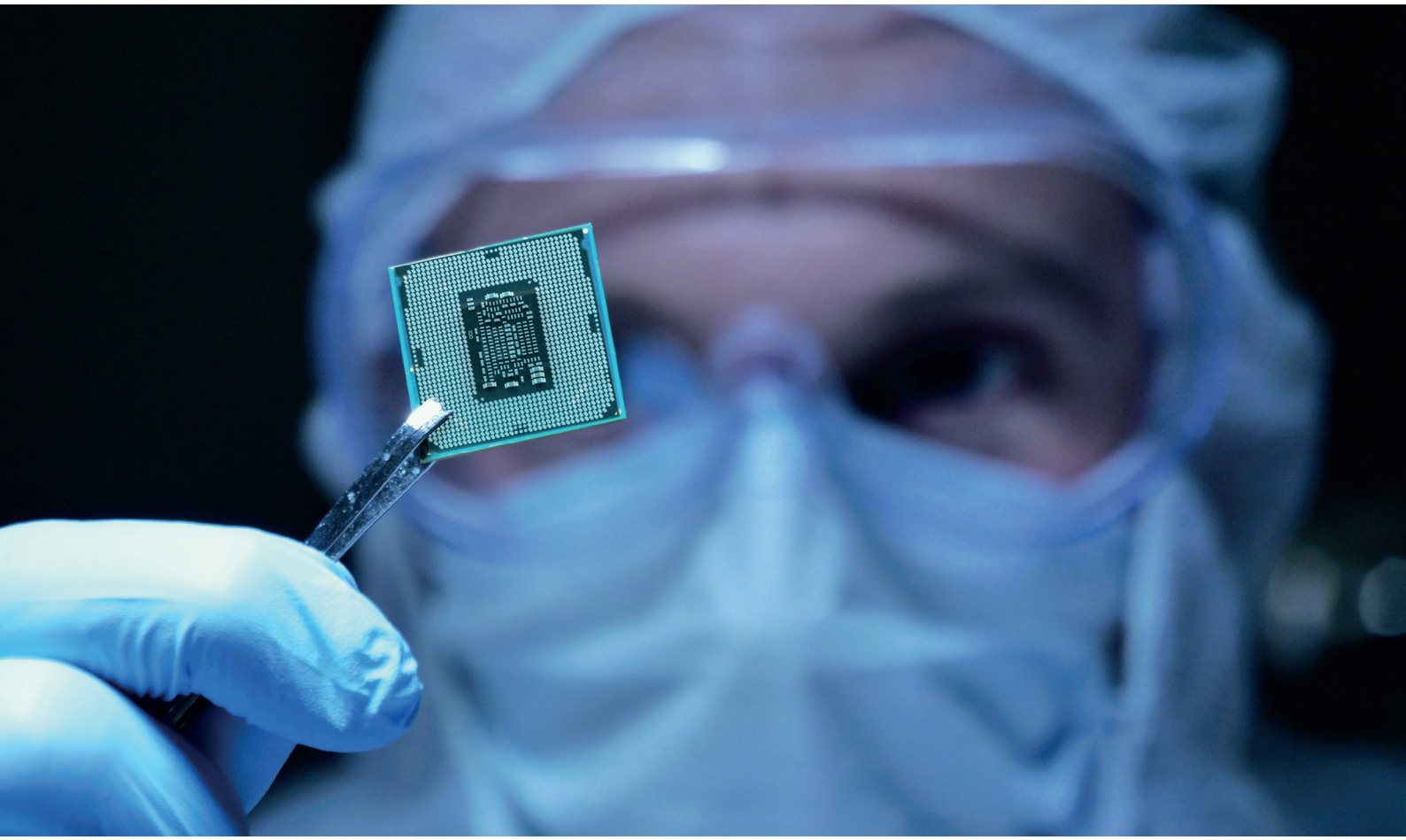
➤ Figure 5. DLS-ECO heating lasers are commercially available at power levels ranging from a few kilowatts to 100 kilowatts

300mm Silicon Wafer Heating

	Laser Power, Watts (10sec Ramp Time)	Laser Power, Watts (Equilibrium)	Effective Absorption
400°C	7,300	2,662	62%
500°C	9,800	4,371	67%
600°C	12,500	6,400	75%
800°C	18,800	13,883	80%



➤ Figure 4. Table calculating laser power requirements to reach target temperature in ten seconds, and maintain the target temperature. We model a hexagonal laser illumination pattern (dark) which overspills only 8.5% of laser energy off the 300m diameter wafer edge.



Chip, Chip, Hooray!

Addressing connected semiconductor and chip growing pains

In almost every industry, a connected tech revolution is underway. The rise of the Internet of Things (IoT), artificial intelligence (AI), and 5G has ushered in an era of unprecedented connectivity and automation. Yet, with this wave of progress comes a great demand for those unassuming pieces of silicon that are needed to power this new era of connectivity: semiconductors.

BY MICHAEL CANTOR, CIO, PARK PLACE TECHNOLOGIES

MICROCHIPS are not mere components, but the bedrock of innovation and infrastructure. And businesses of all sizes are facing a critical juncture, where managing the surge in chip need is essential for growth.

The memory of the 2020 shortage is still fresh in the minds of businesses and governments alike, making semiconductor production a lightning rod for strategic investment in Europe and the UK. In a declaration of intent, the UK and the EU have both announced ambitious plans to boost their semiconductor industries. The UK is set to spend £100m in the global race to produce AI chips, alongside the already £1 billion committed to the sector, and the EU has passed the EU Chip Act. These initiatives are a recognition of the importance of semiconductors to the global economy. Businesses based in countries that are not prepared for the new strategies and challenges could face significant disruptions. They could be forced to delay or cancel product launches, lose market share, or even go out of business. Luckily, there

are opportunities to mitigate these impacts, from creating chips in-house to supercharging a circular economy.

Combatting a chip squeeze

Diversification emerges as a practical strategy, involving the sourcing of components from various geographic locations and suppliers. Collaborative efforts across governments and industries can enhance resilience by nurturing a diverse pool of talent and expertise, in turn reducing reliance on a single source.

There are several routes to diversification. These include changing their chip suppliers, investing in chip inventory, developing contingency plans in case of supply disruptions and investing in research and development to create new chipless technologies.

One of the fascinating developments in the realm of chipless technologies is Radio-Frequency Identification (RFID). RFID is a wireless communication technology that allows for the identification and tracking of objects using electromagnetic fields. Unlike traditional silicon-based chips, RFID does not require an integrated circuit (chip) and instead relies on Antennae, a printed or etched conductive material. Already, RFID is crucial in manufacturing by enabling real-time visibility and automation of critical processes, from production to inventory management. Today's consumers are more demanding than ever, and often, only advanced RFID solutions allow businesses to meet these heightened expectations.

The development of such chipless technologies demonstrates how innovation can lead to more efficient, cost-effective, and versatile solutions that address a variety of business and societal needs.

Taking matters into their own hands

Although hard to imagine, it's true that the world's most important advanced technology today – AI chips – are nearly all created by NVIDIA and produced by a single company. The Taiwan Semiconductor Manufacturing Company (TSMC) makes all the chips that enable modern AI.

However, the trillion-dollar semiconductor supply chain and rapid advances in AI has brought businesses to a crisis point. Today, adapting to the evolving semiconductor landscape demands more than reactive planning. Many larger businesses are now looking to create their own supplies of semiconductors.

For example, in a bid to capitalise on emerging technologies and reduce reliance on NVIDIA, AWS is now developing two types of microchips that will be used to train and run AI models. And Microsoft is doing the same, designing an AI chip code-named "Athena" to power the technology behind AI chatbots.

Taking matters in-house will enable many enterprise-level technology firms to meet the demand of their customers by more effectively responding to market demands without the complications of international supply chains, and accelerate innovation by collaborating even more closely with research teams and having easier access to cutting-edge technology. This can be particularly advantageous for industries dependent on rapid technological advancements, such as electronics and automotive.

Seizing a circular economy

A circular economy mindset will also be key when it comes to semiconductors, as many precious metals and minerals that are needed to create new chips are hidden away in back drawers or piles of e-waste. This mindset transcends the traditional linear "take-make-dispose" model of production and consumption, aiming to reduce waste, conserve resources, and enhance supply chain sustainability. This is especially important as the UK generated the second largest amount of e-waste as a country in 2022, and this is a mounting issue with the UK set to be the worst country in 2024 unless action is taken immediately.

Elements like gold, silver, and copper, which are present in semiconductors, can be recovered through responsible recycling processes. This not only conserves precious resources but also reduces the environmental impact associated with mining and manufacturing these materials.

A circular mindset also encourages a shift toward designing semiconductors with sustainability in mind. This involves optimising chip designs for recyclability, ease of disassembly, and reducing hazardous materials. By adhering to principles of eco-design, businesses can create chips that are not only high-performing but also environmentally responsible.

Circular semiconductor management thrives on collaboration between businesses, consumers, and recycling facilities. Establishing closed-loop systems, where used chips are collected, refurbished, and reintroduced into the supply chain, can minimise waste and promote resource efficiency. By involving various stakeholders, including manufacturers, suppliers, and end-users, a closed-loop approach fosters a holistic and sustainable semiconductor ecosystem.

Ultimately, chips represent a journey towards a future where innovation and pragmatism converge to reshape industries, redefine connectivity, and carve a path towards a smarter, more interconnected world. As Europe stands on the cusp of this new chapter, businesses that harness innovation with a circular mindset, while ensuring resilient supply chains will be key in shaping a future where innovation and adaptability coexist.

Wafer-level integration changes of ALD for 2D materials

Meeting the challenges of advanced process development for the integration of ALD grown two-dimensional (2D) materials at wafer level.

BY FRIEDRICH WITEK, SENIOR MANAGER SENTECH INSTRUMENTS

THE “Research Laboratory Microelectronics Bochum for 2D Electronic Systems” (ForLab PICT2DES) project aims at attaining high-level applications in microelectronics and microsystems technology at a wafer level. The unique optical, thermal, and mechanical properties that exist in two-dimensional (2D) materials such as Transition-metal dichalcogenides (TMDs) have extremely promising applications in the growing areas of micro-technologies including highly-sensitive sensors, ultra-thin logic devices, nanogenerators, electronics, and optoelectronic devices. Although these materials pose some process challenges, the tunability of electrical and optical properties via the layer thickness of the 2D materials has great potential for future use cases. Ruhr-Universität Bochum (RUB) is working to establish a stable and scalable process chain, integrating additive and subtractive technologies with a high yield at a wafer level, that allows a transfer to industrial use. Working with the thinnest, 2D materials in electronics and sensors, 2D materials enable completely new, transparent, flexible, and biocompatible solutions with minimal consumption of resources.

Bridging the gap between research to applications in microelectronics and microsystems technology at a wafer level with molybdenum disulfide (Mos_2) 2d materials

Establishing stable and scalable processes with a high yield at a wafer level using ultra-thin 2D materials creates several process challenges,

- High-quality, large-area monolayer precise growth at low processing temperatures
- Damage-free plasma deposition on 2D materials
- Homogeneous, monolayer precise, low damage, selective etching of 2D materials
- Electrical contacts

One of the key barriers to using 2D materials in an industrial environment is the growth of the material with similar stability, low defect density, and reliability compared to Silicon (Si). From an industrial point of view, avoiding the time and cost-intensive transfer processes of 2D materials is desirable, and therefore creates a demand for a bottom-up approach: direct deposition of high-quality 2D films on the target substrate.

Due to the temperature sensitivity of the substrates, the bottom-up processes developed for 2D flexible electronics should have the lowest processing temperatures available. Thereby, a well-controlled and conformal growth of layer stacks including 2D materials on the wafer is mandatory.

There is a need for dielectric integration with 2D materials for real devices and systems.

The band gap of many 2D materials as well as the transition from a direct to an indirect band

➤ Figure 1

structure depend on the number of layers. Thus, a homogeneous monolayer-precise deposition technology, without affecting the underlying layer is crucial but very challenging.

Since MoS_2 has no chemical bonds on the surface, it cannot bond with metal, leading to a high Schottky barrier and low carrier injection efficiency. MoS_2 has two different stable phases, a metallic 1T phase, and the semiconducting 2H phase, and thus new lateral phase-change contacts can be successfully demonstrated on flakes on a laboratory scale but need to be shown on a wafer scale.

Project requirements

A cost-effective, innovative, monolayer-accurate deposition, etching, and fabrication technology needed to be implemented. The manufacturing processes for flexible microelectronics and ultra-sensitive micro sensors needed to work at low temperatures and be scalable towards a 200 mm wafer technology. Furthermore, the system needed to be compatible with both the Research Fab Microelectronics Germany (FMD) and industrial users.

Meeting the project requirements

The ultra-thin 2D films are sensitive to environmental humidity and oxygen. To avoid degradation during sample transfer there was a requirement for a large cluster tool with direct encapsulation for the growth of the 2D materials, without breaking the vacuum. Due to the aim of scaling up to wafer level, the tool needed to study the performance of mass production techniques, wafer-to-wafer uniformity, homogeneity, and reproducibility, plus monolayer atomic layer deposition (ALD) growth.

Following an open commercial tender process, the cluster tool from SENTECH Instruments (Figure 1) was chosen. This solution provides excellent modules for each process type, plasma enhanced atomic layer etching (PEALE), inductively coupled plasma-enhanced chemical vacuum deposition (ICPECVD), inductively coupled plasma-reactive ion etching (ICP-RIE), and plasma-enhanced atomic layer deposition (PEALD).

For the latter one, a SENTECH True Remote Conductively Coupled Plasma (CCP) Source is used, allowing low-damage deposition of 2D materials. Another key factor is the SENTECH Planar Triple Spiral Antenna (PTSA) ICP source, enabling low-damage processing of 2D materials after their deposition. The individual tools offer port access for all of the plasma diagnostics required by the Chair of Applied Plasma Dynamics and Electrical Engineering (AEPT). The in-situ ALD and atomic layer etching (ALE) monitoring systems allow excellent control of the monolayer deposition and etching of the 2D materials during the entire process. A high level of customisation was required, which the experienced, interdisciplinary SENTECH project team was able to fulfil in conjunction with the transdisciplinary team at RUB.

➤ Figure 2

Process integration using the cluster tool

The process steps,

- Substrate pre-treatment
- High-k dielectric (ALD)
- Second substrate pre-treatment
- Monolayer precise deposition of the 2D material
- Surface passivation and passivation layer, could all be carried out completely under vacuum,resulting in extremely clean surfaces, crucial for proper interfaces within the device. For process steps occurring outside of the vacuum, devices are passivated by a protective encapsulation film and metallisation, so it is possible to avoid a complete degradation of the 2D ultra-thin film.

Key objectives for plasma processing

The key factors needed in the plasma processing were,

- Compatibility with common device materials
- High level of control
- Capable of patterning at high resolution without altering the physical, electronic, and optical properties of the 2D devices, i.e., no-damage processing.

A plasma surface modification, a substrate pre-treatment, a monolayer precise ablation, and only a monolayer precise deposition were required. In all cases, precise control of the plasma properties was mandatory, thus the requirement for the custom plasma diagnostic rings (Figure 2), which were introduced within both the RIE chamber, used for fluorine gasses, and also in the ALE chamber. The rings are removable, which means that they can be replaced with a conventional spacer ring, allowing for a comparison of processes and transfer to any RIE system. They also allow the use of different plasma diagnostic tools, such as a retarding field energy analyser sensor array to determine, ion energies distribution functions and ion flux. Furthermore, optical emission spectroscopy was utilised to get information about the plasma composition.

➤ Figure 3

Supporting the complex cluster tool infrastructure configuration

A great deal of preplanning was required due to the complex and interdisciplinary nature of the project and the integrated cluster tool. All stakeholders worked together, to ensure minimal complications and downtime from delivery, installation, and uptime of the equipment. The configuration of the cluster tool was complex and thus, supporting the infrastructure as a university was a major challenge. The cluster tool required 14 process gas lines, 42 process gas inlets, and around 300 metres of stainless-steel pipework for the gas supply, mainly within the cluster but also for on-site installation, this had to be housed within one room (Figure 3).

The cluster tool and its additional equipment, including gas supply and waste gas management, had to be fully integrated into the safety infrastructure of the cleanroom due to the potentially hazardous nature of Cl-based gases, H_2S, and Silane as well as highly-flammable and toxic ALD precursors. As an extra layer to the project, a waste gas purification plant (a dry bed absorber as a triple column system) needed an additional publication of a call for tenders. This needed to be completed relatively quickly to ensure it met the same timeline as the rest of the machinery.

The customer-specific modifications to the cluster tool took just under a year of interdisciplinary planning discussions between the SENTECH Application Team, Engineering, Technical Service, and experts from RUB. However, due to the scale and complexity of the tool and required infrastructure, the pre-planning proved invaluable in achieving the project goals within the required timescale. Working in close partnership ensured the machine configuration, infrastructure, and the questions concerning the compatibility and implementation of the gas sensor security system with the new equipment were all planned for well in advance.

The integrated cluster tool avoids cross-contamination, undesired doping, and exposure to humid environmental conditions, enabling enhanced film quality. Since March 2022 the tool has been working and initial results are very promising. Future collaborations and adaptations of the system are planned as part of the joint work of the BMBF-funded ForMikro project FlexTMDSense - “Research into a novel, flexible sensor systems based on two-dimensional material systems”. Research subjects include ultra-thin pH and gas sensor systems based on 2D Semiconductor Films from the material class of TMDs.

For further information about the cluster tool and bespoke plasma diagnostic ring, the process sequence, and the initial results for this project, it is possible to request a copy of a full case study. Please visit www.sentech.de and follow the links in the news section on the home page.

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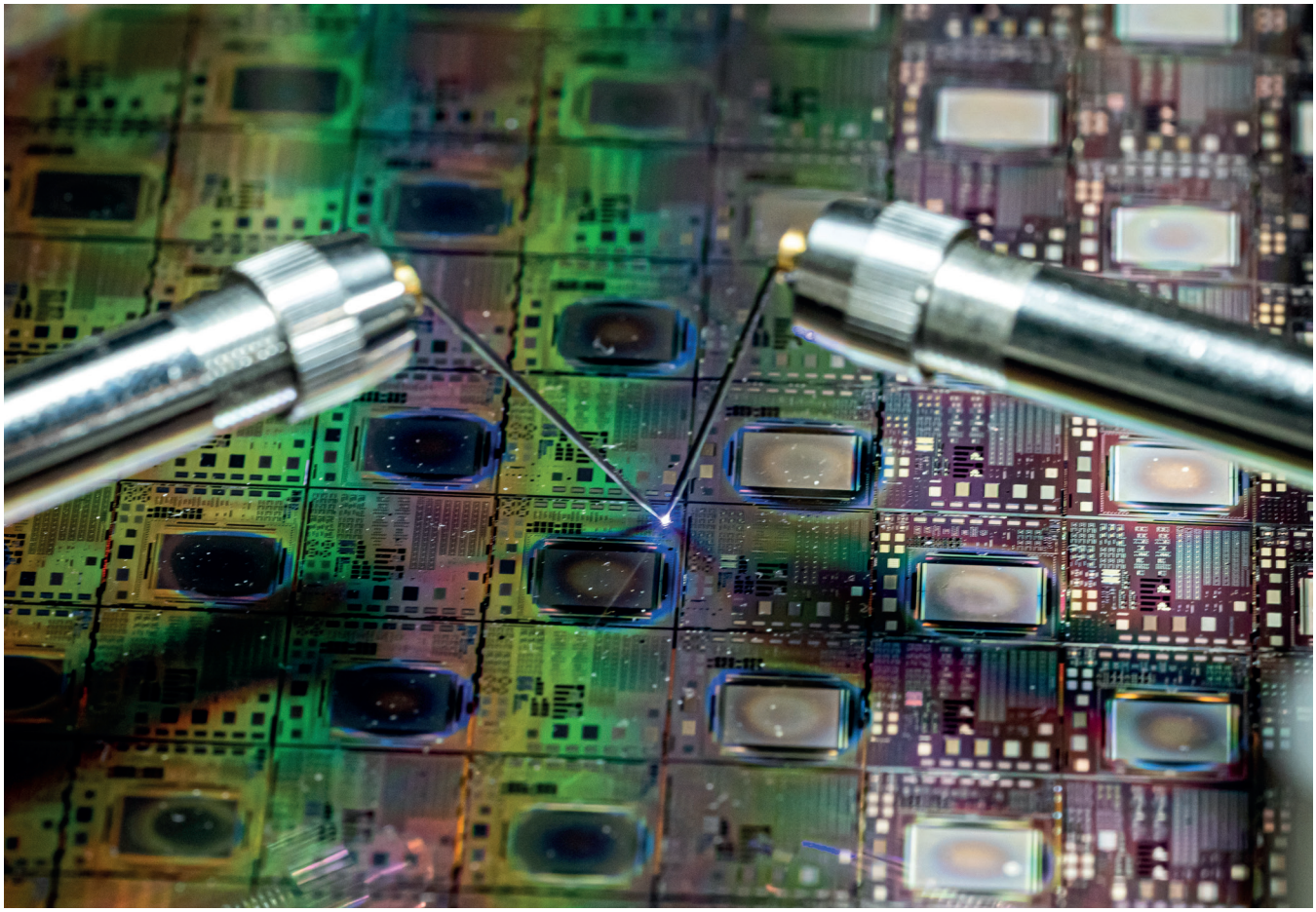
How to integrate silicon and III-Vs

To draw on all the traditional benefits that come from scaling, silicon and the III-Vs must be united via epitaxy and processing in silicon foundries

BY EUGENE FITZGERALD, FAYYAZ SINGAPOREWALA, DANIEL LEPKOWSKI AND JOHANNE CHU FROM NEW SILICON CORPORATION

THE MAINSTREAM semiconductor industry is continuing to head in the same direction. The focus, as always, is the miniaturisation of the silicon transistor. Success on this front today allows more of them to be packed on an IC, making this chip more powerful. It's an approach that enhances the capability of memory and computation but is expected to lead to commoditisation as this industry continues to mature.

In addition to scaling, the silicon industry is exploring other directions. That includes the integration of silicon with compound semiconductors, a marriage that has much promise as it offers the opportunity to draw on the best of both worlds. There is the tantalising prospect of combining the low cost, impressive toolsets and high volumes of the silicon industry with the prowess of the compounds, which include powerful light emission, high blocking

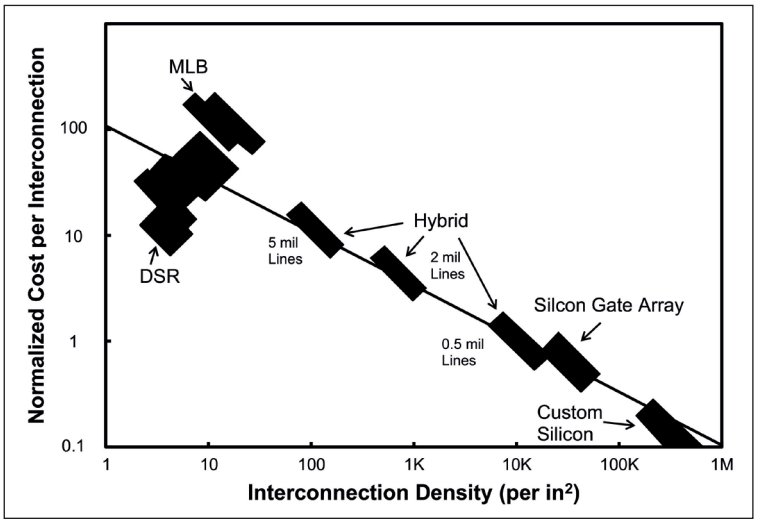


voltages, and efficiency and power in the RF domain.

It is crucial that when the compounds are united with silicon, the strengths associated with the latter technology are retained. Occupying the top spots of this valued list are the need for high-density devices, enhanced performance from scaling, and cost reduction.

Historically, increases in device density have been a major driver behind improvements to microprocessors, multicore processors and silicon memory. In the future, high transistor and LED densities will be needed in augmented-reality displays accommodating millions of pixels, as well as pixelated light sources and highly efficient single-chip phased arrays.

In general, scaling has excelled in increasing the 'bang' while lowering the 'buck'. Miniaturisation can be credited for higher circuit frequencies, lower power consumption, lower parasitics, reduced noise and superior heat removal. It's forecast that these performance enhancement benefits from miniaturisation will continue, with possible new dimensions for the digital control of arrays of high-density devices, such as LEDs and HEMTs.



➤ Figure 1. Cost per interconnection versus interconnection density. Custom silicon and silicon gate array are monolithic silicon chips (BEOL of CMOS is interconnecting high-density transistors). When interconnect (and therefore device) density at the chip level decreased to approximately 10,000 per square inch in 1984, costs favoured the fabrication of longer interconnects at the board/package level. [Adapted from W.H. Knausenberger and L.W. Schaper, "Interconnection Costs of Various Substrates- The Myth of Cheap Wire", IEEE Transactions on Components, Hybrids, and Manufacturing Technology, vol. CHMT-7, pp. 261-263, September 1984.]

The trimming of costs that come from scaling are not just due to an increase in the number of circuits per area, ensuring a reduction in the cost to produce each circuit. There is also the average cost for the interconnects between devices to consider – this depends on the interconnect length, with shorter interconnects more cost-effective.

Since the 1980s, the economics of monolithic integration at the chip level have been understood (see Figure 1, which demonstrates the relationship between interconnect density, cost per interconnection, and device density). We have come a long way since 1984, when interconnect density was below 10,000 per square inch and it made economic sense to have interconnects at the board/package level, rather than at the chip level. Over the intervening years, there has been the introduction of more and more wiring levels in chips, and interconnects have migrated from the board or package level to the chip level.

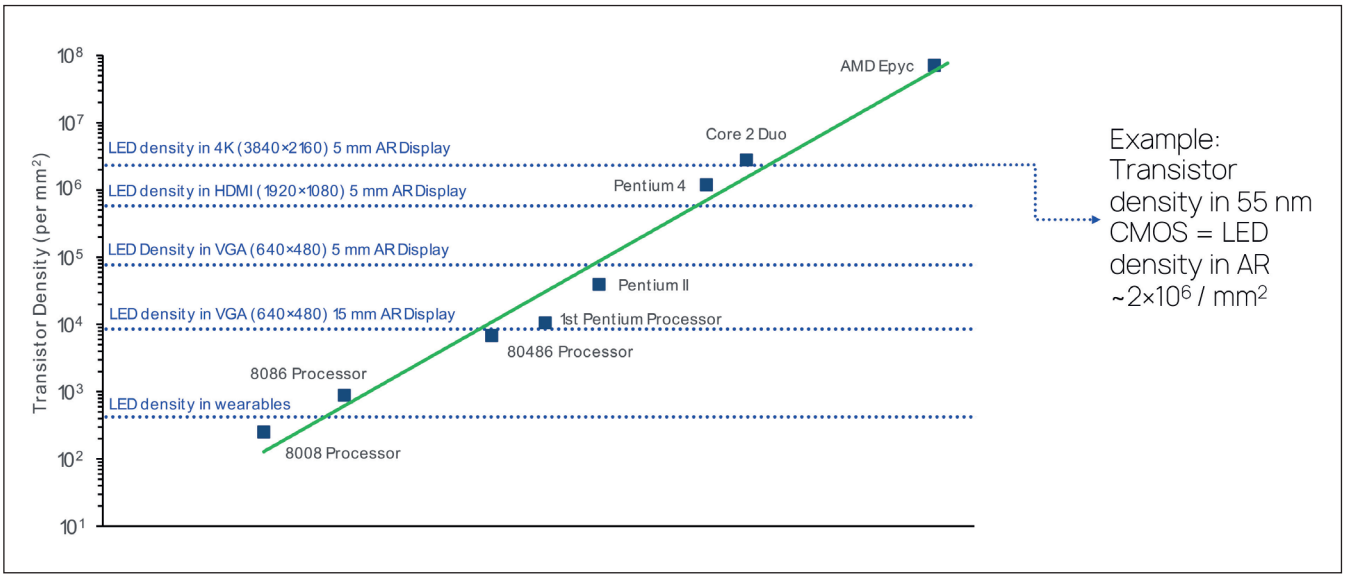
As well as the three strengths just outlined – the new chip possibilities, enhanced performance and cost reduction – there are others associated with silicon manufacturing that should be retained when compound semiconductors are brought onboard. These merits include a high yield, a high level of reliability, and speedy product design cycles. Yield and reliability have undergone steady improvement, due to the use of the same fabrication process for multiple products. A high yield is also aided by low-cost self-diagnostic capabilities for in-line and post-processing measurements – these are features that are facilitated by the integrated design process.

Another asset is the use of a common silicon wafer manufacturing process, which increases the volume of products passing through the process, and drives improvements to yield, reliability, and cost-effectiveness. Crucially, despite the common approach, each customer retains their own design intellectual property.

Integration with LEDs

One attractive opportunity for integration involves the creation of a single-chip LED display, formed by using millions of transistors to drive and address millions of LED pixels. In this case, the LED density in these displays is comparable to the density of transistors in early microprocessors. Due to this, as was the case with those microprocessors, it makes little sense to package all these components together, because it is not feasible to achieve such density, the cost is too high, and such an approach would negate the advantages, in terms of yield and reliability, that come from monolithic integration.

It is possible to compare the density of LEDs in a range of products, including wearables, virtual reality and augmented reality, with historic transistor densities (see Figure 2). This plot shows that the manufacturing of LED displays can be disrupted when LEDs become part of silicon manufacturing and are interconnected with CMOS using the CMOS back-end-of-line (BEOL) approach. Note that arguing against such a trend is as nonsensical as suggesting

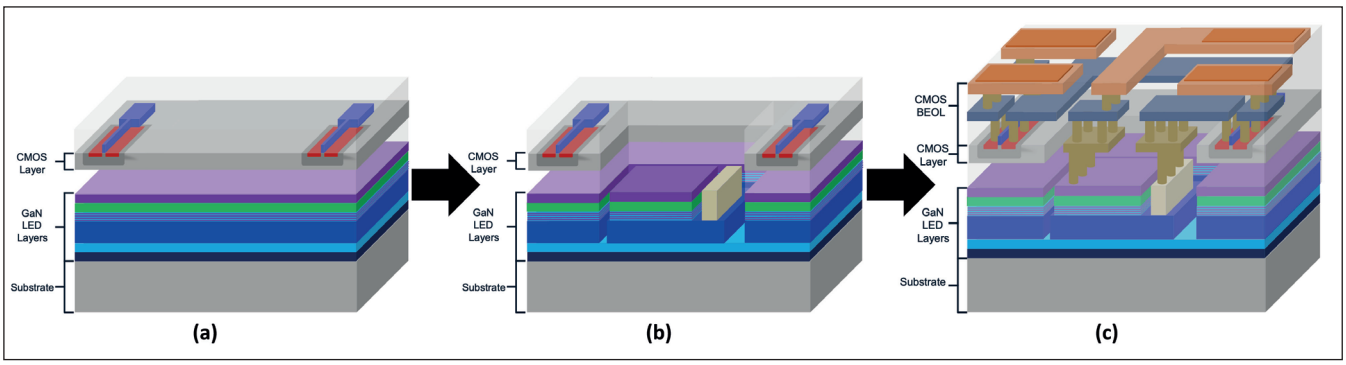


➤ Figure 2. The line across the graph represents the historic increase in the density of transistors over time. Superimposed are LED densities in current and future LED display products. With monolithic silicon integrated circuit manufacturing of CMOS + GaN LEDs, microdisplays will be single-chip and manufactured in silicon fabs.

that the Pentium processor should have been constructed by packaging individual transistors together, such as through mass-transfer or pick-and-place techniques.

To support the advance of single-chip displays, our team at New Silicon Corporation, Singapore, has developed the necessary materials, processes, structures, devices, and software design modules to create integrated circuits using silicon integrated circuit manufacturing that can unite CMOS devices and GaN-based LEDs. Our first set of products will be white or monochrome LEDs, the latter available in red, green and blue. For red and green variants, emission will result from blue light that pumps quantum dots. Further ahead, we plan to produce integrated full-colour displays, with quantum dots present on the red and green pixels.

Our CMOS + III-V process consists of three stages (see Figure 3): CMOS front-end of line (FEOL), new III-V FEOL, and CMOS BEOL. The first and last stages are taken directly from standard silicon CMOS manufacturing, which produces complete circuits by connecting transistors with a FEOL process on silicon wafers using a multi-level metal interconnection network formed in the BEOL. For our CMOS + GaN LED process, we sandwich a GaN FEOL between the CMOS FEOL and BEOL. After GaN LEDs are fabricated, the BEOL's interconnection network connects CMOS transistors and LEDs to create a monolithic integrated circuit. The silicon CMOS BEOL serves as the interconnection network for both silicon and III-V devices. It's an approach that enables an integrated design environment using standard integrated circuit design software.



➤ Figure 3. The monolithic process for creating CMOS + III-V circuits begins by processing III-V devices on the same wafer as the silicon transistors, after the silicon transistors have been processed. With the silicon process strategy of sequential masks, each aligned to the one before it, is critical for a processing platform to gain the benefits of integration and miniaturisation across many product segments. (a) A standard silicon FEOL is fabricated, according to the design, in a foundry and transferred onto a III-V-on-silicon epitaxial wafer. (b) III-V device FEOL is done, automatically aligned to silicon FEOL via sequential masks. (c) Sequential masks form the silicon BEOL, which interconnects the silicon transistors and III-V devices according to circuit design. Diagrams are not to scale or proper aspect ratio.

A tremendous benefit of adopting the silicon front-end and back-end processes for III-V devices is that each mask is aligned to the former one, guaranteeing yield and reliability across the wafer. In addition, this approach eradicates problems that arise when fabricating silicon transistors and III-V devices separately, and then trying to use wafer-scale metallic bonding and alignment to interconnect the devices. When III-V devices are on a separate wafer, realising high-density alignment across the two types of wafers with different materials stacks and thermal expansion coefficients is problematic and low yielding, especially at 200 mm or larger wafer sizes.

Another challenge when uniting III-Vs and silicon is optimising the usable wafer area across both device layers. When wafer bonding is employed to combine silicon die and III-V die, the area occupied by III-V devices is not the same as that occupied by the silicon circuits. Consequently, the unused area on a wafer – often the III-V wafer – is required to spread out circuit components for alignment to the other die on the wafer. This is far from optimal, as it decreases the effective chips per area and increases cost. Unfortunately, this fundamental cost and design constraint is often overlooked, and the limited use cases and higher costs that follow are a headwind to potential wafer sales volumes, further increasing the cost-per-wafer for wafer-bonding approaches.

A far better approach is true monolithic integration. Using sequential masks, as is the case in silicon integrated circuit design and manufacturing, we use integrated circuit designs that intermix silicon and III-V devices. This approach enables the most compact area and the most efficient design, both for circuits and for chips. As all designs employ the same process, wafer volume is maximised, helping to ensure the lowest cost per wafer.

One crucial step in our monolithic process is the transferring of the CMOS FEOL onto a GaN-on-silicon epiwafer. After the transfer, the CMOS FEOL remains on the wafer's surface, resembling a regular CMOS wafer. The GaN LED epitaxy beneath the CMOS FEOL surface is hidden, but the processing of GaN LEDs in specific areas is still possible, by etching through the top thin surface of silicon that hosts the CMOS FEOL.

With our approach, the areas reserved for LED fabrication must be kept separate from CMOS components. This is accomplished by incorporating III-V device models into the standard CMOS design kit that's provided by the foundries that provide the FEOL and BEOL services. The development of a process design kit (PDK) is crucial for bridging the gap between integrated circuit design and semiconductor foundries for chip fabrication.

We have developed an integrated CMOS + GaN PDK that provides comprehensive solutions for large-scale circuit simulation, design, and layout verification. This PDK allows for circuit design and fabrication on our proprietary integrated CMOS + GaN wafer technology. Our PDK libraries are specifically tailored to our CMOS + GaN offerings, and they cater for unique applications that are outside the scope of the portfolio of conventional CMOS or GaN foundries.

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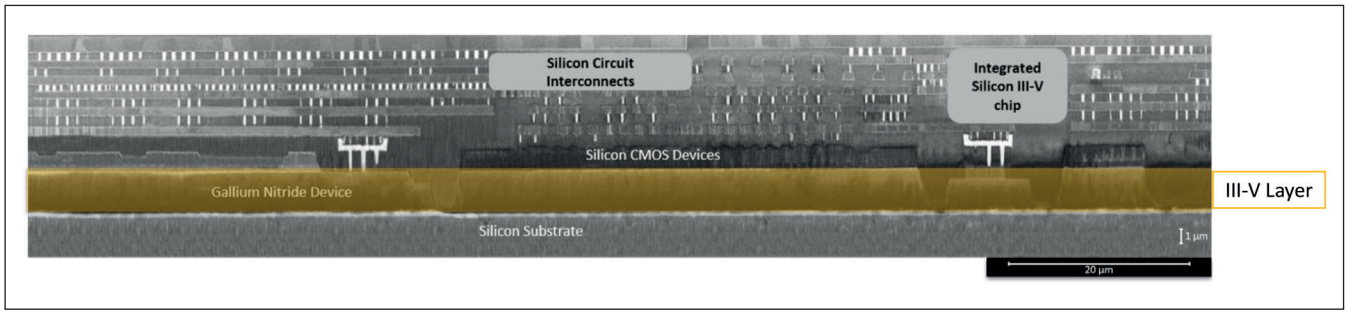
Thanks to close collaboration between the process development and IC design teams, we have carefully fine-tuned every aspect, thereby ensuring a robust, reliable bridge between integrated circuit design and fabrication. Our efforts will provide the catalyst to a new era of chip-based solutions for displays, lighting, and wireless systems, overcoming the challenges of III-V-on-silicon integrated circuit design and fabrication (see Figure 4 for an example of a processed 200 mm CMOS + GaN LED circuit).

So far, we have focused on rolling out our initial platform, the CMOS + GaN LED platform. However, our monolithic integrated circuit process can be applied to any CMOS + X platform, where X could be a III-V, or another semiconductor material or device. For integration, it is essential that: there is the capability to produce epitaxial device layers on silicon wafers with an appropriate diameter for silicon line manufacturing; and the defect density in these epitaxial device layers is low enough to ensure and maintain a satisfactory performance in the final integrated devices in the circuit throughout the product lifetime.

As we ramp production of digitally controlled power amplifiers, we are preparing for the introduction of our next product: single-chip phased arrays for 5G/6G. Faster data rates have led to increases in wireless communication frequencies, which has had the downside of higher degrees of absorption in the atmosphere. Due to this, there's a need to focus the transmission of high-frequency wireless signals on the cell recipient station. In the infrastructure of yesteryear, this would have been accomplished with



➤ Figure 4: A transmission electron microscopy cross-section of a finished 200 mm wafer processed using silicon foundry manufacturing. The tungsten plug process used for the BEOL is used to also connect to the III-V FEOL.

movable dish antennas. However, that's not feasible in consumer devices. In the likes of the smartphone, one way to electronically steer the wireless beam towards the receiver is to use a chip populated with multiple GaN HEMTs, precisely arranged at specific distances from each other on a plane. We view these single-chip phased arrays, manufactured at lower costs in silicon fabs, as crucial for expanding the deployment of high-bandwidth consumer wireless systems.

There is no doubt that the integration of III-V materials and devices into silicon integrated circuits is opening up entirely new market segments for the silicon industry. For that industry, the monolithic integration of new devices into silicon systems will define the next stage of growth, driven by miniaturisation, integration, and scaling of integrated circuits. This will create new high-growth markets, targeted by high-performance systems produced at very competitive costs.

Our immediate focus is the microLED illumination and display market. According to analysis by Spherical Insights and Straits Research, this market had a value of $650 million in 2022, and is forecast to climb at a compound annual growth rate of more than 80 percent through to 2030, when it will be worth $36.5 billion.

Demand is driven by the desire for brighter, more powerful display panels for consumer electronic devices, including high-end smartphones and wearable displays, such as head-mounted devices.

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About SEMI:
SEMI connects more than 2,500 member companies and 1.3 million professionals worldwide to advance the technology and business of electronics design and manufacturing. The breadth and depth of our events, programs and services help members accelerate innovation and collaboration on the toughest challenges to growth.

ESDA Electronic System Design Alliance

FlexTech

FOA Fab Owners Alliance

MEMS & SENSORS INDUSTRY GROUP®

SOI Industry Consortium

Chasing the swarm: the new challenge for chip manufacturers

From the geopolitical sparring of China and the US to the global supply chain upon which we all depend, those watching the worldwide semiconductor market will be witnessing an ever-changing environment – and one that's now never far from the news.

BY MARK LIPPETT, CEO, XMOS

THAT NEWS CYCLE highlights the sheer scale of investment into chip production in 2023. Whether it's TSMC's Arizona fab or Intel doubling investments in Germany, Israel, and Poland, chip manufacture is a higher priority than ever before for many key players.

Such investment demands analysis. Justification of intense spending tends to revolve around the resilience of the supply chain. What it doesn't always consider is that we're building capacity into semiconductor technologies (aka nodes) that might not actually be the dominant nodes for much longer.

Whilst headline-grabbers and policymakers focus on glamorous bleeding edge technologies, suitable for limited use-cases, the intelligent IoT is rapidly driving demand for a more diverse range of chips for an ever-fragmenting marketplace. In McKinsey research, the top five "use case clusters" for the IoT – out of 99 – represent only about 52% of the market's total potential economic value. In the meantime, the number of IoT device connections worldwide, is set to double to 4.3bn by 2026.

In other words: while the IoT may be regarded as a "sum of niches", the depth and breadth of potential markets for intelligent IoT technologies is huge. The landscape is not only growing, but also evolving at pace, as the industry adapts to growing demand for versatility.

The rise of the IoT

As a result, it's no longer the case that one type of chip or system-on-chip (SoC) can be developed for one market sector. SoCs need to adapt quickly and

smartly to this broad range of new applications. From a semiconductor engineering perspective, the foundation for this market explosion will be silicon that prioritises performance and cost-effectiveness above all else. It requires hardware that is financially viable to be deployed at scale, and that can offer the engineer a canvas upon which to rapidly develop – or edit – the perfect solution for their device.

In a survey of product engineers we commissioned in 2022, almost two thirds (63%) of respondents cited greater product functionality as their most common product priority for the year ahead. A similar number (64%) also said that the majority of their product ranges would have the processing power to support the intelligent IoT in the next 2-3 years; while 26% stated that their entire range would be compatible.

And with these smart, networked products comes a host of new spin-offs, upgrades, and opportunities for enhanced functionality. This raises their complexity way beyond the scope of the traditional market models we've seen previously.

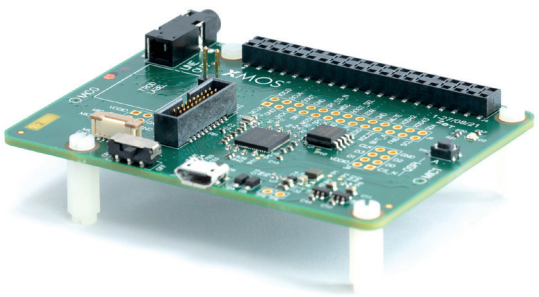
So, what does this mean for chip manufacturers targeting companies in this new era of IoT-dominated product development?

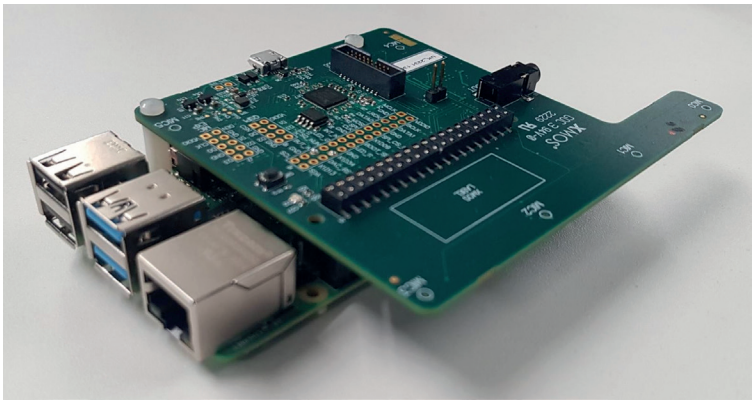
Chasing bees

To use an analogy, over the past 40 years, semiconductor giants have been perfecting how to hunt easily identifiable, relatively slow-moving targets – well-understood markets such as PCs, cameras, or smartphones that we might think of as 'big game'. They did this with sophisticated single-chip solutions which could be targeted at a distance, with approaches that took years to hone and tailor for each of these 'beasts'.

This tactic worked while market requirements moved at a pace that reflected the time-consuming and expensive process of semiconductor tooling and manufacture. Not now. With the increase in IoT-enabled products, the nature of the target has changed. No longer are these companies aiming at a single beast, but instead a fragmented, dynamic, and unpredictable throng, more comparable with being in a room with a swarm of bees.

That's not an ideal scenario for any manufacturer. And when you're designing hardware SoCs, which take a long time to design and produce, that's an even tougher position to be in.





So, to carry the metaphor on, how can these bees be targeted? Certainly not with a hunting rifle at a distance.

A shotgun approach...

In recent years the traditional SoC has evolved from an application-specific solution to a Swiss army knife; a hardware solution that combines tools that each have merit for one or more applications but are rarely all needed in the same device, even if the platform allows it (which it frequently does not).

Why is this happening? Because the enormous cost of traditional SoC development can only be justified by an artificially extended market spread – to return to our hunting analogy, you might call this a shotgun approach.

The irony is that such an approach, which descends from products designed to be application-specific and efficient, are now so laden with features that they compromise both power and unit economics in systems that prioritise both.

The end of the analogy?

Whilst it is tempting to think about the IoT as a monolithic swarm of bees, we must remember that each bee – each niche – has individual needs. In the pursuit of their market, semiconductor customers do not care about features designed to address the needs of others. They do care about the fast and efficient implementation of their requirements.

How can you be fast when a new chip design takes years? The answer is to use an existing chip – one that is available off the shelf.

How is that going to meet the functional needs of your application? By being flexible enough to enable you to adapt it to your needs.

How is that ever going to be cheap enough? By adopting an approach that is not bloated by the needs of other applications.

The requirement for "field programmability" has never been greater. Off-the-shelf silicon that can be rapidly and economically adapted to the needs of the fast-evolving IoT – breaking the mould of system design and delivery.

Waging a war on wastewater

Next-level water utilization and recycling for increased capacity means adopting newer technologies. Membrion is a start-up that has developed a novel electro-ceramic desalination technology that uses electricity and ceramic membranes to shrink the volume of harsh industrial wastewater.

BY MEMBRION

THE WORLD KNEW it had a shortage of semiconductors even before the supply chain snarls of the COVID-19 pandemic. Booming demand is straining production at existing facilities, and while new facilities are under construction, it will be years before they become fully operational. Syncing the supply and demand curves for semiconductors will not happen anytime soon, and using legacy technologies for critical processes, such as the flow of wastewater, will not speed things up.

There is a surprising entrant into this industry: Membrion. Their target is expanding the capacity for wastewater, which can unlock a facility's true potential. Increasing wastewater capacity gives semiconductor manufacturers the capability to upgrade existing facilities with new, higher-throughput tools and the flexibility to meet emerging environmental priorities.

Membrion is a start-up that has developed a novel electro-ceramic desalination technology that uses electricity and ceramic membranes to shrink the volume of harsh industrial wastewater. This provides manufacturing facilities with a faster path to respond to growing demand for their products by ensuring that the limiting factor is not a facility's 20+ year old wastewater treatment processes.

While more semiconductors bring welcome relief to many supply chains, the semiconductor manufacturing process delivers a one-two punch to local water sheds. On one hand, its manufacturing processes require a significant amount of water, and for semiconductors, much of that water must be ultra-pure. On the other hand, semiconductor manufacturing consumes no water and so everything becomes wastewater that must also be treated before being discharged. Together, this translates into two needs: First, a need for next-level water utilization and recycling processes, and second, the need for increased capacity within industrial wastewater facilities.

Next-level water utilization and recycling for increased capacity means adopting newer technologies. These do not include the monolithic, inefficient water systems and tools of the past – Membrion brings a new approach. Membrion technology was proven in multiple industrial markets, including semiconductors. In fact, in 2022, they are one of three water technology

industry finalists for the Startups for Semiconductor Sustainability initiative led by SEMI. Subsequently, Membrion announced an investment from Lam Capital and Samsung Venture Investments. After multiple successful pilots and near-term commercial installations, Membrion has grown into a unique and valuable capacity expansion tool for facilities looking to accomplish more while consuming less.

If a new semiconductor plant is under construction in the United States, chances are good that Membrion's CeramIX® electro-ceramic desalination (ECD) membrane modules are being evaluated. Similarly, exiting semiconductor plants are looking to expand capacity, and Membrion helps them shrink wastewater, enabling expanded capacity.

Electro-ceramic desalination membranes at work

Membrion's flexible electro-ceramic desalination membranes are made from an abundant natural resource, silica. These electro-ceramic desalination membranes are designed to handle harsh conditions, resist fouling, and work in extreme pHs.

Membrion's membranes are manufactured via roll-to-roll processing, which makes these desalination membranes economical. Plus, the beauty as it relates to facilities (and their many constraints) is that the membranes are used in stacked modules which are customizable and compact.

Membrion's team works together with each customer to provide what they need to their exact specification and to maximize the capacity and flexible operation of their facility.

For existing semiconductor manufacturers, maximizing reliability is job number one

Reliability and capacity for wastewater treatment are one and the same. The capacities of the combined reuse and disposal systems of any manufacturing facility must equal or exceed the treatment plant capacity to ensure that the wastewater being processed can go somewhere. Capacity is the ability of facilities to treat, move, or process water. It is typically expressed in MDG (million gallons per day). Generally, when a facility is planned, there is a plan for the capacity for a certain amount of wastewater. What happens over time, as facilities become more and more productive, they end up using up their capacity. The norm becomes the facility operating at the razor's edge of capacity. They cannot just dispose of wastewater down drains; they must treat it first.

Semiconductor facilities require a long time to build products, and yet the demand for what is manufactured is high, so the pressure is on to create a facility with high capacity. For pre-existing facilities, capacity is set and the expanding capacity with traditional technologies often requires significant additional space that is not always available.

Sometimes the facility is built, and the production goals change or increase to meet demand. Then, the wastewater capacity plan needs to be revised to accommodate higher production rates. Membrion, with modules which are customizable, can provide more capacity for existing facilities and more flexibility to meet those demand challenges with a minimal system footprint.

Membrion takes the challenging contaminants in wastewater and shrinks them into a much smaller volume than the volume with which the manufacturing facility started. If operating at or near capacity, Membrion can take that water and shrink it to a range of a factor of 5 to a factor of 50, depending on the wastewater stream. This optimizes and expands the capacity on which the facility may operate. Membrion creates a significant amount of capacity for wastewater treatment to continue to be used and operated effectively.

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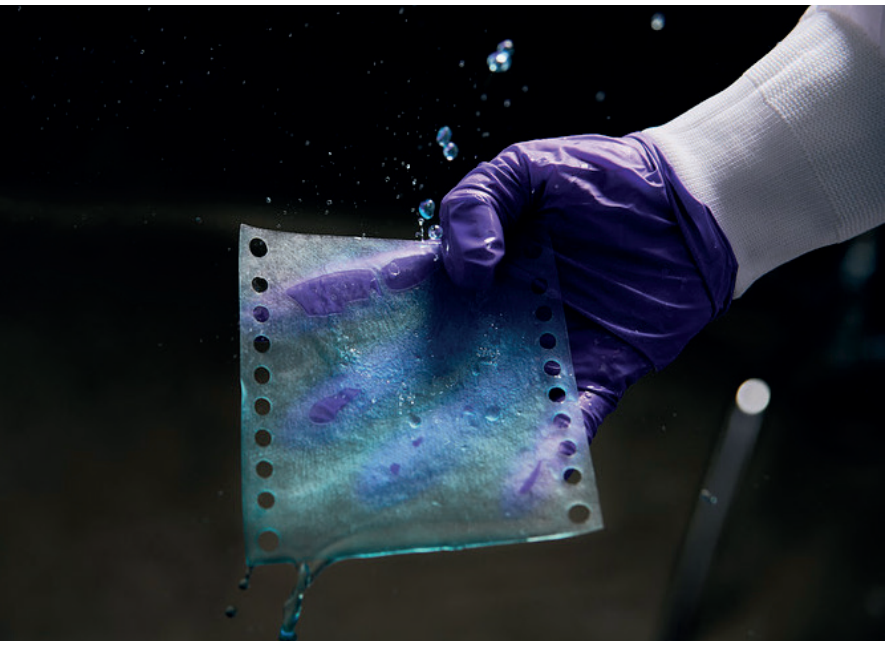

One of the ways the shrinking of the volume of wastewater occurs is through cooling towers. Membrion pioneered a new approach to cooling tower water treatment to reduce water needs in manufacturing. Membrion's innovation, which incorporates its CeramIX® ceramic ion exchange membrane, is to prevent the minerals from building up in the first place. Pulling out minerals slowly over time ensures that the cooling tower can continue recycling its water, leading to higher cycles of concentration of >20 CoC. It can be paired with new or existing cooling towers and enables users across industries to improve water savings.

Membrion also steps in to assist and provide guidance in increasing permitted capacity for operational semiconductor facilities. Most facilities have permits for certain amounts of water, the types, and contaminant levels which they can discharge.

Membrion can assist by helping facilities stay within their existing permits by ensuring that challenging wastewaters, such as copper wastewater, are reduced in volume, which enables them to stay within their existing permits. Further, when new equipment is installed and requires permits, Membrion works with contractors and trade groups during the permitting process to ensure compliance and adequate capacity. There are additional benefits to the use of ECD technology in wastewater processes, including the reduction in the amount of chemicals needed, a reduction in the labor involved, and less energy consumption. Environmental, social and governance goals (ESG) can be met.

Changing compliance rules can also throw a wrinkle in semiconductor manufacturing processes and wastewater treatment capabilities. As those regulations continue to change and evolve, manufacturers must adapt. Since semiconductor manufacturing facilities are designed with older regulations in mind, they do not necessarily have additional space and are challenged to adapt to new regulations due to space constraints, making optimizing and expanding their capacity, and shrinking their wastewater, extremely important.

Opportunities in new semiconductor manufacturing facilities

New semiconductor manufacturing facilities, including the Intel plant in New Albany Ohio, require many years of planning and construction before the plant is operational and can begin to fulfill the demand for semiconductors. They require the involvement of many industries and a variety of expertise to plan, construct, support, and eventually produce semiconductors.

This includes the involvement of the water industry. It is often reported how great the impact of semiconductor manufacturing is on the water industry – using significant amounts of water. Without the integration of new technologies, like ECD, these water demands made the local water sheds gag, and even choke.

Membrion unlocks the potential for new facilities to incorporate state-of-the-art water reuse and water recycling processes from the beginning and to reduce CAPEX and OPEX for the entire life cycle of the facility.

Industry poised for 2024 recovery

The global semiconductor manufacturing industry recovery is taking hold with electronics and IC sales increasing in the final quarter of 2023 and more growth projected for 2024, SEMI recently announced in its fourth quarter 2023 publication of the Semiconductor Manufacturing Monitor (SMM) report, prepared in partnership with TechInsights.

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In Q4 2023, electronics sales edged up 1% Year-over-Year (YoY), marking the first annual rise since the second half of 2022, and growth is projected to continue in Q1 2024 with a 3% YoY increase. At the same time, IC sales returned to growth with a 10% YoY jump in Q4 2023 as demand improved and inventories started to normalize. IC sales are forecast to strengthen in Q1 2024 with 18% YoY growth.

Capital expenditures and fab utilization rates are expected to see a mild recovery starting in Q1 2024 after significant declines in the second half of 2023.

In Q1 2024, Memory CapEx is projected to increase 9% Quarter-on-Quarter (QoQ) and 10% YoY, while Non-Memory CapEx is on track to climb 16% during the quarter but remain at lower levels than recorded in Q1 2023. Fab utilization rates saw a modest improvement from 66% in Q4 2023 to 70% in Q1 2024. Meanwhile, fab capacity grew 1.3% in Q4 2023 and is projected to match those gains in Q1 2024.

Equipment billings in 2023 surpassed projections though growth is expected to be muted in the first half of 2024 mostly due to seasonality. “The electronics and IC markets are recovering from a slump in 2023 with growth expected this year,” said Clark Tseng, Senior Director of Market Intelligence at SEMI. “Although fab utilization remains low at the moment, improvement as 2024 unfolds is anticipated.”

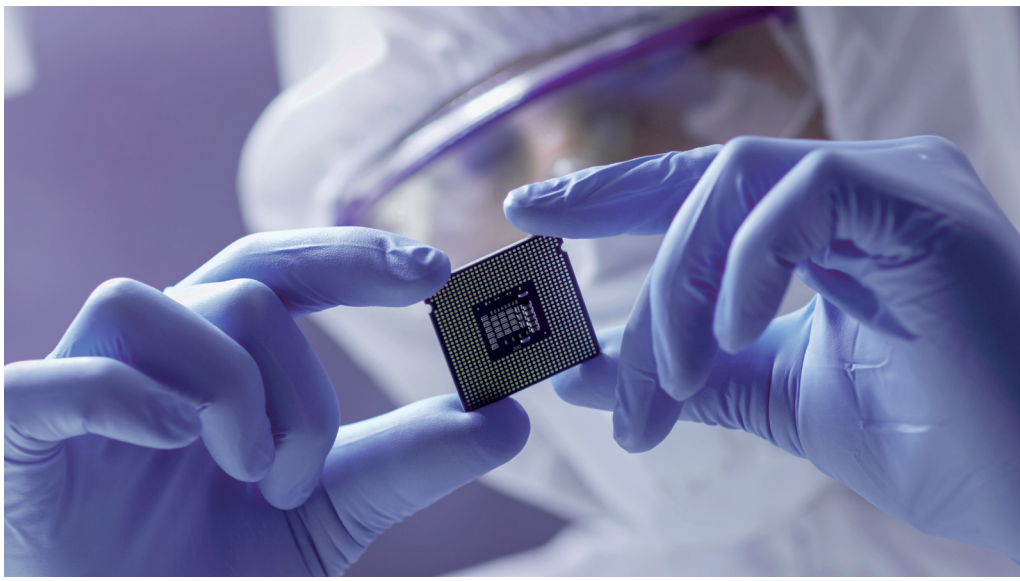
“Semiconductor demand is well on its way in the recovery,” said Boris Metodiev, Director of Market Analysis at TechInsights. “While the overall IC market is growing this year, slowing automotive and industrial markets are hampering the analog expansion. AI will be a huge catalyst for leading-edge semiconductors as the technology proliferates from the cloud to the edge. At the same time, geopolitics is driving excess capacity at the trailing edge.”

Silicon revenues fell in 2023

Worldwide silicon wafer shipments in 2023 decreased 14.3% to 12,602 million square inches while wafer revenue contracted 10.9% to $12.3 billion over the same period, the SEMI Silicon Manufacturers Group (SMG) reported in its year-end analysis of the silicon wafer industry.

The decline, a sharp departure from the previous three years of consecutive growth, stemmed from a slowdown in end-demand, coupled with a broad-based inventory correction. Softening memory and logic sector demand led to a decline in orders for 12-inch wafers, while weakening foundry and analog uptake accounted for a drop in shipments of 8-inch wafers.

“Shipments of 12-inch polished and epi wafers contracted 13% and 5% in 2023, respectively,” said Lee



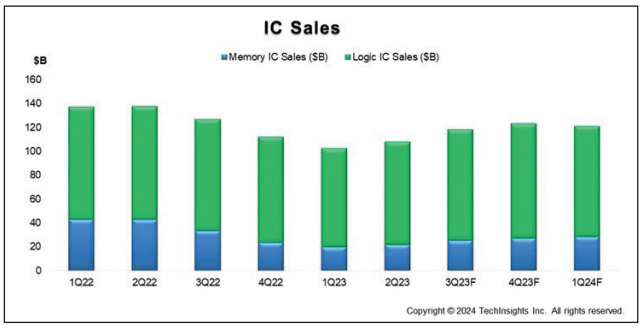
Chungwei, Chairman of SEMI SMG and Vice President and Chief Auditor at GlobalWafers. “Total shipments of all wafer sizes slipped 9% in the second half of 2023 relative to the first half of the year.”

European economic security strategy

SEMI has applauded the European Commission for inviting industry feedback as it formulates the European Economic Security Strategy to strengthen Europe’s economic security in the face of ongoing geopolitical tensions and strategic dependencies that characterize the European semiconductor industry.

SEMI recently published Priorities on the European Economic Security Strategy, a position paper that offers the following key recommendations for policymakers to consider:

- Complement European Economic Security Strategy initiatives with additional promote-side measures and proposals focused on strengthening the European high-tech ecosystem and the European Union’s global competitiveness.
- Bolster international cooperation in the semiconductor and high-tech industries through free trade agreements and international partnerships.
- Maintain proportionality when drafting legislation that addresses risks while avoiding unnecessary bureaucratic burden for companies and preserving the EU’s competitiveness.
- Improve coordination and further harmonize EU export control policies with a view to strengthening the EU’s voice on the global stage.
- Establish ongoing dialogue with the semiconductor industry to prevent unnecessary due diligence, risk management and reporting obligations for companies across the supply chain.



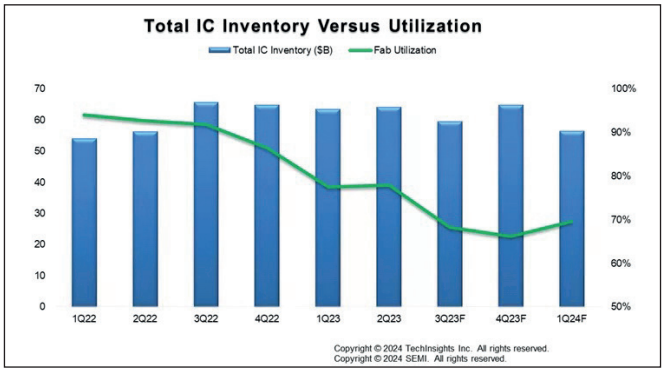
SEMI encourages the European Commission to place equal emphasis on the protect, promote and partner aspects of economic security in order to give European companies the highest possible level of access to global markets.

“The European Economic Security Strategy should foresee a structured dialogue with industry stakeholders based on a common understanding of supply chain risks and economic security,” said Laith Altimime, President of SEMI Europe. “It is vitally important for the European Commission to engage with the chip industry in Europe to enable meaningful conclusions and effective policy decisions.”

SEMI continues to engage with policymakers to encourage a legislative framework that enhances the EU’s economic security across industrial supply chains while preserving Europe’s technological competitive advantage.

300mm fab equipment spending to reach record level

Global 300mm fab equipment spending for front-end facilities is forecast to reach a record US$137 billion in 2027 after topping US$100 billion for the first time by 2025 on the strength of the memory market recovery and strong demand for high-performance computing and automotive applications, SEMI highlighted in its quarterly 300mm Fab Outlook Report to 2027 report.



Worldwide 300mm fab equipment investment is expected to increase 20% to US$116.5 billion in 2025 and 12% to US$130.5 billion in 2026 before hitting a record high in 2027. “Projections for the steepening ramp of 300mm fab equipment spending in the coming years reflects the production capacity needed to meet growing demand for electronics across a diverse range of markets as well as a new wave of applications spawned by artificial intelligence (AI) innovation,” said Ajit Manocha, SEMI President and CEO. “The newest SEMI report also highlights the critical importance of increases in government investments in semiconductor manufacturing to bolster economies and security worldwide. This trend is expected to help significantly narrow the equipment spending gap between re-emerging and emerging regions and the historical top-spending regions in Asia.”

Regional growth

The SEMI 300mm Fab Outlook to 2027 report shows China continuing to lead fab equipment spending with US$30 billion in investments in each of the next four years fueled by government incentives and domestic self-sufficiency policies.

Supported by leading-edge nodes expansion for high-performance computing (HPC) and the memory market recovery, Taiwanese and Korean chip suppliers are increasing their equipment investments.

Taiwan is expected to rank second in equipment spending at US$28 billion in 2027, up from US$20.3 billion in 2024, while Korea is expected to rank third at US$26.3 billion in 2027, an increase from US$19.5 billion this year.

The Americas is projected to double 300mm fab equipment investments from US$12 billion in 2024 to US$24.7 billion in 2027, while spending in Japan, Europe & the Middle East, and Southeast Asia are expected to reach US$11.4 billion, US$11.2 billion, and US$5.3 billion in 2027, respectively.

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