SILICON SEMICONDUCTOR

VOLUME 46 ISSUE III 2025

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

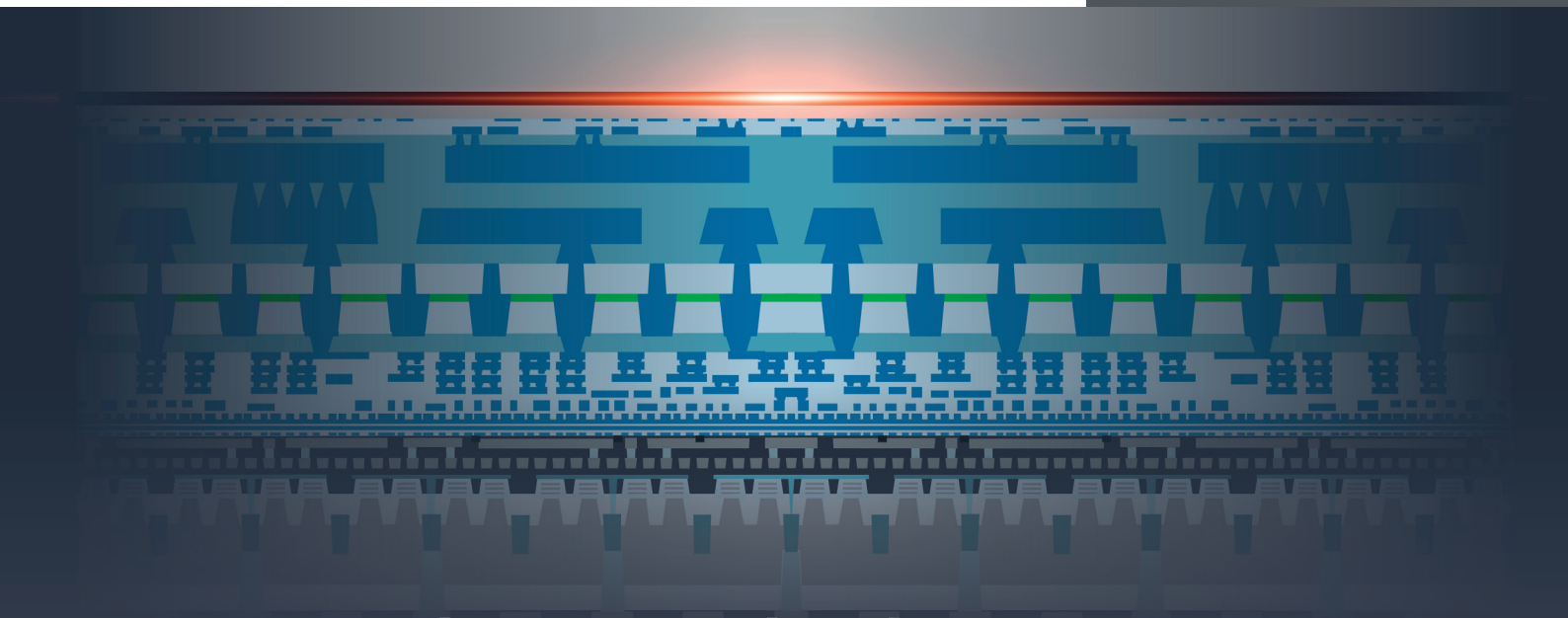
SILICONSEMICONDUCTOR.NET

ADVANCED FABS REQUIRE MORE INNOVATIVE FACILITY SERVICES FOR EFFICIENCY, RELIABILITY AND RESILIENCY

EVG®

invent
innovate
implement

www.EVGroup.com



IR LayerRelease™ Technology

- Replacement for mechanical debonding thanks to through-silicon IR laser
- Enabling ultra-thin film or layer transfer from silicon carriers
- Nanometer-precision release of bonded, deposited or grown layers
- Front-end compatibility through silicon carriers and inorganic release materials
- Supporting future roadmaps in advanced packaging and transistor scaling

EVG®880 LayerRelease™

GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com

VIEWPOINT

BY PHIL ALSOP
EDITOR

Microchips – time for an EU re-think?

WHILE ONE WOULD hesitate to characterise the European Court of Auditors' assessment that 'it is very unlikely that the EU will meet its target of a 20% share of the global market for microchips by 2030' as similar to President Trump's US Chips Act 'reappraisal', in both cases it seems that the initial excitement and euphoria of such large scale investment being made in the semiconductor sector has given way to a more sober and realistic understanding of the difficulties faced in trying to incentivise and support onshoring and re-shoring across multiple regions and countries in an even-handed manner.

The European Court of Auditors' Report acknowledges that the 2002 EU Chips Act 'has brought new momentum to the European microchip sector', but that the investments driven by it 'are unlikely to significantly enhance the EU's position in the field'. In simple terms, the 20% target requires a quadrupling of EU production capacity by 2030, which the current rate of progress is a long way from achieving. Hence the report recommends that 'the European Commission should reassess its long-term strategy to match the reality on the ground'.

As with so much in life, it all seems to be a question of money (or lack of it!). The report points out that, from 2020 to 2023, the top global semiconductor manufacturers budgeted 405 billion euros in investment, while the Chips Act has estimated funding of 85 billion euros in total up to 2030, of which only about 4.5 billion euros is the direct responsibility of the European Commission. In other words, the Commission has 'no mandate to coordinate national investments at EU level to ensure they align with the Act's objectives' – not to mention the considerable gap between 85 billion euros over approximately eight years within the EU and the likely hundreds if not thousands of billions invested by the top manufacturers (although some of this investment might well be within Europe one imagines).

The report also highlights a range of other factors which could impact the EU's plans - dependency on imports of raw materials, high energy costs, environmental concerns, geopolitical tensions and export controls, and a shortage of skilled workers – but these factors, or the majority of them, apply equally in other regions across the world, so this is maybe not such an issue. Indeed, as I think I have written before, there are several individual companies, countries and regions which have the power to completely disrupt, if not destroy, rivals' semiconductor industries, should they choose to do so.

Similarly, the concentration of funding on a small number of high-value projects, subject to possible cancellation, delay or failure (or even moving to a different geography) is pretty much a universal problem, with a potentially significant impact on the whole supply chain. But this is not an unusual scenario – just business as usual.

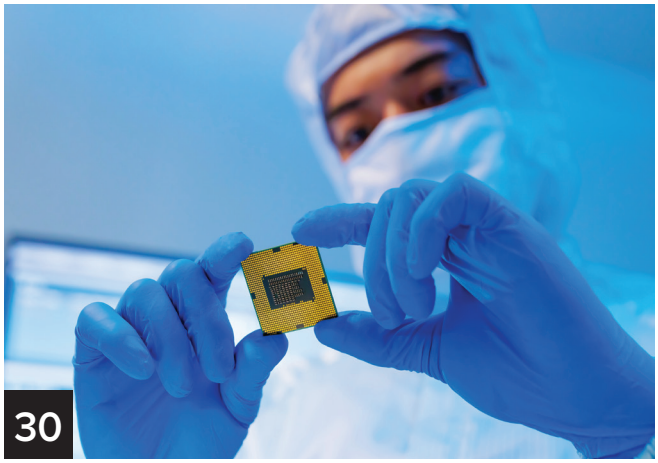
The conclusion of the report is that the Chips Act is 'highly unlikely to significantly increase the EU's share of the microchips market, or to meet the objective of 20% of global output', citing the European Commission's own forecast, published in July 2024, which predicts that 'despite a significant expected increase in manufacturing capacity, the EU's overall share of the global value chain in a fast growing market would increase only slightly, from 9.8% in 2022 to just 11.7% by 2030'.

I believe that a second EU Chips Act is on the horizon, and this might go some way to addressing some of the issues highlighted by the Auditors' report. In the mean-time, we should perhaps admire the energy of all of the various chips investment initiatives across the globe, whilst acknowledging that their timescales and financial targets might be characterised as over-ambitious. Still, better such optimism than an acceptance of the status quo.

CONTENTS

VOL 46 ISSUE III 2025

SILICON SEMICONDUCTOR



NEWS

Publisher Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Editor Phil Alsop phil.alsop@angelbc.com
Sales & Marketing Manager Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214
Chief Executive Officer Sukhi Bhadal sukhi.bhadal@angelbc.com +44 (0)2476 718970
Chief Technical Officer Scott Adams scott.adams@angelbc.com +44 (0)2476 718970

Directors Jackie Cannon, Sharon Cowley

Published by Angel Business Communications Ltd, 6 Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970 E: info@angelbc.com

Silicon Semiconductor is published ten times (6x print and 4x video issues) a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £50.00 per annum (UK) , €60.00 per annum (Europe), $90 per annum (air mail)(USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher. Every effort has been made to obtain copyright permission for the material contained in this publication. Angel Business Communications Ltd will be happy to acknowledge any copyright oversights in a subsequent issue of the publication. Angel Business Communications Ltd © Copyright 2025. All rights reserved. Contents may not be reproduced in whole or part without the written consent of the publishers. The paper used within this magazine is produced by chain of custody certified manufacturers, guaranteeing sustainable sourcing. US mailing information: Silicon Semiconductor, ISSN 1096-598X, is published 5 times a year by Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Rd, Coventry CV5 6SP. UK. Airfreight and mailing in the USA by agent named World Container INC 150-15, 183rd St, Jamaica, NY 11413, USA. Periodicals Postage Paid at Brooklyn, NY 11256. POSTMASTER: Send address changes to Silicon Semiconductor, Air Business Ltd, c/o World Container INC 150-15, 183rd St, Jamaica, NY 11413, USA.

We strive for accuracy in all we publish; readers and contributors are encouraged to contact us if they recognise an error or omission. Once a magazine edition is published [online, in print or both], we do not update previously published articles to align old company names, branding, marketing efforts, taglines, mission statements or other promotional verbiage, images, or logos to newly created or updated names, images, typographic renderings, logos (or similar) when such references/images were accurately stated, rendered or displayed at the time of the original publication. When companies change their names or the images/text used to represent the company, we invite organizations to provide Angel Business Communications with a news release detailing their new business objectives and/or other changes that could impact how customers/prospects might recognise the company, contact the organisation, or engage with them for future commercial enterprise.
Printed by: The Manson Group. ISSN 2050-7798 (Print) ISSN 2050-7801 (Online) © Copyright 2025.

FAMES Pilot Line launches open-access call for chip industry

The FAMES Pilot Line has launched its first Open-Access Call.

A DEDICATED workshop in Brussels generated strong interest from across Europe's semiconductor industry. A great number of potential users participated to learn more about how to submit a User Request to access the pilot line's cutting-edge microelectronics R&D technologies and services.

Initiated in December 2023 by the Chips Joint Undertaking (Chips JU) and coordinated by CEA-Leti, FAMES envisions a strategic leap in semiconductor innovation, while reinforcing Europe's industrial leadership.

Design houses, fabless companies, foundries, integrated device manufacturers, material & tool suppliers, universities and research centers can submit User Requests by responding to the two-month-long Open-Access Call, starting today, or by submitting a Spontaneous User Request throughout the year. Participants whose requests are selected will have access to FAMES technologies as they become available. Open-Access Calls will take place each spring through 2028, with an updated portfolio of available FAMES technologies.

Users of the pilot line will have access to:

- Two types of PDKs
- Pathfinding PDKs for FD-SOI advanced-node performance evaluation,
- PDKs giving access to silicon, via multi-project wafers (MPW),
- Specific process steps, modules, integration flows, and demonstrator esults, and
- Education and training on FAMES technologies.

The Open Access Committee, representing the consortium's 11 Partners, will review and select applicants' proposals. Pricing will

depend on the specifics of each R&D project.

"It is essential that these new technologies can be adopted by EU chip stakeholders. For that reason, FAMES has been strategically structured to leverage them, in order to support all sectors of the EU's semiconductor value chain," said Sébastien Dauvé, CEO of CEA-Leti.

'Imagining New Solutions'

Leveraging the pilot line technology sets enables:

- Further developing customized FD-SOI, eNVM, RF, 3D and PMIC-based solutions to address company-pecific needs,
- Developing innovative designs using FAMES' pathfinding PDKs,
- Testing the unique capabilities of the pilot line's specific circuit designs through MPW opportunities,
- Generating new IP through advanced developments on the pilot line,
- Imagining new solutions for specific markets inspired by FAMES' demonstrators, and
- Training future talent and involving competent individuals in the FD-SOI uropean ecosystem.

The technology sets will enable FAMES to leverage highly differentiating FD-SOI-based solutions. These solutions will strengthen the EU's semiconductor ecosystem's response to rapidly growing demand for low-power, high-connectivity and robustly secure integrated circuits driven by the automotive, IoT, and smart mobile-device markets.

'Beyond Just a Pilot Line'

"We see this initiative, which we expect to go beyond just a pilot line, as a vision for a sustainable, resilient, and innovative Europe. It will bring together industry, SMEs, start-ups, and research institutions, and build an open-access ecosystem that transforms ideas into impactful solutions, fostering collaboration and innovation at every level," said Jari Kinaret, executive director of the Chips JU, an EU public-private partnership dedicated to advancing the EU semiconductor ecosystem.

Specifically, the pilot line envisions new market opportunities for low-power microcontrollers (MCU), multi-processor units (MPU), cutting-edge AI and machine-learning devices, smart data-fusion processors, RF devices, chips for 5G/6G, chips for automotive markets, smart sensors & imagers, trusted chips, and new space components.

'Pan-European Technology Infrastructure'

Nokia, a member of the FAMES External Industrial Advisory Board, said the consortium has the "experience, technological expertise, vision and openness to expand the technology platform further into a pan-European technology infrastructure."

"The pilot line's progress will be essential for Nokia's system-on-chip (SoC) PiCo research program," added Derek Urbaniak, head of SoC development, of Mobile Networks at Nokia. "Nokia's PiCo research group looks forward to receiving results and reports from the FAMES consortium, and possibly to utilize their pilot lines and services for our own validation work and product development."

CHIPDIPLO consortium selected to support international diplomacy in semiconductors

CHIPDIPLO will create a dynamic EU Semiconductor Diplomacy Network to strengthen the EU's economic security and develop a European economic foreign policy.

THE CONSORTIUM is well-connected within industry and policy-maker circles across Member States. It boasts a proven track record of successful policy dialogues and partnerships with leading think tanks in America and Asia.

The call for proposals sought pilot actions to establish dialogues among European non-state actors, such as industry and civil society organizations, with expertise and strategic role in the semiconductors sector, as well as to strengthen relationships with third countries as an important element to achieve a more resilient European semiconductor ecosystem.

CHIPDIPLO aims to create long-term value through three main objectives:

- Enhancing risk evaluation and information sharing among EU semiconductor stakeholders,
- Improving internal coordination,
- Fostering effective international outreach via balanced external partnerships.

As a neutral third party, the consortium will facilitate dialogues, conduct research, and drive advocacy efforts. The consortium plans to host track-2 dialogues focusing on:

- Supply chain resilience,
- Autonomy, indispensability and managing external dependencies,
- Best practices in industrial, innovation, and trade policy,
- Workforce development,
- Competitiveness, technology, and sustainability,
- Weaponisation of value chains amid US-China rivalry,
- Crisis scenarios

Industry webinars will provide a platform for candid discussions among European and global non-state actors.

The consortium will produce policy papers and build monitoring tools such as the EU Semiconductor Risk Monitor, an internal tool for policymakers, supporting monthly updates to the Commission, and the Interactive Map of the EU Semiconductor Ecosystem to enhance collective intelligence and support Member States.

The selected project started on March 1, and will last 18 months. The consortium is composed by:
Institut Montaigne France, Coordinator
www.institutmontaigne.org/en
Central European Institute of Asian Studies (CEIAS) www.ceias.eu
Centre for Security, Diplomacy and Strategy (CSDS)
www.vubtechtransfer.be

European Union Institute for Security Studies (EUISS) - associated partner
www.iss.europa.eu

Strengthening Europe's semiconductor future

AT THE margin of the COMPET Council, responsible ministers of Austria, Belgium, Finland, France, Germany, Italy, Poland, Spain and the Netherlands issued a statement where they agreed to reinforce their cooperation to strengthen European's competitiveness and strategic autonomy in the semiconductor sector by supporting research, expanding production capacity, and fostering a highly skilled workforce.

The European Commission welcomes the Semiconductor Coalition, which provides a strong signal of Member States' commitment to fostering an innovative, competitive, and resilient semiconductor ecosystem in Europe. The Commission strongly supports this initiative and looks forward to continued collaboration with all Member States and with public and private semiconductors stakeholders.

The European Commission has been already working with Member States through the Chips Act, which has mobilized over €80 billion in investments for semiconductor manufacturing and R&D. The work of the Semiconductor Coalition will contribute valuable insights as we evaluate and refine this policy framework to further support Europe's ambitions in the semiconductor field.

Baden-Württemberg attracts imec to lead development of chiplet-based technology

New partnership enables an innovative network together with academia and industry partners to strengthen digital sovereignty in Europe.

IMEC and the State Government of Baden-Württemberg, Germany, have launched the Advanced Chip Design Accelerator (ACDA). The new imec competence center in Baden-Württemberg (Southwest of Germany) will develop state-of-the-art chiplet, packaging, system integration, sensing, and (edge) AI technology as part of imec's Automotive Chiplet Program (ACP). By adding this complementary expertise to imec's existing automotive R&D offering, the new competence center will be able to better support the local and international automotive industry in derisking and accelerating the introduction of automotive chiplets into manufacturing.

The Minister-Presidents of Baden-Württemberg and Flanders have already signed a Memorandum of Understanding (MoU) last year to intensify the cooperation in the field of microelectronics.

With the announcement today a big milestone has been reached in presence of Minister-President of Flanders Matthias Diependaele, Minister-President of Baden-Württemberg Winfried Kretschmann and representatives of academia and industry.

The Advanced Chip Design Accelerator is part of a chip-design strategy of the Federal State of Baden-Württemberg. The project is embedded in the European's Commission strategy to strengthen Europe's digital sovereignty.

The competence center is financially supported by Ministry of Economic Affairs, Labour and Tourism of Baden-Württemberg with 40 million euros, initially for a period of five years. It will be located at the Innovation Park Artificial Intelligence (IPAI) in Heilbronn, Germany.

The new center's objective responds to the emerging shift from traditional chip technologies towards chiplet-based compute architectures in automotive, a technology more suited to enabling demanding functionalities such as autonomous driving and enhanced in-cabin experience. Chiplets are modular chips specifically designed to perform specialized functions, facilitating rapid customization and upgrades, while reducing power consumption, development time and cost. The project also meets the strategic goal of the European Commission to launch the European Connected and Autonomous Vehicle Alliance.

Furthermore, the State of Baden-Württemberg will support the chip-ecosystem with an additional 5 million euros for a network office and the support for scientific cooperation on chiplet technologies, headed by the Fraunhofer-Gesellschaft.

Luc Van den hove, President and CEO of imec: "We are excited to bring our expertise and global partner network to the state of Baden-Württemberg, the cradle of the automotive industry in Germany. We also look forward to expanding our collaboration with Fraunhofer to leverage on our complementary expertise and lay the foundation for future chiplet solutions.

To realize the region's ambitions, we will also focus on growing the talent pipeline across Europe by training engineers in close collaboration with the local ecosystem, including universities. In addition, we aim to expand the developed high-performance computing solutions to the European level, thus contributing to the acceleration of innovation in the European automotive industry with unique and distinctive building blocks."

Minister-President of Baden-Württemberg, Winfried Kretschmann: "We are delighted to warmly welcome imec as a cutting-edge research institution with their new competence center in in Baden-Württemberg. As one of the most innovative regions in the world, with a strong automotive industry and with high expertise in AI, Baden-Württemberg and imec are a perfect match.

A big thank you also goes to the Flemish government - today is a milestone in our cooperation. And with our innovative partners like the Fraunhofer Institute, KIT (Karlsruher Institute of Technology), CyberValley or University of Stuttgart and many other partners from academia and industry, we are boosting innovation for the new generation of automotive chips made in Europe. Strengthening our core competencies in chips, software and AI is crucial for Europe's sovereignty."

Minister-President of Flanders Matthias Diependaele: "A Flemish legacy, a global future. Imec, with its roots in Flanders, has a globally strong reputation in digital technology. This international collaboration with Baden-Württemberg is essential to maintaining imec's technological leadership. The groundbreaking innovation that this research hub demonstrates in various application areas only further strengthens the economic fabric for both regions."

IDTechEx explores emerging applications for PICs

Photonic integrated circuits are the optical equivalent of microchips, using semiconductor industry processes to shrink many photonic components down onto a piece of material often smaller than a human fingernail, writes Sam Dale, Senior Technology Analyst at IDTechEx.

WITH PHOTONIC integrated circuits (PICs), functionality that would previously have required a laboratory-scale optical table can be shrunk to a usable scale and manufactured in high volumes.

As outlined in IDTechEx's recent report "Silicon Photonics and Photonic Integrated Circuits 2025-2035: Technologies, Market, Forecasts", data communications has fast become the "killer app" for PICs. PIC transceivers are fast becoming ubiquitous in data centers, where they increase the throughput of connections between nodes (individual computers) whilst reducing the physical size of transceivers, solving space issues for data center operators.

The ability of PICs to precisely manipulate light at the chip level opens the door to various cutting-edge fields beyond data communication, including sensing, LiDAR, quantum computing, and high-performance computing (HPC). While PIC-based transceivers are set to dominate the market, with long-range transceivers for 5G/6G networks forming the second largest sector of the overall market, other applications for PIC are growing steadily.

IDTechEx's ten-year photonic integrated circuit market forecast put non-communications applications at 7.7% of the overall market by 2035. Whilst this might seem like a small proportion, given IDTechEx's overall 2035 PIC market forecast of US$54.5 billion, this represents substantial opportunity.

PIC-Based sensors: Revolutionizing healthcare and environmental monitoring

One of the most promising applications of PICs lies in the field of sensors. PIC-based sensors leverage the ability of integrated photonics to detect minute changes in environmental parameters, making them invaluable for applications in healthcare, industrial monitoring, and environmental sensing.

Biosensing and Medical Diagnostics: PICs are already finding their way into point-of-care diagnostic devices, where they enhance the sensitivity and precision of biosensors. By integrating photonic waveguides, these sensors can detect biological markers, such as proteins or DNA sequences, with high specificity. This could revolutionize disease detection, enabling early-stage diagnosis and personalized medicine. Gas and Chemical Sensing: Industries such as oil and gas, manufacturing, and environmental science are exploring PIC-based gas sensors to detect trace elements in the atmosphere. Leveraging silicon nitride-based PICs, these sensors can function as highly sensitive "artificial noses" capable of identifying gases and pollutants at extremely low concentrations.

LiDAR and Photonic integrated circuits: Enabling the future of autonomous vehicles

Frequency-Modulated Continuous-Wave (FMCW) LiDAR systems are another emerging application where PICs offer substantial advantages. Traditional LiDAR systems rely on mechanical components to scan their surroundings, which introduces reliability issues and size constraints. PIC-based LiDAR, however, eliminates moving parts, making the systems more compact, robust, and energy-efficient.

PIC-enabled LiDAR is expected to play a crucial role in:

- **Autonomous Vehicles:** High-resolution, long-range detection with precise depth perception is crucial for self-driving cars. PIC-based LiDAR can provide enhanced accuracy in real-time mapping, enabling safer navigation.
- **Aerospace and Defense:** Compact, high-performance LiDAR systems are being developed for drones and military applications, where weight and reliability are critical factors.
- **Agriculture and Industrial Automation:** Beyond mobility, PIC-based LiDAR is being applied in smart farming, where it helps optimise planting and harvesting through high-precision land assessment.

Quantum computing and secure communications

Quantum technologies are another frontier where photonic integrated circuits are proving indispensable. As researchers push the boundaries of quantum computing, PICs provide a scalable and stable solution for controlling quantum states.

Trapped Ion and Photonic Quantum Computing: Quantum computers using trapped ions and photon-based qubits require precise control over light signals. PICs offer a way to miniaturize and stabilize these optical systems, making quantum computing more scalable.
Quantum Cryptography: Secure communication is becoming a pressing concern in the digital age. PICs enable the development of quantum key distribution (QKD) systems, which leverage the principles of quantum mechanics to create virtually unbreakable encryption methods.

Photonic accelerators for high-performance computing (HPC)

The ever-growing demand for computational power, driven by artificial intelligence (AI) and machine learning, has pushed the limits of traditional electronic computing. PICs provide a compelling alternative by enabling ultra-fast optical processing units (OPUs) that outperform traditional CPUs and GPUs in specific tasks.

Infineon bolsters global lead in automotive semiconductors

Infineon Technologies bolsters its global and regional market leadership positions in automotive semiconductors, including its very strong position in microcontrollers.

ACCORDING to the latest market research from TechInsights, Infineon achieved a market share of 13.5 percent in the global automotive semiconductor market in 2024. In Europe, the company climbed to the top spot with a 14.1 percent market share, up from second in 2023. Infineon also strengthened its presence in North America to the second largest market participant with a 10.4 percent share, rising from last year's number three position.

The global market share in microcontrollers rose again, to 32.0 percent, increasing the lead over the second-placed competitor by 2.7 percentage points.
Furthermore, Infineon maintained its leading market positions in the largest market for automotive semiconductors, China, with a 13.9 percent market share as well as in South Korea with a 17.7 percent market share. In Japan, the company confirmed its strong second place with a share of 13.2 percent. In total, the global automotive semiconductor market accounted for US$ 68.4 billion in 2024 – a slight decline of 1.2 percent compared to US$ 69.2 billion in 2023.

"We are the global number one in automotive semiconductors for the fifth consecutive year and we are equally successful across the world.

For the first time in our history, Infineon is among the top two automotive semiconductor companies in every region," said Peter Schaefer, Executive Vice President and Chief Sales Officer Automotive at Infineon. "This global success is a token of our strong product portfolio, outstanding customer support and our dedication to the specific needs of our customers."

Infineon's semiconductors are essential in driving the digitalization and decarbonization of vehicles to make them clean, safe and smart. They serve all major automotive applications such as driver assistance and safety systems, powertrain and battery management as well as comfort and infotainment features. A key focus is to support the evolution of electrical/electronic (E/E) vehicle architectures towards more centralized zonal designs as the basis for software-defined vehicles. This requires state-of-the-art connectivity and data security, smart power distribution and real-time computing power.

"It is the fifth time in a row that the 'TechInsights Automotive

Semiconductor Vendor Market Share Ranking' confirms the Infineon lead, with microcontrollers largely contributing to this success," said Asif Anwar, Executive Director of Automotive End Market Research at TechInsights.

"Semiconductors for advanced driver assistance systems, especially SoCs and memories, were among the best performing product categories.

Infineon did exceptionally well in microcontrollers used in advanced driver assistance systems and many other applications. With an increase of 3.6 percentage points to a 32.0 percent market share, Infineon has held up well in the automotive microcontroller market, which decreased by 8.2 percent year-over-year."

Zero Point Motion emerges from stealth

Bristol-based sensor technology startup, Zero Point Motion has successfully closed a £4million pre-Series A funding round to transform positioning and navigation.

THEY are backed by investors SCVC (the official funding arm of Science Creates), Foresight Group and Verve Ventures, with seed round investor u-blox AG remaining a key strategic partner and customer.

This investment fuels the company's rapid scale-up and team expansion as the company emerges from stealth mode, where they have been working on a scalable, volume-manufacturable process for Zero Point Motion's next-generation positioning and navigation sensors.

At the core of this innovation is a radical fusion of silicon photonics and micro-electro-mechanical systems (MEMS), inspired by Nobel Prize-winning gravitational wave detection principles. This cutting-edge approach enables low-cost, ultra-low noise, miniaturised accelerometers and gyroscopes that are 100x more sensitive than conventional MEMS sensors - delivering unprecedented performance and, crucially, resilience in environments where there is no GPS.

Zero Point Motion's breakthrough in motion sensing is set to transform defence, space exploration, and autonomous systems where precision and reliability are mission-critical. As navigation threats intensify, this technology would enable military operations to function accurately in contested environments – while in space exploration, where every mission is a high-value asset, inertial sensors are crucial for positioning and landing spacecraft. Closer to home, Zero Point Motion's sensors unlock new levels of autonomy in off-highway vehicles, drones, agritech and industrial applications, allowing seamless operation in tunnels, underground networks and other remote locations.

"Our mission is to harness light to redefine the future of sensing," says Dr Lia Li, founder and CEO of Zero Point Motion (pictured). "We're working with two of the world's leading foundries to push MEMS performance beyond its limits. With top-tier investors and partners behind us, we're laser-focused on delivering our inertial sensors to customers who demand the highest precision and reliability.

"We've also brought more integration and packaging R&D in-house, cutting iteration times from eight weeks to just one day. This agility, combined with our expanding patent portfolio and multiple newly granted patents—ensures we stay ahead of the curve. Our next milestone: product qualification and customer deployment."

u-blox AG cofounder and executive director, Andreas Thiel adds: "While satellite positioning technology delivers the highest accuracies in open environments, sensor-based dead reckoning is crucial for resilient performance in dense and obstructed urban scenarios. u-blox is known for its advanced positioning and wireless communication technologies, and we see significant potential in Zero Point Motion's innovative sensor technology. By investing in Zero Point Motion, u-blox can integrate these cutting-edge sensors into our own product offerings, further strengthening our market position and expanding our technological capabilities."

Recognized as one of Sifted's '16 Bristol-based Startups to Watch', Zero Point Motion has also secured major government and EU funding, including £1.3M from the UK's Centre for Connected and Autonomous Vehicles (CCAV) in 2023, followed by a €2.4M grant from the European Innovation Council Accelerator program.

Chris Wiles, director, Foresight's Ventures team, says: "Foresight initially invested in Zero Point Motion in 2021 to help Lia and the founding team bring this breakthrough sensing technology into the public domain. We are encouraged by the progress the team has made and the growing market need for accurate navigation and positioning in challenging environments. We are delighted to support the business in this recent funding round and welcome SCVC onboard." Harry Destecroix MBE, founder of Science Creates, and cofounder/ managing partner of SCVC, says: "We're thrilled to back Zero Point Motion as they develop a truly category-defining technology. By applying cutting-edge quantum approaches to motion sensing, Lia and the team are unlocking massive potential for industries like autonomous vehicles, robotics, and consumer electronics.

"Lia is an exceptional founder—her technical brilliance, vision, and leadership make her exactly the kind of entrepreneur we love to support. This is also a great fit for our partner John Williams, who led the deal and will be working closely with the company. With his experience building Kudan, he knows first-hand the challenges in this space and how transformative Zero Point Motion's technology could be. We can't wait to see what they achieve."

With this funding and industry validation, Zero Point Motion is now scaling to set a new global standard in precision motion sensing—delivering breakthrough performance and accelerating autonomy in a GPS-challenged world.

UMC unveils new fab facility in Singapore

New 22nm fab to be one of the most advanced semiconductor manufacturing facilities in Singapore and is set to create approximately 700 new jobs.

UNITED Microelectronics Corporation (UMC), a leading global semiconductor foundry, has officially unveiled its new fab facility in Singapore in a grand opening ceremony. The first phase of the new facility will start volume production in 2026, bringing UMC's total production capacity in Singapore to more than 1 million wafers annually. It will also be one of the most advanced semiconductor foundries in Singapore, manufacturing semiconductors to enable communications, Internet of Things (IoT), automotive, and AI innovations.

The ceremony was attended by Deputy Prime Minister and Minister for Trade and Industry of Singapore Gan Kim Yong, Senior Minister and Coordinating Minister for National Security of Singapore Teo Chee Hean, Permanent Secretary of Singapore's Ministry of Trade and Industry Beh Swan Gin, Managing Director of the Singapore Economic Development Board (EDB) Jermaine Loy, and JTC Assistant Chief Executive Officer Christine Wong.

The facility, a greenfield expansion adjacent to UMC's existing fab in the Pasir Ris Wafer Fab Park, spans two phases. Up to US$5 billion will be invested to bring the first phase to full capacity of 30,000 wafers per month, with room for further investment in a second phase expansion in the future. The new facility is equipped for manufacturing with UMC's industry-leading 22nm and 28nm solutions – the most advanced foundry processes currently in Singapore's semiconductor sector – for global customers' products including premium smartphone display chips, power-efficient memory chips for IoT devices, and next-generation connectivity chips. The expansion is expected to create approximately 700 jobs locally over the next few years, including process and equipment engineers as well as research and development engineers.

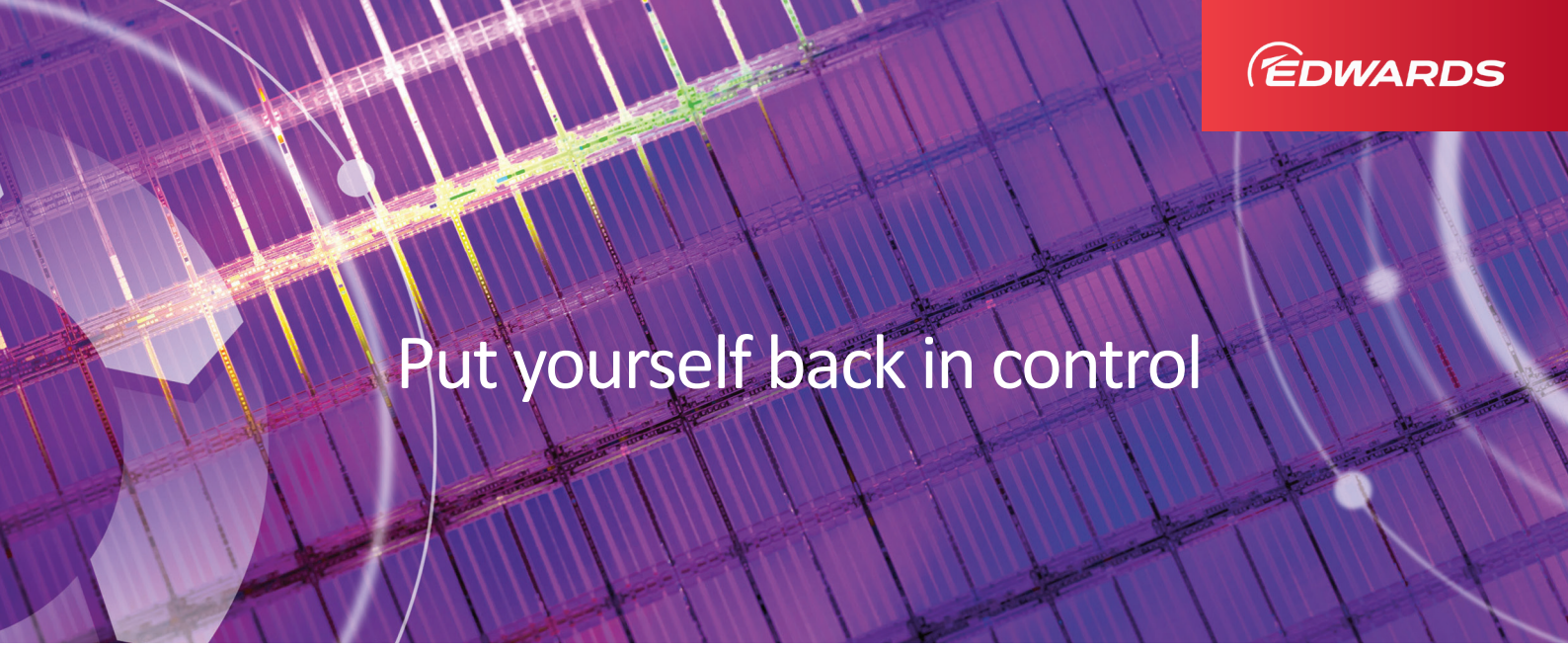
"This new state-of-the-art facility in Singapore signals a new phase of growth for UMC. It enhances our ability to meet future chip demand, driven by continuous innovations in connectivity, automotive, and AI," said SC Chien, President of UMC. "The unique geography of Singapore also makes the new facility well placed to support our customers in strengthening supply chain resilience. This fab expansion closely aligns with the Singapore government's vision to become a leading advanced manufacturing hub, and we are deeply grateful for their support."

This fab expansion closely aligns with the Singapore government's vision to become a leading advanced manufacturing hub, and we are deeply grateful for their support

"We welcome UMC's expansion in Singapore. This new fab introduces new leading edge specialty semiconductor capabilities and production capacity that will enhance Singapore's competitiveness as a critical node in the global semiconductor supply chain.

This significant investment underscores our long-standing partnership with UMC, and we look forward to deepening our collaboration to strengthen Singapore's semiconductor ecosystem," said Jermaine Loy, Managing Director of the Singapore Economic Development Board.

The new facility was built according to rigorous sustainability standards, and has obtained the Green Mark GoldPlus certification from Singapore's Building and Construction Authority. A standard part of all UMC's new fab designs to align with UMC's goal to be 100% powered by renewable energy by 2050, the new facility will be installed with 17,949 square meters of solar panels on its rooftop. In addition to the manufacturing site, the expansion also includes a brand-new office building, a full-sized multipurpose sports hall, and other amenities for employees and community members to enjoy.



Put yourself back in control

Are unplanned dowtimes dragging down your productivity? Is your Fab efficiency and TCoO being damaged by avoidable stoppages? Avoidable? How? By working with us to implement one of our core service plans you can take back control of your throughput and manage equipment with a planned service regime. Talk to us today and head towards a more productive future.

Care Spare parts plan	Maintain Parts and labour for standard maintenance	Perform Standard maintenance with upgrades included
One single purchase order and monthly billing	One single purchase order and monthly billing	One single purchase order and monthly billing
Fixed supply of parts for standard maintenance used on site annually	Preventative and routine maintenance activities, including parts and labour required for each activity	Preventative and routine maintenance activities, including parts and labour required for each activity
Basic operational support provided by our team of experts	Maintenance performed on site by our field service team for Abatement, or at our Service Technology Centres for Dry, Turbo, and Cryogenic Pumps	Maintenance performed on site by our field service team for Abatement, or at our Service Technology Centres for Dry, Turbo, and Cryogenic Pumps
The plan can be enhanced with chargeable options at additional cost, including training and troubleshooting by our service teams	Troubleshooting and operational support provided by our team of experts	Troubleshooting and operational support provided by our team of experts
	The plan can be enhanced with chargeable options at additional cost, including service exchange, upgrades, and inventory management	Can include specific upgrades or improvement components according to the contract.
		Possible to customise the plan with additional options

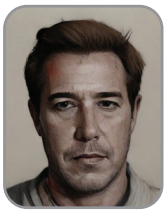
Edwards semiconductor *Intelligent* service

View our range of service plans at www.edwardsvacuum.com

Advanced fabs require more innovative facility services for efficiency, reliability and resiliency

Today's fabs are highly complex environments that demand precision, reliability, and real-time adaptability. Industry success will depend on a stable workforce with specialised skills, a keen eye on processes and efficiencies, and a commitment to embracing innovative facility management partners and solutions.

BY JOSEPH CESTARI, VICE PRESIDENT, SEMICONDUCTOR OPERATIONS AND NEHA DHINGRA, VICE PRESIDENT, SEMICONDUCTOR STRATEGY AT ABM



THE U.S. domestic semiconductor manufacturing is fueled by record-high investment and federal incentives like the CHIPS and Science Act. The manufacturing capacity is poised for a massive expansion in the United States.

According to the Semiconductor Industry Association (SIA), U.S. fab capacity will triple its domestic semiconductor manufacturing capacity in the next decade.

Nonetheless, this manufacturing resurgence faces some significant obstacles. Many facilities need to be built from the ground up, which requires highly specialized skills and training – from pipe fitters to plumbers, electricians, and welders all the way to equipment installation as well as operation and maintenance.

Once up-and-running, keeping these fabs operating at peak efficiency while meeting stringent quality, safety, and environmental standards brings a unique set of challenges. Managing them is a monumental task due to the complexity of the processes, the precision required, and the scale of operations involved. As processes continue to advance (toward 3nm, 2nm nodes), the margin for error drops even further. Tiny deviations in temperature, pressure, or chemical composition during manufacturing can lead to systemic failures, especially with cutting-edge technology like Extreme Ultraviolet (EUV) lithography.

These complex facilities require highly specialized cleaning and facility management solutions, a push toward more digitization, and sustained investment in workforce development.

Impact of facility downtime

Semiconductor facility outages can stem from a myriad of issues from power disruptions, equipment failures, human error and — as evidenced during the pandemic – supply chain shortages.

An unplanned outage lasting 4 hours in a leading-edge fab could cost anywhere from $833,000 to $3.3 million (a massive $3,472 per minute). This means a full day could range from an astounding $5 million to $20 million. Smaller or older facilities producing less advanced chips might see lower costs but can still reach upwards of $500,000 to $2 million per day.

While the actual cost may fluctuate based on the facility's output value and product type, one thing is certain. Any downtown is unquestionably costly. To further complicate matters, finished products can also fail after shipment due to contamination or inconsistent processing leading to costly recalls or even injury to consumer leading to huge fines and penalties, forced work stoppages, lost profit from returned goods, or costly lawsuits.

The clean continuum

Cleanrooms must have one consistent goal – keep contaminants out and remove what's generated inside. This requires a "clean continuum" of establishing, certifying and sustaining the necessary environment. This meticulous process – leverages a combination of competencies of specialized controlled environment cleaning as well as particulate measurement, air flow test and balance, and compliance certification to standards.

A breached filter, a leak in a material supply line, or a careless tech can lead to contamination and yield loss. And a single particle significantly smaller than a micron (one-hundredth the width of a human hair) can ruin an entire wafer.

ISO standards provide the framework necessary to maintain these sterile conditions, defining acceptable particle levels in the air and establishing guidelines. Contamination control from Class 1 to 10,000 scales with particle limits, airflow rigor, and procedural stringency. The primary contaminants are airborne contaminants (dust, microbes, aerosols) introduced by personnel, equipment, materials, or processes. Each step up in cleanliness amplifies the challenge and the stakes.

Managing particular problems

Air pollution, dirt and dust, ferrous metal particles, human hair, skin particles — just to name a few — all must be kept at bay. It's also important to remember that all operations and systems are interconnected and affect each other. Particulates in HVAC systems can increase cooling energy costs. Airborne gases can lead to corrosion and failures. Particles and build up can interfere with critical equipment and cause failures.

Contamination from humans such as skin flakes, hair, and breath can be a major source. A single uncovered cough in Class 1 can undo hours of filtration.

The good news is this type of contamination is mitigated with upgraded contamination and control procedures including entry, gowning and air showers. Strict SOPs must be adhered to within the overall clean environments – encompassing both routine cleaning along with "after action cleaning" such as tool installation or servicing.

Air filtration, flow and exhaust are also critical within these complex environments. A rigorous preventative maintenance schedule is essential to maintain the necessary unidirectional flow critical for Class 1-100.

Digitisation of facility management

Digitising facility services involves leveraging advanced technologies to optimize operations, enhance efficiency, and ensure the stringent conditions required for semiconductor manufacturing are consistently met. It can transform facility services in key areas such as automation, data integration, and environmental control.

Semiconductor fabs generate massive amounts of data from equipment, environmental controls, and production processes. Digitizing facility services means harnessing this data for actionable insights. A data intelligence platform, such as ABM Connect™, can streamline and display analytics tailored for immediate answers to questions. With an integrated IoT hub for visibility and task validation, examples of front-line team data can include:

- Work completion against planned routes
- Quality performance & inspections
- Recognition patterns & performance trends
- Training compliance
- Safe workplace observations

This technology allows greater accuracy and efficiency with real real-time actionable metrics, robust reporting, and up-to-date KPIs.

In highly regulated industries like semiconductor manufacturing, the solution can help meet compliance and audit challenges, while enabling continuous improvement.

Incorporating predictive maintenance

As innovation on the fab floor increases, tech-based solutions can be applied to equipment maintenance. Predictive maintenance (PdM) offers the promise of transforming semiconductor fabs by shifting from reactive or scheduled maintenance to a data-driven, just-in-time approach.

Highly specialized, expensive tools like photolithography machines, etchers, and deposition systems are prone to breakdowns. A laser misfire in an EUV system or a vacuum pump failure can stop a line. Leveraging a PdM model can minimise

disruptions and extend the life of equipment. It's basically the difference between changing a specific part on a sensible schedule and knowing when it is optimal for operations and lifecycle costs.

Real-time monitoring can be achieved with connected sensors. Wireless and wired sensors (along with AI) can monitor for conditions and report to a centralized information system. These types of sensors can be used to monitor key assets such as:

- **Heat Monitoring -** Detects heat caused by insulation issues or conduction problem so you can act before discharge events or arc faults.
- **Partial Discharge Monitoring -** Partial discharge usually isn't visible, but it destroys insulation over time, which will cause a full and destructive discharge.
- **Circuit Monitoring -** Measures power and power quality data, including harmonic disturbance in the wave forms and voltage transients (sags and swells) that can damage to sensitive equipment.

This data is then analyzed using AI and machine learning algorithms to detect patterns or anomalies that signal impending failures. For example, a spike in vibration levels in a pump could indicate wear and prompt preemptive action. Recording this type of data over time gives you the ability to identify asset anomalies and provide advance warnings of equipment failures before they occur. Where just-in-time maintenance strategies have been implemented, the result typically is higher overall equipment efficiency. According to Nucleus Research, PdM initiatives can reduce downtime by between 35 and 50 percent, extend asset lifespan by between 20 and 40 percent, lower costs, improve safety, and enhance product quality.

Yet, effective implementation is not without challenges. Success relies on high-quality, accessible data, and integration with existing systems. It is also critical to define the right parameters for failure prediction models. And as with any connected system, robust security measures are needed to protect sensitive production data. However new solutions are making the process easier and scalable across facilities. An experienced team with the right skillset can help implement PdM to enhance efficiency, reduce costs, and maintain product quality.

Power resilience

Semiconductor fabs are energy-intensive, consuming vast amounts of electricity and water for cooling, processing, and cleanroom operations. They also demand uninterrupted, ultra-stable electricity – with 24/7 uptime with zero flicker. Even a millisecond-long outage can disrupt processes like etching or doping, ruining wafers mid-process.

Yet, the U.S. electric grid is under strain. Projections indicate that the demand for electricity will surge by 50% during the next two decades, with no signs of slowing down. According to Grid Strategies, the U.S. electric grid is not prepared for this level of significant load growth. This poses a key risk for reliability, and could have detrimental effects on fabs, particularly in more drought prone or high-cost areas.

On the bright side, new methods of energy management are now available to increase energy reliability and resiliency. Localized power grids (or microgrids) can provide a decentralized approach to energy distribution to bolster on-site energy capacity, avoid high-cost, peak timeframes, and ensure power resiliency.

In the simplest terms, a microgrid is a local collection of distributed energy resources that also can interact with the broader electrical grid to provide peak load shaving and system resiliency. This autonomy enhances resilience, energy security, and efficiency. Thanks to increased affordability and shifting regulations, more of these microgrids are being powered by renewable energy methods.

What makes a microgrid "intelligent" is the set of control systems that can manage, store, charge, and discharge the entire system at any given time. These controls can be programmed to monitor the supply versus demand of power being pulled from the central grid and the real-time cost of power on the market.

While monitoring, if the control system detects low energy prices, it can switch to purchasing power from the grid to supplement the consumer's needs while using battery systems to store self-generated power from solar panels for future use. Subsequently, the controller can discharge these batteries when prices increase, ensuring more stable energy costs. The system can also operate autonomously, ensuring an uninterrupted power supply even during grid outages or disruptions. This level of real-time energy management improves the energy performance, control costs and increases predictability.

Skilled workforce

The SIA predicts that by 2030, there will be a shortage of approximately 67,000 skilled engineers and technicians in the industry. In addition, a third of the workforce is nearing retirement. More extensive training, upskilling and sustained workforce development is urgently needed. The good news is that many of these roles do not require a four-year degree. Rather, they can be fulfilled with a certification or 2-year training program.

Industry stakeholders must look to develop a national training structure, utilizing government funding and industry momentum to build critical in-house expertise. In the meantime, embracing outsourcing may be the answer to expand the labor pipeline as demand for skilled labor outpaces supply. This is particularly true if the outsourcing partner has in-depth expertise working within these highly specialized and complex environments. Facilities management partners can help fill talent gaps in construction, operations, and maintenance, provide valuable tribal knowledge, and help ensure safety and quality. Leveraging these types of experts may hold the key to revitalization of the U.S. manufacturing industry.

Today's fabs are highly complex environments that demand precision, reliability, and real-time adaptability. Industry success will depend on a stable workforce with specialized skills, a keen eye on processes and efficiencies, and a commitment to embracing innovative facility management partners and solutions.

Why the global semiconductor industry needs SEMI EDA standards

By improving data throughput and seamlessly integrating with modern analytics and artificial intelligence-driven solutions, standards enable real-time process optimisation, predictive maintenance, and more adaptive manufacturing operations.

BY DR. FAHAD GOLRA, DIRECTOR OF PRODUCT INNOVATION, AGILEO AUTOMATION

SINCE THE development of SEMI Equipment Communications Standard 1 (SECS-I) in the early 1980s, SEMI has continually advanced the standardization of semiconductor manufacturing. SECS-I laid the groundwork for communication between semiconductor manufacturing equipment and factory systems.

Over the years, SEMI has expanded its portfolio with SECS-II, GEM (Generic Equipment Model), and the GEM300 standards suite. These standards provide a common language for communication, data exchange, and control between shop-floor equipment and IT systems. By standardizing these interactions, SEMI has enabled seamless integration of equipment from multiple vendors, an essential requirement in wafer fabrication facilities. SEMI standards now underpin key activities such as equipment communication, process control, material management, and data collection.

The evolution from SECS/GEM to EDA

More recently, SEMI introduced Equipment Data Acquisition (EDA), often referred to as Interface A, to expand its standards suite and address the semiconductor industry's increasingly diverse and complex needs. EDA standards facilitate and streamline communication between a factory's data collection applications and manufacturing equipment.

The evolution from SECS/GEM to GEM300 and now EDA is a natural progression that reflects the increasing complexity of semiconductor manufacturing. The original SECS/GEM standards established a robust framework for equipment-to-host communication and standardized equipment behavior, enabling reliable interactions and laying the foundation for automation. With the move from 200mm to 300mm wafers, GEM300 was introduced to address higher throughput requirements and advanced process control. Building on SECS/GEM, GEM300 added features such as job management, automated material handling, and material tracking that were critical to support larger wafers and increased production volumes.

As industry scaled up, the importance of data collection and utilization became paramount. The EDA (Interface A) suite emerged as a solution for high-speed, high-volume data acquisition. Complementing SECS/GEM and GEM300, EDA enables real-time data analysis, process optimization, and predictive maintenance which are vital for data-driven manufacturing.

Together, SECS/GEM, GEM300, and EDA provide a comprehensive roadmap for improving efficiency,

yield, and quality control. This evolution ensures that semiconductor fabs remain competitive, highly automated, and ready to innovate in an ever-evolving market.

Leveraging equipment data for fab efficiency

Modern semiconductor equipment generates large volumes of real-time data that underpin a wide range of critical applications, including:

- **Run-to-run control (R2R):** Dynamically adjusts equipment settings to maintain consistent output quality between production runs.
- **Fault detection and classification (FDC):** Monitors data to detect and classify anomalies, preventing defects.
- **Virtual metrology:** Predicts process parameters using sensor data, reducing the need for physical measurements and improving throughput.
- **Condition monitoring:** Analyses equipment and sensor data to predict and prevent failures, minimizing unexpected downtime.
- **Data analysis:** Identifies patterns and trends to optimize processes, improve yields, and increase overall efficiency.

These data-driven applications illustrate the transformative impact of harnessing equipment data. By implementing robust data collection standards, fabs can operate with greater agility, solve problems proactively, and continually refine their processes to stay competitive.

EDA standards

As Moore's Law continues to drive higher transistor densities, semiconductor manufacturing processes have become more complex. The EDA suite provides standardized data structures, formats, and protocols to enable the efficient data exchange between sophisticated equipment and IT systems. Building on earlier SEMI standards, EDA adds capabilities for managing high-speed, high-volume data.

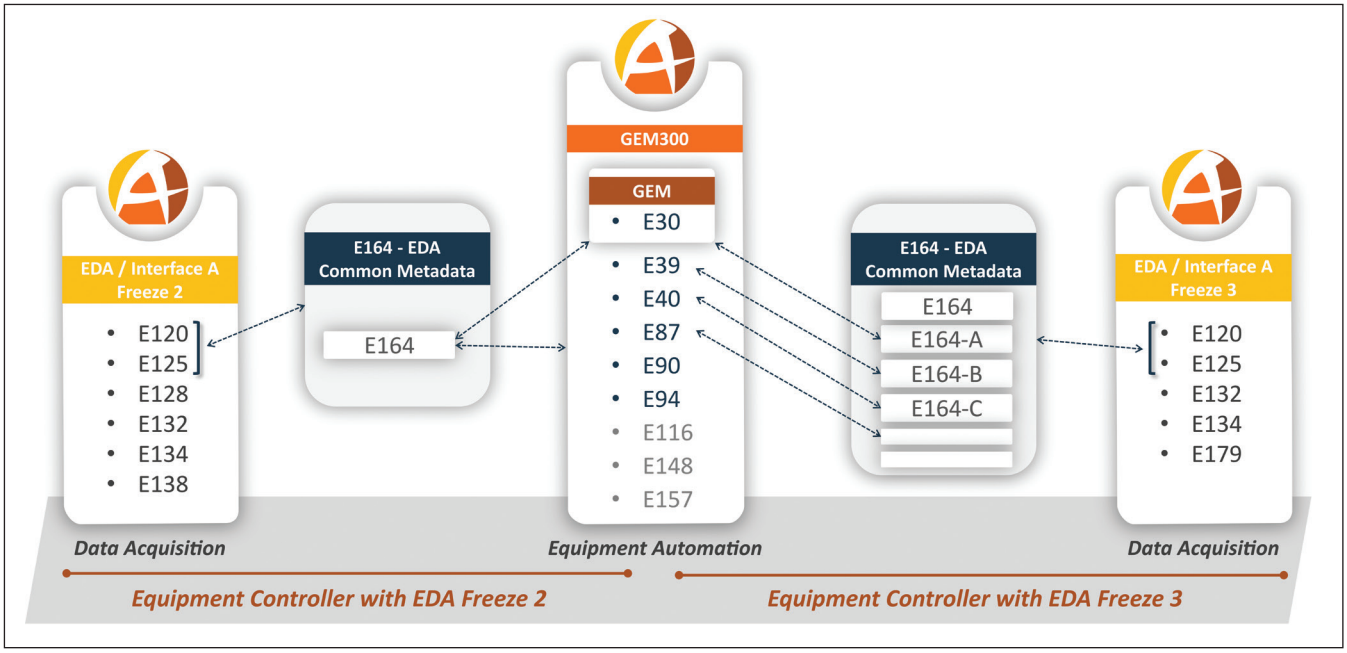
These standards address several critical capabilities such as equipment structure, communication, security, data modeling, and collection planning to enable fabs to gain actionable insights both securely and efficiently.

SEMI E164 bridges EDA and GEM/GEM300 by hierarchically modeling equipment metadata and enabling standardized access to equipment states, regardless of the underlying protocols. This integration ensures seamless data collection from increasingly complex, automated equipment.

The role of freezes

The concept of a "freeze" stabilizes SEMI standards by designating mature, reliable versions that collectively form the standards suite. SEMI E178 governs freeze versions for EDA, with Freeze 2 serving as the current stable framework for high-speed, high-volume data acquisition. As part of the ongoing evolution, the industry is preparing for Freeze 3, which will introduce support for HTTP/2, gRPC, and protocol buffers, among other enhancements.

A key element of Freeze 3 is SEMI E179, the specification for Protocol Buffers Common Components. This standard establishes a unified approach to representing errors, data types, data value types, units, and operators through protocol buffers. It will replace SEMI E138 and SEMI E128 in Freeze 3, moving the industry from XML-based structures to next-generation data exchange formats. While Freeze 3 continues to evolve, SEMI EDA Freeze 2 remains a reliable, proven standard that drives data acquisition and integration in today's semiconductor manufacturing. This evolution underscores the industry's commitment



➤ EDA Freeze 2 & 3 standards suite mapped to GEM/ GEM300 standards

STANDARD	DESCRIPTION
SEMI E120 – Common Equipment Model (CEM)	It provides a unified high-level structure for equipment.
SEMI E125 – Equipment Self-Description (EqSD)	It standardises how equipment capabilities and operational states are presented.
SEMI E128 – Specification for XML Message Structures	It defines XML-based message structures for consistent data exchange.
SEMI E132 – Specification for Equipment Client Authentication and Authorisation	It addresses session management and standardises authentication and authoriszation for secure data access.
SEMI E134 – Specification for Data Collection Management	It outlines the process for planning, managing, and executing data collection.
SEMI E138 – XML Semiconductor Common Components (Freeze 2 only)	It provides XML components tailored for semiconductor communication.
SEMI E179 – Protocol Buffers Common Components (Freeze 3 only)	It specifies a standardized approach to representing errors, data types, data value types, units, and operators through protocol buffers.

to embracing cutting-edge technologies for data-driven semiconductor manufacturing.

With each new process node and the growing adoption of advanced packaging techniques, the global semiconductor industry faces a steep increase in data complexity. With the upcoming Freeze 3 enhancements such as HTTP/2, gRPC, and protocol buffers, SEMI EDA standards are positioned to more efficiently handle these increasing data demands. By improving data throughput and seamlessly integrating with modern analytics and artificial intelligence-driven solutions, these standards enable real-time process optimization, predictive maintenance, and more adaptive manufacturing operations.

Fabs that embrace this evolution will realize superior yields, faster innovation cycles, and a sustainable competitive advantage in an ever-accelerating market.

Dr. Fahad Golra is Director of Product Innovation at Agileo Automation, a French firm specializing in equipment connectivity, control, and supervision solutions for the global semiconductor manufacturing industry. Since joining in 2019, he has driven practical innovations in connectivity technologies, data modeling, and communication architectures. Actively involved in SEMI and the OPC Foundation, Dr. Golra advocates Industry 4.0 adoption, focusing on interoperability, digital twins, and edge-to-cloud architectures. Over his 15-year career, he has served in academia, research, and industry. He is a recognized speaker at global semiconductor events and an accomplished author of conference papers and articles, contributing extensively to the field's ongoing evolution.

semi™

Connecting Semiconductors and Electronics

About SEMI:
SEMI connects more than 2,500 member companies and 1.3 million professionals worldwide to advance the technology and business of electronics design and manufacturing. The breadth and depth of our events, programs and services help members accelerate innovation and collaboration on the toughest challenges to growth.

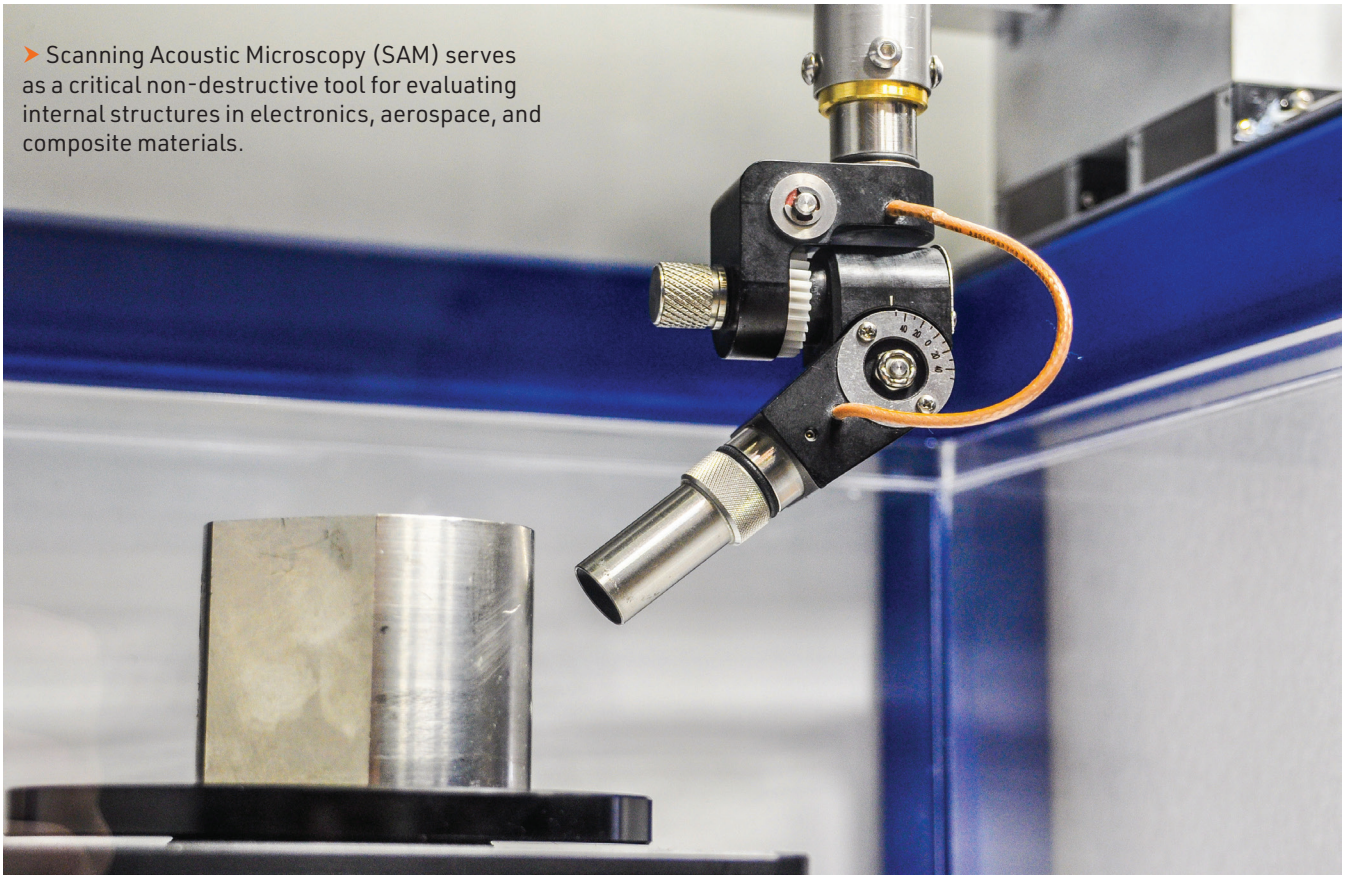
ESDA Electronic System Design Alliance

FlexTech

FOA Fab Owners Alliance

MEMS & SENSORS INDUSTRY GROUP®

SOI Industry Consortium



➤ Scanning Acoustic Microscopy (SAM) serves as a critical non-destructive tool for evaluating internal structures in electronics, aerospace, and composite materials.

The power trio behind superior SAM performance

Selecting and integrating the right transducers, digitizers, and software drives superior Scanning Acoustic Microscopy quality control

BY DEL WILLIAMS A TECHNICAL WRITER BASED IN TORRANCE, CALIFORNIA

FOR MANUFACTURERS in electronics, aerospace, and advanced materials like metals, alloys, and composites, Scanning Acoustic Microscopy (SAM) offers a powerful quality control tool, ensuring structural integrity, reliability, and performance—all without damaging a single component. SAM uses high-frequency ultrasound to inspect and characterize internal features of materials, detecting cracks, voids, inclusions, and delaminations that could compromise performance.

SAM is a powerful non-invasive and non-destructive method for inspecting internal structures in optically opaque materials. Depth-specific information can be extracted and applied to create two- and three-dimensional images without the need for time-consuming tomographic scan procedures and more costly X-rays.

Today, SAM facilitates the detection of much smaller defects than previously possible.

“Advanced, phased array SAM systems make it possible to move to a higher level of failure analysis because of the level of detection and precision involved. In the past, detecting a 500-micron defect was the goal; now it is a 50-micron defect. With this type of testing, we can inspect materials and discover flaws that were previously undetected,” said Hari Polu, President of OKOS, a Virginia-based manufacturer of industrial SAM ultrasonic non-destructive testing systems. The company serves the electronics manufacturing, aerospace, and metal/alloy/composite manufacturers, and end-user markets.

For electronics manufacturers, SAM is indispensable for inspecting microchips, bonded wafers, and underfills, where failure is not an option. Aerospace firms rely on it to identify subsurface flaws in lightweight composites or high-performance alloys, ensuring safety in flight-critical applications. In metals and composites, it verifies adhesion quality and detects fatigue or internal corrosion early, saving money and lives.

However, to unlock the full power of SAM, manufacturers need the right system. Toward this

goal, the most effective SAM systems are built on a triumvirate of high-performance components: transducers, digitizers, and software.

Optimizing SAM with Critical Components
Polu explains how transducers, digitizers, and software seamlessly work together in Scanning Acoustic Microscopy to benefit manufacturers.

"Transducers generate and receive the ultrasound signals, acting as the system's 'eyes.' Digitizers convert high-frequency acoustic signals into precise digital data for analysis. Software brings it all together, enabling real-time visualization, defect identification, and actionable reporting. When these three elements work in harmony, SAM becomes more than a quality control step—it becomes a competitive advantage," says Polu.

Transducers

A Scanning Acoustic Microscope operates by utilizing a transducer that converts electrical energy into highly focused, ultrahigh-frequency sound waves. These waves are directed to a precise point on the target object, enabling internal inspection with exceptional accuracy. The shape of the transducer's lens and the frequency of the sound waves determine both the focal length and the resolution of the scan.

As the sound waves interact with the internal features of the material, they reflect back to the transducer, which then converts the returning acoustic signals into voltage. This returning analog signal is subsequently amplified by a pulser/receiver and digitized for further analysis. All ultrasonic scanning systems rely on this essential dual function—signal generation and detection via at least one transducer—to perform precise, non-destructive evaluations of internal structures.

Transducers come in a variety of sizes and shapes for different applications. Some require direct contact with a material to operate; others use an air gap or are immersed in a fluid, usually water, in order to better transmit the sound wave through a material. OKOS offers a large variety of transducers up to 300 MHz for different applications and can custom engineer transducers for specific applications to suit specific needs.

According to Polu, the OEM offers four general types of transducers (Epoxy, PVDF, Delay Line, Phased Array), each of which has advantages for certain applications:

Epoxy tipped transducers tend to be less than 30 MHz and are useful for imaging thick samples or samples with very attenuative material. These often have the largest focal lengths.

PVDF transducers use a gold-tipped exposed element for high-frequency imaging, operating between 35 MHz and 75 MHz. These are ideal for thin, attenuative materials like silicon-based chips. Focal lengths typically range from 0.25 to 1.5 inches, enabling precise internal inspection.

Delay Line transducers are quartz lens tipped transducers with internal crystals manufactured to a precise thickness to control frequency. These transducers can range from 35 MHz to 300 MHz, have the best depth of field, and can have custom focal lengths.

Phased array transducers use multiple elements, unlike the single-element design of standard types, and can be curved to improve scanning over contoured surfaces. Multiple elements sweep the sample simultaneously, enabling faster scans. Constructive interference allows real-time focal length adjustment for optimal imaging. These transducers typically operate at 20 MHz or below.

Multiple transducers speed scanning

Unlike conventional Scanning Acoustic Microscopy systems that utilize a single-element transducer, phased array systems employ multiple transducers that can be combined to scan the sample simultaneously.

In a phased array system, multiple elements can be activated either simultaneously or sequentially to synthesize a focused acoustic beam. The number of transducer elements incorporated into the array varies significantly depending on the specific application and system design. Common configurations typically include arrays with 16, 32, 64, 128, or 256 elements.

"A conventional 5 MHz sensor could take up to 45 minutes to inspect an 8–10-inch square or disc alloy. Today, however, an advanced phased array with 64-128 sensors and innovative software to render the images can reduce inspection time to five minutes, with more granular detection of small impurities or defects," says Polu.

A phased array scanning system consists of multiple ultrasound transducer elements arranged in an array. Each element within the array is independently controlled with respect to the timing (phase) and amplitude of excitation. This configuration allows for electronic steering and

➤ The effectiveness of SAM depends on the strategic integration of three core components: transducers, digitizers, and software.

➤ Each component must be selected and calibrated according to the specific demands of the application to maximize system performance.

focusing of the ultrasound beam by adjusting the timing and amplitude applied to each element.

Phased array SAM systems offer significant advantages for applications that demand high-throughput inspection. These systems are particularly well-suited for non-destructive evaluation of composites, bonded structures, and electronic assemblies. They also support real-time imaging with adjustable depth of focus, which enhances their effectiveness in assessing internal features at various depths within the material.

"To produce an image, samples are scanned point by point and line by line," explains Hari. "Scanning modes range from single layer views to tray scans and cross-sections. Multi-layer scans can include up to 50 independent layers. Depth-specific information can be extracted and applied to create two-and three-dimensional images without the need for time-consuming tomographic scan procedures or costly X-ray equipment. The images are then analyzed to detect and characterize flaws such as cracks, inclusions, and voids."

According to Polu, SAM can also be custom designed to be fully integrated into high volume manufacturing systems. When high throughput is required for 100% inspection, ultra-fast single or dual gantry scanning systems are utilized along with 128 transducers for phased array scanning.

Digitizers

In a Scanning Acoustic Microscope, the digitizer takes the analog voltage signals received from the transducer—after amplification by the pulser/receiver—and converts them into digital format. This digital data is then used for image reconstruction and analysis, enabling accurate visualization of the internal features of the inspected object. The digitizer is critical for translating raw acoustic information into usable, high-resolution imaging.

Digitizers convert analog signals into digital form by sampling the input waveform at specific intervals, known as the sampling rate. A higher sampling rate captures more data points per second, allowing for a more accurate reconstruction of the original signal. To avoid distortion and preserve signal integrity, the sampling rate usually must be at least twice the highest frequency present in the signal, according to Polu.

"More data is generated as the sampling rate is increased, so the lowest sampling rate that can accurately reproduce the original signal will improve throughput," says Polu.

Software

Software coordinates all the pieces of an ultrasonic scanning system like SAM. It interacts with the digitizer, motion control, and digital pulser/receivers in order to coordinate their operations. Software is used to adjust the position of the sample or the probe (transducer) in three-dimensional space, trigger the transducer, and process the resulting waveform data into 2D and 3D images.

As important as the physical and mechanical aspects of conducting a scan, the software is critical to improving the resolution and analyzing the information to produce detailed scans.

Multi-axis scan options enable A, B, and C-scans, contour following, off-line analysis, and virtual rescanning for a variety of materials. This results in highly accurate internal and external inspection for defects and thickness measurement via the inspection software.

Various software modes can be simple and user friendly, advanced for detailed analysis, or automated for production scanning. An off-line analysis mode is also available for virtual scanning.

Polu estimates that OKOS' software-driven model enables them to drive down the costs of SAM testing while delivering the same quality of inspection results. Consequently, this type of equipment is well within reach of even modest testing labs.

The Bottom Line

In Scanning Acoustic Microscopy, performance depends not solely on the quality of individual components but on their effective integration.

Scanning Acoustic Microscopy achieves peak effectiveness when transducers, digitizers, and software operate in seamless coordination. Performance depends not only on the quality of individual components, but on how well they are integrated as a unified system.

When properly matched, these elements enable higher scanning speeds, enhanced defect detection at smaller scales, and improved imaging clarity. This level of performance allows manufacturers to identify issues early, enhance product quality, and maintain a competitive edge in industries where minor defects can result in significant consequences.

SIS ROUNDTABLE

Connecting Leaders & Experts in the Silicon Semiconductor Field

Not every discussion is a **heated debate...**

- Based around a hot topic for your company, this 60-minute recorded, moderated ZOOM roundtable would be a platform for debate and discussion
- Moderated by an editor, Phil Alsop, this can include 3 speakers
- Questions prepared and shared in advance
- There would be an opportunity to view and edit out any unflattering bloopers

This event would be publicised for 4 weeks through all our mediums including:

- A banner on the Silicon Semiconductor homepage for 8 weeks
- 4x weekly dedicated HTMLs
- 4x news pieces which would also appear on the weekly e-newsletters
- Promoted through our social media platforms for 8 weeks (pre and post event)
- Available as an on-demand asset through all mediums
- All registered attendees' details would be made available to you

Cost: €5995

Contact: Jackie Cannon at jackie.cannon@angelbc.com

ANGEL EVENTS

The future of defence communications

How mmWave RF and beamforming are transforming the battlefield

BY DR. VICKRAM VATHULYA, CEO, SIVERS SEMICONDUCTORS

AS WE NAVIGATE an increasingly digital world, the convergence of commercial telecommunications and defense technologies has never been more apparent. At Sivers Semiconductors, we're witnessing firsthand how millimeter-wave (mmWave) RF and beamforming technologies are revolutionizing both sectors, creating unprecedented opportunities for innovation and cross-industry collaboration.

The digital battlefield demands new solutions

The modern battlefield has evolved into a complex digital ecosystem where success depends on superior data capabilities. In recent conversations with defense partners, one theme consistently emerges: traditional RF systems simply cannot meet the bandwidth, security, and adaptability requirements of next-generation defense platforms. Legacy RF technologies operating in lower frequency bands face critical limitations that make them increasingly unsuitable for advanced defense applications. Spectrum congestion has reached levels that significantly reduce operational effectiveness. The limited bandwidth cannot support the massive data requirements of AI-driven systems and real-time sensor fusion. Perhaps most concerning, these traditional systems' vulnerability to interception and jamming creates unacceptable security risks in contested environments.

These challenges aren't unique to defense - experts are seeing similar constraints in commercial telecommunications, creating a natural technological convergence that's driving innovation across sectors.

Why mmWave Is the answer for both defense and commercial applications

At Sivers, we've been pioneering mmWave solutions for over a decade, and I'm convinced this technology provides a proven solution today and represents the future of high-performance communications for several compelling reasons. mmWave's high-frequency operation (24-100 GHz) delivers exponentially more bandwidth than traditional RF bands. This enables data rates measured in gigabits rather than megabits - essential for applications ranging from battlefield sensor networks to commercial 5G/6G infrastructure.

When combined with advanced beamforming techniques, mmWave offers unprecedented security advantages. Rather than broadcasting signals omnidirectionally, beamforming creates focused, directional transmissions that are inherently more difficult to intercept or jam - a critical capability in both military and sensitive commercial applications.

The precision targeting enabled by mmWave beamforming makes it ideal for high-resolution radar, object detection, and situational awareness systems across defense and commercial sectors alike. This capability transforms everything from military surveillance to autonomous vehicle navigation.

The semiconductor industry's role in enabling this transformation

The widespread adoption of mmWave technology depends entirely on semiconductor innovation. Several breakthroughs have been particularly significant in enabling practical mmWave implementations.

Beamforming ICs with integrated intelligence have dramatically simplified system design while enhancing performance. At Sivers, our beamforming ICs are capable of operating in multiple simultaneous frequency bands and forming multiple simultaneous beams, enabling resilient and multifunctional operation for commercial and defense systems alike. We are also pioneering -enhanced signal processing directly into beamforming arrays, enabling adaptive interference mitigation for simultaneous transmit and receive (STAR) capability that would have been impossible just a few years ago.

GaN amplifier technology has solved critical power and efficiency challenges that previously limited mmWave applications. The superior thermal performance of GaN is essential for the high-power, high-frequency operation required in military-grade systems.

Advanced packaging techniques like Antenna-in-Package (AiP) and 3D integration have also made large-scale phased arrays more compact and cost-effective, opening new deployment possibilities across multiple industries. These innovations are particularly important for defense applications where size, weight, and power matter.

How sivers is bridging defense and commercial innovation

We operate at the intersection of defense and commercial mmWave applications, fostering a self-reinforcing cycle of innovation that delivers mutual benefits to both sectors. Our involvement in the U.S. CHIPS Act's Microelectronics Commons program illustrates this strategic approach.

Through this initiative, we're collaborating with defense leaders including Raytheon and BAE Systems, as well as commercial telecommunications giants like Ericsson, to develop next-generation beamforming solutions. Our focus on dual-use technology has proven particularly valuable as defense agencies increasingly adopt commercial-off-the-shelf (COTS) approaches to technology acquisition.

By designing our mmWave solutions with both commercial and defense requirements in mind, we are able to successfully navigate multiple markets and industries, accelerate innovation and enable cost-effective rapid deployment all while maintaining the performance and security needed for mission-critical applications.

The challenges that still need addressing

Despite significant progress, several challenges must be overcome to fully realize mmWave's potential. As an industry, we must address range limitations and environmental sensitivity. mmWave signals don't propagate as far as lower-frequency alternatives and can be affected by atmospheric conditions.

Power consumption and thermal management remain significant hurdles, since high-frequency operation inherently demands more power. At Sivers, we have developed novel circuit topologies that enhance RF output power to boost range, while increasing efficiency to reduce energy

consumption, directly addressing both challenges. We believe that the next breakthrough in range and power consumption will come from cross-layer optimizations between the antennas, the RF circuitry and the digital signal processing, and we are collaborating with our system partners to deliver those.

Integration with legacy infrastructure presents another challenge. Defense customers need solutions that complement existing systems rather than requiring wholesale replacement. Our modular approach to mmWave design specifically addresses this challenge, allowing incremental adoption that respects the realities of defense procurement cycles.

What's next for mmWave in defense and beyond

Looking ahead, we see several emerging trends that will shape the future of mmWave technology.

The convergence of RF and photonics will create hybrid systems that leverage the strengths of both technologies. We are already exploring photonic-based signal processing to enhance our mmWave solutions, potentially overcoming some of the fundamental limitations of purely electronic systems.

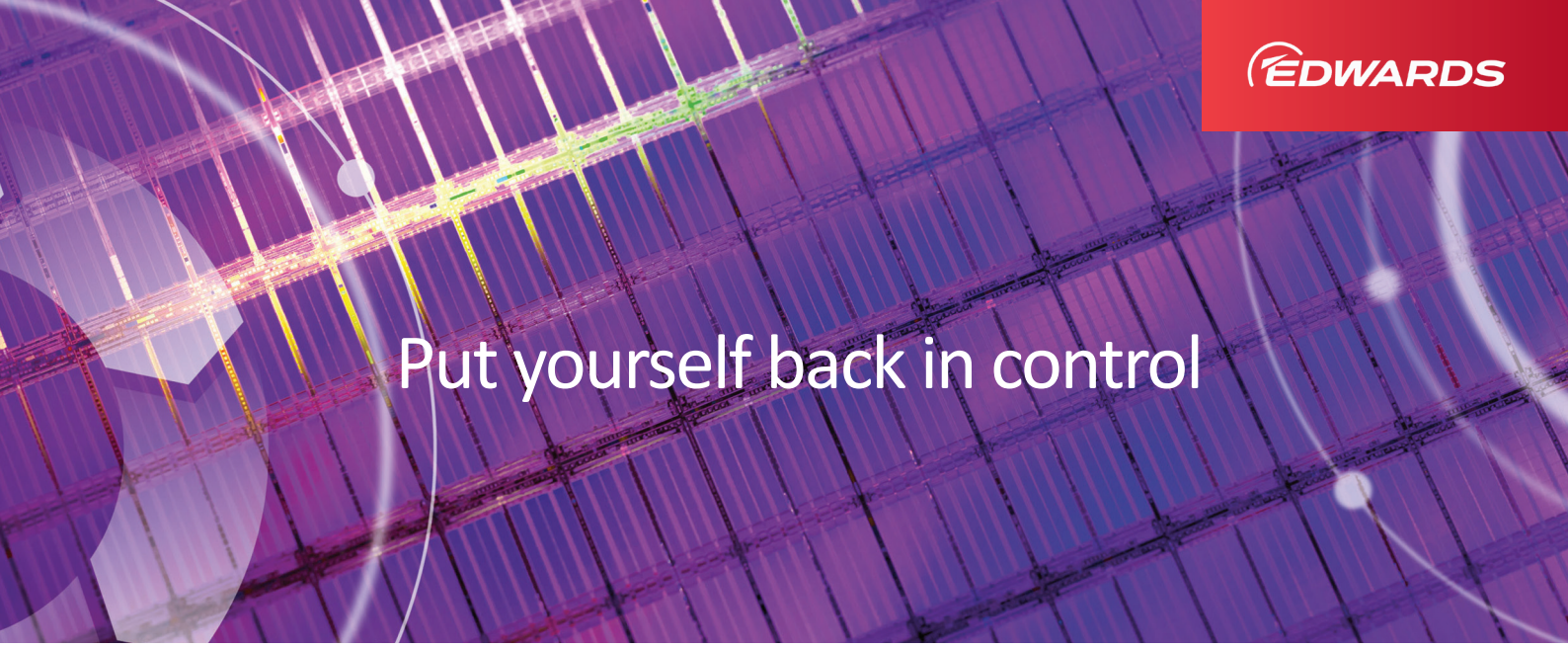
AI-driven adaptive beamforming will become increasingly sophisticated, enabling systems that can autonomously optimize performance in complex and contested environments. This capability will be particularly valuable in electronic warfare applications where the ability to rapidly adapt to changing conditions can mean the difference between mission success and failure.

As defense and commercial requirements continue to converge, we'll see accelerated technology transfer between sectors, creating a positive feedback loop that benefits the entire ecosystem. Long gone are the days when defense technology led commercial innovation.

Today, the most successful defense systems often leverage commercial semiconductor advancements, while adding the ruggedization and security features required for military deployment and use.

At Sivers Semiconductors, we're committed to leading this transformation through continued investment in R&D, strategic partnerships across defense and commercial sectors, and a relentless focus on pushing the boundaries of what's possible with mmWave technology.

The future of defense communications is being shaped today by innovations in mmWave RF and beamforming—and the semiconductor industry stands at the center of this revolution. As we continue to advance these technologies, we're not just improving military capabilities, we're laying the groundwork for the next generation of secure, high-performance communications across all sectors.



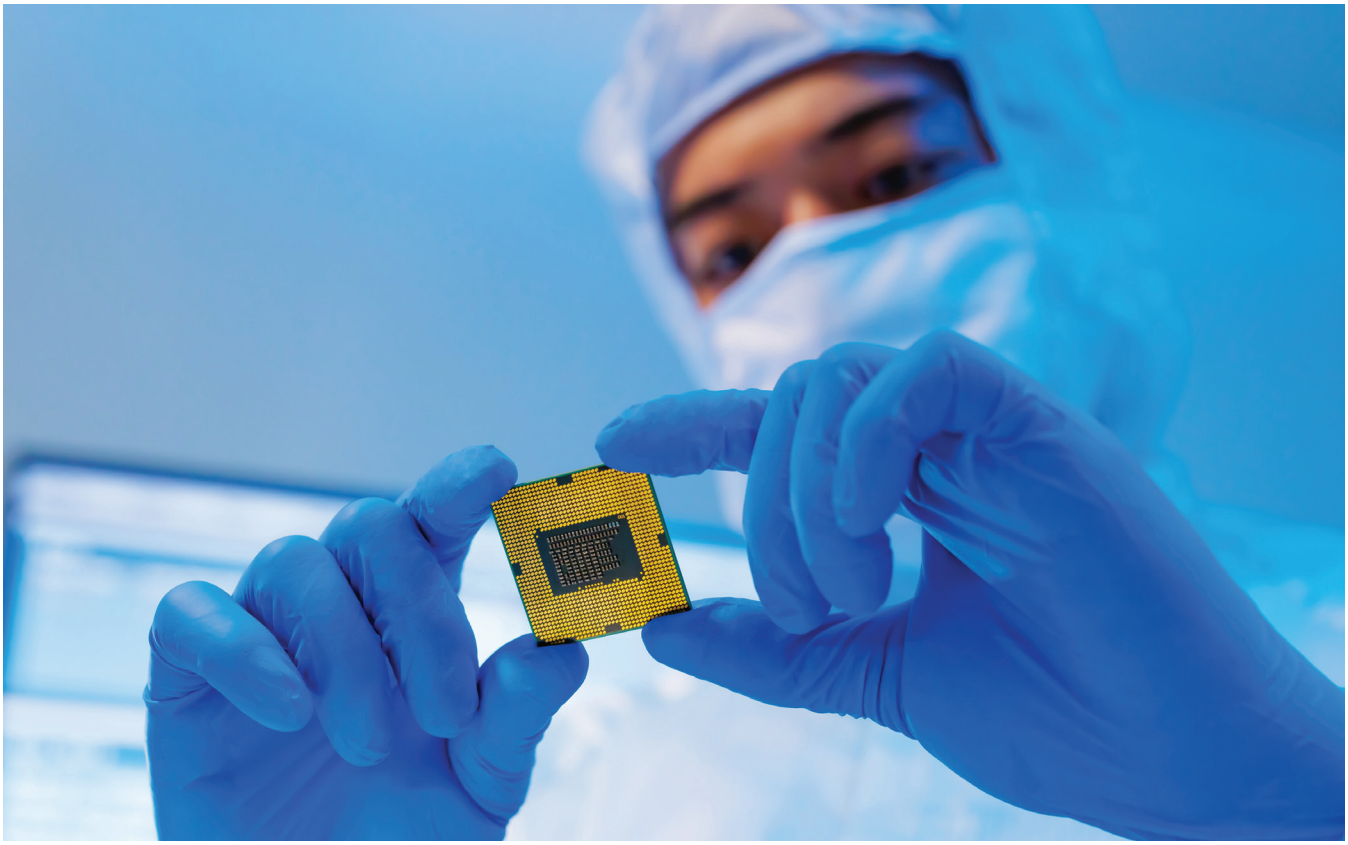
Put yourself back in control

Are unplanned dowtimes dragging down your productivity? Is your Fab efficiency and TCoO being damaged by avoidable stoppages? Avoidable? How? By working with us to implement one of our core service plans you can take back control of your throughput and manage equipment with a planned service regime. Talk to us today and head towards a more productive future.

Care Spare parts plan	Maintain Parts and labour for standard maintenance	Perform Standard maintenance with upgrades included
One single purchase order and monthly billing	One single purchase order and monthly billing	One single purchase order and monthly billing
Fixed supply of parts for standard maintenance used on site annually	Preventative and routine maintenance activities, including parts and labour required for each activity	Preventative and routine maintenance activities, including parts and labour required for each activity
Basic operational support provided by our team of experts	Maintenance performed on site by our field service team for Abatement, or at our Service Technology Centres for Dry, Turbo, and Cryogenic Pumps	Maintenance performed on site by our field service team for Abatement, or at our Service Technology Centres for Dry, Turbo, and Cryogenic Pumps
The plan can be enhanced with chargeable options at additional cost, including training and troubleshooting by our service teams	Troubleshooting and operational support provided by our team of experts	Troubleshooting and operational support provided by our team of experts
	The plan can be enhanced with chargeable options at additional cost, including service exchange, upgrades, and inventory management	Can include specific upgrades or improvement components according to the contract.
		Possible to customise the plan with additional options

Edwards semiconductor *Intelligent* service

View our range of service plans at www.edwardsvacuum.com



Ensuring gas purity for complex semiconductor manufacturing

As demand for chips grows, the semiconductor industry is pushing the limits of current manufacturing capabilities. Companies that invest in cutting-edge QA/QC tools will not only keep pace with demand, but also gain a competitive advantage in a fiercely competitive global market.

BY DANIEL MERRIMAN, SEMICONDUCTOR CONSULTANT AT THERMO FISHER SCIENTIFIC

SEMICONDUCTOR CHIPS are the driving force behind modern electronics. Any electronic device – from the cell phone in your pocket to the LED lights in your home or office – uses semiconductor technology, and many of these devices are becoming smarter and more connected with each iteration. There's expanding use of advanced semiconductor technology across a wide range of applications, such as artificial intelligence (AI), wearable technology and advanced data centers. In fact, Deloitte projected that the industry is on track to reach $1 trillion in chip sales by 2030, largely driven by the demand for generative AI.

As the global semiconductor industry grows to an estimated $1 trillion by 2030 and semiconductor manufacturers transition to advanced, three-dimensional chip designs that support society's technological advancement, there's a critical need for a consistent supply of ultra-high purity (UHP) gases during production. Gas impurities can result in poor device performance, production delays and revenue loss. While tools like electron microscopes can help identify micro-scale physical defects that impact production, innovative analytical technologies, such as UHP electronic gas analyzers that combine atmospheric pressure ionization mass spectrometry (API-MS), can help ensure that semiconductor manufacturers have the UHP gases they need to achieve the precision required for these semiconductors.

API-MS sets a new benchmark in gas analysis by enabling the continuous detection of impurities at exceptionally low levels. This sensitivity ensures even the tiniest contaminants are identified,

addressing the industry's need for extreme precision for manufacturers. The industry needs next-generation gas analyzers to streamline and optimize quality control (QC) processes to meet he stringent demands of semiconductor manufacturing.

Challenges in quality control for semiconductor manufacturing

Challenges in quality control remain even with the most advanced semiconductor production processes. Because chips are susceptible to impurities, which can absorb through the surface of the wafer and affect the properties of subsequent layers, even trace levels of contaminants in the gas supply can result in costly defects, production delays and revenue loss.

To maintain wafer integrity, semiconductor manufacturers need tools for greater precision in electronic specialty gas (ESG) composition, which includes nitrogen, oxygen, argon, hydrogen, helium and carbon dioxide, among others. UHP gas analyzers allow each bulk gas to be monitored for a range of potential contaminants at parts per trillion (ppt) level detection, which meets the most stringent quality requirements.

Historically, techniques such as gas chromatography and thermal desorption have been used to monitor the purity of ESGs. However, as industry focuses on producing smaller, more complex chips, these methods become inadequate for industry demands, where contamination limits must be far lower and more precise.

When impurities go undetected in manufacturing, it can result in scrapped wafers, wasted resources and production line suspensions. The financial and reputational stakes are higher than ever in a growing industry under pressure to deliver flawless devices.

Adopting API-MS into workflow for QC

For continuous impurity monitoring, manufacturers should look to adopt innovative analytical technologies, such as API-MS analyzers. When coupled with sophisticated electronics and software, API-MS analyzers can help overcome the limitations of technologies like gas chromatography.

With real-time feedback, manufacturers are able to quickly address quality issues and avoid costly disruptions. API-MS analyzers can also detect a wider spectrum of impurities, such as combining oxygen and moisture with hydrocarbons, hydrogen, carbon monoxide and inert gases. This information ensures manufacturers can confidently meet evolving standards for gas purity.

Another benefit of adopting API-MS analyzers is that the technology can reduce capital and operational costs by providing multi-component and multi-stream solutions. These analyzers have built-in automated calibration capability which further reduces user intervention and drives down cost of ownership. To ensure that complex semiconductor manufacturing is optimized for maximum yield, gas manufacturers and semiconductor companies should turn to API-MS to identify, reduce and avoid defects and contamination that make high quality output a reality.

Combining analytical techniques to ensure quality

Innovation across the value chain is required to meet the demands of today's semiconductor industry. While API-MS ensures ultra-high purity gases, advanced imaging techniques, such as scanning electron microscopy (SEM), can help manufacturers identify atomic-level structural defects in semiconductors for a comprehensive approach to quality control. SEM tools use low-voltage imaging to analyze miniaturized device features without causing damage, complementing API-MS by addressing physical fault detection.

Additionally, automation in SEM workflows streamlines data collection and enhances precision, reducing production downtime and improving efficiency in fault analysis. Integrating data from API-MS and SEM provides a holistic view of the quality assurance (QA) and QC process, enabling manufacturers to quickly identify and resolve issues, ensuring seamless semiconductor production.

The path forward led by innovative technologies

As demand for chips grows, the semiconductor industry is pushing the limits of current manufacturing capabilities. Companies that invest in cutting-edge QA/QC tools will not only keep pace with demand, but also gain a competitive advantage in a fiercely competitive global market.

Semiconductor manufacturers can create a powerful and cost-effective workflow by adopting next-generation gas analyzers and advanced analytical technologies. They can significantly reduce contamination risks, minimize production delays and maintain the integrity of their products. Precision and accuracy are imperative for quality control and quality assurance in chip manufacturing and innovative tools allow companies to address the growing complexity of devices and meet market demands.

With continuous technological advancements, manufacturers are better positioned than ever to deliver high-quality, flawless devices that meet expectations across industries.

MIT engineers print synthetic “metamaterials” that are both strong and stretchy

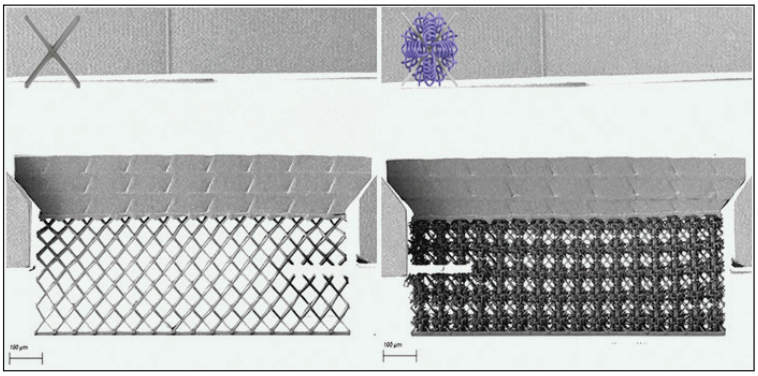
A new method could enable stretchable ceramics, glass, and metals, for tear-proof textiles or stretchy semiconductors.

BY JENNIFER CHU, MIT NEWS

IN METAMATERIALS DESIGN, the name of the game has long been “stronger is better.”

Metamaterials are synthetic materials with microscopic structures that give the overall material exceptional properties. A huge focus has been in designing metamaterials that are stronger and stiffer than their conventional counterparts. But there’s a trade-off: The stiffer a material, the less flexible it is. MIT engineers have now found a way to fabricate a metamaterial that is both strong and stretchy. The base material is typically highly rigid and brittle, but it is printed in precise, intricate patterns that form a structure that is both strong and flexible.

The key to the new material’s dual properties is a combination of stiff microscopic struts and a softer woven architecture. This microscopic “double network,” which is printed using a plexiglass-like polymer, produced a material that could stretch over four times its size without fully breaking. In comparison, the polymer in other forms has little to no stretch and shatters easily once cracked.



➤ MIT engineers have found a way to fabricate a metamaterial (right) that is both strong and stretchy. The base material (left) is typically rigid and brittle, but when printed in precise intricate patterns it forms a material with exceptional properties.
Credit: Courtesy of the researchers

The researchers say the new double-network design can be applied to other materials, for instance to fabricate stretchy ceramics, glass, and metals. Such tough yet bendy materials could be made into tear-resistant textiles, flexible semiconductors, electronic chip packaging, and durable yet compliant scaffolds on which to grow cells for tissue repair.

“We are opening up this new territory for metamaterials,” says Carlos Portela, the Robert N. Noyce Career Development Associate Professor at MIT. “You could print a double-network metal or ceramic, and you could get a lot of these benefits, in that it would take more energy to break them, and they would be significantly more stretchable.” Portela and his colleagues will report their findings in the journal Nature Materials. His MIT co-authors include first author James Utama Surjadi as well as Bastien Aymon and Molly Carton.

Inspired gel

Along with other research groups, Portela and his colleagues have typically designed metamaterials by printing or nanofabricating microscopic lattices using conventional polymers similar to plexiglass and ceramic. The specific pattern, or architecture, that they print can impart exceptional strength and impact resistance to the resulting metamaterial. Several years ago, Portela was curious whether a metamaterial could be made from an inherently stiff material, but be patterned in a way that would turn it into a much softer, stretchier version.

“We realized that the field of metamaterials has not really tried to make an impact in the soft matter realm,” he says. “So far, we’ve all been looking for the stiffest and strongest materials possible.” Instead, he looked for a way to synthesize softer, stretchier metamaterials. Rather than printing microscopic struts and trusses, similar to those of conventional lattice-based metamaterials, he and his team made an architecture of interwoven springs, or

coils. They found that, while the material they used was itself stiff like plexiglass, the resulting woven metamaterial was soft and springy, like rubber. "They were stretchy, but too soft and compliant," Portela recalls.

In looking for ways to bulk up their softer metamaterial, the team found inspiration in an entirely different material: hydrogel. Hydrogels are soft, stretchy, Jell-O-like materials that are composed of mostly water and a bit of polymer structure. Researchers including groups at MIT have devised ways to make hydrogels that are both soft and stretchy, and also tough. They do so by combining polymer networks with very different properties, such as a network of molecules that is naturally stiff, which gets chemically cross-linked with another molecular network that is inherently soft. Portela and his colleagues wondered whether such a double-network design could be adapted to metamaterials.

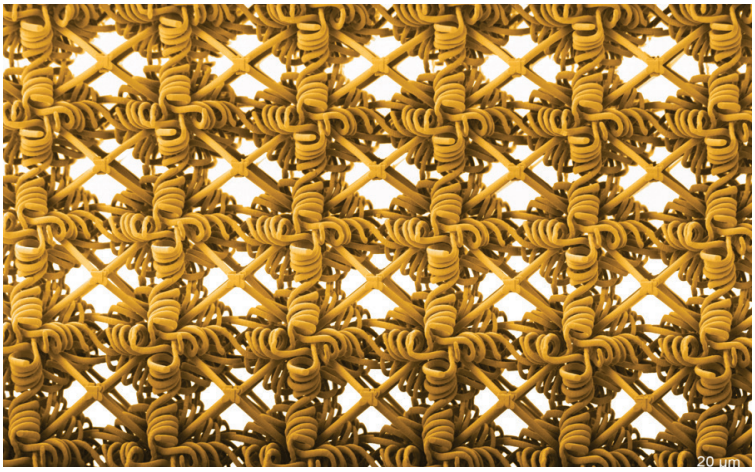
"That was our 'aha' moment," Portela says. "We thought: Can we get inspiration from these hydrogels to create a metamaterial with similar stiff and stretchy properties?"

trut and weave

For their new study, the team fabricated a metamaterial by combining two microscopic architectures. The first is a rigid, grid-like scaffold of struts and trusses. The second is a pattern of coils that weave around each strut and truss. Both networks are made from the same acrylic plastic and are printed in one go, using a high-precision, laser-based printing technique called two-photon lithography.

The researchers printed samples of the new double-network-inspired metamaterial, each measuring in size from several square microns to several square millimeters. They put the material through a series of stress tests, in which they attached either end of the sample to a specialized nanomechanical press and measured the force it took to pull the material apart. They also recorded high-resolution videos to observe the locations and ways in which the material stretched and tore as it was pulled apart. They found their new double-network design was able stretch three times its own length, which also happened to be 10 times farther compared to a conventional lattice-patterned metamaterial printed with the same acrylic plastic. Portela says the new material's stretchy resistance comes from the interactions between the material's rigid struts and the messier, coiled weave as the material is stressed and pulled.

"Think of this woven network as a mess of spaghetti tangled around a lattice. As we break the monolithic lattice network, those broken parts come along for the ride, and now all this spaghetti gets entangled with the lattice pieces," Portela explains. "That promotes more entanglement between woven fibers, which means you have more friction and more energy dissipation."



➤ Metamaterials are synthetic materials with microscopic structures that give the overall material exceptional properties. Credit: Courtesy of the researchers

In other words, the softer structure wound throughout the material's rigid lattice takes on more stress thanks to multiple knots or entanglements promoted by the cracked struts. As this stress spreads unevenly through the material, an initial crack is unlikely to go straight through and quickly tear the material. What's more, the team found that if they introduced strategic holes, or "defects," in the metamaterial, they could further dissipate any stress that the material undergoes, making it even stretchier and more resistant to tearing apart. "You might think this makes the material worse," says study co-author Surjadi. "But we saw once we started adding defects, we doubled the amount of stretch we were able to do, and tripled the amount of energy that we dissipated. That gives us a material that's both stiff and tough, which is usually a contradiction."

The team has developed a computational framework that can help engineers estimate how a metamaterial will perform given the pattern of its stiff and stretchy networks. They envision such a blueprint will be useful in designing tear-proof textiles and fabrics.

"We also want to try this approach on more brittle materials, to give them multifunctionality," Portela says. "So far we've talked of mechanical properties, but what if we could also make them conductive, or responsive to temperature? For that, the two networks could be made from different polymers, that respond to temperature in different ways, so that a fabric can open its pores or become more compliant when it's warm and can be more rigid when it's cold. That's something we can explore now."

This research was supported, in part, by the U.S. National Science Foundation, and the MIT MechE MathWorks Seed Fund.

FTD solutions partners with CEA-Leti to improve water infrastructure management

CEA-Leti has partnered with FTD solutions to evaluate and enhance semiconductor manufacturing water management strategies to meet sustainability goals, with the ultimate aim of helping to shape best practices and drive industry-wide adoption of sustainable solutions. Slava shares some brilliant insights as to sustainable water management within the sector, with a particular focus on the need for water circularity within sites.

BY SLAVA LIBMAN, CEO AND CO-FOUNDER OF FTD SOLUTIONS

SS: *Please can we start with a quick introduction to FTD solutions?*

SL: FTD stands for Facility Technology Development. The company was formed nearly eight years ago recognizing the opportunity to revolutionize efficiency and sustainability in semiconductor facilities and beyond. Our approach involves developing digital twin models of facilities, which reveal the most effective solutions for site-specific water management. We then assist solution providers in aligning their offerings with specific customer needs.

We're talking today because you have announced a partnership with CEA-Leti in the semiconductor industry – how did this collaboration come about? CEA-Leti is championing sustainable manufacturing initiatives in Europe. Our collaboration began two years ago when I met Laurent Pain, a sustainability executive from Leti, in San Francisco. Our shared mission became clear immediately. We initially collaborated on developing a site water model and water conservation solutions for Leti's facility in Grenoble. Now, based on the success of this initial project, we're ready to collaboratively bring water circularity best practices to the broader industry.

SS: *And the partnership is focused on sustainable water management in this sector?*

SL: Yes, primarily. We are also exploring opportunity with energy management.

SS: *More generally, how would you characterise the semiconductor industry's approach to water use as of now and, crucially, where does it need to be (i.e. maybe not in Arizona?!)?*

SL: Water is perhaps the most critical resource and infrastructure component in semiconductor fabrication. The industry's approach to water usage continues to evolve, with each successive generation of technology requiring increased water for both process and non-process applications. Process applications demand more water due to the rising number of layers in semiconductor devices, while non-process uses require additional water for air abatement and evaporative cooling in energy-intensive plants.

A significant shift in the industry's approach can be defined by the emerging concept of "water circularity." Previously, the focus was on purifying incoming water to ultrapure water (UPW) standards and subsequently treating wastewater to ensure compliance. The new emphasis is on conservation and reuse, creating circular interdependencies between various water systems and introducing new challenges for site water management.

Regarding location choices, factors like trained workforce availability, supply chains, land, and business environment play critical roles. While water availability is recognized as important, it is typically not the sole determining factor.

SS: *In order to achieve success when it comes to sustainable water management, what needs to happen; what does the roadmap look like?*
SL: Sustainable water management relies more on the continuity and consistency of data-driven decisions than on specific water treatment technologies. Current technologies generally meet industry needs; the complexity arises from water being inherently local. Facilities must therefore be tailored and optimized according to local conditions, making standardization difficult.

To successfully achieve water circularity, we firmly believe holistic visualization of site water systems and generating actionable insights for data-driven decisions are essential. A clear roadmap requires establishing a known baseline, clearly defining goals and boundaries, and formulating an optimal solution strategy. This strategy is crucial for selecting appropriate water technologies to ensure cost-effective and reliable operations.

SS: *For example, the Genesis Project, of which CEA-Leti is a part, is looking to address sustainable water management?*

SL: As far as I understand, sustainable water management is part of the Genesis project's scope. We are honored to support this initiative both directly and through our involvement with the IRDS organization.

SS: *What are the challenges to be overcome along the way in terms of semiconductor water usage – and what role does FTD have to play?*

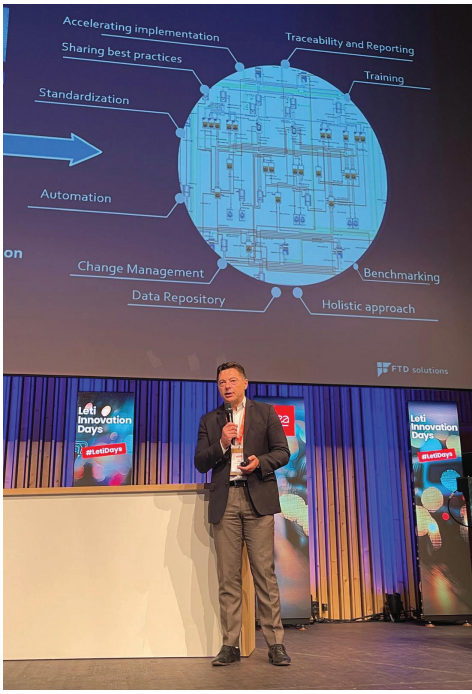
SL: The industry's challenges are substantial. First, the scale and complexity of new facilities under construction will exponentially increase reliability, cost, and compliance issues. Unless adequately prepared, overcoming these challenges will be very difficult. FTD's role is to assist facilities to prepare and help navigate these challenges effectively. Second, there is a growing demand for water expertise at a time when the number of industry experts is decreasing. FTD helps minimize the time experts spend on data collection and management, maximizing their productivity and impact.

Third, the next generation of facilities has heightened sensitivity to yield and reliability issues, requiring highly robust infrastructure. Leveraging advanced technologies, machine learning, and AI is critical, and FTD plays a vital role in enabling these innovations for site water management.

Finally, optimizing water management without negative environmental impacts is crucial. Recently, industry roadmap organizations like IRDS and SEMI Standards developed a new KPI framework to guide the industry in selecting water technology solutions with lower environmental footprints. FTD actively contributes to this initiative.

SS: *And how does the semiconductor industry compare with other sectors when it comes to sustainable water management – can it learn lessons from elsewhere and/or share its learnings?*

SL: The complexity of semiconductor facilities is unparalleled. Historically, this sector has led innovation, developing technologies later adopted by other industries.

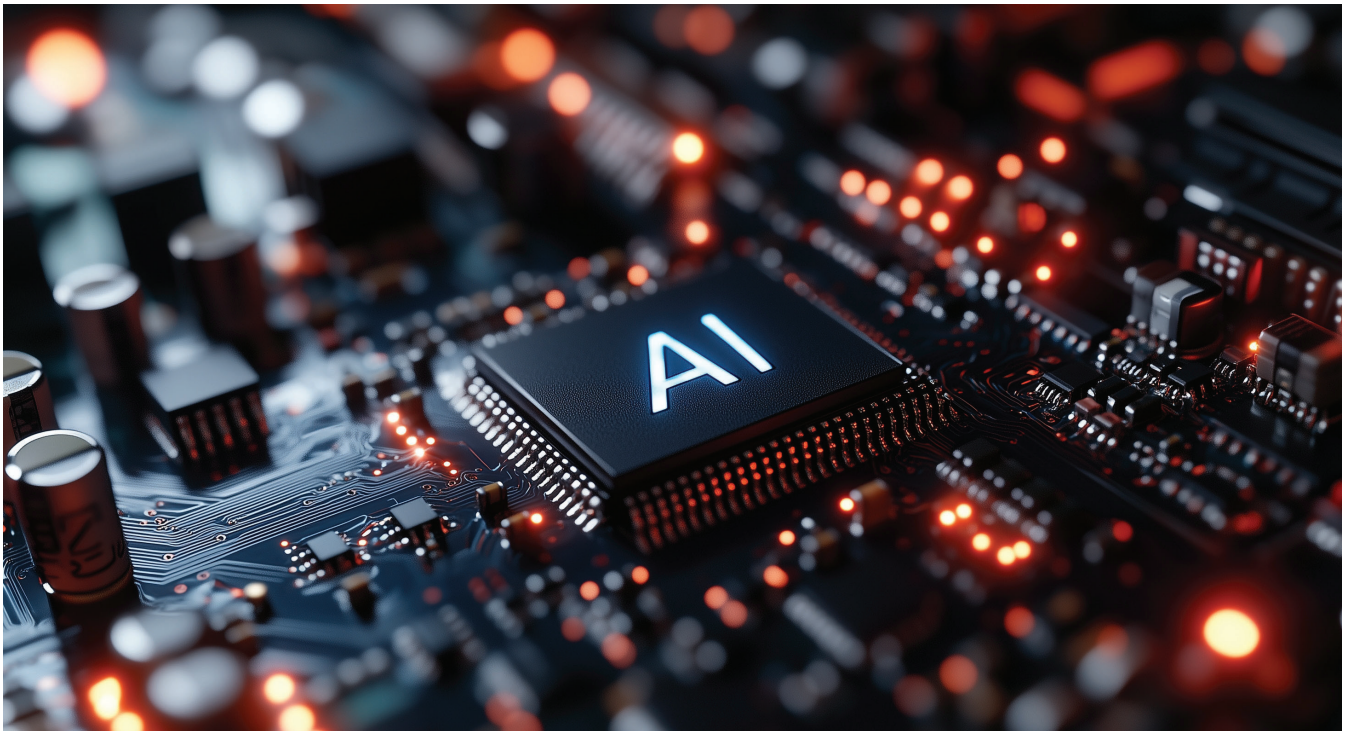


SS: *Which brings us to the importance of sustainable water management across all industry sectors – has there been too much focus on carbon emissions and general pollution reduction and not nearly enough focus on the looming threat of global water scarcity?*

SL: It is often true that water scarcity receives less public attention than global warming, partly because water access is generally guaranteed and subsidized by governments. I personally believe energy and carbon emission challenges will likely be solved faster than water scarcity. Consequently, we must proactively manage water usage to create time for developing necessary water infrastructure, such as desalination plants and improved waterways. Effective water management today reduces demand and frees resources for infrastructure development.

SS: *Set against the issues we have discussed, what does the FTD roadmap look like – how is the company looking to help shape the debate and, perhaps more importantly, the concrete actions which need to happen, and quickly?*

The core strength of FTD's value proposition lies in catalyzing immediate action and fostering innovation at scale. With our scalable solutions, we are uniquely positioned to support significant industrial facility needs swiftly and effectively. Now is a pivotal moment for industry leaders to engage proactively with us, accelerating the transformation of water management practices and gaining a competitive advantage in sustainability leadership.



How simulation is helping to usher in tomorrow's chips

By embracing comprehensive multi-physics simulation and leveraging AI to accelerate design processes, semiconductor companies can navigate the challenges of heterogeneous integration and deliver the computing platforms that will power the next wave of AI innovation.

BY JAYRAJ NAIR, FIELD CTO FOR HI-TECH AND APAC, ANSYS

THE SEMICONDUCTOR INDUSTRY stands at a critical turning point. With global semiconductor sales reaching $57.8 billion in last year the need for the industry to scale has never been more apparent. Yet mounting physical and economic limitations threaten this growth. As AI applications drive unprecedented requirements for processing capabilities, chip designers are turning to advanced simulation technologies to enable the next generation of complex heterogeneous multi-die systems.

Today's chips increasingly integrate specialised processing elements particularly Neural Processing Units (NPUs) for AI workloads - alongside Graphics Processing Units (GPUs), Central Processing Units (CPUs) and memory in sophisticated multi-die packages. It's no secret that designing these systems requires understanding complex interactions across electrical, thermal, and mechanical domains that can only be predicted through comprehensive multi-physics simulation. As the industry embraces this approach, simulation has evolved from a verification tool to a central enabler of innovation, allowing designers to explore novel architectures that would otherwise be too risky to attempt.

Beyond traditional scaling

For decades, the semiconductor industry relied on transistor scaling to improve performance and efficiency. However, as process nodes approach physical limits, the cost benefit equation of scaling has shifted dramatically. The cost per transistor at advanced nodes is no longer decreasing and may even be increasing, pushing manufacturers toward alternative approaches to enhance system performance.

This reality has catalysed a fundamental shift away from simply scaling monolithic CPU and GPU designs. While GPUs revolutionised computing by enabling massive parallelism - first for graphics rendering and later for AI training - even these powerful processors face scaling limitations. With AI chips expected to grow by more than 30% in

2025, heterogeneous integration has emerged as the solution to ensure continued advancement. By combining multiple specialised dies - potentially manufactured on different process nodes - into a cohesive package, system architects can optimise each component for its specific function rather than compromise on a monolithic design.

NPUs represent one of the most significant specialised silicon developments for AI applications. These purpose-built processors contain architectures optimised for tensor operations with specialised data paths, memory hierarchies, and computational elements that dramatically accelerate neural network workloads compared to general-purpose processors. When integrated alongside CPUs for general computing and GPUs for parallel processing tasks, these heterogeneous systems deliver unprecedented computational capabilities for AI applications.

This shift toward heterogeneous integration introduces new design complexities that can't be addressed through traditional prototyping methods alone. As these systems become more intricate, simulation has emerged as the critical enabler, allowing engineers to validate designs before committing to expensive silicon implementation.

Multi-physics challenges in NPU-based systems

The design of heterogeneous multi-die systems with NPUs introduces unprecedented complexity across multiple domains. Traditional simulation approaches that treat electrical, thermal, and mechanical phenomena as separate concerns simply won't cut it for these highly integrated systems where interdependent physical effects significantly impact performance and reliability.

Power delivery networks and thermal management systems must be analysed holistically, as electrical performance affects thermal profiles while heat dissipation impacts electrical performance in a continuous feedback loop. This interdependency is particularly critical for NPUs, which can experience dramatic power fluctuations during different computational phases. Similarly, high-bandwidth, low-power interfaces between dies demand detailed electromagnetic analysis to ensure signal integrity while operating within increasingly tight power constraints – a challenge that grows more complex as die to die communication speeds increase.

Multi-scale physics challenges have become increasingly important as system designs span from nanometer-scale transistors to centimeter-scale packages and beyond. This wide range of physical dimensions requires simulation tools capable of seamlessly transitioning between different scales while maintaining accuracy and computational efficiency. Additionally, as optics and electronics converge in modern systems, thermal stability challenges with co-packaged optics have introduced yet another dimension of complexity requiring sophisticated multi-physics modeling approaches.

The complexity extends to power integrity across multiple domains, as NPUs and other specialised processors typically operate with different voltage levels and power requirements. This necessitates sophisticated power delivery network analysis to prevent voltage droops that could compromise system stability. Mechanical stress presents another significant challenge, as the complex structures in advanced packages experience thermal expansion and contraction during assembly and operation that can affect both reliability and electrical performance through stress-induced parameter shifts.
Beyond these component-level concerns, predicting overall system performance under realistic workloads has become essential for optimising heterogeneous architectures. These limitations have driven the semiconductor industry toward more sophisticated simulation approaches that can address the multifaceted nature of modern chip design.

Advanced simulation methodologies

Modern simulation methodologies for heterogeneous systems are evolving toward unified, multi-physics approaches that capture the complex interactions between different physical domains. Co-simulation frameworks have emerged as particularly valuable tools, enabling simultaneous analysis of electrical, thermal, and mechanical phenomena with bidirectional coupling of results. In these environments, power distribution analysis feeds directly into thermal simulation, which in turn affects electrical performance through temperature-dependent parameters, creating a more realistic model of the system's actual behaviour under operating conditions.

To manage the computational complexity of these multi-physics problems, Domain Decomposition Methods (DDM) have become increasingly important. These techniques strategically divide complex problems into multiple smaller, manageable subdomains that can be solved independently and then combined, substantially improving the capability to solve multi-domain, multi-physics large-scale problems efficiently without sacrificing accuracy. This approach is particularly valuable for heterogeneous systems where different components may require different levels of simulation fidelity.

Time-to-market pressures have become a critical factor, particularly in competitive sectors like automotive, where

manufacturers struggle to meet the growing demand for sophisticated silicon components. Advanced System Architecture Modelers now enable engineering teams to adopt a shift left approach, allowing earlier validation of system-level performance and accelerating development cycles by identifying potential issues before committing to silicon implementation. These tools support new ways of working that break down traditional silos between different engineering disciplines, fostering collaborative environments where thermal, mechanical, and electrical experts can work concurrently rather than sequentially.

The integration of machine learning into the simulation workflow represents another significant advancement. AI-based methods can accelerate simulation by training models on existing results, allowing engineers to quickly explore design spaces without running full-scale simulations for every configuration.

These advances in simulation technology have enabled comprehensive package analysis for the complex 2.5D and 3D packaging configurations that are increasingly common in NPU-based systems. Modern tools can now model through-silicon vias, redistribution layers, and embedded cooling technologies with high fidelity, providing accurate predictions of system performance before physical prototyping.

Die to die interfaces: Critical enablers of NPU integration

The interfaces between dies in heterogeneous systems represent both a key enabling technology and a significant design challenge. High-speed die to die communication is essential for NPUs to efficiently access memory and exchange data with CPUs and other system components. The industry is pursuing several promising technologies to address these connectivity requirements, each with distinct advantages for specific use cases.

Advanced packaging with silicon interposers provides high-density interconnects between dies, enabling wider data paths with shorter trace lengths that significantly reduce latency and power consumption. This approach has proven particularly valuable for connecting NPUs to high-bandwidth memory, where wide data paths are critical for computational performance.

For even greater integration density, hybrid bonding technologies that create direct copper-to-copper connections between dies enable extremely high interconnect densities, supporting the massive parallel data movement required by modern NPU architectures.

Looking toward future systems with more distributed processing, optical interconnect technologies based on silicon photonics promise higher bandwidth with lower power consumption than traditional electrical interconnects, particularly for longer-reach connections between chiplets. Simulating these advanced interfaces requires specialised tools that can accurately capture high-frequency electromagnetic effects, crosstalk between densely packed traces, and the impact of process variations on signal integrity.

Thermal management and power integrity

As heterogeneous systems integrate high-performance NPUs alongside traditional processors, thermal management becomes increasingly challenging. NPUs can generate significant heat during intensive AI workloads, creating localised hotspots that significantly exceed the average power density of the cooling system. This challenge is compounded by thermal coupling between dies, where heat generated by one component affects adjacent dies, creating complex thermal profiles that must be analysed holistically.

The dynamic nature of AI workloads further complicates thermal management, as these

Power delivery networks and thermal management systems must be analysed holistically, as electrical performance affects thermal profiles while heat dissipation impacts electrical performance in a continuous feedback loop. This interdependency is particularly critical for NPUs, which can experience dramatic power fluctuations during different computational phases

semi™

Connecting Semiconductors and Electronics

About SEMI:
SEMI connects more than 2,500 member companies and 1.3 million professionals worldwide to advance the technology and business of electronics design and manufacturing. The breadth and depth of our events, programs and services help members accelerate innovation and collaboration on the toughest challenges to growth.

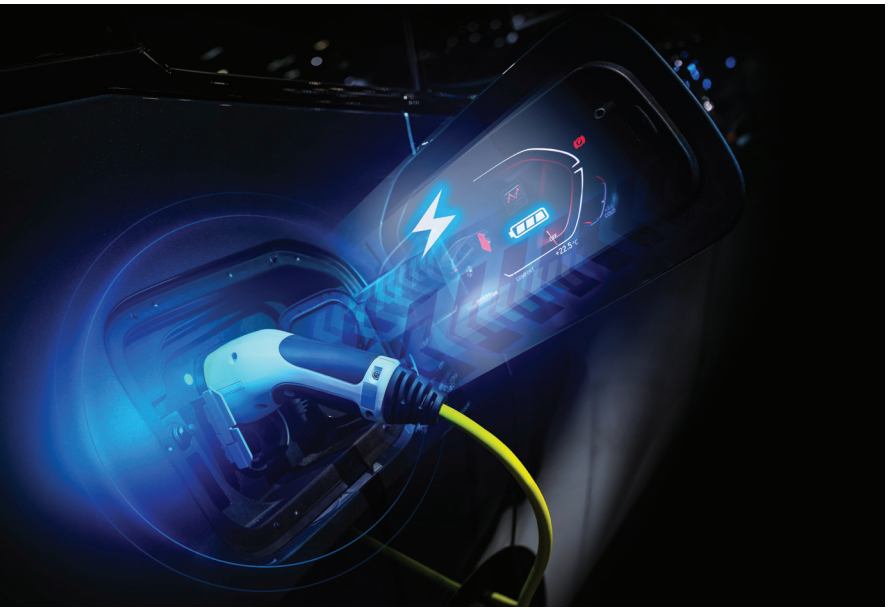
ESDA Electronic System Design Alliance

FlexTech

FOA Fab Owners Alliance

MEMS & SENSORS INDUSTRY GROUP®

SOI Industry Consortium



applications often result in variable power consumption patterns that create transient thermal conditions requiring time-dependent analysis. To address these challenges, engineers are developing advanced cooling solutions including embedded cooling channels and vapor chambers that require detailed modelling to predict performance across various operating scenarios.

Power delivery is equally critical in heterogeneous NPU systems. These specialised processors often require precise voltage regulation under rapidly changing load conditions to maintain performance and prevent errors. Heterogeneous systems typically require distributed power delivery networks to support multiple dies with different voltage requirements, while the dynamic load profiles characteristic of NPU operation can stress power networks and create voltage fluctuations. Many NPU architectures operate at reduced voltage levels to maximise energy efficiency, providing minimal margins for transients and droops and making accurate simulation of the power delivery network essential.

Embracing AI to accelerate simulation and design

The computational demands of simulating heterogeneous NPU systems have become increasingly challenging as designs grow in complexity. Machine learning methods have emerged as valuable tools for accelerating complex simulations while maintaining acceptable accuracy. By training surrogate models on results from detailed physics-based simulations, engineers can rapidly predict system behaviour across numerous design variations without running full electromagnetic or thermal simulations for each configuration.

Beyond simulation acceleration, AI-enhanced design flows can play an increasingly important role in guiding decisions based on accumulated knowledge from previous implementations. Machine learning systems can identify patterns in successful designs and flag potential issues before they become costly problems, effectively capturing and applying institutional knowledge across projects.

Unified design methodologies

As heterogeneous integration with NPUs becomes the dominant paradigm for high-performance computing, the industry is moving toward unified design methodologies that span multiple physical domains and packaging levels. Standardisation of interface files represents a critical step toward more unified workflows, allowing different simulation tools to exchange information and enabling comprehensive cross-domain analysis.

Equally important is the development of secure methods for sharing geometric and physical data without exposing proprietary design details. As heterogeneous systems increasingly incorporate components from multiple suppliers, the ability to exchange essential physical characteristics while protecting intellectual property becomes crucial for enabling better multi-component analysis.

Standardised specification of compliance for interfaces between heterogeneous components will also streamline the integration process and reduce compatibility risks. Unified approaches to specifying and verifying the performance of die-to-die connections, thermal interfaces, and power delivery characteristics establish clear expectations for component suppliers and system integrators. The transformation of the semiconductor industry requires not just technological evolution but a parallel evolution in workforce capabilities. As designs become more complex and interdisciplinary, the industry faces a critical skills gap that threatens to impede progress. Tomorrow's semiconductor professionals need to adopt broader thinking patterns that cross traditional domain boundaries, embracing both deep expertise and systems-level understanding. Companies must invest in upskilling and reskilling their workforce to meet these new demands, fostering environments where electrical engineers understand thermal implications and mechanical engineers appreciate signal integrity concerns. This workforce transformation is just as essential as technological advancement for addressing the semiconductor industry's mounting challenges.

The fact is, by embracing comprehensive multi-physics simulation and leveraging AI to accelerate design processes, semiconductor companies can navigate the challenges of heterogeneous integration and deliver the computing platforms that will power the next wave of AI innovation. As these simulation capabilities continue to mature, they will enable increasingly sophisticated architectures that deliver the computational power needed for next-generation applications while effectively managing system constraints.

Dedicated webinars for the silicon semiconductor industry

Using our 30+ years' experience in B2B vertical technical markets, and as the publisher of Silicon Semiconductor, we offer effective webinars, ZOOM interview and virtual events. We help you get your message, to your desired audience, by marketing to over 55,000 silicon semiconductor professionals.

In addition to organising and managing your webinar, we can also market your webinar to our specialist databases.

In a dedicated 6 week program we will promote through our magazine, newsletters, LinkedIn group and website.

We can also provide the webinar moderator, from our team of highly respected editors.

Let our editors work with you and help you with the content.

Reach Educate Influence

- **Brand Awareness**
  Increase global awareness by running sponsored webinars, Zoom interviews and virtual events
- **Lead Generation**
  Generate and mature leads through the use of online events.
- **Thought Leadership**
  Become the voice of knowledge by generating compelling content via online events

SILICON SEMICONDUCTOR

Find out how Angel Webinars can help you organise and run a webinar within the silicon semiconductor industry.
Contact: Jackie Cannon
jackie.cannon@angelbc.com
+44 (0)1923 690205

SEMI and ESIA rally political support for a European semiconductor strategy

Seeking to explore semiconductor policy measures that can strengthen the industrial policy in the European Union, SEMI and the European Semiconductor Industry Association (ESIA) have successfully held a high-level roundtable event in the European Parliament under the auspices of Members of the European Parliament (MEPs) Bart Groothuis (Renew Europe), Oliver Schenk (European People's Party) and Dan Nica (Socialists and Democrats Party).

THE 2023 European Chips Act marked an important milestone for Europe's semiconductor industry and overall industrial ecosystem, providing concrete measures to enhance competitiveness and technological capabilities. In order to build on the success of the Chips Act, after the roundtable, MEPs signed a joint declaration to the European Commission's Executive Vice President for Tech Sovereignty, Security and Democracy, Henna Virkkunen, calling for an ambitious follow-up to the Chips Act that adds new research and development (R&D) funds, attracts new investments, and increases European competitiveness.

"The creation of a new European semiconductor strategy was a focal point of the discussion today, emphasising on the increasing need to boost the technological capabilities and accelerate innovation across the European semiconductor ecosystem," said Laith Altimime, President, SEMI Europe. SEMI and ESIA strongly appreciate the ongoing initiatives of European policymakers, together with the progress already made to bolster the European semiconductor ecosystem. Nevertheless, considering the existing concerns and challenges of our industry raised today, the European semiconductor ecosystem requires a holistic approach that decisively supports semiconductor design and manufacturing, R&D, materials and equipment capabilities.

ESIA Vice-President Frédérique Le Grevès underlined: "Our sector sees three priorities: We need a clear European semiconductor strategy that is backed by a revised European Chips Act with more quickly advancing administrative procedures. Secondly, we must identify the right approach to trade and foreign policy leading to more resilience, and thirdly, continue our focus on fostering innovation."

SEMI and ESIA will continue to engage with relevant policymakers and stakeholders to create a policy framework that can strengthen the entire European semiconductor supply chain while preserving technological competitiveness.

SEMI Silicon Photonics Industry Alliance launches Special Interest Groups

The SEMI Silicon Photonics Industry Alliance (SiPhIA) recently held the Bridging Light & Silicon: SEMI SiPhIA SIGs Kick-off & Seminar, announcing the

official launch of three Special Interest Groups (SIGs) aimed at integrating expertise from various sectors to formulate industry standards and accelerate technological innovation and commercialization. Mr. K.C. Hsu, Vice President of TSMC, and Dr. C.P. Hung, Vice President of ASE, attended as co-chairs of SEMI SiPhIA and delivered speeches to guide the SIGs. The seminar gathered over 200 industry leaders and experts to discuss the development of silicon photonics technology and the layout of global supply chain.

Silicon photonics has become a key technology driving the development of artificial intelligence (AI) due to its advantages in high-speed data transmission, high bandwidth, low power consumption, and high integration. However, it still faces challenges in manufacturing processes, packaging and testing to meet the rapidly increasing demand for data transmission. These challenges include shrinking chip sizes, reducing costs, minimizing energy loss in photonic integrated circuits, integrating photonic chips with advanced packaging, and developing effective solutions for heat dissipation. To overcome these challenges, SEMI SiPhIA established three SIGs to accelerate breakthroughs and commercialization of silicon photonics technology.

"The SEMI Silicon Photonics Alliance, centered on Taiwan's semiconductor industry, brings together over 110 leading domestic and international companies to develop the world's largest and most comprehensive international platform for silicon photonics technology collaboration," said Terry Tsao, Global Chief Marketing Officer and President of Taiwan, SEMI. "The alliance spans the entire supply chain, integrating cross-enterprise and cross-disciplinary expertise to fuel global innovation. Additionally, it has launched three SIGs focused on driving innovative technology breakthroughs and accelerating standardization efforts to jointly address the challenges posed by technological fragmentation."

The Three SIGs Integrating Industry and Research to Establish a Complete Ecosystem, Focusing on Technological Breakthroughs and Commercialization
SEMI established the SiPhIA in September 2024 to advance silicon photonics technology. The alliance has formed three SIGs, spanning the entire industry ecosystem from system design and component manufacturing to packaging and testing.

- **SIG 1: System, Subsystems, and Silicon Photonics Technology Development,** focusing on the future development trends in silicon photonics technology, including the design, manufacturing, and integration of silicon photonics chips, forming a complete silicon photonics ecosystem.
- **SIG 2: Advanced Packaging and Testing**, focusing on heterogeneous integration and co-packaged optical application packaging and testing technologies, driving optical-electronic integration.
- **SIG 3: Equipment and Others,** dedicated to developing and providing key equipment and technologies needed for the silicon photonics industry, focusing on process automation, including assembly, inspection technologies, and related equipment and innovative applications.

"TSMC will collaborate with the industry to develop a comprehensive roadmap for silicon photonics co-packaging solutions and work diligently to put it into practice," said K.C. Hsu, Vice President of TSMC and Co-Chair of SEMI SiPhIA. "We aim to overcome the technical bottlenecks by collaborating with alliance members through SIGs on cross-group projects to address specific technological challenges or application scenarios."

"ASE has been deeply involved in silicon photonics technology development for over 15 years," said C.P. Hung, Vice President of ASE and Co-Chair of SEMI SiPhIA. "We will collaborate with alliance members through regular cross-group SIGs meetings and establish a shared database to ensure that the technological development strategies of different SIGs align with market demands and facilitate cooperation."

"SEMI SiPhIA has successfully connected the industry and research sectors," said Wei-Chung Lo, Deputy General Director of Electronic and Optoelectronic System Research Laboratories at ITRI and Vice President of the SEMI SiPhIA. "ITRI has long been committed to silicon photonics technology research and development and plays a bridging role within the alliance, promoting the integration of research outcomes with industry demands to accelerate technology commercialization.

Outlook for Silicon Photonics Technology Development Roadmap for 2024 to 2027: Advancing from 2D to 3D Structures to Significantly Improve Energy Efficiency and Meet AI and Data Center Demands
Silicon photonics technology is regarded as a key technology for next-generation signal transmission. By integrating optical components onto silicon chips, this technology significantly enhances data transmission rates and reduces power consumption, addressing the growing demands for higher bandwidth and lower latency in data centers, 5G networks, high-performance computing, and other applications. The key discussion points of the SEMI SiPhIA include the 2024-2027 silicon photonics technology blueprint. It is expected that the technology will gradually evolve from 2D planar structures to 2.5D and 3D structures, significantly reducing energy consumption. As integration increases and energy efficiency improves, it will effectively meet the growing demands of high-speed data centers and AI computing.
Taiwan has laid a solid industrial foundation with its

complete supply chain ecosystem and advanced packaging technology in the semiconductor industry. SEMI will continue to build various open platforms and integrate cross-disciplinary expertise to assist the industry in formulating clear development strategies and collaboratively promoting technological innovation.

Global fab equipment investment to reach $110 billion

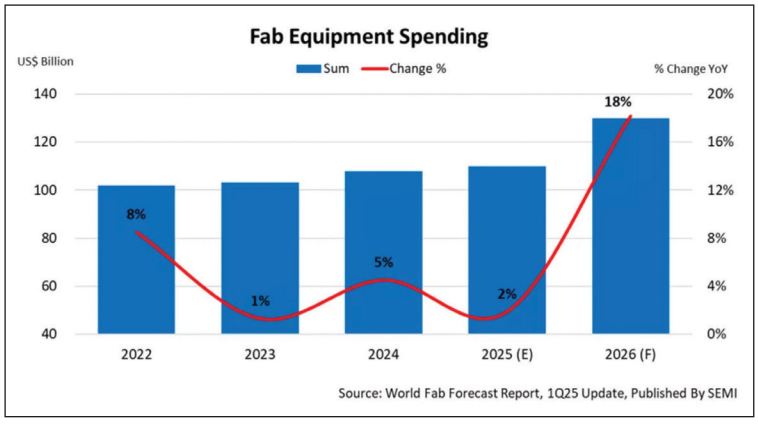
Global fab equipment spending for front-end facilities in 2025 is anticipated to increase by 2% year-over-year (YoY) to $110 billion, marking the sixth consecutive year of growth since 2020, SEMI announced in its latest quarterly World Fab Forecast report.

Fab equipment spending is projected to rise by 18% in the following year, reaching $130 billion. This growth in investment is driven not only by demand in the high-performance computing (HPC) and memory sectors to support data center expansions, but also by the increasing integration of artificial intelligence (AI), which is driving up the silicon content required for edge devices.

"The global semiconductor industry's investments in fab equipment have been edging up for six straight years, and spending is poised to see a strong 18% increase in 2026 as production ramps to meet booming AI-related chip demand," said Ajit Manocha, SEMI President and CEO. "This forecasted capex growth signals an urgent need for intensified workforce development initiatives throughout 2025 and 2026 to deliver skilled workers necessary for the approximately 50 new fabs expected to come online during these two years."

Logic & micro segment lead semiconductor industry expansion

The Logic & Micro segment is anticipated to be a key driver of growth in fab investments. This growth is primarily fueled by investments in cutting-edge technologies, such as 2-nanometer process and backside power delivery technology, which are expected to enter production by 2026. The Logic & Micro segment is projected to see an 11% increase in investments, reaching $52 billion in 2025, followed by a 14% increase to $59 billion in 2026.



Overall Memory segment spending is expected to grow steadily the next two years, increasing by 2% to reach $32 billion by 2025, with an even stronger growth forecast of 27% in 2026. Investments in the DRAM segment are projected to decline by 6% year-over-year, totaling $21 billion in 2025, but are anticipated to rebound with a 19% increase to $25 billion in 2026. Conversely, NAND segment spending is expected to recover significantly, rising by 54% year-over-year to $10 billion in 2025, and further increasing by 47% to $15 billion in 2026.

China continues to lead in regional fab equipment spending

Despite a decline from a peak of $50 billion in 2024, China is expected to maintain its position as the leader in global semiconductor equipment spending, with projections of $38 billion in 2025 representing a 24% year-over-year decrease. By 2026, spending is forecast to decline further 5% year-over-year to $36 billion.

With the growing penetration of AI technology driving higher memory adoption, Korean chipmakers are planning to invest more in equipment for capacity expansion and technology upgrades, which is expected to position the region as the second highest spending through 2026. Korean investment is forecasted to grow by 29% to $21.5 billion in 2025 and by 26% to $27 billion in 2026.

Taiwan is set to secure third place in spending as its chipmakers aim to enhance their leadership in advanced technology and production capabilities. Taiwan is projected to spend $21 billion in 2025 and $24.5 billion in 2026 to meet the growing demand for AI applications across cloud services and edge devices.

The Americas region ranks fourth, with expected spending of $14 billion in 2025 and $20 billion in 2026. Japan, Europe and the Middle East, and Southeast Asia follow in investments, projected to spend $14 billion, $9 billion, and $4 billion in 2025, and $11 billion, $7 billion, and $4 billion in 2026, respectively.

The latest update of the SEMI World Fab Forecast report, published in March, lists more than 1,500 facilities and lines globally, including 156 facilities and lines with various probabilities expected to start operation in 2025 or later.

Global semiconductor equipment billings surged to $117 billion in 2024

Worldwide sales of semiconductor manufacturing equipment increased 10% to $117.1 billion in 2024 from $106.3 billion in 2023, SEMI has reported. The data is now available in the Worldwide Semiconductor Equipment Market Statistics (WWSEMS) report.

In 2024, the global front-end semiconductor equipment market experienced notable growth, with

sales of wafer processing equipment increasing by 9% and other front-end segments rising by 5%. This growth was largely fueled by heightened investments in expanding capacity for both leading-edge and mature logic, advanced packaging, and high-bandwidth memory (HBM), alongside a significant rise in investments from China.

The back-end equipment segment, after two consecutive years of decline, saw a robust recovery in 2024, driven by the increasing complexity and demands of AI and HBM manufacturing. Assembly and packaging equipment sales increased by 25%, while test equipment billings rose by 20% year-over-year, reflecting the industry's push toward supporting advanced technologies.

"The global semiconductor equipment market surged by 10% in 2024, rebounding from a slight dip in 2023 to reach an all-time high of $117 billion in annual sales," said Ajit Manocha, SEMI President and CEO. "Industry spending on chipmaking equipment in 2024 reflects a dynamic landscape shaped by regional investment trends, technological advancements in logic and memory, and the rising demand for chips related to AI-driven applications."

Regionally, China, Korea, and Taiwan remained the top three markets for semiconductor equipment spending, collectively accounting for 74% of the global market. China solidified its position as the largest semiconductor equipment market, with investments surging 35% year-over-year to $49.6 billion, driven by aggressive capacity expansion and government-backed initiatives aimed at bolstering domestic chip production.

Korea, the second-largest market, saw a modest 3% increase in equipment spending, reaching $20.5 billion, as memory markets stabilized and demand for high-bandwidth memory soared. In contrast, Taiwan experienced a 16% decline in equipment sales, falling to $16.6 billion, reflecting a slowdown in demand for new capacity.

Elsewhere, North America recorded a 14% rise in semiconductor equipment investments, reaching $13.7 billion, driven by increased focus on domestic manufacturing and advanced technology nodes.

The Rest of the World saw a 15% increase, with billings at $4.2 billion, supported by emerging markets ramping up chip production. However, Europe faced a significant 25% decline in equipment spending, falling to $4.9 billion, due to weakened demand in the automotive and industrial sectors amid economic challenges. Japan also saw a slight 1% dip, with sales at $7.8 billion, as the region grappled with slower growth in key end markets.

Compiled from data submitted by members of SEMI and the Semiconductor Equipment Association of Japan (SEAJ), the WWSEMS report is a summary of the monthly billings figures for the global semiconductor equipment industry.

Semiconductor Equipment Market Revenue by Region
(U.S. Dollars in Billions)

Region	2024	2023	(YoY) %
China	$49.55	$36.60	35%
Korea	$20.47	$19.94	3%
Taiwan	$16.56	$19.62	-16%
North America	$13.69	$12.05	14%
Japan	$7.83	$7.93	-1%
Europe	$4.85	$6.46	-25%
Rest of the World	$4.19	$3.65	15%
Total	**$117.14**	**$106.25**	**10%**

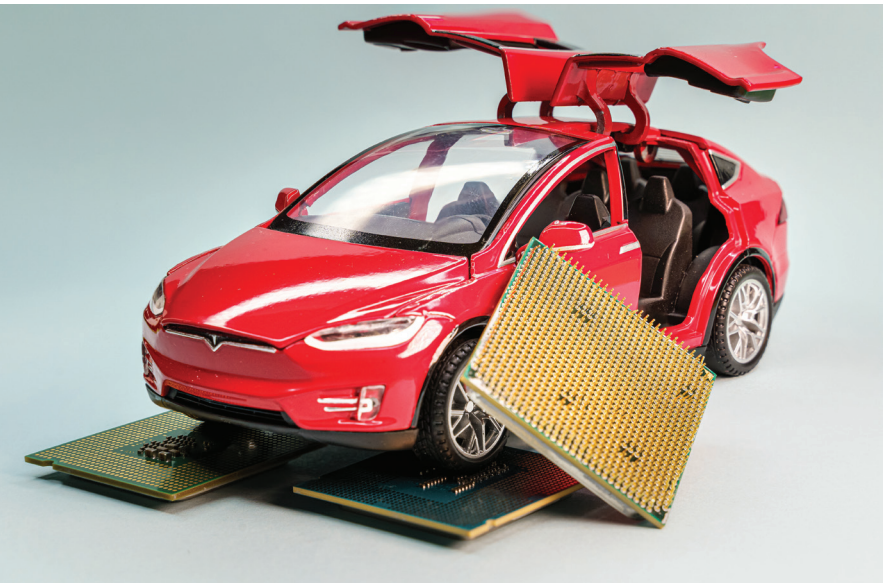
Sources: SEMI (www.semi.org) and SEAJ (www.seaj.or.jp), April 2025
Note: Summed subtotals may not equal the total due to rounding.

European chips skills academy launches ECS summer school

The European Chips Skills Academy (ECSA), an EU-funded project coordinated by SEMI Europe, in collaboration with industry partners AENEAS, EPoSS, and INSIDE, has launched the ECS Summer School 2025. The five-day event themed 'Fascinating Electronics for a Cool World' is designed to inspire and attract new talent to Europe's electronic components and systems sector. This year's session will take place at the Budapest University of Technology and Economics in Hungary from August 24-29, 2025. The program will feature interactive workshops, expert-led discussions, networking sessions, and practical insights into cutting-edge microelectronics and semiconductor technologies. Students enrolled in STEM-related fields from universities across the EU or associated countries are invited to apply until 30 April 2025.

"Initiatives like the ECS Summer School are crucial for inspiring and nurturing the next generation

"The global semiconductor equipment market surged by 10% in 2024, rebounding from a slight dip in 2023 to reach an all-time high of $117 billion in annual sales. Industry spending on chipmaking equipment in 2024 reflects a dynamic landscape shaped by regional investment trends, technological advancements in logic and memory, and the rising demand for chips related to AI-driven applications"



of talent fueling the talent pipeline," said Laith Altimime, President of SEMI Europe.

By engaging directly with leading experts, students will acquire skills and insights essential for their future roles in Europe's rapidly evolving technology landscape.

"The ECS Summer School is an excellent gateway for students to gain practical knowledge and establish valuable industry connections," said Patrick Cogez, Technical Director at AENEAS and lead partner in ECSA for the organisation of the Summer School.

SEMI Europe recognizes NXP and Okmetic leaders

SEMI Europe announced the winners of the SEMI European Award and Special Service Award for 2024 at the SEMI Industry Strategy Symposium Europe (ISS Europe) 2025. Kurt Sievers, President and CEO of NXP Semiconductors, was honored with the SEMI European Award and Anna-Riikka Vuorikari-Antikainen, Chief Commercial Officer of Okmetic, received the Special Service Award.

For over 30 years, these prestigious awards have celebrated influential figures within the semiconductor industry, recognizing their exceptional leadership and strategic contributions that push technological progress forward.

"At SEMI Europe we are honored to recognize the exemplary contributions of Kurt Sievers and Anna-Riikka Vuorikari-Antikainen," said Laith Altimime, President of SEMI Europe. "Their forward-thinking leadership not only sets the standard for the industry but also drives transformative advancements that benefit the entire semiconductor ecosystem.

Their accomplishments serve as a beacon of innovation and resilience, inspiring peers and future leaders alike to push boundaries and pursue a more sustainable, technologically advanced future." Kurt Sievers has been recognized for his exemplary leadership in driving NXP Semiconductors' expansion. A key milestone in his career was the successful merger of NXP and Freescale Semiconductor, which strengthened the company's position as a global leader in automotive semiconductors and secure edge processing.

"I am truly honored and humbled to receive the SEMI European Award for 2024," said Sievers. "I view this award as less a personal achievement, but mainly a testament to the collective efforts and dedication of the global NXP team as we work to become the leader in bringing intelligent systems to the edge. My gratitude goes to SEMI Europe for this prestigious honor."

Anna-Riikka Vuorikari-Antikainen has been recognized for her dedicated contributions to the semiconductor industry. She has played a vital role in understanding the needs of device manufacturers and developing pioneering substrate solutions. Her achievements have enabled advancements in multiple areas including the development of cavity SOI wafers for MEMS devices, high-resistivity wafers for RF applications, and specialised templates for III-N on silicon growth.

"I am truly honored to receive the SEMI Europe Special Service Award, a remarkable recognition of Okmetic's close collaboration with SEMI and our commitment to advancing Europe's semiconductor industry," says Vuorikari-Antikainen. "As we mark our 40th anniversary, we remain committed to driving innovation with cutting-edge silicon solutions for MEMS, RF, and Power devices. Our ongoing capacity expansion, combined with the dedication of our team and our strong partnerships across the semiconductor ecosystem, ensures we continue to contribute to the industry's progress." Nominations for the 2025 SEMI European Award are open. Please see the award guidelines. Prior SEMI European Award recipients hailed from companies including Schneider Electric, ASM, Melexis, imec, Soitec, CEA-Leti, Technical University of Dresden, Catholic University of Leuven, STMicroelectronics, EV Group, Infineon, and the Fraunhofer Institute.

CLEAN AIR

CLEAN ROOMS

COMPONENTS

ETCH

FLOW MEASUREMENT

GAS DELIVERY SYSTEMS

GAS PURIFIERS

HYDROGEN GENERATORS

FLUID SYSTEMS

PLASMA TECHNOLOGY

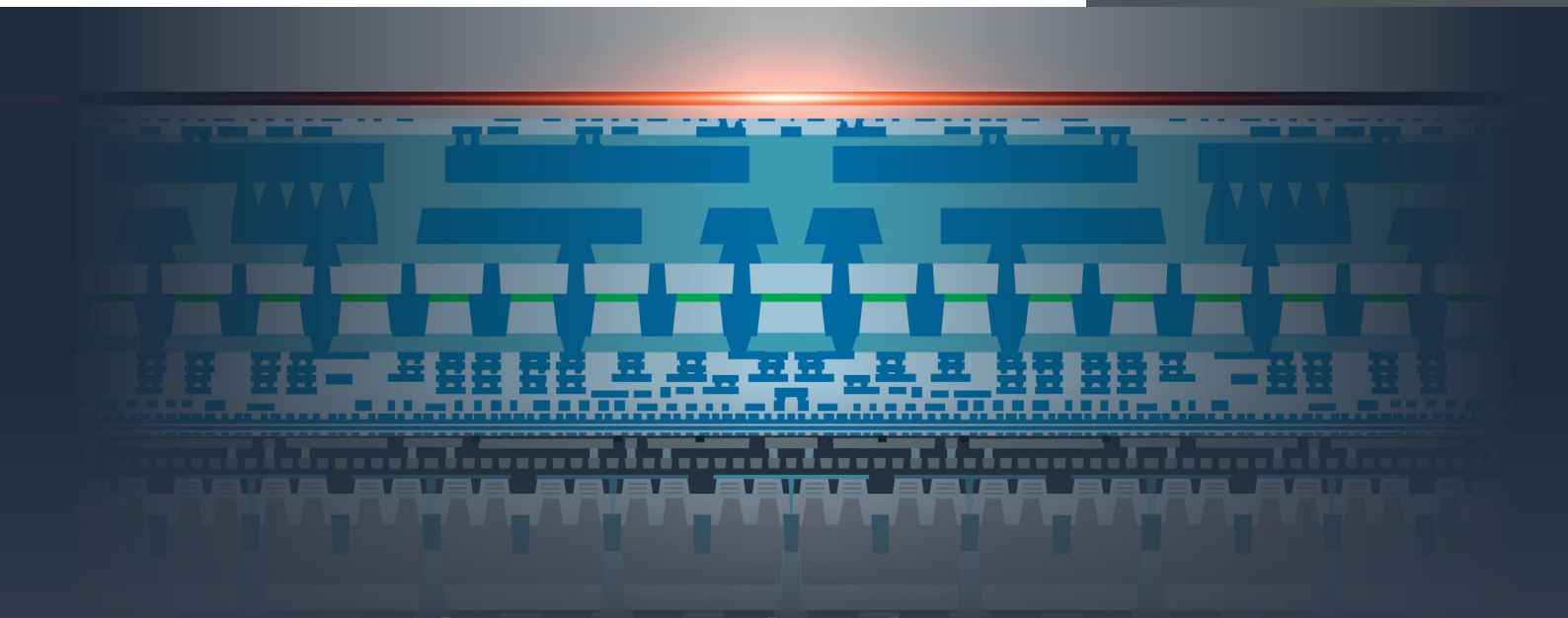
TEST

VACUUM EQUIPMENT

EVG®

invent
innovate
implement

www.EVGroup.com



IR LayerRelease™ Technology

- Replacement for mechanical debonding thanks to through-silicon IR laser
- Enabling ultra-thin film or layer transfer from silicon carriers
- Nanometer-precision release of bonded, deposited or grown layers
- Front-end compatibility through silicon carriers and inorganic release materials
- Supporting future roadmaps in advanced packaging and transistor scaling

EVG®880 LayerRelease™

GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com