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## BEYOND HIGH-NA EUV

Particle accelerator technology promises exciting future for lithography

# VIEWPOINT

BY PHIL ALSOP
EDITOR

## Light at the end of the High-NA EUV tunnel?

THE SEMICONDUCTOR INDUSTRY has always advanced on the back of bold, often improbable, technological pivots. From deep ultraviolet to EUV, each leap has required not only engineering excellence but a willingness to rethink the fundamentals of lithography. Today, as High-NA EUV edges toward its practical and economic limits, the industry finds itself at another such inflection point.

The proposition outlined by TAU Systems is striking precisely because it does not attempt to extend the current roadmap in incremental fashion. Instead, it challenges one of lithography's most entrenched assumptions: that the light source must remain a plasma-based, largely incoherent emitter constrained to a narrow wavelength band. By introducing compact, laser wakefield acceleration (LWFA)-driven free-electron laser concepts - rooted in work demonstrated at facilities such as SLAC National Accelerator Laboratory and European XFEL - this approach reframes the problem at its origin: photon generation.

If realised, the implications are substantial. Brightness and coherence are not just performance metrics; they are enablers of entirely new patterning regimes. A tunable source, in particular, could decouple the rigid interdependencies that have defined EUV's "Goldilocks zone," potentially easing constraints on resist chemistry and mirror design. This alone could unlock a degree of flexibility that the industry has not enjoyed in decades.

Equally striking is the economic dimension. Today's EUV ecosystem, dominated by players such as ASML, represents one of the most capital-intensive manufacturing environments ever created. Any credible successor technology must not only outperform EUV in resolution but also compete on cost, energy efficiency, and fab integration. The promise of a compact, container-scale source directly addresses these pressures, suggesting a future where

lithography scaling is not synonymous with exponential cost escalation.

However, the path from laboratory physics to high-volume manufacturing is notoriously unforgiving. Stability, uptime, and throughput - not peak performance - will ultimately determine viability. The industry has learned this lesson before with EUV itself, whose decades-long maturation underscores the scale of the challenge ahead.

Yet the timing of this exploration is not coincidental. AI-driven demand is compressing development cycles and amplifying the cost of stagnation. Multi-patterning, already a burden, is becoming untenable at advanced nodes. In that context, the appeal of a fundamentally new light source paradigm is clear.

Whether LWFA-based systems become the successor to High-NA EUV remains uncertain. What is increasingly certain, however, is that the next chapter of Moore's Law will be written not just through better optics, but through a reimagining of how light is created, controlled, and deployed within the fab.

# CONTENTS



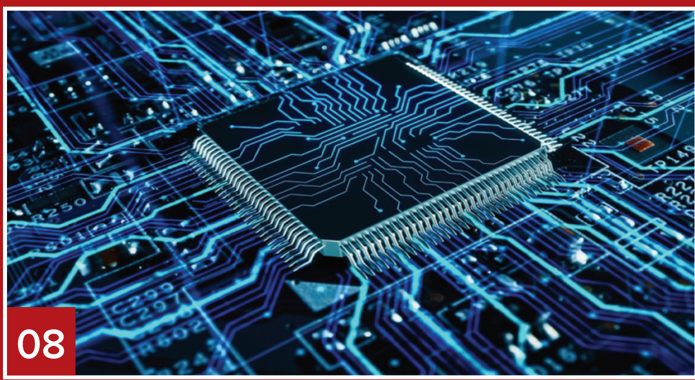
SILICON SEMICONDUCTOR

# COVER STORY

## Beyond High-NA EUV: particle accelerator technology promises exciting future for lithography

# NEWS





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# AI compute boom propels Foundry 2.0 market to $360 billion

**According to IDC's latest Global Semiconductor Supply Chain Tracking Intelligence, the broadly defined Foundry 2.0 market, comprising pure-play foundry, non-memory IDM, outsourced semiconductor assembly and test (OSAT), and photomask fabrication, is projected to surpass USD 360 billion in 2026, representing 17% year-over-year growth.**

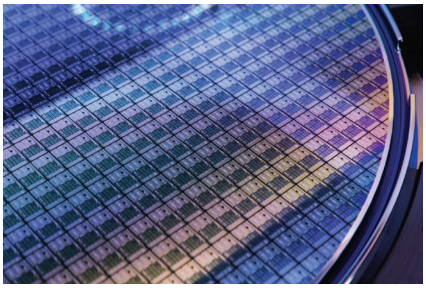
"THE FOUNDRY 2.0 market is entering a steady expansion cycle driven by AI in 2026. Advanced nodes and advanced packaging remain in short supply, while mature nodes are finally leaving behind the era of price competition, supported by accelerating 8-inch capacity reductions and resilient demand growth from AI power-related chips." said Galen Zeng, senior research manager at IDC Asia/Pacific.

**Foundry Industry: TSMC Dominates Advanced Nodes, Mature Node Pricing Cycle Rebounds**

Advanced node foundry is benefiting from strong demand from AI GPU and ASIC customers including NVIDIA, AMD, and Broadcom. Leading foundry, TSMC, has raised its 3nm monthly capacity target to 165,000 wafers and CoWoS monthly capacity to 125,000 wafers, with wafer pricing also raised by more than 5%. Supported by sustained full utilization at 3nm, the ramp of 2nm, and CoWoS advanced packaging order spillover, TSMC is expected to further expand its foundry market share to 44% in 2026.

Samsung Foundry is also benefiting from gradually improving SF2 process yields, with the Exynos 2600 mobile processor and cryptocurrency mining chips entering supply, and 4nm HBM4 base die production commencing, driving higher advanced node utilization. On the customer front, Samsung holds a USD 16.5 billion long-term agreement with Tesla and has secured orders for AI accelerators including NVIDIA Groq 3 LPU, with order momentum recovering and overall operational trajectory improving.

On the mature node side, as both TSMC and Samsung initiate 8-inch capacity reductions and other mature



node players plan 8-inch capacity optimization, global 8-inch total capacity is expected to decline approximately 3% year-over-year in 2026, marking a reversal in supply-demand dynamics. Continued strong demand for server Power ICs and Power Discrete components has prompted select foundries to raise wafer pricing by up to 10%, ending the post-pandemic race-to-the-bottom pricing environment. Overall, IDC forecasts the foundry market to grow 24% year-over-year in 2026.

**Non-Memory IDM: Intel 18A Enters Production, Automotive and Analog IDM Supply-Demand Dynamics Improve**

The non-memory IDM manufacturing segment is recovering in 2026, with estimated year-over-year growth of 5%. Intel is accelerating its process roadmap. The Panther Lake processor completed its first volume production shipments in late 2025, and the Clearwater Forest data center processor was officially unveiled at MWC 2026, marking the full entry of the 18A product line into mass production.

On the external customer front, Intel's 12nm collaboration with UMC is actively engaging potential customers for tape-outs, while leading US HPC companies have begun evaluating the 18A-P process, further supporting Intel's gradual expansion of its customer base.

European automotive IDMs including Infineon, NXP, and STMicroelectronics have completed inventory corrections, with demand expected to gradually recover. Some players are also adopting "China for China" localized manufacturing as a strategic option to manage geopolitical risk, deepening their presence in the Chinese market through joint ventures or contract manufacturing with domestic fabs, generating additional growth momentum. Among US IDMs, Texas Instruments continues to see industrial demand recovery, with automotive business maintaining steady growth.

**OSAT Industry: CoWoS Spillover Accelerates ASE Order Intake, OSATs Compete for Advanced Packaging Opportunities**

The OSAT segment is projected to grow 15% year-over-year in 2026, supported by recovery in both advanced and mainstream packaging markets. The AI chip integration trend continues to elevate the value-add of advanced packaging, with back-end packaging design and system integration now rivaling front-end wafer fabrication in strategic importance. ASE Technology Holding (ASE) is a key driver of the current AI packaging wave, with growth momentum primarily stemming from sustained CoWoS capacity shortfalls at TSMC and the gradual increase in outsourcing share, driving continued volume ramp in on-substrate packaging (oS) and chip probe (CP).

Looking ahead, post-package test (FT/SLT) and full-process packaging are expected to become the next growth engines, with AI CPU and AI ASIC products progressively entering the pipeline and further expanding ASE's growth runway in advanced packaging.

# Gartner forecasts worldwide semiconductor revenue to exceed $1.3 trillion in 2026

Global semiconductor revenue is projected to exceed $1.3 trillion in 2026, exhibiting the highest growth in the last two decades, according to Gartner, Inc., a business and technology insights company.

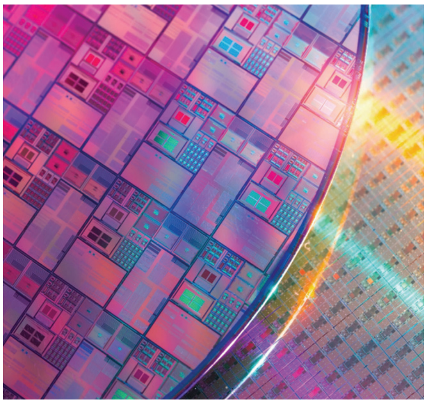
"AMID high demand for AI processing, data center networking and power, and memory price inflation (memflation), the semiconductor industry is projected to achieve a third consecutive year of double-digit growth in 2026 – a milestone that underscores the sector's pivotal role in the AI technology stack," said Rajeev Rajput, Senior Principal Analyst at Gartner.

Gartner forecasts semiconductor revenue will grow 64% in 2026, with memory revenue expected to increase threefold amid memflation (see Table 1). Gartner analysts said that memflation is profound, but it is not perennial. Gartner estimates DRAM and NAND flash annual prices in 2026 will increase by 125% and 234%, respectively, and any meaningful pricing relief is not expected until late 2027.

"Memflation will destroy, or at least delay, non-AI demand into 2028, to varying degrees depending on the application," – Rajeev Rajput, Senior Principal Analyst at Gartner

AI Semiconductors Will Represent 30% of Total Semiconductor Revenue in 2026

AI semiconductors are expected to account for approximately 30% of total semiconductor revenue in 2026 and will remain the driving force behind the overall industry growth. Hyperscaler investment in AI infrastructure buildouts

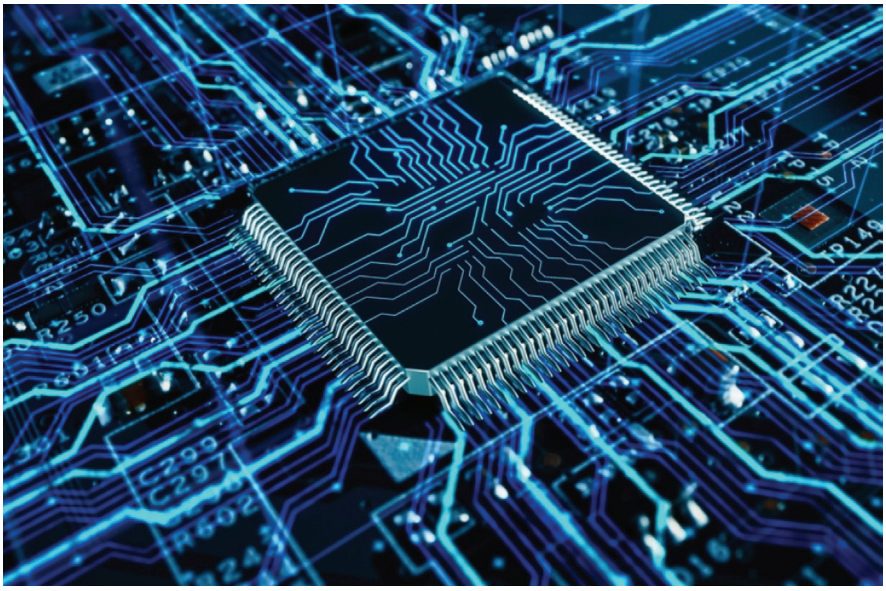


remains strong with spending expected to increase by more than 50% in 2026, driving demand for AI accelerators, including GPUs and custom non GPU chips.

# Innatera selects Synopsys simulation

Innatera adopts Synopsys simulation technology to help design neuromorphic chips that enable low-power AI for wearables, smart home devices, and digital twin industrial sensors.

INNATERA, a leader in brain-like neuromorphic computing for ultra-low-power intelligence at the sensor edge, has selected Synopsys for design and validation of its next-generation neuromorphic microcontrollers. Synopsys' reliable solutions for electrostatic discharge (ESD) and power integrity analysis will help Innatera scale its operations to meet the growing demand for edge processing in industrial sensors, robotics, wearables, and smart home technologies.



Neuromorphic microcontrollers process information through Spiking Neural Networks (SNNs) that mimic how biological neurons communicate, delivering brain-inspired intelligence at the sensor edge. This event-driven approach enables real-time, ultra-low-power operation in sensor-rich environments where responsiveness and energy efficiency are critical. Innatera's architecture combines mixed-signal analog computation, dense interconnects, and low-voltage design — key enablers of efficiency but potential sources of electrical noise and ESD sensitivity.

To address these challenges and ensure robust performance across complex neuromorphic circuits, Innatera leverages PathFinder-SC and Totem to validate power integrity, manage noise coupling, and maintain reliability without compromising speed or efficiency.

PathFinder-SC simulates ESD events at scale, identifying vulnerabilities and root causes before the final design goes to manufacturing and ensuring chips are functioning optimally against real-world electrostatic occurrences. It also provides early, high-fidelity modeling of analog behavior, empowering designers to validate performance under diverse conditions.

Totem performs detailed power integrity analysis at the transistor level, ensuring reliable power delivery and optimal performance for highly efficient AI tasks. By pairing Totem's high-fidelity modeling of typical operating conditions with PathFinder-SC's capacity to identify and address ESD risks, the solution provides designers with a comprehensive reliability tool — one that protects against both expected and unexpected electrical challenges throughout the chip's life cycle and is backed by robust technical support.

"Innatera's mission to redefine edge AI through neuromorphic computing requires both technological innovation and reliable design collaboration," said Aditya Dalakoti, director of SoC and mixed-signal at Innatera. "Synopsys stood out for its leading technology and unwavering support for startups in the edge AI ecosystem. Its ESD analysis solution and collaborative approach enable us to scale into real-world, adaptive applications with enhanced speed, usability, and versatility."

For example, Innatera used Synopsys technology to validate the design of Pulsar, the world's first commercial neuromorphic microcrontroller. Pulsar optimizes AI workloads at the edge by combining flexible computing architecture, resulting in up to 100x lower latency and 500x lower energy consumption than conventional AI processors. Using SNNs, Pulsar only reacts to registered sensor changes, significantly improving data transfer speeds and battery power for "always-on" devices like wearables and smart sensors.

"By enabling Innatera to accelerate product development and scale confidently, Synopsys reinforces its role as a catalyst for cutting-edge technologies shaping the future of embedded AI," said Prith Banerjee, senior vice president at Ansys, part of Synopsys."

"This collaboration underscores our commitment to empowering innovation across the semiconductor ecosystem, from global enterprises to emerging startups. As edge computing becomes increasingly central to real-time intelligence, Synopsys simulation is helping innovators bring efficient AI where it's most needed."

# Axelera AI secures more than $250 million funding

European AI semiconductor leader earns backing from funds managed by Innovation Industries and SiteGround Capital along with EU institutions; edge-first architecture addresses AI's critical energy and cooling constraints.

AXELERA AI, a European leader in AI acceleration hardware, announced its latest funding round led by Innovation Industries, with participation from prominent funds and accounts including BlackRock and SiteGround Capital as new investors, as well as existing investors Bitfury, CDP Venture Capital, European Investment Council Fund, Federal Holding and Investment Company of Belgium (SFPIM), Invest-NL, Samsung Catalyst Fund, and Verve Investments. Axelera AI has attracted over $450 million in equity, grants and venture debt since incorporating in July 2021.

What is said to be the largest investment ever in an EU AI semiconductor company comes as Axelera ships to its 500th global customer across physical AI and edge AI in industries including defense and public safety, industrial manufacturing, retail, agritech, robotics, and security, firmly establishing the company as the global leader in power-efficient AI inference solutions.

Axelera AI's success is rooted in a fundamental insight: to deploy AI at scale, the industry must first solve for energy consumption and cooling requirements.

The company's edge-first architectural approach delivers uncompromising AI inference performance that fits within the power and thermal envelopes of real-world deployment environments to drive real business value. And by providing high performance at the edge, companies can process data locally, which preserves privacy for their users and supports the increasing demand for sovereign solutions.

"Data centers are hitting power and cooling limits, and as analytics move closer to where data is being created, edge AI solutions must operate within strict energy and bandwidth constraints," said Fabrizio Del Maffeo, CEO and co-founder of Axelera AI.

"We designed our architecture from the ground up to overcome these obstacles. Our edge-first approach isn't just about efficiency; it's about making AI deployment economically viable at scale for real-world applications while protecting data and privacy by processing customer information locally."

Inference is projected to be a more than $250B market by 2030.

Over the life of a model, the cost of inference is 15x more than training and utilization is growing at 31x per year. But many organizations still struggle to transition from AI projects to generating value in production.

Axelera's tightly co-designed hardware/software solution simplifies deployment and maximizes performance of inference-based workloads.

Axelera AI's Europa and Metis platforms deliver the price/performance balance enterprise customers need while operating within the energy and thermal constraints of edge computing. The edge AI semiconductor market has attracted over $60 billion in venture funding in just the past three years[iii], creating significant fragmentation and confusion for customers. Axelera AI's strong financial foundation, proven technology, customer traction, scaled manufacturing through partnerships with TSMC and Samsung, and growing ecosystem of software and integration partners position the company for long-term growth and success.

"Axelera is solving one of the most fundamental constraints in Edge AI adoption: the cost and energy efficiency of inference at scale," said Rogier Ketelaars, investment manager at Innovations Industries. "We believe the company is uniquely positioned to become a foundational player in the next generation of AI infrastructure, and we're excited to back the outstanding Axelera team that combines deep technical leadership and real commercial execution."

The funding round represents strong institutional validation of this architectural philosophy, with BlackRock's participation underscoring the financial community's recognition that solving AI's infrastructure constraints is critical to the technology's continued growth and market expansion.

# Siemens accelerates AI chip verification to trillion cycle scale with NVIDIA technology

**Siemens and NVIDIA have achieved a major verification breakthrough, capturing trillions of pre silicon design cycles in days using Siemens' Veloce proFPGA CS combined with NVIDIA's performance-optimized chip architecture.**


SIEMENS, in close collaboration with NVIDIA, says that its Veloce™ proFPGA CS hardware-assisted verification and validation system is empowering designers and system architects to create even more optimized designs by running and capturing trillions of verification cycles, prior to first silicon availability.

As part of their long-standing strategic partnership, NVIDIA and Siemens have mastered a task previously considered impossible, capturing tens of trillions of cycles over a span of just a few days by taking advantage of Siemens' Veloce proFPGA CS scalable and performance-optimized hardware architecture and combining it with NVIDIA's performance-optimized chip architecture.

"NVIDIA and Siemens are partnering in many areas, most recently in advancing hardware-assisted verification methodologies in general and FPGA-based prototyping in particular, to adapt to the verification and validation demands presented by highly complex AI/ML SoCs," said Jean-Marie Brunet, senior vice president and general manager, hardware assisted verification, Siemens Digital Industries Software.

"Veloce proFPGA CS is addressing these challenges by combining a highly flexible and scalable hardware architecture with an advanced, easy-to use implementation and debug software flow, enabling customers to always have the optimal solution for single-FPGA IP validation as well as for multi-billion gate chiplet designs."

"As AI and computing architectures grow increasingly complex, semiconductor teams require high-performance verification solutions to validate massive workloads and accelerate time to market," said Narendra Konda, vice president of hardware engineering, NVIDIA. "The integration of NVIDIA performance-optimized chip architectures with Siemens' Veloce proFPGA CS enables designers to capture trillions of cycles in days, providing the scale needed to ensure reliability for the next generation of AI."

Field-programmable gate array (FPGA) based prototype systems are fast and allow users to run pre-silicon verification workloads in a fraction of the time it would take to run the same workload in simulation or even emulation.

However, today's AI/ML designs are demanding even more, in part due to the chip complexity and in part due to the software complexity.

To scale to these industry demands, meet time-to-market and align to reliability requirements, the ability to run trillions of design cycles in a short amount of time is now critical.

Traditional verification tools like simulation and emulation do not scale beyond running millions, or best case a few billion cycles within a reasonable and practical amount of time.

> As AI and computing architectures grow increasingly complex, semiconductor teams require high-performance verification solutions to validate massive workloads and accelerate time to market. The integration of NVIDIA performance-optimized chip architectures with Siemens' Veloce proFPGA CS enables designers to capture trillions of cycles in days, providing the scale needed to ensure reliability for the next generation of AI

# New ZEISS Crossbeam 750 FIB-SEM designed for high-accuracy sample preparation workflows

**ZEISS has unveiled the new ZEISS Crossbeam 750 focused ion beam-scanning electron microscope (FIB-SEM) that is optimized for demanding sample preparation.**

IT provides a live, high-resolution "see while you mill" view at any imaging and milling condition to enable immediate feedback and eliminate milling interruptions for uniform first-pass transmission electron microscopy (TEM) lamellae and precise FIB cross sections.

For advanced semiconductor and materials workflows, ZEISS Crossbeam 750 FIB-SEM with new Gemini 4 electron optics delivers background-free, real-time endpointing and sub-nanometer precision for TEM lamellae and high-fidelity three-dimensional (3D) analysis. It is ideal for analysis of leading-node logic and memory devices as well as nanofabrication and 3D volume imaging. For materials research and life sciences, ZEISS Crossbeam 750 speeds acquisition times for 3D tomography through a larger field of view with reduced distortion.

"ZEISS Crossbeam 750 was designed around one core principle: Our customers should not have to stop milling to see where in their sample they are working," said Dr. Thomas Rodgers, Senior Director of Market Strategy, Head of Business Sector Electronics, ZEISS Microscopy. "Our new high dynamic range (HDR) Mill + SEM capability maintains a clear, high-resolution SEM view at any FIB condition, from rapid milling with high FIB currents down to fine polishing at 0.5 kV. This real-time clarity, paired with Gemini 4 electron optics, allows customers to fine-tune processes as they work—reducing rework, improving yield and delivering highly uniform lamellae on the first pass."

"See while you mill" transforms advanced semiconductor analysis

As semiconductor device architectures shrink and complexity increases—from fin field-effect transistor (finFET) to gate-all-around (GAA), complementary field-effect transistor (CFET) and emerging two-dimensional (2D) materials—precise, real-time control during FIB processing has become critical. ZEISS Crossbeam 750 directly addresses this need by maintaining a clear, high-resolution SEM view during milling, even at low landing energies and at tilt.

The system enables users to observe FIB-sample interactions in real time, fine-tune thinning and polishing steps as they occur, and to hit nanometer-scale endpoints on the first attempt—achieving consistent lamella quality for leading-node logic and memory device and backside power delivery network workflows.


ZEISS Crossbeam 750 FIB-SEM is essential in materials science workflows for uniform TEM lamella preparation, atom probe tomography (APT) sample preparation, nanofabrication (including electron-beam lithography) and high-fidelity 3D volume imaging. For life sciences and materials research, the undistorted large field of view of ZEISS Crossbeam 750 and its stable low-kV performance improve signal-to-noise ratio and speed acquisition time.

# SEMI projects double-digit growth in global 300mm fab equipment spending for 2026 and 2027

Worldwide 300mm fab equipment spending is expected to increase 18% to $133 billion in 2026 and 14% to $151 billion in 2027, SEMI reported in its latest 300mm Fab Outlook. This strong growth reflects surging AI chip demand for data centers and edge devices, as well as the growing commitment to semiconductor self-sufficiency across key regions through localized industrial ecosystems and supply chain restructuring.

LOOKING further out, the report projects investment will continue to increase 3% to $155 billion in 2028 and another 11% to $172 billion in 2029, respectively.

"AI is resetting the scale of semiconductor manufacturing investment," said Ajit Manocha, President and CEO of SEMI. "With global 300mm fab equipment spending projected to exceed $150 billion in 2027 for the first time, the industry is making historic, sustained commitments to the advanced capacity and resilient supply chains needed to power the AI era."

**Segment growth**

The Logic & Micro segment is expected to spearhead equipment expansion with $228 billion in total investments from 2027 to 2029 mainly due to strong foundry sector demand, driven by sub-2nm cutting-edge capacity investments. Advanced node technology is essential to enhance chip performance and power efficiency to meet rigorous chip design requirements for various AI applications. More advanced node technology is expected to enter volume production from 2027 to 2029. Additionally, AI performance improvements are anticipated to drive massive growth in various edge AI devices. Beyond advanced nodes, demand across all nodes and various electronics devices is anticipated to grow moderately, supporting investment in mature nodes as well.

The memory segment is projected to rank second in equipment spending, totaling $175 billion from 2027 to 2029. This period marks the start of a new growth cycle for the segment. Within the memory category, DRAM equipment spending is expected to reach $111 billion cumulatively from 2027 to 2029, while 3D NAND equipment spending is estimated to be $62 billion during the same time frame.

The demand for memory has significantly increased due to AI training and inference. AI training has notably driven up the demand for High Bandwidth Memory (HBM), while model inference has created substantial demand for storage capacity, thus boosting the growth of NAND Flash applications in data centers. This strong demand has led to sustained high levels of investment in the memory supply chain over the near and long term, helping to cushion potential downturns from traditional memory cycle fluctuations.

**Regional investment trends**

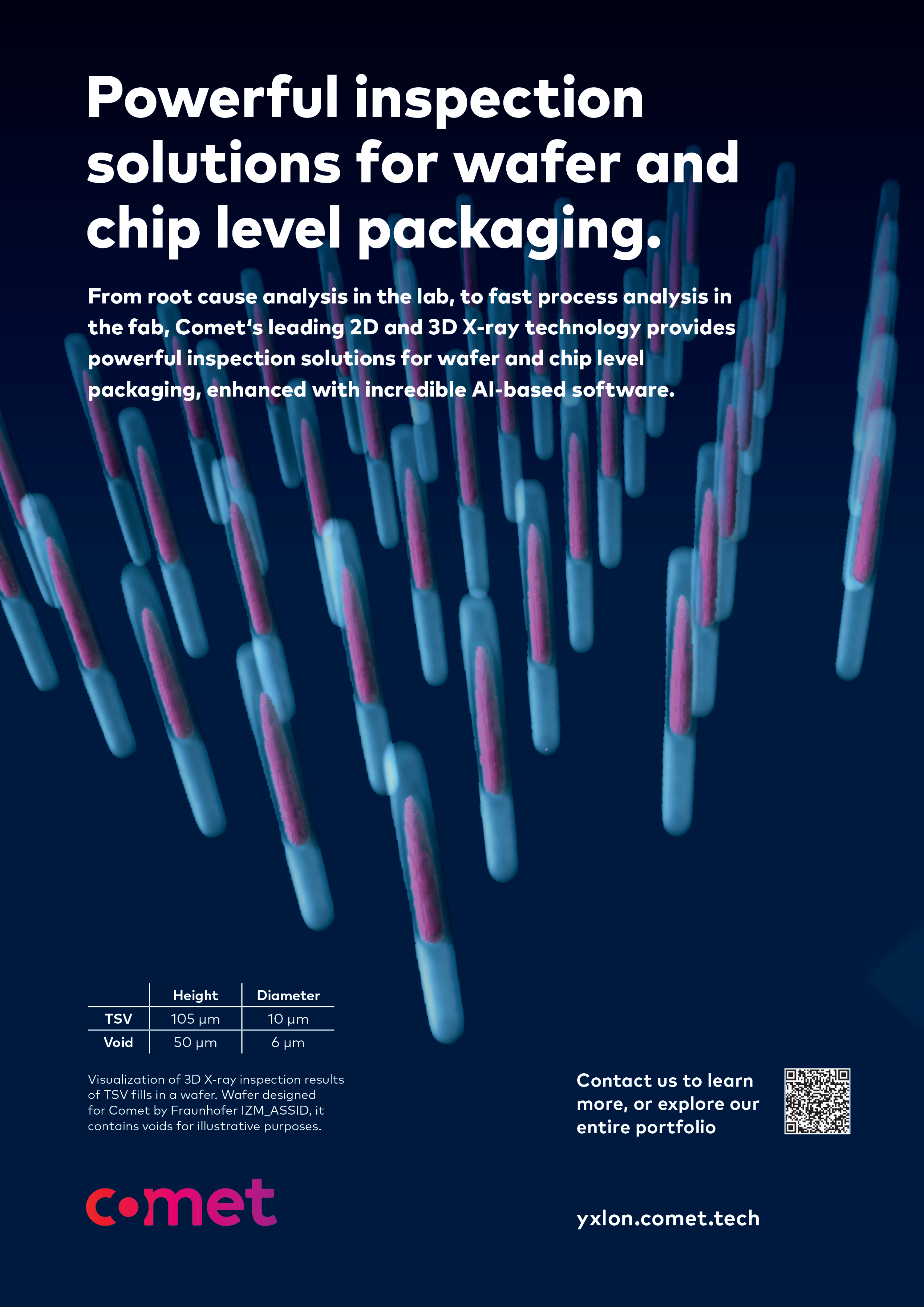
Global 300mm fab equipment investment is expected to remain broadly distributed across the major semiconductor manufacturing regions from 2027 to 2029, reflecting a mix of advanced-node expansion, memory capacity additions, and policy-supported supply chain localization. China, Taiwan, Korea, and the Americas are each expected to see substantial levels of spending during the period, while Japan, Europe & Middle East, and Southeast Asia also continue to expand investment from a smaller base.

In China, investment is expected to remain supported by ongoing domestic capacity expansion and national initiatives aimed at strengthening semiconductor manufacturing capabilities. In the Taiwan region, spending is projected to be driven primarily by continued expansion of leading-edge foundry capacity, including 2nm and sub-2nm technologies. Korea's investment outlook remains closely tied to the memory sector, where AI-related demand is supporting another cycle of capacity and technology upgrades.

In the Americas, spending is expected to be underpinned by advanced process expansion and broader efforts to strengthen domestic manufacturing ecosystems.

Japan, Europe & Middle East, and Southeast Asia are also expected to post meaningful growth through 2029. In these regions, equipment investment is supported by a combination of government incentives, supply chain resilience strategies, and targeted efforts to expand semiconductor manufacturing capacity.

Part of the SEMI Fab Forecast database, the SEMI 300mm Fab Outlook lists 404 facilities and lines globally. The report reflects 198 updates and 9 new fabs/lines projects since its last publication in December 2025.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Diameter
TSV
105 µm
10 µm
Void
50 µm
6 µm
Visualization of 3D X-ray inspection results of TSV fills in a wafer. Wafer designed for Comet by Fraunhofer IZM_ASSID, it contains voids for illustrative purposes.
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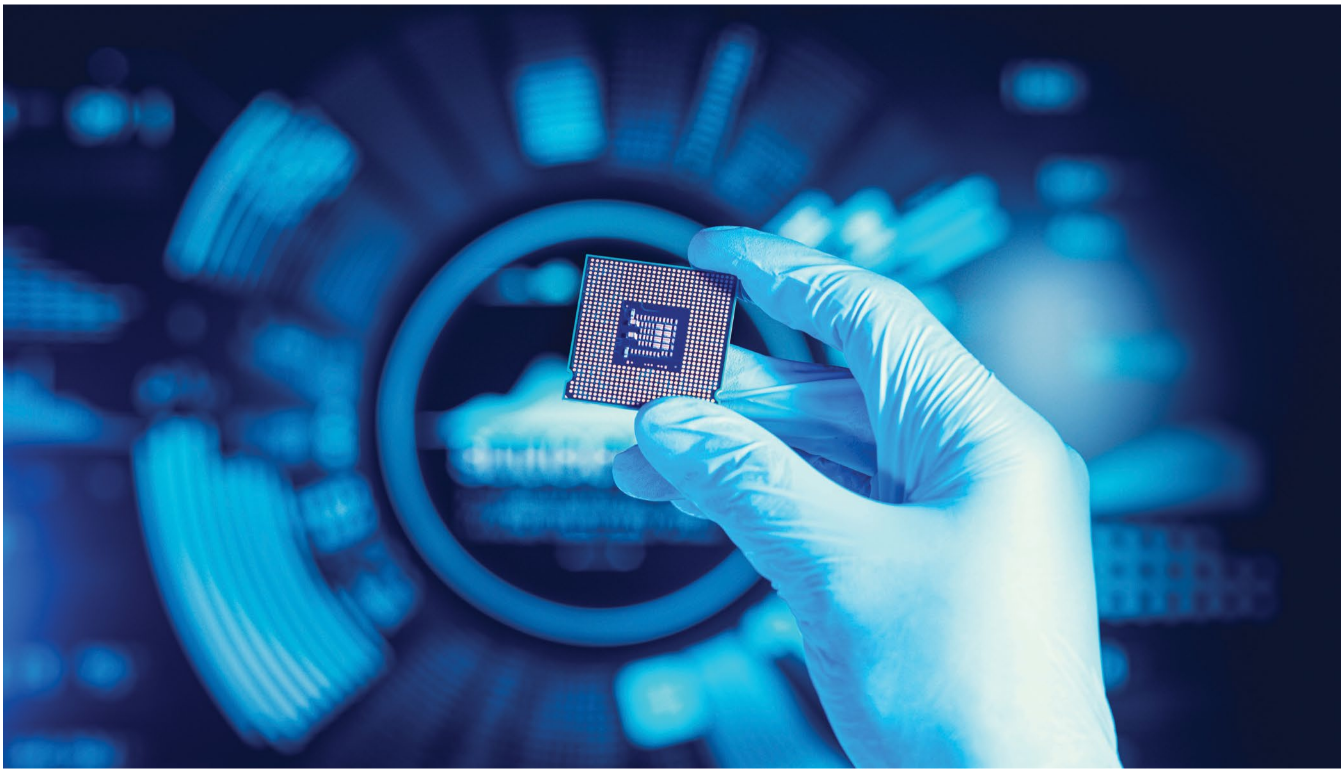


# Cloudberry VC launches Europe's first semiconductor venture fund

Rene Kromhof, Founding Partner, Cloudberry VC, a venture capital firm based in Helsinki and London, explains the background to the company's launch of Europe's first semiconductor venture fund with an initial close of €30 million. The fund invests in companies advancing the technological frontier with semiconductors, photonics and advanced materials to advance compute, connectivity, sensing and power.

EUROPE has no shortage of world-class semiconductor research. From photonics laboratories in Finland to compound semiconductor clusters in Germany and the UK, the continent consistently produces breakthrough technologies at the frontier of compute, connectivity, sensing, and power.
Yet for decades, a familiar problem has persisted: too many of these innovations fail to make the leap from laboratory success to scalable commercial impact.

Cloudberry VC believes the missing ingredient is not talent or ideas, but specialist capital.

Founded by semiconductor veterans and headquartered in Helsinki and London, Cloudberry VC has launched Europe's first dedicated semiconductor venture capital fund, closing an initial €30 million round and setting out an ambitious goal: to become the go-to early-stage investment platform for semiconductor, photonics, and advanced materials startups across Europe.

At the heart of the fund is a simple but powerful thesis. Semiconductors are too important, too complex, and too capital-intensive to be treated as just another category of "deep tech." They require investors who understand how chips are actually built, manufactured, qualified, and scaled — and who can actively help founders navigate that journey.

"We talk a lot about deep tech these days," says Rene Kromhof, Founding Partner at Cloudberry VC. "But it's still a very broad, general term. What's often missing is the very specific know-how needed to build and scale semiconductor companies."

## From the Fab floor to venture capital

Kromhof's conviction is rooted in personal experience. Over the course of his career, he has worked both inside major semiconductor corporates — including ASML — and within startups, as an operator and investor. That dual perspective exposed a recurring gap in Europe's innovation ecosystem.

On one side sit technically brilliant founders, often PhDs with years of highly specialised research behind them. On the other side are investors enthusiastic about "hard tech" but lacking hands-on experience with semiconductor engineering, manufacturing constraints, equipment procurement, or intellectual property strategy.

"The challenge isn't that investors need to know what a nanometre is," Kromhof explains. "It's about understanding how engineering decisions affect manufacturability, how IP strategies are built, how you design something that can actually be produced at scale. Especially in hardware, those choices matter early."

Cloudberry VC was created to bridge that gap — not just by providing capital, but by embedding semiconductor expertise directly into the investment process. The firm's partners and advisors all come from within the industry, allowing them to support founders on issues that generalist investors often struggle to assess.

## A strong signal from global capital

Cloudberry VC's €30 million initial close is notable not only because it reached its original target size, but also because of where the capital came from. Approximately 85% of the fund's capital (excluding Finland's state-owned investor Tesi) was raised internationally. For Kromhof, this is a clear signal that the opportunity extends far beyond any single national ecosystem.

"It shows that semiconductors, photonics, and advanced materials resonate globally," he says. "We have strategic corporate investors, but also institutional investors, angels, and high-net-worth individuals who were actively looking for a fund like this — and simply couldn't find one in Europe before."

Those strategic investors include major industry players such as GlobalFoundries and Radiant Opto-Electronics, whose involvement goes far beyond financial backing. Their presence reinforces Cloudberry VC's position as a sector-specific fund and opens doors that are typically closed to early-stage startups.

"If you're a generalist fund, you might do a semiconductor deal one day and a fintech deal the next," Kromhof notes. "That's not particularly attractive for semiconductor corporates. Our focus aligns directly with their strategic interests."

## Why specialisation matters in semiconductors

The case for a dedicated semiconductor fund is compelling when viewed through a market lens. Semiconductors are already among the most valuable industries in the world, and their importance continues to grow.

Today, the world's most valuable company, NVIDIA, is a semiconductor company. Europe's most valuable technology company, ASML, sits squarely at the heart of the global chip supply chain. By the end of the decade, combined semiconductor and photonics markets are expected to exceed $2 trillion in annual revenues — before accounting for the immense value captured by companies further up the stack.

But scale alone is not the whole story. Semiconductors are also uniquely strategic. They underpin everything from artificial intelligence and data centres to electric vehicles, telecommunications, medical devices, and space systems.

That strategic importance, Kromhof argues, makes focus essential. "When you specialise, you attract the right investors, the right founders, and the right partners," he says. "You create a knowledgeable supply chain of capital, all the way from early-stage startups to strategic LPs."

For founders, that translates into smarter support. Semiconductor startups may have deep technical expertise, but they still face daunting challenges around scaling, qualification, and production readiness. Cloudberry VC aims to complement founders' knowledge with its own operational experience — and with direct access to industry-scale infrastructure.

## Closing Europe's early-stage funding gap

Despite Europe's strengths in semiconductor research, early-stage ventures in the sector remain chronically underfunded compared to their US and Asian counterparts. Kromhof believes much of this stems from outdated perceptions.

"There's a stigma that these technologies are too hard, too expensive, and take too long," he says. "That scares investors away. But the data actually tells a very different story." Semiconductor startups may require patience, but they often build strong IP positions early — creating defensible value long before mass-market revenues arrive. In many cases, strategic acquisitions rather than IPOs provide attractive exit paths.

Cloudberry VC's role, Kromhof says, is partly catalytic. As a first mover, the firm hopes to demonstrate that specialist semiconductor investing is both viable and attractive — encouraging others to follow.

"We're realistic," he adds. "With €30 million, we're not going to change a trillion-euro industry overnight. But if we can de-risk decisions for generalist investors, attract co-investment, and bring more capital into the space, the impact multiplies."

## Beyond the Chips Act: The Role of venture capital

Europe's ambition to strengthen its semiconductor position has been formalised through the EU Chips Act, which aims to double Europe's global market share to around 20% by 2030. Much of the attention, and funding, has focused on large-scale fabs and manufacturing infrastructure.

While Kromhof welcomes these investments, he believes early-stage venture capital plays an equally critical — and often overlooked — role. "The Chips Act has put a lot of capital into big infrastructure projects," he says. "But innovation doesn't start in fabs. It starts in startups."

Rather than attempting to replicate the full end-to-end supply chains of Asia or the US, Kromhof argues that Europe should double down on specific niches where it already has strengths — and where interdependence within the global supply chain creates leverage.

Compound semiconductors for power electronics, photonic integrated circuits for AI infrastructure, and specialised chips for automotive and space applications are just a few examples. Europe has deep expertise in all of these areas, but needs more early-stage capital to turn that expertise into scalable businesses.

"We've done this before," Kromhof points out. "ASML is a perfect example.

Atomic layer deposition was invented in Finland. The legacy is there. What's missing is enough early capital to get the next generation of innovations off the ground."

## Leveraging strategic LPs for real-world scale

One of Cloudberry VC's most distinctive advantages lies in its strategic limited partners. Relationships with GlobalFoundries and Radiant Opto-Electronics allow portfolio companies to engage with mass-production environments far earlier than would otherwise be possible.

This is critical, Kromhof explains, because many startups develop processes that work in a lab — but break down when scaled to industrial volumes.

"Design for manufacturability is everything in this industry," he says. "If you wait too long to think about it, you risk expensive redesigns later." Through access to multi-project wafer runs and industrial-scale testing, Cloudberry VC-backed startups can validate designs in real silicon early on. The benefits extend beyond chip designers to equipment, materials, and metrology startups, which can tap into thousands of experienced engineers for feedback and iteration.

"That level of access is extremely rare at the pre-seed and seed stage," Kromhof says. "For us, it's a real unfair advantage."

## What Cloudberry VC looks for in founders and technologies

Cloudberry VC typically invests between €300,000 and €1 million at the pre-seed and seed stages, with an average first cheque of around €500,000.

Unusually, the fund reserves approximately 70% of its capital for follow-on investments, reflecting the long development cycles common in semiconductor ventures.

When evaluating opportunities, team quality is essential — but IP is paramount.

"Early-stage value in this sector is largely about intellectual property," Kromhof explains. "Patents, know-how, freedom to operate — that's the moat."

While Cloudberry VC does not restrict itself to specific verticals, several technology themes stand out. Edge AI, power-efficient computing, photonic interconnects, advanced cooling, and compound semiconductors all feature prominently. Connectivity — particularly in the context of 6G — is another area where Europe's historical strengths could translate into future leadership.

At the same time, Kromhof is keen to stress that Cloudberry VC is a horizontal enabler rather than a thematic AI fund. "We enable verticals," he says.

"Medtech, space, automotive, industrial — all of them depend on semiconductors and photonics. That's where we play."

## Finland, the Nordics, and a Pan-European vision

Although Cloudberry VC is rooted in Finland and the Nordics, its mandate is explicitly European. The firm already attracts deal flow from across the continent, driven by its specialist reputation.

"Semiconductors may be a huge market, but the community is surprisingly small," Kromhof observes. "People know who does what." Finland offers particular advantages, including a high density of technical universities, strong research institutions such as VTT, and significant involvement in EU Chips Act pilot lines. In fact, Finland is set to host more of these mass-production representative lines than almost any other European country.

Cloudberry VC complements this local strength with a distributed team, including partners in the UK and venture partners in Germany and Switzerland, ensuring proximity to founders across Europe. Building a Platform, Not Just a Fund
Looking ahead, Kromhof is clear that Cloudberry VC's ambitions extend beyond a single fund.

"In the short term, our focus is on delivering strong returns," he says. "That's non-negotiable."

But longer term, the vision is to build Europe's leading semiconductor investment platform — combining capital, strategic partnerships, and hands-on operational support.

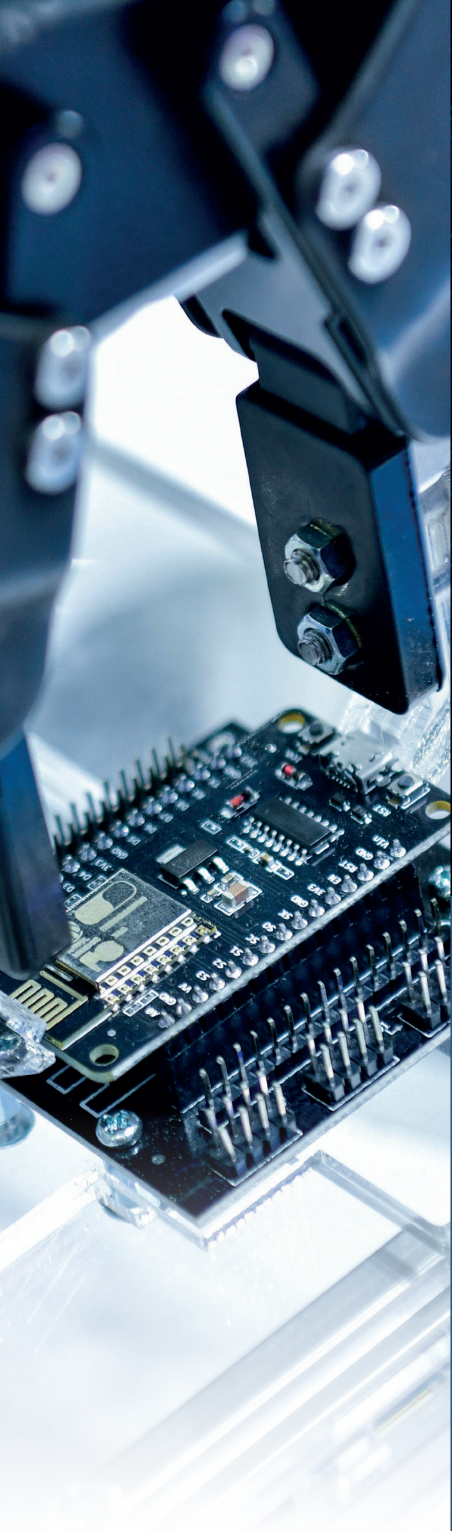
Already, Cloudberry VC works with IP specialists, chip design partners, and organisations that help startups access EU funding mechanisms. Over time, Kromhof hopes to scale this network alongside larger funds and deeper strategic involvement from European industry.

Ultimately, the goal is not complete self-sufficiency — which Kromhof sees as unrealistic — but smarter interdependence.

"The semiconductor supply chain is the most globalised supply chain in the world," he says. "No region can do everything alone. Europe needs to focus on niches, become excellent at them, and invest early enough to make a difference."

If Cloudberry VC succeeds, Europe's next semiconductor success stories may not come from mega-fabs alone, but from the startups quietly laying the foundations today — backed by capital that truly understands the chips they are building.

http://www.cloudberry.vc



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# The semiconductor industry is set to surpass $1 trillion by 2030, driving industry innovation

Marco Van Der Haar, Market Development Manager  Semiconductor at Malvern Panalytical, explains how advanced material analytics is set to transform semiconductor production.

THE GLOBAL semiconductor industry is experiencing an unprecedented surge. In 2025, annual semiconductor sales increased by 25.6% to $791.7 billion, the highest figure on record, and the industry is on track to reach $1 trillion in sales by 2026.*

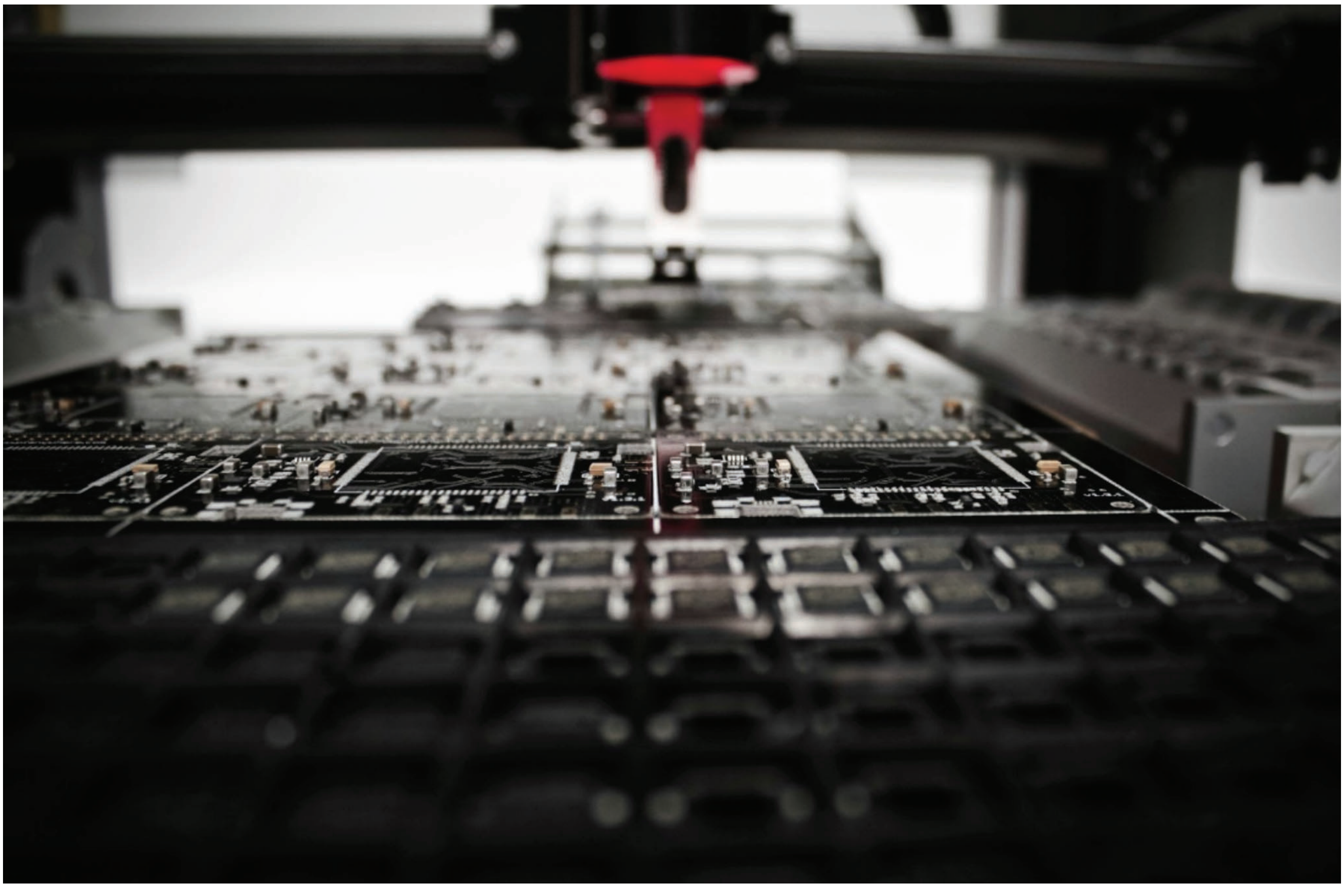
This explosive growth is fuelled by transformative technologies such as AI, data centres, 5G/6G connectivity, electrified transportation and intelligent edge devices. In this environment, producing large volumes is one thing, but consistently delivering high-quality products at scale is what really sets you apart.

Marco Van Der Haar, Market Development Manager - Semiconductor at Malvern Panalytical, explains how advanced material analytics could make 2026 a pivotal year for the industry.

Material precision: the foundation of next-generation semiconductors

In the upstream part of the semiconductor manufacturing process, precursor materials play a crucial role. They enable deposition processes like chemical vapour deposition (CVD), atomic layer deposition (ALD), and physical vapour deposition (PVD).

Precursor processing often involve powders . These powders need to meet strict standards as their particle size, shape, surface area, and chemical compositional affect how thin films form later in the process, hence impact how well the final devices perform. Even

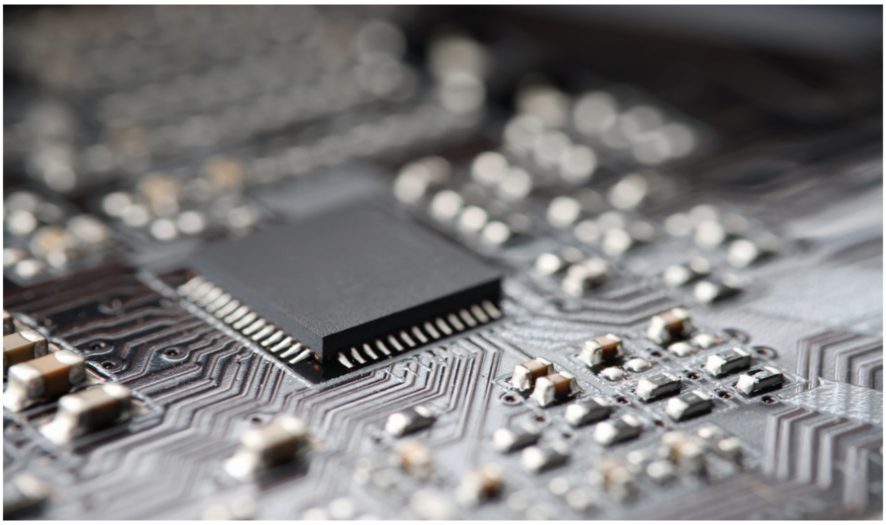


minor errors at this stage can cause issues later, resulting in lower yields and more waste.

Today, manufacturers use advanced analysis tools to check the size and shape of particles, what their surfaces are like, how porous they are, and what elements they contain. These careful checks help make sure each batch of material acts the same way, so production stays consistent and reliable.

Crystal orientation and thin-film control: precision at every scale
Controlling crystal orientation and lattice integrity of ingots and wafers is essential, especially as new wide-bandgap semiconductors such as SiC, GaN, InP and $Ga_2O_3$ become more common in high-performance uses. Good lattice alignment helps grinding, cutting, and ion implantation go smoothly and prevents defects that might harm device performance.

Thin-film stacks are increasingly complex, and even atomic-scale variations in for example thickness, density, or composition can impact electrical behavior and long-term reliability. Tools and technologies such as X-ray diffraction (XRD) and X-ray fluorescence (XRF) enable manufacturers to monitor these parameters in real time, maintaining process stability and accelerating development cycles.



## Advanced packaging: from assembly to reliability

As the industry moves toward 2.5D and 3D packaging, chiplets, and high-density interconnects, new material challenges are emerging. Factors like under-bump metallisation uniformity, polymer filler distribution, and epoxy consistency have a direct impact on mechanical strength, thermal management, and how long devices last. By using analytical methods to measure rheology, porosity, and particle distribution of the materials used, manufacturers can keep quality high and continue to innovate in packaging without losing reliability.

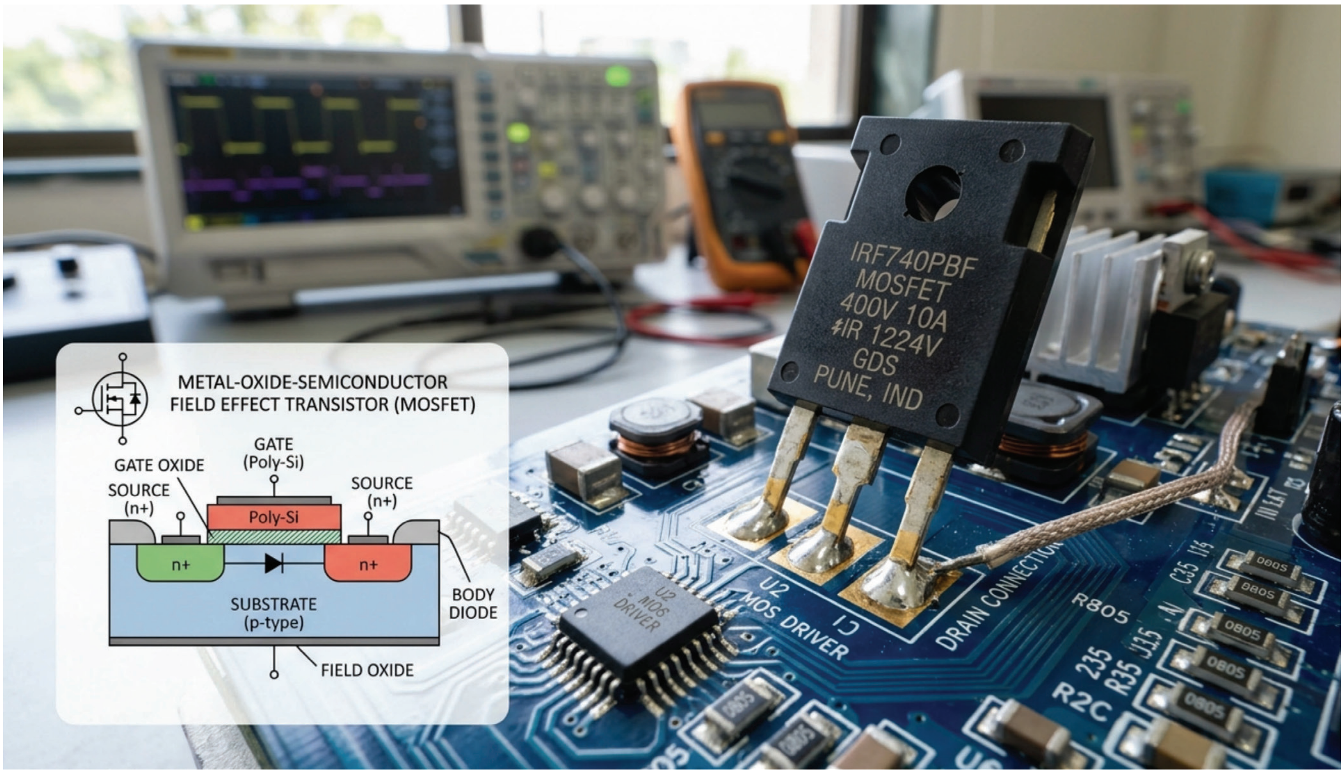
## Materials analytics: a competitive imperative

The companies that will lead tomorrow are the ones that truly understand their materials, from the first batch of powder to the final packaged product. Using advanced analytics, they can spot problems before they happen, reduce variability, improve yield, and scale with confidence.

By 2026, getting materials right isn't just a technical challenge; it's a strategic advantage. Manufacturers who make materials control part of everything they do can deliver next-generation devices with reliability, performance, and trust, setting the pace for the future of the semiconductor industry.

The semiconductor industry is moving into a stage where growth by itself is not enough for success. Control will be what sets leaders apart. As technology advances and production increases and processes get more complex, manufacturers need to better understand how materials behave at every step. If material-level variability goes unnoticed, it can quickly lead to lower yields, reliability problems, and higher costs.

When companies invest in better material insights and strong process control, they can grow more efficiently and innovate with more confidence. In the trillion-dollar semiconductor era, precision in materials leads to precision in devices, and that will be what sets industry leaders apart.




# Metallic oxide semiconductor Field Effect Transistor market to exceed $15.5 billion by 2033

According to Growth Market Reports, the global Metallic Oxide Semiconductor Field Effect Transistor (MOSFET) market size reached USD 8.3 billion in 2024, with a robust compound annual growth rate (CAGR) of 7.1% expected through the forecast period.

BY 2033, the MOSFET market is projected to attain a value of USD 15.5 billion, propelled by increasing demand for energy-efficient electronic devices and expanding applications across automotive, industrial, and consumer electronics sectors.

The market's expansion is underpinned by technological advancements in power electronics and the proliferation of smart, connected devices worldwide.

The Metallic Oxide Semiconductor Field Effect Transistor (MOSFET) market represents a critical segment of the global semiconductor industry, underpinning modern electronics and power systems. MOSFETs are essential components used for switching and amplification in electronic circuits, enabling efficient power management and signal processing across countless applications.

## Key market drivers

**Rising demand for consumer electronics**

The proliferation of smartphones, tablets, laptops, and wearable devices has significantly increased the demand for MOSFETs. These components enable efficient power management, longer battery life, and compact device design. As consumer expectations shift toward high-performance and energy-efficient devices, manufacturers are incorporating advanced MOSFET technologies into their products.

**Growth of Electric Vehicles (EVs)**

One of the most significant drivers of the MOSFET market is the rapid growth of electric vehicles. MOSFETs are widely used in EV powertrains, battery management systems, and charging infrastructure. Their ability to handle high switching frequencies and reduce power losses makes them ideal for automotive applications. The transition from traditional internal combustion engines to electric mobility is expected to further accelerate demand.

**Expansion of renewable energy systems**

The global push toward clean energy has led to increased deployment of solar and wind power systems.

MOSFETs are crucial in power conversion processes such as inverters and energy storage systems. They help improve efficiency and reduce energy losses, making them indispensable in renewable energy applications.

**Industrial automation and IoT**
The rise of Industry 4.0 and the Internet of Things (IoT) has created new opportunities for MOSFET applications. Industrial automation systems rely on efficient power management and high-speed switching, both of which are enabled by MOSFET technology. Additionally, IoT devices require compact, low-power components, further driving market growth.

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## Technological advancements

**Emergence of wide bandgap materials**
One of the most transformative trends in the MOSFET market is the adoption of wide bandgap materials such as silicon carbide (SiC) and gallium nitride (GaN). These materials offer superior performance compared to traditional silicon-based MOSFETs, including higher efficiency, faster switching speeds, and better thermal management.

SiC and GaN MOSFETs are increasingly being used in high-power applications such as EVs, renewable energy systems, and data centers. Their ability to operate at higher voltages and temperatures makes them ideal for next-generation power electronics.

**Miniaturisation and integration**
As electronic devices become smaller and more powerful, there is a growing need for miniaturized components. Advances in semiconductor fabrication technologies have enabled the production of smaller, more efficient MOSFETs with improved performance characteristics. Integration of MOSFETs into complex circuits and systems is also becoming more common, enhancing functionality and reducing overall system size.

**Improved thermal and switching performance**
Modern MOSFET designs focus on reducing on-resistance and improving thermal performance. These enhancements lead to lower power losses and higher efficiency, which are critical for applications such as data centers and industrial systems. Continuous innovation in packaging and materials is further improving device reliability and performance.

## Market challenges

**High initial costs**
Advanced MOSFET technologies, particularly those based on SiC and GaN, involve higher production costs compared to traditional silicon-based devices. This can limit adoption in cost-sensitive applications.

**Supply chain disruptions**
The semiconductor industry has faced significant supply chain challenges in recent years, affecting the availability of raw materials and components. These disruptions can impact production and lead to increased costs.

**Thermal management issues**
Despite advancements, managing heat in high-power applications remains a challenge. Efficient thermal management solutions are essential to ensure device reliability and longevity.

## Future Outlook

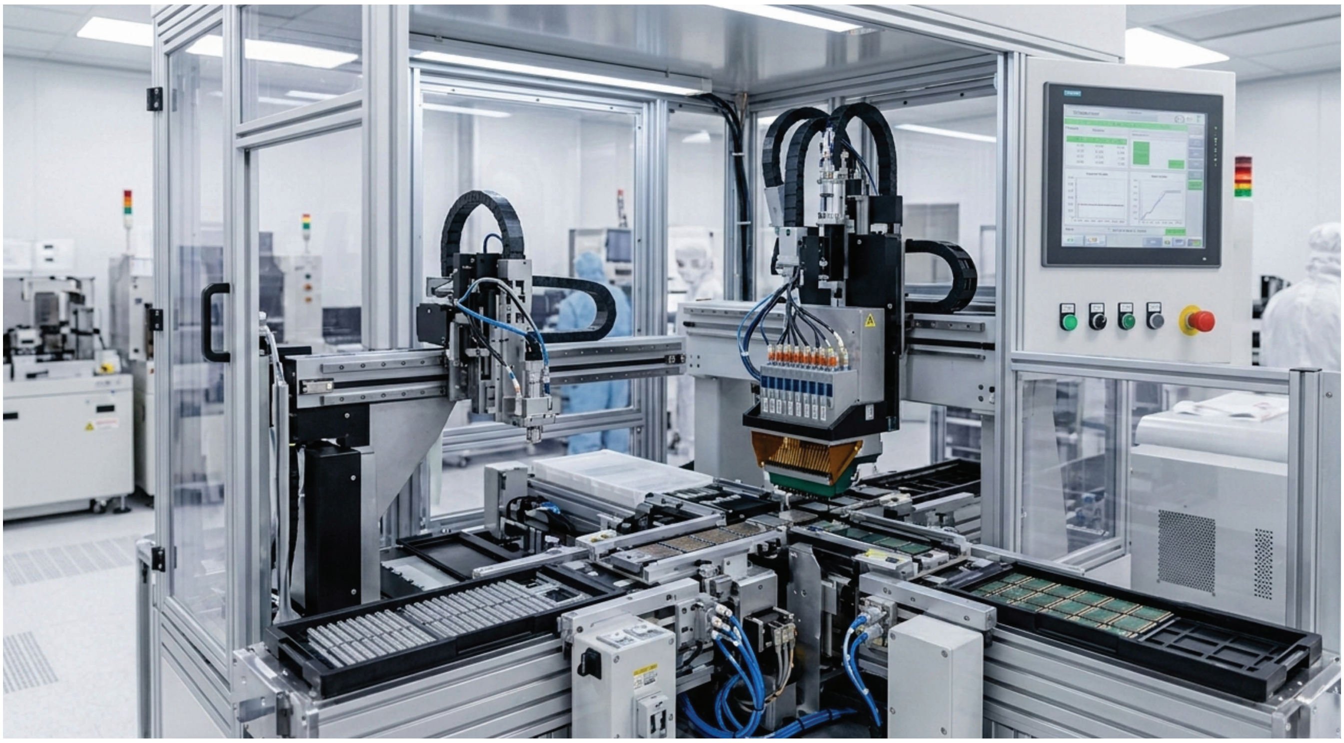
The future of the MOSFET market looks promising, with continued growth expected across various sectors. The increasing adoption of electric vehicles, renewable energy systems, and advanced electronics will drive demand for high-performance MOSFETs.
The shift toward wide bandgap materials such as SiC and GaN is expected to revolutionize the market, enabling new applications and improving overall efficiency.
Additionally, advancements in semiconductor manufacturing and design will continue to enhance device performance and reduce costs.
By 2035, the MOSFET market is anticipated to witness significant expansion, driven by technological innovation and the global transition toward energy-efficient solutions.

## Semiconductor chip test handler market to hit $2.97 billion

**Market summary**
According to latest research by Growth Market Reports, the global semiconductor chip test handler market size in 2024 stands at USD 1.62 billion, reflecting the robust demand for advanced testing solutions within the semiconductor industry. The market is experiencing a compound annual growth rate (CAGR) of 6.8% from 2025 to 2033. By 2033, the market is projected to reach USD 2.97 billion, driven by escalating requirements for high-performance chips across applications such as consumer electronics, automotive, and telecommunications.

The Semiconductor Chip Test Handler Market plays a vital role in the semiconductor manufacturing ecosystem. Test handlers are automated machines designed to transport semiconductor devices to testing equipment where their performance and reliability are evaluated. As semiconductor chips become increasingly complex and widely used across industries, the need for precise and efficient testing solutions has grown significantly. This trend has positioned chip test handlers as an essential component of modern semiconductor production.

**Key drivers**
The semiconductor chip test handler market is primarily driven by the rapid growth of consumer electronics, increasing adoption of automotive electronics, and expansion of global semiconductor manufacturing. The rising demand for smartphones, laptops, IoT devices, and wearable technologies has significantly increased semiconductor production, thereby boosting the need for efficient testing solutions. Additionally, the automotive industry's shift toward electric vehicles, advanced driver assistance systems (ADAS), and connected



car technologies has intensified the requirement for reliable semiconductor testing. Growing investments in semiconductor fabrication plants and packaging facilities across major economies are further accelerating the demand for automated chip test handlers.

**Challenges**

Despite steady growth, the semiconductor chip test handler market faces several challenges, including the high cost of advanced testing equipment and rapid technological evolution in semiconductor design. Test handlers are sophisticated machines that require substantial capital investment for installation, maintenance, and upgrades, which can be a barrier for smaller manufacturers. Moreover, the fast-paced development of semiconductor technologies demands continuous innovation in testing equipment to maintain compatibility with new chip architectures and packaging methods.

**Opportunities**

Significant opportunities exist in the semiconductor chip test handler market due to technological advancements and the emergence of new semiconductor applications. The integration of artificial intelligence, robotics, and automation in test handling systems is enabling faster and more accurate testing processes. Additionally, the growing deployment of 5G infrastructure and the increasing adoption of Internet of Things (IoT) devices are driving the need for high-performance semiconductor chips, which require rigorous testing.

**Technological advancements**

The semiconductor chip test handler market is witnessing significant technological innovations aimed at improving speed, accuracy, and flexibility. Modern test handlers are equipped with advanced robotics, artificial intelligence, and machine learning capabilities that optimize chip handling and testing workflows.

Additionally, manufacturers are developing modular test handler systems that allow semiconductor companies to adapt equipment based on evolving production requirements. High-temperature and low-temperature testing capabilities are also being integrated into new handler designs, enabling manufacturers to simulate real-world operating environments more effectively.

**Future outlook**

The future of the semiconductor chip test handler market looks promising as semiconductor technologies continue to evolve. Emerging applications such as artificial intelligence, 5G infrastructure, and high-performance computing will further increase the demand for advanced semiconductor devices. This growth will require more sophisticated testing equipment capable of maintaining quality and efficiency at large production scales. As a result, the semiconductor chip test handler market is expected to maintain steady growth in the coming years, driven by technological innovation, expanding semiconductor production, and the increasing need for reliable electronic components across multiple industries.

The semiconductor chip test handler market is witnessing significant technological innovations aimed at improving speed, accuracy, and flexibility. Modern test handlers are equipped with advanced robotics, artificial intelligence, and machine learning capabilities that optimize chip handling and testing workflows

[enabling environments where innovation thrives]


# Ganymede

## Performance without compromise

# Digital twin semiconductor supply chain market to teach $7.9 billion by 2033

According to Research Intelo,the Global Digital Twin Semiconductor Supply Chain market size was valued at $1.3 billion in 2024 and is projected to reach $7.9 billion by 2033, expanding at a robust CAGR of 22.4% during the forecast period from 2024 to 2033.

THE MAJOR FACTOR propelling this market's growth is the increasing need for end-to-end supply chain visibility and optimization in the semiconductor industry.

As semiconductor manufacturers face mounting pressure for faster time-to-market, enhanced quality control, and resilient supply chain operations, digital twin technology has emerged as a pivotal enabler.

By providing real-time simulation, predictive analytics, and process automation, digital twins allow stakeholders to proactively manage risks, reduce costs, and optimize performance across the entire semiconductor value chain.

## What is a Digital Twin in the semiconductor supply chain?

A digital twin is a virtual representation of a physical system that mirrors real-world operations using data, simulations, and analytics. In the semiconductor supply chain, this includes modeling factories, logistics networks, inventory systems, and supplier ecosystems.

These digital replicas allow companies to simulate scenarios, identify bottlenecks, and optimize processes without disrupting actual operations.

For instance, manufacturers can predict how a delay in raw material supply will impact chip production and adjust strategies accordingly.

## Market drivers fueling growth

**Increasing complexity of semiconductor supply chains**

The semiconductor supply chain involves multiple stages, including design, fabrication, assembly, testing, and distribution. With global dependencies and multiple stakeholders, managing this ecosystem has become increasingly challenging. Digital twins provide a unified view of these complex processes, enabling better coordination and transparency across the entire supply chain.

**Rising demand for real-time visibility**

In a highly competitive market, real-time data is crucial. Companies need instant insights into production status, inventory levels, and logistics performance. Digital twin technology integrates data from sensors, IoT devices, and enterprise systems to offer real-time visibility, helping organizations respond quickly to changes and disruptions.

**Focus on risk mitigation and resilience**
Events such as global pandemics, geopolitical tensions, and natural disasters have exposed vulnerabilities in semiconductor supply chains. Businesses are now prioritizing resilience.

Digital twins allow companies to simulate risk scenarios and develop contingency plans, ensuring business continuity even during unforeseen disruptions.

## Key market trends

**Integration with AI and machine learning**
The combination of digital twins with AI and machine learning is enhancing predictive capabilities. These technologies enable advanced analytics, helping companies forecast demand, optimize production schedules, and reduce downtime.

**Adoption of cloud-based solutions**
Cloud computing is playing a vital role in the adoption of digital twins. Cloud-based platforms provide scalability, flexibility, and cost-efficiency, making it easier for companies to deploy and manage digital twin solutions.

**Emphasis on sustainability**
Sustainability is becoming a critical focus area in the semiconductor industry. Digital twins help organizations monitor energy consumption, reduce waste, and optimize resource utilization, contributing to greener operations.

## Challenges in the market

**High implementation costs**
Deploying digital twin solutions requires significant investment in technology, infrastructure, and skilled personnel. This can be a barrier for small and medium-sized enterprises.

**Data integration issues**
Integrating data from multiple sources and ensuring its accuracy can be challenging. Inconsistent or incomplete data may affect the performance of digital twin models.

**Cybersecurity concerns**
As digital twins rely on interconnected systems and data sharing, they are vulnerable to cyber threats. Ensuring robust security measures is essential for successful implementation.

## Future outlook

According to Research Intelo, The future of the Digital Twin Semiconductor Supply Chain Market looks promising, with continuous advancements in technology and increasing adoption across the industry. As the demand for semiconductors continues to rise, companies will increasingly rely on digital twins to enhance efficiency, reduce costs, and improve resilience. Emerging technologies such as 5G, IoT, and edge computing will drive the adoption of digital twins, enabling more sophisticated and real-time applications.

# Chip-processing method could assist cryptography schemes to keep data secure

By enabling two chips to authenticate each other using a shared fingerprint, this technique can improve privacy and energy efficiency.

**BY ADAM ZEWE, MIT NEWS OFFICE**

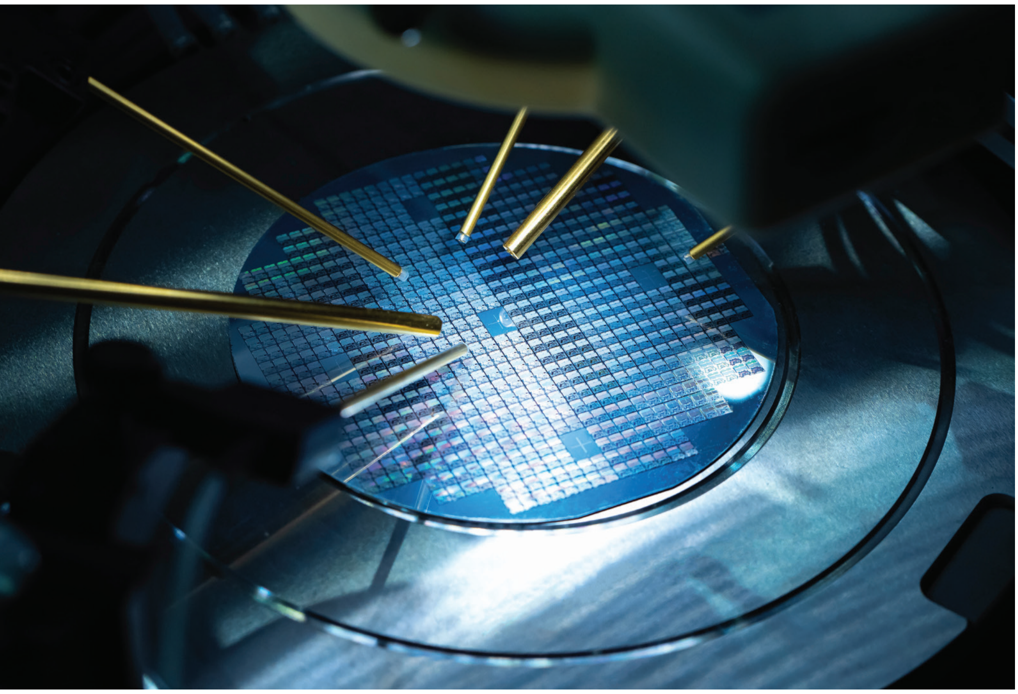
JUST LIKE each person has unique fingerprints, every CMOS chip has a distinctive "fingerprint" caused by tiny, random manufacturing variations. Engineers can leverage this unforgeable ID for authentication, to safeguard a device from attackers trying to steal private data.

But these cryptographic schemes typically require secret information about a chip's fingerprint to be stored on a third-party server. This creates security vulnerabilities and requires additional memory and computation.

To overcome this limitation, MIT engineers developed a manufacturing method that enables secure, fingerprint-based authentication, without the need to store secret information outside the chip.

They split a specially designed chip during fabrication in such a way that each half has an identical, shared fingerprint that is unique to these two chips. Each chip can be used to directly authenticate the other. This low-cost fingerprint fabrication method is compatible with standard CMOS foundry processes and requires no special materials.

The technique could be useful in power-constrained electronic systems with non-interchangeable device pairs, like an ingestible sensor pill and its paired wearable patch that monitor gastrointestinal health conditions. Using a shared fingerprint, the pill and patch can authenticate each other without a device in between to mediate.



"The biggest advantage of this security method is that we don't need to store any information. All the secrets will always remain safe inside the silicon. This can give a higher level of security. As long as you have this digital key, you can always unlock the door," says Eunseok Lee, an electrical engineering and computer science (EECS) graduate student and lead author of a paper on this security method.

Lee is joined on the paper by EECS graduate students Jaehong Jung and Maitreyi Ashok; as well as co-senior authors Anantha Chandrakasan, MIT provost and the Vannevar Bush Professor of Electrical Engineering and Computer Science, and Ruonan Han, a professor of EECS and a member of the MIT Research Laboratory of Electronics. The research was recently presented at the IEEE International Solid-States Circuits Conference.

"Creation of shared encryption keys in trusted semiconductor foundries could help break the tradeoffs between being more secure and more convenient to use for protection of data transmission," Han says. "This work, which is digital-based, is still a preliminary trial in this direction; we are exploring how more complex, analog-based secrecy can be duplicated — and only duplicated once."

## Leveraging variations

Even though they are intended to be identical, each CMOS chip is slightly different due to unavoidable microscopic variations during fabrication. These randomizations give each chip a unique identifier, known as a physical unclonable function (PUF), that is nearly impossible to replicate. A chip's PUF can be used to provide security just like the human fingerprint identification system on a laptop or door panel.

For authentication, a server sends a request to the device, which responds with a secret key based on its unique physical structure. If the key matches an expected value, the server authenticates the device.

But the PUF authentication data must be registered and stored in a server for access later, creating a potential security vulnerability.

"If we don't need to store information on these unique randomizations, then the PUF becomes even more secure," Lee says.

The researchers wanted to accomplish this by developing a matched PUF pair on two chips. One could authenticate the other directly, without the need to store PUF data on third-party servers. As an analogy, consider a sheet of paper torn in half. The torn edges are random and unique, but the pieces have a shared randomness because they fit back together perfectly along the torn edge.

While CMOS chips aren't torn in half like paper, many are fabricated at once on a silicon wafer which is diced to separate the individual chips.

By incorporating shared randomness at the edge of two chips before they are diced to separate them, the researchers could create a twin PUF that is unique to these two chips.

"We needed to find a way to do this before the chip leaves the foundry, for added security. Once the fabricated chip enters the supply chain, we won't know what might happen to it," Lee explains.

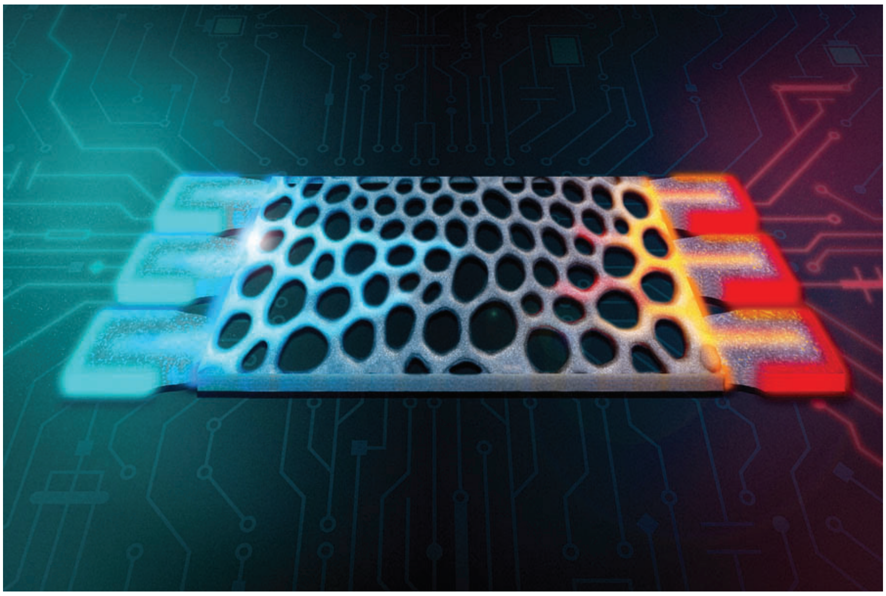


Image: Jose-Luis Olivares, MIT

➤ This artistic rendering shows a thermal analog computing device, which performs computations using excess heat, embedded in a microelectronic system.

## haring randomness

To create the twin PUF, the researchers change the properties of a set of transistors fabricated along the edge of two chips, using a process called gate oxide breakdown.

Essentially, they pump high voltage into a pair of transistors by shining light with a low-cost LED until the first transistor breaks down. Because of tiny manufacturing variations, each transistor has a slightly different breakdown time. The researchers can use this unique breakdown state as the basis for a PUF.

To enable a twin PUF, the MIT researchers fabricate two pairs of transistors along the edge of two chips before they are diced to separate them. By connecting the transistors with metal layers, they create paired structures that have correlated breakdown states. In this way, they enable a unique PUF to be shared by each pair of transistors. After shining LED light to create the PUF, they dice the chips between the transistors so there is one pair on each device, giving each separate chip a shared PUF.

"In our case, transistor breakdown has not been modeled well in many of the simulations we had, so there was a lot of uncertainty about how the process would work. Figuring out all the steps, and the order they needed to happen, to generate this shared randomness is the novelty of this work," Lee says.

After finetuning their PUF generation process, the researchers developed a prototype pair of twin PUF chips in which the randomization was matched with more than 98 percent reliability. This would ensure the generated PUF key matches consistently, enabling secure authentication.

Because they generated this twin PUF using circuit techniques and low-cost LEDs, the process would be easier to implement at scale than other methods that are more complicated or not compatible with standard CMOS fabrication.

"In the current design, shared randomness generated by transistor breakdown is immediately converted into digital data. Future versions could preserve this shared randomness directly within the transistors, strengthening security at the most fundamental physical level of the chip," Lee says.

"There is a rapidly increasing demand for physical-layer security for edge devices, such as between medical sensors and devices on a body, which often operate under strict energy constraints. A twin-paired PUF approach enables secure communication between nodes without the burden of heavy protocol overhead, thereby delivering both energy efficiency and strong security. This initial demonstration paves the way for innovative advancements in secure hardware design," Chandrakasan adds.

This work is funded by Lockheed Martin, the MIT School of Engineering MathWorks Fellowship, and the Korea Foundation for Advanced Studies Fellowship.

## MIT engineers design structures that compute with heat

MIT researchers have designed silicon structures that can perform calculations in an electronic device using excess heat instead of electricity. These tiny structures could someday enable more energy-efficient computation.

In this computing method, input data are encoded as a set of temperatures using the waste heat already present in a device. The flow and distribution of heat through a specially designed material forms the basis of the calculation. Then the output is represented by the power collected at the other end, which is thermostat at a fixed temperature.

The researchers used these structures to perform matrix vector multiplication with more than 99 percent accuracy. Matrix multiplication is the fundamental mathematical technique machine-learning models like LLMs utilize to process information and make predictions.

While the researchers still have to overcome many challenges to scale up this computing method for modern deep-learning models, the technique could be applied to detect heat sources and measure temperature changes in electronics without consuming extra energy. This would also eliminate the need for multiple temperature sensors that take up space on a chip.

"Most of the time, when you are performing computations in an electronic device, heat is the waste product. You often want to get rid of as much heat as you can. But here, we've taken the opposite approach by using heat as a form of information itself and showing that computing with heat is possible," says Caio Silva, an undergraduate student in the Department of Physics and lead author of a paper on the new computing paradigm. Silva is joined on the paper by senior author Giuseppe Romano, a research scientist at MIT's Institute for Soldier Nanotechnologies and a member of the MIT-IBM Watson AI Lab. The research appears in Physical Review Applied.

### Turning up the heat

This work was enabled by a software system the researchers previously developed that allows them to automatically design a material that can conduct heat in a specific manner. Using a technique called inverse design, this system flips the traditional engineering approach on its head. The researchers define the functionality they want first, then the system uses powerful algorithms to iteratively design the best geometry for the task.

They used this system to design complex silicon structures, each roughly the same size as a dust particle, that can perform computations using heat conduction. This is a form of analog computing, in which data are encoded and signals are processed using continuous values, rather than digital bits that are either 0s or 1s.

The researchers feed their software system the specifications of a matrix of numbers that represents a particular calculation. Using a grid, the system designs a set of rectangular silicon structures filled with tiny pores. The system continually adjusts each pixel in the grid until it arrives at the desired mathematical function.

Heat diffuses through the silicon in a way that performs the matrix multiplication, with the geometry of the structure encoding the coefficients. "These structures are far too complicated for us to come up with just through our own intuition. We need to teach a computer to design them for us. That is what makes inverse design a very powerful technique," Romano says. But the researchers ran into a problem.

Due to the laws of heat conduction, which impose that heat goes from hot to cold regions, these structures can only encode positive coefficients. They overcame this problem by splitting the target matrix into its positive and negative components and representing them with separately optimized silicon structures that encode positive entries. Subtracting the outputs at a later stage allows them to compute negative matrix values.

They can also tune the thickness of the structures, which allows them to realize a greater variety of matrices. Thicker structures have greater heat conduction.

"Finding the right topology for a given matrix is challenging. We beat this problem by developing an optimization algorithm that ensures the topology being developed is as close as possible to the desired matrix without having any weird parts," Silva explains.

### Microelectronic applications

The researchers used simulations to test the structures on simple matrices with two or three columns. While simple, these small matrices are relevant for important applications, such as fusion sensing and diagnostics in microelectronics.

The structures performed computations with more than 99 percent accuracy in many cases. However, there is still a long way to go before this technique could be used for large-scale applications such as deep learning, since millions of structures would need to be tiled together. As the matrices become more complicated, the structures become less accurate, especially when there is a large distance between the input and output terminals. In addition, the devices have limited bandwidth, which would need to be greatly expanded if they were to be used for deep learning.

But because the structures rely on excess heat, they could be directly applied for tasks like thermal management, as well as heat source or temperature gradient detection in microelectronics.

"This information is critical. Temperature gradients can cause thermal expansion and damage a circuit or even cause an entire device to fail. If we have a localized heat source where we don't want a heat source, it means we have a problem. We could directly detect such heat sources with these structures, and we can just plug them in without needing any digital components," Romano says.

Building on this proof-of-concept, the researchers want to design structures that can perform sequential operations, where the output of one structure becomes an input for the next. This is how machine-learning models perform computations. They also plan to develop programmable structures, enabling them to encode different matrices without starting from scratch with a new structure each time.

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# CEA-Leti and NcodiN partner to industrialise 300 mm Silicon Photonics

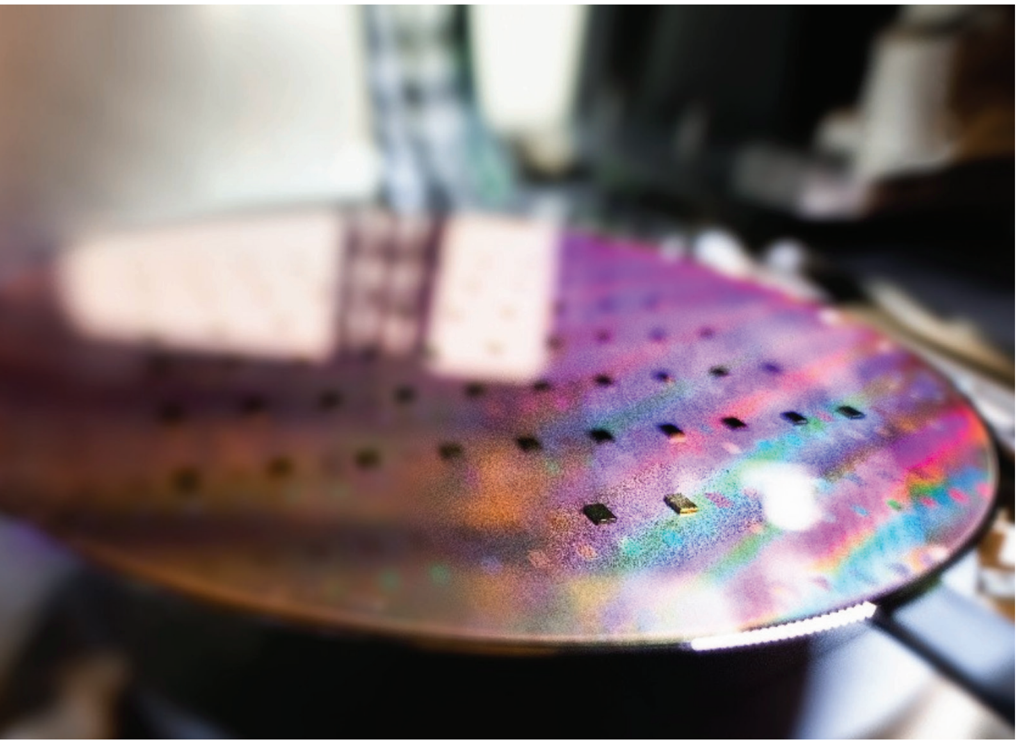
CEA-Leti and NcodiN, a French deep-tech startup pioneering nanolaser-enabled photonic interconnects, have formed a strategic collaboration to industrialize NcodiN's optical interposer technology on a 300 mm integrated photonics process.

NcodiN, which received €16 million in seed financing last November, is developing optical interconnects designed to relieve a critical data-movement bottleneck limiting performance in next-generation semiconductors. The collaboration will accelerate the company's proof-of-concept work into industrial-grade 300 mm processes—moving beyond copper interconnects and marking a major step toward scalable, in-package, long-reach optical links for future computing architectures and artificial intelligence (AI) chips.

As AI systems demand orders of magnitude increases in bandwidth and energy efficiency, the industry is shifting from copper to optical interconnects.

## World's smallest laser on silicon

NcodiN is building NConnect, the integrated optical interconnect platform powered by the world's smallest laser on silicon—500× smaller than today's industry-standard devices. The company's nanolaser-enabled photonic interposers pave the way to ultra-dense integration (>5,000 nanolasers/mm$^2$) and record-low energy operation (~0.1 pJ/bit). Building on CEA-Leti's advanced photonics integration expertise, NcodiN is transitioning its nanolaser to a 300 mm silicon photonics platform. This is a foundational step toward scalable, wafer-level optical interconnects for high-end computing and AI applications.



➤ III-V semiconductor dies bonded to 300mm wafer using direct bonding and high-precision alignment. Credit : AUBERT/CEA

"NcodiN's nanolaser-enabled photonic interconnects overcome the long-standing bottleneck of bulky, inefficient photonic components that have prevented large-scale adoption," said Francesco Manegatti, co-founder and CEO of NcodiN. "Our collaboration with CEA-Leti aims to demonstrate NConnect's compatibility with 300 mm wafers, which is essential for commercial-scale production and cost-effective adoption in AI-centric processors and high-bandwidth computing systems."

'Turning Point for Optical Interconnects'
Sébastien Dauvé, CEO of CEA-Leti, said the partnership underscores the two parties' shared commitment to enabling scalable photonic infrastructure capable of meeting tomorrow's computing demands.
"Transitioning photonics to a 300 mm CMOS-compatible process is a turning point for optical interconnects that can finally be produced at the scale, cost, and reliability the AI industry requires," he said. "This collaboration with NcodiN highlights a key part of CEA-Leti's mission: transferring advanced semiconductor and microelectronics technologies to industry, where they serve a range of vital markets."

## CEA-Leti and Fraunhofer IPMS

## validate wafer exchange

CEA-Leti and Fraunhofer IPMS have successfully completed the first exchange of ferroelectric memory wafers within the FAMES Pilot Line, marking a pivotal milestone in establishing a shared European platform for advanced embedded non-volatile memory (NVM) technologies. Launched in December 2023 and coordinated by CEA-Leti, the five-year initiative has demonstrated the viability of circulating complex material stacks across some of its leading research fabs.

The collaboration initially focused on the processing and electrical characterization of hafnium-zirconium oxide (HZO) ferroelectric capacitor stacks. Utilizing the combined 300 mm CMOS cleanroom capabilities of both institutes, they circulated the wafers in short process loops to enable joint evaluation of materials, electrode configurations, and device behavior.

The work also validated the wafer exchange and contamination-control protocols implemented in the pilot line, demonstrating that complex material stacks can be processed reliably across multiple advanced semiconductor facilities across all wafers.

The entire process adhered to standardized contamination control procedures, verified through VPD-ICP-MS (Vapor Phase Decomposition – Inductively Coupled Plasma Mass Spectrometry) and TXRF (Total Reflection X-Ray Fluorescence) analytics. Devices were evaluated using a ferroelectric capacitor (FeCAP) array test vehicle designed by CEA-Leti, with electrical characterization performed via the PUND (Positive-Up-Negative-Down) methodology to isolate true ferroelectric switching from parasitic effects.

## Critical insights

"The successful wafer exchange marks an important step toward a joint European material-testing platform for ferroelectric memories," said Dr. Wenke Weinreich, Division Director of Fraunhofer IPMS' Center Nanoelectronic Technologies, a member of the 11-member FAMES consortium. "By combining our processing expertise with CEA-Leti's CMOS integration capabilities, the pilot line provides a powerful environment for evaluating new ferroelectric stacks and accelerating their path toward system-level applications."

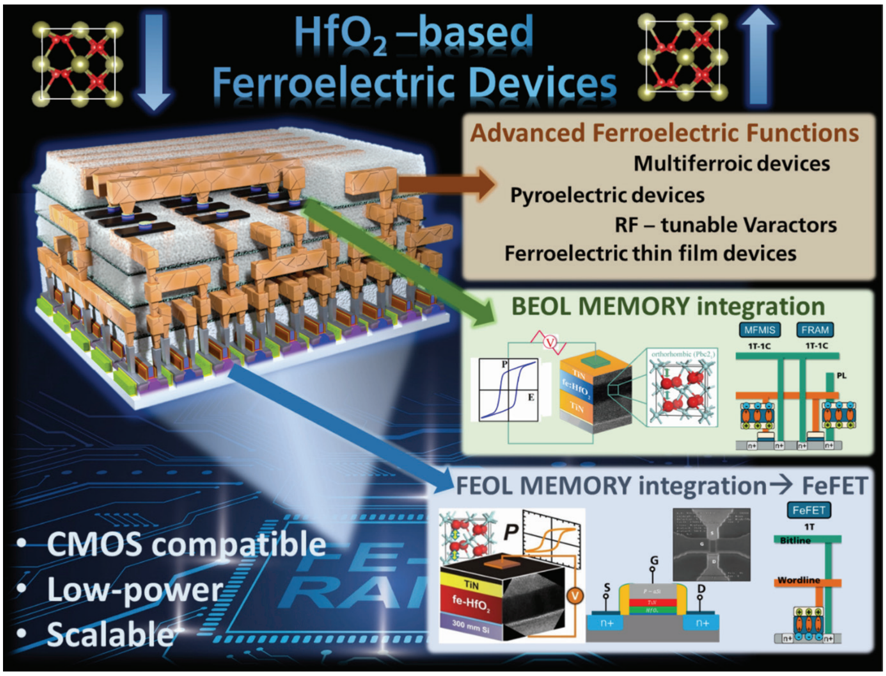



Illustration of $HfO_2$-based ferroelectric devices enabling scalable, CMOS-compatible NVM. The architecture supports integration in both front-end (FeFET) and back-end memory structures, while opening pathways to advanced ferroelectric functionalities such as multiferroic, pyroelectric, and tunable RF devices. © Fraunhofer IPMS

Initial experimental results have already yielded critical insights. The team screened various electrode materials to enhance performance, finding that titanium nitride (TiN) bottom electrodes significantly outperform tungsten. In reliability tests, TiN exhibited lower failure rates after $10^7$ field cycles at 4 MV/cm. Furthermore, clear cross-split effects were observed across different electrode configurations, confirming the sensitivity of the test vehicles to process variations.

## Seamless wafer exchanges across FAMES sites

"This first exchange between CEA-Leti and Fraunhofer IPMS demonstrates that shared process flows, test vehicles, and characterization environments can work seamlessly across FAMES sites," noted Dominique Noguet, pilot line coordinator and CEA-Leti vice president. "Establishing reliable wafer loops between leading research fabs is essential for accelerating ferroelectric memory development."

Looking ahead, the wafer loops lay the groundwork for broader collaborative development. Upcoming phases will integrate $HfO_2$-based ferroelectric stacks from Fraunhofer IPMS into CEA-Leti CMOS processes, followed by array-level evaluations on GlobalFoundries' 22nm FDX® Memory Advanced Demonstrator Multi-Project Wafer shuttle prepared by CEA-Leti. This builds on Fraunhofer IPMS' recent completion of a first chip tape-out using the same 22nm FDX® technology, which also initiated research on algorithm-based AI compute-in-memory accelerator architectures.

The roadmap further includes studies on electrode process variations, long-term reliability, and back-end-of-line (BEOL) integration approaches, such as nanosecond laser annealing (NLA).

Together, these efforts advance the core mission of the FAMES Pilot Line: to provide a unified European platform for developing and validating emerging memory technologies—including OxRAM, MRAM, FeRAM, and FeFET.

By enabling collaborative material development and standardized characterization, the initiative aims to strengthen Europe's capacity to design and manufacture the low-power, next-generation chip architectures required for the future of computing.

## CEA-Leti, CEA-List and PSMC

CEA-Leti and CEA-List, a specialist in smart digital systems, have announced a strategic collaboration with Powerchip Semiconductor Manufacturing Corporation (PSMC). The collaboration will leverage CEA-List's RISC-V design expertise and CEA-Leti's silicon photonics expertise to introduce high-bandwidth communication and high-efficiency computing technologies into PSMC's established 3D stacking and interposer platforms to deliver solutions for next-generation artificial intelligence (AI) systems.

The semiconductor industry faces mounting challenges, including the physical limits of traditional copper interconnects, increasingly stringent power budgets, and the urgent need for flexible, scalable computing architectures. By integrating short-reach, high-bandwidth optical links for energy-efficient data movement and customizable RISC-V processor architectures, the collaboration directly addresses these constraints and establishes a new paradigm in high-performance data transport and computing architecture.

"RISC-V is transforming processor design by combining openness, flexibility, and cost efficiency. Its customizable architecture allows industrial players to develop solutions tailored to their needs," said Olivier Thomas, Deputy Head of the Digital IC Design Division at CEA-List. "Our joint effort will give customers a customizable compute platform that meets the performance and power targets."

"In the collaboration, microLED is a critical enabling technology that will boost optical-communication throughput using low-power GaN LED solutions," added Sébastien Dauvé, Chief Executive Officer of CEA-Leti.

"This collaboration enriches PSMC's 3D stacking and interposer technology envelope with high-efficiency RISC-V computing IP and high-bandwidth silicon photonics chiplet communication. By leveraging the expertise of CEA-Leti and CEA-List alongside PSMC's technologies, we will provide foundry services to customers for next-generation AI applications," said Dr. Shou-Zen Chang, Chief Technology Officer of PSMC.

**About Fraunhofer IPMS**

Fraunhofer IPMS is a leading international research and development service provider for electronic and photonic microsystems in the fields of intelligent industrial solutions, medical technology and health, mobility, and green and sustainable microelectronics. Its research focuses on customer-specific miniaturized sensors and actuators, MEMS systems, microdisplays, and integrated circuits, as well as wireless and wired data communication. Its services range from consulting and design to process development and pilot series production. With the Center Nanoelectronic Technologies (CNT), Fraunhofer IPMS offers applied research on 300 mm wafers for microchip producers, suppliers, device manufacturers and R&D partners.

## FAMES announces 2026 Open-Access Call

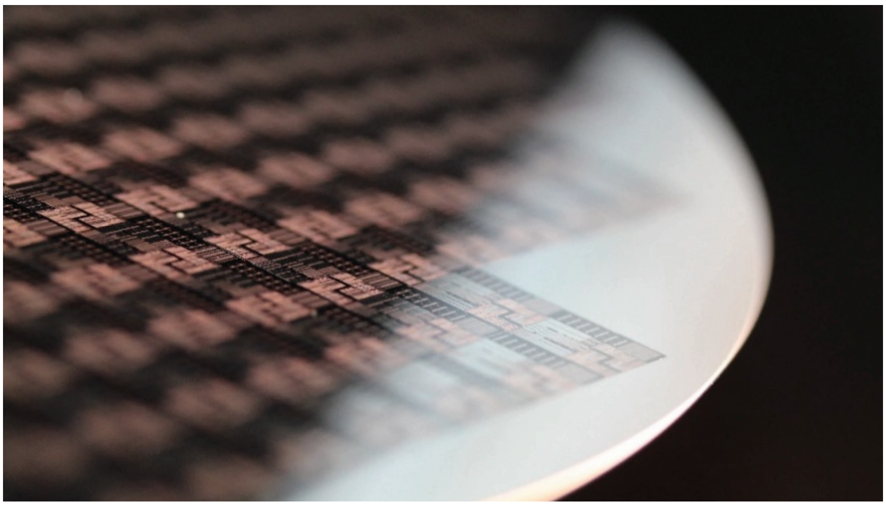
The FAMES Pilot Line has launched its second Open-Access Call for European semiconductor stakeholders to join the groundbreaking EU initiative focused on new chip architectures to boost European tech sovereignty.  An online launch event was held this afternoon to provide researchers, academia, and industry teams with a detailed overview of the technologies currently available and the application process for accessing the pilot line.

Building on the strong interest and early silicon results of the 2025 open-access call, the 2026 program adds four new process design kits (PDKs) and research advances in integrated radio frequency filters and switches and components for power-management integrated circuits (PMIC).

Design houses, fabless companies, foundries, integrated device manufacturers, material & tool suppliers, universities and research centers can submit User Requests by responding to the two-month-long Open-Access Call, starting today, or by submitting a Spontaneous User Request throughout the year. For more information on the Open-Access mechanisms, participants can download the User Guidelines and Procedures document from the FAMES website (https://fames-pilot-line.eu/guidelines-for-open-access/). Open-Access Calls will take place each spring through 2028, with an updated portfolio of available FAMES technologies.
New Process Design Kits

**This year's open-access call PDKs:**

- 15 GHz LiNbO3 Bulk Acoustic Wave Resonator (BAW-SMR) Filter PDK and 7-15 GHZ AlN/ScAlN BAW RF Filter PDK, making these state-of-the-art highly miniaturized RF components, having band pass filtering capabilities in the FR3 range, accessible to the chip ecosystem,
- Phase Change Material-based RF switch PDK, allowing users to design their own demonstrators and integrate them for the first time on high-resistivity 300 mm silicon wafers,
- FAMES' magnetics on silicon MagIC technology R&D samples and subsequent PDK, enabling users



➤ FeFET wafer. © Fraunhofer IPMS

to integrate micro-inductors directly on their power management systems-on-chip, closest to the SoC load, and

- The FD-SOI 10nm pathfinding PDK release 1 for testing the capabilities of this advanced low-power technological node.

"The 2026 Open-Access Call supports the European Union's sovereign technological strengths with enriched technologies thanks to two years of successful R&D results," said Susana Bonnetier, open-access chairperson. "The radio frequency components PDKs are especially noteworthy this year, because for the first time, participants will be able to access and test sovereign 7-15 GHz acoustic RF filter and PCM switch technologies of their own design."

Bonnetier explained that users will also be able to test the impact on power-delivery efficiency of integrating micro-inductors directly on their power-management ICs and explore the performance advantages of the FD-SOI 10nm technology node with the Pathfinding PDK that is now ready for licensing and delivery.

Launched in December 2023 by the Chips Joint Undertaking (Chips JU) and coordinated by CEA-Leti, FAMES envisions a strategic leap in semiconductor innovation, while reinforcing Europe's industrial leadership. The FAMES project has two main objectives:

- To offer Europe a domestic semiconductor pilot line for advanced technologies providing:
  - Two generations of FD-SOI (Fully Depleted Silicon-on-Insulator) technology at the 10nm and 7nm nodes,
  - Various non-volatile memory (NVM) options in metallic interconnects above transistors,
  - Radiofrequency (RF) components (passives, switches, and radio frequency filters), and
  - 3D technological stacking options (3D sequential integration and 3D heterogenous integration),
  - Seven application-driven demonstrators for brain computing interface, radar, neuromorphic computing, cybersecurity and optical communication networks.
- To promote FAMES Pilot Line technologies and to give Europe the opportunity to follow the miniaturization evolution of electronics on a wide spectrum of semiconductor markets strengthening European leadership and opening new opportunities.

In addition to the pilot line coordinator, France-based CEA-Leti, the FAMES consortium includes imec (Belgium), Fraunhofer (Germany), Tyndall (Ireland), VTT (Finland), CEZAMAT WUT (Poland), UCLouvain (Belgium), Silicon Austria Labs (Austria), SiNANO Institute (France), Grenoble INP (France) and the University of Granada (Spain).

# Imec unlocks lever for EUV dose reduction

## Oxygen injection during metal-oxide resist post-exposure bake emerges as game-changer for throughput.

AT THE 2026 SPIE Advanced Lithography + Patterning Conference, imec demonsrated that precise control of gas compositions during post-exposure EUV lithography steps can help in minimizing the required exposure dose, thereby unlocking higher wafer throughput. In particular, improved dose response of metal-oxide photoresists (MORs) has been achieved when the EUV post-exposure bake step is performed under elevated oxygen concentrations.

Metal-oxide resists (MORs) have emerged as leading candidates for advanced EUV lithography applications, offering superior resolution, reduced line-edge roughness, and good EUV dose-to-size performance compared to chemically amplified resists (CARs). Their better pattern transfer capability for small features and thin resist films makes them particularly attractive for the highest resolution metal layers, exposed using High NA EUV lithography. Imec now demonstrates that the dose response of MORs can be further improved by raising the oxygen concentration above atmospheric levels during the EUV lithography post-exposure bake step – a critical heat treatment step after EUV resist exposure and before resist development.

Ivan Pollentier, Senior Researcher at imec: "We observe a 15-20% faster photo-speed when increasing the oxygen concentration from atmospheric 21% to 50% during post-exposure bake. The trend is observed for both model MOR and commercial MOR materials. This finding shows for the first time that carefully controlling the gas composition during key lithography steps can significantly cut the required EUV exposure dose, directly boosting the throughput of the EUV scanner and reducing process costs. This is just a first result from the BEFORCE tool: the controlled gas composition provides an additional knob to study the origins of environmental effects on the lithographic variability of MOR materials. Equipment manufacturers can use these insights as a guideline to adapt their tools for improved EUV lithography throughput and stability."

The results were achieved using BEFORCE, a unique research tool developed by imec to investigate the role of the ambient environment on critical dimension (CD) stability and performance of MORs. Kevin Dorney, R&D Team Lead at imec: "In commercial EUV clusters, resist-coated wafers are exposed in vacuum and then transferred to the post-exposure bake unit, where they are heated under atmospheric conditions. Our BEFORCE tool mimics these operations, but the wafer transfer and post-exposure bake are isolated from the cleanroom atmosphere and can be performed in precisely controlled environments allowed by gas injection and mixing systems. This unique ability, in combination with an integrated photo-speed measurement, was key to revealing the role of oxygen in boosting MOR's dose response."

To optimally exploit the positive impact of gas compositions on the MOR performance, a more fundamental understanding of the chemical mechanism at play during the resist's post-exposure bake is essential. Experiments are ongoing to correlate MOR performance to observations of chemical changes during bake – captured by an integrated Fourier transform infrared spectrometer – under varying environmental conditions. The planned expansion of the BEFORCE tool with advanced metrology capabilities will enable imec to drive even more impactful results. BEFORCE can be used more broadly to study both MOR and CAR resists and is accessible to imec's partners for resist evaluation.

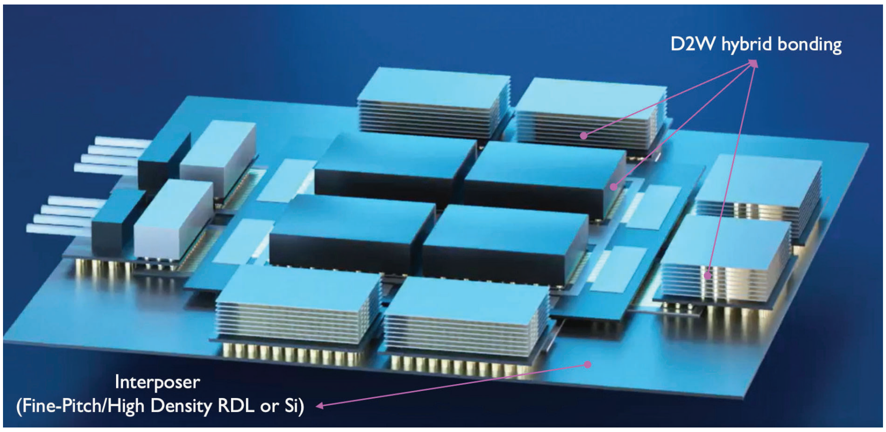

### The world's most advanced High NA EUV system

Recently, imec received delivery of the ASML EXE:5200 High NA EUV lithography system, the most advanced lithography tool available today. With this strategic milestone, imec reinforces its position as the industry's launchpad into the ångström era, giving its global partners ecosystem unparalleled early access to the next generation of chip-scaling technologies. Integrated directly with a comprehensive suite of patterning and metrology tools and materials, the High NA EUV system will empower imec and its ecosystem partners to unlock the performance needed to pioneer sub-2nm logic and high-density memory technologies that will fuel the rapid growth of advanced AI and high-performance computing.

Luc Van den hove, CEO of imec: “The past two years have marked an important chapter for High NA (0.55NA) EUV lithography, with imec and ASML joining forces with the ecosystem in its joint High NA EUV Lithography Lab in Veldhoven (The Netherlands) to pioneer High NA EUV technology. With the installation of the EXE:5200 High NA EUV lithography system into our 300mm cleanroom in Leuven (Belgium), we aim to bring these High NA EUV patterning technologies to an industry-relevant scale and to develop the next-generation High NA EUV patterning use cases. Its unmatched resolution, improved overlay performance, high throughput, and a new wafer stocker that improves process stability and throughput, will give our partners a decisive advantage in accelerating the development of sub-2nm chip technologies. As the industry moves into the ångström era, High NA EUV will be a cornerstone capability, and imec is proud to lead the way by offering its partners the earliest and most comprehensive access to this technology.”

This milestone is a key element of imec’s five-year strategic partnership with ASML supported by the EU (Chips Joint Undertaking and IPCEI), the Flemish government, and the Dutch government. Luc Van den hove: “As an integral part of the EU funded NanoIC pilot line, the tool is set to play a pivotal role in strengthening Europe’s position as a leader in advanced semiconductor R&D in the decades to come.”

Having the ASML EXE:5200 High NA EUV lithography system in imec’s cleanroom firmly positions imec as the most comprehensive development environment for advanced patterning. Imec’s deep ecosystem collaboration with leading chip manufacturers, equipment, material and resist suppliers, mask companies, and metrology experts will allow us to




ramp up learning cycles and enhance process stability to develop and demonstrate cutting-edge patterning for next generation logic and memory device technology, driving breakthroughs that will shape the future of advanced computing and AI in the years to come.

Christophe Fouquet, CEO of ASML: “Imec’s installation of the EXE:5200 marks an important step into the ångström era. Together, we’re accelerating High NA EUV extendibility for the next generations of advanced memory and compute.”

Imec anticipates the EXE:5200 High NA EUV lithography system to be fully qualified by Q4 2026. In the meantime, the joint ASML-imec High NA EUV lithography Lab in Veldhoven will remain operational, ensuring continuity in the High NA EUV R&D activities for imec and its ecosystem partners.

## NanoIC opens access to first-ever fine-pitch RDL and D2W hybrid bonding interconnect PDKs

The NanoIC pilot line, a European initiative coordinated by imec and dedicated to accelerating innovation in chip technologies beyond 2nm, has released two first-of-a-kind advanced interconnect process design kits (PDKs): a fine-pitch redistribution layer (RDL) and die-to-wafer (D2W) hybrid bonding PDK. These early-access PDKs bring advanced packaging capabilities within reach of universities, startups, and industry innovators and mark an important step in enabling highdensity, energyefficient chiptochip connectivity.

As the semiconductor industry moves toward ever more complex and heterogeneous system architectures, advanced packaging has become a key enabler in supporting this progress. Instead of merely enclosing individual chips, today’s packaging technologies bring multiple dies (chiplets) together into tightly integrated systems where performance, energy efficiency, and bandwidth hinge on how effectively those components can interact. By enabling chiplets to be interconnected at high density, advanced packaging provides the foundation for the next generation of highperformance computing, AI accelerators, and dataintensive applications.

To enable universities, startups, SMEs, and industrial players to turn these concepts into practical designs, NanoIC today releases the first version of its fine-pitch redistribution layer (RDL) and dietowafer (D2W) hybrid bonding process design kits (PDKs). These PDKs, built on the NanoIC pilot line, give designers early access to the design rules and validated building blocks needed to explore highdensity chiptochip integration.

**Finepitch RDL PDK: highdensity routing on polymerbased substrates**

The finepitch redistribution layer (RDL) PDK introduces a new way to achieve highdensity chiptochip connections using polymerbased substrates. Traditionally, these substrates could not support extremely fine lines, limiting their use in advanced packaging. Imec’s technology, developed within the NanoIC project, overcomes this barrier by enabling exceptionally smallpitch interconnects in a polymerbased RDL, offering capabilities that go beyond what leading commercial fabs provide today. With line widths and spaces down to 1.3 microns and microbump pitches as tight as 20 microns, the RDL PDK gives designers access to interconnects that can improve communication speed by up to 40% and reduce energy per bit by as much as 15%, on a UCIe-Advanced die-to-die interface. As a result, finepitch RDL becomes an appealing integration option for a wide range of emerging applications, from automotive and highperformance computing to nextgeneration GPU architectures.

**D2W hybrid bonding PDK: ultradense dietodie 3D connections**
D2W hybrid bonding adds a second powerful integration technique by enabling extremely compact, direct connections between dies using the third dimension. Instead of relying on traditional copper bumps, hybrid bonding forms direct oxidetooxide links between the CMOS die and the package interface. This eliminates the parasitics associated with copper bumping and enables lowloss, energyefficient communication pathways.
With its ability to create ultradense, highbandwidth chiptochip links, the D2W hybrid bonding PDK is particularly suited for AI applications, advanced computing platforms, and highperformance GPU architectures.

**An important step toward full tape-out capabilities**
With this release, imec becomes the world's first to offer easyaccess interconnect PDKs at these integration levels and dimensions. This initial "exploratory version" provides the essential tools designers need to begin assessing the technology: systematic layout creation, automated and custom routing, and design rule checks.

"This first release is a pathfinding PDK," Nicolas Pantano, head of the demonstrator architect team at imec, explains. "It gives researchers, startups, and companies the essential tools to start designing, testing ideas, and providing feedback. As the PDKs mature, they will grow from exploratory design kits into complete, fabricationready toolsets with tapeout capabilities, enabling designers to take a layout created with these PDKs and have it physically manufactured on the pilot line, validating their concepts in silicon, not just in simulation."

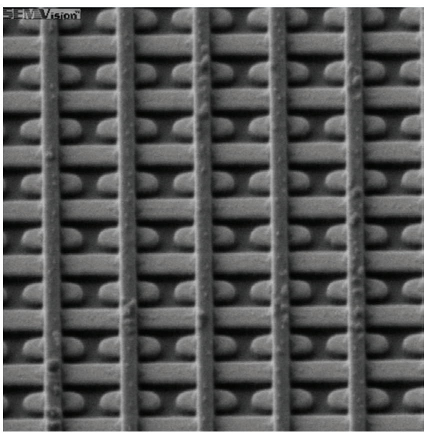
With the launch of these two interconnect PDKs, NanoIC expands its offering to a total of five publicly accessible process design kits. Following earlier releases of the N2, A14, and eDRAM PDK, the introduction of the finepitch RDL and D2W hybrid bonding PDKs marks the next milestone in building a complete beyond2nm design toolkit, spanning logic, memory, and now also interconnect technologies. To support handson exploration, NanoIC also hosts a dedicated workshop on the RDL and D2W PDKs on May 27, 2026. All practical details are available on the NanoIC website.

## Permanent DNA-based data storage for the AI Age

Imec and Atlas Data Storage, a pioneer of production-scale DNA data storage, have formed a new strategic partnership to accelerate the development of digital data storage using synthetic DNA. The collaboration combines Atlas' ASIC design expertise and scalable DNA synthesis technology with imec's deep expertise in advanced chip development, fabrication, and integration. In addition to prototyping and strategic support, imec is investing in Atlas.

As data creation and storage accelerates in the AI age, magnetic media such as tape and hard disk drives face unavoidable limits in density, sustainability, cost, and long-term reliability. DNA data storage compresses vast datasets into tiny volumes while ensuring ultra-long durability with minimal energy and maintenance.

DNA, nature's most compact and durable information storage medium, has preserved the evolution of life over billions of years within its biochemical four-letter code. One gram of DNA can potentially encode up to hundreds of




petabytes of digital data, achieving dramatic footprint and energy improvements impossible with magnetic storage media. While magnetic media requires data migration due to media deterioration - rewriting to new tapes and disk drives - DNA remains stable for thousands of years when properly encapsulated, meaning stored data never needs migration.

**DNA & Silicon: 100's of Gigabytes of data in a single synthesis cycle**
To help bring Atlas' vision to life, imec co-developed and monolithically manufactured a custom, exceptionally dense nano-scale array of electrochemical cells on top of a control CMOS ASIC designed by Atlas. The integrated chip orchestrates and controls millions of individual synthesis sites.

"To make DNA-based digital data storage viable, the synthesis throughput needs to scale by several orders of magnitude over today's approach," explains Siraj Nour ElAhmadi, Atlas Chief Operating Officer. "To meet this challenge, we anchored our solution on silicon, leveraging the very large-scale integration benefits afforded by CMOS technology. Our collaboration with imec was crucial to build the nano device layer on top of our CMOS ASIC. imec's 300 mm silicon platform is key to reach the necessary throughput and scale."

"One of the challenges was etching the platinum devices at very small dimensions, explains Simone Severi, imec Vice President of R&D. "Another critical design challenge was minimizing leakage currents between neighbouring devices at these extremely small dimensions. Our R&D team developed a custom process flow to ensure electrical isolation and stable operation across the dense array, a key enabler for reliable synthesis at scale."

IC-Link by imec manages the supply chain to source Atlas custom wafer for further post-processing on imec's processing line.

As demand for data storage grows, so does the need for sustainable high-density storage solutions. imec and Atlas partnership shows how the convergence of life science and semiconductors can unlock radically new ways to store, sense, and process data.

**Research and investment partnership**
Beyond the technical collaboration, imec and Atlas Data Storage are embarking in a deeper strategic collaboration where imec will become a shareholder of Atlas Data Storage. This approach is part of imec's venturing strategy where selected ventures benefit of the same type of support and strategic alignment as imec's own spinoffs. "With this approach, imec becomes a direct investor in Atlas Data Storage," observes Olivier Rousseaux, imec director of venture development. "As with other imec venture portfolio companies, Atlas will benefit from cutting-edge R&D and nano fabrication processing capabilities, as well as hands-on business support, leveraging imec's unique ecosystem of partners, investors and venture capital funds."

## Imec launches university consortium around next generation of chips

Imec has launched a first of its kind consortium with 26 European university groups that will jointly work on the technology roadmap beyond CMOS scaling (CMOS 2.0). This initiative will focus on design automation and chip architecture research for the next generation of chips. The consortium will benefit from the NanoIC pilot line, turning academic insights into industry-focused innovations. In the future, similar consortia will be set up around advanced materials and alternative compute systems.

CMOS 2.0 refers to a new paradigm, introduced by imec, that expands the chipmaking toolbox beyond traditional transistor scaling and its associated scaling challenges. CMOS 2.0 allows for more design flexibility by exploiting fine-grain wafer stacking technology to improve on-chip connectivity and offer higher technology heterogeneity to the system. It will result in tailored chips comprising multiple 3D-stacked layers that fulfil smartly partitioned functions. In that way, CMOS 2.0 will provide advanced, versatile 3D stacked platforms that push the boundaries of compute performance.

Introducing this new paradigm will have profound implications on how computing architectures are designed and optimized for future workloads and applications. CMOS 2.0 is a key differentiator for the realization of next-generation energy efficient compute


systems and is expected to impact a wide variety of applications from general purpose processors to High Performance AI Computing systems and even further for embedded AI applications at the edge.

This strategically important research requires cross-pollination between different areas of the ecosystem. Within imec's CMOS 2.0-consortium, 26 PhDs will be funded. The PhD students will stay at their home university, embedded in their research group, allowing them to tap into complementary fields of expertise and stimulate cross-fertilization. The participating universities and imec will jointly develop the necessary know-how that lays down the foundation of the next generation CMOS technology platforms and their associated compute architectures. Moreover, the collaboration will support workforce and skill development in Europe to meet current and future industry needs.

Sahar Sahhaf, Director Academic Partnership Development: "The attraction for the concept of CMOS2.0 is clear, but the obstacles are equally substantial. Leveraging the benefits in both connectivity and heterogeneous integration enabled by 3D wafer stacking will reshape every stage of design and chip architecture. It requires convergence of expertise, close collaboration, and coordination. It's the first time that imec brings together such a network of premium European university teams in a structured way to have guided contributions to the future semiconductor roadmap. We are excited to further connect academic inputs in our industry-driven programs to put Europe in the forefront of research on advanced computing technologies."

Of particular importance is the presence of the NanoIC pilot line hosted by imec in Leuven and its decisive role in empowering the CMOS 2.0 academic consortium. Its state-of-the-art tools are embedded within a strong, collaborative ecosystem of industry partners. PhD students can gain early exposure to next-generation semiconductor logic, memory and 3D technologies through process design kits (PDKs), which will enable them to develop system-level thinking; which is typically only encountered much later in a research or industrial career.

As such, it bridges the gap from academia to industry, facilitating a rapid transfer of knowledge and advanced technology from research labs to the market, thus strengthening Europe's industry.

**The CMOS 2.0 university consortium consists of following universities:**
- National Technical University of Athens
- Delft University of Technology
- École Polytechnique Fédérale de Lausanne (EPFL)
- Eidgenössische Technische Hochschule Zürich
- Karlsruhe Institute of Technology
- Katholieke Universiteit Leuven
- KTH Royal Institute of Technology
- LIRMM, University of Montpellier, CNRS
- Politecnico di Torino
- Sabancı University
- Universidad Complutense de Madrid
- Universiteit Gent
- Université libre de Bruxelles
- University of Thessaly

# Beyond High-NA EUV:

## Particle accelerator technology promises exciting future for lithography

**Jerome Paye, CEO of TAU Systems, outlines how the company's compact free-electron laser technology addresses the semiconductor industry's most pressing bottleneck, manufacturing ever smaller, more complex chips at a faster rate than currently possible.**

THE semiconductor industry is entering a period of profound transition. As extreme ultraviolet (EUV) lithography approaches both its physical and economic limits, and as AI-driven workloads push demand for ever-denser and more energy-efficient compute, the question of "what comes next" has shifted from theoretical to urgent.

High numerical aperture (High-NA) EUV systems represent the current frontier, but even these machines are increasingly viewed as stepping stones rather than endpoints.

Jerome Paye, a senior technology leader working at the intersection of accelerator physics and semiconductor manufacturing, outlines a vision that departs significantly from conventional lithography roadmaps: compact, laser wakefield acceleration (LWFA)-driven light sources designed to replace traditional EUV source architectures. The implications of such a shift are not incremental - they suggest a potential restructuring of how advanced lithography tools are conceived, built, and integrated into fabrication environments.

### The approaching limits of EUV scaling

The semiconductor industry's lithography roadmap has historically been defined by successive leaps in light source technology - from deep ultraviolet (DUV) to EUV, and now toward High-NA EUV. Each transition has enabled smaller feature sizes, tighter transistor densities, and improved performance-per-watt.

However the industry is now approaching a critical inflection point. The current EUV ecosystem, particularly at the 13.5 nm wavelength, is already the product of extraordinary engineering trade-offs. It relies on a complex chain of systems: high-power $CO_2$ lasers, tin droplet plasma generation, and highly specialized multilayer mirrors capable of reflecting EUV photons with extreme precision. Even within this optimized architecture, further scaling is becoming increasingly difficult.

High-NA EUV extends resolution by increasing optical numerical aperture, but at the cost of dramatically more complex and expensive optical systems. The industry is therefore confronting a dual constraint: physical limits in wavelength reduction and escalating economic burdens in system scaling. This is not a distant concern. It is a present-day engineering reality requiring immediate research investment.

Each lithography generation requires long development cycles, meaning that "what comes after High-NA EUV" must already be in development today if it is to be viable in the next decade.

## From accelerator physics to lithography: a shift in paradigm

The proposed alternative originates not from traditional semiconductor equipment design, but from the field of particle acceleration and free-electron laser (FEL) science.

Laser Wakefield Acceleration (LWFA) uses ultra-intense laser pulses to generate plasma waves capable of accelerating electrons over extremely short distances. The compact accelerator technology is proven. Getting to high repetition rate and average power is the engineering challenge. This approach can produce electron beams of very high energy and brightness in compact footprints compared to conventional radio-frequency accelerators.

These electron beams can then be used to generate extremely bright radiation sources, including in the X-ray regime, via undulator structures or related emission mechanisms.

This brightness is the key differentiator. In semiconductor lithography, the ability to generate extremely fine features depends directly on photon brightness and coherence. Traditional EUV sources, while powerful, are fundamentally incoherent plasma emitters - closer in behaviour to a light bulb than a laser pointer.

By contrast, accelerator-driven systems offer the possibility of far higher brightness and potentially more coherent emission, opening pathways to tighter feature control and improved pattern fidelity.

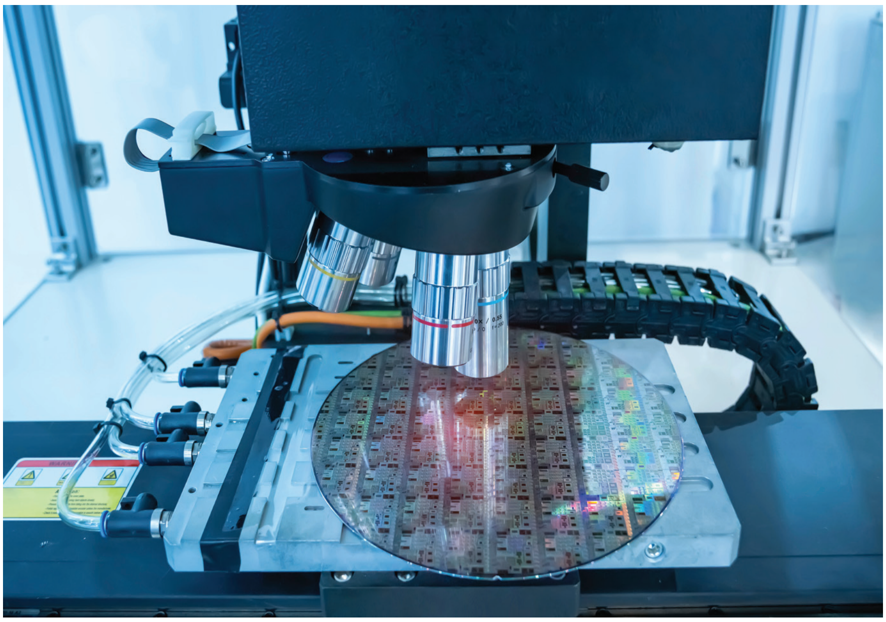
This technological lineage is not purely theoretical. Large-scale facilities such as the Stanford Linear Accelerator Center (SLAC) and the European XFEL (European X-ray Free-Electron Laser) have already demonstrated the extraordinary brightness achievable with FEL-based architectures. However, these installations are vast - spanning campus-scale infrastructure and hundreds of meters of accelerator tunnels. The challenge, therefore, is not whether the physics works, but whether it can be miniaturized into something compatible with semiconductor manufacturing environments.

## Rethinking EUV: from incoherent plasma to tunable sources

To understand the significance of LWFA-based lithography sources, it is important to contrast them with the existing EUV generation method. Conventional EUV systems rely on high-power lasers firing at streams of tin droplets. These droplets are vaporized into plasma, and as the tin ions recombine, they emit EUV radiation centered around 13.5 nm.
This wavelength is not arbitrary; it represents a carefully optimized balance between mirror reflectivity, resist sensitivity, and plasma efficiency. However, the emission process is inherently incoherent. It produces photons across a distribution of phases and directions, requiring extensive downstream optics to collect, filter, and shape the usable radiation.

Moreover, EUV lithography is locked into a tightly coupled system constraint: the light source, reflective optics, and photoresist materials must all be co-optimized around a single wavelength. This "Goldilocks zone" is one of EUV's greatest engineering achievements - but also one of its fundamental limitations.

The LWFA-based approach aims to break this constraint by introducing a tunable light source. Rather than forcing all subsystems to converge around a fixed wavelength, the source itself can be adjusted. This decouples one of the most rigid dependencies in lithography system design. Such tunability could allow engineers to select optimal wavelengths for both mirror coatings and resist chemistry, rather than forcing all components into a narrow, predefined band. In principle, this could simplify the materials science challenge that has historically constrained lithography scaling.



> This technological lineage is not purely theoretical. Large-scale facilities such as the Stanford Linear Accelerator Center (SLAC) and the European XFEL (European X-ray Free-Electron Laser) have already demonstrated the extraordinary brightness achievable with FEL-based architectures

## Economic and energy constraints in advanced lithography

Beyond physics, economics plays a central role in determining lithography viability. Today's EUV scanners, particularly those developed by leading equipment manufacturers such as ASML, represent some of the most complex and expensive machines ever built.

**Their cost structure is driven by multiple subsystems:**

- High-power laser sources, often housed in separate installations
- Precision plasma generation systems
- Multilayer reflective mirror systems with near-atomic precision
- High-speed wafer handling and positioning systems

Each subsystem is independently complex, and together they create a capital-intensive ecosystem.

Energy consumption is also a growing concern. EUV systems require significant electrical input to generate usable photon output, and as throughput demands increase, energy scaling becomes a non-trivial constraint for fabs.

The LWFA-based approach proposes a rebalancing of this equation. By focusing exclusively on the light source component, and by leveraging highly efficient laser-to-light conversion mechanisms, the goal is to improve the capital efficiency and energy performance of the most fundamental element of the lithography chain. Rather than attempting to replicate the full complexity of EUV systems, the strategy is to replace one critical bottleneck: the light source itself.

## Compact systems and fab integration

One of the most striking differences between traditional accelerator-based light sources and the proposed LWFA system is physical scale. Conventional FEL facilities, including those at SLAC and the European XFEL, require extensive tunnel infrastructure and dedicated buildings. This scale is incompatible with semiconductor fabrication environments, where floor space is both expensive and tightly constrained. The envisioned alternative is dramatically smaller, on the order of a shipping container.

]This reduction in footprint is not merely an engineering convenience. It fundamentally changes deployment strategy. Rather than centralizing light generation in a remote facility and distributing beams (a non-starter for EUV due to loss and complexity), the system can be integrated directly into fabrication facilities.

This enables a "one light source per scanner" model, analogous to current EUV tool architectures, but with significantly reduced spatial and infrastructural demands. Fabs cannot be relocated to accommodate equipment. Instead, equipment must adapt to the existing fab environment. This design philosophy is central to the LWFA development roadmap.

## Toward industrial reliability: repetition rate and stability

A major challenge in translating accelerator physics into semiconductor manufacturing lies in reliability and repeatability. Laboratory systems often operate under conditions that are unsuitable for industrial deployment.

The system under development is based on a 100 Hz laser repetition rate, supplied via a dedicated industrial laser configuration. While modest compared to eventual lithography throughput requirements, this represents a significant step forward from earlier academic demonstrations.

Repetition rate is critical because it enables feedback control systems. At sufficiently high pulse frequencies, real-time stabilization becomes possible, allowing correction for vibration, drift, and other environmental factors.

However, lithography is ultimately an average power problem. To meet industrial throughput requirements, both pulse energy and repetition rate must scale together. The current work therefore focuses on a dual challenge: increasing per-pulse energy while simultaneously increasing repetition frequency, all while maintaining beam stability and reproducibility.

## AI demand and the economics of scaling nodes

The urgency of next-generation lithography is being accelerated by the rapid expansion of AI workloads. AI accelerators and advanced logic devices require increasingly complex patterning, pushing lithography systems toward their limits.

One of the key constraints in current EUV-based manufacturing is multi-patterning. When a single exposure is insufficient to define a feature, multiple exposures are required, increasing cost, reducing throughput, and adding process complexity.

Shorter wavelengths, potentially achievable through LWFA-driven sources, could enable single-pattern exposures for features that currently require multiple steps. This would represent a major shift in manufacturing economics, reducing both cycle time and process variability.

This is a return to a more direct patterning regime, where scaling is achieved through physics rather than repeated process layering. While fundamental physical limits ultimately remain - no lithography system can extend indefinitely toward atomic-scale resolution - the potential headroom beyond current EUV systems is considered significant.

## Roadmap: from laboratory system to industrial tool

The path from experimental accelerator technology to semiconductor-grade lithography source is long and complex.

The most critical milestones are not purely about performance, but about industrialization.

**Key priorities include:**
- Increasing repetition rate for higher throughput
- Achieving pulse-to-pulse stability
- Demonstrating long-term operational reliability
- Integrating diagnostic and feedback systems for real-time control

The system currently being developed is intended as a testbed for these capabilities. It incorporates extensive diagnostics and stabilization mechanisms designed to convert a scientific instrument into a production-grade tool.

The interviewee acknowledged that this transition is non-trivial and likely to take years, comparable in complexity to the historical development of EUV itself. However, they also noted a key advantage: modern development benefits from decades of prior work in free-electron laser research across global institutions.

Unlike earlier generations of lithography innovation, much of the foundational physics has already been demonstrated in large-scale scientific facilities.

## Redefining Moore's law through new light sources

The broader question raised by this technology is whether it could extend or reshape the trajectory of Moore's law. Rather than focusing solely on transistor scaling, the next phase of semiconductor advancement may depend on the evolution of the

lithography light source itself.
If compact, accelerator-driven systems can deliver higher brightness, shorter wavelengths, and improved tunability, they could open a new scaling pathway beyond EUV and High-NA EUV.

However, this is not as a replacement for existing technology, but as an expansion of possibilities. The goal is not to declare EUV obsolete, but to remove the current bottlenecks that limit future node development.
In this sense, LWFA-based lithography represents a potential third paradigm shift in optical lithography: following deep UV, EUV, and now toward tunable accelerator-driven sources.

## A new frontier for lithography infrastructure

The semiconductor industry has repeatedly reinvented its core manufacturing technologies to sustain scaling. From optical lithography to immersion systems and EUV, each transition has required a convergence of physics, engineering, and economic alignment.

Laser wakefield acceleration represents a radically different direction - one that draws from high-energy physics rather than traditional optical engineering. Its promise lies not only in performance but in rethinking the architecture of light generation itself.

While significant challenges remain in scaling, stability, and integration, the potential impact is substantial: smaller footprints, tunable wavelengths, improved energy efficiency, and new pathways for resolution scaling.
As AI continues to accelerate demand for compute, and as EUV approaches its structural limits, the search for the next lithography paradigm is no longer speculative. It is becoming a defining question for the future of semiconductor manufacturing.

Whether compact accelerator-driven light sources ultimately fulfill that role remains to be proven. But the direction of travel is increasingly clear: the next revolution in lithography may not come from better optics alone, but from fundamentally rethinking how light itself is generated.

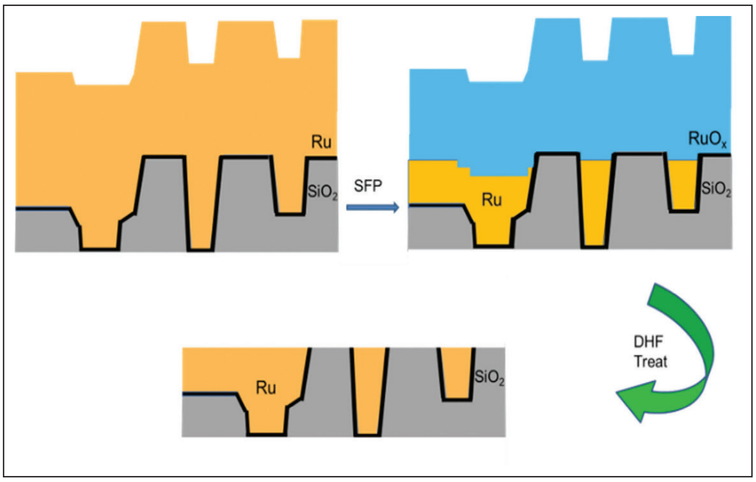
# Emerging stress-free ruthenium removal in advanced-node interconnects

A proposed SFP–wet etch integration demonstrates strong potential as a replacement for conventional CMP in advanced-node Ru interconnect fabrication and has the potential to minimize defects due to the absence of mechanical stress, abrasive particles and chemical components from the CMP slurry.

**BY LEO ARCHER, TECHNICAL PROGRAM DIRECTOR, ACM RESEARCH**

THE PROCESS technology and materials in sub-3nm semiconductor chips are changing rapidly to improve device performance. In the interconnect layers of semiconductor chips, the material and electrical resistance of copper titanium/titanium nitride

(Ti/TiN) films increase as the critical dimensions of advanced transistors shrink. The electromigration of the Ti/Tin copper (Cu) stack can also become a challenge due to the high current levels passing through the interconnects. These conventional films do not meet the criteria needed for an advanced interconnect in leading-edge logic devices. Copper's physical and electrical properties lead to higher resistance, which reduces the amount of current that can effectively run through the interconnect. The performance of the transistor slows down and generates considerable heat, which can also impact the performance of the transistor and computer system.




➤ Figure 1. Stress-Free Polish and HF Etch Process Flow.

## Utilizing Ruthenium for advanced-node semiconductor processing

Within advanced nodes for semiconductor processing, new materials for interconnect technology are emerging to address the challenges in the interconnect region. In a research collaboration between ACM Research (Shanghai), Inc., and the School of Materials Science and Engineering at Tsinghua University[1], it was found that Ruthenium (Ru) is a new material being explored for use as a liner and interconnect material for advanced-logic chips. Ru is especially useful in high-performance computing and artificial intelligence applications.

Ru's resistance and electrical performance are superior to Cu at dimensions below 17nm[2]. Chemical vapor deposition (CVD) of Ru exhibits significant potential as a contact, liner or interconnect material in advanced semiconductor technologies, making it an optimal replacement material for the Cu Ti/Tin stack. In addition to Ru's electrical advantages at smaller features, the material is less prone to diffusion in silicon (Si) and silicon dioxide ($SiO_2$) and thus does not need a barrier layer or a liner such as the Ti/TiN liner used for Cu. This simplifies the interconnect process, as only one deposition step is required[3].

## Ruthenium removal challenges

The ability to use CVD or atomic layer deposition in place of sputtering can eliminate voids in the interconnect that also impact the resistance of contacts and vias. Copper provides an advantage by being easily planarized using chemical-mechanical planarization (CMP) technology. Ruthenium, on the other hand, has a higher hardness and a greater chemical inertness, making its removal challenging in a conventional CMP process. These challenges include a low removal rate and poor selectivity between Ru and the metal nitride barrier layer. A different process technology is needed to more easily integrate Ru into the interconnect process. This article details an integrated stress-free polishing (SFP) and wet etching process developed as a novel solution for efficient Ru removal to eliminate some of the above challenges. By using an electrochemical reaction mechanism, the SFP step modifies the Ru surface to form a thin ruthenium oxide ($RuO_2$) layer. This oxide layer can be readily etched by hydrofluoric acid (HF) solution.

Because Ru is essentially inert in HF, there is excellent selectivity between Ru and $RuO_2$; an optimized process demonstrates this high removal selectivity. Moreover, the absence of mechanical stress, abrasive particles and chemical components from the CMP slurry during the process is expected to significantly minimize associated defects and potentially improve yields. The proposed SFP–wet etch integration reveals strong potential to serve as a replacement for conventional CMP in advanced-node Ru interconnect fabrication, offering etch rates and selectivity that will meet the requirements of advanced interconnect processes.

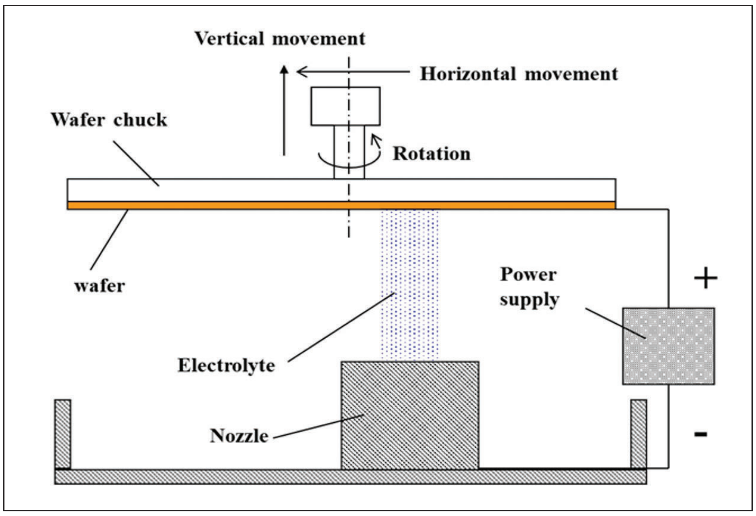
## Emerging Ruthenium removal solution

An SFP technology using an electrochemical reaction mechanism was applied to treat the Ru surface and form a $RuO_2$ film, which was then etched by HF, while the metallic Ru, which has a significantly lower etch rate in HF, was barely affected. By carefully controlling the electrochemical reaction, the thickness of the $RuO_2$ can be controlled, removing the $RuO_2$ and resulting in a planar surface. The integrated process flow consisted of oxidizing the Ru and a stress-free polish with a HF etch, all processed sequentially in the same chamber (Figure 1).

Figure 2 shows the experimental setup for the SFP. The wafer is fixed on a chuck, which carries the wafer and can be moved horizontally and vertically, along with the rotational movements typically used in a CMP process. The thickness of the $RuO_2$ is controlled by electrolyte property, process current, wafer rotation speed, horizontal movement speed and electrolyte flow rate.

The process conditions can be optimized for the formation of the $RuO_2$. The absence of mechanical stress, abrasive particles and chemical components typically found in a CMP slurry process is expected to significantly reduce defects on the wafer surface.

Two different samples were prepared for the experiments. Silicon wafers with a 200nm Ru layer were diced into approximately 4cm x 4cm pieces for the preliminary tests. Each piece was affixed to a 300mm blanket Cu wafer at a radial position of 75mm from the wafer center using conductive Cu tape. The samples were subjected to a sequential SFP and diluted HF (DHF) cleaning process. To create a reference surface, the left half of each Ru piece was masked with a piece of rectangular tape to prevent polishing.




➤ Figure 2. Stress-Free Polish Mechanism.

The second set of samples for the experiment were Si wafers coated with a Ru layer. This sample set also had tape covering a small part of the surface at a similar location as the first experiment, with a radial position of 75mm. The experimental process formed a step height between the masked and unmasked regions.

A stylus profilometer was used to measure the resulting step height, and the Ru removal rate was calculated accordingly. The ESP9000 chemistry developed for the experiment was used as the polishing electrolyte with a flow rate of 32 LPM from the main nozzle (see Figure 2). The wafer was rotated at a speed of 100 RPM. The varying constant voltage of 0, 50, 100 and 200V was applied, respectively, for four samples with a polishing time of 60 seconds. The DHF cleaning/removal process used a solution of 3 %wt. DHF at a flow rate of 1.5 LPM for 120 seconds.

## Test results and insights

The results of the first set of experiments using diced Ru samples on a blanket Cu wafer are shown in Table 1. Upon removal of the tape, which prevented polishing the Ru, the stylus measurements gave the following results. The baseline sample with no voltage applied and no SFP demonstrated only 99Å of Ru removal. When 50V

| No | Process Condition | Removal Thickness (Angstrom) |
|---|---|---|
| 1 | No SFP | 99 |
| 2 | SFP 50V | 90.4 |
| 3 | SFP 100V | 959.2 |
| 4 | SFP 150V | 1336.2 |

➤ Table 1. Removal Thickness Under Different SFP Conditions.

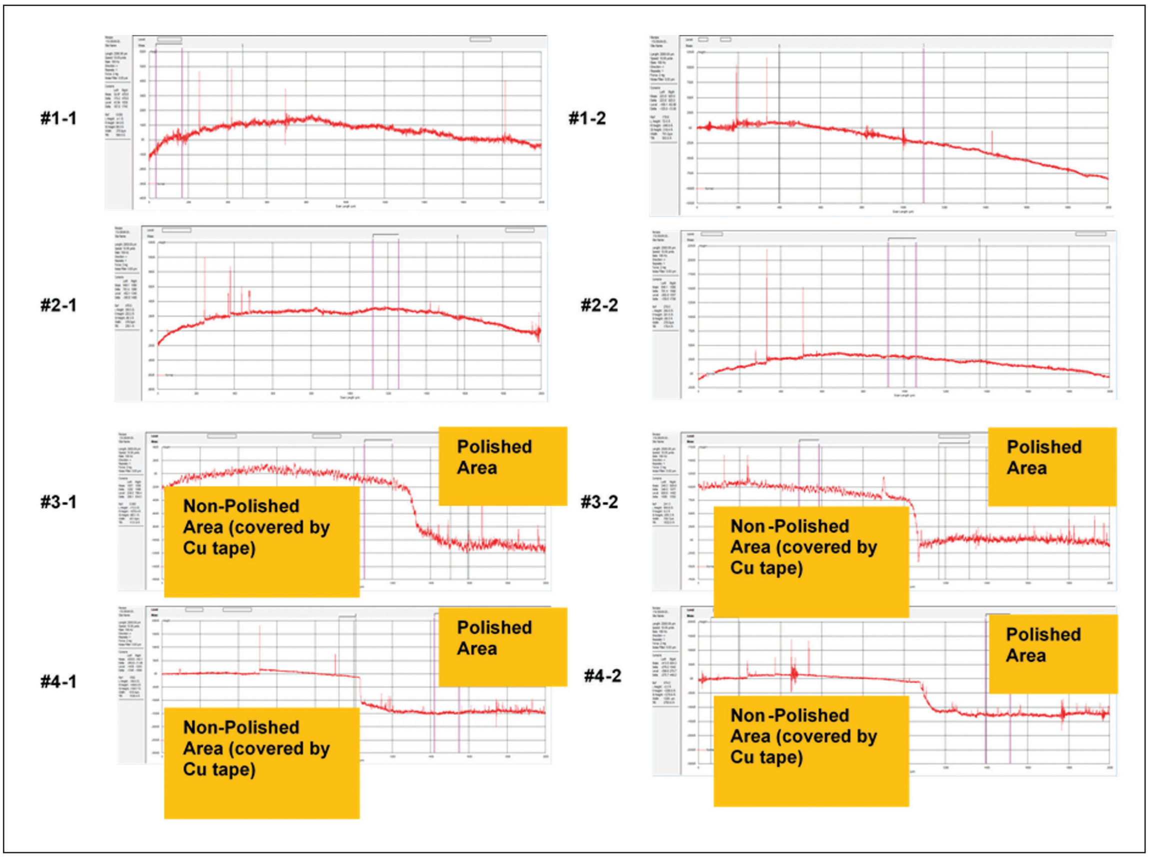



Figure 3. Removal Thickness vs. SFP Process Voltage.

was applied with the SFP, there was also very little removal, with only 90Å of Ru removed. The higher voltages of 100V and 150V, combined with SFP, resulted in higher etch rates of 959.2Å and 1336Å, respectively. Figure 3 shows the step profiles of the first set of samples using diced Ru chips on a 300mm Cu wafer.

Because Ru is relatively inert in HF, sample 1 had minimal etching, as was expected. Increasing the voltage to 50V and adding the SFP also showed limited etching, as the voltage was not strong enough to induce the electrochemical reaction to form significant $RuO_2$ on the wafer surface. The higher voltages of 100V and 150V, respectively, demonstrated oxidation of the Ru film and the subsequent etching of the $RuO_2$ layer. Based on these results, it was concluded that the Ru layer had a very limited reaction with the HF etch, making it an effective etch-stop layer between the $RuO_2$ and the Ru. Hence, the Ru removal is equal to the oxidized $RuO_2$ thickness during the SPF process.

In the second sample set, the voltage was increased to 200V to maintain a higher level of current density due to the larger surface area that needed to be polished. After a 120-second SFP, the measured step height was 1820.9Å and 1814.8Å between the polished and unpolished areas on the selected sample, respectively. This demonstrates that a Ru removal rate of more than 15 Å/s can be achieved, which would be acceptable for a manufacturing-worthy process with a blanket Ru deposition across the wafer.

The formation of the $RuO_2$ is primarily controlled by the voltage and the electrolyte applied to the wafer surface during the SFP. From the thicknesses that were obtained, the higher the voltage, the faster the formation of $RuO_2$, and thus the higher the etch rate when exposed to HF. Figure 4 shows Ru removal on a 300mm wafer.

## Ru/$SiO_2$ removal selectivity

The Ru interconnect structure also includes a $SiO_2$ layer that is used as an insulator under the interconnect and is used for defining the structure in the interconnect regions. Many times, this material is a low-k $SiO_2$ to improve the resistance capacitance

Figure 4. Removal Thickness for the Whole Ru Wafer.

properties of the transistor. Because $SiO_2$ is readily etched by HF, it was critical to evaluate the selectivity between the $SiO_2$ and the $RuO_2$. To do so, a series of experiments was designed to look at different HF concentrations on $RuO_2$ and $SiO_2$ during the SFP process using the same conditions as the above experiments.

As Table 2 illustrates, the higher the concentration of HF, the higher the etch rate of the $SiO_2$ layer. The $SiO_2$ also etches faster than the $RuO_2$. Thus, the HF used in the process will need to be of a lower concentration to achieve the optimum selectivity and etch rate for the Ru-removal SFP process.

Figure 5 shows the Pourbaix (potential-pH) diagrams for Cu and Ru in aqueous solution, which illustrate how the different Cu and Ru oxides form with varying pH and electrode potential. Copper readily forms oxides or is dissolved to ionic species over a wide pH range, even at relatively low electric potentials. Ru, however, is markedly inert; the formation of an oxide requires much higher potentials, and direct dissolution of Ru (in the form of $RuO_4$-) occurs only under restricted conditions.

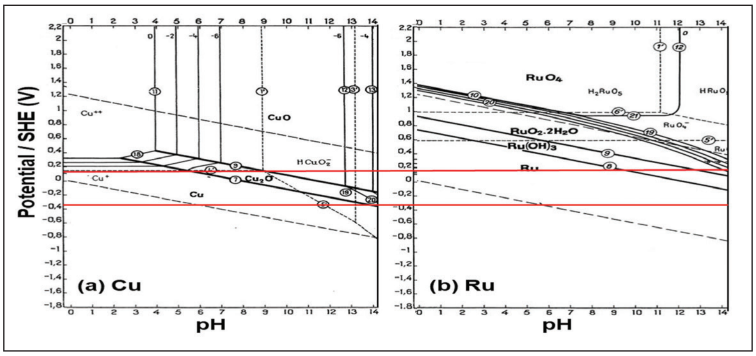
This is why common oxidizers in CMP slurries struggle to oxidize Ru and why it is challenging to remove using conventional CMP processing. It also highlights the advantage of applying a voltage during the SFP to deliberately regulate $RuO_2$ formation and its subsequent removal in the SFP process.

During the SFP using the external bias, the obtained Ru(III), Ru(IV) or Ru(V) oxides and hydroxides react with DHF to form soluble species, Hx [RuF6], through reactions 1–5 below. The ruthenium oxides are carried away by the solution flow, efficiently removing the oxidized material. Meanwhile, the underlying metallic Ru remains intact because DHF alone cannot oxidize and react with the inert Ru, allowing the film-removal thickness to be precisely controlled within the integrated process parameter.

The integrated process uniformly and efficiently removes the oxidized Ru, leaving a uniform Ru surface. By adjusting the HF dilution levels, the selectivity between the $RuO_2$ and the $SiO_2$ insulation layer can be optimized to leave a uniform surface. The lack of abrasives could minimize defects and result in higher yields.

## Future outlook of advanced-node ruthenium interconnect fabrication

In this work, an integrated process of SFP and HF wet etch was developed as an emerging stress-free Ru-removal solution. Through the optimization of process parameters of voltage, electrolyte and HF concentration, the rapid removal of Ru on Si wafers of more than 1800Å within 120 seconds was achieved. Furthermore, by fine-tuning the DHF concentration, a high removal selectivity between Ru and $SiO_2$ was also realized. The proposed SFP–wet etch integration demonstrates strong potential as a replacement for conventional CMP in advanced-node Ru interconnect fabrication and has the potential to minimize defects due to the absence of mechanical stress, abrasive particles and chemical components from the CMP slurry.




➤ Figure 5. Potential-pH Equilibrium Diagram for Cu-$H_2O$ and Ru-$H_2O$ Systems at 25°C.

| No. | Condition | Removal Rate Selectivity ($SiO_2$/Ru) |
|---|---|---|
| 1 | Ra (SFP + $SiO_2$ 1% DHF 20s)/Ra(SFP + Ru 1% DHF 20s) | 1.64 |
| 2 | Ra (SFP + $SiO_2$ 3% DHF 20s) Ra(SFP + Ru 3% DHF 20s) | 3.31 |

➤ Table 2. Removal Rate Selectivity ($SiO_2$/Ru).

| | |
|---|---|
| $Ru(OH)_3 + 6HF \rightarrow H_3[RuF_6] + 3H_2O$ | (1) |
| $Ru_2(OH)_3 + 12HF \rightarrow 2H_3[RuF_6] + 3H_2O$ | (2) |
| $RuO_2 + 6HF \rightarrow H_2[RuF_6] + 2H_2O$ | (3) |
| $RuO(OH)_3 + 6HF \rightarrow H_2[RuF_6] + 2H_2O$ | (4) |
| $Ru_2(OH)_5 + 12HF \rightarrow 2H[RuF_6] + 5H_2O$ | (5) |

➤ Table 3. Reactions.

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# Optimising SiCr deposition for high-yield bipolar-CMOS-DMOS manufacturing with picosecond ultrasonics

With picosecond ultrasonic technology, manufacturers have a powerful, non-destructive tool for monitoring thickness and reflectivity at the ready, one that ensures that SiCr films meets stringent performance standards.

**BY HUAYUAN LI, ALEX HONG, JOHNNY MU, TIMOTHY KRYMAN, AND PRIYA MUKUNDHAN AT ONTO INNOVATION**

FROM THE CARS we drive to the devices we hold and the medical systems that safeguard our health, bipolar-CMOS-DMOS (BCD) technology is at the heart of many modern electronics.

Today's vehicles are packed with electronics like power engine management, anti-lock braking systems (ABS), airbag controllers, and electric vehicle (EV) charging infrastructure, each one demanding a seamless integration of analog, digital, and power functions. In the case of smartphones, audio amplifiers, and smart home devices, BCD devices help balance power efficiency with high performance.

Meanwhile, medical imaging systems, such as ultrasound, and advanced power management solutions, rely on semiconductor technologies like BCD devices to handle diverse electrical requirements without compromising accuracy or safety.

Important as BCD devices may be, what exactly are they?

BCD devices are an advanced semiconductor process technology that integrates three distinct types of transistors – bipolar, CMOS, and DMOS – onto a single chip. The integration of these three transistors enables the simultaneous handling of analog, digital, and power functions within a compact and high-performance platform, with each transistor type contributing unique strengths:

- Bipolar transistors offer high current handling and precise analog control.
- CMOS transistors provide low power

consumption and high integration density for digital logic.
- DMOS transistors are optimized for high-voltage and high-current power applications.

For BCD devices to meet performance expectations, proper process control measures are needed, especially in the case of silicon-chromium (SiCr) thin films.

SiCr films play a critical role in BCD technology, primarily as precision resistive elements within analog and power management circuits (Figure 1.). SiCr resistors offer high stability, low temperature coefficient resistance (TCR), and excellent linearity, making them ideal for applications requiring accurate voltage and current control. Given the stringent reliability standards for BCD technology as demanded by the automotive industry and others, SiCr deposition must exhibit high reproducibility and minimal defectivity to support high-yield manufacturing and robust device performance under thermal and electrical stress.

Uniformity across the wafer and repeatability between lots are critical. After all, minor thickness or compositional variations can lead to resistance drift which impacts analog accuracy and long-term reliability. Tight process control during the deposition step—including chamber stability, target conditioning, and plasma uniformity—ensures consistent film morphology and stoichiometry.

During SiCr sputtering, the precise regulation of specialty gas flow, in particular reactive gases such as nitrogen or oxygen, is critical, as their partial pressures influence plasma chemistry and the kinetics of silicide formation on the substrate. This silicide layer governs nucleation and grain growth, which directly affects grain boundary spacing and, consequently, TCR. Variations in gas flow can alter the stoichiometry and microstructure of the SiCr film, leading to shifts in TCR behavior, including the onset of a pronounced negative coefficient if the process is not tightly controlled.

Given the importance of these demands, manufacturers need the right tools on hand to maintain proper process control and optimize the

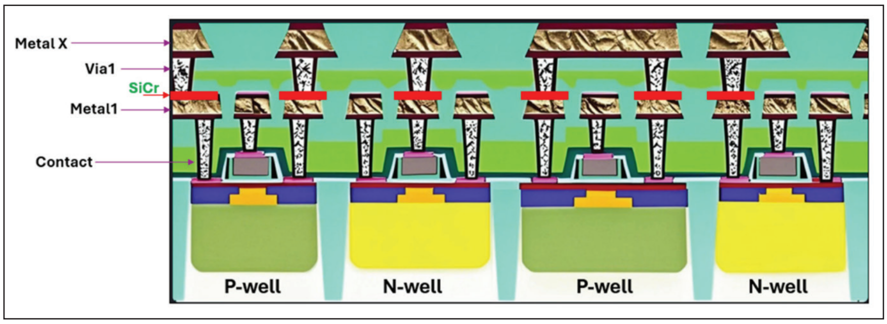



Figure 1. Schematic of the BCD process, with SiCr film identified.

performances of their BCD devices. In this article we will discuss the application of picosecond ultrasonic technology in two parts: one as a robust thickness metrology solution for qualifying SiCr deposition process and the second for excursion monitoring in BCD devices.

## About Picosecond Ultrasonic Technology

Picosecond ultrasonic technology (PULSE™ technology) is a non-contact, non-destructive pump-probe laser acoustic technique for the measurement of metal film thickness. It is a proven workhorse in semiconductor fabs around the world. A 0.1ps laser pulse (pump) is focused to a small (~ 8´10mm2) spot onto a wafer surface to create a sharp acoustic wave. The acoustic wave travels away from the surface through the film at the speed of sound. At the interface with another material, a portion of the acoustic wave is reflected and comes back to the surface while the rest is transmitted.

The probe pulse detects this reflected acoustic wave as it reaches the wafer surface. One can detect the change of optical reflectivity that is caused by the strain of the acoustic wave or alternatively detect, using a position sensitive detector (PSD), the deflection of the reflected probe beam that is

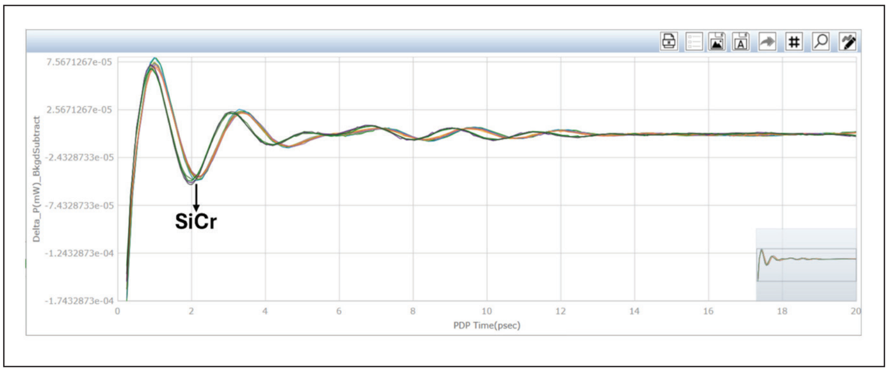



Figure 2a. Raw data of reflectivity change vs time shown. The cross-wafer variation is identified by the shift in acoustic echoes.

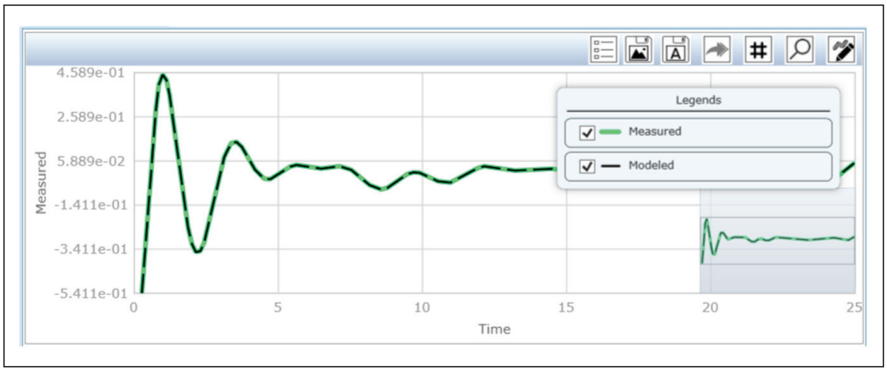



Figure 2b. Modeled fit to measured data shown. The green curve represents the measurement, and the black curve represents the fit.

caused by the deformation of the surface due to the acoustic wave. Both modes, reflectivity (REF) and PSD, are used in characterizing metal films. Knowing the speed of sound in the material, and the arrival time of the echoes, thickness is readily extracted using the first principles technique.

## Film Thickness

With background on picosecond ultrasonic technology out of the way, we will turn our attention to the application of this technology as a robust thickness metrology solution for qualifying SiCr deposition process in BCD devices. To demonstrate this, we measured the nominal thickness of SiCr thin films using picosecond ultrasonic technology.

Figure 2a shows the raw data from the SiCr thin film. The acoustic echoes identified in the figure are used to calculate the thickness of the film using the speed of sound and round-trip transit time through the film. Nominally, textbook values for the longitudinal speed of sound would be used. In the case of SiCr films, the longitudinal speed of sound will vary from the bulk material and depend on the deposition process (sputtering, evaporation, etc.) and specific film composition (stoichiometry, density, etc.).

As a one-time calibration, we used cross-section transmission electron microscopy (TEM) to obtain SiCr film thickness and calculated the speed of sound for this specific process to be 69.7Å/ps. The modeled fit to the measurement is shown in Figure 2b.

In Figure 3a, raw data from the DOE skew is shown. The shift in echo position between the different wafers demonstrates the sensitivity of the technique for monitoring the process. Within wafer uniformity profiles from 13 points across the wafer show consistent trends (Figure 3b).

Given the critical function of SiCr films in BCD device architecture, it is imperative to maintain highly uniform deposition with stringent process control to meet electrical and reliability specifications. Yield optimization is directly correlated with film uniformity as variations can significantly degrade device performance and long-term stability. As part of chamber qualification, more extensive sampling across the wafer, including to the edge, was performed (Figure 4). Those profiles are also consistent across the thickness skew.

Repeatability is a key metric in SiCr thin film metrology for ensuring robust process control and consistent device performance. Poor repeatability can obscure true process shifts, leading to incorrect corrective actions and potential yield loss. Gage capable repeatability measurements ensure compliance with automotive industry standards and are critical for long-term reliability. The dynamic repeatability data indicates performance is better than 0.5Å (1σ) and is more than sufficient to meet the process monitoring needs.

As demonstrated, picosecond ultrasonic technology provides a precise, non-destructive method for

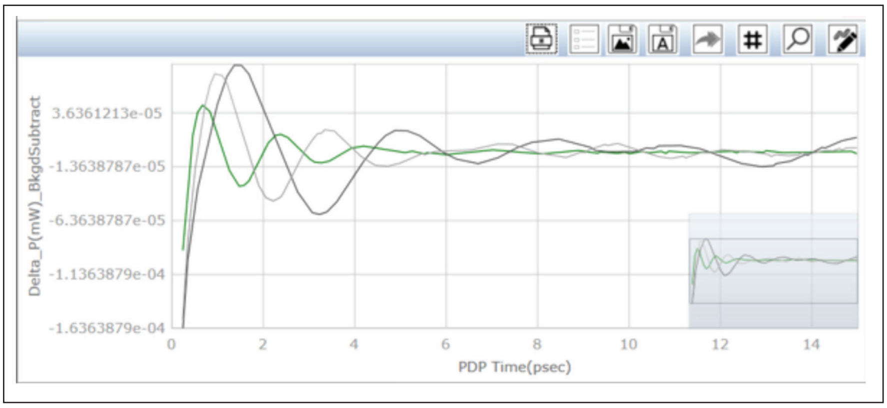



Figure 3a. Raw data from the DOE thickness skew. Delta represents the skew in thickness from the target. The shift in echo position demonstrates the sensitivity for process monitoring.

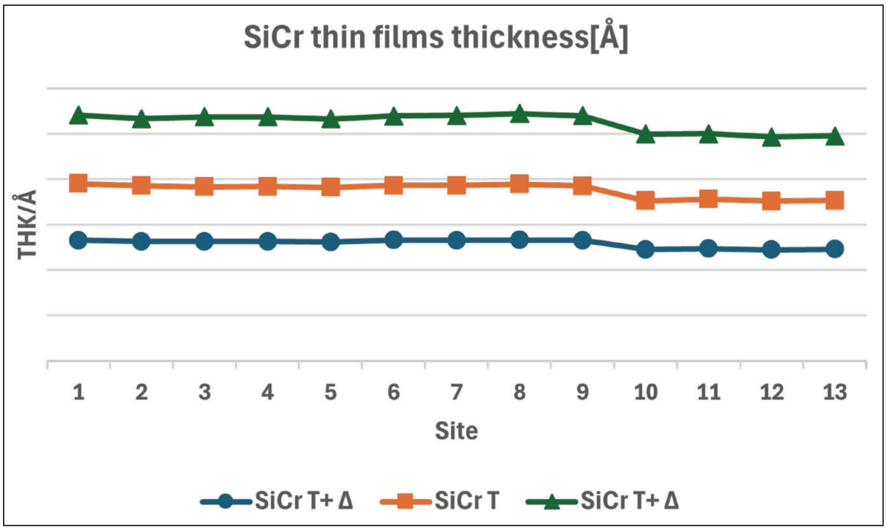
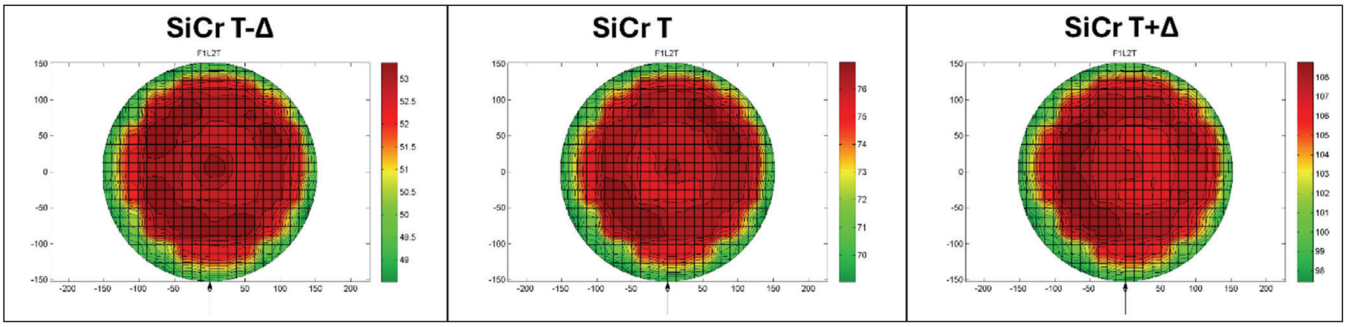



Figure 3b. Consistent cross wafer uniformity profiles for the three wafers.

In picosecond ultrasonic technology, acoustic echoes are used to calculate SiCr film thickness. However, simultaneously available probe reflectivity data can be leveraged to provide information that can be used for process optimization (i.e., gas flow) and flagging process excursions



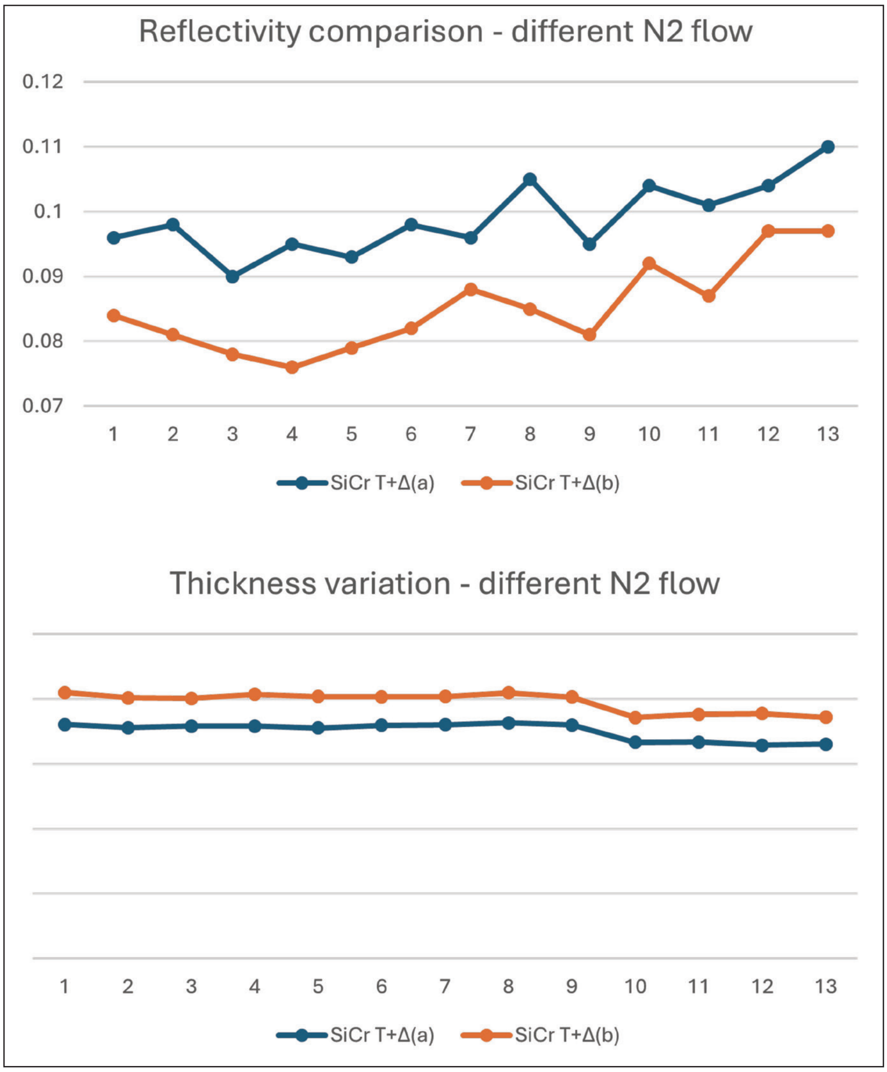

➤ Figure 4. Forty-nine point wafer uniformity profiles for the three wafers, including measurements to the edge of the wafer. The profiles were consistent across the entire wafer.

measuring film thickness, validated against TEM calibration. The technique also offers exceptional repeatability and sensitivity, enabling manufacturers to monitor wafer-to-wafer and within-wafer uniformity with confidence. This capability is critical for maintaining tight process windows, as even minor deviations in thickness can lead to resistance drift and compromise analog precision. By integrating this metrology into chamber qualification and process monitoring, fabs can ensure consistent SiCr deposition, optimize yield, and meet stringent reliability standards.

## Film quality

In picosecond ultrasonic technology, acoustic echoes are used to calculate SiCr film thickness. However, simultaneously available probe reflectivity data can be leveraged to provide information that can be used for process optimization (i.e., gas flow) and flagging process excursions. As such, this technique can be used to monitor the surface reflectivity of SiCr films; this application serves as a qualitative indicator of the film morphology and surface roughness and can be used for process control.

During the sputtering of SiCr films, gas flow has a strong influence on TCR as it impacts the film's microstructure and stoichiometry (density and composition). This, in turn, determines the film's stability, stress, and electromigration resistance in BCD applications. Uneven gas distribution causes local variations in thickness and composition leading to resistor mismatches and unpredictable TCR. The surface reflectivity of the target wafer at two different gas flow rates is shown in Figure 5. Reflectivity data was collected at the same time as the acoustic data and shows the variation in surface reflectivity. At gas flow rate (b), the surface was more




➤ Figure 5. Surface reflectivity comparison for films having the same target thickness but different reflectivity. Average reflectivity variation (top) across wafer is much higher than the thickness variation (bottom). Orange represents the lower flow rate, and blue represents the higher flow rate.

reflective corresponding to a smooth, dense film, whereas at flow rate (a), the reduced reflectivity indicates increased surface roughness which can degrade resistor uniformity and TCR stability. Also, the thickness variation SiCr film is thinner at the higher N2 flow. N2 is known to affect silicide/nitride formation, grain spacing, etc., and impacts both thickness and reflectivity. Studies are underway to characterize the impact of annealing temperature. The results are promising.

In summary, the surface quality of SiCr films plays an equally critical role in device stability and long-term performance. The study highlights how reflectivity measurements, captured alongside thickness data using the same picosecond ultrasonic platform, serve as a powerful indicator of film morphology and density.

Variations in gas flow during sputtering were shown to significantly influence both reflectivity and thickness, underscoring the importance of precise control over deposition parameters. A smoother, more reflective surface correlates with improved resistor uniformity and predictable TCR behavior, while rougher films can degrade electrical performance.

Based on these results, we have demonstrated that reflectivity measurements, along with thickness measurements, can be leveraged for in-line monitoring to detect deviations in deposition parameters. By leveraging dual metrics – thickness and reflectivity – manufacturers gain a comprehensive, in-line process control solution that enables early detection of excursions and proactive corrections, ensuring robust SiCr thin film integration in advanced BCD architectures.

## Conclusion

From automotive safety systems to medical imaging and consumer electronics, BCD technology enables the seamless integration of analog, digital, and power functions that modern applications demand. Yet, this versatility hinges on precise control of SiCr thin films whose stability and uniformity directly influence device reliability.

Achieving this level of integration comes with significant manufacturing challenges, particularly in controlling SiCr film thickness and gas flow during sputtering, factors which directly impact resistor stability and temperature performance, which are critical for reliability in demanding environments. To overcome these hurdles, we propose using picosecond ultrasonic technology.

With picosecond ultrasonic technology, manufacturers have a powerful, non-destructive tool for monitoring thickness and reflectivity at the ready, one that ensures that SiCr films meet stringent performance standards. In doing so, manufacturers will be able to safeguard the integrity of BCD devices while supporting the continued evolution of new technologies across the automotive, medical, and consumer electronics sectors.

# Unlocking yield improvements in advanced packaging through materials-driven failure analysis

Materials-driven failure analysis offers a systematic, multidisciplinary framework for understanding why defects occur, how they propagate, and what conditions exacerbate them.

**BY DR. PRADYUMNA (PRADY) GUPTA, FOUNDER & CHIEF SCIENTIST, INFINITA LAB | FOUNDER & CEO, INFINITA MATERIALS**

THE SEMICONDUCTOR INDUSTRY is at a pivotal moment. As digital transformation accelerates, driven by artificial intelligence, edge computing, 5G/6G connectivity, and electrification, advanced packaging has moved from being an incremental enhancement to a strategic imperative. Today's heterogeneous systems, ranging from 2.5D and 3D ICs to fan-out wafer-level packaging (FOWLP), deliver unprecedented performance density, improved power efficiency, and reduced form factors. Yet these benefits come with an unavoidable challenge: Yield pressure.

Yield is no longer merely about defect counts; it's about understanding how materials behave across scales, interfaces, and processes. Traditional defect inspection methods, while still valuable, are no longer sufficient on their own. The key to unlocking sustainable yield improvements lies in materials-driven failure analysis: a multidisciplinary approach that links material characteristics, structural integrity, process interactions, and comprehensive failure mechanisms into a unified diagnostic framework.

This article examines how materials science, advanced characterization, cross-functional collaboration, and predictive analytics converge to identify hidden failure drivers, enhance process accuracy, and deliver measurable gains in advanced packaging yield.

## Why yield matters more than ever in advanced packaging

Advanced packaging technologies, including FOWLP, 3D TSV stacks, chiplets, and integrated passive devices, are increasingly used to meet the demand for higher performance and smaller footprints. These approaches promise reduced interconnect length, improved signal integrity, and enhanced thermal performance. But they also introduce complex materials interfaces, thermal stresses, and multi-physics interactions that are highly sensitive to process variability.

In traditional packaging, yield problems could often be traced to specific process steps. In advanced packaging, yield excursions can originate from subtle variations in material properties, interfacial degradation, or microscale stress accumulationthat may not be readily observable with optical or electrical inspection alone.

The economic implications are significant. Yield improvements directly influence usable wafer output, which in turn affects revenue per wafer, cost of goods sold (COGS), and profitability. Even small incremental yield gains in high-value advanced packages can generate substantial financial returns. This is where materials-driven failure analysis becomes indispensable: it transforms yield investigation from reactive troubleshooting into a proactive engineering discipline.

## What materials-driven failure analysis actually means

At its core, materials-driven failure analysis is the systematic investigation of failure modes through the lens of materials behaviour and interactions. Rather than simply identifying that a failure occurred, this approach seeks to understand why it occurred at a fundamental level:

- What specific material property variations contributed to the defect?
- How did interfacial stress accumulate under processing conditions?
- Did thermal expansion mismatch cause microcracking or delamination?
- Were contamination or unintended residue responsible for electrical anomalies?

In advanced packaging, these questions often revolve around a handful of recurring themes:

- **Interfacial integrity:** Particularly between dielectrics, metal interconnects, solder joints, and underfill materials.

- **Thermo-mechanical stress:** From thermal cycling during reflow and operation, especially in stacked components.
- **Material anisotropy:** Variations in material properties depending on orientation or deposition method.
- **Environmental susceptibility:** Moisture ingress and electromigration in dense interconnect networks.

Materials-driven analysis involves correlating microscale material behavior with macroscale system performance. It assumes that to improve yields at scale, engineers must first understand the underlying multiscale physics.

## Bringing the right tools to the investigation

To implement materials-driven failure analysis, organisations must expand beyond conventional electrical tests and optical inspection. Modern failure analysis blends multiple characterization techniques:

- **Electron Microscopy and X-ray Imaging**
  Scanning electron microscopy (SEM), focused ion beam (FIB) cross-sectioning, and X-ray computed tomography (XCT) enable visualization of sub-micron defects, voids in solder joints, delamination, and dielectric cracking. These tools reveal structural anomalies that are invisible in traditional 2D microscopes.
- **Nanoindentation and Mechanical Property Mapping**
  These methods provide insights into local stiffness, hardness, and modulus variations, particularly at interfaces where materials with differing elastic properties meet. Mapping these mechanical gradients helps identify stress concentration zones prone to failure.
- **Thermal Imaging and Infrared Thermography**
  Because advanced packages often suffer from localized heating, thermal imaging helps pinpoint hotspots and thermal patterns that correlate with material degradation or poor thermal conduction paths.
- **Elemental and Phase Analysis**
  Techniques such as energy-dispersive X-ray spectroscopy (EDS) and electron backscatter diffraction (EBSD) reveal compositional variations, grain orientation, phase transformations, and unintended inclusions all of which influence reliability.
- **In-situ Stress/Strain Measurement**
  Advanced optical and X-ray-based methods enable stress mapping during thermal cycling or mechanical loading, providing a direct correlation between process conditions and material responses.

By combining these tools into an integrated workflow, engineers can transform raw data into actionable insight.

## Case study: Interfacial delamination in a 3D package

Consider a common failure mode of advanced packages: interfacial delamination between an organic substrate and a redistributed layer (RDL). On the surface, delamination appears as an area of poor adhesion detectable through acoustic microscopy. But mixed materials analysis often reveals the root cause lies in:

- A mismatch in the coefficient of thermal expansion (CTE) between layers
- Micro-scale voids generated during lamination
- Localised moisture trap points exacerbate thermal stress

Materials-driven analysis might proceed as follows:

- Thermo-mechanical modelling identifies zones of highest mechanical stress under reflow and service conditions.
- Nanoindentation and modulus mapping detect unexpected stiffness gradients near the interface.
- XCT imaging reveals micro-void clusters that act as stress concentrators.
- EDS analysis uncovers contamination or residue at the interface that reduced adhesion strength.

With this information, engineers can adjust the substrate prep process, revise laminate materials, or modify reflow profiles to minimise stress buildup — leading to measurable yield improvements.

This kind of diagnostic precision is only possible when material behavior is the starting point, not an afterthought.

## Materials databases and predictive analytics

Modern yield improvement practices increasingly incorporate materials databases and predictive models. By cataloguing materials properties, including modulus, thermal conductivity,

moisture uptake, and ageing behaviour, organizations can develop multi-factor predictive models that estimate failure probability under given process conditions.

Machine learning tools can also be employed to detect patterns in historical failure data, linking material signatures to defect types. For example, correlating shifts in specific viscoelastic properties with increased solder joint fatigue can pre-emptively flag future yield risks.

These data-driven methods reduce reliance on iterative trial-and-error and accelerate actionable insight across design, engineering, and production teams.

## Collaborative failure analysis workflows

High-volume manufacturing environments benefit from integrating failure analysis into cross-functional workflows. Materials insights must be communicated upstream to design and process engineers, and downstream to production teams. A robust feedback loop ensures that lessons from failure analysis directly influence design rules and process controls.

Increasingly, organisations are standardising failure reporting and remediation frameworks, enabling accountability and trend identification at enterprise scale.

Collaborative platforms unify data from lab analysis, field returns, reliability testing, and statistical process control, creating a closed-loop system of continuous improvement.

## Execution challenges and cultural shifts

Materials-driven failure analysis is not simply a set of tools; it is a mindset. Organisations that excel in yield improvement cultivate a culture where:

- Engineers embrace multidimensional investigation, not one-dimensional metrics
- Materials science is treated as a core competency, not a peripheral function
- Cross-disciplinary dialogue is encouraged between materials, reliability, process, and design teams

Investing in analytical infrastructure and talent is part of this shift, but so is enabling domain expertise to evolve through applied learning rather than rote troubleshooting.

## Benefits beyond yield

The value of materials-driven yield improvement extends beyond defect reduction. Organisations that understand their materials at a fundamental level benefit from:

- More predictable process windows
- Reduced time-to-market for new packages
- Higher confidence in reliability performance
- Fewer field failures and warranty costs
- Better readiness for next-gen materials like low-k dielectrics, novel underfills, and heterogeneous substrates

The approach builds resilience into the entire product lifecycle, from research to mass production to service.

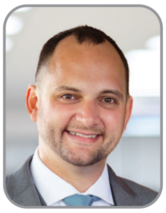
## Conclusion: A new imperative for advanced packaging

Advanced packaging is indispensable for meeting future compute, connectivity, and power requirements. Yet without a deliberate focus on materials behavior and failure mechanisms, yield challenges will remain a primary barrier to scalability and profitability.

Materials-driven failure analysis offers a systematic, multidisciplinary framework for understanding why defects occur, how they propagate, and what conditions exacerbate them. By leveraging advanced characterization, predictive analytics, and collaborative workflows, organisations unlock yield not as a temporary improvement but as an ongoing engineering discipline.

In an era when performance expectations are high and process margins are tight, the differentiator will not be inspection alone, but insight - insight into material behaviour, interface integrity, and how the tiniest anomalies can create the biggest impacts.

# When mechanics become yield-critical: motion design for the advanced packaging era



Advanced packaging has created new process bottlenecks related to the internal mechanics of the packaging equipment. As alignment tolerances compress from microns to tens of nanometers, motion platforms stop being background automation and instead become yield-critical infrastructure.

**BY JUSTIN BRESSI, BUSINESS DEVELOPMENT MANAGER, AEROTECH INC.**

VARIATIONS that previously sat comfortably below the sensitivity of the packaging processes — vibration, thermal drift, mechanical compliance, encoder latency — now surface directly as bonding defects, layer misalignment, or via inconsistency.

This shift is evident in production environments for hybrid bonding, fan-out packaging, and glass interposer manufacturing. The discussion below reflects the engineering challenges emerging across these applications, and how system-level motion design is reshaping what precision means in semiconductor assembly.

**SIS:** *What's driving the spike in motion-related failures in next-generation packaging equipment?*

**JB:** The primary driver is the tightening of alignment tolerances from the micron domain into the nanometer domain. At this scale, position stability is not determined by encoder resolution alone — it depends on how mechanical stiffness, thermal behavior, controller latency, cabling dynamics, and metrology timing interact while executing precise motion profiles.

Processes such as wafer-to-wafer hybrid bonding, high-bandwidth memory stacking, and through-glass via drilling expose this clearly. Any deviation in planarity, any vibration mode left undamped, or any drift over time becomes visible as yield loss. Effects once considered negligible now matter.

System-level precision is not a property driven by any one individual component; it is the emergent behavior of the entire motion system. Improvements must therefore be systemic, not incremental.

**SIS:** *Why can't legacy motion architectures simply be upgraded to meet these new tolerances?*

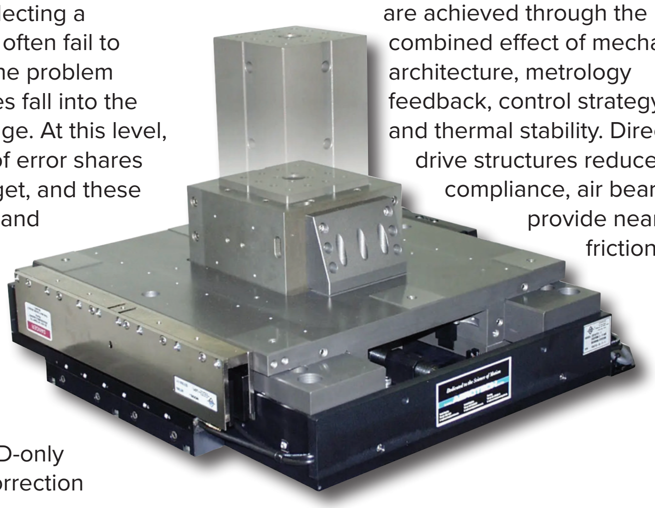
**JB:** Traditional upgrade paths — swapping to a higher-resolution encoder, adding compensation routines, or selecting a stiffer stage — often fail to fully address the problem once tolerances fall into the nanometer range. At this level, every source of error shares the same budget, and these errors interact and compound.

Legacy architectures often rely on stacked mechanical assemblies, PID-only control, and correction applied after error is detected. These approaches work when tolerances allow room for adjustment. They break down when correction latency exceeds the mechanical response time of the system.

The shift required is conceptual: motion must be co-engineered with the process, rather than added on as an automation layer. Integration, not component improvement, becomes the mechanism by which stability is achieved.

**SIS:** *How do you achieve sub-micron alignment and planarity in high-throughput hybrid bonding tools?*

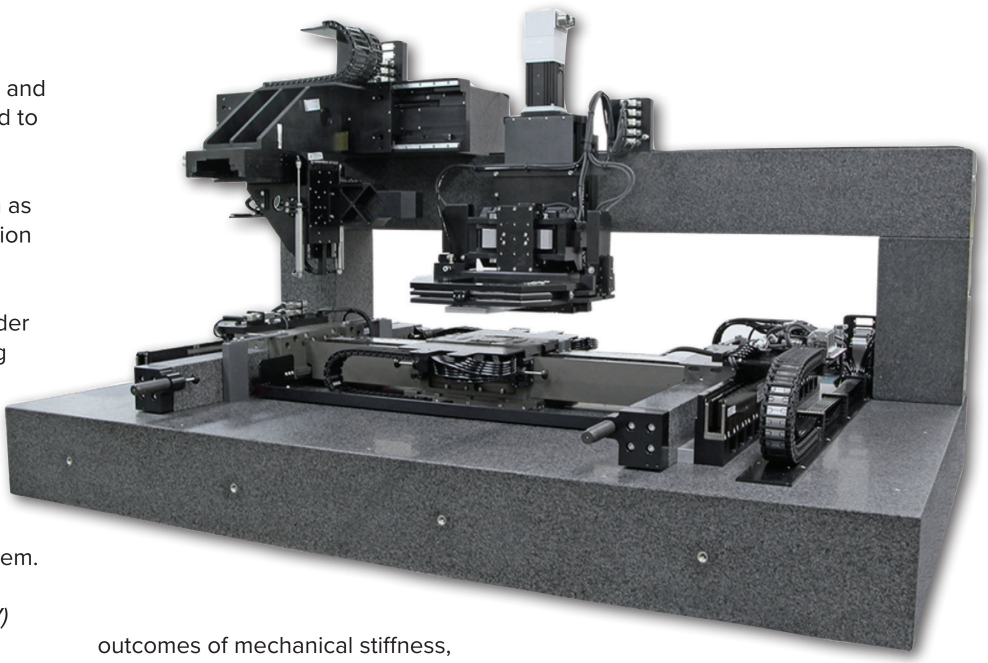
**JB:** Sub-micron alignment and planarity are achieved through the combined effect of mechanical architecture, metrology feedback, control strategy, and thermal stability. Direct-drive structures reduce compliance, air bearings provide near-frictionless



movement, high-resolution digital encoders or laser interferometers supply nanometer-scale feedback, and synchronization latencies are tuned to microseconds.

Thermal behavior matters as much as structural accuracy. Material selection and heat path design influence how the system behaves during extended operation, especially under the highly dynamic and demanding motion profiles needed to meet throughput targets.

Alignment is not produced by a single stage or sensor. It is the result of the entire motion stack being engineered as a unified system.



**SIS:** *Why is through-glass via (TGV) drilling considered a "worst-case" motion problem — and how is it being addressed?*

**JB:** TGV drilling simultaneously requires pinpoint accuracy, timing coordination between several subsystems, and extreme throughput. The substrate must be positioned precisely, the laser path must be synchronized with motion, and pulse placement must remain consistent even as the system accelerates through complex trajectories.

To achieve this in production environments, the servo stages and galvo scan heads must operate as a single coordinated motion system. Infinite Field of View (IFOV) blends the motion of both elements, eliminating stitching errors across the substrate. Position Synchronized Output (PSO) ensures each laser pulse is triggered at the correct spatial coordinate.

Setup and optimization are accelerated through machine-learning-based step-and-settle tuning (via Aerotech's DrillOptimizer tool), which identifies efficient motion and pulse parameters automatically.

This allows TGV performance to be repeatable and scalable, not just achievable in isolated demonstrations.

**SIS:** *Can precision and speed be co-optimized, or will they always compete?*

**JB:** Precision and speed can conflict if they are treated as independent objectives. In practice, they are both outcomes of mechanical stiffness, inertial sensing, and control design.

Increasing structural stiffness raises the natural resonance frequency of the system, allowing higher acceleration without inducing vibration. Real-time inertial feedback — such as integrated accelerometers — enables more aggressive servo tuning without overshoot. Control strategies that reflect the mechanical resonance profile maintain throughput without sacrificing accuracy.

The goal is not to balance speed against precision, but to engineer the system so that speed and precision are both reinforced by the system architecture.

**SIS:** *What challenges do equipment builders face when scaling from R&D tools to high-volume manufacturing systems?*

**JB:** A common issue is control platform discontinuity. Many tools begin development on one control architecture and shift to another for volume deployment, which forces re-tuning, re-validation, and software re-integration — often delaying high-volume introduction.

Consistent control architecture from prototype through pilot and into production avoids this disruption.

Software, motion behavior, and servo tuning should travel intact across the development cycle, and subsystems should scale rather than be redesigned. The motion architecture should scale with the tool, not reset when production begins.

## Where motion control is headed next

Motion control in advanced packaging is moving toward closer integration of motion, sensing, and real-time analysis. Rather than correcting drift or vibration after the fact, next-generation control layers will predict and compensate continuously, informed by models of mechanical and thermal variation.

Motion system data and in-process metrology are beginning to be fused natively, allowing deviations to be detected earlier and compensated automatically.

Machine-learning-driven auto-tuning will gradually reduce manual optimization, particularly as production tools accumulate operational datasets that can generalize across recipes and substrates. Meanwhile, the motion platform itself is increasingly recognized as part of the process architecture, rather than a mechanical subsystem — especially in chiplet assembly, hybrid bonding, and glass interposer manufacturing.

The next phase of advanced packaging will depend not just on accurate positioning, but on how effectively motion, sensing, and control evolve together as a unified system.

# Why new developments in MEMS are fundamental for next-generation devices

Advances in MEMS are set to be crucial for the future of sensors and mobile phones, but there are many other applications.

**BY DR. JOSEP MONTANYÀ I SILVESTRE, CEO AT NANUSENS**

SENSORS have tiny mechanical parts that move as a result of a specific stimulus and this movement is identified to form an electrical signal. MEMS (Micro-Electro-Mechanical Systems) technology is fundamental in the design and development of high functioning sensors and capacitors which are needed for next-generation devices.

With traditional MEMS there are some significant barriers, but there have been new developments in MEMS that are designed to address these issues.

Novel MEMS technology looks set to be at the heart of cutting-edge sensors and it is also being leveraged to deliver a solution to the challenge of creating better RF front ends for 6G.

## Barriers with traditional MEMS

Traditional MEMS involves bespoke design processes that can take years to perfect. MEMS production is usually undertaken on a custom line by specialized companies using proprietary processes to build each MEMS structure. Small variations during MEMS manufacturing can cause performance problems, so yields tend to be relatively low when compared to standard semiconductor manufacturing. Therefore, costs are high, scalability is a challenge and time-to-market is considerable for traditional MEMS devices.

Size is another important issue. Traditional manufacturing builds a MEMS structure on a tiny sliver of silicon. These are either packaged into the familiar black unit with wire connections to be mounted on a PCB or fixed beside the main chip as a bare die. Both are quite large and expensive, with no options to reduce size or costs. Furthermore, there are sensitivity and noise concerns that mean MEMS devices can be rather fragile and impacted by thermal noise. Power consumption is also a problem for some of these devices.

Modern sensors require small multiple elements to be embedded in a single package to achieve the enhanced functionality of the next-generation of smart wearables. Demand for MEMS is accelerating, but in order to keep up with the growing appetite across the globe for more complex, compact, power-efficient and robust sensors and devices, fresh developments in MEMS need to be adopted and the key barriers with traditional MEMS must be overcome.

## New developments in MEMS

There is a company that has been focused on resolving these issues with MEMS for many years. Nanusens has made a major breakthrough with a novel technology approach, creating MEMS structures using the metal layers within a CMOS (Complementary Metal-Oxide Semiconductor) chip. This means that specialized processes are no longer needed and the costs are significantly lower due to the huge economies of scale achieved when manufacturing in giant CMOS fabs.

In terms of size, there has also been a big change. Traditional MEMS structures have feature sizes of one micron or larger. However, as the Nanusens process occurs within the CMOS chip the structures are nanoscopic in size rather than microscopic. These NEMS

(Nano Electro Mechanical Systems) structures have features of 0.3 microns or less - a 100x area reduction.

A traditional MEMS sensor package has two chips, one with the MEMS structure built on it and a second with the control electronics. The package size is around 2.6mm3. In contrast, a Nanusens NEMS sensor package has it all on one chip and the size is only 0.6mm3. As a result, there is room for multiple sensors to be embedded into the chip and power requirements are much lower.

Enhanced performance is another advantage with this novel NEMS due to very small parasitic capacitances. With traditional MEMS, where the structure is placed on top of a CMOS wafer or wire bonding is involved, there is a parasitic capacitance of around a picofarad. The MEMS-in-CMOS approach offers a rather considerable signal to noise ratio improvement as this falls to around ten femtofarads or less.

A new way to measure the capacitance of the Nanusens nanosensors has also been developed using a digital circuit instead of the traditional analog method. Consequently, in order to cut power consumption and size even further, the sensor designs and digital circuit can be ported to smaller nodes without any reliability concerns.

## Technology overview

The Nanusens nano-mechanical devices are created using the metal layers in the back-end of the CMOS wafer. Some of the silicon oxide that is surrounding the layers has to be etched away, so that these can move. To do this Hydrofluoric Acid is applied to the wafer during the vapor stage (vHF) using standard equipment. The vHF etches away the silicon oxide around the metal layers through the pad opening placed above the MEMS cavity. This maskless, simple and swift process typically only takes 30 minutes and occurs after the CMOS process is completed.

Although the new approach may not seem overly complicated, it has certainly been a challenge to make this work effectively. Until now metal layers have never been used in a CMOS process to create mechanical devices as their mechanical properties are not well suited for this. In contrast to a custom MEMS process, these are thin, with large residual stress. Even more concerning, there is a large vertical stress gradient. However, with this new process comes some significant advantages, such as; submicron feature sizes and gaps, and a minimal capacitance to connect the MEMS and the ASIC, as well as a large number of structural layers that allow for creative 3D solutions.

## Technology use case – improving sensor data processing

Rather than just sending sensor data to the AI processing center, there is now another idea being considered, processing sensor data locally before sending it to the Cloud. There is good reason for this approach. There are some situations when sensors are capturing data where there is nothing for most of the time. For example, a smart microphone where there is often silence. Sending silence to the Cloud is simply wasting communication bandwidth and computing power in the Cloud. It would be much better to process this sensor data locally where the smart microphone is located. Then this will be sent to the Cloud for processing at the AI center when a person is talking or some sound needs to be analyzed.

Edge processors are digital or AI processors that are optimized to have low power consumption and are located with each other with the sensors. When sensors and edge processors are placed together the term AIoT (Artificial Intelligence of Things) is used. Nanusens can build the edge processor monolithically with the sensors into the same CMOS die, which shrinks the size and cuts power consumption. Another justification for local sensor data processing is with health monitoring devices. The processed results can be sent to the Cloud without including all the patient's details, so that the privacy of the user can be protected.

## Technology use case – finding a solution for 6G RF front end

The mobile phone industry has seen many exciting developments over the last 30 years. Innovation in this sector looks set to continue as smart mobile devices have become a critical part of most people's daily lives. There is a big buzz around the arrival of 6G, but technology bottlenecks exist that must be addressed before adoption of 6G can really take off. For example, 6G mobile phones will need to operate at a wide range of frequency bands and often at higher frequencies.

Therefore, the antenna tuning circuit found at the RF front end will have to be totally rebuilt. Currently, 5G phones use a set of distinct capacitors on a PCB. These are connected and disconnected to the antenna in real time by a separate control chip created by leveraging Silicon-On-Insulator (SOI) technology.

However, this method results in ohmic losses at higher frequencies, with the antenna efficiency falling below an acceptable level. Operating at high frequencies with high voltages would also distort the signal and 6G demands very high linearity.

With the Nanusens approach, building MEMS structures using standard CMOS can be implemented to create digitally tunable MEMS capacitors with the CMOS layers. This provides the low losses and high linearity that is required for 6G phones. These RF Digitally Tunable Capacitors (DTCs) offer a solution that meets the needs of the RF front end of 6G mobile phones.

The nanoscale capacitors are embedded into the same chip as the control circuitry to deliver a far smaller, single chip solution than the SOI approach, and with far greater levels of performance, power-efficiency and reliability. Following tests on these capacitors for 5G the results demonstrate that there is a 90% increase in talk times. For 6G, the power-efficiency at the antenna can be enhanced even more with this technology. With production taking place in giant CMOS fabs in great volumes this means that it will be possible to satisfy the huge demand for use in 6G phones.

## Potential applications

Advances in MEMS are set to be crucial for the future of sensors and mobile phones, but there are many other applications. Nanusens is developing this innovative MEMS technology for the next generation of embedded sensors such as gyroscopes, magnetometers, pressure sensors, IR imagers and gas sensors as variants on the accelerometer design. The opportunities for MEMS are vast.

# Process-reliable high purity cleaning:

## Why rinsing determines success or scrap

During rinsing, it is decided whether high-purity components reach the required cleanliness limits or whether recontamination after cleaning leads to scrap. Three factors are particularly critical: ultrapure water quality directly at the point of use (particles, organics/TOC, conductivity, pH), minimal carryover between process stages and a clearly defined rinsing strategy and plant engineering and loop hygiene: suitable materials, well-designed piping, and continuous monitoring. The following article, from BvL Oberflächentechnik GmbH, explains the background to these key levers and shows why rinsing becomes a system-critical process step in high purity component cleaning.

IN HIGH PURITY component cleaning, cleanliness requirements are more demanding than in almost any other field: permissible limits for the chemical composition of the component surface in atomic percent, extremely low outgassing rates, and particle freedom in the submicron range.

These stringent requirements result from extreme vacuum conditions in which the components are used, for example in EUV lithography, aerospace, or mass spectrometers for analytical applications. In these environments, cleanliness is not "nice to have" — it is a system characteristic.

This means the entire process chain must be designed to deliver technical cleanliness reliably and to prevent recontamination. This applies in particular to the process media: every contact medium must meet the same high limits so the specification is not compromised. Otherwise, either the required cleanliness cannot be achieved or the component is recontaminated after cleaning.

For ambient air and process air, limit values are generally manageable using cleanroom technology and HEPA/ULPA filtration. Process water, however, is often far more challenging: in rinsing, it must not introduce particles or organic residues onto the component otherwise, recontamination and scrap may occur.

### What does "rinsing" actually mean?

Rinsing is not simply "washing off" cleaner. In essence, it is the controlled dilution of the liquid film that is carried over on the component surface with rinse water. Through dilution, remaining contaminants are simultaneously removed and transported out.

Rinsing therefore becomes a mass transfer challenge: the objective is to reduce contamination concentrations from stage to stage in a defined manner below the relevant limits, both particulate and filmic/organic.

In short: a component can only become as clean as the final rinse allows.

## Key factors for high rinse quality

The decisive factors for high rinse quality are water quality at the point of use and minimal carryover.

The required water quality depends on the applicable cleanliness requirements. In many cases, ultrapure water (UPW) is used in the final rinses. Terminology is sometimes inconsistent, as standardized definitions for "ultrapure water" are not widely established across Europe.

Water quality is influenced by the quality of municipal feed water. Depending on hardness, conductivity and dissolved salts, pretreatment may be necessary, for example through activated carbon filtration, particle filtration, manganese removal, or iron removal.

Typically, reverse osmosis is then used: pressure forces water through a semipermeable membrane, separating low-salt permeate from concentrate.

For the highest demands, further treatment often follows via mixed-bed ion exchange or alternatively electrodeionization (EDI), which operates continuously without regeneration chemicals. Depending on requirements, additional stages such as UV treatment for microbial reduction or degassing may be added.

Ultimately, water quality is defined and monitored using parameters such as conductivity, pH, and TOC (total organic carbon).

Modern water treatment can deliver excellent values at the outlet of the treatment system. The crucial factor, however, is maintaining that quality at the point of use, i.e., in the tank or chamber of the cleaning system itself.

## Plant engineering as the enabler: materials, carryover control, loop hygiene

This is where sophisticated plant engineering is required: it must ensure excellent water quality at the point of use through minimal carryover, appropriate materials, and where necessary effective loop hygiene. Because rinse quality is only as good as the system that carries it.

From the outset, the cleaning system must be designed to minimize carryover. This includes strict separation of media circuits: each tank has its own piping, its own filter units, and its own pump. Piping runs should be flow-optimized to prevent residual water from collecting anywhere.

Workpiece carriers and racks are frequently underestimated. Following the "form follows function" principle, they must be designed to avoid scooping points and unnecessary surface areas where water residues can remain.

Depending on the system type, additional features apply: in transfer immersion systems, defined overflows and separation baffles between tanks are important. Drip times and vibration of carriers support carryover prevention.

In chamber systems, a drain-optimized chamber design, complete draining, and chamber cleaning between treatment steps are beneficial.

In addition, water quality should be monitored directly in the cleaning system, at the point of use, using appropriate sensor technology.

Selecting suitable materials and surfaces is also essential. Due to improved compatibility, V4A stainless steels (e.g., 1.4404, 1.4571) should be used instead of V2A; weld quality must be ensured. Brass should be avoided entirely. PP and PVDF may also be suitable for piping, depending on the application.

## Practical example: Designing cleaning systems for high purity rinsing processes

As an example of practical implementation, BvL Oberflächentechnik GmbH refers to cleaning systems that can be designed for high rinse quality at the point of use — among other things through separate media circuits, suitable materials, and in-process monitoring of water quality.

As examples, the NiagaraUP chamber cleaning system and the AtlanticTR immersion cleaning system are referenced.

Test cleanings are possible in the company's Technology Center. A UPW treatment system (EnviroFALK) is also available for tests (key values: conductivity 0.04 µS/cm; TOC 13.58 ppb).

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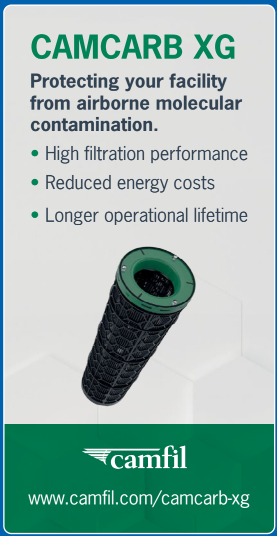
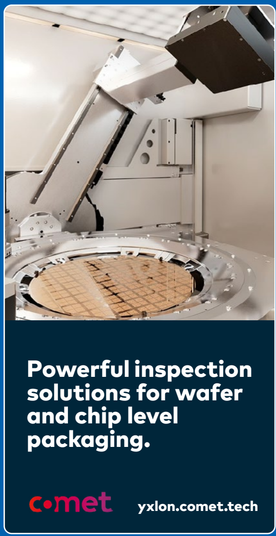
## CLEAN AIR




## INSPECTION SYSTEMS

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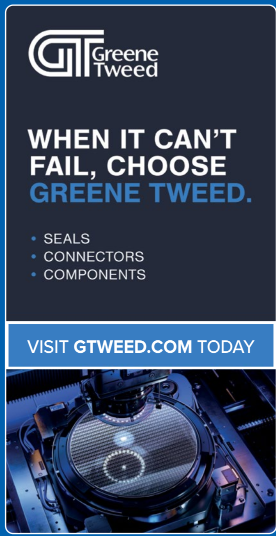
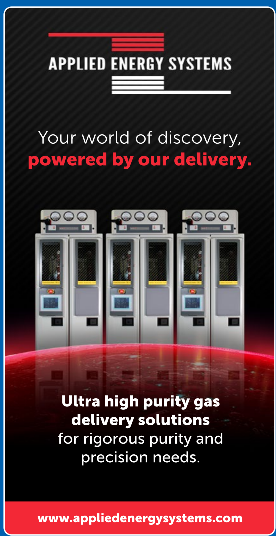



## ETCH


## FLUID SYSTEMS

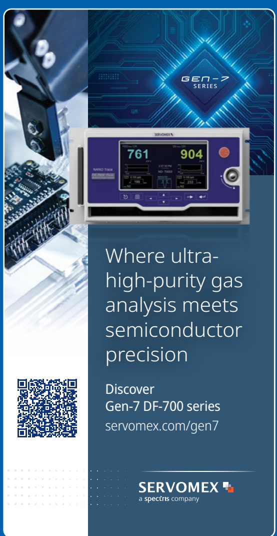

## GAS DELIVERY SYSTEMS




## GAS PURIFIERS


## HYDROGEN GENERATORS


## GAS ANALYSERS




## PLASMA TECHNOLOGY


## TEST


## VACUUM EQUIPMENT