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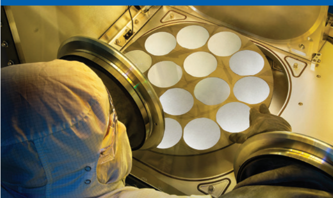
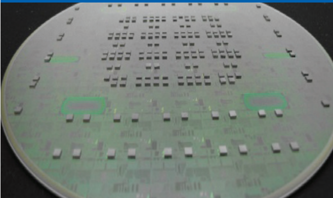
Sensor searches demanding application

Modifying wet process cleaning equipment

VEECO targets new VCSEL requirements



Photonic technologies are converging



MediaTek unveils 5G SoC for flagship devices

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Fingerprinting analysis on electronic materials

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editor's view

By Mark Andrews, Technical Editor

Is 2019 a year for 'conservative optimism'?

A CHERISHED former professor used to tell new undergrads that he was 'conservatively optimistic' his eager-eyed students would succeed and prosper in a world undergoing radical change. Fast-forward four decades and the world is *still* undergoing radical change. As semiconductor manufacturers, we embrace radically different ideas and change—so long as we can manage that change while pocketing a tidy dollar, pound or euro.

As we speed towards SEMICON West we hope that our ideas and determination will change this industry for the better even as 'changeability' summarizes today's economic headlines more often than not.

In mid-June 2019, the SEMI trade group announced that first quarter worldwide equipment billings were down 19 percent. Not a perfect opening act for SEMICON West in July. But worry not—the very next day SEMI announced that global fab equipment spending will rebound in 2020, growing 20 percent.

While the perennially upbeat trade group might be lauded for finding a silver lining amidst 2019's ups and downs, SEMI in its own way addresses what industry veterans know all too well: this is not the business for someone who can't tolerate change.

While trade disputes, tariffs and sliding memory chip sales (with a projected 2020 recovery,) continue to make headlines, industry vitality continues to amaze. Researchers at Yole Developpement reported early in June that long-standing MEMS leaders, Broadcom and Robert Bosch, continue to push sales ever higher. MEMS sales blew past (USD) $10 billion for the top 30 manufacturers, achieving nearly 5 percent annualized growth. For automotive chip makers, merger and acquisition (M&A) activity grabbed headlines, with IHS Markit reporting that Infineon's $10 billion bid to acquire Cypress Semiconductors would likely push the auto chip maker into the number-one spot, unseating previous leader NXP.

In this edition of Silicon Semiconductor, the experts at Linde share details about the lengths they pursue to insure that electronic materials—the building blocks of IC structures—have ever-increasing levels of purity and quality to fight defects. Researchers at imec provide insights into two advances: a newly-released innovation to bring Raman spectroscopy to chip-level devices and an optically-based sensor that is resistant to EM interference. VEECO instruments describes ways that it is supporting next generation VCSEL development while Edwards describes its innovative approach to reducing sub-fab downtime based on service records from 100 EUV systems world-wide. Enjoy this edition and meet us at SEMICON West in San Francisco, 9-11 July.

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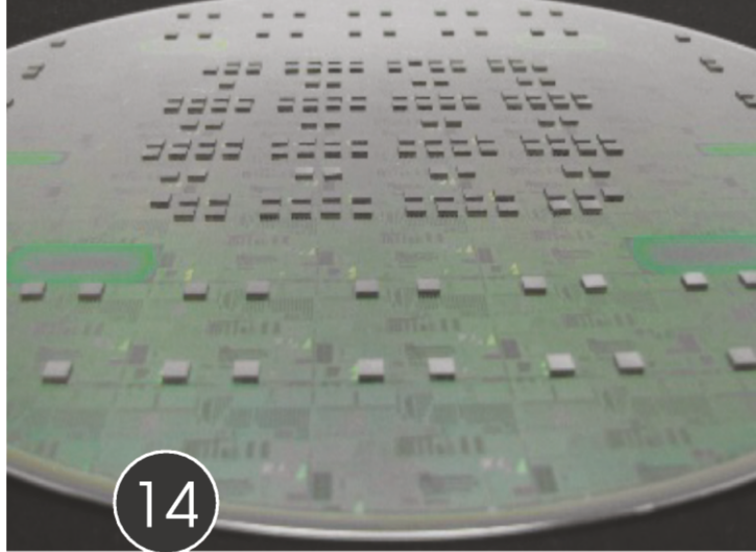

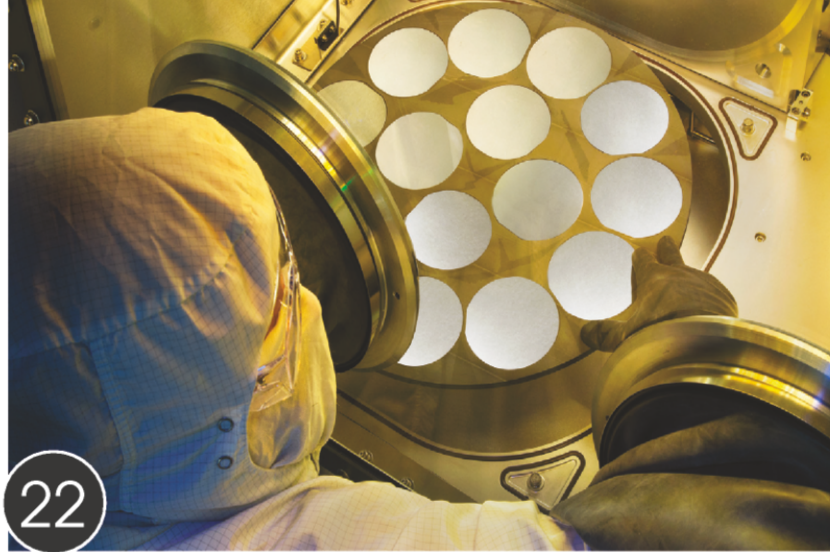

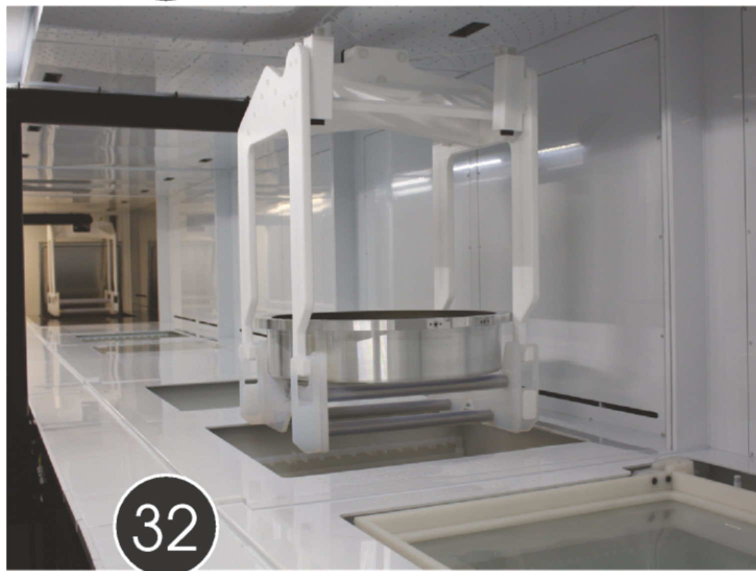

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Fingerprinting analysis on electronic materials

Using all the evidence to advance semiconductor manufacturing

As semiconductor device geometries continue to shrink, electronic materials are increasingly critical to reducing defects while ensuring high yields. The experts at Linde describe the extraordinary lengths they pursue to ensure purity, quality and consistency.

By Carl Jackson, Head of Electronics R&D, Linde

"YOU CAN'T MANAGE what you can't measure" is an often-quoted business mantra developed in the 1950s by the prominent operational management thinkers of the time, the same era as the start of the semiconductor age. Peter Drucker was one of the key proponents of this new approach referring to the increasing need for objective data to improve business processes. In semiconductor manufacturing, this approach has been taken to the extreme, allowing the industry to shrink transistors one million-fold in size through a cycle of measurement, innovation, and refinement. But in the current age of exponential data growth, knowing which data are important and how to combine different data sources to get the necessary information for decisions is critical.

In this article, we describe how we at Linde have taken an advanced, holistic approach to chemical metrology for electronics materials which we call *fingerprinting*. As the quality gatekeepers between industrial chemical sources and zero-defect atomic-scale manufacturing, we demonstrate the application of these advanced methods throughout the electronic materials supply chain with real production examples.

Electronics materials: semiconductor building blocks sourced from the chemical industry

Electronic materials are the molecular building blocks used for semiconductor manufacturing. These materials are critical to all semiconductor manufacturing processes (Figure 1, refer to page 8), and are often cited by leading-edge companies and OEMs as one of the key enablers to drive future innovation. Many of the materials in use today – such as silane, ammonia, and hydrochloric acid – have been used since the start of the semiconductor industry, and the purity requirement for these materials has tightened as transistor sizes have shrunk. There are also many new materials like gallium and antimony sources being quickly developed and introduced in response to the increasing challenges of our customers to make electronics devices faster, lower-power or lower-cost. Before any new material can be introduced into manufacturing, metrology must be developed for its entire supply chain.

Almost all these materials originate from industrial or mined sources instead of being specifically synthesized for use in electronics. This supply is driven by the cost advantage of manufacturing

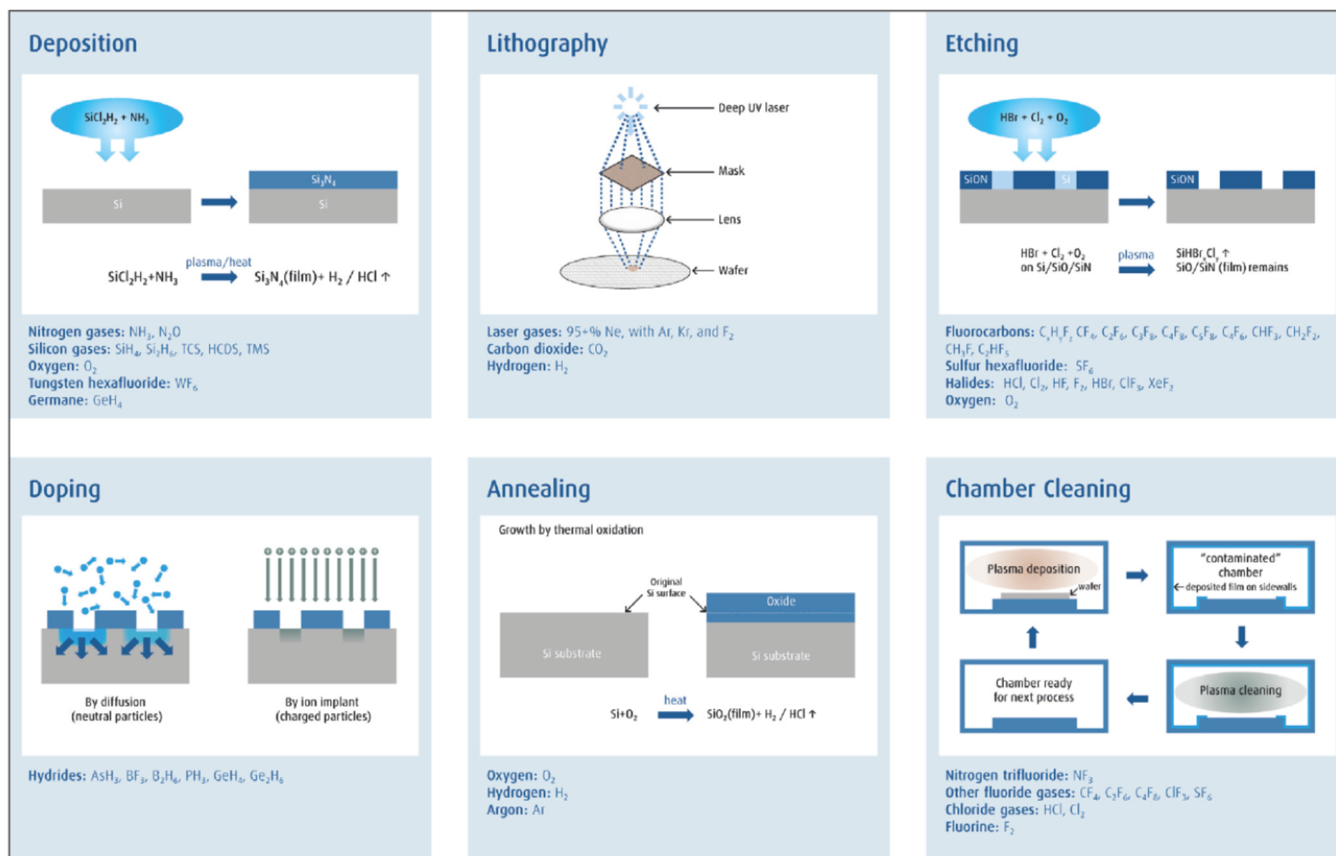


Figure 1: A wide portfolio of electronic materials are used in every major semiconductor process.

scale. As seen in Figure 2 (refer to page 9), the industrial supply for common materials dwarfs the electronics demand. However, there is a large quality gap between most industrial applications and semiconductor manufacturing. The challenge for electronic material suppliers is identifying stable sources, working with suppliers to understand our sector's control requirements, and purifying and packaging the materials for use in electronics fabs. Underwriting this supply chain are analytical measurements at each step.

Chemical analysis is the lead metric for ensuring semiconductor-grade quality materials

Long before Peter Drucker's contributions to business management, nineteenth century scientist Lord Kelvin expounded "to measure is to know." Chemical analysis and chemical science have developed together, one enabling the other. Early analytical techniques for electronic materials focused on a few impurities from ambient contamination, namely moisture, oxygen, and particles. These are normally measured by analyzers designed to measure a single impurity.

As process flows became more complex, measurement of a greater number of impurities was essential to characterize and control electronic materials. Spectral techniques which can identify and measure many different species are now typically used. The three most important of these techniques are introduced in Figure 3 (refer to page 10), along with examples of their methods for fingerprinting distinguising between two simple and similar impurities.

In all electronic materials, many different impurities may be simultaneously present, with most in very minute amounts, even by our industry's standards. Typically, a subset of the most prevalent or impactful impurities are measured as metrics for both upstream supply chain control and downstream process control. These constitute an agreed specification for the material, and each package or batch of materials is shipped with a list of these measurements called a certificate of analysis, or CoA.

Recently, electronic material suppliers have worked cooperatively with leading-edge device manufacturers to enhance the feedback loop for quality control. *Ship-to-control* describes the improvement quality feedback loop in which the statistical variation of product impurities and other metrics are continuously evaluated and improved, resulting in quality beyond the CoA specification and a higher-value material product.

Fingerprinting: compiling the data

Fingerprinting is a broad-spectrum chemical analysis which utilizes a collection of instrumentation and analytical techniques to provide a complete characterization or fingerprint of a material. It is not limited to impurities specified on the CoA or even

known impurities. Rather, it utilizes spectral techniques like FTIR (Fourier-transform infrared spectroscopy), GC (gas chromatography) and MS (mass spectrometry) which can simultaneously detect a wide range of impurities, in combination with other measurements, to make a comprehensive profile for a material.

Fingerprinting is particularly powerful for impurities which may be detected, but not fully identified or characterized. This is becoming more common as complex molecules are introduced into semiconductor manufacturing, and these complex materials have similarly complex impurities. These impurities may not even be stable outside the matrix of the bulk material, and standards may not be available to calibrate their concentration. Using fingerprinting we can detect the relative changes in the overall composition of a material from different sources, through different points in our manufacturing process, or over time. It allows us to control for multiple variables at the same time, and over all of the points in our supply chain. Fully realized, fingerprinting enables the continuous improvement goal of ship-to-control.

We have been using this approach for many years to help with root-cause analysis when there has been a quality excursion. This has required a bespoke, project-by-project approach where a complex assortment of metrology equipment is required along with the development of new analysis methods. The recent step-change in our approach is twofold. First, we have established an electronic materials laboratory in Taiwan with capabilities to more efficiently apply fingerprinting on the more than 50 products in our portfolio. The second, more profound change, is that we are now applying the same metrology capabilities not only for complex problem diagnosis, but also for each step in the manufacturing value chain.

- **Raw material characterization:** We can identify and qualify preferred sources of raw materials during our development phases, and we can monitor the quality control of our suppliers with techniques much more powerful than those at the supplier.
- **Purification:** Chemical analysis guides the development of our purification technologies, and ensures that production lines remain in control and improve over time.
- **Analysis:** Just as we develop our own purification processes, we also must develop our own analytical methods. Fingerprinting guides us to look at the challenge from many different angles. For production, we can assure our customers that the CoA specification is indicative of our control over the entire profile of the product.
- **Packaging, logistics and shelf life:** Our responsibility for quality doesn't end with production, but extends to product stewardship through the packaging, transport, and lifetime of our products.

Linde analytical chemists discuss results

Case studies: using data to add value to our materials

Case Study #1: Complex fluorocarbon materials make for challenging sourcing, purification and analysis

Fluorocarbons have long been used as etch materials in electronics manufacturing. When activated by a plasma in an etching tool, chemically active fluoride ions and radicals are produced, which react with many deposition materials to form volatile products which in turn are removed by vacuum pumping. Initially, simpler, more common materials like CF_4 and C_2F_6 were the primary etchants used. Now, more complex materials like C_4F_6, C_4F_8, and C_5F_8 are used to achieve a greater selectivity for preferentially removing one material while leaving a desired second material in place.

The greater complexity of these fluorocarbon materials also means the sources have many more potential impurities, and the purification and analysis become

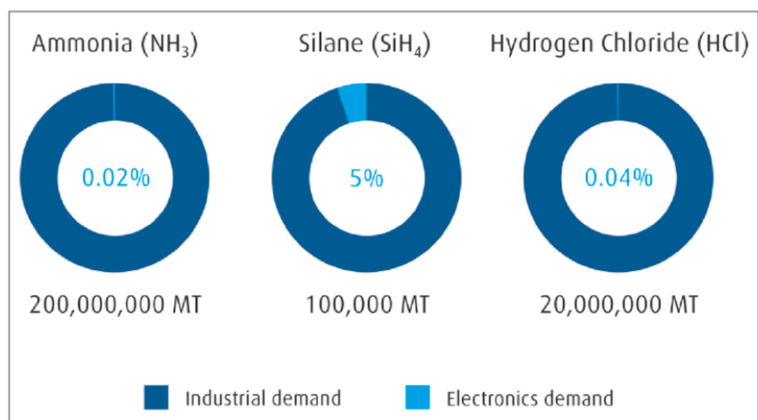


Figure 2: Global electronic material demand is a small fraction of industrial production.

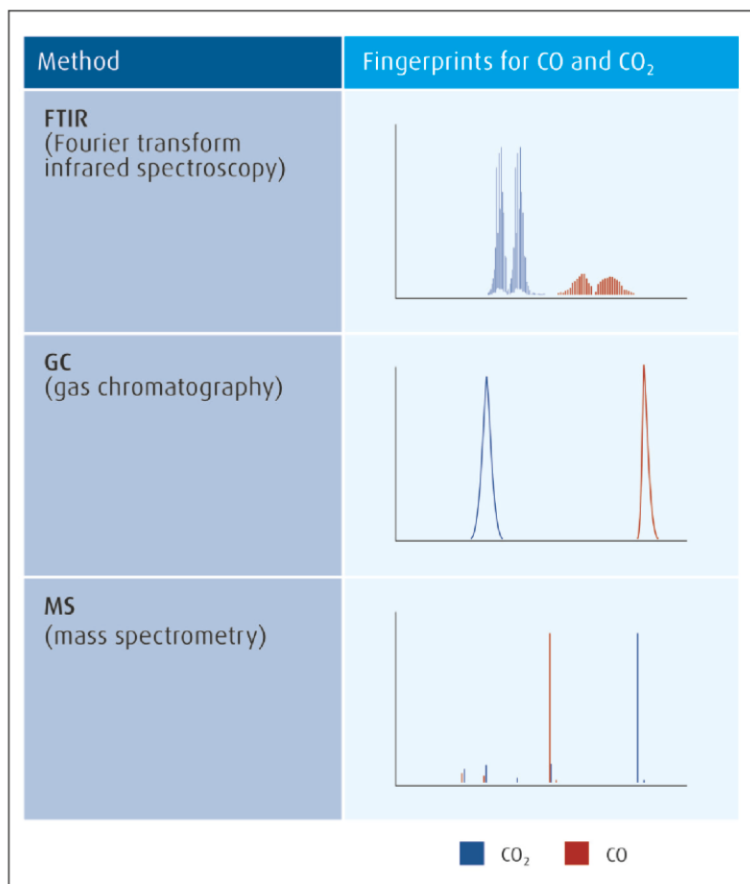


Figure 3: The three most common spectral methods for electronic material analysis, with examples of their fingerprints for carbon monoxide (CO) from carbon dioxide (CO_2).

more challenging. Figure 4 (refer to page 11) is indicative of the fingerprint of a potential source material for our process, where we have used a combination of GC and MS techniques to separate and identify the many impurities present. We used fingerprinting to choose and qualify material sources; develop our proprietary purification technology; and to further develop advanced hybrid analytical techniques to ensure ship-to-control quality.

● Case Study #2: Carbon monoxide – a simple molecule with extremely low but impactful metal impurities

Carbon monoxide (CO) is also used in etch processes, and is added to further modify the selectivity. The challenge for supplying CO is its reactivity with many common metals, like iron and nickel, to form gas-phase metal-containing compounds called metal carbonyls. Because they are volatile molecules, metal carbonyls can travel unimpeded through particle filters.

Leading-edge processes are extremely sensitive to metallic impurities, and now have a specification of less than 100 parts per trillion (ppt) for both nickel carbonyl and iron carbonyl species. Current detection limits of commercially available analytical instruments do not allow for measurements of carbonyls at the ppt level, and furthermore, the sampling system and analysis instrument itself can react with carbon monoxide to produce carbonyl levels that are higher than in the material being analyzed.

For this reason, we limit our analysis system to non-carbonyl generating wetted materials, which can preferentially capture and concentrate the metal carbonyls. In addition, we have developed state-of-the-art compound methods with both high resolution and high sensitivity to achieve detection and measurement of these species to the low ppt range.

● Case Study #3: Silane and the case of the hidden impurities

Silane is the most basic precursor for the deposition of silicon-containing thin films, and has been used for many decades as a workhorse in electronics manufacturing, not only for semiconductors, but also for display and photovoltaic panels. However, even with well-characterized sources and processes, new challenges can arise.

In addition to developing technologies to look at impurity levels that are below current industry practice such as the CO example above, we also have been addressing challenges where the use of standard industry metrology techniques would effectively hide an unknown impurity – a phenomena called *matrix interference*. Using a variety of analytical techniques with unique overlapping capabilities to look at a wide array of analytes ensures that something hidden by matrix interferences isn't missed. In the case of silane, GC is the principle analytical technique employed to look for impurities.

However, since some light hydrocarbons have a similar boiling point and vapor pressure curve to silane, they are hard to separate during the purification process. Unfortunately, this also means they are difficult to separate in the GC analysis. In this case, product shipped to our photovoltaic customer met all agreed specifications, but due to an undetected hydrocarbon contamination, the process performance on the customer tool was resulting in a lower panel power output. In response to this issue, we developed

"Just as we develop our own purification processes, we also must develop our own analytical methods. Fingerprinting guides us to look at the challenge from many different angles. For production, we can assure our customers that the CoA specification is indicative of our control over the entire profile of the product"

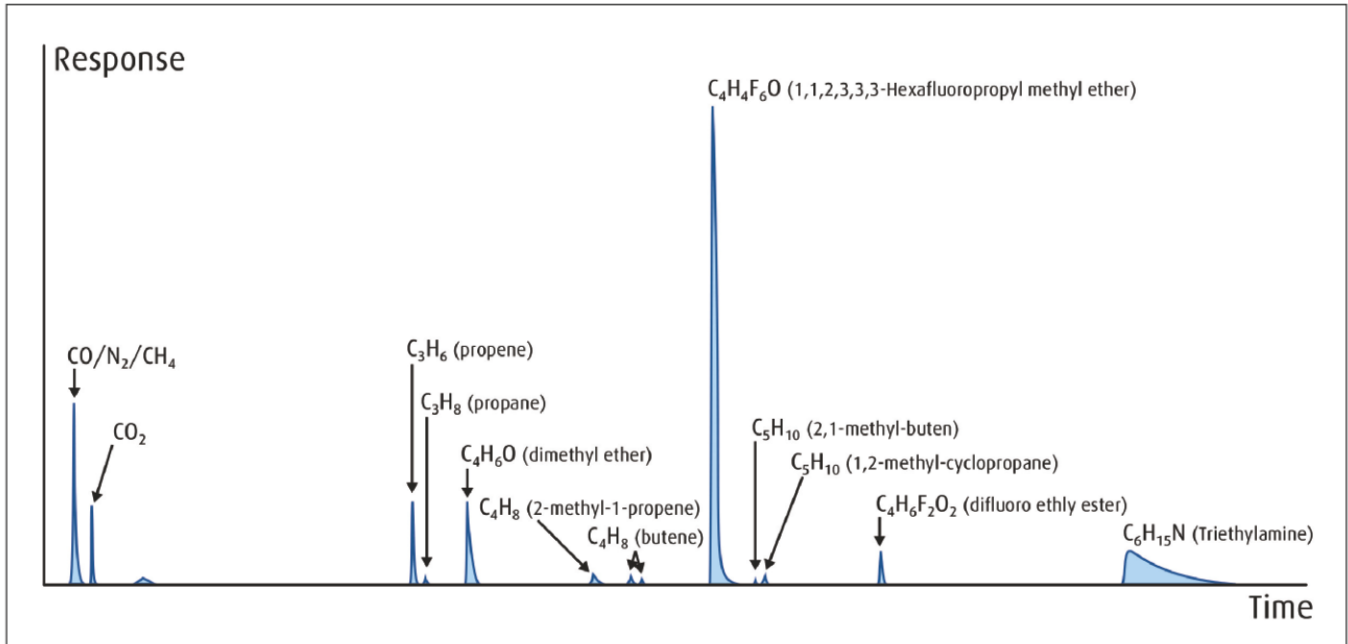


Figure 4: Candidate raw material source for advanced fluorocarbons with a complex mixture of impurities identified by combining GC and MS methods.

a complementary FTIR method for analyzing silane where we could look at the material from a different perspective.

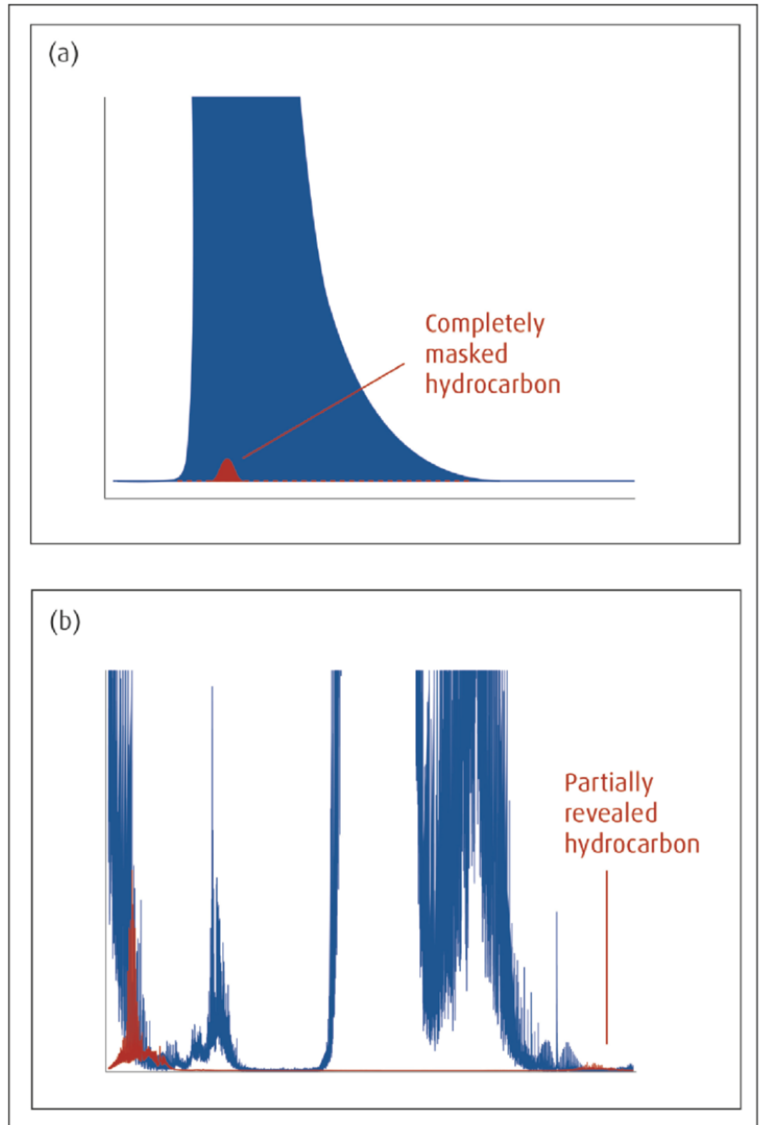
This allowed us to integrate these new measurements with the original GC results and detect the very low levels of hydrocarbon bad actor, which we then subsequently upgraded our purification systems to remove. See Figure 5 (refer to page 12) for an example of how we were able to identify one of these contaminants.

Case Study #4: Diborane analysis showcases quality control for shipping and storage

Diborane (B_2H_6) is used both as a source of boron for silicon doping as well as to modify tungsten deposition processes. There are a number of materials used that have the potential to change their

Inside view of Linde Electronics R&D Center analytical laboratory

Right: Figure 5: (a) Principle GC production method – 100 ppm hydrocarbon fingerprint (red) is completely masked by pure silane (blue). (b) Complementary FTIR method – hydrocarbon fingerprint is partially revealed. We were able to match this partial fingerprint to a reference fingerprint for ethane and measure it at 100 ppm.



composition and purity during shipping and storage. Diborane is one such product that is a critical material for our customers, however can be unstable if not handled correctly, especially if the diborane packages are exposed to high temperatures during transport or storage. The impurities which can be formed are a result of its reaction with itself to form larger compounds called *higher boranes,* which have more boron and hydrogen atoms. These higher boranes can cause significant customer process issues. Unfortunately, they are very difficult to measure using current state-of-the-art analytical technologies. Adding to the challenge, there are no chemical standards for higher boranes.

Working with our customers, we have developed technology to allow us to look directly at part per million (ppm) levels of higher boranes. The traditional approaches with FTIR, GC-FID and GCMS didn't detect any of the higher boranes that we specifically engineered into the product to simulate a production problem. Instead, we first separated and identified higher boranes in our engineered material using a very advanced combination GC-ICP-MS technique. This technique is powerful, and uses the same inductively coupled plasma technology used in semiconductor deposition and etch processes, but is not always the most consistent and reliable for electronic material production. We then cross-correlated the first results with a more production-robust pure GC technique.

Conclusion: continue to measure and improve

Measure, know, improve. The insights from Lord Kelvin and Drucker continue to guide us and drive us to improve in order to enable our customers' innovation roadmaps. For the supply of electronics materials, we must bridge a constantly widening gap between industrial raw material sources and ultra-precision atomic level manufacturing. Chemical analysis is our strongest tool to know our products and our processes, and we continuously improve both.

Linde has pioneered the practice of fingerprinting electronic materials. We understand that material development is a critical enabler for our leading customers. By investing and leveraging our world-class analytical production and development facilities in Asia and the US, Linde has focused on high-impact materials for the industry. We continue to invest, develop, and enable technology for the future.

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Photonic technologies are converging into a CMOS compatible silicon photonic platform

Silicon photonics technology has definitely reached a first level of maturity, as it can be found nowadays in commercial products for intra- and inter-datacenters communications at high data rates. Higher volume markets such as intra-rack communications could be addressed by solving three main challenges: the packaging, the energy consumption, and the laser integration.

By Karim HASSAN, PhD, Researcher and Project Manager at CEA-Leti

THE CONVERGENCE of photonic technologies into a CMOS compatible silicon photonic platform remains a key challenge while several fabrication supply chains and industrial products are available in the field of high speed communications on optical fiber. Nowadays, the circuit design tools are available on several software platforms. However, silicon photonics is still suffering from the lack of integrated light sources. Existing packaging solutions offer a straightforward way to combine III-V laser sources and silicon photonics integrated circuits in order to address the market today, at the expense of a high cost and low volume production. On the other hand, the hybridization of III-V gain material (which remains the materials of choice to achieve semiconductor laser sources) can be realized using III-V direct bonding on top of patterned silicon. Subsequent laser demonstrations relying on CMOS-compatible process for the silicon part have been in most cases followed by process steps carried out with small wafer III-V fabrication lines (typically below 4-inch wafers). With such integrations, the cost advantage of silicon photonics based on the use of CMOS platforms and large wafer format is not valid.

The issues regarding the integration of III-V material go beyond the introduction of the material itself on CMOS lines. In fact, fundamental aspects such as having a low access resistance with CMOS back-end of line (BEOL) metals onto III-V compounds is not straightforward since noble metals, e.g. gold, cannot be used. The thin SOI (<310nm) used for getting single mode silicon photonic integrated circuits (PICs) makes optical coupling with the thick III-V gain material (>2μm) difficult. It is worth noting that the topology of III-V components, having a large height of about 3μm, makes the co-integration within the BEOL of active silicon devices interconnects incompatible.

Furthermore, while large format of III-V wafer epitaxy is still in progress, most of the III-V suppliers can provide laser stack onto wafers smaller than 4 inch, which makes the use of dies rather than wafer mandatory for the hybridization on 200mm silicon wafer (as well as 300mm).

Nevertheless, the use of III-V dies generates additional difficulties for III-V processing due to undesired lateral etching of the dies during the III-V substrate removal. An overall integration strategy must be developed in order to solve these technological barriers.

Successful laser integration on fully CMOS-compatible silicon photonics platform

In order to break the existing technological limitations for mass production of hybrid PICs, CEA-Leti's R&D fabrication platform has developed a first laser integration on a 200mm fully CMOS-compatible silicon photonics platform, as depicted in the Figure 1.
The fabrication process can be divided into three main parts, with first the silicon patterning followed

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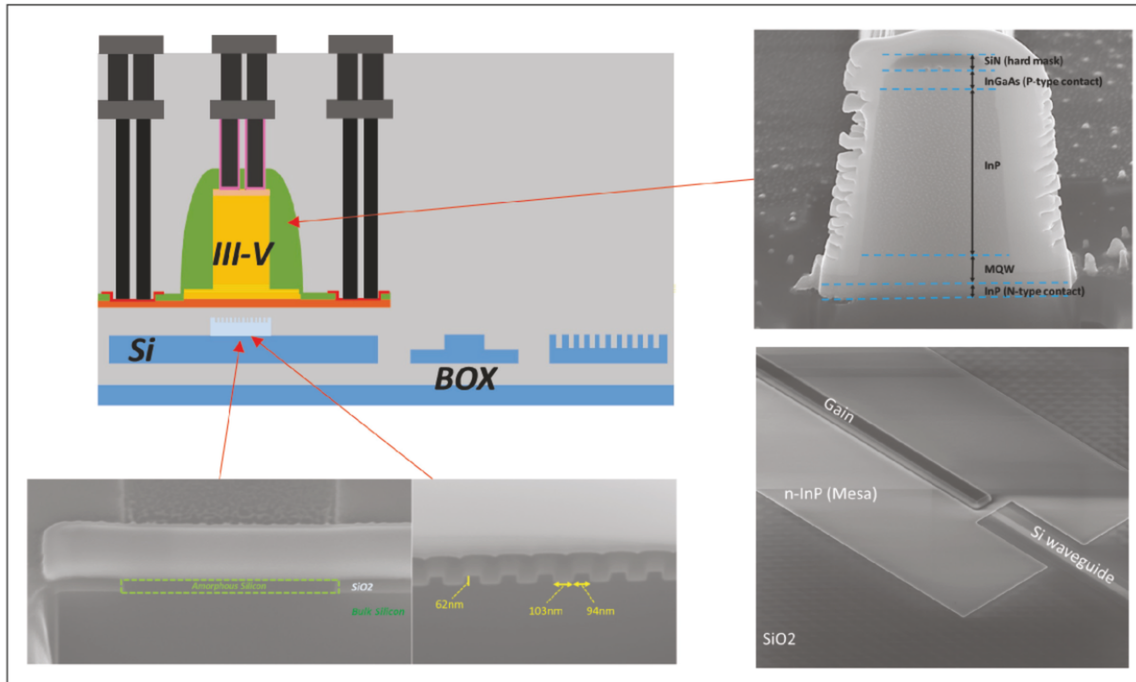

Figure 1. Schematic view and scanning electron microscopy images of III-V on silicon laser fabricated on 200mm CMOS lines.

by the III-V hybridization through molecular bonding, prior to the III-V patterning (including the CMOS metallizations). The optical coupling between III-V and silicon requires thick silicon waveguides, which is obtained by a localized thickening with amorphous silicon, as shown in Figure 1. Next, a chemical and mechanical planarization (CMP) is used to provide a smooth oxide layer for the direct bonding of III-V on silicon. The novel patterning of the III-V material that has been developed relies entirely on the 200mm platform. The new process flow proposed by CEA-Leti uses selective reactive ion etching (RIE) steps on both p-InP and p-InGaAsP.

New BEOL for lasers

Such a new patterning sequence allows us to encapsulate the III-V completely prior to the BEOL, which will remain planar, similar to standard silicon photonics components. Consequently, a high density of vias can be patterned on the SiO_2 encapsulation and subsequently filled with tungsten on top of both contact sides made of Ti metallization deposited by magnetron sputtering (PVD), prior to the final AlCu micron-thick pad layer, as depicted in Figure 2.

This new CMOS BEOL for lasers, developed within the framework of the IRT Nanoelec Photonic Program, a French consortium involving CEA-Leti, ST Microelectronics, ALMAE, CNRS-LTM, and Mentor Graphics, results in a state-of-the-art serial resistance on hybrid lasers ranging from 3 Ohms to 4 Ohms.

Large scale automated testing

Large scale automated testing is also of great interest when arguing about large volume production of hybrid PICs. Thanks to the novel 200mm process, full wafers can be thoroughly mapped with electro-optical fiber-to-fiber measurements. Such a test is made possible by the use of fiber grating couplers fabricated onto the silicon, similarly to standard silicon PICs. Most of the developments required specifically for the tests of hybrid lasers relies on the spectral (CW and pulsed) and thermal characteristics. Even though silicon devices are also sensitive to temperature variations, the behavior of hybrid lasers regarding thermal fluctuation and the aging of such object is vital to ensure the operability on datacenter environments.

There are still some challenges in this regard to provide high temperature tests before the packaging, with, for instance, the improvement of optical fiber position and vibrations due to convection over the wafer and dilation of it. The development of on-wafer laser testing is not only relevant for the monitoring of the fabrication yield, but also for sorting out the hybrid photonics chips as a function of their performances before packaging.

Efficient die bonding

Beyond the performances and efficiency, the cost of hybrid III-V/Si transceivers is of great interest. While mass production of silicon chips is cheap, the addition of III-V materials can increase significantly the budget per PIC. One can note that the consumption of III-V material must be minimized in order to reduce the environmental impact (by the material itself or the chemicals used for waste treatment). Figure 3 shows 3 mm x 3 mm III-V dies on top of a 200mm SOI wafer (including silicon photonics circuits for high lasers) after the molecular bonding. The newly developed 200mm die bonding reached a yield ranging from 70 to 99%, with 90% of the successfully die transferred having 99% of III-V material bonded onto the SOI surface. While the molecular bonding itself can

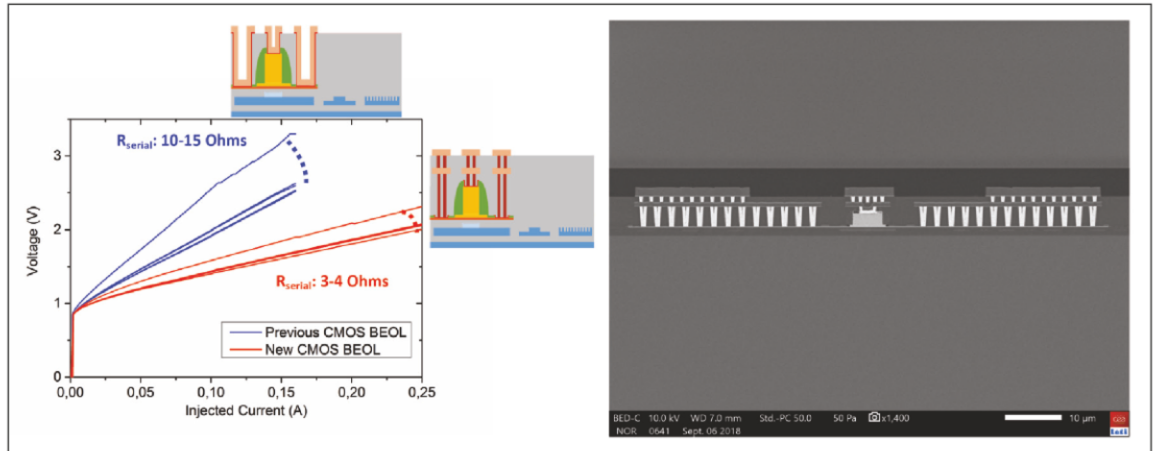

Figure 2. Experimental IV curves on 200mm CMOS hybrid lasers with 1 and 2 levels of BEOL and scanning electron microscope view of the cross-section of such laser developed on CEA-Leti's R&D fabrication platform.

be executed the same way as wafer bonding, the substrate removal is more critical for dies due to undesired lateral etching.

The thinning was ensured by first an original sequence of grinding operation down to 50μm III-V remaining prior to a chemical wet etching used to remove the remaining part of the substrate. By adding a grinding step before the wet etching, the lateral consumption of III-V during the substrate removal was reduced by a factor between 3 and 5. The III-V patterning on those dies is now in progress to realize hybrid lasers.

Conclusions

Recent developments led by CEA-Leti within IRT Nanoelec have led to a full CMOS friendly laser integration process, exhibiting very low serial resistance thanks to novel contacts metallurgy. In addition, wafer scale approaches allows high yield bonding of reduced area III-V coupons/dies onto SOI wafers, drastically reducing the cost of next generation photonic transmitters. The scalability towards 300mm for both CMOS contacts and die bonding is currently under development, paving the way for the adoption of silicon photonic technology in a variety of emerging applications such as system in a package photonic transceivers, high performance computing and PIC based LiDARs.

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About CEA-Leti (France)

CEA Tech is the technology research branch of the French Alternative Energies and Atomic Energy Commission (CEA), a key player in innovative R&D, defence & security, nuclear energy, technological research for industry and fundamental science. CEA was named by Thomson Reuters as the second most innovative research organization in the world in 2017. CEA Tech leverages a unique innovation-driven culture and unrivalled expertise to develop and disseminate new technologies for industry, helping to create high-end products and provide a competitive edge.

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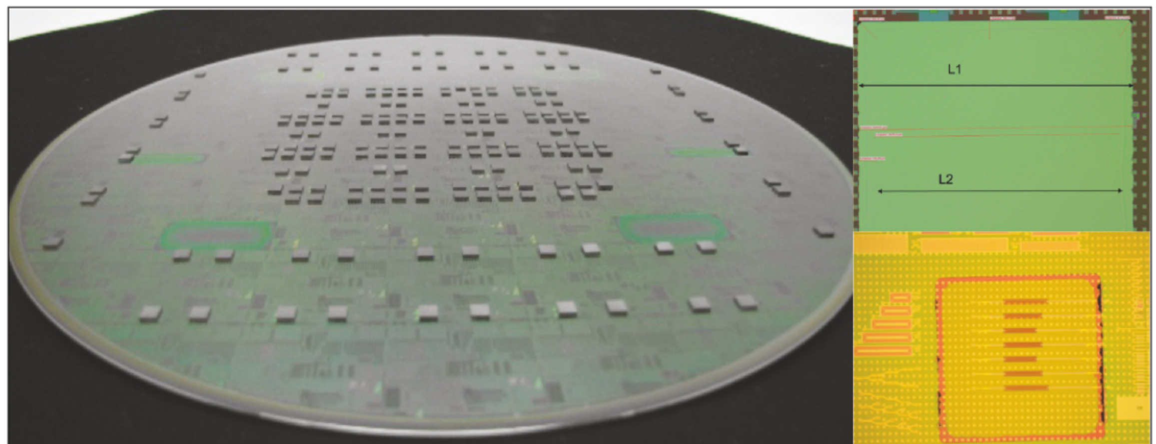

Figure 3. III-V dies on 200mm silicon wafer, and microscope images of such die after the III-V substrate removal and during the 200mm CMOS process of hybrid lasers.

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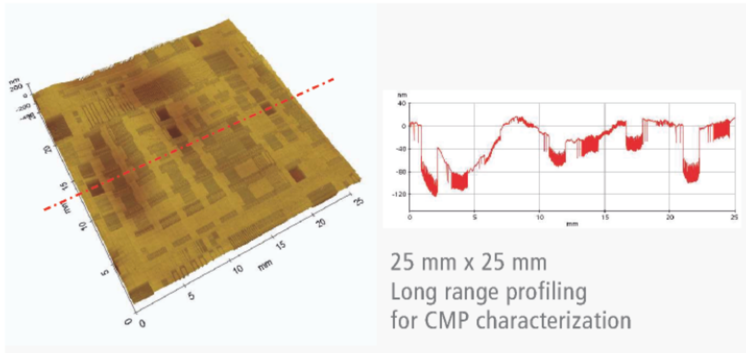

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Data-driven continuous improvement in the sub-fab is critical for HVM EUV lithography

As EUV lithography moves into high-volume production, having a sophisticated, systematic approach to track and prevent downtime translates into money saved, directly impacting the bottom line. Edwards explains how a data driven approach can pay for itself many times over.

By Nicolai Tallo, Product Manager, Edwards

EXTREME ULTRAVIOLET (EUV) lithography is poised to enter high-volume manufacturing (HVM) in 2019 at several fabs. With total EUV investments expected to be measured in the high $100Ms dollars, the capital investment alone warrants extraordinary efforts to ensure maximum availability. The cost of downtime is further multiplied by the "bottleneck" role lithography plays in the overall process, such that EUV downtime will unavoidably cause significant production losses. Sub-fab support systems, such as those providing process vacuum and abatement, are mission-critical components in EUV lithography. Failures there carry the same costs for availability and production losses as failure in the EUV system itself. Maximizing availability requires a data-driven program that identifies potential failure modes and allocates resources to mitigate consequences, with priority given to the most likely and most costly causes. Having the right spare parts on hand when they are needed is one critical component of system availability. An examination of a data-driven approach to managing spare parts inventories for EUV sub-fab systems will clearly show the methodology employed and its potential value in maximizing availability and minimizing production losses.

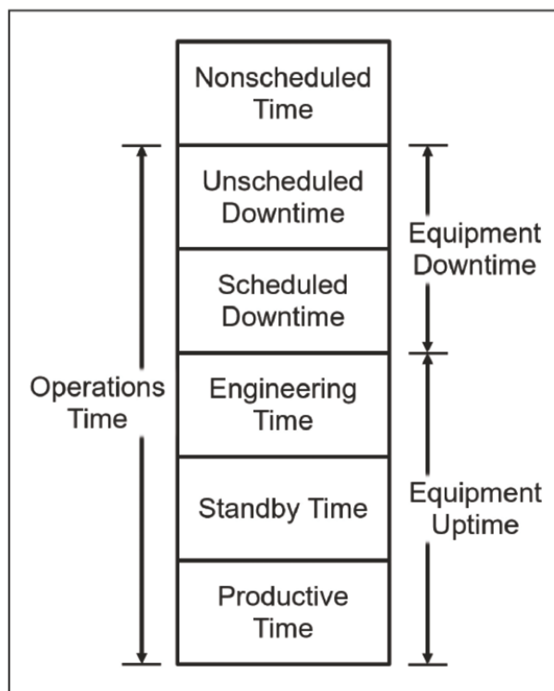

Figure 1: SEMI E-10 defines the various classes of time used to compute system availability.

A data-driven approach requires, above all, consistent, standards-based data and lots of it. Over the last 10 years Edwards has acquired data from more than 100 EUV vacuum systems, comprising, as of this writing, 100 percent of current EUV installations. Consistency within the data is ensured by the strict application of the SEMI E-10 standard as a basis for calculating availability. The data, based on global availability reporting across the installed base, are used to define, refine and update an availability matrix, which, in turn, is used to prioritize and pre-position spare parts inventory, identify common root causes of failure, and direct efforts in continuous improvement.

Calculating availability – SEMI E-10

Figure 1 is a schematic representation of the time states defined by SEMI E-10. Availability is Equipment Uptime as a percentage of Operations Time. Time spent waiting for spare parts is a maintenance delay

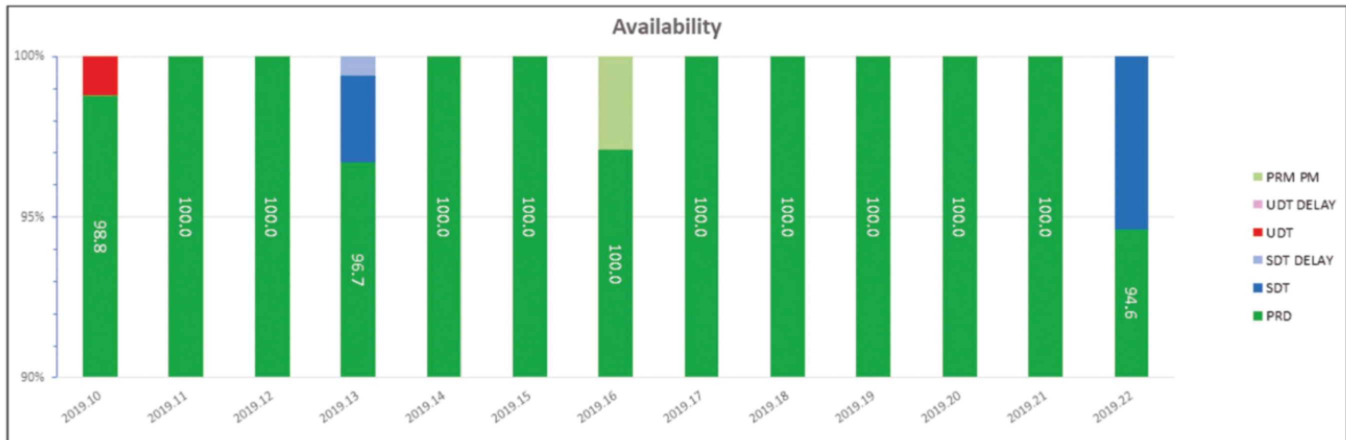

Figure 2: Standards-based reporting of system availability provides actionable data for a program of reporting and continuous improvement.

and is included in either scheduled or unscheduled downtime. Figure 2 shows what a weekly availability report for a system might look like. Reporting in this manner allows for effective fleet management by identification of critical issues and the respective parts and resolution required.

The availability matrix

The development and use of an availability matrix is a key enabler to the application of a "just-in-time" (JIT) philosophy to spare parts inventory management. It is a process of continuous improvement that seeks to minimize customer risk with global knowledge, locally applied. Figure 3 illustrates the ongoing improvement cycle.

Underlying a summary report like the one in Figure 2 is a detailed matrix of every activity affecting system availability (Figure 4). In addition to a description of the activity the matrix includes information about the frequency of occurrence, a holistic approach to the different ways time (to the minute) is spent in making the repair, and the impact of the repair on availability. This level of detail is a necessary component for calculating the overall tool availability and allows for prioritisation based on this rather than sub-fab availability alone. Considerations as subtle as where the spares are stored on site, within reach, in another room, or in another building, are captured in this matrix and available for analysis. Statistical analysis of this information across the global installed base permits an evaluation of the impact of each part on system availability and determines what parts are likely to be needed where. This allows for a localised approach to inventory management utilising global insight.

Continuous improvement

An initial availability matrix is developed during system design based largely on input from design engineers, component suppliers and in-house testing. The matrix is continuously updated with information reported from the field to determine true availability. The matrix also provides a basis for defining specific improvement projects. Figure 5 shows the projected impact on overall availability of a series of improvements. The hard data provided by the availability matrix supports a proactive approach to failure analysis and improvements in design and testing with component suppliers. The evidence-based approach promotes the development of collaborative relationships over extended periods of engagement. Figure 6 shows the results of an improvement project undertaken with a supplier of gas sensors to reduce the number of maintenance events associated with their sensor.

The next step involves introducing an intelligent health monitoring system that can anticipate the need for a spare part well before it occurs. If necessary, the supplier can be alerted to prepare for a timely deployment of the required component. This is especially valuable for long-lead time parts with complex supply chains. The semi-automated process

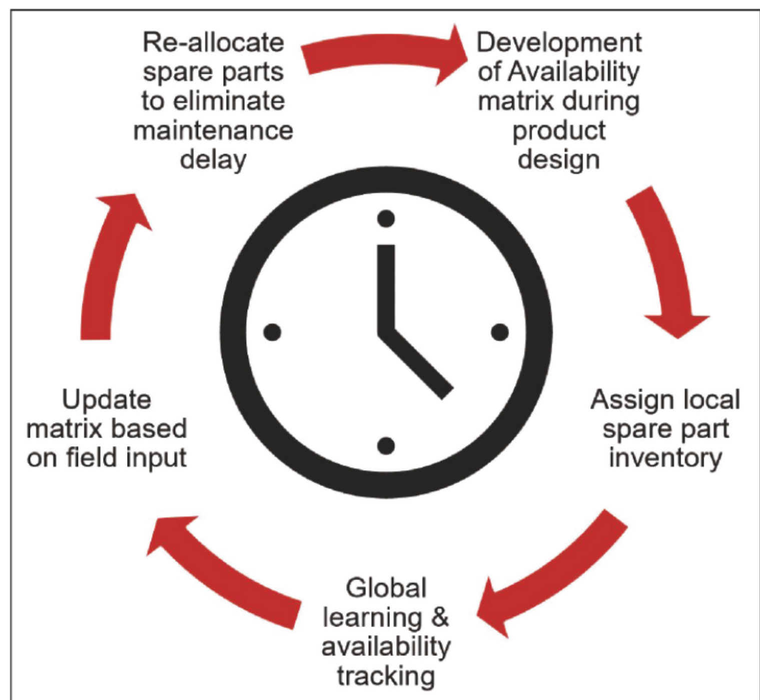

Figure 3: Continuous improvement is a repeating cycle of data collection, analysis and action.

Item	Activity	Frequency per year	Repair time	Spares location	Impact on Availability
Part A	Annual Maintenance	1	5hrs	Onsite (2hrs)	0.08%
Part B	Unscheduled Maintenance	0.5	4hrs	Warehouse (4hrs)	0.05%
Part C	Unscheduled Maintenance	0.5	1.5hrs	Next to system (0.5hrs)	0.01%

Figure 4: The availability matrix includes detailed information about every event that affects system availability.

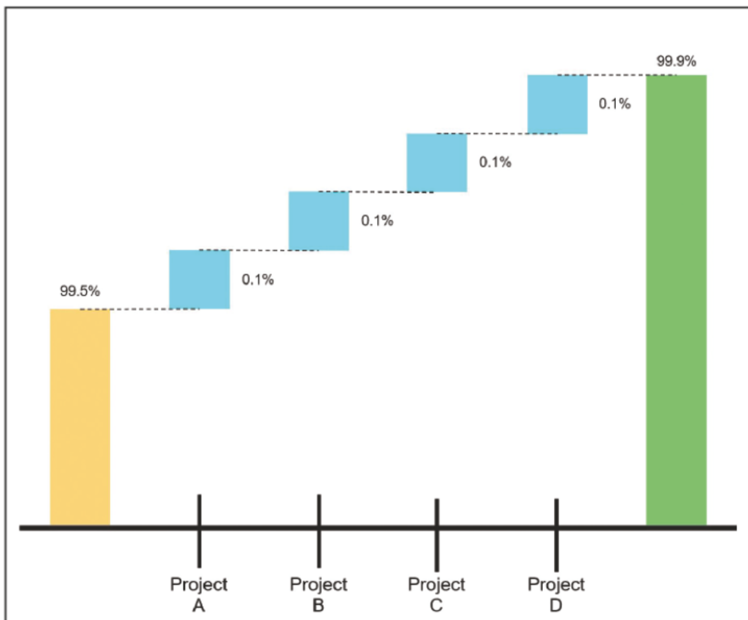

Figure 5: The availability matrix permits the intelligent allocation of resources to improvement projects likely to have the greatest impact on system availability.

reduces the risk of extended downtime waiting for critical parts.

Summary

The high cost of EUV lithography systems and their role as a bottleneck in the manufacturing process make maximizing their availability a high priority. The same priority must be given to critical sub-fab systems required to support EUV operations. Failure in the sub-fab directly affects the availability of the EUV process and imposes the same costs for production losses.

A data-driven program of continuous improvement is essential for optimizing availability. We have described the application of this approach to the management of spare parts inventories, one component of availability. Standards, such as SEMI E-10, are required to ensure the quality and consistency of the data used to construct the availability matrix. The approach also requires the availability of historical data from a broad base of installed systems. Given the high cost of EUV systems and the risk of production losses resulting from downtime, every effort must be made to optimize sub-fab system availability – any compromise in this area is likely to prove penny-wise and pound-foolish.

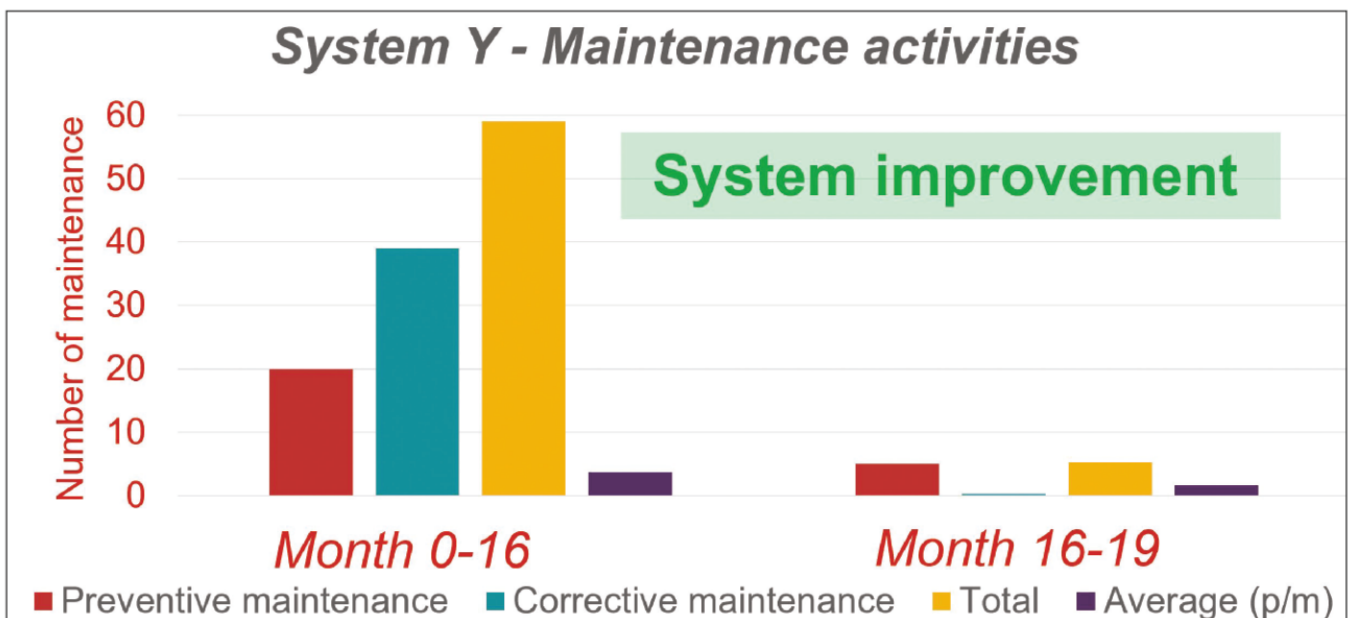

Figure 6: Solid data encourages productive discussion and collaborative relationships with component suppliers.

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VEECO Instruments
targets next-gen VCSEL requirements

VCSELs play an increasingly central role in advanced facial recognition applications after years of service in computer peripherals such as mice, scanners and printers. Silicon Semiconductor invited VEECO Instruments to describe key challenges and solutions for increased performance, higher throughput and greater repeatability in VCSEL manufacturing.

Replies from Somit Joshi, VP of MOCVD Marketing and Anil Vijayendran, VP of Precision Surface Processing Marketing, Veeco Instruments

VEECO and VCSELs

Left: Close-up of wafers processed in a VEECO TurboDisc system, optimized for superior wavelength, uniformity and defect control

Q VCSELs (vertical cavity surface emitting lasers) have played a role in computer peripherals for decades and are now central components within facial ID and advanced automotive applications. How did VEECO develop its portfolio and what is new in VCSEL technology?

A Veeco designs, manufactures and markets thin film process equipment that enables high-tech electronic device R&D and production worldwide, including VCSELs. Since our IPO in 1994, we have delivered advanced packaging lithography, laser annealing, single-wafer etch/clean, ion beam, MOCVD, MBE, ALD and related technologies to solve tough materials engineering challenges for our customers.

Veeco's expertise and innovations are used in the development and high-volume manufacturing of advanced silicon semiconductor devices for logic and memory applications (e.g., AI, IoT, Cloud Computing); as well as compound semiconductor products for solid-state lighting/displays (e.g., microLED) and power/RF (e.g., pHEMTs for 5G), photonics for 3D sensing (e.g., VSCEL, LiDAR, Augmented Reality) and data communications (e.g., Big Data, autonomous vehicles), to name a few.

In terms of MOCVD, Veeco has been a leader since the year 2000 in the compound semiconductor arena with 100+ man-years of solid domain expertise. Since then, Veeco has released a steady stream of MOCVD systems including the industry leading K475i platforms that have increased capacity and production while lowering cost of ownership. The patented TurboDisc® MOCVD technology is at the core of our capability enabling Veeco's systems to very precisely apply material to wafers exactly to our customers' specifications with many inherent advantages.

A VCSEL is a complex compound semiconductor device that's been around for many years (e.g., in computer peripherals like mice, scanners) and subsequently used primarily in the optical communication in the data and telecom space. More recently (2017 onwards), VCSELs have been applied in the 3D sensing arena (e.g., facial recognition applications, ADAS in driverless vehicles) which will be the main growth driver of the VCSEL industry within the next 5 years.

However, moving from traditional and historical applications to 3D sensing applications adds several challenges related to design and manufacturing. The design challenges include the move to higher power, bigger die size, more cavities and greater precision; all while needing to be integrated into larger modules with complex optics. Manufacturing challenges in VCSELs include the transition to 150mm wafers and more stringent process control for higher reliability and yield requirements in applications like 3D sensing.

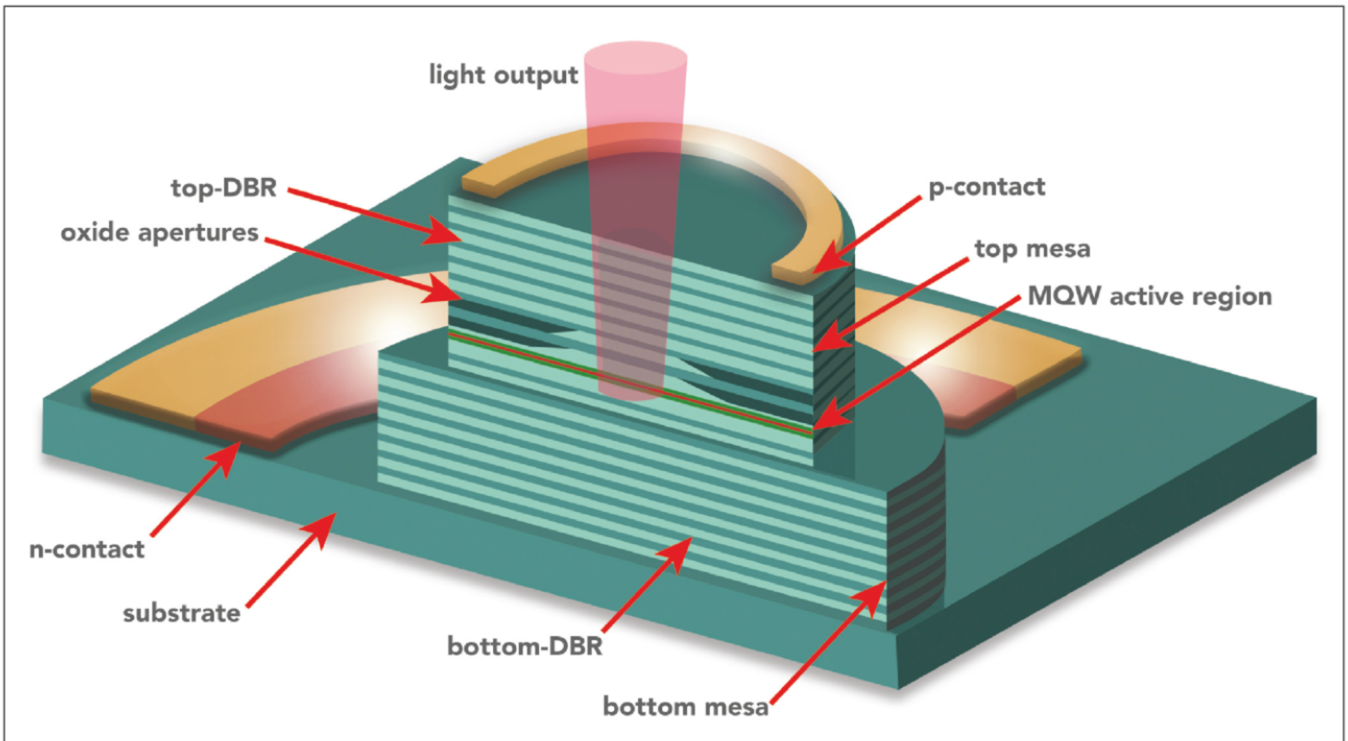
Q How does Veeco Instruments see the market for advanced VCSELs growing, and will this growth be primarily for higher-order devices with greater performance?

A We expect existing VCSEL use to grow and proliferate into additional applications over the next few years. We anticipate explosive growth for new applications in step with megatrends like AI, VR/AR and autonomous transportation, gesture sensing, augmenting cameras with 3D information, LiDAR arrays for distance ranging, short-haul datacom, materials processing, etc.

Veeco scientists have taken this proven domain expertise and optimized our existing platform for VCSEL manufacturing. We believe we have an advantage in this market because our TurboDisc technology provides the performance requirements

Somit Joshi

Anil Vijayendran



A simplified VCSEL cross-section illustration

without compromising productivity and uptime, resulting in an overall lower cost of ownership. We have demonstrated excellent uniformity and defectivity data using TurboDisc technology with extremely positive customer feedback.

Also, reactor design incorporating Veeco's Uniform FlowFlange™ technology produces films with very high uniformity and improved within-wafer and wafer-to-wafer repeatability with the industry's lowest particle generation. The simple design provides ease-of-tuning for fast process optimization and fast tool recovery time after maintenance for the highest productivity for applications such as lighting, solar, laser diodes, VCSELs, pseudomorphic high electron mobility transistors (pHEMTs) and heterojunction bipolar transistors (HBTs). Veeco is closely working with industry leaders in enhancing TurboDisc technology that delivers to tighter requirements for the next wave of more demanding applications–world facing applications for smartphones (and other mobility devices) and LiDAR for mission critical ADAS applications. We have validated (with industry leaders) that the TurboDisc roadmap provides the path to meet their tighter requirements on Oxide Layer composition control, Fabry Perot dip uniformity, etc.

Q Are VCSELs as a product class undergoing fabrication and performance enhancements, and what is essential from Veeco's perspective for supporting next-generation requirements?

A Let's look at the typical steps required to manufacture VCSEL chips: Epitaxy growth, p-side contact, mesa etching #1, passivation, mesa etch #2, and n-side contact. The n-side contact could be a top-side or back-side contact. Note that light emits from the front, while the back may be mounted to a heat spreader for high-power chips.

As mentioned earlier, VCSELs are mainly seen in low-power (few milliwatts) applications for optical data transmission, but higher power (over 100 mW devices emitting at around 980 nm) and higher (implying larger area) are being explored. Problems/challenges as we transition to production include:

- High yield for total population in 6 nm bin (for matching with detector optics)
- Composition uniformity for aperture size control (defines beam power and divergence)
- Low defectivity ($< 1/cm^2$) for structured light and large area VCSELs
- Migration to 6-inch wafers from 4-inch

In terms of testing and yield, VCSEL processing (vs. EEL for example) offers cost advantages because testing can be performed while the devices are still in wafer form. Moreover, wafer processing lends itself easily to 2-D array fabrication. Key epi level parameters that directly impact performance and are measured at the wafer level include:

- Uniformity (wavelength, composition, sheet resistance)
- Linewidth
- Defectivity
- Power level, threshold voltage, etc.

Most of the manufacturing complexity is in the epitaxial structure and the oxidation process to define the aperture since the remainder of the processing

is similar to other compound semiconductor devices such as LEDs, HEMTs, etc. Wavelength control is critical since VCSELs for sensing applications are paired with detectors and narrow band filters. All the die must be within the narrow wavelength window which could be as narrow as 6 nm. Thus, uniformity and repeatability are key. Defectivity control is also important, especially for larger arrays and chips.

The oxidation process sets the aperture size which impacts brightness. The major enhancement is the move to VCSEL arrays, which are large chips, where low defectivity and a uniform aperture are very important so that the performance of each chip in the array is well matched. The multi-quantum-well (MQW) wavelength, FP dip, and DBR stop band must be positioned precisely with respect to each other for the VCSEL to operate efficiently at the rated power. Several strategies come into play for improving VCSEL performance (e.g. power output, switching speed, efficiency) and reducing manufacturing costs so they can enter more applications. In a VCSEL, the light generated in the active MQW region bounces off highly reflective DBR mirrors on either side of the active region and is partially absorbed as it bounces between the mirrors, while a small portion escapes through the top mirror as the laser beam. Thus, each of these factors must be optimized.

While the epitaxial structure sets the upper bound for the VCSEL performance, real-life performance is based on how closely the epi structure can mimic the targeted design. For example, MQW quality defines the internal quantum efficiency, sharp interfaces in the DBR mirror enhance reflectance, precise positioning of dopants and intrinsically low background doping reduce light absorption and high conductance of the doped regions lowers the series resistance. These in combination set the lasing threshold current, the power conversion efficiency and the linearity of power with current. VCSEL designs for high speed switching require sub 5-micron apertures, strained layers, sharp doping gradients and ultra-thin layers.

Q What are key cost issues impacting VCSEL production and how can manufactures optimize performance while mitigating cost escalation?

A Most of the VCSEL manufacturing cost is associated with the epitaxial growth. Achieving consistent performance and high yield through multiple deposition campaigns and across a fleet of tools while maximizing the productivity per chamber (quantified as capex and foot-print efficiency) has the biggest impact on epitaxial manufacturing cost.

This is similar to LED manufacturing, although the manufacturing requirements for VCSELs are much more stringent. Veeco's TurboDisc technology has proven to be the tool-of-choice that enabled the ramp of LED manufacturing to high volume worldwide. Veeco's most recent GaN MOCVD system is the EPIK 868, the LED industry's highest productivity MOCVD system that reduces cost per wafer over 22 percent compared to previous generations.

The LED industry required a cost per lumen reduction roadmap to penetrate a very price-sensitive consumer

The VEECO Instruments K475i

market, and Veeco's TurboDisc platform delivered the solutions over time that enabled these targeted reductions on the strength of superior brightness performance and higher uptime and stability.

In fact, Veeco's historical impact on the LED industry, where over 50 percent of the world's LEDs were manufactured using Veeco equipment at one point, and the associated energy efficiency and sustainability benefits are often overlooked. Now, TurboDisc technology brings similar productivity and quality benefits to advanced LEDs (for example: microLEDs) and VCSEL manufacturing as the industry positions for the manufacturing ramp. In summary, Veeco is enhancing 6-inch wafer uniformity and controlling Al composition while managing defects and improving doping control by 25-50 percent over the current industry baseline. This is on top of the 40 percent higher productivity provided by TurboDisc technology.

Q Can you discuss the importance of removing excess photo resist when creating advanced VCSEL devices?

A In addition to MOCVD equipment, VEECO has world class wet processing systems that are currently used in VCSEL production. For instance, Metal-Lift Off (MLO) is an alternative to dry etching that is used to pattern metal lines. This technique is found most prominently in compound semiconductor applications where metals are not easily etched by plasma. Less expensive than dry etching, MLO relies on the quality of the incoming metal deposition, efficacy of the resist and solvent, and superior system design for success. If during the MLO process, the metal or photo resist is not effectively removed, this will lead to shorting between the lines and yield loss.

The WaferStorm® platform with ImmJET™ technology addresses both technical and productivity challenges. Technically, there is a trend to smaller features which increases the degree of difficulty of removing resist residues. More difficult to remove resists will increase process times and chemical costs. The ImmJET approach of combining batch and single wafer spray combines the best attributes of both technologies. First, the wafer is immersed in solvent for a longer period of time to allow for adequate swelling of resist.

Next, the wafer is moved to a single wafer chamber and the high-pressure spray easily removes the already swelled resist. Veeco's proprietary software enables the immersion and spray to occur in parallel to enable very high productivity. Innovative filtration and recirculation designs enable low chemical usage and reduced downtime. By enabling superior process control with industry leading throughput and cost of ownership, the WaferStorm and WaferEtch® platforms have achieved process tool of record (PTOR) status at leading customers today.

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Sensor searches demanding application

Micro opto-mechanical sensors (MOMS) are radiation-hard and combine a wide range with high sensitivity. Their specific structure and operation make them potentially very versatile but what are the advantages and possible applications of MOMS?

By Xavier Rottenberg, scientific director and group leader, for wave-based sensors and actuators at imec

How does this work?

At the end of 2017, imec presented a pressure sensor based on MOMS technology (MOMS = micro-optomechanical systems). In short, it's a sensor that converts the mechanical movement of a membrane (on micrometer scale) into an optical signal. Which works as follows: an optical circuit, e.g., a long waveguide, is built on a membrane. Subjected to a differential pressure stimulus, the membrane deforms, thus modifying the properties of the optical circuit, e.g., the phase of the light emerging from a long waveguide. By optically reading out this phase shift, one can determine the pressure that was initially applied to the sensor.

What can it be used for?

Two major categories of advanced pressure sensors exist in the industry: MEMS sensors and photonic sensors. Pressure sensors based on MEMS technology (micro-electromechanical systems) have a

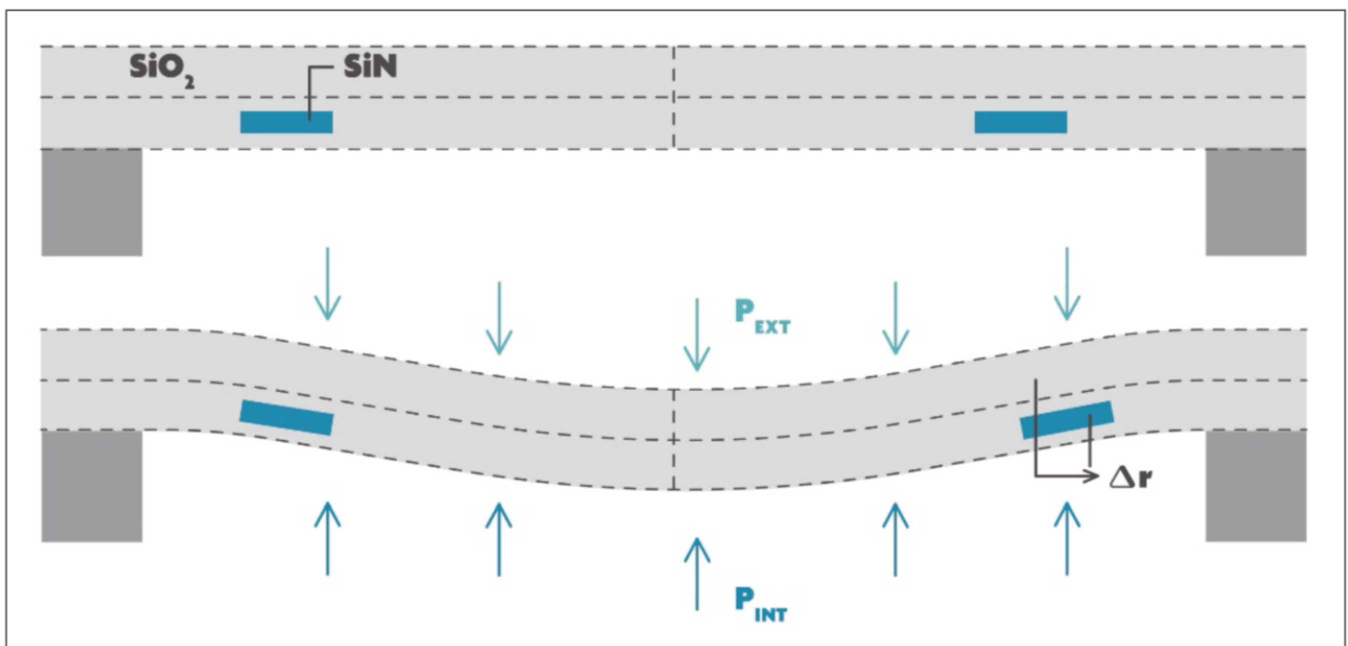


Figure 1. The deflection of a membrane carrying an optical waveguide causes a phase shift of an optical wave and allows to calculate the applied pressure.

With MOMS technology, imec makes sensors that have the same performance as the photonic sensors and the small size of MEMS sensors. They combine great accuracy and linearity with a wide dynamic range and thus the best of two worlds

similar mechanical detection principle (deflection of a membrane), but combined with an electrical readout (changing properties of an electric current). Because of their miniaturisation and performance, they are well established in areas such as the automotive and medical industry, height- and depth-measurements and flow sensing.

Photonic sensors use the changing properties of an optical wave when passing through a material that's being strained. They are popular because of their higher sensitivity and lower noise, but are not available in miniaturized and integrated systems. With MOMS technology, imec makes sensors that have the same performance as the photonic sensors and the small size of MEMS sensors. They combine great accuracy and linearity with a wide dynamic range and thus the best of two worlds.

Searching for the most demanding application

For several reasons, imec sees potential in MOMS. First because a small mechanical deflection in the sensor can induce a large optical effect and thus results in a high sensitivity. Secondly, the MOMS sensors do not contain metals, which makes them particularly interesting for medical applications. Think of sensors that are compatible with magnetic systems such as an MRI-scanner. Also, their biocompatibility has already been proven, so they are potentially suitable for implants, such as detecting intracranial pressure.

Another advantage of MOMS is that the mechanical movement and the optical reading are decoupled and independent from electric currents. It makes MOMS radiation-hard and insensitive to electromagnetic interference. And at least as important: it allows massive multiplexing: the parallel readout of an unprecedented number of sensors via an optical bus, not requiring integrated support electronics.

Imec reaches out to industry to jointly find the killer application that would require such performance. For example, we have envisioned a surgical glove with thousands of integrated MOMS sensors, which can be used for haptic detection of tumors.

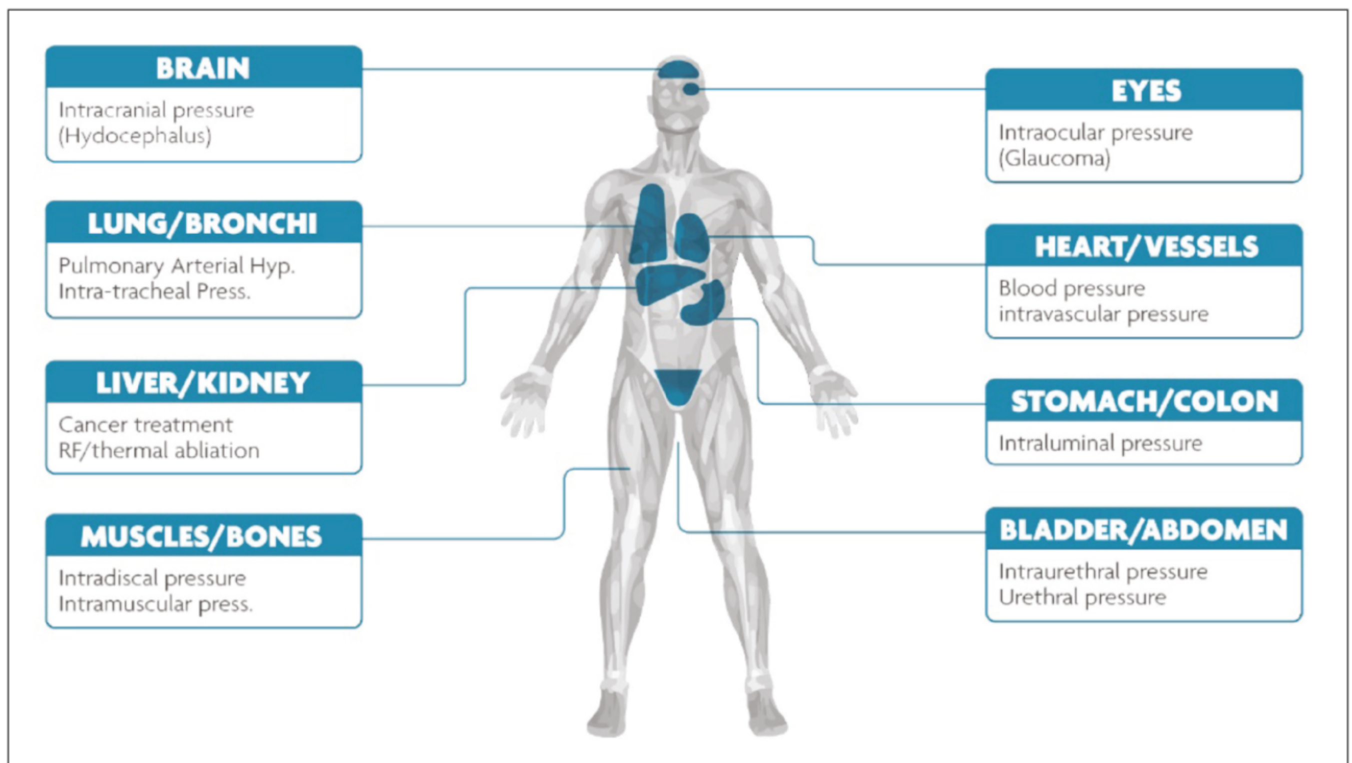
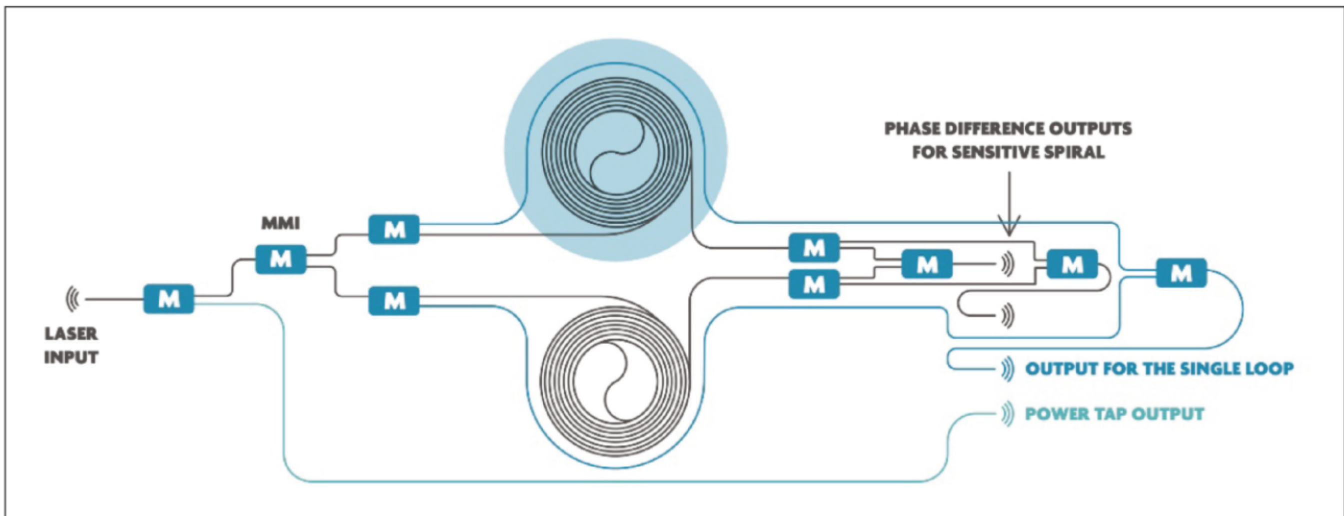


Fig 2: The imec sensor is radiation-hard and biocompatible, so it is extremely suitable for potential medical applications.



From top to bottom: Classic MZI design and the new design by imec (scheme and photo), in which multiple loops of different shapes result in a high sensitivity across a wide range.

Increasing popularity

MOMS technology, however, is not new. First references in scientific literature date back to the nineties. Nevertheless, the technology is still in its infancy. Largely because advanced miniaturization and process technology are required for MOMS to reach their full potential compared to classic photonic sensors. It is therefore no coincidence that in recent years the popularity of MOMS has increased in parallel with accelerated developments in the area of photonics. At least, this is what happened at imec, where research on MOMS started a few years ago, by combining imec's robust SiN-based photonics platform with the imec expertise in MEMS technologies. Meanwhile, MOMS have their own process flow in the imec pilot line, based on low-temperature SiN deposition (PECVD) and 200 mm deep UV lithography. This level of process integration improves the quality of the sensors and also allows post-processing on optical imagers. But the biggest gain in performance of imec's MOMS sensor came from its design.

Smart system design

The common way to design a MOMS pressure sensor is based on Mach-Zehnder Interferometers (MZI) or ring resonators. Imec applied a clever approach to the design of the MZI, giving them a wider range thanks to the number of loops and their shapes.

Adding loops increases the sensitivity of the sensor but decreases its unambiguous measurement range. The imec design therefore combines short (single loop) and long spiral waveguides on a single membrane. By cleverly combining the signals from both waveguides, the imec sensors maintain a high sensitivity and a wide range.

First measurements indicate a standard deviation of less than 1Pa at a range that can go beyond 100kPa, which is similar to commercial sensors, but without the electromagnetic sensitivity of MEMS sensors and in a smaller form factor than typical photonic sensors.

The future

For imec, the pressure sensor is a first example of how MOMS technology can complement MEMS and photonic sensors. The aim is to eventually develop a robust MOMS platform with a wide range of sensors.

"At the same time, imec is reaching out to industry to discover in which applications the sensor's high performance and broad applicability can prove their added value."

About Xavier Rottenberg

Xavier Rottenberg is scientific director and group leader wave-based sensors and actuators at imec. He received the MSc degree in Physics Engineering and a supplementary degree in Theoretical Physics in 1998 and 1999 from "Université Libre de Bruxelles", Belgium. He received further his PhD degree in Electrical Engineering in 2008 from KU Leuven, Belgium. He worked one year at the Royal Meteorological Institute of Belgium in the field of remote sensing from space and joined imec in 2000.

Modifying wet process cleaning equipment maximizes automation benefits

Semi-customizing a variety of automated cleaning tools enhances process repeatability, throughput, and safety

TO MEET APPLICATION specific requirements, design engineers in industries that manufacture sensitive components often need more flexibility than standard options allow for a utomating wet process cleaning equipment.

These specialized components can range from chips, wafers, semiconductors, and electronic devices to the specialized optics for world-class lasers. In fact, the more complex the equipment, the greater the need becomes for more advanced adaptable cleaning options.

Cleaning, an integral part of many manufacturing and maintenance process, is often critical to the performance of a broad range of technologies and refers to the use of agents such as solvents, acids or bases to remove unwanted particulates and other contaminates. It also refers to the etching process utilized in semiconductor fabrication, where the "cleaning" is the precision removal of thin layers of material.

Fortunately, a wide range of wet process equipment automation now exists that can more flexibly accommodate specific cleaning requirements. Modifying these automated cleaning tools to fit the application can cost-effectively enhance process repeatability, throughput, and safety. In many cases, only minor editing to the standard equipment is all that is necessary.

The benefits of cleaning process automation

"Companies that automate a cleaning process usually do so to improve process repeatability, production throughput, or safety," says Louise Bertagnolli, president of JST Manufacturing (Boise ID). JST designs and manufactures a variety of manual to fully automated cleaning equipment, including proprietary systems that include all of the features and transfer devices required for a complete turnkey cleaning process.

Repeatability involves the ability to precisely repeat a cleaning process and is critical to maintaining quality. This includes exact measurement and dispensing of cleaning agents and rinsing solutions as well as providing the systems and tools needed to transport the cleaned items from one bath to another.

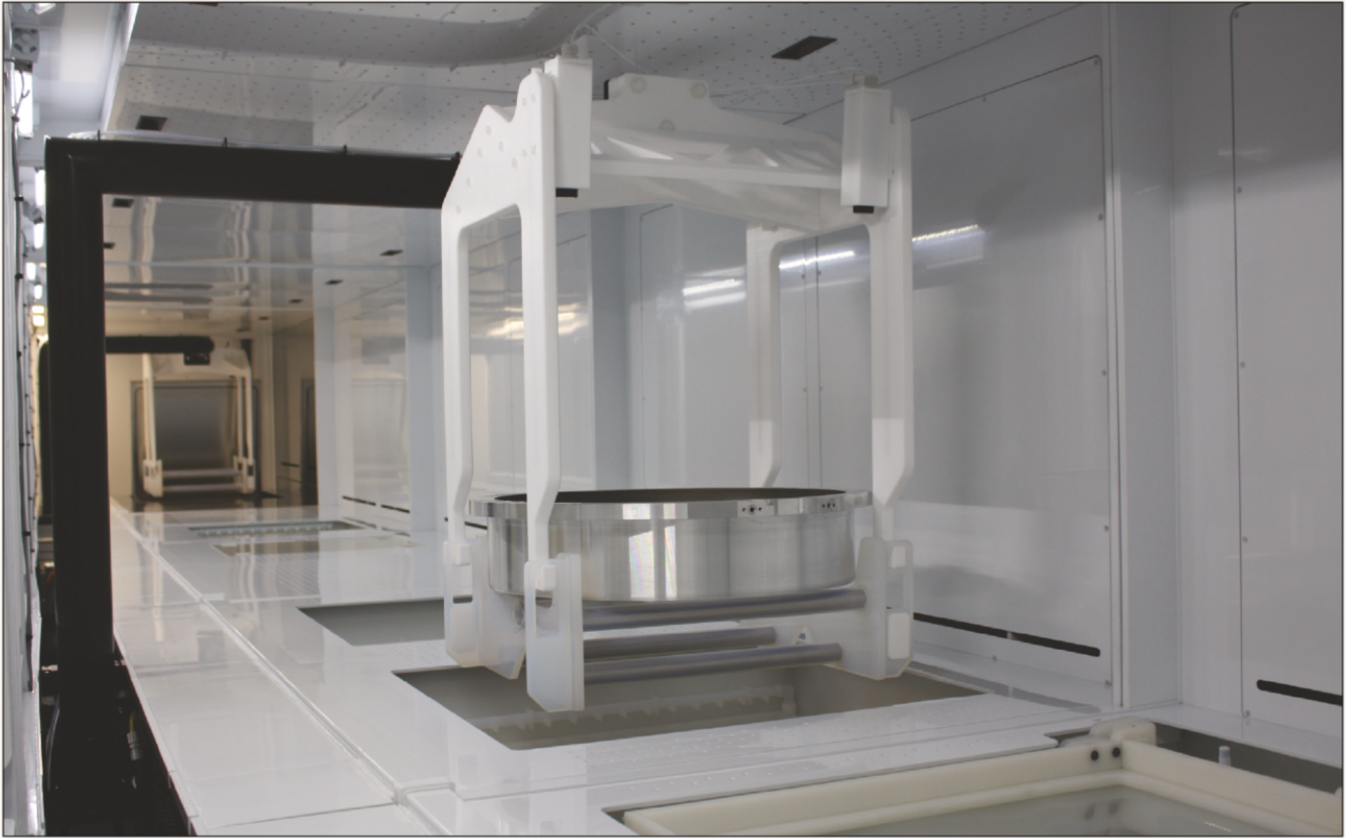
Automating the cleaning process, of course, can increase production throughput for high-volume production. If the process takes place in a cleanroom, then the entire system including motors and robotics must be appropriate for that environment.

Since production can involve moving products around above hot tanks or near chemical baths, automating can improve safety as well. Similarly, it can improve production ergonomics, for example, by eliminating the need for employees to repeatedly rotate or handle the parts being processed, which reduces the potential for injury.

How to cost-effectively automate cleaning

Determining when to automate cleaning usually depends on the stage of development of the part or product.

According to Bertagnolli, while a manual cleaning



process is normally utilized during R&D, when the process is defined and the company has buying customers, it is a good idea to automate.

However, to successfully automate, it is often best to customize the cleaning systems to the specific needs of the application as much as possible.

"When considering job modifications, it is important to take into account the requirements for floor space, product size, production throughput, etc.," says Bertagnolli. "Since one size does not fit all, it is crucial not to shove everybody into the same platform."

Bertagnolli cautions, however, that not every project needs to be fully customized from the ground up. Quite often standard automation platforms can be customized according to length and height and number of baths. Cleaning process design engineers can consult with automation suppliers to determine where to put the transfer system and what automation modules will fit best in the space available.

"Unlike proprietary platforms that do not allow modification, the best platforms are tried and true, but offer a range of options that utilize the same motors, actuators, and automation in an interchangeable way," says Bertagnolli. "This allows flexibility while minimizing cost and complexity."

This type of an approach can be successfully utilized in fully automated, special project, and semi-automated cleaning processes.

Fully automated stations

Semi to fully automated, multitask cleaning stations typically utilize at least four baths. Such stations can pick up and drop off product via robots at the baths as required, while following preprogrammed recipe sequences. However, the stations often need modification to operate most effectively.

In order to allow for modification, cleaning specialists like JST offer multiple automation platforms that can accommodate various space constraints. The

Unlike proprietary platforms that do not allow modification, the best platforms are tried and true, but offer a range of options that utilize the same motors, actuators, and automation in an interchangeable way

company can also tailor loading to the specific task by utilizing front, rear, or overhead robots with either front or side loading. Optional turntables can enable ergonomic side loading as well as rear access for ease of maintenance as well.

"For automated stations, the number of tanks; robot location, movement speed, loading; as well as sizing of everything is based on the specific requirements," says Bertagnolli.

In regards to modifying such automated cleaning systems, the company works closely with automation partners such as Bosch Rexroth (Charlotte, NC) to develop cleaning stations using linear motion and electric drive and control technology.

Recently, the two firms worked together to create an automated system for cleaning silicon chunks to the extreme purity of 11N to meet requirements for the manufacture of semiconductor chips. The project entailed building a cleaning line 138 ft. in length and incorporating multiple gantry robots.

The throughput volume requirement for the chunks was four tons for every 22-hour shift. To accomplish this, JST had to develop a unique basket system to transport the material throughout the process.

To provide for such a long cleaning system, JST engineered and built it in two units. In the 24-ft-long unit, baskets of chunks are manually loaded through an auto-door. Then two-axis robots cycle the baskets through five acid etch baths and two rinse baths arranged in a single row down the length of the second unit.

Special automated projects

When automated cleaning and stripping of wafers, optics, disk drives, flat panels and other delicate parts is required for special projects, equipment is available that operates on a completely self-contained, dry-to-dry basis.

One such unit is JST's 300 CLV Cleaner and Stripping Tool. Once product is placed in the dry tank, the unit can process through either single or multiple chemical processes, rinse and dry according to a pre-programmed recipe without operator intervention or mechanical moving parts to maintain.

As an example, the National Ignition Facility (NIF) at Lawrence Livermore National Laboratories (LLNL), Livermore, CA has utilized such a tool. NIF, the world's highest-energy laser system – a stadium-size machine – consists of 192 laser beams that will focus nearly two million joules of energy and create temperatures and pressures that exist in the cores of stars and giant planets.

One of the innovations in the NIF cleaning tool – utilized in a tank-like configuration and designed to clean up to 300-pound laser optics – was eliminating the need to move the optics to different locations in order to perform the washing, rinsing and drying functions.

"Our engineers suggested that rather than transport these heavy optics for such functions, we could simply transport the chemistry (solutions) to the optics in a fixed location," explains Bertagnolli. "We also designed a sling-like device to hold the optics and also let technicians rotate them during the inspection process."

JST built two cleaning tools for NIF which are mirror images for the same price a traditional linear transfer tool could be built. This affords NIF double the capacity and most important, provides redundancy.

Semi-automated systems

Many processors with lower-volume throughput requirements might consider using semi-automated cleaning systems. Compared to manual systems, these provide better repeatability, faster production, and added safety. This type of cleaning system is appropriate for MEMs, LEDs and silicon applications. It is compact, software controlled, and usually easy to service.

JST manufactures a standard compact semi-automated wet bench called the Tigress, a two axis, front-to-back compact system that is used by smaller semiconductor companies. A dual version of this semi-automatic system is also available. It is popular among semiconductor manufacturers that use it for cleaning, stripping, and etching of semiconductor substrates when cleaning acids, bases or solids are used to remove photoresists.

"While design engineers may be resigned to using standard, automated, wet process cleaning equipment, tailoring options to the project can significantly enhance quality, production, and safety while actually cutting cost," concludes Bertagnolli.

MediaTek unveils 5G SoC for 5G flagship devices

At COMPUTEX, MediaTek revealed its full 5G readiness with the introduction of its 5G chipset, a multi-mode, 7nm 5G system-on-chip (SoC) designed to power the first wave of high-end 5G smartphones.

The integrated 5G chipset, with the MediaTek Helio M70 5G modem built in, packs world-leading technology into its compact design. It includes Arm's newest Cortex-A77 CPU, Mali-G77 GPU and MediaTek's most advanced AI processing unit (APU) to meet the power and performance demands of 5G to deliver super fast connectivity and extreme user experiences.

The multi-mode 5G chipset is for 5G stand alone and non-stand alone (SA/NSA) sub-6GHz networks. It supports connectivity from 2G to 4G to bridge existing network access while 5G networks roll out globally.

"Everything about this chip is designed for the first wave of flagship 5G devices. The leading-edge technology in this chipset makes it the most powerful 5G SoC announced to date and puts MediaTek at the forefront of 5G SoC design," said MediaTek President Joe Chen. "MediaTek will power rollouts of 5G premium level devices."

The MediaTek 5G chipset is integrated with its previously announced Helio M70 5G modem to give device makers a comprehensive solution for ultra-fast 5G in a power efficient package. MediaTek's single 5G chip design is superior to two chips solutions, especially in being able to deliver power efficient performance. The new chipset will be ready for lead customer samples in Q3 of 2019 and be in commercial devices by Q1 of 2020. Full specifications of the MediaTek 5G SoC will be introduced in the coming months.

"The industry, OEMs and consumers have high expectations for 5G. We are confident devices powered by MediaTek's 5G chipset, with its impressive architecture, leading imaging features, powerful AI and ultra-fast 5G speeds, will deliver incredible experiences," said Chen. The ultimate winners of MediaTek's entrance into the high end 5G chipset market are consumers as MediaTek helps spur the introduction of more 5G devices, so more people can access great technology.

The 5G SoC's integrated Helio M70 modem supports LTE and 5G dual connectivity (EN-DC) with dynamic power sharing capability, plus multi-mode support for every cellular connectivity generation from 2G to 5G. It also has dynamic bandwidth switching technology that allocates 5G bandwidth required for specific applications to improve modem power efficiency by 50 percent and extend battery life.

Samsung plans aggressive rollout of next-gen transistors

SAMSUNG'S FOUNDRY DIVISION has offered an update to its process technology roadmap, including the first process design kit for its forthcoming 3-nm gate-all-around (GAA) technology. Company executives also provided some details about advanced 3D packaging technologies and introduced a new cloud-based design environment.

Samsung plans to begin risk production of one of two 3-nm GAA processes that it plans to offer by the second half of next year, with mass production expected in 2021. The company plans to begin risk production of the next 3-nm GAA process in 2021, with mass production expected in 2022.

Last month, Samsung began volume production on its 7-nm FinFET process, the first to make use of next-generation extreme ultraviolet (EUV) lithography. While the company plans to roll out derivative 6-, 5- and 4-nm pro cesses with FinFETs over the next two to three years, Samsung considers 3 nm to be its next major process technology node and the first that will use GAA 3D multibridge-channel FETs, which feature gate material surrounding the channel region on all sides.

Voltage scaling of FinFET technology runs out of steam at 0.75 V at the 10-nm node. Samsung is implementing its GAA technology — which utilizes nanosheets as opposed to nanowires, enabling greater current per stack — to reduce the operating voltage to 0.7 V, said Yongjoo Jeon, a principal engineer with Samsung's foundry marketing team. Conventional GAA with nanowires requires a larger number of stacks due to its small effective channel width.

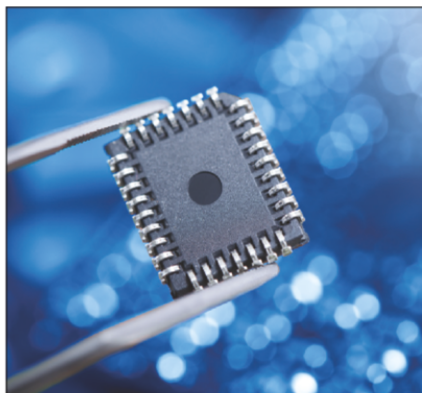
Socionext adopts Cadence tools for 7nm designs

CADENCE DESIGN SYSTEMS have announced that Socionext used the Cadence full-flow digital and signoff tools for the successful production tapeout of its latest large, 16nm ASIC chip and has built a design environment for its 7nm designs. Using the capabilities of the integrated full flow, Socionext sped design closure on its 16nm design when compared with its previous solution.

The Socionext certified flow for the 16nm and 7nm designs includes the Cadence Genus Synthesis Solution, Cadence Conformal Equivalence Checker, Cadence Innovus Implementation System, Cadence Quantus Extraction Solution, Cadence Tempus™ Timing Signoff Solution, Cadence Voltus IC Power Integrity Solution, and Cadence Physical Verification System (PVS). In particular, the Tempus Timing Signoff Solution enabled the Socionext team to meet design productivity goals for its 16nm production designs by using the Tempus SmartScope hierarchical models.

The Tempus SmartScope models facilitate hierarchical static timing analysis (STA) signoff and signoff-accurate engineering change orders (ECOs) by letting users dynamically abstract portions of the design so they can analyze blocks with accurate chip-level context. Additionally, the Voltus IC Power Integrity Solution enabled Socionext to reduce electromigration (EM) analysis turnaround time by 60 percent, which is critical for 16nm and below FinFET process technologies.

For Socionext's 7nm design, the Innovus Implementation System's Flex H-Tree capability in particular has already proven to be critical in enabling power, performance and area (PPA) benefits. The Flex H-Tree is an advanced clock synthesis technology that enables users to consider floorplan blockages and power tradeoffs, allowing Socionext to meet its target goal for clock skews. "As a leading ASIC and ASSP product supplier for various market segments, power, performance and area as well as overall turnaround time are incredibly



important to us," said Mr. Takuya Yasui, General Manager of LSI Development Division, Automotive & Industrial Business Group at Socionext Inc. "We have successfully used the Cadence full-flow digital and signoff tools to deliver multiple chips at 16nm and have chosen the Cadence flow as our plan of record for both our 16nm and 7nm designs. Our close collaboration with Cadence was essential for our 16nm design success, and the Cadence full flow is now also an integral part of our development of future 7nm products."

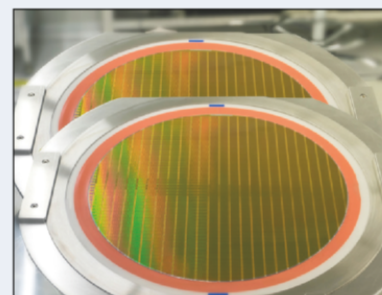
"We recognize that the ASIC and ASSP market presents growing competitive requirements and design challenges, including added design complexity and shorter time-to-market demands," said Dr. Chin-Chi Teng, senior vice president and general manager of the Digital & Signoff Group at Cadence. "Cadence has collaborated with Socionext to successfully deploy the Cadence full-flow digital and signoff tools to help achieve design success. We look forward to continuing to support them with future designs."

From synthesis through implementation and signoff, the Cadence integrated full-flow digital and signoff tools provide a fast path to design closure and better predictability. The digital and signoff full flow supports the company's overall Intelligent System Design strategy, which enables system and semiconductor companies to create complete, differentiated end products more efficiently.

Trymax receives multi-system orders

TRYMAX SEMICONDUCTOR EQUIPMENT BV (Trymax), has announced it has received multi-system orders for its NEO 2000 and NEO 3000 series from a leading Taiwanese packaging house.

This order will expand the existing NEO install base at the customer in Taiwan and allows Trymax to break into the customer's fab in China. Shipping of the systems will start in Q2 and continue during Q3 2019.



"We are pleased to receive this order for several shipments in two different fabs, said Jonathan Lee, General Manager of Trymax in Asia. Many companies claim to deliver the best Cost of Ownership but these repeat and expansion orders are a concrete example that our solutions are truly delivering it".

NEO 2000 series is a dual chamber system for wafers up to 200mm. NEO 3000 series is a dual chamber system for wafers up to 300mm. All systems will be configured with Trymax's dual source plasma technology combining RF and microwave to provide the best ashing rate and uniformity trade-off. The dual source technology is the choice recommended by Trymax for many wafer level packaging applications such as bumping or Fan-Out Wafer Level Packaging.

TSI introduces new remote airborne particle counters

TSI has announced a new range of AeroTrak+ Remote Airborne Particle Counters (APCs) for monitoring manufacturing cleanrooms. TSI is so confident about the performance of the new laser technology inside, that all models are covered by an industry-exclusive standard 5 year laser warranty.

AeroTrak+ Remote APCs supply uninterrupted, reliable particle counting data during the cleanroom manufacturing process. Flexible installation options reduce system complexity and cost of ownership with LoRaWAN long range wireless communications and Power over Ethernet (PoE) capabilities. With use, facilities can protect themselves from increased risk and decrease operational costs related to waste, downtime, and redeployment – with minimal maintenance.

AeroTrak+ Remote APCs are available for use in facilities with (7000 Series) or without (6000 Series) an external vacuum system. They incorporate second-by-second sampling. The instant an excursion occurs or an adverse trend starts, the end-user is notified to enable proactive steps to minimize product waste.

"TSI's AeroTrak+ Remote Airborne Particle Counters have been designed with the rapidly changing demands of modern clean manufacturing processes in mind. To deliver maximum flexibility and reduce installation complexity for our customers, LoRaWAN long range wireless technology is the logical choice," states Tim Russell, TSI Controlled Environments Business Director. "Now, installing and relocating remote airborne particle counting systems has never been easier.

"Disco completes new silicon valley office Japanese semiconductor equipment manufacturer Disco has relocated and expanded its USA head office in California in order to strengthen its ability to respond to the needs of its customers. The relocation completion date is scheduled for early July, 2019.
The $21 million office building, based San Jose, has three times the floor area and 3.5 times the processing space of the previous building, including a clean room. Disco says that with advances in IoT, medical, communications, and self-driving technology, the development needs for semiconductors and electronic components is expanding, causing the number of requests from these companies for processing verifications and contracted processing in the device development stages to increase.

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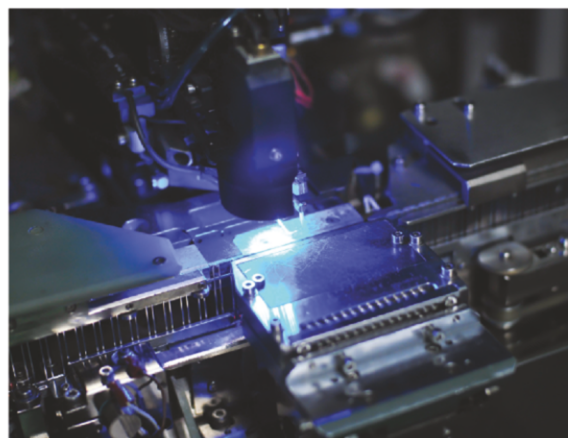
Chip equipment billings plummet due to U.S. China trade war



GLOBAL BILLINGS for chipmaking equipment during the first quarter this year plummeted as the semiconductor industry reacts to the trade war between the U.S. and China.

Billings in the first quarter plunged 19 percent from the same period a year ago to $13.8 billion, according to global electronics industry association SEMI.

Equipment billings peaked in the first quarter of 2018 at $16.99 billion and have been declining each quarter since that time, according to SEMI.

The standout in the data was Taiwan, which boosted its first quarter investment while all other regions covered by SEMI turned negative. The island that's home to TSMC and a host of other semiconductor companies topped the global list at $3.81 billion in billings for the first quarter.

After peaking in 2016 at $12.2 billion, the equipment market in Taiwan contracted for two consecutive years, Chamness said. TSMC's strong investment in 7nm+ capacity and preparation for the rollout of 5nm is a key part of the growth this year, she added.

SEMI expects that investments in China and in memory will rebound next year, making 2020 a recovery year.
The SEMI data are gathered jointly with the Semiconductor Equipment Association of Japan (SEAJ) from over 80 global equipment companies that provide data on a monthly basis.

Global chip sales will drop by 7.2% from last year as the semiconductor market works through a supply glut and ducks crossfire from the U.S.-China trade war, market research firm International Data Corporation (IDC) said last month. Other analysts said the outcome could be worse than expected, given a number of negative factors.

Sales this year are set to reach $440 billion compared with $474 billion in 2018, IDC said in a May 15 press statement. This year may mark the first decline after three years of growth.

For 2019, the logic segment is likely to grow 1% to $319 billion while DRAM and NAND are expected to decline in 2019 and 2020, IDC said.

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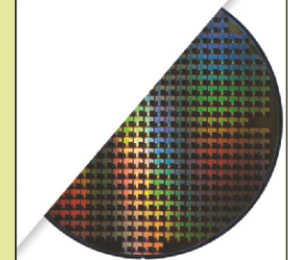

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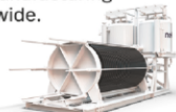

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