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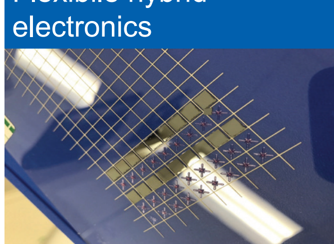
Security and privacy for future devices

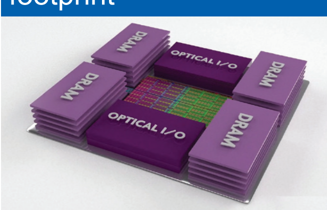
Flexibile hybrid electronics



Advanced inspection control

The future of transport automation

3D integration reduces footprint



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editor'sview

By Mark Andrews, Technical Editor

SEMICON Europa and the drive for Industry 4.0

SEMICON EUROPA convenes 14-17 November at Messe Munchen in Bavaria, Germany. Collocated with productronica, the event will bring together thousands of exhibitors and attendees.

The timing could not be better. Shifting the conference to Munich places it at the heart of Europe's hope to recapture roles in global electronics industries that faded when IC production shifted largely to Asia. Industry 4.0 is Europe's hope for home grown growth.

Munich and other key European manufacturing centers are driving the program that began in 2010 as an EU initiative, followed by Germany's Action Plan for High-Tech Strategy 2020. Industry 4.0 envisions manufacturing entering a fourth evolutionary wave; the first began with 19th century steam, followed by electrification enabling mass production, which led to the third wave: automated manufacturing.

The fourth wave – Industry 4.0 – is seen of by many as machine interconnectivity, but it is actually much more. Industry 4.0 envisions using sophisticated, high-end sensors (HES), M2M communication, additive manufacturing (3D printing on steroids), robotics, AI, analytics and cloud computing to unify cyber and physical systems into harmonized control that lowers costs and increases quality.
SEMICON Europa is the next major non-governmental forum with an Industry 4.0 emphasis. But while Europe works to drive automation, the Chinese are busy at what might be called 'Industry 3.0 Ultimate.' They are positioning China to vault over its low-wage-manufacturing status to land as a semiconductor leader in eight years.

China calls it Made-in-China 2025 (MIC 2025,) putting the resources of the world's second largest economy behind its aspirations. How serious are they? Twenty four semiconductor fabs are now under construction in the PRC—a new global record.

China is expected to consume 13 percent of chips produced by pure-play foundries in 2017, up from 12 percent last year, according to IC Insights. China already consumes most of the world's chips as components of products made there. Is there enough market growth for all? Right now forecasts says chip sales could grow 20 percent this year, but one should remember that last year offered tepid growth while sales actually ***declined*** much of 2014-2015.

As we gather for SEMICON Europa, Industry 4.0 programs will dominate many conversations—as they should. We need to get this right. Europe has Industry 4.0 and its 2020 goals while China has MIC 2025. China will not relax; it wants industrial dominance. If we want the next wave to be led by Europe, now is the time to act.

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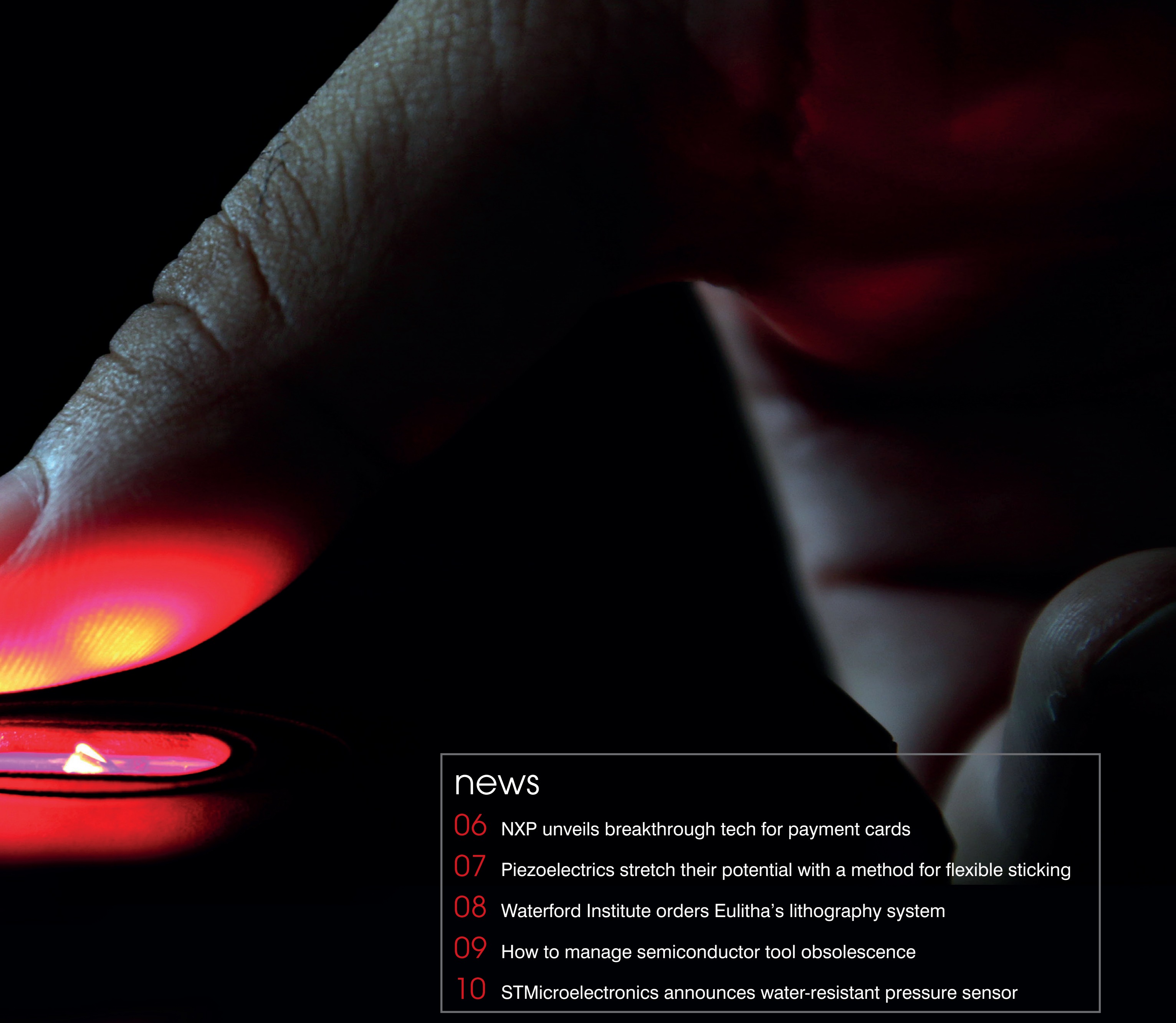

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NXP unveils breakthrough tech for payment cards

NXP SEMICONDUCTORS N.V. has debuted two significant technology breakthroughs at the largest fintech innovation event, Money 20/20, October 22-25, 2017, in Las Vegas. The company will showcase its new contactless fingerprint-on-card solution while also demonstrating a new world benchmark for payment card transactions speeds.

Fingerprint sensors on payment cards

The fingerprint-on-card solution gives payment network operators and banks a secure, convenient and fast payment card option to consumers. Coupling dual interface cards with an integrated fingerprint sensor enables faster transactions without the need for end-users to enter a PIN number.

"The result provides a secure and dramatically more convenient way for consumers to make payments. The convenience provided by mobile payment in today's NFC-based mobile wallets can now be replicated with cards. It is also ideal for use in other form factors and applications such as electronic passports," said Rafael Sotomayor, senior vice president and general manager of secure transactions and identification business. "The breakthrough reinforces NXP's commitment to the payment and secure identification space by helping our customers deliver next-generation applications and solutions to the market."

To ensure a lower barrier of entry for card makers, the company's secure fingerprint authentication solution on cards does not require a battery and easily fits into standard card maker equipment as part of the broader payment ecosystem.

Cards with fingerprint authentication are fully compliant with existing EMVCo point-of-sales (POS) systems.

New benchmark for blazing transaction speeds

Demonstrating seamless, fast, and smart card transaction experiences, the NXP high-performance platform makes it possible to achieve M/Chip transactions speeds of <200 ms, surpassing the industry requirement of 300 ms.

"This increased level of performance offers flexibility to add new features or higher crypto countermeasures and still meet current industry transaction requirement," said Sotomayor. "The requirement for faster payment transaction will continue, and NXP is committed to providing the performance to meet these needs and make contactless transactions faster and flawless."

Critical Manufacturing reports record orders

CRITICAL MANUFACTURING, provider of Global Manufacturing Execution Systems for complex discrete manufacturers is pleased to announce record growth in orders of 60% by the end of Q3, 2017, compared with the same period in 2016. Total revenue is up by 24% and is expected to grow significantly by year-end, marking the 5th consecutive year of revenue growth.

New customer acquisition has contributed to the increase, along with strong interest in Critical's unique capabilities to accelerate the adoption of Industry 4.0 concepts into manufacturing, including its 3D digital twin of manufacturing assets, sensor technology, mobile and connectivity, shop-floor marketplace and vertical and horizontal integration. Critical Manufacturing has made strategic investments in North America, Europe and Asia to align with customers' needs for global deployment and support. In addition, the company is expanding its partner ecosystem to ensure continued customer success across the globe. Critical Manufacturing is focused on helping manufacturers of highly complex and regulated discrete products in the hi-tech industries such as semiconductor, electronics, medical device and automotive.

The unique challenges of these industries coupled with rapid innovation cycles and demand for low volume and personalized products are driving the adoption of modern MES as the backbone of Industry 4.0 transformation.

Francisco Almada Lobo, Critical Manufacturing CEO, commented: "Our robust financial position is a key indicator of the trust that our large customers place in us to deliver business value to them for the long-term. We expect continued sustainable growth and have a strong pipeline of product innovations which will help our customers to realize additional benefits." Critical differentiates from traditional MES with its high level of flexibility where any complex physical or business process can be configured in minutes, creating a huge advantage for industries that require rapid turnaround of improvement cycles and faster new product introduction.

Francisco Almada Lobo concludes: "We are continuously investing in our solution to become the most modern, flexible and agile MES solution available, with a committed roadmap for industry specific suites to allow for the most out of the box capabilities and rapid implementation.

Unlike traditional MES systems, Critical has no legacy technology and is designed to enable manufacturing and quality operations to easily adapt to future change."

Piezoelectrics stretch their potential with a method for flexible sticking

PIEZOELECTRIC MATERIALS are used for applications ranging from the spark igniter in barbeque grills to the transducers needed by medical ultrasound imaging. Thin-film piezoelectrics, with dimensions on the scale of micrometers or smaller, offer potential for new applications where smaller dimensions or a lower voltage operation are required.

Researchers at Pennsylvania State University have demonstrated a new technique for making piezoelectric microelectromechanical systems (MEMS) by connecting a sample of lead zirconate titanate (PZT) piezoelectric thin films to flexible polymer substrates. Doctoral candidate Tianning Liu and her co-authors report their results this week in the Journal of Applied Physics, from AIP Publishing.

"There's a rich history of work on piezoelectric thin films, but films on rigid substrates have limitations that come from the substrate," said Thomas N. Jackson, a professor at Penn State and one of the paper's authors. "This work opens up new areas for thin-film piezoelectrics that reduce the dependence on the substrate."

The researchers grew polycrystalline PZT thin films on a silicon substrate with a zinc oxide release layer, to which they added a thin layer of polyimide. They then used acetic acid to etch away the zinc oxide, releasing the 1-micrometer thick PZT film with the polyimide layer from the silicon substrate. The PZT film on polyimide is flexible while possessing enhanced material properties compared to the films grown on rigid substrates.

Piezoelectric devices rely on the ability of some substances like PZT to generate electric charges when physically deformed, or inversely to deform when an electric field is applied to them. Growing high-quality PZT films, however, typically requires temperatures in excess of 650 degrees Celsius, almost 300 degrees hotter than what polyimide is able to withstand without degrading.

Most current piezoelectric device applications use bulk materials, which hampers miniaturization, precludes significant flexibility, and necessitates high-voltage operation.

"For example, if you're looking at putting an ultrasound transducer in a catheter, a PZT film on a polymer substrate would allow you to wrap the transducer around the circumference of the catheter," Liu said. "This could allow for significant miniaturization, and should provide more information for the clinician."

The performance of many piezoelectric thin films has been limited by substrate clamping, a phenomenon in which the rigid substrate constrains the movement of the piezoelectric material's domain walls and degrades its properties.

Some work has been done crystallizing PZT at temperatures that are compatible with polymeric materials, for example using laser crystallization, but results thus far have led to porous thin films and inferior material properties.

The released thin films on polyimide that the researchers developed had a 45 percent increase in remanent polarization over silicon substrate controls, indicating a substantial mitigation in substrate clamping and improved performance. Even then, Liu said, much work remains before thin-film MEMS devices can compete with bulk piezoelectric systems.

"There's still a big gap between putting PZT on thin film and bulk," she said. "It's not as big as between bulk and substrate, but there are also things like more defects that contribute to the lower response of the thin-film materials."

Newly optimized entry-level deposition system from Kurt J. Lesker

Kurt J. Lesker Company has launched the 2018 NANO 36 Thin Film Deposition System Platform, a newly optimized entry-level deposition system that is fully capable for glovebox integration. The platform offers increased deposition capabilities and substrate platen options while decrease system footprint. The NANO 36 provides an accessible price point and exceeds all KJLC quality standards.

"Our products are used by the world's largest and most well-known manufacturers, research facilities, and scientists," said Kurt J. Lesker IV, president and CEO at Kurt J. Lesker Company. "In response to increasing demand for new and enhanced high-quality vacuum equipment, our R&D team created the NANO 36 for use within the controlled atmosphere of a glove box."

The 2018 NANO 36 Thin Film Deposition System Platform is compatible with multiple deposition techniques and substrate fixture options.

Waterford Institute orders Eulitha's lithography system

EULITHA, a Swiss startup company offering innovative lithography equipment and services for the nanotechnology, photonics and optoelectronic markets has received an order for one of its PhableR 100 photolithography systems from Waterford Institute of Technology (WIT) in Ireland.

The PhableR 100 exposure tool incorporates Eulitha's proprietary Displacement Talbot Lithography technology that enables robust printing of very high resolution periodic patterns at low-cost. The system was purchased by the Institute to enable production of metallic nano-patterns for use in new types of bio-sensors. The purchasing of this innovative system was made possible following the award to WIT of close to €1m in funding from Science Foundation Ireland's Research Infrastructure Awards that form a key part of implementing the country's science and technology strategy – Innovation 2020.

The new system will enable researchers at WIT's Pharmaceutical and Molecular Biotechnology Research Centre (PMBRC) to scale up the development of its next generation diagnostic sensors based on surface plasmon resonance. The PhableR 100 exposure tool allows the precise replication of nanopatterns onto the sensor substrate that is required for the extreme multiplexed sensor system to be further developed.
The tool will also be used by researchers to exploit the optical resonance properties of plasmonic nanostructures to further develop applications in NIR spectroscopy for Process Analytical Technologies (PAT), healthcare and smart agriculture. The Pharmaceutical and Molecular Biotechnology Research Centre (PMBRC) is an applied research centre which aims to support the sustainable growth of the pharmaceutical and healthcare industry in Ireland. The PMBRC consists of an 800 m2 state-of-the-art facility with 34 highly-trained research personnel. The PMBRC has established links with national and international partners in academia, industry and medical care institutions. Joseph O'Mahony, project leader at PMBR said "The PMBRC is enthusiastically looking forward to receiving the PhableR 100 tool and working with Harun and his team at Eulitha to demonstrate the exceptional capabilities of Displacement Talbot Photolithography. When fully integrated within the PMBRC's state of the art laboratories the PhableR 100 will underpin a new research facility that will comprise state of the art equipment in nanofabrication, printable materials deposition and materials characterisation. This national facility will further develop the PMBRC's collaborative research actions with Irish and international academics and industries."

Harun Solak, CEO of Eulitha, said: "we are very pleased to add WIT to our growing base of installations at academic institutions worldwide. The unique ability of our Displacement Talbot Lithography technology to print on different types of substrates and surfaces and the proven performance of our systems in the field were critical factors in helping us win this important contract. We look forward to working with the group ofJoseph O'Mahony to help them use the capabilities of the system in the most effective way."

The PhableR 100 system can expose periodic patterns down to feature sizes below 150 nm which rivals much more expensive high-end i-line steppers. The patented focus-free imaging technology used by the system enables uniform printing on non-flat samples often found in photonic and optoelectronic sectors. Eulitha had recently announced the delivery of further lithography systems to the CIOMP institute in China and University of Bath in the UK. Eulitha is a spin-off company of the Paul Scherrer Institute, Switzerland. It specialises in the development of lithographic technologies for applications in optoelectronics and photonics.

It produces and markets nano-patterned samples and templates using its own PHABLE tools and e-beam lithography systems.

IC Insights raises 2017 IC market forecast to +22%

IC INSIGHTS has raised its IC market growth rate forecast for 2017 to 22%, up six percentage points from the 16% increase shown in its Mid-Year Update. The IC unit volume shipment growth rate forecast has also been increased from 11% depicted in the Mid-Year Update to 14% currently. As shown below, a large portion of the market forecast revision is due to the surging DRAM and NAND flash markets.
In addition to increasing the IC market forecast for this year, IC Insights has also increased its forecast for the O-S-D (optoelectronics, sensor/actuator, and discretes) market.

In total, the semiconductor industry is now expected to register a 20% increase this year, up five percentage points from the 15% growth rate forecast in the Mid-Year Update.
For 2017, IC Insights expects a whopping 77% increase in the DRAM ASP, which is forecast to propel the DRAM market to 74% growth this year, the largest growth rate since the 78% DRAM market increase in 1994. After including a 44% expected surge in the NAND flash market in 2017, including a 38% increase in NAND flash ASP this year, the total memory market is forecast to jump by 58% in 2017 with another 11% increase forecast for 2018.

At $72.0 billion, the DRAM market is forecast to be by far the largest single product category in the semiconductor industry in 2017, exceeding the expected NAND flash market ($49.8 billion) by $22.2 billion this year. As shown in Figure 1, the DRAM and NAND flash segments are forecast to have a strong positive impact of 13 percentage points on total IC market growth this year.

Excluding these memory segments, the IC industry is forecast to grow by 9%, less than half of the current total IC market growth rate forecast of 22% when including these memory markets.

How to manage semiconductor tool obsolescence

WHEN IT COMES TO semiconductor manufacturing equipment obsolescence, there's no good way to avoid the issue. With the significant expansion of the Internet of Things (IoT) and MicroElectroMechanical Systems (MEMS) markets as well as the continuation of More than Moore (MtM), the demand for devices on legacy equipment is increasing. Semiconductor fabs using this legacy equipment will inevitably lose part of their supply lines to obsolescence every year.

Many Integrated Device Manufacturers (IDMs) put off dealing with the issues until it is too late, but there are significant drawbacks to this approach. In many cases, waiting until obsolescence becomes a problem can have serious consequences. These include extended system downtime, lost production and potential yield loss when replacement parts are not fully engineered and tested with urgency to get the systems back to production.

Semiconductor manufacturing equipment parts become obsolete when the Original Equipment Manufacturer (OEM) discontinues making the part or servicing the systems in which is it used. This commonly occurs when the demand for such devices drops to a level that makes it unsustainable for the OEM to continue manufacturing it. Oftentimes they may also be getting pressure through the supply chain for the sub-assemblies that make up the part in question.
As the devices we use become smaller and we are ever more connected through IoT and MEMS Devices, the entire supply chain that serves semiconductor manufacturers is affected, especially the systems used in 150mm and 200mm tech nodes.

The Reactive Approach to Obsolescence Management Manufacturers typically have about 6-12 months to react to an end-of-life announcement on critical components. This leads to a last time buy process in which they try to bulk up on inventory to extend the life of their production lines, but this is a temporary solution at best. In many cases the amount of inventory needed to extend equipment lifetime is simply unavailable. According to research on obsolescence challenges faced by IDMs, "a typical end of life announcement generates product orders to the Original Component Manufacturer (OCM) that cover only 60 percent of future demand for that specific part." While the last time buy process quickly consumes the remaining inventory for an obsolete component, there are other ways to manage end of life announcements. Some manufacturers will simply upgrade their production lines with newer equipment, but this is not cost effective in the long-term. It is only a short term fix at best, as this equipment will also have parts going obsolete early into its life cycle. Supply chain managers know that investing in new equipment every time a tool part goes obsolete is not sustainable.

Building Relationships and Planning Ahead Alternatively, some IDMs will engage with a licensed OEM partner to develop a repair and refurbishment program, or to develop new upgrades for their current systems. This works best when there is a wider relationship between the IDM community and the licensed OEM partner. When customers and suppliers work together on a holistic strategy to combat the obsolescence issue, everyone benefits. When they are aware of systems and parts that need to be replaced, manufacturers can work with licensed OEM partners to re-engineer sustainable solutions without heavily investing in new equipment. These third-party partners have relationships with the OEMs and access to parts and designs that are used to tailor custom solutions and value added manufacturing.

Samsung completes qualification of 8nm LPP process

SAMSUNG ELECTRONICS has that 8-nanometer (nm) FinFET process technology, 8LPP (Low Power Plus), has been qualified and is ready for production.

The newest process node, 8LPP provides up to 10-percent lower power consumption with up to 10-percent area reduction from 10LPP through narrower metal pitch. 8LPP will provide differentiated benefits for applications including mobile, cryptocurrency and network/server, and is expected to be the most attractive process node for many other high performance applications. As the most advanced and competitive process node before EUV is employed at 7nm, 8LPP is expected to rapidly ramp-up to the level of stable yield by adopting

the already proven 10nm process technology.

"With the qualification completed three months ahead of schedule, we have commenced 8LPP production," said Ryan Lee, Vice President of Foundry Marketing at Samsung Electronics. "Samsung Foundry continues to expand its process portfolio in order to provide distinct competitive advantages and excellent manufacturability based on what our customers and the market require."

"8LPP will have a fast ramp since it uses proven 10nm process technology while providing better performance and scalability than current 10nm-based products," said RK Chunduru, Senior Vice President of Qualcomm.

Details of the recent update to Samsung's foundry roadmap, including 8LPP availability and 7nm EUV development, will be presented at the Samsung Foundry Forum Europe on October 18, 2017, in Munich, Germany.

The Samsung Foundry Forum was held in the United States, South Korea and Japan earlier this year, sharing Samsung's cutting-edge process technologies with global customers and partners.

STMicroelectronics announces water-resistant pressure sensor

STMICROELECTRONICS has taken underwater accuracy to new heights with its latest miniature pressure sensor, which is featured in the new Samsung Gear Fit 2 Pro. As smart watches and wearable fitness trackers permeate the fabric of everyday life, owners want to go further with their devices and track performance across extra activities like swimming. Samsung's Gear Fit 2 Pro, the next generation of sports band, supports these trends with features like built-in GPS, continuous heart rate monitoring, and larger on-board memory to do more even when not connected to a smartphone.

ST's new waterproof pressure sensor, the LPS33HW, is part of the mix: resistant to chemicals like chlorine, bromine, and salt water, it is ideal for pool or sea swimming, and will also resist soaps or detergents used when showering or cleaning. Wearables are only just beginning to swim, and waterproofing pressure sensors creates challenges beyond just protecting the electronics. The LPS33HW is not only the most accurate, but also helps OEMs get their products to the store-shelves more quickly by recovering sooner after the stresses of manufacturing. Other sensors can require up to seven days to regain maximum accuracy after coming off the production line, but devices containing the LPS33HW are ready for action in less than half that time. This is due to the sensor's high-performance built-in processor and the advanced formula of its water-resistant gel filling.
"Wearable trackers enhance smart living, and can now deliver an important extra boost with the go-anywhere ruggedness aided by our water-resistant LPS33HW sensor," said Andrea Onetti, MEMS Sensor Division General Manager, STMicroelectronics.

"Samsung takes advantage of the pressure sensor's best-in-class performance for the new Gear Fit 2 Pro range and users will appreciate both its accuracy and toughness." In addition to smart consumer devices like wearables, other equipment including industrial sensors and utility meters can also benefit from the robustness and high measurement accuracy of the LPS33HW. The 10bar pressure sensor can withstand being submerged up to 90 meters, and the very low RMS pressure noise of 0.008mbar allows apps like an altimeter, depth gauge, or weather monitor to deliver consistent and stable results. The sensor accuracy drifts by less than ±1mbar per year. When soldered to a circuit board during product manufacture, the accuracy is affected by less than ±2mbar, and returns to normal after less than 72 hours – significantly quicker than similar water-resistant pressure sensors.

ClassOne announce financing program

CLASSONE GROUP, provider of semiconductor processing systems, has announced a special new financing program that seeks to give more attractive options to equipment purchasers. ClassOne stated that the new financing program can eliminate the upfront cash outlay typically associated with equipment purchases, instead allowing more affordable and budgetable monthly payments.

The new financing options will include capital leases, fair-market-value leases, term loans, payment deferrals and bridge-to-budget solutions.
ClassOne has developed its new program in association with First American Vendor Finance, one of the nation's largest and most highly respected equipment finance providers. The new financing program will be available both to current and future ClassOne customers.

"Our goal is to make it easier for users – especially budget-limited users – to acquire the tools and technology they need to achieve more profitable revenues," said Byron Exarcos, CEO of ClassOne Group. "By integrating affordable new financing options directly into the equipment purchase process we can provide buyers with more attractive, more turnkey solutions – and put their new tools to work more quickly."

Microsemi acquire high performance business of Vectron

MICROSEMI and Knowles Corporation, have jointly announced that Microsemi has entered into a definitive agreement to acquire the high performance timing business of Vectron International, a Knowles company, for $130 million.

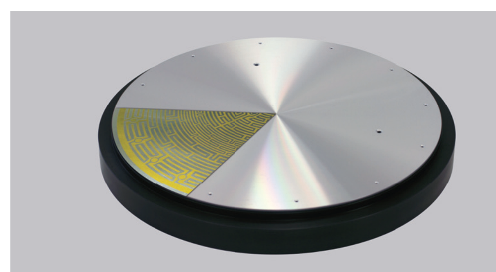
Vectron design, manufacture and mark frequency control, sensor and hybrid solutions using the latest techniques in both bulk acoustic wave (BAW) and surface acoustic wave (SAW)-based designs from DC to microwave frequencies.

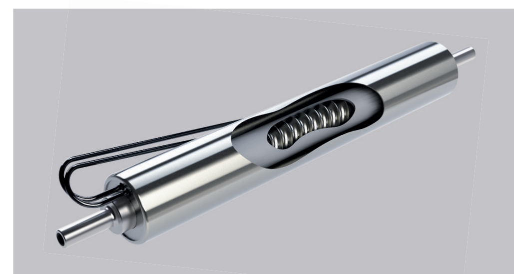
"Microsemi is focused on building the industry's most comprehensive portfolio of high value timing solutions," said James J. Peterson, Microsemi's chairman and CEO.

"Vectron's highly complementary technology suite expands our product offering with differentiated technology and allows Microsemi to sell more to its tier one customers in the aerospace and defense, communications and industrial markets while improving upon the operating performance of the combined model as we execute on significant synergy opportunities."

SEMICONDUCTOR

Watlow's Thermal System Solutions Enable Next Generation Technology





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It takes vision to automate transport

Automobile and truck manufacturers see automation as the surest means to reduce injury and death on motorways. Automotive sensing technology is set for a radical upgrade as engineers add cameras, radar and LiDAR systems to cars and trucks like never before.

Slide into the driver's seat of any contemporary automobile or light transport vehicle and it is immediately clear that driving has come a long ways in a short while. Look past the touch screens, infotainment options and back seat DVD players to discover a world of new safety technology. As amazing as today's digital systems may seem, they are only precursors to auto makers' ultimate goal: autonomous driving.

Long before automobiles and trucks are 'driving themselves,' scores of tech challenges need to be solved, not the least of which involve the myriad high-end sensors (HES) needed to enable 'sight' under any conditions. Sensors are needed to navigate without full-time GPS, to avoid roadside obstacles, and to effortlessly complete complicated tasks such as telling the difference between falling rains and falling rocks: easy for humans/impossible using today's automotive tech.

Three technologies are vital to automating the future of vehicle transport:Radar, LiDAR and digital camera systems.
Radar Perhaps the most familiar of all navigational and driver assistance aids, Radar offers superior long-range performance, but has its drawbacks. Although all Radars share common qualities, automotive radar varies in terms of power, frequency and range. Today's clunky Radars employ multiple chipsets using silicon and other technologies. Tomorrow's systems will need to be radically smaller and cost less to be viable, efforts being driven by companies including Infineon, NXP, Renesas and Texas Instruments (TI).

LiDAR Another detection system, but more complex than Radar, it performs a similar function but is better at recognizing objects and establishing distance. LiDAR (light imaging, detection and ranging) utilizes laser energy instead of high frequency RF signals, and is steadily decreasing in functional complexity and cost. LiDAR is affected by weather conditions more than radar, but LiDAR is better at resolving sizes and shapes, helping drivers to determine whether a 'light shower' up ahead is falling water or tennis ball-sized rocks from a mountain avalanche.

Cameras Advanced digital vision—already a part of many automotive sensing arrays—provides an edge that neither radar nor LiDAR can match in terms of resolving detail, but obviously suffers during nighttime and in conditions that substantially reduce visibility. While some companies such as Mobileye assert that camera-based systems can fulfil all necessary sensing roles, few automotive manufacturers agree. Industry analysts believe advanced driver assistance systems and fully autonomous automobiles will be served by a combination of Radar, LiDAR and digital camera sensors. Get the full story at HES International Tomorrow's technology is being researched and built today in the many advanced semiconductor, photonic integrated circuit and hybrid device manufacturing centers across Europe, Asia and the Americas.

Learn about the evolving future of automotive sensing technology and the advanced sensors that will make it possible by attending HES International, 10-11 April 2018, in Brussels, Belgium.

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High-end equipment for high-tech industries

MEYER BURGER is global technology company specialising on innovative systems and processes based on semiconductor technologies. The company's focus is on photovoltaics (solar industry) while its competencies and technologies also cover important areas of the semiconductor and the optoelectronic industries as well as other selected high-end markets based on semiconductor materials.

The company's comprehensive product portfolio is complemented by a worldwide service network with spare parts, consumables, process know-how, customer support, after-sales services, training and other services. Meyer Burger is represented in Europe, Asia and North America in the respective key markets and has subsidiaries and own service centres in China, Germany, India, Japan, Korea, Malaysia, the Netherlands, Switzerland, Singapore, Taiwan and the USA. The company is also working intensively to develop new markets such as South America, Africa and the Arab region. The registered shares of Meyer Burger Technology Ltd are listed on the SIX Swiss Exchange.

Drawing upon broad experience and expertise, Meyer Burger provides advanced technology solutions for high-precision coating, structuring and processing of surface areas through the application of plasma and ion beam technologies. The process systems feature a modular composition that ensures a flexible adaption to various methods of surface treatment, such as plasma-enhanced chemical vapor deposition (PECVD) or ion beam trimming (IBT). Mobile communications products require a significant number of frequency filter components, such as SAW (Surface Acoustic Wave) or BAW (Bulk Acoustic Wave) filters. The manufacturing process of these MEMS (Micro Electro Mechanical Systems) components utilizes a frequency trimming process.

Meyer Burger's IonScan platform for ultra-precise surface smoothing in the sub-nanometer scale is the leading solution that opens new possibilities for high-tech applications not only in MEMS, but also in semiconductor, sensors and high precision optics.

Some novel concepts require further and new coating techniques. Meyer Burger accommodates this demand for flexibly configurable coating equipment with the MAiA® platform. Being a leading system in the photovoltaic industry, MAiA® is entering other high-end markets due to its flexibility, multiple applications, and capability of coating both front and back side of a substrate within one machine and in one run.

Customer focus drives AP&S growth

Ever-changing global manufacturing requirements have driven AP&S expansion programs that give customers access to an industry-leading suite of wet processing and metal lift-off tools.

AP&S INTERNATIONAL GmbH has a deeply ingrained customer focus that has led to waves of company expansions, creating one of industry's most extensive wet process portfolios along with unique metal lift-off technologies and unparalleled responsiveness to changing market opportunities.

Getting to know AP&S International (Donaueschingen, Germany) is somewhat like receiving a nesting or Matryoshka doll: there is a new layer to be discovered at every turn. Silicon Semiconductor editor Mark Andrews spoke with AP&S CEO, Alexandra Laufer-Müller, to learn more. He discovered a growing

portfolio of products and services supporting wide-ranging semiconductor requirements including MEMS and micro-structuring as well as an R&D program focused on long-range customer requirements. AP&S constantly innovates. Its almost three-fold Demo Center expansion created a hands-on customer pre-sale experience; its expanding customer care programs are centered on maximizing up-time and first-to-market advantages.

"We specialize in wet process technology," Laufer-Müller said, "But we offer so much more, which

The steadily increasing challenges of the industries that we target make it necessary to offer customers not only high quality wet process tools, but to guarantee maximum uptime in their production everywhere and every time

is a reason we encourage customers to visit our headquarters. But because we know that this is not possible for everyone, we have focused on bringing our expertise to the customer as well as after sales service that strives to be the very best."

"Our aim is to cover the full range of wet process solutions, which are required across both front- and back-end production chains. Thus, our products perform functions such as cleaning, etching, metal etching, PR strip, electroless plating, lift-off, drying and developing processes. That is the beginning. Together with our customers we steadily develop new, outstanding processes, like the AP&S metal lift-off process, which is unique in today's market. We also offer manual-, semi- and fully-automated applications," she explained.

Today's AP&S grew out of 2003 acquisitions; collectively the company has served semiconductor manufacturers for two decades. When AP&S discovers a need it will set about identifying ways to meet that need, which often results in new hardware or software tool development. AP&S can dedicate its resources with confidence since each expansion it has undertaken is based upon customer requirements, thereby helping ensure ROI. The company takes its customer-centric focus to the point that business units are organized around the way process tools are typically purchased: single wafer tools or batch processing tools. One of their latest innovations and third major business group is the After Sales Unit that was established this year.

"The After Sales Unit was established at the beginning of 2017. The reason for this is quite simple. The steadily increasing challenges of the industries that we target make it necessary to offer customers not only high quality wet process tools, but to guarantee maximum uptime in their production everywhere and every time. The goal of this new unit is to offer exactly that to our global customers via the best after-sales support worldwide. Having these three units we are able to offer our customers everything they need from one source," she explained.

The focus of After Sales support is built around helping customers by having a primary access point for determining what parts or repair services are needed and to help ensure that customers have little or zero down time through preventative maintenance programs, long-distance diagnoses, easy access through smartphone/App-based interfaces and AP&S personnel dedicated to the customers' long-term satisfaction. The system supports 'typical' needs for spare parts and fast, on-site service, but goes farther by offering global service that leverages the company's deep knowledge of customers' preferred way to do business.

"With AP&S, customers have a reliable partner, offering them everything they need for efficient wet processes. In addition to the already

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mentioned advantages, we also provide services like tool relocations, on-site upgrades and cost-efficient refurbishment programs for used tools. Furthermore AP&S has developed some new, innovative IoT tools for more comfortable operation, monitoring and ordering of required spare parts and/or technical support, which bring added customer value," she said. Because each customer has unique needs, the After Sales Unit consciously tailors services to suit those preferences and needs.

"As we all know, handling wafers and substrates within cleanrooms consists of numerous steps and critical processes, which have to be optimally coordinated in order to obtain high-quality results. Wet processing is certainly just one of these many steps, but one that decisively influences quality. AP&S makes a significant contribution by helping to ensure the stability and purity of wafers and substrates. Our tools make sure that no residues or unwanted particles remain on wafer surfaces; we also prevent unintentional mixing of chemicals and in this way we create a clean basis for further processing."

Laufer-Müller said that some examples of the company's most well-known products include the SpinMask tool from the AP&S single wafer portfolio that provides outstanding mask cleaning results. In the wet bench range the AP&S A-Series tool (available with 100 wafer half-space features for high volume manufacturing [HVM]) is flexible and can handle up to 200mm wafers; for 300mm, AP&S is developing a new platform called TeraStep™ that accommodates up to 50 wafers at once. The CleanStep AP&S Carrier Box is another example of an ideal cleaning and drying tool for carrier boxes along with open cassettes, pods or FOUPs—it employs a combination of spray and spin process techniques. Given the company's deep roots in semiconductor manufacturing, AP&S is also sensitive to the fact that while some customers need the latest technology to support next-generation products, others need the most cost-effective approach possible. Refurbished tools are ideal for these customers as well as for companies that are just getting started.

"Refurbishment of an older tool can be very cost-effective, and this is a hot topic in the market today, and therefore it is, of course, a part of the AP&S service range. We offer comprehensive refurbishment programs not only for used AP&S tools, but also for HMR, Steag (successor: Mattson / Akrion), Lotus Systems and FSI Mercury."

"We renew outdated hardware components and install effective, state-of-the-art software and SECS/HSMS automation that make the tool fit for existing and future market technology requirements. New electric components and pneumatic cabinet enclosures complete the process, along with secured spare parts availability, which is quite an important aspect when a customer purchases refurbished equipment. Again our intention of offering maintenance, spare parts, technical service and software support—all from one hand, also stays in focus here."

The CEO noted that while some customers seeking refurbished tools need to reduce manufacturing costs, others—like those developing new MEMS products—typically only need 200mm or smaller wafer sizes, which can usually be satisfied only with older tools. At the same time the customer wants to be certain that process tools (refurbished or otherwise,) are ready for future needs and are compatible with the latest factory automation/MES requirements. AP&S ensures that refurbished tools are completely updated to every extent possible.

Semiconductor manufacturing is constantly changing, which is another reason that AP&S invests heavily in research and development, including its distinctive approaches to sales and service.

"We began our current expansion in 2016. From the customer perspective the biggest change is the substantial growth of our Demo Center, which includes 300mm process capability that we can now show 'live' for those who wish to see a new tool in action before they buy. The customer can test the wet process application of interest and get all crucial information such as a comprehensive test report containing complete parameters of the process set-up, a recommendation for the process recipe based upon test results and further important system configuration details."

"In 2017 we completed installation of a new UHPW system in our primary Donaueschingen, Germany facility. The system reduces impurities of municipal water to what is considered an 'ultratrace' level of less than 1ppb per cationic element, which helps us further eliminate the possibilities of any particles surviving a cleaning process," she said, adding that, "by rinsing and cleaning AP&S tools with ultrapure water prior to delivery, they can be qualified much faster and less effort by customers is needed on-site. The defect density requirements for production output can be achieved much more quickly."

"We have also expanded our cooperation network with external partners like renowned universities, among which I would like to highlight our latest partnership with the Fraunhofer Gesellschaft. The synergy effect here is clearly the bundled in-depth expertise between AP&S and the latest institute research into semiconductors. Finally, the ongoing development process of our wet process applications plays a significant role and is essential to keep pace with future market trends as guided by the ITRS roadmap and individual specifications of our customers," she explained.

Reinvestment to anticipate and meet customers' rapidly changing needs keeps the company's developers thinking constantly about what may be needed months and years in the future. AP&S recently expanded its internet connectivity options with its Web Worker App that provides convenient control and fast data access from anywhere in the world. By scanning QR codes on process tools and parts on-site technicians can immediately access data sheets, manuals, guides and instructions, as well engage spare parts ordering and other support needs.

The company's wide range of wet process tools, cleaning applications, R&D investments combined with a constant pursuit of customer satisfaction are at the forefront of the AP&S commitment to semiconductor manufactures. The company is also looking ahead to further ways that on-site service and its After Sales Unit can earn business while improving the customer experience. A new effort to elevate ease of access will debut at SEMICON Europa (14-17 November, at Messe Munich, Booth Number 1739, Hall B1).

"Our software team has been working on a fascinating project with the Microsoft Hololens. Those who have seen it feel it is simply amazing. I do not wish to reveal too much ahead of SEMICON Europa. But I encourage all interested parties to visit our booth where they can step into the virtual, futuristic world of AP&S wet process technology. I just want to emphasize that the Microsoft HoloLens is a great tool, bringing many new, until now unused advantages and possibilities for both customers and solution providers in our industry."

"As you can see, we are totally focused on customer requirements. Whether that customer needs a single tool for manual wafer cleaning or the most advanced, fully-automated wet processing application for 10nm and below devices, AP&S has the solutions needed today and for the years to come," she said.

Chips with fingerprints make the connected world safer

Chip biometrics form one of the cornerstones of imec's research into a tight and lightweight hardware security that should help ensure the security and privacy of billions of future IoT devices.

SLIGHT VARIATIONS during fabrication make each chip slightly different from the next. This is a headache for chip designers, who must ensure that chips all behave the same. But security specialists rejoice: they can exploit the chip variation flaw to stamp each chip with a unique fingerprint. And with these fingerprints, chips can authenticate and generate encryption keys in a more secure way, making connected applications much safer to use.

No two chips are made alike

If your self-driving car is contacted to come and drive you to the airport, it has no way of knowing that it was contacted by the one unique smartphone that can call it. It could have been called by a copy. So here is a security issue: people can be identified uniquely, electronic applications not (yet). People have fingerprints and other biometric characteristics that are unique, that you can measure easily, and that are very hard to duplicate. Not so for the growing number of connected intelligent applications such as self-driving cars, drones, IoT sensors … In the electronic world, it is much harder to distinguish the real from the fake.

Ingrid Verbauwhede, Leads the embedded systems and hardware group at imec, COSIC, KU Leuven

One solution that comes to mind, an easy and cheap way out, would be to use unique fabrication identifiers for each chip. When the chip is contacted by an application – 'challenged' in security parlance – it will send a unique response that is derived from that identifier (or a cryptographic key derived from that identifier). The application then checks if the response is a valid one. If so, it will hence trust the chip.

But this is far from secure, because it is e.g. possible to have a second, rogue chip use the same identifier. What we need is something that uniquely and physically identifies one chip and no other.

Enter physically unclonable functions (PUFs), or the equivalent of a human fingerprint. They are made possible because, during the chip's fabrication, countless random variations compound to give each chip unique characteristics.

On the nanoscale, it is simply not possible to fabricate two chips that are identical. Researchers have long been thinking about how they could profit from this uniqueness and derive an identifier that when used, can unequivocally identify a chip. The result has been a whole range of proposals for PUFs, each with their strength and weaknesses.

For imec, PUFs are a natural extension of the research in process variability and its mitigation. "With shrinking dimensions, the relative importance of variability on a chip's performance is growing. And our experts have amassed world-class expertise in how to mitigate these effects," says Thomas Kallstenius, Program Director Security and Distributed Trust at imec.

"With the recent expansion of imec, we now also have an R&D group that has a world reputation in hardware security. They had all the knowledge about PUFs but lacked the fabrication capability and variability expertise. Together, we can now work on all aspects of providing chips with fingerprints."

What an ideal fingerprint would look like

"What we are looking for is a chip identity not based on a program that is installed in the circuits, but on the physical characteristics of that chip. That identity should be unique and impossible to copy, not because it is protected by passwords and cryptography but because it is based on random, uncontrollable physics that are impossible to fabricate twice," says Ingrid Verbauwhede, who leads the embedded systems and hardware group at imec – COSIC – KU Leuven.

Some examples of PUFs that have been proposed and tried are e.g. arbiter PUFs, ring oscillator PUFs or SRAM PUFs. The latter e.g. rely on the fact that an SRAM cell powers up to 0 or 1 depending on its nanofabrication characteristics. So, reading out a chip's SRAM bank after power up is a good basis for a unique fingerprint. Ingrid Verbauwhede: "Each of the PUFs that have been proposed have their advantages and disadvantages. Some cost more, e.g., because you need additional circuits. Other have a fingerprint that will change over time, and for others the security community has already found security flaws. And that is why we're still looking for new methods of creating PUFs, e.g. making use not of circuits but of the characteristics of transistors in the latest technology nodes."

An ideal chip fingerprint should be easy to evaluate and stable. This means that it doesn't cost the chip much time and energy to use its fingerprint, and that the fingerprint will not change over time. Moreover, it should be unique for that chip and near impossible to physically clone in another chip. Also, it should be unpredictable from all the responses (or keys) that the chip divulges. Last, in the ideal

case it should be tamper resistant: if someone tries to physically unlock the chip, this should destroy or change the fingerprint.

Ingrid Verbauwhede: "Such a chip fingerprint can basically be used in two ways. One is as a very lightweight way to authenticate the chip, to make sure that this is the correct chip. You send it a challenge and it gives you the response. You then check this response against your database of all legitimate responses. That database has been made beforehand and should of course be kept protected. And – very important – each challenge should only be used once, because otherwise a hacker could listen in, record the challenge/response pairs and use them to hack the chip."

"A second application of chip fingerprints is to use them as basis to generate cryptographic keys. This is a bit more complicated, and you'll need some additional algorithms and helper data to make the keys 100% secure. But the result is effectively a key that is derived from the chip's random properties and not from some stored secret or physical process that can be wiretapped."

A second application of chip fingerprints is to use them as basis to generate cryptographic keys. This is a bit more complicated, and you'll need some additional algorithms and helper data to make the keys 100% secure

A fingerprint based on deeply-scaled transistors

Dimitri Linten is R&D manager at imec's reliability team. With his colleagues, he has been studying the variations in FinFET fabrication, and is now examining how these could be used to create a new PUF.

"Given the problems with some of the other PUFs, we especially looked for a fingerprint that would require no additional circuits or processing and that would remain stable during the chip's lifetime." The new method they came up with uses the intrinsic randomness of the positions at which the gate oxide goes into soft-breakdown. The oxide layer at the gate has been made extremely thin. Over time, with voltage being applied repeatedly, random defects will accumulate in the gate oxide. At a certain point, these defects create a percolation leakage path through the gate. "At that point," says Dimitri Linten, "the transistor can no longer serve its purpose, it has gone into soft breakdown. But what we are interested in is that the location of the percolation path in the gate will be randomly distributed between source and drain, and their position can be measured."

"Of course, oxide breakdowns are an ageing effect. We want to keep a chip healthy for as long as possible and mitigate or delay this ageing breakdown effect as much as possible. But we could reserve a circuit where we can intentionally apply a high voltage to force the gates to form soft-breakdown paths. So, we force part of the chip to age very fast and as a side-effect give us a random fingerprint. And compared to e.g. fingerprints based on SRAMs, this PUF allows a more robust readout, meaning that there is less error correction and post processing needed."

The way that this PUF is constructed, by way of a momentanous ageing, offers an additional security advantage. Most other PUFs are created during the production process itself and can thus be read out by the chip producer. This poses a security risk, because a third party could become aware of the secret identifier. But with the oxide breakdown applied by imec, the PUF is activated at a later stage, by the application builder (e.g. a car engineer) or even by the end-user. In this case, no other party will know the chip's true identity.

Comprehensive hardware security

A lot of research and work is still needed before this PUF can be used in commercial chips, but the researchers see a wide variety of use cases, e.g. in the chips that make up the wireless control networks of cars, industrial machinery or medical equipment. Says Thomas Kallstenius: "Such networks are especially vulnerable. They employ many small connected processors that rely on each other to perform the right actions. It's thus a key issue that they are able to authenticate and trust each other in the most secure way possible, and that is through hardware security."

The work on oxide breakdown PUFs is supported in part by the European Commission through the Horizon 2020 research and innovation program under grant agreement No 644052 HECTOR.

Innovations in plasma-resistant elastomer sealing for semiconductor processes

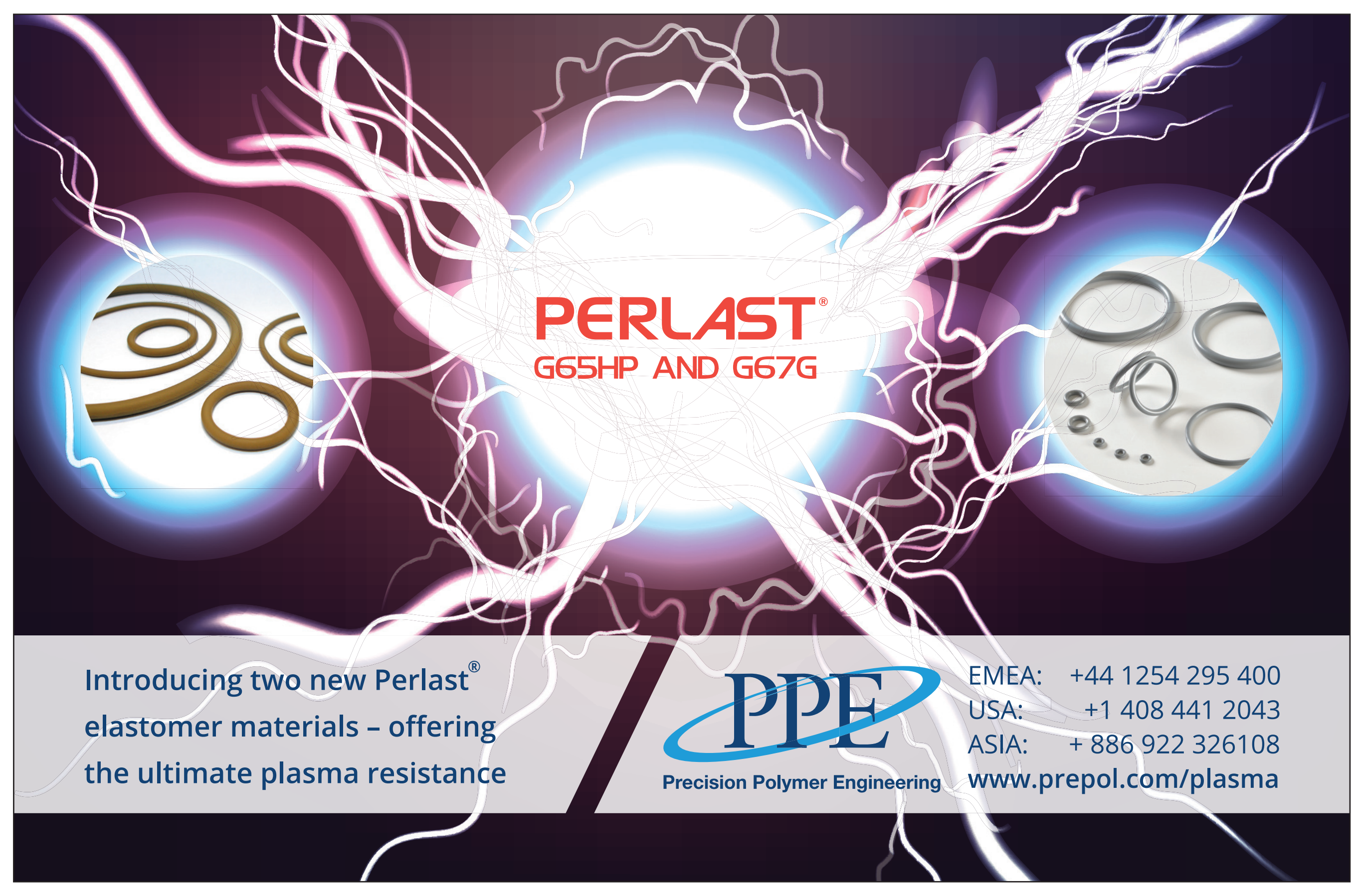
SEMICONDUCTOR processes present some of the most aggressive operating environments for elastomer seals. This chemical aggression is particularly prominent in plasma processes, especially radical based plasmas, including remote NF_3 etching and chamber cleans using remote plasma sources (RPS). The impact of plasma erosion on elastomeric components cannot be understated in an industry where product purity is paramount. While degradation of seals through plasma exposure cannot be prevented altogether, recent material innovations have allowed fabs and OEMs to lower their cost of consumables by extending their Preventative Maintenance (PM) cycles and improving yields by minimising particle generation.

Continued development work with perfluoroelastomers (FFKMs) has been one of the most fruitful areas of research. FFKM seals are required in the most critical of applications, where high temperature stability, chemical resistance and the lowest possible levels of process contamination are the most important factors. An outcome of this FFKM research from the labs at Precision Polymer Engineering is the development of two new materials; Perlast® G65HP and Perlast® G67G. Both materials boast low trace metal content, which reduces the risk of lower yield and warranty failures. But aside from the common advantages, there are also distinct benefits from each of these new materials.

Perlast® G65HP has a unique organic formulation which has excellent resistance to radical rich fluorine based plasmas and provides minimum risk of particle generation. With fewer than 10k parts per billion trace metals, this material is ideal for manufacturers of devices at advanced technology nodes, and those manufacturers wishing to ensure the integrity of device electrical specifications and minimal reliability failures.

Perlast® G67G has been formulated to deliver excellent resistance to aggressive oxygen, chlorine and fluorine-based plasmas. Additionally, Perlast® G67G is developed using low levels of advanced nano-particle fillers to minimise particle contamination. The plasma resistance of this material is maximised by dispersing individual nano-particles perfectly in the polymer matrix, meaning that particle agglomeration or large particle contamination are far less likely.

With ever more resilient semiconductor material grades, sealing developers and manufacturers can confidently solve sealing problems associated with the miniaturization of the chip market across a range of critical applications. Aggressive plasma chemistries will always be a major challenge, but improvements in sealing and material technology will continue to give OEMs and fabs notably lower erosion rates with minimum chance of contamination.



Reno Sub-Systems

sets pace in plasma process control

Unconventional startup Reno Sub-Systems demonstrates that its performance advances in plasma process control is winning over global semiconductor manufacturers. By Mark Andrews, Technical Editor.

RENO SUB-SYSTEMS isn't a typical startup. The company's executive officers and senior staff bear no resemblance to the cast of HBO's 'Silicon Valley.' Their offices are in Nevada, not someone's San Jose, California garage. And they are changing plasma processing tools in a big way.

Being somewhat atypical fits Reno Sub-Systems. The company's founders and pivotal executives have brought more than a 120 years of industry experience and pockets full of patents to the game. Reno has captured the investment confidence of Intel, Lam Research, Samsung and an impressive collection of other top tier industry notables.

Reno has managed in two years to shake up the rather staid RF power, match and gas flow segments of the plasma world that serves atomic level deposition/etch (ALD/ALE) and related processes including PELAD, PECVD for memory and logic circuits. Their products have already sold to nearly 80 percent of the industry's largest manufacturers, which most would find amazing for a company that shipped its first customer orders a bit more than 18 months ago.

The Reno team just might be on to something.

Reno Sub-Systems was co-founded in 2014 by Dr. Imran Bhutta, now CTO of RF products; and Chris Davis, senior vice president of sales and marketing. Together they bring more than 50 years industry experience focused on RF power, gas flow tech, automation, filtration and other key enablers of sub-system performance. They came to Reno after developing semiconductor subsystems for years, leveraging the multiple patents that they hold. CEO Bob MacKnight joined the group in April 2015, bringing over four decades of semiconductor industry experience to the group. Much of MacKnight's earlier years were spent helping young companies grow in highly competitive tech markets.

As sales and marketing chief Chris Davis explained, Reno's founders started the company from positions at the forefront of their fields. They realized that there was an opportunity to rethink key sub-systems in ways that could radically improve performance, but more importantly, that overcome some of the challenges to extending Moore's law through innovation. They used their networks and experience to meet early with several OEM chip makers and equipment suppliers to

Reno Precis microwave generator

size-up interests in new technology. The reaction to Reno's approach was extremely positive, noted Davis, and when the company concluded its Series A funding round in late 2014 backers included Intel's venture capital group, Innovacorp and a major unnamed OEM. 2015 and 2016 were focused on product development and securing design wins for both gas flow control and RF power / match technologies.

Davis and CEO Bob MacKnight explained that once early funding was secured, the company dove into the challenging tasks of building a company from the ground up. Even when working with highly experienced staff, a great many things can challenge the process even as front-facing personnel reached out to build relationships for Reno throughout the supply chain. As many failed startups can attest, having a good idea is not a guarantee of success. While semiconductor manufacturing creates amazing product innovations, the nuts-and-bolts of process technology evolves slowly since high yields and superior efficiency depend on well understood, time-tested practices.

"The thing about RF power in 2014 is that nothing significant had changed for years," remarked MacKnight in discussing Reno's early days. "The OEMs and ODMs were used to certain performance factors; processes were finely tuned around existing sub-system capabilities. Then along comes Reno with big promises to substantially change plasma processing… There is always skepticism until promises turn into actual hardware."

In September 2017, following a successful Series C funding round, MacKnight explained how far they had come in a short while, "Leveraging its patented technologies, Reno has now successfully demonstrated the highest performance radio frequency (RF) matching networks, RF power generators and gas delivery systems for leading-edge nanoscale manufacturing processes. Reno has generated strong customer demand based upon on-tool performance data, which has allowed the company to transition from technology and product development to high-volume adoption within two years," he said.

Reno Sub-Systems' main focus is on two critical areas supporting ALD and ALE: RF power paired with critical RF matching network components, and extremely precise gas flow management systems for plasma process chambers. Deposition and etch have long been used at various semiconductor nodes or for specialized applications, but new device generations are demanding more widespread use of atomic-scale techniques.

Each generation brings smaller device structures that challenge designers and process engineers to accommodate tighter tolerances and finer pitch.

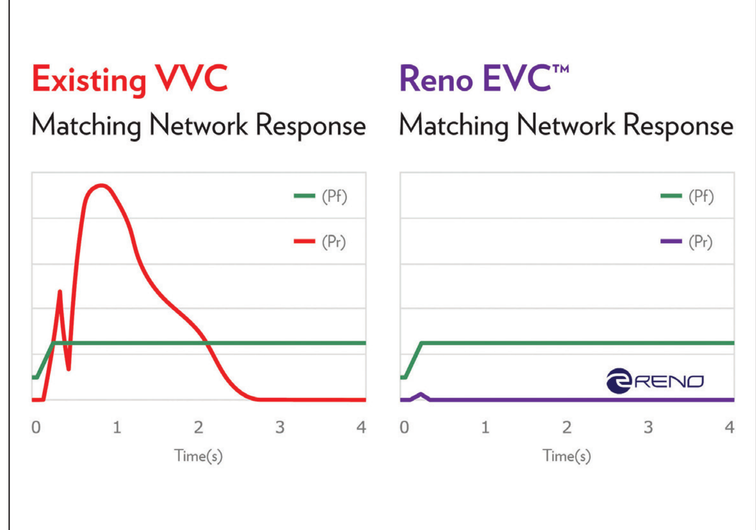


Figure 1: Reno Sub-System plasma etch data show that the company's EVC technology has reduced a 10 second plasma process to ~8 seconds, a 20% throughput improvement.

While older plasma process tools met customer needs, Reno appreciated that requirements were fast changing as manufacturers moved inexorably towards devices below 10nm with 3D structures.

A measurable difference

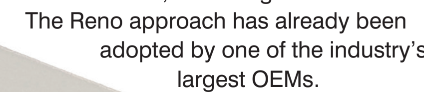
Plasma processing – either for deposition or etch – is critical for device fabrication below 10nm. Any new solution needs to be repeatable, predictable and controllable. Among key factors are shorter cycle times combined with the ability to achieve process stability in the shortest time possible. Legacy technologies required around 30 seconds to achieve RF match, stabilize gas flow and complete the step. The Reno Sub-System approach focuses on reducing the overall process to 10 seconds or less, with RF match and gas stabilisation takingf less than 50µs.

> Leveraging its patented technologies, Reno has now successfully demonstrated the highest performance radio frequency (RF) matching networks, RF power generators and gas delivery systems for leading-edge nanoscale manufacturing processes

Reno calls their plasma process control system Velocity. Its key advantage is the Electronically Variable Capacitor (EVC) that replaces legacy Vacuum Variable Capacitors (VVC). The solid-state technology employed by Reno's EVC can generate power more quickly and since a solid-state system is intrinsically more precise / less susceptible to failure it also provides greater repeatability and fewer maintenance concerns including down-time. In the company's latest tests (See Figure 1) the EVC has reduced a 10-second process to approximately eight seconds – a 20 percent improvement.

This is possible through the very fast matching phase, reduced from one to three seconds in a VVC-based system to 500μs (0.0005 seconds) using an EVC, roughly 2,000 times faster.

"With IDMs, process times need to continue to shrink from tens of seconds to two or three seconds, or less; the technology that is best suited to achieve that goal is with an EVC match," MacKnight remarked. The Reno approach has already been adopted by one of the industry's largest OEMs.



While Reno's Velocity RF matching system could improve performance by itself, when paired with a new type of RF generator its potential could be optimized, the goal when Reno announced its Precis solid-state RF generator portfolio. The latest Precis addition came in July with its newest generator delivering 1.6kW output at 2.45GHz. The company said it believes the Precis is the highest power microwave generator available for plasma applications in semiconductor manufacturing. The key advantage for Reno's microwave generators is an all solid-state design, which replaces the magnetron typically used in other RF/plasma systems.

Reno FlowNode Series

"For the first time in decades, subsystems are enabling new processes and future device generations. The ultimate validation of our technology is that 80 percent of the top semiconductor device manufacturers and equipment makers have ordered Reno products," MacKnight said. The Precis microwave generator delivers accurate, repeatable and stable micro-second ramp times using a highly reliable solid-state architecture. Its microwave power control offers significantly better frequency control than comparable magnetron-based generators.

Eliminating magnetron technology from the system is also expected to reduce maintenance requirements, which improves cost of ownership. Precis generators are the latest addition to Reno's highly differentiated Velocity Series with EVC matching networks supporting power needs from 500W to 4.5kW and frequencies from 500 KHz to 40 MHz.

Plasma processing time is also heavily affected by a manufacturer's choice of gas flow systems. The Reno approach, called FlowNode, offers advancements including much faster response times averaging 50μs. It also provides greater dynamic range, more precise accuracy and greater repeatability. The system also eliminates pneumatic delays thanks to removing the bulky mass flow controller (MFC) from the system. Collectively, the Reno tool substantially reduces component size, which MacKnight described as, "…a 7 MFC equivalent, but in a four-gas-stick footprint."

Perhaps more important than size reduction is the increased performance that is proving to be a key differentiator for manufacturers. Like its RF power and matching network solutions, speed plays a major role is gas management, too.

"Reno's FlowNode technology eliminates historic mass flow limitations by eradicating upstream and downstream pressure sensitivity, resulting in (more) stable gas delivery and better process control. FlowNode operates with near-zero internal volume at the diaphragm of the valves, which enables accurate, repeatable, industry leading ultra-low flows for advanced etch and PEALD applications.

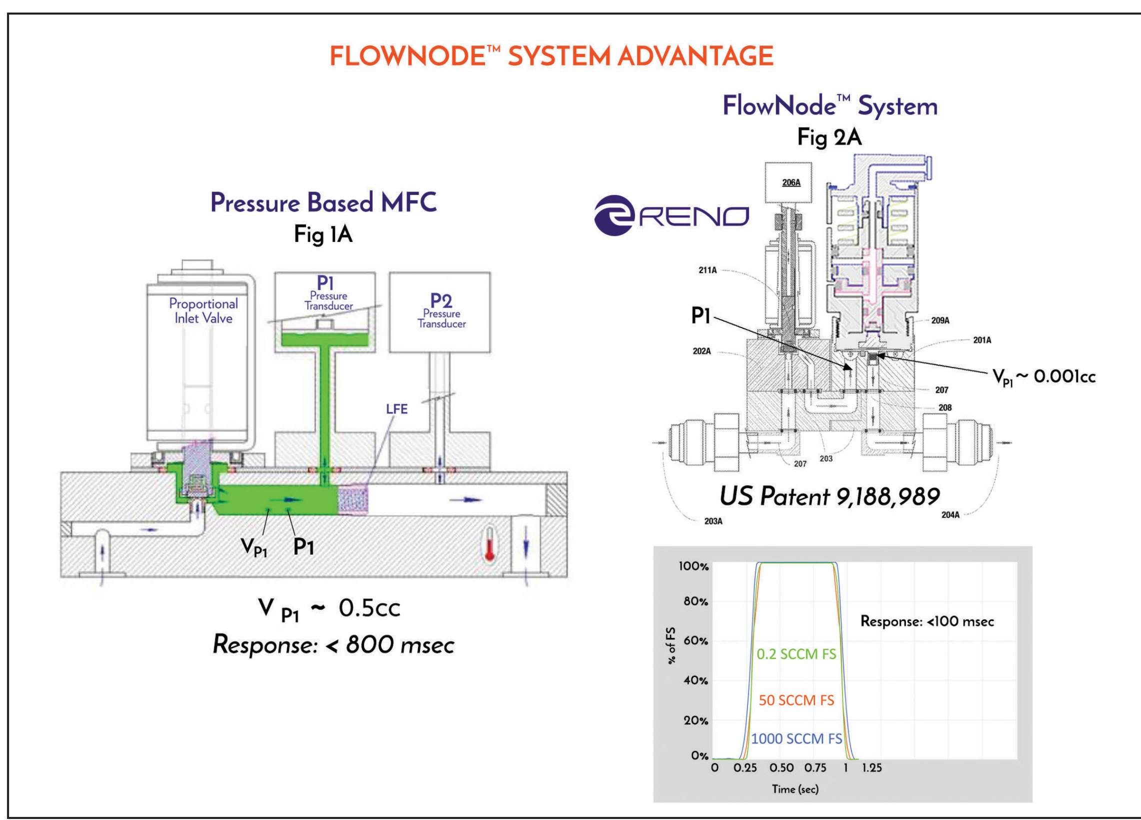


Figure 2: The Reno FlowNode system eliminates the mass flow controller (MFC), significantly reducing gas volumes and pneumatic delays, taking volume in the P1 assembly from 0.5cc to 0.001cc and reducing response time from under 800µs to less than 100µs.

Finally, multiple FlowNode elements can be put next to each other, enabling the widest flow ranges achievable today and reducing the traditional gas box footprint," MacKnight explained. (See Figure 2)

"Many MFCs have insensitivity to upstream pressure changes. However, none except Reno's FlowNode system is insensitive to both upstream and downstream pressure changes. This provides more stable continuous flows, even when there are perturbations induced by other systems turning on and off that feed back to the existing gas flow systems from the main line manifold."

"Due to FlowNode's modular design, we can share valves for multiple functions and eliminate redundant sticks," he explained. "It has been a part of (historic) MFC evolution to go from thermal MFC to pressure-based MFCs. While a pressure-based system greatly improved gas flow control over its thermal MFC predecessor, our FlowNode system is 100 times more stable and repeatable than either of these technologies. This improvement is very important at smaller geometries, where gas stability becomes more critical."

Following Reno's announcement of new products in July, the company sought further investment to expand its product line, serve the global manufacturing base and continue advanced research into new devices and product enhancement.

The company raised (USD) $11.2 million during its Series C funding round; investors were led by Samsung Venture Investment Corp., Hitachi High-Technologies Corporation and SK Hynix. Existing investors Intel Capital, Lam Research and MKS Instruments also participated in the September 2017 funding round.

Although Reno has seen a meteoric revenue increase (10 times larger than in 2016,) no company succeeds by resting on its laurels. While Reno has already sold systems to many of the industry's largest manufacturers, great opportunity remains, including developing new plasma process tools that meet specific needs for various applications.

"We collaborate with our customers to understand future requirements, and we are actively developing modifications to our existing designs—as well as new methodologies—to address their future needs. We are also designing additional, innovative solid-state-technology RF match and power products, and we are adding new flow features for enhanced gas flow control capabilities," MacKnight said.

Flexible hybrid electronics: a new paradigm for semiconductors

As printed electronic circuits continue to evolve, the NextFlex consortium promotes a hybrid approach to accelerate the development and commercial viability of flexible ICs and systems.

By: Paul Semenza, Director of Commercialization, NextFlex.

The limitations of rigid electronics

The fundamentals of electronics manufacturing – packaged semiconductors and other components assembled onto printed circuit boards produced in high-temperature processes – have not changed for decades. This process results in durable, reliable systems and is widely available from numerous suppliers. The process is well suited for computing- and memory-intensive applications such as servers, communications systems, industrial process equipment and other installed systems.

As interest has increased in devices for Internet of Things (IoT) applications, the limitations of established approaches have become apparent. Many IoT devices must necessarily be thin and lightweight, and often must be flexible (to accommodate movement of the body or of systems) or conformable (to blend into curved structures). Packaged components on rigid circuit boards are not able to meet these requirements. Manufacturing has evolved somewhat with the development of rigid-flex circuitry, in which flexible circuit substrates provide a backbone of wiring with rigid multilayer circuit sections built up as modules where needed. This can enable some flexibility, but does not allow for the electronics to be fully integrated into clothing or other materials, or worn directly on the body.

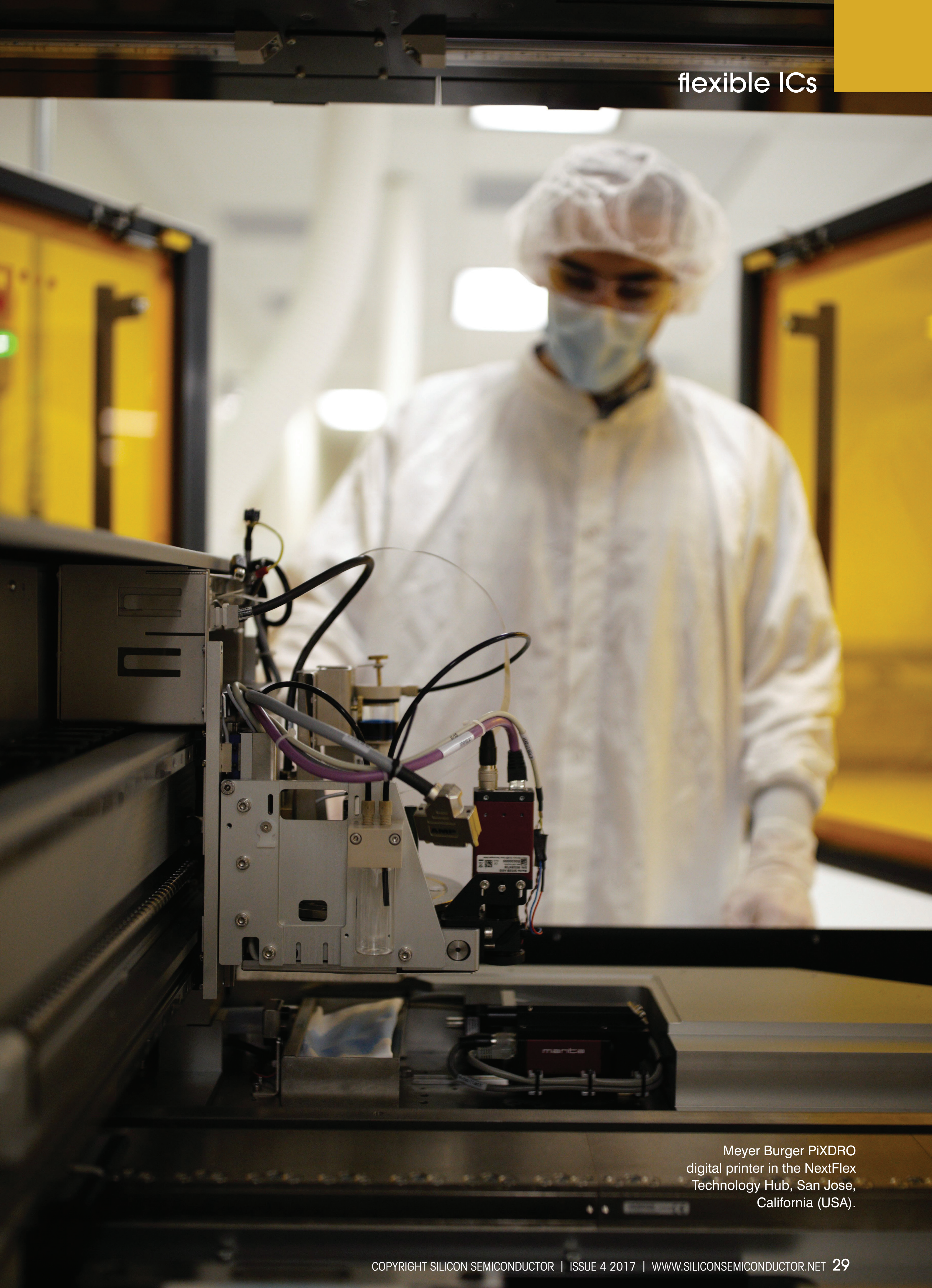
Interest in flexible electronics has led many companies and research groups to pursue printed electronics, in which interconnect, passive devices, and even semiconductors are fabricated directly onto flexible substrates. These processes enable thin, lightweight, and flexible electronic devices. However, the use of printing or other additive processes to fabricate semiconductors has proven to be very limited, lagging the density achieved by photolithography by many orders of magnitude.

Getting electronics out of the box

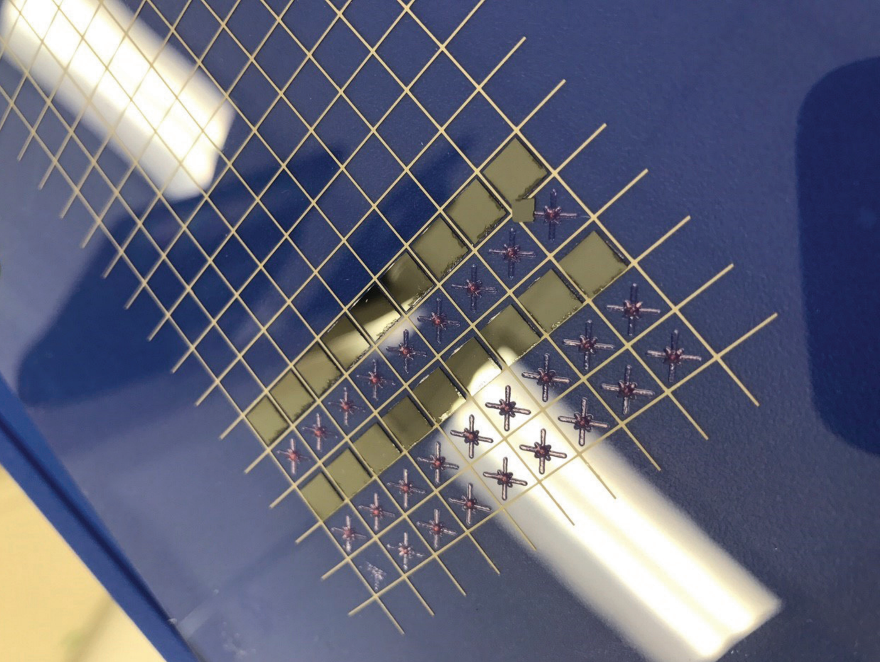
New forms of electronic manufacturing are required to create intelligent devices that can sense, take action, and communicate in real time while being integrated into the real world. Whether the operating environment is on the human body, the surface of a vehicle, precious cargo in transit, or a robotic system, these and many other environments need a new approach. Flexible hybrid electronics (FHE) is an approach that utilizes electronic printing and other additive techniques in conjunction with bare semiconductor die to create thin, flexible circuits. Starting with a flexible substrate, such as plastic or polymer film, metal foil, fabric, paper, or even thin versions of glass or ceramic, low-temperature printing and additive processes can be used to create interconnects, sensors, antennas, passive components, and some active devices. Bare semiconductor die that have been thinned (to a thickness of 50 microns or less) are then integrated into the printed circuitry and the system is encapsulated.

The FHE approach provides significant benefits. Because it utilizes semiconductor devices, it enables system performance equivalent to rigid PCB-based solutions that purely printed electronics approaches are not able to achieve. At the same time, the combination of flexible substrates, printing, and thinned semiconductor devices results in system form factors that can be bent, flexed, stretched and conformed to non-planar surfaces.

What does this mean for the silicon supply chain? The FHE approach creates opportunities for semiconductor device and electronics manufacturers



Meyer Burger PiXDRO digital printer in the NextFlex Technology Hub, San Jose, California (USA).



Thin die being attached to flexible substrates at NextFlex

to address emerging applications that cannot be satisfied by existing assembly approaches. New products envisioned for human performance monitoring, patient monitoring, structural monitoring, preventative maintenance, asset tracking, integrated array antennas, soft robotics, and assistive technologies such as exoskeletons will not be possible using packaged semiconductors on printed circuit boards. By embracing FHE manufacturing, supply chain participants will be able to build new lines of business.

Because FHE processes are low temperature and additive in nature, manufacturing and assembly capabilities can be built as needed, and importantly, where they are needed. Also, FHE manufacturing can be scaled from prototyping to volume manufacturing as needed. Small-scale investments can enable rapid prototyping capabilities, while larger investments will enable manufacturing close to customers and markets.

Taking advantage of the potential of FHE manufacturing will require changes to the semiconductor supply chain. The existing supply chain is built on the assumption that almost all semiconductor devices are packaged and assembled onto circuit boards. The development of FHE manufacturing requires that bare semiconductor die, in many cases thinned to 50 microns or less, are available for assembly.

Equipment and processes for thinning wafers up to 300 mm are available, but in most cases this equipment is embedded in a supply chain that involves thinning, singulation, and packaging. To take advantage of the new markets enabled by FHE manufacturing, semiconductor device manufacturers will need to either develop or support a sales and distribution network for thin die, or to sell fully manufactured wafers directly to FHE manufacturers, who would then thin wafers, singulating them into die.

Another area of opportunity will be in assembly equipment. Unlike surface-mount technology, in which packaged components are soldered to circuit boards at high temperatures, FHE assembly involves placement and attachment of thin, bare semiconductor die (and possibly other components) onto thin sheets of polymers or other materials at low temperature. This requires specialized handling and bonding techniques not widely available now.

NextFlex: enabling FHE manufacturing through collaboration

Many of the fundamental materials and technologies for FHE, such as thin substrates, high-resolution printing, and bare die assembly, already exist in some form. What has been missing is an effort to integrate these disparate technologies, demonstrate their feasibility, and create the standard processes, design rules, and other underlying capabilities required for a robust supply chain. This drove the creation of NextFlex in 2015, under a contract with the Department of Defense, to serve as a catalyst for the development of a flexible hybrid electronics manufacturing ecosystem in the United States.

By bringing together dozens of companies, universities, research centers, and government agencies into a public-private collaborative research consortium, NextFlex has created a forum to tackle common FHE industry challenges. In just over two years of operation, over 80 industry, academic, and non-profit organizations have joined NextFlex as members, which enables them to participate in and share results of research projects.

NextFlex members create roadmaps for manufacturing processes and application needs and identify key performance gaps, which are then addressed through collaborative research projects funded by NextFlex, with cost sharing by the project team and other organizations. Currently there are 24 ongoing projects, funded at $45 million (including NextFlex funding and cost sharing), and is in the process of selecting a third round of projects. Sample current NextFlex funded projects in human health and performance monitoring include: Flexible Smart Wound Dressing; Flexible Oral Biochemistry Sensing, and Attaching Ultra-thin ICs onto Printed Flexible Substrates for Wearables.

To facilitate project work and technology development, NextFlex has constructed a pilot manufacturing and prototyping facility in San Jose, CA, which also serves as a testbed for ongoing and completed collaborative projects. Finally, NextFlex conducts education and workforce development activities, to draw K-12 and college students into FHE manufacturing, and to support U.S.-based manufacturers needs for a trained manufacturing workforce.

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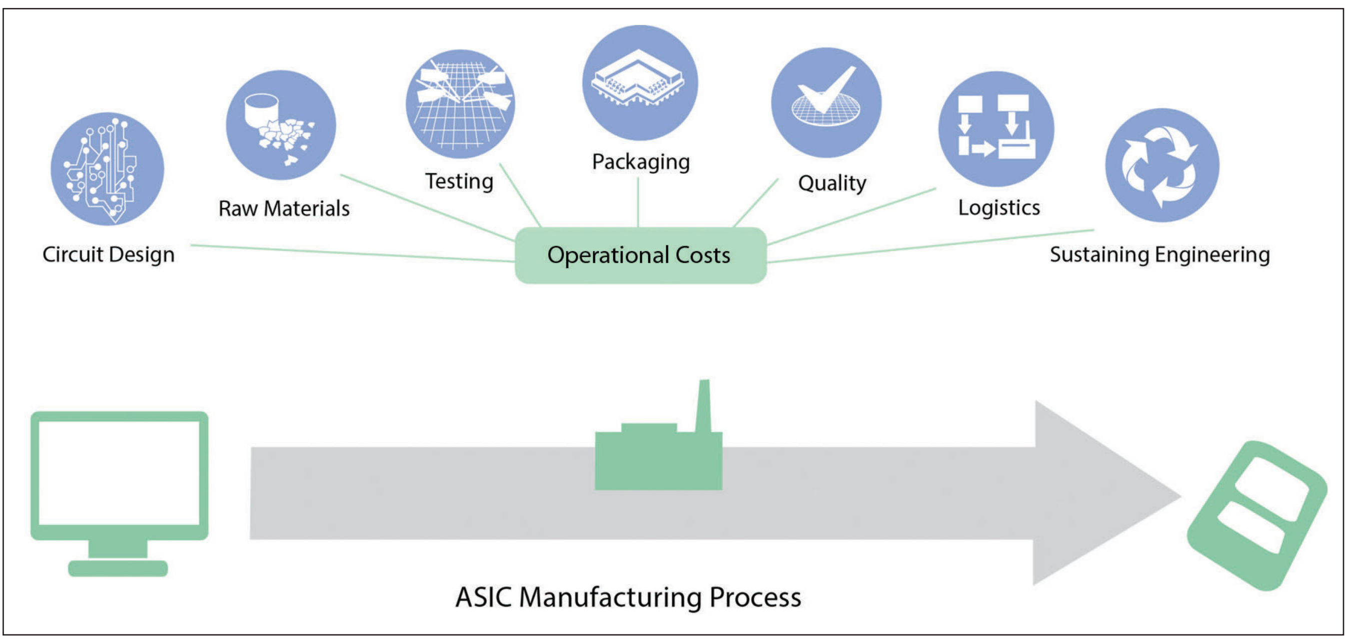
Speed IoT product development and reduce risk with outsourced operations

New manufacturing techniques and device-level security measures can bring secure Internet of Things (IoT) devices to market more rapidly than ever before. Michel Villemain, CEO, Presto Engineering, Inc.

APPLICATION SPECIFIC integrated circuits (ASICs) are cheaper and easier to make than ever before, and the range of applications for which they offer significant benefits is expanding rapidly, especially with the emergence and growth of the Internet of Things (IoT). While it is now quite possible to bring a new ASIC to market for less than $5 million dollars (USD), the complexity of manufacturing silicon products remains daunting for many potential product developers. Producing an ASIC requires expertise in many different disciplines. In large companies these needs are typically met by a team of experts, but assembling such a team can be prohibitively costly and time-consuming. This need for manufacturing expertise has led to the creation of "outsourced operations" companies like Presto Engineering that provide turn key services to manage the entire production process, from tape-out of the final design to the delivery of the finished, tested product.

By reducing the risk, cost, time and difficulty of the process, these companies are playing a key role in accelerating the proliferation of application-specific semiconductor solutions.



Manufacturing complexity

The wafer fabrication processes alone are arguably the most complex manufacturing process ever conceived. And wafer fab does not include additional aspects of the overall production process, such as qualification, the procurement of raw materials, testing, packaging, logistics, quality assurance, and sustaining engineering.

Complexity can be considered another aspect of cost – as it impacts both the cost of execution and the potential cost of execution errors. Just finding the right experts can take considerable time, but proceeding without them risks delay or failure in production. In either case, the promised return on a large development investment can evaporate quickly if a delay enables the competition to be first to market.

The electronics market waits for no one

Being first to market with a new product allows the manufacturer to collect a price premium and capture market share. Historically, leading semiconductor companies have built their success on being first to market with the latest performance-enhancing innovations, time after time. Now we are looking at a market where many of the most significant growth opportunities will be in specialized segments. These will require application specific products that will be conceived and produced by companies that are not primarily semiconductor manufacturers, but makers of cars, medical devices, smart building appliances, industrial systems, or something else no one has thought of yet. How are these product developers to confront and master the complexity of the semiconductor manufacturing process?

Large companies, like automotive manufacturers, have traditionally met the need for ASICs by creating a dedicated organization, often called an "operations" department. Starting with a completed design, their sole task is to manage the production of the specialized devices they need. Such a team necessarily includes experts in planning, purchasing, logistics, IT, quality assurance, product engineering, device engineering, failure analysis, and test engineering. For a small company, with a game-changing new product idea, the cost and time required to assemble such a team can be fatal. If a competitor beats you to market you might not get a second chance. Outsourcing operations offers an affordable, low-risk solution.

Reduce risk – by outsourcing these operations, you gain from the management and technical experience of a team of experts with well-established relationships to resource and service providers.

Get to market faster – maximize margins and return on investment by commanding premium prices. Take valuable market share and establish a strong competitive position. Avoid delays required to assemble experts for an in-house team.

Minimize start-up costs – reduce capital expenditures: the IT infrastructure alone – enterprise resource planning (ERP), manufacturing execution system (MES), disaster recovery planning (DRP), and security – needed to manage a semiconductor production operation can cost a million dollars. Outsourcing operations converts fixed costs to variable expenses, minimizes headcount and avoids the dilution of equity required to recruit top talent.

Optimize production processes – outsourced operations can match the device requirements to the best fabrication process to ensure optimal performance at the lowest cost. And after wafer fabrication, different technologies still require different skill sets. For example, radio frequency testing, especially in the millimeter wave bands that are now coming online, is still as much an art as a science, requiring specialized knowledge and, frequently, customized fixturing. Secure devices must be provisioned in secure facilities with secure communication protocols.

Outsourcing and security

As IoT products proliferate, manufacturers and the industry in general have developed a heightened awareness of the security risks inherent in any connected device. Though specific requirements do vary from application to application, ultimately, every connected device needs some level of security. Thus, product developers are faced with yet another addition to the expense and complexity of producing their devices.

A variety of security solutions exist, ranging from software-only approaches to the addition of secure "chips" and the inclusion of secure capabilities in off-the-shelf controllers or custom ASICs.

All of these solutions share a need for secure provisioning – the introduction in each device of the "secrets" essential for secure identification, authentication, communication, processing and storage. Outsourced operations for IoT products clearly must include secure provisioning.

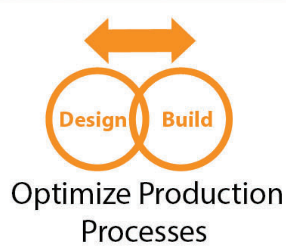
Michel Villemain, CEO, Presto Engineering, Inc.

Benefits of Outsourced Operations

Reduce Risk

Get to Market Faster

Minimize Start-up Costs



Optimize Production Processes

Important security considerations when outsourcing production for an IoT device include:

Hardware – Although software-only solutions are available, tying security to hardware adds confidence and makes intrusion more difficult. Hardware solutions include: adding a separate secure chip (Secure Element or similar technology), implementing secure capabilities included in a stock MCU, or incorporating security functionality in a custom designed ASIC. MCU and ASIC based solutions can reduce costs significantly. A key question to consider before beginning a new program: what is the most cost-effective solution given the technical and security requirements and anticipated unit volume of the application?

Trust – All hardware configurations require provisioning by a trusted partner. Indications of trust include that partner's level of investment in the owned physical plant and equipment, history and volume of secure operations, and staff experience in secure applications.

What stake does the provisioner have in maintaining a reputation for security? What investments have they made to secure that reputation? Is trust an essential component of their business model and brand equity?

Standardization EAL5+ Certification

Competitive Pricing at Low to Medium Volume*

Large Variety of Device Types**

Multiple Options at Varying Price Points

* 50K to 100K unit range
** not limited to Secure Element (SE) chip technologies

Secure and Flexible Provisioning Services

Facility – Is the provisioning facility designed for both physical and data security? Can it ramp up in volume for IoT growth?

Certification – Does the provisioner conform to industry standards including the Common Criteria for Information Technology Security Evaluation (ISO/IEC 15408)? What Evaluation Assurance Level (EAL 1-7) certification has the provider achieved? Are there regular audits and re-certifications?

Equipment – Does the provider have the equipment needed to handle the particular solution, i.e.: wafer, package, circuit board?

Flexibility – Can the provisioning process be configured to provide a cost-effective solution that meets security requirements and budgetary constraints?

Ideally, an outsourced provisioner should offer certain key capabilities:

- A standardized and certified (EAL5+) secure process.
- The ability to provision a wide range of device types, form factors and security technologies.
- Competitive pricing at low and medium volumes with the ability to scale to larger volumes as required.
- The flexibility to configure the provisioning process and infrastructure to meet varying security and budgetary requirements.

Conclusion

ASICs offer superior value and performance, especially for IoT products. The availability of less expensive fab capacity on mature process technologies has significantly reduced their cost. It is now possible to design and build an ASIC for about $5 million dollars, which increases the applications space in which they provide an economically attractive solution.

Outsourcing operations to produce ASICs manage the risks associated with the complex semiconductor manufacturing process, reducing costs, increasing value, and minimizing risk. Security and secure provisioning must be essential considerations in defining any outsourced operations solution.

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3D SoC

Improve circuit size, cost and performance by repartitioning

3D integration has evolved into economically interesting alternatives to traditional 2D design. Mieke Van Bavel, PhD, Imec Science Editor explains how 3D integration allows a significant reduction of a system's footprint and enables ever shorter and faster connections between that system's sub-components.

Mieke Van Bavel, PhD, Imec Science Editor

IN RECENT YEARS, the technology of 3D integration has evolved into economically interesting alternatives to traditional 2D design. In particular, the technology is used to package the CMOS imagers found in smartphones, the high-bandwidth DRAM memory stacks used in high-end computing and in advanced graphics cards. 3D integration allows a significant reduction of a system's footprint and enables ever shorter and faster connections between that system's sub-components.

Rather than stacking chips, it is also possible to repartition a 2D systems-on-chip (2D-SoC) design into circuit blocks, realized in separate wafers that are stacked and tightly interconnected. This is called 3D systems-on-chip (3D-SoC). By clever partitioning of the circuits, the power-performance-area can be significantly improved, providing a path to extend Moore's law scaling.

The 3D technology landscape

The continued scaling of microelectronic circuits has allowed the creation of extremely complex systems-on-chip (SoC). At the same time, several specific applications (such as high density memory, high voltage, analog signaling and sensors) have driven technology developments in various directions. In this complex landscape, on the one hand, many electronic systems still consist of a multitude of components that are packaged individually and interconnected using conventional printed circuit boards.

On the other hand, more advanced 3D integration and interconnect technologies have emerged, reducing the size of the electronic systems, and enabling faster and shorter connections between their sub-circuits. These abilities have made 3D integration one of the techniques that will allow the industry to keep pace with Moore's Law.

In this 3D technology landscape, several classes of integration can be defined. The main difference between these classes is related to the level of partitioning, in other words, the level at which the systems are 'cut' into different pieces in the interconnect hierarchy. Each of these classes requires different process schemes and 3D integration techniques, achieving progressively smaller contact pitches. A first class is what we call system-in-a-package (or SiP), where the partitioning is done at package level by stacking packaged devices on top of each other, or by integrating multiple die in a single package.

Among the technologies used to realize SiPs are package-to-package reflow and fan-out wafer level packaging, in combination with solder balls. Contact pitches of current solutions are rather coarse, in the 400 micrometer range. Imec's research into new approaches to fan-out wafer level packaging intends to increase the interconnectivity of this class of SiP by a factor 100, targeting interconnect pitches of 40 micrometer. The technique is applied (for example) for mobile applications such as smartphones.

In a second class, called 3D stacked IC or 3D-SIC, the partitioning is done at die level and individual dies are stacked on top of each other. 3D-SIC partitioning is achieved using die-to-interposer stacking or die-to-wafer stacking, where finished dies are bonded on top of a fully processed wafer. Dies are interconnected using through-Si vias and microbumps. In the industry, microbump pitches down to 40 micrometer are achieved today. Imec's research goal is to bring this pitch down, well below 20 micrometer, as such increasing the interconnectivity by one to two orders of magnitude. A typical application example is wide I/O memory, where vertically stacked DRAM chips (3D-DRAM) are connected on a Si interposer together with a logic die and an optical I/O unit.

3D systems-on-chip: higher density through heterogeneous integration

With advanced CMOS scaling, new opportunities for 3D chip integration with even higher interconnect densities and smaller pitches are possible. Rather than realizing a SoC as a single chip, it has now become possible to realize different functional partitions of a SoC circuit. Stacking such partitions results in a so-called 3D system-on-chip. These are packages in which partitions with varying functions and technologies are stacked heterogeneously, with interconnect densities below 5 micrometer. The system partitioning can be done at different levels of the interconnect hierarchy – at the global wiring level (long wires, cross chip), intermediate wiring level, or local wiring level (short wires, interconnecting e.g. intra-core modules).

The main technological approach to stack these partitions is wafer-to-wafer bonding – either through hybrid (via middle) wafer-to-wafer bonding, or with dielectric (via last) wafer-to-wafer bonding techniques. This is achieved by a highly precise alignment of top and bottom wafers that are then bonded. Recently, excellent results in wafer-to-wafer overlay accuracy have been obtained, for both hybrid bonding (1.8 micrometer pitch) and dielectric bonding (300nm overlay across wafer). Accurate overlay is needed to align the bonding pads of the stacked wafers and it is essential to achieving a high yield.

One of the main drivers for 3D-SoC development is functional repartitioning of high performance systems.

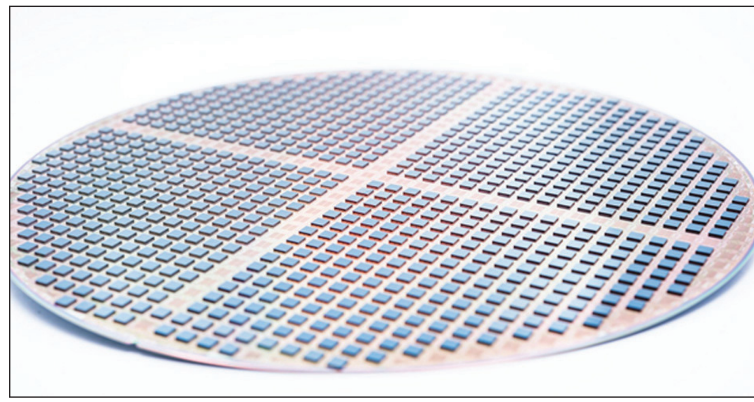


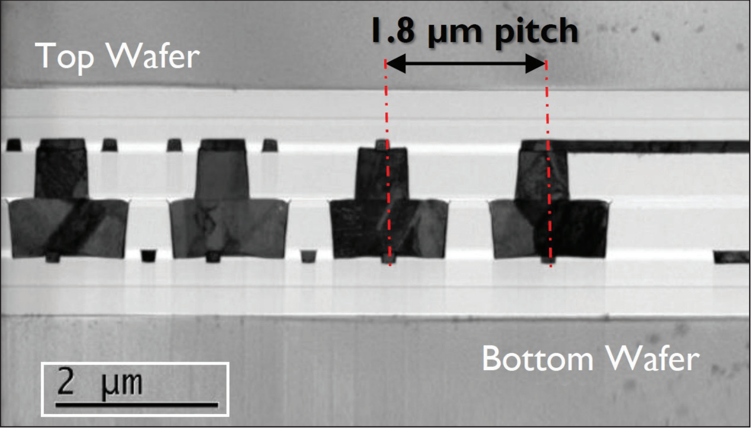
Fig 1: 3D stacked IC: processed wafer with chips stacked on top using a die-to-wafer process.

In such approach, different parts of the SoC system are realized using tailored technologies in different physical layers, but remain tightly interconnected. The trend in processor development, for example, has been towards an ever increasing number of cores. This trend will continue, enabled by scaling towards the 7nm and 5nm technology nodes. However, more cores will also need more on-chip memory. And all this will result in more overall silicon area that is needed, plus more back-end-of-line requirements, and hence, increasing wafer cost. One way to cope with this trend is by functional repartitioning of the processor followed by heterogeneous 3D integration.

Power, performance, area and cost benefits through clever partitioning

Imec researchers use physical design tools to find an optimal 3D functional partitioning of high-performance systems. A typical example is a larger SoC which consists of many cores, the L1 memories associated with these cores and L2 memory that is shared. This can be redesigned so that all the memory is brought to a top die, with the logic moved to a bottom die. This approach ends up with two die, half the size of the original big die, which improves the system's yield (defined as the percentage of good die on a wafer) which decreases as a function of the die's area. In addition to this cost and area gain, the length of the wires between the processor and the memory

Fig 2: Wafer-to-wafer bonding with 1.8 micrometer pitch overlay accuracy.



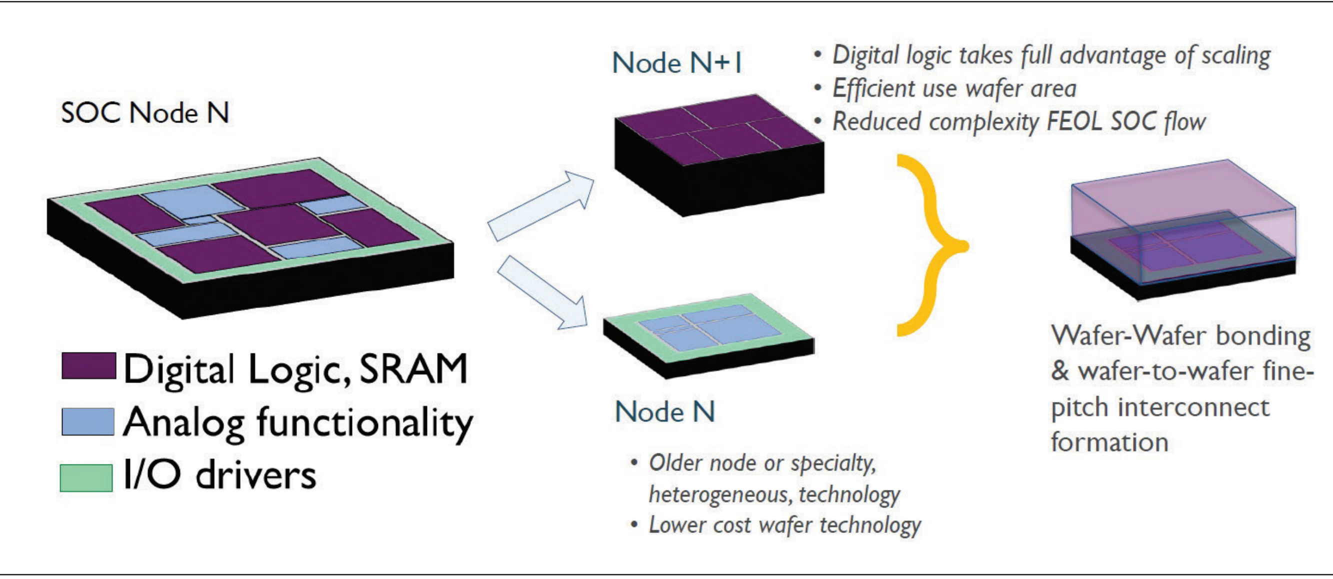


Fig 3: Illustration of 3D- SoC partitioning based on the scalability of the technologies.

becomes significantly shorter after stacking the two dies, giving additional gain in power and performance. These die-related gains are typical for anything that is 3D.

But there is more. For the original 2D die, the wafer manufacturing process needs to be optimized for both logic and memory technologies. By splitting the die into two dies, one for logic, one for memory, the processes can be tuned for logic and memory separately. And this will further improve the yield. Also, logic typically requires a large number of metal layers (typically 12 to 14), while memory typically requires fewer layers (5 or 6). This implies that the wafer containing the memory part can now be made relatively cheaply – as the back-end-of-line cost makes up a large part of the total wafer cost. Partitioning can be further revised by making even smaller functional IP blocks and by rearranging them into another shape that would further reduce the wire length.

Fig 4: Illustrating principles of multicore processor repartitioning.

The re-partitioning should, however, be done in a clever way to avoid over-partitioning. For example, if a circuit consists of sub-circuits that are extremely interconnected, ripping them apart may result in too many wires that go up and down between the two resulting dies. And that would cause more problems than repartitioning can solve.

A clever way of partitioning may be based on the scalability of the different technologies, for example. While we keep on scaling transistors according to Moore's Law, it gets more and more difficult to achieve an overall process which encompasses everything of the SoC. For these applications, partitioning in function of scalability turns out to be an interesting solution. If a technology is split into parts that highly scale (e.g. digital blocks) and parts that hardly scale (e.g. analog blocks and I/O drivers), you can optimize the die with highly scalable technologies separately from the die containing less scalable technologies.

3D Integration: A landscape and not a roadmap

3D-SoC sand 3D-ICs complete imec's 3D technology roadmap that outlines different paths for 3D integration. However, imec researchers refer to a 3D technology 'landscape' when discussing evolutionary paths instead of a 'roadmap'. A technology landscape is not like a traditional 2D roadmap that can be read from left to right. For 3D, there are a lot of technology options that will coexist, even within the same system. The technologies differ in where they intercept the hierarchy of interconnects on the chip, in other words, where we divide-up devices and create 3D interconnectivity. And this will determine the required 3D pitch. So, the future of circuit design evolution is more like a collection of technologies that allow a system to be integrated into a much smaller form factor, with increased performance and lower manufacturing cost.

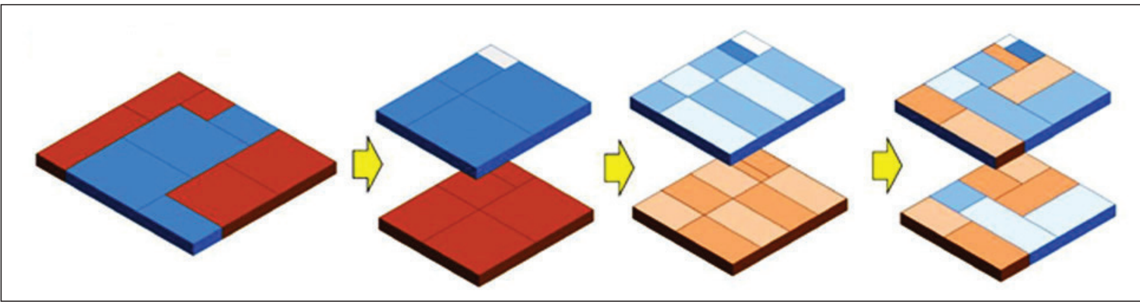


Fig 5: From a 2D- SoC (multiple large IP blocks) to a 3D-SoC (IP blocks re-arranged across two chip levels and further IP block sub-partitioning).

Further down the road: 3D-ICs

Eventually, the drive to achieve smaller, faster, higher performance ICs will lead to even tighter integration, such as stacking transistors on top of each other, achieving contact pitches as small as (a few) 100nm. Imec is exploring ways of stacking, for example, nMOS transistors on top of pMOS transistors – or vice versa – instead of putting them next to each other; this stacking approach is also known as CFET (or CMOS FET). To accomplish this involves a completely different approach not utilizing through-silicon-via-like processes; it will be realized through sequential processes or layer transfer processes. The alignment of the two transistors in a CFET should not be wafer alignment defined but lithography defined. A typical application is an SRAM cell in a 3D format, which will have a much smaller footprint than its 2D equivalent.

Another example is 3D NAND technology in which a single channel contains multiple transistors or bits (up to 58), integrated into one single structure, making the approach a few levels of granularity lower than 3D-SoC partitioning. It is one of the future paths imec is exploring that has a potential to extend Moore's law scaling.

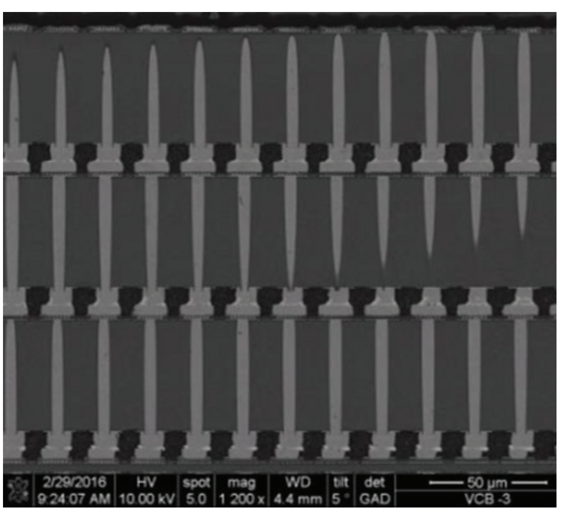


Fig 7: 3D-die stack: four die, connected vertically using 20 micrometer pitch microbumps and 5 micrometer diameter, 50 micrometer deep TSV connections.

	3D-SIP			3D-SIC	3D-SOC			3D-IC
3D Technology	"PoP"	"Chip last"	"Chip first"	Die stacking	Parallel W2W		Sequential FEOL	
3D-Wiring level	Package I/O	Chip I/O Interposer I/O	Chip I/O	Global	Semi-global	Intermediate	Local	FEOL
				Chip BEOL Wiring Hierarchy				
Partitioning	Functional unit	subsystem	Embedded die	Die	Blocks of standard cells		Standard cells	Transistors
Technology	Package-to Package reflow	Multi-die SIP 3D/2.5D stack	FO-WLP Embedded die	3D D2D, D2W 2.5D Si-interposer	Wafer-to-Wafer bonding Hybrid bonding	Via-last	Active layer transfer or deposition	
2-tier stack Schematic								
Characteristic	Solder ball Stack	• C4, Cu-pillar Si-Organic • Through-Mold-vias	• Bumpless • Si-RDL • Through-Package-vias	• µbump • Si-to-Si • Through-Silicon-Via	BEOL between 2 FEOL layers Overlay 2nd tier defined by W2W alignment/bonding		Overlay 2nd tier defined by litho scanner alignment	FEOL stack
Contact Pitch	400⇒350⇒300µm	120⇒80⇒60µm	60 ⇒40 ⇒20µm	40 ⇒20 ⇒10⇒5µm	5µm ⇒ 1 µm	2 µm ⇒ 0.5 µm	200nm ⇒ 100 nm	< 100 nm
Relative density:	1/100⇒1/77⇒1/55	1/9⇒1/4⇒1/2.3	1/2.3 ⇒ 1 ⇒ 4	1 ⇒ 4 ⇒16⇒ 64	64 ⇒ 1600	400 ⇒ 6400	4 10^4 ⇒ 1.6 10^5	> 1.6 10^5

Fig 6: Imec's 3D interconnect technology landscape.

Why ultrathin power semiconductors call for advanced inspection process control

Thin and ultrathin ICs are in high demand, but yield that sacrifices reliability has little value. Inspection process control can be the solution, according to UnitySC. By Gilles Fresquet, CEO, UnitySC.

THE DEMAND for thin and ultrathin semiconductor devices rises continuously, driven in part by explosive growth in high-performance computing, networking, automotive and industrial applications. Quite simply, thinner devices often mean a reduced footprint. But this is not the only benefit. For some applications such as power semiconductors, the thinner the dies, the better the device performance. Because of this, backside thinning processes are critical manufacturing steps. While macro-inspection is a suitable process-control approach for backside thinning in many applications, full backside wafer inspection is needed for power semiconductors. This is especially true for power devices with backside processing that includes not only thinning, but backside metallization and even backside shallow junction formation. One example is insulated-gate bipolar transistor (IGBT) devices that require final thickness less than 100μm. This article examines the importance of full wafer backside inspection for IGBT devices.

The IGBT story

While not new, the IGBT has become a popular power semiconductor device choice for a wide range of industrial power-conversion applications, due to recent technological advancements such as rugged switching characteristics, low losses and simple gate drives. These applications include strategic emerging and high-growth industries such as high-speed rail transportation, electric and hybrid vehicles, smart grids and renewable energy. The latest approaches for manufacturing IGBT devices focus on decreasing power losses and switching time. To optimize its performance, the final thickness of a power device is essential. Newer IGBT technology relies on extremely shallow p-doped backside implants to accurately control its emitter efficiency. Any excess in device thickness would result in both an increase of the forward saturation voltage and turn-off losses. Because of this, roadmaps are targeting a final device thickness between 20μm and 50μm by 2020.

Causes of backside defects in IGBTs

For most devices, backside grinding is the most popular method for reducing wafer thickness, due to its relative low cost and high speed. However, the mechanical stress and heat applied during this process can damage wafers. This potential damage needs to be carefully understood and controlled to avoid any negative performance and reliability impacts to the final devices.

An IGBT is a two-layer, bipolar device with a transistor drain that requires not only backside thinning, but also a p and n type backside-doped region formation, followed by metallization to create an active diode. As such, any occurrence of backside defects caused by wafer-thinning processes can be particularly detrimental to the end-device reliability. Compared with standard CMOS, IGBTs can incur defects not only from the thinning itself, but also from the doping process steps that follow.

Ticking time bombs

Traditional approaches to backside wafer inspection include manual microscope visual inspection, which is an unrepeatable process that relies on the perceptions of the human eye, with limited defect characteristics. It requires a specific skillset and isn't always fully accurate nor reliable.

Figure 1: UnitySC's 4See Series combines PSD and CC technology to perform nanometric wafer backside surface and edge defect inspection after thinning and metallization.

Automated optical inspection (AOI) is also used to perform macro-inspection of the wafer surface. Unfortunately, this method, even with increased magnification, is not sufficient for detecting all the defects, particularly those that occur at the nanometer level.

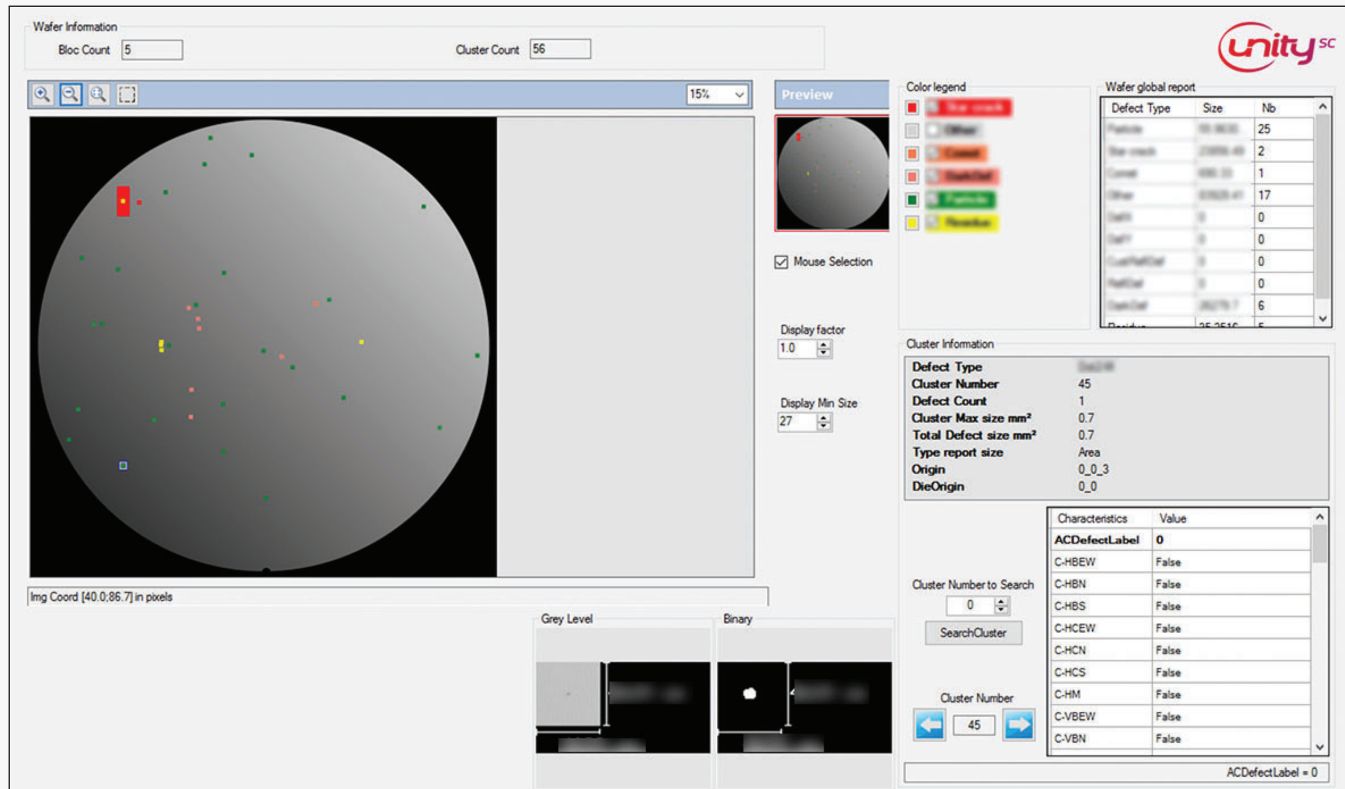
More advanced darkfield inspection might be a solution for some processes. However, due to the high roughness level following the grinding process, the haze level makes the darkfield system almost blind. Additionally, darkfield systems require a perfectly flat surface, and a chucking system is mandatory. For backside inspection, this would mean a chuck on the frontside, which is not possible due to the potential for damage and contamination to the active part of the device.

Nanometer-level defects that go undetected can be ticking time bombs because—though they will not be discovered during the final probe test for electrical reliability—they might fail down the road once they are implemented in a system. For example, in IGBT devices, crystal extrusions on a small area of the backside diode can cause it to fail, which in turn creates hotspots in the final device. This device failure could happen at the system level, due to an undetected wafer-level defect. While device failure in a smartphone is a mere inconvenience, in critical applications it can be catastrophic.

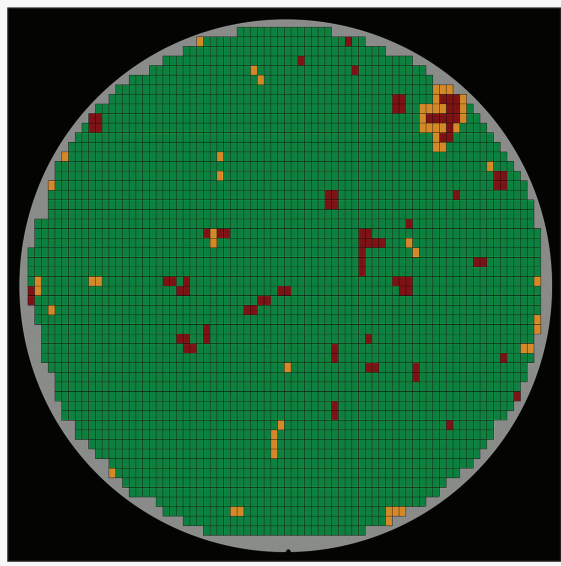
Defusing the time bomb

To address this growing need for more accurate backside wafer inspection, a new nanometric defect-detection approach has been developed that combines phase-shift deflectometry (PSD) and conformal confocal (CC) inspection technology; UnitySC's approach is unique and patented. PSD allows for the detection of topographic wafer defects that are only a few nanometers high, on both the frontside and backside surfaces. Combined with wafer reflectivity and global topography results, PSD provides a reliable method to detect defects such as scratches, cracks, stains and more.

CC technology is based on a white-light beam generated by an LED source that passes through chromatic multi-lenses to separate each wavelength in the vertical direction. It is used to perform wafer-edge inspection (top, top bevel, apex, bottom bevel and bottom) by combining high lateral resolution with a large depth of focus. CC edge inspection



Above (2a) & right (2b): Figure 2: This backside inspection defect map, shown in the top image (2a), is mirrored and combined with a frontside electrical probe test map in the bottom image (2b), to show all detected defects (red from the backside defect map; orange from the frontside electrical probe map). Every die overlapping a defect is reported as bad if it is determined to be part of the 'killer' defect class.



detects typical defects, such as chips, shells, cracks, contamination areas and more, which can propagate on the wafer.

Combining PSD and CC into one system for high-volume manufacturing (HVM) provides reliable and accurate surface topography measurement. For example, UnitySC has implemented PSD and CC technology in the Deflector and Edge modules of its 4See Series automated defect inspection platform, so that inspection can be performed all around and through the device wafer (Figure 1).

Why reliability is more important than yield

Defect detection has always been important during the technology-development phase to adjust processes so that yield is improved. In HVM, finding these defects earlier is becoming more critical to end-device reliability since high yield with low or poor quality is actually a disadvantage for manufacturers. Generating a backside defect map using a system that combines PSD and CC, and then overlaying it with a frontside electrical probe test map allows for a more accurate picture of production yield (Figure 2a & 2b). At the end of the day, it is important for fab managers, device manufacturers and end users alike to understand that, in critical applications, the reliability of the end device begins at the wafer level. With this understanding and by working to improve reliability, the added value for the fab is that the system integrator will come to rely on them for their high-quality devices, which puts them at a premium.

Conclusion

Device manufacturers are under constant pressure to increase their production yields while also minimizing product defectivity. Both objectives can be achieved by implementing a highly accurate approach to backside inspection with systems that feature nanometric defect-inspection technologies.

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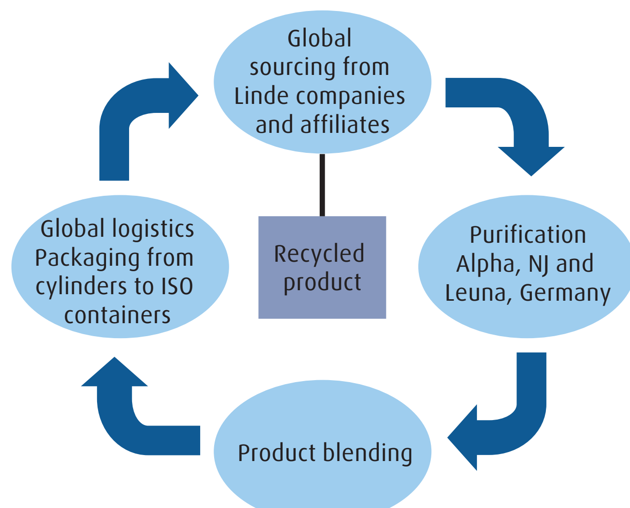

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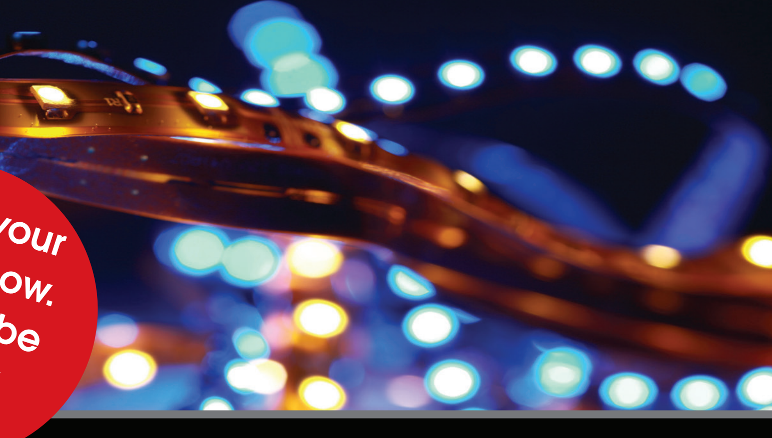

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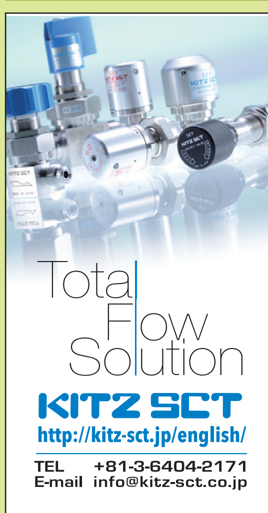

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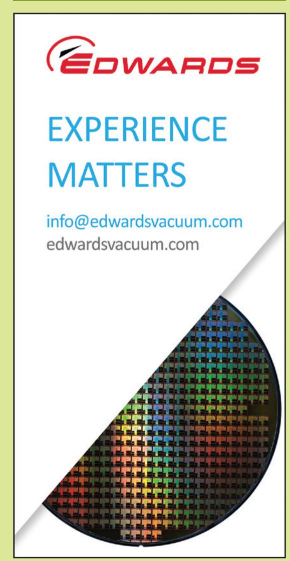

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