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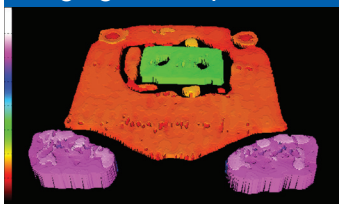
Data management for automotive electronics

X-Ray and acoustic 3D imaging of components



Silicon photonics to detect heart diseases

Trade disputes fuel supply chain worries

AI chip design platform to give industry a boost

AP&S Sets New Wafer Processing Standards

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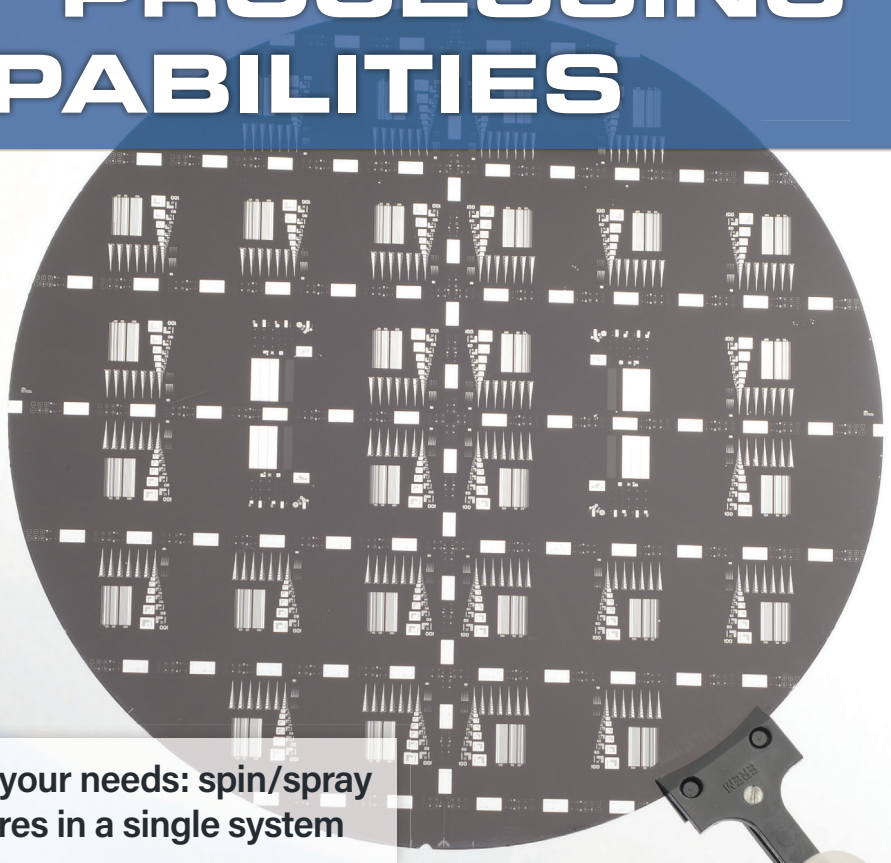

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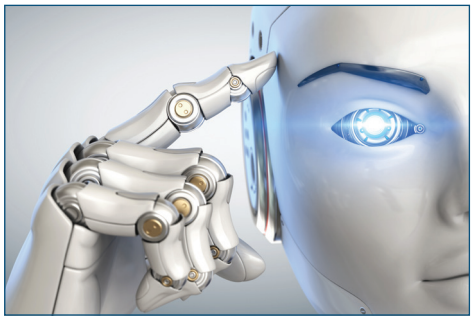
editor's view

By Mark Andrews, Technical Editor

New opportunities at SEMICON Europa 2019

SEMICON Europa convenes 12-15 November in Munich, Germany. Co-located with Productronica, the event will bring together thousands of exhibitors and attendees in a forum considered the strongest single event for European electronics manufacturers.



This year's SEMICON Europa focuses on initiatives to strengthen Europe's manufacturing base. Many leverage artificial intelligence (AI) and Industry 4.0 techniques to create new, compelling applications for the home and business. The event also looks at digitization across industries including mining and energy that have specialized needs and operating conditions.

This year's event will continue promoting Industry 4.0 automation, data analytics and related manufacturing enhancements. SEMICON will have a dedicated session on R&D and EU-funding for electronics components and systems highlighting the new European excellence initiative, ECSEL JU project MADEin4. The project brings together nearly 50 players from 10 countries working to further digitize European electronics and manufacturing through wide-ranging programmes. Other highlights include a focus on sensor fusion technologies, AI and new levels of ADAS automation on the road to achieving fully autonomous vehicles. The programme will also include highlights of initiatives within medical technology using the novel capabilities of fused sensors, MEMS devices, AI, and photonic integration to make the future of healthcare a more personalized process.

Building on highlights of this year's SEMICON Europa, Silicon Semiconductor examines the way that Industry 4.0, AI and other advancements are at the heart of more powerful process tools and systems for manufacturers. At AP&S (Donaueschingen, Germany,) the company has invested heavily to enable advances in machine operational diagnostics to maximize performance and productive uptime for customers. Even as it continues to deliver exceptional wet bench processing platforms, AP&S has also added new AI and augmented relativity capabilities from tepcon while expanding its *try-it-before-you-buy-it* machine Demo Center by adding new clean room space and advanced systems.

While the latest in wafer processing will remain a SEMICON Europa centerpiece, global manufacturers are also continuing to watch the trade dispute between the United States and China. Recent moves by both parties signal behind-the-scenes progress, yet experts at the Chartered Institute of Procurement and Supply (CIPS) point to lasting supply chain implications for global manufacturers. We also examine new innovations in device inspection techniques from Sonoscan while Rudolph Technologies delves into ways that enhanced data management is bringing new efficiencies and productivity gains to manufacturers world-wide.

See you in Munich at SEMICON Europa 2019!

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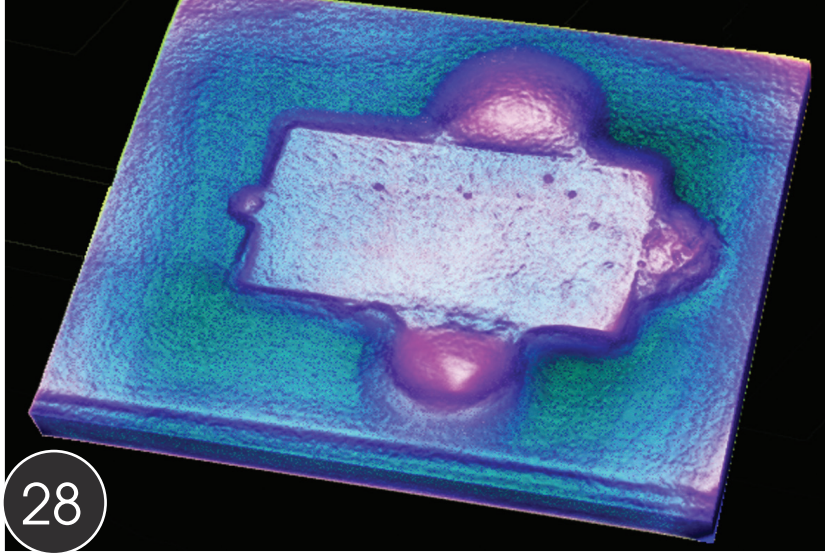

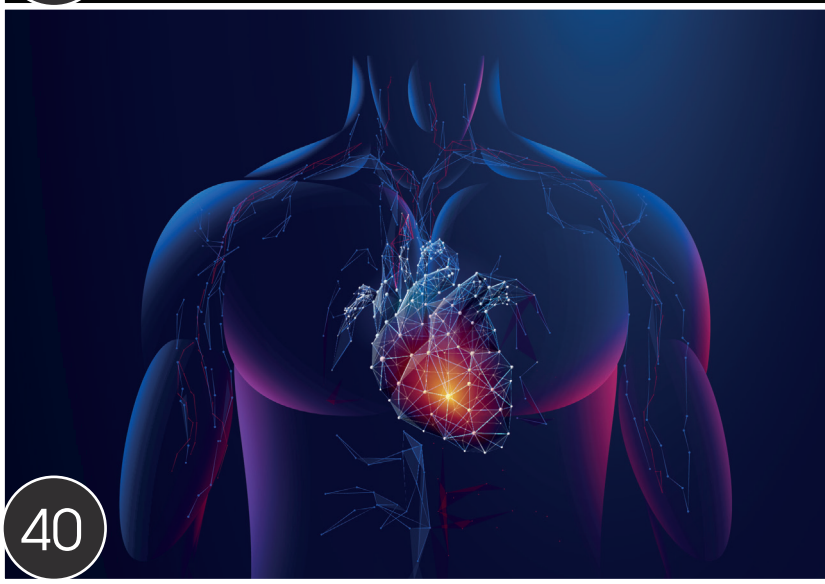

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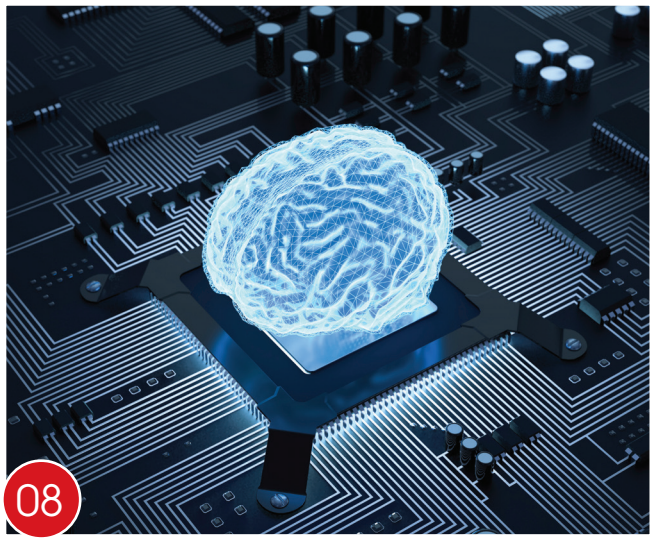


imec and KU Leuven spin-off, closes first-round funding

PULSIFY MEDICAL, a digital medical technology company focused on the development of wearable ultrasound patches, announced the first closing of its seed funding round, raising €2.6 million euro. Imec.xpand and KU Leuven led the investment together and were joined by University Hospitals Leuven. As a spin-off of imec and KU Leuven, Pulsify Medical will build on the unique and IP-protected technology of both research institutes: on the one hand, imec's unique flexible ultrasound transducer technology and design know-how for transducers, thin film transistors and system architecture, and on the other hand, KU Leuven's world-class expertise in cardiac ultrasound imaging.

Pulsify Medical was founded as Carpatchiot B.V. in June 2019 by Professor Jan D'hooge (KU Leuven, University Hospitals Leuven), Dr. Lieven Herbots (Jesse Hospital, University Hospitals Leuven), Xavier Rottenberg (imec) and Steve Stoffels (imec). Iwan Van Vijfeijken and Chris Japp are joining as CEO and independent Chairman of the Board, respectively.

Pulsify Medical brings together a very seasoned and experienced leadership team. Mr. Chris Japp, independent Chairman of the Board, is a 30 year veteran of the medical device industry, having worked around the world at large healthcare companies such as GE, Boston Scientific, Pentax Medical, and Hitachi Medical in senior leadership capacities.

He has also served on several company boards, and has a successful track record in early and mid stage company development. Chris also has extensive experience in ultrasound technology, products, and solutions in multiple clinical areas, particularly in cardiac applications. He is currently the CEO and Managing Director of Keeler Ltd, based in the UK.

Mr. Iwan van Vijfeijken, CEO, has over 25 years of professional experience in a very broad set of industries including MedTech & Life Sciences, Semiconductors and Electronics. He has led several medical device companies, including start-ups.
Mr. Steve Stoffels is VP Technology, with over 15 years' experience in researching and developing cutting edge micro-technologies. He has extensive experience both in the field of micro-mechanics as well as semiconductors, bringing new concepts from incubation in the lab to manufacturable technologies in the fab.

Iwan van Vijfeijken, CEO of Pulsify Medical, said: "We envision a breakthrough in ultrasound-based medical imaging. Accurate and non-invasive cardiac monitoring will change current practice at intensive care units. In Europe, approximately 70 million people suffer from cardiovascular diseases of which each year 15% are hospitalized. Our technology will follow patients' basic health parameters all over the hospital and at home, without requiring the intervention of specially trained individuals to obtain and interpret results. Changes in the functioning of the heart will be signaled, allowing doctors to intervene."

Xavier Rottenberg, Scientific Director at imec stated: "Ultrasound imaging is a safe technique to produce images with exquisite details revealing critical information on a patient's health.

However, it isn't yet widely available as a monitoring tool in intensive care units, let alone in ambulatory settings. Pulsify Medical will change this. We will improve life quality, by preventing adverse events and allowing shorter hospital stays, and we will even save lives."

Frank Bulens, Partner at imec.xpand, added: "We are extremely pleased to have a stellar team in place to develop a smart device for accurate, continuous monitoring of vital functions of the human body non-invasively and wirelessly, and hence generate opportunities in the hospital and home setting which do not exist today."

TE Connectivity signs agreement to acquire Silicon Microstructures

Measurement Specialties, a subsidiary of TE Connectivity Ltd, has signed a definitive agreement on September 20 to acquire Silicon Microstructures from Elmos Semiconductor. The agreement is subject to customary closing conditions; the parties expect to close the transaction this calendar year.

The acquisition of Silicon Microstructures will expand TE's global leadership in pressure sensing technology, particularly in medical, transportation, and industrial applications. Upon completion, the transaction would bring together SMI's micro-electro-mechanical systems (MEMS) sensor technology design and manufacturing capabilities, with TE's operational scale, customer base and existing sensors technologies into a more comprehensive global sensing solutions offering for customers.

"Silicon Microstructures' MEMS pressure sensing design and manufacturing capability is utilized in various applications requiring miniature design and high-performance packaging,' said John Mitchell, senior vice president and general manager of TE's Sensor Solutions business unit. "The MEMS low pressure sensing capability compliments TE's pressure offering while strategically aligning to its market and application focus."

Dialog Semiconductor to acquire creative chips

DIALOG SEMICONDUCTOR, a provider of power management, charging, AC/DC power conversion, Wi-Fi and Bluetooth low energy technology, has announced it has signed a definitive agreement to acquire Creative Chips GmbH, a prominent supplier of Integrated Circuits (ICs) to the Industrial Internet of Things (IIoT) market.

Headquartered in Bingen close to Frankfurt, Germany, with an additional design center in Dresden, Creative Chips is a fabless semiconductor company with a growing IC business supplying a broad portfolio of industrial Ethernet and other mixed-signal products to top-tier, blue-chip manufacturers of industrial and building automation systems. The technology is optimized to efficiently connect large numbers of IIoT sensors to industrial networks. Building on its long-established custom IC business, Creative Chips is also developing a range of highly complementary standard IO-Link IC products, driving broader connectivity in the Industry 4.0 revolution.

The new acquisition is strategic for Dialog to establish itself as a proven supplier, well-positioned to capture the significant growth potential of the Industrial IoT market. It also provides Dialog with a rich portfolio of core IC products and a broad library of relevant analog, digital and RF technologies. The acquisition includes the addition of an experienced engineering team with a wealth of unique skills that, when combined with Dialog's worldwide engineering, marketing and sales teams, will accelerate IC sales on a global basis.

Both companies operate well-established fabless semiconductor business models with a focus on mixed-signal products and technology. With Dialog's global scale, operations, product development and extensive IC technology resources, the combined companies are strongly positioned to quickly address opportunities in the IIoT market. "The acquisition of Creative Chips is instrumental for Dialog, giving it a strong foothold in the Industrial IoT market, while still highly complementary to Dialog's current mixed-signal business," said Jalal Bagherli, CEO of Dialog. With Creative Chips, Dialog gains an impressive set of top-tier industrial customers with trusted relationships that have been built over the course of nearly 20 years. This will extend Dialog's global sales reach of its existing wireless low power connectivity, configurable mixed-signal and power management ICs while establishing a key strategic building block for Dialog to realize its larger ambitions in the Industry 4.0 market.

Creative Chips is expected to generate revenues of approximately $20 million in calendar year 2019 with revenue growth of over 25% per annum anticipated over the next few years. The acquisition will be funded from Dialog's balance sheet for a cash payment of approximately $80 million, with an additional contingent consideration of up to $23 million, based on future revenue targets in 2020 and 2021. The transaction is expected to close in the fourth quarter of 2019.

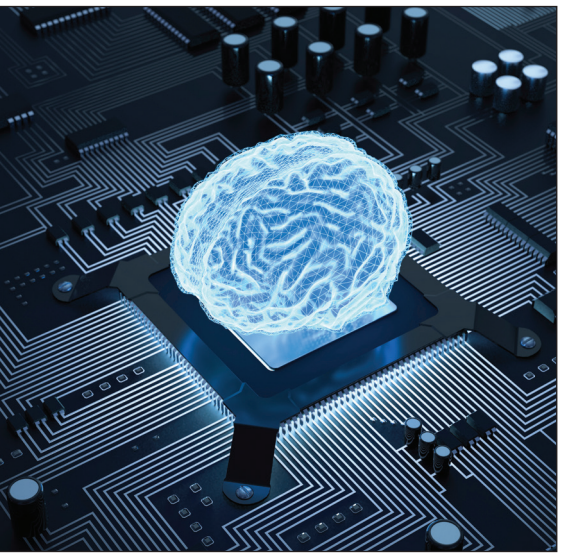
A*STAR's AI chip design platform to give semiconductor industry a boost

A*STAR researchers have developed an AI chip design platform that has the potential to transform the multibillion-dollar global integrated circuit (IC) design industry by accelerating design optimisation, reducing IC design turnaround time, and improving productivity significantly by twofold.

The traditional way of designing integrated circuits is a complicated process that requires experienced engineers with domain knowledge. It is a manual, laborious process where designers rely on trial-and-error to achieve their design goals, slowing down productivity in the process.

As technology advances, the complexity of chip design is ever increasing.
To combat these challenges, A*STAR's Smart IC Design with Learning Enablement (SMILE) is an AI platform that uses machine learning to automate these complex processes.

The SMILE platform is able to augment the circuit design process to improve productivity and quality, perform design space exploration, and enable rapid IP development. It can enable accelerated and automated design closure even in the absence of an experienced designer.



To demonstrate its effectiveness, the platform has been deployed internally within A*STAR's laboratories, and researchers were able to show two times silicon-proven performance boost compared to the best human optimised design – all within the span of a day.

This is a breakthrough in terms of productivity in IC design.The developed capability is in the intersection of deep learning and circuit design. It combines integrated circuit design and electronic design and automation (EDA) expertise from the Institute of Microelectronics (IME), and AI algorithms from the Institute for Infocomm Research (I^2R).

By employing state-of-the-art AI semi-supervised learning, and an algorithm unique to A*STAR, the system is able to improve its learning accuracy with a significantly less amount of training data.

In conjunction with EDA to capture prior knowledge of the circuits and suggest an optimised solution, SMILE is a smart system which balances the trade-offs in speed, area, power, and overall performance. An image of the integrated circuit designed by SMILE can be found in Annex A.

This development will benefit semiconductor design industries, ranging from IP development and fabless IC design companies, as it will greatly improve the productivity of the research and development of integrated circuits, and reduce the time to push the product to the market.

"With this novel technology, we can advance science in the wider ecosystem and give the semiconductor industry a boost in productivity. Companies can leverage A*STAR's technologies to scale up and remain competitive." said Prof Dim-Lee Kwong, Executive Director of IME.

Mycronic receives order for two Prexision Lite 8 Evo mask writers

MYCRONIC AB (publ) has received an order for Prexision-series mask writers for display applications from Photronics Inc, for deployment in Asia. The order consists of two Prexision Lite 8 Evo mask writers and constitutes Mycronic's first order for this product. The order is valued between USD 20-25 million. The first system is planned for delivery in the first quarter of 2021 whereas the second system is planned for delivery in the second quarter of the same year.

Mycronic offers mask writers for the manufacture of photomasks within different areas of application. These are display manufacturing (TV, smartphones and tablets) and applications within multi-purpose, a broad segment comprising many different application areas.

Prexision Lite 8 which was launched in April this year, is built on the new control platform Evo and designed to meet the requirements for cost-efficient production of photomasks for main stream displays up to G8 mask size. Despite the clear trend towards more advanced photomasks for displays, the market for less complex photomasks will remain a significant and important segment.

The Evo control platform was launched in September this year and is based on a new modern software and hardware architecture designed to meet the future requirements within both production automation and big data applications.
"It is always extra gratifying to receive the first order for a newly launched product, which also confirms that Prexision Lite 8 Evo is well positioned to meet our customers' need for a cost-efficient photomask production", says Charlott Samuelsson, Sr VP Pattern Generators at Mycronic.

Samsung develop 12-layer 3D-TSV chip packaging

SAMSUNG'S new innovation is considered one of the most challenging packaging technologies for mass production of high-performance chips, as it requires pinpoint accuracy to vertically interconnect 12 DRAM chips through a three-dimensional configuration of more than 60,000 TSV holes, each of which is one-twentieth the thickness of a single strand of human hair.

The thickness of the package (720 μm) remains the same as current 8-layer High Bandwidth Memory-2 (HBM2) products, which is a substantial advancement in component design.

This will help customers release next-generation, high-capacity products with higher performance capacity without having to change their system configuration designs.

In addition, the 3D packaging technology also features a shorter data transmission time between chips than the currently existing wire bonding technology, resulting in significantly faster speed and lower power consumption.

"Packaging technology that secures all of the intricacies of ultra-performance memory is becoming tremendously important, with the wide variety of new-age applications, such as artificial intelligence (AI) and High Power Computing (HPC)," said Hong-Joo Baek, executive vice president of TSP (Test & System Package) at Samsung Electronics. "As Moore's law scaling reaches its limit, the role of 3D-TSV technology is expected to become even more critical. We want to be at the forefront of this state-of-the-art chip packaging technology."

Relying on its 12-layer 3D-TSV technology, Samsung will offer the highest DRAM performance for applications that are data-intensive and extremely high-speed.

Also, by increasing the number of stacked layers from eight to 12, Samsung will soon be able to mass produce 24-gigabyte (GB)* High Bandwidth Memory, which provides three times the capacity of 8GB high bandwidth memory on the market today. Samsung will be able to meet the rapidly growing market demand for high-capacity HBM solutions with its cutting-edge 12-layer 3D TSV technology and it hopes to solidify its leadership in the semiconductor market.

*8GB mass-production product = 8Gb x 8 layers, 24GB newly developed product = 16Gb x 12 layers

AP&S sets new wafer processing standards with next-gen technologies

The wet process and manufacturing service experts at AP&S are setting new benchmarks for semiconductor wafer surface performance through expansions, partnerships and by incorporating AI and AR into their portfolio to transform the customer service experience.

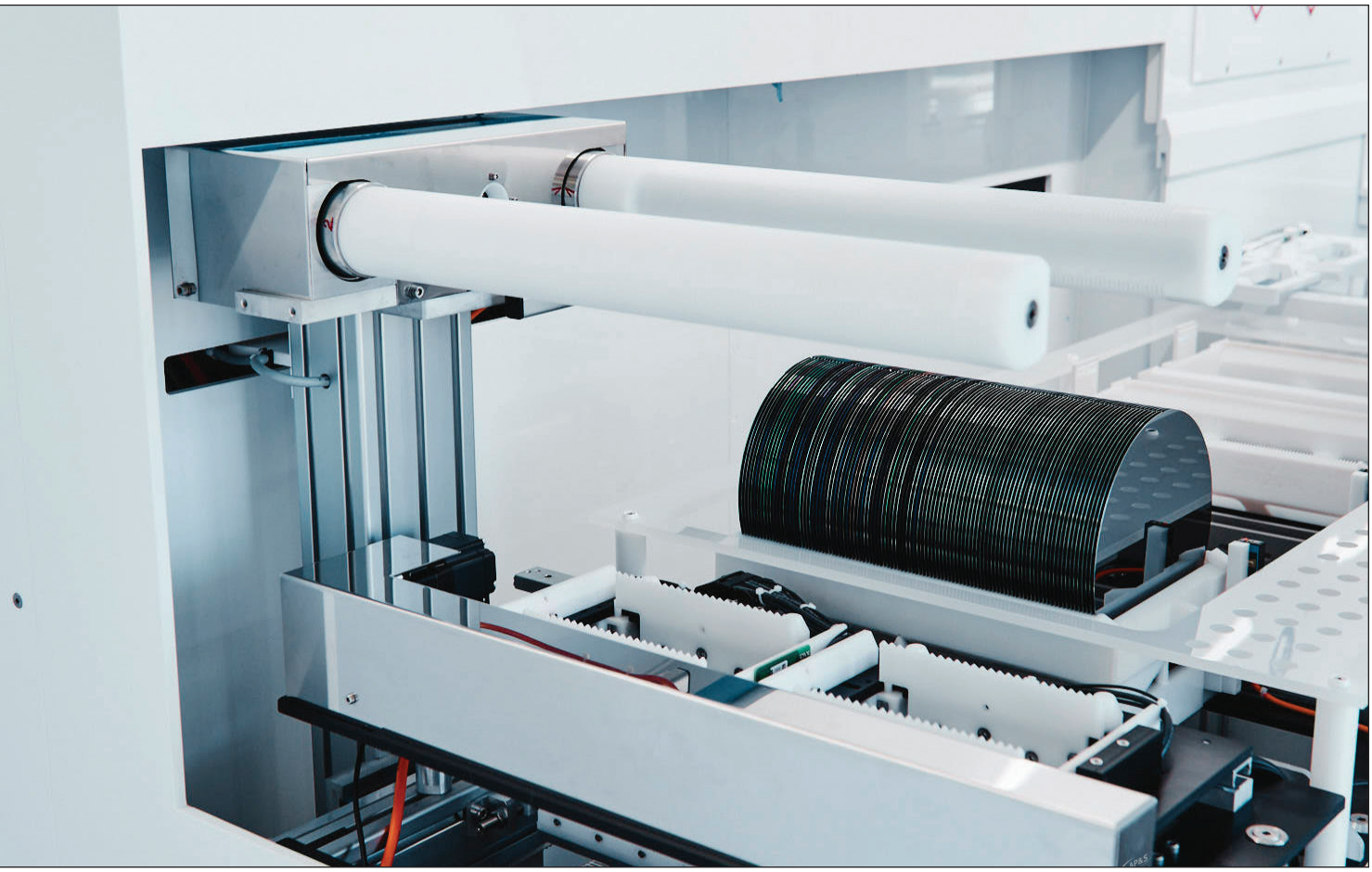
AP&S INTERNATIONAL GmbH (Donaueschingen, Germany) may perhaps be best known for its semiconductor wafer surface treatment expertise. From wet bench single- and multi-wafer platforms to cleaning and precision materials applications, the company has outfitted IC manufacturers across the globe. But there is much more to AP&S besides wafer processing and equipment service. And their portfolio is growing.

The company has celebrated many awards and industry 'first's throughout its history, but a large part of its efforts to diversify and expand services in the last two years has been tied to an overarching concern for customer satisfaction. Three main areas exemplify their approach. First, the addition of new clean room space at the headquarters facility was a substantial investment to enhance the company's ability to test equipment under real-world conditions. Beyond new cleanroom space, AP&S made other substantial commitments to expand its Demo Center where customers, field service engineers and other company personnel can see, test and operate various machine configurations. AP&S has also grown through investing and partnering with tepcon, a company renowned for its Industry 4.0 automation technologies; machine networking; enhanced human-machine interfaces (HMI), as well as work in artificial intelligence which also ties to its augmented reality (AR) programme portfolio. And the company continues to enhance and expand its hallmark wet bench solutions as exemplified by the Vulcanio system for under bump metallization (UBM) processes.

AP&S CEO, Alexandra Laufer-Müller, started to move the company towards greater levels of automation before the practices were widespread across every sector of semiconductor manufacturing. The 2016 tepcon investment showed leadership at a time when Industry 4.0 initiatives were in their early stages and digitalization within semiconductor manufacturing was progressing at different rates. The investment began showing dividends and by 2017 AP&S was using new augmented reality programmes with the Microsoft HoloLens and other AR/VR headgear to enhance machine performance data review in ways that were not only visually exciting but much more efficient and interactive. Christoph Kluge, tepcon's Managing Director, noted that service and maintenance operations across semiconductor manufacturing is quickly automating to gain greater efficiency and reduce cost while leveraging the data collected through many platforms to deliver greater situational awareness across a manufacturing floor.

"Machine monitoring by humans, as we know the process from the past, is no longer necessary and won't exist in the future," explained Kluge, Head of the Software Department at AP&S and Managing Director of tepcon GmbH, an AP&S subsidiary. "In the condition monitoring area our solutions provide a configurable visualization of real-time data in tables,

Operators begin wafer processing using the AP&S GigaStep with a pre-defined recipe



AP&S surface preparation systems handle single- and multi-wafer batch requirements

graphics or flow diagrams, monitoring of threshold values and very timely alerts through via email, SMS or WhatsApp. The customer can intervene flexibly from anywhere at any time via his mobile device. Machine failures can be avoided in real time. Analyzing process data enables the recording and tracking of recipes. Incorrect operations can be seen through a comparison with historical data, which leads to an optimization of recipe sequences and efficient planning of service assignments."

Kluge went on to say that while tepcon is specialized in software that provides condition monitoring, machine learning, AR and telematics solutions for manufacturers and the machines they build, what sets tepcon capabilities apart from others is the use of a unique Industrial IoT (IIoT) portal that acts as a gateway for collecting, storing and utilizing critical data points.

"This interconnection brings some substantial advantages. For example, important data from a wet process machine generated by machine monitoring software can be visualized as a 3D overlay via augmented reality. As a result, when walking past the machine, the operator can read critical values of the system via his smartphone or a Microsoft HoloLens or another device. There is no need to log-in to retrieve some data archives. In addition, there are valuable synergy effects from the interconnection of condition monitoring and machine learning solutions too," he said.

According to Kluge and other AP&S experts, the way a manufacturing floor operates is going to change radically within the next five to 10 years, with more efforts directed towards automation and preventative maintenance; reducing downtime will be optimized to increase overall efficiency. One of the real challenges that today's manufacturers also face is how to maintain high levels of efficiency and production in markets where skilled labor is scarce.

"AI and AR are essential key technologies to solve the shortage of skilled workers in mechanical engineering. AI offers the opportunity to 'listen and see' into the machine and to assess and predict its condition. Previously, this was possible only by experienced employees that through their many years of professional experience, these skilled workers developed a fine feel for the ways machines operate so they could assess the status of a system over time. Today, vibration sensors can take this role: the vibration of the machine can be automatically recorded and evaluated by accelerometer sensors. The data can be used for making predictions for maintenance cycles. Over time with machine learning these predictions get better and better until they

become correct most of the time, which is a huge advantage for the customer."

"Semiconductor manufacturing is extremely complex and these complexities grow with each new generation of technology. Everything that we can do to simplify the process from the customers' perspective is an important and valuable addition," he said.

While Kluge emphasized the role of tepcon expertise in preventative maintenance, he also explained ways that the same technology can be used as a training tool for service personnel – to help pass along accumulated knowledge. They can leverage the software's capabilities to remember everything while being more than an archive – the system becomes an intelligent partner in the development of performance enhancement strategies. Variations of the software enable a potential customer to visit AP&S facilities remotely, and participate in meetings with service managers, engineers and other process tool experts in collaborations that were never before possible, pointing to the long-term possibilities of this evolving technology.

One place where tepcon technology is already enhancing other aspects of AP&S services is in the company's Demo Center at its headquarters. The largest investment was in new clean room space which enables real world operational conditions for a wide variety of process tools and related hardware. The expansion offers ISO5 cleanroom space with state-of-the-art 3D microscopic substrate inspection and structure measurement. The company's topographic measurement capabilities complements other skill sets to create an in-house laboratory for tool demonstrations, process evaluations, tests, and in-house training programmes.

"We see the ability to have an intensive dialogue with our customers as the basis for our success. The Demo Center creates a perfect 'room' for knowledge exchange and joint research projects with our customers and partners. Furthermore, it is a factor that distinguishes us from other wet process solution suppliers in our market who usually do not have an in-house laboratory," remarked Stefan Zürcher, Team Leader of Process Engineering & Laboratory at AP&S.

Zürcher explained that while coming to the Demo Center in person is the best way to see a tool in action, remote access is possible, so a customer can visit the Demo Center via a video feed or augmented reality for some demonstrations. The advantage of 1:1, personal exchanges with the engineers who build AP&S systems remains the top-draw for being there in person.

"In all our tools, webcams are installed to enable a remote access to the demo in case someone cannot come personally to AP&S. Within a process demonstration, videos are typically taken and afterwards are shared with the customer together with a detailed test report including all relevant process and tool parameters, chemical consumption, etc. This also enables customers to calculate a cost of ownership of the equipment they are considering," he explained.

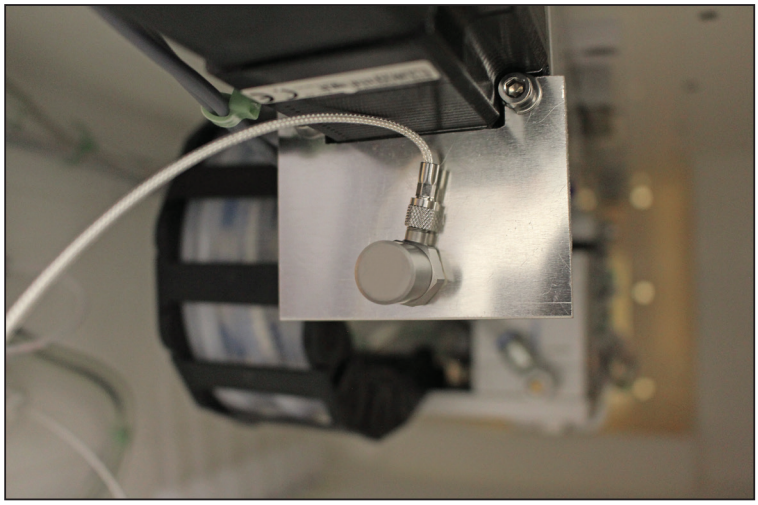
Zürcher said that while enabling equipment demonstrations is a key Demo Center benefit, the facility also serves as a research hub where discoveries aid the development of new wafer processing tools, techniques and service processes. "We were motivated to perform process demonstrations under production related conditions combined with achieving 'best practices' for the performance of our tools. We can evaluate the tool performance and external effects, like airborne particles; we can test their impacts. Particle contamination is of course to be avoided.

The Vulcanio eLess plating wet bench system delivers advanced under bump metallization performance

Handling service assignments is easier thanks to virtual data that can include step-by-step instructions downloaded via AR glasses and processed one-to-one on the machine. Even untrained personnel can handle many repairs error-free

We can also ensure that wafers processed in our AP&S Demo Center are clean so that they can be directly transferred back to a customer's facility for subsequent process steps or to their metrology department," he explained, noting that AP&S also offers particle counters for liquids and cleanroom gases that give customers and the company more data for ongoing improvement and quality control.

The company's renowned attention to detail and customer satisfaction also helps fuel their R&D programmes including ongoing updates to the company's extensive hardware portfolio.



Acceleration sensors in AP&S tools enable remote monitoring so that service intervals are anticipated ahead of a breakdown. Many conclusions can be drawn utilizing vibrations detected by sensors; up to 40,000 values per second (40 KHz) per sensor are captured to monitor rotation, pressure and overall performance

The Vulcanio wet bench system is constantly studied to improve upon its class-leading capabilities. As device geometries shrink and height requirements become more stringent, more devices are moving away from wire bonding to flip chip designs, including MEMS components that may range from microphones to sensors of many types; MEMS devices are also actuators and essential control system elements.

"The AP&S Vulcanio system utilizes under bump metallization to support device shrink and better reliability. Device input and output pads need a solderable surface to be an interface between the I/O pad and the solder bump—the UBM. This surface is typically a thin, multi-layer metal film between the pad material and the solder bump. It acts as a diffusion barrier to stabilize IMP's. The UBM is also the right (technology) in the context of the ongoing MEMS development, too, as MEMS devices will also shrink massively," explained Tobias Bausch, the AP&S Vice President of Sales & Marketing.

The company has sharpened the performance of Vulcanio since its inception, first moving under bump metallization to lead-free solders for underfill helical interconnections between 200-100 micron. Most manufacturers today are utilizing 50-20 micron underfill while future requirements will include much tighter tolerances "We are already anticipating customers in the future will focus on nano interconnects with 10-1 micron underfill," he added. The Vulcanio wet bench is an electroless or auto-catalytic deposition system that operates without external electrical power to energize metallic deposition. Electroless or 'eLess' deposition is preferred for integrated circuit wet bench applications.

"To reach optimal electroless process results the following aspects are critical, which are all covered with the AP&S Vulcanio wet bench – the eLess chemistry needs closed loop control to ensure stable IMP results and to prevent IMP changes during additional processing steps. On-line analytic and in-situ dosing is needed for process and device stability. Finally, a detailed process interaction modeling assessment is needed to define processing windows," he explained.

"Our Vulcanio wet bench shows excellent reliability performance, which has been demonstrated from 40-90 degrees C. It also provides superior over nickel and gold structures. Thanks to our superior control system, metal thickness from 0.05 μm to 5 μm is possible without sacrificing performance. Thinner gold layers also reduce cost while helping to reduce the risk of gold embrittlement in solder joints. These many advantages have led to the system's long use within the market. Our constant analysis of performance and optimization through close cooperation with our customers along with scientifically proven good performance has led to the very positive customer feedback," he concluded.

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Trade disputes

fuel supply chain worries, opportunities

Long-smoldering trade disputes between the United States and China have impacted many sectors of global economies with semiconductor manufacturers amongst those hardest hit. Recent headlines in Washington, DC and Beijing have signaled a compromise may be coming, but long-term consequences could persist for years. Silicon Semiconductor asked experts at the Chartered Institute of Procurement and Supply (CIPS) to examine today's issues and how these may affect business in 2020 and beyond.

REPLIES FROM: BILL MICHELS, VP OPERATIONS, CIPS AMERICAS

Q Trade disputes between the US and China were ratcheted up this summer when US President Donald Trump announced additional sanctions. What has the 'tit for tat' done to affect business and supply chain conditions for semiconductor manufacturers?

Bill Michels: The recent developments in the US-China trade conflict are pushing organizations to accelerate reassessment of their supply chains. For many companies, the cost savings of sourcing from China have been diminishing for some time, while risks have been increasing, so changes were in the works before the trade war began. As the tit for tat between the two governments' ebbs and flows, it has not brought a resolution of the conflict into focus. Instead, uncertainties are growing, forcing the hand of risk-averse organizations to 'reshore' or move their sources to other new origins not subject to tariffs.

Companies that can raise the capital to invest in automation or other manufacturing innovations are finding that those investments can offset the benefits of low-cost country sourcing. Black and Decker is an example of that, as it has announced it will build a highly automated, $90 million dollar facility to produce Craftsman hand tools.

However, we can't expect a huge migration back to the US. Technology companies that have made huge investments in equipment and training a workforce are not likely to move back quickly. In fact, A.T. Kearney's 6th annual Reshoring Index confirms that growth in manufactured goods imported into the United States from the 14 largest low-cost country (LCC) trading partners in Asia rose by $66 billion or 9 percent for the year, the largest annual increase since the beginning of the economic recovery. US gross manufacturing output, by comparison, grew only 6 percent year-over-year in 2018.

Another response to changing world markets is to build smaller, autonomous plants close to the markets they serve. In that scenario production may stay in China, but primarily to serve Asian markets. The notion of one location distributing to the world is diminishing, based on the changing political, social, and environmental conditions of the global economy.

President Trump has asserted that China needs a US trade deal because Chinese companies are more adversely affected by tariffs than American corporations. But global economists have argued that China's current growth is not much slower than expected and that China is using the dispute to grow internal demand and supply sources that bypass the US – what's your view?

Bill Michels: The worst unintended consequence of the dispute could be a downturn in the global economy. According to IHS Markit, the Future Output Index in the J.P. Morgan Global Composite PMI hit a seven-year low in July. Panelists surveyed cited the US-China trade war as one of the factors lowering their forecasts. The rising uncertainties from the dispute also appear to be affecting the US stock market – sending it up or down depending on what signal comes out of Beijing or Washington.

Have US-China supply chains been rerouted because of the dispute?

Bill Michels: Categories with low complexity can easily be moved to Vietnam, Malaysia, Thailand, the Philippines, and other countries not subject to the tariffs. No doubt the trade issues are forcing the reengineering of supply chains and creating a redistribution of products.

Some of the rerouting going on now predated this particular dispute. Samsung, for instance, reportedly has moved a significant amount of its production from China to Vietnam. Apple may be considering a similar move, and a continuing dispute could accelerate their decision.

Have you seen evidence that Chinese manufacturers are developing alternative resources either from within China or other regions?

Bill Michels: I have not seen specific evidence of Chinese manufacturers developing alternative sources from within their own country or other, less hostile countries; however it could be that the Chinese government is holding its position so firmly because it feels that companies there can find alternative sources. I have also seen some Chinese investment in the US. The sale of the GE appliance business to Haier is a great example

Have key members of the US/China supply chain learned from this experience to the point that they are factoring how-to-operate amidst a trade war into present day operations and/or future planning?

Bill Michels: It seems clear that many of the firms we have mentioned, Samsung, Apple, Black & Decker, as well as others have been taking a lot of factors besides labor costs into their sourcing decisions for some time. For those forward-looking companies, the risks of a trade war are simply one more factor to go into a complex decision. They have likely been looking at logistics issues and the risks of intellectual property or data theft as other potential costs of sourcing from China.

President Trump may have delayed tariffs on many popular consumer products, and there may be a more comprehensive deal reached eventually, but the well has been poisoned for now and it will likely bring long-term changes. The lesson here is that supply chain professionals have an obligation to continually manage innovation and geopolitical risk. They can't wait for a crisis, they must prepare for whatever might come. The application for exemptions to tariffs has benefited some firms. Applie got 10 exemptions and some of my clients were successful.

Within the US, media coverage has focused on how tariffs have hurt general manufacturing and farmers due to reductions in sales to Chinese markets, higher costs of component goods and other consumer-centric impacts. Will trade to return to 'normal' once the dispute ends?

Bill Michels: The electronics industry has capitalized its industry and workforce in Asia, and it would take a very long time and a great deal of money to change and recapitalize the industry. In addition, they would have to find and train a new workforce. Asia is also a huge market for electronics products, so even as companies might build new facilities outside China, there is still a good reason to keep production

in that country to serve the region. The "new normal" for many companies will keep them in China, but not simply to export to US customers.

The agricultural industry is a bit different as its products are true commodities, subject to supply and demand sensitivity. When disputes are resolved it may take one or two seasons or growing cycles to re-establish "normal" levels of imports and exports; however, nothing is guaranteed. Other countries may be able to carve out market share while US exports to China are restricted. Subsidies to farmers can mitigate the hardships here in the short term only, they could worsen the situation if, for instance, farmers cannot start moving their products again, so they decrease future planting. Even if farmers get subsidies the crop stays and compounds the following year when new crop comes in. At some point the supply must balance with demand

Has the impact been felt by manufacturers producing solar (PV) energy components, cells or modules?

Bill Michels: The domestic suppliers of solar panels have capacity, innovations, and quality and are priced to compete with imported panels. Unfortunately, without competition from Asia, the pricing for domestic components will rise to match the levels of imported panels with tariffs. While increasing the margins for US producers while the tariffs continue, customers will be seeing higher prices.

While much attention has focused on China-US disputes, Japan and Korea had their own tussle recently over complex materials critical to high-tech manufacturing. Are global trade tensions growing? Don't most companies dig deeply on supply chain details only when this is trouble?

Bill Michels: If you have not mapped your supply chain upstream all the way back to raw materials, you are asking for trouble from a potential tariff, single-source supplier, natural disaster or logistics snafu that you knew nothing about. Once you know where everything is coming from you can systematically assess every link in your chain to see if every supplier in every step is adding sufficient value to make it a worthwhile partner. Supply managers must look beyond cost to see how every supplier adds value to the overall benefit of the organization. That means analyzing changing market demand, economic conditions and risk as they choose suppliers.

And you are right – most companies only know all their supplies deeply when there is risk. Pharma companies, for instance, operate under fairly rigorous chain of custody rules for their supply chains, so they are well mapped. Going to chain of custody documentation is a step beyond simply knowing who your suppliers are. Rigorous chain of custody can identify which boat and day of the catch went into a can of tuna, what section of the field in the farm grew a box of strawberries, what day and what mine extracted the lithium in a battery and so on. There are industry associations that are trying to create systems to generate that granular data as part of their certifications of sustainability, but the efforts vary in their scope and effectiveness.

And yes, there are consultants who work with companies to develop supply chain maps because it can be a difficult process. Suppliers generally find it a burden at best, and an intrusion into their business at worst. It sometimes takes a contract renegotiation and a significant amount of trust to get suppliers to reveal their own supply chains.

In spite of those obstacles, the rising global pressures for corporate social responsibility make it imperative for companies to better map their supply chains and educate their suppliers to maintain ethical standards. A few countries have already established severe penalties for forced labor in the supply chain, putting new responsibilities on procurement and supply chain managers. The reputation risk is very high for companies that do not develop supplier training and audit capabilities to manage supply chain ethical, environmental and employment practices. A revelation of bad behavior deep in the supply chain could have catastrophic effects for buyers.

Do trade tensions in Asia and the US create opportunities for other regions, and if so, what are these regions and why might they benefit?

Bill Michels: Places that have infrastructure and labor advantages can benefit from the current trade difficulties. A recent Boston Consulting Group study highlighted the cost advantages of Mexico, Thailand and Indonesia over China – even before tariffs.

Vietnam is also aggressively courting manufacturing companies and has the success of attracting Samsung as sales message. The country is struggling a bit to develop its workforce, but even so, it might have a leg up on other low-cost countries that want to build silicon chips or solar panels. Ironically, some of the infrastructure improvements that China is making in Africa could help position African countries as low-cost competitors to China itself. The opportunities for Africa are largely in low-technology categories for the foreseeable future, simply because it's easier to move simple parts than complex assemblies that require precision tools and a highly skilled workforce.

Finally, the trade war with China was started in order to benefit the US, and it may, in fact, do that – to the extent that tariffs help offset companies' investments in automation or other innovations. Once robots are in place they never get tired or sick and they produce consistent quality.

Bill Michels, VP Operations, CIPS Americas

Automated AFM surface profiling for CMP applications

A new generation of atomic force profiler (AFP) using a decoupled scanners design from Park Systems

Keibock Lee, President of Park Systems

AS THE FEATURE SIZE is shrinking in the foundries, the need for inline high-resolution surface profiling with versatile capabilities is increasing. One of the important areas is the chemical mechanical planarization (CMP) process. To address this issue, Park Systems introduced a new generation of atomic force profiler (AFP) using a decoupled scanners design. This system is capable of providing small-scale profiling using an XY scanner and large-scale profiling using a sliding stage. Decoupled scanners design enables enhanced vision, which helps to minimize the positioning error for locations of interest in case of highly polished dies.

Non-Contact mode imaging is another important feature in this system, which is used for surface roughness measurement, automatic defect review, and deep trench measurement. In this article, examples of the measurements performed using the atomic force profiler are demonstrated, showing the significance of AFP as the next generation in-line reference metrology tool in fabrication labs. Atomic force profiler (AFP) using decoupled flexure guided scanners is the newly designed system that is capable of performing non-contact mode imaging for AFM applications such as surface roughness measurement. Enhanced vision enables the system to perform better positioning on highly polished patterned wafers, and it is also used in automatic defect review.

With the low scaling of devices and scaling up in production, nanometrology has attracted more attention than ever before resulting in the increasing need for high functionality metrology tools. To keep up with the demand, the metrology tools are expected to improve four major specifications: precision, repeatability, throughput, and cost of ownership [1]. In terms of precision, the tools need to be compatible with the fabrication process for smaller nodes sizes and larger wafers. Therefore, the demand for higher

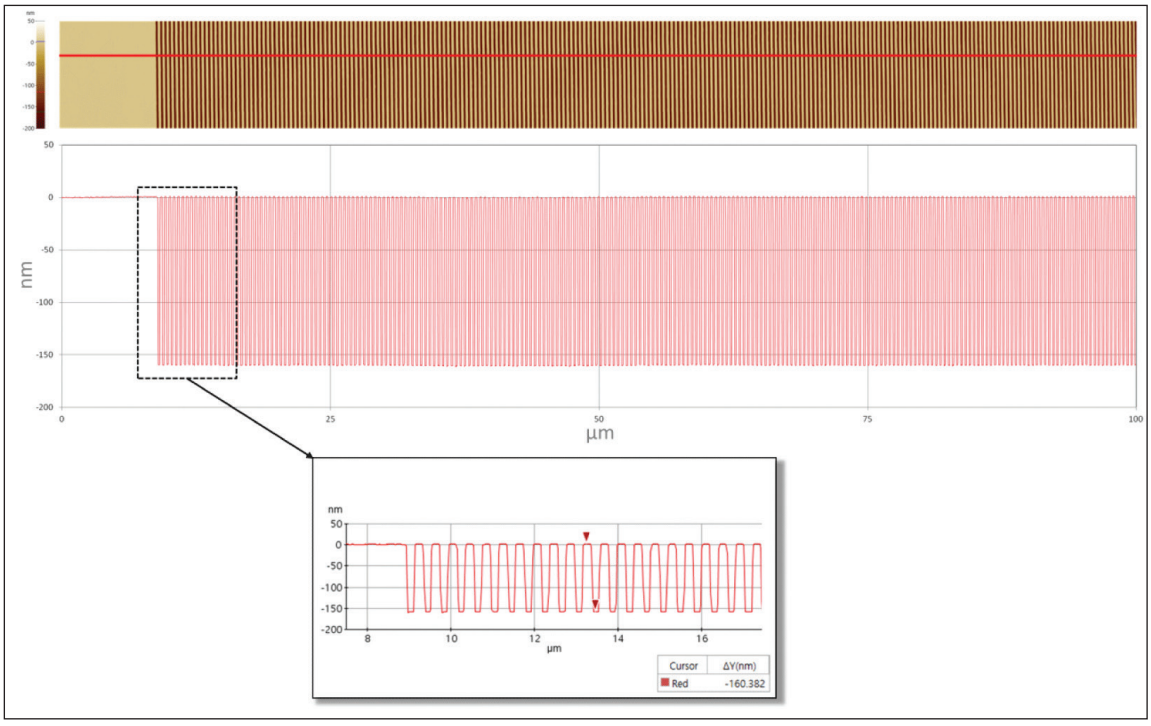

Figure 1. Small-scale profiling using AFM decoupled XY scanner. The range is 100 µm (top) and the step height is 160 nm. The inset shows a magnified section of the same profile.

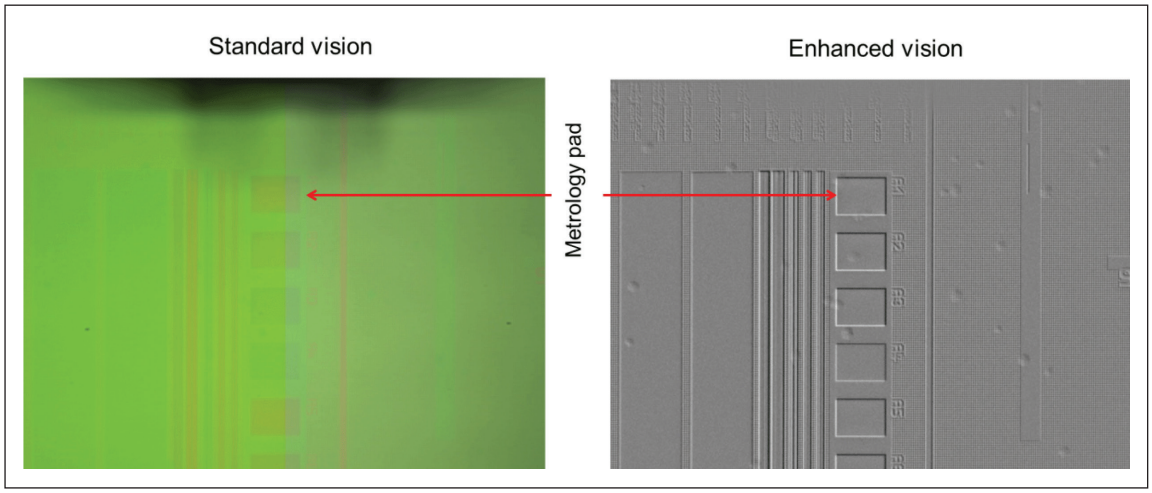

Figure 2. The plot on the right shows dishing and erosion measurement of a 9μm/1μm structure using a 2 mm line profile. The inset on the left shows a zoomed area from the profile on the right, showing high resolution of the collected AFP data.

resolution has increased significantly. However, higher resolution comes at the cost of throughput, which includes the time required for sample preparation. This results in higher cost of ownership while maintaining measurement repeatability and has presented a challenge for the latest generations of high-resolution metrology tools. This is true for surface characterization as well.

The chemical mechanical planarization (CMP) process is used to polish the surface of a wafer by using a physical pad and chemical active slurry, to remove topography and control the surface flatness to sub-nanometer [2]. The CMP process has a significant role in process of shallow trench isolation (STI) and trenched metal interconnection (Damascene). However, CMP is a blind technique which makes it hard to know if desired amounts of material are removed. Therefore, metrology tools such as surface profilers and AFM are required for monitoring the CMP process. Surface characterization has been performed using two major tools: surface profilers, and atomic force microscopes (AFM). Surface profilers have been in use for a longer period of time and the tools have been used for both surface profiling and wafer stress measurement. The typical in-plane range of measurement is a few hundred mm scale with an out-of-plane range of up to 1 mm.

The in-plane resolution of tens of nm and out-of-plane resolution of angstrom level are typical specifications of surface profilers. Therefore, it would be challenging for surface profilers to provide sub-angstrom surface roughness measurement over dielectric or poly-silicon, perform deep trench measurements, or detect defects with few nm in lateral dimension.

Atomic force microscopes (by Park Systems) have been introduced to and used in fabs for over a decade. Their major application has been surface roughness, step height, and critical angle measurements for monitoring etch, deposition, and CMP processes. The typical lateral dimension of below 70 μm with out-of-plane dimensions of around 10 μm has been measured by AFM. The noise level in the fab environment has been one of the major challenges of automated AFM systems. The systems were traditionally using piezo tube tip scanning systems. The piezo tube scanners were associated with a background out-of-plane motion that had to be compensated or filtered from the images. Tapping mode has been used as the standard imaging mode. As the result of using tapping mode, the tip life has been short and it led to challenges in repeatability of the system. In order to achieve the higher resolution of AFM and the larger measurement range of surface profilers, a hybrid tool, atomic force profiler (AFP), was

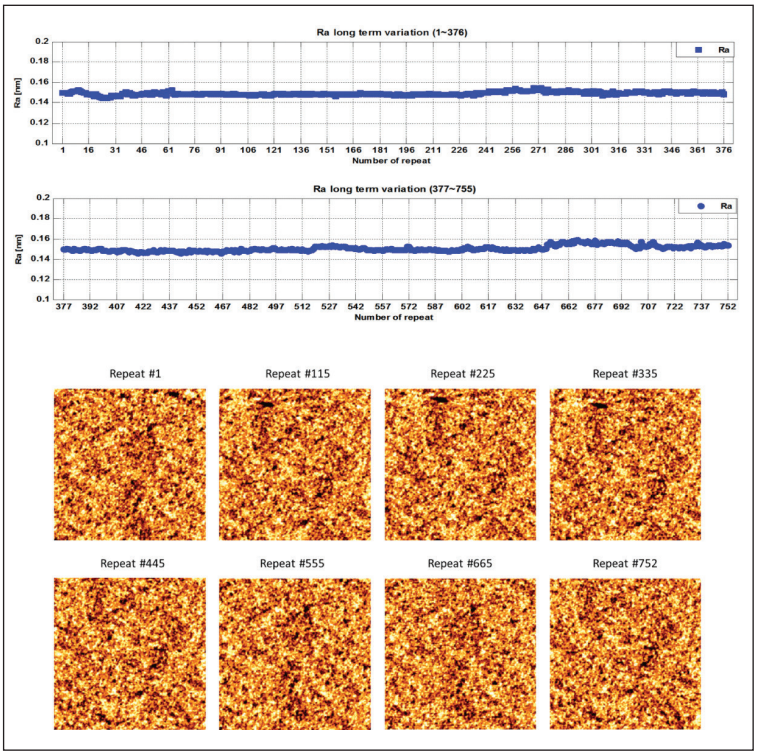

Figure 3. The results of monitoring wafer edge with AFP are shown. The AFP image is 3 mm x 3 mm. Two line profiles are shown in the middle plots. The plots on the right show magnified height scale profiles.

introduced. The conventional AFP has the associated limitations of conventional tube based AFM systems [3]. In this article the latest in-line AFP solution is discussed which was developed to address the aforementioned limitations associated with traditional AFMs. This system is based on decoupled XY and Z scanner design to eliminate the cross-talk between the scanners and provide better positioning capabilities. As a result of the improved positioning capability, the system is also used for automatic defect review (ADR). The decoupled XY scanner allows additional capabilities such as improved optical vision especially for wafers after CMP process and unpatterned wafers with small defects. This product has a commercial name of Park NX-WAFER and can perform measurements for 300 mm wafers and EUV reticles.

Profiling with decoupled flexure guided xy scanner

To address the limitations in lateral scan range of conventional AFM and the significant out-of-plane background, decoupled flexure guided XY scanners are developed and used in the new design. In this design, the scanner's main plate is moved by two pairs of stacked piezo actuator in two in-plane directions. The background out-of-plane motion for the XY scanner is below 2 nm for 100 μm scan range. The reduced background out-of-plane motion of XY scanner allows for surface profiling of up to 100 μm ranges using only the XY scanner. Figure 1shows an example of small-scale surface profiling using only the AFM XY scanner.

In the new decoupled design, the Z movement of the cantilever is controlled by a flexure guided decoupled Z scanner. Comparing to traditional tube scanners, the lowered mass of flexure scanner and its flexure design allows increased resonance frequency by approximately nine-fold. This design has multiple advantages. First, the Z scanner straightness is uniquely preserved as its movement is independent of the XY scanner offset, unlike the traditional tube scanners. Second, the smaller dimension of tube scanner allows direct on-axis optical camera, which ultimately enables enhanced optical vision for AFM. Third, higher resonance frequency of the Z scanner allows its faster response and fast scanning functionality.

Long range profiling

Long range profiling capability has become possible by the addition of a sliding stage underneath the XY scanner in the system. The sliding stage provides surface profiling using decoupled Z scanner over longer mm-scale ranges comparing to μm-scale range for AFM scanner. The decoupled Z scanner provides an engaging orthogonal angle with less than 0.015% deviation. No special software algorithm is required in order to maintain the orthogonality of the Z scanner comparing to some of the conventional scanners. One of the common applications of long range profiling is monitoring erosion and dishing in copper based structure on a patterned wafer. There is a polishing rate difference between copper and silicon. The difference leads to disproportionality in the polished amount on various areas on the wafer. The dishing and erosion of the structures after CMP process can be measured and characterized accurately using AFP. Comparing to other techniques, AFP provides minimal force during the measurement, hence, it eliminates damages to the sample. It also provides high resolution in both vertical and lateral directions. An example of such measurement with AFP is shown in Figure 2.

Another application of AFP is wafer edge profiling. Utilizing the most area on the wafer is one of the objectives in foundries. Hence, the information on the quality of devices at the edge of the wafer becomes crucial for both process engineers and process tool providers. Figure 3 shows an example of wafer edge characterization using AFP. Another example of AFP usage for characterizing Fin CMP process in SADP Fin process and Cu pad CMP process in wafer-to-wafer hybrid bonding can be found in the reference [4].

Conclusion

The new generation of atomic force profiler (AFP) using decoupled flexure guided scanners is anewly designed system, capable of performing non-contact mode imaging for AFM applications such as surface roughness measurement. Developed exclusively for the semiconductor device industry, this advanced nanometrology system offers unique capabilities including enhanced vision, which enables the system to perform better positioning on highly polished patterned wafers and is also used in automatic defect review. The decoupled XY scanner has minimized out-of-plane background motion and can be used for small-scale surface profiling up to 100 μm. The long range profiler is enabled using a sliding stage for mm-scale profiling ranges. Long range profiling is used for various applications such as monitoring CMP process of Cu pads or wafer edge bevel measurement.
AFP has been demonstrated as the valuable in-line reference metrology tool in the fab, providing reliability and accuracy in the inline production process

Further reading

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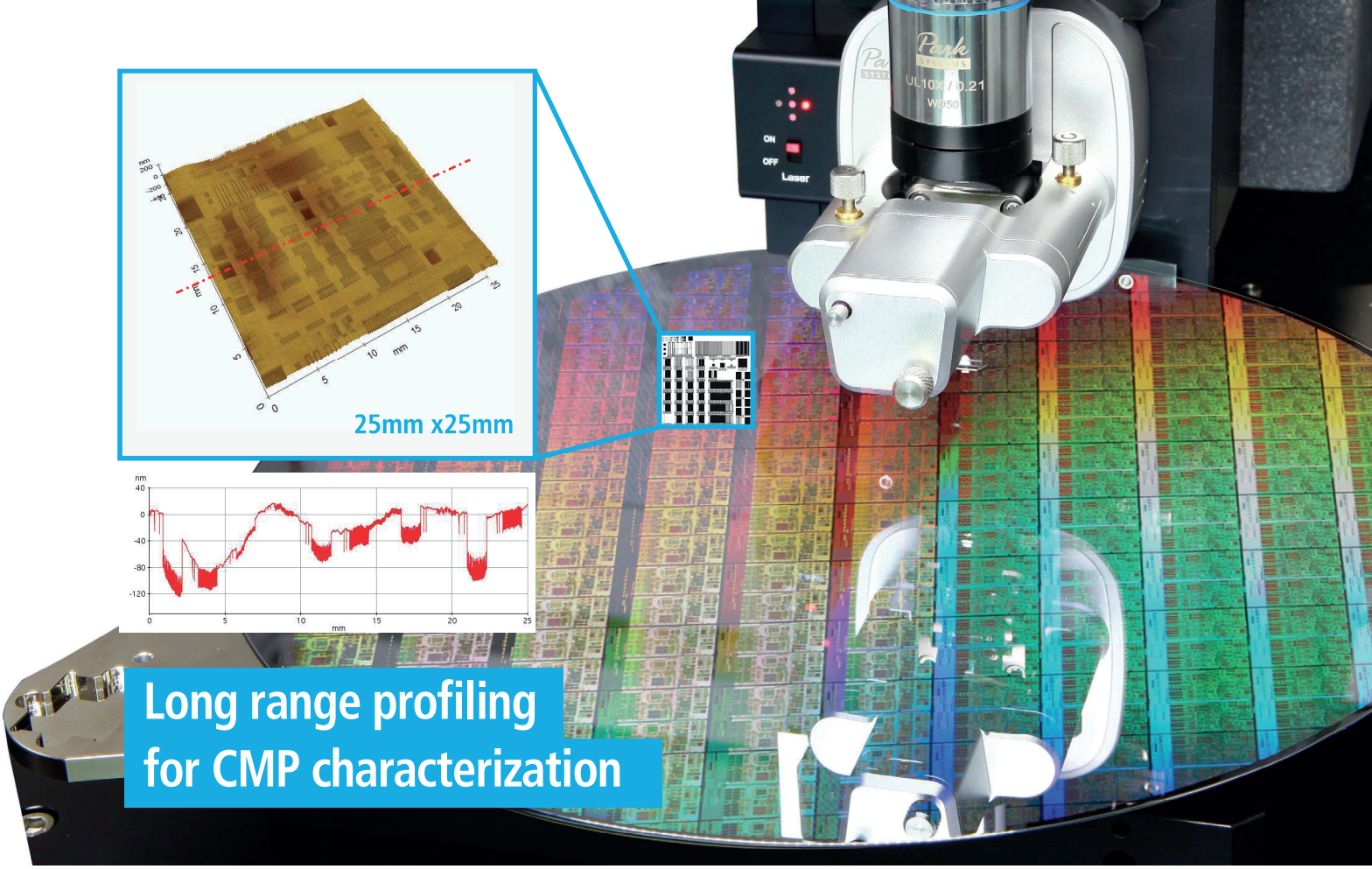

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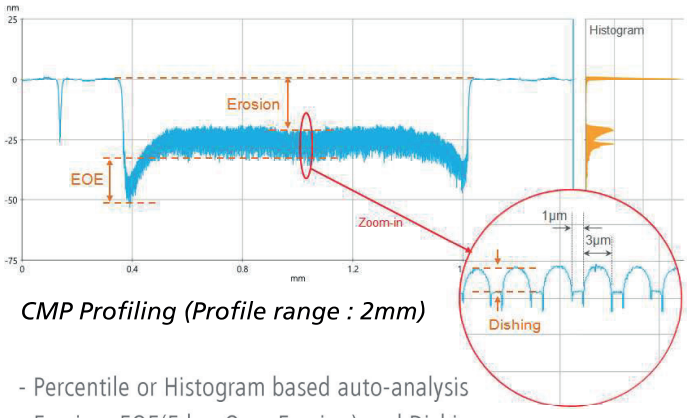

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PIC Manufacturing - TAP, Co-Packaging & Fab

As early generations of PICs are moving into commercial applications the need for automated test, assembly and packaging (TAP) is paramount to ensure long-term reliability. Opportunities for co-packaging hold promise while foundry consolidation and applications beyond datacom have implications for substrate suppliers, EDA/EPDA and many others across the supply chain.

PIC Technology - Solutions, Analysis & Research

The rapidly evolving nature of photonic integration, silicon photonics (SiP), optical computing and automotive SoCs tied to PICs offers new manufacturing opportunities. We will explore programmable PICs, the coherent vs. incoherent debate, quantum encryption and the latest integration/hybridization approaches for light sources and other PIC devices.

PIC ROI - Quality Metrics & Scalability

Scalability is a key manufacturing interest as pilot lines set the stage for volume manufacturing. What metrics can best be applied to design and manufacturing as the industry pivots to higher production levels? Is a total quality management (TQM) approach vital to long-term vitality? We'll explore TAP within a quality matrix and how today's systems can be readied for long-term scalability and margin growth.

PICs Vision - Evolution and Revolution

As PICs move from 100G to 400G, the future will require 800/1600G devices - can we set the stage today for a smooth transition? We will explore leading pathways to a PIC-enabled future and what needs to be initiated in the short-term to satisfy long-term requirements. What role might quantum technologies play to increase performance, reduce power consumption and improve quality?

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X-Ray and acoustic
3D imaging of components

Both x-ray and ultrasound can non-destructively image internal features in solid objects such as electronic components. Since the two methods use different forms of energy for imaging, employing both methods can greatly enhance and speed problem solving. Most images are two-dimensional, but both methods can also create three-dimensional images of internal features - again, in different ways.

BY TOM ADAMS, CONSULTANT, NORDSON SONOSCAN

AS X-RAY PROPAGATES through a given material, it is attenuated at a rate specific to that material. Although the mechanics of travel are very different for ultrasound, it is also attenuated at its own specific rate for a given material.

If both types of energy [Figure 1] are traveling through the same material and encounter the same bonding interface between two materials, the x-ray simply crosses the interface and keeps going, although its rate of attenuation will likely be different in the second material. The pulse of ultrasound, however, will be partly reflected back to the receiver and partly transmitted across the interface. The portion of each is determined by the identity of the two materials and covers a wide range. But if the second material is a gas such as air, nearly 100 percent of the pulse is reflected, and none of it crosses the interface.

Making a 3D x-ray image is quite different from making a 2-dimensional planar image. Three-dimensional images depend on viewing the object from an angle. To make the 3D image, the beam (or the object) is rotated to various angles and data collected from

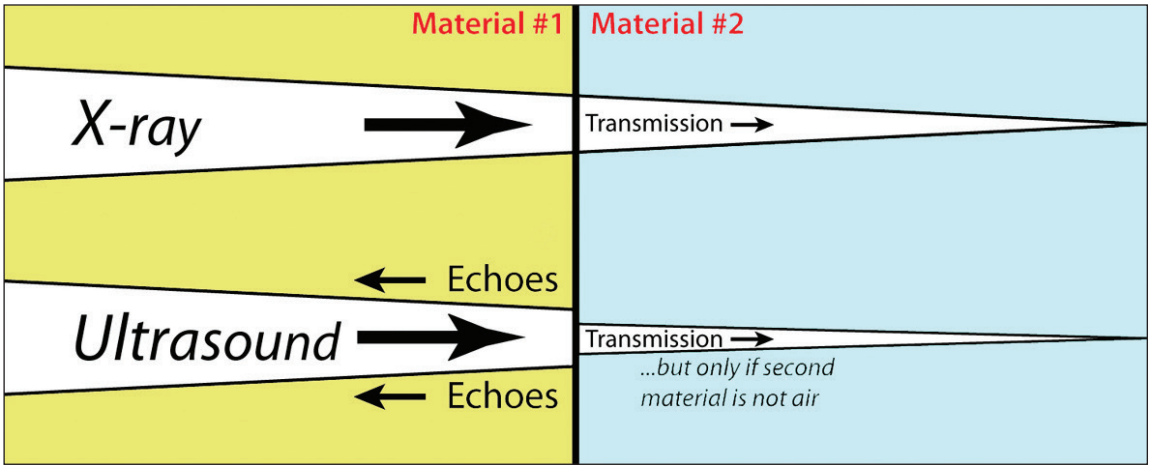

Figure 1. Reaction of an x-ray beam (top) and an ultrasonic pulse (bottom) as they encounter a material interface between two solids.

each view. Then software is used to digitally create the view desired by the operator in 3D. The process is somewhat similar to a CAT (Computer Aided Tomography) scan of a human body to obtain 3D images of bones and other internal structures. Figure 2 is the 3D x-ray image of the die region of a TO-220 device. The rectangular item at center is the die. Imaging was performed by a Nordson DAGE Quadra 7 system. Some observations:

- The die is flat, but the edges give some suggestions of its vertical dimension.
- There are two wires attached to the top surface of the die, but they are not visible at this resolution because they are very thin and, relative to the whole thickness of the encapsulated package, cause little change in attenuation of the x-ray beam.
- At all four sides of the die there is an apparent extrusion of die attach material from beneath the die. The brightness of some of the areas of extrusion does not indicate greater height or reflected visible light, but suggests that the material comprising the die attach material is less attenuating than the mold compound or the heat sink, with the result that the beam that passes through the tops of the extrusions will be less attenuated than those passing through other regions. Being less attenuated, they are imaged more brightly.
- There are about a half-dozen very small black features on the die, mostly on the right side. They represent material that is dense enough to locally attenuate the x-ray beam. They are certainly not voids, which would appear brighter than the surrounding area. Possibly they are small foreign particles, most likely above the die.

Ultrasound creates 3D images in a very different way. The ultrasonic transducer scans back and forth above the sample, sending many thousands of pulses into the sample each second. An echo reflected from an internal interface travels straight back to the receiver. However, if a surface is far from being perpendicular to the beam, the pulse can be reflected at a large angle, and the echo will be lost, thereby creating a dark area in the image.

The TO-220 shown in Figure 3 is the same TO-220 imaged in Figure 2, but imaged with ultrasound, and with the leads included at the bottom of the image. Figure 3 is a Time-of-Flight image made by a Nordson SONOSCAN C-SAM® acoustic microscope. In this imaging mode an echo arriving at the receiver is assigned a color depending upon its arrival time. In the vertical color map at the left of Figure 3, the highest features - the leads - are pink, the die is green, and the heat sink - the deepest interface - is orange.

The travel time of each echo is converted into distance. After the full 3D scan of a sample such as a TO-220, the distance from the top surface of the device to each x-y reflection site on all imaged internal interfaces is known.

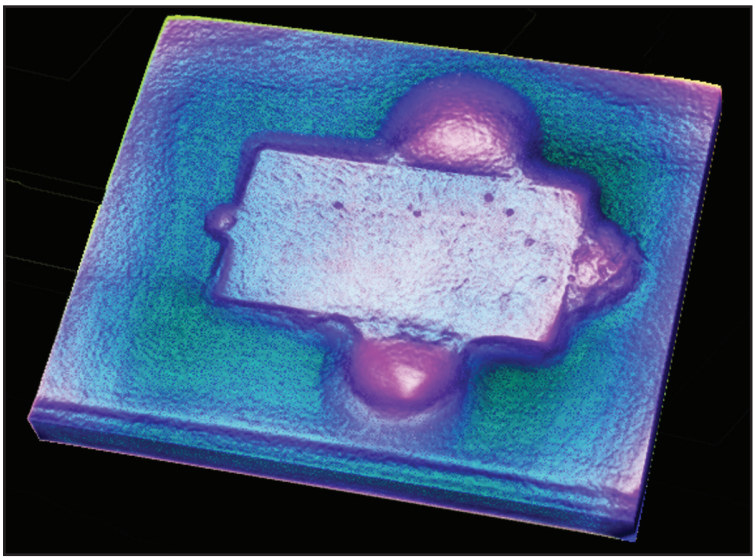

Figure 2: 3D x-ray image of the die region of a TO-220 package.

The whole component package is 6.4mm thick. The "gate" (the vertical extent from which echoes are accepted for imaging) runs from just below the top surface of the device to below the top of the heat sink. The orange surface of the heat sink is about 1mm above the bottom, the top of the die about 2mm, and the tops of the leads so high, at about 5mm, that the wires were not imaged.

If viewed from directly above, the 3D acoustic image of the TO-220 would look flat and many-colored. An observer could surmise the depth of each feature but could not see the depth directly. For that reason, acoustic 3D images are typically viewed from an oblique angle.

In Figure 3, the die at center is green (almost halfway up the color map) because it is higher than the heat sink. In this image, the die appears to be fairly thick but it is probably much thinner than it appears; 3D software exaggerates the thickness to achieve a 3D effect. In making a 3D image, ultrasound sees the top surfaces of features but cannot see the vertical sides (if any) of an object, so it creates a straight side using the same color used for the top of the feature. If the top surface is other than flat, the wall may have multiple colors.

This image shows that there are no cracks visible in the top surface of the die. The two black spots in the die are locations where wires are attached. The wires are round in cross section; when a pulse of ultrasound strikes a wire, it is reflected in many directions and has essentially no chance of being returned to the transducer where its distance will be recorded. No ultrasound travels through the wire to the die surface. What the transducer "sees" is an area having no return signals, so the area is colored black and is given colored interior walls.

Much of the area close to the die is also black - "no return signal." These are regions where excess die

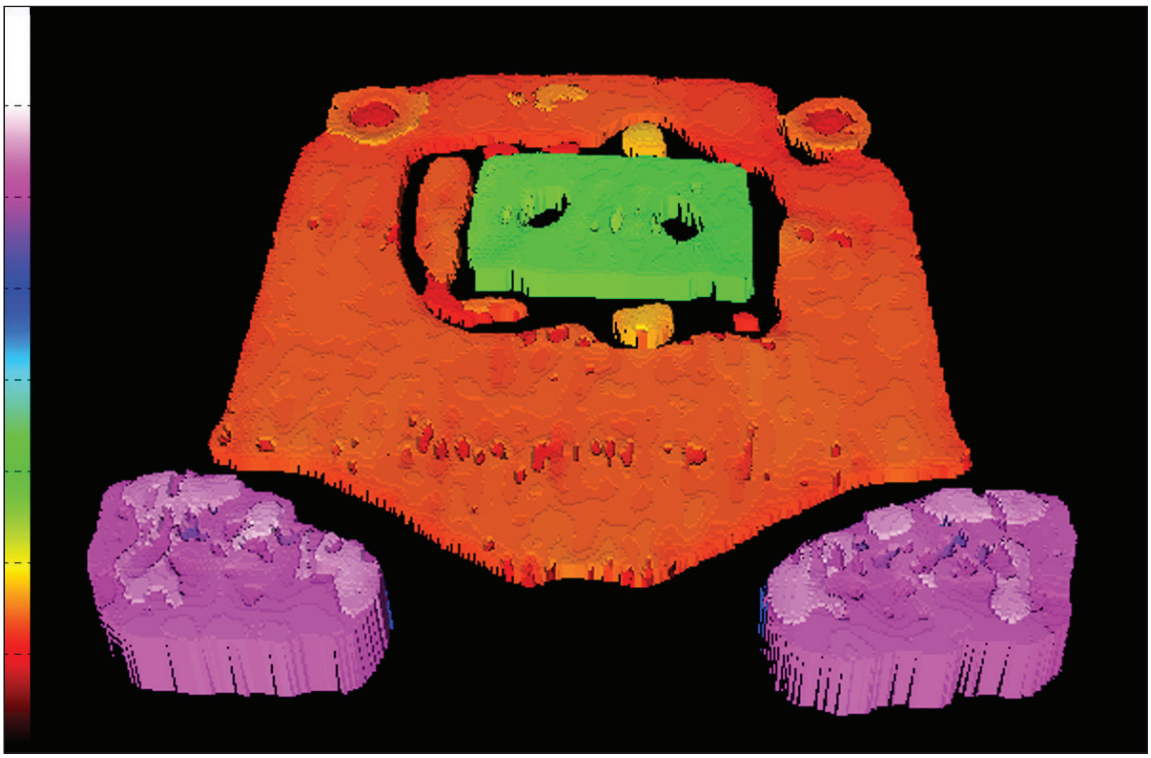

Figure 3: Acoustic image of the same package, but including the leads.

attach material has been extruded from beneath the die and formed steep mounds. Since the mounds are not flat, ultrasound from the transducer was again scattered and no signal was received. The isolated orange island to the left of the die is more or less flat and represents a delamination of the mold compound from the heat sink. A thin delamination in this location would agree with the x-ray image, which shows no feature here because a delamination would be invisible to x-ray.

At the far end of the orange heat sink are two more or less circular features that are slightly paler orange. These are mold marks in the mold compound just above the heat sink. Running horizontally across the heat sink near the pink leads is a rather straight row of small marks. Their arrangement and their small size suggest that they are not some strange type of defect in the heat sink, but are more likely the acoustic shadows of alphanumerics on (and penetrated into) the surface of the package; i.e., echoes returning from the heat sink that were slightly distorted by the alphanumerics.

The highest features in the image of this TO-220 are the two pink leads. These are the ends of the long, straight leads that extend much farther out of the component package. As with the die and other items, software has used the height-reporting color of the top surface to give the leads side walls; they are actually thinner than they appear to be here.

Taken together, the two 3D images tell a great deal about this TO-220. Ultrasound found a probable delamination; x-ray found suspicious dark features. Both ultrasound and x-ray can also image a sample in multiple progressive horizontal slices: each slice creates its own image, and the result is much like a slide show through the sample, one user-defined layer at a time. As with the 3D images shown here, the two sets of images give a very thorough picture of internal structure.

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End-to-end data management essential to meet reliability requirements of **automotive electronics**

Automobile manufacturers need more robust electronic systems. Yet chip suppliers pursuing this opportunity face a dilemma: quality controls optimized for consumer electronics can't deliver in a sector where products must function for years, not months. Rudolph Technologies explains why advanced data management is key to future success.

BY MIKE MCINTYRE; DIRECTOR, SOFTWARE PRODUCT MANAGEMENT; RUDOLPH TECHNOLOGIES

THE RAPIDLY INCREASING electronic content in automotive applications has revealed tremendous differences in reliability expectations between two industries. Car makers think of lifetimes in tens of years while electronics may become obsolete in tens of months. The automotive market will certainly not adopt the limited expectations of the electronics consumer and so the onus is on the electronics industry to improve reliability and extend product lifetimes.

Electronics manufacturers, who have grown up in an environment driven by process yield, must shift their focus to product reliability. For suppliers of inspection and metrology systems this shift will manifest in at least two important areas, system performance and data management. To tighten process control and reduce defects, measurement systems must be more precise and inspection systems more sensitive.

The increase in metrology and inspection required to improve reliability will generate a tsunami of data that must be collected, stored, and analyzed to extract actionable information. Most importantly, electronics manufacturers will require data management systems that provide die level traceability across an increasingly complex supply chain. Although semiconductor manufacturers have long collected large volumes of data, as much as 90% of it has typically lain dormant, never to be interrogated. Some projections of activity in an advanced datastore more than flip that number, estimating as much 99% of data will be actively mined. One of the biggest challenges may be cultural, persuading individual suppliers to interact and provide access to data on a “trusted source” basis.

For most of its history the automobile industry’s reliability concerns have focused primarily on mechanical systems. That focus is changing rapidly as the electronic content of cars comprises a rapidly increasing share of value, and the number of electronic components, each a potential point of failure, grows at an exponential rate. If devices are counted at the individual transistor level, the number quickly becomes astronomical. Device failure rates of one in a million are not adequate and even one in a billion can yield unacceptable levels of system failure. Though zero-defect quality control may not be achievable in a literal sense, the term captures the essential premise of a continuous improvement program in which no level of failure is acceptable.

The automotive industry has well-developed systems for testing and quality assurance. Components are expected to work for 18 years in a dirty, harsh environment with substantial vibration and wide temperature swings. In a mechanical system with hundreds or thousands of parts, failure rates in the parts-per-million range are not excessive. The electronics industry also has exacting requirements for quality and control, but historically it has focused on increasing the yield of functional devices at the end of the manufacturing process. Relatively short product lifetime requirements have put less emphasis on long-term reliability, and most electronic components are designed to operate in a relatively benign and well controlled environment.

Product liability is another important difference between the industries. Few consumer electronic products carry the significant risks to the health and safety of the user found in automotive applications. An

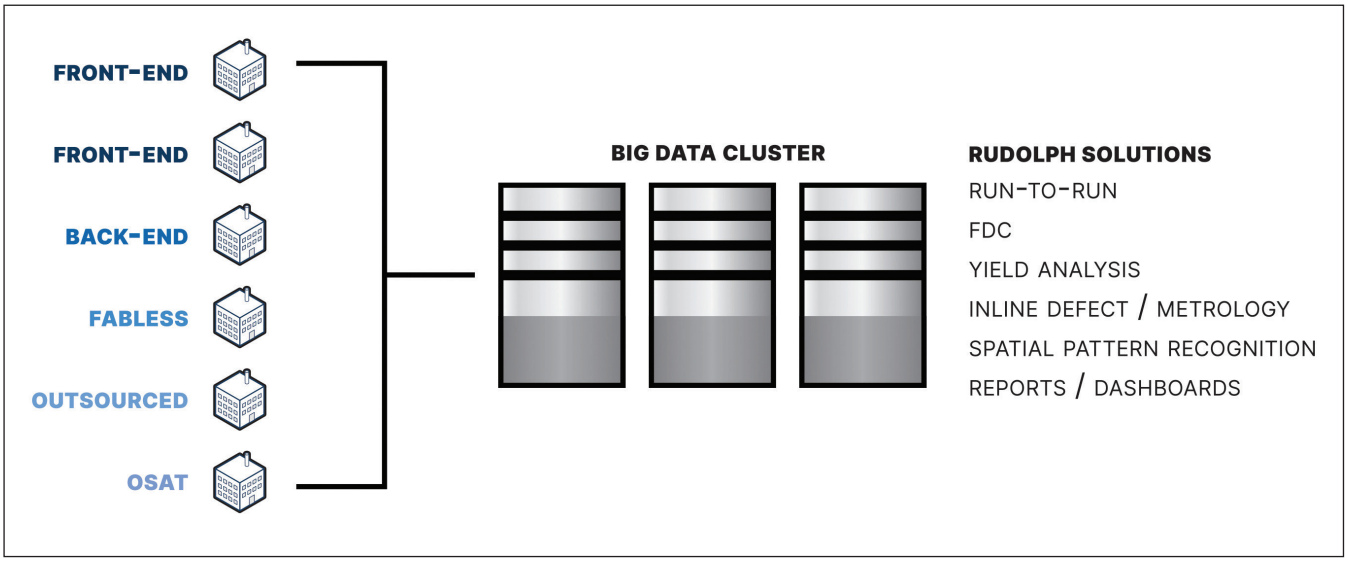


Fig 1. Data collection and management across an increasingly complex electronics manufacturing supply chain requires warehousing of data in a central integrated database where disparate data structures are pre-aligned to permit fast, thorough analysis and extraction of actionable data.

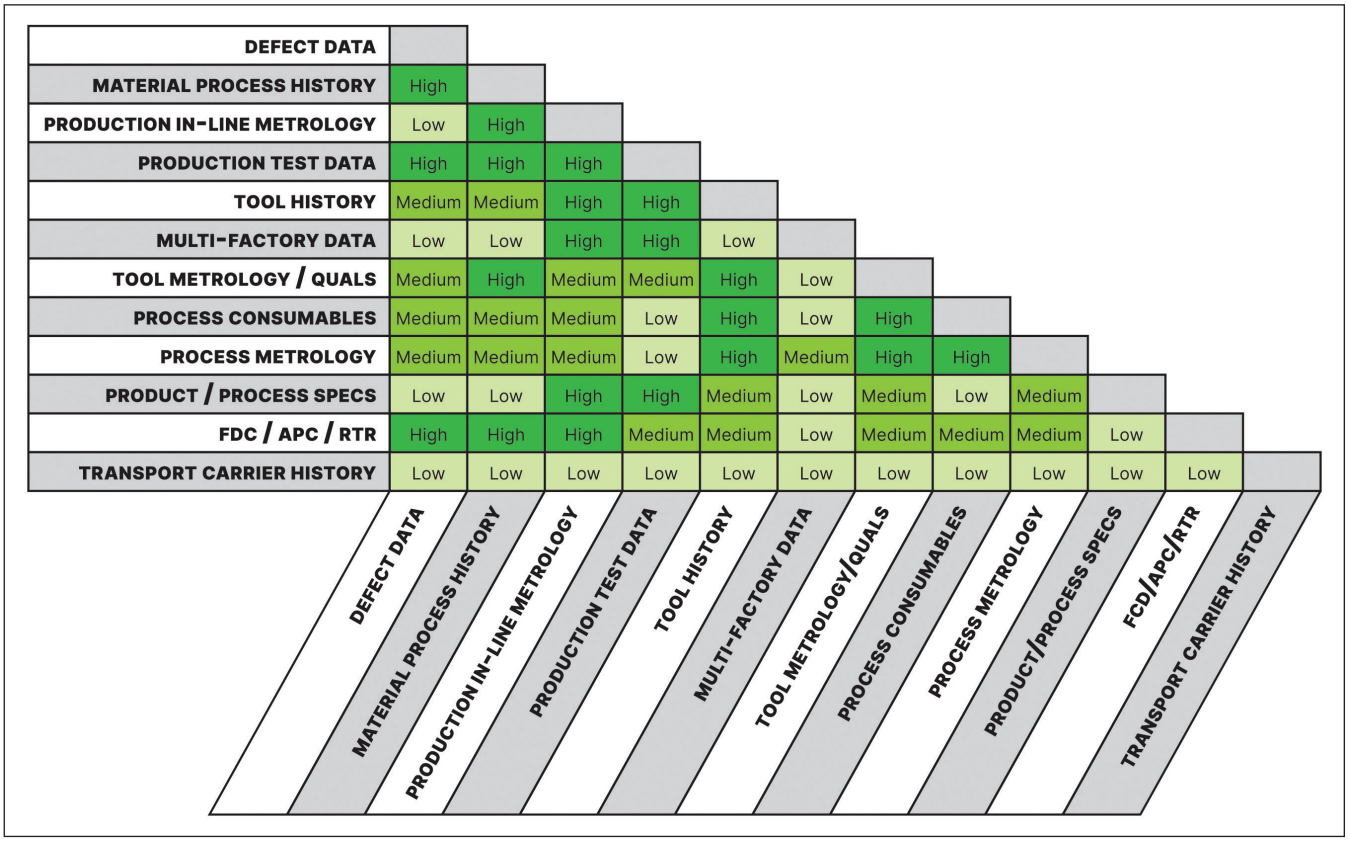


Fig 2. The importance of integrated access to pre-aligned data from a variety of sources is emphasized by this chart which shows the likelihood – high, medium, or low – that data from any two sources will interact in a fab-wide problem-solving scenario.

aspect of product liability more unique to electronic assemblies derives from the somewhat monolithic nature of the finished component. The assembly may consist of multiple die and millions of transistors that are not individually repairable. If the assembly fails all these components are lost. The financial liability for the failure passes upstream, so that a supplier of a defective die may ultimately be held liable for the cost of the entire assembly. This model may work for a phone or smart watch but will not work for an automobile.

Current trends will only increase emphasis on reliability. While the number of electronic components and their share of value are increasing rapidly, experts also point to changing patterns of usage. Today an automobile typically spends most of its time parked, unused. If we move to an era of autonomous vehicles summoned on-demand from a shared pool, usage may approach 100%, with vehicles travelling hundreds of thousands of miles in a year.

To meet these challenges the electronics industry will have to make a fundamental shift in focus from process yield to product reliability. In an environment where the cost of reliability failure far exceeds the cost of yield loss, reliability and testing approaches that scrap nominally acceptable parts may be adopted more widely. Examples include guard-banding, where devices are scraped simply because they are located near a known defect, and part-averaging, which rejects statistical outliers even if they fall within process control limits. Process engineers and inspection and measurement system suppliers must focus on understanding the underlying causes of reliability failures with ever tighter process control, more precise measurements and more sensitive inspection. In addition, electronics manufacturers will need end-to-end process control with data management tools that provide detailed visibility across a supply chain that will certainly grow more complex.

Returns containment

Once a failed part returned from the field has been analyzed to determine the cause of the failure, automotive manufacturers must quickly determine what other vehicles contain parts likely to fail for the same or related causes. Die-level traceability, sometimes called genealogy, allows engineers to look back throughout the production process to find die with similar characteristics or history. These may include common material lots, processing equipment, events, timing, location, manufacturing plant, shipper, and more – the list is nearly endless.

Data sources may include defect detection, yield analysis, automated process control, and fault detection and classification systems, all from different manufacturers. Engineers are confronted by numerous challenges, including the amount of data, differences in data formats, and access to the data at different entities in the supply chain. An efficient solution requires an integrated database

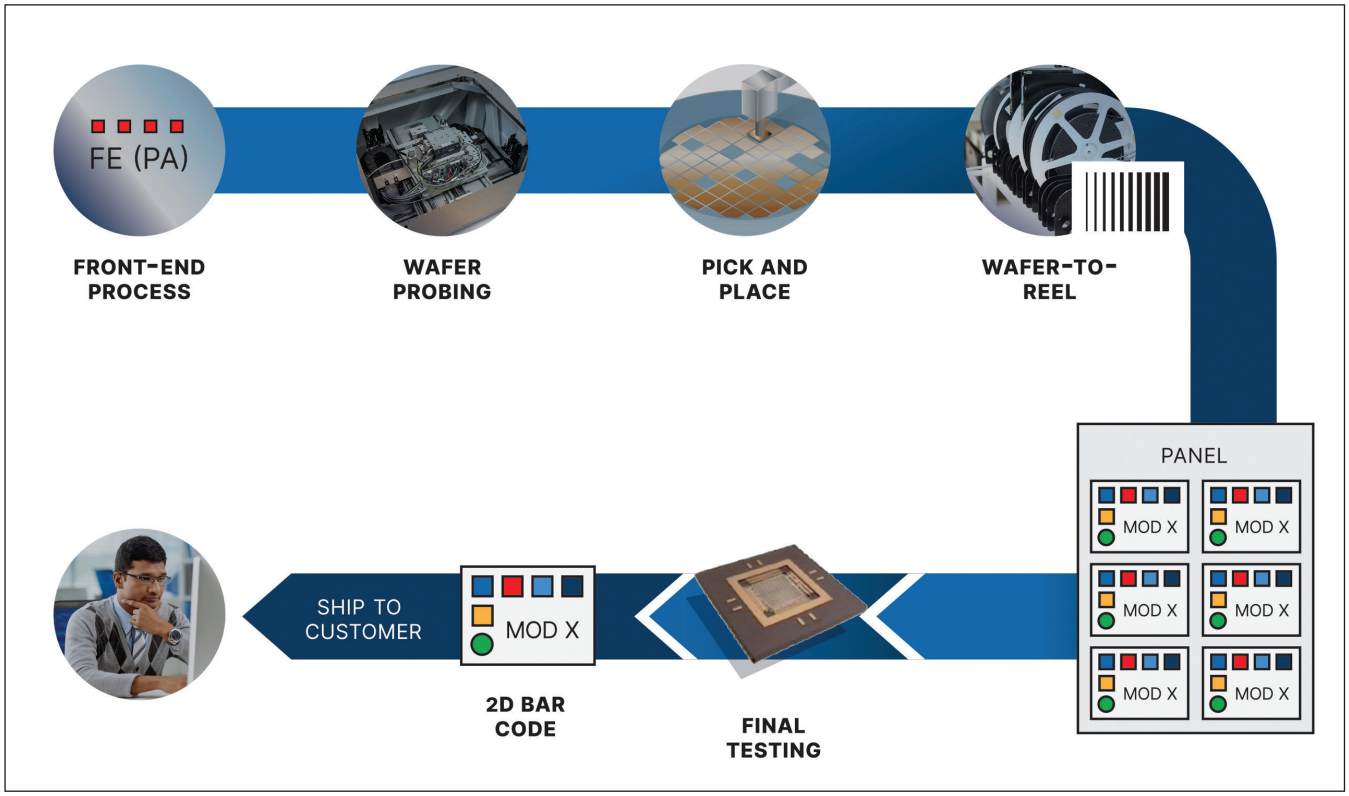


Figure 3. Die level traceability requires tracking of individual die as they are configured and reconfigured at various steps in the manufacturing process – from wafer to reel to panel to module – with each reconfiguration often occurring at a different supplier.

with high speed and large capacity and the ability to pre-align data from disparate sources to facilitate algorithmic searches for significant correlations. When common factors are found and at-risk die identified, manufacturers can minimize their costs and liability by issuing a recall for those vehicles and only those vehicles likely to be affected.

Corner case identification

Engineers routinely test products and processes to determine acceptable limits for variables. A variable near the limit is known as an edge case. The problem becomes more challenging when there are multiple interacting variables. Extending the edge metaphor to multivariate analysis, cases where variables in multiple dimensions are near their limits are known as corner cases. In low risk applications, corner cases may receive less attention, on the presumption that the likelihood that a component will encounter a situation where multiple conditions are near their limits is low.

In automotive applications, where the cost of failure can be high because of risks to the health and safety of the operator, corner cases are much more important. For every failure, engineers will want to know if this is a corner case they have not seen before. While the analogy of a two-dimensional corner is easy to appreciate, finding a "corner" as the number of variables/dimensions increases becomes more challenging. The ability to recognize when a part or module fails at a never validated corner in a multivariate parameter space is essential in preventing escapes.

Guard banding

In conventional engineering, guard banding refers to establishing a zone around a specification limit equal to some proportion of the measurement system's precision. For this reason, the capabilities of measurement and inspection systems must be well

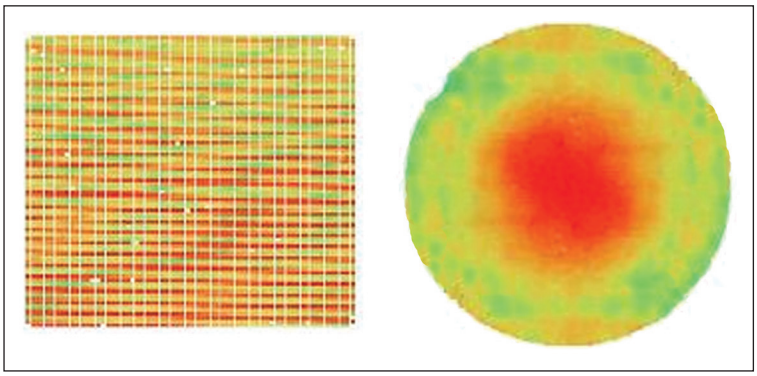
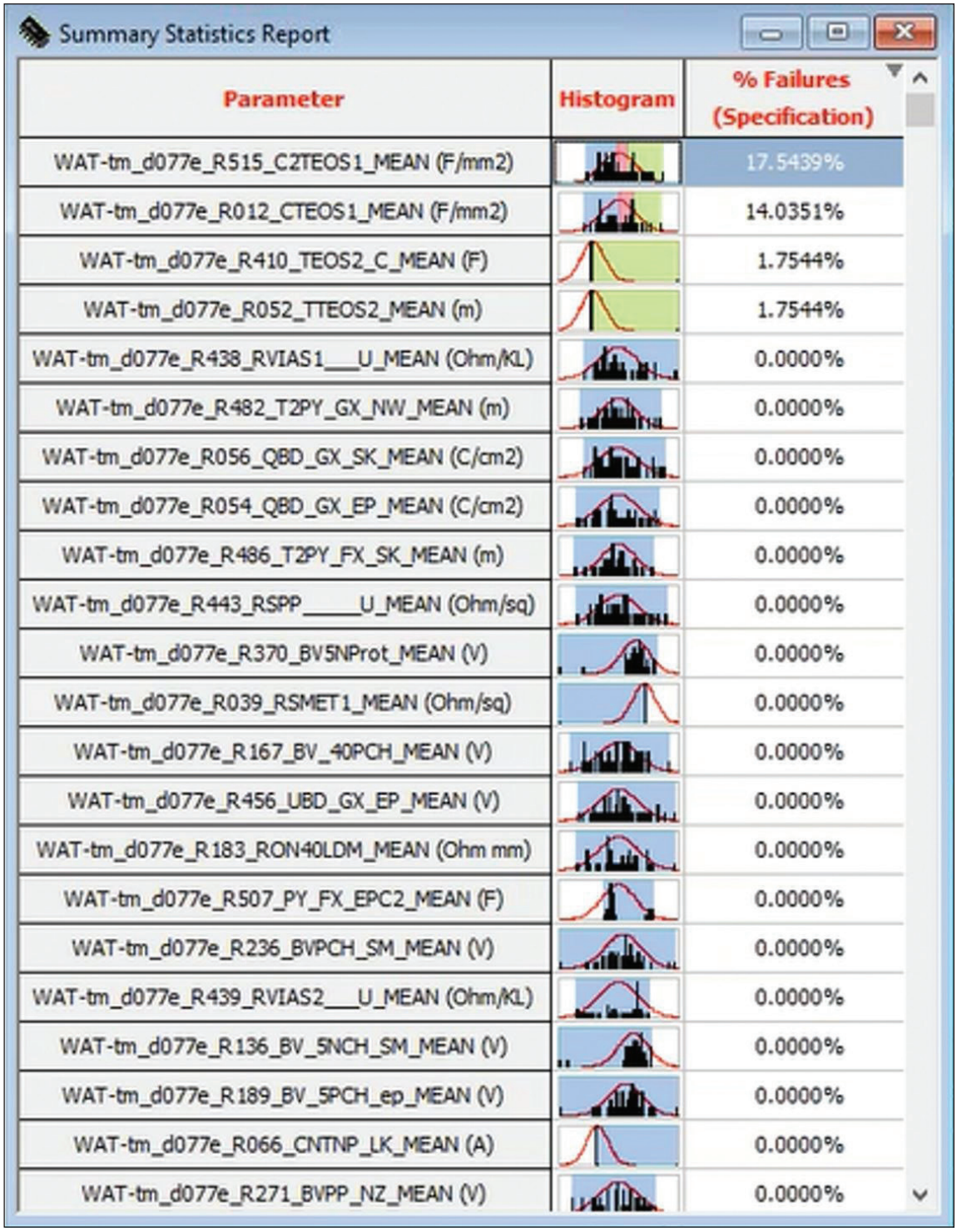


Figure 4. Back mapping can reveal spatial relationships that are not obvious. Engineers observed a characteristic striped pattern in visual displays of test results from panel die. Back mapping results showed original wafer die locations that revealed a front-end process issue. A similar approach can identify die at risk of failure.

Figure 5. This list is an example of the large number of variables that must be monitored. Automated routines can constantly mine an integrated datastore to find new corners.



characterized, with error bars or some other graphic representation of precision included in all results. Guard banding has also been used in semiconductor engineering to refer to the practice of including additional, redundant circuitry to ensure that failure of a single device does not cause failure of the whole circuit. More relevant to this discussion is geometric guard banding, where a die may be scrapped simply because it is located near a detected defect on a wafer.

For example, die immediately adjacent to a scratch or several die in the extended direction of a scratch may be rejected on the presumption that they are more likely to fail. In these cases, the potential cost of failure is judged to be higher than the cost of yield loss.

Adaptive sampling

There is a constant tension between throughput and measurement/inspection requirements. Time spent on these functions is, in the strictest sense, non-

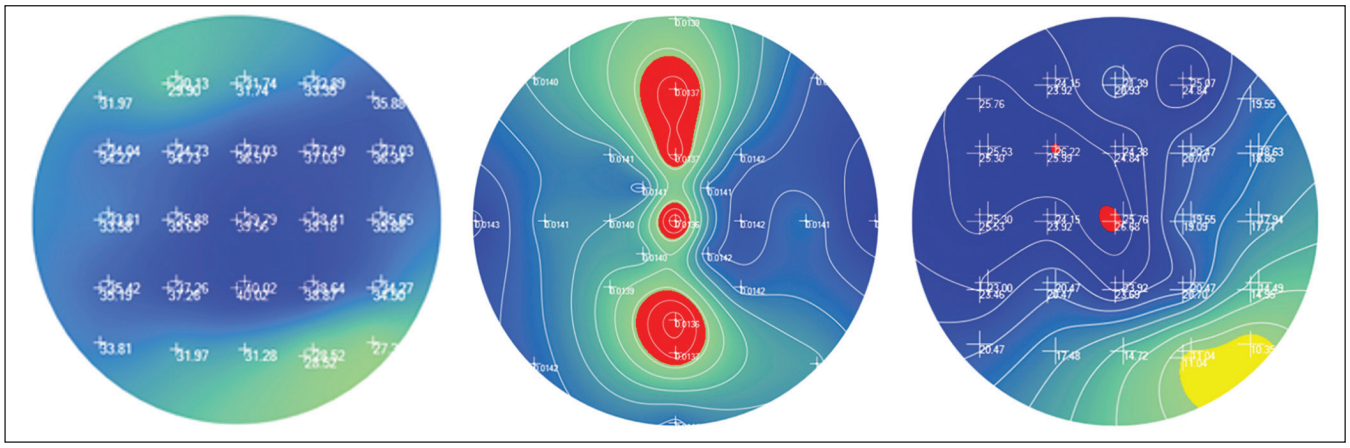


Figure 6. Adaptive sampling adjusts sampling rates in response to measured values to optimize the trade-off between measurement and throughput.

productive, but it is essential in maximizing the yield of good devices and their reliability. Adaptive sampling seeks to optimize the trade-off by dynamically adapting the sampling rate or density in response to highly variable measurement results. Figure 6 shows an example where the sampling density would be changed from one wafer to the next based on the variability of sample measurements. As demonstrated in Figure 6, these wafer maps utilize continuous color to show the actual variation of the measured parameter (unknown to the measurement system.) The white numbers show sampled values measured at specific locations. Given the underlying uniformity of the left wafer, the measurements would show little variability, providing high confidence that they are representative of all points on the wafer. On the middle and right wafer, the sampled measurements show greater variability, suggesting the need for increased sampling density to completely characterize the full wafer and provide confidence that all points fall within acceptable limits.

Part average testing

Part average testing (PAT) is a technique developed by automotive manufacturers. It is another example of a practice that discards nominally good parts judged to be at higher risk of failure. In part average testing, die that meet specification but fall outside the normal distribution of their cohort population are rejected.

Conclusion

Electronic and automotive manufacturers have historically had different expectations for product reliability. The increasing electronic content of automobiles will require electronics manufacturers to dramatically increase product lifetimes and reliability in much more demanding environments. Key to their ability to do so will be the intelligent use of process data. Major challenges that must be addressed include accommodating massive data volumes, aligning disparate data structures in an integrated datastore, and developing trusted relationships with data sources across a complex supply chain. We have described several examples of the use of advanced data analysis and data mining to address the reliability needs of the automotive market, including return containment, corner case identification, adaptive sampling and part average testing. All these techniques and more will be necessary to drive automotive electronics into the quality and reliability space required by car manufacturers and their customers.

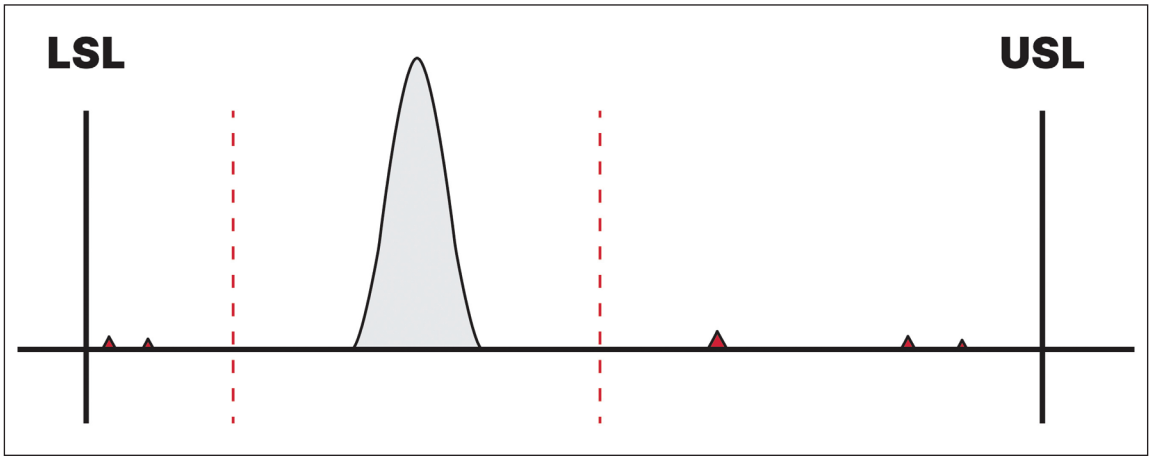


Figure 7 For static part average testing (PAT) the normal distribution is taken from a representative sample spanning several lots and is refreshed periodically. For dynamic PAT the normal distribution is calculated from a rolling sample of recently tested parts.

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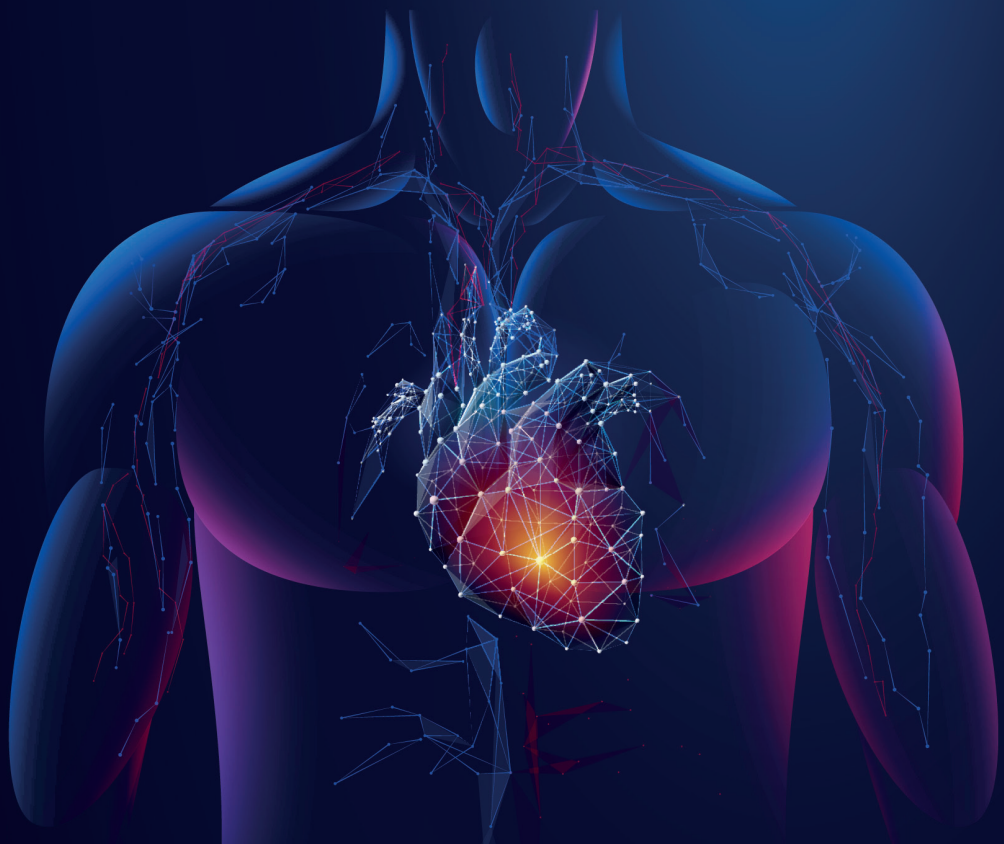


Prototype screening device leverages silicon photonics to detect cardiovascular diseases

The successful EU-funded CARDIS project created a better means to diagnose and treat one of humanity's greatest health threats: cardiovascular disease (CVD). The handheld prototypes, now in clinical trials, leverage advanced sensors to deliver results accurately while being faster and simpler than legacy tools. PIC Magazine invited Prof. Dr. Roel Baets, principal researcher and project coordinator, to speak about ways that CARDIS points to the future of healthcare.

By Roel Baets, Professor at Ghent University (Belgium) and associated with imec

EACH YEAR, cardiovascular diseases (CVDs) are responsible for 30% of deaths worldwide. Key to reducing their impact (i.e. to avoid hospitalization and reduce CVD morbidity and mortality rates) are tools and devices that help general practitioners and paramedical personnel diagnose CVDs in an early stage.

Current CVD risk assessment methods are largely based on clinical judgment and traditional vital signs measurements (heart and respiratory rate, blood pressure, etc.). More ideally, however, those vital sign measurements should be complemented with new biomarkers such as pulse wave velocity (PWV) to get to a more accurate diagnosis. Adding PWV data – an important biomarker for arterial stiffness – is regarded as a very important first step to improving diagnoses. However, no tools are available today to easily screen large numbers of patients' PWV at doctors' offices.

In this context, and within the scope of the recently finished European H2020 CARDIS project, researchers have developed a mobile (handheld) and low-cost point-of-care CVD screening device based on silicon photonics. This device measures a patient's pulse wave velocity in a fast, reproducible and reliable way. A medical screening using the CARDIS device is non-invasive and requires minimal operator skills. Putting the prototype's capabilities and performance to the test, a clinical feasibility study with 100 patients has already successfully been completed at the Georges Pompidou European Hospital in Paris (France).

Challenging the gold standard to measure pulse wave velocity (PWV) in the arteries

Pulse wave velocity is defined as the velocity at which pressure waves, generated by the contraction of the heart, propagate along the arterial tree. It is an important marker for the stiffness of the arteries and can complement more traditional clinical parameters (e.g. blood pressure) to assess the risk of developing conditions such as atherosclerosis (with plaque – such as fat, cholesterol or calcium – building up inside one's arteries, over time hardening and narrowing those arteries) and arteriosclerosis (the thickening and hardening of the artery walls).

Today's gold standard to measure one's pulse wave velocity relies upon pressure sensors being placed over the carotid artery in the neck and the femoral artery in the groin to measure the speed with which pulse waves travel down the aorta. Such PWV measurements, however, come with quite some drawbacks: it is a pretty cumbersome approach and does not allow for a quick and easy screening of large numbers of patients. Moreover, it only provides the average PWV over a long segment of arteries (each having different mechanical characteristics) – meaning that it cannot be used to evaluate arterial stiffness in a small area; nor will it give information about the exact location of any arterial abnormalities.

Prototype medical device to perform LaserDoppler Vibrometry on a patient's skin to deduce metrics for arterial stiffness and to diagnose cardiovascular diseases

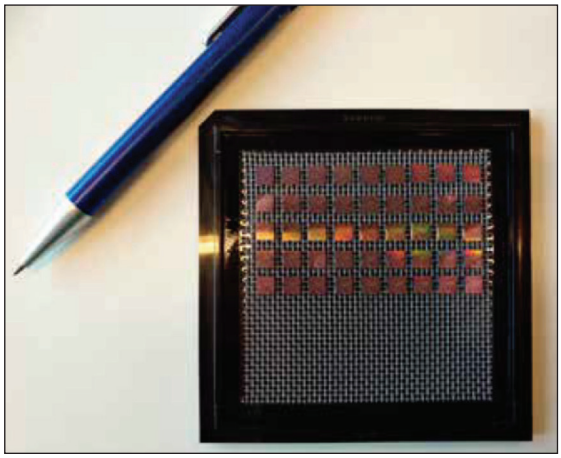
In response to those limitations, the prototype handheld device that has been developed and tested by the CARDIS consortium measures pulse wave velocity more locally – making for a quick and easily reproducible assessment, while still allowing for the carotid-femoral measurement.

Leveraging the compactness and cost-effectiveness of silicon photonics

The CARDIS prototype device makes use of multi-beam Laser Doppler Vibrometry (LDV), whereby a set of low-power laser beams are shone onto the skin above the carotid artery of the patient. The power level is so low (well below 1 mW) that it is completely harmless to the eye and skin. The reflected light is Doppler shifted in optical frequency due to the tiny movements of the skin above the artery as a result of the heartbeat. By doing measurements at multiple locations, the PWV can be deduced.

The new CARDIS device is very compact because it makes use of silicon photonics for the basic LDV engine, allowing the hardware to be miniaturized to a handheld device.

The photonic chips which are at the heart of the system have been designed and manufactured at imec using the silicon photonics iSiPP50G process – including passive functions, modulation and switch functions as well as germanium detectors. The chip is co-assembled with a micro-optic bench holding a 1550nm single mode laser, a miniature optical isolator and coupling structures to the chip. The packaging



The photonic chip, key in realising the handheld device for measuring arterial stiffness

of the photonic chip was executed at Tyndall National Institute (Cork, Ireland).

Imec's integrated Silicon Photonics Platform co-integrates a wide variety of passive and active components, thus enabling competitive photonic integrated circuits for a broad range of functionalities and markets – including data centers, telecom, sensors, LIDAR, etc. As demonstrated in the CARDIS use-case, silicon photonics makes a huge difference when a device needs to be miniaturized to the extreme, or when the device – as in the case of a point-of-care device – needs to be optimized with respect to cost; but also when reliable manufacturing and/or large volume production is needed.

Putting the prototype to the test during a clinical feasibility study

The CARDIS prototype has been put to the test during a clinical feasibility study with 100 patients at the Georges Pompidou European Hospital in Paris, whereby a substantial clinical dataset has been collected – both from healthy subjects as well as from patients with cardiovascular conditions.

The quality of the device's readings was found to be very good and adequate measurement results could be obtained in all subjects. When using the device in a carotid-femoral mode, the measurement data as well as the variability within sessions were in line with those acquired by reference techniques. That being said, the local carotid measurement approach is substantially more demanding with respect to the algorithms to extract robust PWV-numbers – so further optimization is still needed.

According to the cardiologist in charge of the feasibility study, the CARDIS device was well accepted by all patients, and considered useful by the medical staff. The team noted that a useful signal was acquired in 100% of the patients. Tolerance was excellent too, the time to get useful signals was less than 10 minutes, and patients barely noticed that a measurement was performed.

Technological and medical next steps

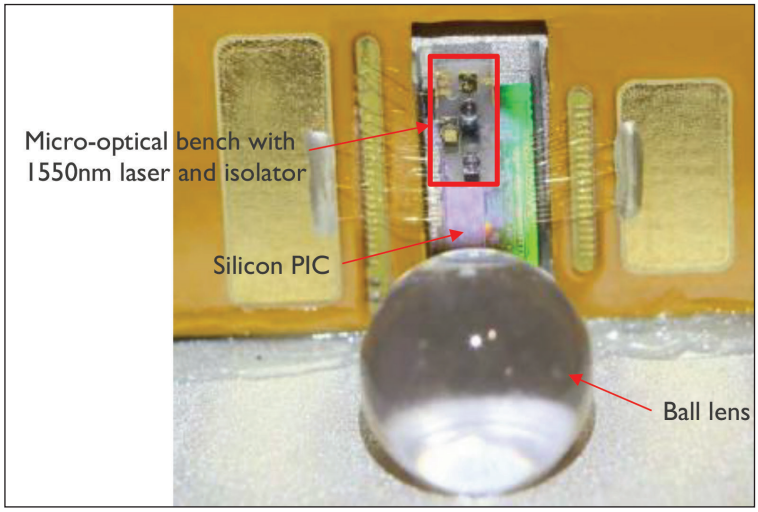
The team's future plans are two-fold. At the technological level, they want to continue to improve and optimize the user-friendliness of the device – for instance by making it completely wireless and substantially lighter and smaller. At the medical level, the data provided by the CARDIS device will be validated more in-depth against other methods.

To this end, the algorithms used to convert the LDV signals in relevant and robust medical markers will be finetuned up to the point where they will allow for diagnostic and therapeutic decision-making.

In a next step, a small series of prototype devices will be produced to perform a clinical feasibility study on a larger group of patients over a longer period of time. If this feasibility study demonstrates the technology's ability to detect cardiovascular diseases at an early stage, high volume production can be initiated. Again, one of the benefits of the silicon photonics technology is that – at high volumes – the chip can be produced at low cost.

It is worth noting that Laser Doppler Vibrometry (LDV) can support a wealth of other applications beyond the medical case described here. It can be used for structural monitoring of critical infrastructure (e.g. bridges), to capture acoustic signals, and much more. For many of those applications, miniaturization and cost are key to their widespread introduction. As such, the future of LDV, enabled by silicon photonics, looks bright!

About CARDIS: *The H2020 CARDIS project consortium includes a variety of partners – from widely acknowledged universities to leading technology companies: Ghent University, imec, INSERM, Maastricht University, Medtronic, QMUL, SIOS and Tyndall. The project was coordinated by Fundico.*



Packaged silicon photonic chip with co-assembled laser source, optical isolator and ball lens for coupling light back and forth to the patient's skin.

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Silicon photonics market growth depends on maturing processes and overcoming TAP challenges

Initial optimism over Silicon Photonics (SiP) potential to unseat incumbent transceiver and switch technologies suffers today from the years it took process tool and TAP manufacturers to adapt CMOS hardware to the eccentric needs of photonic device manufacturing. CEA-Leti experts delve into potential remedies that could be the tonic SiP needs to lead in short- and medium-reach applications.

By Daivid Fowler[a], Phillipe Grosse[a], Stéphane Bernabé[a], Fabien Gays[a], Bertrand Szelag[a], Charles Baudot[c], Nathalie Vuillet[b], Jonathan Planchot[b] and Frederic Boeuf[b] CEA-Leti, Grenoble, France[a], STMicroelectronics, Crolles, France[b], ACCIENA, Québec, Canada[c]

FOLLOWING the initial demonstrations of silicon-based photonic devices in the 1990s[1], the suggestion that photonic integrated circuits (PICs) could be cheaply and reliably mass-produced using existing CMOS infrastructure led to optimism that this technology could rapidly supplant established technologies for short-to-medium range digital communications[2]. Today, silicon-photonics based transceivers are gaining market share, especially for single-mode fibre-based interconnects in hyper-scale data-centres. Several companies like Intel and Cisco have significantly invested a lot of technology, putting 100 Gbps modules on the market while beginning to roll out 400 Gbps versions.

However, silicon photonics is still competing with VCSELs for short range (<300m) and with InP-based modules for Inter Data-Centre interconnects, resulting in fewer sales than expected a decade ago. This is despite the increasing number of Si-based photonic components and circuitry with demonstrated performance comparable to, or in excess of, equivalent discrete optical components. One of the reasons behind this delay may have been the initial time to develop a photonic-specific fabrication process, as well as the availability of key software and hardware for simulation, layout and test that must be heavily adapted with respect to standard CMOS electronics infrastructure.

At CEA-Leti, whose role is to develop emerging technologies for transfer to industry, our silicon photonics program has been working to this end with numerous academic and industrial partners (e.g. within the IRT Nanoelec program) since from about 2005.

Among the various components we have developed, the fibre grating coupler (FGC) illustrates this situation very well. This structure is used to couple light from the PIC to an optical fibre, and its performance in terms of insertion loss (IL) is a key specification for allowing Si-photonic transceivers to compete with other technologies. Indeed, one of the unique challenges to creating low-cost silicon-photonic transceivers is an efficient means to couple light from a single-mode fibre with a mode field diameter of ~10μm, to an on-chip mono-mode Si waveguide, which due to the large optical index contrast of Si/SiO_2 has a mode size of just several hundred nanometric. Indeed, this mode size mismatch is at the origin of a significant cost both monetarily and in terms of

optical losses related to fibre coupling to Si-based PICs. Several solutions exist, but the use of diffraction-grating-based fibre couplers is well established due to the convenience of wafer-scale testing and relatively large alignment tolerances[3].

Figure 1 shows the general architecture of a recent version of the CEA-Leti O/C band fibre grating coupler [4]. It is composed of 310nm-thick SOI on a 1500nm BOX layer, partially etched to 160nm and fully encapsulated in SiO_2. Input guided light is diffracted by a series of pits, narrow and wide trenches towards an out-of-plane single mode fibre placed at 8° to the vertical. The non-uniform, curved diffraction grating is carefully optimised using Finite-Difference Time Domain (FDTD) simulation so that the output optical field best overlaps the Gaussian mode profile of the fibre, in order to decrease mode-matching losses. The minimum pit size is ~110nmx140nm and the minimum continuous trench width is 120nm. The fabrication process uses (non-immersion) 193nm lithography on 300mm wafers, with a CMOS equivalent node-size of 65nm.

Although the minimum feature size is significantly in excess of the notional minimum critical dimension of the lithography, this collection of non-rectilinear geometrical features of widely varying size, creates particular challenges for device fabrication with technology derived from CMOS electronics. Firstly, layout files entering a CMOS foundry environment undergo automatic 'Design Rule Checking' (DRC) to alert the designer to errors as well as to highlight design aspects that are not compatible with subsequent stages of fabrication. Until the recent emergence of DRC tools with 'equation-based' algorithms (e.g. Calibre nmDRC from Mentor Graphics), access to CMOS foundries has relied on the adaptation of DRC software designed for the 'Manhattan' layouts found in electronics. Owing to the wide variety of shapes and sizes of photonic structures, at CEA-Leti, we have incrementally developed a DRC that applies component specific rule subsets, one of which applies directly to our fibre grating couplers.

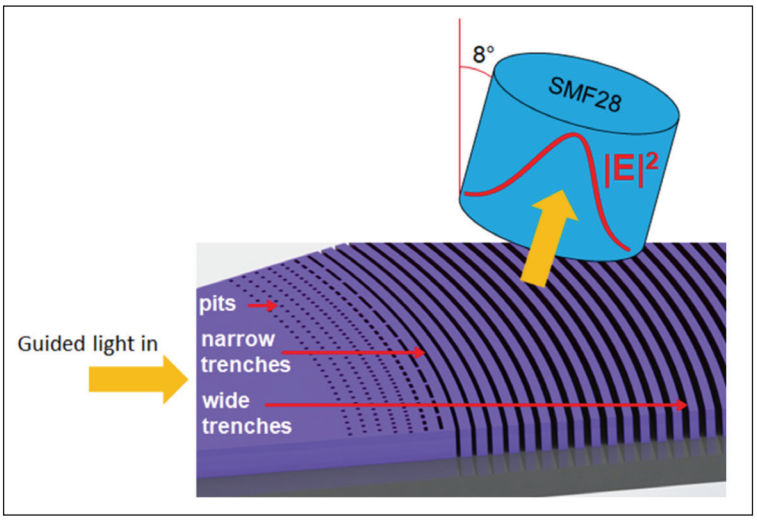

Figure 1. General architecture of the CEA-Leti O-band fibre grating coupler. Incoming guided light is scattered by a non-uniform, curved diffraction grating into a single mode fibre placed above at 8° to the vertical.

Once past the DRC stage, the target design layout must then undergo a post treatment process designed to compensate for unavoidable geometric distortions induced by the fabrication process. This treatment is known as Optical Proximity Correction (OPC) and is routinely applied in the CMOS industry. However, as for DRC, off-the-shelf OPC software is based on algorithms optimised for Manhattan-style electronic structures and is not well suited to the curvilinear structures found in photonics[5].

Figure 2a shows an image of a grating coupler, fabricated in 2013, with a similar design to that in Figure 1, using nominal process conditions on a platform without OPC. The pits are not present and the finest trenches are poorly defined. Figure 2b shows a typical layout before and after OPC (grey boxes and black lines, respectively), as well as the simulated result of the etched grating structure (red boxes). Figure 3 shows a later fabrication run with

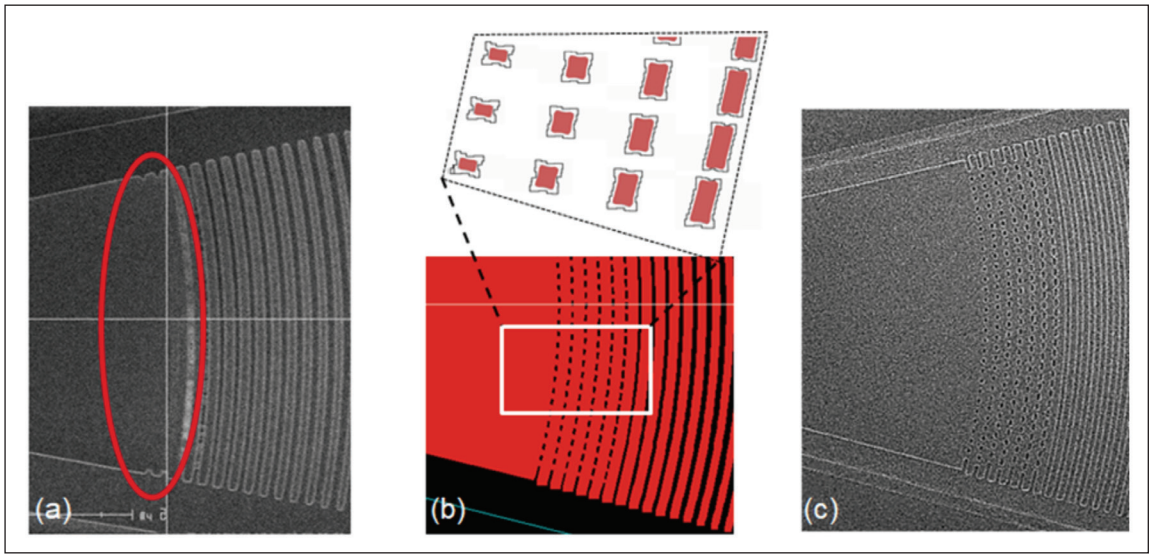

Figure 2a. Image of device fabricated in 2013 without OPC treatment, with missing features. 2b. OPC treatment of target design, the black lines show the post-OPC layout. 2c. Image of device fabricated in 2018 using OPC.

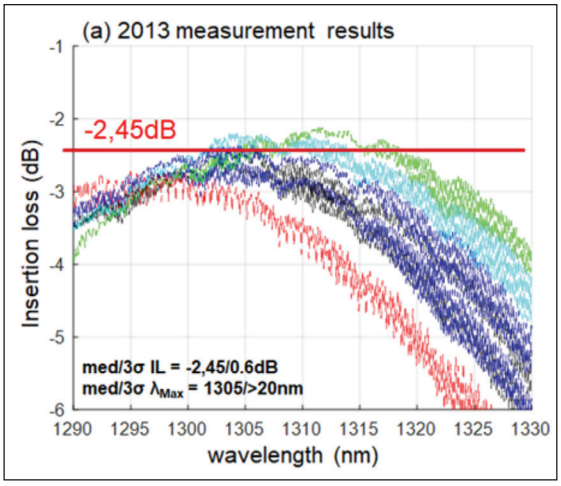

Figure 3a. CEA-Leti fibre coupler Insertion loss measured in 2013.

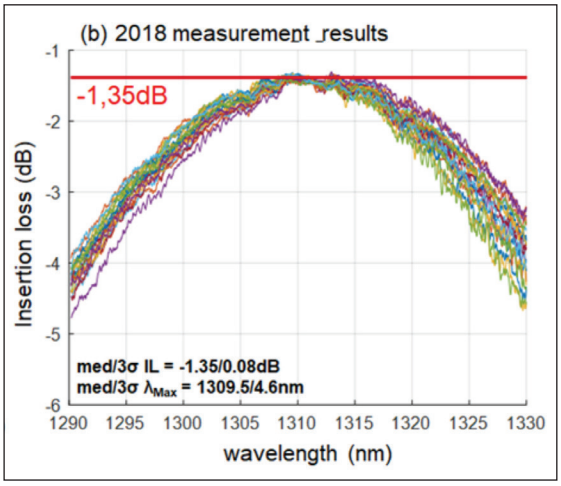

Figure 3b. CEA-Leti fibre coupler insertion loss measured in 2018 following iterative improvements in design, process and testing

an optimized OPC treatment in which the diffraction grating is correctly defined.

Another crucial contribution the development of the fibre grating coupler and of the photonic design-kit in general is a means of precise, reproducible and automated device characterization. Unlike obtaining insertion loss values of other photonic devices in which fibre coupling losses can be subtracted using a suitable reference structure, measuring the insertion loss of the coupling structure itself is subject to greater uncertainty. Like the layout tools described above, dedicated hardware for testing PICs is slowly coming to the market (e.g. www.ficontec.com,www.cascademicrotech.com), but as mentioned previously, achieving automated characterisation is another area where CMOS electronics hardware has had to be significantly modified for photonics applications.

At CEA-Leti, our wafer-scale characterization benches are based on CASCADE prober stations with piezo-mechanic fibre holders, which provide rapid (~100ms) submicron active lateral alignment, together with active fibre height control and polarisation control. We estimate the measurement precision and reproducibility of our system to be around 0.1-0.2dB.

Figure 3a shows a measurement made in 2013 of the IL spectra of our nominal CEA-Leti fibre grating coupler over the wafer surface. The median minimum insertion loss is -2.45dB. A 2018 measurement, shown in figure 3b, shows a marked improvement in IL, with a medium value of 1.35dB. The coupler design was very similar in both cases, the difference is due to enhanced lithographic control and a functioning OPC. Furthermore, the reduced dispersion over the wafer of the minimum insertion loss value (3σ=0.08dB, c.f. 3σ=0.6dB) in the 2018 data can be attributed to a combination of improved process control (notably the stability of the partial etch step) and stability of the measurement system.

Conclusion and prospects

Several key aspects of the development of the CEA-Leti fibre grating coupler have been presented. Using this as a case study, we seek to illustrate just a few of the many ways in which silicon photonics, while using the same set of materials and process techniques as in CMOS electronics, has required, and continues to require, significant development in order to fully exploit the economies of scale available to CMOS electronics.

At CEA-Leti, we are currently introducing immersion lithography to have access to finer lithographic control. This will allow the use of more aggressive grating designs and potentially lower fibre coupling insertion loss.

For more information on CEA-Leti visit: www.leti-cea.com/cea-tech/leti/english/Pages/Applied-Research/Strategic-Axes/optics-photonics.aspx

Further reading

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