SILICON SEMICONDUCTOR

Connecting the Silicon Semiconductor Community

Volume 39 Issue V DECEMBER 2017 @siliconsemi www.siliconsemiconductor.net

See you in 2018

inside News Review, News Analysis, Features, Research Review, and much more...
Free Weekly E News round up go to: www.siliconsemiconductor.net

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

www.EVGroup.com

Laser Debonding Solutions for Advanced Packaging

- High-throughput equipment solution for low-temperature debonding of wafers and panels
- Laser system with minimal consumable costs combined with proprietary optical design for excellent beam reproducibility
- Open adhesive platform – laser debonding solution compatible with several material systems

Visit us at
SEMICON® EUROPA
Booth B1-1424

EVG®850 DB

GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com

editor'sview

By Name, Title

Publishing Editor Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Technical Editor Mark Andrews
Sales Manager Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215
USA Representatives Tom Brun Brun Media tbrun@brunmedia.com +001 724 539-2404
Janice Jenkins jjenkins@brunmedia.com +001 724-929-3550
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214
Circulation Director Jan Smoothy jan.smoothy@angelbc.com +44 (0)1923 690200
Chief Executive Officer Stephen Whitehurst stephen.whitehurst@angelbc.com +44 (0)2476 718970

Directors Bill Dunlop Uprichard – EC, Stephen Whitehurst – CEO, Jan Smoothy – CFO, Jackie Cannon, Scott Adams, Sharon Cowley, Sukhi Bhadal, Jason Holloway.

Published by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK. T: +44 (0)1923 690200 E: ask@angelbc.com

Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. T: +44 (0)2476 718 970 F: +44 (0)2476 718 971 E: info@angelbc.com

Silicon Semiconductor is published four times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £50.00/€60 pa (UK & Europe), £70.00 pa (Outside Europe), $90.00 pa (USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher. Every effort has been made to obtain copyright permission for the material contained in this publication.

Angel Business Communications Ltd will be happy to acknowledge any copyright oversights in a subsequent issue of the publication. Angel Business Communications Ltd © Copyright 2017. All rights reserved. Contents may not be reproduced in whole or part without the written consent of the publishers.

The paper used within this magazine is produced by chain of custody certified manufacturers, guaranteeing sustainable sourcing.
US mailing information: Silicon Semiconductor is published four times a year for a subscription of $90.00 by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts, WD17 1JA, UK. Periodicals postage paid at Rahway, NJ. POSTMASTER: send address changes to: Silicon Semiconductor, c/o Mercury International Ltd, 365 Blair Road, Avenel, NJ 07001.
Printed by: The Manson Group. © Copyright 2017. ISSN 2050-7798 (Print) ISSN 2050-7801 (Online).

VOLUME 39 ISSUE V DECEMBER 2017

CONTENTS

08 **2017 Review: opportunity abounds in year characterised by record growth**

2017 became the year that solid, double-digit growth returned across semiconductor manufacturing as sales surged to all-time highs and hopes remain strong for a bright 2018.

36 **Extending the era of Moore's Law through lower-cost patterning**

Researchers at the University of California at Berkeley and Axcelis Technologies have taken a different approach to extending the Moore's Law era of solid-state transistor evolution.

42 **Automating cleaning processes for quality and volume**

Cleaning process repeatability is often critical to uniform product quality and can enable higher volume production throughput explains JST Manufacturing.

44 **Sophisticated coatings on challenging substrate shapes**

KJLC describe a completely new method of achieving excellent uniformity on both flat and curved surfaces without masks.

50 **Hydrogen in Electronics: Growing applications and consumption**

Hydrogen will play an increasing role in semiconductor manufacturing due to its wide serviceability and importance in extreme ultraviolet (EUV) lithography.

56 **Wafer defects can't hide from Park Systems**

Atomic Force Microscopy (AFM) leader Park Systems has simplified 300mm silicon wafer defect review by automating the process of obtaining high-resolution 3D images, making it faster and simpler than ever before.

62 Wet BATCHSPRAY power device manufacturing

As history tells us, before a solution can be found, a problem must first arise that needs to be solved.

66 Plasma dicing strength in numbers

The demand for smaller electronic products including burgeoning IoT applications has led to new focus on die size and wafer singulation.

72 New wafer dicing approach for silicon carbide devices

With the transition to new substrates like SiC, as well as thinner wafers, smaller feature sizes and larger-size substrates, wafer dicing has evolved into a critical process step that can enhance SiC device yields.

76 Transforming sub-fab service and support to lifecycle management

Edwards Vacuum President Paul Rawlings seeks to transform productivity by changing the way semiconductor manufacturers think about servicing their sub-fab equipment.

80 Designing microfabrication lab equipment with research flexibility in mind

Optimising R&D labs usually involves vendor collaboration and planning to provide required versatility.

84 Automated systems increase wafer lapping and polishing productivity

Logitech’s new automated lapping and polishing systems for almost all substrate materials dramatically increases wafer end productivity by up to 40 percent.

88 Silicon photonics for a post-Moore era

What solutions are in the pipeline to support higher performance devices in a post-Moore era?

96 Using manifold technology to optimize cost of ownership

The management of fluid systems is experiencing a drastic change on how a customer perceives the importance of the component.

98 ME Migration: Don't put your head in the sand

There are numerous reasons why manufacturers don't change their Manufacturing Execution System (MES) but, in many cases, there are also many reasons why they should.

102 Wireless charging poised to go the distance

The benefits of wireless battery recharging over a distance appeared about as likely as jet packs and flying cars until Dialog Semiconductor and Energous Corporation began their quest to cut the cords.

106 Equipnet delivers proactive asset management

Dedicated asset managers offer a means to deal more effectively with the equipment implications of mergers, closures and start-ups across ever-changing global chip markets.

110 Rare gases in electronics: nobility in the gases world

Rare gases offer unique properties essential to advanced semiconductor manufacturing.

116 NXP reveals new power product line solutions

NXP has released a new line of processors and microcontroller solutions for the IoT, low power requirement designs and high performance multimedia applications.

120 Building a portable charger without expensive ASICs or bloated PMICs

Silego Technology explains how a small, flexible chip can be configured just like an ASIC, but allows designers to design and program prototypes in a matter of minutes vs. the weeks needed for true ASICs.

130 Mapping tilt and warp of internal and external component interfaces

Inside an automotive engine control module, a plastic-encapsulated microcircuit is about to fail because of an internal structural problem.

134 Customer focus drives AP&S growth

Ever-changing global manufacturing requirements have driven AP&S expansion programs that give customers access to an industry-leading suite of wet processing and metal lift-off tools.

140 Chips with fingerprints make the connected world safer

Chip biometrics form one of the cornerstones of imec's research into a tight and lightweight hardware security that should help ensure the security and privacy of billions of future IoT devices.

144 Why ultrathin power semiconductors call for advanced inspection process control

Thin and ultrathin ICs are in high demand, but yield that sacrifices reliability has little value. Inspection process control can be the solution,

148 Reno Sub-Systems sets pace in plasma process control

Unconventional startup Reno Sub-Systems demonstrates that its performance advances in plasma process control is winning over global semiconductor manufacturers.

152 3D SoC Improve circuit size, cost and performance by repartitioning

3D integration has evolved into economically interesting alternatives to traditional 2D design.

156 Speed IoT product development and reduce risk with outsourced operations

New manufacturing techniques and device-level security measures can bring secure Internet of Things (IoT) devices to market more rapidly than ever before.

160 Flexible hybrid electronics: a new paradigm for semiconductors

As printed electronic circuits continue to evolve, the NextFlex consortium promotes a hybrid approach to accelerate the development and commercial viability of flexible ICs and systems.

Opportunity abounds in year characterized by record growth

2017 became the year that solid, double-digit growth returned across semiconductor manufacturing as sales surged to all-time highs and hopes remain strong for a bright 2018.
By Mark Andrews, Technical editor.

SALES across almost all segments of the global semiconductor market surged to new highs throughout 2017 as worries over the sustainability of 2016 momentum evaporated. Growth of end user/consumer device sales, ongoing new fab construction in China and a surge in process tool sales led indices to new highs as manufacturers simultaneously celebrated growth and hoped for continued health in the New Year.

While 2016 could be described as a recovery year in which signs of steady growth returned in third and fourth quarters, 2017 has focused on steady growth that turned into a torrent of upwardly mobile forecasts and revised analyses. Unlike 2015 that was characterized by 'merger mania' and sales declines, 2017 saw fewer major deals come to fruition while sales across important consumer segments such as mobile computing and smartphones saw increases. A major factor for 2017's growth spurt was a shortage of key memory components that led to higher prices for suppliers and pledges by major makers such as Samsung to increase their 2018 capacity.

Although most of 2017 was relatively quiet in terms of large-scale mergers and acquisitions, industry watchers were surprised when Broadcom made an unsolicited bid to acquire Qualcomm Communications in November for a record-setting (USD) $103 Billion.

The Broadcom offer was announced in the midst of Qualcomm's poor earnings reports tied to its legal battles with Apple. At the same time that Broadcom sought a marriage with Qualcomm, the mobile devices giant continued is battle for NXP Semiconductors, with both sides extending offers to allow EU regulators the time needed to further investigate implications of the deal. The European Commission twice halted their investigations in 2017.

By early December, the World Semiconductor Trade Statistics (WSTS) group that is comprised of 55 major chip companies sharing data said that 2017 sales would increase by more than 20 percent to a record (USD) $408 billion.

If revenue gains continue through 31st December, 2017 would mark the first time that the industry's sales topped the $400 billion mark in any one year—this milestone comes just four years after surpassing the $300 billion mark for the first time.

JANUARY

The Consumer Electronics Show (CES) started trade fair season in the new year with announcements from Qualcomm that it 10nm Snapdragon 835 smartphone SoC would offer upgrades across all its subsystems that analysts called impressive, yet evolutionary. Despite that less than enthusiastic characterization, the new SoC provided support for Quick Charge 4.0 technology, a 35 percent decrease in package size with 25 percent better power efficiency compared to the existing 821. The new SoC was also the company's first ARM-based processor to support Windows 10 on a mobile device.

"This is big news, with Microsoft adding x86 emulation on ARM to Windows 10," said Kevin Krewell, principal analyst at Tirias Research. "I see this as a real threat to Intel. It may also be a step in Microsoft bringing a Windows server to ARM as well," he added.
In January the 835 was expected to debut in the next generation of premium smartphones when it ships by the first half of 2017. Its predecessors, the 820/821, were used in smartphones including the Google Pixel, the LG G5 and the Galaxy S7/Edge.

2016 tally: Sales up sharply

While CES saw hundreds of new devices introduced, the Semiconductor Industry Association (SIA) trade group reported that global semiconductor sales posted a year-to-year sales increase of 7.4 percent in November 2016 while the industry continued to pick up steam headed toward year's end.
The November increase was the largest for the semiconductor industry since January 2015, the SIA said. That fourth quarter jump increased the likelihood that semiconductor sales for 2016 would finish flat compared with 2015. Many market watchers—including the SIA—had predicted modest declines for semiconductor sales at the beginning of 2016 while recent sales data indicated that the industry could achieve sales of about (USD) $335 billion, roughly unchanged from 2015.

John Neuffer, SIA

SIA President John Nueffer noted that as global semiconductor sales continued to pick up steam in November, the increase was at the highest rate in almost two years. Nueffer added that the strong close to 2016 left the industry well-positioned to start 2017.

Global chip sales for November 2016 totaled $31 billion, up from $28.9 billion in November 2015, according to the SIA.

ZigBee Alliance offers language for IoT

Also at CES, the ZigBee Alliance demonstrated 'dotdot' as a universal language for the IoT, making it possible for smart objects to work together on any network. Members of the ZigBee alliance and Thread Group will also showcase the first demonstrations of dotdot devices running over Thread's IP-based networks.

"Dotdot represents the next chapter in the ZigBee Alliance's continued commitment to create and evolve open standards for the smart networks in our homes, businesses and neighborhoods," said Tobin Richardson, ZigBee Alliance president and CEO, in a statement.

Most IoT devices don't speak the same language, even if they use the same wireless technology. The result is an Internet of Things that is often a patchwork of translations, adding complexity for developers and limiting users to single-vendor systems. According to the ZigBee Alliance, the solution lies in a common language between all IoT devices on any network, giving developers a common platform to innovate on, and users the freedom to choose products that work for them.

Right, yet wrong

Gartner Inc. put their forecast hats on sideways in January, saying that it expected combined shipments of PCs, mobile handsets and tablets—major drivers of the electronics supply chain over the past few years—were projected to remain flat in 2017.

"The global devices market is stagnating," said Ranjit Atwal in January; Atwal is research director at Gartner. "Mobile phone shipments are only growing in emerging Asia/Pacific markets, and the PC market is just reaching the bottom of its decline."

Gartner projected that PC shipments would decline in 2017 for a sixth consecutive year. The firm also predicted that PC shipments would return to growth in 2018 thanks to an expected replacement cycle and the allure of premium ultra-mobile models.

Qualcomm gets slapped

The US Federal Trade Commission got the attention of Qualcomm when it sought a court order against what it alleges are unfair licensing practices for its cellular baseband patents. The complaint alleges among other things that the company "precluded Apple from sourcing baseband processors from Qualcomm's competitors from 2011 to 2016."

The FTC also charged that Qualcomm maintains a "no license, no chips" policy that requires handset makers to agree with Qualcomm's licensing terms to get supplies of its baseband chips. The company also refuses to license standard-essential patents to competitors, the FTC said. In its complaint, the FTC charged, "Qualcomm is unique in requiring an OEM, as a condition of sale, to secure a separate patent license requiring royalty payments for handsets that use a competitor's components."

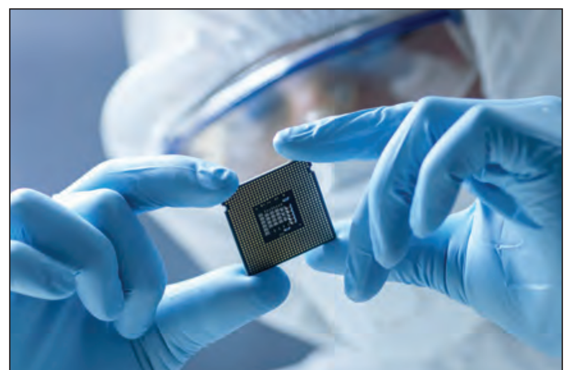
The FTC's action comes less than a month after the Korea Fair Trade Commission (KFTC) fined Qualcomm 1.03 trillion won (nearly USD $1 billion), charging unfair patent licensing practices. The KTFC levied similar charges of failing to license standards-essential patents to competitors and forcing customers to agree to unfair terms including "making them provide [the customer's] patents for free."

Qualcomm said it will appeal both cases. It described the US complaint as a politically opportunistic move that got the facts wrong and is based on flawed legal theory. "Qualcomm has never withheld or threatened to withhold chip supply in order to obtain agreement to unfair or unreasonable licensing terms," the company said in a statement.

Gartner points to modest 2016 chip sales growth

Global chip revenue increased by 1.5 percent in 2016 as a late-year surge enabled the semiconductor industry to avoid widely anticipated contraction, according to the market research firm Gartner Inc.

Total semiconductor sales for the year were (USD) $339.7 billion in 2016, up from $334.8 billion in 2015, according to Gartner's estimates. Combined sales for the top 25 chip vendors increased 7.9 percent compared to 2015, accounting for nearly 76 percent of the market, Gartner added.



Adrian Blanco, a senior research analyst at Gartner, said that 2016 chip sales got off to a slow start due to inventory reduction schemes, but accelerated in the second half of the year thanks to inventory replenishment and improved pricing.

The semiconductor industry's 1.5 percent growth in 2016 is notable because at the start of the year most market watchers—including Gartner—predicted that the industry would contract.

Analysts project 7% growth in 2017

Global semiconductor revenue was projected by Gartner Inc. to grow 7 percent this year driven by chip inventory replenishment and increased average selling prices.

Gartner spokespeople said their analysts expected 2017 semiconductor sales to total $364 billion, up from an estimated $340 billion last year. The firm said it increased its 2017 sales projection by $14.1 billion from its most recent forecast, $10 billion of which comes from an increased forecast for memory sales.

"The worst is now over with a positive outlook emerging for 2017 driven by inventory replenishment and increasing average selling prices (ASPs) in select markets, particularly commodity memory and application-specific standard products," said Ganesh Ramamoorthy, research vice president at Gartner, in a statement issued 23rd January. He added that the turnaround which started in the second half of last year is expected to gain momentum and carry throughout 2017.

"Memory market supply and demand have turned positive for vendors who are pushing ASPs higher to recover margins," Ramamoorthy said.

The IIoT comes into bloom

A new survey by researchers at ON World showed significant growth in the industrial Internet of Things (IIoT) and rising competition among low power wide area (LPWA) networks.

Nearly a third of industrial IoT networks now have more than 1,000 nodes, according to the survey that was conducted of more than 180 industrial automation professionals by ON World. That's twice the level of large scale networks it found in a 2014 survey.

ON World reported that it found 12 percent of respondents have deployed 1,000 or more wireless field devices at a single site, and 11 percent are using LPWA networks such LoRa or Sigfox. Two out of five respondents are researching, pilot testing or developing LPWA solutions and three-quarters of those developing LPWA plans are targeting new applications that cannot be met with other technologies. Networks that support links of up to one mile make up the majority of today's deployments with rising interest in mesh nets such as 802.15.4-based WirelessHART. But over the next five to 10 years, ON World predicts faster growth for LPWA networks including Sigfox, LoRa, Ingenu and LTE variants such as Category M1 and Narrowband-IoT.

Apple rises (again) thanks to iPhone sales

Apple Inc. returned to growth by the end of fourth quarter 2016 following three consecutive quarters of sales declines. The company's record quarterly revenue was lifted by strong iPhone sales, paced by strong demand for the iPhone 7+. While both iPhone and Mac sales fared better than expected, sales of iPads declined versus one year ago, Apple said.

Kevin Krewell, principal analyst at Tirias Research, said a higher than normal number of "switchers" from Android to Apple during the period, which is the first quarter of Apple's fiscal 2017, may have been related to rival Samsung's disastrous Galaxy Note 7 recall in 2016.

Apple reported record quarterly revenue of $78.4 billion, up 3 percent from the same period of 2015. The company reported a net income for the quarter of $17.9 billion, a decline of 3 percent versus the year ago period.

Trump and Brexit could cloud 2017, analysts say

The semiconductor industry should have a good 2017 as long as potentially volatile political issues and politicians stay neutral or positive. Growth could hit 5 percent, led by DRAMs and flash as well as 32-bit microcontrollers, analog and automotive, according to analysts at IC Insights.

That was the view from Bill McClean's annual Silicon Valley Talk. The president of market watcher IC Insights doesn't believe the big plans cooking in China or the Trump administration will substantially impact the industry in 2017, but rising populism in Europe could dampen growth.

"We think this is a milestone year," with IC sales of $314.1 billion, cracking the $300 billion mark for the first time, said McClean. He estimated the next milestone at $400+ billion in 2023, a long period of 4 to 5 percent compound growth. Interestingly, the

global revenue forecast updated near the end of 2017 points to sales reaching more than $400 billion by year's end, beating the McClean forecast by six years.

FEBRUARY

Apple dominates smartwatch growth

The Apple Watch captured 63 percent market share in the fourth quarter of 2016 as the global smartwatch market returned to modest growth following two consecutive quarters of declines, according to researchers at Strategy Analytics.

In the same study Strategy Analytics reported that smartphone shipments increased by 9 percent while tablet shipments declined by the same percentage. Shipments of smart watches increased by 1 percent compared to the fourth quarter of 2015, reaching 8.2 million units, Strategy Analytics reported. Apple shipped some 5.2 million Apple Watch units during the quarter, the firm said.

South Korea's Samsung Electronics maintained its position as the second-place seller of smart watches globally in the fourth quarter with about 10 percent market share, Strategy Analytics said. Samsung's estimated fourth quarter watch shipments dipped to 800,000, down 38 percent compared to the fourth quarter of 2015, researchers said.

(ESD), IP core reuse, and design rule checking. Rosenbaum's research team will explore use of recurrent neural nets to model ESD characteristics of circuits so that systems pass qualification tests the first time.

"We were facing common problems. We needed behavioral models that interfaced across electro-migration and circuit domains and didn't know how to go about getting them, given that colleagues were interested in different applications," Rosenbaum said in a panel on the topic at DesignCon.

"We knew we would get no funding for one specific problem, so we decided we needed to solve them all, reaching out to other universities to work together to investigate different machine-learning techniques and algorithms that are well suited to use in electronics," she said.

The work got backing from the National Science Foundation as well as support from nine companies: Analog Devices, Cadence, Cisco, Hewlett-Packard Enterprise (HPE), IBM, Nvidia, Qualcomm, Samsung, and Xilinx. The center is jointly hosted at the University of Illinois Urbana-Champaign, North Carolina State University (NCSU), and Georgia Tech.

February 2017 (continued)

New EDA paradigm is needed says TSMC

TSMC R&D Director Cliff Hou said at the International Solid State Circuits Conference (ISSCC) that engineers need a new class of Electronic Design Automation (EDA) tools to keep up with the complexity of designing today's semiconductors. Separate tools need to target today's four major markets using new techniques and assumptions including machine learning.

Hou observed that over the last 10 years the industry has been driven by mobile applications, building its design databases around smartphone SoCs. "Now we realize mobile is OK as a starting point but we also have to optimize circuits for automotive, high- performance systems and IoT where the considerations are very different," he said, showing four different SRAM designs TSMC uses just for a range of mobile and wearable designs.

Hou's keynote gave a laundry list of knotty challenges where TSMC is seeing some progress.
For example, resistance at metal layers has doubled between the 40nm and 7nm nodes. TSMC has built up complex stacks of via pillars under wires to significantly reduce but not fully mitigate the issue.
In addition, power networks must be built with greater care to avoid declines in cell utilization as transistor density increases, he said. He sketched out improvements that showed cell utilization rebounding from about 74 percent to 79 percent at 7nm.

Intel's Arizona fab comes with $7B tab

Intel CEO Brian Krzanich went to Washington on 8th February to stand beside President Donald Trump to announce the company's (USD) $7 billion investment in a semiconductor fab, known as Fab 42, in Arizona. The partially competed facility has stood vacant and unequipped in Chandler, Arizona since the building's shell was completed at the end of 2013.

"The completion of Fab 42 in three to four years will directly create approximately 3,000 high-tech, high-wage Intel jobs for process engineers, equipment technicians, and facilities-support engineers and technicians who will work at the site," Intel said in a statement. Fab 42 is expected to produce devices at Intel's 7nm device node.

While some analysts believed the move was as much about making a political statement as positioning itself for future production requirements, Rob Lineback,

senior market research analyst at IC Insights, said he believes the decision is not about capacity, which Intel has aplenty. He believes Fab 42 is where EUV lithography tools will go. "Availability of EUV lithography tools and processes will help make 7nm successful, but this exposure technology represents a major change."

Globalfoundries debuts 45nm RFSOI

Process design kits (PDKs) are now available for Globalfoundries 45nm RF SOI, a node particularly suited for making millimeter-wave chips in 24-100 GHz bands for 5G cellular. Skyworks Solutions Inc. signaled its plans to use the technology for next-generation chips.

The process provides a substrate resistivity of greater than 40 ohm-cm to enable reduced parasitic capacitance and minimize disparity in phase and voltage swing, the company said.

Designers can stack RF FETs in the process to achieve higher power and reliability. Active FETs can be tuned for very high Ft/Fmax for millimeter wave circuits in 5G products and front-ends for car radar. The process delivers the highest Fmax the foundry offers and is running on 300mm wafers in the former IBM fab in East Fishkill, N.Y.

Skyworks indicated it will use the process to "create RF solutions that … further advance the deployment of highly integrated RF front-ends for evolving millimeter wave applications," said the company's CTO, Peter Gammel, in a statement it issued concerning the move. RF SOI has long been one of the success stories of the foundry business from IBM fabs Globalfoundries acquired in July 2015.

UMC Begins 14nm device production

United Microelectronics Corporation (UMC, Taiwan) announced on 23rd February that it has initiated mass production of 14nm chips using FinFET technology. The company added that it is shipping 14nm wafers to lead customers and has achieved "industry-competitive yields" using the process.

Po-Wen, CEO of UMC, said earlier this month that the company would bring 14nm to production this quarter, ahead of the original schedule. Last April, UMC said 14nm would be in production in the second half of this year.

UMC says that its 14nm FinFET technology offers 55 percent higher speeds and twice the gate density compared to its 28nm process technology. The process also consumes about 50 percent less power than 28nm, the company indicated.

Any surface can be a user interface

Bosch, the biggest and oldest micro-electro mechanical systems (MEMS) maker, introduced a new product at the GSM Mobile World Congress that combines an infrared micro-scanner and laser projector. Together, the paired technologies are capable of transforming any surface into a virtual user interface.

The MEMS device, small enough for wearables and cheap enough for toys in high volumes, is also finding a plethora of applications anywhere a human-machine interface (HMI) is needed, such as on the factory floor, in industrial equipment, for robotics, medical devices, infotainment and in-car heads-up displays.

The new micro scanner BML050 extends Bosch Sensortec's portfolio into optical microsystems and moves the firm from its familiar role as a component supplier into the realm of systems supplier.

Because it is based on an integrated IR-RGB (infrared + red, green, blue) the module is just 6mm tall with resolution approaching high-definition class. Its two MEMS scanning mirrors can both project images and collect the reflected light so as to determine where a user's finger is touching the projected image. The technique also can be adapted to 3D scanning using time-of-flight calculations on light reflected from an object.

Miles Gained, Yet Miles to Go for EUV

According to both Intel and Samsung Electronics, extreme ultraviolet (EUV) lithography is making significant progress towards volume manufacturing. But enough hurdles remain to prevent either company from making public commitments about when it will start using the technology.

Separately from the two chip leaders, the Imec research institute (Leuven, Belgium) announced techniques for creating a 5nm process technology using EUV to assist today's immersion scanners. EUV is generally expected to see adoption in about 2020 for a few critical steps that will enable manufacturers to avoid using more than four exposures with today's 193nm immersion steppers.

"It's my belief immersion will be the workhorse and EUV will be used for select layers," said Ben Tsai, chief technologist of KLA-Tencor in a keynote opening the SPIE Advanced Lithography conference. Samsung suggested it is pressing forward with plans

announced in October (2016) to use EUV for its 7nm node, but it has yet to say how and when. Intel reiterated its guidance of the last several years that EUV is. "…highly desirable for the 7nm node, but will only be used when it is ready."

MARCH

Capital expenditures expected to grow in 2017

Total capital spending by semiconductor companies is expected to increase 6 percent this year to (USD) $73.2 billion, with the vast majority coming from the top 11 spenders, according to a new forecast from market researchers at IC Insights.

The 11 chip companies that plan to spend $1 billion or more will account for about 78 percent of total global capital spending this year, the forecast said. By contrast, in 2013, only eight chip companies increased their capital spending by $1 billion or more.

The difference between the spending of the largest chip manufacturing companies and the rest of industry is wide and, according to IC Insights' President Bill McClean, getting wider. About 10 years ago, the top five capital spenders accounted for roughly 40 percent of global semiconductor capital spending; this year that number is expected to be 62 percent, he said.

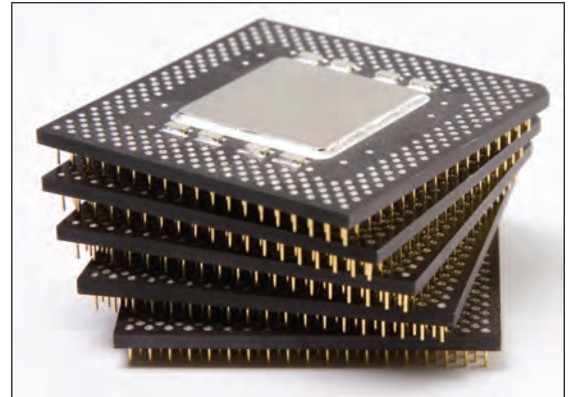
China's semiconductor building plans currently dominates the capital spending landscape among chip manufacturers. The country's stated goal of pumping $161 billion into developing a domestic semiconductor industry over the next 10 years means fab construction. According to the SEMI trade group, of the 62 new front end chip fabs scheduled to begin operations between 2017 and 2020, 26 are in China, or about 42 percent. However, the vast majority of China's projects won't be ready to start spending on equipment until 2018 at the earliest.

Chip sales leap 14% in January

January chip sales tallies showed the largest year-to-year increase in more than six years as the semiconductor industry continued a run that started in the fourth quarter of last year and drove the industry to surprising growth in 2016.

According to the Semiconductor Industry Association (SIA), chip sales for January totaled about (USD) $30.63 billion, 13.9 percent higher than in January 2016. Sales were down 1.2 percent compared to December 2016, however. The first month of each calendar year tends to have lower production and sales compared to other months due to product seasonality.

The 13.9 percent annual increase for January, based on a three-month-moving average for sales, was the largest year-to-year increase for chip sales since November 2010. John Neuffer, SIA president and CEO, said through a statement that the industry is off to a "strong and encouraging" start in 2017. "Sales into the China market increased by more than 20 percent year-to-year, and most other regional markets posted double-digit growth," Neuffer explained. "Following the industry's highest-ever revenue in 2016, the global market is well-positioned for a strong start to 2017."



Most market watchers—including the SIA and the World Semiconductor Trade Statistics (WSTS) organization, had predicted that the semiconductor industry would contract moderately in 2016. However, based on a stronger-than-expected second half of the year, semiconductor sales finished the year at nearly $339 billion, up about 1 percent compared to 2015.

1 Trillion+ semiconductors will ship in 2018

Semiconductor unit shipments are projected to top the 1 trillion mark for the first time in 2018, with the vast majority comprised of optoelectronic, sensor, actuator and discrete devices, according to market research firm IC Insights Inc.

Semiconductor shipments totaled 868.8 billion units last year and are expected to top 900 billion in 2017, according to IC Insights. In 2018, unit shipments are forecast to surpass 1 trillion after growing an average of 9 percent per year since 1978, when some 32.6 billion semiconductors shipped, according to the firm. At the time of the IC Insights report, 2017 was forecast to see modest growth compared to 2016; however, 2017 took a runaway growth tangent, and final unit shipments may exceed 1 trillion faster than expected.

TSMC announces plans for multiple nodes

World-leading Taiwanese foundry TSMC disclosed plans for new high-, mid- and low-end processes on 16th March. The processes included an enhanced 7nm FinFET node using extreme ultraviolet lithography, a 12nm upgrade of its 16nm process and a 22nm planar technology, which the company expects will compete head-to-head with fully depleted silicon-on-insulator (FD-SOI) technologies offered by Globalfoundries.

TSMC also described enhancements to its two chip-stacking techniques, advances in RF CMOS and work

in transistors and materials, paving the way to a 3nm node and beyond. In addition, it previewed design capabilities using machine learning that it will offer before the end of 2017. Among its achievements, TSMC noted 76 percent yields on the 256Mbit SRAM made in its first-generation 7nm node, which will be in volume production next year. It also reported that an ARM Cortex-A72 processor in the node exceeded 4GHz using a new design flow.

The Taiwanese company, already the world's largest foundry, expects to ship 11 million 12-inch-equivalent (300mm) wafers this year, a typical 10 percent annual increase. The biggest share, two million wafers, will utilize its planar 28nm processes, a fact driving its planned 15 percent capacity expansion this year.

China fab construction fuels equipment spending

Sales of semiconductor manufacturing equipment grew 13 percent in 2016 and are projected to grow further in each of the next two years in what would mark the first three-year period of consecutive growth for fab tools since the mid-1990s, according to the SEMI trade group.

Much of the growth in fab tool spending in 2016 and particularly, the anticipated growth in 2017 and 2018, is being driven by semiconductor fab building in China. Of the 62 front-end fabs scheduled to begin operation globally between 2017 and 2020, 26 are in China, according to tracking reports issued by SEMI last year.

The Chinese fab building escalation is driven by the PRC's stated goal of creating more homegrown semiconductor manufacturing to feed its massive internal electronics market. The Chinese government has said it will pump (USD) $161 billion over the next decade into building a domestic chip industry.

International semiconductor powerhouses including Intel, Globalfoundries and TSMC are all building or expanding fabs in China, and a number of domestic Chinese firms are planning fabs, notably Tsinghua Unigroup Ltd., which has announced plans to spend $54 billion on two huge memory chip fabs inside the PRC.

Peregrine buys MIT spinoff

RF chip vendor Peregrine Semiconductor Corp. has acquired Arctic Sand Technologies, an MIT spinoff that offers low-power chips for DC-DC power conversion. Financial terms of the deal were not disclosed.

Arctic Sand (Burlington, Massachusetts) was founded in 2010 by Gary Davison, who took over as CEO of the company in 2014. Artic Sand claims that its technology delivers power conversion efficiency enabling platforms for a variety of applications to be made thinner. In certain applications, the company claims its technology reduces the space occupied by power components by 50 percent while also reducing the height of components while reducing power loss and increasing run time.

Intel describes its 10 and 22nm processes

Intel will start making 10nm chips in 2017 that it claims will lead the industry in transistor density using a metric it challenged rivals to adopt. Separately, it announced a 22nm low-power FinFET node to compete for foundry business with fully depleted silicon-on-insulator (FD-SOI) from rivals such as Globalfoundries.

At 10nm, Intel said it will pack 100.8 million transistors per square millimeter. It estimated 10nm foundry processes now in production from TSMC and Samsung have about half that density.
Intel's metric averages density of a small and a large logic cell. Specifically, it uses a two-input NAND cell with two active gates and a scan flip-flop cell with as many as 25 active gates.

"I think it's a comprehensive, quantitative and honest metric," said Mark Bohr, a senior fellow and director of process architecture and integration at Intel. "TSMC, and I think Samsung, used to quote (similar metrics), but my guess is they weren't looking very good with this metric anymore…" which prompted them to discontinue the practice, he said.

Surging memory prices drive optimistic chip forecast

Semiconductor industry watcher IC Insights has more than doubled its forecast for industry growth in 2017 based upon surging average selling prices (ASPs) for DRAM and NAND flash memory.

The researchers announced in late March that they now expects integrated circuit revenue to increase by 11 percent this year due to a substantial upgrade to the forecasts for DRAM and NAND, which the analysts now expect to grow by 39 percent and 25 percent, respectively. IC Insights had previously forecast that the chip market would grow 5 percent in 2017.

Analysts and market researchers generally agree that 2017 should be a year of moderate growth for the semiconductor market after the industry

posted a surprising 1 percent increase in 2016 sales. However, an 11 percent 2017 leap is among the most aggressive predictions to date. The World Semiconductor Trade Statistics (WSTS) organization and market research firm Gartner Inc. are both calling for around 7 percent growth this year.

APRIL

Intel Says there is life after CMOS

Intel described more than a dozen technologies to transcend the limitations of CMOS that it is developing in conjunction with universities and the Semiconductor Research Corporation industry consortium at the International Symposium on Physical Design (ISPD 2017).

"We are looking beyond CMOS logic and computation methods to discover how to do it differently," said Ian Young, a senior fellow with Intel's Technology Manufacturing Group and director of exploratory integrated circuits in components research. "We want to lower the power supply voltage well below 0.5V, but the 60mV per decade sub-threshold swing of the MOSFET limits us from doing this for CMOS logic."

The hitch is that no matter which new technology is adopted, it must be integrated with the existing CMOS process because some CMOS transistors will be needed for the clocking and I/O analog circuits. Never fear, said Young, who stated that Intel believes there are around a dozen different ideas being researched to use the same fabs while achieving significantly lower supply voltages.

Semiconductor sales surge again

February semiconductor sales were up by 16.5 percent compared to February 2016, the largest year-to-year increase in more than six years according to the Semiconductor Industry Association (SIA) trade group. However, sales of (USD) $30.4 billion for February declined by 0.8 percent compared with January sales of $30.6 billion. The SIA said the month-to-month decline was less than is typical for the January to February cycle.

SIA President John Neuffer said that early 2017 chip sales have been strong, led by strength in memory products such as DRAM and NAND flash. "Year-to-year sales increased by double digits across most regional markets, with the China and Americas markets showing particularly strong growth," Neuffer said. "Global market trends are favorable for continuing sales growth in the months ahead."

The year is indeed shaping up to be a strong one for semiconductor sales, with market watchers generally forecasting moderate to strong annual growth. Last week, market research firm IC Insights Inc. more than doubled its forecast for 2017 chip sales growth to 11 percent, crediting surging average selling prices for DRAM and NAND.

The need for speed

Google's Tensor Processing Unit (TPU) beat Intel's Xeon and Nvidia GPU in machine-learning tests by more than an order of magnitude, Google reported. A 17-page paper gives a deep dive into the TPU and benchmarks showing that it is at least 15 times faster and delivers 30 times more performance/watt than the merchant chips.

In May, Google announced the ASIC designed to accelerate inference jobs for a wide range of applications on its data center servers. Now it is providing a first in-depth look at the chip and its performance in a paper to be presented at a computer architecture conference in June.

Machine learning impacts IC design

Semiconductor engineers are already hearing AI's footsteps as highly advanced software systems encroach on their design work. Why? Consider the vast amount of design data and variability required of chip designers, especially when developing a variety of chips with different power, temperature and performance specs. Complex IC designs might well be one of the logical areas to apply machine learning.

At least one EDA software company is making headway with home-grown machine-learning algorithms, calling it "machine learning for engineering" and applying it to variation-aware design and characterization software.

That company is Solido Design Automation, a privately-held EDA software vendor founded in 2005 in Saskatoon, Canada. Solido became the first vendor to make commercially available its machine-learning algorithms to semiconductor customers when it launched Machine Learning (ML) Labs. Solido's plan is to "collaboratively work with semiconductor companies to develop new ML-based EDA products," according to the company.

Qualcomm v. Apple disputes widen

According to a court document filed by Qualcomm, Apple refused to pay mobile device chip royalties, pressured its contractors not to pay them, instigated regulatory investigations and throttled performance of an LTE modem chip. The charges are contained in a 134-page court document the chip vendor filed

in response to Apple's (USD) $1 billion suit filed in January. Apple alleged Qualcomm charges exorbitant patent royalties and paid the iPhone maker not to talk to regulators.

The document provides a rare look into the sometimes combative relationship and complex web of agreements between the two mobile giants. It also sheds light on the murky area of patent royalties. In its suit, Apple claimed Qualcomm asks for five times the royalties of all other cellular patent holders combined. Qualcomm countered Apple offered "a small fraction" of the royalties that other smartphone makers pay and asked for an agreement that included more patents, including some pertaining to 5G cellular designs. In the latest court document, Qualcomm asked the Southern District Court of California for a jury trial and unspecified damages.

Gartner forecasts semiconductor market to grow 12% in 2017

Predictions of 2017 semiconductor market growth are increasing as the year rolls on; favorable conditions in the commodity memory market continue to be seen as the main driver.

Market research firm Gartner Inc. said on 13th April that it expects semiconductor industry sales to grow 12.3 percent this year, reaching $386 billion. The researchers said that favorable market conditions that gained momentum in the second half of 2016 have raised the outlook for the chip market in both 2017 and 2018. But Gartner also cautioned that the rush to add DRAM and NAND flash capacity to capitalize on the market conditions and the rise in manufacturing in China would likely result in a market correction in 2019.

Gartner said PC DRAM pricing has doubled since the middle of 2016, with a 4GB module that cost $12.50 in the middle of last year now commanding just under $25 today. NAND flash average selling prices (ASPs) also increased sequentially in the second half of 2016 and the first quarter of 2017.

EUV lithography moves toward commercial adoption

Executives from ASML NV (The Netherlands) said on 19th April that the company expects to ship 20 to 24 extreme ultraviolet (EUV) lithography tools in 2018 as the industry continues edging closer to production deployment of the oft-delayed next-generation lithography technology.

Peter Wennink, ASML's president and CEO, told analysts following the company's first quarter financial report that the company continues to make progress toward its goals for EUV of producing 125 wafers per hour with 90 percent light-source availability. Wennink made reference to presentation at the recent SPIE Advanced Lithography Conference from Intel, Samsung and TSMC showing their latest results with EUV systems and the status of current EUV infrastructure.

"And while there is still work to be done on things like the pellicle, there appear to be no major roadblocks for EUV insertion in the timeframes indicated by our customers," Wennink said. ASML said Wednesday it has an order backlog in the pipeline of 21 NXE:3400B EUV systems—its most advanced EUV tool which started shipping this year—worth 2.3 billion euro (about USD $2.46 billion).

Fab tool billings reach 16-year highpoint

The three-month rolling average of billings among semiconductor equipment vendors based in North America hit (USD) $2.03 billion in March, its highest total in 16 years, according to the SEMI trade organization. The three-month average of billings was up 69 percent compared to March 2016, the sixth consecutive month of year-over-year growth. The billings figure was also up 3 percent from February.

"March billings reached robust levels not seen since March 2001," said Dan Tracy, senior director of industry research and statistics at SEMI, in a statement. "The equipment industry is clearly benefiting from the latest semiconductor investment cycle."

Intel increases capital spending 20%

As consensus looks to continued growth in 2016, Intel increased its 2017 revenue forecast slightly, elevated in part by a slight rise in PC prices. It also increased its annual capital equipment budget to $12 billion, a level it expects will continue into 2018, in part to support ramping 3D NAND and 3DXP memories.

For its first quarter, the chip giant reported revenue of $14.8 billion and net income of $3 billion, up from 8 and 45 percent last year, respectively. A 7 percent increase in PC prices drove Intel's client group, its biggest division, to $8 billion in quarterly revenues, a 6 percent increase. Intel's data center group, which targets high-single-digit growth, turned in a 6 percent revenue rise as unit sales fell slightly ahead of the summer release of new server CPUs. Intel's smallest units turned in its highest growth. Its flash group grew fastest at 55 percent to $866 million, followed by the former Altera FPGA group, up 18 percent to $425

million. The nascent IoT group also moved forward by 11 percent to $721 million.

All in all, the PC CPU maker reported progress in its slow transition to broaden its base. It lifted its annual revenue forecast by $500 million to $60 billion, which would mark a new high.

Apple stops paying royalties, reducing Qualcomm's revenue forecast

Qualcomm is lowering its third-quarter guidance by about $500 million, claiming that Apple said it will not pay patent royalties. The disclosure suggests that Qualcomm receives a whopping $2 billion a year, or roughly $8 per device, in royalties for Apple products.

Qualcomm specifically lowered its third-quarter guidance from a range of (USD) $5.3 to $6.1 billion to a range of $4.8 to $5.6 billion. Apple said that it will withhold Qualcomm royalty payments starting in the first calendar quarter until the patent dispute between the companies is resolved, Qualcomm said in a press statement.

Apple filed suit against Qualcomm in January, claiming that Qualcomm's royalties were exorbitant and the chip vendor pressured it to remain silent. In a countersuit filed earlier this month, Qualcomm said that it paid Apple to refrain from asserting patents and revealed that it gets royalty payments for iPhones and iPads through Apple's contract manufacturers including Compal, Foxconn, Pegatron, and Wistron.

MediaTek's Smartphone Market Share is Shrinking
MediaTek, the second-largest smartphone chip supplier after Qualcomm, said it is losing market share after nearly four years of strong gains in the 4G mobile segment. MediaTek has slowed upgrades for its flagship Helio product line, offering only an LTE Category 6 modem, while rival Qualcomm early this year raised the bar with the world's first 10nm processor, the 835 Snapdragon, including a Category 16 modem.

"We have been losing market share for the Helio X and P series products," said MediaTek Senior Vice President David Ku on a conference call to announce the company's first-quarter results. "Based on our design wins, we expect to gain back some market share by the second half."

MediaTek and Qualcomm are chief rivals in China, the world's largest smartphone market, with both companies seeking handset deals with companies such as Oppo, Vivo, Xiaomi and Meizu. The companies have in the past year had sales growth exceeding Samsung and Apple. Qualcomm has been gaining share in China. Moreover, Chinese chip designers such as Spreadtrum and HiSilicon are ratcheting up the competition.

MAY

Microsoft dives deeper into HoloLens

A computer vision specialist from Microsoft gave a deep dive into the challenges and opportunities of its HoloLens in a keynote address at the Embedded Vision Summit taking place in Santa Clara, California. His talk sketched out several areas where augmented reality products such as HoloLens still need work to live up to their promises.

According to Marc Pollefeys, an algorithm expert who operates a computer vision lab at ETH Zurich and joined the HoloLens project in July as director of science, stated he believes that HoloLens, "…will be the next generation of personal computing devices with more context…' compared to today's PCs and smartphones.

Jeff Bier, host of the event and founder of the Embedded Vision Alliance, praised the headset as "one of the first AR and VR products that didn't give me a splitting headache…" But he added that the $3,000, 1.2-pound developer version available today, "…needs to get smaller and cheaper."

Slumping sales and lawsuits drag down Apple's China growth trajectory

Apple reported modest growth in the last three months despite continued gains by smartphone rivals in China. Looking ahead, financial analysts cited concerns about the ongoing iPhone slump in China, high memory prices and Apple's lawsuit with Qualcomm.

Apple increased second quarter revenues 5 percent from the same period last year to $52.896 billion despite a 14 percent decline in China sales. Overall sales of iPhones—which account for almost two-thirds of Apple's revenue—were up just 1 percent, while iPads continued their decline (off 12 percent). Mac revenues were the upside note, increasing 14 percent year-over year.

TSMC prosecutes ex-employee for leaks

Taiwan Semiconductor Manufacturing Company (TSMC), the world's largest semiconductor device foundry, said it is prosecuting a former employee for leaking intellectual property in its second such case in the past five years. The employee, who TSMC only identified by his surname, Hsu, printed out what the company called an "abnormal volume" of documents

related to the company's 28nm process technology. The employee also said he planned to resign from TSMC and join rival foundry Shanghai Huali Microelectronics Co. (HLMC). The case is the second major incident involving leaks of TSMC intellectual property in the past five years. In 2015, TSMC won a lawsuit against Liang Mong-song, a former senior director of R&D who later became Samsung's System LSI division chief technology officer.

Tablet shipments continue declining

Global shipments of tablets declined year-over-year for the 10th consecutive quarter during the first three months of this year as enthusiasm for the devices continues to wane, according to market research firm International Data Corporation.

Ryan Reith, IDC vice president and operator of the company's tablet tracker program, noted that although device sales continue to erode, the rate at which the tablet market exploded from the launch of the original iPad in 2010 until 2013 was unlike most consumer-oriented markets. "However, it appears for many reasons consumers have become less eager to refresh these devices, or in some instances purchase them at all," Reith said.

IDC believes the leading driver for tablet contraction continues to be increased dependency by consumers on smartphones along with minimal technology and form factor progression in tablets. With laptop prices continuing to fall across many categories, and with designers creating laptops that combine tablet-like touch screen capabilities with substantially greater storage and processing power, these factors make replacing a tablet, or choosing a tablet instead of a laptop less likely than ever before.

DSL pioneer foresees a terabit future

At a time when carriers are pondering an expensive shift from copper cables to optical fibers, a pioneer of digital subscriber lines (DSL) is proposing a novel upgrade that someday could deliver terabit data rates. In a keynote at the G.Fast Summit in Paris on 9th May, John Cioffi unveiled ideas behind what he calls Terabit DSL (TDSL). They include carrying 50-600 GHz wireless signals through the tiny spaces between individual twisted pairs of the cables containing a hundred or more such pairs.

"We are shooting for a terabit/second over 100 meters, 100 Gbits/s at 300 meters and 10 Gbits/s at 500 meters -- all those are 200 to 1,000 times better than traditional DSLs," said Cioffi, whose research at Stanford in the 1980s led phone companies to embrace DSL for broadband.

Consolidation continues to affect vendor ranks as merger fever subsides

The world's largest chip vendors have growth rates in outsized proportion compared to other supply chain vendors due to the impacts of merger activity occurring in 2015-2016, concluded a new report by Gartner Inc.

Gartner said it believes that global semiconductor sales reached $343.5 billion in 2016, an increase of 2.6 percent compared to 2015. The growth rate was higher than that estimated by other market watchers like the World Semiconductor Trade Statistics organization, which said in February that industry sales grew by 1.1 percent.

The top 25 vendors, however, grew sales by a combined 10.5 percent in 2016, according to Gartner. These companies accounted for nearly 75 percent of total market share. By contrast, other semiconductor vendors in the market saw their sales decline by 15.6 percent, Gartner reported.

According to James Hines, a research director at Gartner, the relative growth of the top 25 vendors compared to the rest of the market is skewed by the high degree of merger and acquisition activity that took place in 2015 and 2016.

"If we adjust for this M&A activity by adding the revenue of each acquired company to the revenue of the acquirer for both 2015 and 2016 where necessary, then the top 25 vendors would have experienced a 1.9 percent revenue increase, and the rest of the market would have increased by 4.6 percent," Hines said, in a press statement.

Imec describes new ai chips

The Imec research institute (Leuven, Belgium) reported during its annual Technology Forum that it is developing machine learning accelerators using arrays of resistive and magnetic memory cells rather than neural networks to reduce cost and power. Initial results included an MRAM array that lowered power by two orders of magnitude.

Imec is withholding details of the chips' architecture and their performance until later in the year when it has its patents filed. The research institute started a machine learning group 18 months ago as part of its ongoing efforts to expand beyond its core work on silicon process technology.

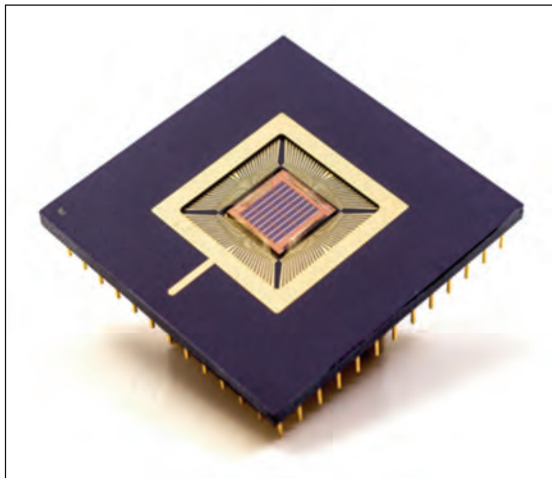
Record wafer shipments continue

Defying typical seasonal weakness, worldwide shipments of silicon wafers increased sequentially in the first quarter of 2017, logging their highest recorded quarterly level, according to the SEMI trade group.

All silicon wafer area shipments reported totaled 2.86 billion square inches in the first quarter, up 3.4 percent compared to the fourth quarter of 2016. Shipments were also 12.6 percent higher compared to the first quarter of 2016, based on results collected and reported by SEMI's Silicon Manufacturing Group (SMG).

Samsung spinoff will grab foundry share
Samsung Electronics' plan to spin-off foundry operations from its system LSI division is expected to increase the company's share of global contract chip manufacturing at the expense of Taiwan Semiconductor Manufacturing Company (TSMC) and smaller rivals.

Samsung's chip operations, consisting of memory and system LSI, will be split into three, making the foundry business an independent unit, according to the Korea Economic Daily.



The separation of Samsung's contract chip making from its branded semiconductor business would remove a conflict of interest with potential customers such as Nvidia and MediaTek, and create a new threat to dedicated foundries such as TSMC, according to analysts studying the process.

Imec offers 4 views of silicon's future
The Imec research institute's semiconductor road map as discussed by senior researcher An Steegen shows a new node in the upper right hand corner – 14 . The placeholder for a 14-angstrom process; this represents a 0.7x shrink from a 2nm node in 2025, displaying optimism that this stage of semiconductor evolution will be achieved at a future point.

"We're still trying to come up with what goes into that bucket, but how we fill it in may be quite different than what we have done before," said Steegen at the annual Imec Technology Forum held in Antwerp. A 14- node suggests the atomic limits ahead. A single arsenic atom, one of the larger elements used in semiconductors, measures about 1.2.

As they approach a 14-angstrom future, engineers may start to mix on the same die FinFETs with nanowires or event tunnel FETs or spin-wave transistors. They will certainly start to experiment with more types of memories, and they may be building chips for new kinds of non-Von Neumann computers. In the near-term, Steegen sees extreme ultraviolet lithography (EUV) being adopted at 7 nm, FinFETs living on to 5- and even 3-nm nodes, and nanowire transistors emerging somewhere along the way.
China Could Shape the Future of FD-SOI
Globalfoundries and the municipality of Chengdu are counting on China to play a significant role in the evolution of FD-SOI technology. This public/private partnership announced on 23rd May that it plans to pump (USD) $100 million into a project to "spur innovation in China's semiconductor industry" around FD-SOI.

The move is a significant step in efforts to ignite broader acceptance of the non-bulk CMOS technology in China. The plan rests on the fact that China today consumes more than 58 percent of semiconductors produced worldwide, and its leaders are spearheading a national drive to substantially expand indigenous semiconductor production capacities.

While China held only a 16.2 percent share of worldwide semiconductor production in 2015 according to a PricewaterhouseCoopers report, the nation is currently going through an unprecedented fab boom, backed by 120 billion yuan National IC fund (more than USD $17 billion) and supported by 600 billion yuan (USD $85 billion) from local government and private equity companies.

The newly unveiled $100 million budget allocated for building the FD-SOI ecosystem in Chengdu is a part of $10 billion investment that Globalfoundries and Chengdu's leaders announced to support fab construction.

Samsung plans to achieve 4nm in 2020
Samsung Electronics released an updated foundry technology roadmap on 24th May, including details of its second-generation FD-SOI platform, several bulk silicon FinFET processes (that scale down to 5nm) and a 4nm "post FinFET" structure process set to be in 'risk production' by 2020.

Samsung, which formally broke its foundry operation into a separate business unit called Samsung Foundry earlier in May, also reiterated previously announced plans to put extreme ultraviolet (EUV) lithography into production in 2018 at the 7nm node.

"We are extremely aggressive with our roadmap, not only in planning, but in announcing what we are going to be doing in the next three to four years," said Kelvin Low, senior director of foundry marketing at Samsung.
Silicon's Future to be reshaped by Big Data

The huge data sets collected by web giants such as Amazon, Google, and Facebook are fueling a renaissance of new processing chip designs. Two of the latest efforts will be described at an annual conference on computer architecture in late June.

Stanford researchers said they will describe Plasticine, a reconfigurable processor that sports nearly 100x better performance/watt than an FPGA while being easier to program. Separately, two veteran designers at Nvidia were part of a team that defined an inference processor that delivers more than twice the performance and energy efficiency of exiting devices.
MEMS Market Growth Aided by RF Filters
The total value of the global MEMS market is projected to grow from about $13 billion in 2017 to more than $25 billion in 2022, driven largely by growth in RF applications including RF MEMS filters, according to a new report by research researchers at Yole Développement (France).

The growing demand for RF MEMS filters is being fueled by further growth in 4G mobile technology and increasing complex cellular communications, according to Yole. The analysts expect sales of RF MEMS filters — the biggest business in the RF front-end — to increase at a compound annual growth rate (CAGR) of 35 percent between 2017 and 2022.
"Beyond the development of these RF MEMS devices, the RF front-end demonstrated comfortable growth, at 14 percent CAGR during the same period," said Claire Troadec, Yole's RF devices and technologies activity leader, in a press statement.

JUNE

Big data making waves

One might speculate that Big Data can trace its ancestral roots to the days when Sergy Brin and Larry Page (Google) helped develop an algorithm that found more relevant results on the web than the search engines of their rivals. The lesson of Google continues to ripple through all businesses seeking competitive insights from their data pools, however large or small.

Today, the Internet of Things (IoT) is opening vast new data sources, expanding big data's promise to reshape business, technology, and the ways that technologists approach their work. Along the way, big data is inspiring new kinds of processor and systems architectures, as well as evolving algorithms and programming techniques.

At Stanford's Data Science Initiative, researchers are working the big-data techniques in the hands of the average company.

"Machine learning is impressive but really hard to use. Even the most sophisticated companies might only have a couple of people that can apply those techniques optimally," said Stephen Eglash, executive director of Stanford's program. "I can imagine the day when these tools are available in the equivalent of Microsoft Office."

To get there, Stanford researchers are developing 'Snorkel,' a tool to automate the process of labeling and ingesting big data sets. "It's far enough along that you can see that it will work," said Eglash. "We want the domain experts to use these techniques without needing a computer science expert."
The IEEE Big Data Initiative is taking a different approach, making large data sets freely available for research through its Dataport service. So far, they include examples as diverse as real-time feeds of New York City traffic and neuron movements in a human brain.

Nvidia CEO touts death of Moore's Law

Nvidia CEO Jensen Huang has become the first head of a major semiconductor company to say what academics and researchers at prominent institutes have been suggesting for some time: Moore's Law is dead.

Moore's Law, named after Intel cofounder Gordon Moore, reflects his 1965 observation that transistors were shrinking so fast that every year twice as many could fit onto the same surface of a semiconductor. In 1975, the pace shifted to a doubling every two years and has subsequently been modified further as more design architectures permeate an increasingly global market.

The enablers of increased speed and density at every generation, increasing the size of pipelines, shortening signal pathways and various additions to lithography tool sets, are among the techniques that are now failing to keep pace with the expected 50 percent increase in transistor density each year, Huang told a gathering of reporters and analysts at the Computex show in Taipei. The diminishing returns from Moore's Law and Dennard scaling have seen the semiconductor industry enter a mature stage in which just a handful of chipmakers can afford the multibillion dollar investments required to push process

technology forward. The semiconductor industry is exploring a number of pathways beyond Moore's Law. Some 'upstart' Chinese chipmakers are taking a stake in Fully Depleted Silicon-On-Insulator FD-SOI. Others see a future in going beyond planar design to three-dimensional chips.

Nvidia's bet on artificial intelligence to take the silicon industry forward is bullish, and time will tell if their approach delivers performance enhancements that will resonate across the supply chain, and ultimately with consumers looking for newer, faster and better products.

NAND shortage fuels price increases
Contract pricing for NAND flash memory surged by 20 to 25 percent in the first quarter, a strong testament to the undersupply condition that persists in the market, according to DRAMexchange, a firm that tracks memory chip pricing.

NAND revenue typically falls off considerably between seasonally strong fourth quarters and the first quarter of each New Year, traditionally a slow season for end device shipments. But in the first quarter of 2017, global NAND revenue declined by just 0.4 percent, as the reduction of two-dimensional NAND capacity was severe enough to create tight demand, DRAMexchange said.

Prices of mobile storage products such as embedded multi-chip package (eMCP) devices, embedded multi-media card (eMMC) products and universal flash storage (UFS) also continue climbing, DRAMexchange said.

DRAMexchange expects the NAND shortage to persist throughout 2017, resulting in sequential sales increases for NAND suppliers.

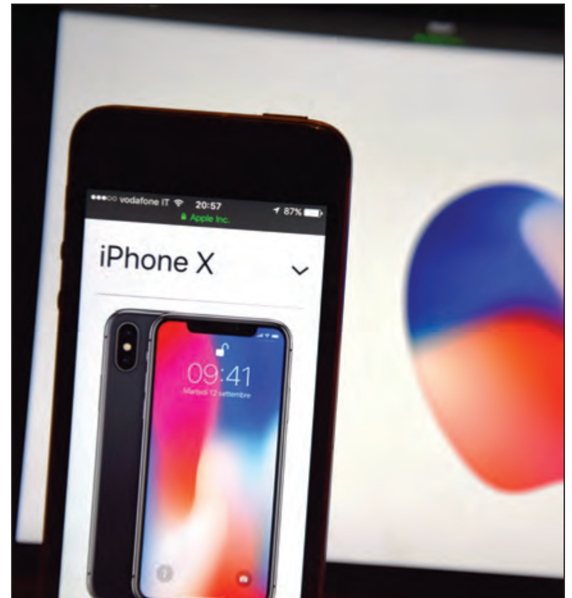
iPhone 10 year anniversary a time of reflection at Apple

Memories of Steve Jobs illuminated some of the brightest moments of on-stage discussions with four engineers from the original Apple iPhone development team. The Computer History Museum organized the event as part of a tribute to the landmark handset's 10th anniversary, moderated by former New York Times tech reporter John Markoff.

The iPhone "had a very circuitous route," said Scott Forstall, the software team leader for the original iPhone.

An acquaintance of Jobs worked on tablet PCs at Microsoft, a topic that got under the Apple co-founder's skin. "Steve hated this guy … and that was the actual origin of the iPhone," said Forstall in his first public appearance in five years, speaking about Apple route to the landmark achievement.

"One time, [Jobs] came back from seeing this guy and … Steve came out with a set of expletives and said, 'Let's show them how it's done. Let's not use a stylus. We're born with ten styluses.'"



The team quickly decided to work on capacitive rather than resistive screens and to support multi-touch. An early demo letting fingers move a picture displayed by a large projector mounted on a conference room ceiling "wouldn't fit in a bathroom, much less a pocket or bag, but the moment we saw it, we knew that was the way to go," said Forstall, who is named on 200 Apple patents.

Handsets will drive the IC Market

Sales of chips for cellular handsets will surpass sales of chips for personal computers for the first time in 2017 as the multi-year PC sales slump continues and tablet shipments also plummet, according to market research firm IC Insights Inc.

Sales of integrated circuits (ICs) for handsets are projected to grow 16 percent this year to reach $84.4 billion, researchers said. Meanwhile, sales of ICs for PCs, including desktop and laptop computers, tablets and ultra-thin Internet-centric client devices, are forecast to grow 9 percent to reach $80.1 billion, analysts predict.

Booming memory chip prices will boost growth in both phones and PCs, IC Insights explained. But due to their higher growth rate, handsets will become the largest application for ICs this year for the first time, they predicted.

Toshiba and the indelible flash lesson

Toshiba Corporation's plan to spin-off its chip business has put the company's flagship NAND flash memory products in the spotlight. Toshiba engineers invented flash memory in the 1980s, setting off a revolution that ultimately transformed many facets of consumer and industrial electronics. But Toshiba

management, initially failing to foresee the bounty that awaited flash developers, came close to letting the big one get away.

By 1980, the need for a more economical data-storage alternative to E2PROM had become apparent to Fujio Masuoka, a factory manager at Toshiba. E2PROM incorporated two transistors per cell and had to be completely erased before being rewritten. So Masuoka assembled a team of four engineers to develop a smaller and more affordable memory chip architecture that could store a lot of data but would speed erase and write times.

Masuoka's team came up with a design that replaced the E2PROM two-transistor cell structure with a single-transistor cell and allowed data to be read and written in blocks or pages. The design eventually led to the creation of much smaller memory chips. Masuoka based his work on the premise that the cost of new memory chips would continue to drop as transistors shrank in size.

To help pitch their concept, Masuoka and his team developed a catchy name that would highlight the new memory technology's ultrafast erasing capability. Team member Shoji Ariizumi suggested "flash," as in the wink-of-an-eye trigger of a camera's flash system. The rest of the story is the stuff of technology legend. Masuoka's team presented the idea that was rejected by Toshiba executives. But convinced their idea had merit, the group presented their ideas in a paper at a 1984 IEEE IEDM meeting in San Francisco.

Intel developed its own approach independently that led to the first NOR flash chips, which drove the Toshiba team back to the drawing board. A year after Intel launched its NOR flash, the Japanese tech giant came up with a version of its NAND flash chip design that reduced the erase and write times and mandated less area per cell. Toshiba's NAND flash chips were able to offer greater storage density and lower cost per bit, while their mass data storage capability made NAND flash the memory technology of choice in devices such as solid-state drives (SSDs), memory cards, and music players.

The rest, as they say, is history.

DRAM prices continue to climb

The average selling price (ASP) of DRAM chips is projected to increase by 5 percent from the second quarter of 2017 to the end of the third quarter as tight supply persists, according to market watcher DRAMeXchange.

While demand for DRAM chips, particularly from the smartphone market, has been rather luke warm this year, the pace of technology migration has been slow and contributed to a tightening of supply, according to Avril Wu, research director of DRAMexchange, which tracks pricing of memory chips.

"This situation is anticipated to last (until) 2018 since suppliers will not take on significant additional production capacity in the short term," Wu said in a press statement. "Meanwhile, ASPs of various DRAM products will remain high."

Unlike previous supply and demand cycles in memory chips, DRAM chips are now being used in more and broader applications, said DRAMexchange. New DRAM applications include graphic processing, cloud computing, automotive electronics and hardware acceleration for machine learning, which have helped to stabilize ASPs for DRAM, the firm said.

It takes a little purple to mimic the sun

Seoul Semiconductor Co. Ltd., in partnership with Toshiba Materials Co. Ltd., has created an LED that it says more closely mimics the spectrum of natural daylight.

Called SunLike, the LEDs combine Seoul Semiconductor's high-brightness purple LEDs with advanced red, green, and blue (RGB) phosphors developed at Toshiba Materials. Up to now, most attempted to create full spectrum LEDs have mimicked daylight by combining blue-emitting LEDs with yellow and red phosphors to fill out the rest of the spectrum, but that method results in peaks in the blue spectrum.

Blue peaks are undesirable because the amount of blue light the human eye can accept is limited. Over-illumination with blue light results in scatter, which distorts the texture and color of illuminated objects. Research also suggests that exposure to excess blue light can have negative health effects related to interruption of the circadian rhythms, which has led health advocates to encourage only limited exposure to blue light emitting LED and LCD screens prior to bedtimes, especially for children.

The secret to SunLike's performance is the phosphors, said Seoul Semiconductor CEO Chung Hoon Lee. "Other companies that have tried to use purple LEDs to mimic daylight still suffer from purple peaks," he said. "Toshiba Materials' new phosphor is

perfect, and that's the difference."

ARM's approach to neural computing still hush-hush

Global chip giant ARM is developing neural networking libraries for its core as the company pursues a different path to advanced chip architectures while NXP is supporting inference jobs such as image recognition in software on its i.MX8 processor. The company aims to extend its approach for natural-language processing later this year, claiming that dedicated hardware is not required in resource-constrained systems.

NXP is following in the footsteps of its merger partner, Qualcomm. However, the mobile giant expects to eventually augment its code with dedicated hardware even as ARM seeks another path that it has declined to fully discuss publicly.

JULY

NASA seeks a 'tricorder' for Mars

NASA wants to take a geological 'tricorder,' to Mars according to a researcher preparing for the mission who asked attendees at last week's Sensors Expo if they could build one based upon concepts of the device seen regularly in the original Star Trek television series and throughout the show's 50-year history on television and in motion pictures.

Right now the space agency has four portable scientific instruments weighing about 21 pounds to do the job. They do reasonably good work, but there's room for improvement; four different instruments is a bit much to carry. Astronauts will be laden with bulky suits, oxygen tanks and backpacks. They have limited time to accomplish a broad range of missions walking over a rocky terrain with no hospitals within 35 million miles if they fall.

"We'd like to have multiple instruments in one (device). Can we build this thing?" asked Alexander Sehlke, a research fellow in the BASALT project at NASA Ames, speaking in a keynote address at Sensors Expo.

FTC okay's Broadcom deal to buy Brocade

The US Federal Trade Commission (FTC) has approved Broadcom Ltd.'s (USD) $5.9 billion acquisition of Brocade Communications Systems Inc. after Broadcom agreed to establish a "firewall" to prevent Brocade from accessing proprietary information about Broadcom customer Cisco Systems Inc.'s fibre channel switches.

The FTC said in a statement on 3rd July that it voted 2-0 to accept Broadcom's proposal and allow 30 days for public comment. The FTC will decide after Aug. 2 whether to make the proposed consent order final, it said.

Broadcom announced in November it would acquire Broadcom for $5.9 billion to add Broadcom's fibre channel switches to round out its network storage business. The deal calls for Broadcom to subsequently sell the company's Ethernet networking business for an expected $1-2 billion.

China makes significant IoT decisions

Two of China's Web giants tapped domestic and U.S. chip partners for embedded voice software and services competing with Amazon Alexa and Google Home. Their efforts mark a new front in the war over an emerging market for natural-language and machine-learning services targeting everything from cars to thermostats.

Alibaba announced its Tmall Genie, similar to Amazon's Echo, using a Mediatek SoC. Rival Baidu announced two- and four-mic far-field reference designs for its DuerOS software using Mediatek and Conexant chips as well as support for Nvidia's Shield TV streaming device. It had previously shown DuerOS running on chips from Shanghai-based RDA Microelectronics.

Alibaba and Baidu announced products in separate events on 4th July. The same day, Tencent (China's third largest Web company,) announced a deal to supply content for TCL Corp.'s smart TVs. The move follows Tencent investments of nearly (USD) $90 million in TCL in recent weeks, according to a Reuters report.

The news comes at a time when Amazon dominates the still small market for voice-enabled smart services. Amazon's Echo, based on a Texas Instruments chip set, is said to have shipped 7-10 million units to date, mainly in the U.S. and the U.K.

Amazon is expected to add at least one new semiconductor partner later in 2017 to an OEM program that already includes Conexant, Microsemi and NXP. So far, Alexa is not available in China, nor does it support Chinese, leaving a wide-open door for its Web rivals there.

Memory prices drive record Samsung profit

South Korean electronics powerhouse Samsung Electronics said on 7th July that it expects to report a record profit of about 14 trillion Korean won (about USD $12.1 billion) for the second quarter as surging memory chip prices boost the company's bottom line. Samsung said it expects its profit to increase 72 percent compared with the second quarter of 2016. The firm said sales rose to an estimated 60 trillion won (about USD $52 million), an increase of 18 percent compared with one year ago.

Memory chip prices have been on the rise since late last year as tight supply in DRAM and NAND flash memory have chip vendors scrambling to add capacity. Flash memory chips are also finding uses in more applications, such as consumer electronics and

solid state drives in mobile and stationary applications, leading to higher consumption.

5G will drive cellular BTS sales – In 2021

Despite enthusiasm over 5G, spending on cellular base stations will continue a significant decline over the next three years before returning to growth in 2021, according to a new report from the Dell'Oro Group.

The report is roughly in line with the outlook from infrastructure giant Ericsson that reported worse than expected quarterly results. Dell'Oro predicted a high single-digit percentage decline in base station sales this year followed by two years of declines in low single digits. Ericsson expressed hope that the market would be only 'somewhat flat' in 2019.

The news underscores the precarious position for wireless vendors. They are making significant investments now in 5G technologies and services while navigating the end of major 4G deployments. "The lull is impacting all regions and all vendors ... so far, Huawei has weathered the downturn better than Ericsson and Nokia," said Stefan Pongratz, a senior director and analyst at Dell'Oro. "We see some promising signs in North America, but the China market is expected to contract in 2017, and Europe will overall see a near-term decline."

For its part, Ericsson reported a $145.3 million second-quarter loss, with both sales and gross margins below consensus forecast, according to a Reuter's report that said the company will make cuts of about a billion dollars.

The rapid rise of LTE, especially in China, drove base station sales to a peak of $33 billion in 2014. Since then, annual sales have fallen nearly $4 billion and will fall nearly $6 billion more before they nudge up in 2021, fueled by sales of 5G macro base stations and LTE small cells, said Pongratz.

ASML sales surge thanks to EUV orders

Semiconductor lithography equipment vendor ASML Holdings (The Netherlands) posted better-than-expected second quarter revenue driven by sales to the booming memory chip sector. ASML also reported a significant increase in sales of next-generation extreme ultraviolet (EUV) lithography tools.

ASML reported that it sold an additional eight EUV systems in the second quarter, bringing its EUV backlog to 27 tools valued at about 2.8 billion euro (about USD $3.26 billion). The firm also announced that it demonstrated the key productivity metric of 125 wafers per hour (125) on an EUV tool at its headquarters. ASML said it expects sales to memory companies (DRAM vendors) to grow about 50 percent this year as the memory sector enjoys one of its best upward trajectories in history.

Chip M&A fever cools in 2017

The blistering-hot pace of merger and acquisition activity that dominated the semiconductor industry for more than two years cooled markedly in the first half of 2017 as the absence of so-called 'mega deals' brought down the total value of transactions.

The combined value of about a dozen pending transactions announced in the first half of this year totaled just (USD) $1.4 billion, down from $4.6 billion in the first half of 2016 and $72.6 billion in the first half of 2015, according to market research firm IC Insights Inc.

Despite the slow start to M&A in 2016, several large transactions announced during the second half of the year pushed the total value of deals to near $100 billion, within striking distance of the all-time record of $107.3 billion set in 2015, researchers said. Despite the existence of several pending or rumored deals, including the pending sale of Toshiba's memory chip business, it is unlikely that a second half M&A surge will emerge to bring the value of transactions for the year anywhere close to either 2016 or 2015, the firm said.

Foxcon to make $10 billion US investment

Hon Hai Precision, the parent company of Foxconn, will spend $10 billion to build a LCD manufacturing facility in Kenosha, Wisconsin. The plant will be a 10.5-generation LCD facility for next-generation 8K displays. The deal brokered by the Trump Administration includes $3 billion in tax breaks to create at least 3,000 Foxconn jobs in the US.

"TV was invented in America, but it does not have a single fab to produce a single 8K system--we are going to change that," said Foxconn chairman and founder in a White House event. "We are committed to build the most advanced 8K ecosystem in America – the most advanced in the world," Gou said.

The deal initially includes a 20 million square foot Foxconn campus. The company said it could ultimately create up to 13,000 Foxconn manufacturing jobs and up to 22,000 indirect jobs throughout the supply chain that would serve the plants requirements both in Wisconsin and elsewhere. The Foxconn jobs will have an average annual salary of (USD) $53,000 plus benefits, said Wisconsin Governor Scott Walker.

PC sales raise Intel's profits

In the midst of a bull market year for semiconductors, Intel reported strong results and lifted its financial forecast, thanks in part to better than expected sales of PC processors. Revenue hit (USD) $14.8 billion, up 9 percent from the same period last year, while net profits jumped 111 percent to $2.8 billion. The company now expects 2017 revenues of $61.3 billion at 61 percent gross margins.

Intel's PC group, which still makes up 60 percent of

company sales, grew 12 percent to $8.2 billion in the quarter. While volumes were only up in modest single digits, sales continue to shift toward gaming PCs and thin-and-light notebooks that command a premium.
Semiconductor Equipment Sales Continue Rising
Sales of semiconductor capital equipment continue to accelerate, driven by a booming memory chip market and the migration to more advanced technology nodes, according to the SEMI trade association.

North America based fab tool vendors posted both sequential and year-over-year increases in billings once again in June, setting a quick pace while the industry remains on track for record sales.

"Through the first half of the year, 2017 equipment billings are 50 percent above the same period last year," said Dan Tracy, senior director for industry research and statistics at the SEMI trade association.
Samsung Takes Number-One Spot in 2Q Chip Sales
South Korea's Samsung Electronics Company has unseated Intel Corporation as the world's leading semiconductor vendor, at least for one quarter. Samsung reported this week that its semiconductor division posted sales for the second quarter of 17.58 trillion won, or about (USD) $15.78 billion, which beats the $14.8 billion in second quarter sales that Intel reported on 27th July.

Analysts have been saying since early this year that Samsung could rise to take the top spot in chip sales in 2017, surpassing Intel, which had previously led the semiconductor industry in sales every year since 1992. The booming memory chip market, which is led by Samsung, is driving growth for that company and other memory vendors at a faster pace compared to sales advances enjoyed by makers of logic chips.

It's unclear how long Samsung can retain the top spot in chip sales. The market for memory chips is notoriously cyclical. Growth in sales for DRAM and flash memory chips has begun to slow, and analysts forecast that a downturn in memory may be looming late next year or in 2019 as new capacity comes online and new Chinese competitors enter the fray.

AUGUST

Sales rise as Apple readies to debut iPhone 8

As it prepares to celebrate the 10th anniversary of its flagship iPhone products, Apple reported its third consecutive quarter of accelerating annual sales growth which was substantially driven by an all-time high in services revenue and year-over-year growth across all its product lines.

Apple will mark the 10th anniversary of the iPhone with the launch of the iPhone 8 (and later iPhone X); new phones are typically announced at key developers conferences such as the September annual gathering of Apple enthusiasts.

The company reported on 1st August that sales for the most recent quarter totaling $45.4 billion, down 28 percent compared with the previous quarter, but up 15 percent compared with the year-ago quarter. Apple reported a net income of $8.7 billion, up 9 percent compared with the year-ago quarter.

Apple's services revenue in its fiscal third quarter grew to $7.27 billion, higher than sales of all Apple products other than iPhone. Overall sales, led by apps, music and web services, were up 3 percent from the previous quarter and up 22 percent compared to the third quarter of fiscal 2016.

Capex forecasts rise as semiconductor boom continues

Market researchers at Gartner Inc. increased their capital spending forecast for the semiconductor industry to more than 10 percent based on continued aggressive spending on new wafer-level equipment for memory and leading-edge logic circuit manufacturing. Gartner said it now expects semiconductor industry capital spending to rise 10.2 percent to reach (USD) $77.7 billion this year. The firm had previously forecast that capital spending would rise by a tepid 1.4 percent.

A shortage of NAND flash memory chips, which has led to increased prices, was more pronounced in the first quarter of the year than Gartner expected, leading to more than 20 percent growth in sales of etch and chemical vapor deposition (CVD) equipment this year with a strong capacity ramp-up for 3D NAND, according to Takashi Ogawa, a research vice president at Gartner.

Gartner's move to raise its semiconductor capital equipment forecast is right in line with other market watchers' increasing expectations for what is shaping up to be the best year for the semiconductor industry in quite some time. Several organizations, including Gartner and the World Semiconductor Trade Statistics (WSTS) organization, have increased their forecasts, predicting sales will grow more than 10 percent in 2017. Market researchers at IC Insights Inc. revised the 2017 semiconductor forecast as well, saying it now expects chip sales to rise 16 percent this year after

projecting 7 percent growth earlier in 2017.

Even More Growth Optimism from the SIA
Semiconductor sales are up nearly 21 percent year-to-date, punctuated by the highest ever sales total in the second quarter, says the Semiconductor Industry Association (SIA).

Chip sales for the second quarter totaled a record (USD) $97.9 billion, up 6 percent from the previous quarter and up 24 percent compared with the second quarter of 2016, according to the SIA. June's semiconductor sales rose to $32.6 billion, up 2 percent from May and up 24 percent from June 2016, the SIA said.

Rudolph expands in China, announces new litho systems

Rudolph Technologies, Inc. announced on 2 July that it has received an order for a JetStep® G lithography system from a second customer in China for pilot line manufacturing of next-generation AMOLED (active-matrix organic light-emitting diode) displays.

"Customers continue to invest in Rudolph's unique lithography solution for their R&D and pilot lines because it enables them to prove-out new processes more easily and at lower cost," Rudolph's vice president of Marketing, Elvino da Silveira said. "The JetStep system is especially beneficial in pilot line environments where there is a high level of product change-over and pressure to minimize cost. A JetStep mask set is a fraction of the cost of a mask set for scanner-based photolithography tools, making it an ideal choice for new product development."

Startup Sees a Cheaper Approach to 3D Chips
A startup emerged from stealth mode with a new low-cost approach to building 2.5-D chip stacks that targets Internet of Things (IoT) applications. zGlue has developed a substrate that can link more than a dozen die as an alternative to designing a more expensive and time-consuming SoC or a much larger circuit board.

The startup is one of many companies using novel packaging to make up for the increasing complexity and cost of CMOS scaling. To date, most chip stacks have been too expensive for anything but the most high performance devices, but many companies are working on lower cost options.

zGlue uses a trailing-edge interposer of 24 to 48 mm2 with integrated passives as well as a controller supporting power management and security. Its chip-to-chip interface can be configured in software and can accommodate most packages but is optimal for WLCSPs.

ITC investigates Apple

The US International Trade Commission said it will investigate Apple following allegations by Qualcomm that the iPhone maker is violating six of its non-standards-essential patents. The review is the latest move in an escalating legal battle between the world's largest cellular chip vendor and one of its largest customers.

One Wall Street analyst said he still believes the two companies could resolve most of their disputes before the end of the year, but given the escalating war of suits and counter-lawsuits, that estimate could be optimistic.

"Our forecasted resolution timing at year-end looks to be increasingly optimistic," said Ross Seymore of Deutsche Bank in a research note. The ITC typically completes an investigation within 15 months of an announcement, in this case about November 2018, he added.

Samsung Verdict Reverberates Across South Korea
A South Korean court sentenced the head of Samsung Group, Jay Y. Lee, to five years in prison. The decision is seen as a watershed for the country's techno-political climate long dominated by large conglomerates. At the same time, the court's ruling is not expected to immediately impact South Korea's fast-growing, massive electronics businesses.

The sentence was the mandatory minimum for Lee, who was convicted along with four other Samsung executives of charges including bribery of the former South Korea president, Park Geun-hye, according to a Korean newspaper report. It marks the first time a Samsung leader has been jailed, although Lee's father and grandfather both faced court actions during their tenures running the group, it said. Samsung's attorneys called the verdicts unacceptable and are expected to appeal the decisions.

Fab tool sales show signs of slowing

Billings for North American semiconductor manufacturing equipment firms increased on a year-over-year basis for the 10th consecutive month in July, but declined on a sequential basis, according to the SEMI trade association.

"We observed softening in the equipment billings in July following a strong surge in the first half of the year," said Ajit Manocha, president and CEO of SEMI, in a press statement.

The three-month rolling average for equipment billings in July totaled (USD) $2.27 billion, down 1.4 percent compared with June, SEMI said. The figure was up 32.8 percent compared with July 2016 billings of $1.71 billion.

SEPTEMBER

Lam buys modeling software leader Coventor

Semiconductor manufacturing equipment vendor Lam Research Corporation said it has acquired Coventor Inc., a provider of modeling and simulation software for chip process technology. Terms of the deal were not disclosed.

The deal brings Lam (Fremont, California) new capabilities to enable customers to address process technology challenges through software prior to fabricating a design on wafers in the fab. Coventor (Cary, North Carolina) claims that its proprietary 'virtual fabrication' technology enables engineers to understand process variation effects early in the development of a new chip, reducing the number of silicon learning cycles necessary to bring that chip to market. Such capabilities become even more valuable as chip makers push scaling further and are confronted with daunting new technical hurdles. Lam said the acquisition would support its process control vision and accelerate process integration simulation.

5G to span 'last mile' to handsets

A senior Ericcson engineer, speaking at Hot Interconnects on 5th September, said that 5G cellular will start with fixed-wireless services, lead to big changes in smartphones and ultimately rack up some staggering numbers.

Verizon and AT&T have already announced plans to use 5G at 28 and 39 GHz as a last-mile access technology starting late next year. "It will be easier to plop a pole in a neighborhood than connect homes via fiber," said Dave Allen, Ericsson.

Thanks in part to such services, Ericsson expects that more traffic will run over wireless than wired nets by 2027. The initial 5G fixed-wireless services will act as neighborhood extensions of carriers' core LTE networks. The collaborative 4G/5G roll out is different from the past, in part because pure 5G requires a fair amount of heavy lifting.

For example, millimeter wave transmitters and receivers will need to use massive MIMO antennas with beam forming on both sides. The techniques are needed to compensate for about 40 dB signal loss leaping from traditional 3G to 5G 39 GHz radios.
Semiconductor Sales Rise for 12th Month in a Row
Semiconductor sales continued to boom through July, increasing for the 12th consecutive month, according to the Semiconductor Industry Association (SIA) trade group.

Global chip sales for July totaled (USD) $33.6 billion on a three-month average basis, up 24 percent from July 2016, according to the SIA, which reports sales figures compiled by the World Semiconductor Trade Statistics (WSTS) organization. The figure also represents a 3.1 percent increase from June.

EU regulators again halt Qualcomm-NXP deal queries

European Union regulators have for a second time halted their investigation into the proposed (USD) $38 billion acquisition of NXP Semiconductors by Qualcomm.

The European Commission said in a posting on its website that the investigation was suspended on 17th August. The Reuters news service reported on 6th September that Qualcomm and NXP failed to supply regulators with key information about the proposed merger and that the investigation would resume after the information was received.

Qualcomm (San Diego) announced its bid last October to acquire NXP (The Netherlands). The EU launched an investigation into the proposed acquisition in June, citing concerns over the merged entity's position in near field communications (NFC), mobile devices and vehicle-to-vehicle and vehicle-to-infrastructure technology.

Fab tool sales set another quarterly record

Worldwide billings for semiconductor manufacturing equipment hit an all-time high in the second quarter, breaking a record that had been set in the first quarter, according to the SEMI trade association. The industry remains on track to post its best year ever, SEMI stated.

Second quarter equipment billings totaled (USD) $14.1 billion, shattering the record of $13.08 billion set in the first quarter by more than $1 billion, or 8 percent, SEMI said. Second quarter equipment billings were up by 35 percent compared with the second quarter of 2016.

Semiconductor equipment sales are riding the wave of capacity expansions and node scaling in what is shaping up to be a huge year for semiconductor sales, particularly in the memory segment. In July, SEMI projected that tool sales would hit $49.4 billion this year, breaking the record set in the dot com heyday of 2000.

Growth in the second quarter was strongest in South Korea, which is projected to be the No. 1 region for fab tool buying this year, SEMI said. Taiwan and China ranking second and third, respectively, in tool sales for the second quarter.

Samsung says EUV on schedule for 2018

South Korea's Samsung Electronics confirmed that it expects extreme ultraviolet (EUV) lithography will be placed into initial production with its 7nm Low Power Plus (LPP) process in the second half of next year.

Samsung also announced the addition of an 11nm LPP process utilizing FinFET technology to its technology offerings, saying it would deliver up to 15 percent higher performance and up to 10 percent reduction in chip area compared to its 14nm LPP process while consuming the same amount of power. EUV, the long-heralded successor to 193nm lithography that has been delayed numerous times over the past decade, finally appears to be poised for prime time with leading edge chip makers Intel, TSMC, Samsung and Globalfoundries all targeting production deployment over the next 18 months.

Rudolph proclaims 'Firefly' a hit with customers

Rudolph Technologies, Inc. announced on 12th September that its Firefly™ Inspection Systems, shipped to fulfill previously announced orders from multiple semiconductor manufacturers, are now qualified for production. The Firefly Inspection Systems provide high-resolution visual and non-visual inspection in a variety of advanced packaging processes, including fan-out wafer-level packaging, panel-level packaging and wafer-level chip-scale packaging. Rudolph expects over (USD) $5 million in revenue in Q3 2017 from the systems. Additional Firefly System shipments are expected in Q4 2017.

AI reshapes fab operations

Chipmakers are adopting artificial intelligence (AI) to boost fab operations, an effort that is starting to pay off, according to Micron Technology. Fab managers need to juggle fluid customer demand while simultaneously implementing constantly changing process technologies in multiple manufacturing sites around the globe. All this happens as chipmakers aim to achieve yield and quality targets on a corporate level as quickly as possible, according to Buddy Nicoson, vice president of wafer fabs with Micron.

AMD Solutions fare well in Tesla Systems

Tesla is examining samples of a machine-learning chip that it developed in collaboration with Advanced Micro Devices, according to a report from CNBC. AMD and Tesla both declined to comment on the story.

The chip was developed by Tesla's Autopilot group, a team of about 50 engineers under Jim Keller, a veteran microprocessor designer who led work on AMD's Zen x86 processor. The chip is expected to replace an Nvidia GPU that Tesla currently uses, which itself replaced a Mobileye chip, the CNBC report stated.

Samsung and Intel back Reno sub-systems

A group of chip companies led by Samsung and Intel have invested (USD) $11.2 million in Reno Sub-Systems, a supplier of semiconductor manufacturing process control systems.

The series C venture round was led by Samsung Venture Investment Corporation, the VC arm of South Korea's Samsung Electronics. Samsung was joined in the funding round by Hitachi High-Tech, sk Hynix and existing investors Intel Capital, Lam Research and MKS Instruments, according to the Nevada-based company. Reno Sub-Systems was founded in 2014 by a group of semiconductor industry veterans with backgrounds in the manufacturing equipment and process control space. The company offers two principal technologies: flow control for gases used in chip making and RF power generation and impedance matching of electrical loads used in the process. Both of the company's primary products offer substantial increases in performance compared to legacy solutions, the company stated.

OCTOBER

TSMC aims to build first 3nm fab

Taiwan Semiconductor Manufacturing Company (TSMC) will build the world's first 3nm fab in the Tainan Science Park in southern Taiwan, where the company does the bulk of its manufacturing.
The announcement lays to rest speculation that the company might build its next chip facility in the US because of incentives offered by the administration of President Donald Trump to bring more manufacturing to America.

About a year ago, TSMC said it planned to build its next fab at the 5nm to 3nm technology node as early as 2022. The more recent one-paragraph

announcement from TSMC on 29th September did not provide a timeframe for the opening of the 3nm fab. Monthly Chip Sales Cross $35 Billion Milestone Monthly semiconductor sales hit (USD) $35 billion for the first time in August, increasing on a sequential basis for the 13th consecutive month, according to the Semiconductor Industry Association (SIA).

The three-month moving average of chip sales increased by 4 percent sequentially and 24 percent year-to-year in August, as the semiconductor sales rally that began in the second half of 2016 continues to steamroller previous records, the SIA stated.

Dialog to buy Silego for $306 million

Dialog Semiconductor (UK) said it intends to buy privately held configurable mixed-signal IC (CMIC) vendor Silego Technology (Santa Clara, California) for up to $306 million, to grow Dialog's sales with existing customers and also expand its customer base.

Dialog executives described Silego's technology as highly complementary to Dialog's own power management and connectivity offerings. They estimated the deal would expand Dialog's total addressable market by more than (USD) $1.4 billion. Silego's CMICs combine analog, digital, and nonvolatile-memory functionality with software tools in a flexible, cost-effective design and prototyping platform. Silego announced in August that it shipped its 3 billionth device.

Chip sales forecasts continue to climb

Market watchers once again increased their forecasts for 2017 semiconductor sales growth as the 'red hot' memory chip market shows no signs of cooling. Market research firm Gartner and independent industry analysts are now predicting that chip sales will top the (USD) $400 billion mark for the first time in 2017. Gartner is forecasting that chip sales will reach $411 billion this year, a 19.7 percent increase from last year, while other forecasts fall at or slightly over the $400 billion milestone.

Price increases for memory chips, particularly DRAM and NAND flash, continue to set the pace. Gartner is now projecting that memory chip sales will rise 57 percent this year. In first quarter of the year, most industry analysts said they expected modest growth in the 5-7 percent range because of momentum that began in mid-2016.

ARM unveils new AI group

A new machine learning group at ARM will create accelerator cores, blocks for its CPU and GPU cores and software to tie everything together. Exactly what the group will deliver and when remains under wraps. Analysts suggest ARM could be as much as three years behind products from rivals such as Cadence, Ceva and Synopsys. ARM counters that these are still the early days for emerging markets where software is rapidly evolving, and that many AI-related tasks are already running on its exiting cores.

ARM declined to share the number of people or budget for the group, run by ARM fellow Jem Davies, best known for a decade working on ARM's media blocks. Rene Haas, president of ARM's intellectual property group, defined it simply as "a big team in hardware and software."

Intel again lifts its 2017 forecast

Intel raised its forecast for 2017 sales and profit after delivering third quarter results that topped Wall Street's expectations. Intel said it now expects sales for the year to total between (USD) $61.5 billion and $62.5 billion and earnings per share to be between $2.88 and $2.98 for the year. The company had earlier projected sales of between $60.8 billion and $61.8 billion with earnings per share of between $2.61 and $2.71.

IoT may require very cheap SoCs

The Internet of Things (IoT) could rise or fall on the cost of its chips—no surprise. But the latest analyst projections say that success could depend on devices costing far less than $1 each. This 'informed speculation' was delivered by a panel of technologists at ARM TechCon in Santa Clara, California during 27th October meetings. SoCs will need new kinds of memories, connectivity and sensors to scale to dimensions that the IoT will demand, but the path to get there is still unclear, they said.

Today's SRAM and flash memories, Bluetooth interfaces and sensors consume too much power to serve volume IoT nodes in 2027, panelists said. They sketched out a few possibilities for what may replace them. Ideally, a 2027 end node SoC will consume just 10 microwatts/MHz and transmit data on a radio drawing only 1 or 2 milliwatts, said Jason Hillyard, a director of software in ARM's wireless group. His "slideware SoC" used a new architecture built of sub threshold circuits suited for its energy harvesting power source.

Samsung chip sales hit another high

South Korea's Samsung Electronics Company nearly tripled its third-quarter profit, largely on the strength of (USD) $17.8 billion in chip sales, a company record for any quarter.

Growth in semiconductor profit offset sequential profit declines in Samsung's mobile handset and display businesses. The company's semiconductor business accounted for $8.9 billion of Samsung's $12.9 billion in profit, as sales of memory chips enjoyed widespread strength across all applications, especially high-performance memory chipsets for servers. Samsung, the world's largest seller of memory chips, is all but certain to pass Intel to become the number one chip vendor globally in 2017. Samsung's $17.8 billion in third quarter chip sales compares to about $16.1 billion for Intel.

Overall Semiconductor Sales Hit $108 Billion in 3Q
Global semiconductor sales topped $100 million in third quarter 2017 for the first time, reaching (USD) $107.9 billion, according to the Semiconductor Industry Association (SIA) trade group.

Third quarter sales were up more than 10 percent from the second quarter, which set the previous high-water mark for chip sales in a quarter by reaching $97.9 billion, according to the SIA, which reports sales figures compiled by the World Semiconductor Trade Statistics organization. Year-to-date, semiconductor sales are tracking more than 20 percent ahead of last year's pace. The semiconductor industry is almost certain to set a sales record this year, with sales potentially topping $400 billion for the first time, thanks largely to tremendous growth in memory revenue amid tight supply.

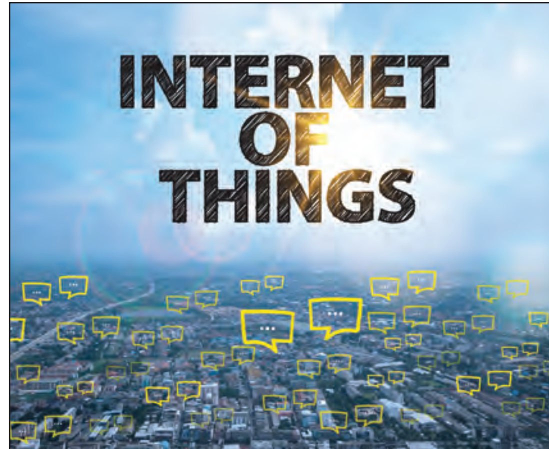
MediaTek shifts to IoT

MediaTek, which has seen its share of the smartphone business plummet during the past two years, is turning to new products such as Internet of Things (IOT) chips to drive sales growth.

MediaTek is placing more emphasis on products that are boosting sales in the third quarter, which collectively brought in about one third of the company's revenue. These chips primarily supported applications including IoT, game consoles and ASICs. The company is selling IoT devices to new customers including Amazon, Google and Chinese internet companies that MediaTek declined to name. MediaTek did say it has also made chips, including ASICs, that go into game consoles for Sony and Microsoft.

Qualcomm Profits Drop amid Apple Disputes
It is not a challenge to tell that something is 'amiss' when a high-flying company like Qualcomm has no less than five top executives on an earnings call. So it was when the company reported results for the end of its fiscal 2017.

Quarterly and annual revenues of (USD) $5.9 billion and $22.3 billion respectively were both down 5 percent compared to 2016 results, using GAAP figures. Given the loss of licensing revenues from Apple and another unnamed customer, it was not surprising profits took a bigger dive to $200 million for the quarter and $2.5 billion for the year, down 89 percent and 57 percent from 2016, respectively. The forecast is grim considering the company's storied past.



The mobile chip giant expects flat revenues for its next quarter despite a 5 percent expected rise in its chipset unit sales. Overall cellular device unit sales could rise 8 percent next year, but their average selling prices may drop given the fact that a growing share are going into more cost-sensitive systems in cars, networking and the Internet of Things.

Apple may drop Qualcomm chips

Apple is working on designs for iPhones and iPads that use modem chips from Intel and MediaTek rather than Qualcomm, according to multiple media reports citing unnamed sources. Apple may replace Qualcomm modems in the next-generation iPhone set for release next fall, according to the reports by the Wall Street Journal, the Reuters news service and the Bloomberg news service, among others.

Qualcomm has supplied basebands chips for every generation of iPhone and iPad since the first model debuted 10 years ago. However, the relationship between Apple and Qualcomm turned adversarial early this year, and the two companies are currently awaiting trial in a (USD) $1 billion lawsuit filed in US federal court by Apple in January over the royalties that Apple pays to Qualcomm, which Apple has called excessive. Qualcomm chip sales to Apple are projected to be worth about $2.1 billion this year, or about 13 percent of its total revenue, according to a report by the Wall Street Journal.

NOVEMBER

Greater DRAM supply may be coming in 2018

The DRAM supply bottleneck that resulted in slowed end-use device production and higher prices for suppliers throughout 2017 may be coming to an end. Samsung Electronics is ratcheting-up capacity to extend its lead over competitors and freeze new entrants from China out of the market, according to the market research firm, DRAMexchange. Researchers are predicting that the DRAM bit supply

will grow by 22.5 percent in 2018, up from about 19.5 percent in 2017. The firm had predicted as recently as September that DRAM bit supply would grow by 19.6 percent next year. Samsung, which owns about 45 percent market share in DRAM, is considering a plan to allocate some capacity that had been set aside for NAND flash to DRAM at its new facility in Pyeontaek, South Korea. Samsung may also add more DRAM capacity to its Line 17 fab in Hwaseong, South Korea, according to DRAMexchange.

Broadcom makes $103 billion bid for Qualcomm

Broadcom Ltd. launched an unsolicited takeover bid to acquire larger rival Qualcomm for roughly (USD) $103 billion in what would be the largest tech acquisition ever, if accepted and approved by international regulatory bodies.

Broadcom said it would offer $70 per share to acquire Qualcomm, the largest maker of mobile phone chips, a 28 percent premium over Qualcomm's closing stock price on 2nd November, the day before reports that Broadcom was planning a takeover offer surfaced amidst Qualcomm's fiscal year earnings report. Broadcom did not approach Qualcomm to discuss the deal prior to launching the bid, according to reports. The magnitude of the deal would be difficult to overstate, even in a period of unprecedented consolidation for the semiconductor industry. Qualcomm itself is still in the process of trying to close a deal for European chip maker NXP Semiconductors that was first announced a year ago, which is to date the largest announced semiconductor firm acquisition.

A combined Qualcomm, NXP and Broadcom could have total semiconductor sales of $40 billion, making it the third largest chip company ahead of TSMC but below Samsung and Intel, according to the market watchers at IC Insights. Such a deal would make 2017 the largest on record in semiconductor mergers with an estimated value of $120 billion including a reported merger proposal between Cavium and Marvell, he added. Prior to this latest announcement, 2017 had been far quieter in terms of M&A activity than 2015 and 2016.

A better lithium battery?

Want to boost the lifetime performance of a lithium-ion battery without risking fire or explosion? Taiwan's Industrial Technology Research Institute (ITRI) is proposing a quick-fix solution: a composite paste that OEMs can apply to battery electrodes. ITRI claims, with the test data to support it, that its ChemSEI-Linker paste increases Li-ion batteries' lifetime up to 70 percent. ITRI also says ChemSEI-Linker is a green technology because it enables easier recycling of Li-ion cells at the end of their extended lifetimes.

ITRI engineered the new material after analyzing why the electrodes always seem to be the weak link that causes Li-ion batteries to fail in the field. In this case, researchers looked at performance degradation, not the failures that result in fires or explosions that have been traced to the formation of dendrites on cell electrodes.

After surveying the literature and testing the most likely culprits in its labs, ITRI concluded that the primary cause of full-lifetime failure is the buildup of a predatory solid-electrolyte interface (SEI) layer starting with the very first recharge cycle. The buildup layer thickens over the lifetime of the battery, gradually degrading its performance until it works so poorly that it needs to be replaced.

Samsung to Show its EUV Plans at Next ISSCC
Samsung will describe a 7nm SRAM made with extreme ultraviolet lithography (EUV) at the International Solid-State Circuits Conference in February 2018, the company announced. Other ISSCC papers will detail memories, sensors and processors spanning everything from fast DRAMs to location trackers embedded in a boot. Reinforcing its commitment earlier this year to be the first chip maker to use EUV, Samsung will describe a 0.026µm2 SRAM bit cell in a 7nm process it plans to make available next year. The chip is the smallest SRAM described to date and uses a double-write driver to reduce minimum supply voltage.

IBM quantum computer goes primetime

IBM's quantum computer is taking a leap into commercial availability at the Supercomputing Conference 2017 this week in Denver, Colorado. Dubbed the IBM Q, and available at the time for free on-line, the system now has time-proven capabilities, attained from the free trial period. It will still be cloud hosted with a ready-to-go 20-qubit version and a 50-qubit prototype that demonstrates how to solve NP Hard (non-deterministic polynomial-time hard) problems impossible for the fastest supercomputer today. IBM will also provide an open-source quantum information software kit (QIS-Kit).

The key to its QIS-Kit is you don't need a quantum computer to compose and debug your quantum application software, but can prove its correctness first on a conventional computer. Once debugged, the software can be assured to achieve its desired goals with NP-Hard problems. In fact, IBM claims over 60,000 users have beta-tested and debugged

their QIS-Kit on over 1.7 million quantum application programs.

STMicro grows its low power MCU family

Chip vendor STMicroelectronics (Geneva, Switzerland) this week rolled out the successor to its STM32L4 series microcontrollers, offering significantly higher performance at ultra-low power consumption. The STM32L4+ devices, part of STMicro's STM32 family, feature an Arm Cortex-M core and can achieve performance of 150DMIPS (233 ULPMark-CP) at 120MHz, according to the company. Its new devices can serve as the central controller in range of products, including fitness bands, smart watches, medical devices, smart meters and industrial sensors, according to the company.

Samsung likely to hold its top chip slot

Samsung Electronics is poised to unseat Intel as the world's largest semiconductor company this year based on sales. The South Korean electronics giant has benefitted throughout 2017 from strong demand for memory chips, according to market research firm IC Insights.

Intel, which has held the lead since 1993, is expected to fall to second place behind Samsung in 2017 sales rankings, with the two separated now by a (USD) $4.6 billion gap, according to the market research firm's latest report. The jump in sales by Samsung, the world's largest memory-chip maker, is primarily attributable to soaring DRAM and NAND flash prices. Samsung first emerged in the top spot during the second quarter this year by displacing Intel. Surging memory prices are also helping SK Hynix and Micron, which are expected to make the biggest moves in IC Insights' 2017 top-10 ranking from the 2016 ranking. The memory makers are forecast to move up two spots in the top-10 ranking with SK Hynix occupying the third position and Micron moving up to number four.

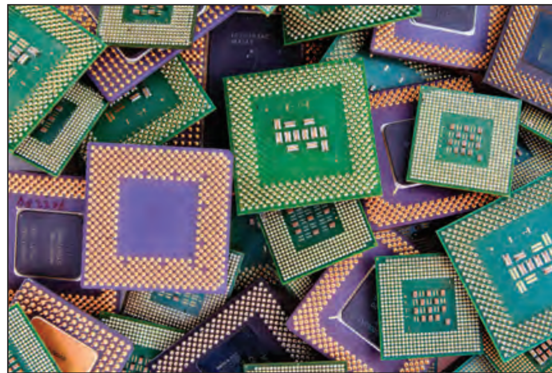
Fab tool sales decline sequentially amidst continuing IC sales boom

It is a curious condition, but one that semiconductor market watchers have seen before. Even as chip sales soar to record 2017 levels, the SEMI trade organization reported on 28th November that semiconductor manufacturing equipment sales declined on a sequential basis for the fourth straight month in October. Nevertheless, sales remained well ahead of last year's pace, beating the October 2016 figures by 23.7 percent.

SEMI reported that the three-month average of billings for North American semiconductor tool manufacturers slid to (USD) $2.02 billion in October, down 1.8 percent compared with September, while the overall equipment market is on pace for a record year with sales of greater than $50 billion expected. SEMI said in July that it expected sales to be up nearly 20 percent this year, but growth since then has pushed the number higher. The trade group had previously predicted that the market would grow another 8 percent in 2018. Almost all other market watchers predicted (in first quarter) that sales would increase between 5 and 7 percent in 2017 with modest growth in 2018.

Semiconductor stocks may be overvalued, analyst says

The market capitalization of publicly-traded semiconductor companies has risen dramatically over the past three years, driven largely by a frenzy of merger and acquisition activity and the performance of the chip market as a whole, according to International Business Strategies (IBS). The recent run-up in company valuations has most recently come from the unexpected growth that the industry has experienced, with most analyst firms predicting 20 percent expansion or more for the year.



The cumulative valuation of 15 selected non-memory companies studied by IBS rose from about $520 billion in 2015 to more than $1.07 trillion today.

Expectations of additional M&A activity and a positive assessment of the long-term prospects for the semiconductor industry among analysts and investors have also helped the cumulative valuation of the group more than double, according to IBS, which is based in Los Gatos, California.

GaN Chip vendor secures $15 million in new funding

High-voltage gallium nitride (GaN) semiconductor vendor Transphorm has secured (USD) $15 million in funding from Japan's Yaskawa Electric, bringing the total it has raised so far to more than $230 million. Transphorm (Goleta, California) was founded in 2007 and said it plans to use the funding for product development. The company announced in September that Yaskawa is using Transform's 650V GaN chips in its Σ-7 F servo motor, the first servo motor to make use of high-voltage GaN technology.

In addition to servo motors, Transphorm maintains that its high-voltage GaN technology offers performance, efficiency and reliability advantages over silicon for automotive systems, data center and industrial power supplies, renewable energy and other broad industrial applications.

DECEMBER

Walmart lends its clout to the call for cheap IoT sensors

Chris Enslin wants a sensor for his Internet of Things (IoT) applications that costs less than a dollar. Enslin knows discount retailing; as a vice president for digital enterprise solutions at Walmart he believes that if the IoT will play a large role in his company's operations the sensors will need to be 'everywhere' and will need to pay for themselves quickly. And for the right product at the right price, his company might be willing to purchase a few million of them—every year. The biggest items on his IoT shopping list are cheap sensors.

It's (almost) official: Chip sales will top $400 billion in 2017

A key semiconductor market watcher has once again revised its 2017 chip sales forecast upward after the industry posted yet another all-time record month in October. The World Semiconductor Trade Statistics (WSTS) organization said it now expects sales to increase 20.6 percent this year to reach more than $408 billion. This would mark the first time that the industry's sales topped $400 billion in any one year, just four years after surpassing the $300 billion mark for the first time. "Market growth continues to be driven in part by high demand for memory products, but combined sales of all other semiconductor products were up substantially as well, showing the breadth of the market's strength this year," said John Neuffer, president and CEO of the Semiconductor Industry Association (SIA) trade group.

Analysts have consistently raised chip forecasts along with predictions for sales of capital equipment in 2017 as surging memory prices have set the pace for what has been a strong market across almost all indices. Last week, researchers at IHS Markit projected sales would grow by 21 percent this year. In October, research firm Gartner forecast nearly 20 percent growth while IC Insights last month lifted its forecast to 22 percent growth for the year.

Startup creates a new benchmark for NB IoT

Great ideas can sometimes be found in unexpected places, like ideas espoused by startup Riot Micro that came out of stealth mode in December to announce it can offer the market a narrow band Internet of Things (NB-IoT) device that takes cellular networking to new lows in terms of power and price. Riot Micro is sampling a modem tailored for the latest 4G IoT standards. It claims that its RM1000 chip draws milliamps to microamps of power and could sell for well below the industry's target of a $5 module. Carriers around the world are just starting to turn on various flavors of LTE-based cellular IoT networks. They aim to leapfrog an emerging crop of emerging low-power wide-area networks such as LoRa, Sigfox, 802.11ah Wi-Fi, and others. The Riot Micro device is designed to handle both the Narrowband IoT and LTE Cat M1 (aka eMTC) standards.

Depth sensors potential goes deeper than iPhone X

The FaceID system in the iPhone X has demonstrated how depth sensing can enable facial detection, recognition, and authentication. But potential applications for depth sensors extend beyond those situations and the Apple iOS platform as well. Qualcomm, for one, has taken its Spectra image signal processor (ISP) technology to the next level with a 3D depth-sensing camera module for Android developed in collaboration with Apple supplier Himax Technologies. Next year could see the emergence of a depth-sensor ecosystem, including firmware and apps, as more smartphone and wearable-device vendors incorporate third-party modules in their designs, industry insiders predict.

Qualcomm combined the Spectra imaging technology with Himax's expertise in wafer optics, sensing, drivers, and module integration to create the SLiM depth sensor for mobile, augmented-reality (AR), virtual-reality (VR), automotive, and surveillance applications. Himax CEO Jordan Wu said his company had been working with Qualcomm for more than four years to develop the 3D sensing solution.

Fab tool forecast to hit record $56 billion

Sales of semiconductor manufacturing equipment are now expected to grow by nearly 36 percent in 2017, an increase from earlier forecasts that projected 20 percent growth, according to the SEMI trade association. The group expects sales to grow by another 7.5 percent next year. SEMI said it now expects sales for fab tools to reach a record $55.9 billion in 2017, passing the $50 billion mark for the first time.

The earlier forecast, issued in June, had predicted sales of $49.4 billion, which itself would have been a record. This year's semiconductor equipment buying spree, fueled by capacity expansion and record chip sales, is expected to shatter the sales record set in 2000 at the height of the dot-com bubble.

Toshiba and Western Digital bury their hatchets

Toshiba and Western Digital have announced a deal to settle all ongoing litigation and arbitration, extending their existing partnership and NAND flash development and manufacturing. The deal, which was expected by 15th December, extends the joint venture agreements between the firms to 2027 and beyond. It gives WD the right to fully participate in Toshiba Memory's Fab 6 at its Yokkaichi Operations site, which will be devoted to the mass production of bit cost scalable BiCS 3D NAND.

Walter Coon, an analyst and director for technology, media and telecom at IHS Markit, said that the settlement was in the best interests of both parties. "From the WD perspective, they had to get resolution to this [to secure future supply of NAND]," Coon said. "In the long term, even if they felt like they would prevail in the courts, I think the risk was too high."

LOGITECH
Materials Technologists & Engineers

Precision system solutions for Semiconductor wafer processing

Precision materials processing systems provide a quick and effective route to complete success in any device fabrication process

Over 50 years in the design and manufacture of precision lapping & polishing, cutting and bonding technologies:

www.logitech.uk.com

Get in touch to discuss your wafer processing needs:

enquiries@logitech.uk.com

Extending the era of Moore's Law through lower-cost patterning

Researchers at the University of California at Berkeley and Axcelis Technologies have taken a different approach to extending the Moore's Law era of solid-state transistor evolution. By using their techniques, it may be possible to forestall introducing extreme ultraviolet (EUV) lithography or simplify the multi-pattern processes that are typically used to produce today's most powerful ICs. By Peng Zheng[A], Leonard Rubin[B], Tsu-Jae King LiuA and Mark Andrews

INTEGRATED CIRCUITS (ICs) at the heart of today's most advanced computers, smartphones and myriad other devices depend upon solid-state transistors that have reliably gotten smaller and less expensive since the mid-1960s. Intel Co-Founder Gordon Moore's principles (Moore's Law) have predicted the evolution of transistor technology for more than 50 years. But miniaturizing device structures to pack more transistors into smaller spaces can only continue to a certain practical limit, which most manufacturers agree is fast approaching [1].

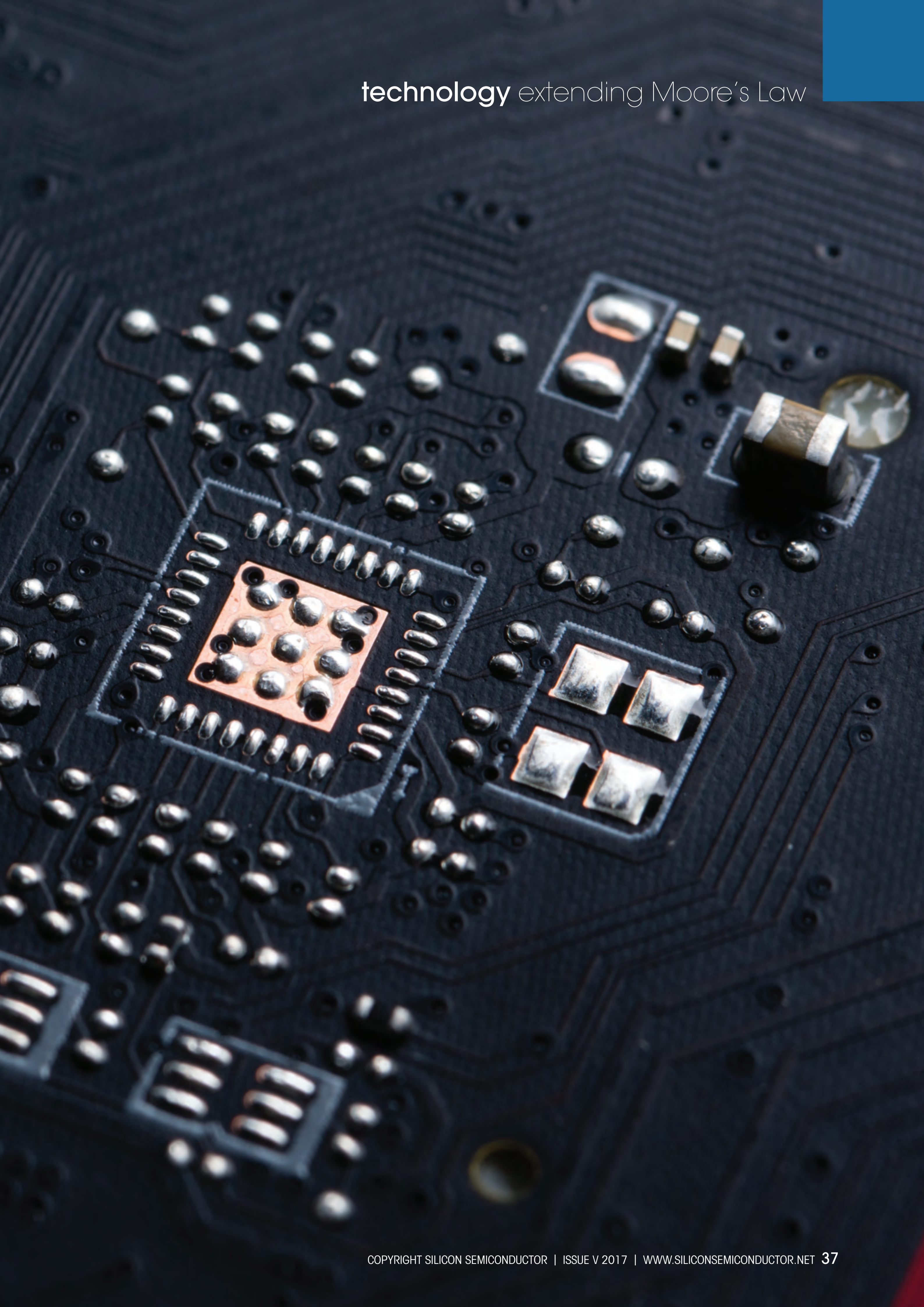
To achieve regular cost reductions through smaller geometries and increased transistor density semiconductor manufacturers have developed novel techniques that extend the limits of 193nm photolithography. As the minimum feature size of an IC has been scaled to well below the wavelength of UV light, the semiconductor industry has faced a growing challenge to increase transistor density at ever lower costs [1]. To pattern features with a resolution and pitch beyond photolithographic limits, more restrictive design rules [2] and "multiple patterning" techniques have been adopted in high-volume IC manufacturing.

But while multiple pattern approaches along with FinFETs, fully-depleted silicon-on-insulator (FDSoI), 3D ICs and chip stacking designs have enabled better performance in smaller form factors, these approaches have also typically elevated costs or extended processing time, or both. But even if cost-neutral, no multi-patterning technique can rewrite physical laws that will eventually end CMOS device miniaturization.

Self-aligned double-patterning (SADP) is a multiple patterning approach that was first demonstrated to be advantageous for forming sub-lithographic fins in a FinFET fabrication process [3] and more generally for increasing feature density [4], which has since been used for the manufacture of non-volatile memory chips (beginning at the 34 nm node in 2008 for Micron's 32 Gb flash memory product [5]) and more recently for leading-edge microprocessors (Intel's 14 nm FinFET process [6]).

It is anticipated that iterative double-patterning ("quadruple patterning") will be needed to achieve ever higher transistor density [1]. Also, as the feature density of the lowermost interconnect layers increases, more IC layers will need to be patterned using SADP or other double-patterning techniques. As a result, patterning-related costs will escalate [7] and could bring the era of Moore's Law to an end.

Major silicon IC manufacturers have considered other



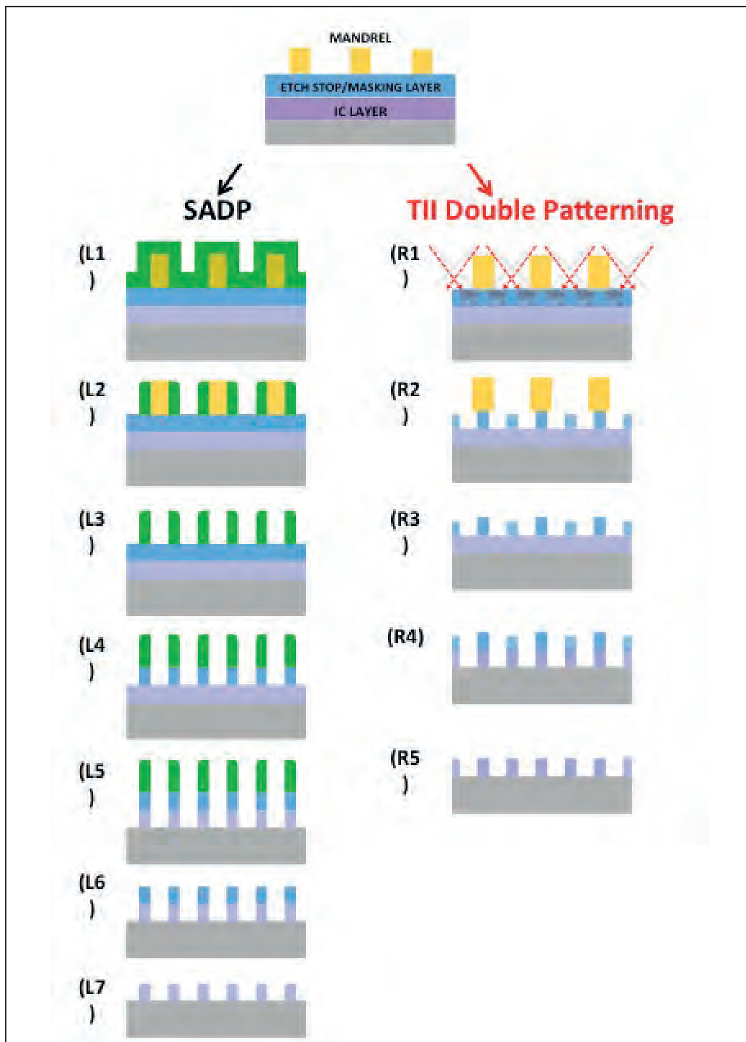


Figure 1. Schematic cross-sections illustrating the self-aligned double-patterning (SADP) and tilted ion implantation (TII) double-patterning methods. TII utilizes fewer process steps yet achieves high quality.

approaches to continue Moore's Law device evolution including extreme ultraviolet (EUV) lithography, which most believe will be required below the 7nm node.

But EUV adds still more costs and complexity to processes that are already the most complex ever seen in modern high volume manufacturing (HVM). According to ASML (Veldhoven, Netherlands,) each EUV process tool will cost upwards of (euro) 100 million. EUV photolithographic tools are about the size of a large transit bus; operational electricity is significantly more than what is used by industry-standard 193nm photolithography tools.

To address this growing challenge, Berkeley researchers proposed and demonstrated a double-patterning method that utilizes tilted ion implantation (TII) to achieve sub-lithographic features and pitches, down to below 10nm half-pitch [8-10]. The basic concepts are:

1. To use ion implantation to alter the etch rate of a thin masking layer;
2. To perform the implantation at a tilted angle since it has been demonstrated that this will achieve sub-lithographic implanted regions that are self-aligned to pre-existing photoresist or hard-mask features over the masking layer on the surface of the IC layer to be patterned.

The process sequences for SADP and TII double-patterning methods are compared side-by-side in Figure 1.

Both the SADP and TII techniques start with a patterned mandrel layer on top of an etch-stop layer or thin masking layer. SADP utilizes these steps as shown in Figure 1:

(L1) A relatively thin hard-mask layer is conformally deposited;

(L2) An anisotropic etch process is used to form hard-mask "spacers" along the sidewalls of the mandrel features;

(L3) The mandrel layer is selectively removed and the

Due to various significant issues that EUV has been facing it's not quite clear when EUV will become HVM ready. The primary driver for TII is to achieve a low-cost, sub-lithographic patterning technique with conventional CMOS processes that are already HVM ready. Compared to self-aligned double patterning, TII double patterning can reduce the processing cost and increase throughput by approximately 50% and 35%, respectively.

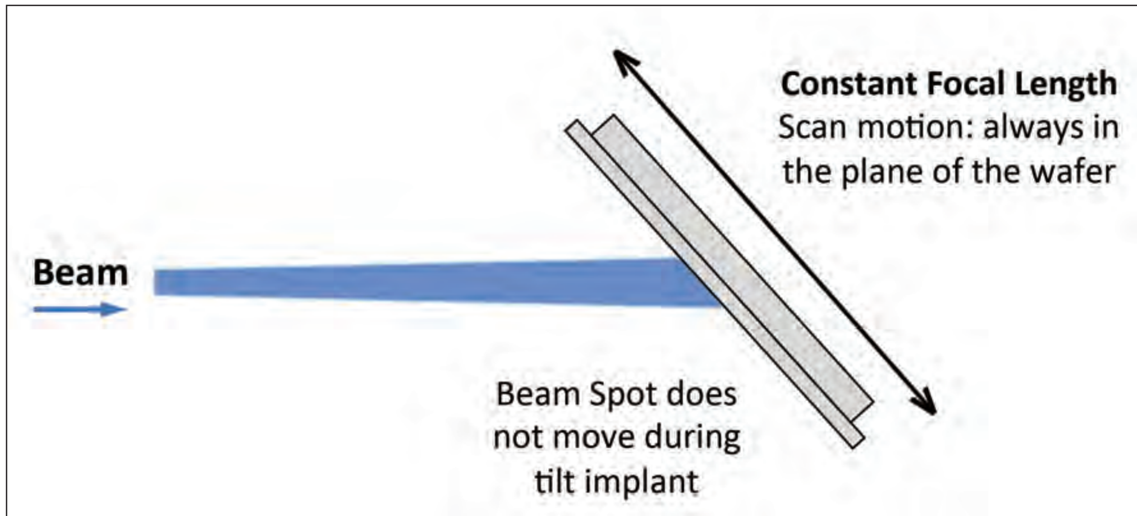


Figure 2. An illustration of tilted ion implantation (TII). An Axcelis Purion implanter was utilized to perform TII in the UC Berkeley study. Implantation is usually performed in a high-vacuum environment. Implanters can precisely control the tilt angle, ion acceleration energy and dose. TII is a contamination-free, highly precise IC manufacturing technique.

wafer is then cleaned;
(L4-L5) A multi-step etch process is used to transfer the hard-mask pattern to the IC layer;
(L6-L7) The spacers and the etch-stop layer are selectively removed.

TII double patterning utilizes these steps:
(R1) Ion implantation is performed at positive tilt angle as shown in Figure 2 and also at negative tilt angle to selectively damage regions of the mask layer, leaving the central region between the mandrel features undamaged due to the shadowing effect;
(R2) Portions of the damaged mask layer are etched away more rapidly than the undamaged portions;
(R3) The mandrel layer is selectively removed;
(R4) An etch process is used to transfer the pattern of the mask layer to the IC layer;
(R5) The mask layer is selectively removed.
The new TII double patterning approach essentially inserts an ion implantation process step between lithography and etch process steps, and can be used in conjunction with SADP to achieve quadruple patterning. It should be noted that ion implantation is a relatively simple process step as compared to deposition and etch process steps, so that the TII double patterning approach is more cost-effective.

Table I compares the number of steps and costs for TII double-patterning against those for SADP using arbitrary units (a.u.) to depict standard costs across

Table I. Cost Comparison of Double Patterning Approaches

Self-aligned Double Patterning			TII Double Patterning		
Process Steps		Cost	Process Steps		Cost
Process	**Description**	**(a.u./wafer)**	**Process**	**Description**	**(a.u./wafer)**
PECVD	Etch stop layer	1.5	LPCVD	Mask layer	2
CVD	Mandrel layer	2	CVD	Mandrel layer	2
Photolithography	Patterning	30	Photolithography	Patterning	30
Dry etch	Mandrel etch	10	Dry etch	Mandrel etch	10
ALD	Spacer deposition	3	Ion implantation	Double implants	1.7
Dry etch	Spacer etch	16	Wet etch	Selective mask etch	1
-	Mandrel pull	-	Dry etch	Mandrel removal	16
Wet clean	Clean	1	-	Pattern transfer	-
Dry etch	Pattern transfer	16	Wet etch	Mask removal	1
	Pattern transfer	-	-	-	-
Wet etch	Spacer removal	1	-	-	-
Wet etch	Etch stopper strip	1			
	Total:	**81.5**		**Total:**	**63.7**

each processing step. Clearly the TII approach requires fewer steps, which provides more than a 20% reduction in double-patterning costs.

It should be noted that the photoresist layer itself could be used as the mandrel layer in a TII double-patterning process [9] to achieve further cost savings. This is in contrast to SADP, for which the mandrel layer must be able to withstand high process temperature (greater than 150°C) associated with the hard-mask deposition process.

Summary

By eliminating the deposition, etch, and clean process steps associated with the mandrel layer, the cost of TII double-patterning can be approximately 50% the cost of utilizing SADP techniques. With TII patterning, the researchers experimentally demonstrated feature sizes of 9 nm, which indicates an approximate 20 nm pitch is achievable.

The Taiwan Semiconductor Manufacturing Company said in its latest 7 nm technology paper[11] presented at the 2016 IEEE International Electron Device Meeting (IEDM), that the smallest metal pitch is 40 nm. Hence, TII is expected to be a very intriguing new candidate for the 5nm technology node and beyond.

TII double-patterning presents a technological pathway for the semiconductor industry to extend the era of Moore's Law without additional costs or process steps. A number of semiconductor companies have expressed interest in developing the TII technique for high volume manufacturing (HVM) and the researchers are pursuing those queries.

The research team welcomes industry collaboration to further develop different aspects of TII techniques.

© 2017 Angel Business Communications.
Permission required.

Researcher Affiliations:
A) Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, 94720 USA
B) Axcelis Technologies, 108 Cherry Hill Drive, Beverly, Massachusetts 01915 USA

References:

[1] Mark Lapedus, "What If EUV Fails?" Semiconductor Engineering, April 17, 2014. http://semiengineering.com/what-if-euv-fails/

[2] C. Webb, "45nm Design for Manufacturing," Intel Technology Journal, vol. 12, no. 2, pp. 121-130, 2008.

[3] Y.-K. Choi, T.-J. King, C. Hu, "Nanoscale CMOS spacer FinFET for the terabit era," IEEE Electron Device Letters, Vol. 23, No. 1, pp. 25-27, 2002.

[4] Y.-K. Choi, J. S. Lee, J. Zhu, G. A. Somorjai, L. P. Lee, J. Bokor "Sublithographic nanofabrication technology for nanocatalysts and DNA chips," Journal of Vacuum Science and Technology B, vol. 21, p. 2951, 2003.

[5] Ann S. Mutschler, "Intel, Micron launch 34-nm, 32-Gb NAND flash memory at SSDs," EDN Network, May 29, 2008. http://www.edn.com/electronics-news/4326011/Intel-Micron-launch-34-nm-32-Gb-NAND-flash-memory-at-SSDs

[6] S. Natarajan et al, "A 14nm Logic Technology Featuring 2nd-Generation FinFET Transistors, Air-Gapped Interconnects, Self-Aligned Double Patterning and a 0.0588μm2 SRAM cell size," in IEDM Tech. Dig, 2014, pp. 71Ð73.

[7] A. Raley, S. Thibaut, N. Mohanty, K. Subhadeep, S. Nakamura, A. Ko, D. O'Meara, K. Tapily, S. Consiglio, P. Biolsi "Self-aligned quadruple patterning integration using spacer on spacer pitch splitting at the resist level for sub 32nm pitch applications," Proc. SPIE vol. 9782, Advanced Etch Technology for Nanopatterning V, 97820F (April 1, 2016).

[8] P. Zheng, S. Kim, D. Connelly, K. Kato, F. Ding, L. Rubin and T.-J. King Liu, "Sub-lithographic Patterning via Tilted Ion Implantation for Scaling beyond the 7 nm Technology Node," IEEE Transactions on Electron Devices, Vol 64, No. 1, pp. 231-236, 2017: http://ieeexplore.ieee.org/document/7740901/

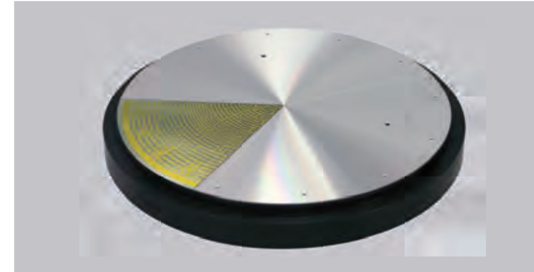
[9] P. Zheng, "Advanced MOSFET Structures and Processes for Sub-7 nm CMOS Technologies" Ph.D. dissertation, Department of Electrical Engineering and Computer Sciences, University of California at Berkeley, Berkeley, CA, USA, 2016: https://www2.eecs.berkeley.edu/Pubs/TechRpts/2016/EECS-2016-189.pdf

[10] Rick Merritt, "Process Makes Smaller, Cheaper Chips" EE Times, January 6, 2017. http://www.eetimes.com/document.asp?doc_id=1331098

[11] Shien-Yang Wu (Et Al) Taiwan Semiconductor Manufacturing Company (TSMC), "A 7nm CMOS Platform Technology Featuring 4th Generation FinFET Transistors with a 0.027um2 High Density 6-T SRAM cell for Mobile SoC Applications," IEEE International Electron Device Meeting (IEDM), December 3-7, 2016. http://ieeexplore.ieee.org/search/searchresult.jsp?newsearch=true&queryText=A%207nm%20CMOS%20Platform%20Technology%20Featuring%204th%20Generation%20FinFET%20Transistors%20with%20a%200.027um2%20High%20Density%206-T%20SRAM%20cell%20for%20Mobile%20SoC%20Applications

WATLOW® SEMICONDUCTOR

Watlow's Thermal System Solutions Enable Next Generation Technology



Watlow® offers:

- Precision designed heater circuits embedded in ESCs and chamber components
- Innovative solutions for gas line heating
- Thermal system integration with heaters, sensors and controllers
- Analytical, FEA and CFD capabilities
- Over 12,000 square feet of cleanroom manufacturing

Powered by Possibility

Visit us at **SEMICON® WEST** *booth #5344, and ask us about our new ATS technology.*

For more information visit our website at www.watlow.com

Automating cleaning processes **for quality and volume**

Cleaning process repeatability is often critical to uniform product quality and can enable higher volume production throughput explains JST Manufacturing.

THE CONSISTENT PURITY of materials used to fabricate components of electronic devices can have a critical impact on their performance. For example, producing semiconductor-grade silicon used for electronic chips involves upstream cleaning of polysilicon chunks to a purity of has high as 11N, which translates to 99.999999999 percent. For photovoltaic applications such as solar cells, the silicon purity levels are not quite as high (5N) but critical to producing efficient photoeffect.

These and many other types of products used by the MEMs, biotech, LED panel and other micro-and nano-technologies that depend on uniformity that is provided by the repeatability of automated cleaning systems. The cleaning process usually incorporates cleaning agents such as chemicals, an appropriate rinse bath, and a method of drying the material.

Chemicals may also need to be heated and or product agitated to provide optimal cleaning results. An accurate means of measuring and dispensing cleaning agents safely and also safely transporting the products and materials being cleaned are required.

Manually operating a cleaning process calls for at least some worker intervention to precisely perform the above activities using a production system such as a wet processing bench. Because some cleaning processes require etching with harsh chemicals, worker safety is also a concern.

"Companies that choose to automate a cleaning process usually do so for one or both of two reasons", says Louise Bertagnolli, president of JST Manufacturing (Boise ID). JST designs and manufactures a variety of manual and automated cleaning equipment, including proprietary systems that include all of the features and transfer devices required for a complete turnkey cleaning process. "The first reason is repeatability, the ability to precisely repeat a cleaning process, including the exacting measurement and dispensing of the cleaning agents and rinsing solutions as well as providing the systems and tools necessary to clean and transport the items being cleaned from one bath to another," Bertagnolli explains. "This ensures that all materials or products will be uniform in purity, and a 'plus' benefit of worker safety is also provided."

The second reason some companies automate the cleaning process is to enable greater throughput for high-volume production. If the process takes place in a cleanroom, then the entire system including motors and robotics must be appropriate for that environment.

"There is also another class of semi-automatic equipment that enables automated process control, a built-in transfer system and other features on a relatively small footprint," Bertagnolli adds. "This type of system is an economical solution to lower-volume cleaning of such products as nuclear sensors, crystals, and polysilicon."

Ensuring successful automation

Customizing cleaning systems can provide high dividends, yet it is also a complicated undertaking and requires engineers and technicians who understand the individual needs of customers.

JST works with automation partners such as Bosch Rexroth (Charlotte, NC) to develop comprehensive wet-bench cleaning stations using linear motion and electric drive and control technology.

In a recent project the two firms worked together to create an automated system for cleaning silicon

chunks to the extreme purity of 11N to meet requirements for the manufacture of semiconductor chips. The project entailed building a cleaning line 138 ft. in length and incorporating multiple gantry robots.

"The throughput volume requirement for these chunks was four tons for every 22-hour shift," Bertagnolli explains, "so we had to develop a basket system to transport the material throughout the application. The process included etch-cleaning and vacuum drying that volume, which was difficult because the chucks all had a variety of uneven surfaces."

To provide for such a long cleaning system, JST engineered and built it in two units. In the 24-ft-long unit, baskets of chunks are manually loaded through an auto-door. Then two-axis robots cycle the baskets through five acid etch baths and two rinse baths arranged in a single row down the length of the second unit.

Throughout the silicon cleaning process, protecting the components against contamination and pitting is critical. Yet, one on the unusual aspects of this cleaning system is that the first unit of the line employs overhead gantry, or Cartesian robots, which are not often used in semiconductor process systems to avoid generating particles over the product.

However, after extensive particle testing in cleanroom conditions, the system proved to generate far fewer particles than the specifications allowed. Proprietary seals keep the linear motion rolling strips clean and prevent the chemical etch from pitting the linear modules. The system incorporated other features to ensure the system met Class 10 cleanroom standards or better.

JST and Bosch Rexroth also partnered on a "sister" project that involved the cleaning of silicon "seed rods" that grow the polysilicon ingots from which the chucks are made.

The seed rod cleaning tool also utilizes a gantry robot to move the ingot-carrying cylindrical carriages through a sequence of etch baths. One of the keys to that solution is a custom designed fixture that rotates the rods in order to have them etched evenly.

"This rotational fixture also enables the rods to be cleaned to a very high purity," Bertagnolli notes. "We use a variety of rotational cleaning fixtures quite often, but also incorporate other designs and techniques as well – whatever will be most effective in getting the job done efficiently."

Bertagnolli advises that not every project is fully customized from the ground up. Quite often standard automation platforms can be customized according to length and height and number of baths. Cleaning

process designers can consult with automation suppliers to determining where to put the transfer system and what automation modules will fit best in the space available,

The semi-automated system

Many processors with lower volume throughput requirements might consider semi-automated cleaning systems, which can provide the advantage of repeatability as well as other production advantages and added safety. This type of cleaning system is appropriate for MEMs, LEDs and silicon applications. It is compact, software controlled and usually easy to service.

JST manufactures a standard compact semi-automated wet bench called the Tigress, a two axis, front-to-back compact system that is used by smaller semiconductor companies.

A dual version of this semi-automatic system is also available. It is popular among semiconductor manufacturers who use it for cleaning, stripping, and etching of semiconductor substrates who use cleaning acids and bases or solids to remove photoresists.

"These semi-automated cleaning systems are ideal for companies that are cleaning MEMs and smaller semiconductors. They are a very cost-effective means of automation," Bertagnolli says.

© 2017 Angel Business Communications.
Permission required.

Sophisticated coatings
on challenging substrate shapes

KJLC describe a completely new method of achieving excellent uniformity on both flat and curved surfaces without masks.

MANY OPTICAL COATING applications require excellent uniformity in both the physical thickness and optical properties of the deposited films. As interest grows in sophisticated coatings on challenging substrate shapes, such as aspheres, high performance eyewear, bevelled cell phone screens, camera lenses and a variety of other products, meeting these uniformity requirements becomes more difficult.

Physical masks are typically used along with substrate motion to control thickness uniformity. In the case of thermal evaporation, which uses small sources, large throw distances, and is line-of-sight in nature, this is often adequate and numerous models exist for generating mask designs [1]. However, even when models are used, shadow masks take time to produce and adjust and can be a source of flakes leading to particulate defects. And as the substrate size is reduced, properly aligning the masks over a large number of small parts becomes a problem. Achieving uniformity for sputtered coatings is even more difficult. Sputtering uses relatively large sources and small throw distances, scattering by the working gas makes it non-line-of-sight, and the distribution of the sputtered material can change with time as the target erodes. These factors make calculation of a precise mask design for complex shapes very challenging. Furthermore, the scattering of sputtered material depends on the atomic mass so that a single set of masks may not be able to provide the needed uniformity for two materials. To address these issues, complex motion of the masks or masks that are attached to the substrates has been suggested [2,3]. The approach taken here eliminates the need for such complicated solutions.

The system relies on inverted cylindrical magnetrons, which sputter from the inside surfaces of cylindrical cathodes. The plane of the substrate holder is perpendicular to the cathode axis, so that the substrates are coated in an off-axis configuration (not directly facing the targets). By adjusting the position of the substrates along the cathode axis and

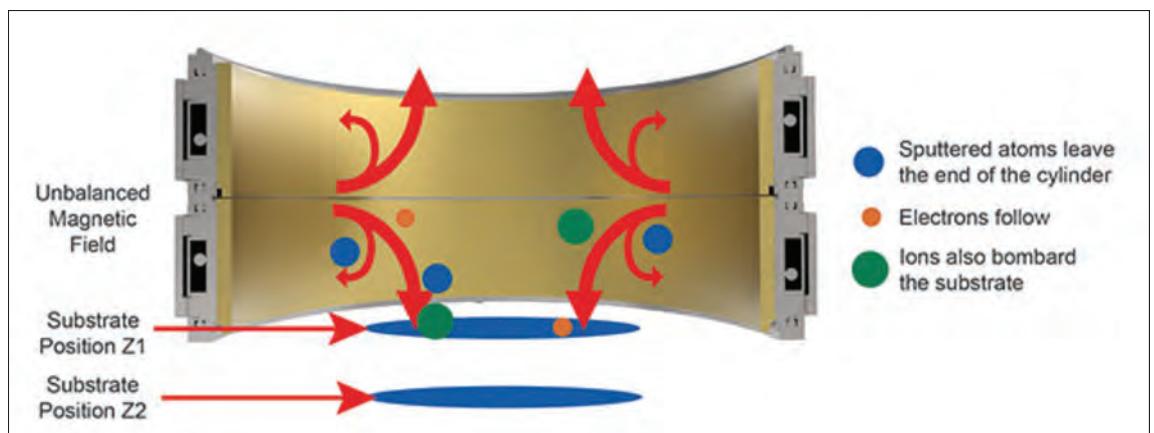
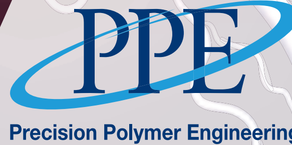


Figure 1. Cutaway view of a cathode showing the unbalanced magnetic field and off-axis substrate configurations

Introducing two new Perlast® elastomer materials – offering the ultimate plasma resistance



EMEA: +44 1254 295 400
USA: +1 408 441 2043
ASIA: + 886 922 326108
www.prepol.com/plasma

A4 SERIES

Energy efficient dry multi-stage Roots process pumps for all semiconductor applications

- Low energy consumption
- Improved temperature management to optimize the pump according to your process
- Protection of the pump against precursor cracking or condensable deposition
- Corrosion resistant and high particle tolerance
- Extended monitoring functionalities

Are you looking for a perfect vacuum solution? Please contact us:
Pfeiffer Vacuum, Inc. · USA · T 800-248-8254 · F 603-578-6550 · contact@pfeiffer-vacuum.com
www.pfeiffer-vacuum.com

rotating them in a conventional dual planetary motion, excellent uniformity is possible on substrates ranging in shape from flat to cylindrical.

System description

a. Cathodes and cathode operation

The key to the system is the use of two inverted cylindrical magnetron (ICM) cathodes. Each cathode has two electrodes that are driven with mid-frequency AC power, as shown in Figure 1.

Metal targets with inside diameters of 400 mm and heights of 100 mm fit inside each electrode and for the work reported here, one cathode contained two Si targets and the other cathode contained two high index material targets, either Ti or Ta. Sputtering was done with the target surfaces completely oxidized (the fully poisoned mode) in order to work in a stable part of the hysteresis curve. The process gases were introduced above both cathodes and typical conditions were 35 sccm of both Ar and O2, which resulted in a pressure of 3 mTorr as measured by capacitance manometers in each cathode. The SiO2 was deposited at a total power of 2.0 kW, the TiO2 at 4.0 kW and the Ta2O5 at either 4.0 kW or 6.0 kW. At 2.0 kW the SiO2 deposition rate is 12 nm/min and at 6.0 kW the Ta2O5 rate is 11 nm/min.

Figure 1 shows two alternative substrate locations, referred to as the z position. When the substrate holders are on the transfer arm in the central chamber their z position is zero and a z position of 30 cm places them at the bottom of the lower target in each cathode. Thickness uniformity on substrates with different curvatures is controlled by simply adjusting the z position of the substrate holder.

Figure 2. Cutaway view of the system layout showing the load lock on the left and sputtering cathode on the right.

b. Ion Assisted Deposition without an Ion Source

The ICM cathodes incorporate unbalanced magnetic fields, as illustrated by the arrows in Figure 1 [4,5]. A very important consequence of this magnetic field configuration in combination with mid-frequency power is that significant ion production occurs when secondary electrons cross the field lines as they flow to the instantaneous anode [6]. In addition, secondary electrons can move easily along the unbalanced field lines, represented by the large arrows extending out the ends of the cathode, and they produce a significant negative self-bias on the substrate. The self-bias and high ion density result in a low energy ion flux of approximately 2 mA/cm2 that bombards the growing film [5]. This is similar to the ion fluxes found in other ion enhanced deposition systems, but without the need for a separate ion source.

c. Mechanical Configuration

Figure 2 is an illustration of the mechanical configuration of the system. The chamber on the upper left is a load lock and a cutaway of one of the cathodes can be seen on the upper right. The second cathode is in the rear.

Substrates are held on 300 mm diameter platens and in the configuration used for this work each platen contained 16 substrate holders, each with a diameter of 50.8 mm. The holders are arranged in four sets of four moving in dual planetary motion. That is, each set of four holders rotates about a central axis and each holder rotates about its own axis. Other configurations are possible and in one set of experiments 100 mm diameter rotating substrates replaced the 50 mm substrates. We also measured the uniformity for 250 mm diameter stationary substrates.

The load lock is used to increase throughput and improve coating repeatability. A platen is manually loaded into the load lock and once the setpoint pressure is reached it automatically moves from the load lock onto a transfer arm in the large central chamber. The platen is then rotated to a position below the appropriate cathode and lifted into position in that cathode. Full computer control tracks the platen and takes it through the deposition cycle following a defined program recipe.

The system is pumped by a 2,000 l/s turbomolecular pump in the central chamber and the process gases are introduced above the cathodes, as described earlier. The platens are designed so that they limit the conductance between the cathodes and the central chamber, so that during operation the central chamber is at less than 1 mTorr pressure. This allows the pressure in each cathode to be independently varied between 1 and 5 mTorr while both are operating. Platens can be in process in both cathodes simultaneously and while a platen is being pumped down or vented in the load lock. This

Material	Present system	Prototype system
SiO_2	1.459 ± .004	1.47
Ta2O5	2.147 ± .016	2.14

Table 1. Refractive indices for films made in the present system measured using reflectance spectroscopy and for films made in a prototype system that were measured using ellipsometry.

offers remarkable flexibility in how the system can be operated. Since the uniformity for a given substrate curvature depends on where the platen is positioned within the cathode, substrates of different curvatures can be in process simultaneously. Moreover, platens receiving different coating structures can be in process simultaneously as well. A platen of substrates requiring a 16 layer structure and a platen requiring a 200 layer structure can be coating together and when the 16 layer structure is complete it can be removed from the system while the 200 layer structure continues. Accommodations for an optical monitoring system capable of either reflection, transmission or both are built into the system.

There are several additional advantages to the cathode design and off-axis configuration. Because the substrates do not face the targets directly, they are not bombarded by high energy reflected neutral atoms and negative oxygen ions formed at the target surface, which are known to produce high levels of stress in sputtered coatings. Moreover, the total target area in each cathode is 2,500 cm2 so that cylindrical targets that are only 2 mm thick provide the same material inventory as a 25 cm diameter by 1 cm thick conventional circular magnetron. The much shallower erosion grooves that result with thin targets have a minimal effect on the sputtered material distribution over the target lifetime. Finally, the large target area permits operation at power densities of 3 W/cm2 or less, which virtually eliminates arcs and microarcs that are sources of particulates that can get entrained in the coatings.

Experimental procedures and results

a. Refractive indices

The reflectance spectra of coatings deposited on Si wafers were measured using a Filmetrics Model F2 and the values for the indices and thicknesses were found by using the Filmetrics internal software to generate the best fit to the data in each case. The fits for the SiO2 and Ta2O5 measurements were 99.9% for three samples of each material made in separate runs. Previously, indices for SiO2 and Ta2O5 were measured using ellipsometry on coatings produced in a prototype system having targets with inside diameters of 330 mm, but that were otherwise identical to the ones in the present system [5]. Table 1 shows the results for the real part of the index at a wavelength of 633 nm for both sets of measurements.

The data in Table 1 show that the coatings produced with unbalanced inverted cylindrical magnetron cathodes using mid-frequency power have indices that are comparable to those produced in other ion enhanced deposition processes.

Ta2O5 samples were submitted for durability testing according to MIL-C-675C, MIL-C-48497A and MIL-M-13508C and met the requirements for adhesion, humidity stability, temperature stability and moderate abrasion. SiO2 and Ta2O5 samples deposited in the prototype system were measured for their change in thickness and index as functions of temperature up to 350 C using ellipsometry [5].

No changes in either the thicknesses or indices were seen up to 150iC. At 350iC the indices of both materials increased by approximately 0.4% and the thicknesses of both decreased by approximately 0.4%, leaving the optical thickness unchanged in both cases.

b. SiO_2 Stress

The stress of SiO2 deposited in the system was measured in two separate experiments. In the first, a 965 nm thick coating was deposited onto a 25 mm diameter by 250 micron thick BK7 glass disc and the change in curvature was measured optically. In the second a 957 nm thick coating was deposited onto a 50.8 mm diameter by 500 micron thick <100> oriented Si wafer and the change in curvature was

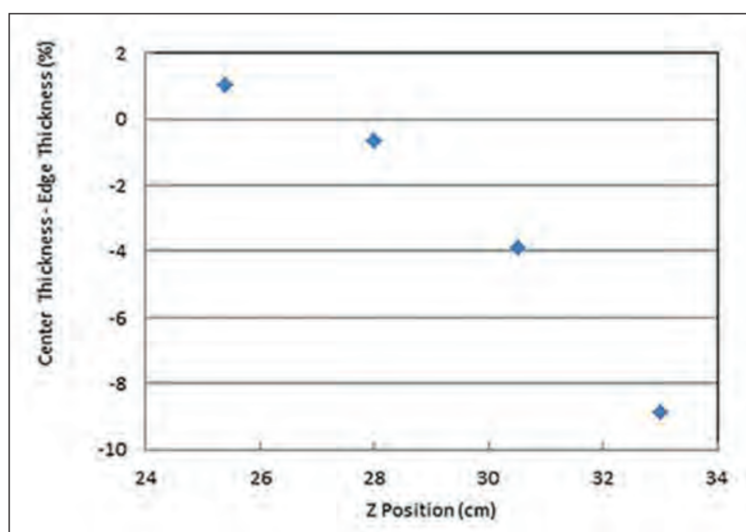


Figure 3. Relative difference in TiO2 film thickness from the center to the edge of convex lenses coated at different z positions. In each case the substrate diameter was 50.8 mm and the radius of curvature was +51.5 mm.

Diameter	Radius of curvature	Uniformity
50.8 mm	Flat	±0.1%
50.8 mm	+200 mm	±0.15%
50.8 mm	+100 mm	±0.15%
50.8 mm	+50 mm	±0.3%
50.8 mm	-50 mm	±0.5%
100 mm	Flat	±0.3%

Table 2. Coating thickness uniformity for substrates with a variety of curvatures at the optimum z position in each case

measured using a stylus profilometer. In both cases Stoney's equation was used to calculate the stress and yielded compressive values of -230 MPa and -200 MPa, respectively.

c. Thickness uniformity

As discussed, film thickness uniformity on substrates with different curvatures is controlled by adjusting their z position along the axis of a cathode during deposition. In order to map the thickness uniformity on substrates with various curvatures, TiO2 was deposited onto 50.8 mm diameter BK7 flats and lenses at different z positions. The radii of curvature of the lenses were -51.5, +51.5 mm, +103 mm and +206 mm, where Ð refers to concave and + to convex. Dual planetary rotation was used in all of these cases. Si wafers with diameters of 127 mm were also coated and were only rotated about their own axes. Finally, 152 mm diameter Si wafers were used to measure the thicknesses from the center of the substrate holder to a radius of 125 mm at several z positions without any substrate rotation.

The reflectance spectra of the coatings on the BK7 substrates were measured at the center and edge using a Filmetrics F10 AR unit with a fiber optic probe. The relative thickness difference from the center to the edge for each substrate was calculated by measuring the difference in the wavenumbers at which the reflectance extrema occurred divided by the average wavenumber. Using this method, three replicate sets of measurements of a lens having a radius of curvature of -50.8 mm gave a pooled standard deviation for the total variation of a given measurement of the thickness of 0.05%. The thicknesses on the Si wafers were measured using a Filmetrics Model F2 unit.

Figure 3 shows the difference in thickness from center to edge as a function of z position for TiO2 coatings on BK7 lenses having a radius of curvature of +51.5 mm.

These data illustrate the general result that as a convex substrate is moved further into the cathode, the relative thickness on the edge increases. This agrees well with calculated results based on a model that assume a cosine distribution of material from the targets.

Table 2 summarizes the optimum uniformity results for the BK7 flats and lenses as well as for the Si wafers.

We should emphasize that because we are taking advantage of the material distribution produced by the targets, coatings can be produced on small lenses with uniformities that would be very difficult to achieve using masks because of the registry problem mentioned earlier.

Figure 4 shows the relative thickness from the center of the substrate platen out to a radius of 125 mm for Ta2O5 deposited onto a stationary substrate.

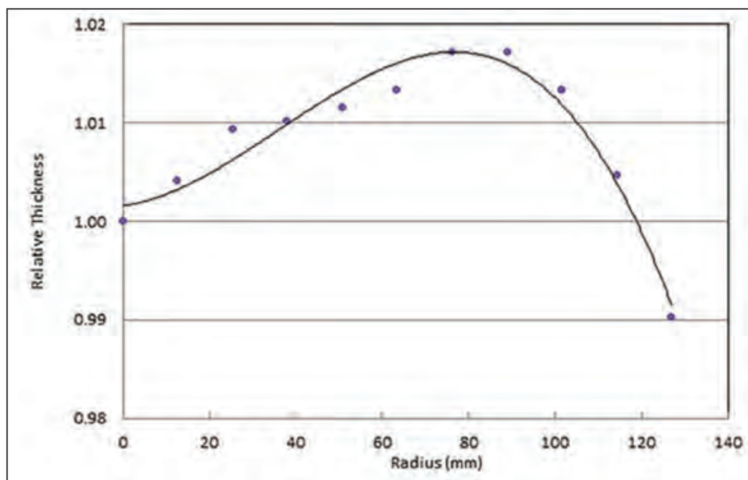


Figure 4. Relative thickness measured from the center of the substrate platen for a stationary substrate

These data show that a thickness uniformity of ±1.0% can be achieved over 200 mm diameter stationary substrates or ±1.5% over 250 mm diameter stationary substrates. And in some applications it may be desirable to take advantage of the ±0.5% uniformity that can be achieved over a 20 mm to 100 mm annulus, which is an area of 300 cm2.

Summary

We have presented results on a new method of depositing coatings onto both flat and curved surfaces with excellent uniformity without the need for masks using sputtering sources that achieve ion enhanced coating quality without a separate ion source. The system is simple and extremely flexible, allowing

substrates of different shapes with different layer structures to be in process simultaneously. In the case of flat substrates, excellent uniformity is possible over large areas without motion.

© 2017 Angel Business Communications.
Permission required.

The VIPER platform utilizes inverted cylindrical magnetrons for generating high precision optical coatings on planar, concave, and convex substrates.

Further reading

1. C. Liu, M. Kong, C. Guo, W. Gao and B. Li, Theoretical design of shadowing masks for uniform coatings on spherical substrates in planetary rotation systems, Opt. Express, Vol. 20 No. 21, 23790Ð23797 (2012)
2. L. Abel-Tiberini, F. Lemarquis and M. Lequime, Masking mechanisms applied to thin-film coatings for the manufacturing of linear variable filters for two-dimensional array detectors, Applied Optics, Vol. 47 No. 30, 5706-5714 (2008)
3. K. Lee, M. Mazur, K. Lee and R. Martinson, System and method for transporting and sputter coating a substrate in a sputter deposition system, U. S. Patent No. 6,406,598, issued June 18, 2002
4. D. A. Glocker and M. M. Romach, Unbalanced plasma generating apparatus having cylindrical symmetry, U. S. Patent No. 6,497,803, issued December 24, 2002
5. M. M. Romach, G. Scherer, J. Eichenberger, J. Lanzafame, D. Glocker, M. Jaszcar and B. Rayner, Inverted cylindrical magnetron sputtering of optical coatings, Proceedings of the 57th Annual Technical Conference of the Society of Vacuum Coaters, 233-238 (2014)
6. D. A. Glocker, M. M. Romach and V. W. Lindberg, Recent developments in inverted cylindrical magnetron sputtering, Surface and Coatings Technology, Vol. 146-147, 457-462 (2001)

Authors

David Glocker[1], John Lanzafame[1], Rob Belan[2], Nick Griffin[2] and Sean Armstrong[2]
[1]Isoflux Incorporated [2]Kurt J. Lesker Company

Benefit from a reprint featuring your company

They can be ordered after publication and can be customised to your exact needs.

For more information, contact the sales team now.

Shehzad Munshi
T: +44 (0) 1923 690 215
E: shehzad.munshi@angelbc.com

Adam Richardson
T:+44 (0) 2476 718 970
E: adam.richardson@angelbc.com

Hydrogen in Electronics:

Growing applications and consumption

Hydrogen will play an increasing role in semiconductor manufacturing due to its wide serviceability and importance in extreme ultraviolet (EUV) lithography. Linde Electronics' head of market development, Dr. Paul Stockman, explains why ensuring a safe and reliable source of hydrogen will be critical for next-generation device manufacturers.

COLORLESS, odorless, and even burning with an invisible flame, hydrogen is nevertheless omnipresent in the semiconductor fab and an increasingly important material for chip manufacturing. Leading-edge wafers consume more than their own weight of this ultra-light gas during processing and the long-anticipated adoption of EUV (extreme ultra-violet) lithography will drive demand even further.

This article reviews the properties of hydrogen that make it essential for leading-edge semiconductor manufacturing, details the specific processes that require hydrogen including the coming high-demand EUV application, and reviews the different supply options available.

Important properties of hydrogen

Composed of the lightest element, molecular hydrogen (H_2) has some extreme properties that give rise to its usefulness and hazards.

Chemical reducer: Molecular hydrogen is useful for the direct substitution of hydrogen atoms for other elements, as well as influencing the pathways of key chemical reactions.

Heat transfer: Hydrogen is able to convectively remove heat faster than any molecule other than helium.

Light mass: Hydrogen is one of the smallest molecular compounds of any gas or liquid fluid and can therefore "fit" in places that other molecules cannot, including in the porous voids of some solid materials. Its light mass also makes it relatively inexpensive to transport on a volume basis, but conversely expensive to transport on a mass basis. Compared to air, hydrogen is nearly 15 times lighter and quickly rises and diffuses.

Kinetic isotope effect: Chemical reaction rates change when one stable isotope of an atom is changed for another. Often this is a slight effect, but because hydrogen's (mass = 1 amu) stable isotope deuterium (mass = 2 amu) is twice as heavy, this effect can be significant.

Low boiling point: Hydrogen boils at a very low 20.7 K (-423.2°F or -252.9°C), second only to helium. It therefore takes a lot of energy to liquefy hydrogen, a consideration in its transport and purification.

Flammable and explosive limits: Hydrogen's most hazardous properties are its wide range for flammability (ability to burn with an ignition source) and explosivity (ability to explode or to cause a shock wave) in air. Hydrogen forms flammable mixtures between 4 and 75% concentration in air, and explosive mixtures between 18 and 59% in air. Fortunately, the buoyancy of hydrogen relative to air means small leaks of hydrogen usually diffuse rapidly below these limits.

Existing process applications

Hydrogen has been adopted as a material in processes throughout the fab. Its unique chemical properties continue to expand its usefulness. These applications typically use flows of 100s to 1,000s of sccm (standard cubic centimetre per minute):

Epitaxy: Hydrogen is used as a reducing agent during the epitaxial growth of crystalline thin-films. This is often used to make a starting silicon surface for semiconductor manufacturing by reacting newly cut and polished silicon wafers with trichlorosilane ($SiHCl_3$) in an epi-house or end-user fab. The hydrogen reduces the gas-phase chlorine atoms, and the HCl product is removed from the reactor as a gas. Leading-edge channel materials like strained silicon, silicon-germanium, and germanium are also grown using hydrogen-mediated epitaxy.

Deposition: Hydrogen can also be incorporated directly into thin-films to disrupt crystal lattices to make them less crystalline, more amorphous. This is often used with silicon thin-films, which need to be made more electrically insulating.

Plasma etch: Hydrogen and hydrogen-containing plasmas are used to directly react with the surface of the wafer in order to clean or remove unwanted thin films, especially for removing unwanted fluorocarbon deposits on silicon oxides.

Anneal: Silicon wafers are heated to temperatures over 1000°C, often at elevated pressure, in order to repair their crystal structures. Hydrogen assists by transferring heat uniformly over the surface of the wafer, and also by penetrating into the crystal lattice to react with atomic impurities.

Passivation: Hydrogen is used to react and remove native oxides on silicon surfaces and to mediate the reconstruction of silicon-silicon bonds in the final layers of the crystal.

Ion implantation: With more precision than bulk annealing and passivation, protons produced from hydrogen gas can be implanted to specific depths and concentrations in a thin film using ion implanters. Not only can hydrogen atoms be inserted to modify a thin film, but in higher doses and implantation energies, it can be used to cleave slivers of silicon and sapphire wafers.

Carrier gas: Hydrogen is used as a carrier gas to entrain (entrap) and transport less volatile chemicals—ordinarily liquids at atmospheric pressure and room temperature—into the reaction chamber. The hydrogen is heated and bubbled through the liquid chemicals. Because the mass of hydrogen is very light compared to entrained chemical vapor, specialized mass flow controllers can then be used to sense, measure, and precisely control the amount of chemical vapor dispensed.

Deuterium defense against hot-carrier injection: Hydrogen bonds to silicon at thin-film interfaces are susceptible to breakage by hot carrier injection, which are electrons and holes caused by short-wavelength radiation like x-rays and gamma rays. In semiconductor structures, deuterium-passivated thin-films have different bond strengths, and a much lower probability of cleavage due to hot carriers.

This is particularly important for chips in critical applications and those in environments with high levels of short-wavelength radiation, like spacecraft. Like regular hydrogen annealing and passivation, deuterium is reacted with wafers in a pressurized furnace at high temperatures.

Material stabilization: The addition of hydrogen extends the shelf life of important electronic materials like diborane (B_2H_6) and digermane (Ge_2H_6), which otherwise slowly decompose. The slightly stronger bonds in deuterated stannane (SnD_4) allow it enough stability in a deuterium balance to be useful; the normal isotope version of stannane (SnH_4) decomposes too quickly to have commercial applications.

Application for EUV

Extreme ultraviolet (EUV) lithography is the much-anticipated new application expected to simplify the process patterning complexity for critical dimensions in leading-edge devices. While it has taken a long time for this technology to come close to commercialization, top-tier manufacturers are coalescing their predictions for volume manufacturing adoption in the 2018-2020 window. Whereas other hydrogen-consuming applications have a usage rate of 100s of sccm, EUV will require much larger flows of 100s of slm (standard liters per minute), or roughly 100 to 1000x more per individual tool.

Deep ultraviolet (DUV) lithography, the current workhorse of the patterning tools, uses an electrical discharge in neon or krypton mixed with halogen gases like fluorine to produce UV light at 193 nm and 248 nm; EUV light production is much more complicated. Tin metal is heated above its melting

Package	Volume [m^3]
Cylinder	7
Compressed gas trailer	10,000
Liquid trailer	40,000

point of 232°C, and small droplets of tin (~25 μm diameter) are rapidly (50,000 droplets per second) produced. These droplets are first vaporized and then excited with high-power CO_2 lasers. The excited tin atoms emit EUV light at 13.5 nm, which is more than 14 times shorter than the DUV tools.

The light is emitted in all directions and is collected and collimated (aligned) by an array of mirrors. The light is then passed to the primary lithography tool for focusing and image transfer before illuminating the photoresist on the wafer. All materials heavily absorb EUV light. Absorption losses are minimized by using multi-layer reflective optics instead of the transmissive lenses used in DUV lithography, and the entire light source and patterning systems are housed in vacuum chambers. These highly complex tools are expected to cost end users around $100 million USD each, and when fully adopted, a leading-edge fab could require 20 or more of these tools.

Scattered tin debris from the vaporization of droplets is a major potential source of contamination of both the collector and focusing optics. Unmitigated, the lifetimes of these expensive components would be unacceptable. Hydrogen gas is used to shroud the tin excitation region, and tin vapor and aberrant droplets are reacted to form stannane (SnH_4), which is then removed from that section of the housing by means of the vacuum line. Higher flows of hydrogen can be used in periodic plasma-based cleaning to remove tin that deposits on the collector optics.

Demand and supply

Even before the adoption of EUV technology, leading-edge logic and foundry processes have begun consuming several normal cubic meters (1000 liters) of hydrogen per wafer processed. This usage trend is expected to continue increasing in the 10 nm and 7 nm nodes commercialized before widespread EUV use. Consequently, major fabs now use hundreds of Nm^3 per hour. EUV, when fully extended to all of the critical layers, will roughly double the amount of hydrogen used in these fabs. In a related application, the largest LED fabs also use hundreds of Nm^3 of hydrogen per hour, primarily as a carrier gas and diluent for the gallium, arsine, and phosphorus precursors used to make the light-emitting devices.

Supply of hydrogen to electronics customers has historically been driven by regional source types, engineering and transportation codes, and by end user preferences and process qualification. However, steep demand curves are causing users to consider new supply schemes for access to larger volumes,

Supply of hydrogen to electronics customers has historically been driven by regional source types, engineering and transportation codes, and by end user preferences and process qualification. However, steep demand curves are causing users to consider new supply schemes for access to larger volumes, greater supply chain security, and lessening of local fab logistics

Compressed gaseous hydrogen (CGH_2)

Economical transport for short to medium distances

Liquid hydrogen (LH_2)

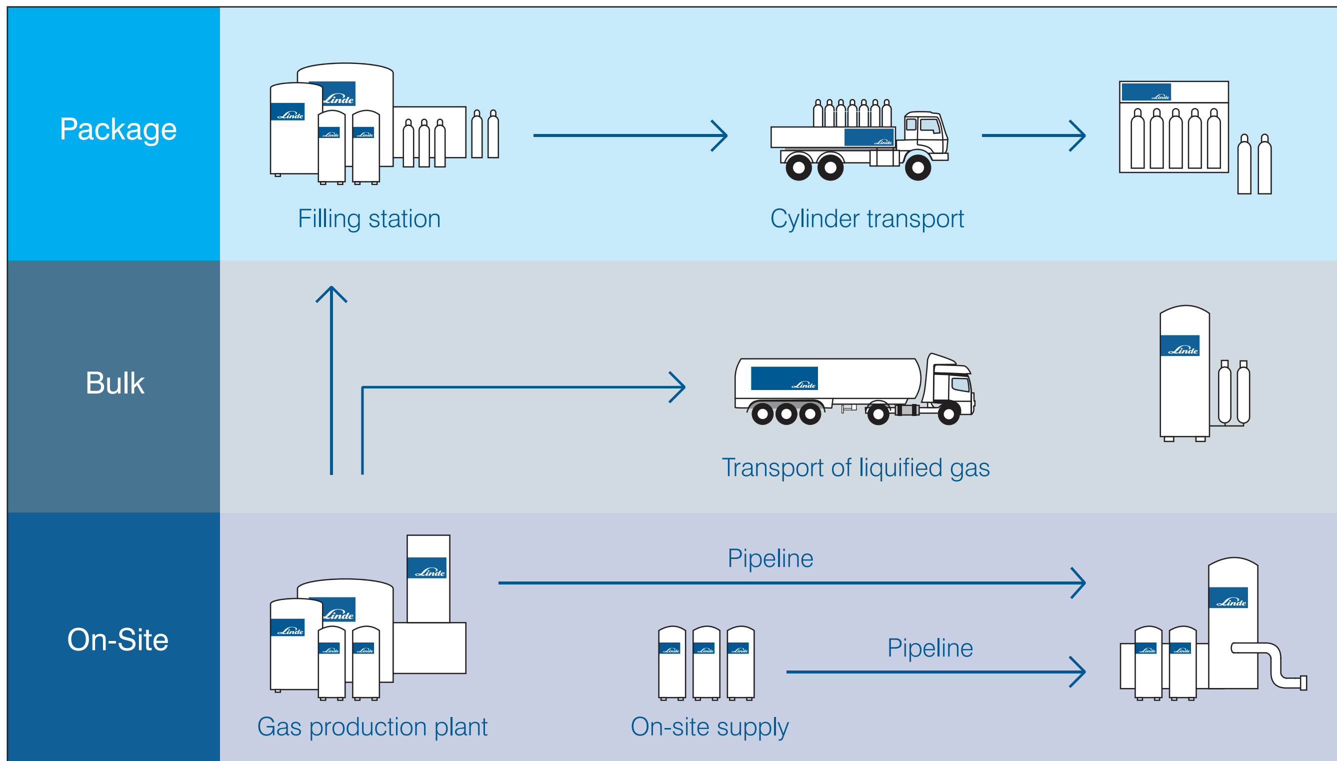
Economical transport for medium to long distances

(only in U.S. and Europe)

On-site production

Production through steam reforming or electrolysis

No hydrogen transport costs



greater supply chain security, and lessening of local fab logistics.

Over 60 million metric tons of hydrogen are produced globally, almost exclusively from hydrocarbon feedstocks: natural gas, oil, and coal. Most of this is used as a chemical intermediate to make ammonia, methanol, and transportation fuels. Electronics manufacturing consumes much less than 1% of global hydrogen production.

Hydrogen is supplied in the following modes:

Cylinders: In smaller volumes, hydrogen is supplied in standard-sized gas cylinders, which hold about 7 m³ of gas pressurized at approximately 175 bar (250 cu ft at 2,500 psi). The largest fabs now consume this amount in less than one minute. Individual cylinders can be manifolded together to create larger packs of cylinders, which are typically mounted into metal pallets for easier handling. These packs can even be arrayed into full truck trailers of connected cylinders. Despite the increased volume, there is a limitation on the level of mass flow that can be safely achieved from this configuration.

Compressed gaseous hydrogen (CGH) trailers: To improve on both mass distribution and packaging/handling costs, specialized trailers with much larger, pressurizable vessels are used. These CGH (compressed gaseous hydrogen) trailers can hold 10,000 Nm³ at pressures similar to smaller packages, yet are the distribution equivalent to over 1,400 individual cylinders. Just as importantly, fewer, larger vessels are faster to fill, and easier to maintain quality to the very high standards required by the semiconductor industry. Fewer components and human interactions also reduce safety risks.

Liquified hydrogen transport: In North America and much of Europe, liquefied hydrogen transport is allowed. This further increases the amount of hydrogen per truck to 40,000 Nm³ gas, or the equivalent of around 6,000 cylinders. In addition to increasing the volume, liquefication of hydrogen is also an added purification step. By cooling the material down to the boiling point of 21 K (-252°C), most impurities are solidified and can be reduced in concentration by absorption.

These benefits come with a trade-off, however. Liquefying hydrogen to the very low required temperatures consumes a lot of energy, and mandates additional safety protocols. Moreover, there are fewer liquid hydrogen production sources versus gaseous facilities, and transportation distances and supply logistics can be substantially increased. It is important to note that liquid hydrogen transport is not allowed in the primary semiconductor producing countries of Asia (China, Japan, Singapore, South Korea, and Taiwan), and therefore not a consideration for users in that region.

On-site hydrogen production: A solution that is becoming appropriate for some fabs is on-site hydrogen production. All major fabs already have either direct on-site production of gaseous nitrogen, or are supplied via pipeline by local plants. On-site hydrogen production has similar considerations of footprint, redundancy, and back-up.

On-site hydrogen technologies suitable for semiconductor processes are either electrolysis of water or so-called “shifting” or “cracking” of hydrocarbon feedstocks. Electrolysis is relatively expensive at volume because of the energy needed to break water molecule bonds even though achieving purity in the feedstock water is relatively simple. More economical are hydrocarbon feedstocks like natural gas, LPG (liquefied petroleum gas – mostly propane and butane), and methanol. Choices for the exact plant technology depend upon the local feedstocks available and the customer quality profile requirements.

Regardless of whether the hydrogen is supplied in gaseous or liquefied containers or made on-site, semiconductor hydrogen supply schemes incorporate on-site, and often additional point-of-use, purification using various technologies: adsorption, gettering, and application of the unique property of hydrogen to diffuse through palladium metal membranes, which are impervious to most other molecules.

In addition, hydrogen purity is monitored at several points in the distribution by multiple types of detectors. Deuterium, an isotope of hydrogen, increasingly is being used as chips are put into critical applications, and device dimensions are reduced to the atomic scale where one misplaced atom can result in chip failure. Because it is used in smaller amounts and is a very high cost material, deuterium is only packaged in individual cylinders.

Deuterium is produced by electrolysis of heavy water (D_2O), which is then further dried and purified before being compressed and packaged. Heavy water is produced primarily as a reaction moderator of certain uranium-based nuclear reactors. For higher flow applications, it can be feasible to recover deuterium from the waste stream and reprocess it off-site.

Safety

As with all chemical supplies, safety is paramount. With hydrogen, the main safety risk is associated with its wide range of flammability and explosivity. Throughout production and packaging, multiple types of redundant protocols are used to ensure that no oxidizers are contacted or incorporated into the hydrogen and plant designs minimize the risk for leaks.

Specialized clothing resistant to fire and static is worn in some hydrogen producing and using environments. Materials of construction and component qualification are also important to guard against a phenomenon known as hydrogen embrittlement, where at elevated temperatures and/or pressures, hydrogen can permeate and weaken certain metals and alloys. Finally, liquefied hydrogen introduces the additional risk associated with cryogenic materials and the need to use insulating vessels and personal protection.

Conclusion

Semiconductor manufacturing has long used hydrogen in an essential and expanding portfolio of applications. The supply of hydrogen is already a bulk material scheme, with source, transport, and logistic considerations.

The adoption of EUV at leading-edge fabs in the next few years will accelerate the pace of hydrogen consumption, and drive the consideration of new supply schemes. End users should evaluate hydrogen supply options for future fabs as part of their advanced planning to ensure that their quality, supply, and process integrity requirements will be met.

© 2017 Angel Business Communications.
Permission required.

The Linde Group provides its customers with the most comprehensive package of hydrogen supply and technology. Linde manages a large and diverse portfolio of hydrogen producing and transport assets, supplying the semiconductor industry in Asia, Europe, and North America. Linde Kryotechnik pioneered hydrogen liquefaction, and has supplied over 1,000 cryogenic hydrogen plants globally. Linde Engineering is a leading technology partner for plant engineering and construction, including the production of hydrogen from multiple feedstocks designed into modular and automated on-site plants. Linde Gas is the world’s leading civilian producer and supplier of deuterium. Linde Electronics supplies hydrogen to its electronics customers as part of a material offering of over 100 gas and chemicals with the highest safety, quality, and reliability. Through collective management, Linde offers customers in worldwide locations access to hydrogen products when, where, and how they need them.

Wafer defects can't hide from Park Systems

Atomic Force Microscopy (AFM) leader Park Systems has simplified 300mm silicon wafer defect review by automating the process of obtaining high-resolution 3D images, making it faster and simpler than ever before.

SEMICONDUCTOR MANUFACTURERS have options for defect review once inspection tools have identified potential flaws on bare silicon wafers. While conventional AFM provides data-rich 3D images, the process is slow compared to 2D, SEM-based techniques. A new AFM process developed by Park Systems changes that equation like none other.

Park Systems (Suwon, Korea and Santa Clara, California, USA) is one of the leading pioneers of atomic force microscopy (AFM) for semiconductor manufacturers and researchers. The company's founder (Sang-Il Park, PhD) led early efforts to commercialize the technology after being an integral part of AFM's development team at Stanford University in the 1980s.

Park Systems made the extreme, high-resolution 3D imagery of AFM commercially practical, going on to develop products and software for surface roughness measurement in hard disk media that became an industry standard (the Park HDM series product family). Park's AFMs are also 'non-contact' review tools, which eliminates the possibility of tool tips accidentally touching surfaces and possibly damaging wafers under review.

While quality, data-rich images have been a hallmark of Park's AFMs from the beginning, this extreme quality came at the price of speed and simplicity. The company subsequently automated AFM scanning for disk media and has now brought a similar approach to reviewing defects of interest (DOI) on silicon wafers up to 300mm. Its hardware and software also support extreme ultraviolet (EUV) reticle photo masks, a critical step in creating future 450mm silicon wafers.

Finding silicon wafer DOIs is challenging. All bare silicon wafers have a unique crystalline structure that is prone to small defects (Figure 1)that may be one nanometer or smaller. Manufacturers determine threshold sizes of interest along with shape and

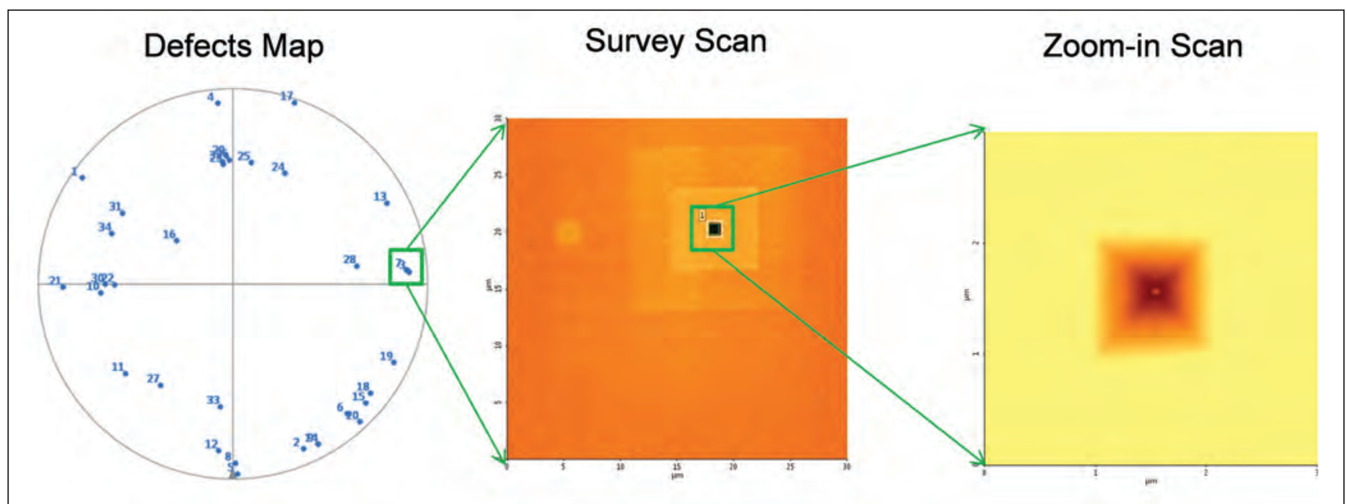


Figure 1: After coordinate mapping, ADR AFM will automatically perform a survey scan, zoom-in, processing, analysis and classification of each defect.

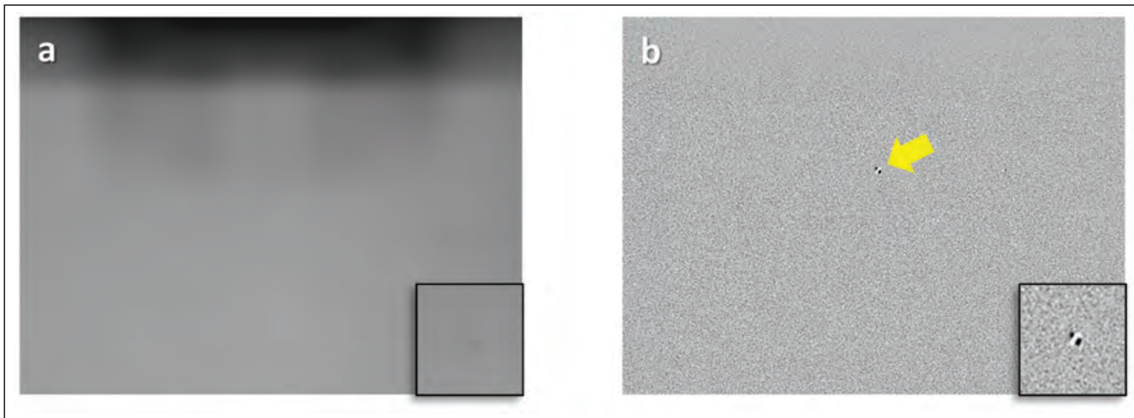


Figure 2: Images collected via (a) standard vs. (b) enhanced vision of a bare silicon wafer with one small defect. The insets show magnified views. The small defect is easily observable in enhanced vision.

depth characteristics that need attention. But while thresholds vary by manufacturer, it is clear that shrinking device geometries will impact whether defects once considered too tiny for concern could present problems for next-generation devices. There are a variety of laser light scattering techniques and process tools for inspecting wafers quickly, scanning hundreds or even thousands per hour. But inspection is just the beginning. A follow-up review by scanning electron microscope (SEM) or AFM takes inspection coordinates and zeros in on each location to image the defects. While SEM review is relatively quick, it cannot reveal much detail beyond a 2D image: a defect's 'X' and 'Y' dimensions. AFM goes much farther, creating X, Y and Z 3D images along with detailed topographic maps that further help identify and characterize an imaged DOI. AFM reveals defect details that SEM can routinely miss.

Park's AFM defect review is highly accurate, which is a key ingredient for success in an industry that measures in microns and nanometers. The accuracy of their AFMs is so great that the company holds a roughly 90 percent share of the market for hard disk drive defect review systems.

"Whether the defect is on a silicon wafer or the surface of hard drive media, the key is how accurately the review device locates it and delivers the information needed for proper defect classification. SEM may give

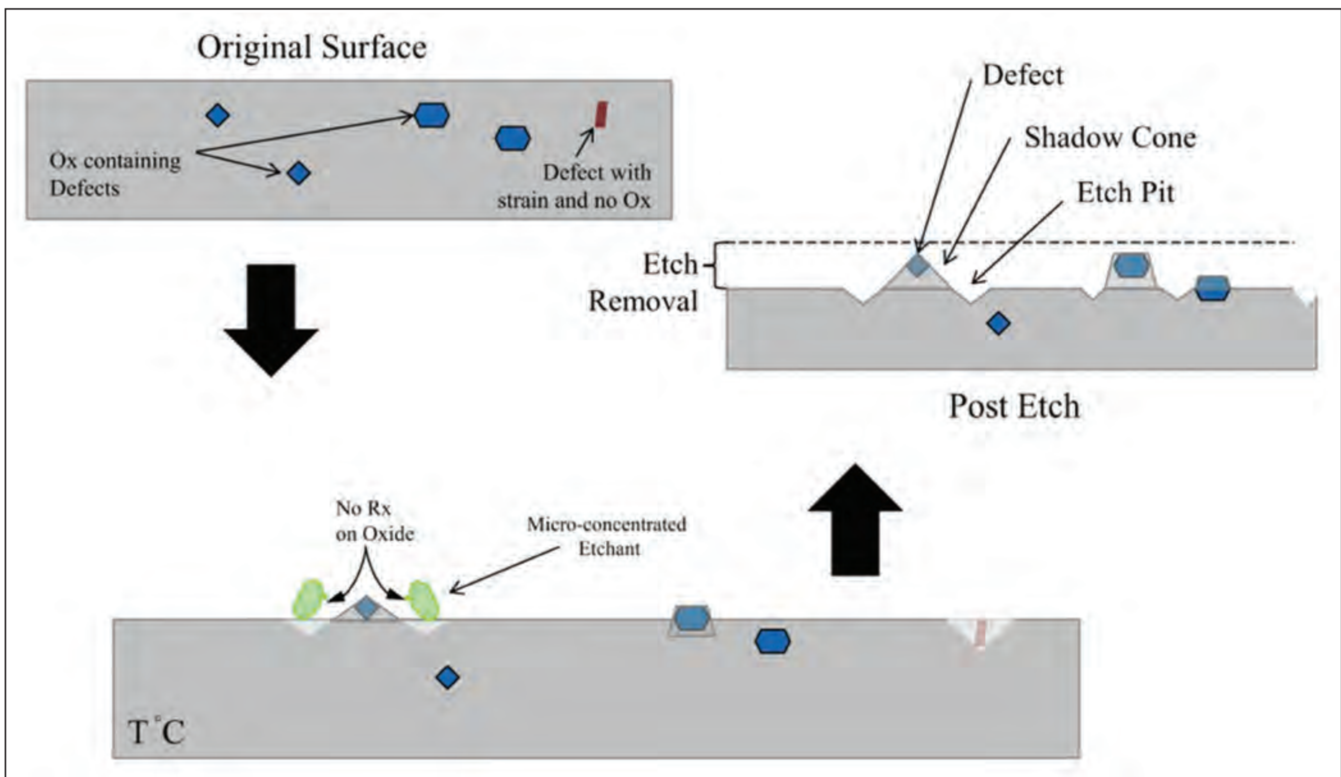
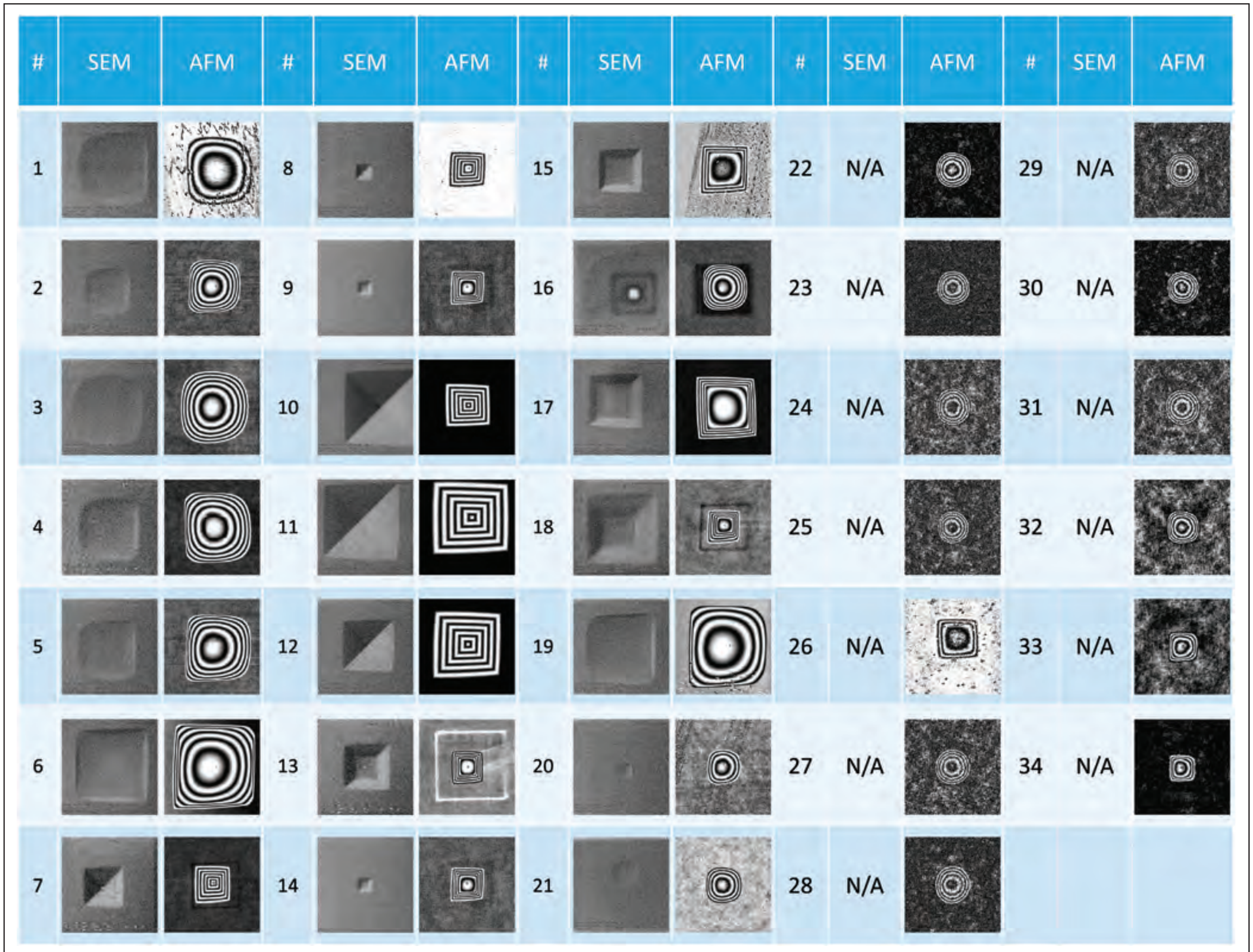


Figure 3: Schematic of the process used to decorate crystal imperfections for defect inspection.



#	SEM	AFM	#	SEM	AFM	#	SEM	AFM	#	SEM	AFM	#	SEM	AFM
1			8			15			22	N/A		29	N/A	
2			9			16			23	N/A		30	N/A	
3			10			17			24	N/A		31	N/A	
4			11			18			25	N/A		32	N/A	
5			12			19			26	N/A		33	N/A	
6			13			20			27	N/A		34	N/A	
7			14			21			28	N/A				

Figure 4: Defect review results with ADR AFM vs. SEM are shown. ADR AFM was able to locate and image all defects; SEM did not find defects 22 to 34. AFM and SEM images are rotated 180 degrees with respect to each other.

a quick image, but it lacks the information that can be provided by AFM (see figure 4).

"As a reference tool, AFM is the 'go-to' technology. Other AFMs can be a challenge to operate, so Park Systems addresses the problem with ADR: automatic defect review. We automated defect review and simplified it, so any technician can start the review process, and then simply walk away to do other tasks while the ADR AFM is operating," said Ardavan Zandiatashbar, PhD, Park's senior applications scientist.

While different manufacturers have varying approaches to how they handle silicon wafer defects, all likely agree that better data about a particular defect determines whether it is serious enough to affect lithographic processing, or whether defects are so great in number and size that a wafer should be rejected outright.

"We started with hard drive media defect review. Manufacturers needed to know the source of defects for failure analysis purposes. While SEM can give a quick image, its image can't easily tell you if a defect is a pit or a bump or how tall or how deep it is. This is where AFM comes in; it helps you to identify and classify defects accurately and completely. We do what others cannot do," Zandiatashbar said.

Wafer defects in Park's study typically fall into eight basic categories—additional categories in different wafer surface reviews are possible. Some defects can't be classified at the inspection stage and may not fit into a typical category even after AFM review. But through AFM, the manufacturer will definitely know a defect's size and depth; they can apply their own standards to determine what actions should be taken.

"Many manufacturers want to use AFM routinely, but locating the defects and linking the AFM to inspection tools were critical issues previously. Results from conventional AFMs depend on the skill of the operator. We eliminated those issues by automating the process. Now, instead of reviewing just a few defects per day through laborious efforts and changing

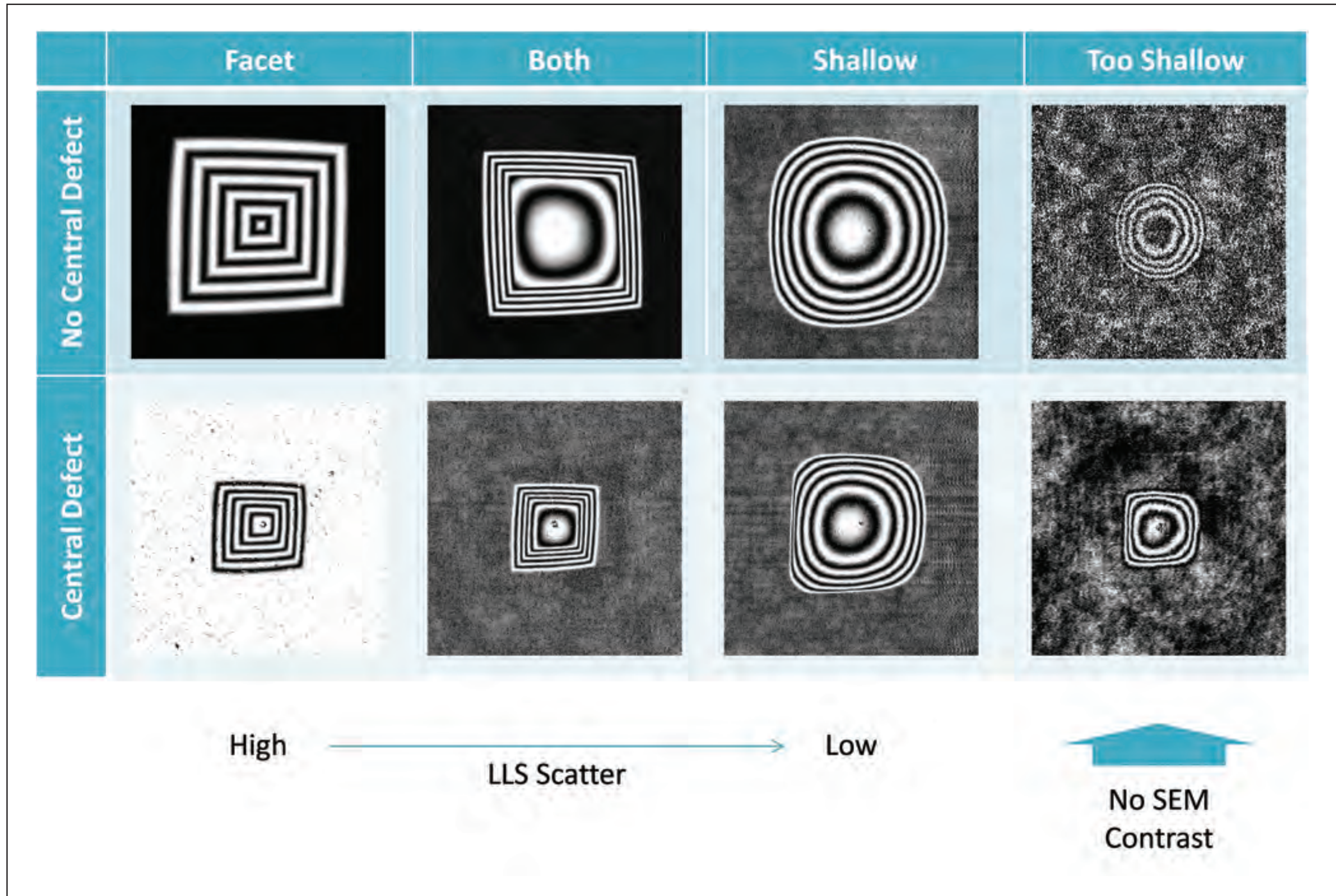


Figure 5: Defect classification based on the AFM data.

numerous tool tips, Park's ADR AFM can image and fully characterize between four and 10 defects per hour. A technician can start ADR and let it run 24/7. Manual AFM review proceeds only as quickly as a skilled operator can function," he added. "Park's ADR AFM is a turn-key solution."

In addition to automating the review process, Park's non-contact approach to AFM does not alter the wafer's surface in any way, meaning every wafer reviewed can go onto further processing as needed. SEM-based review processes have another issue beyond quality of data. Their electron beams also have the potential to 'burn' scan areas (see figure 6). This effect is typically more critical for photo-resist layers, but any disruption of a wafer's surface area can affect yield or other important factors.

The differences in results obtained using Park Systems ADR AFM compared to SEM-based results are dramatic. In a test conducted by Park, a wafer containing surface defects was reviewed using both SEM and AFM-based techniques. The ADR AFM utilized was from Park's NX-WAFER family of products. 34 defects identified at the inspection stage were candidates for review. The first 21 defects were imaged by SEM, which delivered aerial, 2D views without sufficient information about the depth or out-of-plane dimensions. The remaining 13 defects were not found by SEM despite identification during a laser light scattering (LLS) inspection (see figure 4).

Park's ADR AFM was able to find all 34 defects. The SEM had found defects down to a certain size threshold; those imaged by ADR AFM were typically

The differences in results obtained using Park Systems ADR AFM compared to SEM-based results are dramatic. In a test conducted by Park, a wafer containing surface defects was reviewed using both SEM and AFM-based techniques. The ADR AFM utilized was from Park's NX-WAFER family of products. 34 defects identified at the inspection stage were candidates for review.

Cursor	ΔX(µm)	ΔY(nm)	Angle(deg)
Red	2.355	-23.962	-0.583
Green	3.293	0.230	0.004
Blue	0.105	13.672	7.386

Figure 6: Comparison of data collected by SEM vs. ADR AFM. SEM shows a 2D, aerial view, while ADR AFM includes 3D data, thereby enabling a line profile, 3D construct and contoured colour scale.

smaller or shallower than defects that the SEM could identify. The SEM also had issues identifying defects that had less edge sharpness, whereas the AFM in its automated scanning mode found everything (see figure 6) .

"From the customer perspective, locating the defects of interest during the review process and determining size and depth can be critical. While SEM-based techniques can locate larger defects, it does not find them all and in fact missed 13 of 34 in this case. The lack of 3D information and SEM's inability to image the shallow and small defects matters to manufacturers. With Park's automatic defect review manufactures can have high quality 3D data of DOIs more quickly using a turn-key solution that any technician can operate," said Zandiatashbar. Automatic defect review from Park Systems maximizes productivity by up to 1,000 percent as reported by customers. But what satisfies customers most is the unprecedented level of accuracy including 3D imagery and detailed topographic information of even the smallest defects. With ever-shrinking semiconductor device geometries reaching beyond 14nm, defects critically impact microelectronic device performance. Park's approach to automating 3D imaging is revolutionary because it makes the benefits of AFM practical for leading device manufacturers and researchers pushing future product generation boundaries.

© 2016 Angel Business Communications.
Permission required.

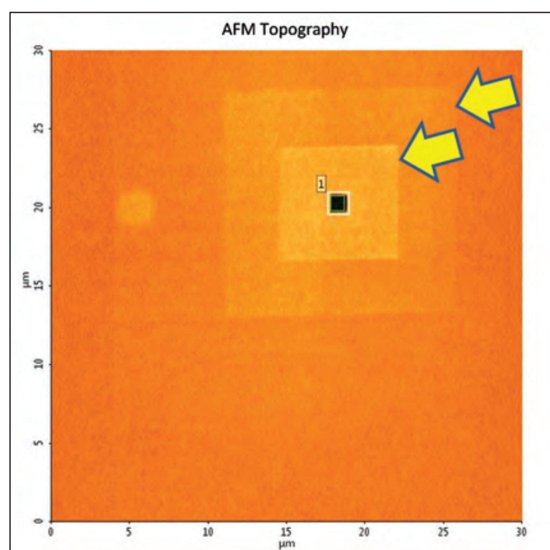


Figure 7: AFM image of a facet defect with several SEM burn-marks is shown; burns are marked by arrows.

NEW VAT BUTTERFLY
ULTRA-FAST ACTUATION IN A TENTH OF A SECOND – HIGH THROUGHPUT

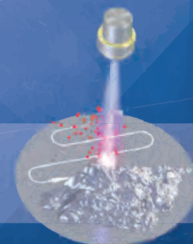
- Position only control version – ideal for simple throttling applications
- Sealing and non-sealing type
- Heater options

www.vatvalve.com

HIGH-END EQUIPMENT
FOR HIGH-TECH INDUSTRIES

IonScan
Systems for ultra-precise film thickness trimming and ion beam figuring

- Contactless trimming or figuring
- Optimization of error distributions by the factor of 10 and more
- Ion beam process applicable to almost all materials

Ion Beam Technology


Visit us at SEMICON Europa
November 14-17, 2017 in Munich/GER
Booth B1-1815

www.meyerburger.com

WET BATCHSPRAY POWER DEVICE MANUFACTURING

As history tells us, before a solution can be found, a problem must first arise that needs to be solved. The history of Siconnex began when a power device manufacturer was faced with this challenge and since then many new applications and solutions have been enabled throughout the semiconductor industry, including power, LED, analog/ mixed signal, MEMS, and many more.

Optimization of a standard power process: Al(Si) – freckle or Ti/TiN etch and resist strip

One of the most common processes within the power industry is Al etch followed by barrier or freckle etch and resist strip. This process sequence opened up the door to success for Siconnex at a European customer's site 12 years ago. The main issue faced by the customer was that this process sequence requires a large number of different wet benches full of chemicals, which at that time were mainly manually operated. This procedure involved wasting huge amounts of cleanroom space, exhaust gas, chemicals, and operator time. In addition, the result was barely sufficient in terms of particles and uniformity.

In standard production conditions, nobody wants to change an existing process or system. It's good to maintain a healthy scepticism when it comes to amending processes, but the possibility for improvement will eventually be exhausted. In this case, it was the sheer number of factors which were far from the optimum level that led to the decision being made to change the process.

At this stage, Siconnex introduced the Siconnex BATCHSPRAY technology. The system used was equipped with three chemical tanks and the option of using ozone in the process. With the Siconnex BATCHSPRAY solution, all the chemicals, water, ozone, and other gases are channelled to a process chamber, where they are sprayed onto a rotating batch or batches of wafers.

This principle enhances chemical exchange significantly. Furthermore, drying can also be performed inline in the process chamber.
With this solution, the customer combined the whole process sequence into one system with a 2.2 m^2 footprint and on a dry in–dry out basis.

As a further benefit, uniformity dropped to below 2 percent as a result of the high chemical exchange. This was achieved for "within wafer," "wafer to wafer," and even "batch to batch" uniformity thanks to the in-situ, automated end point detection system.

Throughput saw a significant improvement too once the whole sequence was processed without interruption and intermediate drying. With operators not having to carry the wafers from one wet bench to another, the throughput was more than doubled.
One of the most important benefits was the use of ozone, which made it possible to replace the solvent chemical entirely. This is a huge benefit in terms of cost, since only O_2 is needed to generate O_3.

Additionally, this is an advantage for the operators. Since most solvents are hazardous chemicals and replacing them with what is basically air leads to a much better working environment.

"The use of ozone made it possible to replace the solvent chemical entirely." When all the benefits of this optimized process technology are summarized together, the real cost-saving potential is revealed:

- Combination of four processes:
- Al etch
- Freckle etch
- Ti/TiN etch
- Resist strip

(up to five processes are possible in total)

- Simultaneous processing of 50 wafers
- Average process: 45 min
- Average throughput: 67 wph
- Uniformity: <2 percent
- No solvent required
- Dry-to-dry process

Taking all of this into account, the typical time for return on investment (ROI) is close to one year, depending on the existing process.

This process with the Siconnex BATCHSPRAY technology has been implemented at 16 plants around the world and continues to be in high demand among existing and new customers alike even after 12 years.

State-of-the-art technology, processing of SiC, and GaN for high-end technology

One of the changing factors within the power device industry is the wafer material used. For high frequency, high power, high temperature, or low leakage current, compound semiconductor substrates are used to ensure that the increasing requirements are met. The two materials most commonly in use at the moment are SiC and GaN.

For these materials, Siconnex has developed, and is still developing, processes so as to put itself in a position to provide state-of-the-art equipment. The focus of these investigations is to provide cleaning technologies for new materials, as well as the possibility to perform uniform etching.

300 mm Semiconductor Manufacturing

Although the current power market is focused predominantly on 200 mm or below, Siconnex is already one step ahead, providing its BATCHSPRAY platform–fully automated and ready for full integration in state-of-the-art 300 mm fabrication plants–for all semiconductor sectors.

In this case, two BATCHSPRAY process chambers share one robot. Each chamber is able to process 25 wafers with a diameter of 300 mm simultaneously. The results for 300 mm wafers are the same as or even better than the results achieved for 200 mm,

meaning that uniformity values below 2 percent are standard. The Siconnex BATCHSPRAY system is the method of choice for high-volume, low-cost production.

Future challenges

Siconnex is looking forward as technology progresses, seeing every challenge as a possibility to provide the ideal solution. A future step within the power sector is going to be keeping an eye on the evolution of emerging materials like AlN, diamond or Ga_2O_3 and developing the solutions the industry needs.

Besides the power sector, Siconnex also provides solutions for markets such as LED, MEMS, analog/mixed signal, and many more. Our goal is to replace wet benches with the Siconnex BATCHSPRAY technology to help our customers save resources and money, while also achieving better process results. For this reason, Siconnex is constantly looking into new applications within existing and new markets. In the Siconnex laboratory, new processes are developed and existing processes continually optimized.

The Siconnex equipment development team works closely with the process team to guarantee that the rising demands placed on Siconnex systems are fulfilled and that our systems are at the cutting edge of technology.

© 2017 Angel Business Communications. Permission required.

> “Besides the power sector, Siconnex also provides solutions for markets such as LED, MEMS, analog/mixed signal, and many more. Our goal is to replace wet benches with the Siconnex BATCHSPRAY technology to help our customers save resources and money, while also achieving better process results”

Angel
BUSINESS COMMUNICATIONS

THiNK
OUTSiDE
THE BOX

WE'VE BUILT AN APP FOR THAT.

Many companies are now thinking of offering their customers and potential customers an app.

Angel Online are one of the UK's leading app development companies providing both iPhone and Android app development. We have specialist industry knowledge of vertical B2B markets. We can help you build an app for your sales, marketing or internal communications purposes.

Visit **www.angelbc.com/online** to think outside the box.
E: sukhi.bhadal@angelbc.com **T:** +44 (0)24 76718970

- WEBSITE DEVELOPMENT
- MARKETING AND SEO
- EMAIL MARKETING
- ONLINE MARKETING
- APP DEVELOPMENT
- WEBCASTS

PLASMA DICING

Strength in numbers

The demand for smaller electronic products including burgeoning IoT applications has led to new focus on die size and wafer singulation. Richard Barnett, Etch Product Manager at SPTS Technologies explains how the benefits of plasma dicing grow as die continue to shrink.

WITH THE ever-constant evolution of new technologies for mobile applications now extending to even smaller "wearables", the need to make device packages even smaller, thinner, faster and power efficient shows no signs of abating. We, the consumer, are fuelling this with our expectations; that mobile and wearable devices survive lifestyle activities; that medical/automotive/smart-home sensors function for as long as is needed, etc.

One parameter above all others coming to the fore as a consequence of device shrink and performance expectations is die strength, which is something that plasma dicing has the capability to improve significantly.

Conventional blade and laser dicing will still be a cost-effective method to singulate die in some cases; however, there are a growing number of applications where plasma dicing can offer economic and die quality benefits when compared to conventional techniques. In some cases, namely for smaller and thinner die, plasma dicing enables singulation which is virtually impossible with the other methods. Plasma dicing before grind (DBG) has been used in selected applications for a number of years, but plasma dicing after grind (DAG) is at the early stages of adoption for volume production. The trend toward thinner, smaller die, along with the in-service reliability demands, distinguishes plasma dicing as an increasingly attractive alternative.[1]

Silicon plasma dicing uses Deep Reactive Ion Etch (DRIE) technology, more typically referred to as the "Bosch" process. This is a well-established production technology, used in silicon MEMS micromachining and via etching in 3D packaging. DRIE is now adding dicing technology in the "back-end" of semiconductor processing to its portfolio of production applications. Like any other dry step in the device process flow, integration is key, and these challenges are the only gate to the use of plasma as a singulation method. These considerations are not only related to wafer layout and preparation, but also accommodating the standard back-end frames and tape combinations. The objective is that the process flow not be disrupted to the point where it becomes a hindrance to the adoption of a technology that offers so many potential benefits.

Benefits of plasma dicing

No Damage = Stronger Die / Higher Yield

In mechanical dicing, (especially for small die or thin wafers when using high feed speeds), the risk of chipping at the edge of the die is an issue. In laser dicing heat damage has to be accounted for, which becomes a more significant threat for smaller/thinner die. As a chemical process, plasma dicing eliminates all of the damage caused by the other mechanical methods, e.g. crack initiation, thermal damage, edge chipping, and vibrations. Plasma can also remove the need for fluids used to cool blades and remove debris. The Bosch process, which is made up of alternating etch and passivation steps, creates characteristic "scallops" on the sidewalls of the die (see Fig 1), with each scallop representing a single etch-passivation cycle. They are generally <3μm in depth and as they are the result of a chemical etch do not cause crack initiation nor act as stress raisers. In plasma dicing the wafers are held electrostatically on a chuck with active cooling to maintain a low wafer and tape temperature, which are important for maintaining tape integrity for the subsequent expansion and pick-and-place steps. Plasma dicing is also attractive for fragile devices

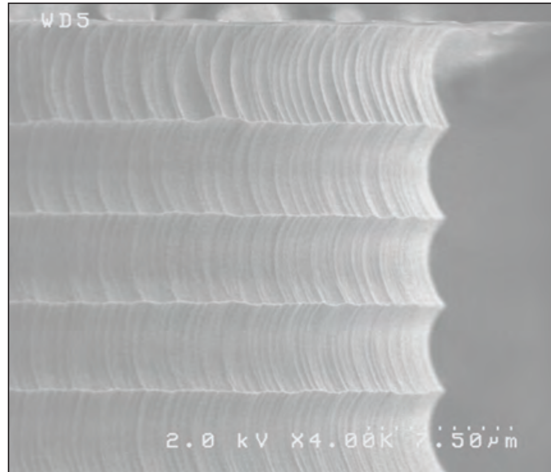


Fig 1 Characteristic DRIE scallops cause no crack initiation

such as MEMS, with movable structures and thin membranes, as there are no physical forces to vibrate the wafer and damage the devices.

Increased die counts

When using a conventional dicing method, the lane width is determined not just by the width of the saw blade or laser spot, but also by the placement and accuracy for test pads and damage limitation. Considering plasma, lanes are not restricted in the same way and can be made much narrower, freeing up valuable silicon real estate for more die per wafer. For smaller die, like RFID chips (at~0.04mm²), this saved real-estate can give a potential increase of 80% more die per wafer. With plasma dicing eliminating the risk of crack initiation at the die edge, any "crack stop areas" can be eliminated from the die layout freeing up yet more space for active die. (There still needs to be a motivation by the user to move test structures out

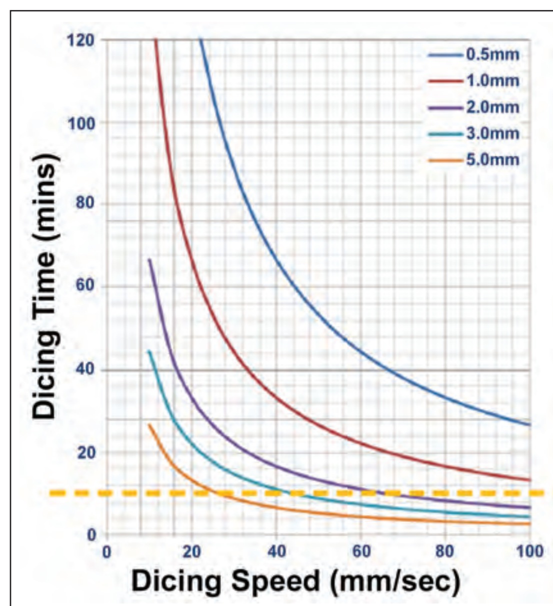


Fig 2: Curves showing how blade and laser increase cycle time as die size reduces. Plasma dicing (orange dashed line) has constant dicing "rate" regardless of die size.

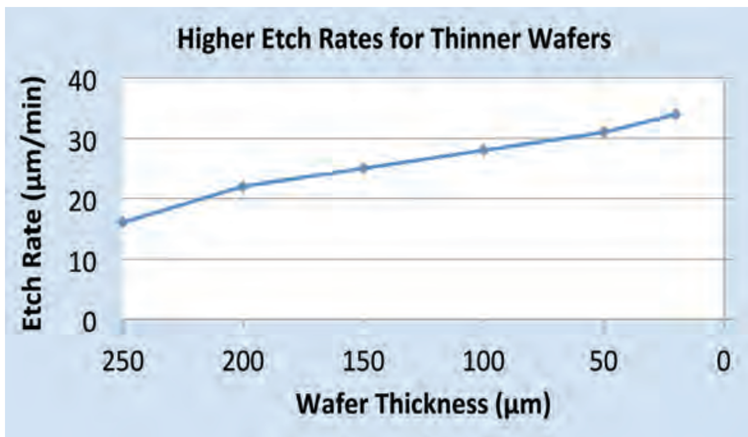


Fig 3 Effect of wafer thickness on silicon etch rate

from lanes to achieve full realisation of benefits.) As well as reducing lane width, plasma dicing can also increase die per wafer because the wafer layout is not constrained by the need to have orthogonal dicing paths. Plasma dicing gives device designers much greater flexibility with regard to fundamental die shape and size, removing guard rings and positioning test groups to make best use of the available wafer area.

Increased throughputs for smaller, thinner die

As die sizes shrink, allowing more die to be patterned onto wafers, the number of dicing lanes increases. For serial methods such as laser or saw, the consequence is a significantly reduced throughput as the number of cutting passes grows as the die size reduces (see Fig 2). Plasma dicing is a parallel process, with all dicing lanes etched simultaneously. The throughput of plasma dicing is largely governed by the wafer thickness, or aspect ratio of the etch, and not by the number of dicing lanes or die per wafer.

Also, with the industry generally driven toward thinner die, mechanical sawing and laser dicing become more difficult. Further decreases in throughput occur as feed speeds are reduced to prevent damaging these fragile devices. Conversely for plasma dicing, thinner wafers are quicker to etch through because there is less silicon to remove, and etch rates are higher for thinner wafers (see Fig 3). Both these factors increase throughput, while still improving the physical integrity of the die.

Due to the front-end genesis of the plasma approach, cluster platforms are available capable of carrying multiple modules thereby giving an easy scaling from pilot to volume production.

Consistency = Increased throughput

Plasma dicing is a repeatable technique which will process wafer-after-wafer in exactly the same manner, unlike blade dicing that requires regular blade dressing (reducing throughput) to maintain a consistent blade shape and performance. Consistency reduces the need for inspection and further cements the yield and quality advantage for the plasma dicer.

Integration considerations

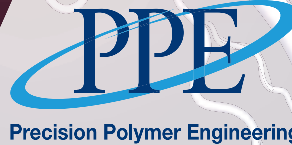
Designing in plasma dicing from the outset of a device lifecycle is the easiest way to realise all of the benefits that the technique can provide. However, in this article we present novel approaches which have already proven that plasma dicing can be immediately adopted into existing process flows.

The most common integration challenge facing plasma dicing is the potential range of materials that can be encountered in the dicing lane. Currently, plasma dicing is a silicon etch activity and as previously mentioned uses the Bosch process to achieve this in a process module designed as a silicon etcher. This means that any metals or dielectrics in the dicing lane cannot be etched without causing compromise to the substrate. To complete die singulation additional steps are required. Metal is the worst case scenario. Metal in the lanes can be “designed out” for new device layouts, but for existing products it may be necessary to remove the metal layers earlier in the process flow.

Alternatively, lasers or mechanical saws can be used to “pre-define” the dicing lanes. Using this method is more typically valid for larger die which will be less affected by the obvious throughput impediments of the definition step. Other methods for defining the dicing lane include standard photolithography, although the additional masking step to define the dicing lanes is sometimes viewed by some as a

As die sizes shrink, allowing more die to be patterned onto wafers, the number of dicing lanes increases. For serial methods such as laser or saw, the consequence is a significantly reduced throughput as the number of cutting passes grows as the die size reduces

Introducing two new Perlast® elastomer materials – offering the ultimate plasma resistance



EMEA: +44 1254 295 400
USA: +1 408 441 2043
ASIA: + 886 922 326108
www.prepol.com/plasma

A4 SERIES

Energy efficient dry multi-stage Roots process pumps for all semiconductor applications

- Low energy consumption
- Improved temperature management to optimize the pump according to your process
- Protection of the pump against precursor cracking or condensable deposition
- Corrosion resistant and high particle tolerance
- Extended monitoring functionalities

Are you looking for a perfect vacuum solution? Please contact us:
Pfeiffer Vacuum, Inc. · USA · T 800-248-8254 · F 603-578-6550 · contact@pfeiffer-vacuum.com
www.pfeiffer-vacuum.com

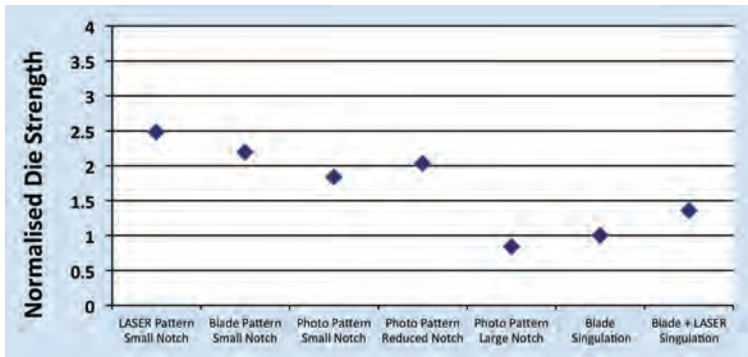


Fig 4 Effect of dicing method on die strength

hindrance to adoption. More easily adopted is the approach of using existing layers that are extended to allow for erosion of this material during plasma etching. This latter method can be described as maskless.

Test pads are a crucial part of back-end flow, and test probes need a certain size for testing. In conventional dicing schemes, the pads are often located in the relative large dicing streets and simply removed away by the dicing method. When plasma dicing is introduced, allowing the designer to reduce the lane widths, it leaves the question of where to put the test pads. Utilising the additional real estate from reducing the lane widths and combining with the flexibility of die shape/positioning it is fairly straightforward to move test pads elsewhere on wafer, or even adopt an "on-die" test pad scheme.

Tape choice is important. With proper process control most can be used, but some will behave better than others. The choice will depend on the subsequent steps e.g. if you have a backside metal, the DRIE will not etch this. As part of backside metal separation the metal must stick to the tape during pick and place, while the adhesive is able to release the die for easier picking. There are a variety of materials used for tapes and adhesives and when checking suitability for plasma dicing, the user must concentrate on the film material and the adhesive strength parameter. Both of these will give some early warning of potential problems during plasma dicing. Tape properties due to exposure to the plasma also need to be considered. Most tapes are non-conductive and will become positively charged during the plasma processing, which deflects negative ions within the plasma towards the silicon sidewall, creating a "notch" at the bottom of the etch feature near the tape. The same effect is observed in etching MEMS devices from silicon-on-insulator (SOI) wafers where the oxide becomes charged once exposed. Patented methods to combat this "notching" developed for the MEMS industry have now proved useful to optimise plasma dicing to a tape.

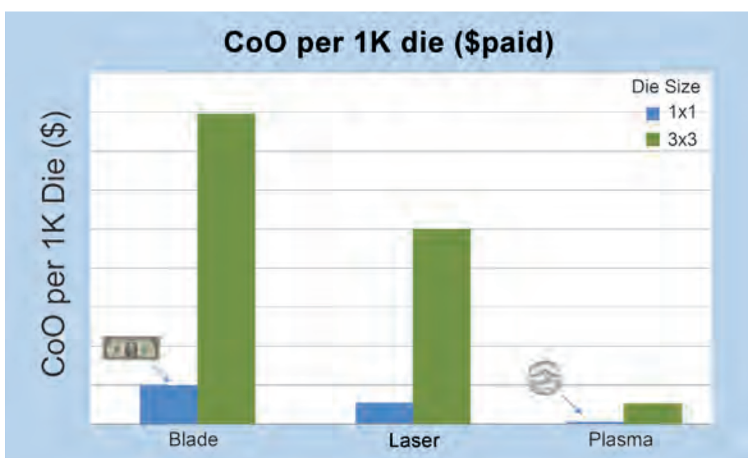


Fig 5: Cost of ownership comparison for blade vs. laser vs. plasma dicing for two different die sizes, (incorporating the possibility of a thinner wafer and narrower dicing lanes for plasma dicing.)

Die strength comparison

Recent work [2] has shown that plasma dicing typically doubles the strength of resulting die, even if integration with the existing process flow determines that the dicing lanes must be pre-defined by a blade or laser. Even with these combination methods, significant strength/yield increase can still be achieved. However, Fig 4 also emphasises the importance of plasma processing control, illustrating how plasma dicing, even defined by photolithography, can in fact reduce die strength if the process control is poor and a large notch is allowed to form at the tape interface. Plasma dicing can offer significant advantages over other dicing methods, but without good process control these benefits can be negated by undesirable damage to the die.

Plasma dicing eliminates all physical damage phenomena as seen with conventional methods. For plasma it is also important that notching at the Si-to-tape interface mentioned above is also tightly controlled. Two patented technologies, already well-established and proven in SOI MEMS manufacturing, can be employed to prevent damage to the silicon and the tape during plasma dicing. First, a proprietary end-pointing technology [3] can accurately monitor the progress of the etch front and manage a change in recipe conditions when the tape is exposed. Patented "bias pulsing" [4] can then be used during the final stage of die singulation to control the final stages of the etch, preventing any lateral under-etching of the die, or "notching." Fig 4 shows how the strength of plasma diced die with "small" or optimized "reduced" notching is typically twice that of a blade or blade/laser approach. However, plasma dicing with no control of the notching will severely compromise die strength.

Cost of ownership comparison

In some cases, where the die size is not particularly small, the relative throughput of laser dicing could appeal to prospective users, especially when the capital cost of a laser dicing system is generally less than a plasma etch system. However, careful consideration must be given to the ongoing cost of ownership when selecting the right solution for an application, as well as the trends in die size and

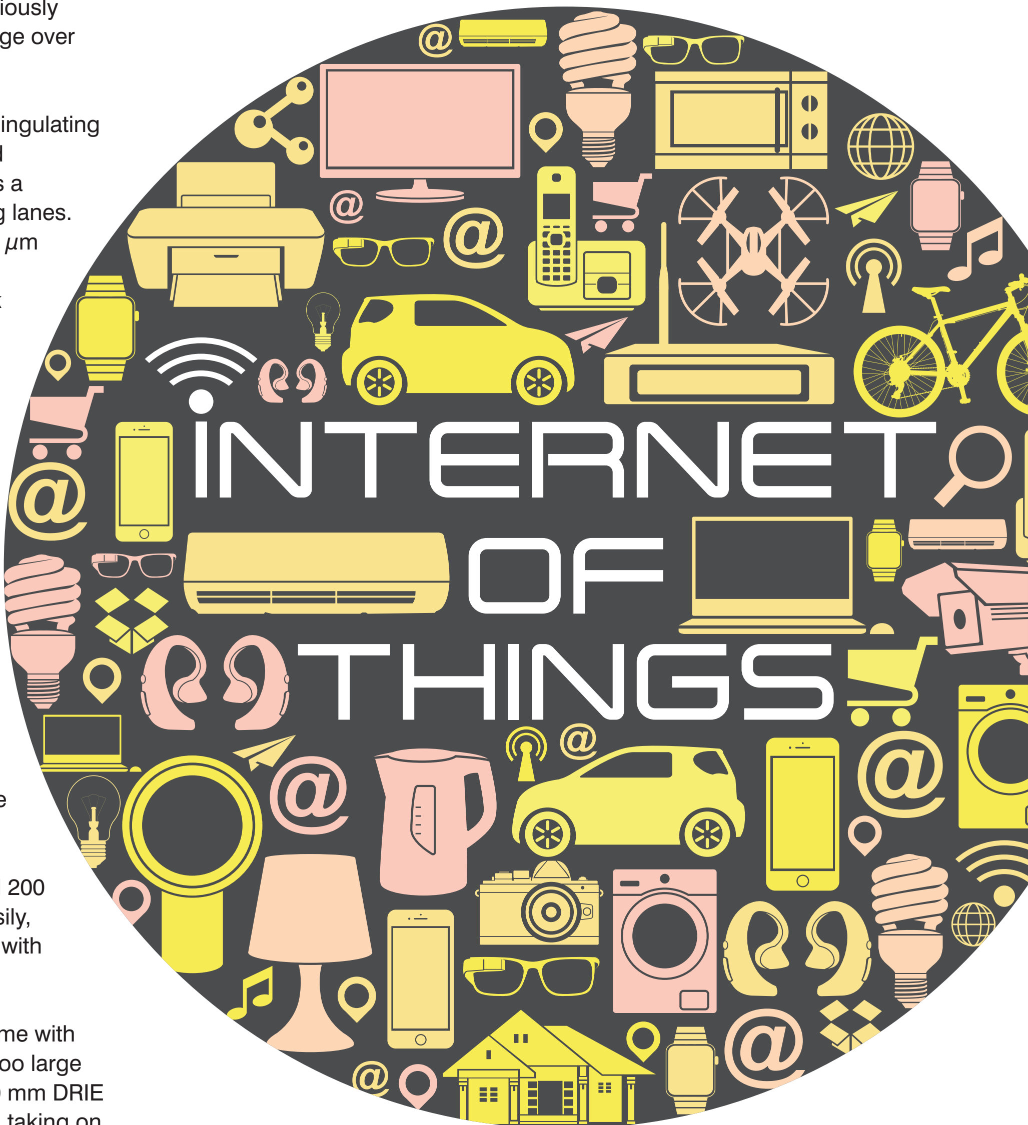
wafer thickness. When all the benefits of plasma are realised, combining all of the topics previously discussed, this reveals a major cost advantage over conventional methods.

In the Fig 5, we have compared the cost of singulating 1,000 die for two die sizes, 1 mm x1 mm and 3 mm x 3 mm. For the conventional methods a 100 μm thick wafer is used with 80 μm dicing lanes. For plasma dicing, the wafer is thinned to 50 μm with lanes reduced to 10 μm. When coupled with yield gains and ability to eliminate crack stop areas, it is easy to see that the plasma approach significantly reduces the cost contribution of the singulation step. For the 1 mm x 1 mm die, the blade singulation cost per 1000 die is 20 x that of the plasma dicing approach.

Dice after grind for 300 mm wafers

Plasma dicing after grind is typically carried out on thinned, ground wafers mounted on tape frames. Until recently DRIE sources were only available for processing silicon wafers up to, and including 300 mm in diameter. A 200 mm/8" wafer, on a standard tape frames with an external diameter of 296 mm, could therefore be accommodated within an existing 300 mm-compatible silicon etch plasma source. This enabled plasma dicing of taped 200 mm wafers to be demonstrated relatively easily, notwithstanding the other issues associated with etching to a tape, discussed above.

A 300 mm/12" wafer, however, requires a frame with an exterior diameter of 400 mm, which was too large to be handled and processed in existing 300 mm DRIE equipment, so a new system was developed taking on board all of the learning achieved on the original 200 mm DAG platform and process module. In 2016, SPTS released a new silicon etch source with a larger plasma chamber and automated wafer handling for this larger substrate size.



Summary

Despite many integration challenges, plasma dicing offers considerable benefits for die singulation, providing opportunities to achieve increased throughput and die count per silicon area as well as flexibility for die layout and design. Perhaps most important of all, plasma dicing provides improved die quality and strength. As such, plasma dicing is well positioned to become the benchmark technology for fabs seeking to increase die strength, throughputs and yields for small or thinned and fragile die on 150 mm, 200 mm or 300 mm wafers.

© 2017 Angel Business Communications.
Permission required.

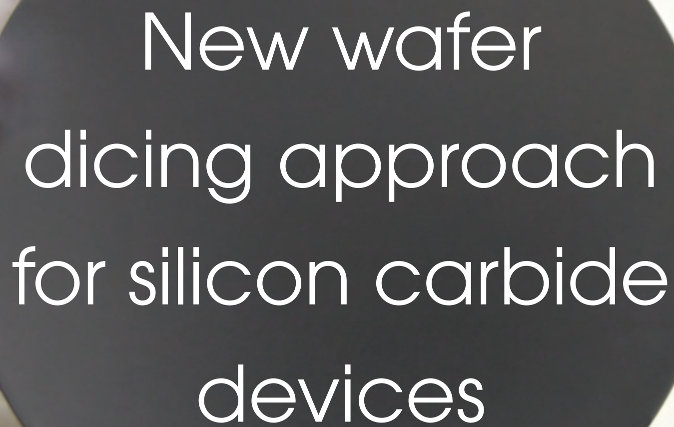
Further reading

[1] Thin Wafer Processing and Dicing Equipment Market report, Yole Développement, May 2016

[2] R. Barnett, D. Thomas, O. Ansell, J, Carpenter, W. Worster, G. Ragunathan "Improving Device Yields and Throughput using Plasma Dicing" presented at IWLPC2015

[3] US Patent No 9,159,599 – "Apparatus for chemically etching a workpiece"

[4] US Patent No: 6,187,685 - "Method and apparatus for etching a substrate"



New wafer dicing approach for silicon carbide devices

With the transition to new substrates like SiC, as well as thinner wafers, smaller feature sizes and larger-size substrates, wafer dicing has evolved into a critical process step that can enhance SiC device yields.

Explains Dr. Hans-Ulrich Zuehlke and Mandy Gebhardt, 3D-Micromac AG

AS A WIDE BANDGAP MATERIAL, silicon carbide (SiC) is considered a replacement material for silicon (Si)-based semiconductors in the electronics industry in certain applications due to its wide band gap, high mechanical strength, and high thermal conductivity. For example, SiC power devices can operate at higher voltages, frequencies and temperatures, as well as convert electric power at higher efficiency or lower power losses. At the same time, SiC is an extremely hard and brittle material (Mohs scale 9.2), which can create processing challenges. This is particularly true in back-end processing where wafers must be singulated into individual die prior to packaging.

Historically, wafer dicing has been treated as an after-thought in the overall semiconductor fabrication process—a necessary evil that adds little value to the overall process. However, with the transition to new substrates like SiC, as well as thinner wafers, smaller feature sizes and larger-size substrates, wafer dicing has evolved into a critical process step that can enhance SiC device yields.

3 EVENTS 2 DAYS 1 TICKET

10-11 April 2018

Sheraton Brussels Airport Hotel, Belgium

One ticket gives you access to a 2 day event which will see 3 groups of device makers gathered under one roof.

Hear over 90 presentations covering the entire spectrum of the compound semiconductor, integrated photonics and high-end sensors value chain.

Over 80 speakers CONFIRMED so far.

Book your place now, as it will be another sellout

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry

www.cs-international.net

PIC INTERNATIONAL CONFERENCE

Creating and strengthening links between chipmakers and network builders

www.picinternational.net

HES INTERNATIONAL CONFERENCE

High-end sensors: Market opportunities

www.highendsensors.net

REGISTER NOW, AND SECURE YOUR PLACE. REGISTRATION ALLOWS ACCESS TO: CS INTERNATIONAL, PIC INTERNATIONAL AND HES INTERNATIONAL

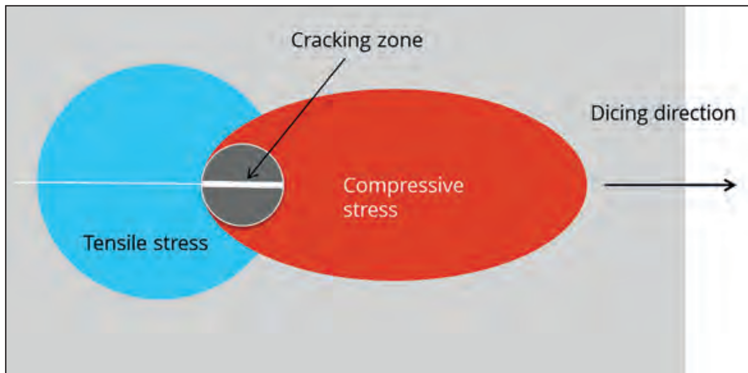


Fig. 1.
Principle of TLS

Limitations of established dicing technologies

Mechanical diamond blade dicing is the traditional technique for separating SiC wafers. The wafer is mounted on a dicing tape and is cut by a diamond coated saw blade rotating at high speed. The width of the dicing street is typically in the range of 50 to 100 μm. Due to the hardness of SiC, blade sawing suffers from low feed rate and high wear of the dicing blade, resulting in higher cost. In addition, blade sawing can result in chipping and delamination at the edge of the die. As SiC wafer sizes transition from 4-inch to 6-inch diameters, the cumulated street length more than doubles and is beyond the ability of one standard saw blade to completely cut. As a result, the blade has to be changed while the wafer is in work-position, and can break during the middle of the dicing process thereby damaging the wafer.

Laser ablation is an alternative approach to mechanical wafer dicing. The laser beam is focused into the dicing street. The material is heated up by the absorbed laser energy. This leads to a significant heat affected zone and micro cracks. There can also be a thermal impact on the dicing tape, which can affect subsequent packaging processes. In addition, the ablation rate is very low and multiple passes are needed to separate the dies. The number of repetitive passes depends on wafer thickness and cutting speed. To avoid material residues on the chips, the surface of the wafer has to be coated by a protection layer. Major disadvantages of this dicing technique are low edge quality and low throughput. In stealth dicing, a short pulsed laser beam at a wavelength that transmits through the SiC wafer is focused inside of the material. It generates a layer of localized defects inside the material that serves as a starting point for wafer separation. First, the laser beam is focused into the lower part of the wafer and moves layer by layer stepwise toward the top. Because it is a cleaving process there is no material removed in the dicing street—resulting in zero kerf. Second, the final separation of the dies must be done by a separate mechanical breaking process and expansion of the dicing tape. Since the laser heats up the material inside of the wafer, there is no heat damage to the wafer surface. Defects in a pearl chain pattern with overlapped areas only occur inside of the material. In addition, the feed rate for one pass is approximately 200 mm/s, though it can be up to 300 mm/s in some applications.

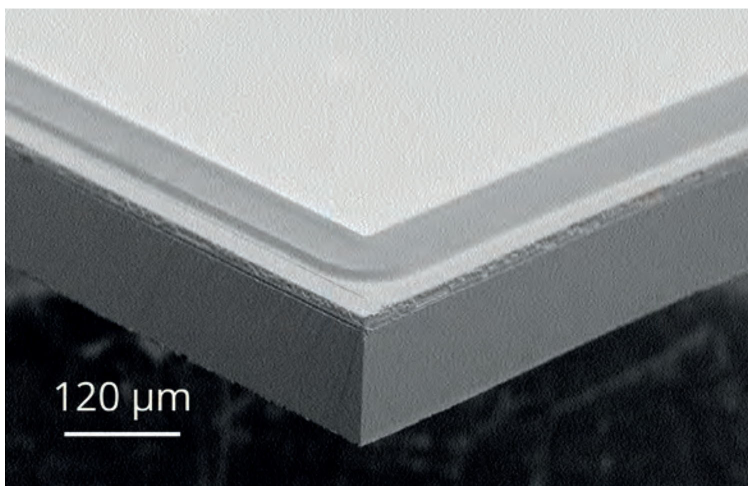
However, depending on the thickness of the material, several passes of the laser are needed to separate the dies. This leads to damages of the chip sidewalls due to the modified layers. To focus the laser beam on a very small spot inside the wafer, a smooth and minimizing beam that scatters across a flat surface in the dicing street is needed. To avoid reflection of the laser, a metal free dicing street is required. A further disadvantage is that the required width of the open street is a function of the wafer thickness (typically, 40 percent of the wafer thickness), which means that for a standard SiC wafer with a thickness of 350 μm, a minimum dicing street width of 140 μm is necessary.

Thermal laser separation

Thermal Laser Separation (TLS-Dicing) is a fast, clean and cost-effective alternative to separating SiC wafers. A laser heats up the material and generates a zone of compressive stress, surrounded by a zone of tangential tensile stress pattern (Figure 1). A jet of extremely small amounts of deionized water spray is then applied, which creates a second cooled zone near the first zone that induces a tangential tensile stress pattern. The resulting tensile stress in the overlaying region of both stress patterns opens and guides the crack tip through the material.

TLS-Dicing is a one-pass process that separates the whole thickness of the wafer with a separation speed of up to 300 mm/s. The starting point is given by a shallow scribe that is either local or continuous at the wafer's surface. Due to the fact that TLS-Dicing is a cleaving process, it has the potential to reduce the width of the dicing street and increase the number of chips per wafer. The die edges are smooth and free of remaining stress or micro cracks and chipping zone (Figure 2). Metal structures (PCM) in the street on the front side and polyimide on the dies are acceptable. In addition, since the separation is due to the cleave as opposed to subsequent physical

Figure 2:
SiC die edge after TLS-Dicing process shows smooth edges and no micro cracks or chipping



> TLS-Dicing is a one-pass process that separates the whole thickness of the wafer with a separation speed of up to 300 mm/s. The starting point is given by a shallow scribe that is either local or continuous at the wafer's surface. Due to the fact that TLS-Dicing is a cleaving process, it has the potential to reduce the width of the dicing street and increase the number of chips per wafer.

separation/breakage, the backside metal can be separated with no delamination or heat affects. Yield analyses on the use of the TLS-Dicing process on a typical power device wafer with full backside metallization, polyimide and metal structures in the dicing streets have shown an average yield value of more than 98 percent.

In addition, TLS-Dicing has demonstrated a significant improvement in terms of cost per wafer. A typical mechanical sawing process wears out one saw blade per wafer due to the enormous hardness of SiC, and is insufficient to completely cut a 6-inch wafer as noted earlier. To match the throughput of the TLS process, an investment in nine times more mechanical sawing tools is required. The added capital equipment cost combined with additional factors such as cost of consumables, projected tool depreciation and increased footprint result in a nearly 15X increase in overall cost per 6-inch wafer for mechanical sawing compared to the TLS-Dicing system. (Figure 3) [1]

Conclusion

Laser dicing processes are very promising methods to separate SiC dies with high efficiency. All laser dicing technologies described in this article offer higher separation speed than mechanical blade dicing. However, in laser ablation the dicing speed depends on the wafer thickness and the edge quality is not ideal. On the other hand, stealth dicing may require several passes depending on the wafer thickness, and requires an additional breaking process to separate the dies. With stealth dicing, it is also not possible to separate wafers with metal layers on the surface.

TLS-Dicing has demonstrated unique advantages for separating SiC wafers. The cleaving is always a one-pass process, so the feed rate of up to 300 mm/s applies. It produces excellent sidewall quality with no chipping, and has a far lower cost of ownership compared to mechanical blade dicing.

The cleaving principle shows unique advantages for SiC-based products with backside metallization, such as power devices.

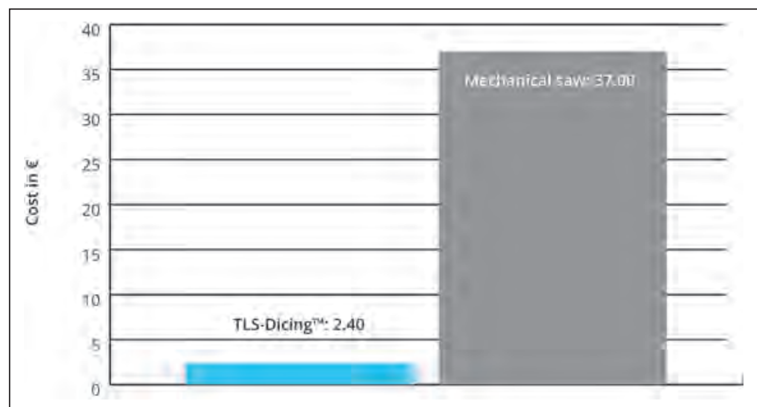


Figure 3: Throughput comparison for dicing a 6-inch wafer using TLS-Dicing and mechanical saw methods.

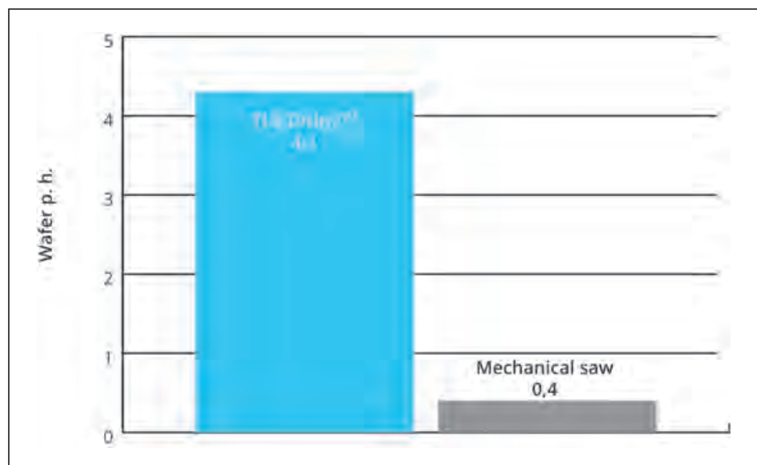


Figure 4: Cost per wafer comparison for dicing a 6-inch wafer using TLS-Dicing and mechanical saw methods.

Reference
[1] TLS-Dicing™: A Novel Laser-based Dicing Approach for Silicon Carbide Power Devices
http://3d-micromac.com/int/applications/tls-dicing

Transforming sub-fab service and support to lifecycle management

Edwards Vacuum President Paul Rawlings seeks to transform productivity by changing the way semiconductor manufacturers think about servicing their sub-fab equipment.

SERVICE AND SUPPORT now plays a key role in fabs to enhance process yields and reduce total cost of ownership. This has led to service models evolving away from the simple "break and fix" approach to a lifecycle management methodology, using techniques such as advanced diagnostics and predictive maintenance based on real-time monitoring of operational performance metrics. Reflecting this ever-increasing emphasis, equipment suppliers have elevated the service function to an equivalent status with other critical business functions, such as research and development and production. To support its vision of service as a customer centric enterprise that encompasses the entire product lifetime within the fab, Edwards has recently restructured its semiconductor service operation as a separate division.

Service and support for semiconductor manufacturing has evolved dramatically since the early days of the industry. For instance, our industry was among the first to put uptime requirements on equipment suppliers. To be competitive in the current environment, equipment suppliers must seek out opportunities to improve their customers' experience at all points in the product and fab lifecycle. Among the challenges we face today are: support for increasingly complicated manufacturing processes and materials; complying with increasingly stringent environmental regulations; and optimizing the use of scarce resources, such as water and energy. These are in addition to the ever-present pressure to reduce total cost of ownership and require a service model that is tailored to the varying needs at different points in the fab lifecycle. In considering this approach, it is convenient to divide the lifecycle into stages, each with its own requirements and opportunities for enhancement. The stages include: planning, installation, ramp, high-volume production, and end of life.

Planning

Engagement should begin at the earliest planning stage for a new fab or expansion of an existing facility. In this phase, it is critical that vendors explain the equipment options available to their customers and the benefits of the various choices. Important considerations include the process chemistry and vacuum demand, the evolving regulatory environment, demands of consumers for environmental responsibility, and the opportunities for lifecycle and data management.

Installation

Installation is an incredibly busy time in any new fab—when the emphasis must be on getting the equipment delivered, bolted down, hooked up and running as quickly and efficiently as possible. Given the large investment required to build a state-of-the-art fab, there is immense pressure to complete installation in the shortest possible time, and detailed knowledge of solutions that have worked in other similar applications are crucial in achieving that goal. Strong project management and the deployment of field-proven best-known-methods (BKMs) are the key to ensuring that fabs can start-up quickly and begin the critical ramp phase, proving-out tools and processes.

Ramp

The ramp phase is a race to achieve economic process yields. This invariably presents a myriad of challenges and opportunities to optimize the performance of sub-fab equipment and customize its operation to best match the process and application. Changes are inevitable, even with the best-laid plans, and it is in this situation that the deep expertise and broad experience of supplier personnel are most critical. For example, many cutting-edge deposition processes involve condensable materials that can deposit and eventually block exhaust lines unless temperature is precisely controlled along the entire exhaust pathway from the chamber exit through the vacuum pump and abatement system.

High-volume Production

High-volume production is probably where the

Figure 1: Lifecycle stages

greatest opportunity lies for tailored lifecycle management as even the slightest advantage in performance or efficiency can have a significant impact on output and the economic performance of the manufacturing process. It is here that managed maintenance—tracking the status of equipment and planning service interventions and the efficient use of on-site teams to maximize the efficiency of the fab—can have the greatest impact. It is here also that management systems (like Edwards EdCentra product), designed specifically to collect and analyze data from an entire fleet of systems installed across a facility, are essential in implementing a data-driven approach to service.

Massive and detailed data collection and analysis present many opportunities to optimize equipment performance. Each system's critical process steps can be custom tuned, before and after service, to an individualized "fingerprint" state to improve process repeatability. Predictive maintenance, which monitors critical operating parameters to determine when maintenance is required and coordinates scheduling with other process equipment, can significantly extend service intervals and reduce process downtime.

Monitoring parameters such as temperature, pressure, vibration, power consumption, and more, allows active management of equipment health and performance and can extend product lifetimes substantially. Historical usage and application data from individual systems can be used to optimize and customize the remanufacturing process for each system. Advanced diagnostics can ensure that when service is required the service engineer knows what the problem is, what to bring along to fix it and how to ensure that the repaired system will precisely replicate the performance of the system it replaces. Finally, analysis of real-time and historical data may provide an opportunity to move away from fixed price service to a more flexible and adaptive pricing approach.
On a much larger scale, aggregating data across large numbers of systems presents yet another set of opportunities. The full data set includes information acquired at every stage of the product's life cycle from original manufacture, through operation and remanufacture. Sophisticated modeling and data mining techniques can compare the performance of different products and setups in multiple situations to extract actionable information that helps service personnel to get the most from existing products and helps designers and engineers develop new products that better meet customers' needs.

End of Life

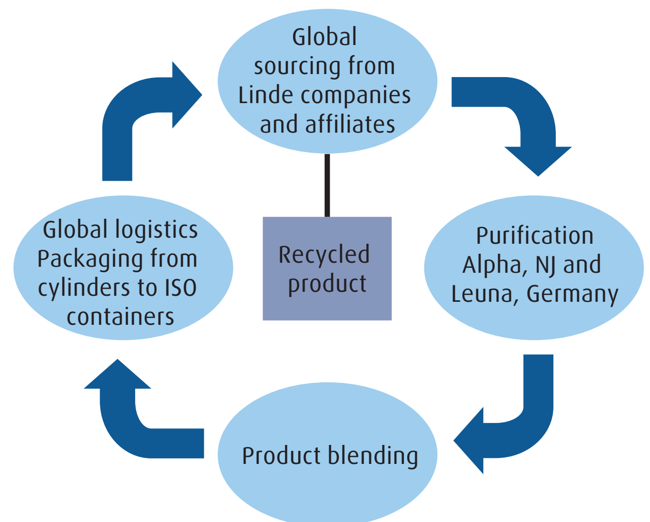
End of life management is next and is taking on a new dimension as older fabs find new life meeting the growing demand for mobile, automotive, and Internet of Things devices. This presents an opportunity to upgrade ageing electronic parts and components not typically replaced at a standard service or to take advantage of technological advances to upgrade or replace equipment with newer models that offer better performance or higher energy efficiency.
All this opportunity hides a real risk of analysis paralysis. Manufacturers must maintain their focus on meeting customer needs and delivering tangible results. Monitoring key service performance indicators, such as on-time delivery, timely installation, and speed of response for unscheduled repairs and problem solving success, can help. But the trick is to be sure that the manufacturers' indicators align with customers' priorities. Ultimately, the real opportunity lies in developing a shared view of total cost of ownership over the lifecycle of a fab. This will be the key step in implementing a fab lifecycle service model.

Leading the market with end-to-end rare gases supply chain

Investing in multiple-site rare gas production, blending, and purification facilities to assure long-term and secure supply worldwide

Linde is the only rare gases provider that can provide a robust supply chain including internal production and external partners, cryogenic production and purification technology, proprietary IP for the blending and analysis of laser gas mixes, in-house quality control capabilities, plant design and production, plus this product line:

- Helium – Most diverse portfolio of helium-producing assets
- Argon – Production off-site, delivery and on-site storage as liquid, and distribution on demand
- Neon, krypton, and xenon – Air separation units, purification, blending, and mixing
- Xenon difluoride – Global distributor and direct air shipment
- Xenon and neon recovery – On-site recovery and off-site reclamation, purification, and analysis
- Complete portfolio of laser gases – ArF, KrF, Kr/Ne, Ar/Xe/Ne, and HCl and BCl_3 mixes



www.linde.com/electronics
electronicsinfo@linde.com

THE LINDE GROUP
Linde

Designing microfabrication **lab equipment** with research flexibility in mind

Optimising R&D labs usually involves vendor collaboration and planning to provide required versatility. Louise Bertagnolli, president of JST Manufacturing explains.

AS RESEARCH becomes more complex, sophisticated cleanrooms have become a virtual necessity for a wide range of cutting edge physical science, material science, and biomedical disciplines.

Due to the financial investment required for such facilities, both university and private R&D laboratories are designed and built to accommodate the needs of a wide range of researchers. This presents a challenge: few administrators have the experience to select and set up lab equipment with the versatility required to serve such a diverse group of users over decades of continually changing research.

Now a growing number of lab administrators are optimising their microfabrication equipment, both for current and future needs, by involving their vendors early in the process. This enables expert planning as well as the selection of standard equipment options that can improve safety, usability, and efficiency while cutting cost.

"Often university lab administrators have never built their own cleanroom before, so they hire an architectural firm to do the design, but are still a little lost on how to lay out the equipment for all the different potential uses," says Louise Bertagnolli, president of JST Manufacturing. "Because universities are always pushing the boundaries of research, the equipment has to be very flexible so it can be used in ways not even conceived of yet."

A nationwide manufacturer of manual and automated wet processing equipment, JST's mechanical, electrical, and chemical engineers have many years of experience in industries including semiconductors, both silicon and compound, MEMS, photovoltaics, LEDs, Flat Panel Displays, and sensors.

Whether for compound semiconductor, nanotechnology, Micro-Electro-Mechanical Systems (MEMS), biophotonics, biomedical electronics, or creating solar power alternatives to traditional silicon wafer construction, much of the advanced research done in labs today requires microfabrication operations.

This typically includes wet processing equipment for metal lift-off, stripping, etching, plating/coating, cleaning, and de-bonding.

Dennis M. Schweiger, Senior Director of Infrastructure at the University of Michigan's Lurie Nanofabrication Facility (LNF), feels that the right combination of user requirements and assistance from the equipment fabricator can make a significant difference in the design, layout, and operation of a wet processing station. The LNF is a world-class facility in all areas of semiconductor device and circuit fabrication, integrated microsystems and MEMS technologies, nanotechnology, nanoelectronics, nanophotonics and nanobiotechnology. The LNF is an open use facility with hundreds of users from various UM departments, as well as many other universities and businesses.

Schweiger states, "Since we essentially rent lab space and equipment to our diverse users, it is important that we provide them with benches that suit their purposes well, from those who are processing wafers to those who may be doing very advanced research or testing on non-wafer components."

We like to give customers added flexibility by programming their equipment to do everything that the equipment is capable of doing. This enables them to dial in applications, such as chemical concentrations. They can also turn various features on or off, depending on your process requirements. Even though they may not need some of the features today, they may want to turn them on in the future, which can be both economical and powerful

According to Bertagnolli, who has guided numerous R&D lab administrators through the equipment design and selection process, the main concern is about setting up the cleanroom and procedures to serve the needs of users, but the process is not always well defined and there are many unknowns.

"When designing and laying out cleanroom equipment, it is important to talk with a vendor or consultant with the experience to help you achieve your evolving research goals," says Bertagnolli. "It is also essential that they help ensure it is correctly set up, that the proper safety, operation, and maintenance procedures are in place, and that lab managers are properly trained to carry these out."

Bertagnolli says that maintaining safety and flexible function for wet processing equipment often requires selecting the most appropriate options from a number of technologies. This may involve various chemistries, temperature controls, chemical baths/dips, ergonomic designs, as well as cleaning, filtration, ventilation, safety, and disposal technologies.

Designing modular and custom parameters

To facilitate the economical design and building of a wet processing equipment solution, many users insist on a standardized approach with customizable features that will best handle their applications parameters.

For example, JST utilizes standard products and standard methodologies to design and manufacture equipment. The equipment is modular by design, allowing for easy changing and reconfiguration should process or product requirements change.

Another powerful feature: each unit is designed with software that is capable of performing all tool functions, including those that are not required. With this, end users can create their own process, or recipes, with all sub-routines at their disposal. "We like to give customers added flexibility by programming their equipment to do everything that the equipment is capable of doing," explains Bertagnolli. "This enables them to dial in applications, such as chemical concentrations. They can also turn various features on or off, depending on your process requirements. Even though they may not need some of the features today, they may want to turn them on in the future, which can be both economical and powerful." Specifying the design parameters for many manual benches may not be as involved as those of automated systems. However, soliciting the opinion of equipment manufacturers regarding equipment design may be highly beneficial.

"Certain processes like etchings and cleanings lab managers will want to be flexible enough to accommodate a wide range of users and projects," says Bertagnolli. "We are often asked for tank construction materials that can withstand several concentrated acids, so part of design flexibility is ensuring you use the most compatible materials for the most acids."

"Another aspect to consider is properly separating, neutralizing, and disposing of all the chemistries involved after use, whether in drains or tanks for treatment or pick up," she adds.

According to Bertagnolli, having the vendor visit the user's facility can contribute to equipment design versatility that can accommodate changes in lab use over the long term.

"An eye toward optimizing working space, operating cost, or maintenance can go a long way toward creating a cleanroom that will serve the user community well now and in the future," says Bertagnolli.

Optimising LNF's Lab

The LNF's Schweiger at the University of Michigan explains that the original equipment design for the new lab areas wet processing benches was very specific, and determined by LNF staff.

"We had looked at it in terms of process flow, from start to finish, not really considering the variety, and variation, of process samples that our user community might be working with, how we'd accommodate non-standard sample sizes, or what the impact might be in total cost of ownership with respect to chemical usage," he says.

Schweiger adds that the some of the new benches had their decks reconfigured once the tools were installed. Several of the earlier benches, some of which were purchased over 20 years ago, were also modified to allow for more flexibility in meeting the process needs of the user community.

"In retrospect, our initial plan for the deck space, and processing capability of the benches, wasn't adaptable or flexible enough, and we worked with JST to implement modifications so that the bench decks were simpler, and could provide more working space," Schweiger concluded.

3 EVENTS
2 DAYS
1 TICKET

10-11 April 2018

Sheraton Brussels Airport Hotel, Belgium

One ticket gives you access to a 2 day event which will see 3 groups of device makers gathered under one roof.

Hear over 90 presentations covering the entire spectrum of the compound semiconductor, integrated photonics and high-end sensors value chain.

Over 80 speakers CONFIRMED so far.

Book your place now, as it will be another sellout

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry

www.cs-international.net

PIC INTERNATIONAL CONFERENCE

Creating and strengthening links between chipmakers and network builders

www.picinternational.net

HES INTERNATIONAL CONFERENCE

High-end sensors: Market opportunities

www.highendsensors.net

REGISTER NOW, AND SECURE YOUR PLACE. REGISTRATION ALLOWS ACCESS TO: CS INTERNATIONAL, PIC INTERNATIONAL AND HES INTERNATIONAL

Automated systems increase wafer lapping and polishing productivity

Logitech's new automated lapping and polishing systems for almost all substrate materials dramatically increases wafer end productivity by up to 40 percent.

THE LAPPING and polishing of wafers used to manufacture semiconductors and optical devices is a time consuming task that can risk damage to expensive custom wafers worth in excess of (USD) $5,000 each if things do not go to plan. Logitech has substantially automated the process, speeding productivity and increasing repeatability by approximately 40 percent compared to non-automated techniques.

In wafer end fabrication, lapping and polishing processes have become more predictable, but there is often the need for a significant level of user expertise, guesswork and development time in order to optimise surface finish and repeatability. This can hamper the development of new technologies, especially as a process that is optimised at the pilot stage will often need to be revisited when transitioned to full production.

The path to better process control lies within Preston's Law (see Figure 1), which provides a framework for predicting the amount of material that will be removed in a given time by lapping and polishing processes. By controlling variables using automated precision lapping and polishing systems with high levels of user control, operator variability can be minimised while process accuracy and greater repeatability can be achieved.

The Preston's Law equation states that the material removal rate (MRR) is proportional to the product of

0.014
MODE
SET
-0.0003
MODE
SWISS MADE
SET

the processing pressure/load/down-force and plate velocity. In the chemical mechanical polishing (CMP) process, polishing rates and overall accuracy are affected not only by the flow of the slurry and the characteristics of the polishing plate, but also by the mechanical action between the wafer and the plate, chemical reactions arising from slurry component molecules, and the interactions between these variables. Preston's Law can be used to accurately predict the amount of material removed from a sample and confirm stability in the process. High degrees of process stability are possible by using a stable/accurate/repeatable processing platform such as the Logitech Akribis-air, which handles up to 150mm wafers, or the PM6 Precision Lapping & Polishing system designed for wafer samples up to 100mm.

Meeting demanding wafer requirements using manual lapping and polishing tools is hard to achieve with silicon, III-V or other very hard semiconductor wafer materials because of the high level of operator skill needed to manually stage and control such operations. Setup is a time consuming process that is not conducive to the high productivity that is demanded by semiconductor research and production facilities. Cost reduction in device production is driven by volume and yield. Automated systems designed to eliminate manual steps will ultimately increase productivity in wafer fabrication processes.

Logitech's Mark Kennedy, Head of Process Technology Development, frequently works with customers in the field who appreciate the precision of an automated systematic approach to wafer lapping and polishing. "The customer used our new Logitech PM6 and reported seeing substantially higher throughput and greater control, which allowed them to achieve sample specifications that were previously unobtainable on other equipment. The features and functionality of the machine including its recipe modes, auto plate flatness and real time data collection allowed operators with basic training to achieve the same accuracy and throughput that a skilled engineer might deliver. They achieved a real boost in productivity," Kennedy said.

Silicon lapping & polishing

Every semiconductor wafer undergoes several common stages during manufacture including slicing the wafer from its crystal ingot, preparing the surface prior to fabrication and subsequent thinning of the wafer through lapping and polishing techniques.

After slicing, wafers made of silicon or III-Vs materials are lapped to remove surface scratches and flaws that occur during cutting processes. Typically performed by the wafer manufacturer, lapping removes saw marks and surface defects from the wafer and also helps relieve any internal mechanical stress that accumulated during the slicing process.

Lapping typically involves counter-rotating plates using an aluminium oxide abrasive with defined grain size distribution. During lapping, wafer flatness is improved while micro-roughness is also reduced. An edge grinding procedure may also take place. When edge grinding is needed manufacturers may also follow this step with polishing the wafer edge since doing this can greatly reduce the probability of wafer breakage further down the process line.

Chemical mechanical polishing is the final material removal step utilized in manufacturing wafers. This process allows the attainment of super-flat, mirror-like surfaces with a remaining roughness on an atomic scale. Polishing the wafer can be seen as the most crucial step in the manufacturing process since the polished wafer face is used for device fabrication; it must be as damage free as possible. Typically, CMP is achieved using a rotary or orbital motion of a chemical slurry injected in precise quantities and flow rates between the polishing plate and the wafer itself.

There are many reasons why manufacturers need stability and repeatability when it comes to wafer sample preparation. For instance, stringent quality requirements dictate that parameters such as total thickness variation (TTV), surface roughness and plate flatness must be carefully monitored. In all cases, a fundamental understanding of the process is required to ensure a quality outcome. Different types of wafer materials, slurries and polishing pads, along with polishing rate, pressure and uniformity can all impact the resulting surface. It is also important not to overburden the surface with too much slurry as this has the potential to impair detection of when the

polishing process is complete. To put this in simple terms, it is vital to accurately predict the amount of material removed from a sample in a given time. Here, Preston's Law is fundamental to successful lapping and polishing. Indeed, it is possible to analyse the Prestonian behaviour of material removal rate (MRR) to confirm that all-important process stability has been achieved.

Silicon lapping and polishing trials

Lapping and polishing trials using a typical silicon substrate deployed in semiconductor applications such as the manufacture of integrated circuits, solar and waveguide devices can be extremely revealing. In a typical silicon lapping and polishing process, a series of steps are used, each with a different slurry solution.

Firstly, a coarse lapping process is undertaken to remove material within 50 μm of the end point target. Previous experiments have shown that slurries containing Al2O3 particles measuring 20 μm provide the optimum balance between material removal speed and maintaining the integrity of the underlying silicon wafer. In a second stage, a medium/fine lapping process is conducted, during which a finer, less abrasive 9 μm Al2O3 slurry is used to remove materials to within 10 μm of the end point target. The final stage involves removing the last micrometres of material; the removal of any damage caused to the wafer during the lapping process is also undertaken using 32nm colloidal silica, such as the Logitech SF1 polishing slurry. After undergoing all three stages a typical surface roughness of Ra<1nm is achievable.

Tests to determine average silicon lapping at 50 rpm versus 100 rpm showed an average MRR of 18-22 μm/min using an automated system: the Logitech Akribis-air. This was compared to that of a standard Logitech lapping and polishing system with an MRR of 7-9 μm/min. Substantial time savings and accuracy were achieved with the automated set-up and control platform; the Akribis-air tool also provided internal clean-up facility. Collectively, all automation-derived improvements delivered a total process time savings of approximately 40 percent.

Differentiating features found in automated systems such as the Logitech Akribis-air and PM6 Precision Lapping & Polishing System are key to achieving such impressive results. Automated air jigs (available with the Akribis-air) and intelligent automated controls on both systems have positive impacts on processing that benefits not only by creating a flatter, more defect-free wafer but also in terms of substantial process time reductions. These technologies can help semiconductor and optical device manufacturers to precisely optimise their sample preparation processes.

A high degree of geometric precision, flatness and parallelism can be achieved by taking advantage of automatic wafer thickness control. Software-driven

set-up within automated systems permits faster processing times (in tandem with plate speeds of up to 100rpm) and more reliable results. There is also extensive parameter control for the processing of complex and fragile wafers; metered abrasive feed supplies for optimal processing and reduced wastage of consumables are other substantial cost saving factors. Automated system like the Logitech PM6 or the Akribis-air also provide for the export of critical data as an information base for future process refinement and documenting productivity improvements over time.

Semiconductor and optical device manufacturers demand greater process control and real-time data in their quest for improved productivity and reliable, repeatable quality. By utilizing an automated approach in wafer sample preparation such as the Logitech Akribis-air or the PM6, researchers and manufacturers alike can achieve faster throughput, more precisely prepared and polished wafers, all with dependable repeatability that also frees their most highly skilled engineers and technicians to focus on other critical endeavours.

Silicon photonics
for a post-Moore era

What solutions are in the pipeline to support higher performance devices in a post-Moore era? Koji Yamada, head of the Silicon Photonics Group at the Electronics and Photonics Research Institute - a division of Japan's National Institute for Advanced Industrial Science and Technology (AIST), explores the opportunities provided by silicon photonics and discusses the next steps for this exciting PIC platform.

MOORE'S LAW expresses an empirical trend in device integration in electronic circuits, such as micro-processor chips. The device integration status is defined as the number of elemental devices -- such as transistors -- integrated on a chip, which doubles every two years. However, such exponential growth defined by Moore's law is now coming to an end, because -- ultimately -- miniaturised devices see the de Broglie wave of electrons (more details below). In other words, we are now entering the post-Moore Era. At the same time, we are seeing explosive growth in information systems, which is one of the major applications of electronic circuits, and improvements in their performance must continue. To cope with such an information explosion, various post-Moore electronic circuit technologies are now being developed under guidelines referred to as 'More Moore', 'More than Moore', and 'Beyond CMOS'. In 'More Moore', further geometrical integration is achieved by introducing novel materials and three-dimensional (3D) integration methods. 'More than Moore' is a system-on-chip (SoC) approach, where non-digital devices are implemented. 'Beyond CMOS' refers to devices based on novel principles, such as electron spins, and novel architectures suitable for these novel devices.

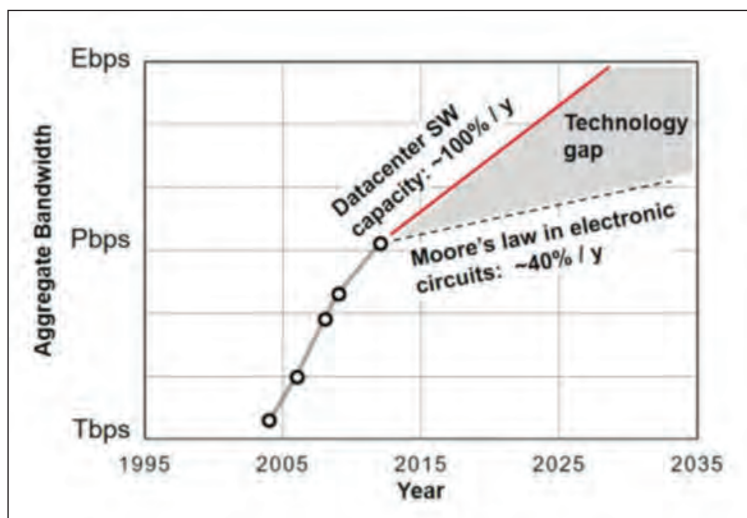


Figure 1: Trend of switching capacity in a typical large-scale datacentre.

Moore's Law in data transmission, which is an important aspect of information systems, is also facing its end. For example, as shown above, switching capacity in a typical large-scale data centre is growing at a rate of 100 to 1000 times every 10 years1, which is overwhelming Moore's Law in electronic circuits. Since electronic circuits are used for switching systems at present, such explosive growth will become unsustainable soon. In the global network system, we are also facing the end of Moore's Law. For more than 30 years, data transmission capacity per fibre has been increasing with a growth rate of 80 percent a year through various paradigm shifts in

technology, such as from TDM to WDM and multi-level modulations2. However, it has now reached the nonlinear Shannon limit.

To cope with such explosive growth in data transmission, we also need post-Moore technologies for photonics as well as for electronics - because data transmission systems consist of electronic and photonic elements. For the development of post-Moore photonics technology, the same approaches in electronics can be applied, and silicon photonics provides a platform for post-Moore photonics.

Silicon photonics as a post-Moore photonic technology

Thanks to the very strong optical confinement ability of silicon photonics technology, photonic circuits can be miniaturised considerably, and data transmission capacity per unit chip area can be increased. An example is an integrated WDM receiver chip consisting of multi-channel wavelength filters, photodiode (PD) array, and electrodes for signal output. By using silicon photonics, an arrayed-waveguide-grating (AWG) wavelength filter, which is a standard multi-channel wavelength filter, can be miniaturised to 1-mm square. Moreover, germanium PDs and through-silicon via (TSV) electronic wiring can be scattered over the whole the chip.

Therefore, as shown above, the required area of a 100-ch WDM receiver chip will be reduced to 1 cm2, which is 1/100 of the area of chips based on conventional technology. Assuming PD operation at 25 Gbps, total capacity will reach 2.5 Tbps/cm2. In parallel transmission systems, where no wavelength filter is required, total bandwidth can be increased up to 30 Tbps/cm2 3.

Spatial division multiplexing (SDM) can also be categorised as two-dimensional geometrical integration. By using silicon photonics technology to make ultra-small optical coupling structures within the area of a fibre core, highly integrated SDM modules consisting of an SDM fibre interface and optical processing circuits can be constructed4.

More than Moore: Photonics - electronics SoC

Integration with electronics is the most impactful post-Moore technology for photonic circuits. Integration with modulation drivers, transimpedance amplifiers for PDs, and various control circuits on a silicon photonics chip can significantly reduce the size of photonic-electronic integrated modules. Moreover, since electronic circuits can be placed very close to photonic devices, high-frequency performance can be significantly improved5.

Since silicon photonics is based on silicon electronics technology and the silicon platform is reliable and robust, electronic circuits can be integrated by both monolithic and hybrid approaches. Concepts of such photonics-electronics convergence can be seen above. The monolithic approach is very attractive from the viewpoint of ultra-high-volume production, and some short-range data transmission modules have already been commercialised6.

However, we must consider that device performance might be degraded because of narrow margins in the fabrication process for photonics-electronics convergence. For example, in monolithic photonics-electronics convergence, the dark current of germanium PDs is likely to increase. Moreover, typical CMOS electronics technology cannot provide the high-speed electronics required for high-bit-rate optical data transmission.

For improving device performance both in photonic and electronic circuits, the hybrid approach is

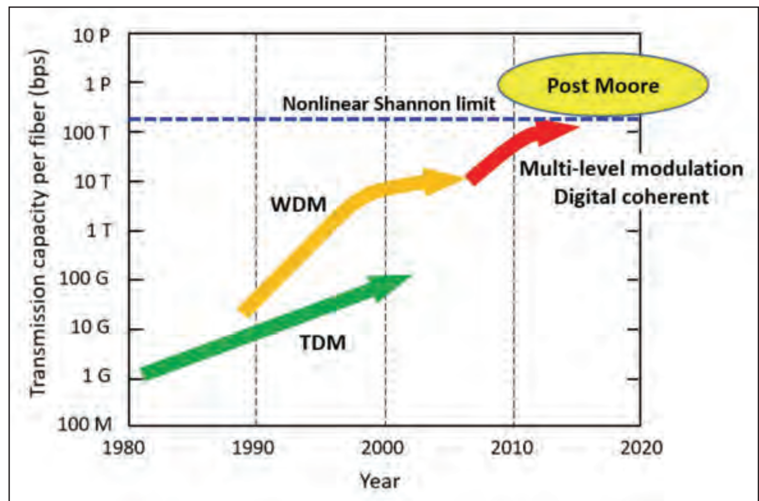


Figure 2: Trend of data transmission capacity per fibre.

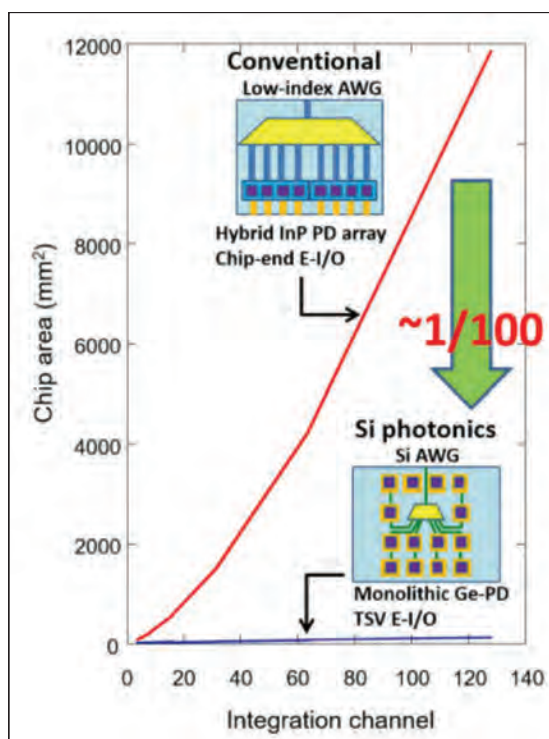
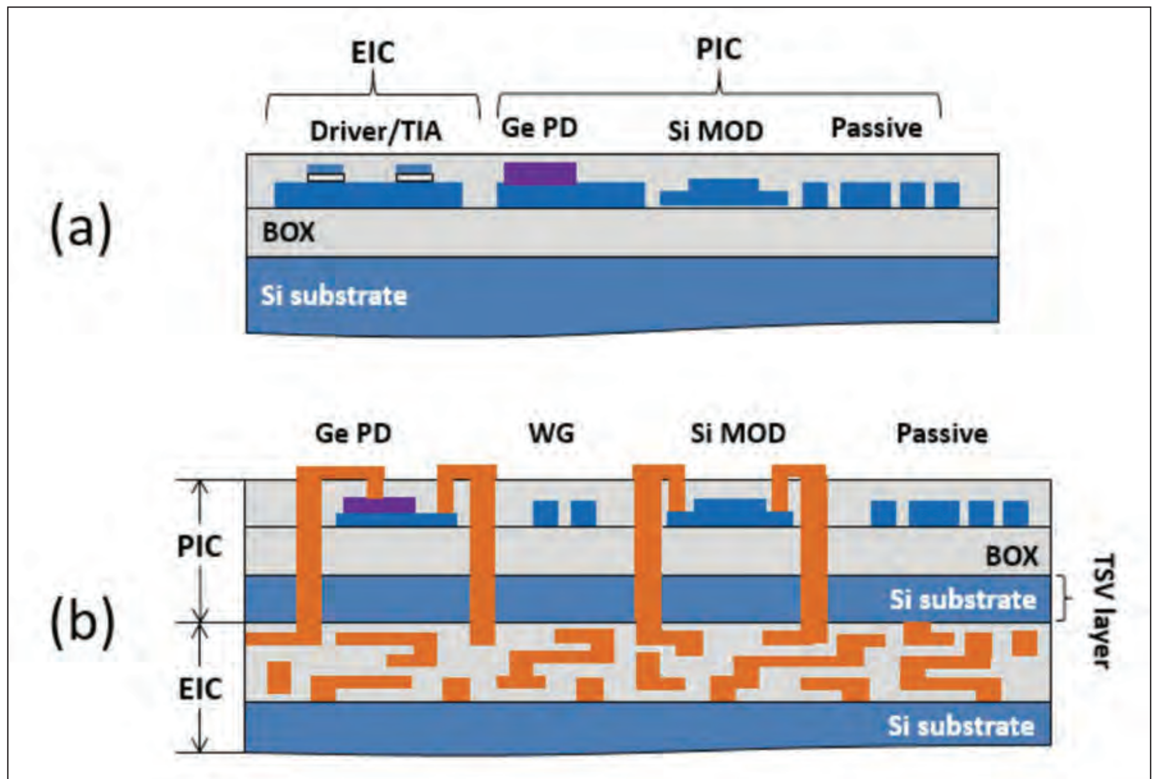


Figure 3: Estimated chip area of integrated WDM receiver sub-assembly.

Figure 4: Photonics-Electronics convergence. (a) Monolithic and (b) TSV-based hybrid integration.



attractive. Since both types of circuits can be fabricated by their respective optimised fabrication process, high-performance photonics-electronics convergence can be achieved. Hybrid integration is performed by using various wafer-bonding/die-bonding techniques with TSV and micro-solder bump technologies7. Since hybrid integration technology is a kind of 3D integration technology, it can also contribute to geometrical integration in the More Moore approach.

Novel-principle devices and architectures: replacement of electronics with photonics

Since current optical fibre transmission systems show excellent performance, we currently have very small margins for novel-principle devices. However, if we consider data transmission systems replacing electronic circuits with photonic ones corresponds to an approach for implementing novel-principle devices and architectures. This approach can be seen

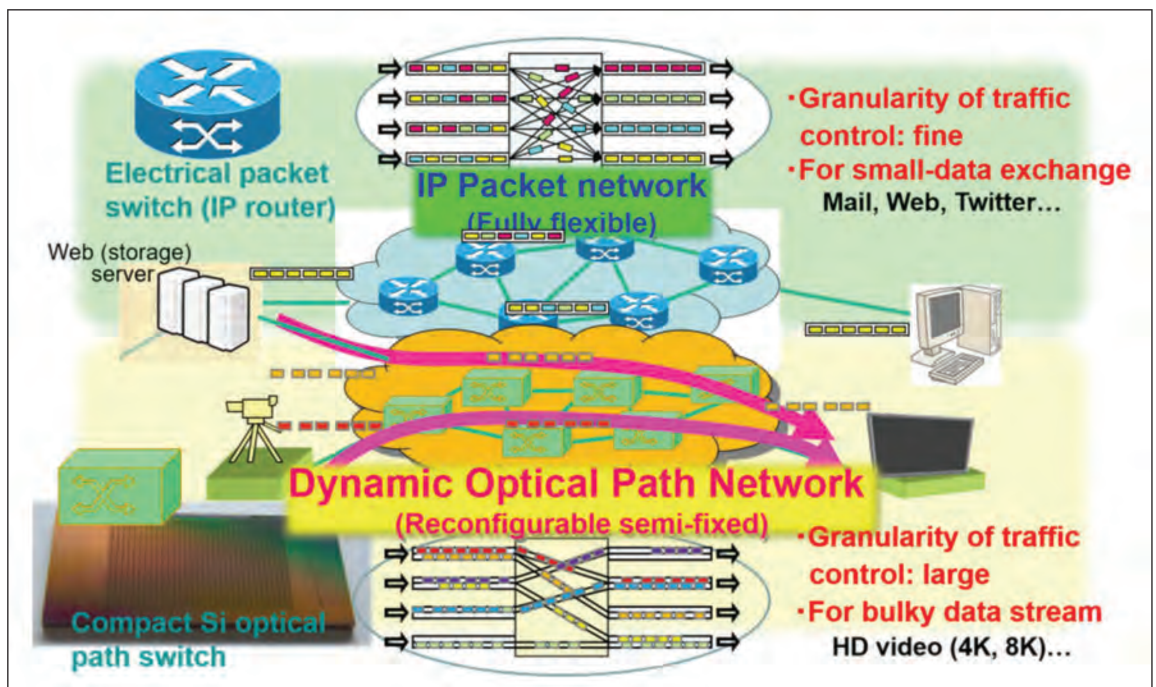


Figure 5: Dynamic optical path network.

SEMICON® EUROPA
Munich, Germany

Visit us at
Booth 1739, Hall B1

AP&S

Discover the fascinating world of wet process technology

The AP&S product range includes manual, semi-automated and fully automated wet process tools. These are developed for cleaning, etching, metal etching, PR strip, electroless plating, lift-off, drying and developing processes.

Come to our booth, visit our website www.ap-s.de and find out more. To prearrange a meeting with us at the Semicon Europa trade fair, please contact our team at sales@ap-s.de

Furthermore we offer you:

- Chemical management systems, laboratory equipment and refurbishment programs for used tools like FSI Mercury, Lotus, Steag, etc.
- Extensive expert support in our in-house laboratory
- Process demonstrations at our headquarters prior tool ordering
- Innovative IoT solutions
- Fast and reliable After Sales Service worldwide

AP&S International GmbH
Obere Wiesen 9
78166 Donaueschingen
Germany
Tel.: + 49 771 8983-0
E-mail: sales@ap-s.de
Website: www.ap-s.de

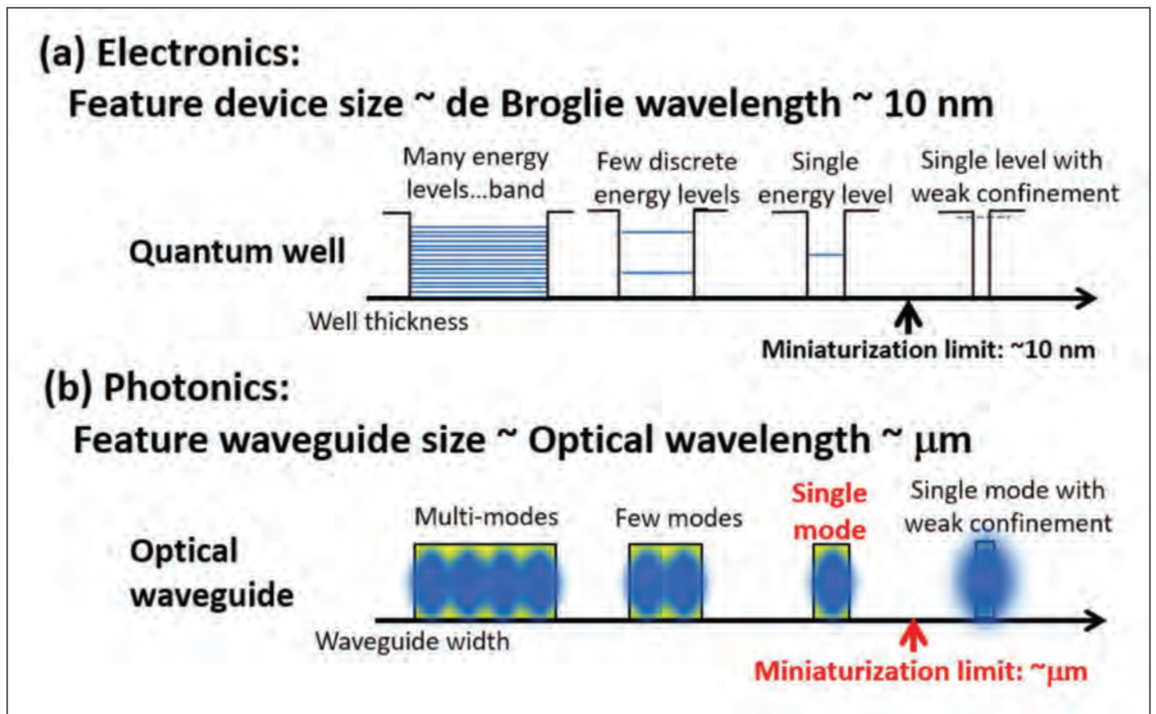


Figure 6: End of miniaturization scaling.

in the dynamic optical path network (DOPN) using large-scale optical switch matrixes8,9. Conventional switching systems are made of electronic devices, where numerous small packets are independently routed to several unspecified terminals. Thus, power consumption for the switching increases proportionally to the data traffic.

This conventional packet switching scheme, however, is not suitable for the transmission of bulky video data to specified terminals, which has been a dominant factor in the recent traffic increase. In the DOPN, as shown above, dedicated optical transmission channels are temporarily constructed by an optical switching matrix. Since packet switching is not utilised in the DOPN, the power consumption for bulky data transmission can be greatly reduced. Recently, a DPON field trial using a silicon-photonics-based optical switch matrix has been carried out8.

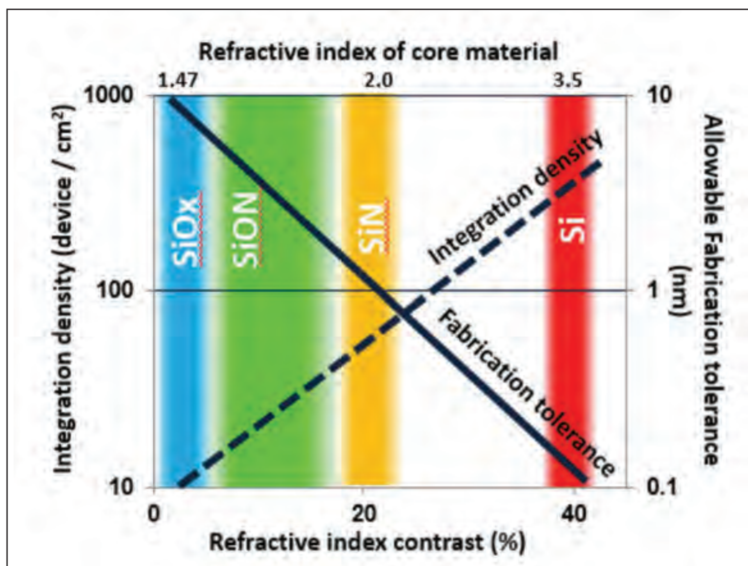


Figure 7: Integration density and fabrication tolerance in AWG wavelength filters. (200 GHz x 16 ch, neighbouring channel crosstalk < -20 dB)

Evolution of silicon photonics

As mentioned, silicon photonics technology provides immediate solutions for data transmission systems in the post-Moore era. However, to deal with the expected increase in traffic in the future, silicon photonics itself must evolve much further. This is because there are serious obstacles to further performance improvement and miniaturisation. One hurdle is the severe fabrication tolerance in silicon photonics, which is a fatal problem. Typical fabrication errors in thickness and width of Si waveguide cores are nanometres in scale. Since a silicon waveguide is very small, such errors can result in large crosstalk and strong polarisation dependence, which significantly degrade performance10.

Nonlinear effects in silicon waveguides are also serious problems in practical applications. Silicon has a large nonlinear coefficient, which is about 100 times larger than that of silica. Moreover, the optical field size in a silicon waveguide is extremely small. Thus, nonlinear effects, such as four-wave mixing and two-photon absorption, are greatly enhanced. The resulting large channel crosstalk and poor power tolerances significantly degrade device performance. Poor carrier mobility in silicon is also a serious obstacle to achieving ultra-high speed device operation of over 40 Gbps.

But what about the end of Moore's Law in silicon photonics? As discussed earlier, Moore's Law in

electronics is ending because device size has reached the wavelength of the de Broglie wave. Referring to Figure 6(a) -- for example -- as an electronic quantum well becomes thinner, the number of energy levels decreases. Eventually, the number is reduced to a single energy level, and this is the end of miniaturisation. The critical thickness is about 10 nm. Any thinner and electron confinement becomes very weak and the device will not work well.

The same analogy is applicable to optical waveguides, as shown in Figure 6(b). In other words, a single-mode waveguide, whose core size is comparable to the optical wavelength, is the end of miniaturisation. Any smaller and photon confinement becomes very weak and the device will not work well. The critical core size is about half of a micrometre for infrared transmission in the 1.55-μm telecommunications band. Since the single mode waveguide has been the most essential element in silicon photonics, Moore's Law has already ended.

Through these discussions, we cannot help but conclude that silicon photonics requires post-Moore technology, and -- we believe -- three approaches in the development of post-Moore electronics can be applied here again for the development of post-Moore silicon photonics technology.

More Moore: further geometrical integration (3D)

For 3D photonic integration, backend photonics is a promising technology. Backend photonics is a performance-assisting technology using additional waveguide systems made of various materials. The requirements for the additional waveguide systems are 1) a low-loss and compact photonics system comparable to the silicon photonics system; 2) functionalities comparable to those in the silicon photonics system; 3) low-loss interlayer coupling between the additional waveguides and silicon waveguides; and 4) the ability to fabricate the additional waveguide system without damaging the silicon photonic system underneath it. In other words, the additional waveguide systems should be constructed by using the backend fabrication technology for silicon semiconductors, which is the reason we refer to the additional waveguide systems as backend photonics.

Silicon-nitride-based materials, such as SiOx, SiON and SiN, are promising for backend photonics. The most attractive feature of these materials is that their refractive index can be largely tuned11. These materials cover a wide refractive index range, and optical waveguides using these moderate-index materials would significantly relax fabrication tolerance. The above chart shows the estimated integration density and fabrication tolerance as a function of refractive index contrast of a waveguide. Using moderate-index materials, fabrication tolerance is significantly relaxed while keeping still high integration density.

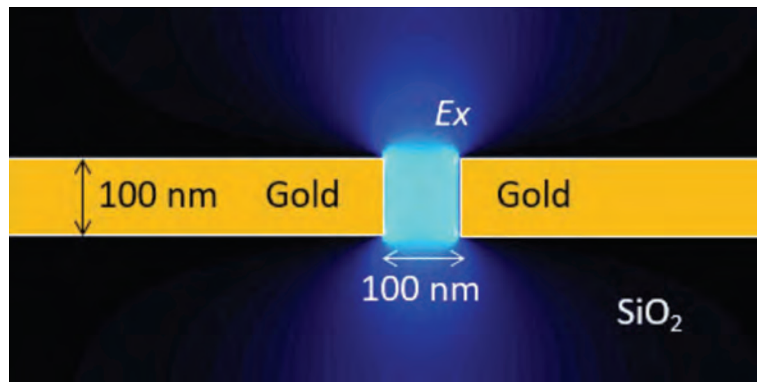


Figure 8: Structure and optical mode field of plasmon waveguide.

Table 1 shows nonlinear coefficients and thermo-optic coefficients of such materials. These coefficients are less than one-tenth of silicon's. Recently, low-loss interlayer coupling structures have been developed using inverted tapers12,13. By using PECVD technology, the deposition temperature can be reduced to less than 350 degC, which would not damage the silicon/germanium devices underneath the additional waveguide system.

This silicon-nitride-based backend photonics technology has been used to develop low-crosstalk high-resolution AWG wavelength filters and integrated them with silicon-based modulators and germanium-based PDs on a silicon photonics platform14, 15.

More than Moore: heterogeneous photonic SoC

The additional waveguide system can integrate various additional photonic functionalities on the silicon photonics platform, because it can increase the degree of freedom in device design. For example, by using silicon-nitride-based waveguides constructed on silicon waveguide systems; polarisation

Silicon-nitride-based materials, such as SiOx, SiON and SiN, are promising for backend photonics. The most attractive feature of these materials is that their refractive index can be largely tuned11. These materials cover a wide refractive index range, and optical waveguides using these moderate-index materials would significantly relax fabrication tolerance

Table 1: Nonlinear and thermo-optic coefficients of Si and backend photonics materials

	Si	SiN/SiON/SiOx
$n_2 / n_{2(SiO2)}$	175	< 10
γ $[W^{-1}m^{-1}]$	300	< 1.4
β_{TPA} [cm/GW]	0.9	-
dn/dT [$\times 10^{-5}$/°C]	19	1~5

manipulation16, 17 and fibre-mode MUX/DEMUX18, have already been demonstrated. Because of material incompatibilities, these functionalities were constructed outside the silicon photonic chip by using bulky conventional optical components.

Novel-principle devices: restarting Moore's Law

As mentioned above, the core size of a silicon waveguide cannot be reduced to less than a half of the wavelength, and Moore's Law has already ended in silicon photonics. However, we know that radio waves, which have metres of wavelength, can be confined in a centimetre-diameter cable. Radio waves are confined as a TEM-like wave supported by surface electron density waves in metals. Here, recall that the miniaturisation limit of electron density waves is determined by the de Broglie wavelength, which is around 10 nm. Thus, we can restart Moore's Law in photonics. Roughly speaking, a photonic system based on such a metallic confinement is referred to as plasmonics.

The above schematic shows a photonic waveguide based on plasmonics on a Si photonic platform. The optical field is confined in a 100-nm-wide gap between two metallic plates. By filling this gap with electro-optic (EO) polymers and applying voltage to these metallic plates, we can change the refractive index of the EO polymer. Thus, we can construct a very compact optical phase shifter, which is a fundamental element of optical modulators.

Recently, such a plasmonic-polymer waveguide system has been used to develop Mach-Zhender interferometer optical modulators19. Since the gap is very narrow, the electric field in the gap is very strong and the modulation efficiency becomes extremely high. For example, the voltage-length product -- which is a measure of the efficiency of phase shifters -- reaches 0.006 V.cm, which is less than 1/100 of that of a typical silicon modulator. Thus, a device a few tens of micrometres long can function as a modulator with practical modulation depth, and such a small device can operate at very high frequencies of over 100 GHz. Such plasmonic devices would be a significant breakthrough in the post-Moore photonics technology.

Summary

Moore's Law in data transmission systems is nearing its end, and we need post Moore-photonics technology. In the development of post-Moore photonics technology, we can apply the same approaches that have been established in electronics, and silicon photonics can provide immediate solutions for post-Moore photonics technology.

However, we must note here that silicon photonics itself requires post-Moore technology because of the quantum limit in miniaturisation and poor material characteristics. Here again, the same approaches established in electronics are applicable to post-Moore silicon photonics with the help of backend photonics and plasmonics.

References and further reading

[1] A. Singh et al., Proc. annual conference of the ACM Special Interest Group onData Communications (SIGCOMM 2015), London (2015).
[2] D.J. Richardson, Science 330, 327 (2010).
[3] Y. Urino et al., Proc. ECOC 2013, Mo.4.B.2F, London (2013).
[4] C.R. Doerr et al., Proc. ECOC 2011, Th.13.A.3, Geneva (2011).
[5] M. Usui et al., Proc. ICEP-IAAC 2015, 660-665, Kyoto (2015)
[6] T. Pinguet et al., Proc. IEEE GFP 2012, ThC1, San Diego (2012).
[7] J-M. Fedeli et al., IEEE J. Selected topics in Quantum Electronics 20, p.8201909 (2014).
[8] J. Kurumida et al., Proc. ECOC 2014, PDP 1.3, Cannes (2014).
[9] K. Tanizawa et al., Optics Express 23, 17599 (2015)
[10] K. Okamoto, Laser & Photonics Review 6, 14 (2011)
[11] T. Tsuchizawa, "Guided Light in Silicon-Based Materials," Handbook of Silicon Photonics (ed. by L. Vivien and L. Pavesi, CRC Press, 2013)
[12] T. Hiraki et al., Electronics Letters 51, 74 (2015).
[13] R. Takei et al., Optics Express 23, 18602 (2015).
[14] H. Nishi et al., Applied Physics Express 3,102203 (2010).
[15] T. Hiraki et al., IEEE Photonics Journal 5, 4500407 (2013).
[16] H. Fukuda et al., Optics Express 16, 4872 (2008).
[17] L. Chen et al., Optics Letters 36, 469 (2011).
[18] T. Hiraki et al., Proc. OFC 2015, W1A.2, Los Angeles (2015).
[19] C. Haffner et al., Nature Photonics 9, 525 (2015).

LOGITECH
Materials Technologists & Engineers

Precision system solutions for Semiconductor wafer processing

Precision materials processing systems provide a quick and effective route to complete success in any device fabrication process

Over 50 years in the design and manufacture of precision lapping & polishing, cutting and bonding technologies:

www.logitech.uk.com

Get in touch to discuss your wafer processing needs:

enquiries@logitech.uk.com

Using manifold technology to optimize cost of ownership

The management of fluid systems is experiencing a drastic change on how a customer perceives the importance of the component. By Stephane Domy, Global Marketing Manager, High Purity Systems at Saint-Gobain Performance Plastics

WE HAVE MOVED from only looking at the component as a standalone item, which has its own specification and benefits for the carried fluid, to looking at the impact of a set of components, which can also be called a manifold on the installation / application. This evolution has been a driving force in the micro-e industry and prompting it to embrace the co-development of products, which is something Saint-Gobain has recognized and supported for years. It is part of our DNA.

To review what the manifold approach may bring to your installation/system, let's split the benefits provided by manifolds into three main categories: Safety, Cleanliness and Cost of ownership.

One of the direct impacts that is inherent when you manifold a set of components is that you are reducing the number of leak points. You are not simply improving the sealing efficiency of a connection; you are totally eliminating it. On average, you can expect a leak point reduction above 60 percent on some occasions it can be significantly higher than that, but that percentage relates directly to what you are manifolding. As an example, in the simple manifold illustration below we are moving from 26 connection points down to 6 (All red connection points are removed. We only keep the green ones).

Remove potential leak points (identified in red) through manifolding

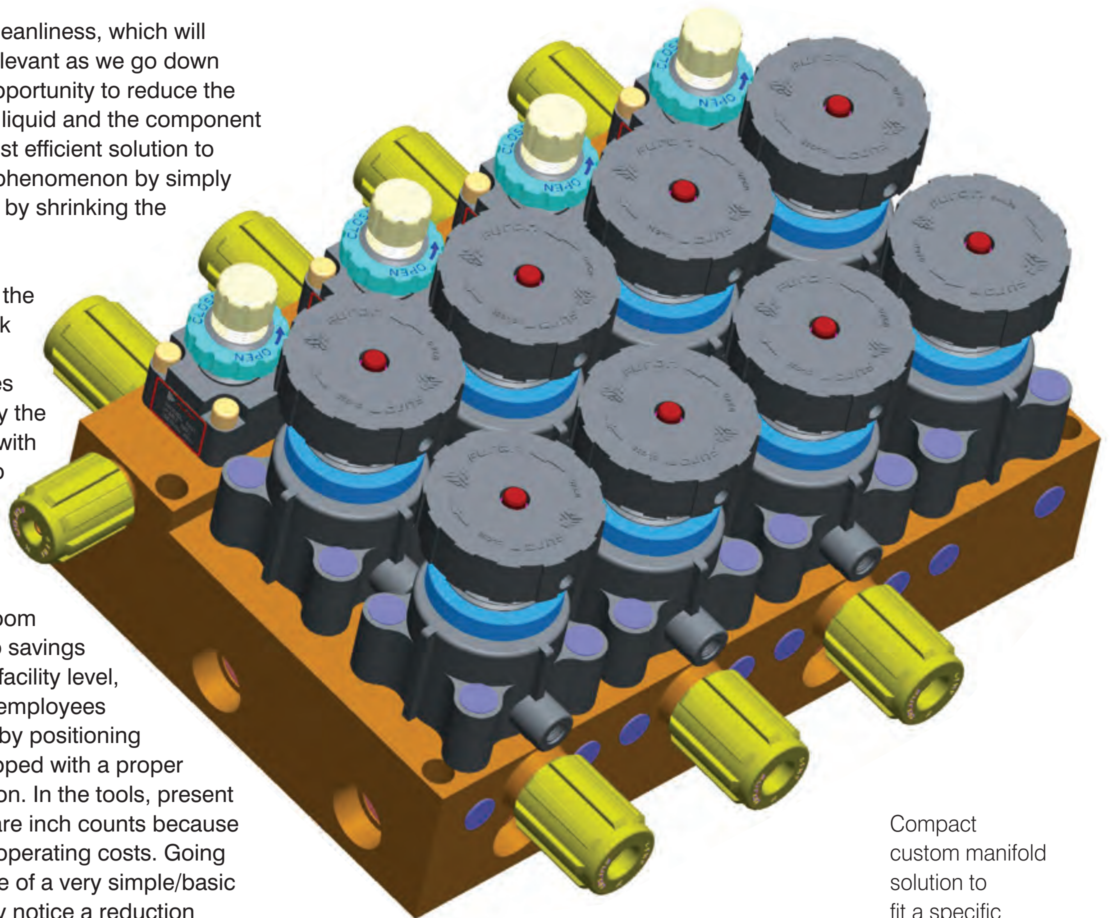
Another advantage related to safety, though less obvious than previously described, derives from the fact that when we are designing these manifolds, we (under our hat of component experts) can choose products that have the same level of performance and operating factor. Generally, this specific selection offers longer life time for components as they are installed in proper condition of use.

Following the same logic as above, but this time related to cleanliness, when we design a manifold based on a customer-specific requirement, we also ensure that from a cleanliness and SEMI standard point of view we are using components that belong to the same category. Cleanliness of a system is also directly related to the number of connections that are present in your design, as all connection points are equal to a potential entrapment point regardless of how good a fitting may be or a weld may be. So removing connection points turns your system into a cleaner system even if you are using the best connection system.

Additionally, given we are designing a custom component; we know how it will be installed (orientation), its purpose and most likely the carried liquid. Thanks to this information, we will be able to minimize entrapments zone (which is often a plague in slurry applications) as we will know how the fluid will have to flow through this given device. Based on the same logic but for a different application, we will be able to design the manifold in order to minimize potential dead volume, which is especially critical for analyzer systems.

A final comment regarding cleanliness, which will start to be more and more relevant as we go down in the printing node, is the opportunity to reduce the contact surface between the liquid and the component carrying it out, as it is the most efficient solution to limit the leaching/exchange phenomenon by simply reducing the contact surface by shrinking the component design.

As we have just seen above, the feature of being able to shrink the design of a given set of components actually provides a double advantage. Not only the one mentioned here above (with improve cleanliness) but also by allowing you to reduce your cost of ownership. If you manage to shrink down a design both at the facility level as well as in the cleanroom there is a direct translation to savings that can be achieved. At the facility level, it allows you to protect your employees as well as the manifold itself by positioning it in compact valve box equipped with a proper sensing system and ventilation. In the tools, present in the cleanroom, every square inch counts because of their high installation and operating costs. Going back to our previous example of a very simple/basic manifold, once again we may notice a reduction of over 60 percent, but this time in terms of the component's foot print.

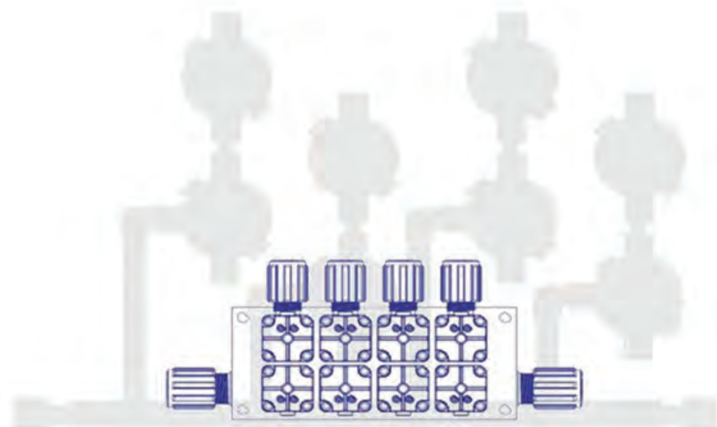


Compact custom manifold solution to fit a specific customer's needs

Manifolds also provide you significant savings if you are an end user or if you are an OEM. For the end user, this is mostly related to the maintenance/service of your installation. The first reaction that we may have is due to the fact manifolds prevent you from having discrete items, the cost impact on your maintenance may be larger. However if you look at the total cost of ownership, working with manifolds may allow you to generate significant savings. Because it's only a few components that you have to keep in stock, you are sure to always have the right parts, whereas if you are running discrete components the one that you will need to replace will always be the one you are missing.

In addition, when you are changing such a manifold it's like you are renewing the full subsystem at once and prevent to have multiple down time on components that are facing the same wearing phenomenon which may lead to potential need for replacement in a similar time frame. For the OEM, you receive a full small sub-unit that has already been assembled and tested which saves time and money related to hook up & plumbing. Also it allows you to be more nimble to address fast installations for the customer when you have a full fab install to do, using manifold design vs discrete components may save you hundreds hours of labors. The benefit to using manifold design is it enables you to get a custom answer to your unique needs. Understandably that the initial cost difference between discrete components and manifolds might be seen as a barrier to go toward this specific technology; however if you compare the cost of ownership of the two solutions inevitably you will realize that manifold systems are more economic and at the same time provides you premium benefits such as safety and cleanliness.

At Saint-Gobain we have seen numerous customers who were reluctant to make the move but once they did, they embraced this different approach by looking at the overall benefits package provided by a manifold.



How manifolding may impact a component's overall size.

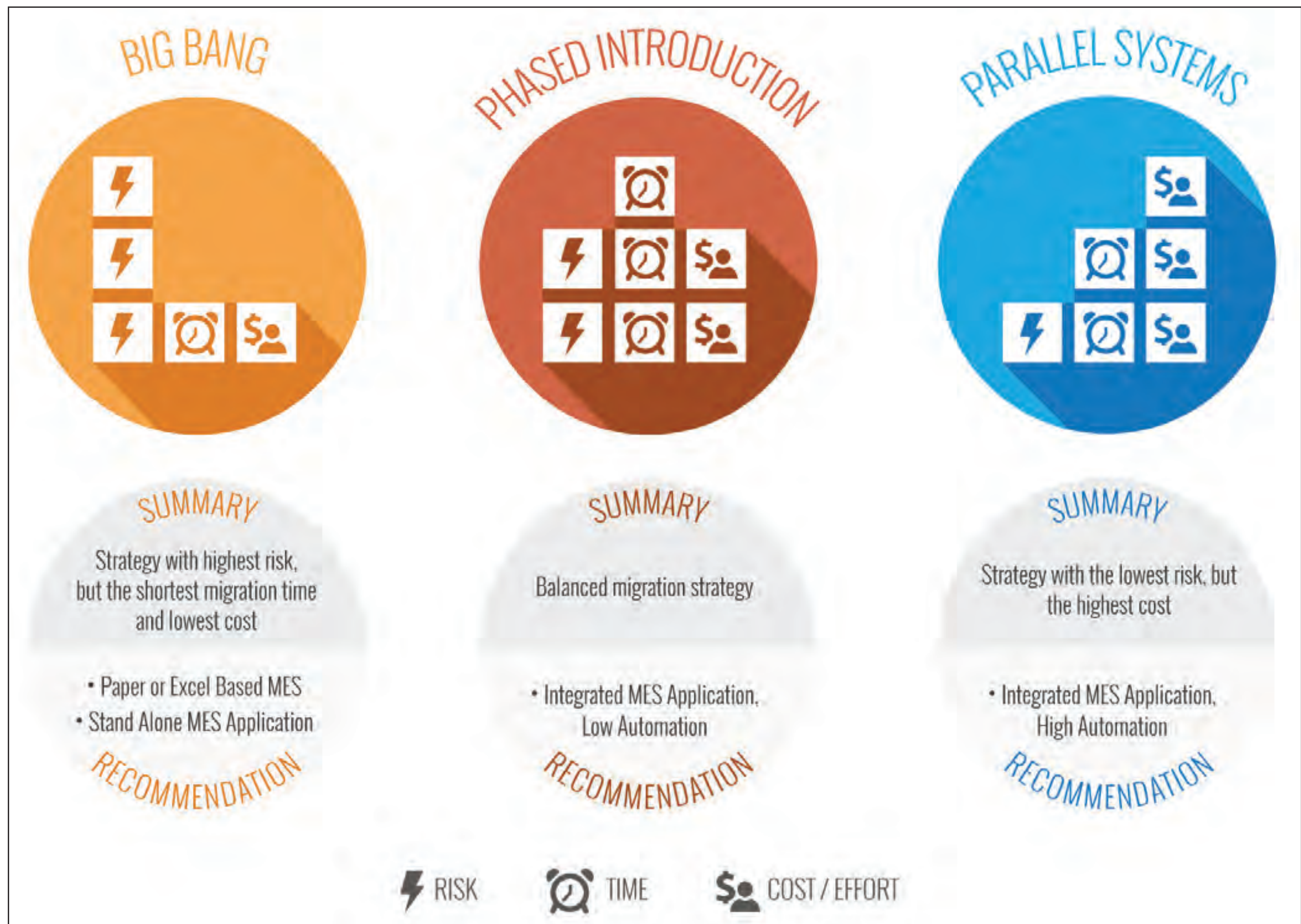
There are numerous reasons why manufacturers don't change their Manufacturing Execution System (MES) but, in many cases, there are also many reasons why they should. One of the biggest obstacles to change is risk. The very nature of an MES system means that it is at the heart of the manufacturing process. Francisco Almada Lobo, CEO, of Critical Manufacturing explains why companies should consider a change and what needs to happen for successful migration?

MES MIGRATION: Don't put your head in the sand

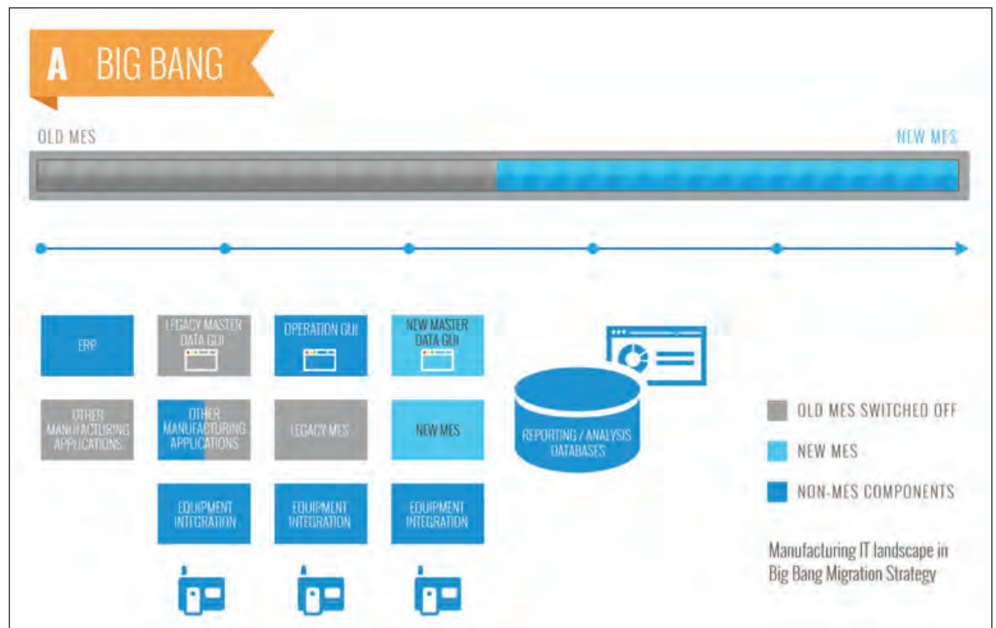
MANUFACTURERS in high tech areas of production, such as semiconductor, were early adopters of MES technology. The concept bought a great deal of benefit to their sophisticated manufacturing processes. As time has moved on, these systems have been adapted to changing needs with upgrades and add-ons that were often proprietary. This has left some production plants with a creaking MES based on hardware and software that is at the end of its life.

The system, however, is such an intricate part of the plant that the thought of replacing it is a very scary option with risk, time and overhead costs that may be perceived as unacceptable. But nothing lasts forever and not upgrading the system may bring real peril to the future of the business. An old MES solution may limit the ability of a company to be competitive today and into the future. Increasing overheads for maintenance will be accompanied by a growing inability to adopt new technology choices that can increase productivity, reduce costs and improve quality. With changing market trends towards the demand for smaller batches of higher mix products with more customised, individualised solutions; getting left behind could be a very costly mistake. In the semiconductor industry, most systems have been in place for over 10 years with some even dating back more than 20 years. Legacy MES constrain evolution and limit effectiveness with the main areas of concern being realistic modelling of the processes, comprehensive rule enforcement, functional coverage, integration and usability. These limitations can compromise traceability, precise control of processes, product quality and productivity. Old MES also inhibit producers from capturing the benefits of major technological advancements in recent years. These include mobile computing; 3D and augmented realities; advanced statistical process control models; advanced data analysis software with the ability to even predict production scenarios, and the use of 'Big Data' to gain greater understanding of processes, costs and issues. These technologies are driving production efficiency to new levels; increasing the speed with which new products can be introduced and fostering greater innovation.

For sure, production can be so dependent on an old MES that the thought of turning it off will give most production managers sleepless nights, particularly in high tech industries. However, the benefits of migration are huge and the cost of not changing equally risky. Staying with an old MES can only be a short term solution and can only lead to increasingly onerous end of life support, high maintenance, rising costs for modifications and a distinct lack of agility to meet changing production and market demands. With



the correct planning and support MES migration to a modern solution that will protect the future of a business can happen smoothly.

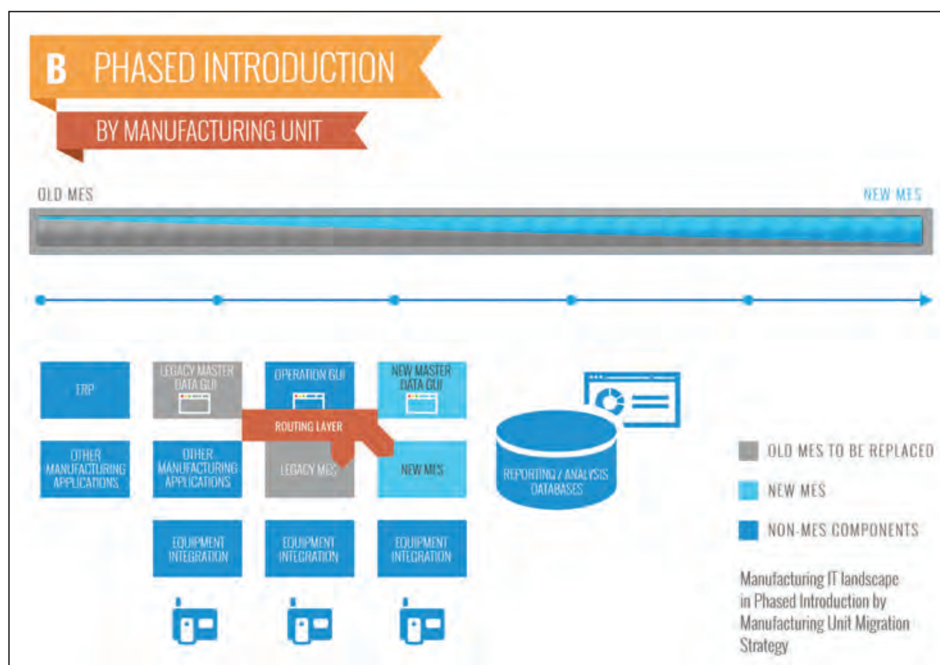


Manufacturing IT landscape in Big Bang Migration Strategy

MES selection

As with any project, the first step of considering a MES migration is to evaluate the return on investment. Along with understanding the costs and limitations of the legacy MES, this requires a definition of the migration scope, target and strategy. The process starts with selection of the migration project team and choosing the best MES system for the application. A project team needs manufacturing and MES knowledge but should also include someone with migration experience to help foresee and resolve challenges that the project may encounter. For system selection, shortcomings of the current MES need to be assessed and the functionality of new systems compared with the needs of the plant.

The new system should have high levels of flexibility to ensure it meets future as well as current business needs. It should include modelling possibilities for materials, equipment, containers, product structures, flows, steps, data collection. There is also certainly no point in upgrading a 15 or 20 year old system to a 10 year old one. A new system should support the plant for a minimum of 10 years. The ability of a new MES to help with the actual migration process by being able to mimic the legacy MES is also a consideration.

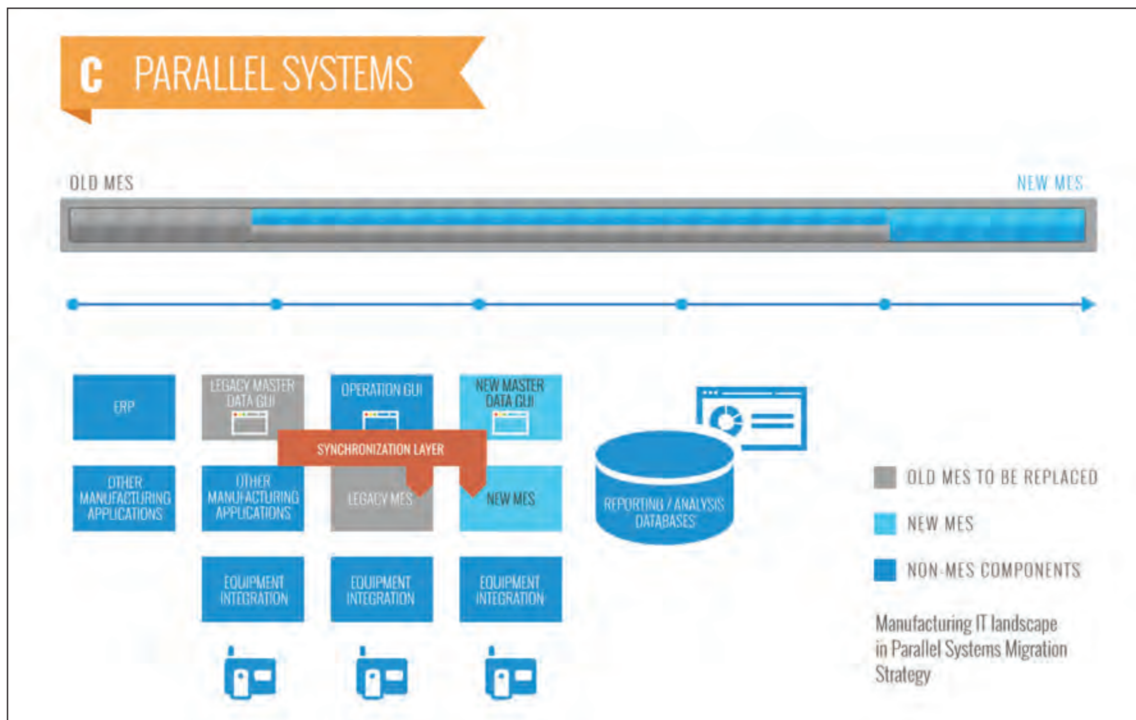


Manufacturing IT landscape in Phased Introduction by Manufacturing Unit Migration Strategy

Migration strategies

The migration to a new system can be carried out in a number of ways, each with varying levels of risk, cost and time. These include 'Big Bang', Phased and Parallel approaches. Big Bang is the fastest and lowest cost option with the legacy system being turned off and the new MES turned on. This single point switch over, however, also carries the highest risk as the offline testing phase of the new system may not re-create all live conditions of the plant or cover all inter-dependencies. Phased introduction of a new MES involves introducing the system into parts of the production process while leaving the old MES supporting other areas. These phases may be by manufacturing unit, MES function or by product lots. This approach reduces risk as confidence in the new system increases over time and parts that have been migrated can be rolled back if problems occur. This strategy does involve higher costs than the Big Bang approach, however, as routing layers and migration procedures are required to ensure the two systems work in harmony across the plant. It also costs the most in terms of time to fully implement the new system with many small migration phases.

Taking a Parallel approach puts both systems online at the same time, working in a master and slave configuration. When confidence is built that the new MES is operating successfully, it can be designated as the master and the old system switched off. This is the lowest risk approach as any problems that are encountered can be handled by the legacy MES. The time taken



is also shorter than a phased approach. A parallel migration, however, carries the highest costs as synchronisation layers with orchestration logic need to be designed and implemented at application layer and, as data is duplicated in both systems, at the ETL (data extraction) routing layer.

There is no right or wrong migration strategy and the process selected is highly dependent on choosing one that fits the needs of the plant. This includes the level of risk that is acceptable and the amount of investment a business is willing to put into the project. Assessment of complexity of interdependence and interaction with other systems and applications; level of automation, and impact of downtime will also guide the choice of strategy for migration. While each migration project has its own individual challenges, and is highly dependent upon the application, in very broad terms the Big Bang approach is more suitable where there is no integrated MES (maybe a paper based system is still being used or the MES is a stand-alone application). A Phased migration may lend itself more to integrated MES with low levels of automation. A Parallel migration is a good option to consider where there is an integrated MES with high levels of automation.

Migration planning

Whichever migration strategy is selected, the project will need to follow a number of steps. The phases of the project go through Definition, Preparation, Execution and Closure. Definition of the migration provides the groundwork for a successful project. Steps include capturing the current system landscape, defining the future landscape and determining how the migration will happen using the selected migration strategy. The Preparation phase then covers the tasks need for the following Execution phase to go ahead. This includes activities such as configuring, modelling and customizing the new MES; adapting applications to accommodate data migration; testing and validation of the new system, and even rehearsal of the migration execution. The Execution phase is highly dependent upon the effectiveness of the Definition and Preparation stages. It involves the roll-out of the new system as defined in earlier parts of the project, monitoring of the new system to ensure there are no glitches and shutdown of the routing and synchronization layers installed to enable the migration.

Finally, the Closure phase closes down the project and decommissions unnecessary hardware and software. It includes archiving data from the old MES and may incorporate the activation of new functionality in the installed MES.

Summary

Let's be clear – migration to a new MES is a complex undertaking, especially in highly automated industries. Where current MES are old and present a risk to the future of a business, however, ignoring the issues they have will not make them go away. Inevitably outdated MES will need to be replaced and leaving them in place for longer simply adds to the risk and complexity of a migration project. With the correct planning and expertise, MES migration can happen smoothly even in complex, high volume manufacturing environments. Although payback is not a short term view, modern MES systems can deliver enormous benefits to medium and long term business strategies. Their implementation should certainly be considered before legacy systems become critical and the competitiveness of a business is compromised.

WIRELESS CHARGING POISED TO GO THE DISTANCE

The benefits of wireless battery recharging over a distance appeared about as likely as jet packs and flying cars until Dialog Semiconductor and Energous Corporation began their quest to cut the cords.

WHILE CONSUMERS clearly love their smartphones, laptops and tablets, they equally detest the tangle of power converters and charger cables cluttering backpacks and briefcases from Bristol to Burbank. This love/hate relationship could be about to change if power technology companies Dialog Semiconductor and Energous Corporation successfully deploy their new WattUp® family of wireless charging solutions.

Wirelessly recharging mobile device batteries is hardly new. Existing wireless solutions typically employ coils to carry power to receiving devices; however, these have their limitations. According to Dialog Semiconductor's Senior Director of Corporate Strategy, Mark Hopgood, it is precisely those limits that make the solutions developed by Energous Corporation with support from Dialog so compelling. Without charger mats, precise alignment or other persnickety requirements, the WattUp solution offers benefits that Hopgood says consumers expect: no clutter, and more importantly, no wires.

"I think wireless charging has not lived up to a lot of consumers' expectations. In some cases it can be downright frustrating to find that your device has not charged because it wasn't placed quite right on the charging mat. We believe this new solution is much closer to consumer expectations – it will be a difference they appreciate when it comes time to buy," Hopgood said.

Dialog traces its roots back to 1981 and included times as a Daimler Benz AG subsidiary infused with CMOS and semiconductor technology from Silicon Valley's International Microelectronic Products company; its expertise in power management electronics later extended into smartphones incorporating ARM processors. Work with LED power technology and sensors were later added as the company grew to multiple locations in the UK, Europe, Asia and the US. Dialog's broad power-focused market appeal eventually led to a relationship with Energous Corporation that began in 2014 and was formalized with a partnership and cash infusion of (USD) $10 million in 2016 to support Energous' development of its WattUp wireless technology.

Energous developed its WattUp technology that provides over-the-air power at a distance as an alternative to existing wireless recharging techniques including those of other AirFuel Alliance members. Although Energous and Dialog stress the wireless

aspect of their technology enabling recharging at a distance, WattUp could be employed to create near field charging mats, but without the precise placement requirements some consumers find challenging. Both companies believe most consumers will realize additional benefits as longer-distance charging applications become available, such as deciding when a device is 'refueled.' Consumers can choose priority devices for recharging, or let anything properly equipped sip power as needed. WattUp receiver technology can be incorporated in a very wide range of consumer products that can ultimately be charged from various types of WattUp transmitters.

Even if WattUp devices are positioned in a wireless recharging mat in a near field application similar in appearance to existing systems, Hopgood said Energous' core technology has important advantages. "One of the things we looked at comparing coil based tech vs. Energous (WattUp) was the fact that the receiver coils tend to require a large diameter and an added physical dimension—a 'z' height thickness. Because of this, (coils) are often too big to be integrated into many products that could benefit from wireless charging. But if we reduce the footprint at the device level—which WattUp technology does, this translates into the antenna becoming nothing more than the tracking on a PCB; we can even use the same antenna for charging that you would use for Bluetooth," Hopgood said.

Besides eliminating the coil that other wireless charging technologies depend upon, Hopgood said Dialog and Energous have worked to move from discrete components to integrated semiconductors that further reduce space and increase efficiency. At the same time, WattUp software is designed to ensure that charging waveforms are dynamically directed, focused and controlled via proprietary algorithms; for mid field and far field charging applications consumers can choose various control options including recharging when electricity rates are lowest.

Dialog and Energous have moved forward with their plans to further miniaturize key component technology with the announcement in January of their first jointly produced integrated WattUp wireless power transmit (Tx) IC, the DA4100. This new System-on-Chip (SoC) integrates an ARM Cortex-M0 along with RF power generator, power management and secure element functionality into a single 7x7mm device. It also features on-chip DC-DC conversion and

M	=	a * p * v * t * + C						(y = mx + c)		
Material Removed (µm)	=	Constant	*	Processing Pressure (g/cm2)	*	Plate Speed (rpm)	*	Processing Time (mins)	+	Constant

embedded software, providing seamless integration to Dialog's SmartBond™ family of highly integrated, low power BLE SoCs. The new DA4100 minimizes board space needed to implement, enabling smaller charging transmitters and simplifying overall design-in requirements. Gordon Bell, VP of Marketing at Energous, said that the DA4100 is the backbone of all WattUp transmission designs including the near field transmitter that the US Federal Communications Commission (FCC) recently approved.

"We are engaged with a large number of product companies currently looking to incorporate the WattUp receiver technology into their devices. These companies would typically bundle a WattUp near field transmitter along with their product to offer devices that are charged wirelessly," said Bell.

Bell elaborated that while many end use designs are possible using WattUp receiver technology, Energous and Dialog expect that WattUp-enabled transmitters will most likely appear in future consumer markets focused on two primary applications: standalone and embedded transmitters.

"Standalone transmitters have a single function to allow for wireless charging to WattUp-enabled receivers. A standalone near field transmitter would likely be a small charging pad included inside the box of many small electronics (replacing the USB cord and power brick typically bundled inside today). A standalone mid field transmitter may be incorporated into the dashboard of a car or may be a small device that sits on your desktop, allowing for charging in the 2-3 foot range. A standalone far field transmitter may look similar to a Wi-Fi access point installed on the wall or ceiling, allowing for wireless charging at up to 15 feet," Bell explained.

"Embedded transmitters would be part of another product. For instance, the near field transmitter technology may be embedded into the top of a Bluetooth speaker, allowing you to charge small electronics simply by placing them on top of the speaker.… A desktop assistant type of product may offer mid field WattUp charging to other devices nearby. And the bezel of your TV may one day offer far field WattUp (utility), charging its own remote control, game controllers and other devices within 15 feet of your TV. All of these implementations would use the DA4100 as the backbone of the wireless charging function," he concluded. As the WattUp technology moves from development stages to design-in with lead customers, Dialog's Mark Hopgood said that the change from coil-based wireless charging approaches and other technologies to antennas working with directed RF signals will affect consumer purchasing. The degree to which a consumer has adopted mobile devices and uses them away from mains power supplies could be decisive.

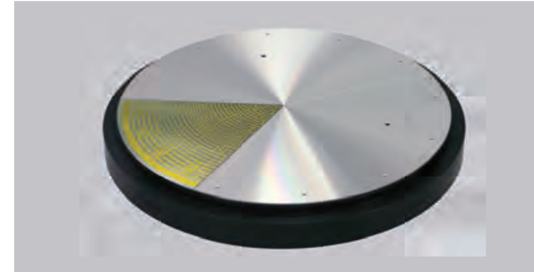
"There are so many gadgets that are a slave to a socket; WattUp technology has the potential to change the way we use our battery powered devices…let's look at near field; at face value one might think that our technology doesn't really add much advantage, but actually when you go from a coil to an antenna based system, you dramatically reduce the footprint and the cost, so just doing that opens up a whole new category of devices. Also, RF is less precious about positioning the device on the charge mat.

"The paradigm shift may occur that when you are using a device, you are sending just enough energy over the distance (using WattUp technology) to keep the devices topped-up. This could be done constantly…so you can reduce the size of the battery, or you can simply not worry about charging them again by keeping them under a managed constant charge. That is where the paradigm shift will occur that the consumer will appreciate," he concluded.

While both Dialog and Energous could not share details regarding the original equipment manufacturers that are currently working to incorporate WattUp technology into future end user devices, they did indicate that product sampling and qualification tests were underway. The companies expect consumer devices incorporating WattUp wireless charging may begin appearing in some global markets later in 2017.

WATLOW® SEMICONDUCTOR

Watlow's Thermal System Solutions Enable Next Generation Technology



Watlow® offers:

- Precision designed heater circuits embedded in ESCs and chamber components
- Innovative solutions for gas line heating
- Thermal system integration with heaters, sensors and controllers
- Analytical, FEA and CFD capabilities
- Over 12,000 square feet of cleanroom manufacturing

Powered by Possibility

Visit us at **SEMICON® WEST** *booth #5344, and ask us about our new ATS technology.*

For more information visit our website at www.watlow.com

EQUIPNET

DELIVERS PROACTIVE ASSET MANAGEMENT

Dedicated asset managers offer a means to deal more effectively with the equipment implications of mergers, closures and start-ups across ever-changing global chip markets. By: Mike Zunino, Director Semiconductor at EquipNet Inc.

COMPANIES across the semiconductor industry now more than ever are taking advantage of second-hand capital asset management to reap the benefits of identifying, tracking and redeploying equipment internally, as well as to buy and sell major assets. Using software programmes for the internal redeployment of capital assets helps to avoid the cost of purchasing new equipment and provides a return on the original investment of idle surplus equipment and support spares. The program also creates significant savings by buying secondary equipment. With the high demand and cost of new semiconductor equipment, purchasing assets from secondary markets can help to save time and money and still maintain the high-quality standards of having such machinery on production lines.

This article considers the revolution of tracking and redeployment systems within the semiconductor industry, as well as the wider benefits of proactive asset management. It will also focus specifically on the LED market as a perfect example of a key secondary user segment that has benefitted tremendously in cost avoidance.

The semiconductor market has been through a vast amount of change over the past few years in the form of mergers and acquisitions. In many cases merging companies find that assimilating capital assets creates a distraction from daily business responsibilities. This disruption comes from having to determine the machinery to keep and sell along with establishing the roles and responsibilities of executing sales or repurposing capital equipment. It is commonplace for an organisation to take several months to identify and sort through assets before this is finally resolved.

The challenges they face include decision making, asset configuration and capability review, as well as financial responsibilities and buyer discovery as well as project management for excess equipment sales. This pull on the merged company's focus can become so distracting that leaders miss important marketplace opportunities. These challenges can be made more difficult when factory closures occur, which can often lengthen the process to up to a year or longer. So, at the time of a merger or acquisition, professional asset management is crucial to ensure a smooth transition. It allows full understanding of each company's capital asset inventory without having to commit resources from both the acquiring and acquired companies to obtain detailed information concerning all equipment now jointly held.

A revolutionary method

Asset management companies fully understand the issues of professional equipment and instrumentation management, with first-hand experience of work with major semiconductor companies. These professional asset managers have created an all-encompassing solution to this issue. EquipNet's bespoke solution to managing complex equipment issues includes its

Asset Redeployment Management System (ARMS). EquipNet deploys a trained and experienced team to a company's facilities to fully document all current excess equipment, including idle production, lab, metrology, test and measurement and even facility support equipment. All the information is uploaded to the ARMS software program (see Figure 1) that is fully customized to a client's requirements and only accessible internally by authorized departments and personnel. Clients are able to obtain full visibility of asset configuration details, location and a current status of their assets 24/7, allowing them to make real-time decisions for redeployment between sites, as well as list assets for remarket, sale or auction. With ARMS, once a decision is made about an asset's disposition, EquipNet's Global Logistics department can arrange crating, shipping, exportation and importation documentation for the final destination—all through the simple click of a button.

Furthermore, there are a number of important additional asset management requirements provided by EquipNet. For example, EquipNet assigns a dedicated Project Management team to each client. This team provides current market values to the client, as well as coordination of de-installation, rigging, relocation and installation, post sale management, as required, handling all requirements up to and including full site closures.

An example of how EquipNet is continuing to expand its support to clients is its acquisition of Quality Equipment Source, Inc. (QES), a refurbishment and repair facility in San Jose, CA. Additional end user requirements can now be performed through this newly acquired facility, and with the QES team joining forces with more than 170 EquipNet employees worldwide, the company is fully capable of managing any business's asset requirements regardless of size or location. EquipNet combines the skills of appraisal, brokerage, and auctioneering of instrumentation and equipment, as well as the de-installation and re-installation of equipment, rendering it a one-stop-shop for companies working in the semiconductor industry. Why use an asset management program?

In recent years, there have been a number of issues in the secondary equipment market due to the amount of start-ups and companies entering the instrumentation auction market. End users can often find themselves faced with conflicting information regarding equipment market values and the availability of instrumentation. 'Ghost markets' have been created, with multiple companies representing and advertising pieces of equipment that are owned by only one of these businesses. This can drive down the market value of equipment since the practice makes it appear that there are multiple assets available; this can also set future market value precedence for all similar makes and models of equipment.

EquipNet staff package and load process tools located in an Idaho (US) fabrication facility to another location in the United States

Ghost markets can also cause a problem for end users seeking to purchase a piece of equipment in the secondary market. Without direct access to the seller, companies find themselves paying over the odds for equipment and instrumentation. An example of the problems that buyers and sellers face include an end user that was purchasing a piece of equipment through the secondary market that later discovered they had purchased one of their own pieces of excess equipment from another of their sites.

Using an asset management program informs the buyer of the location of equipment that is for sale as well as identification of the seller. Programs also provide other critical instrumentation facts such as specifications and warranty details. Furthermore, asset management providers implement critical

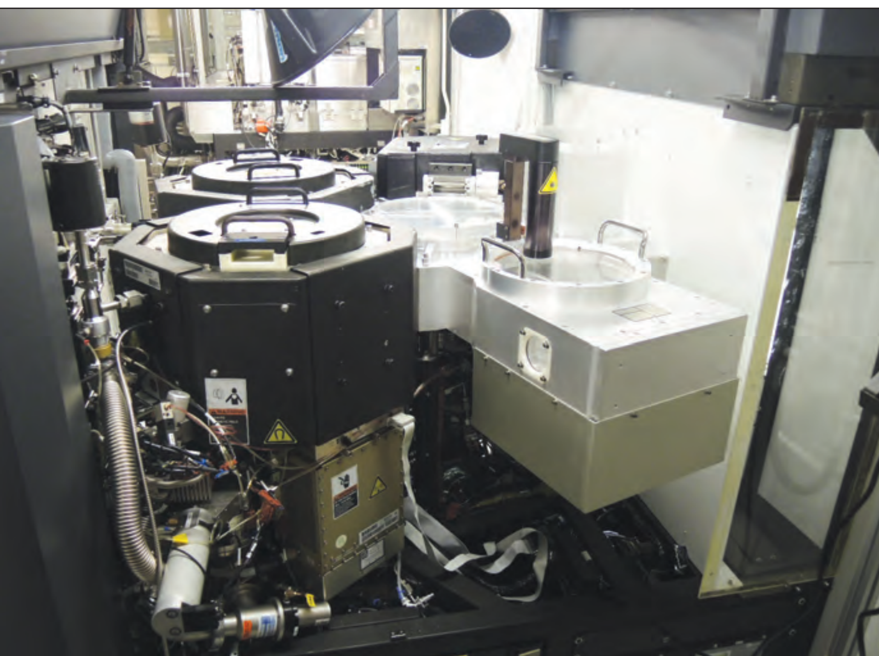
Unfortunately, for some buyers many of the larger semiconductor companies have already scrapped a vast amount of their legacy equipment due to the limited buyer base prior to LED manufacturing's ascendency, which has often left manufacturers seeking quality, smaller format equipment scrambling for process tools at affordable prices

services such as refurbishment and installation. It is therefore important that end users have the confidence to use an asset management provider, giving them the experience, transparency, reliability and trust they need when dealing in the secondary equipment market.

The LED solution

With the LED market growing worldwide, the demand for 4-inch (100mm), 5-inch (125mm) and 6-inch (150mm) manufacturing equipment has also increased dramatically. Because many of the largest semiconductor manufacturers converted to 8-inch (200mm) or 12-inch (300mm) wafer processing equipment, the process tools for handling smaller size wafers went into the secondary equipment market or were scrapped, which meant that with the advent of LED manufacturing and its smaller size wafer requirements, the demand for legacy 6-inch equipment has begun to increase.

Unfortunately, for some buyers many of the larger semiconductor companies have already scrapped a vast amount of their legacy equipment due to the limited buyer base prior to LED manufacturing's ascendency, which has often left manufacturers seeking quality, smaller format equipment scrambling for process tools at affordable prices.



EquipNet staff relocated this Applied Materials P5000 chemical vapor deposition (CVD) tool in Wales (UK) to a manufacturer's facilities in China.

Today, the demand for legacy processing equipment is high, with more semiconductor products including power devices, MEMS and IGBTs using this technology. Proactive asset management companies, such as EquipNet, continually monitor and provide clients with real time market analysis and industry trends to help them handle both the buying and selling decisions of such legacy processing equipment. This can have a positive impact on their financial bottom line and help buyers to obtain rare and in-demand instrumentation.

Conclusion

Due to the current upsurge in semiconductor mergers/acquisitions, site closures and downsizings, it is crucial that companies have accurate asset information readily available to them. Asset management and redeployment services have been crucial to the success and growth of other industries including biotech, pharmaceutical and wide-ranging consumer product manufacturing over the past 15 years; those same services are now being offered to the semiconductor industry. A team of industry experts that understand the requirements of end user semiconductor companies can empower their clients with services including capital asset redeployment, logistics, refurbishment, repair, installation, purchasing, sales and market evaluations.

Asset management solution providers offer manufacturers critical services to maintain accurate information about the value and location of major capital assets. Programmes such as EquipNet's ARMS enables these businesses to focus on what they do best—producing products—without taking on the added responsibilities of managing excess capital or engaging directly with the secondary equipment market. Surplus asset management allows buyers to acquire good quality, second-user semiconductor equipment, whilst sellers can obtain a good return on their initial investment, hassle-free. With over 170 employees worldwide in North America, Latin America, Europe and Asia, EquipNet can directly support any company's requirements, regardless of size, to provide maximum returns without exhausting internal resources.

PASSION. PRECISION. PURITY.

NEW VAT BUTTERFLY

ULTRA-FAST ACTUATION IN A TENTH OF A SECOND – HIGH THROUGHPUT

- Position only control version – ideal for simple throttling applications
- Sealing and non-sealing type
- Heater options

www.vatvalve.com

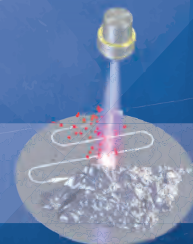
HIGH-END EQUIPMENT
FOR HIGH-TECH INDUSTRIES

IonScan

Systems for ultra-precise film thickness trimming and ion beam figuring

- Contactless trimming or figuring
- Optimization of error distributions by the factor of 10 and more
- Ion beam process applicable to almost all materials

Ion Beam
Technology



Visit us at SEMICON Europa
November 14-17, 2017 in Munich/GER
Booth B1-1815

www.meyerburger.com

RARE GASES IN ELECTRONICS THE NOBILITY OF THE GASES WORLD

Rare gases offer unique properties essential to advanced semiconductor manufacturing. Linde Electronics explains the role they play in everything from chip making to IoT sensors and beyond. By Sahir Khan (left), Global Product Manager, Linde Electronics and Paul Stockman (right), Head of Market Development, Linde Electronics

RARE – OR NOBLE – GASES, which constitute less than 1 percent of the total air in the earth's atmosphere, play an essential role in the world of electronics manufacturing. These chemical elements make up column 18 of the periodic table, which includes helium (He), neon (Ne), argon (Ar), krypton (Kr), xenon (Xe), and radon (Rn). The term rare denotes that they were first identified as being different from oxygen, while the term noble is an analogy to the inertness of noble metals like gold and platinum.

Chemists group rare gases in the last column of the periodic table because they all have completely filled outer electron shells. This renders them nearly non-reactive and means they exist as gases at ambient conditions, even for the heaviest among them.
Rare gases have unique properties that make them indispensable in electronics manufacturing processes. In this article, we will explore their history, properties and applications, production and supply chain, and market.

History

Sun god, New, Lazy, Hidden, Stranger: the direct translations from the Greek for helium, neon, argon,

Helium tube trailer

krypton, and xenon denote the elusiveness of these elements from discovery. Due to their evasive qualities – inert, invisible, gaseous, sparse – the rare gases remained undetected during much of the period of chemical enlightenment of the 18th and 19th centuries. In fact, the location of the first real identification of a rare gas in 1868 was not on the earth at all, but rather from the spectral discharge of helium in the sun.

However, technology quickly enabled a rapid progress in understanding (Figure 1). Building upon earlier scientific and commercial successes with refrigeration, Carl von Linde developed the first apparatus for the liquefaction of air, which was patented in 1895.

While preserving the commercial benefits, Linde also realized the scientific impact of this technology, and distributed early prototypes to major academic centers across Europe. Within 10 years of this technical breakthrough, all five rare gases were isolated and identified, culminating in Nobel Prizes in 1904. Moreover, their discovery was essential to the formulation of the periodic table by Dimitri Mendeleev, and indeed modern atomic theory.

Properties and applications

Properties. The complete, outer electron shells of rare gases are not only an organizing nomenclature for the periodic table, but they also underlie the physical source of key properties associated with these molecules. Essentially similar electronically, rare gases are differentiated among themselves by their mass. Here, we describe four properties important to supporting electronics manufacturing.

- **Inertness:** Foremost among the properties utilized from rare gases is their inertness to chemical reaction. This is why the analogy to noble metals was made by early researchers, noting their lack of oxidation under the most extreme conditions. The complete electron shells mean that these molecules are already at their lowest chemical energy potential, and no reactions with other atoms will improve upon their energy state. Because many of the applications in electronics manufacturing are highly energetic, rare gases are relied upon as an inert medium for conductance of mass, heat, and light.
- **Ionization potential:** Ionization is the removal or addition of electronic charge to an atom or molecule; ionization potential is the energy required to accomplish this charging. Relative to similarly

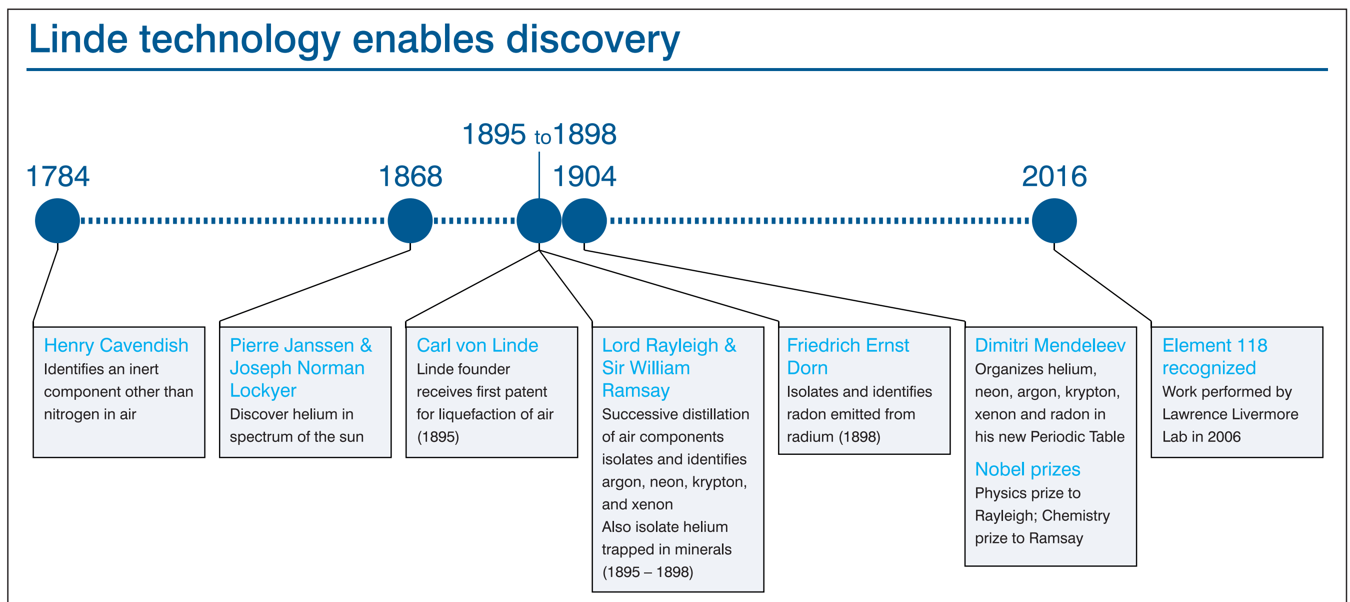


Figure 1. The development of air liquefaction technology by Carl von Linde catalyzed a decade of rare gas discovery, culminating in the organization of the periodic table by Mendeleev and the award of two Nobel Prizes.

massed atoms, rare gases have very high ionization potentials due to their complete electron shells. This allows them to remove or conduct electronic charge efficiently to other atoms and molecules. Helium has the highest ionization potential of any atom or molecule.

- **Thermal conductivity:** Atoms and molecules have different rates at which they conduct heat energy, and this is quantified by their thermal conductivity. Helium, as well as hydrogen, have the highest thermal conductivity among gases, which is due to their low mass. Because of the high-energy reactions of many electronics manufacturing reactions, the combination of high thermal conductivity along with inertness means helium is often used to quickly change the temperature of objects.
- **Mass:** Mass itself is an important property for rare gases. Matching the mass of the rare gas to certain mechanically-enabled applications, again along with their inertness, means the selection of a specific rare gas can optimize outcomes.

Applications. Rare gases are used throughout the wafer substrate and device manufacturing process chains. Here we briefly describe some of the more common applications using rare gases, and show how they are associated with individual rare gases and their properties in Figure 2.

- **Backside wafer cooling:** Helium is often used to control the temperature of wafers and sometimes glass substrates in display manufacturing. This is becoming increasingly important as thermally sensitive, low temperature deposition and etch processes are adopted.
- **Loadlock cooling:** Likewise, helium is used to cool wafers between process steps.
- **Carrier gas:** Helium, and sometimes argon, are used to entrain and transport less volatile chemicals – ordinarily liquids at ambient conditions – into the reaction chamber.
- **Plasma:** Argon, and sometimes helium, are used to support plasmas in deposition and etch processes due to their high ionization potential and inertness.
- **Silicon ingot production:** Nitrogen is reactive to silicon at its melting point of 1414°C, and so argon is used instead to inert the surfaces of the molten silicon and newly formed ingots.
- **Cryogenic cleaning:** Microscopic aerosols of liquid argon have found use to clean delicate, high aspect ratio structures in advanced semiconductor manufacturing.
- **Excimer laser lithography:** Deep UV laser lithography has been used for 20 years in high-volume semiconductor manufacturing to pattern critical layers of devices. Laser gases are mixtures of 98+ percent neon with other rare gases (argon, krypton, and xenon) and halogen (usually fluorine).
- **Sputtering:** Sputtering is the direct removal, or indirect deposition, of material. The process is initiated by the physical impact of gas-phase atoms or molecules upon solid surfaces. By selecting a rare gas of similar mass, sputtering yields can be optimized.
- **Etch:** Rare gases are used to mediate etch reactions. Xenon is used in certain high aspect ratio etch applications for its combination of ionization potential and chemical inertness to adjust charge distributions in the etch reaction.

Production and supply

Cryogenic Distillation. Production and supply of rare gases are enabled by the same cryogenic distillation separation of air components pioneered by Carl von Linde more than 130 years ago.

The relative abundance of the components in air (Figure 3) and boiling points (Figure 4) indicate the cost to produce and availability to supply these critical materials to the typical 99.999+ percent purity.

Argon

Argon is the fourth most abundant gas in the earth's atmosphere. It is produced in air separation units (ASUs) alongside oxygen and nitrogen by means of secondary distillation of the liquid oxygen rather than from the primary distillation of air. Because the boiling point of argon is between that of nitrogen and oxygen, an argon-rich mixture is taken from a tray near the center of the distillation column and is further cryogenically separated. It can also be recovered from ammonia plant purge gas streams, which also process very large flows of air as an initial feedstock for nitrogen.

Neon, Krypton, and Xenon

Neon, krypton, and xenon are similarly obtained as by-products from the production of nitrogen and oxygen. Because the concentrations in air are miniscule, commercial quantities of crude products are obtained from only the largest ASUs with huge air intakes: on the order of at least 1,000 tons per day (tpd) oxygen capacity are needed. Neon has a much lower boiling point than nitrogen and oxygen and thus passes through the nitrogen distillation column unliquefied. This "light" stream is compressed and sent to secondary sites for further purification and packaging. Krypton and xenon conversely have much higher boiling points and are rejected from the oxygen distillation column as "heavy" waste. They are pre-purified at site to remove most of the oxygen before similarly being sent to secondary sites for further purification – including separation from each other – and packaging.

Helium

Helium is the most abundant element found in the universe after hydrogen, but it is relatively rare on earth. Helium is formed on earth as a result of the radioactive decay of thorium and uranium in the crust. It rises through geological fissures and accumulates in the same rock formations as natural gas. However, only certain deposits have concentrations high enough to be commercially viable, but which are less costly than distillation of air.

Commercial production of helium began in the United States as a strategic material spurred by the military applications for observation blimps during World War I. The primary commercial source for much of the 20th century was the Hugoton gas basin spanning parts of Kansas, Oklahoma, and Texas. During this period, the US government continued to treat the material as strategic, and excess crude material obtained as the by-product of natural gas extraction was stored by returning it to depleted reservoirs of permeable rock. Known as the Federal Helium Reserve and managed by the Bureau of Land Management (BLM) the reserve is in the process of being sold off under the Helium Stewardship Act of 2013 and this erstwhile primary supply will be tapered to negligible commercial impact in the near future. Meanwhile, significant new sources have been developed over the past few decades across the globe. The potential development of large sources in Siberia promises to continue to meet growing global demand.

Recovery

Due to their inert property, rare gases are not consumed, either by chemical change or incorporation into the finished product, during electronics manufacturing. Consequently, they are available in the waste streams from fabs, albeit highly diluted and contaminated. The technology to recover

Applications and Properties

	Gases					Properties			
Applications	Helium	Argon	Neon	Krypton	Xenon	Inert	Ionization potential	Heat coefficient	Mass
Backside wafer cooling	●					●		●	
Load lock cooling	●					●		●	
Carrier gas	●	●				●			
Plasma	●	●				●	●		
Silicon ingot production		●				●			
Cryogenic cleaning		●				●			
Excimer lasers		●	●	●	●	●	●		
Sputtering		●		●	●	●			●
Etch					●		●		

Figure 2. Specific and often extreme properties of rare gases result in their roles for essential electronics applications.

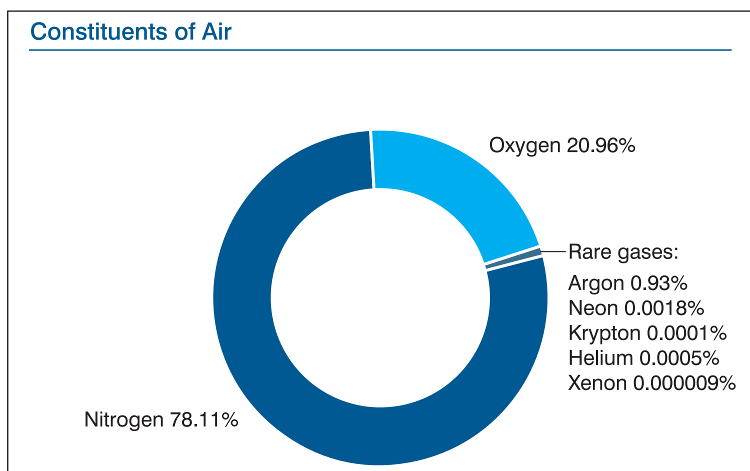


Figure 3. Rare gases are a small part of the atmosphere.

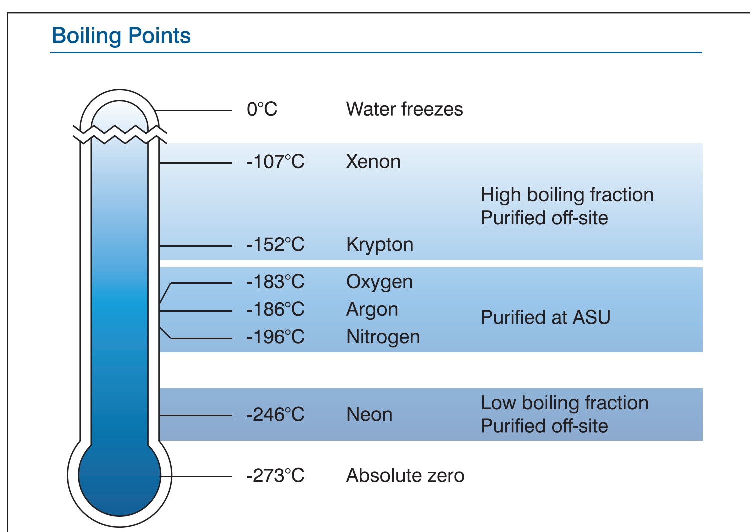
these materials is straightforward, with the potential to recycle them for electronics or other applications. However, as with most recovery processes, the choice to recover vs. supply with new material is made on the relative costs of the whole supply chain. Only the very largest use applications are candidates for commercially successful recovery.

Supply Modes. Rare gases are available in a variety of gas and liquid packaging, as indicated in Figure 5. These span from lecture bottle cylinders holding a few liters of gas to liquid bulk trucks for land and ISO containers for sea shipment of millions of gas-equivalent liters of product. Like most materials, the commercially viable transport cost is directly related to the value of the material (Figure 6). Because most rare gases are truly scarce, they are commonly distributed globally and generally independent of the geographic location of the source. The exception is argon, which is relatively inexpensive, and is produced in many geographies at large ASUs. However, it can be shipped regionally as supply imbalances dictate.

Figure 4. Extracting rare gases requires cryogenic distillation of large quantities of air.

Market

The demand for rare gases has grown substantially in the past few decades on the back of new applications both for electronics and non-electronics markets. Moreover, while the overall demand for these materials has experienced a more-or-less smooth upward trend, the underlying application basis has sometimes changed dramatically. For example, the development and rapid adoption of LED lighting has quickly eroded the market for halogen lighting and display signage. Likewise, the market for plasma displays as a successor to cathode ray tube televisions was short-lived and eclipsed by the introduction of LCD technology. Below, we take a brief look at the electronics market demand, as well as significant non-electronics applications. These market shares are summarized in Figure 7.



Helium

- **Electronics:** Electronics usage, which represented less than 1 percent of total global demand for helium, has grown exponentially to constitute more than 15 percent of the market demand today. The total demand for helium for a single fab can now exceed 200,000 m^3 per year.
- **Non-electronics:** Non-electronics applications include cooling in metal production and adoption of MRI scanners, whose superconducting magnets require liquid helium as a refrigerant. Fiber optic manufacture can also benefit from using helium as a coolant to speed the manufacturing process.

Neon

- **Electronics:** Dominated by DUV laser lithography, usage continues to out-scale wafer start growth as the complexity of leading-edge chip designs drives adoption of multi-patterning lithographic techniques. Laser annealing and lift-off for new display technologies will further accelerate demand.
- **Non-electronics:** Dissolution of signage applications has quickly reduced the non-electronics demand and ceded supply availability to electronics.

Argon

- **Electronics:** Argon is the primary inert gas used in the fab due to its relative inexpensive cost to supply. Usage continues to trend with process complexity. Geographic supply imbalances occur sometimes when large wafer or ingot fabs are built in regions lacking in ASU-intensive industries like steel and chemical production.
- **Non-electronics:** Usage is widely varied for inerting of high-temperature material processing, like the manufacture of stainless steel and as a plasma gas for welding.

Krypton

- **Electronics:** Usage in electronics is co-reactant in DUV excimer lasers and sputtering account for the relatively small electronics demand.
- **Non-electronics:** In these applications, krypton is used as an insulator between panes of glass.

Xenon

- **Electronics:** Long used in R&D as an etch enhancer for high-aspect ratio etch, xenon is finding

Packaging

	Gas			Liquid		
	Cylinder	MCP (multi-cylinder pack)	Tube trailer	Dewar	ISO container	Bulk truck
Helium	●	●	●	●	●	
Argon	●		●			
Neon	●	●		●	●	●
Krypton	●					
Xenon	●					

Figure 5. Rare gases are supplied in a wide range of gas and liquid packages.

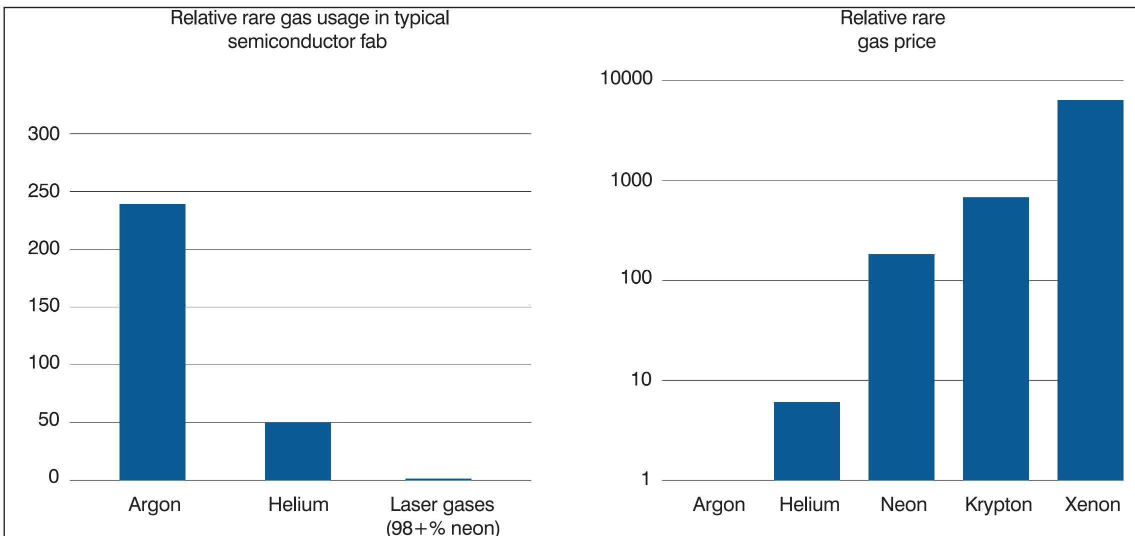


Figure 6. Rare gas usage and price are inversely proportional.

high-volume commercial adoption for such etch applications in new 3D semiconductor structures.

- **Non-electronics:** LED adoption has reduced xenon use for halogen lighting to one third its former demand in the span of the last three years. However, its use as the propellant for space satellites in non-military launches is growing rapidly, which is replacing lighting as the demand driver.

Conclusion

Long invisible to us although they surround us in the air, rare gases were quickly discovered after the enabling invention of air liquefaction by Carl von Linde. The technology to produce these molecules is advanced and the sourcing and production of rare gases is a specialist niche field. Scaling of ever larger ASU plants have made supply of these gases commercially viable, along with exploration and development for geological sources of helium.

From the beginning of semiconductor processing, rare gases have been important for the inerting properties they provide. As the industry has developed in technical complexity, rare gases have filled an ever widening matrix of essential applications. And now, electronics applications form a significant share of the market demand for all of these with the exception of argon.

Linde is the leading supplier of the technology to extract these needed gases. Using the world's largest portfolio of its own production plants as well as contracts with third-party producers, Linde manages the full supply chain of rare gases to meet the volume and quality demands of its electronics customers. Linde anticipates its customers' developing requirements by continuing to be the innovator in its field.

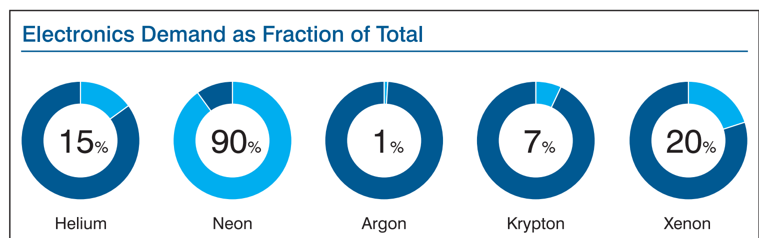


Figure 7. Electronics application demand makes up widely varying fractions of the total market for each of the rare gases.

NXP reveals new power product line solutions

NXP has released a new line of processors and microcontroller solutions for the IoT, low power requirement designs and high performance multimedia applications. Silicon Semiconductor's Mark Andrews spoke with NXP's Ron Martino, VP and GM of the company's i.MX product line, about their new solutions and the company's nod towards FD-SOI technology.

NXP Semiconductors (Eindhoven, Netherlands) announced in March that it was bringing new processors and microcontroller solutions to market based upon FD-SOI (fully depleted silicon on insulator) technology, supplanting CMOS in wide-ranging applications. The company also announced new development frameworks and SoCs.

NXP subsequently announced that Amazon was utilizing i.MX products in next-generation 'Alexa' devices. In a separate announcement the company said that its Android Things platform, utilizing i.MX applications processors, supports the new Google Cloud IoT Core, which is a managed service for securely connecting and managing devices at a global scale.

NXP previously announced that its i.MX 7ULP design would deliver 'deep-sleep' suspended power consumption of 15 uW or less: about 17 times better than its previous low-power i.MX 7 devices. Dynamic power efficiency for the new device family is 50 percent better in real-time domains, said the company.

Although NXP's new product line offers superior performance compared to earlier generations, some industry watchers found the news of NXP's commitment to a long-range plan broadly migrating design of general purpose processors and microcontrollers from CMOS nodes over to FD-SOI as most significant. What proved to be deciding factors for the company are the capabilities they find in FD-SOI to deliver designs that can provide low power consumption, high efficiency and scalability. NXP indicated that it sees prospects for developing a variety of processor families all from one FS-SOI process node.

NXP's embrace of FD-SOI began two years ago after Samsung announced 'dramatic improvements' in power, performance and

efficiency in their process recipe. Earnest development began shortly thereafter; qualification came early in 2016, with the first devices arriving at NXP offices late last year.

For NXP, FD-SOI technology represents what some might characterize as an easy transition from SOI—technology with which their design engineers were already well experienced. Key advantages include the flexibility brought by its back-biasing and forward-biasing techniques.

In a nutshell, 'forward back-bias' is an ideal way to increase performance, while 'reverse back-bias' is an excellent way to reduce leakage.

Power Electronics World's Mark Andrews spoke to Ron Martino, VP and GM of NXP's i.MX product line about the new solutions and his company's commitment to FD-SOI technology.

MA: Does the switch to FD-SOI for i.MX devices indeed signal a shift to that technology for low-power solutions overall, or primarily for IoT-related applications?

Ron Martino: The choice of 28nm FD-SOI for next-generation i.MX offerings signals a new paradigm (for the) applications processor -- optimization of power, performance and integration for a diverse set of applications. Our low power solutions (i.MX 7ULP), delivering power efficiency for battery operated devices, will concentrate the transistor design and mix to minimize the leakage through Reverse Body Bias (RBB), as well as lowering dynamic power through Forward Body Biasing (FBB). The performance solutions (i.MX 8 and i.MX 8X), targeting optimized power-performance for wired operated devices, will leverage Forward Body Bias for high performance modes, as well as having the ability to achieve extremely low power wait states for efficient system design and operation. In addition, multiple

applications will leverage the process' inherently high immunity to soft errors and latch-up to dramatically improve system reliability.

MA: Are there other applications for which NXP believes FD-SOI is the ideal tech?

Ron Martino: FD-SOI will benefit many markets targeted by NXP: consumer, industrial and automotive. All three markets require the power-performance benefits. The industrial market will benefit from the significantly improved Soft Error Rates (SER), which can go up to 100x versus bulk, as well as the immunity to latch-up.

MA: Does NXP favor FD-SOI due to its forward back-bias for a performance increase, while its reverse back-bias is a superior choice to reduce leakage?

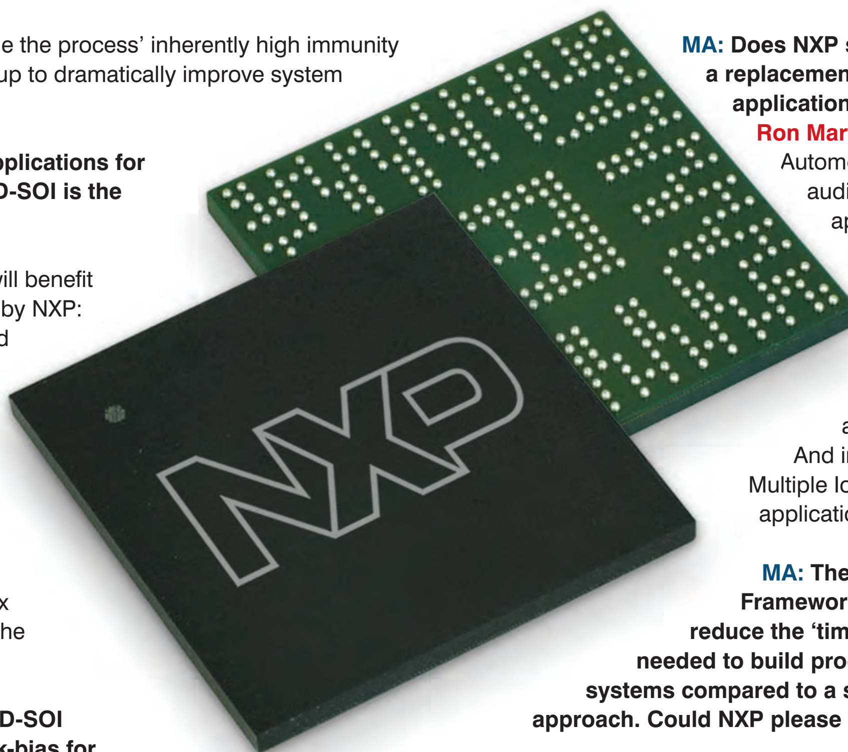
Ron Martino: FD-SOI enables a significantly wider range of RBB and FBB compared to bulk technology alternatives. Lower Vmin operation is achievable without the need of additional devices, which add cost and complexity to the technology and integrated circuit development. The basic technology integration has fewer masking steps compared to alternative bulk options, so short cycle times can be achieved in development and manufacturing of product.

Lower failure rates can be achieved based on superior immunity to latch-up and SER. Device oxide is thicker than some alternatives in the industry allowing for more reliable solutions for automotive and industrial applications. Analog and RF integration significantly benefits from superior characteristics in gain, noise, and switching.

In addition to the above which link to product attributes, there are benefits to internal development efficiency. The wide dynamic range of FD-SOI enables the broadest range of scalable solutions on a single technology platform.

MA: Does NXP see other benefits that FD-SOI technology offers?

Ron Martino: FD-SOI offers the ability to deliver a full range of new leadership products across the continuum of microcontroller, microprocessor and connectivity offerings. The future integration of disparate technologies such as novel NVM, innovative analog leveraging benefits of FD-SOI and RF capability with leadership low power capability enables NXP to apply its innovative culture to create impactful safe, secure and connected solutions for its customers.



MA: Does NXP see FD-SOI as a replacement for CMOS in applications outside IoT?

Ron Martino: We do in key areas: Automotive: Cluster, display audio, telematics and V2X applications processor benefits. Also in Industrial: Industrial control, Point of Sale (POS), robotics, industrial transportation application benefits. And in consumer products: Multiple IoT and wearable/portable application benefits.

MA: The new NXP IoT Framework is said to drastically reduce the 'time, effort and expertise' needed to build production-ready IoT systems compared to a system integrator approach. Could NXP please elaborate?

Ron Martino: In addition to the leadership embedded processing and connectivity products that NXP has introduced to the market, it also delivers leadership enablement and solutions around these offerings to improve time-to-market and reduce development efforts for its customers. In particular, NXP is delivering an Integrated Development Environment (IDE) that simplifies system development requiring connectivity (Thread, ZigBee, Wi-Fi Ethernet, NFC), security (secure element, integrated hardware security), embedded processing reference design, and smart device/cloud computing enablement and interoperability.

MA: How does the NXP time-sensitive network (TSN) benefit Industry 4.0 applications?

Ron Martino: NXP's TSN offering extends its leadership in networking solutions by providing the next-generation of IEEE AVB which converges OT /IT traffic in a single network; (it also) provides determinist Ethernet at gigabit speeds, reduces network delays and improves network robustness of industrial applications.

MA: Intel has released its 22nm FinFET process to foundry customers, saying it offers simplified design rules compared to FD-SOI, that it provides simpler interconnects and that it is a 'technology for the masses.' How does NXP feel FD-SOI compares to Intel's offering?

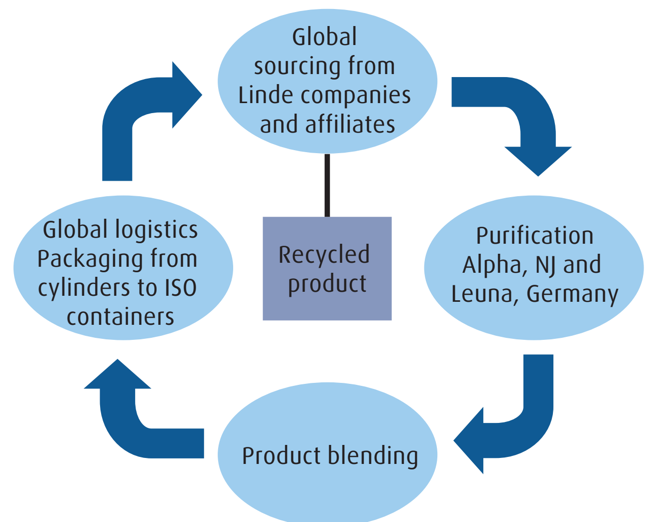
Ron Martino: NXP reviews all competitive technology offerings in the industry in order to make the best selection for its portfolio. In general, a subset of NXP products with very high digital content and performance requirements will benefit from FinFET at more advanced nodes. FD-SOI is a planer technology with simpler integration. Both are fully depleted solutions, however, FD-SOI has the buried oxide which gives better latch-up immunity. Finally, FD-SOI has a large power-performance dynamic range enabled by the body-bias capability.

Leading the market with end-to-end rare gases supply chain

Investing in multiple-site rare gas production, blending, and purification facilities to assure long-term and secure supply worldwide

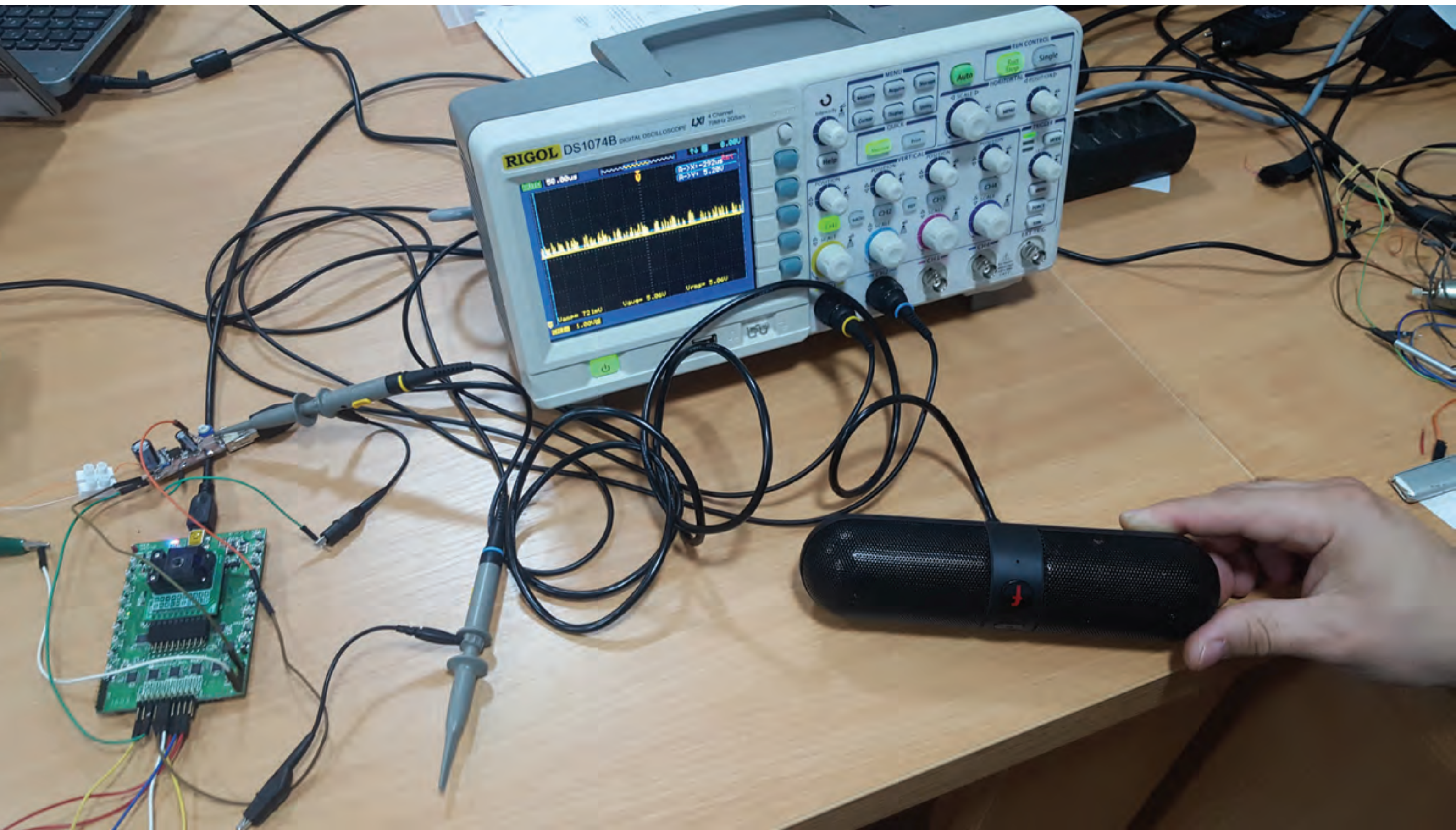
Linde is the only rare gases provider that can provide a robust supply chain including internal production and external partners, cryogenic production and purification technology, proprietary IP for the blending and analysis of laser gas mixes, in-house quality control capabilities, plant design and production, plus this product line:

- Helium – Most diverse portfolio of helium-producing assets
- Argon – Production off-site, delivery and on-site storage as liquid, and distribution on demand
- Neon, krypton, and xenon – Air separation units, purification, blending, and mixing
- Xenon difluoride – Global distributor and direct air shipment
- Xenon and neon recovery – On-site recovery and off-site reclamation, purification, and analysis
- Complete portfolio of laser gases – ArF, KrF, Kr/Ne, Ar/Xe/Ne, and HCl and BCl_3 mixes



www.linde.com/electronics
electronicsinfo@linde.com

THE LINDE GROUP
Linde



Building a portable charger

without expensive ASICs or bloated PMICs

Silego Technology explains how a small, flexible chip can be configured just like an ASIC, but allows designers to design and program prototypes in a matter of minutes vs. the weeks needed for true ASICs.

ONE OF THE BIGGEST improvements that can be made to the smartphone user experience is longer battery life. While users may browse on their phones for hours on end, size-limited, internal, non-removable batteries often come up short. Balancing long battery life with size, however, is a tricky problem to solve. As the battery industry struggles to provide higher energy density battery chemistries and technologies, many smartphone users have turned to portable chargers to support their highly active usage habits. This, in turn, creates a great opportunity for low cost, high-efficiency portable chargers.

Portable chargers are relatively simple devices which comprise a few main components; most commonly Lithium Polymer (LiPo) batteries, a charging circuit, a power distribution switch, a power management IC (PMIC), and a DC-DC boost converter. There are PMIC solutions on the market today which can address these different functions, however many are expensive, power-hungry, and contain many more components and features than are needed for this simple application, leading to a less than ideal solution. Another option is to develop a custom ASIC, however this is only practical in very high volume and

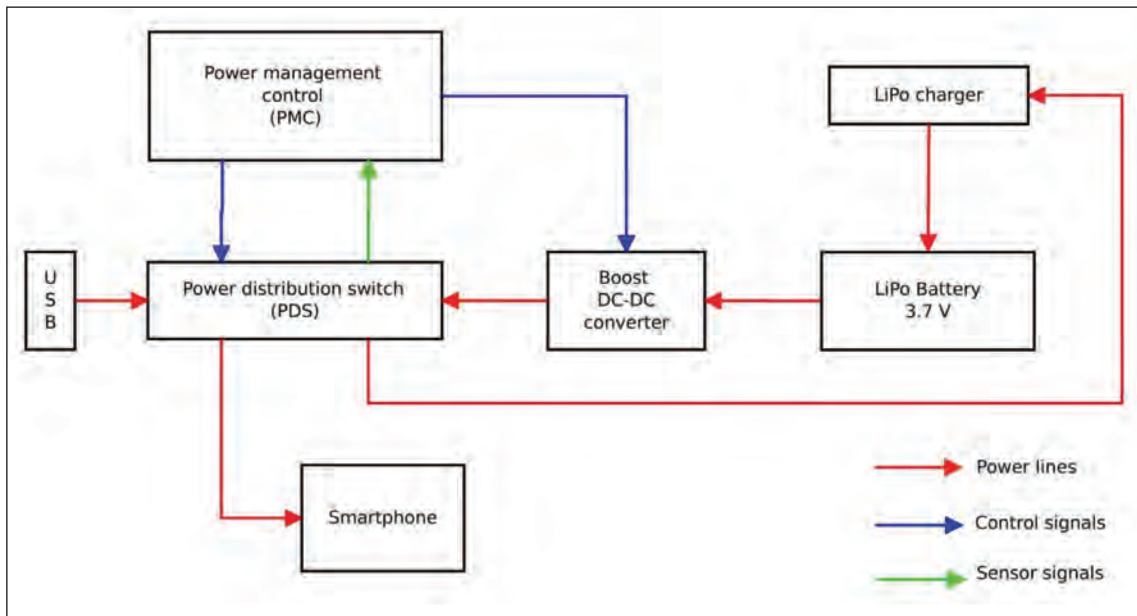


Figure 1: Functional diagram

often at an exorbitant price, volume commitment, and risk of price hikes in the future.

Enter Silego Technology's GreenPAK, a Configurable Mixed-signal IC (CMIC) with one-time programmable non-volatile memory (NVM). This incredibly small, flexible chip can be configured just like an ASIC, but allows designers to design and program prototypes in a matter of minutes vs. the weeks needed for true ASICs. It doesn't require a minimum volume commitment or NRE, either. Using Silego's GreenPAK SLG46620V CMIC, it is possible to implement a full featured, low-power, universal portable charger control circuit in just 2.0 x 3.0 mm."

Many smartphone users have the need for prolonged battery life; – and employ the use of auxiliary power banks. They allow extended usage of their smartphones by up to 6 times (depending on the capacity of the power bank). Power banks are usually mounted on back of the smartphone and they are connected via a charging connector (lightning or USB). For enhanced user experience, they are allowed to be get charged using the same smartphone charger and the user doesn't have to worry about charging it separately. Circuit design of these devices include LiPo batteries power bank, charging circuit for the power bank, the power distribution switch, power management control and the DC-DC boost converter (used to provide the phone with the required voltage (5V).

Hardware design of portable charger power management circuit

Figure 1 depicts the functional hardware design of an portable charger power management circuit. It is composed of the following segments:

- Power management control (PMC) unit – this is the main logic unit of the device. It decides whether to route power to the smartphone or to the additional power bank. It decides when to turn the boost DC-DC converter on, in order to stop the internal battery power to smartphone.
- Power distribution switch (PDS): It is composed of MOSFETs that are controlled by the PMC unit.
- LiPo battery – For this design, a single cell 3.7V

INPUTS			OUTPUTS		
VBAT	CHG_IN	CUR_SENSE	LIPO_CHG	S_PWR	BOOST_CTRL
0	0	0	0	0	0
0	0	1	0	0	0
0	1	0	1	1	0
0	1	1	0	1	0
1	0	0	0	1	1
1	0	1	0	1	1
1	1	0	1	1	0
1	1	1	0	1	0

Figure 2: LUT tables

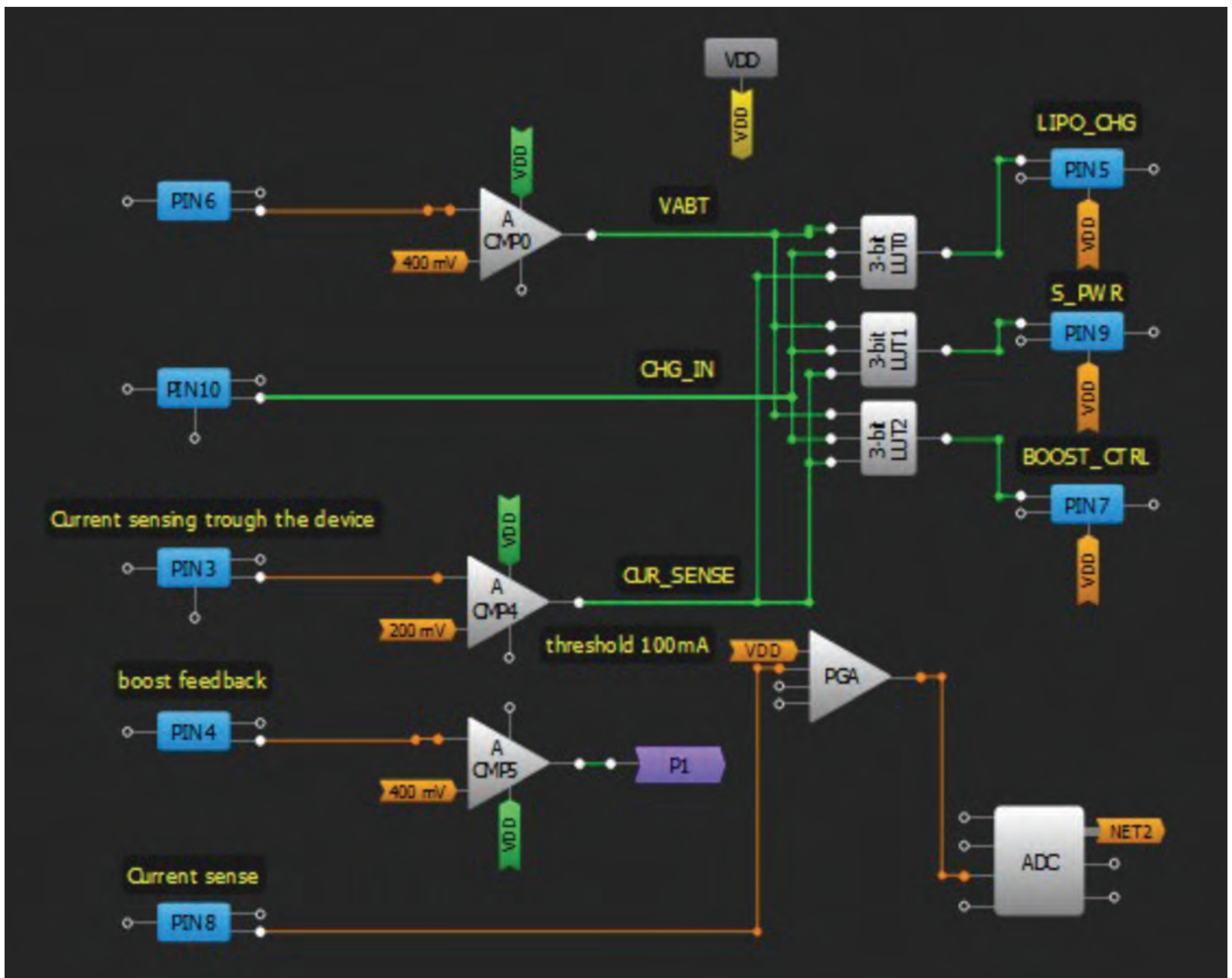


Figure 3: LUT tables implementation using GreenPAK SLG46620V CMIC

1000mAh battery is selected as the power bank unit.

- LiPo charger – A controllable DC-DC buck converter design is used as a LiPo charger.
- Boost DC-DC Converter – boost DC-DC converter is required to boost the LiPo battery
- 3.7V voltage to 5V required by the smartphone.

Power management control (PMC) unit design and implementation

Power management control (PMC) unit uses inputs from the rest of the device to make power routing decisions. PMC controls the PDS and the DC-DC boost converter.

Inputs to PMC are:

- Charger present indicator (CHG_IN).
- Device power consumption (CUR_SENSE) indicator. This indicator will be implemented using the current sensing method. In case smartphone is drawing current bellow the determined threshold, PMC will route power from the input to LiPo charger as well, so that the power bank can be charged. If the current is above the determined threshold, power from the input will be routed to the smartphone only.
- Power bank voltage indicator (VBAT). This indicator is used so that PMC can determine whether to turn the DC-DC boost converter on (to step up voltage from the power bank and provide it to smartphone) or not.

Outputs from PMC are:

- LiPo charger control (LiPO_CHG) – this output will send signal to the PDS to route power to the LiPo charger.
- Smartphone power control (S_PWR) – this output will send signal to the PDS to route power from input to the smartphone.
- Boost control (BOOST_CTRL) – this output will turn the boost converter on and send signal to the PDS to route power from the boost to the smartphone.

PMC is a digital logics circuit with 3 inputs and 3 outputs. This can be easily implemented using LUT tables. Three 3-bit LUT tables are used for implementation of PMC using GreenPAK SLG46620V CMIC.

Figure 2 shows the functional table for the PMC input and outputs. Each output is implemented using one

3bit GreenPAK SLG46620V CMIC LUT unit. Inputs from the pins are routed to each LUT table. Figure 3 explains the implementation of the PMC using GreenPAK SLG46620V CMIC.

Power distribution switch design and implementation

Power distribution switch is controlled by the PMC outputs LIPO_CHG, S_PWR, BOOST_CTRL.

Figure 4 depicts block schematics of the PDS. Control signals are provided by the PMC. PDS provides sensor signals to the PMC: CHG_IN and CUR_SENSE. Current sensing is used at two places in the design and Figure 5 shows the schematics used for this task. The SLG88101 OP-AMP is used to make the current sensing circuit, and as it is dual OPAMP, only one IC is used.

Figure 6 depicts the PDS implementation schematics. A Silego GreenFET3 is used for PDS implementation. The SLG59M1709 is a perfect match for load switching since the maximum continuous current of 4A; which is 2-3 times more than the required charging current for most of smartphones on market.

LiPo charger design and implementation

LiPo charger is implemented using a controllable buck DC-DC converter. Constant current (CC) and Constant Voltage (CV) modes are used to charge the LiPo battery. CC mode is used when battery voltage is below 4.2V and CV mode is used when battery voltage is above 4.15V. Figure 7 shows the charging curve for the LiPo battery using both CC and CV modes. In order to implement this charging method, the charging current and LiPo battery voltage are monitored.

The input from the USB charger is stepped down using a buck DC-DC converter that provides a 4.2V output. In order to achieve the constant current (CC) mode, the average voltage on the battery must be variable. Current is tracked using the current resistor and the OP-AMP. Output from the OP-AMP is compared with a specific voltage threshold. When the current through the battery goes above the specified current, output from the PWM is simply disabled; when it goes back under the threshold, output from the PWM is enabled again.

When battery voltage reaches 4.15V, the LiPo charger goes in CV mode and it provides a constant 4.2V output. Current is sensed again and it is compared with different thresholds; when it reaches 10% of the maximum charging current, it sends a signal to terminate the charging and the PWM output. Current sensing is implemented using approach described in Figure 5 and the SLG88101 OP-AMP.

Figure 8 depicts the buck DC-DC converter analog design. Following are parameters used for the buck converter design:

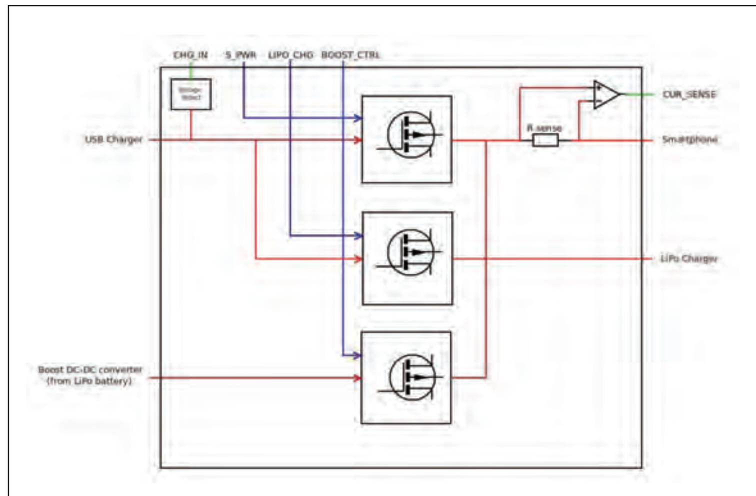


Figure 4:Power distribution switch design

- $V_{in(max)}$=5.1V, max voltage input
- V_{out}=4.2V, output voltage
- I_{out}=1.2A, max output current
- f_s=62.5kHz, minimum switching frequency
- ΔV_{out}=50mV, output voltage ripple
- n=0.85, efficiency

Above are set parameters that are used for calculation of next parameters for buck:

- $D\ max = \frac{Vout*n}{Vin\ (max)} = 0.7 \rightarrow$ 70%, max duty cycle
- $\Delta IL = (0.2\ to\ 0.4) * I_{out} = 0.24A$, current ripple
- $L = \frac{(Vin(max) - Vout)}{\Delta IL * fsVin(max)} = 49.41$ uH, minimum inductor
- $I_F = I_{out} * (1-D) = 0.36A$, diode current
- $C_{out(min)} = \frac{\Delta IL}{8 * fs\Delta Vout} = 10uF$, minimum capacitor
- $I_{sw(max)} = \Delta IL + @\ Iout = 1.32A$, max switching current

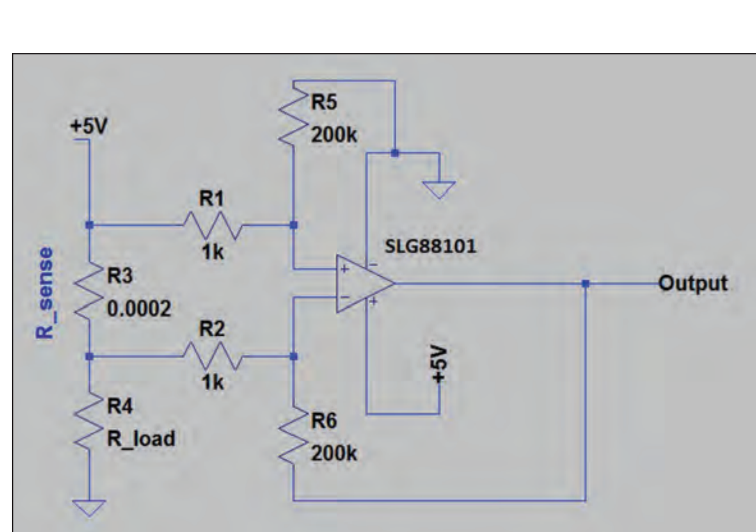


Figure 5: Current sensing circuit

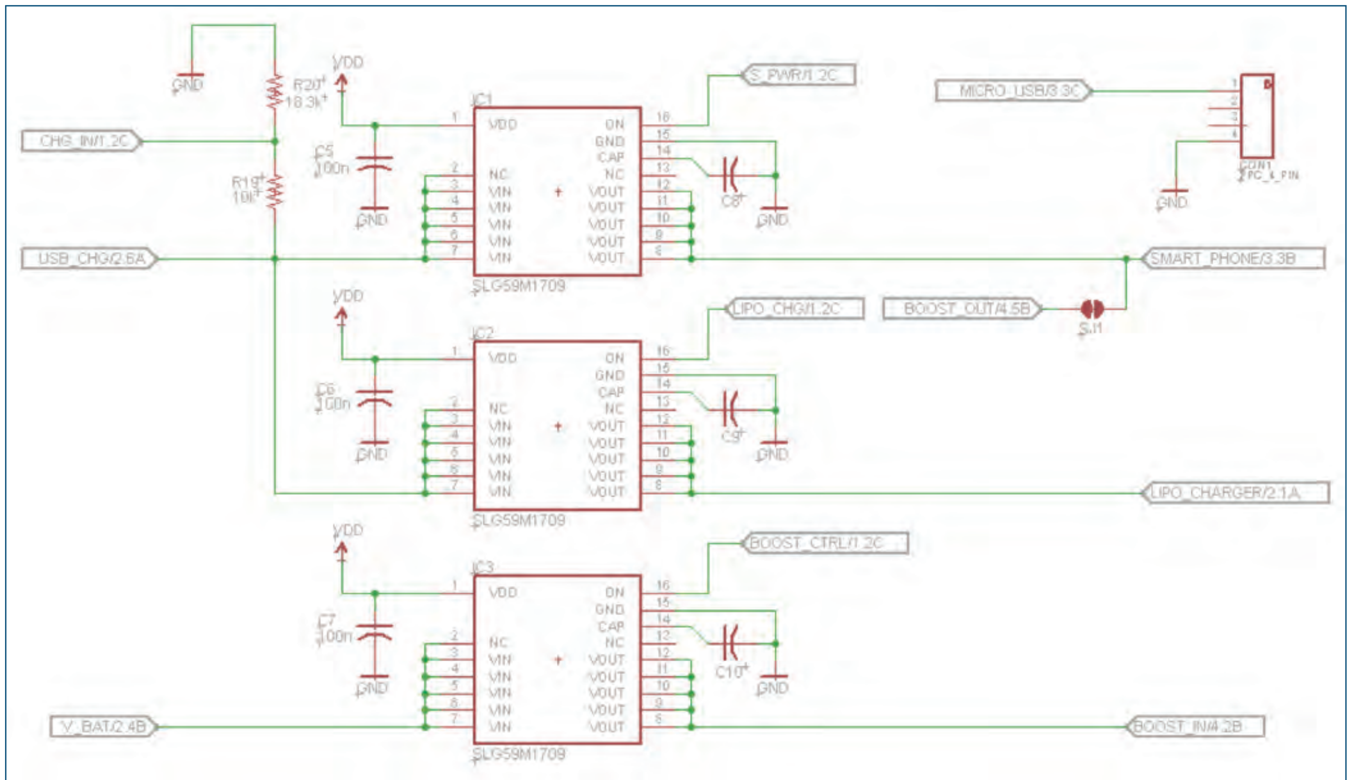


Figure 6: Power distribution switch implementation

The PWM signal for buck can be implemented using the PWM module of the GreenPAK SLG46620V CMIC. The PWM2 and CNT8 modules are used for implementation of the PWM signal.

Figure 9 depicts the implementation parameters used for the PWM signal for buck converter. The PWM2 and CNT8 modules are used to generate the PWM signal. The IN+ selector for PWM2 the module is set to Register 3 and the IN- to counter (CNT8). Switching frequency is determined by the following formula:

$$fsw = \frac{fclk}{Counter_{o*s*} + 1}$$

Duty cycle is determined by the value present in Regsiter3. CNT8 is set to count till 15 and Register3 to 10, in order to achieve the switching frequency of 62.5kHz with a 62.5% duty cycle.

Figure 10 depicts the LiPo charger implementation using the GreenPAK SLG46620V CMIC. Following are I/0 pins used for LiPo charger implementation:

- PIN12, input pin for over-temperature protection
- PIN13, input pin for CC/CV switch
- PIN14, output pin for over-voltage and over-temperature indication
- PIN15, input pin za CV mode
- PIN16, input pin for over-volatge protection
- PIN17, output pin for Buck PWM
- PIN19, CC/CV switching indication
- PIN20, battery full indication
- PIN8, ADC input (Current sensing trough the battery)

Following are GreenPAK SLG46620V CMIC components used for LiPo charger implementation:

- PGA
- ADC
- DCMP0/PWM0, used as digital comparator
- DCMP1/PWM1, used as digital comparator
- DCMP2/PWM2, used as PWM signal generator for buck
- CNT8/DLY8, used as counter
- OSC, used for clock generation and boost PWM signal generation

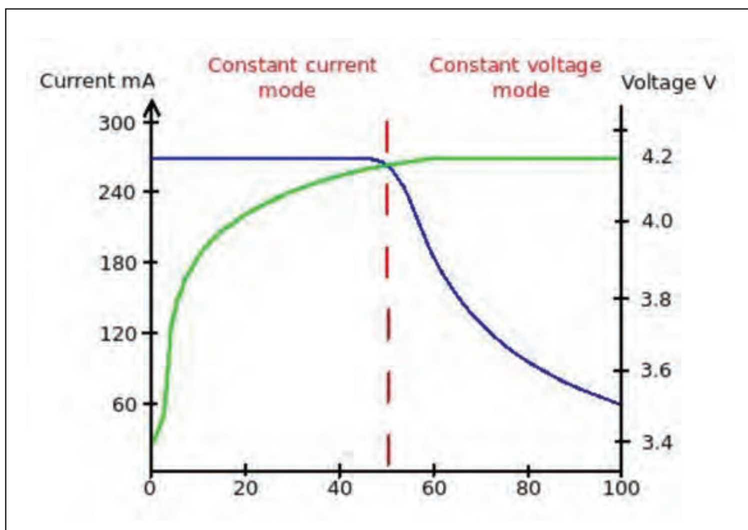


Figure 7: LiPo battery charging modes

- ACMP1, analogue comparator H=50mV
- ACMP2, analogue comparator H=50mV
- ACMP3, analogue comparator H=0mV
- 3-L8, multiplexer
- 3-L9, multiplexer
- 3-L10, multiplexer
- 4-L1, AND logic gate
- 2-L7, OR logic gate
- 2-L4, inverter
- 2-L5, inverter
- 2-L6, inverter
- 3-L12, inverter

The design of the LiPo charger is already explained; the following text will put focus on the implementation using the GreenPAK SLG46620V CMIC.

CC/CV switch:
The CC/CV switch is responsible to switch the LiPo charger between two charging modes. If voltage on the battery is below 4.15V, the charger stays in CC mode; if it is equal or slightly above 4.15V, charger is in CV mode.

In Figure 10, a depiction of the CC/CV switch using an analog compartor can be seen. Input for the ACMP2 2 is PIN13 which is connected to an external voltage divider shown on Figure 11. Output of the ACMP2 is connected as a selector bit of the 3L10 multiplexer. When ACMP2 is 0, the 3L10 will output left channel (CC mode) and if the voltage on battery is above 4.15V, it will output 1 that will make 3L10 output the right channel (CV mode).

IN- on ACPM2 is set to 500 mV, so in order to detect whether the voltage on the battery is above 4.15V, the voltage resistor must be designed to output 500mV when input (Vbat) is 4.15V. Following is the required calculation for the voltage divider:

$$R2 = \frac{Vt}{\frac{Vbat - Vt}{R1}}$$

- Vt = 500mV, output
- Vbat = 4150mV, voltage on battery
- R1 = 15Kohm

A simple RC LP filter is used to cancel any noise on input to the CC/CV switch. Cut off frequency of the designed filter is 3.38Hz. Also, 5mV hysteresis is used on ACMP2 as the voltage on battery varies during the charging .

CC mode:
The CC (constant current) mode is used when voltage on the battery is below 4.2V. In this mode, electronics is needed to maintain constant current through the battery. For current sensing, the circuitry in Figure 5 is used. R_sense is set to 2mOhm. The gain of current sensing OP-AMP is set to 200. If current trough

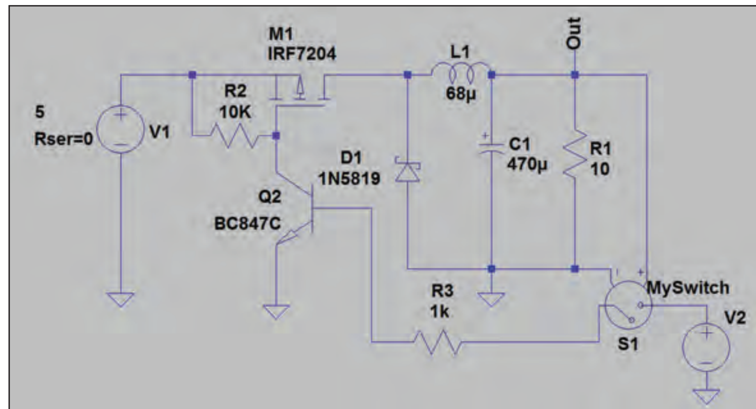


Figure 8: Buck design

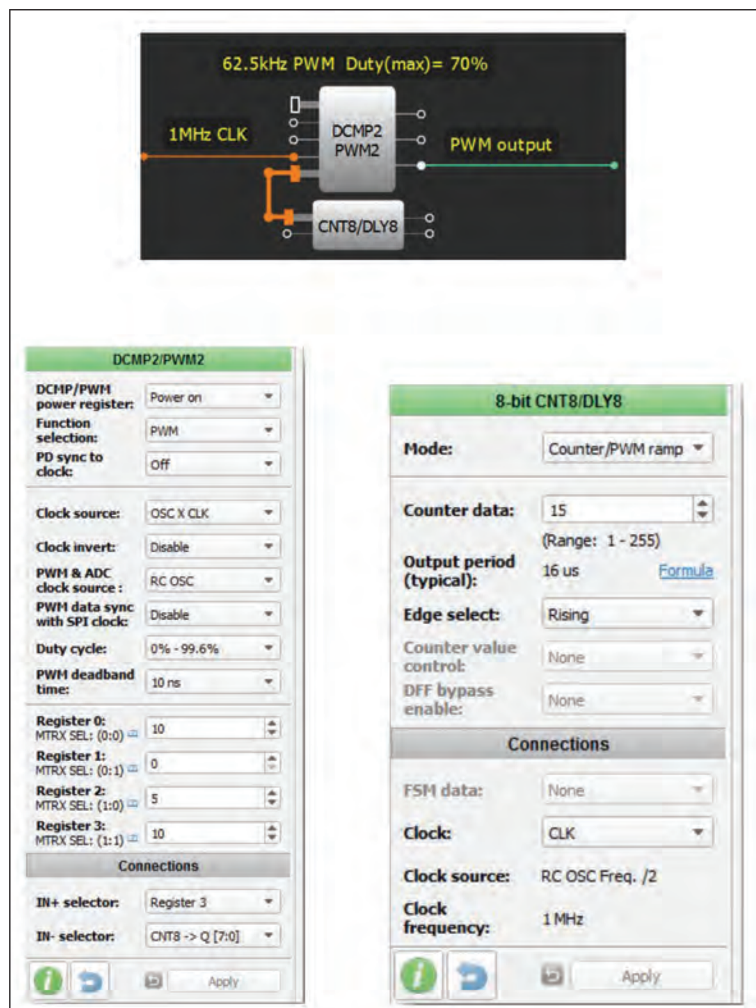


Figure 9: PWM signal generation used for buck – GreenPAK SLG46620V CMIC implementation

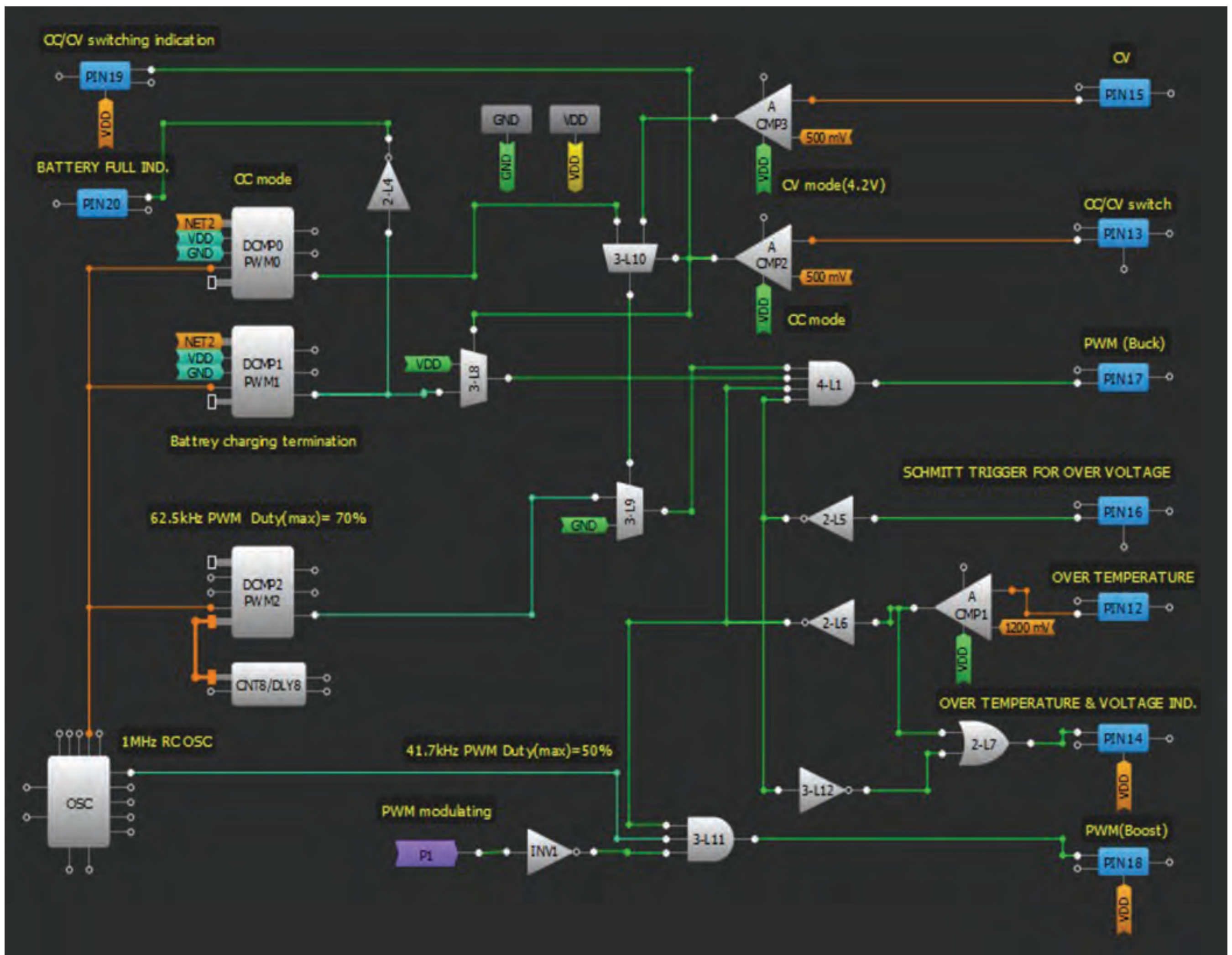


Figure 10: GreenPAK implementation (Matrix 1)

R_sense is 0.5A, voltage on input of OP-AMP is Vin = I*R_sense=1mV. When amplified with 200, we have 200mV at the input of the ADC module in GreenPAK SLG46620V CMIC. 50% of the maximum charging current is used for charging battery, and in this case it is 0.5A. Output of the current sensing circuit is connected to PIN8, which is connected to PGA. The PGA is, in turn, connected to the ADC. Output of the ADC is connected to the digital comparators DCMP0 and DCMP1. Using DCMP0, the LiPo charger maintains constant charging current of 500mA.

In the GreenPAK Designer Software's DCMPO settings, the IN+ selector is ADC output and the IN- selector is Register 0. In order to have information, if current is above 500mA, the Register 0 is set to 50 using the following calculation: GreenPAK SLG46620V CMIC ADC is 8 bit, so resolution is:

$$\frac{Vref \quad 1.2 \qquad V \quad mV}{\& = 256 \; 4.6875 \; sample \; 2}$$

When current trough R_sense is 0.5A, voltage on the ADC input is 200mV as explained earlier, so

$$Register\ 0 = @|| ______ = 42.66 \approx 43$$
$$, \wedge ?_ ' \ )!$$

If the current through R_sense is above 0.5A, the DCMP0 output will disable the PWM buck output in order to prevent rise of current and will maintain it to a constant. The DCMP0 output is connected to a 3L10 multiplexer input and when in CC mode, if output of DCMP0 is 0 (current bellow 0.5A), the output of the 3L9 multiplexer will be the output of PWM2 module. In case DCM0 output is 1(current above 0.5A), output of the 3L9 will be GND.

CV mode:
When CC/CV switch switched charger is in CV mode, output of 3L10 multiplexer will be the output of ACMP3. ACMP3 is supplied with an external voltage divider so that when the voltage on battery is above 4.2V, it is able to output 1. This will also put an output of 3L9 to GND and turn the buck output off. In case, the battery voltage is below 4.2V, the ACMP3 will output 0 so that the 3L9 output is the PWM signal, generated by PWM2 module. This method is used to

keep the voltage constantly 4.2V on the battery. Figure 13 depicts the analog frontend for ACMP3 (voltage divider set to output 500mV when voltage on the battery is 4.2V and the RC filter to cancel noise).

Battery charging termination:
The DCMP1 is used to detect the battery charging termination. When the charger is in CV mode and the current is 10% of maximum charging current (0.1A), charging will be terminated. Register 2 is compared with the value generated by the ADC using the digital comparator DCMP1. Value in the Register 2 is calculated as follows:

$$V_{R\text{-}sense} = 0.1\ A * 0.0002\ V = 0.2\ mV$$

$$V_{out} = G * V_{R_sense} = 40\ mV$$

$$\frac{Vref}{2^{8}} = \frac{1.2\ V}{256} = 4.6875\ \frac{mV}{sample}$$

Register 2 =]\)! / , ∧?_')!] = 8.5333 ≈ 9

Figure 14:

Over-temperature protection
Figure 14 depicts the circuitry used for over-temperature protection. A 10KOhm NTC resistor with a constant B=4050K is used for temperature monitoring. If the temperature is above 50°C, the ACMP1 will terminate battery charging.

Boost DC-DC converter design and implementation

Boost DC-DC converter is used to step power bank 3.7-4.2V voltage up to 5V required by the smartphone. Boost parameters are following:

- n = 0.85, for calculations 0.85 efficiency is used
- ΔV_{out}=50mV, output voltage ripple
- Vin(min) = 3.3V, this is minimal input in boost
- Vin(max = 4.2V, this is maximum input in boost
- fs = 41.7kHz, this is switching frequency
- Vout = 4.9-5.2V

- D =1 – Vin(min)*n =50%, duty cycle
- IL = (0.2 to 0.4) * I_{out} (max) = 0.496 A, inductor ripple current
- L = Vin*(Vout–Vin) = 62.5uH,inductor
- Isw max = IL + Iout(max) = 2.56A, max output current ( ) @ x3y
- Cout (min) = Iout(max)*D / 78*4!'#$ = 311uF

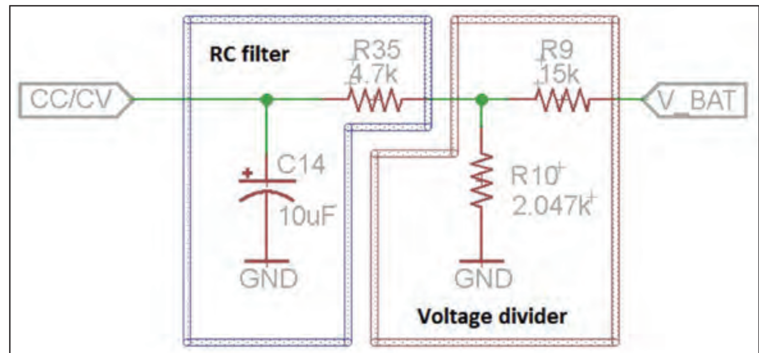


Figure 11: Voltage divider and RC LPF for the CC/CV switch

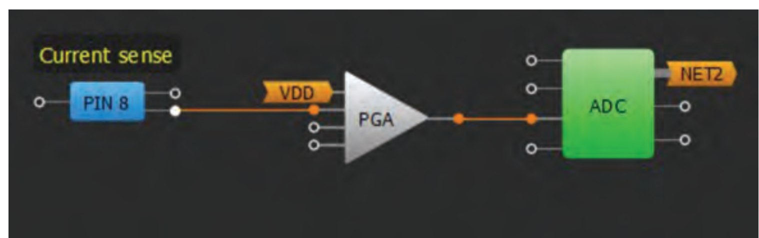


Figure 12: ADC

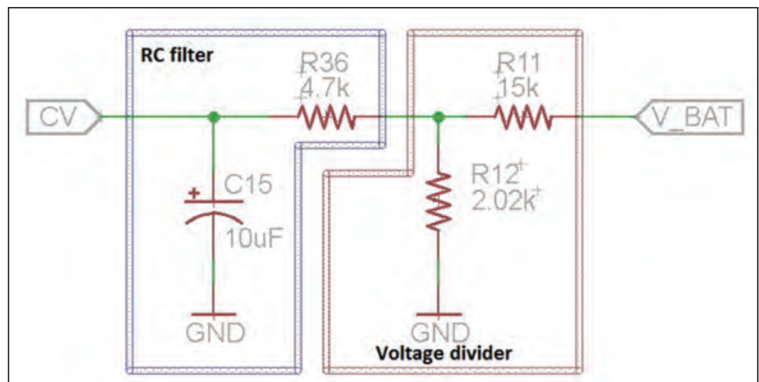


Figure 13: Analogue frontend for ACMP3

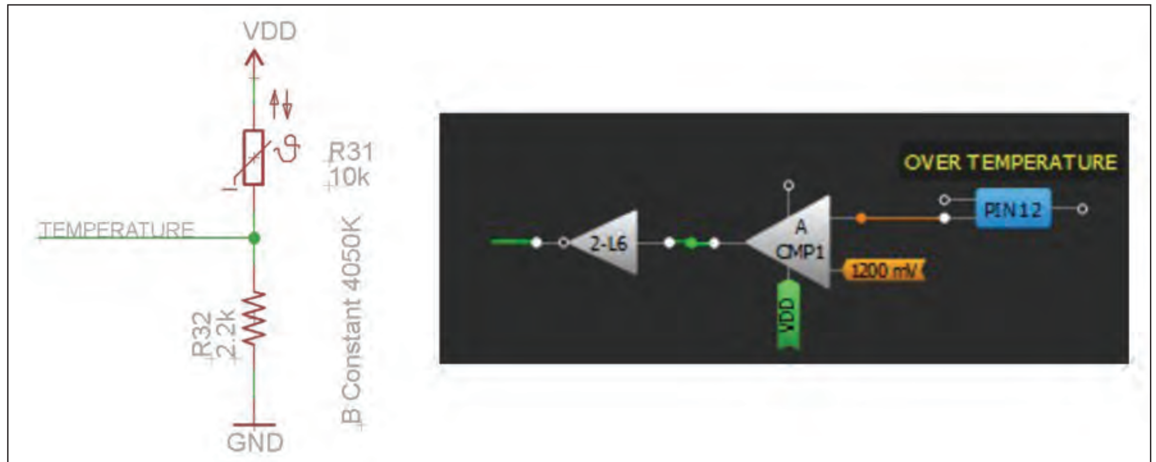


Figure 14: Over temperature protection

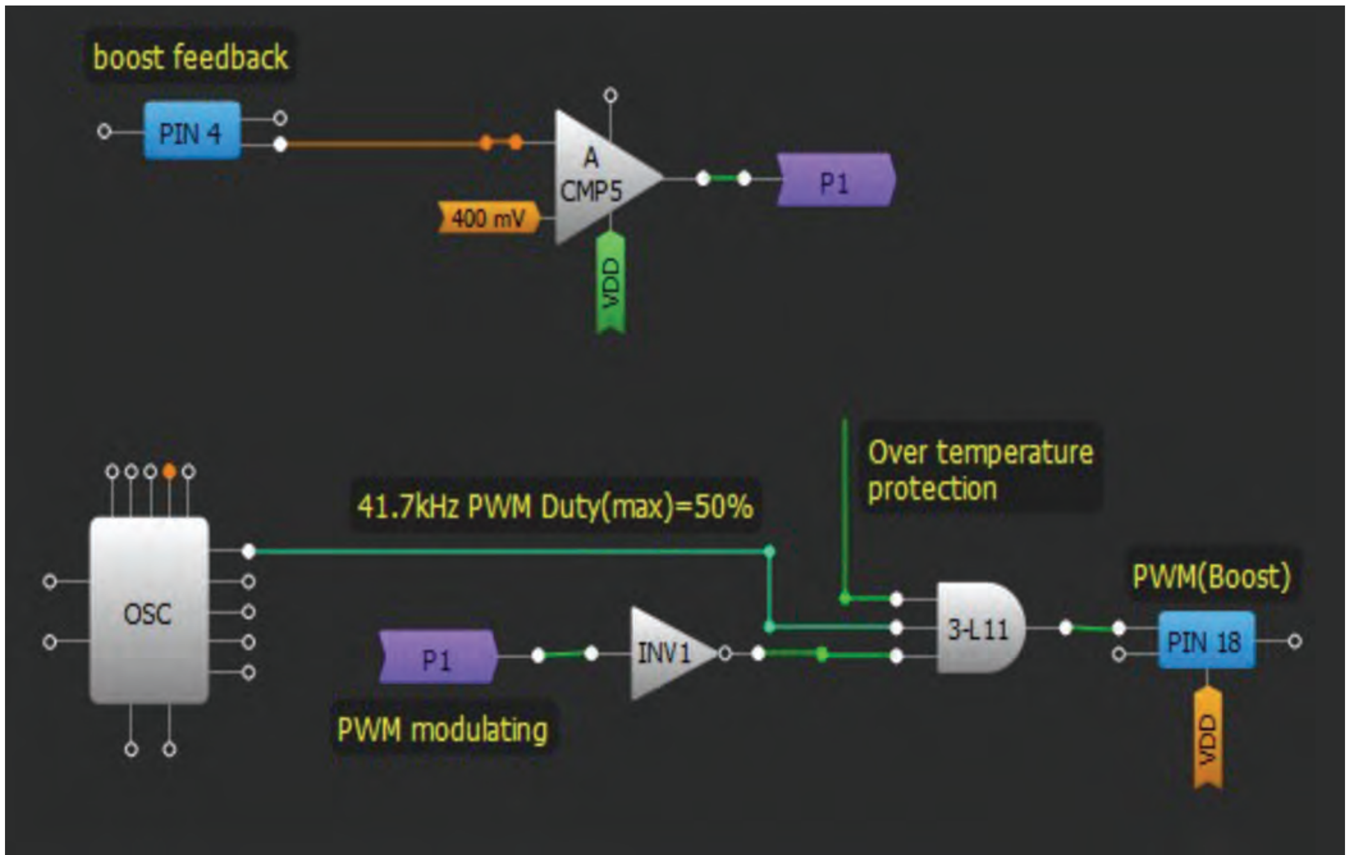
Figure 15 depicts the boost implementation using GreenPAK. PWM is generated using the OSC with the clock predivider set to 2 and the OUT0 second divider set to 24 (in order to achieve the 41.7kHz frequency). A Comparator ACMP5 is used to compare feedback with the set voltage threshold. When voltage on the feedback pin is above the set threshold, the PWM source is turned off. This is a simple way of controlling the output voltage on the boost converter.

Extensions of implemented system:
Implemented system covers all logics, clock generation and feedback provided by sensors to the power management controller for the LiPo battery. The system can be expanded in the analog domain by simply using additional voltage protection circuits. Regarding the implementation on the digital side, the presented design implements all major requirements.

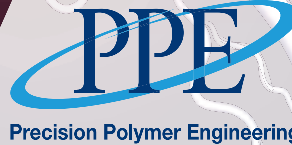
Conclusion

The proposed design and implementation shows that the power management controller and the LiPo charger (including the buck and boost DC-DC converters) can easily be implemented using a GreenPAK SLG46620V CMIC. Using a GreenPAK SLG46620V CMIC allows us to get the desired behaviour of the system without having to invest in custom silicon development. This shows that similar products can be designed and implemented using the Silego technology.

Figure 15: GreenPAK4 Boost implementation



Introducing two new Perlast® elastomer materials – offering the ultimate plasma resistance



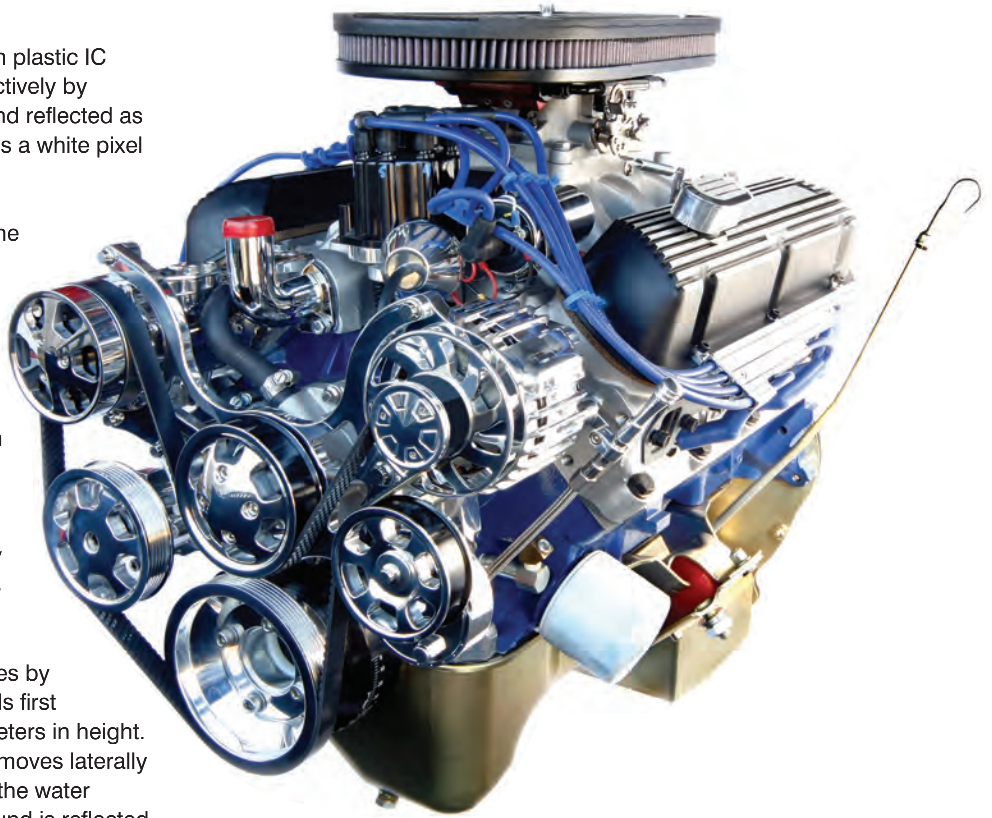
EMEA: +44 1254 295 400
USA: +1 408 441 2043
ASIA: + 886 922 326108
www.prepol.com/plasma

A4 SERIES

Energy efficient dry multi-stage Roots process pumps for all semiconductor applications

- Low energy consumption
- Improved temperature management to optimize the pump according to your process
- Protection of the pump against precursor cracking or condensable deposition
- Corrosion resistant and high particle tolerance
- Extended monitoring functionalities

Are you looking for a perfect vacuum solution? Please contact us:
Pfeiffer Vacuum, Inc. · USA · T 800-248-8254 · F 603-578-6550 · contact@pfeiffer-vacuum.com
www.pfeiffer-vacuum.com



VOIDS, NON-BONDS and other gaps in plastic IC packages can be examined nondestructively by acoustic micro imaging tools. Ultrasound reflected as an echo from any air-filled gap becomes a white pixel in the acoustic image.

Even though no gap may be present, the stresses that are causing the control module failure could have been found by an acoustic micro imaging tool such as the C-SAM® tools from Sonoscan. The telltale signs of stress are external or external surfaces that should be flat and horizontal, but which instead are warped or tilted. Warped or tilted component surfaces are mapped by the C-SAM's Time of Flight mode, while internal interfaces are mapped by the Time Difference mode. Both modes produce contour maps.

The ultrasound pulsed at or into samples by tools in Sonoscan's C-SAM® line travels first through a column of water a few millimeters in height. The transducer pulsing the ultrasound moves laterally at speeds that may exceed 1 m/s, and the water column moves with it. Because ultrasound is reflected only by material interfaces, a portion of the ultrasound is reflected by the water-to-sample interface.

Mapping tilt and warp of internal and external component interfaces

Inside an automotive engine control module, a plastic-encapsulated microcircuit is about to fail because of an internal structural problem. The problem is not the usual void or delamination that eventually, by expanding or corroding, leads to electrical failure. Instead, it is mechanical stress within the die.

By Tom Adams, consultant, Sonoscan, Inc.

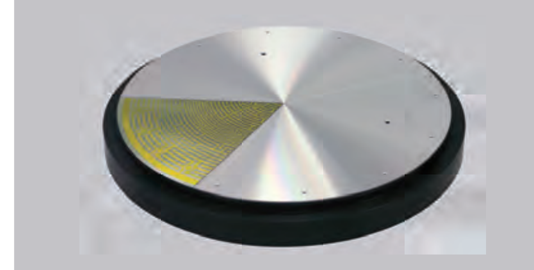
From here the rest of the pulse travels into the sample, where it may strike and be reflected by a second interface. If the pulse strikes only solid-to-solid interfaces, it may be reflected by several of the interfaces. But if it strikes a solid-to-air interface, it goes no deeper and there are no further echoes. The pulse -echo sequence occurs several thousand a times a second as the transducer is moving. Each echo (or the absence of an echo in a homogeneous sample with no internal interfaces) represents one x-y location at depth z and becomes one pixel in the acoustic image.

Time of flight mode

The Time of Flight mode measures the time required for a launched pulse to travel back to the transducer from the top surface of the sample. If the surface of a sample is perfectly flat, the transducer will read the same time, measured in nanoseconds, at each of the thousands or millions of x-y locations where a pulse

WATLOW® SEMICONDUCTOR

Watlow's Thermal System Solutions Enable Next Generation Technology



Watlow® offers:

- Precision designed heater circuits embedded in ESCs and chamber components
- Innovative solutions for gas line heating
- Thermal system integration with heaters, sensors and controllers
- Analytical, FEA and CFD capabilities
- Over 12,000 square feet of cleanroom manufacturing

Powered by Possibility

Visit us at SEMICON® WEST booth #5344, and ask us about our new ATS technology.

For more information visit our website at www.watlow.com

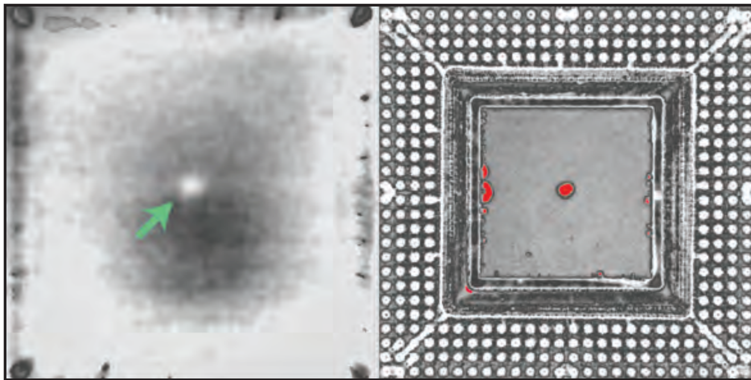


Figure 1. The bump (white, at left) at the surface of this plastic BGA package was caused by a void (red, at white) between the die and the mold compound.

was launched. On a perfectly flat sample, all locations will report the same Time of Flight, and the image of the surface flatness will have pixels all the same color (or the same shade of gray). Variations in elevation will produce a map displaying multiple colors.

Slight variations in surface flatness are not likely to be significant, so why map the component surface at all? Because some variations in surface elevation are caused by internal anomalies such as voids, or by internal stresses other than gaps. Either of these items may change during the component's service and cause an electrical failure. Local mechanical stress may blossom into a crack. A small innocent-looking gap may grow and break a wire bond.

The user may employ reflection mode imaging and limit the return echoes used to make the acoustic image to a specific depth of interest. This process is called gating, and a gate may be wide (vertically) or narrow. If a void appears bright in a reflection mode acoustic image, the void must lie within the gated depth, .

Figure 1 left is the Time of Flight image of a plastic BGA package. The image shows the relative elevation of the top surface of the package: lighter colored regions are higher, darker colored regions are lower.

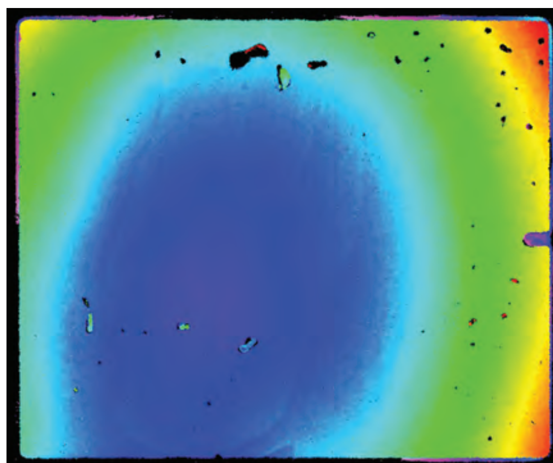


Figure 2. Colors display the contours of a warped ceramic raft, seen through the heat sink of an IGBT module.

Note four indented - and therefore dark - mold marks at the corners. Overall, the package surface is higher (lighter) near the edges and lower (darker) near the center. There is one significant anomaly - the small bright white spot marked by an arrow near the center of the package. Changes elsewhere are mostly gradual, but here the package surface spikes upward. Such an anomaly is typically caused by internal feature.

Figure 1 right is a reflection mode image of the same area of the package, gated on the die face - meaning that only echoes from the die face are used to make the acoustic image. Here colors display the degree of reflection from internal interfaces. The anomaly seen in the Time of Flight image at left was converted from white to red, the conventional color for defects, and is clearly a void between the die face and the overlying mold compound. This void has sufficient vertical dimension to cause the mold compound at the top surface of the package to be pushed upward, as seen in the contour map in the image at left. There are smaller voids near the periphery of the die, but these do not appear in the Time of Flight image and so have not significantly altered flatness at the surface.

Time difference mode

The Time Difference mode measures the difference in arrival time between two different echoes. Both may be from internal interfaces or one may be from the top surface of the component.

Time Difference is often used to map internal contours in IGBT (Insulated Gate Bipolar Transistor) modules. IGBT modules are high-power switches used in environments where high power loads need to be controlled. Mining equipment, ships, trains and wind farm generators are examples. A module typically contains multiple die mounted on ceramic rafts. The rafts are bonded, usually by solder, to a metal heat sink. The amount of heat that must be removed from IGBTs is usually large, with little room for error.

Anything that interferes with heat flow from the die is dangerous. Voids and non-bonds in the solder are the big problem, but tilting or warping of the raft may also impair performance and lifetime. Voids block heat, and can thus cause the die to overheat. Tilting and warping of the raft cause uneven heat loss across the die, and can lead to internal thermal variations that can cause the die to crack. Because failure of an IGBT module may be expensive, disruptive and dangerous, acoustic inspection is often performed to remove (or, before encapsulation, to rework) flawed modules. To avoid deposition of any residue at all on the die, IGBT modules must be imaged through the heat sink by an inverted C-SAM system developed by Sonoscan.

Figure 2 is the Time Difference image of one warped ceramic raft in an IGBT module. To make this image, return echoes were collected only from (gated on) the depth from the heat sink to those points on the the undulating surface of the raft farthest from the heat

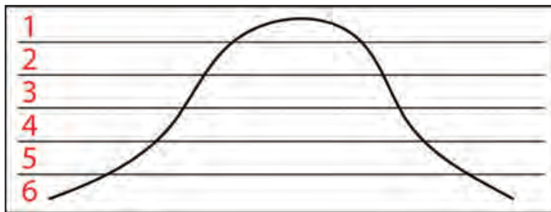


Figure 3. Gating the return echoes produced six depth-specific acoustic images.

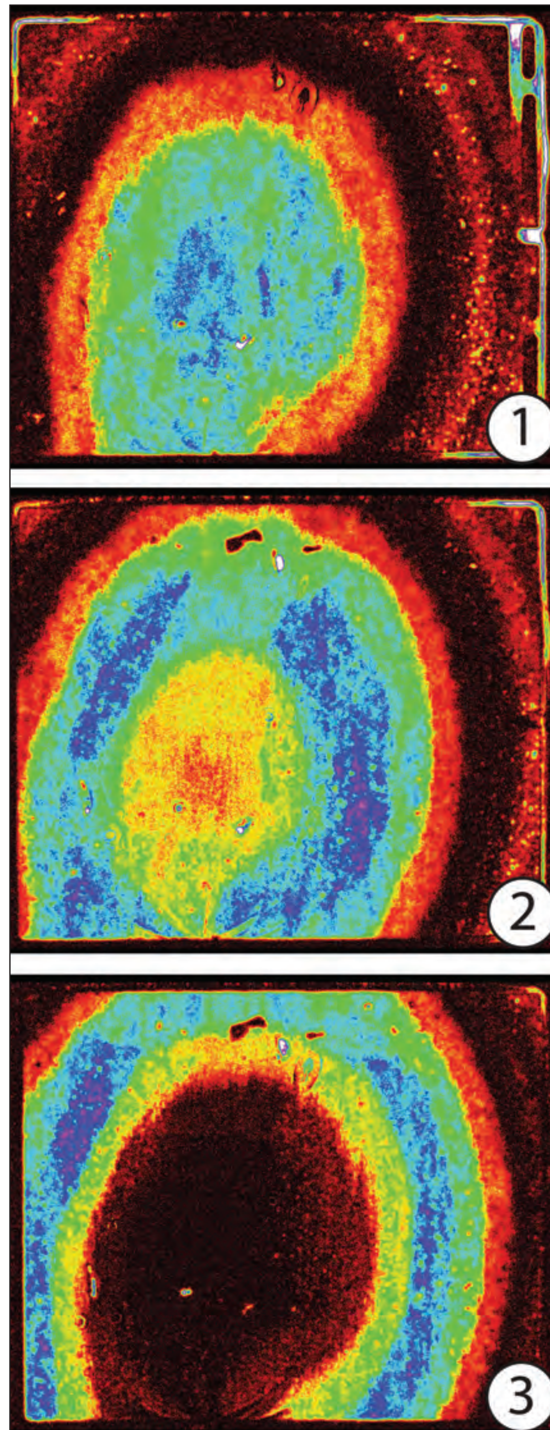


Figure 4. The top three gated depths.

sink. Colors indicate the distance from the raft surface at a given x-y location to the reference point (the heat sink). Those regions of the raft farthest from the heat sink are red. From that depth the surface of the raft moves upward (yellow, green) to dark blue, which is the highest point. The warped raft has formed what amounts to a low hill, with the top of the hill nearest to the heat sink. The solder is thickest in the red areas and thinnest in the dark blue areas.

There are gap-type defects here as well: the numerous small, mostly dark features are voids in the solder. Most appear black, probably because they are above the gate and above the top of the high point of the warped raft. Being outside the gate, they are not imaged directly. Instead, they block ultrasound returning from the raft and create a black acoustic shadow. A few of the voids (at lower left, for example) lie within the gate and are colored according to their distance.

What can we say about this raft? It is rather strongly warped, and its warpage will cause uneven heat removal from the die, and may lead to die cracking. The vertical distance between the red and dark blue regions is about 400 microns. In addition, the small voids will block some heat from reaching the heat sink. This IGBT module is probably not a good candidate for long-term use in a critical application. There are other acoustic methods for visualizing the warping of samples such as this raft. One method involves setting several to many gates. Each gate produces its own acoustic image. The result is that the sample may be viewed in a sequence of non-destructive horizontal slices.

The raft shown in Figure 2 was later imaged as six adjacent horizontal slices, as shown in Figure 3. Each gate was about 65 microns in its vertical extent. The colors represent distance from the reference point. Gate 1 was at the top of the ceramic, and gate 6 at the bottom.

The three topmost gates are shown in Figure 4. The center of gate 3 is dark because at this depth the center of the gate is in the bulk of the raft material and thus has uniform distance from the reference point. The outer colored regions of gate 3 represent the downsloping interface between the ceramic and the solder at this depth. In gate 2 the bulk ceramic material has nearly vanished because this slice is near the top of the warped area. In gate 1 there is no trace of the bulk ceramic. Gates 4, 5, and 6, lying below gate 3, looked much like gate 3 but with increasing areas of dark bulk ceramic.

Acoustic measurement of flatness is not limited to IGBT modules and BGA packages. Wafers are scanned to map their flatness before undergoing processes such as dicing that can damage non-flat wafers. Sonoscan has developed a system that, while scanning a wafer for defects, adjusts the transducer height to accommodate each die.

Customer focus drives AP&S growth

Ever-changing global manufacturing requirements have driven AP&S expansion programs that give customers access to an industry-leading suite of wet processing and metal lift-off tools.

AP&S INTERNATIONAL GmbH has a deeply ingrained customer focus that has led to waves of company expansions, creating one of industry's most extensive wet process portfolios along with unique metal lift-off technologies and unparalleled responsiveness to changing market opportunities.

Getting to know AP&S International (Donaueschingen, Germany) is somewhat like receiving a nesting or Matryoshka doll: there is a new layer to be discovered at every turn. Silicon Semiconductor editor Mark Andrews spoke with AP&S CEO, Alexandra Laufer-Müller, to learn more. He discovered a growing

portfolio of products and services supporting wide-ranging semiconductor requirements including MEMS and micro-structuring as well as an R&D program focused on long-range customer requirements. AP&S constantly innovates. Its almost three-fold Demo Center expansion created a hands-on customer pre-sale experience; its expanding customer care programs are centered on maximizing up-time and first-to-market advantages.

"We specialize in wet process technology," Laufer-Müller said, "But we offer so much more, which

> The steadily increasing challenges of the industries that we target make it necessary to offer customers not only high quality wet process tools, but to guarantee maximum uptime in their production everywhere and every time

is a reason we encourage customers to visit our headquarters. But because we know that this is not possible for everyone, we have focused on bringing our expertise to the customer as well as after sales service that strives to be the very best."

"Our aim is to cover the full range of wet process solutions, which are required across both front- and back-end production chains. Thus, our products perform functions such as cleaning, etching, metal etching, PR strip, electroless plating, lift-off, drying and developing processes. That is the beginning. Together with our customers we steadily develop new, outstanding processes, like the AP&S metal lift-off process, which is unique in today's market. We also offer manual-, semi- and fully-automated applications," she explained.

Today's AP&S grew out of 2003 acquisitions; collectively the company has served semiconductor manufacturers for two decades. When AP&S discovers a need it will set about identifying ways to meet that need, which often results in new hardware or software tool development. AP&S can dedicate its resources with confidence since each expansion it has undertaken is based upon customer requirements, thereby helping ensure ROI. The company takes its customer-centric focus to the point that business units are organized around the way process tools are typically purchased: single wafer tools or batch processing tools. One of their latest innovations and third major business group is the After Sales Unit that was established this year.

"The After Sales Unit was established at the beginning of 2017. The reason for this is quite simple. The steadily increasing challenges of the industries that we target make it necessary to offer customers not only high quality wet process tools, but to guarantee maximum uptime in their production everywhere and every time. The goal of this new unit is to offer exactly that to our global customers via the best after-sales support worldwide. Having these three units we are able to offer our customers everything they need from one source," she explained.

The focus of After Sales support is built around helping customers by having a primary access point for determining what parts or repair services are needed and to help ensure that customers have little or zero down time through preventative maintenance programs, long-distance diagnoses, easy access through smartphone/App-based interfaces and AP&S personnel dedicated to the customers' long-term satisfaction. The system supports 'typical' needs for spare parts and fast, on-site service, but goes farther by offering global service that leverages the company's deep knowledge of customers' preferred way to do business.

"With AP&S, customers have a reliable partner, offering them everything they need for efficient wet processes. In addition to the already

3 EVENTS 2 DAYS 1 TICKET

10-11 April 2018

Sheraton Brussels Airport Hotel, Belgium

One ticket gives you access to a 2 day event which will see 3 groups of device makers gathered under one roof.

Hear over 90 presentations covering the entire spectrum of the compound semiconductor, integrated photonics and high-end sensors value chain.

Over 80 speakers CONFIRMED so far.

Book your place now, as it will be another sellout

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry

www.cs-international.net

PIC INTERNATIONAL CONFERENCE

Creating and strengthening links between chipmakers and network builders

www.picinternational.net

HES INTERNATIONAL CONFERENCE

High-end sensors: Market opportunities

www.highendsensors.net

REGISTER NOW, AND SECURE YOUR PLACE. REGISTRATION ALLOWS ACCESS TO: CS INTERNATIONAL, PIC INTERNATIONAL AND HES INTERNATIONAL

mentioned advantages, we also provide services like tool relocations, on-site upgrades and cost-efficient refurbishment programs for used tools. Furthermore AP&S has developed some new, innovative IoT tools for more comfortable operation, monitoring and ordering of required spare parts and/or technical support, which bring added customer value," she said. Because each customer has unique needs, the After Sales Unit consciously tailors services to suit those preferences and needs.

"As we all know, handling wafers and substrates within cleanrooms consists of numerous steps and critical processes, which have to be optimally coordinated in order to obtain high-quality results. Wet processing is certainly just one of these many steps, but one that decisively influences quality. AP&S makes a significant contribution by helping to ensure the stability and purity of wafers and substrates. Our tools make sure that no residues or unwanted particles remain on wafer surfaces; we also prevent unintentional mixing of chemicals and in this way we create a clean basis for further processing."

Laufer-Müller said that some examples of the company's most well-known products include the SpinMask tool from the AP&S single wafer portfolio that provides outstanding mask cleaning results. In the wet bench range the AP&S A-Series tool (available with 100 wafer half-space features for high volume manufacturing [HVM]) is flexible and can handle up to 200mm wafers; for 300mm, AP&S is developing a new platform called TeraStep™ that accommodates up to 50 wafers at once. The CleanStep AP&S Carrier Box is another example of an ideal cleaning and drying tool for carrier boxes along with open cassettes, pods or FOUPs—it employs a combination of spray and spin process techniques. Given the company's deep roots in semiconductor manufacturing, AP&S is also sensitive to the fact that while some customers need the latest technology to support next-generation products, others need the most cost-effective approach possible. Refurbished tools are ideal for these customers as well as for companies that are just getting started.

"Refurbishment of an older tool can be very cost-effective, and this is a hot topic in the market today, and therefore it is, of course, a part of the AP&S service range. We offer comprehensive refurbishment programs not only for used AP&S tools, but also for HMR, Steag (successor: Mattson / Akrion), Lotus Systems and FSI Mercury."

"We renew outdated hardware components and install effective, state-of-the-art software and SECS/HSMS automation that make the tool fit for existing and future market technology requirements. New electric components and pneumatic cabinet enclosures complete the process, along with secured spare parts availability, which is quite an important aspect when a customer purchases refurbished equipment. Again our intention of offering maintenance, spare parts, technical service and software support—all from one hand, also stays in focus here."

The CEO noted that while some customers seeking refurbished tools need to reduce manufacturing costs, others—like those developing new MEMS products—typically only need 200mm or smaller wafer sizes, which can usually be satisfied only with older tools. At the same time the customer wants to be certain that process tools (refurbished or otherwise,) are ready for future needs and are compatible with the latest factory automation/MES requirements. AP&S ensures that refurbished tools are completely updated to every extent possible.

Semiconductor manufacturing is constantly changing, which is another reason that AP&S invests heavily in research and development, including its distinctive approaches to sales and service.

"We began our current expansion in 2016. From the customer perspective the biggest change is the substantial growth of our Demo Center, which includes 300mm process capability that we can now show 'live' for those who wish to see a new tool in action before they buy. The customer can test the wet process application of interest and get all crucial information such as a comprehensive test report containing complete parameters of the process set-up, a recommendation for the process recipe based upon test results and further important system configuration details."

“In 2017 we completed installation of a new UHPW system in our primary Donaueschingen, Germany facility. The system reduces impurities of municipal water to what is considered an ‘ultratrace’ level of less than 1ppb per cationic element, which helps us further eliminate the possibilities of any particles surviving a cleaning process,” she said, adding that, “by rinsing and cleaning AP&S tools with ultrapure water prior to delivery, they can be qualified much faster and less effort by customers is needed on-site. The defect density requirements for production output can be achieved much more quickly.”

“We have also expanded our cooperation network with external partners like renowned universities, among which I would like to highlight our latest partnership with the Fraunhofer Gesellschaft. The synergy effect here is clearly the bundled in-depth expertise between AP&S and the latest institute research into semiconductors. Finally, the ongoing development process of our wet process applications plays a significant role and is essential to keep pace with future market trends as guided by the ITRS roadmap and individual specifications of our customers,” she explained.

Reinvestment to anticipate and meet customers’ rapidly changing needs keeps the company’s developers thinking constantly about what may be needed months and years in the future. AP&S recently expanded its internet connectivity options with its Web Worker App that provides convenient control and fast data access from anywhere in the world. By scanning QR codes on process tools and parts on-site technicians can immediately access data sheets, manuals, guides and instructions, as well engage spare parts ordering and other support needs.

The company’s wide range of wet process tools, cleaning applications, R&D investments combined with a constant pursuit of customer satisfaction are at the forefront of the AP&S commitment to semiconductor manufactures. The company is also looking ahead to further ways that on-site service and its After Sales Unit can earn business while improving the customer experience. A new effort to elevate ease of access will debut at SEMICON Europa (14-17 November, at Messe Munich, Booth Number 1739, Hall B1).

“Our software team has been working on a fascinating project with the Microsoft Hololens. Those who have seen it feel it is simply amazing. I do not wish to reveal too much ahead of SEMICON Europa. But I encourage all interested parties to visit our booth where they can step into the virtual, futuristic world of AP&S wet process technology. I just want to emphasize that the Microsoft HoloLens is a great tool, bringing many new, until now unused advantages and possibilities for both customers and solution providers in our industry.”

“As you can see, we are totally focused on customer requirements. Whether that customer needs a single tool for manual wafer cleaning or the most advanced, fully-automated wet processing application for 10nm and below devices, AP&S has the solutions needed today and for the years to come,” she said.

Visit AP&S at SEMICON Europa,
14-17 November
Messe Munchen – Booth 1739 / Hall B1

See AP&S live new Microsoft HoloLens mixed-reality demonstration

Interact with AP&S wet process tools live!

Chips with fingerprints make the connected world safer

Chip biometrics form one of the cornerstones of imec's research into a tight and lightweight hardware security that should help ensure the security and privacy of billions of future IoT devices.

SLIGHT VARIATIONS during fabrication make each chip slightly different from the next. This is a headache for chip designers, who must ensure that chips all behave the same. But security specialists rejoice: they can exploit the chip variation flaw to stamp each chip with a unique fingerprint. And with these fingerprints, chips can authenticate and generate encryption keys in a more secure way, making connected applications much safer to use.

No two chips are made alike

If your self-driving car is contacted to come and drive you to the airport, it has no way of knowing that it was contacted by the one unique smartphone that can call it. It could have been called by a copy. So here is a security issue: people can be identified uniquely, electronic applications not (yet). People have fingerprints and other biometric characteristics that are unique, that you can measure easily, and that are very hard to duplicate. Not so for the growing number of connected intelligent applications such as self-driving cars, drones, IoT sensors … In the electronic world, it is much harder to distinguish the real from the fake.

Ingrid Verbauwhede, Leads the embedded systems and hardware group at imec, COSIC, KU Leuven

One solution that comes to mind, an easy and cheap way out, would be to use unique fabrication identifiers for each chip. When the chip is contacted by an application – 'challenged' in security parlance – it will send a unique response that is derived from that identifier (or a cryptographic key derived from that identifier). The application then checks if the response is a valid one. If so, it will hence trust the chip.

But this is far from secure, because it is e.g. possible to have a second, rogue chip use the same identifier. What we need is something that uniquely and physically identifies one chip and no other.

Enter physically unclonable functions (PUFs), or the equivalent of a human fingerprint. They are made possible because, during the chip's fabrication, countless random variations compound to give each chip unique characteristics.

On the nanoscale, it is simply not possible to fabricate two chips that are identical. Researchers have long been thinking about how they could profit from this uniqueness and derive an identifier that when used, can unequivocally identify a chip. The result has been a whole range of proposals for PUFs, each with their strength and weaknesses.

For imec, PUFs are a natural extension of the research in process variability and its mitigation. "With shrinking dimensions, the relative importance of variability on a chip's performance is growing. And our experts have amassed world-class expertise in how to mitigate these effects," says Thomas Kallstenius, Program Director Security and Distributed Trust at imec.

"With the recent expansion of imec, we now also have an R&D group that has a world reputation in hardware security. They had all the knowledge about PUFs but lacked the fabrication capability and variability expertise. Together, we can now work on all aspects of providing chips with fingerprints."

What an ideal fingerprint would look like

"What we are looking for is a chip identity not based on a program that is installed in the circuits, but on the physical characteristics of that chip. That identity should be unique and impossible to copy, not because it is protected by passwords and cryptography but because it is based on random, uncontrollable physics that are impossible to fabricate twice," says Ingrid Verbauwhede, who leads the embedded systems and hardware group at imec – COSIC – KU Leuven.

Some examples of PUFs that have been proposed and tried are e.g. arbiter PUFs, ring oscillator PUFs or SRAM PUFs. The latter e.g. rely on the fact that an SRAM cell powers up to 0 or 1 depending on its nanofabrication characteristics. So, reading out a chip's SRAM bank after power up is a good basis for a unique fingerprint. Ingrid Verbauwhede: "Each of the PUFs that have been proposed have their advantages and disadvantages. Some cost more, e.g., because you need additional circuits. Other have a fingerprint that will change over time, and for others the security community has already found security flaws. And that is why we're still looking for new methods of creating PUFs, e.g. making use not of circuits but of the characteristics of transistors in the latest technology nodes."

An ideal chip fingerprint should be easy to evaluate and stable. This means that it doesn't cost the chip much time and energy to use its fingerprint, and that the fingerprint will not change over time. Moreover, it should be unique for that chip and near impossible to physically clone in another chip. Also, it should be unpredictable from all the responses (or keys) that the chip divulges. Last, in the ideal

case it should be tamper resistant: if someone tries to physically unlock the chip, this should destroy or change the fingerprint.

Ingrid Verbauwhede: "Such a chip fingerprint can basically be used in two ways. One is as a very lightweight way to authenticate the chip, to make sure that this is the correct chip. You send it a challenge and it gives you the response. You then check this response against your database of all legitimate responses. That database has been made beforehand and should of course be kept protected. And – very important – each challenge should only be used once, because otherwise a hacker could listen in, record the challenge/response pairs and use them to hack the chip."

"A second application of chip fingerprints is to use them as basis to generate cryptographic keys. This is a bit more complicated, and you'll need some additional algorithms and helper data to make the keys 100% secure. But the result is effectively a key that is derived from the chip's random properties and not from some stored secret or physical process that can be wiretapped."

A second application of chip fingerprints is to use them as basis to generate cryptographic keys. This is a bit more complicated, and you'll need some additional algorithms and helper data to make the keys 100% secure

A fingerprint based on deeply-scaled transistors

Dimitri Linten is R&D manager at imec's reliability team. With his colleagues, he has been studying the variations in FinFET fabrication, and is now examining how these could be used to create a new PUF.

"Given the problems with some of the other PUFs, we especially looked for a fingerprint that would require no additional circuits or processing and that would remain stable during the chip's lifetime." The new method they came up with uses the intrinsic randomness of the positions at which the gate oxide goes into soft-breakdown. The oxide layer at the gate has been made extremely thin. Over time, with voltage being applied repeatedly, random defects will accumulate in the gate oxide. At a certain point, these defects create a percolation leakage path through the gate. "At that point," says Dimitri Linten, "the transistor can no longer serve its purpose, it has gone into soft breakdown. But what we are interested in is that the location of the percolation path in the gate will be randomly distributed between source and drain, and their position can be measured."

"Of course, oxide breakdowns are an ageing effect. We want to keep a chip healthy for as long as possible and mitigate or delay this ageing breakdown effect as much as possible. But we could reserve a circuit where we can intentionally apply a high voltage to force the gates to form soft-breakdown paths. So, we force part of the chip to age very fast and as a side-effect give us a random fingerprint. And compared to e.g. fingerprints based on SRAMs, this PUF allows a more robust readout, meaning that there is less error correction and post processing needed."

The way that this PUF is constructed, by way of a momentanous ageing, offers an additional security advantage. Most other PUFs are created during the production process itself and can thus be read out by the chip producer. This poses a security risk, because a third party could become aware of the secret identifier. But with the oxide breakdown applied by imec, the PUF is activated at a later stage, by the application builder (e.g. a car engineer) or even by the end-user. In this case, no other party will know the chip's true identity.

Comprehensive hardware security

A lot of research and work is still needed before this PUF can be used in commercial chips, but the researchers see a wide variety of use cases, e.g. in the chips that make up the wireless control networks of cars, industrial machinery or medical equipment. Says Thomas Kallstenius: "Such networks are especially vulnerable. They employ many small connected processors that rely on each other to perform the right actions. It's thus a key issue that they are able to authenticate and trust each other in the most secure way possible, and that is through hardware security."

The work on oxide breakdown PUFs is supported in part by the European Commission through the Horizon 2020 research and innovation program under grant agreement No 644052 HECTOR.

LOGITECH
Materials Technologists & Engineers

Precision system solutions for Semiconductor wafer processing

Precision materials processing systems provide a quick and effective route to complete success in any device fabrication process

Over 50 years in the design and manufacture of precision lapping & polishing, cutting and bonding technologies:

www.logitech.uk.com

Get in touch to discuss your wafer processing needs:

enquiries@logitech.uk.com

Why ultrathin power semiconductors call for advanced inspection process control

Thin and ultrathin ICs are in high demand, but yield that sacrifices reliability has little value. Inspection process control can be the solution, according to UnitySC. By Gilles Fresquet, CEO, UnitySC.

THE DEMAND for thin and ultrathin semiconductor devices rises continuously, driven in part by explosive growth in high-performance computing, networking, automotive and industrial applications. Quite simply, thinner devices often mean a reduced footprint. But this is not the only benefit. For some applications such as power semiconductors, the thinner the dies, the better the device performance. Because of this, backside thinning processes are critical manufacturing steps. While macro-inspection is a suitable process-control approach for backside thinning in many applications, full backside wafer inspection is needed for power semiconductors. This is especially true for power devices with backside processing that includes not only thinning, but backside metallization and even backside shallow junction formation. One example is insulated-gate bipolar transistor (IGBT) devices that require final thickness less than 100μm. This article examines the importance of full wafer backside inspection for IGBT devices.

The IGBT story

While not new, the IGBT has become a popular power semiconductor device choice for a wide range of industrial power-conversion applications, due to recent technological advancements such as rugged switching characteristics, low losses and simple gate drives. These applications include strategic emerging and high-growth industries such as high-speed rail transportation, electric and hybrid vehicles, smart grids and renewable energy. The latest approaches for manufacturing IGBT devices focus on decreasing power losses and switching time. To optimize its performance, the final thickness of a power device is essential. Newer IGBT technology relies on extremely shallow p-doped backside implants to accurately control its emitter efficiency. Any excess in device thickness would result in both an increase of the forward saturation voltage and turn-off losses. Because of this, roadmaps are targeting a final device thickness between 20μm and 50μm by 2020.

Causes of backside defects in IGBTs

For most devices, backside grinding is the most popular method for reducing wafer thickness, due to its relative low cost and high speed. However, the mechanical stress and heat applied during this process can damage wafers. This potential damage needs to be carefully understood and controlled to avoid any negative performance and reliability impacts to the final devices.

An IGBT is a two-layer, bipolar device with a transistor drain that requires not only backside thinning, but also a p and n type backside-doped region formation, followed by metallization to create an active diode. As such, any occurrence of backside defects caused by wafer-thinning processes can be particularly detrimental to the end-device reliability. Compared with standard CMOS, IGBTs can incur defects not only from the thinning itself, but also from the doping process steps that follow.

Ticking time bombs

Traditional approaches to backside wafer inspection include manual microscope visual inspection, which is an unrepeatable process that relies on the perceptions of the human eye, with limited defect characteristics. It requires a specific skillset and isn't always fully accurate nor reliable.

Figure 1: UnitySC's 4See Series combines PSD and CC technology to perform nanometric wafer backside surface and edge defect inspection after thinning and metallization.

Automated optical inspection (AOI) is also used to perform macro-inspection of the wafer surface. Unfortunately, this method, even with increased magnification, is not sufficient for detecting all the defects, particularly those that occur at the nanometer level.

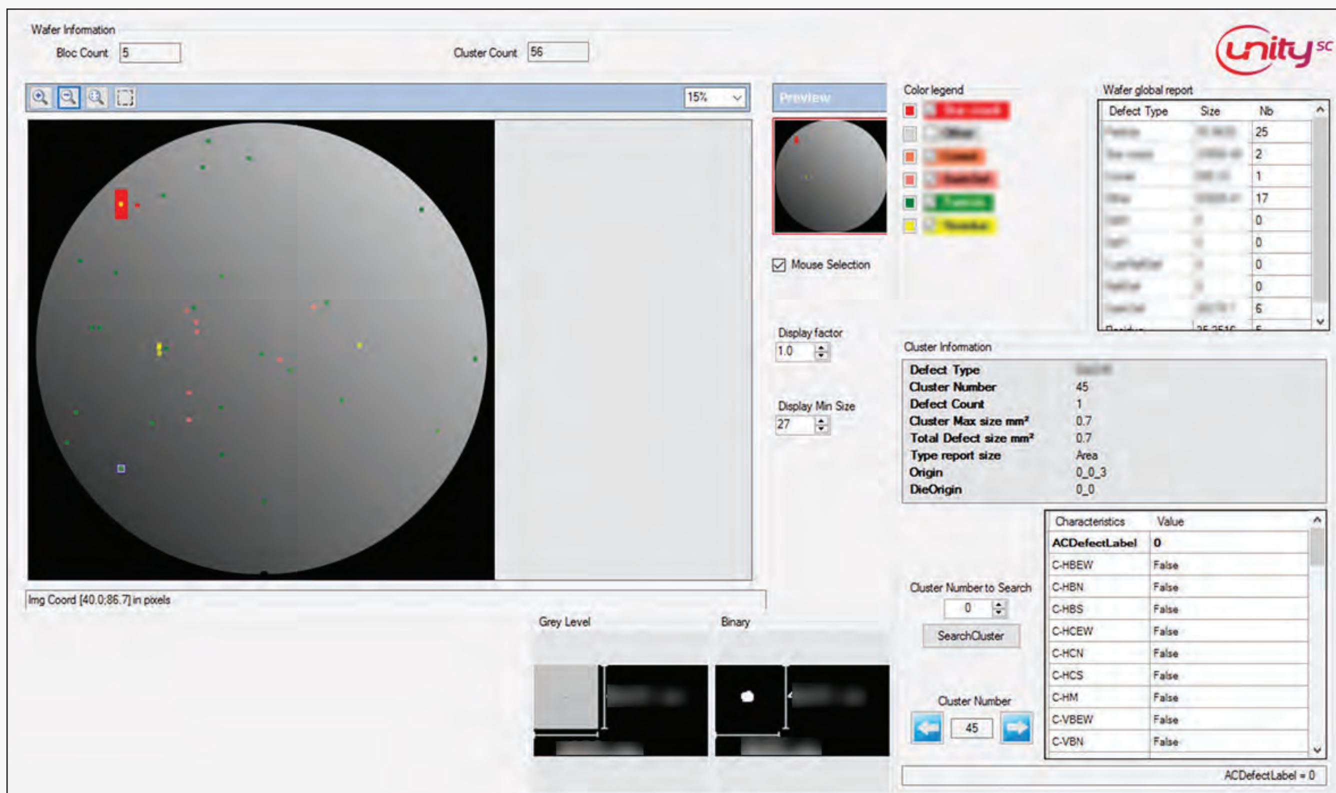
More advanced darkfield inspection might be a solution for some processes. However, due to the high roughness level following the grinding process, the haze level makes the darkfield system almost blind. Additionally, darkfield systems require a perfectly flat surface, and a chucking system is mandatory. For backside inspection, this would mean a chuck on the frontside, which is not possible due to the potential for damage and contamination to the active part of the device.

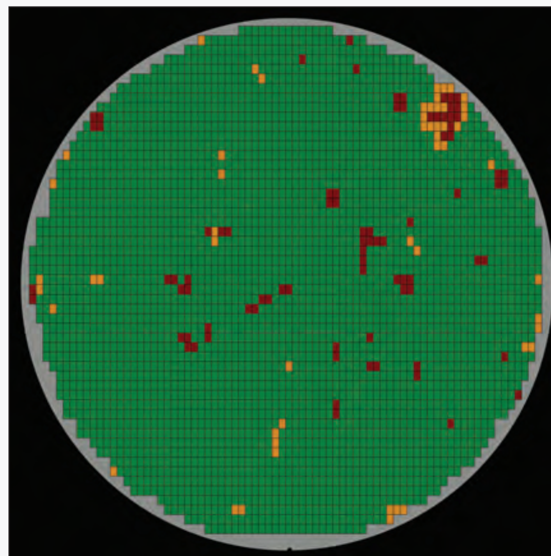
Nanometer-level defects that go undetected can be ticking time bombs because—though they will not be discovered during the final probe test for electrical reliability—they might fail down the road once they are implemented in a system. For example, in IGBT devices, crystal extrusions on a small area of the backside diode can cause it to fail, which in turn creates hotspots in the final device. This device failure could happen at the system level, due to an undetected wafer-level defect. While device failure in a smartphone is a mere inconvenience, in critical applications it can be catastrophic.

Defusing the time bomb

To address this growing need for more accurate backside wafer inspection, a new nanometric defect-detection approach has been developed that combines phase-shift deflectometry (PSD) and conformal confocal (CC) inspection technology; UnitySC's approach is unique and patented.
PSD allows for the detection of topographic wafer defects that are only a few nanometers high, on both the frontside and backside surfaces. Combined with wafer reflectivity and global topography results, PSD provides a reliable method to detect defects such as scratches, cracks, stains and more.

CC technology is based on a white-light beam generated by an LED source that passes through chromatic multi-lenses to separate each wavelength in the vertical direction. It is used to perform wafer-edge inspection (top, top bevel, apex, bottom bevel and bottom) by combining high lateral resolution with a large depth of focus. CC edge inspection





Above (2a) & right (2b): Figure 2: This backside inspection defect map, shown in the top image (2a), is mirrored and combined with a frontside electrical probe test map in the bottom image (2b), to show all detected defects (red from the backside defect map; orange from the frontside electrical probe map). Every die overlapping a defect is reported as bad if it is determined to be part of the 'killer' defect class.

detects typical defects, such as chips, shells, cracks, contamination areas and more, which can propagate on the wafer.

Combining PSD and CC into one system for high-volume manufacturing (HVM) provides reliable and accurate surface topography measurement. For example, UnitySC has implemented PSD and CC technology in the Deflector and Edge modules of its 4See Series automated defect inspection platform, so that inspection can be performed all around and through the device wafer (Figure 1).

Why reliability is more important than yield

Defect detection has always been important during the technology-development phase to adjust processes so that yield is improved. In HVM, finding these defects earlier is becoming more critical to end-device reliability since high yield with low or poor quality is actually a disadvantage for manufacturers. Generating a backside defect map using a system that combines PSD and CC, and then overlaying it with a frontside electrical probe test map allows for a more accurate picture of production yield (Figure 2a & 2b). At the end of the day, it is important for fab managers, device manufacturers and end users alike to understand that, in critical applications, the reliability of the end device begins at the wafer level. With this understanding and by working to improve reliability, the added value for the fab is that the system integrator will come to rely on them for their high-quality devices, which puts them at a premium.

Conclusion

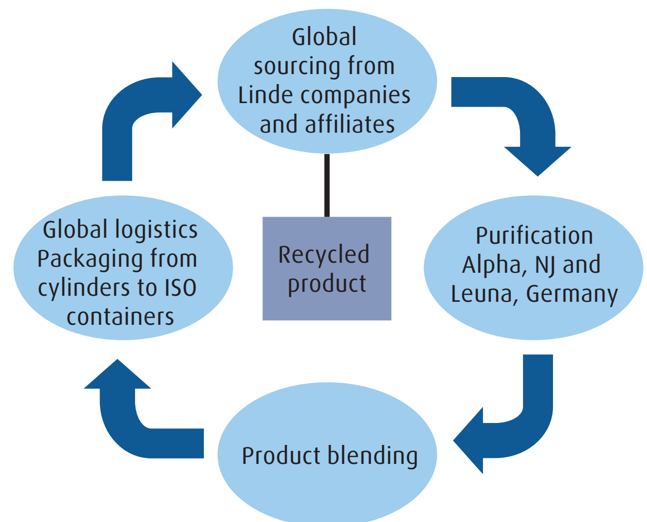
Device manufacturers are under constant pressure to increase their production yields while also minimizing product defectivity. Both objectives can be achieved by implementing a highly accurate approach to backside inspection with systems that feature nanometric defect-inspection technologies.

Leading the market with end-to-end rare gases supply chain

Investing in multiple-site rare gas production, blending, and purification facilities to assure long-term and secure supply worldwide

Linde is the only rare gases provider that can provide a robust supply chain including internal production and external partners, cryogenic production and purification technology, proprietary IP for the blending and analysis of laser gas mixes, in-house quality control capabilities, plant design and production, plus this product line:

- Helium – Most diverse portfolio of helium-producing assets
- Argon – Production off-site, delivery and on-site storage as liquid, and distribution on demand
- Neon, krypton, and xenon – Air separation units, purification, blending, and mixing
- Xenon difluoride – Global distributor and direct air shipment
- Xenon and neon recovery – On-site recovery and off-site reclamation, purification, and analysis
- Complete portfolio of laser gases – ArF, KrF, Kr/Ne, Ar/Xe/Ne, and HCl and BCl_3 mixes



www.linde.com/electronics
electronicsinfo@linde.com

THE LINDE GROUP
Linde

Reno Sub-Systems

sets pace in plasma process control

Unconventional startup Reno Sub-Systems demonstrates that its performance advances in plasma process control is winning over global semiconductor manufacturers. By Mark Andrews, Technical Editor.

RENO SUB-SYSTEMS isn't a typical startup. The company's executive officers and senior staff bear no resemblance to the cast of HBO's 'Silicon Valley.' Their offices are in Nevada, not someone's San Jose, California garage. And they are changing plasma processing tools in a big way.

Being somewhat atypical fits Reno Sub-Systems. The company's founders and pivotal executives have brought more than a 120 years of industry experience and pockets full of patents to the game. Reno has captured the investment confidence of Intel, Lam Research, Samsung and an impressive collection of other top tier industry notables.

Reno has managed in two years to shake up the rather staid RF power, match and gas flow segments of the plasma world that serves atomic level deposition/etch (ALD/ALE) and related processes including PELAD, PECVD for memory and logic circuits. Their products have already sold to nearly 80 percent of the industry's largest manufacturers, which most would find amazing for a company that shipped its first customer orders a bit more than 18 months ago.

The Reno team just might be on to something.

Reno Sub-Systems was co-founded in 2014 by Dr. Imran Bhutta, now CTO of RF products; and Chris Davis, senior vice president of sales and marketing. Together they bring more than 50 years industry experience focused on RF power, gas flow tech, automation, filtration and other key enablers of sub-system performance. They came to Reno after developing semiconductor subsystems for years, leveraging the multiple patents that they hold. CEO Bob MacKnight joined the group in April 2015, bringing over four decades of semiconductor industry experience to the group. Much of MacKnight's earlier years were spent helping young companies grow in highly competitive tech markets.

As sales and marketing chief Chris Davis explained, Reno's founders started the company from positions at the forefront of their fields. They realized that there was an opportunity to rethink key sub-systems in ways that could radically improve performance, but more importantly, that overcome some of the challenges to extending Moore's law through innovation. They used their networks and experience to meet early with several OEM chip makers and equipment suppliers to

Reno Precis microwave generator

size-up interests in new technology. The reaction to Reno's approach was extremely positive, noted Davis, and when the company concluded its Series A funding round in late 2014 backers included Intel's venture capital group, Innovacorp and a major unnamed OEM. 2015 and 2016 were focused on product development and securing design wins for both gas flow control and RF power / match technologies.

Davis and CEO Bob MacKnight explained that once early funding was secured, the company dove into the challenging tasks of building a company from the ground up. Even when working with highly experienced staff, a great many things can challenge the process even as front-facing personnel reached out to build relationships for Reno throughout the supply chain. As many failed startups can attest, having a good idea is not a guarantee of success. While semiconductor manufacturing creates amazing product innovations, the nuts-and-bolts of process technology evolves slowly since high yields and superior efficiency depend on well understood, time-tested practices.

"The thing about RF power in 2014 is that nothing significant had changed for years," remarked MacKnight in discussing Reno's early days. "The OEMs and ODMs were used to certain performance factors; processes were finely tuned around existing sub-system capabilities. Then along comes Reno with big promises to substantially change plasma processing… There is always skepticism until promises turn into actual hardware."

In September 2017, following a successful Series C funding round, MacKnight explained how far they had come in a short while, "Leveraging its patented technologies, Reno has now successfully demonstrated the highest performance radio frequency (RF) matching networks, RF power generators and gas delivery systems for leading-edge nanoscale manufacturing processes. Reno has generated strong customer demand based upon on-tool performance data, which has allowed the company to transition from technology and product development to high-volume adoption within two years," he said.

Reno Sub-Systems' main focus is on two critical areas supporting ALD and ALE: RF power paired with critical RF matching network components, and extremely precise gas flow management systems for plasma process chambers. Deposition and etch have long been used at various semiconductor nodes or for specialized applications, but new device generations are demanding more widespread use of atomic-scale techniques.

Each generation brings smaller device structures that challenge designers and process engineers to accommodate tighter tolerances and finer pitch.

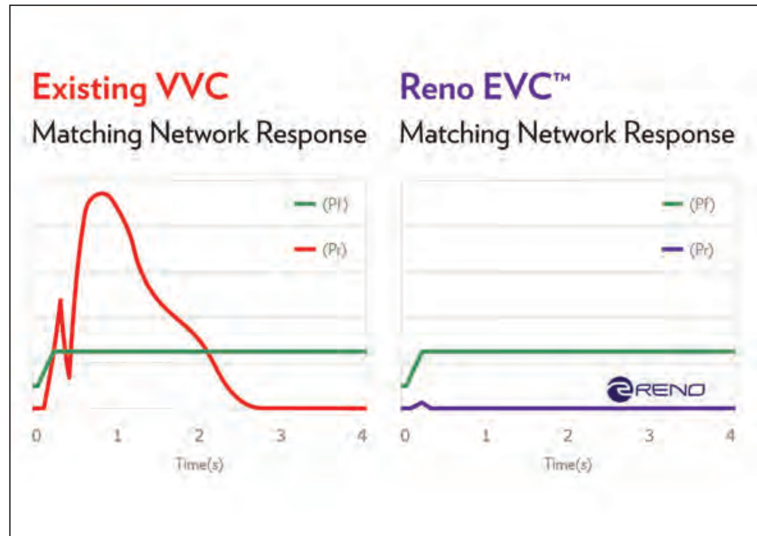


Figure 1: Reno Sub-System plasma etch data show that the company's EVC technology has reduced a 10 second plasma process to ~8 seconds, a 20% throughput improvement.

While older plasma process tools met customer needs, Reno appreciated that requirements were fast changing as manufacturers moved inexorably towards devices below 10nm with 3D structures.

A measurable difference

Plasma processing – either for deposition or etch – is critical for device fabrication below 10nm. Any new solution needs to be repeatable, predictable and controllable. Among key factors are shorter cycle times combined with the ability to achieve process stability in the shortest time possible. Legacy technologies required around 30 seconds to achieve RF match, stabilize gas flow and complete the step. The Reno Sub-System approach focuses on reducing the overall process to 10 seconds or less, with RF match and gas stabilisation takingf less than 50μs.

Leveraging its patented technologies, Reno has now successfully demonstrated the highest performance radio frequency (RF) matching networks, RF power generators and gas delivery systems for leading-edge nanoscale manufacturing processes

Reno calls their plasma process control system Velocity. Its key advantage is the Electronically Variable Capacitor (EVC) that replaces legacy Vacuum Variable Capacitors (VVC). The solid-state technology employed by Reno's EVC can generate power more quickly and since a solid-state system is intrinsically more precise / less susceptible to failure it also provides greater repeatability and fewer maintenance concerns including down-time. In the company's latest tests (See Figure 1) the EVC has reduced a 10-second process to approximately eight seconds – a 20 percent improvement.

This is possible through the very fast matching phase, reduced from one to three seconds in a VVC-based system to 500μs (0.0005 seconds) using an EVC, roughly 2,000 times faster.

"With IDMs, process times need to continue to shrink from tens of seconds to two or three seconds, or less; the technology that is best suited to achieve that goal is with an EVC match," MacKnight remarked. The Reno approach has already been adopted by one of the industry's largest OEMs.

While Reno's Velocity RF matching system could improve performance by itself, when paired with a new type of RF generator its potential could be optimized, the goal when Reno announced its Precis solid-state RF generator portfolio. The latest Precis addition came in July with its newest generator delivering 1.6kW output at 2.45GHz. The company said it believes the Precis is the highest power microwave generator available for plasma applications in semiconductor manufacturing. The key advantage for Reno's microwave generators is an all solid-state design, which replaces the magnetron typically used in other RF/plasma systems.

"For the first time in decades, subsystems are enabling new processes and future device generations. The ultimate validation of our technology is that 80 percent of the top semiconductor device manufacturers and equipment makers have ordered Reno products," MacKnight said. The Precis microwave generator delivers accurate, repeatable and stable micro-second ramp times using a highly reliable solid-state architecture. Its microwave power control offers significantly better frequency control than comparable magnetron-based generators.

Eliminating magnetron technology from the system is also expected to reduce maintenance requirements, which improves cost of ownership. Precis generators are the latest addition to Reno's highly differentiated Velocity Series with EVC matching networks supporting power needs from 500W to 4.5kW and frequencies from 500 KHz to 40 MHz.

Plasma processing time is also heavily affected by a manufacturer's choice of gas flow systems. The Reno approach, called FlowNode, offers advancements including much faster response times averaging 50μs. It also provides greater dynamic range, more precise accuracy and greater repeatability. The system also eliminates pneumatic delays thanks to removing the bulky mass flow controller (MFC) from the system. Collectively, the Reno tool substantially reduces component size, which MacKnight described as, "…a 7 MFC equivalent, but in a four-gas-stick footprint."

Perhaps more important than size reduction is the increased performance that is proving to be a key differentiator for manufacturers. Like its RF power and matching network solutions, speed plays a major role is gas management, too.

"Reno's FlowNode technology eliminates historic mass flow limitations by eradicating upstream and downstream pressure sensitivity, resulting in (more) stable gas delivery and better process control. FlowNode operates with near-zero internal volume at the diaphragm of the valves, which enables accurate, repeatable, industry leading ultra-low flows for advanced etch and PEALD applications.

Reno FlowNode Series

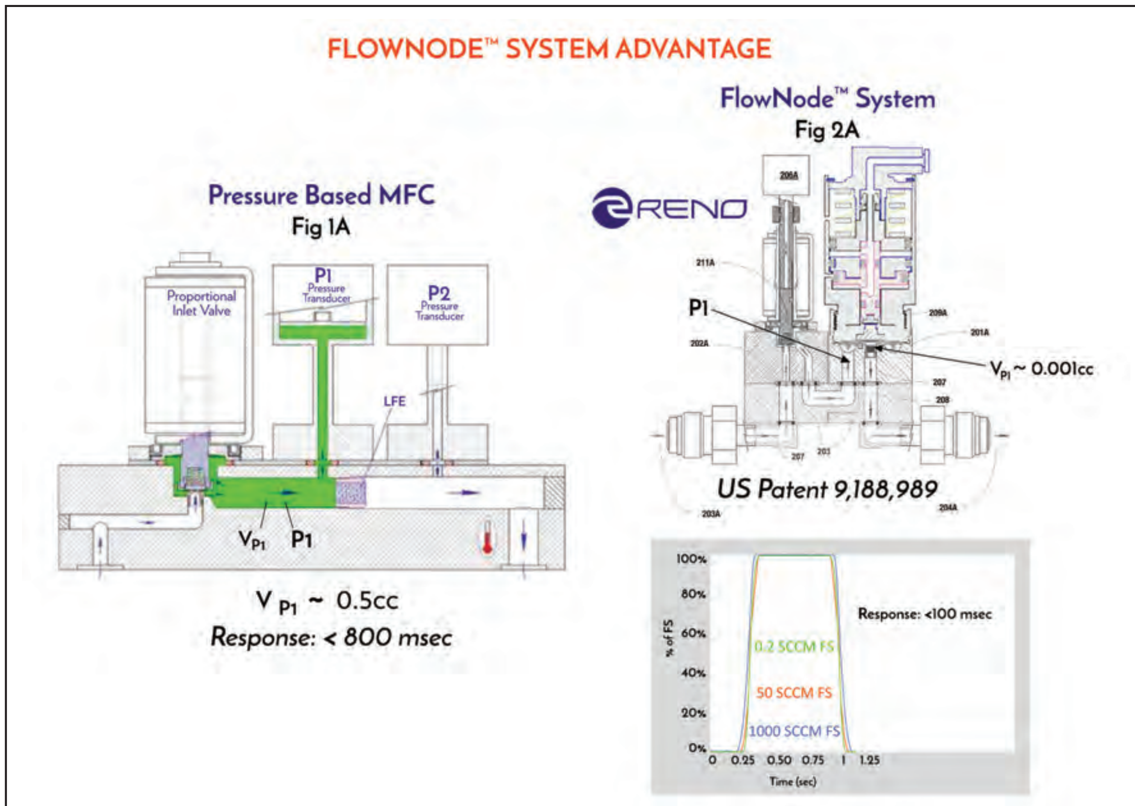


Figure 2: The Reno FlowNode system eliminates the mass flow controller (MFC), significantly reducing gas volumes and pneumatic delays, taking volume in the P1 assembly from 0.5cc to 0.001cc and reducing response time from under 800µs to less than 100µs.

Finally, multiple FlowNode elements can be put next to each other, enabling the widest flow ranges achievable today and reducing the traditional gas box footprint," MacKnight explained. (See Figure 2)

"Many MFCs have insensitivity to upstream pressure changes. However, none except Reno's FlowNode system is insensitive to both upstream and downstream pressure changes. This provides more stable continuous flows, even when there are perturbations induced by other systems turning on and off that feed back to the existing gas flow systems from the main line manifold."

"Due to FlowNode's modular design, we can share valves for multiple functions and eliminate redundant sticks," he explained. "It has been a part of (historic) MFC evolution to go from thermal MFC to pressure-based MFCs. While a pressure-based system greatly improved gas flow control over its thermal MFC predecessor, our FlowNode system is 100 times more stable and repeatable than either of these technologies. This improvement is very important at smaller geometries, where gas stability becomes more critical."

Following Reno's announcement of new products in July, the company sought further investment to expand its product line, serve the global manufacturing base and continue advanced research into new devices and product enhancement.

The company raised (USD) $11.2 million during its Series C funding round; investors were led by Samsung Venture Investment Corp., Hitachi High-Technologies Corporation and SK Hynix. Existing investors Intel Capital, Lam Research and MKS Instruments also participated in the September 2017 funding round.

Although Reno has seen a meteoric revenue increase (10 times larger than in 2016,) no company succeeds by resting on its laurels. While Reno has already sold systems to many of the industry's largest manufacturers, great opportunity remains, including developing new plasma process tools that meet specific needs for various applications.

"We collaborate with our customers to understand future requirements, and we are actively developing modifications to our existing designs—as well as new methodologies—to address their future needs. We are also designing additional, innovative solid-state-technology RF match and power products, and we are adding new flow features for enhanced gas flow control capabilities," MacKnight said.

3D SoC

Improve circuit size, cost and performance by repartitioning

3D integration has evolved into economically interesting alternatives to traditional 2D design. Mieke Van Bavel, PhD, Imec Science Editor explains how 3D integration allows a significant reduction of a system's footprint and enables ever shorter and faster connections between that system's sub-components.

Mieke Van Bavel, PhD, Imec Science Editor

IN RECENT YEARS, the technology of 3D integration has evolved into economically interesting alternatives to traditional 2D design. In particular, the technology is used to package the CMOS imagers found in smartphones, the high-bandwidth DRAM memory stacks used in high-end computing and in advanced graphics cards. 3D integration allows a significant reduction of a system's footprint and enables ever shorter and faster connections between that system's sub-components.

Rather than stacking chips, it is also possible to repartition a 2D systems-on-chip (2D-SoC) design into circuit blocks, realized in separate wafers that are stacked and tightly interconnected. This is called 3D systems-on-chip (3D-SoC). By clever partitioning of the circuits, the power-performance-area can be significantly improved, providing a path to extend Moore's law scaling.

The 3D technology landscape

The continued scaling of microelectronic circuits has allowed the creation of extremely complex systems-on-chip (SoC). At the same time, several specific applications (such as high density memory, high voltage, analog signaling and sensors) have driven technology developments in various directions. In this complex landscape, on the one hand, many electronic systems still consist of a multitude of components that are packaged individually and interconnected using conventional printed circuit boards.

On the other hand, more advanced 3D integration and interconnect technologies have emerged, reducing the size of the electronic systems, and enabling faster and shorter connections between their sub-circuits. These abilities have made 3D integration one of the techniques that will allow the industry to keep pace with Moore's Law.

In this 3D technology landscape, several classes of integration can be defined. The main difference between these classes is related to the level of partitioning, in other words, the level at which the systems are 'cut' into different pieces in the interconnect hierarchy. Each of these classes requires different process schemes and 3D integration techniques, achieving progressively smaller contact pitches. A first class is what we call system-in-a-package (or SiP), where the partitioning is done at package level by stacking packaged devices on top of each other, or by integrating multiple die in a single package.

Among the technologies used to realize SiPs are package-to-package reflow and fan-out wafer level packaging, in combination with solder balls. Contact pitches of current solutions are rather coarse, in the 400 micrometer range. Imec's research into new approaches to fan-out wafer level packaging intends to increase the interconnectivity of this class of SiP by a factor 100, targeting interconnect pitches of 40 micrometer. The technique is applied (for example) for mobile applications such as smartphones.

In a second class, called 3D stacked IC or 3D-SIC, the partitioning is done at die level and individual dies are stacked on top of each other. 3D-SIC partitioning is achieved using die-to-interposer stacking or die-to-wafer stacking, where finished dies are bonded on top of a fully processed wafer. Dies are interconnected using through-Si vias and microbumps. In the industry, microbump pitches down to 40 micrometer are achieved today. Imec's research goal is to bring this pitch down, well below 20 micrometer, as such increasing the interconnectivity by one to two orders of magnitude. A typical application example is wide I/O memory, where vertically stacked DRAM chips (3D-DRAM) are connected on a Si interposer together with a logic die and an optical I/O unit.

3D systems-on-chip: higher density through heterogeneous integration

With advanced CMOS scaling, new opportunities for 3D chip integration with even higher interconnect densities and smaller pitches are possible. Rather than realizing a SoC as a single chip, it has now become possible to realize different functional partitions of a SoC circuit. Stacking such partitions results in a so-called 3D system-on-chip. These are packages in which partitions with varying functions and technologies are stacked heterogeneously, with interconnect densities below 5 micrometer. The system partitioning can be done at different levels of the interconnect hierarchy – at the global wiring level (long wires, cross chip), intermediate wiring level, or local wiring level (short wires, interconnecting e.g. intra-core modules).

The main technological approach to stack these partitions is wafer-to-wafer bonding – either through hybrid (via middle) wafer-to-wafer bonding, or with dielectric (via last) wafer-to-wafer bonding techniques. This is achieved by a highly precise alignment of top and bottom wafers that are then bonded. Recently, excellent results in wafer-to-wafer overlay accuracy have been obtained, for both hybrid bonding (1.8 micrometer pitch) and dielectric bonding (300nm overlay across wafer). Accurate overlay is needed to align the bonding pads of the stacked wafers and it is essential to achieving a high yield.

One of the main drivers for 3D-SoC development is functional repartitioning of high performance systems. In such approach, different parts of the SoC system are realized using tailored technologies in different physical layers, but remain tightly interconnected. The trend in processor development, for example, has been towards an ever increasing number of cores. This trend will continue, enabled by scaling towards the 7nm and 5nm technology nodes. However, more cores will also need more on-chip memory. And all this will result in more overall silicon area that is needed, plus more back-end-of-line requirements, and hence, increasing wafer cost. One way to cope with this trend is by functional repartitioning of the processor followed by heterogeneous 3D integration.

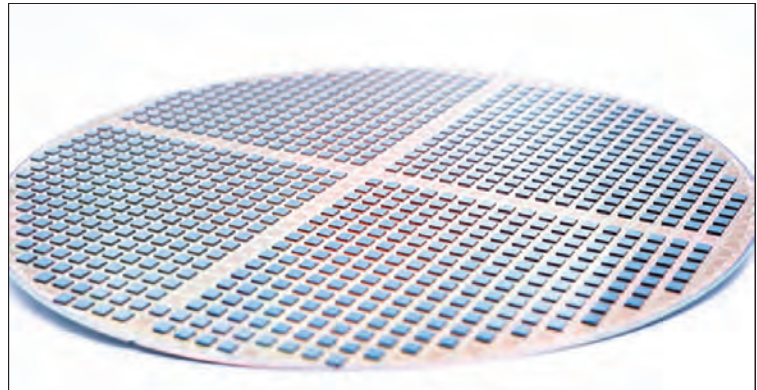


Fig 1: 3D stacked IC: processed wafer with chips stacked on top using a die-to-wafer process.

Power, performance, area and cost benefits through clever partitioning

Imec researchers use physical design tools to find an optimal 3D functional partitioning of high-performance systems. A typical example is a larger SoC which consists of many cores, the L1 memories associated with these cores and L2 memory that is shared. This can be redesigned so that all the memory is brought to a top die, with the logic moved to a bottom die. This approach ends up with two die, half the size of the original big die, which improves the system's yield (defined as the percentage of good die on a wafer) which decreases as a function of the die's area. In addition to this cost and area gain, the length of the wires between the processor and the memory

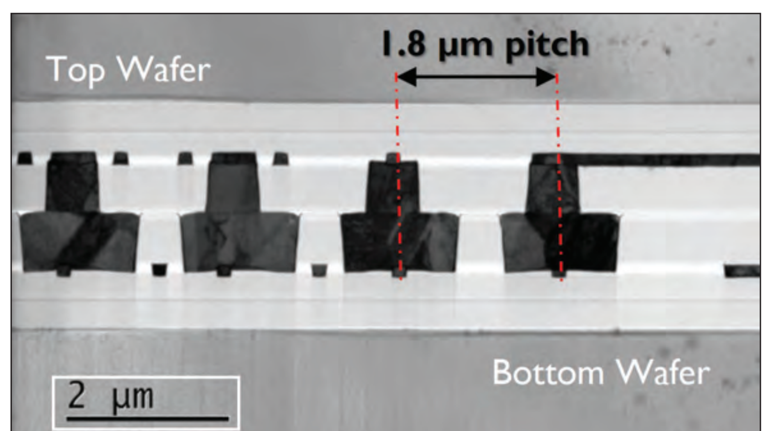


Fig 2: Wafer-to-wafer bonding with 1.8 micrometer pitch overlay accuracy.

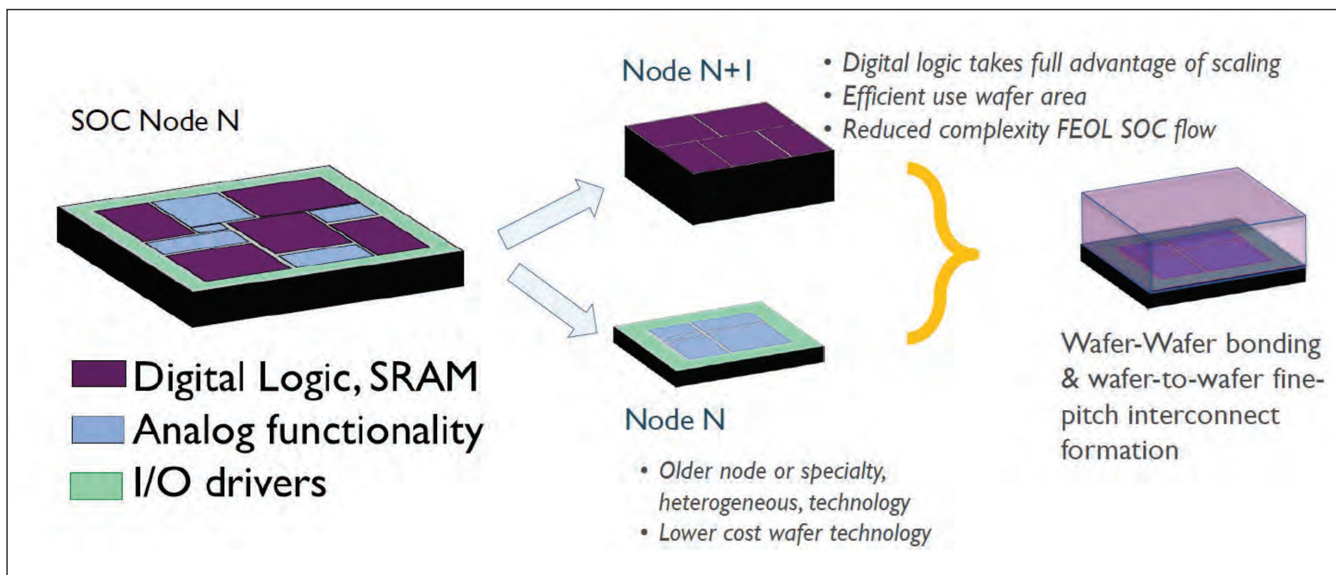
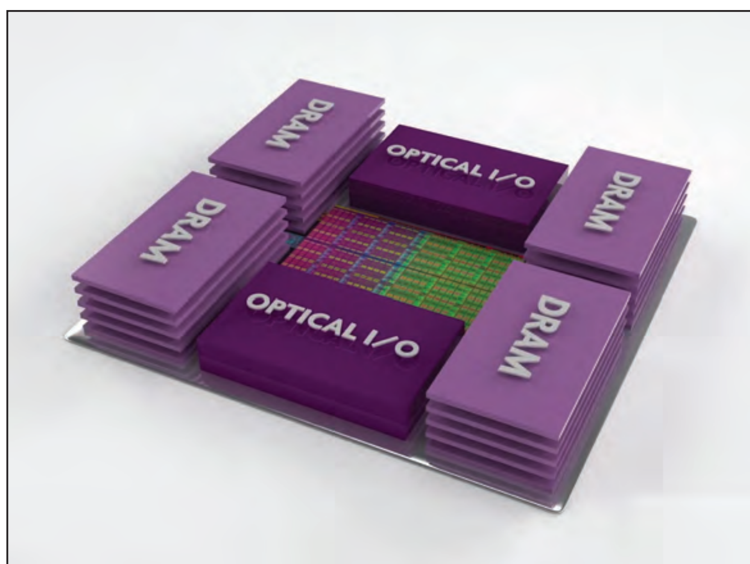


Fig 3: Illustration of 3D- SoC partitioning based on the scalability of the technologies.

becomes significantly shorter after stacking the two dies, giving additional gain in power and performance. These die-related gains are typical for anything that is 3D.

But there is more. For the original 2D die, the wafer manufacturing process needs to be optimized for both logic and memory technologies. By splitting the die into two dies, one for logic, one for memory, the processes can be tuned for logic and memory separately. And this will further improve the yield. Also, logic typically requires a large number of metal layers (typically 12 to 14), while memory typically requires fewer layers (5 or 6). This implies that the wafer containing the memory part can now be made relatively cheaply – as the back-end-of-line cost makes up a large part of the total wafer cost. Partitioning can be further revised by making even smaller functional IP blocks and by rearranging them into another shape that would further reduce the wire length.

Fig 4: Illustrating principles of multicore processor repartitioning.



The re-partitioning should, however, be done in a clever way to avoid over-partitioning. For example, if a circuit consists of sub-circuits that are extremely interconnected, ripping them apart may result in too many wires that go up and down between the two resulting dies. And that would cause more problems than repartitioning can solve.

A clever way of partitioning may be based on the scalability of the different technologies, for example. While we keep on scaling transistors according to Moore's Law, it gets more and more difficult to achieve an overall process which encompasses everything of the SoC. For these applications, partitioning in function of scalability turns out to be an interesting solution. If a technology is split into parts that highly scale (e.g. digital blocks) and parts that hardly scale (e.g. analog blocks and I/O drivers), you can optimize the die with highly scalable technologies separately from the die containing less scalable technologies.

3D Integration: A landscape and not a roadmap

3D-SoC sand 3D-ICs complete imec's 3D technology roadmap that outlines different paths for 3D integration. However, imec researchers refer to a 3D technology 'landscape' when discussing evolutionary paths instead of a 'roadmap'. A technology landscape is not like a traditional 2D roadmap that can be read from left to right. For 3D, there are a lot of technology options that will coexist, even within the same system. The technologies differ in where they intercept the hierarchy of interconnects on the chip, in other words, where we divide-up devices and create 3D interconnectivity. And this will determine the required 3D pitch. So, the future of circuit design evolution is more like a collection of technologies that allow a system to be integrated into a much smaller form factor, with increased performance and lower manufacturing cost.

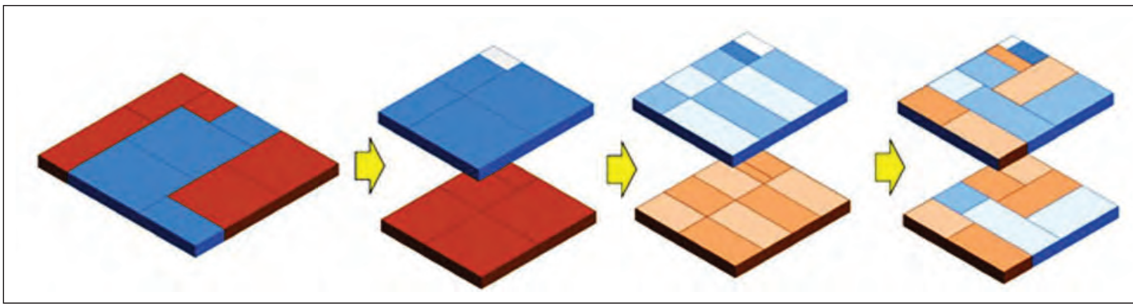


Fig 5: From a 2D- SoC (multiple large IP blocks) to a 3D-SoC (IP blocks re-arranged across two chip levels and further IP block sub-partitioning).

Further down the road: 3D-ICs

Eventually, the drive to achieve smaller, faster, higher performance ICs will lead to even tighter integration, such as stacking transistors on top of each other, achieving contact pitches as small as (a few) 100nm. Imec is exploring ways of stacking, for example, nMOS transistors on top of pMOS transistors – or vice versa – instead of putting them next to each other; this stacking approach is also known as CFET (or CMOS FET). To accomplish this involves a completely different approach not utilizing through-silicon-via-like processes; it will be realized through sequential processes or layer transfer processes. The alignment of the two transistors in a CFET should not be wafer alignment defined but lithography defined. A typical application is an SRAM cell in a 3D format, which will have a much smaller footprint than its 2D equivalent.

Another example is 3D NAND technology in which a single channel contains multiple transistors or bits (up to 58), integrated into one single structure, making the approach a few levels of granularity lower than 3D-SoC partitioning. It is one of the future paths imec is exploring that has a potential to extend Moore's law scaling.

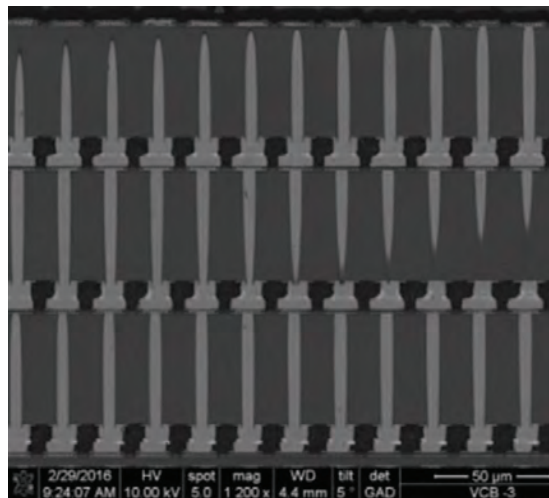


Fig 7: 3D-die stack: four die, connected vertically using 20 micrometer pitch microbumps and 5 micrometer diameter, 50 micrometer deep TSV connections.

	3D-SIP			3D-SIC	3D-SOC			3D-IC
3D Technology	"PoP"	"Chip last"	"Chip first"	Die stacking	Parallel W2W		Sequential FEOL	
3D-Wiring level	Package I/O	Chip I/O Interposer I/O	Chip I/O	Global	Semi-global	Intermediate	Local	FEOL
				Chip BEOL Wiring Hierarchy				
Partitioning	Functional unit	subsystem	Embedded die	Die	Blocks of standard cells		Standard cells	Transistors
Technology	Package-to Package reflow	Multi-die SIP 3D/2.5D stack	FO-WLP Embedded die	3D D2D, D2W 2.5D Si-interposer	Wafer-to-Wafer bonding: Hybrid bonding	Via-last	Active layer transfer or deposition	
2-tier stack Schematic								
Characteristic	Solder ball Stack	• C4, Cu-pillar • Si-Organic • Through-Mold-vias	• Bumpless • Si-RDL • Through-Package-vias	• µbump • Si-to-Si • Through-Silicon-Via	BEOL between 2 FEOL layers; Overlay 2nd tier defined by W2W alignment/bonding		Overlay 2nd tier defined by litho scanner alignment	FEOL stack
Contact Pitch	400⇒350⇒300µm	120⇒80⇒60µm	60 ⇒40 ⇒20µm	40 ⇒20 ⇒10⇒5µm	5µm ⇒ 1 µm	2 µm ⇒ 0.5 µm	200nm ⇒ 100 nm	< 100 nm
Relative density:	1/100⇒1/77⇒1/55	1/9⇒1/4⇒1/2.3	1/2.3 ⇒ 1 ⇒ 4	1 ⇒ 4 ⇒16⇒ 64	64 ⇒ 1600	400 ⇒ 6400	$4\ 10^4 \Rightarrow 1.6\ 10^5$	$> 1.6\ 10^5$

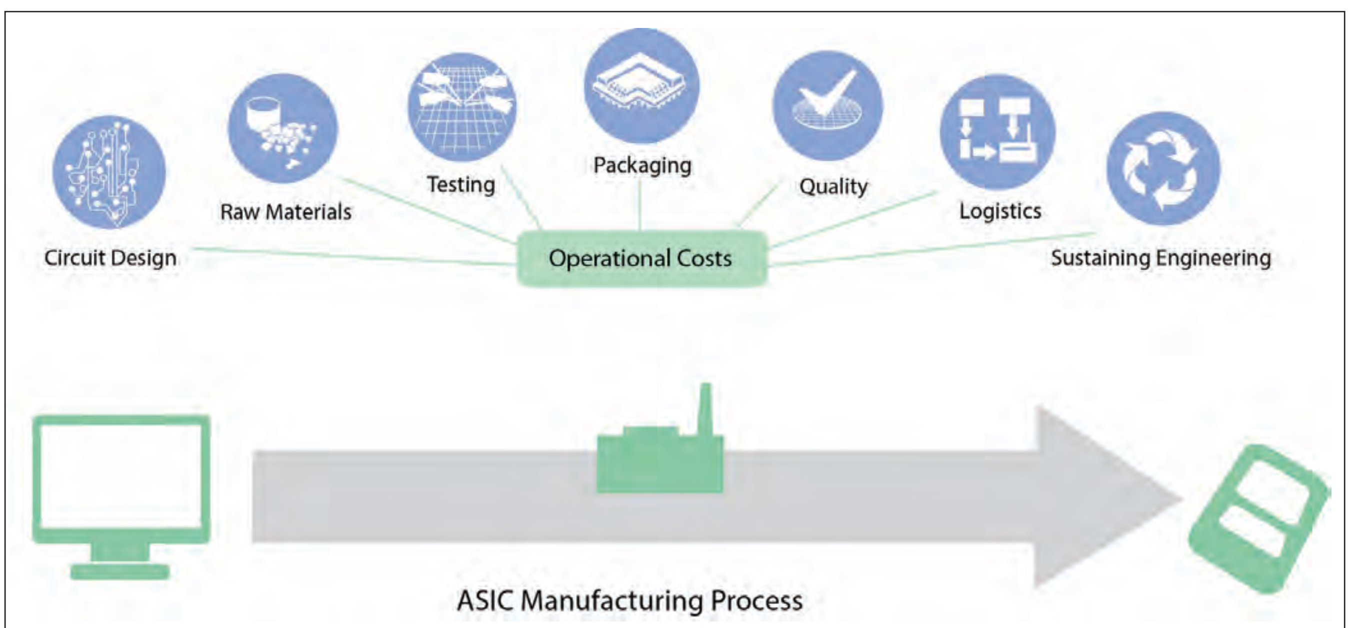
Fig 6: Imec's 3D interconnect technology landscape.

Speed IoT product development and reduce risk with outsourced operations

New manufacturing techniques and device-level security measures can bring secure Internet of Things (IoT) devices to market more rapidly than ever before. Michel Villemain, CEO, Presto Engineering, Inc.

APPLICATION SPECIFIC integrated circuits (ASICs) are cheaper and easier to make than ever before, and the range of applications for which they offer significant benefits is expanding rapidly, especially with the emergence and growth of the Internet of Things (IoT). While it is now quite possible to bring a new ASIC to market for less than $5 million dollars (USD), the complexity of manufacturing silicon products remains daunting for many potential product developers. Producing an ASIC requires expertise in many different disciplines. In large companies these needs are typically met by a team of experts, but assembling such a team can be prohibitively costly and time-consuming. This need for manufacturing expertise has led to the creation of "outsourced operations" companies like Presto Engineering that provide turn key services to manage the entire production process, from tape-out of the final design to the delivery of the finished, tested product.

By reducing the risk, cost, time and difficulty of the process, these companies are playing a key role in accelerating the proliferation of application-specific semiconductor solutions.



Manufacturing complexity

The wafer fabrication processes alone are arguably the most complex manufacturing process ever conceived. And wafer fab does not include additional aspects of the overall production process, such as qualification, the procurement of raw materials, testing, packaging, logistics, quality assurance, and sustaining engineering.

Complexity can be considered another aspect of cost – as it impacts both the cost of execution and the potential cost of execution errors. Just finding the right experts can take considerable time, but proceeding without them risks delay or failure in production. In either case, the promised return on a large development investment can evaporate quickly if a delay enables the competition to be first to market.

The electronics market waits for no one

Being first to market with a new product allows the manufacturer to collect a price premium and capture market share. Historically, leading semiconductor companies have built their success on being first to market with the latest performance-enhancing innovations, time after time. Now we are looking at a market where many of the most significant growth opportunities will be in specialized segments. These will require application specific products that will be conceived and produced by companies that are not primarily semiconductor manufacturers, but makers of cars, medical devices, smart building appliances, industrial systems, or something else no one has thought of yet. How are these product developers to confront and master the complexity of the semiconductor manufacturing process?

Large companies, like automotive manufacturers, have traditionally met the need for ASICs by creating a dedicated organization, often called an "operations" department. Starting with a completed design, their sole task is to manage the production of the specialized devices they need. Such a team necessarily includes experts in planning, purchasing, logistics, IT, quality assurance, product engineering, device engineering, failure analysis, and test engineering. For a small company, with a game-changing new product idea, the cost and time required to assemble such a team can be fatal. If a competitor beats you to market you might not get a second chance. Outsourcing operations offers an affordable, low-risk solution.

Reduce risk – by outsourcing these operations, you gain from the management and technical experience of a team of experts with well-established relationships to resource and service providers.

Get to market faster – maximize margins and return on investment by commanding premium prices. Take valuable market share and establish a strong competitive position. Avoid delays required to assemble experts for an in-house team.

Minimize start-up costs – reduce capital expenditures: the IT infrastructure alone – enterprise resource planning (ERP), manufacturing execution system (MES), disaster recovery planning (DRP), and security – needed to manage a semiconductor production operation can cost a million dollars. Outsourcing operations converts fixed costs to variable expenses, minimizes headcount and avoids the dilution of equity required to recruit top talent.

Optimize production processes – outsourced operations can match the device requirements to the best fabrication process to ensure optimal performance at the lowest cost. And after wafer fabrication, different technologies still require different skill sets. For example, radio frequency testing, especially in the millimeter wave bands that are now coming online, is still as much an art as a science, requiring specialized knowledge and, frequently, customized fixturing. Secure devices must be provisioned in secure facilities with secure communication protocols.

Outsourcing and security

As IoT products proliferate, manufacturers and the industry in general have developed a heightened awareness of the security risks inherent in any connected device. Though specific requirements do vary from application to application, ultimately, every connected device needs some level of security. Thus, product developers are faced with yet another addition to the expense and complexity of producing their devices.

A variety of security solutions exist, ranging from software-only approaches to the addition of secure "chips" and the inclusion of secure capabilities in off-the-shelf controllers or custom ASICs.

All of these solutions share a need for secure provisioning – the introduction in each device of the "secrets" essential for secure identification, authentication, communication, processing and storage. Outsourced operations for IoT products clearly must include secure provisioning.

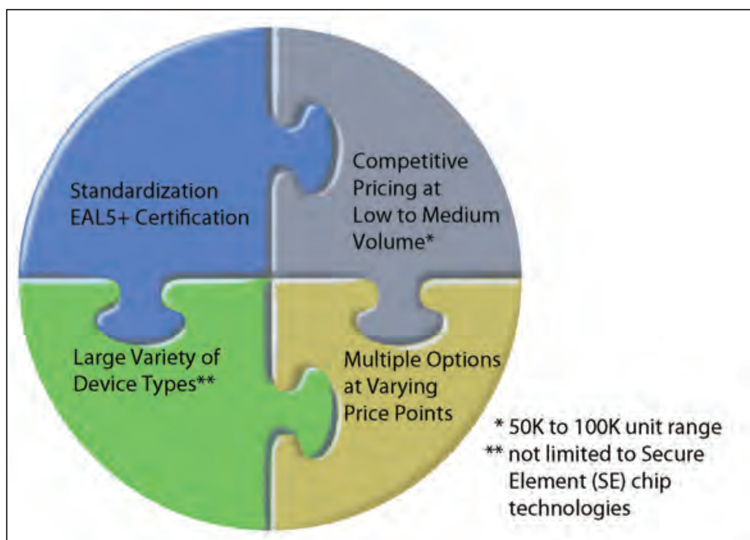
Michel Villemain, CEO, Presto Engineering, Inc.

Important security considerations when outsourcing production for an IoT device include:

Hardware – Although software-only solutions are available, tying security to hardware adds confidence and makes intrusion more difficult. Hardware solutions include: adding a separate secure chip (Secure Element or similar technology), implementing secure capabilities included in a stock MCU, or incorporating security functionality in a custom designed ASIC. MCU and ASIC based solutions can reduce costs significantly. A key question to consider before beginning a new program: what is the most cost-effective solution given the technical and security requirements and anticipated unit volume of the application?

Trust – All hardware configurations require provisioning by a trusted partner. Indications of trust include that partner's level of investment in the owned physical plant and equipment, history and volume of secure operations, and staff experience in secure applications.

What stake does the provisioner have in maintaining a reputation for security? What investments have they made to secure that reputation? Is trust an essential component of their business model and brand equity?



Secure and Flexible Provisioning Services

Facility – Is the provisioning facility designed for both physical and data security? Can it ramp up in volume for IoT growth?

Certification – Does the provisioner conform to industry standards including the Common Criteria for Information Technology Security Evaluation (ISO/IEC 15408)? What Evaluation Assurance Level (EAL 1-7) certification has the provider achieved? Are there regular audits and re-certifications?

Equipment – Does the provider have the equipment needed to handle the particular solution, i.e.: wafer, package, circuit board?

Flexibility – Can the provisioning process be configured to provide a cost-effective solution that meets security requirements and budgetary constraints?

Ideally, an outsourced provisioner should offer certain key capabilities:

- A standardized and certified (EAL5+) secure process.
- The ability to provision a wide range of device types, form factors and security technologies.
- Competitive pricing at low and medium volumes with the ability to scale to larger volumes as required.
- The flexibility to configure the provisioning process and infrastructure to meet varying security and budgetary requirements.

Conclusion

ASICs offer superior value and performance, especially for IoT products. The availability of less expensive fab capacity on mature process technologies has significantly reduced their cost. It is now possible to design and build an ASIC for about $5 million dollars, which increases the applications space in which they provide an economically attractive solution.

Outsourcing operations to produce ASICs manage the risks associated with the complex semiconductor manufacturing process, reducing costs, increasing value, and minimizing risk. Security and secure provisioning must be essential considerations in defining any outsourced operations solution.

NEW VAT BUTTERFLY
ULTRA-FAST ACTUATION IN A TENTH OF A SECOND – HIGH THROUGHPUT

- Position only control version – ideal for simple throttling applications
- Sealing and non-sealing type
- Heater options

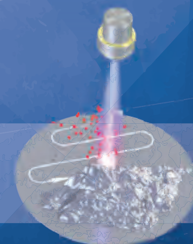
www.vatvalve.com

HIGH-END EQUIPMENT
FOR HIGH-TECH INDUSTRIES

IonScan
Systems for ultra-precise film thickness trimming and ion beam figuring

- Contactless trimming or figuring
- Optimization of error distributions by the factor of 10 and more
- Ion beam process applicable to almost all materials

Ion Beam Technology



Visit us at SEMICON Europa
November 14-17, 2017 in Munich/GER
Booth B1-1815

www.meyerburger.com

Flexible hybrid electronics:
a new paradigm for semiconductors

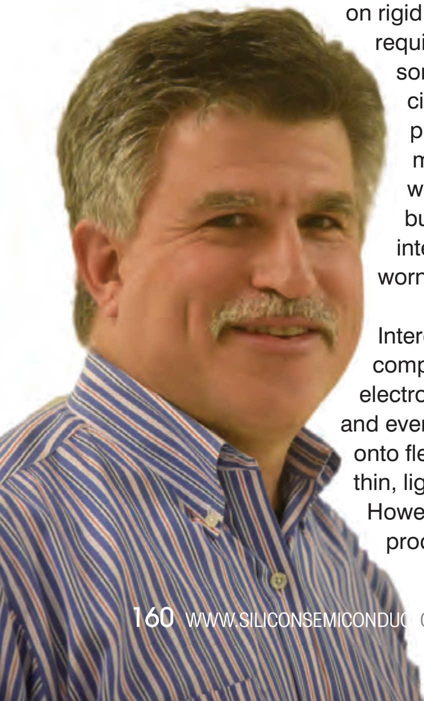
As printed electronic circuits continue to evolve, the NextFlex consortium promotes a hybrid approach to accelerate the development and commercial viability of flexible ICs and systems.

By: Paul Semenza, Director of Commercialization, NextFlex.

The limitations of rigid electronics

The fundamentals of electronics manufacturing – packaged semiconductors and other components assembled onto printed circuit boards produced in high-temperature processes – have not changed for decades. This process results in durable, reliable systems and is widely available from numerous suppliers. The process is well suited for computing- and memory-intensive applications such as servers, communications systems, industrial process equipment and other installed systems.

As interest has increased in devices for Internet of Things (IoT) applications, the limitations of established approaches have become apparent. Many IoT devices must necessarily be thin and lightweight, and often must be flexible (to accommodate movement of the body or of systems) or conformable (to blend into curved structures). Packaged components on rigid circuit boards are not able to meet these requirements. Manufacturing has evolved somewhat with the development of rigid-flex circuitry, in which flexible circuit substrates provide a backbone of wiring with rigid multilayer circuit sections built up as modules where needed. This can enable some flexibility, but does not allow for the electronics to be fully integrated into clothing or other materials, or worn directly on the body.



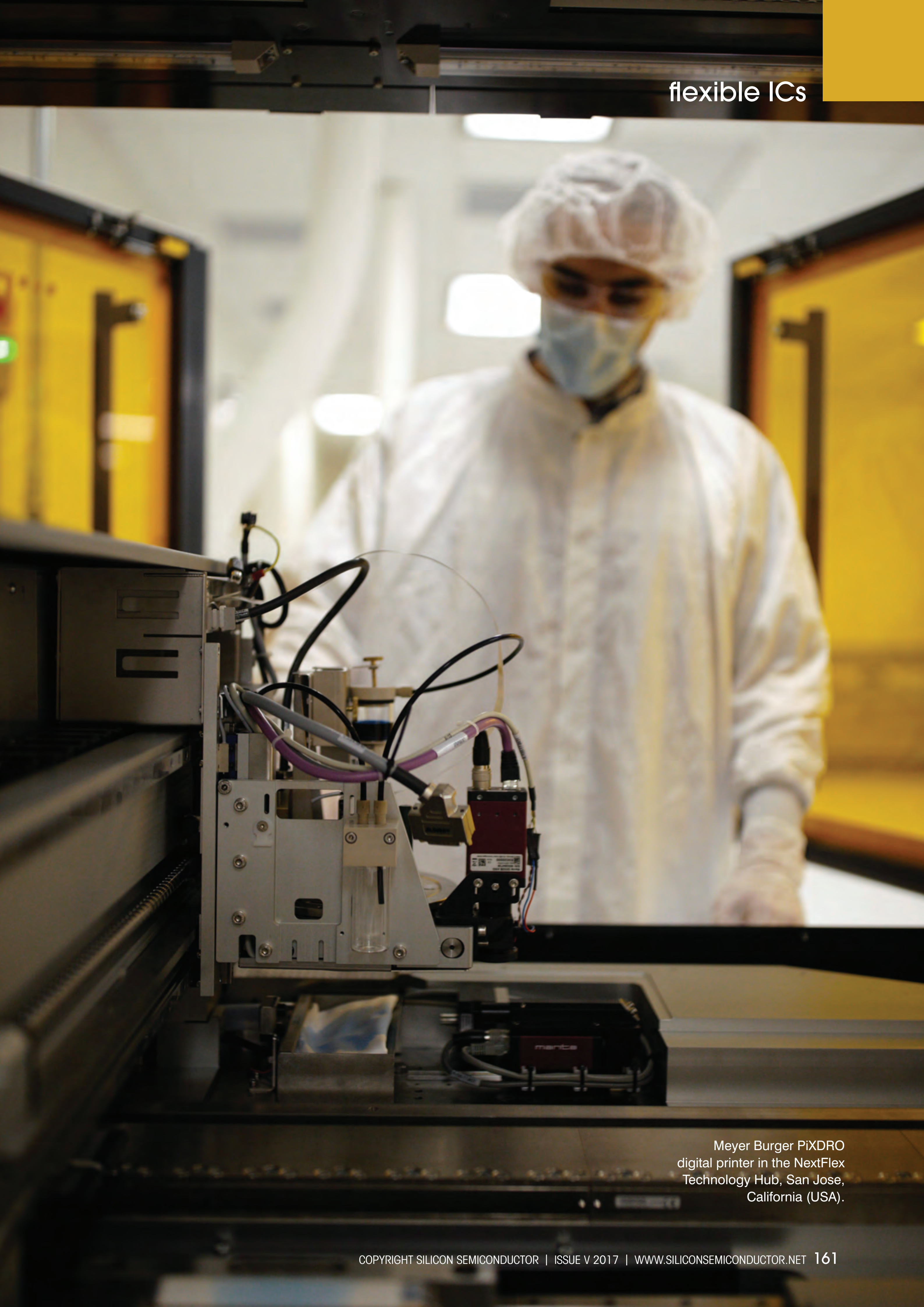
Interest in flexible electronics has led many companies and research groups to pursue printed electronics, in which interconnect, passive devices, and even semiconductors are fabricated directly onto flexible substrates. These processes enable thin, lightweight, and flexible electronic devices. However, the use of printing or other additive processes to fabricate semiconductors has proven to be very limited, lagging the density achieved by photolithography by many orders of magnitude.

Getting electronics out of the box

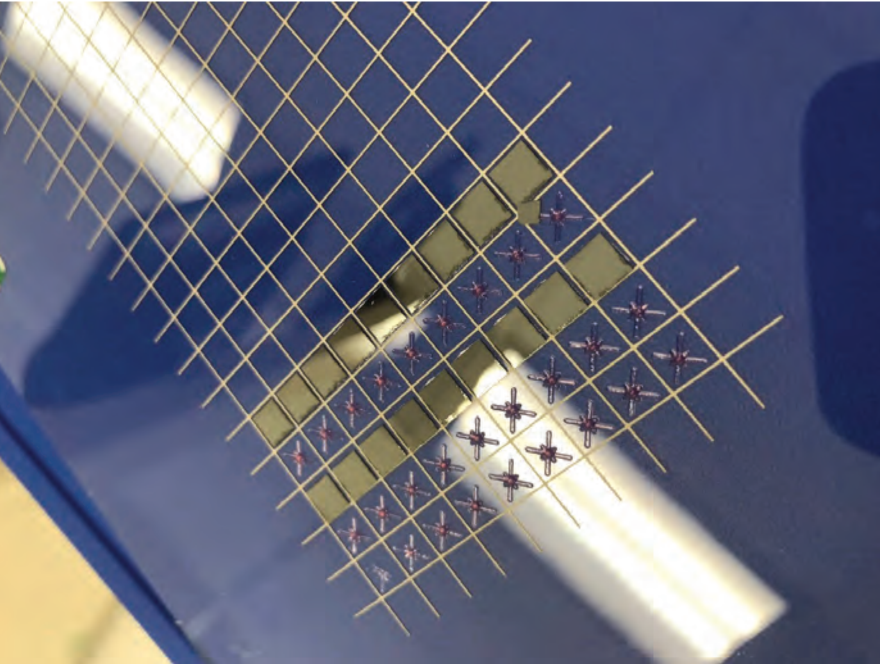
New forms of electronic manufacturing are required to create intelligent devices that can sense, take action, and communicate in real time while being integrated into the real world. Whether the operating environment is on the human body, the surface of a vehicle, precious cargo in transit, or a robotic system, these and many other environments need a new approach. Flexible hybrid electronics (FHE) is an approach that utilizes electronic printing and other additive techniques in conjunction with bare semiconductor die to create thin, flexible circuits. Starting with a flexible substrate, such as plastic or polymer film, metal foil, fabric, paper, or even thin versions of glass or ceramic, low-temperature printing and additive processes can be used to create interconnects, sensors, antennas, passive components, and some active devices. Bare semiconductor die that have been thinned (to a thickness of 50 microns or less) are then integrated into the printed circuitry and the system is encapsulated.

The FHE approach provides significant benefits. Because it utilizes semiconductor devices, it enables system performance equivalent to rigid PCB-based solutions that purely printed electronics approaches are not able to achieve. At the same time, the combination of flexible substrates, printing, and thinned semiconductor devices results in system form factors that can be bent, flexed, stretched and conformed to non-planar surfaces.

What does this mean for the silicon supply chain? The FHE approach creates opportunities for semiconductor device and electronics manufacturers



Meyer Burger PiXDRO digital printer in the NextFlex Technology Hub, San Jose, California (USA).



Thin die being attached to flexible substrates at NextFlex

to address emerging applications that cannot be satisfied by existing assembly approaches. New products envisioned for human performance monitoring, patient monitoring, structural monitoring, preventative maintenance, asset tracking, integrated array antennas, soft robotics, and assistive technologies such as exoskeletons will not be possible using packaged semiconductors on printed circuit boards. By embracing FHE manufacturing, supply chain participants will be able to build new lines of business.

Because FHE processes are low temperature and additive in nature, manufacturing and assembly capabilities can be built as needed, and importantly, where they are needed. Also, FHE manufacturing can be scaled from prototyping to volume manufacturing as needed. Small-scale investments can enable rapid prototyping capabilities, while larger investments will enable manufacturing close to customers and markets.

Taking advantage of the potential of FHE manufacturing will require changes to the semiconductor supply chain. The existing supply chain is built on the assumption that almost all semiconductor devices are packaged and assembled onto circuit boards. The development of FHE manufacturing requires that bare semiconductor die, in many cases thinned to 50 microns or less, are available for assembly.

Equipment and processes for thinning wafers up to 300 mm are available, but in most cases this equipment is embedded in a supply chain that involves thinning, singulation, and packaging. To take advantage of the new markets enabled by FHE manufacturing, semiconductor device manufacturers will need to either develop or support a sales and distribution network for thin die, or to sell fully manufactured wafers directly to FHE manufacturers, who would then thin wafers, singulating them into die.

Another area of opportunity will be in assembly equipment. Unlike surface-mount technology, in which packaged components are soldered to circuit boards at high temperatures, FHE assembly involves placement and attachment of thin, bare semiconductor die (and possibly other components) onto thin sheets of polymers or other materials at low temperature. This requires specialized handling and bonding techniques not widely available now.

NextFlex: enabling FHE manufacturing through collaboration

Many of the fundamental materials and technologies for FHE, such as thin substrates, high-resolution printing, and bare die assembly, already exist in some form. What has been missing is an effort to integrate these disparate technologies, demonstrate their feasibility, and create the standard processes, design rules, and other underlying capabilities required for a robust supply chain. This drove the creation of NextFlex in 2015, under a contract with the Department of Defense, to serve as a catalyst for the development of a flexible hybrid electronics manufacturing ecosystem in the United States.

By bringing together dozens of companies, universities, research centers, and government agencies into a public-private collaborative research consortium, NextFlex has created a forum to tackle common FHE industry challenges. In just over two years of operation, over 80 industry, academic, and non-profit organizations have joined NextFlex as members, which enables them to participate in and share results of research projects.

NextFlex members create roadmaps for manufacturing processes and application needs and identify key performance gaps, which are then addressed through collaborative research projects funded by NextFlex, with cost sharing by the project team and other organizations. Currently there are 24 ongoing projects, funded at $45 million (including NextFlex funding and cost sharing), and is in the process of selecting a third round of projects. Sample current NextFlex funded projects in human health and performance monitoring include: Flexible Smart Wound Dressing; Flexible Oral Biochemistry Sensing, and Attaching Ultra-thin ICs onto Printed Flexible Substrates for Wearables.

To facilitate project work and technology development, NextFlex has constructed a pilot manufacturing and prototyping facility in San Jose, CA, which also serves as a testbed for ongoing and completed collaborative projects. Finally, NextFlex conducts education and workforce development activities, to draw K-12 and college students into FHE manufacturing, and to support U.S.-based manufacturers needs for a trained manufacturing workforce.

www.EVGroup.com

Laser Debonding Solutions for Advanced Packaging

- High-throughput equipment solution for low-temperature debonding of wafers and panels
- Laser system with minimal consumable costs combined with proprietary optical design for excellent beam reproducibility
- Open adhesive platform – laser debonding solution compatible with several material systems

Visit us at
SEMICON® EUROPA
Booth B1-1424

EVG®850 DB

GET IN TOUCH to discuss your manufacturing needs
www.EVGroup.com