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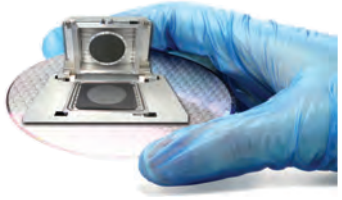
Brewer Science and next-gen solutions

ATV's new path to better device bonds



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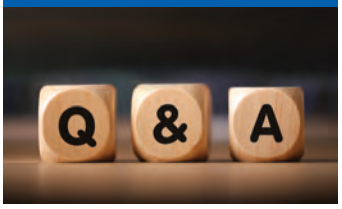

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editor's view

By Mark Andrews, Technical Editor

2019: A wild ride in semiconductor manufacturing

AS 2017 counted down, most industry watchers pondered what 2019 might hold. 2017 had quite literally set records: chip sales grew nearly 22 percent while fab tool sales set records quarter after quarter. 2017 had been amazing.

While 2019 sales could not equal 2017 figures, it did not disappoint in terms of solid performance amidst many twists and turns. And growth—even though not at 2017 levels—was still evident. Overall 2019 semiconductor sales were mostly strong through third quarter even as tool sales started to slide. We'll soon see how the industry fared against a backdrop of international trade disputes, tariffs, fears and real-world resets.

This edition of Silicon Semiconductor is dedicated to 2019's major industry news. We examine the highs and lows, ever mindful that early predictions often proved faulty. One prediction that did come true was a rebalancing across memory chip markets; supply caught up to demand. Another came after what some analysts called Apple's 'experiment' with tier one phone pricing. The market seemed to say that (USD) $1,000+ was a bit much for even the world's most advanced smartphone. And yet, Apple showed what a truly advanced 3D facial recognition system could do compared to 2D systems. At least for now.

2019 also saw realization of how major manufacturing economies (such as China and the US) can impact global manufacturing when two '800 pound gorillas' don't agree about intellectual property, market access, and technology transfer. Tensions between the US and China were already ratcheting up by mid-2019. Deteriorating relations led to shock waves in

their respective financial exchanges. Once US President Donald Trump and Chinese President Xi Jinping met in late November at the G-20 summit without reaching a hoped-for accord, tensions increased further, only to be topped on 1st December when Canadian officials, at US request, detained Huawei's CFO. The China-US trade war, combined with a partial US governmental shutdown over budget disputes, sent US stock exchanges on their wildest December ride in market history.

What hope does 2019 hold? Plenty. Despite 2019's negatives, sales were strong and positive news outweighed the bad. While no one can accurately predict when and how the US-China trade dispute will end, it bears remembering that compromise is crucial in settling any disagreement. As 2019 unfolds, expect ups and downs; but also expect solutions, innovation and cooperation. When we actively pull together, nothing can tear us apart.

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Published by Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. T: +44 (0)2476 718 970 F: +44 (0)2476 718 971 E: info@angelbc.com

US mailing information: Silicon Semiconductor is published four times a year for a subscription of $90.00 by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts, WD17 1JA, UK. Periodicals postage paid at Rahway, NJ. POSTMASTER: send address changes to: Silicon Semiconductor, c/o Mercury International Ltd, 365 Blair Road, Avenel, NJ 07001.
Printed by: The Manson Group. © Copyright 2018. ISSN 2050-7798 (Print) ISSN 2050-7801 (Online).

VOLUME 40 ISSUE V 2018

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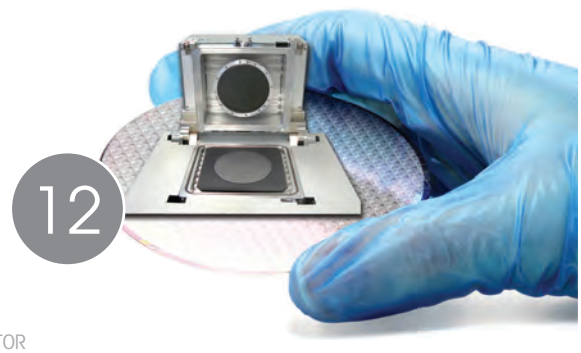

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Brewer Science

delivers next-gen DSA and WLP solutions

Traditional CMOS scaling faces compound lithographic challenges at each new node. Brewer Science's materials experts are reducing complexities and improving performance through new directed self-assembly innovations, while enabling packaging advancements with its temporary wafer bonding portfolio for WLP. Whichever direction the industry pivots, Brewer Science offers solutions.

THE ROAD to next generation semiconductors becomes increasingly complicated at each new node. Geometric CMOS scaling worked well through 28nm, but today's 14/10nm devices typically rely on double- or quadruple-patterning solutions plus a litany of other complex techniques to create transistor elements, manage edge roughness and control pitch. Getting smaller isn't getting any easier.

Major semiconductor manufacturers pursuing greater density, high efficiency and better performance have pinned their hopes to extreme ultraviolet (EUV) lithography for transistors below 7nm. But development complications have repeatedly pushed the introduction of EUV to succeeding generations.

Ram Trichur of Brewer Science

Intel, Samsung, TSMC and other major fabs have indicated they will introduce EUV at 7-5nm by the end of this decade. But what comes after 5nm? Will it be affordable and flexible enough to fit wide-ranging circuit requirements? This is uncharted territory where no one can risk multimillion, let alone multibillion, dollar/pound/euro investments.

Many manufacturers are actively seeking alternatives to EUV for myriad reasons including the fact that cost/benefit ratios that have favored incremental lithographic technique enhancements are getting much harder to calculate. As sophisticated tools have driven costs up sharply, manufacturers need mutigenerational benefits to commit resources. Many seek alternatives to market requirements or have explored alternative scenarios to leverage existing capital investments. Some shifted part of their capacity to manufacturing micro electromechanical systems (MEMS) devices that do not depend on 300mm wafer fabs or the most advanced process technology, showing it is possible to create value and strong revenue streams while diversifying product portfolios.

Brewer Science (Rolla, Missouri and worldwide) has been supporting advanced lithographic materials and process technology requirements since 1981 when company founder and CEO Terry Brewer created and delivered antireflective coatings that enabled new lithographic solutions—foundations of today's industry standards. The company continues to pioneer new technologies, including its significant work with temporary wafer bonding (TWB) and debonding solutions.

"In backend manufacturing, we look for technical problems where the material solutions for existing requirements do not meet the future needs of our customers. We offer advanced material solutions that

Brewer Science's manufacturing automation is key to ensuring quality is maintained.

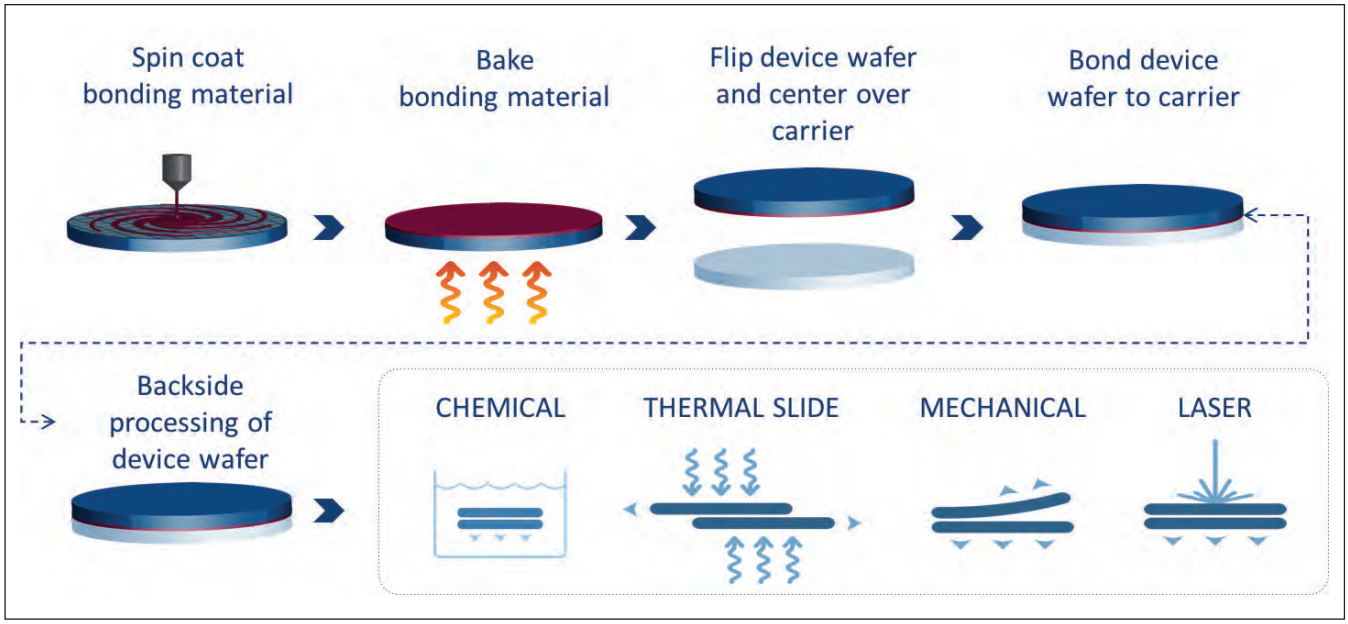
go beyond present day customer requirements by also offering a clear advantage in terms of process simplification, yield improvement and/or throughput enhancement," said Ram Trichur, Director of Wafer Level Packaging Business Development at Brewer Science Inc.

Brewer Science's temporary bonding and debonding techniques are especially applicable in fan-out wafer-level packaging (FOWLP). While the 'chip-first' approach has been in high volume manufacturing for some while, the 'chip-last' approach is still developing. Brewer Science sees many of its product solutions as offering a complete range of options for customers, whichever approach they are taking.

TWB has become the technology of choice for most applications in which a 300mm silicon wafer is thinned, flipped and temporarily mounted on a carrier after which its backside is further processed on the road to producing 3D integrated circuits. Creating and handling thinned wafers is a challenging process; however, thin wafer-based devices allow for better heat dissipation, reduced form factors, greater performance and less power consumption. But thinning involves risks including fragility, stress leading to warpage or cracks, and thermal expansion match issues. After thinned wafers receive backside processing, the temporary mount needs to be smoothly dislodged (debonded) and device wafers need to be cleaned before subsequent processing. Manufacturers typically utilize one of three main approaches to safely and cleanly dislodge a temporary bond: thermal slide, mechanical or laser.

Brewer Science has supported temporary bonding/debonding requirements across multiple device generations and is one of the few companies to support every major type of physical debonding approach. Their products continue to evolve and now include fourth generation solutions for laser systems; they have succeeded in raising the temperature range of these processes up to 350° C.

"We have almost 15 years of experience in temporary bonding materials development and commercialization for the manufacturing of 2.5D, 3D, compound semiconductor, fan-out and other process flows. We realized very early that one product or even one platform of temporary bonding materials may not



TWB process flow showing all major methods of temporary bond release.

be suitable for all of the processes used in advanced packaging applications. Each process flow or device type has a unique set of requirements, and we offer a broad portfolio of bonding materials and release layers designed to support these individual processes. This approach results in maximized customer benefits in terms of delivering simple processes with high yield and low cost of ownership," said Trichur.

The company is seeing growing interest in the latest generation of tools, especially across Asia and most notably in China. While all customers see benefits, some report rather remarkable results, especially when they had previous solutions that were not delivering as needed.

"All of our customers benefit from the advances we deliver, yet some have particularly striking success stories. A manufacturer that was producing compound semiconductor devices and bonding with wax materials had a total yield loss of around 30 percent during backside processing due to the poor thermal and mechanical properties of wax. We introduced a new temporary bonding material, and their yields subsequently increased to over 99%," said Trichur.

Historically, the industry has relied on equipment enhancements to reach the next technology node. Now, materials solutions are stepping in to provide that edge and extend tool capabilities. The OptiLign™ product family is an example of this paradigm shift

Other new device architectures are key to many companies' strategies to either delay or bypass the need for expensive EUV transitions. A new technology seeing widespread development work on the road to commercialization is directed self-assembly (DSA). Brewer Science partnered with Arkema (Grenoble, France) in 2015 to bring first-generation DSA materials to the commercial marketplace. Arkema is a high-performance materials specialist with a global presence and 2016 sales of 7.5 billion euro. The companies' collective goal is to ultimately support device geometries down to 5nm and below so that regardless of the path to next-generation devices that manufacturers choose, Brewer Science will have an advanced solution enabling faster throughput, higher yield and superior performance.

At the SPIE Advanced Lithography 2019 conference (February 2019), Brewer Science announced that it had achieved a new milestone in the support of commercial-quality DSA materials. Brewer Science's new OptiLign™ system includes three DSA materials: block copolymers, neutral layers and guiding layers that Brewer Science and Arkema believe provide a cost-effective path to advanced node wafer patterning processes for feature sizes down to a 22nm pitch.

"Taking OptiLign materials from pilot line to commercial-scale production represents the next significant milestone in making DSA a viable option for

semiconductor manufacturing," said Dr. Srikanth (Sri) Kommu, executive director, Semiconductor Business, Brewer Science Inc. "Historically, the industry has relied on equipment enhancements to reach the next technology node. Now, materials solutions are stepping in to provide that edge and extend tool capabilities. The OptiLign product family is an example of this paradigm shift."

Brewer Science's OptiLign family of DSA products provides all the materials needed for self-assembly. Block copolymers define the pattern. Neutral layers allow the pattern to be formed on each layer. Lastly, guiding layers give the material directional orientation. All the materials are designed to work together for optimal performance, and are dependent on material and surface energy.

Through its partnership with Arkema, Brewer Science has tapped into a way to deliver DSA materials that allows for consistent feature sizes via a unique polymer production process. Critical to high-volume manufacturing is the fact that this new process enables the type of scaling needed to support an entire technology node, as well as unique polymer quality and reproducibility, all of which sets OptiLign materials apart from competing solutions.

Block copolymers (BCPs) are polymers containing two (or more) polymers joined together that will spontaneously segregate when coated and annealed on a neutral layer. The neutral layer has a surface energy that both blocks will adhere to equally; hence the name neutral layer. However, the features naturally created by BCP are random, so a "guide" is needed to make the BCP go where circuit designers wish.

There are many process flows for guiding the BCP, including creating physical features and aligning the BCP between them (graphoepitaxy), or treating the surface to create areas of the neutral layer that have a preference for one section of the BCP in order to align them (chemoepitaxy). Depending on the BCP and guiding method that are used, DSA can be used to create lines, holes, pillars, and other features.

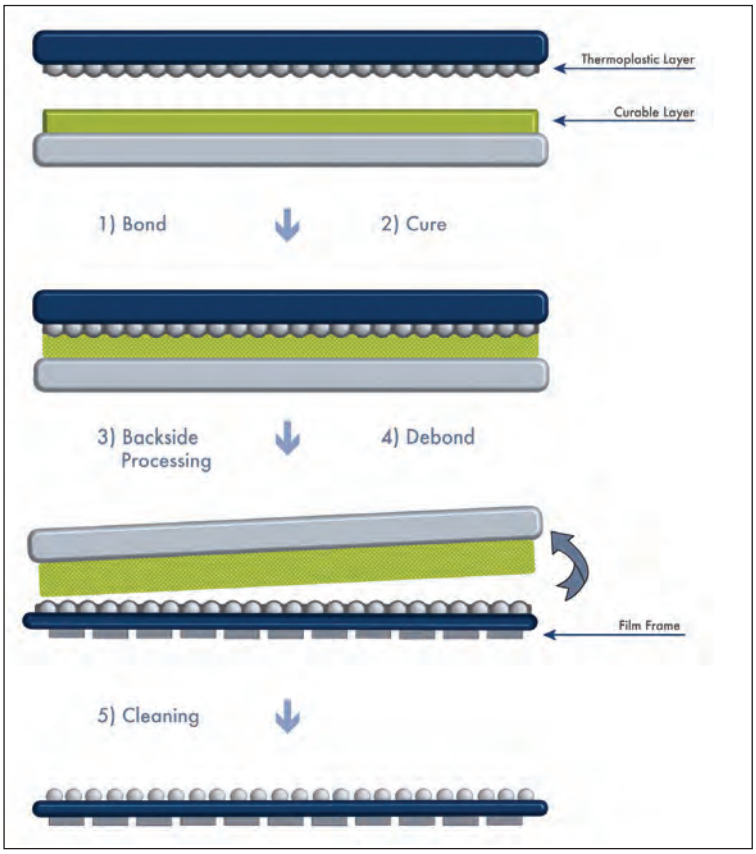
"Feature size is built into the molecular structure of the DSA materials and can vary from batch to batch, so securing a sub-nanometric reproducibility can be challenging," explained Dr. Ian Cayrefourcq, Director of Emerging Technologies, Arkema. "Arkema's special process for formulating large batches of polymers of the same size allows Brewer Science to supply a fab with consistent feature sizes for the technology node's life span."

In July 2017, Brewer Science announced that it had extended its relationship with Arkema to further work towards next-generation DSA materials. Brewer Science scientists have been able to reduce the feature size by 20% compared to the first-generation materials, another milestone towards the ultimate goal of supporting 5nm and smaller features. This benchmark is important since most industry experts agree that extending device scaling without relying on EUV or complex multi-patterning schemes is essential to any new technologies' ultimate success. And DSA offers even more benefits.

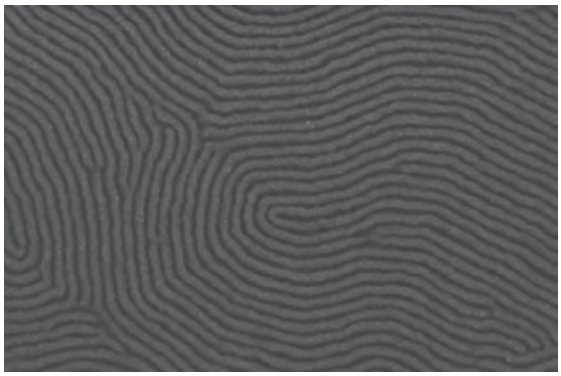
"DSA represents a lower-cost and higher-throughput solution over EUV, but another big cost advantage lies in the reduced mask requirements. DSA still needs lithography and etch processes, but these are lower cost compared to multiple patterning. EUV masks are a significant part of the EUV step cost. DSA also offers a technical advantage in that it can reach lower feature sizes now (compared to) other patterning technologies," said Hao Xu, Director of Semiconductor Business Development at Brewer Science.

Xu also believes that major fabs which have already committed to EUV may conclude that combining DSA with EUV will better support their ultimate goals.

"DSA and EUV are complementary because smaller pitches can be printed with EUV that are not accessible with immersion litho. Smaller pitches means two things: lower multiplication factors can be done with DSA, which leads to a lower possibility for defects. Also, there is the possibility of eliminating the trim etch step in the chemoepitaxy flow when using EUV. EUV can also provide graphoepitaxy templates for contact hole multiplication. It is also important to note that because of the resolution limitations of



Brewer Science Gen4 TB-DB process flow.



9nm lines formed using Brewer Science's next-generation OptiLign™ DSA materials.

EUV at smaller nodes, it is possible that DSA will help stretch out the timing for, or even eliminate, the need for high-NA (numerical aperture) EUV tools," Xu added.

Conclusion

Brewer Science enabled key developments in semiconductor photolithography with its introduction of antireflective coatings. The company grew and expanded to offer a wide range of advanced solutions for global semiconductor manufacturing. Today, Brewer Science products and services support all major approaches to advanced lithography, thin-wafer handling and 3D integration as well as chemical and mechanical device protection and products based on nanotechnology. In its quest to support next-generational / emerging technologies, Brewer Science enables 3D advanced semiconductors through its temporary wafer bonding (TWB) and debonding product lines.

Its latest Gen4 solutions for laser-based applications have elevated working temperatures to 350° C. Recognizing the potential of directed self-assembly (DSA) to revolutionize advanced device fabrication, Brewer Science partnered with Arkema in 2015 to introduce commercial-ready OptiLign™ materials for DSA features down to 22nm pitch.

That partnership, extended in 2017, is positioned to continue innovation with next-generation solutions for even smaller DSA features; on-going work targets supporting devices to 5nm and below. As manufacturers seek alternatives to multi-pattern lithography that are less complex and costly, or for those seeking to delay or augment extreme ultraviolet (EUV) lithography, Brewer Science offers alternatives that extend device scaling while reducing costs, increasing performance and simplifying complex advanced node manufacturing.

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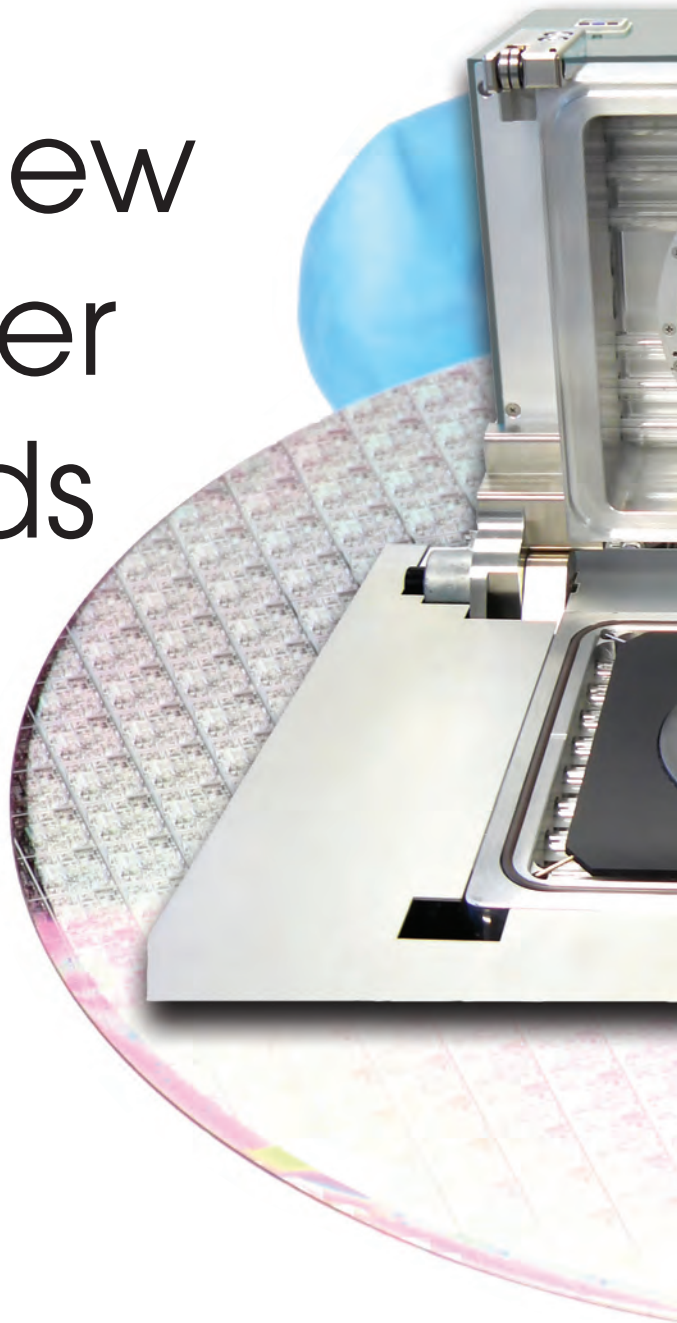
ATV charts new path to better device bonds

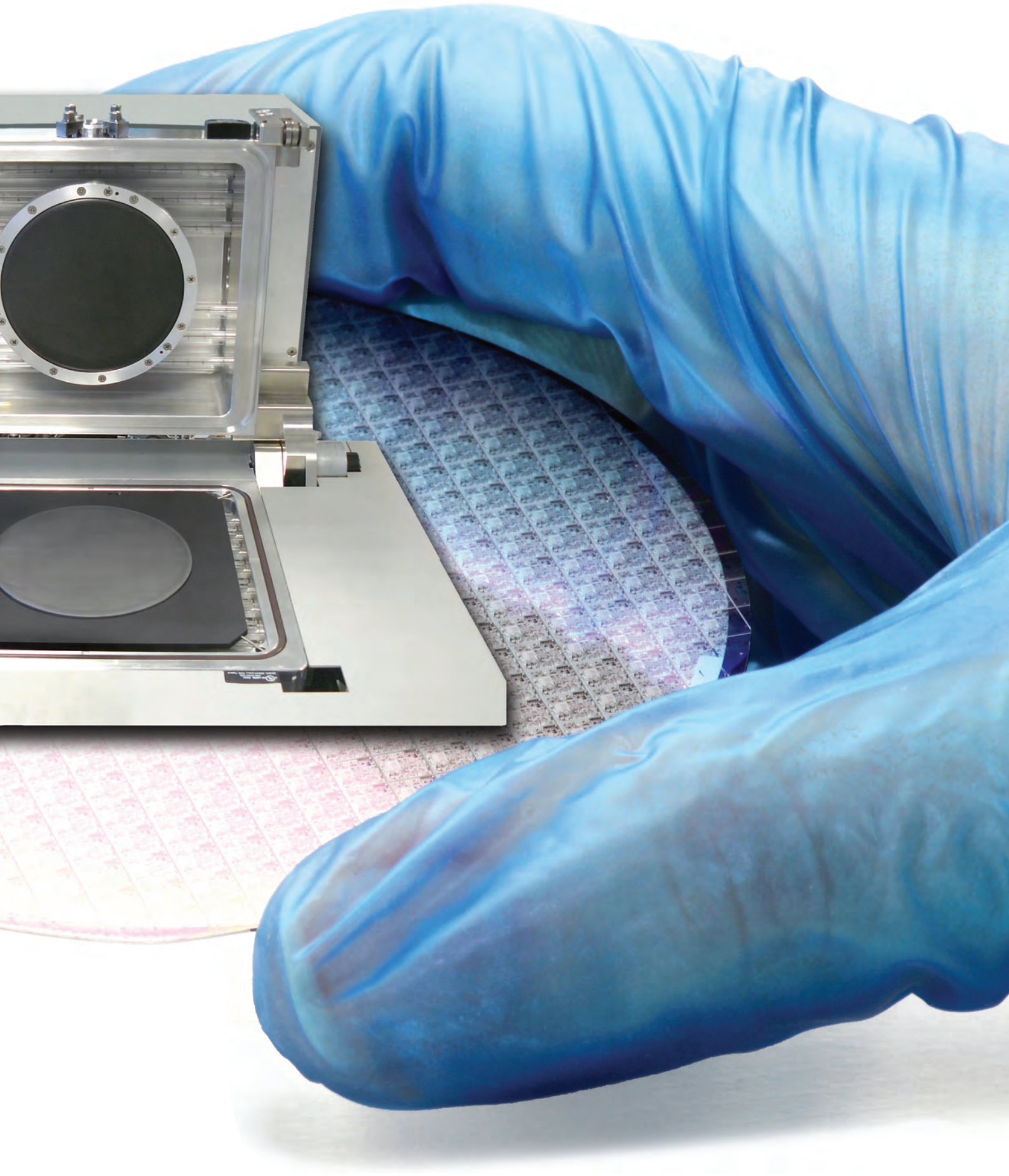


New generations of high power/high performance semiconductors are enabling more robust electronic systems. But higher power densities, new materials and demanding process requirements have challenged existing bonding techniques. ATV Technologie has a new solution that reduces pressure, strengthens bonds and improves throughput.
By Mark Andrews technical editor Silicon Semiconductor.

HIGH DENSITY SEMICONDUCTOR DIE that increase a component's power handling capabilities while saving space and increasing efficiency are key to the functionality of electric vehicles (EVs) and renewable energy systems along with aviation and aerospace power assemblies.

Designers and manufacturers often face a dilemma: how to create void-free, permanent bonds between die, thermal spreaders and other module components without dramatically slowing production, adding costs or crushing yield. The researchers and designers at ATV Technologie GmbH (Vaterstetten, Germany) are well positioned to understand the complexities of bonding processes. They have met the challenges of creating bonds effectively, with high repeatability and sufficient throughput to satisfy the needs of environments that vary greatly such as those found at research institutes, across prototype lines and volume manufacturing.

In order to create void-free bonds, existing systems such as silver (Ag) sintering often utilize pressure as great as 15-40 MPa. While these systems deliver good bonds, the high amount of relative pressure often creates situations where breakage is more likely,



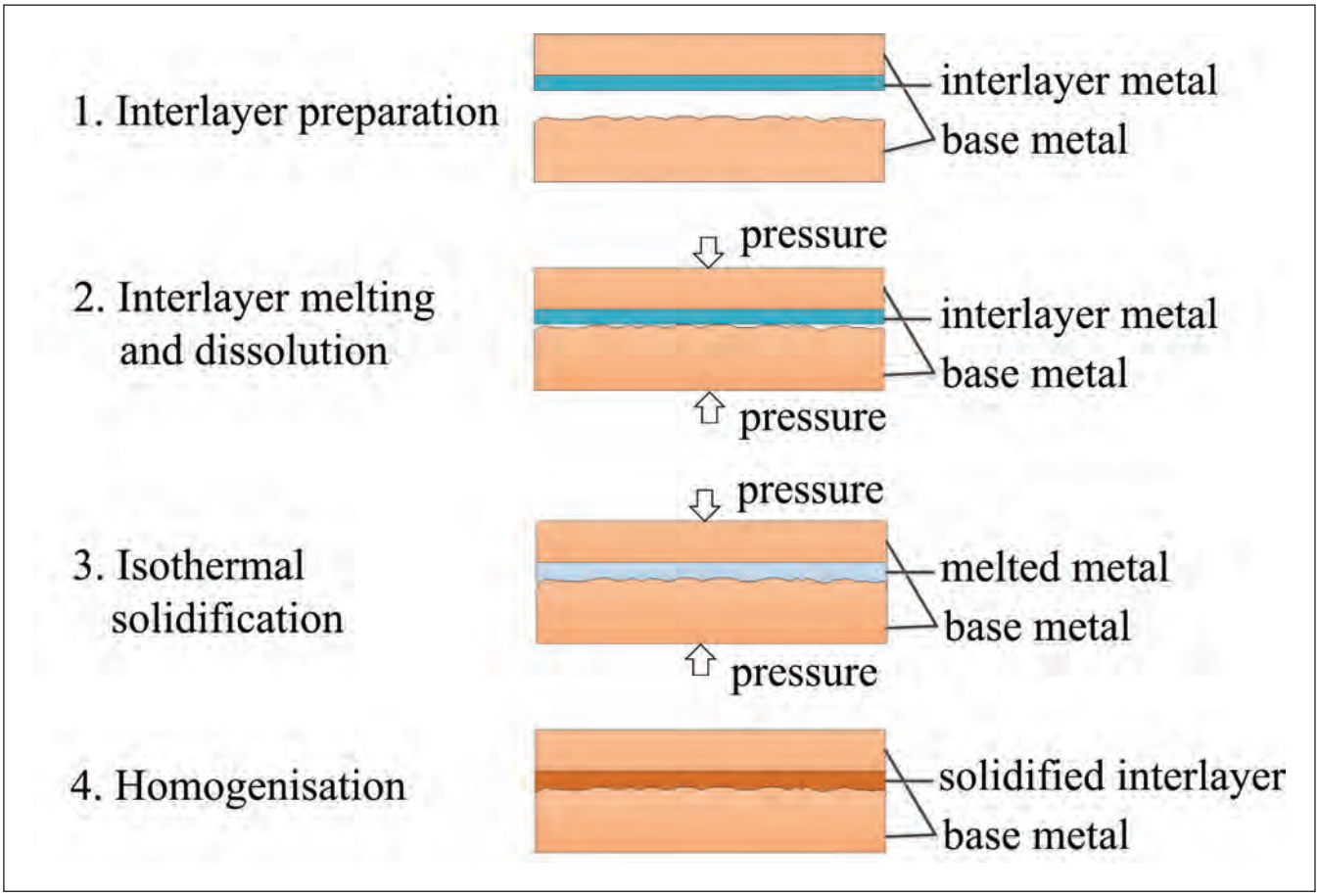


Figure 1: Process stages of Transient Liquid Phase Bonding (TLPB)

adversely affecting yield and long-term reliability. Existing systems also frequently do not handle devices with varying height profiles in the same batch, or require special, complex tooling to accommodate such needs. High temperature sintering typically does not support bonding temperature-sensitive semiconductor components that might warp, crack or lose electrical viability due to intense pressure or heat.

Wide bandgap technologies including gallium nitride (GaN) and silicon carbide (SiC) are moving rapidly into high volume manufacturing (HVM) since issues that limited widespread use of these high power technologies are largely being overcome by industry-wide efforts. The development of ATV's new system was largely driven by the demand for highly reliable insulated-gate bipolar transistor (IGBT) power modules in EVs; however, any similar need could be served. The company explained that die bonding of power LEDs has great potential, as well as applications such as piezoelectric devices for energy harvesting, TC coolers and RF power modules demanding new packaging solutions.

Automotive applications are particularly challenging since operating environments are many degrees centigrade above that of consumer electronics, and zero defects is the quality target for such devices that have to last at least 10 years in-service.

While manufacturers are regularly extending GaN device lifetimes and yield improvements have made the technology completely viable across market sectors, packaging requirements can present vexing issues. As ATV Technical Director, Dr. Ventzeslav Rangelov remarked, conventional lead-free reflow soldering has reached its limits in most applications that are becoming more critical to the future of high power semiconductor markets.

"For assemblies that need to operate at or above 165°C, new die attach techniques including silver sintering and transient liquid phase bonding (TLPB) have been developed," he noted. "The latest system that ATV developed with the Technical University of Berlin and the Fraunhofer Institut can solve vexing issues that can hold back needed products from entering production. It can help researchers explore new device types and even higher levels of power without the drawbacks of other approaches."

ATV's new approach to device bonding processes remedies the drawbacks of other techniques, such as pressure assisted Ag sintering. While silver is prized for its high melting point and excellent thermal conductivity, standard sintering processes have issues related to their requirement for high applied pressure. In standard reflow soldering there is also excess material present when peak temperatures are reached, resulting in certain amounts of self-realignment driven

by capillary action. This misalignment can in particular cases affect yield and function of the assembly. With Ag sintering, mechanical pressure is exerted to enable diffusive joining mechanisms. But to be effective the pressure can be as great as 40 MPa, often resulting in some warpage, cracks in device structures or outright device breaks. When pressure combines with high levels of heat (250°C or greater) there can be a loss of surface contact across the device, often in unpredictable directions with negative performance consequences.

While pressure-assisted silver sintering processes have been refined and have widely entered volume manufacturing, a new approach that addresses shortcomings is now available, Rangelov noted.

"In TLPB, a thin layer of lower-melting metal such as tin or indium is placed between the two higher melting base metals, such as silver, gold or copper," he explained. "During thermal bonding, the solder interlayer melts and wets the base metal surfaces—the interlayer dissolves an amount of the base metal, forming new intermetallic phases. This process leads to isothermal solidifications that create a joint layer with significantly higher melting temperature than the initial solder interlayer." (See Figure 1)

"Once the intermetallic components are formed during bonding, they cannot be melted anymore at the original process temperature, which is close to the melting point of the interlayer metal, such as tin or indium. This is because of the change of the material composition during TLPB. It is defined by the material properties and their proportion and not by the process itself. The change of material composition is due to diffusion and promotes the isothermal solidification. This is also the main difference in our process compared to conventional reflow soldering where the composition of the solder material remains quite the same," he explained.

Conventional Ag sintering and TLPB both require some levels of mechanical pressure under heat, but TLPB only requires enough pressure to hold the surfaces being bonded together to the point that a bond can form without misalignment.

Thermal load requirements are also far less. ATV has also eliminated the need for complex additional mechanical pressure tooling to cope with whole assemblies that exhibit complex topographies. ATV's system has been tested with form factors varying from 0.5mm to 3.0mm—all in the same batch.

Despite the sizeable variations in height profiles, bonding was void free with high yield. In most competing systems, the ability to compensate for height variations drives up complexity and costs of tooling, Rangelov noted. Also, the fact that bare metals are involved in processing requires gas-tight chambers with controlled inert or reducing process atmosphere. ATV's approach handles these needs while others do not.

"The main benefit is that customers do not need expensive height compensating tooling, which is individually designed for any different layout. This lowers the costs and has a positive effect on yield. In the bonding system, whole electronic assemblies with complex topographies can be processed. Passive and active devices as well as clips can be bonded in one process run. This can give more flexibility in the packaging process flow."

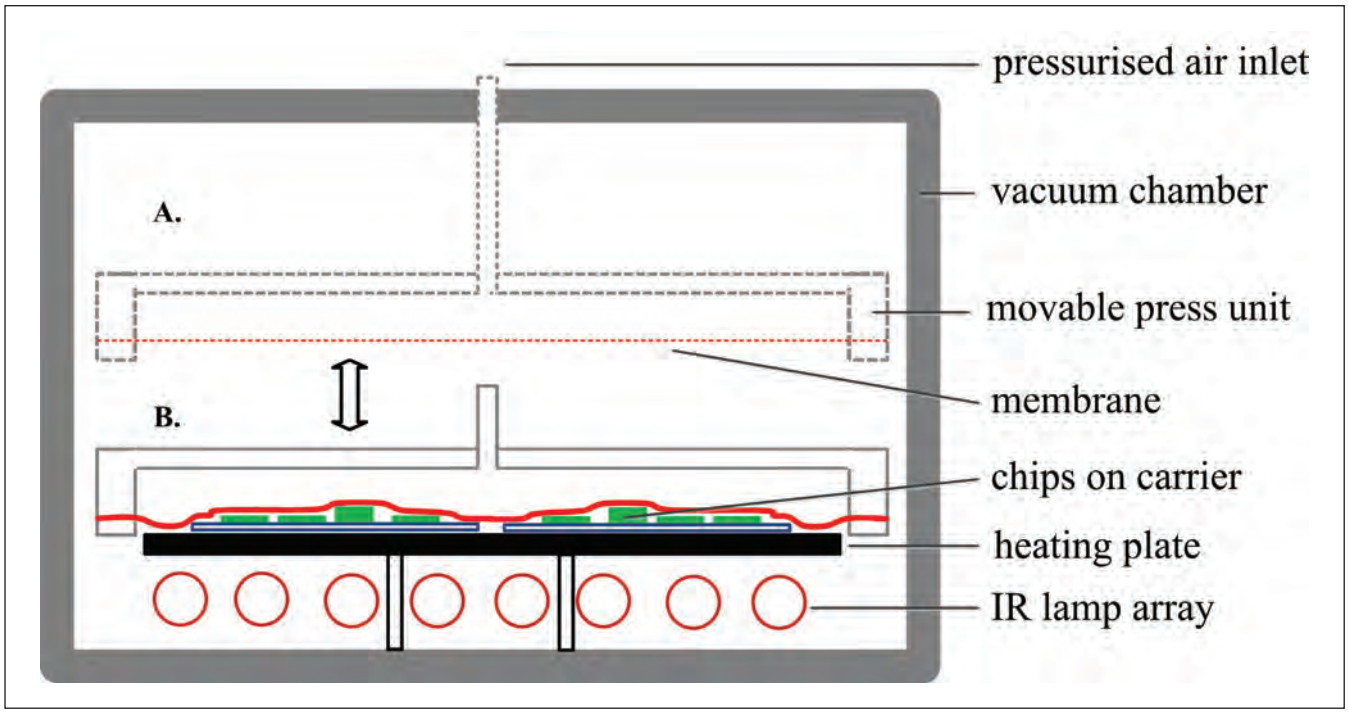


Figure 2: Schematic drawing of ATV's new bonding oven

ATV developed a system that combines established equipment for vacuum reflow soldering with a dedicated press unit (see Figure 2). Their process supports semiconductor die or other packaged components that are aligned and placed on a substrate for DCB (direct copper bonding). It also supports wafers that are either flipped or face up utilizing industry standard handling equipment

"Our bonding system techniques can also be beneficial in conventional reflow soldering, when parts have to be kept in position precisely during the liquidity phase. This is not always possible with alignment masks (other systems require), especially when parts are very small, or different CTE might be an issue," he remarked.

ATV developed a system that combines established equipment for vacuum reflow soldering with a dedicated press unit (see Figure 2). Their process supports semiconductor die or other packaged components that are aligned and placed on a substrate for DCB (direct copper bonding). It also supports wafers that are either flipped or face up utilizing industry standard handling equipment. For tacking operations, Rangelov said a liquid adhesive, ultrasonic energy or thermo-compression can be used, offering flexibility to suit existing practices, whether in the lab or fab.

ATV Technical Director, Dr. Ventzeslav Rangelov

High throughput can be achieved at the highest alignment accuracy, he added. In repeated tests of their new system, Rangelov noted that ATV utilized subjects that varied in thickness, achieving excellent void-free results. This was also achieved with pressures of only 0.5 MPa (or less), substantially reducing the possibility of warpage or cracks. While ATV developed their bonding approach with an eye on high density power semiconductors including SiC MOSFETs and GaN devices in power amplifiers, switches and similar applications, he noted that silicon and gallium arsenide (GaAs) technologies may also benefit due to the high reliability of the bond combined with the fact that warping of thinned semiconductor wafers or devices can be prevented due to lower temperature process environments combined with the fact ATV's approach utilizes substantially less pressure than other systems.

Utilizing their proprietary process approaches and materials, ATV found that Ag sintering exhibited similar joint properties as sintering without mechanical pressure applied, but with significantly reduced process time. The great advantage of the ATV bonding oven is seen when undertaking transient liquid phase bonding (TLPB). The combination of vacuum capability, controlled reducing atmosphere, and 'light-touch' mechanical pressure enables a variety of additional applications beyond high-power electronics including MEMS packaging, chip-to-wafer packaging, and 3D system integration.

"We see our process and oven design as having great potential for chip-to-wafer and 3D system integration independent of the bonding technology used (reflow soldering or TLPB). Bonding of silicon chips with fine pitch micro-bumps has also been demonstrated. A further topic of interest is currently copper sintering as we work to expand the number of technologies and applications that can be served. We are always interested in additional customer engagement," he concluded.

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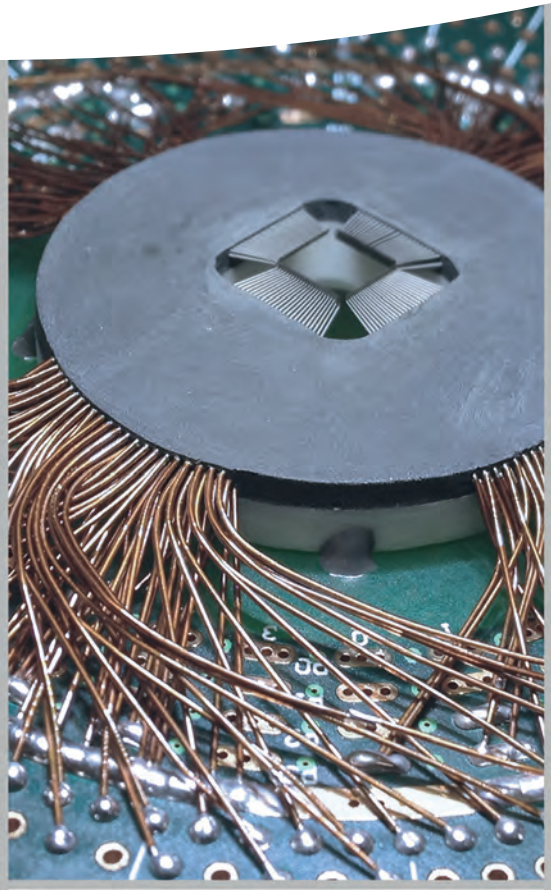
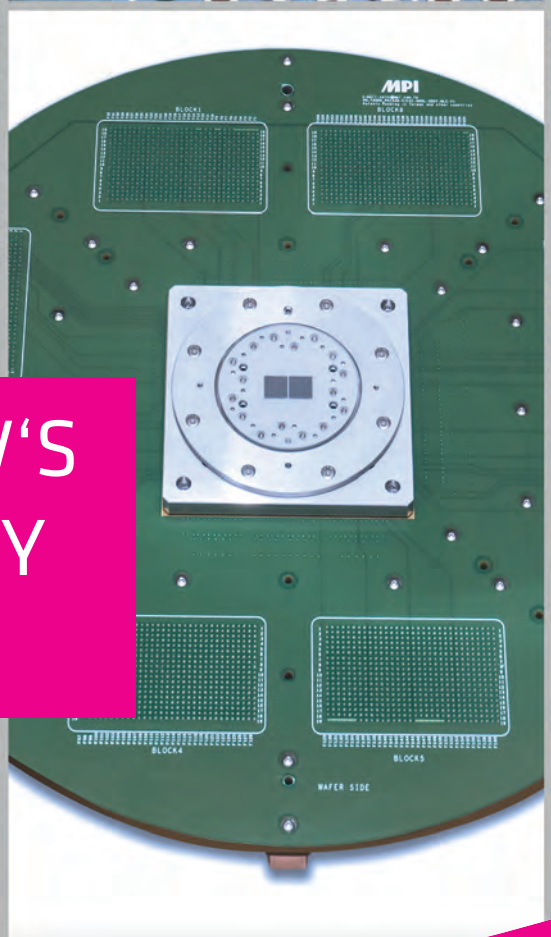
30 YEARS





TOMORROW'S TECHNOLOGY TODAY.

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Driving growth, safety, and quality in automotive electronics

Sophisticated electronic systems continue to increase their impact across today's automotive sector. Radar, LiDAR, and a host of new artificial intelligence (AI)-based systems are becoming the norm as vehicle makers seek to improve safety, performance and efficiency on the road to fully autonomous vehicles. Linde Electronics describes ways that the automotive manufacturing supply chain can meet tight performance standards in pursuit of global market opportunities.

By: Dr. Paul Stockman, Head of Market Development, and Greg Shuttleworth, Technical Quality Manager, Linde Electronics

In 1913, Henry Ford revolutionized manufacturing with the inauguration of the first assembly line to produce automobiles, which reduced the time to make a new car from 12 hours to 2.5 hours, and more importantly, drove down the cost by 65%. Semiconductor manufacturing has been a beneficiary of this approach, as increasing automation has been complementary to the geometry shrinking forces responsible for Moore's Law. Both industries manufacture on a very high volume: there were approximately 87 million passenger vehicles and 87 million 300mm equivalent wafers fabricated in 2017. Today, robotics drives both industries to further cost reduction and improved quality.

More and more, these industries are connected, as electronic systems and semiconductors become a larger part of the total automotive bill of materials, and automotive applications become a larger percentage of the total semiconductor market. At the same time, electronics are responsible for a larger portfolio of car functions, progressing rapidly towards an anticipated revolution of fully automated driving vehicles. While electronics become more safety critical in vehicle operation, the quality requirements of the semiconductor components are increasing in ways the industry has not seen before. We can see in the daily financial news the competing headlines between large strategic plays in automated driving investments and developments punctuated by reports of crashes by test vehicles and private owners pushing their cars into uncharted levels of self-driving.

In this article, we look first at the expanding market and drivers that are linking the growth of the semiconductor and automotive businesses. Next, we evaluate the status of automotive semiconductor quality requirements and the developing needs for further specifications. Finally, we look further into the supply chain to examine the role that semiconductor process materials play in enhanced requirements for safety and quality.

Market overview

Electronic systems and passenger vehicles are both significant contributors to the global economy, representing about 2% each of global GDP, and their growth is increasingly interdependent. According to NXP, electronic systems represent more than one-third of the bill of materials for new cars. The chips themselves, including OSDs (optical, sensors, and discretes) now average nearly (USD) $500 per vehicle. From the semiconductor industry perspective, automotive ICs and OSDs are 13% of application sales, and growing almost twice as fast as the overall industry. Just like PCs and smartphones, we expect the chip value of the overall electronics assembly to increase as the applications become a more critical part of vehicle operation.

This growth potential has attracted attention from many of the major players in semiconductor manufacturing as they try to both directly benefit from the higher multiples of the automotive sector, and to influence what kinds of chip designs will control future vehicles.

Many recent mergers and acquisitions have been viewed through the lens of increasing the acquirer's position in automotive applications: NXP's acquisition of Freescale, which had a larger share of automotive chip sales, and Qualcomm's pending takeover of NXP. Likewise, On Semiconductor increased its share by acquiring Fairchild, and Infineon has bought Wolfspeed and International Rectifier for silicon carbide technology important for power control in electrified vehicles.

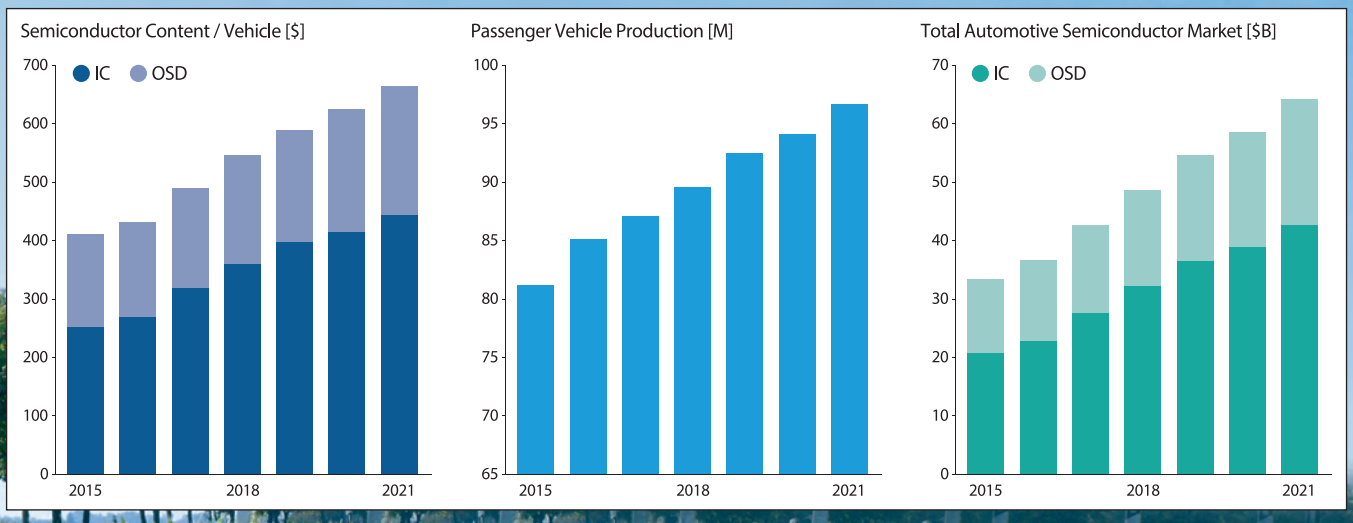


Figure 1: Growth of automotive, semiconductor and vehicle markets [adapted from IC Insights]

Even more strategic plays have been pursued in the past year by Intel and Samsung. Intel has made a portfolio of automotive acquisitions, capped recently by the $15 billion purchase of Mobileye for chip designs that support assisted and autonomous driving for customers like Tesla and BMW. For its part, Samsung purchased Harman for $8 billion. Known best for its premium car audio offerings, Harman's products also include automotive navigation, communication, and cybersecurity. It brings with it a customer portfolio of most of the major vehicle manufacturers in Europe, Japan, and the United States.

Primary drivers

While we may think of semiconductors as being rather recent introductions, associated with many of the comfort, convenience, and infotainment options now available, computer chips have long been an integral, if unseen, part of the cars we drive.

- **Operations and environmental controls**
  In 1968, just ten years after the modern IC industry was born, Volkswagen introduced an electronic control unit (ECU) manufactured by Bosch for regulation of fuel injection. As emission and fuel efficiency requirements became more stringent, ECUs were made standard on most vehicles manufactured. Controllers have proliferated in cars ever since: engine temperature, electronic steering and braking, automatic transmissions, as well as controls for smaller parts like wipers, mirrors, and illumination. Airbag sensors/actuators and anti-lock brakes have made driving safer.

- **Convenience, comfort and infotainment**
  More obvious in modern cars are the proliferation of many electronic functions, which have a higher density than our connected offices and homes. Conveniences and comfort functions are almost everywhere accessible in the vehicle: power windows, climate control, charging ports, remote operations, as well as those actually related to driving like cruise control and passive seatbelt use indicators. More recently, infotainment offerings have also quickly advanced from radio and recorded media players to include multiple display screens for indicators, controls, navigation, and entertainment in addition to connectivity for the vehicle and the devices we bring inside it. As a safety feature, the US National Highway Traffic Safety Administration has required rear-view cameras for vehicles less than 4500 kg sold after May 2019.

- **ADAS to full autonomy**
  The basics of ADAS (advanced driver assistance systems) are already in premium vehicles today: adaptive cruise control, lane departure warnings, and drowsy driver detection are just a few of the controls and sensors available. However, these are just the beginning of what is anticipated to be a rapidly advancing revolution in driving technology, which will transform the operation of driving from one where the driver is assisted passively by various electronic information and controllers, to one where the vehicle operates fully autonomously, that is independently, of any occupant in the vehicle.

The roadmap to full autonomous driving is populated not only with significant developments in technology, but also with safety protocols. Various automotive authorities have created stages on this roadmap, such as the SAE (Society of Automotive Engineers) characterization in Figure 2. Common protocols among autonomous vehicles will need to be agreed to benefit from information sharing between vehicles.

To achieve fully autonomous driving, sensors and controllers are just the beginning of the electronics requirements. Extreme amounts of data will need to be received, prioritized, analyzed, and shared in real time. Intel estimates that cars will generate data at a rate of nearly 0.75 Gb/s, or around

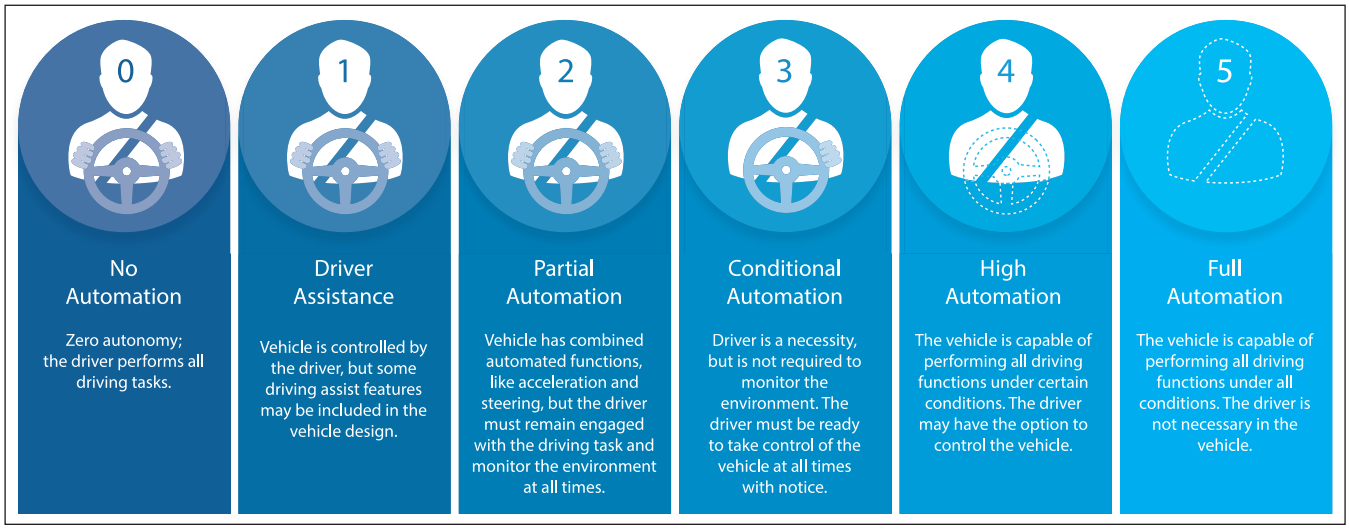


Figure 2: SAE designated level of autonomous driving capability

4 Tb per average 90-minute usage per day, rivaling the fastest broadband connections available today. Processors like emerging GPUs for artificial intelligence are thought to be the likely means of dealing effectively with data-rich processing, which gives companies like Nvidia and AMD and the foundries that supply them access to this emerging application. And autonomous vehicles will need to receive and share relevant data with each other, which will require new levels of cloud connectivity and capacity, explaining the strong early investment in ADAS from cloud giants like Baidu, Google, and Microsoft.

- **Electrification**
  In a development roadmap roughly parallel to autonomous driving, electrification of powertrains will also transform the automotive industry and become a new growth application for semiconductors. Already available from established and new automobile manufacturers either as fully electric vehicles or as hybrid electric motor-combustion engine models, electrified vehicles have roughly double the semiconductor content per vehicle. The adoption of electric vehicles is driven by environmental concerns – the reduction of greenhouse gas, NOx, and particle emissions – as well as improvement of vehicle performance and maintenance. Bolstering adoption is the future ban of sales of combustion engines by major economies like India, China, and much of Europe by 2040. Already, 3% of vehicles sold in 2017 were electric.

Diverse electronics content

Automotive electronics is an application that cannot be defined by specific technologies or applications, which benefits almost all sectors of the semiconductor industry. Currently, it is characterized by a very large portfolio of products based on mostly mature technologies, spanning from discrete, optoelectronics, MEMS and sensors, to integrated circuits and memories.

Figure 3 shows the distribution of silicon content from an analysis of an early electrified car in 2014. Important to note is that this car has no autonomous driving capability. If all vehicles made today had the same level of electronics intensity as this example car, the semiconductor content would require the equivalent of 600,000 wafer starts per month of 300mm fab capacity.

Enhanced quality

Until now, the automotive electronics market has been the preserve of specialized semiconductor manufacturers with long experience in this field. The reason for this is the specific know-how required for quality management. As applications proliferate, become safety critical, and progress towards leading-edge processes, enhanced quality protocols will be required.

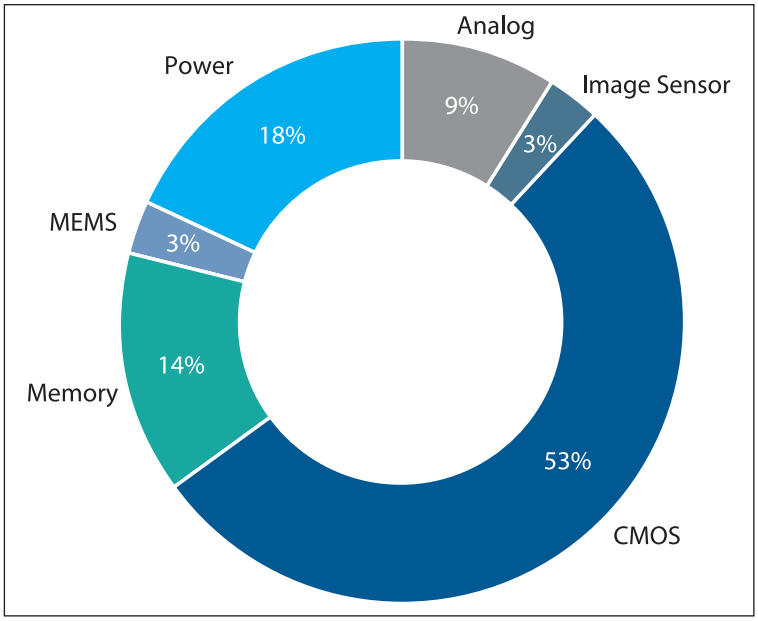


Figure 3: Semiconductor content in BMW i3 in relative silicon area [adapted from Applied Materials]

A component failure that appears harmless in a consumer product could have major safety consequences for a vehicle in motion. Furthermore, operating conditions of automotive electronics components (temperature, humidity, vibration, acceleration, etc.), their lifetime, and their spare part availability are differentiators to what is common for consumer and industrial devices.

Currently, some of the most technologically advanced vehicles integrate around 450 semiconductor devices. As they become significantly more sophisticated, the semiconductor content will drastically increase, with many components based on the most advanced semiconductor technology available. Introducing artificial intelligence will require advanced processors capable of computing a massive amount of data stored in high-performance and high capacity memory devices. This implies that not only the most advanced semiconductor processes will be used, but that these will need to achieve the highest degree of reliability to allow a flawless operation of predictive algorithms.

It is expected that smart vehicles capable of fully autonomous driving will employ up to 7,000 electronic components. In this case, even a failure rate of 1ppm, already very low by any standard today, would lead to 7 out of 1,000 cars with a safety risk. This is simply unacceptable. The automotive electronics industry has therefore introduced quality excellence programs aimed at a zero-defect target. Achieving such a goal requires a lot of effort and all constituents of the supply chain must do their part.

The automotive electronics industry is one of the most conservative in terms of change management. Long established standards and documentation procedures

Typical operating conditions for different electronics market segments

	Consumer	Industrial	Automotive
Temperature	0 to 40°C	-10 to 70°C	-40 to 160°C
Operation time	2 to 5 years	5 to 10 years	Up to 15 years
Humidity	Low	Environment	0% to 100%
Supply	Average 1 year	2 to 5 years	Up to 30 years
Tolerated failure rate	<10%	<<1%	Target: 0% failure

Figure 4: Typical operating conditions for different semiconductor applications

ensure traceability of design and manufacturing deviations. Qualification of novel or modified products is generally costly and lengthy. This is where material suppliers can offer competence and expertise to provide material with the highest quality standards.

What does this mean for a material supplier?

As a direct contact to its customer, the material supplier is responsible for the complete supply chain from the source of the raw material to the delivery at the customer's gate. The material supplier is also accountable for long-term supply in accordance with the customer's objectives.

There are essentially two fields where the material supplier can support its customer: quality and supply chain.

Given the constraints of the automotive electronics market, material qualification must follow extensive procedures. While a high degree of material purity is a prerequisite, manufacturing processes are actually more sensitive to deviations of material quality, as they potentially lead to process recalibration. Before qualification starts, it is critical that candidate materials are comprehensively documented. This includes the manufacturing process, the transport, the storage, and, where appropriate, the purification and transfill operations. Systematic auditing must be regularly performed according to customers' standards. As a consequence, longer qualification times are expected. Any subsequent change in the material specification, origin, and packaging must be duly documented and is likely to be subject to a requalification process.

Material quality is obviously a critical element that must be demonstrated at all times. This requires the usage of high-quality products with a proven record. Sources already qualified for similar applications are preferred to mitigate risks. These sources must show long-term business continuity planning, with process improvement programs in place. Purity levels must be carefully monitored and documented in databases.

State-of-the-art analysis methods must be used. When necessary, containment measures should be deployed systematically. Given the long operating lifetime of automotive electronic components, failure can be related to a quality event that occurred a long time before.

Because of the necessary long-term availability of the electronics components and the material qualification constraints, manufacturers and suppliers will generally favor a supply contract over several years. Therefore, the source availability and the supply chain must be guaranteed accordingly.

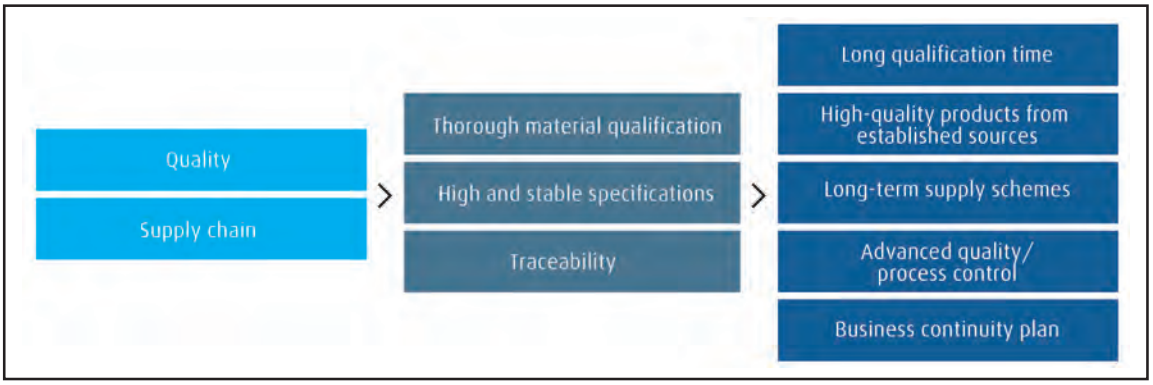


Figure 5: Quality and supply chain control determine supplier planning and actions

Material suppliers are implementing improved quality management systems for their products to fulfill the expectations of their customers, in terms of quality monitoring and traceability. Certificate of analysis (COA) or consistency checks are not sufficient anymore; more data is required. In case deviation is detected, the investigation and response time must be drastically reduced and allow intervention before delivery to the customer. Finally, the whole supply chain must be monitored.

Several tools must be implemented to maintain a reliable supply chain of high-quality products: statistical process and quality controls (SPC/SQC), as well as measurement systems analysis (MSA), allow systematic and reliable measurement and information recording for traceability. Implementing these tools particularly at the early stages of the supply chain allows an "in-time" response and correction before the defective material reaches the customer's premises. Furthermore, some impurities that were ignored before may become critical, even below the current detection limits. Therefore, new measurement techniques must be continuously investigated to enhance the detection capabilities.

Finally, a robust supply chain must be ensured. It is imperative for a material supplier to be prepared to handle critical business functions such as customer orders, overseeing production and deliveries, and other various parts of the supply chain in any situation. Business continuity planning (BCP) was introduced several years ago to identify and mitigate any risk of supply chain disruption.

Analyzing the risks to business operations is fundamental to maintaining business continuity. Materials suppliers must work with manufacturers to develop a business continuity plan that facilitates the ability to continue to perform critical functions and/or provide services in the event of an unexpected interruption. The goal is to identify potential risks and weakness in current sourcing strategies and supply chain footprint and then mitigate those risks.

Because of the efforts necessary to qualify materials, second sources must be available and prepared to be shipped in case of crisis. Ideally, different sources should be qualified simultaneously to avoid any further delay in case of unplanned sourcing changes. Material suppliers with a global footprint and worldwide sourcing capabilities offer additional security. Multiple shipping routes must be considered and planned to avoid disruption in the case, for instance, of a natural disaster or geopolitical issue affecting an entire region. Material suppliers need to be aware and monitor regulations specific to the automotive electronics industry such as ISO/TS16949 (quality management strategy for automotive industries). This standard goes above and beyond the more familiar ISO 9001 standard. By understanding the expectations of suppliers to the automotive industry, suppliers can ensure alignment of their quality systems and the documentation requirements for new product development or investigations into non-conformance.

Future of automotive electronics

With the increasing automation of future vehicles, new and more advanced semiconductor technologies will be used and vehicles will become supercomputers and data centers on wheels. Most of these components (logic or memory) will be built by manufacturers relatively new to the automotive electronics world—either integrated device manufacturers (IDM) or foundries.

In order to comply with the current quality standards of the automotive industry, these manufacturers will need to adhere to more stringent standards imposed by the automobile industry. They will find support from materials suppliers like Linde that can deliver high-quality materials associated with a solid global supply chain with acquired global experience in automotive electronics.

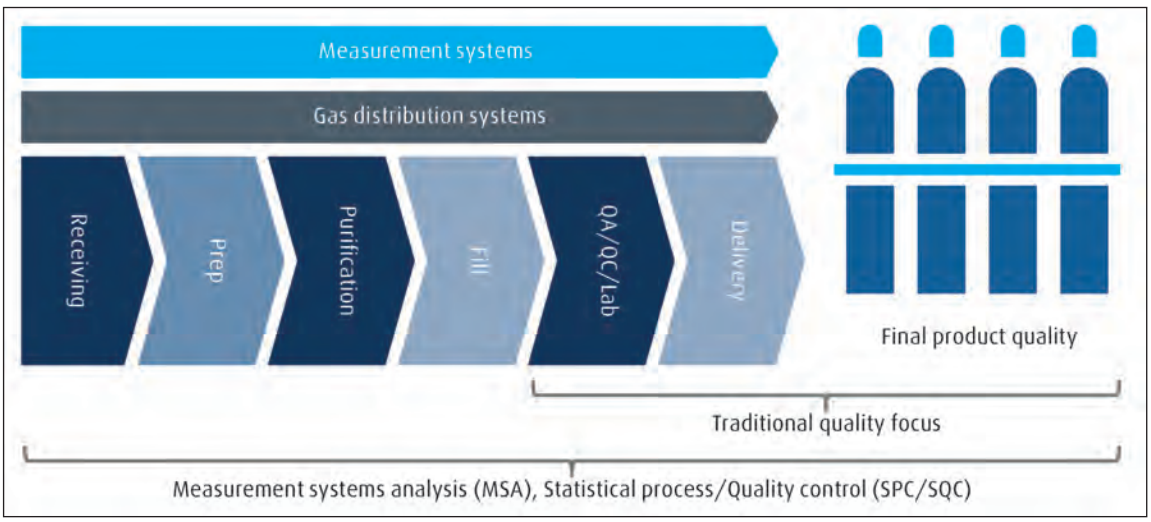
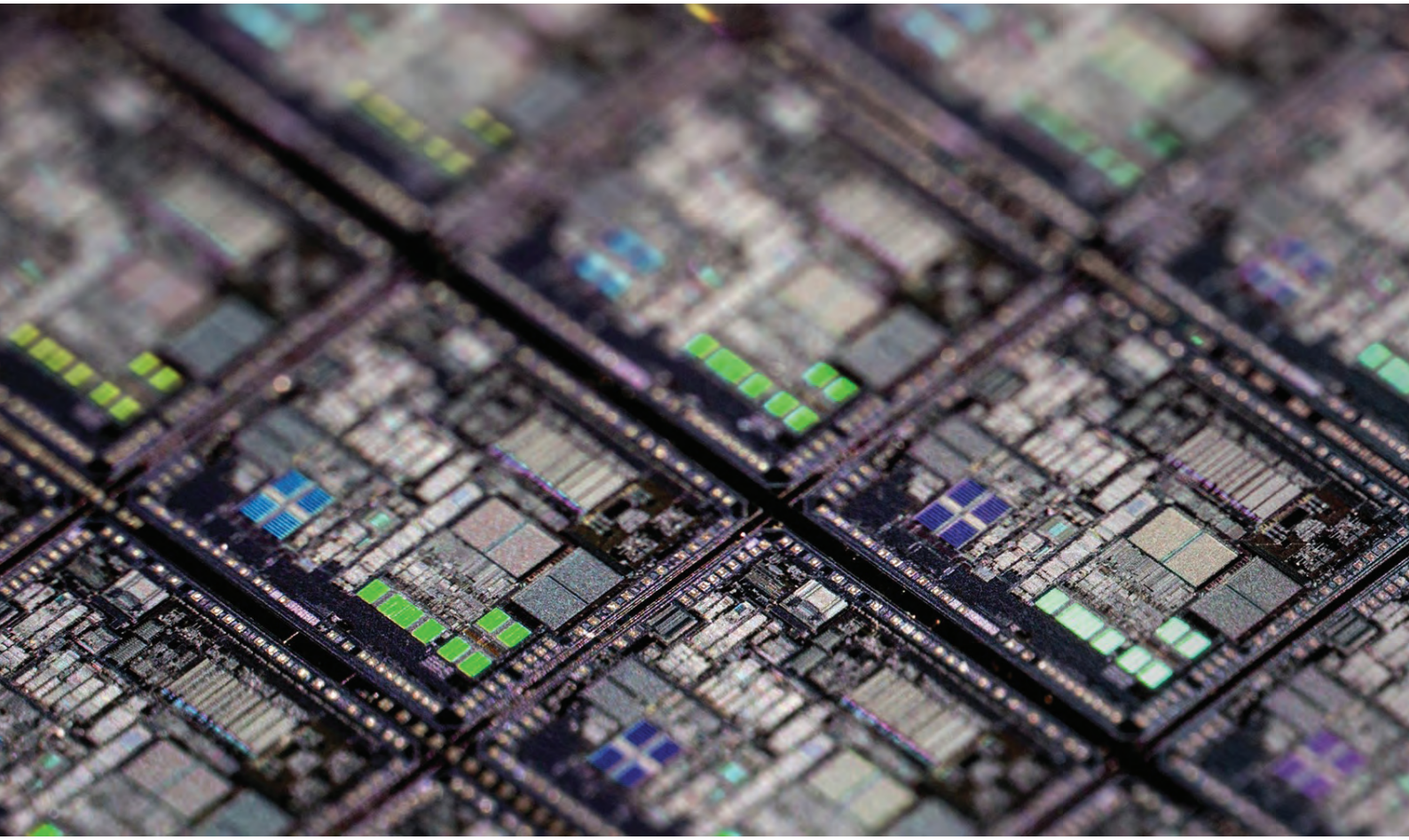


Figure 6: Enhancing material quality requires expanding traditional quality focus



New WID120 Wafer ID reader

simplifies, speeds semiconductor wafer processing

The ´Made in Germany´ IOSS WID120 Wafer ID Reader sets the standard for highest quality results and reliability.
By HTT Group

THE IOSS WID120 Wafer ID Reader is the latest generation of advanced wafer ID readers. It was designed to close the gap between easy usability and highest flexibility while eliminating time consuming (re-)teaching procedures for process tool operators. Thanks to its fully automatic light control and intelligent configurations handling, the IOSS WID120 is able to tweak itself and improve read rates drastically. It is the first tool of this kind, which saves the re-teaching completely.

WID120 – The benchmark for ID reading in the semiconductor industry

The IOSS WID120 Wafer ID Reader was developed to meet the very high demands of the semiconductor industry. It easily decodes OCR, Barcode, DataMatrix and QR code markings on any kind of wafer regardless of the wafer material and coating.
The ´Made in Germany´ IOSS WID120 Wafer ID Reader sets the standard for highest quality results and reliability. These self-contained systems with a

compact design achieve the highest read rates and counts with customer proven reliability.
- All-in-one camera for reading OCR, Barcode, DataMatrix and QR-Code

Easy to use GUI for reaching results within minutes
The new WID120 Graphical User Interface (GUI) revolutionizes the ID Reader market. This GUI concept with an easy to understand teaching wizard, enables any technician to perform the simplified camera setup process. With the automatic illumination control, it helps receiving results even under sub-optimal conditions. WID120 software also contains a sophisticated intelligence that significantly decreases time needed for support. The software adapts to new reading conditions like different coatings on the wafer and adds the new light setting automatically to the existing recipes.

Intelligent state of the art illumination system

Thanks to the unique IOSS patented optical system with RGB (Red / Green / Blue) illumination, the WID120 Wafer ID Reader can image any ID mark. Different surrounding light conditions do not have any impact on its settings and reading results.
Wafers with super-soft marks, ultra-thin coatings and sapphire- substrates can be used with the WID120 without extra setup procedures. The intelligent and of course fully automatic selected light modes, like bright- and multiple dark-field illuminations, offer a huge number of variations for the user. Up to 15 internal RGB light modes as well as an auto-adjustment function are available to adjust lighting to application needs. With these excellent, integrated illumination possibilities and three optional external light modes, future applications easily can be matched.

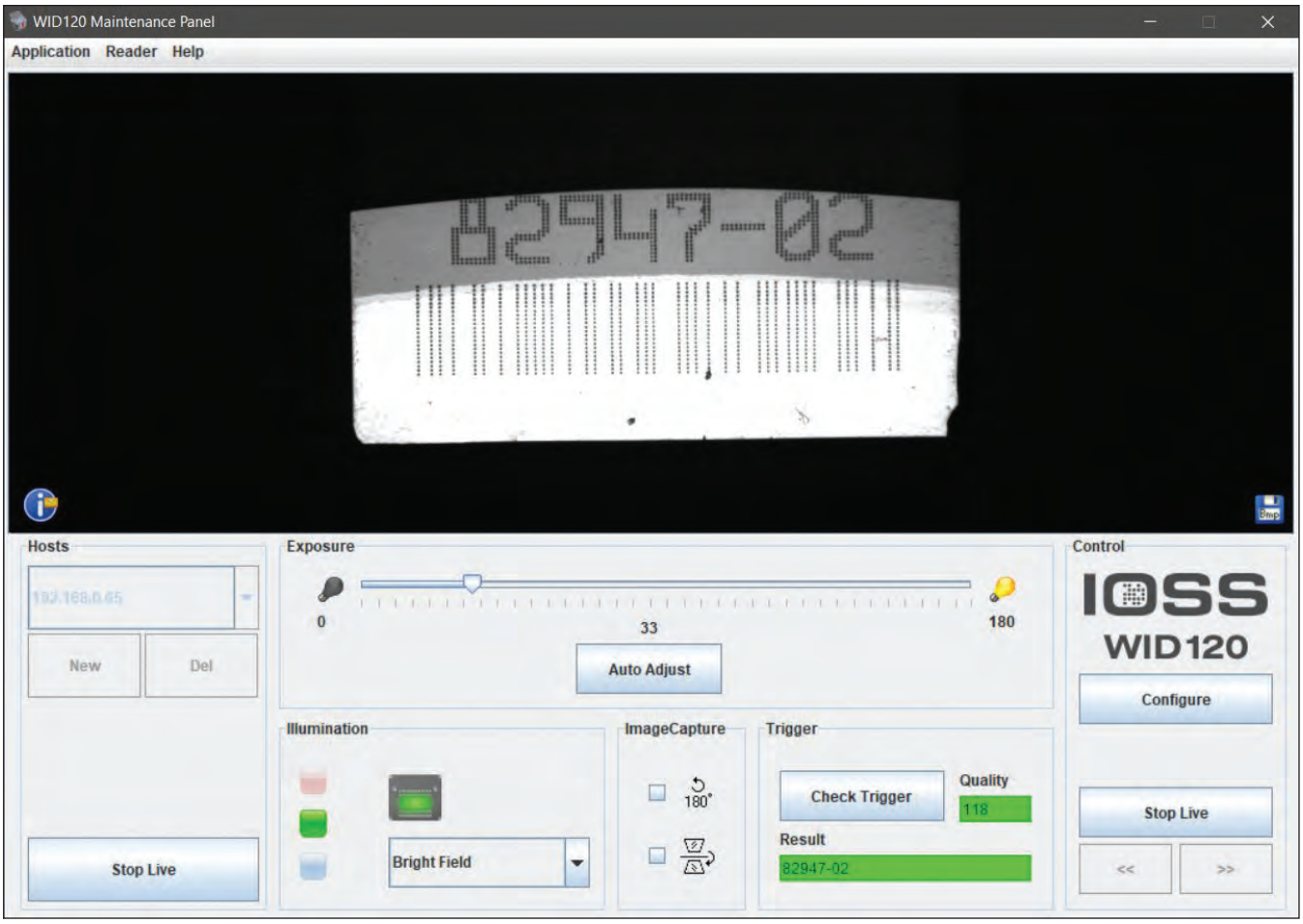
The intelligent illumination system of WID120 decreases time for reading ID codes. It will speed up your systems and will give you more flexibility in production.

Special interfaces for easy integration into your production equipment are also available.
The longer it works, the faster it gets.

Unlimited reading algorithms

The IOSS WID120 Wafer ID Reader system can make 100% wafer traceability a reality. Our long-time experience has proven ID recognition algorithms for OCR Codes, Barcodes as well as DataMatrix and QR-Codes on all types of wafers.

The system offers a flexible handling of different fonts as well as customized output formats.
The read out results can be automatically checked



Caption

via database, to ensure a perfect performance. Our algorithms are customer proven to achieve excellent reliability and robustness in the field of wafer ID readers.

Image enhancement by using intuitive digital filters

The IOSS WID120 Wafer ID Reader utilizes fully automated image enhancement filters, in addition to its unique RGB illumination technique.

It reads OCR, Barcode, DataMatrix and QR-Code in one-step, due to its ultra-wide field of view.

Examples for WID120 Upgrade Kits
Wafer Prober:
Accretech / TSK, TEL, MARTEK/Electroglas, SEMICS and others

Wafer Inspection:
ASTI, QES Mechatronic, RUDOLPH, CAMTEK and others

Wafer Sorter:
RORZE, MECHATRONIC, NADATECH, BROOKS, PST, ASYST, RORZE, R2D, COMET, TB PLONER and other

Even in the most complex cases, this combination is able to turn a read-failure into a read-success while increasing steadiness.

All codes can be read all over our field of view. Even if the code shifts its position or changes the angle, IOSS WID120 is able to read it using our so-called 'code shift compensation.'

Fastest reading performance

IOSS WID120 Wafer ID Reader is the most advanced, high-end system on the market. It is extremely powerful and reliable. Using a high power processor IOSS WID120 Wafer ID Reader permits intensive image analysis to deliver extraordinarily reliable results, together with superlative short read times. The IOSS WID120 provides up to 10x faster reading results compared to others.

Advanced automatic recipe optimization

The software features of the WID120 automatically optimize settings to read the most demanding wafer marks. It allows reading OCR, Barcode, DataMatrix and QR-Code in one job only. The flexible recipe handling offers additional options to fulfill special application requirements.

WID120 has the possibility to modify the results via a

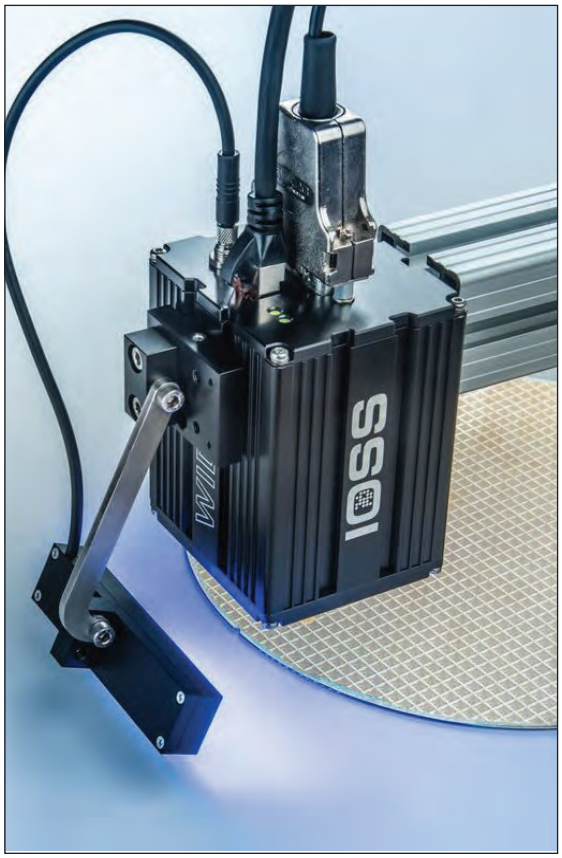
database configuration. Per trigger, it can adjust up to 10.000 different settings. Two readers can operate at the same time on a single reader interface to read FRONT- and BACK- side using only one trigger signal. Working with these systems requires no operator intervention.

Optimum use of recipes

ID marks on wafers can vary from wafer to wafer and between lots. The ´Made in Germany´ IOSS WID120 Wafer ID Reader automatically adapts to the current situation and fulfills its job. Automatic optimization of the unique intelligent illumination technique, RGB light as well as using additional image enhancement filters allow a fluent workflow at a stretch. The system requires no manual optimization or adjustments by an operator.

Flexibility, ease of integration and first level service beyond comparison

The IOSS WID120 Wafer ID Reader can be integrated into existing tools very easily and requires less space. It works independent from software platforms and uses a software version with a comprehensive user interface. Thanks to the compact design and additional available optical options for special applications, the IOSS WID120 Wafer ID Reader can be integrated into any kind of wafer processing and handling equipment. Our top-class technical support and service is well known for its high level knowledge throughout our customer base.



Facts:

- All-in-one camera for reading OCR, Barcode, DataMatrix and QR-Code
- Evolutionary integrated RGB-LED illumination
- Sophisticated intelligence
- Code-Shift-Compensation
- Intelligent illumination concept
- Additional external RGB-Illumination connectable
- Up to 99 different configurations per job file
- Supports database and master-slave option for FRONT- and BACK- side reading
- Easy GUI - Graphical User Interface
- Integrated help, different languages for any menu option
- User guiding teach-in wizard
- Preview of fonts – Easy add new fonts
- Touch Screen ready
- Images can be stored via FTP
- Logging data can be stored via UDP
- Identification of every single Reader in local network
- Modified housing for more flexible integration

Strength:

- Increase tool uptime due to 100% wafer traceability
- Optimized functions for highest efficient wafer throughput
- Easy integration into your production equipment
- Fastest reading, up to 10x faster than others
- Biggest Field of View in the market: 35mm x 13mm (called ultrawide Field of View)
- Development, Production is “Made in Germany´
- >10.000 systems installed worldwide
- Reader with best ROI (Return of Investment) in the market

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Q&A

Edwards Vacuum

Mark Andrews, Technical Editor of Silicon Semiconductor discusses the importance of abating Nitrous Oxide with Mike Czerniak Environmental Solutions Business Development Manager at Edwards.

Q Where is N_2O used?

A Nitrous Oxide (N_2O) is widely used in semiconductor manufacturing in chemical vapour deposition (CVD) of silicon oxy-nitride (doped or undoped) or silicon dioxide, in diffusion for oxidation and nitridation, in rapid thermal processing (RTP), and in chamber seasoning. N_2O also has a variety of other industrial and medical applications. Worldwide, the majority of N_2O (67%) comes from agricultural activities. Fossil fuel combustion and industrial processes, of which semiconductor manufacturing is a small part, accounts for 10%.

Q Why abate N_2O?

A After CO_2 and CH_4, N_2O is the 3rd most impactful human-induced greenhouse gas (GHG), accounting for 7% of emissions. This is as a result of its widespread use and its atmospheric lifetime of 114 years, which gives it a global warming potential (GWP100) of 298. Refined IPCC (intergovernmental panel on climate change) guidelines, to be released in 2019, will include new emission factors for N_2O. In addition to its global warming potential, N_2O is noxious, with a threshold limit value (TLV) for daily workplace exposure of 50 parts-per-million. Even though semiconductor manufacturing is only a minor emitter of N_2O, the industry has included limits on emission in its roadmap (ITRS/IRDS), primarily because it is a gas that can be abated and there is increasing pressure to do everything possible to reduce the industry's CO_2 footprint (to which N_2O contributes). Market pressure is also coming into play as green labelling is introduced and many customers are beginning to monitor emissions-per-product.

Q What are the options for abating N_2O?

A N_2O can be abated by oxidation or reduction. Catalytic reduction, though possible, is generally not suitable for semiconductor process exhausts, which often include corrosive gases or solids that can "poison" the catalyst. Edwards' preferred method for N_2O abatement is combustion in a reducing environment in a carefully controlled, inward fired combustor. The reducing agent may be methane (a commonly used fuel gas) or even a hydrogen-containing process gas such as silane (often used in conjunction with N_2O). The flow of the reducing agent must be closely regulated and synchronized, ideally with real-time signals from the process tool.

Oxidation, by combustion in air (in the absence of a reducing agent), will convert N_2O to NO_2, which then requires additional abatement, usually by scrubbing. Oxidation and NO_2 production can also occur unintentionally in a non-optimized reducing combustor.

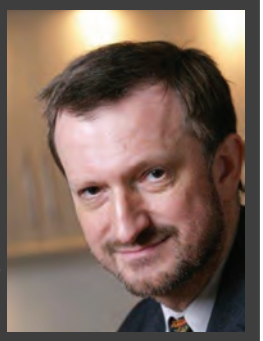
Q What about NOX?

A NOX is a generic term for mono-nitrogen oxides (NO and NO_2). These are produced during combustion in air, especially at high temperatures and in the presence of hot metal surfaces. NOX emissions cause smog, which can damage lung tissue, especially in vulnerable individuals. NO has a TLV of 25ppm and NO_2 of 3ppm. NOX eventually forms nitrous and nitric acids, components of acid rain. For these reasons, NOX emissions are tightly regulated in most territories worldwide.

Q What's the take-away?

A Both the IPCC and the ITRS recognize N_2O is a greenhouse gas pollutant that should be abated. Proven abatement technologies exist. Of them, reducing combustion has the advantage of minimizing the production of NOX, when executed in a carefully controlled, well-designed system synchronized with process gas flows.

About the author:
Mike Czerniak is Environmental Solutions Business Development Manager at Edwards. He earned his PhD in Electrical Engineering at Manchester University (UK) in 1982. His professional career began with Philips in their UK R+D labs and subsequently in their Nijmegen, Holland fab. He had subsequent marketing roles at UK-based OEMs including Cambridge Instruments, VSW and VG Semicon before joining Edwards in 1997. Mike has numerous published articles and patents to his name; he co-chairs two SEMI standards committees; participates in the IRDS; is a UK PFC expert on the United Nations IPCC (Intergovernmental Panel on Climate Change; he is now an IPCC lead author); he wrote the chapter on Vacuum and Environmental Issues in the Handbook of Semiconductor Manufacturing (2nd edition). He has been a Visiting Industrial Professor in the School of Chemistry at the University of Bristol since September 2017.



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As 2017 wound to a close, double-digit semiconductor sales growth left manufacturers hoping for a robust 2018. Twelve months have since passed with the year delivering mixed results; many positive. Alternately, the simmering US-China trade dispute escalated when Huawei's CFO was detained in Canada at US request; Brexit has UK and the broader EU focused on what happens after 29th March. Growth continued for much of 2018 even as chip and equipment sales slid in late third quarter. Opportunities and cautions marked the start of 2019 as industry began what will surely prove to be a pivotal year for semiconductor manufacturing.

Mark Andrews, Technical Editor explains

A remarkable year in **semiconductor manufacturing**

The global semiconductor industry celebrated 2017's performance as final figures from most analysts and industry watchers tallied chip sales growth of more than 22 percent. Although many forecasters thought 2018 could slide backwards, much of the year saw high growth levels accompanied by notable innovations and news of promising research developments that could prove foundational for future industry growth.

And then there was the US-China trade war. Tensions were already at a high level by mid-2018, with both countries trading accusations and threats of higher tariffs, which regularly sent shock waves through their respective financial sectors and stock exchanges. After valuations of some Chinese companies slid as much as 20 percent, and US stock markets took a roller coaster ride much of fourth quarter, anxiety was at an all-time high after a meeting between China's President, Xi Jinping and US President Donald Trump failed to reach an accord when the two met at the G-20 summit in Buenos Aires on 29th November.

Tensions between China and the US ratcheted to a new high just days later when on 1st December Huawei's CFO, Meng Wanzhou (daughter of the company's founder), was arrested in Canada at request of the US while she attended an industry conference. Wanzhou remains in Canada on bail awaiting a February hearing. Following those events and continuing tensions between US and Chinese leaders, the US stock market went on its wildest December ride in recent history, erasing all the gains of 2018, a performance that included a new 'lowlight': a 650-point slide on Christmas Eve—the largest in the Exchange's history for the day before Christmas. With these events as a backdrop, the US president and Congress could not agree on continuing funding resolutions that shuttered many US governmental agencies in December while others are kept operating under emergency protocols. What a way to end the year! The shutdown continued as of this writing, but both sides vowing to stand their ground.

As political tensions kept financial sectors on their toes, semiconductor manufacturers were focused on near- and long-term prospects, earnestly working towards engineering solutions and business innovations that will steer towards better products at lower costs and greater efficiencies. 2018 also saw several large-scale acquisition bids stall or fail, with Qualcomm rejecting a $121 billion bid from Broadcom in February, while four days later the company increased its offer to $44 billion in its efforts to purchase NXP. Other major acquisitions went forward, but none valued at the tens of billions of pounds, euros or dollars as we saw in 2017 and 2016. Yet the 2018-year end and holiday gift giving season was the strongest ever, raising hopes that trade disputes and other international misgivings will impede continued growth across semiconductor sectors. 2018 saw many highlights with many notables highlighted in the coming pages.

2017 Chip Sales Grew More than 22 Percent

According to researchers at Gartner, semiconductor sales grew by 22 percent in 2017 to reach a record (USD) $419.7 billion; memory chip sales led the way according to the firm's preliminary report. Gartner (Stamford, Conn.) estimates that increased sales of memory chips due to shortages of NAND flash and DRAM accounted for about two-thirds of overall chip market growth in 2017. Memory also become the single largest semiconductor products category last year, they said.

Gartner's figures of $419.7 billion, even though preliminary, are more aggressive than the latest forecast issued by the World Semiconductor Trade Statistics (WSTS) organization in December 2017. The WSTS — an organization of more than 50 semiconductor companies that pool sales data — expects 2017 semiconductor sales to be about $409 billion, an increase of 21 percent compared with 2017.

As expected, the world's largest memory chip vendor, Samsung Electronics, rose to the top spot in overall semiconductor sales for the first time. Samsung displaced Intel, which had held the top spot in sales every year since 1992. Samsung's 2017 chip revenue of $62.2 billion accounted for 14.6 percent of the industry's total, while Intel's $57.7 billion in sales was good for about 13.8 percent of the market, according to Gartner.

Andrew Norwood, a research vice president at Gartner, said he expects memory pricing to weaken in 2018 and 2019, which would cause Samsung to lose the gains in revenue it has made and could boost Intel back to the top spot. "Samsung's lead is literally built on sand, in the form of memory silicon," Norwood said in a press statement.

In fact, Samsung could slip all the way to the No. 3 in chip sales when the next memory downturn hits in 2019 as researchers forecast, if plans for Qualcomm to acquire NXP Semiconductors and Broadcom to acquire Qualcomm come to fruition, according to Norwood. However, other analysts including Bill McClean of IC Insights believe that Samsung's dominance in memory and strength in other semiconductor product categories will make it difficult for Intel to beat, even when the memory cycle turns.

Forecasters predict a sales slowdown

The mood of semiconductor executives at the Industry Strategy Symposium was upbeat albeit somewhat restrained at their annual gathering in Half Moon

Bay (California). The weather was an appropriate backdrop for the cautious optimism market watchers recommended here.

Semiconductors should have another good year in 2018, but growth is slowing, they said. Further out, a downturn may be coming for the industry and the broader economy — but just when and why is still not clear, speakers said.

Gartner predicts after last year's 22.2-percent revenue surge, the chip market will settle down to a still better-than-average 7.5-percent growth this year. It predicted the chip market will cool off in 2019 and 2020 with two basically flat years. (By July 2018, most forecasters including the SEMI trade group revised their figures, with most calling for chip sales growth of about 15 percent for 2018.)

US government approves a Chinese firm's acquisition

A Chinese supplier of semiconductor manufacturing equipment has finalized the acquisition of Akrion Systems, a US provider of wafer surface preparation tools, following approval of the deal by US officials. (This relatively small event would prove to be one of the few highlights in China-US relations throughout 2018.)

Beijing-based Naura Microelectronics Equipment Co. Ltd. said this week it closed its $15 million deal to acquire Pennsylvania-based Akrion. The deal is believed to be the first acquisition of a US semiconductor technology company to be approved the Committee on Foreign Investment in the United State (CFIUS) since Donald Trump was sworn in as US president.

Handel Jones, founder and CEO of market research and consulting firm International Business Strategies Inc. (IBS), characterized the acquisition of a niche player in semiconductor equipment as something of an outlier, saying the approval by CFIUS is not likely indicative of a general shift in stance by Washington.

"I don't think it moves the needle at all," Jones said. "I think the policy [of blocking U.S. chip firms from being acquired by Chinese firms] is going to become more restrictive rather than less restrictive in the next six to 18 months."

Over the past two years, Washington has grown increasingly wary of efforts by Chinese companies to acquire U.S. and Western tech firms in general; they are especially concerned about efforts to acquire advanced semiconductor firms. In one high-profile example, Trump last year blocked the proposed acquisition of Lattice Semiconductor by Canyon Bridge Capital Partners, an investment firm funded in part by China's central government, after CFIUS recommended that he do so.

China has indicated that it plans to spend more than $160 billion over 10 years to beef of its domestic semiconductor industry to provide more parts to massive internal electronics markets. US business advocates and politicians have expressed concern that China's ambition and policies that distort the market in its favor represents a threat to US standing in the semiconductor industry.

Osram Moves from Lightbulbs to Optoelectronics

Osram, a German company once known in the United States for Sylvania light bulbs (Osram GmbH acquired GTE's Sylvania lighting division in 1993), identifies itself as a "tech company" rather than an LED specialist, pointing towards the company's longer-term ambitions. Osram is driving R&D projects into such diverse fields as broader usages of illumination tech, sensing and visualization.

If its booth at the Consumer Electronics Show earlier this month was any indication, Osram is a core light-source supplier to LiDAR systems that analyze vehicles' surroundings as well as a provider of headlights that shine the road ahead but can automatically adjust intensity to prevent blinding oncoming vehicles or pedestrians. Osram also provides lights for iris scanning and facial recognition in smart phones in addition to sensors embedded in wearable devices.

After successfully divesting its lamps business, Osram GmbH — with 4 billion euro earnings in FY 2017 — last year generated revenues from three business units: Opto Semiconductors (1.7 billion euros), Specialty Lighting (2.3 billion euros) and Lighting Solutions and Systems (1.0 billion euros).

Today, Osram Opto Semiconductors (Regensburg, Germany) is the world's second largest manufacturer of optoelectronic semiconductors after Japan's Nichia.

EU display panel firms get funding

Displays received plenty of attention from investors this week in Europe, with two firms announcing funding for developing next-generation technologies: one working on a 3D LED technology based upon nanowires, the other at an earlier stage looking at new reflective technology that it believes will enable low cost, printable dynamic displays.

In France, Aledia, a developer and manufacturer of 3D LEDs for display applications based on its gallium-nitride-nanowires-on-silicon platform, closed a (USD) $37 million Series C financing round with Intel Capital as a new investor, bringing its total funding to date to around 67 million euros (about $83 million at current exchange rates).

Meanwhile, in the UK, Bodle Technologies, an Oxford University spinout that says it aims to transform how and where we interact with displays, attracted about $8.5 million in Series A funding.

Both companies have teams with strong management expertise from previous work in optical technologies: Aledia execs gained experience from Bookham while Bodle senior leaders worked at Cambridge Display Technologies.

Aledia is targeting greater efficiency and brightness for mobile displays, as well as emerging requirements for virtual reality and augmented reality displays. Giorgio Anania, CEO, chairman and co-founder of Aledia, said that current 2D LEDs face major manufacturing difficulties that its nanowire technology aims to overcome. "If you succeed in developing this technology for creating complex mobile displays, then it is a $75 billion market just in this sub-sector," Anania said.

Nvidia to partner with Continental on vehicle automation

Nvidia is teaming up with German tier one automotive supplier Continental to develop "top-to-bottom AI self-driving vehicle systems" built on the Nvidia Drive platform. They are planning on a market introduction starting in 2021.

Elmar Degenhart, Continental CEO, and Jensen Huang, founder and CEO of Nvidia, finalized the partnership to create AI-based highly automated vehicle systems on 2nd February.

For Continental, the partnership with Nvidia is neither the first nor an exclusive deal in the automated vehicle platform segment. The company last June made a similar announcement with the BMW/Intel/Mobileye group, Nvidia's rival, as a member of their self-driving platform alliance.

Many tier ones, however, are expected to specialize in select platforms, or will be more focused on developing interfaces between different modules. "Probably traditional OEM-Tier One relationship (one OEM sourcing only one semi-owned tier one's system) like Toyota-Denso or Hyundai-Mobis may not be competitive any more, and more versatile and flexible tier ones would survive" in the future.

Chip market finishes record 2017 with strong December sales

Semiconductor sales grew again on both a sequential and annual basis in December (2017), capping a record year in which the industry's total global revenue exceeded $400 billion for the first time, according to the Semiconductor Industry Association (SIA).

The three-month moving average for chip sales totaled a record (USD) $38 billion in December, up 0.8 percent from November and 22.5 percent compared to December 2016, according to the SIA. December's sales brought the total for the year to $412.2 billion, up 21.6 percent compared to 2016 the group said. The SIA reports sales figures compiled by the World Semiconductor Trade Statistics (WSTS) organization.

Fourth quarter 2017 chip sales also set a new all-time high for semiconductor sales for the fourth consecutive quarter. Sales totaled $114 billion in the fourth quarter, up 22.5 percent compared to the fourth quarter of 2016 and up 5.7 percent compared with the third quarter of 2017.

Chip sales soared early in 2017 and picked up steam throughout the year. The market was boosted by high average sales prices for memory chips amid a shortage. Memory revenue increased by 61.5 percent in 2017, with DRAM sales growing by a staggering 76.8 percent while NAND sales increased by 47.5 percent, according to WSTS.

Chinese firm to open UK chip R&D center

The China-based parent company of Dynex Semiconductor announced that it is establishing a semiconductor R&D center in the UK. The center will employ up to 200 engineers over the next three years and provide additional research capability for its CRRC's two UK subsidiaries, Dynex and Soil Machine Dynamics.

CRRC Times Electric, a Chinese developer of rail and electric vehicle control systems, said it plans to establish the Times Electric Innovation Centre (TEIC) in the first half of 2018 in Birmingham, England. It will focus on cutting-edge research and development of semiconductor-based products and technology across a wide power range.

This research will be applicable to key growth markets, including electric vehicles, rail traction, aerospace, power distribution and renewable energy, the firm said.

Dynex is headquartered in Lincoln, which is located in England's East Midlands region, where it plans to continue conducting R&D. In the last 12 months, Dynex has been heavily focused on new product such as its trench gate and DMOS high-power IGBT modules, press-pack IGBTs, new HVDC products, and the launch of its new foundry services business. The Lincoln R&D center expects to have more new product releases in the coming months from Dynex.

"The TEIC will have significant capabilities in semiconductor innovation, as well as other power electronics and related systems," said Clive Vacher, Dynex president and CEO. "It will support Dynex, SMD, and all CRRC entities. Over time, its capabilities will develop in several different directions and will not be limited to high-power semiconductors."

Qualcomm says more 5G OEMs, carriers will use its platform

Qualcomm announced that 19 OEMs plan to use its Snapdragon X50 5G cellular modem and 18 carriers will conduct 5G field trials with the platform. The news marks some of the first system commitments in a race to deliver commercial 5G devices and services by early 2019.

The OEMs include five of the top 10 smartphone makers, but not Apple or Huawei. Wall Street analysts speculate that Apple is poised to shift entirely to Intel LTE modems in its next handsets, and Huawei's HiSilicon division may design a 5G baseband on its own or in its partnership with Taiwan's Mediatek. Samsung, the world's largest smartphone maker, announced previously that it is working with Qualcomm on 5G.

Qualcomm listed as users of its 5G baseband top smartphone vendors Oppo and Xiaomi, ranked fourth and fifth, as well as LG and ZTE, also in the top 10, according to Strategy Analytics. Among its other 5G customers are Asus, Fujitsu, HMD Global, HTC, Sharp, and Sony.

Qualcomm said that 18 carriers have committed to use the X50 chip in sub-6 GHz and millimeter-wave field trials, planning to roll out commercial 5G services in 2019. While not be Qualcomm's direct customers, they typically have chipset certification programs that are checkboxes for OEMs getting products to work on their networks. The carriers include AT&T, British Telecom, China Telecom, China Mobile, China Unicom, Deutsche Telekom, KDDI, KT Corporation, LG Uplus, NTT Docomo, Orange, Singtel, SK Telecom, Sprint, Telstra, TIM, Verizon, and Vodafone Group.

Qualcomm Again Spurns Broadcom's M&A Bid
Qualcomm has again rejected a $121 billion acquisition offer from Broadcom after a meeting between the two companies last week. At the same time a prominent shareholder advisory firm recommended that Qualcomm continue to engage in negotiations on a deal.

In a letter to Broadcom President and CEO Hock Tan Friday (16 February), Qualcomm said its board of directors once again unanimously rejected Broadcom's takeover bid as too low, but said the company was willing to engage in further discussions.

Qualcomm said Broadcom representatives expressed a willingness to agree to anti-trust related divestitures but resisted other commitments that might be required by regulatory bodies.

Qualcomm raises NXP offer to $44 billion

Qualcomm entered into a new amended acquisition agreement with NXP Semiconductors, worth $44 billion, in a move that may cause Broadcom to abandon its hostile takeover attempt of Qualcomm.

Qualcomm said Tuesday (20th February) that the new deal to acquire NXP is worth $127.50 per share in cash, up from the initial $110-per-share price that the companies agreed to 16 months ago.

Qualcomm's acquisition of NXP, first announced in October 2016, has been cleared by most antitrust review agencies throughout the world. However, the deal is still awaiting the seal of approval from China's Ministry of Commerce. Signoff from China was reportedly expected sometime this month, although some reports have since suggested that the approval may take even longer to secure.

Thus far, the deal hasn't come anywhere close to the threshold of 80% of shares tendered that the original agreement required. However, Qualcomm said Tuesday that it has entered into binding agreements with nine NXP shareholders who collectively own more than 28% of NXP's outstanding shares.

Qualcomm was forced to sweeten the deal partly because of NXP's financial success and stock performance in the time since the proposed acquisition was announced. Several large institutional shareholders have said publicly in recent months that they would not support the acquisition at the original purchase price, which totaled roughly $38 billion.

The revised deal could cause Broadcom to withdraw its $121 billion bid to acquire Qualcomm, a proposal that Qualcomm's board has twice voted unanimously to reject.

Random EUV defects seen at 5nm node

Researchers reported random defects appearing in extreme ultraviolet (EUV) lithography at 5nm nodes, prompting an array of efforts to eliminate them. However, there was no clear solution in sight when the news surfaced in February 2018.

The news came as Globalfoundries, Samsung, and TSMC are racing to rev EUV systems up to high availability with 250W light sources for 7nm production next year. The defects show that there's no panacea for the increasing costs and complexity of making semiconductors.

The latest EUV scanners can print the 20-nm-and-larger critical dimensions that foundries plan at 7nm, said Greg McIntyre, a patterning expert from the Imec research institute in Belgium. However, their ability to make finer lines and holes is unclear, a point made during a talk at the 2018 SPIE Advanced Lithography conference.

Optimists such as McIntyre believe that a basket of solutions will emerge for the so-called stochastic effects. Some skeptics see the results as one more reason to doubt that the expensive and long-delayed EUV systems will become mainstream tools for chipmakers.

The latest defects are cropping up at critical dimensions around 15nm needed to make 5nm chips for foundry processes targeting 2020. EUV maker ASML is preparing a next-generation EUV system for printing finer features, but those systems won't be available until about 2024, it said at the event last year. The random defects take many forms. Some are imperfectly made holes; others are tears in lines or shorts where two lines or two holes meet. Given their tiny dimensions, researchers sometimes spend days just to find them.

Another issue is that it's unclear exactly what happens to resist materials when hit with EUV light. "It's still unknown how many electrons are generated and what kinds of chemistries are created … we're a little way from a full understanding of the physics, so we're doing more experiments," said McIntyre, who also noted that researchers have tested as many as 350 combinations of resists and process steps.

Semiconductor sales continue growing

The calendar may have turned to 2018, but semiconductor sales show no signs of slowing the blistering pace that characterized 2017, according to the Semiconductor Industry Association (SIA). Chip sales increased on an annual basis in January (2018) for the 18th consecutive month, according to the SIA trade group. Sales in January decreased 1 percent compared with December, reflecting a typical seasonal slowdown.

The three-month average of chip sales reached $37.6 billion in January, up 22.7 percent from January 2017, according to the SIA, which reports figures compiled by the World Semiconductor Trade Statistics (WSTS) organization, a group made up of more than 50 semiconductor companies that pool sales data.

"All major regional markets saw double-digit growth compared to last year, with the Americas leading the away with year-to-year growth of more than 40 percent," said John Neuffer, the SIA's president and CEO, in a press statement. "With year-to-year sales also up across all major semiconductor product categories, the global market is well-positioned for a strong start to 2018."

Last year, chip sales rose by 21.6 percent to reach a record $412.2 billion. It marked the first time the industry posted more than $400 billion in sales, just seven years after eclipsing the $300 billion mark for the first time.

On a year-to-year basis, chip sales increased by 40.6 percent in the Americas region and 19.9 percent in Europe. Sales grew by 18.6 percent in the Asia Pacific region, by 18.3 percent in China and by 15.1 percent in Japan, according to WSTS. However, on a sequential basis, sales rose only in Europe, which increased by 0.9 percent. Sales were roughly flat month-to-month in China, but fell in the Americas, Japan and the Asia Pacific region, WSTS said.

Broadcom's Jericho2 rides a 2.5D stack to leapfrog competing ASICs

Broadcom's latest communications processor rides a 2.5D chip stack with HBM2 memory. Their Jericho2 uses the boost in memory bandwidth to substantially surpass the performance of OEM ASICs in high-end switches and routers.

The chip expands into networking the packaging technology pioneered by AMD, Nvidia, and Xilinx in high-end FPGAs and graphics processors, the company indicated. With its StrataDNX Jericho2, Broadcom also takes a small step toward open-programming environments by providing C++ tools for the chip to select customers.

The 16nm processor, announced Tuesday (6th March), packs a whopping 208 50-Gbits/s PAM4 SerDes to deliver 10 Tbits/s of aggregate throughput, supporting up to 36 400-Gbits/s Ethernet links. It leads a wave of high-end networking devices aiming to enable 400-Gbits/s links in telecom core networks and large data centers.

Google joins the quantum race

This week Google leaped into an increasingly competitive race in quantum computing with its Bristlecone 72-qubit processor. IBM has an operational 50-qubit quantum computer. Intel has shipped a 49-qubit quantum processor to its research partners for testing. Rigetti has an operational 19-qubit quantum computer. D-Wave has an operational 2048-qubit annealing quantum computer, and Fujitsu has an operational 1024-qubit annealing quantum computer. The last two are not so-called general-purpose systems, but they are still relevant to the industry racing to quantum supremacy.

Quantum supremacy is the crossover point when quantum computers can solve or massively accelerate relevant problems that classical computers cannot solve today. Proof of quantum supremacy also requires that the result of the quantum program can be validated.

Google joined this race when it announced its internal delivery of its 'Bristlecone' system for testing with its research partners. Google did not say it has run programs on the new quantum processor. However it did say the following:

"The purpose of this gate-based superconducting system is to provide a testbed for research into system error rates and scalability of our qubit

technology, as well as applications in quantum simulation, optimization, and machine learning…We are cautiously optimistic that quantum supremacy can be achieved with Bristlecone, and feel that learning to build and operate devices at this level of performance is an exciting challenge!"

Optical Networks prep for 400G and beyond

As many as a dozen companies are expected to demo prototype 400 Gbit/second Ethernet optical modules at this week's Optical Fiber Conference (OFC) that data center and telco networks expect to deploy starting late next year. At the same time, standards efforts are already seeking a pathway for the next generation of optical-based technologies to keep up with rising demands.

The emerging 400G products typically use eight 50G serial connections based on the latest PAM-4 modulation techniques. Last week, the IEEE gave preliminary approval to start work on standards for 100G serial links that could drive future 800G Ethernet standards.

Meanwhile, the Consortium for On-Board Optics (COBO), an ad hoc group of about 70 companies, released its first specification for modules embedded on routers and switch motherboards. The spec aims to reduce heat and power issues for 400-800G products as the first step toward a future of merged optical and electrical components.

All the efforts face tough balancing acts achieving the highest possible data rates while maintaining acceptable distance, power, heat and cost. They come at a time when optical links are now widely used inside data centers and carrier central offices. Today's large data centers are transitioning from 10G to 25G Ethernet inside racks of servers, deploying 100G Ethernet between the racks.

"400G is the next phase…People are hoping by late 2019 or early 2020 to start deploying, and it looks like a lot of the components are coming on line now; we're already seeing the switch silicon showing up," said Brad Booth, a networking specialist for Microsoft's data center group and chairperson of COBO.

France's Prophesee Expects Event-Driven CIS, Lidar In fast-growing factory automation industries as well as IoT and autonomous vehicles markets, CMOS image sensors appear destined for a role capturing data not for human consumption, but rather for machines to see what they need to make sense of the world.

CMOS image sensors, "…are becoming more about sensing rather than imaging," said Pierre Cambou, activity leader, MEMS & Imaging at Yole Développement in a recent report. The market research and technology analysis company (Lyon, France) predicts that by 2030, 50 percent of CMOS image sensors will serve "sensing" devices.

Paris-based Prophesee SA (formerly Chronocam) styles itself as a frontrunner in that revolution. A designer of advanced neuromorphic vision systems, it advocates an event-based approach to sensing and processing. Prophesee's bio-inspired vision technology has been deemed too radically different from conventional machine vision by some market analysts, with some even edscribing it as, '…perilously ahead of its time…' But Luca Verre, co-founder and CEO of Prophesee, has stated in media reports that this is no longer the case.

Verre said that his company has secured its Series B+ funding (the startup raised $40 million in funding in the last three years). It now has a partnership deal with a large unnamed consumer electronics company. Most importantly, Prophesee is now advancing its neuromorphic vision system from the usual technology concept pitch to promoting its reference system for consideration by developers.

Prophesee's first reference design, available in VGA resolution, consists of Prophesee's Asynchronous Time-Based Image Sensor (ATIS) chip and software algorithms. The ASIC will be manufactured by a foundry partner in Israel, said Verre. The company declined to detail its ASIC and the specification of the reference design. Prophesee said that it is planning on a formal product announcement at a future date.

Nonetheless, the startup reached a milestone when the reference design proved able to offer system designers the opportunity to see and experience just what an ATIS can accomplish in data sensing. The ATIS will be characterized by its high temporal resolution, low data rate, high dynamic range, and low power consumption, said Prophesee.

KLA-Tencor buys Israel-based Orbotech for $3.4 Billion

Chip equipment vendor KLA-Tencor announced on 20th March that it is set to acquire Israel-based Orbotech for (USD) $3.4 billion in a move that the firm says will help diversify its revenue base and add $2.5 billion of addressable market opportunity in high-growth printed circuit boards, flat panel displays, packaging and semiconductor manufacturing.

KLA-Tencor (Milpitas, California) says the broader portfolio of products and services as well as increased exposure to technology megatrends will support its long-term revenue and earnings growth targets.

"This combination will open new market opportunities for KLA-Tencor, and expands our portfolio serving the semiconductor industry," said Rick Wallace, KLA-Tencor's president and CEO, in a statement. "Our companies fit together exceptionally well in terms of people, processes, and technology." Wallace added

that KLA-Tencor has had a strong presence in Israel over the years and said this deal would further expand its operations "in this important global technology region."

Incorporated in 1981, Orbotech recently announced that SPTS Technologies, a supplier of advanced wafer processing solutions for semiconductor and related industries that it acquired in 2014, had received $37 million in orders for multiple etch and deposition systems from two GaAs foundry customers. The company's Omega plasma etch, Delta PECVD and Sigma PVD systems are to be used to manufacture RF devices, including power amplifiers, for 4G and emerging 5G wireless infrastructure and mobile device markets. Orbotech will continue to operate under its own brand as a standalone business of KLA-Tencor based in Yavne, Israel.

Web giants want optical, flash advances

Web giants Facebook and Microsoft joined other datacom/data center moguls in calling for significant shifts in networking, storage and software at the Open Compute Summit to keep their heads above a rising flood of data.

Facebook said it will need switch ASICs with optical interfaces within three years for its next big network upgrade. Microsoft announced a new low-level interface for NAND flash drives to make better use of storage. And the Open Compute Project (OCP) struck a partnership with the Linux Foundation to plug holes integrating and testing systems and software together.

Interestingly, little was said about the adoption of machine learning, the latest force driving the data explosion. Security, however, is a rising focus with increasing support for a root-of-trust module announced last year and a broader security project just getting off the ground.

More than 3,000 people registered for the ninth annual event sponsored by OCP and launched by Facebook in 2011. The group now has 175 members that have created 375 specifications related to open hardware for data centers. Indeed, even OCP's most vocal members, the aforementioned Facebook and Microsoft, showed separate flavors of server and switch designs. The largest data center operator, Amazon, continues to quietly go its own way.

Can Huawei Match Apple's 'TrueDepth'?
Now that Samsung's Galaxy S9 is already on the market and Huawei's P20 announcement is looming large (the Chinese mobile giant will hold a press conference at the end of March), imaging experts have declared 3D sensing the new battleground for the mobile industry.

That being said, it is far from clear whether Samsung or Huawei will be able to catch up with Apple's iPhone X, according to leading researchers at Yole Développement (Lyon, France.) The bar set by Apple's TrueDepth camera is so high, according to Pierre Cambou, activity leader for MEMS and imaging at Yole, that the group predicts it may take a year or longer for competitors to offer 3D sensing technologies comparable to iPhone X.

Unlike the megapixel race of olden days, 3D sensing will be a tougher challenge for most smartphone vendors simply because a 3D camera contains myriad components that need to be aligned. It also requires very competent supply chain management. Cambou called the 3D camera "a bundle of sub-devices." He said, adding that in the iPhone X key suppliers include STMicroelectronics, LG Innotek, Foxconn, ams, and Lumentum—all leaders in their fields

As for Samsung's Galaxy S9, some reviewers are already calling its front-facing sensing technology "a disappointment." A CNET story earlier this month said: "An in-depth look at Samsung's new biometrics verification system (and how it stacks up against the iPhone X's Face ID,) shows it is not quite safe enough for mobile payments." This is because Samsung's facial recognition system uses a regular camera to create a 2D map of the user's face, contrasted with Apple's Face ID, which creates a complex 3D scan of a user's facial pattern. People were able to fool Samsung's technology on last year's Galaxy S8 by using photos. Apparently, that trick still works with the S9.

MRAM uptake prompts MCU design

Magnetoresistive random access memory (MRAM) is gathering steam as an alternative to incumbent memory architectures through increasingly cost-effective applications and through this an ecosystem is also emerging to support it.

eVaderis recently announced co-development efforts on an ultra-low-power microcontroller (MCU) reference design using GlobalFoundries's embedded MRAM technology on the 22-nm FD-SOI (22FDX) platform. Together, the companies are looking to support a wide range of low-power applications such as battery-powered Internet of Things (IoT) products, consumer and industrial microcontrollers, and automotive controllers.

GlobalFoundries has been aggressive on the MRAM front of late. As one of several foundries that publicly announced plans to put MRAM into production by the end of last year and into 2018, it has a deep collaboration with Everspin Technologies, the first MRAM maker to gain any commercial traction with the emerging memory. At the 2017 International Symposium on VLSI Technology, Systems and Applications in Japan, Globalfoundries outlined in a technical paper Everspin's progress with moving eMRAM forward into the 22-nm process node and how it can significantly improve data retention for embedded applications. Meanwhile, Spin Transfer

Technologies has made progress recently on its efforts to commercialize MRAM technology.

FCC votes to exempt small cells from some citing review steps

The Federal Communications Commission (FCC) adopted new rules that include removing small cells from some environmental and historical review processes. While that should accelerate 5G deployment in rural areas, it's not without controversy.

Specifically, the FCC's press release noted that one of the new rules excludes small wireless facilities deployed on non-Tribal lands from National Historic Preservation Act (NHPA) and National Environmental Policy Act (NEPA) review, concluding that these facilities are not 'undertakings' or 'major federal actions.' Small wireless facility deployments continue to be subject to currently applicable state and local government approval requirements.

Small cells are but one part of an overall wireless network. They can provide cellular access in otherwise inaccessible places, and augment larger area coverage networks for fill coverage gaps or augment system deliverables during peak traffic periods.

All five FCC commissioners agreed that there is a need to deploy 5G and to keep the US at or near the top of 5G development. In this case, 5G deployment centers around small cell coverage approaches. One advantage of small cells over macro cells comes in the form of smaller antennas. Especially if the cells use millimeter wave frequencies (28 GHz, 39 GHz, and others in the US) All commissioners agreed that existing rules for deploying cells are now outdated as technology has advanced.

Security outlook getting darker said RSA attendees, experts

Thirty-four companies have signed onto a position statement advocating the idea that hardware design needs to focus more on security and less on performance, according to some experts at the annual RSA Conference in San Francisco in mid-April. All sides agreed that the number and sophistication of threats are growing in a landscape where tech companies and governments can be both adversaries and partners.

To fight back, Brad Smith, President and chief legal officer of Microsoft, announced the Cybersecurity Tech Accord, an agreement initially among 34 tech companies including ARM, Cisco, Dell, Facebook, HP, and Microsoft.

They agreed not to participate in government cyberattacks and to collaborate on stronger defenses for their customers. So far, giants including Amazon, Apple, Alphabet, and Twitter did not sign the Microsoft-led pledge.

Participants at the meeting noted that in the past year the dark side of social networks was revealed in greater clarity following the 2016 US presidential election. According to attendees and participating companies, the past year brought the largest government-sponsored attacks to date. It also has shown that blockchain and quantum computing are neither immediate threats nor panaceas for security, said the experts.

"The threat picture is getting darker," said Kirstjen Nielsen, Secretary of the U.S. Department of Homeland Security (DHS), in a keynote at the event that attracted nearly 50,000 registrants. "In each morning briefing, I see digital threats multiplying faster than we can keep up."

Last year's (2017) Equifax hack alone exposed data of half of all U.S. citizens. NotPetya was considered the costliest single hack to date, and the annual costs of cyberattacks are projected to hit $6 trillion, or 10% of the world's GDP, in a few years.

"Our adversaries are getting more sophisticated and sinister and harder to detect … with diverse actors and objectives … every facet of our society is targeted at every level," she said.

"We live in an era when we feel the attackers are winning," said Ron Rivest, co-developer of RSA, one of the first public-key-cryptography systems.

The state-sponsored NotPetya and WannaCry attacks were a wakeup call, said Microsoft's Brad Smith. "We saw governments attack civilians in a time of peace — these are not just attacks on machines; they are endangering people's lives."

Switch Chip startup snags $77 million

Startup Innovium announced on 25th April that it secured (USD) $77 million in Series D financing, bringing its total to date to a whopping $160 million. The deal shows investors have confidence the designer of Ethernet switch chips will grab sockets away from Broadcom, which currently dominates the field.

The round closes as Innovium announced it is sampling its 12.8 and 6.4 Terabit/second switches aimed at large data centers. The funds will be used in part to ramp production of the chips and fuel their road map.

The news comes four months after Broadcom announced its own 12.8 Tbit/s switch, the Tomahawk-3. Market watchers say Broadcom

commands a 73 to 94 percent share of the $1 billion market for Ethernet switch chips. Its closest rival, Cisco Systems, takes most of the rest with systems using its own ASICs.

Innovium is one of seven semiconductor startups and established companies angling for a slice of Broadcom's business. Others include Barefoot, Cavium, China's Centec, Marvell, Mellanox and Nephos.

Apple shrugs off iPhone sales fears

After weeks of trepidation in the electronics supply chain over fears of a precipitous decline in sales of the high-end iPhone X, Apple reported on 2nd April its best fiscal second quarter sales and announced plans to invest another (USD) $100 billion in share buybacks.

Apple shrugged off recent warnings of softness in smartphone market demand to report selling 51.75 million iPhones in the fiscal second quarter, which closed March 31. Sales of iPhone units came in slightly below analysts' expectations of about 53 million but were up 3 percent on a unit basis compared with the same period of 2017.

More importantly, Apple's iPhone sales generated $38 billion in revenue for the quarter, an increase of 14 percent compared to the year-ago quarter. The higher iPhone average selling price was generated by the iPhone X — released last November at a retail price of $999 — which remains Apple's top-selling iPhone has been in the most popular iPhone in every week it's been available.

Apple CEO Tim Cook seized on the status of the iPhone X as a "beloved product," telling analysts on a conference call following the quarterly report that this marks the first time since 2014 that a top-of-the-line iPhone model has also been the most popular.

Analysts have questioned the sustainability of the $1,000 price point in the smartphone market. Over the last few weeks, several analysts have cut their forecast for iPhone sales in the first two quarters of calendar 2018.

Apple reported sales of $61.1 billion for its fiscal second quarter, an increase of 16 percent compared with the year-ago quarter and a decrease of 31 percent compared with the previous quarter. The company reported a profit of $13.8 billion for the quarter, up 25 percent year-over-year.

TSMC's roadmap full, but thin

Continuing to move fast in multiple directions at once, TSMC announced on 2nd April that it is in volume production with a 7nm process and will have a version using extreme ultraviolet (EUV) lithography ramping early next year. In addition, it gave its first timeline for a 5nm node and announced a half-dozen new packaging options.

Meanwhile, the foundry is pushing power consumption and leakage down on more mainstream 22-/12-nm nodes, advancing a laundry list of specialty processes and rolling out an alphabet soup of embedded memories. At the same time, it is exploring future transistor structures and materials.

Overall, the Taiwanese giant expects to make 12 million wafers this year with R&D and capex spending both on the rise. It has even started production of 16nm FinFET chips in Nanjing, a big first for China.

The only bad news is that the new process nodes are partial steps delivering thinner gains. The 'new normal' is for performance increases and power reductions that generally fall in a 10% to 20% range, a reality that makes the new packaging and specialty processes increasingly important.

Chip sales running 20% above 2017 pace

Semiconductor sales ran 20 percent ahead of 2017's pace through the first quarter of the year, a strong start to the year in an industry coming off record revenue, according to the Semiconductor Industry Association (SIA) trade group.

The three-month rolling average of chip sales for March totaled (USD) $37 billion, up 20 percent from March 2017 and up nearly 1 percent compared with February, according to the SIA, which reports sales data compiled by the World Semiconductor Trade Statistics (WSTS) organization.

"Sales in March increased year-to-year for the 20th consecutive month," said John Neuffer, SIA president and CEO, in a press statement. "All regional markets experienced double-digit growth compared to last year, and all major semiconductor product categories experienced year-to-year growth, with memory products continuing to lead the way."

Through the first quarter, total worldwide semiconductor sales totaled $111.1 billion, up 20 percent from the first quarter sales in 2017.

March sales were ahead of 2017's pace across all major regions, with growth strongest in the Americas, where sales were up 35.7 percent compared to March 2017, and Europe, were sales were up by 20.6 percent compared with March 2017. Sales also increased on a sequential basis across all regions except the Americas, which declined by 2 percent, according to the WSTS.

Lidar Tech Today, Lidar Vendors Tomorrow
Two factors have turned LiDAR systems into a fair-haired technology in the eyes of investors and the automotive industry. One is the still to be finalized technology landscape for LiDAR's. Alexis Debray, a technology and market analyst at Yole Développement, considers LiDAR "not [yet] mature." He said, "We are at the beginning of big changes" coming to LiDAR. Another is a broadly accepted yet unproven notion that LiDAR is a must-have technology for autonomous vehicles. Yole pointed out that companies like Waymo, Uber, Lyft, Baidu and Mercedes-Benz are integrating "an average of $200,000 worth of sensors [including LiDAR devices] into hundreds of conventional cars," to transform them into fully autonomous vehicles able to operate on city streets.

Key players

In Yole's view, LiDAR technologies have two roots, one coming from digital photography, another derived from laser-based range finders. The complexity and diversity in LiDAR is partly explained by "the mix of these technologies" going into products, Debray noted.

Broadly speaking, two types of LiDAR exist in the automotive field. "Industrial-grade" LiDAR that is used for autonomous vehicle applications such as robotic taxis or buses. The other, which Debray calls "automotive-grade" LiDAR, will be deployed in mass-market consumer autonomous cars.

The industrial grade LiDAR is defined as "durable enough for 24-hours usage, good sensitivity and performance." Since they are used for industrial/commercial applications, the cost of LiDAR, for now, is not a primary concern. They are expensive.

In contrast, when it comes to automotive-grade lidars anticipated in mass-market cars, OEMs worry about everything from price and size to cosmetic look-and-feel.

Thread, Zigbee and Bluetooth Mesh compared

Silicon Labs reported on its recently released benchmarks of Bluetooth, Thread and Zigbee mesh networks for the Internet of Things (IoT), saying in essence that all networks are not created equal, and that different versions of chips running on different networks will perform differently than comparable chips operating on different networks.

Selecting the right mesh protocol for an IoT application can be challenging. Each protocol has its own set of unique characteristics and advantages, depending on use cases and application requirements. Developers need to understand how each protocol performs in the key areas of power consumption, throughput, latency, scalability and security.

Silicon Labs recently released the industry's first performance benchmark results for Zigbee, Thread and Bluetooth mesh, comparing how each protocol performs in different test conditions and network configurations.

Key takeaways include:

- Thread, Zigbee and Bluetooth mesh perform similarly in small networks under small payloads.
- Thread and Zigbee outperform Bluetooth mesh when payload and throughput needs increase. Bluetooth mesh performance can improve after installation if the installer manually optimizes the network by disabling some routing nodes.
- Latency increases for all three protocols as network size grows, but Bluetooth mesh experiences the largest increase.
- For large Bluetooth mesh networks, relay optimization can be used to optimize performance.
- Bluetooth mesh works best when short messages (of 11 bytes or less) are used, especially for multicast messages.

According to Silicon Labs, there is no winning mesh protocol. Performance varies greatly based on the application requirements. The test results underscored several factors that are critical in making the right protocol choice.

Linux-Friendly Arduino Simplifies IoT Development
Arduino's support for Linux IoT devices and single-board computers (SBCs) announced at the Embedded Linux Conference+Open IoT Summit in March cemented Arduino's focus on cloud-connected IoT development, extending its reach into edge computing. This move was likely driven by multiple factors such as increased complexity of IoT solutions and to a lesser extent, by more interest in Arduino boards running Linux.

In a "blending" of development communities for the masses — Arduino, Raspberry Pi, and BeagleBone — Arduino's support for Linux-based boards lowers the barrier of development for IoT devices by combining Arduino's sensor and actuator nodes with higher processor-powered boards like Raspberry Pi and BeagleBone. Top this with a user-friendly web wizard to connect the Linux boards via the cloud and it simplifies the entire process.

Imec and New Company Partner to Shrink SRAM Cells
A startup led by one of the pioneers of flash memory worked with the imec research institute to design the smallest SRAM cells to date. The 0.0205-mm2 and 0.0184-mm2 6T-SRAM cells use a vertical gate-all-around transistor being developed by Unisantis as a building block for tomorrow's leading-edge chips.

The work was one of a handful of announcements at the opening day of the Imec Technology Forum. Other news from imec includes work on more accurate indoor location capabilities over Bluetooth, a dense

lab-on-a-chip, and a camera-free approach to eye tracking, all developed solely by imec.

A team from Unisantis and Imec is using the startup's so-called 'Surrounding Gate Transistor' with a 5nm minimum pillar pitch. The design is suited to a 5nm SRAM, but is less optimal for logic because it would require three of the transistors to provide the performance of a single FinFET.

The Unisantis design is similar to what's generally known as a vertical nanowire, a candidate for years as a future transistor. Vertical nanowire transistors have the potential to reduce chip area significantly, one of the last remaining areas of potential progress in overall CMOS scaling technologies.

To date, most researchers see vertical transistors as having challenges that prevent their practical use in commercial chips for many years. The Unisantis design, in particular, would need two to three times more performance to compete in logic with FinFETs. FinFETs are expected to scale down to use through the 5nm node expected to hit volume production in 2020. A horizontal gate-all-around transistor, sometimes called a nanosheet, nanowire, or nano-slab, is widely expected to be its successor at the 3nm node.

Intel to Spend $5 Billion on 10nm Fab in Israel
Intel Corporation announced that it plans to invest (USD) $5 billion over the next two years to upgrade its fab in Kiryat Gat in Israel from 22nm to 10nm technology.

There was no official announcement from Intel, but Israel's ministry of finance said in a statement that approval is expected from Israel's governmental bodies in weeks and that the new plant will employ an additional 250 people. Intel had apparently considered several possible expansion sites but, after two years of discussion with Israel's finance ministry, decided to expand its site in the country.

Intel has been a major employer in Israel, starting with five employees in Haifa in 1974, and has invested about $11 billion since then. Now the company employs 10,000 people in the country directly, with 60% of employees in research and development.

The Four Essential Elements of Testing IoT Devices
IoT devices present tremendous opportunities, but at the same time have the potential to pose a tremendous threat to cybersecurity. Many devices have weak security features and receive insufficient testing. The global Internet of Things (IoT) market is slated to grow to (USD) $8.9 trillion by 2020. IoT segments in the B2B sector alone will generate more than $300 billion annually by 2020, according to Bain & Company. These figures attest to IoT's enormous potential, and with more than 11 billion connected things projected to be in use this year; its overall potential is already being realized.

But the promise of IoT is not without risk. Hackers have exploited connected devices to mine cryptocurrency and launch high-profile cyberattacks, fostering public distrust and generating regulatory scrutiny that could ensnare a wide range of stakeholders. Amid this climate, it has never been more essential to ensure the proper testing of IoT devices.

Often combining new technology with rapidly developed software on newly created hardware, IoT devices can be difficult to test, and the means by which these devices are developed can expose them to bugs that could undermine functionality, interoperability, reliability, safety, and performance. Here are the four most important aspects to avoiding disaster while enabling IoT to securely fulfill its potential.

Interoperability testing

Software systems' ability to communicate, exchange, and apply information, their interoperability, is at the heart of IoT. When testing interoperability, testers check syntax and data format compatibility, physical and logical connection methods, and user-friendliness. Software programs must be able to route data back and forth without compromising the device's operation or losing data.

Automated test

Companies are delivering software-based services, products, updates, and patches at an ever-accelerating rate. Factors such as time-to-market can make or break a company. Test automation is crucial to both a company's continued, fast-paced operations and time-to-market, making it not a nice bonus but rather an absolute necessity.

Security focus

Shortcomings in security rank among the biggest risks to the continued growth and success of the IoT market. A study conducted by scholars at the Technical University of Denmark, Orebro University in Sweden, and Innopolis University in Russia underscores the legitimacy of such concerns. The researchers found that 80% of IoT devices do not require sufficiently complex passwords, while 70% used unencrypted network services.

Moreover, 70% of devices effectively allowed hackers to identify legitimate user accounts via enumeration. And once hackers gain access to a Wi-Fi enabled lightbulb or some other household device, they can easily gain access to all the devices on the network.

End-to-end testing

Ensuring a system's integrity requires end-to-end testing. The multiple subsystems that comprise a software system must all function properly and collectively, lest the entire system risk failure. End-to-end testing verifies a system's functionality and the proper communication of its sub-systems, which makes this process essential to understanding how well an application will function.

Inside the Summit Supercomputer

Interconnects have long been key to supercomputer performance, but the recent Summit system bucks the trend to proprietary designs by leveraging standards and off-the-shelf components. On June 8, America's Summit supercomputer at the Department of Energy's Oak Ridge National Laboratory was announced as up and running at an impressive 200 petaflops maximum theoretical performance. It became the fastest system in the world, retaking the lead from China which had claimed dominance for several years.

Competition remains stiff. China has multiple exaflop projects expected to be running a year or more before the U.S. has a system at that level.

The Summit supercomputer consists of 4,608 compute nodes, containing a total of 9,216 IBM Power 9 processors and 27,648 Nvidia Tesla V100 GPU modules. The Power 9 and V100 chips talk over NVLink, a high speed, high bandwidth mesh interconnect.

NXP launches mobile wallet solution for wearables, IoT

One of the ongoing challenges for device manufacturers is how to move up the value chain and offer system-level solutions that can add more value than competitors. Addressing the mobile wallet ecosystem, NXP Semiconductors has developed an end-to-end hardware and software solution for OEMs looking to add mobile payment capability to wearable, mobile, or IoT devices.

German high-end luxury goods manufacturer Montblanc is set to use NXP's new solution, mWallet 2Go, in a smartwatch strap. Developed in collaboration with Mastercard and Visa, mWallet 2Go comprises NXP's near-field communications (NFC), secure element (SE), NFC middleware, SE JavaCard operating system, SE applets, secure element management service (SEMS), wallet application and software developer kit (SDK), wallet server, and Mastercard digital enablement service (MDES) and Visa token service (VTS) tokenization platforms. This entire system enables OEMs to develop a pre-certified and validated turnkey solution. Mastercard had already teamed up with NXP to develop a "loader service," an applet and client accessible to developers looking to deploy secure NFC payments.

Wi-Fi Expects New 11ax Standard OK in July

July 1 will be a big day for 802.11ax if all goes according to plan. The 802.11ax standard is the 'next big thing' in Wi-Fi and 1st July is the date that engineers are expected to approve an initial draft of the standard.

It's been a longer-than-anticipated road to get to this point. First and second drafts failed to get the required 75% approval from the group in November 2016 and September 2017. At one point, pundits thought that early 11ax products might ship in 2017.

Typically, IEEE standards take three years. The 11ax group has been at it for four years so far. That's longer than today's 11ac standard took but still shorter than the complex 11n standard before it.

Participants blame the complexity of the spec. It aims to boost users' data rates up to 30% while lowering latency nearly four times and delivering as much as four times the overall data on the same spectrum as today's 11ac.

China tariffs seen hurting tech sector

The Trump Administration is preparing to further ratchet up the budding trade war between the US and China with a series of measures designed to limit the ability of Chinese firms to invest in US companies with 'industrially significant' technology. The administration is also reportedly working to beef up export controls to prevent U.S. technology from going to China.

Meanwhile, the clock is ticking on the tariffs that the Trump Administration announced earlier this month. The first of these measures, which would levy a 25% tariff on about $35 billion worth of Chinese goods, are currently set to take effect in less than two weeks on 6th July.

Many continue to believe that the China tariffs are part of a negotiating strategy by Trump designed to get a better deal to help reduce the $375 billion trade deficit with China. However, at this point, China has not yielded, announcing instead plans to levy similar tariffs on US products, most of which are food related.

The idea of imposing tariffs against Chinese products, many of which are tech goods or materials, is almost universally opposed by economists, analysts and trade groups. While many applaud efforts to protect US industries and intellectual property from policies seen as unfair, opposition experts and groups argue that tariffs will only serve to damage the global business climate and hurt US jobs and wages.

Both the Semiconductor Industry Association and the SEMI trade group have publicly stated their support for exacting better intellectual property protections from China, but don't approve of tariffs, which they say will be bad for business.

"Supply management is reacting quickly to the unfolding US-China trade dispute," said Tom Derry,

CEO of the Institute for Supply Management, another trade group concerned with the looming trade war. "Supply managers across most industries are looking to replace their Chinese suppliers with those from other countries, to avoid the import tariffs. And US corporations are postponing investment because of uncertainty about tariffs.

The first reaction is not good for the Chinese economy, and the second reaction is not good for the US economy, which only goes to show that no one wins in a trade war." The US National Association of Manufacturers (NAM) expressed a similar sentiment.

DARPA unveils $100M EDA project

The US will pour $100 million into two research programs over the next four years to create the equivalent of a 'silicon compiler' aimed at significantly lowering the barriers to design chips. The programs, involving 15 companies and more than 200 researchers, were described for the first time in a talk at the Design Automation Conference by the Defense Advanced Research Projects Agency (DARPA).

The two programs are just part of the Electronics Resurgence Initiative (ERI) expected to receive $1.5 billion over the next five years to drive the US electronics industry forward. ERI will disclose details of its other programs at an event in Silicon Valley in late July.

Congress recently added $150 million per year to ERI's funding. The initiative, managed by DARPA, announced on Monday that the July event will also include workshops to brainstorm ideas for future research programs in five areas ranging from artificial intelligence to photonics.

ERI used the stage of DAC to whet the industry's appetite with what it is doing in areas related to EDA. The July event will be a coming-out party for projects in materials and chip architectures.

With $100 million in finding, the IDEAS and POSH programs represent "one of the biggest EDA research programs ever," said Andreas Olofsson, who manages the two programs.

Together, they aim to combat the growing complexity and cost of designing chips, now approaching $500 million for a bleeding-edge SoC. Essentially, POSH aims to create an open-source library of silicon blocks, and IDEAS hopes to spawn a variety of open-source and commercial tools to automate testing of those blocks and knitting them into SoCs and printed circuit boards.

Sensor network company develops ammeter for IoT Apps

UK-based AltoNovus announced that it has developed a low-range ammeter to measure current consumption in low-power IoT devices. The company's new NanoRanger ammeter comes from a company in a different business than test equipment.

AltoNovus (primarily) develops low-power sensor networks wherein 'low power' means that a device needs to run for 10 years on the equivalent of 2 'AA' batteries. The company's sensor products focus on environmental monitoring for agriculture or security monitoring for unoccupied buildings. To get such long life, the connected sensor devices might need to draw as little as 600 nA in standby mode.

To develop these products, AltoNovus engineers needed to characterize their devices' power consumption in all modes of operation. That includes measuring how much charge — current × time (mAh) — is consumed during a radio transmission.

Being a startup company (established in 2015), AltoNovus needed a low-cost ammeter that could make the needed measurements. "DMMs capable of measuring down to 1 nA typically retail from about £1k," director Geoff Dean told EE Times. You can find numerous bench DMMs that can measure 1 nA, but yes, they will cost about £1,000 and up. Plus, they're bench instruments.

Figuring they could do better, AltoNovus engineers developed their own ammeter. "To measure down to these very low levels," said Dean, "we designed and built our own low-current meter, NanoRanger, initially as an internal development and diagnostic tool. We then thought that NanoRanger would be of interest to other professionals, enthusiasts, and makers."

To fund the development and production of the NanoRanger, AltoNovus has launched a Kickstarter campaign through which the company hopes to raise $33,000. Initial backs will be able to buy a NanoRanger for £99 instead of the list price of £149, according to Dean.

Part 2 of year in review will be in the next issue of Silicon Semiconductor magazine.

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