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ALD has emerged as an important aspect of advanced semiconductor manufacturing

LITHOGRAPHY CAN BOOST FOPLP YIELD
Fan-out panel level packaging (FOPLP) has many advantages to impact yields and costs

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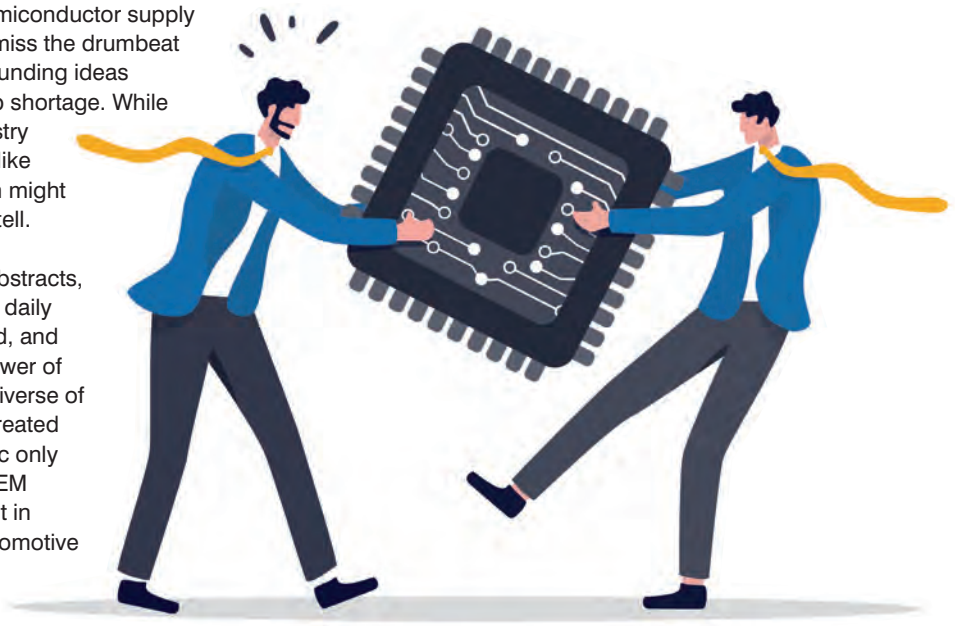
VIEWPOINT

By Mark Andrews Technical Editor

End the chip shortage? It just takes time

AS PART of the semiconductor supply chain you cannot miss the drumbeat of oh-so-simple sounding ideas for ending the current chip shortage. While demand has put our industry in the spotlight, it is more like being on a hot seat. When might 'normal' return? Time will tell.



Economists often talk in abstracts, but manufacturers live the daily realities of supply, demand, and market expansion. The power of adding electronics to a universe of consumer products has created demand that the pandemic only fueled. Simultaneously, OEM demand for older ICs (built in 200mm fabs including automotive chips,) also came at a time when those fabs fell from 202 in 2006 to around 180 by 2015. Even though manufacturers have reopened some older fabs and new 200mm plants are under construction in China, demand still outpaces capacity.

The shortage has at least focused attention on a critical part of the global economy—the supply chain—and ways to build resiliency. There are efforts to build more chips within the US, yet Intel still needs a year-plus to open its newest Southwest fab while a second is just getting off the ground. TSMC's US project has yet to begin. The EU has its European Chips Act, but this won't bring needed capacity online for years. It is noteworthy that Intel CEO Pat Gelsinger predicts the shortage will ease in 12 to 18 months while AMD's CEO, Lisa Su, predicted an end by late 2022.

In this edition of Silicon Semiconductor we take a look at a new Adaptsys solution to speed backend production. Adaptsys' new Reflex II tape-forming system gives manufacturers the ability to place their devices into industry standard, pocketed tape with an economical, in-house system already in use by global customers. We also examine an innovative ALD-based solution for meeting tightening RF filter performance requirements by Veeco and guidance from Swagelok for choosing ALD valves that cost-effectively address HVM performance needs. Onto Innovation shares the success story of its new feedforward metrology and advanced outlier control system that identifies problem chips to significantly increase yield and throughput for display panel manufacturers.

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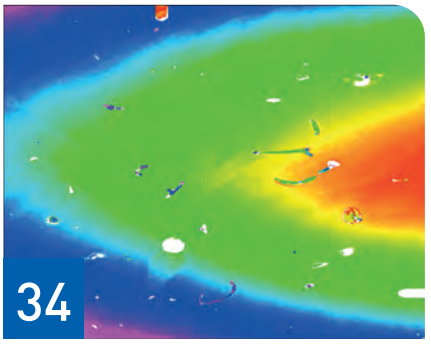

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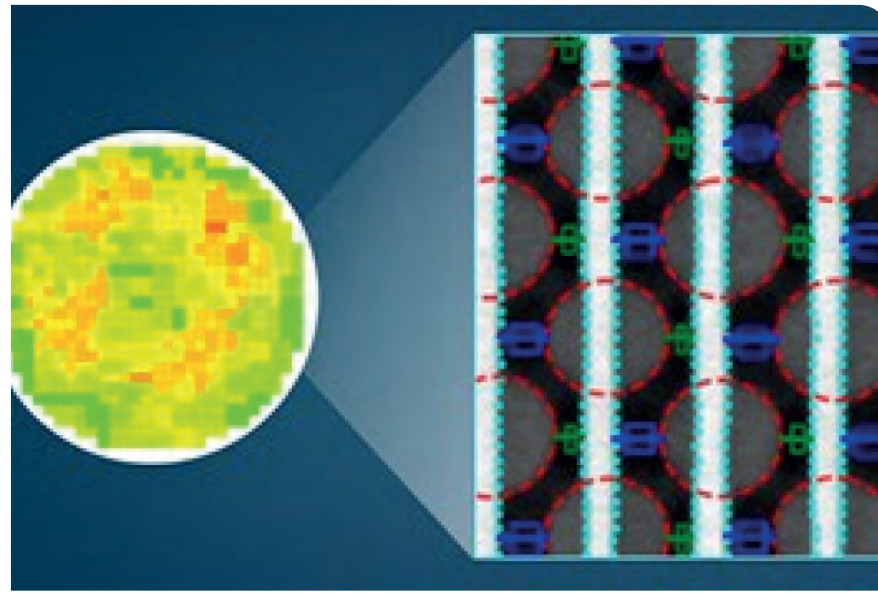
Applied Materials Unveils eBeam Metrology System

APPLIED MATERIALS has unveiled a unique eBeam metrology system that enables a new playbook for patterning control based on massive on-device, across-wafer and through-layer measurements.



Advanced chips are built one layer at a time, and each of billions of individual features must be perfectly patterned and aligned to create working transistors and interconnects with optimal electrical characteristics. As the industry increasingly moves from simple 2D designs to more aggressive multipatterning and 3D designs, a commensurate breakthrough in metrology is needed to perfect each critical layer and enable the best performance, power, area-cost and time to market (PPACt).

Traditionally, patterning control has been achieved using optical overlay tools that help align die patterns with "proxy targets" which are guide marks printed into the spaces between die that are removed from the wafer during die singulation. Proxy target approximation has been complemented with statistical sampling of a small number of die patterns from across the wafer.

However, after successive generations of feature shrinking, broader adoption of multipatterning, and the introduction of 3D designs that cause interlayer distortions, the traditional approach is leading to measurement deficiencies – or "blind spots" – that are making it more difficult for engineers to correlate intended patterns with on-die results.

With the arrival of new eBeam system technology that can directly measure semiconductor device structures across the wafer and through layers at high speed, customers are moving to a new patterning control playbook based on big data.

Applied's latest eBeam metrology innovation – the PROVision 3E system – is especially designed for this new playbook. "As the leader in eBeam technology, Applied Materials is giving our customers a new playbook for patterning control that is optimized for the most advanced logic and memory chips," said Keith Wells, Group Vice President and General Manager, Imaging and Process Control at Applied Materials. "The resolution and speed of the PROVision 3E system allows it to see beyond the blind spots of optical metrology, performing accurate measurements across the wafer and between the many layers of a chip. This provides chipmakers with the multidimensional data sets they need to improve PPAC and accelerate the time to market of new process technologies and chips."

Jenoptik intends to acquire Berliner Glas Medical and SwissOptic

JENOPTIK AG is set to acquire from Berliner Glas GmbH, a 100 percent subsidiary of ASML Holding N.V.

Overall, Berliner Glas Medical and SwissOptic currently employ around 500 people worldwide. The transaction is still subject to approval from the German antitrust authorities. Closing is expected in December 2021. "With this strategic acquisition we will strengthen our global and fast-growing photonics business thus significantly expanding our already strong semiconductor equipment business, and, in particular, our highly attractive medical technology business," says Stefan Traeger, President & CEO of Jenoptik AG.

"We are pleased to have reached this agreement whereby Jenoptik will acquire the Medical Applications and SwissOptic business of Berliner Glas (part of ASML)," says Andreas Nitze, CEO of the Berliner Glas Group. "We are convinced that the combined businesses are well positioned to realize the potential we see for the business and will offer the best environment for its employees."

EV GROUP brings high-speed high-precision metrology to 3D heterogeneous integration

EV GROUP (EVG), a supplier of wafer bonding and lithography equipment for the MEMS, nanotechnology and semiconductor markets, has unveiled the EVG®40 NT2 automated metrology system, which provides overlay and critical dimension (CD) measurements for wafer-to-wafer (W2W), die-to-wafer (D2W) and die-to-die (D2D) bonding as well as maskless lithography applications. Designed for high-volume production with feedback loops for real-time process correction and optimization, the EVG40 NT2 helps device manufacturers, foundries and packaging houses accelerate the introduction of new 3D/heterogeneous integration products as well as improve yields and avoid scrapping of highly valuable wafers.

EVG will showcase the EVG40 NT2 system for the first time at the SEMICON Europa tradeshow, taking place November 16-19 at the Messe München in Munich, Germany.

As traditional 2D silicon scaling reaches its cost limits, the semiconductor industry is turning to heterogeneous integration – the manufacturing, assembly and packaging of multiple different components or dies with different feature sizes and materials onto a single device or package – in order to increase performance on new device generations. In W2W, D2W and D2D bonding, tight alignment and overlay accuracy is required to achieve good electrical contact between the interconnected devices.

As interconnect pitches become tighter with each new product generation, wafer and die bond alignment and overlay processes must also scale accordingly, with greater accuracy and more frequent measurements to identify process problems when they occur in order to provide corrective action or the possibility for rework, leading to higher production yields. Maskless exposure, an innovative lithographic approach for 3D/heterogeneous integration, requires increasingly precise pattern fidelity and pattern overlay on highly warped and distorted wafers that often incorporate shifted dies—driving the need for metrology that delivers crucial information on die position.

"Process control is increasingly critical for leading-edge 3D and heterogeneous integration applications," stated Dr. Thomas Glinsner, corporate technology director at EV Group. "The EVG40 NT2 represents a major breakthrough in metrology performance to meet the new demands for the advanced packaging industry. It provides not only greater overlay accuracy but also a significant boost in throughput to enable higher measurement density per wafer, giving more detailed feedback on hybrid bonding performance, for example. This new metrology solution rounds out EVG's comprehensive portfolio of process solutions for 3D/heterogeneous integration, and complements our existing EVG40 NT system, which remains the de facto bond metrology standard for MEMS and complex photonic devices. The EVG40 NT2 is already playing a key role in several joint development projects underway at EVG's Heterogeneous Integration Competence Center™."

The EVG40 NT2 system provides highly precise measurements of critical bonding and lithography process parameters for current and future leading-edge 3D/heterogeneous integration applications. These measurements include: alignment verification and monitoring for W2W, D2W, D2D and maskless exposure processes; CD measurement; and multi-layer thickness measurement. It is a highly scalable system that features multiple measurement heads and a high-precision stage designed for high-throughput and high-accuracy (down to the low single-digit nm range) bonding and maskless exposure alignment verification. For alignment verification, the EVG40 NT2 generates an overlay model that can be used in a feedback loop for improving overall alignment. This reduces systematic errors and results in increased production yields. The system is compatible with multiple line optimization concepts for overlay feedback and die position feed-forward required by next-generation fabs supporting Industry 4.0 manufacturing.

EVG is now accepting orders for the new EVG40 NT2 automated metrology system and offering product demonstrations at EVG's Heterogeneous Integration Competence Center at its headquarters in Austria. For more information, please visit **https://www.evgroup.com/products/metrology**

Park Systems combines AFM with white light interferometry

PARK SYSTEMS, a manufacturer of Atomic Force Microscopes, has announced the Park NX-Hybrid WLI, the first fully integrated system that combines Atomic Force Microscopy (AFM) with White Light Interferometer (WLI) profilometry. White light interferometry (WLI) is a nondestructive, non-contact, optical measurement technique used to generate 2D and 3D models of surfaces, and is now widely used for semiconductor production quality assurance. Park Systems introduces the Park NX-Hybrid WLI as a powerful semiconductor metrology tool that incorporates the best of AFM and WLI technologies into one seamless system.

Park NX-Hybrid WLI, the first fully integrated system that combines Atomic Force Microscopy (AFM) with White Light Interferometer (WLI) profilometry, a powerful semiconductor metrology tool that incorporates the best of AFM and WLI technologies into one seamless system. Park NX-Hybrid WLI, the first fully integrated system that combines Atomic Force Microscopy (AFM) with White Light Interferometer (WLI) profilometry, a powerful semiconductor metrology tool that incorporates the best of AFM and WLI technologies into one seamless system. The Park AFM in the integrated system is based on the Park NX-Wafer, the industry leading automated atomic force microscopy system for semiconductor and related devices manufacturing, in-line quality assurance, and research and development.

The combined AFM/WLI system provides high throughput imaging over a very large area with the WLI module, and nanoscale metrology with sub-angstrom height resolution over the areas of interest using AFM. Defects of a patterned structure can be detected by comparing images of reference and target sample areas using high speed "hot spot detection", a technique that enables fast localization of defect sites for high resolution AFM review.

The Park WLI module supports both White Light Interferometry and Phase Shifting Interferometry (PSI) modes. The PSI mode is enabled by a motorized filter changer that allows the two objective lenses to be replaced automatically. The Park NX-Hybrid supports objective lens magnification of 2.5x, 10x, 20x, 50x and 100x, featuring a CMOS camera. Fusing the two complementary techniques, Park NX-Hybrid WLI is a comprehensive automated metrology system, providing substantial cost savings over two separate systems.

"Unlike legacy standalone WLI and AFM systems, Park NX-Hybrid WLI accomplishes more, in a seamless manner, at drastically lower cost of ownership, creating a completely holistic integrated tool," comments Byoung-Woon Ahn, VP of Nanotechnology R&D, Park Systems.

"With both tools on the same mount and fed by one EFEM, the system creates fully integrated and exchangeable data, reducing the "fab footprint" and increasing throughput over a larger area."

Park NX-Hybrid WLI was developed for use in applications requiring much higher resolution and accuracy beyond the capability of WLI alone, such as advanced chemical mechanical polishing (CMP) metrology and monitoring, dishing, erosion, and edge-over-erosion (EOE), film thickness, pillar height, hole structure and die to die comparison. It will also be useful in advanced packaging applications including through-silicon via (TSV) and micro bump measurement redistributed layer (RDL) measurement and photo resist residue detection.

The new Park NX-Hybrid is part of a series of hybrid metrology products Park Systems plans to offer this year to enhance and improve the utilization of atomic force microscopy across a wide range of industrial and academic research applications.

BASF and Entegris sign agreement on sale

BASF and Entegris have signed an agreement on the sale of the Precision Microchemicals business to Entegris for $90 million. The transaction includes technologies, intellectual property and trademarks and is expected to be completed by the end of 2021.

The Precision Microchemicals business is part of the Surface Treatment business unit of BASF's Coatings division, operating under the Chemetall brand. It develops, manufactures, and markets high purity materials, including cleaning chemistries and Chemical Mechanical Planarization (CMP) slurries used in the machining and surface conditioning of electronic materials. The products are primarily used for cleaning and polishing of hard disk drives (HDD) and wide band gap semiconductor (WBGS) ultra-hard surface materials, including silicon carbide (SiC) used in power electronics and advanced communications. This business will be part of the Specialty Chemicals and Engineered Materials (SCEM) Division of Entegris.

"Under the ownership of Entegris – a leading global player in specialty chemicals and advanced materials solutions for the microelectronics industry – the Precision Microchemicals business will be well positioned to realize its full potential," said Christophe Cazabeau, Senior Vice President, Surface Treatment, BASF.

"The acquisition of BASF's Precision Microchemicals business adds technical expertise, intellectual property and talent to our broad specialty chemicals portfolio," said Bertrand Loy, President and CEO of Entegris. "In particular, it will build on our leadership in the CMP slurry market for ultra-hard surface materials, serving some of the fastest growing end-markets globally, including electric vehicles and 5G communications."

The all-round smart proximity sensor chip

STARRYCOM SENSING TECHNOLOGIES, a US technology startup, has announced the release of its SPX-1 smart proximity sensor IC product. The IC is now available for sampling.

For decades, proximity sensor design engineers have done everything possible to achieve higher sensing distance, reduction factor one, magnetic field immunity, selective sensing, etc. etc. over even wider temperature range, through many very different technology platforms.

Now a single smart proximity sensor chip can do it all until the SPX-1, the industry's first and currently only all-round smart proximity sensor chip.

SPX-1 is a mixed signal VLSI system on chip based on Starrycom's patented technology platform. Its dual tank oscillator analog front end design guarantees differential detection, higher sensitivity, temperature tracking, and better noise immunity. The embedded microcontroller and nonvolatile memory bring the proximity sensor intelligence and flexibility for configuration and programming.

Proximity sensors built with SPX-1 smart chip can achieve unparalleled temperature stability through the IC's unique autonomous machine learning algorithm. SPX-1 IC consumes less than 2mA current and can be configured for both three wire and two wire proximity sensors and in both cases the sensors are plug programmable- meaning no additional wires or pins are needed for programming and calibration and programming/calibration can be done after sensor is fully assembled and encapsulated.

To facilitate design and development of SPX-1 based proximity sensor products, Starrycom engineers have developed a whole line of supporting devices, software tools and systems for sensor's programming, calibration and automatic testing. This makes SPX-1 IC users' job much easier, from proximity sensor design all the way to manufacturing process.

SPX-1 can also be used for high-end capacitive proximity sensor design. The IC's dual tank oscillator design can greatly improve capacitive proximity sensor's noise immunity, one of the major problems in capacitive proximity sensor development. The IC's buffered sensing tank signal output provides an ideal guide for sensor's shielding design.

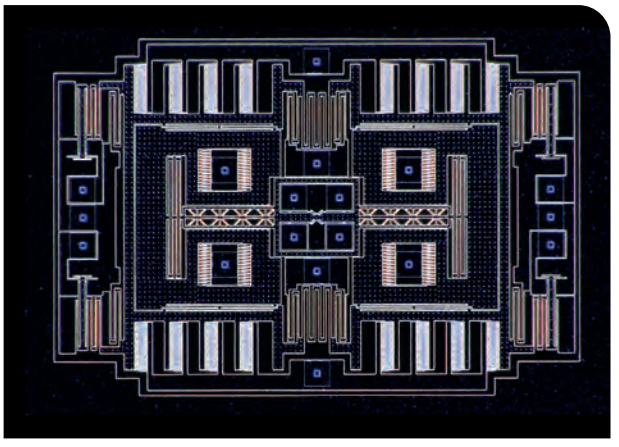
SPX-1 IC samples in QFN24 package are now available to customers. We also offer evaluation boards and programming/calibration modules with an intuitive, easy-to-use graphic user interface (GUI) running on a PC. Mass production will launch at the end of the third quarter of 2022.

CEA-Leti unveils navigation-grade gyroscopes

CEA-LETI scientists, in collaboration with researchers at Politecnico di Milano have developed the world's smallest-footprint MEMS gyroscope that can provide navigation-grade performance. The researchers were able to meet these specifications with a sensor footprint of only 1.3 mm2 by leveraging nano-resistive sensing.

Low-power MEMS gyroscopes are now ubiquitous in everyday objects. They monitor and control device position, orientation, direction, angular motion and rotation. With the growing development of driver-assist systems and other automated functions, the need for improved performance and robustness has increased significantly, fueled by the demand for miniaturization and cost control for real inertial navigation systems.

To address new demands for high-performance inertial measurement units (IMU), these gyroscopes must reach the navigation grade, which means improved characteristics of one or two orders of magnitude compared to the best commercial MEMS gyroscopes. Thus, they require a bias instability well below 0.1°/h and an angular random walk (ARW) of less than 0.01°/√h. CEA-Leti, in collaboration with Politecnico di Milano, reached these targets by demonstrating performance matching the best state of the art on ultra-miniaturized MEMS gyroscopes. The results were reported in a paper, "1.3 mm2 Nav-Grade NEMS-Based Gyroscope", in the Journal of Microelectromechanical Systems.



"This improved performance must not come with a high cost so the device will be priced competitively in large-volume markets, such as the automotive and consumer markets," said Philippe Robert, MEMS business development manager and senior expert at CEA-Leti. "The size of these new gyroscopes must therefore not exceed 2 mm² per axis, while maintaining standard MEMS technology and using wafer-level vacuum packaging."

Combining CEA-Leti's expertise in highly sensitive sensors based on silicon nano-gauges and Politecnico di Milano's expertise in gyroscope design, this new gyroscope solution reaches "0.004 °/ √hr ARW and 0.02 °/hr stability on average over several tested samples, unrivalled results for a 1.3 mm²-size gyroscope footprint", the paper reported.

The ARW and bias instability performance were highlighted on non-static operations: "After 9-minute long in-operation navigation where the gyro is repeatedly tilted by 180° constant angle rotations and by AC random motion with about 200-dps peak-to-peak value, the residual angle error at the end of navigation corresponds to only 0.07°." This result was achieved without Kalman filter compensation.

To keep manufacturing costs low, the team focused on both the sensor's size and the robustness of the fabrication process, especially on vacuum-WLP. The CEA-Leti and Politecnico di Milano NEMS-based gyroscope is fully compatible with standard MEMS foundries for high-volume markets such as the automotive industry. They also are working on 3-axis gyroscope co-integration, whose feasibility has already been demonstrated, but where the objective will be to bring the same level of performance according to the three axes.

In addition, to address a wide range of applications (short-term navigation in a GPS outage, indoor navigation, platform stabilization, accurate robotic motion control for Industry 4.0, guided munitions, etc.), the team ensured a resonant frequency greater than 25 kHz to withstand conventional vibration environments.

YES partners with Osiris for edge film removal technology

YES (Yield Engineering Systems), a manufacturer of process equipment for semiconductor advanced packaging, life sciences and "More-than-Moore" applications, has announced that it has signed an exclusive agreement with Osiris (Osiris International GmbH) to license its smartEBR technology for edge bead removal on panels. This proprietary process, based on wet etch chemistry, will enable YES to expand its wet processing capabilities.

"We are very pleased to partner with YES in this effort to extend our smartEBR technology to more complex applications," said Pirmin Muffler, Managing Director of Osiris. "We selected YES as our partner because of their proven ability to rapidly bring innovation to high-volume manufacturing production environments. YES is committed to developing a variety of solutions for panel-based applications in the PCB and advanced packaging markets" said Zia Karim, CTO of YES. "When combined with our extensive process expertise, the smartEBR technology will allow our customers to remove metal, photoresist and dielectric coatings efficiently from a variety of panel types, ensuring high yield and defect control."

"Our mission is to be the preferred provider of surface modification and material enhancement solutions in the markets that we serve," said Rezwan Lateef, President of YES. "The Osiris EBR technology adds an important element to our product portfolio, as we continue to support and enable the ambitious roadmaps of our key semiconductor customers."

SUSS MicroTec and SET to develop equipment solution for 3D chip integration

SUSS MICROTEC and SET have announced a partnership in sequential die-to-wafer (D2W) hybrid bonding, a die-based interconnect technology, to provide a fully automated, customizable, highest-yield equipment to customers. This solution will accelerate the industry's path towards advanced 3D multi-die solutions such as stacked memory and chiplet integration.

Saint-Jeoire, France and Garching, Germany - September 1st, 2021 - SUSS MicroTec -leading supplier of equipment and process solutions for the semiconductor industry- and SET -leading supplier of high precision flip-chip bonders- signed a joint development agreement to develop a cluster, including several modules such as surface preparation, cleaning, bonding and metrology. As part of this partnership, SUSS MicroTec's high-efficiency surface preparation modules and throughput-optimized metrology solutions for post bond overlay verification will be combined with SET's latest ultra-high accuracy D2W hybrid bonding platform.

As today's 2.5D and 3D packaging schemes are limited by the minimum interconnect density that traditional microbump technology can offer, hybrid bonding solves this problem by bonding the direct contact between two metal pads (mostly copper) and surrounding dielectrics in one single bonding step.

This bumpless bonding approach allows for substantially smaller pitches and higher interconnect density which are the key enablers for future generations of multi-die solutions.

Make, Don't Buy, for Freedom and Flexibility

Taping components for delivery to customers? Owning the entire process, from pocket forming to taping, can drive out supply-chain risks, reduce costs, and shorten turnaround time

BY JAMES CAWKELL, TECHNICAL DIRECTOR, ADAPTSYS

TAPE-AND-REEL is the expected delivery packaging for a wide variety of components, to provide protection during transit and present parts efficiently to automated placement machines.

Component manufacturers and many distributors operate taping capabilities in house. The pocketed tape, however, is often purchased pre-formed from external suppliers. Various tape widths, pocket sizes, and designs are needed to provide suitable protection for the wide variety of ICs, discrete, and passive components currently being used throughout the industry.

Tape Supply Risks

Orders cannot be fulfilled if suitable tape is not available. Component suppliers are therefore challenged to ensure that the right types of tape

are always in stock. As an alternative, producing the required pocketed tape in-house, as and when needed, could help overcome this challenge. Owning the pocket-forming process lets component suppliers buy raw, unformed tape and create the packaging they need on demand. It prevents running out of the right type of tape while also simplifying inventory, reducing expenditure, and saving storage space.

Adaptsys introduced the industry-changing Re-flex II tape-forming system as a cost-effective and usable solution to this challenge. Unique because it produces carrier tape "on demand", Re-flex II was originally created to fulfil Adaptsys' own need for pocketed tape. The resulting system proved so easy to use and versatile that the concept was readily commercialised. Adaptsys is now supporting multiple systems in operation with customers worldwide.

Some businesses may view making their own tape as a "non-core" activity that demands time, resources, and floor space that is better devoted to other materials and processes. But they are as vulnerable as any of their competitors if an important order needs to be fulfilled immediately and there simply is not enough tape on the premises. Waiting for tape to be delivered could translate into a lost opportunity. Re-flex II can provide emergency taping capability that requires no particular expertise and hence can be used on an ad hoc basis.

In this way, Re-flex II can be used in a backup role to mitigate tape-supply risks and provide the flexibility to turn unexpected orders around quickly. However, the system is equally suited to intensive use, fulfilling a company's entire tape requirements.

Speed and Efficiency

With the latest upgrades, Re-flex II can form pockets at a tape-throughput rate up to four metres per minute. This is faster than typical component-taping equipment, so users have the option to feed freshly pocketed tape directly into their component-packaging process for optimum efficiency. It saves the overheads associated with storing and retrieving lengths of pocketed tape. Storing a supply of flat tape on standard sized reels can save up to 95% of the space usually needed to keep various types of pre-formed tape.

Feeding the tape straight into component-packaging equipment also reduces the stoppage time taken to change reels during component taping. The Re-flex II supply reel can contain up to 1000 metres of flat tape. If the taping process operates at 2 metres per minute, this allows up to eight hours of continuous operation before the input reel needs to be changed.

A similar reel of pre-formed pocketed tape can contain only about 40 metres, assuming a pocket depth of 6mm. Hence the reel needs to be changed every 20 minutes. In this way, Re-flex II significantly reduces operator intervention, raising productivity and enabling faster fulfilment of customer orders.

Return on Investment

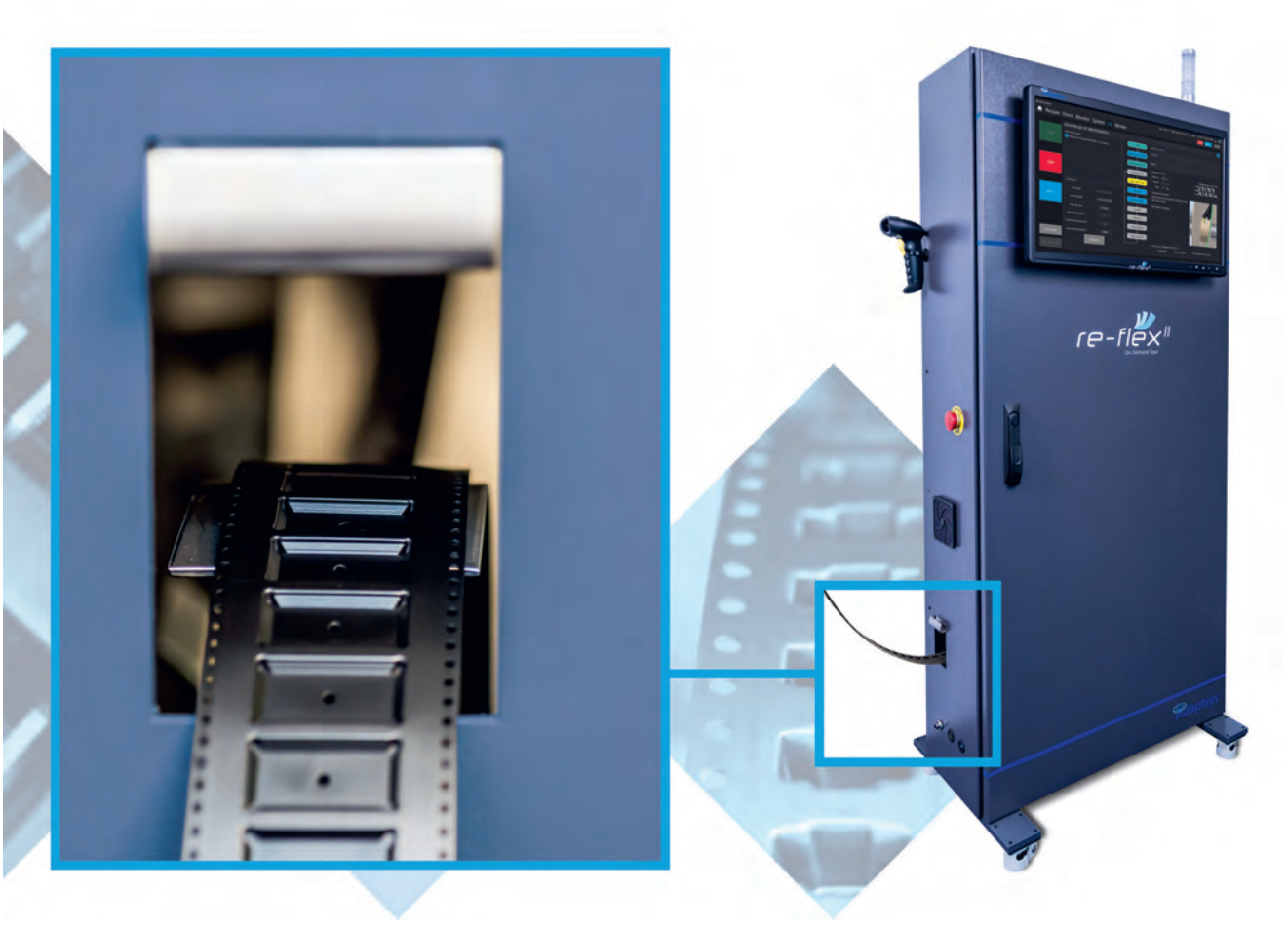
The up-front investment needed to start making tape in house can be surprisingly low. Companies can recoup their investment in Re-flex II within 12 months, depending on usage. Its compact footprint, measuring just 75cm x 35cm occupies minimal real-estate in a factory or packing area and the system requires only a standard AC supply and compressed air.

The system can handle tapes up to 88mm wide and gives users the flexibility to create pockets in standardised or custom dimensions simply by changing the tooling. Quality inspection and traceability are provided for each formed pocket. The pockets may be simple shapes, such as a square, rectangular, or rounded recess, or may be specifically shaped to fit a particular component or provide certain functions such as protecting vulnerable pins or protrusions. Adaptsys can help customers create custom tooling where required and has successfully developed solutions for various special components such as small electronic modules and electrical connectors.

Re-flex II can produce intricate pocket designs suitable for protecting large semiconductor components, which are often supplied in other types of packaging such as trays, as well as smaller ICs, discretes, and passives that are typically supplied on tape and reel. It is also suited to creating pocketed tape for small engineering components such as stamped metal shields or miniature springs.

Changing the tooling to a different tape design in a production setting requires no special skills and takes just a few minutes, enabling users to produce pocket designs in almost any quantity from low and medium volumes to high volume.

Re-flex II can be used with any standard-size input and output reels up to 22" (560mm) in diameter, taking unformed tape from the input reel and delivering formed tape to the output reel.



Efficiency-Boosting Option

Now, Adaptsys has introduced a new option that enables tape/reel storage and transport to become even more space efficient without compromising reliability and ease of use. While Re-flex II is intended primarily for feeding pocketed tape directly into a component taper, the new Crosswinder option now enhances owners' flexibility to produce tape onto reels to be stored for later use.

Similar to the development of the Re-flex II system itself, Adaptsys created the Crosswinder initially to meet an internal requirement for an ultra-efficient way to produce and store pocketed tape in extended lengths. It is now available commercially, ready to further boost the return on customers' investment in Re-flex II. The Crosswinder neatly winds tape of a standard width, say 12mm, across a 100mm-wide reel to increase the storage capacity by a factor of 8 compared to an ordinary 12mm reel. Also, a crosswound reel can supply significantly more parts to a high-speed component taper before needing to be replaced, thereby reducing changeovers. Crosswinder ensures the tape is neatly ordered to unwind smoothly, which helps avoid problems that may otherwise require the taper to stop. Crosswound reels are available in various widths to provide high maximum capacity.

Re-flex II can produce intricate pocket designs suitable for protecting large semiconductor components, which are often supplied in other types of packaging such as trays, as well as smaller ICs, discretes, and passives that are typically supplied on tape and reel

Conclusion

Pocketed tape is an established medium for transporting electronic components and feeding automated high-speed assembly equipment. Many component suppliers have in-house parts-taping capabilities yet lack a suitable solution for producing the required pockets. However, the ability to form pockets in flat tape, on demand, can greatly increase flexibility and provide protection against supply-chain risks.

The Re-flex II pocket-forming equipment combines high throughput with ease of use and permits both standard and custom pocket designs. Changing the setup and tooling to create pockets of any required design takes only minutes and requires minimal training. Every component manufacturer should have one.

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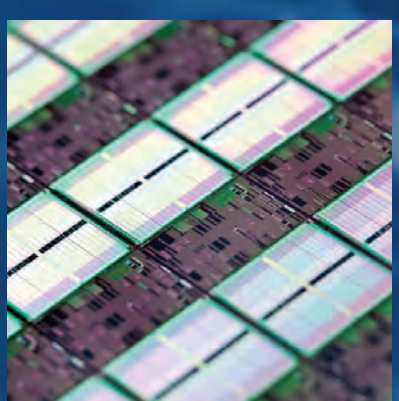
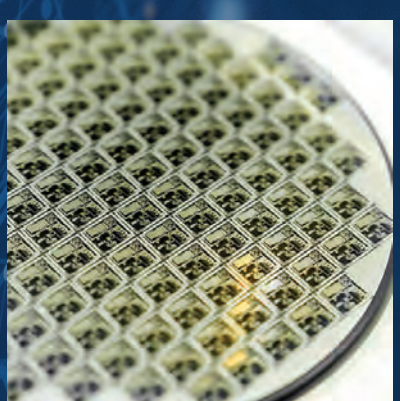


Advanced Lithography

Smart Devices and PE Foundry



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Manufacturers can reap dividends by properly managing IP reuse

This article is the second in a two-part series examining the challenges and benefits of IP reutilization within semiconductor manufacturing. Perforce is expert in navigating the complicated issues surrounding IP protection and ways to safely reuse IP in manufacturing. The article series is provided as a guide to the role and significance of IP across industrial sectors and is not intended to replace counsel.

BY SIMON BUTLER, GENERAL MANAGER, METHODICS BY PERFORCE

AS CHIPS become more complex, the demand for reusable and pre-verified IP blocks of Intellectual Property (IP) has grown. However, while it has some powerful benefits, IP reuse in practice has multiple challenges that need to be clearly understood and strategically addressed, which many organisations continue to find hard. Apart from inefficiencies around IP management (which can undermine the potential benefits of reuse), IP leakage continues to be a huge problem, meaning that companies' valuable assets are being used without their permission.

So that begs the question, if IP reuse is so tricky, is it worth the effort? Arguably, without IP reuse, the industry cannot keep up with demand. We all know the drill: time-to-market timescales are shrinking, whether across automotive, the IoT, or consumer goods. So new design is not an option. These days most designs must start at 60-80 per cent reuse design to keep on schedule. Taking a previous design as a starting point does not work because enhancements and new features need to be added. Therefore, a design must use a collection of lower-

level modules, or IP, to accommodate improvements, customisation, and new ideas.

The lower-level IP that frequently serves as a foundation for new work can come from several sources, such as previous designs developed internally; the creation of new IP, but the content is 'packaged' in such a way that it can be repurposed into multiple designs, and finally third party IP, whether from partners or commercial IP providers. Indeed, IP reuse is also a business opportunity in itself, creating a new revenue stream for many organisations. This more open, collaborative approach helps the industry to increase development velocity and support innovation collectively.

Not So Easy

The business case for IP reuse is clear, but in practice, IP reuse has multiple challenges. First, designers may be resistant to change and concerned that IP reuse means more work. IP can also be hard to discover, particularly in an ecosystem where there are potentially thousands of pieces of IP to consider. Not finding these assets quickly or easily can make it tempting to start from scratch rather than trying to repurpose existing IP that at least at first appears somewhat hidden from plain sight. Different teams will have different workspaces and preferred tools, which exacerbates the visibility and accessibility of IP further, especially if they are remotely dispersed. Plus, while everyone needs to collaborate in an efficient, virtual way, the security of IP is paramount. Just like the end product, IP has a tangible market value.

In an ideal world, development processes must make it easy for the designer to make IP available, for changes and modifications to be easy, and for any additional workload overhead to be minimal. When sharing with others, IP should be easy to find, ideally with a centralised catalogue of all IP that is constantly maintained and covering all the relevant metadata within the IP, what we refer to as the six Ws: Who, What, Where, When, Why, and hoW. That catalogue needs to gather data from different contributors around the world and span different workflows.

Staying with that point, workspace management must be rationalised to support efficient IP reuse so that users can stay within their environments and provide a unified view that supports collaboration. However, there is a caveat: data must be kept secure, with not everyone seeing everything. For instance, contract workers and consultants may only have access to certain parts of the design. Clearly, organisational security policies and protocols must always be enforced; these may vary by industry, such as ITAR restrictions for military applications.

Best Practice Steps

Fortunately, many steps can be taken towards achieving more secure, better-managed IP reuse. These steps are not just theory but are already being implemented successfully by various organisations around the globe. First, do not delay: it is never too early to adopt IP management practices that support reuse because, as we all know, the next design requirement is just around the corner. Second, proper IP reuse techniques will lead to better design results for the long term, with an increased level of testing across different usage scenarios contributing to a reduction in errors. Third, think globally; IP management is only as strong as its weakest points. Best practices need to be universally and uniformly embraced across all teams; otherwise, groups not on board could break an entire design. This is not just a wild claim: companies that have allowed teams to work outside the system have had catastrophic failures as a result. Block any back doors.

As a baseline, create an environment that allows designers to work the way they want to but have the IP system take care of all aspects of IP lifecycle management, supporting different methodologies, design tools, and infrastructure. Implementing a platform to manage and track a company's internal and external IP assets is a somewhat new concept and the majority of the metadata needed to qualify an IP's quality, context, state, and other factors is typically scattered across the various implementation and verification tools used in the design. The challenge is to extract this metadata and associate it with a versioned set of dependent IPs for project milestone releases.

An integrated product lifecycle (IPLM) system, of which there are now a variety available (and some are also focused on the specific requirements of semiconductor IP), should handle these hierarchical IP/ metadata requirements and the accompanying release flow required to deliver these versions. Ideally, it would also enable the deployment of the required project IP versions (IPVs) to user workspaces and guide the user to update these workspaces as the project Bill of Materials (BoM) evolves. This allows the support team to take a more proactive approach to keeping users on track with the correct IP versions, best practices around IP reuse, and discovery of new candidates for IP reuse.

Security must become an integrated part of the IP management process, with the PLM system enforcing policies such as:

- Geofencing to control access to key assets according a user's physical location.
- Partial workspaces to enable a single project hierarchy control of what IPs are available to individual users.
- Security assurance to track an IP's development and ensure its provenance hasn't been compromised during its lifecycle.

While these steps require quite some effort, they will pay dividends both now and in the future. As the semiconductor industry continues to evolve – with the complexity of hardware and software assets exploding and teams operating remotely even more frequently then they have in the past – more efficient management, protection, and reuse of IP have to be a priority.

ALD can help solve 5G RF filter challenges

The global push to roll out 5G mobile services is creating vast opportunities, but these bright prospects have not reduced the technical challenges facing manufacturers of critical componsents such as RF filters. Veeco explains how its ALD technology is making a difference for wireless device manufacturers.

BY GANESH SUNDARAM, PH.D., VICE PRESIDENT, RESEARCH & ENGINEERING, VEECO

WITH THE ADVENT OF 5G, RF filters are expected to do more for much less. On the one hand, they face the challenge of receiving and transmitting ever-larger amounts of data at increasingly faster speeds.

In the sub-6GHz range, this is further complicated by the allocation of relatively narrow slices of the frequency spectrum for mobile communications, often sandwiched between frequency bands allocated for a variety of applications, some of them critical. That puts drift, performance and power in the critical path. On the other hand, in terms of cost, RF filters are becoming commoditized.

Atomic layer deposition (ALD) can help

ALD produces ultrathin conformal films with atomic-level control. In terms of deposition methods, this technique is unmatched for combining film conformality, low temperature processing, stoichiometric control and inherent film quality. While ALD has existed for over half a century, its low deposition rate made it less attractive for applications that required high throughput processing.

After a decade of advancements, ALD is now a fast and cost-effective technology suitable for a wide range of applications. Deployment got a big boost with high-K and in advanced DRAMs. Many technologists and researchers are replacing older deposition techniques such as evaporation, sputtering and chemical vapor deposition (CVD) with ALD to take advantage of its unique ability to produce conformal coating in and around 3D objects in a highly consistent manner. For RF filters, the ultrathin layers of dielectrics grown by ALD can cost-effectively address stability, reliability and power durability.

Why ALD for RF Now?

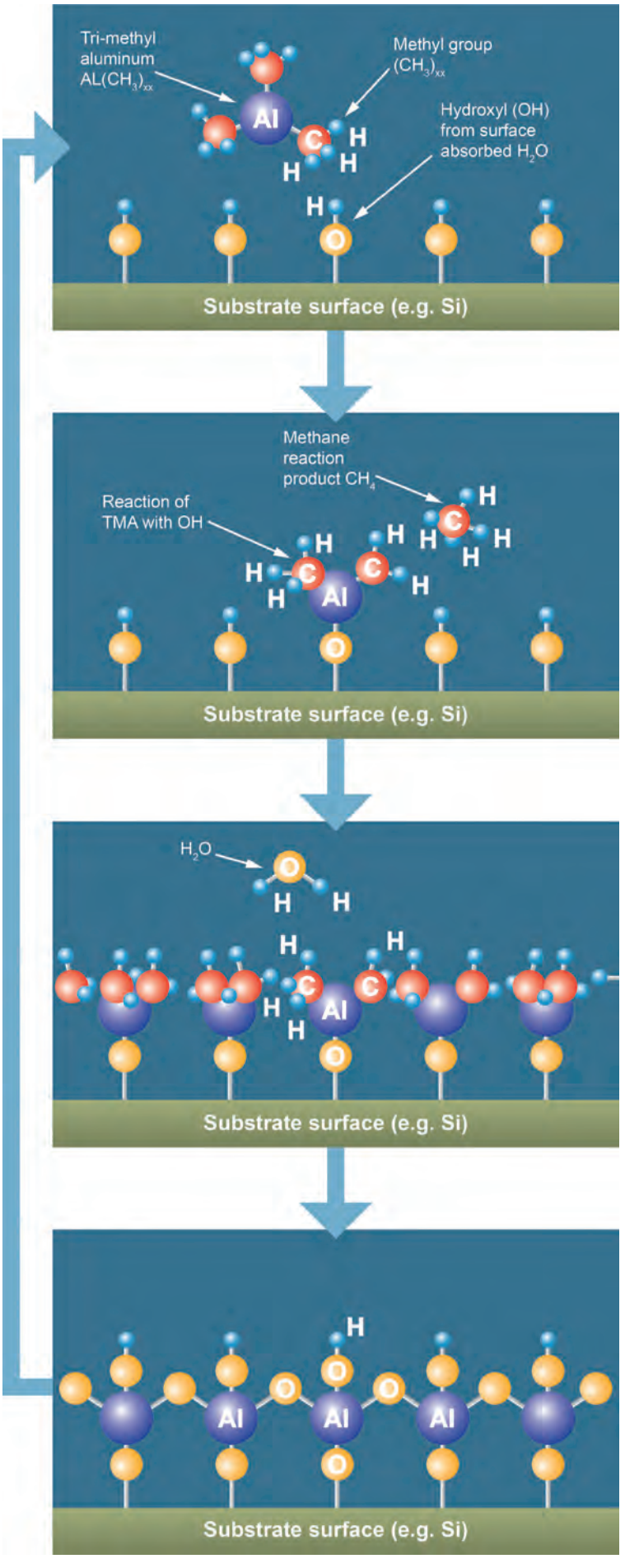
RF filter functionality within the handset can be varied, but in general, it allows signals of a certain frequency to pass through, whether they are receiving (downlink) frequencies – Rx, or transmission (uplink) frequencies – Tx. The key filter performance parameters are:

- Low loss of the desired signals in the passband of frequencies; and
- Sufficient attenuation of undesired interference in the stopband of frequencies.

Every antenna and new frequency requires a new filter. With 5G, the number of filters in a smartphone will double, reaching well over 100 per phone. The requisite RF filter parameters must be met over environmental and production variations. Up to 4G/LTE, designers were able to build allowances for sources of variation into the system.

But now that available bands in the lower frequencies for 5G are so closely spaced, the guard bands between useable frequencies are just a few megahertz, and the duplexer gap (the transition space between transmitted and received frequencies) is minimized.[1] Improvements in reception also contribute to increases in data capacity. This is often realized through higher power requirements to minimize signal attenuation.

➤ Right: Figure 1. How Does ALD Work? Film growth by ALD is sequential by nature. The precursor materials are kept separate during the reaction, so the reaction cycle is controlled one atomic layer at a time until the desired film thickness is achieved. This differs from CVD, which introduces multiple precursor materials simultaneously.



New approaches to RF filter design are needed.

Most smartphones now use acoustic filters. Consider surface acoustic wave (SAW) filters, which handle lower frequencies, and bulk acoustic wave (BAW) filters, which handle higher frequencies.

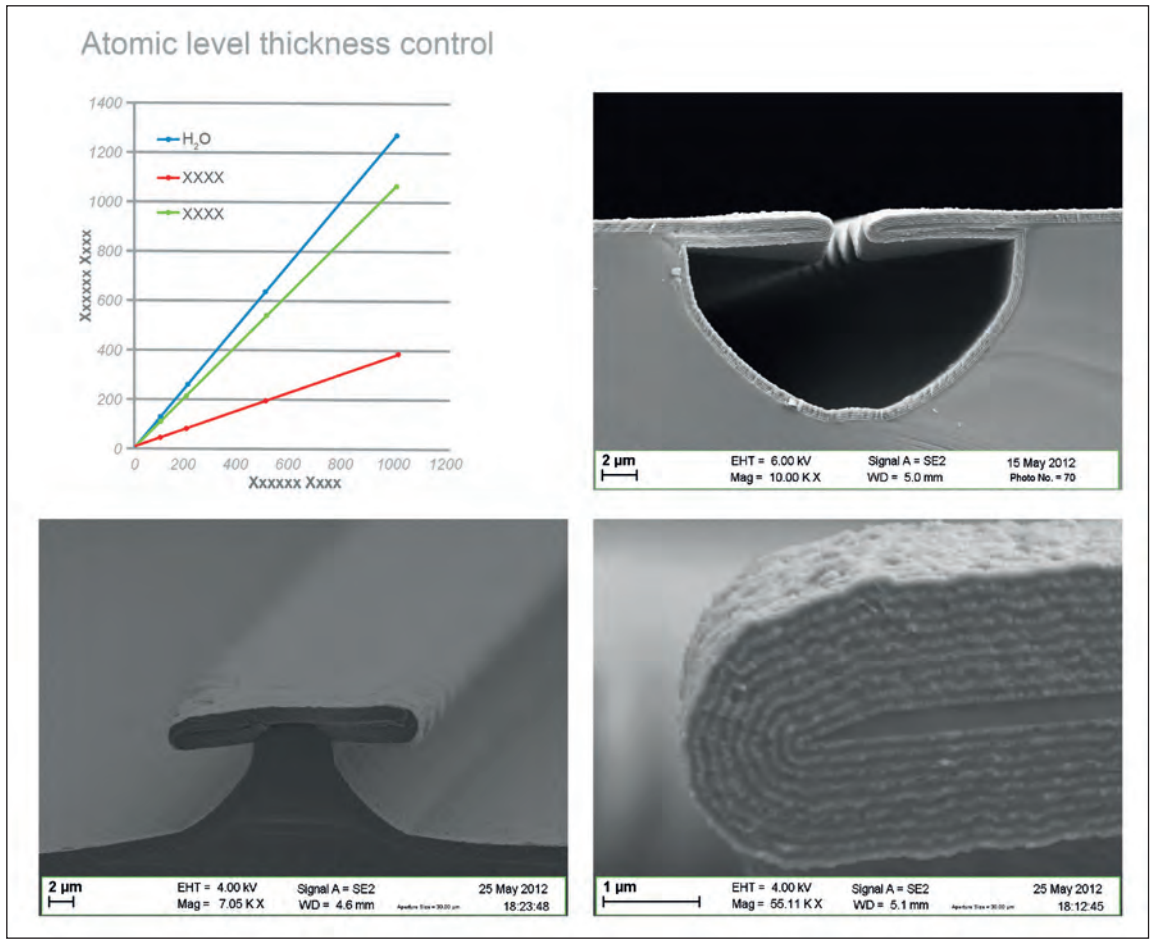
SAW filters are typically based on piezoelectric materials such as lithium niobate (LNO) or lithium tantalate (LTO). For BAW filters, aluminum nitride (AlN) is the piezoelectric material of choice. In both cases, the filters now require lower losses, higher-Q, far steeper frequency cutoff performance and a stronger signal-to-noise plus interference ratio (SINR) over a wide range of operating conditions.

Achieving steep cutoffs in RF filters demands thin films with improved etch-quality profile and uniformity. Thinner layers call for improved deposition, as well as pinhole-free, ultrathin passivation layers. Additionally, run-to-run repeatability is essential to meet high productivity at a low cost of ownership, as well as to meet volume requirements.

As the material sets for RF devices entail the use of complex piezoelectric materials such as LNO and LTO, ALD makes it possible to obtain high-stability filter performance through the application of encapsulation and barrier films. The conformal and dense nature of the ALD films provides excellent protection against environmental degradation, thereby ensuring stable operation of the devices.

Material Changes and Temperature

Drilling down further, we know that while many factors can affect acoustic filter frequency performance, a leading cause of frequency drift in the resonant frequency is temperature. This is because the stiffness of the piezoelectric material changes with temperature. Most of the piezoelectric materials in commercial use have a negative temperature coefficient of frequency (TCF). This means exposure to higher temperatures will result in a loss of stiffness, causing a drift to lower frequencies. Conversely, lower temperature exposure will increase the material's stiffness, leading to a drift to higher frequencies.[2] So far, these temperature effects have been mitigated within the industry by integrating materials such as SiO_2 (which possess a positive TCF) into the filter manufacturing process. This can offset the effects of temperature fluctuations on the negative TCF piezoelectric materials.[3] But with 5G, that's no longer enough.



➤ Figure 2. ALD results in pinhole-free coatings that are perfectly uniform in thickness, even deep inside pores, trenches and cavities. These micrographs demonstrate the ability of ALD technology to provide extremely thin, highly conformal films.

Optical studies have shown the link between the TCF and the refractive index of the dielectrics used for temperature compensation.[4] In RF filters, ALD-grown dielectrics such as SiO_2, Al_2O_3, TiO_2, Ta_2O_5 with positive TCFs can be used:

- Separately;
- As nanolaminates;
- As multicomponent films;
- As doped films to investigate the use of advanced materials as temperature compensation layers.

➤ Figure 3. The Veeco Firebird batch ALD system address the challenges encountered in processing RF filter products.

These can be applied to both BAW and SAW devices. Along with the efforts to minimize frequency drift in RF filters, the ability to protect the device from environmental impact is essential to ensure the stability and overall filter reliability. Use of ALD films to provide protection from environmental effects and enhance device stability is well-documented.

Given the thermal sensitivity of piezoelectric materials such as LNO and LTO, the low temperature processes offered by ALD provide an excellent solution for negotiating the thermal budgets often associated with these materials. The use of ALD films can help to ensure that filter performance metrics – such as sharp cutoff characteristics and high Q-factors – are maintained and don't drift over time, causing interference with adjacent frequencies and signal degradation.

Enhanced Power Durability

Another area in which ALD can benefit RF filters is with power durability (the ability for a filter to work for extended periods under high power conditions). As filters evolve to address higher frequencies, durability becomes more challenging. Resonator areas shrink and layers become thinner; thus, the overall resonator volume decreases. Consequently, the power density in the device increases, which can increase the likelihood of failures due to thermal or fatigue issues and degrade the overall device reliability.[5,6]

Estimated Cost of Ownership
Veeco Firebird ALD System for RF Filters

Parameter	Assumptions	Impact
System Price	$2.5M, amortized over 5 years	$500,000/year
Consumables + maintenance	10% of price	$50,000/year
Throughput	1350 wafers/day x 365 days/year	492,750 wafers/year
Cost per wafer	$550,000/492,750 wafers	$1.11/wafer
Size of packaging for SAW devices 1.6mm x 1.2mm	Assume device might be 1.4mm x 1.0mm (a bit smaller than packaging)	–
Area of 150mm wafer with 5mm edge exclusion	pi (140mm) $^2/_4$	15,393mm^2
Possible number of devices on a 150mm wafer	15,393mm^2/1.4mm^2	10,995 devices
Cost per filter	Cost per wafer / No. of filters = $1.11/10,995	$0.0001/filter
Or, assume filters are larger and there are only 100 filters per wafer, so throughput is down by 3x	Then cost per filter = 3($1.11/100)	$0.3/filter

The filter's power durability can be improved by adding an ultrathin buffer layer between the piezoelectric material and the metal electrodes. This is an application area in which the extremely thin, dense films created using ALD technology can be beneficial. Buffer layers can help change the texture of the electrode materials by changing grain structure morphology. This in turn helps suppress the migration of electrode material atoms, such as Al, under high power conditions.

Equipment and Process Solutions

When it comes to RF filters, the brittleness and susceptibility to thermal variations in materials such as LNO and LTO pose unique production challenges. Additionally, these piezoelectric materials are pyroelectric (they can generate temporary voltage when heated or cooled).

Therefore, ALD systems for RF filters must meet particular challenges, including:

- Wafer handling (to prevent breakage of the brittle materials);
- Throughput: preheat and process modules need to operate in parallel to address thermal variations and
- Scheduling and process consistency for high yield.

Veeco's Firebird™ is an example of an ALD system that is particularly suited to addressing the needs of the 5G RF filter process. It uses a unique handling architecture in combination with controlled environment load locks to realize breakage-free movement of wafers within the system. The system is highly configurable and can be composed of a combination of process modules and preheat modules corresponding to the required level of productivity. Additionally, multibatch operation employing Firebird's intelligent scheduler enables superior throughput and process consistency, resulting in high-performance RF devices. Veeco has perfected ALD as a manufacturing-grade technology by scaling up the process and implementing it into automation lines and cluster tools around the world. Manufacturers that have integrated its ALD systems have seen increased product quality and reliability as well as decreased operating costs and a greener footprint as compared to previous coating technologies.

Conclusion

Improvements in RF Filter technology are critical to the growth of 5G mobile communications. As the push to expand data transmission capacity increases, the challenges to producing filters that meet those specifications and needs also grow. Within that context, ALD technology can provide a robust, cost-effective solution to meet the ever-tighter filter performance specifications.

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Achieving ALD consistency is key to maximizing chip yields

Atomic Level Deposition (ALD) has emerged as an increasingly important aspect of advanced semiconductor manufacturing. The experts at Swagelok explain the role that valves play in maximizing chip yields.

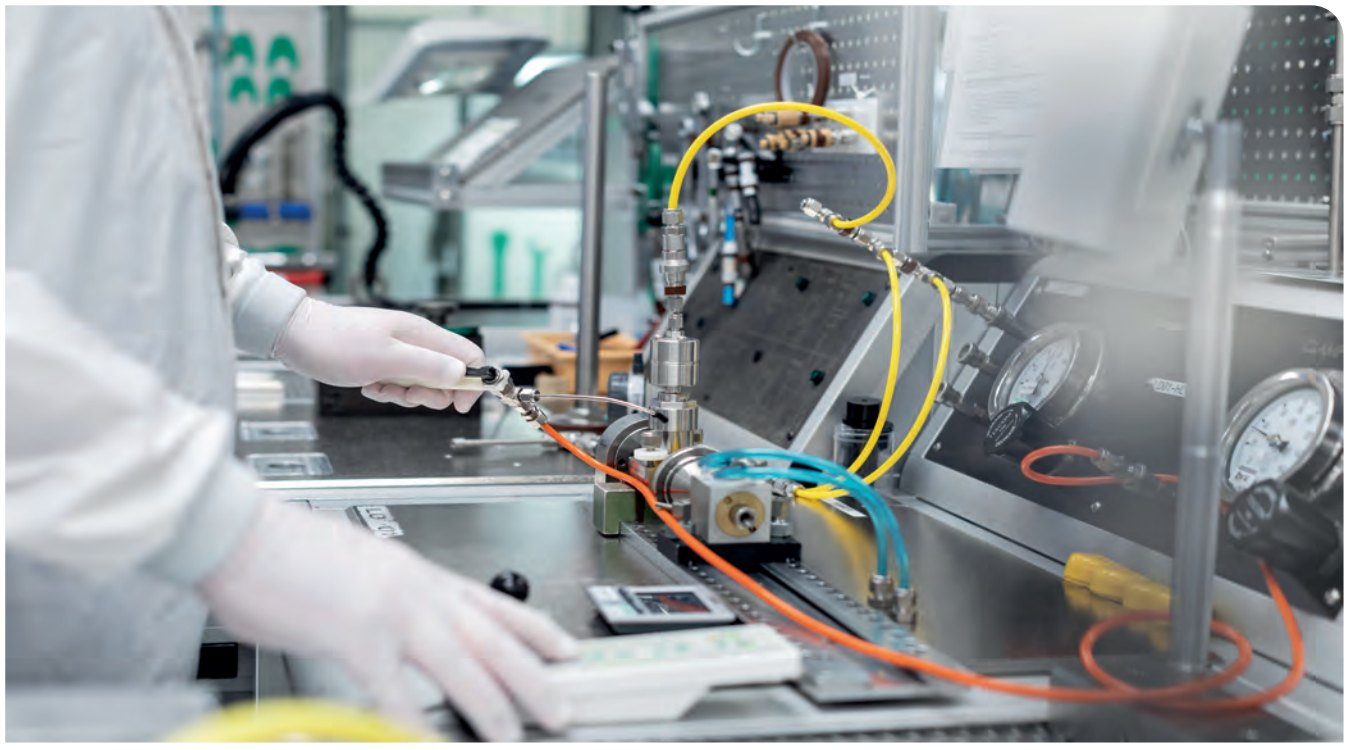
BY MASROOR MALIK, MARKET MANAGER FOR SEMICONDUCTOR, SWAGELOK COMPANY

The Keys to Optimized Microchip Production

Moore's Law, attributed to Fairchild Semiconductor and Intel co-founder Gordon Moore, predicted that chip complexity (density) would roughly double every year, reducing the cost of computing by half. While the original 12-month timeframe has been extended and modified over the years as chip complexity grew, Moore's prediction in 1965 has largely held true, and the semiconductor industry has worked hard to make it happen.

Maximizing throughput in the increasingly complex and sensitive processes required to manufacture modern microchips is one of today's biggest challenges for semiconductor producers. Tighter process controls and narrower performance tolerances in production processes represent some primary strategies fabs are using to achieve ever-shrinking device feature size while optimizing chip yields.

As the desire to increase transistor density drove chip architecture innovation, process tool manufacturers have created increasingly complex front-end processes to support design goals and maintain quality, performance and serviceable lifetimes. While



➤ Figure 2. Corrosion that forms in the valves, tubing, or fittings, can produce particles that contaminate the wafer. In ALD, particularly with liquid or solid precursors, condensation on cold spots or parasitic deposition in the valves or delivery system can also produce particle defects and negatively impact yield.

today's definition of 'advanced node' has breached 5nm on the way to 3nm and below, manufacturers can in a sense be divided by how they achieve greater transistor density and/or performance goals while maintaining high, profitable yields. The largest fab operators are increasingly relying on extreme ultraviolet (EUV) lithography to achieve this aim. But the $125 million price for a single EUV lithographic station is evidence that the growing expense of traditional CMOS scaling has led some manufacturers to pursue other paths. Nontraditional innovation includes the move to 2D and 3D structures, wafer bonding, advanced packaging technologies like FOWLP that increases inputs/outputs (I/O), as well as moves to make production processes once seen as novelties fully suitable for high volume manufacturing.

➤ Left: Figure 1. It has become increasingly evident that high levels of precision in chemical dosing and delivery are essential parts of an optimally productive ALD process. Importantly, that precision must be maintained consistently at every dose. But pulling off both conditions simultaneously becomes inherently more challenging as feature size is reduced.

One increasingly popular process used in manufacturing advanced semiconductors is atomic level deposition (ALD). The modern ALD process has become a focal point for achieving increased accuracy and consistency. It has become increasingly evident that high levels of precision in chemical dosing and delivery are essential parts of an optimally productive ALD process. Importantly, that precision must be maintained consistently at every dose. But pulling off both conditions simultaneously becomes inherently more challenging as chip size is reduced. (See Figure 1).

How can fabs achieve such consistency and precision in the ALD process? It has been shown that advanced, well-designed ALD valve technology can contribute to achieving these goals.

At the Intersection of Precision and Reliability

Within the ALD process, semiconductor fabricators are generally working to maintain atomic layer precision in deposited films over an entire 300-millimeter diameter wafer. To give a sense of scale, that is the equivalent of applying a 1-centimeter layer over the entire moon. And in modern semiconductor devices, even the smallest variations in that film (even a few extra atoms)

In ALD, particularly with liquid or solid precursors, condensation on cold spots or parasitic deposition in the valves or delivery system can also produce particle defects and negatively impact yield

can noticeably and negatively impact end-user device performance.

One significant factor that influences the deposited layers is the specific concentration of chemicals in each atomic layer process dose. Maintaining the proper concentration requires high levels of precision in chemical delivery throughout each dose, necessitating specialized ALD valves to start and stop the flow of chemical reagents into the process chamber in the desired manner. Considering that ALD processes typically involve hundreds of dosing steps, these process valves are actuated continuously. It is not uncommon for valves of this nature to cycle upward of 1 million times each week.

Thus, extremely high-cycle reliability is a requirement. Simultaneously, because process valves may also function as a flow-limiting element in some applications, flow capacity and consistency may also be important to maintain over the life of the valve. In addition, flow consistency from valve to valve will be critical in achieving process matching and in maintaining process consistency after valves have been changed.

Heightened Actuation Speed Contributes to Consistency and Efficiency

Raw actuation speed can also contribute to more efficient production. Faster actuation can compress the time between process steps, and when taken cumulatively, such compression can contribute to a significant reduction in the total processing time.

However, it is also important to remember that valves with high, consistent flow and fast, repeatable actuation are only useful if they are compatible with the chemicals being delivered and the temperatures of the delivery system. Corrosion in the valves, tubing, or fittings can produce particles that contaminate the wafer. In ALD, particularly with liquid or solid precursors, condensation on cold spots or parasitic deposition in the valves or delivery system can also produce particle defects and negatively impact yield (See Figure 2).

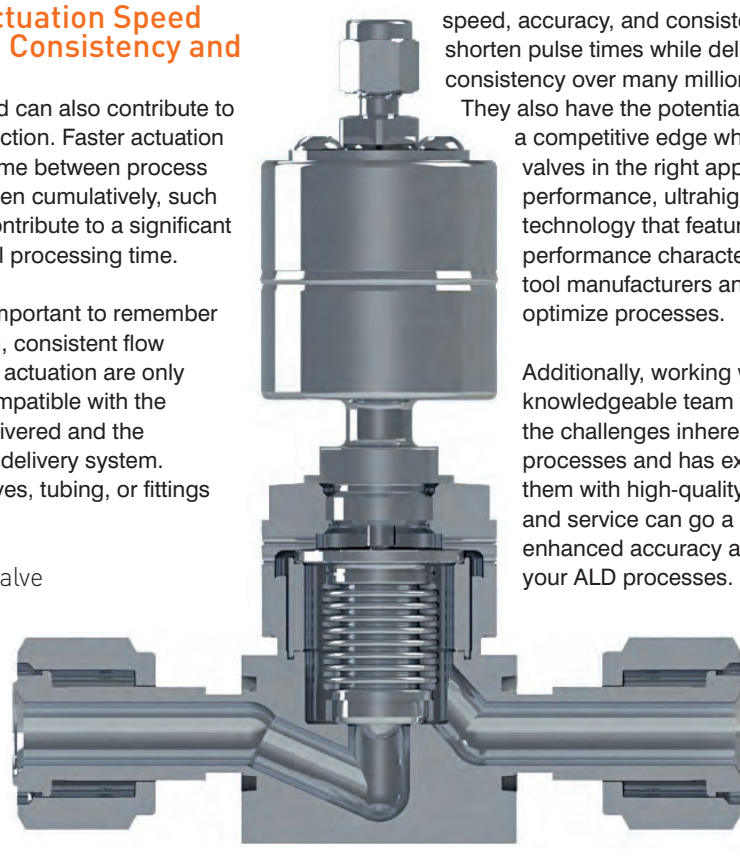
ALD repeatability is unambiguously linked to the consistency and accuracy of the discrete chemical doses used. Anything that may lead to some form of change or difference within the chemical doses will cause a change or difference in the associated process.

Achieving More Profitable Production

Given the complexity involved in achieving consistent, accurate dosing, there is no single solution to account for all factors that go into devising absolutely consistent and reliable ALD processes. However, there are dependable ways to improve processes that you can take advantage of today.

Advanced ALD process valve technology has evolved to meet the cutting-edge needs of semiconductor chip fabricators and tool OEMs (See Figure 3). Available ALD valves can deliver improved speed, accuracy, and consistency, helping to shorten pulse times while delivering outstanding consistency over many millions of cycles. They also have the potential to help you gain a competitive edge when using such valves in the right application. High-performance, ultrahigh-purity ALD valve technology that features several critical performance characteristics can help tool manufacturers and fabricators optimize processes.

Additionally, working with a knowledgeable team that understands the challenges inherent to atomic layer processes and has experience solving them with high-quality components and service can go a long way toward enhanced accuracy and consistency in your ALD processes.



➤ Figure 3. Advanced ALD process valve technology has evolved to meet the needs of semiconductor chip fabricators and tool OEMs. Available ALD valves have the capability to deliver improved speed and consistency, helping to shorten pulse times while delivering outstanding consistency over many millions of cycles.

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Outlier control technology and feedforward lithography can boost FOPLP yield

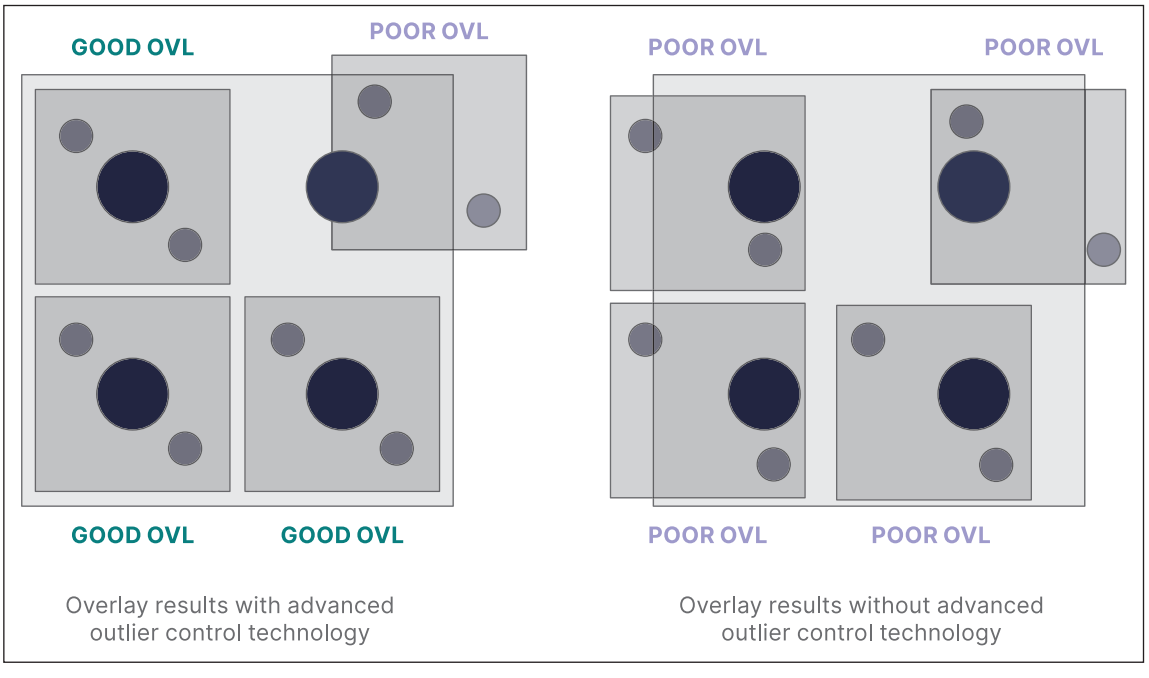
Fan-out panel level packaging (FOPLP) has many advantages, but the critical challenge of die placement error can substantially impact yields and costs. The experts at Onto Innovation describe how they are helping solve the problem for customers by substantially increasing both yield and throughput.

BY JOHN CHANG, ONTO INNOVATION INC.

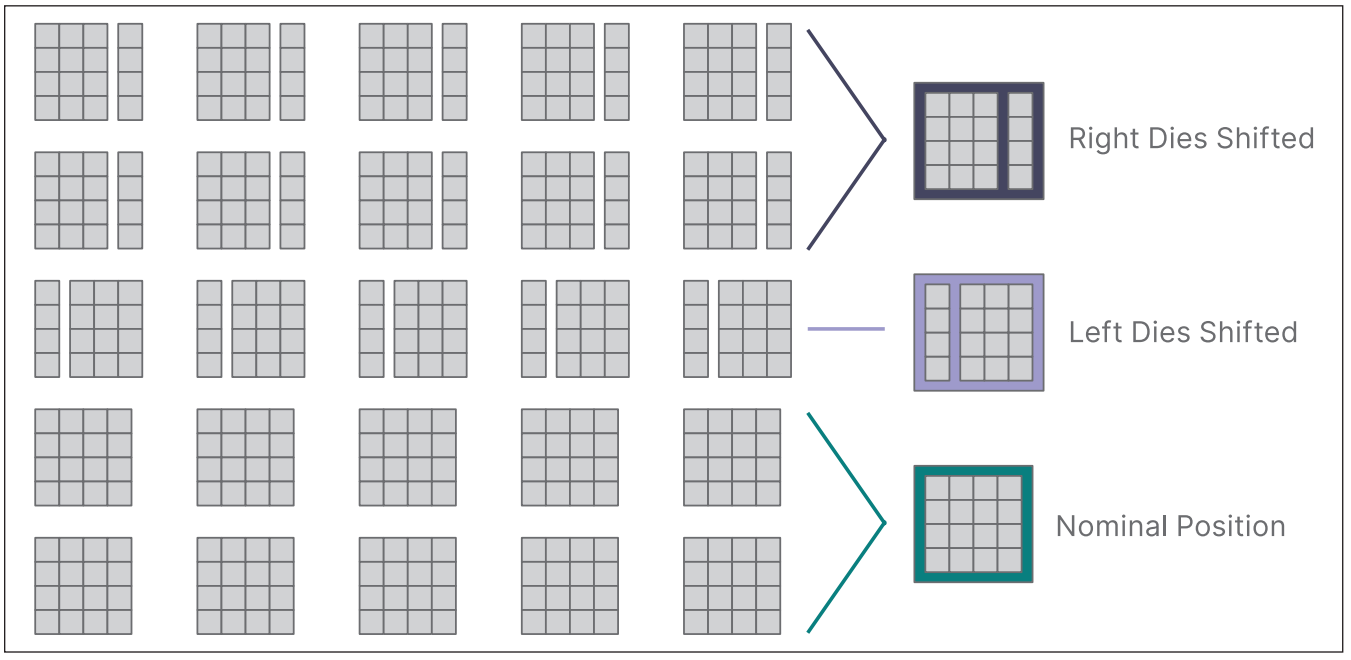
FAN-OUT PANEL LEVEL PACKAGING (FOPLP) has multiple benefits in advanced packaging applications, including enhanced connectivity and reduced costs. FOPLP differs from wafer-level packaging processes in that FOPLP utilizes large, rectangular panels rather than the round silicon wafers typically associated with IC manufacture. FOPLP's rectangular panels more efficiently fit rectangular die, which can reduce costs since manufacturers can process more packages in each run.

Despite many advantages, FOPLP also faces specific challenges, such as yield loss caused by inaccurate die placement and the resulting overlay errors. In this context, dies with unusually large placement errors, or outliers, can be especially troublesome.

These outliers cause losses of both the misplaced die and surrounding dies. However, integrating outlier control with feedforward metrology can greatly improve both yield and throughput.



➤ Figure 1. Outliers with large placement errors can cause unacceptable overlay errors, but excluding outliers from the correction calculation preserves the remaining dies.

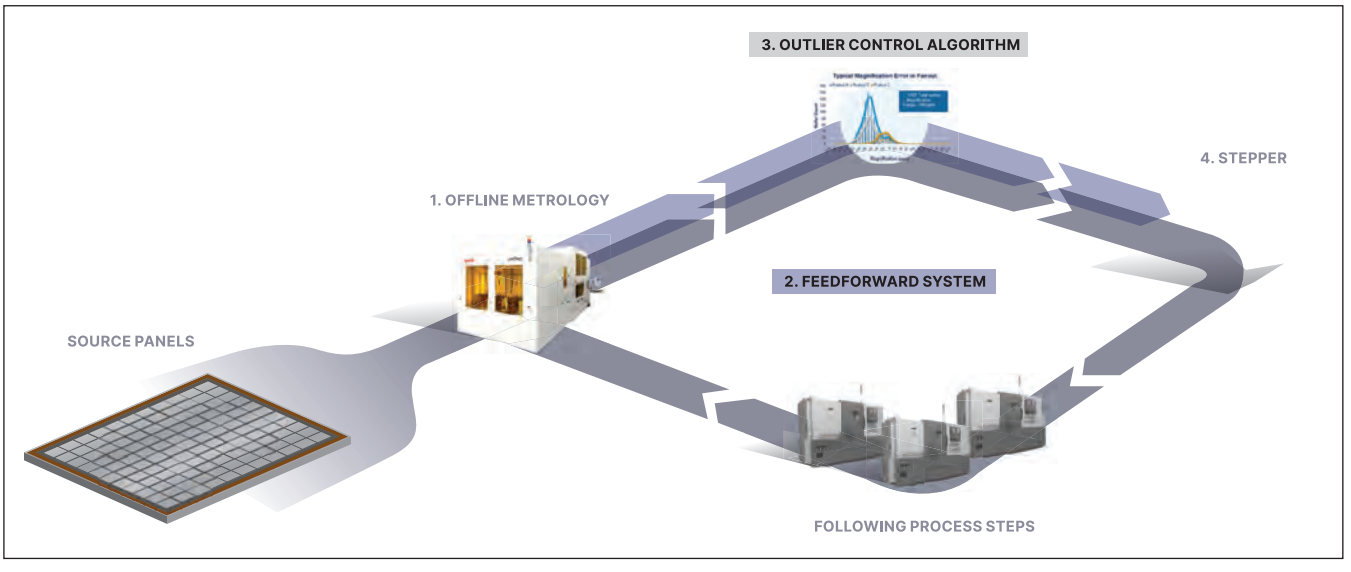


➤ Figure 2. The die clusters in the first three rows included intentional placement errors: in the first two rows, the rightmost column of each die cluster was shifted 100µm to the right; in the third row, the leftmost column of each die cluster was shifted 100µm to the left. The fourth and fifth rows did not include intentional errors.

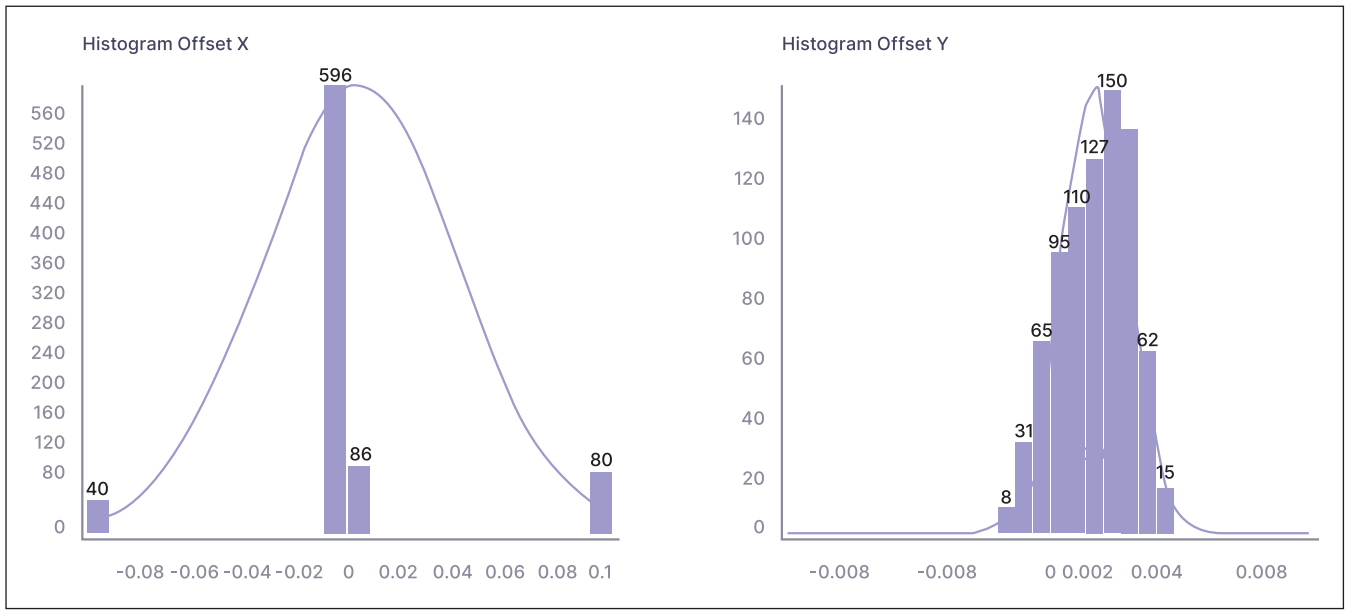
Fan-out processes cut individual dies from the wafer and reconstitute them on a processing substrate separated by additional space. Subsequent steps fabricate redistribution lines in multiple layers and end with the creation of contacts on the surface of the package. The area available for contacts is increased by the additional space between chips, allowing more contacts per chip.

One critical challenge for FOPLP is die-placement error. This error originates during the robotic pick-and-place operation in which chips are positioned on the reconstitution substrate. The problem arises when die positions shift during subsequent processing steps. If uncorrected, these die-placement errors can result in overlay errors and reduced yield.

While die-placement errors can be measured and corrected, die-by-die in the lithography tool, this greatly reduces throughput. Feedforward lithography, which measures placement errors and calculates corrections in a separate system and then feeds



➤ Figure 3. Feedforward lithography and advanced outlier technology integrated in a FOPLP process. 1) A panel is processed by an offline metrology tool. 2) The metrology data is fed forward to the outlier control algorithm. 3) The outlier control algorithm identifies the outliers. 4) The processed metrology data is fed forward to the lithography tool for site-by-site or die-by-die exposure corrections.

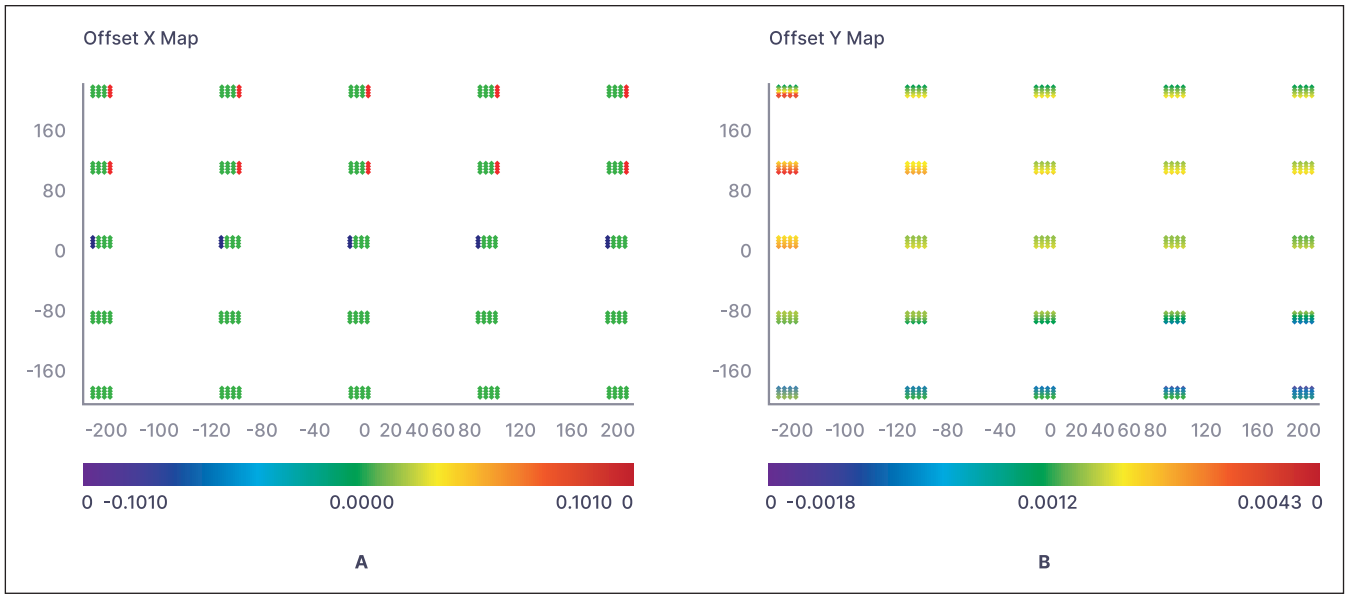


➤ Figure 4. (left). The X placement deviation histogram shows most die having little error and some die with +100µm and -100µm errors, which matched the designed die errors of the test panel. The Y placement deviation histogram shows a small range (+4µm to -2µm), as expected.

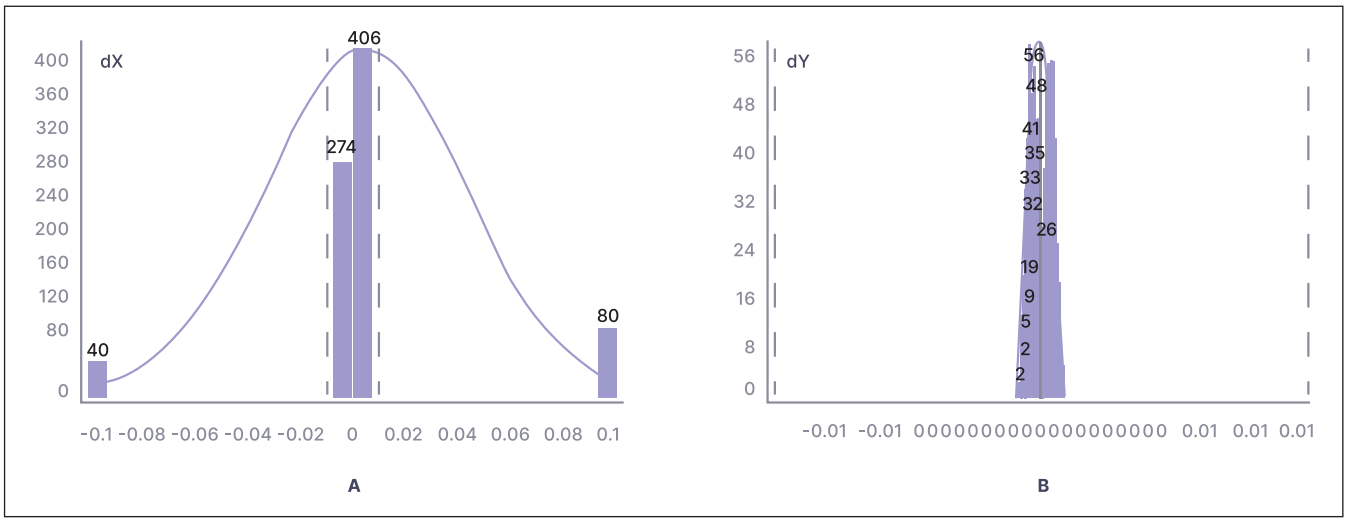
the corrections forward to the lithography system, is much faster. Lithography throughput can be further increased by including more than one die in each exposure site and then applying site-by site corrections to the exposures.

In this scheme, dies with unusually large placement errors can have an outsized impact on yields by skewing the site correction to such a degree that the site correction causes unacceptable overlay errors for all dies in the site. A solution: advanced outlier control technology (Figure 1). This technology detects outliers and excludes them from the correction calculation, thereby sacrificing the outlier to optimize overall yield and throughput.

Onto Innovation evaluated the use of advanced outlier control technology with feedforward lithography on a test panel. The test panel included intentionally displaced dies with large known placement errors. In the evaluation, integrating site-by-site exposure, offline feedforward metrology and advanced outlier control significantly improved both yield and throughput. To demonstrate the benefit of site-by-site exposure, offline feedforward metrology and advanced outlier control, these technologies were evaluated using



➤ Figure 5. (a) Heat map of die error in X axis. The right dies in the first two rows (red) have +100µm error. Left dies in the third row (blue) have -100µm error, reflecting intentional errors in test panel. (b) Heat map of die errors in Y axis. All the die errors are within -2µm to 4µm. No large Y axis errors are seen within clusters.



➤ Figure 6. (a) Predicted residue values in X: two groups are observed at ±100µm from the designed outliers. The rest of the data points are within ±3µm. (b) Predicted residue values in Y axis: all the predicted residue values are within ±2µm, which matches expectations.

a 510mm x 515mm test panel containing 400 dies (Figure 2). The dies were grouped in 25 clusters arranged in a 5 x5 array across the panel. Each cluster contained 16 die in a 4 x4 array and was included in a single exposure site. A site correction was calculated from the individual placement errors measured for the included dies and then applied to each exposure.

The die clusters in the first three rows included intentional placement errors: in the first two rows, the rightmost column of each die cluster was shifted 100µm to the right. In the third row, the leftmost column of each die cluster was shifted 100µm to the left. The fourth and fifth rows provided a control group that did not include intentional errors. Without advanced outlier control technology, researchers expected all dies in the first three rows to suffer poor overlay when using site-by-site exposure.

Test panel placement errors were measured using an offline metrology tool that analyzed the measurements to identify outliers. The outlier threshold was set to 15µm. Dies with placement errors that exceeded the threshold were marked, and their information was discarded during the correction calculation. The correction data were fed forward to the stepper and used in the site-by-site exposure process.

Figure 3 shows the working scenario of feedforward lithography and advanced outlier technology.

Researchers used an Onto Innovation JetStep® 3500 Lithography System. This system supports up to 720mm x 600mm glass panels or up to 510mm x 515mm copper clad laminate (CCL) substrates. The optical system has a 2:1 magnification and an exposure field of up to 59mm x 59mm. The system can achieve 2µm resolution with ±400ppm magnification compensation. Compensation is required in a fan-out process to correct the die errors.

The lithography tool's pattern recognition system can be trained to use a unique pattern within the field of view as an alignment site and measure the X and Y positions of patterns across the panel. This enables local die-by-die exposure and site-by-site exposure capability without the use of offline metrology. The system can also accept feedforward corrections from an offline metrology tool, as evaluated in this study.

The Onto Innovation Firefly® automated optical inspection (AOI) system was utilized for the offline measurement of die-placement errors for feedforward metrology. This tool supports up to a 510mm x 515mm substrate.

Adding outlier control technology and feedforward lithography increases throughput to 62.7 panels per hour and yield to 85%. The numbers will vary for different processes, but feedforward lithography and outlier control offer significant improvements in yield and throughput in this evaluation

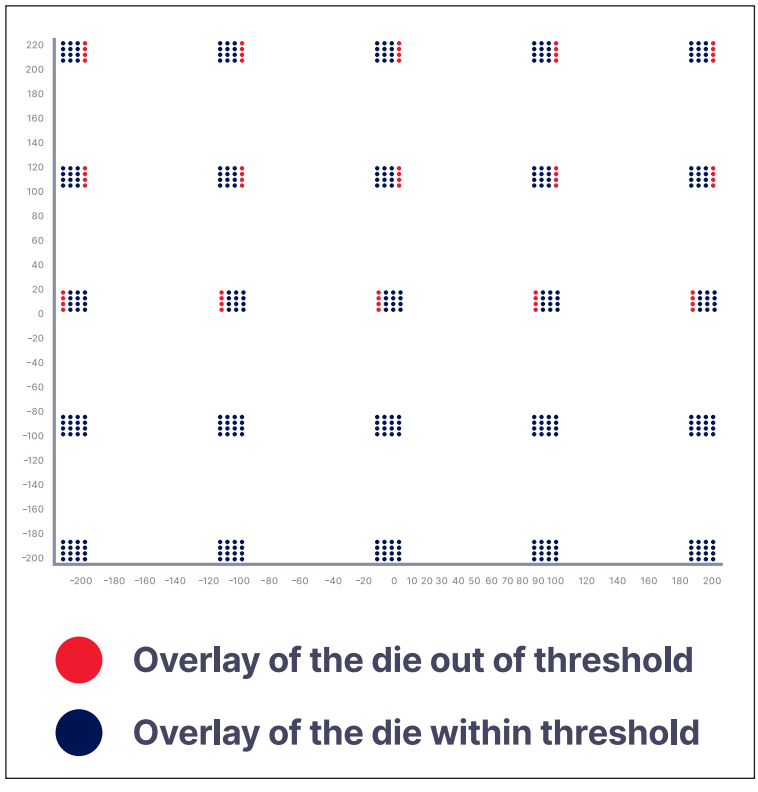
Ef Num	Yield	Offset Threshold	Outlier Shot Num	Outlier Point Num
min		min	min	
25.0000	0.8500	0.0150	0.0000	120.0000

➤ Figure 7. Predicted yield of the test panel is 85%. Yield prediction is a feature of the feedforward system used in this study. The overlay threshold is set to ±15 µm.

In the feedforward operation, die location and error data are automatically sent to the outlier algorithm and the stepper.

Results

Figure 4 shows the die-error histogram of the metrology data from the offline metrology tool. The left side of Figure 4 shows the placement deviation of the dies on the test panel in the X direction. The maximum X deviation was around +100µm, and the minimum X deviation was around -100µm, which matched the die errors that were designed into the test panel. The right side of Figure 4 shows the placement deviation of dies in the Y direction. The Y deviation range was from -2µm to +4µm, which was normal and expected.



➤ Figure 8. Heat map created by an offline metrology tool of actual overlay results for the test panel: the distribution of good and bad die overlays matched the design layout and expectation with outlier control enabled.

Figure 5 shows heat maps of the die error in the X axis (left) and the Y axis (right) on the test panel. The right dies in the first two rows are marked red, indicating a die error around +100µm. The left dies of the third row are marked blue, indicating a die error around -100µm. Rows 4 and 5 are all green, meaning there is no shift in the X axis. Y errors show no large placement errors within the clusters. In the study, any die with an error of more than 15µm was marked as an outlier and discarded during site-by-site correction calculations.

Figure 6 shows the predicted X and Y residue values after correcting the die error using site-by-site exposure. The site-by-site exposure was run using the processed metrology data that was fed forward by the outlier control algorithm. The left side of the figure shows the residue values of most points are within ±3µm. The residue values for the rest of the points are around +100µm and -100µm, as expected. The right side of the figure shows that all data points have very small residue values in the Y axis, ±2µm. Figure 7 shows that the final predicted overlay yield is 85%, using site-by-site exposure with the overlay threshold set to ±15µm. Predicted residue values and yields are features of the feedforward system.

Following all the processes (feedforward metrology, site-by-site exposure and developing), actual overlay results for the test panel were measured with the offline metrology tool. The actual overlay results are shown in Figure 8 and Table 1. In the overlay heat map a blue dot indicates the overlay is within specification, in this case ±15µm. A red dot indicates the overlay is out of specification. The heat map matched predicted and expected results. Table 1 shows the overlay statistics of the good dies in the test panel; deviations in X and Y are less than 5µm, and all numbers are within the overlay threshold.

Table 2 compares the impact on yield and throughput of the various technologies we have described. With regular die-by-die lithography, the yield is 100%, but the throughput is only three panels per hour. With site-by-site lithography, the throughput increases to 32 panels per hour, but the yield drops to 40%. Adding outlier control technology and feedforward lithography increases throughput to 62.7 panels per hour and yield to 85%. The numbers will vary for different

	Average	Max	Min	Range	Std Dev
dx	1.04	2.20	-0.31	2.50	0.60
dy	0.25	1.40	-0.75	2.15	0.34

➤ Table 1. The statistics of good dies on the test panel. All the numbers are within ±2.5µm and the ±15µm overlay threshold.

	Features Used				Shot Number (ea)	Yield (%)	Throughput (pcs/hr)	Throughput Improved (%)
	Die by Die	Site by Site	Outlier Control	Feed Forward				
Condition 1	•				400	100	3	NA
Condition 2		•			25	40	32	966.67%
Condition 3		•	•		25	85	32	966.67%
Condition 4		•	•	•	25	85	62.6	1986.96%

➤ Table 2. Yield and throughput comparison table.

processes, but feedforward lithography and outlier control offer significant improvements in yield and throughput in this evaluation.

Summary

In the metrology data collected for this demonstration, the outliers showed large die errors compared to other nominal dies. The outlier control algorithm correctly identified all outliers using a customized threshold set to 20µm. Outliers were marked and discarded in the following exposure processes. The rest of the dies maintained good overlay. The outlier control technology worked as expected.

The study demonstrates the ability of outlier control technology and offline feedforward metrology to accurately identify outliers, eliminate their negative influence on site-by-site corrections and send optimized correction data to a lithography tool. It also shows that these technologies can be integrated to work together in a FOPLP process line.

Adding outlier control technology to site-by-site exposure boosted yield from 40% to 85%, and the combination of outlier control with off-line feedforward metrology increased throughput by approximately 20 times.

FURTHER READING

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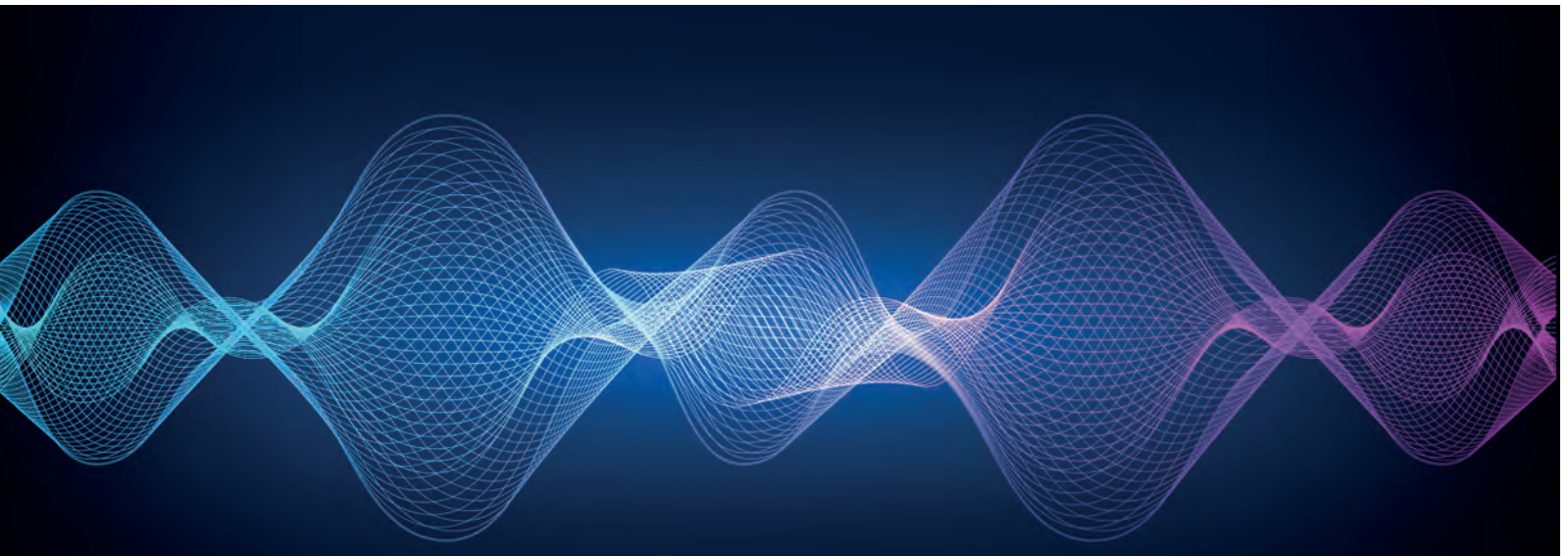


Screening and analyzing:
The two realms of acoustic micro imaging

From the time they exist merely as part of an undiced wafer until they are installed in the end product, electronic components undergo testing and measuring by a variety of instruments to ensure a long, failure-free life. One instrument is the Acoustic Micro Imaging (AMI) tool, which uses the multiple types of data delivered by ultrasonic echoes to its transducer to characterize internal material interfaces and material properties within a given component.

BY TOM ADAMS, CONSULTANT, NORDSON TEST & INSPECTION

EVEN BEFORE production of a component begins, the Acoustic Micro Imaging tool's ability to locate and image internal structural features in component prototypes permits evaluation of the package design's integrity and robustness without activating or cutting open the component. The tool's images can verify, for example, that a prototype's die bond contains no unbonded areas, or that the encapsulant or underfill has no air-filled voids. The tool is also valuable in evaluating and viewing the results of thermal excursions in components after stress testing.

When a component in normal service has experienced a field failure, AMI data and images can help pinpoint the cause by non-destructive imaging before the component is physically cut open to permit visual inspection. The destructive process is known as Acoustically Guided Destructive Physical Analysis (AGDPA).

In the design and prototype applications mentioned above, the AMI tool operates in a laboratory, and usually analyzes small numbers of components at a time. But both the manufacturer and the user of the components perform large-scale screening.

The components are placed on trays and imaged at high speed by an automated AMI tool. The two imaging environments - low-volume analysis and high-volume screening - are described separately in this article.

Principles of Acoustic Micro Imaging

When the transducer of an Acoustic Micro Imaging tool fires a pulse of ultrasound into the surface of an electronics component, the pulse moves (#1 in Figure 1) through the water that couples the transducer to the component. When the pulse strikes the interface (#2) between the water and the surface of a component, a portion of the pulse's energy is reflected (#3) back to the transducer, where its arrival time reports the distance from the transducer to the component's surface.

The other portion of the pulse enters (#4) the first layer of material, which is typically an encapsulant. The smaller size of the pulse represents the partitioning of the energy at the interface.

The ultrasound travelling through the encapsulant reaches the interface (#5) between the encapsulant and the silicon die. From this material interface a portion of the ultrasound will again be reflected (#6) back to the transducer. The rest of the ultrasound crosses (#7) the interface into the die.

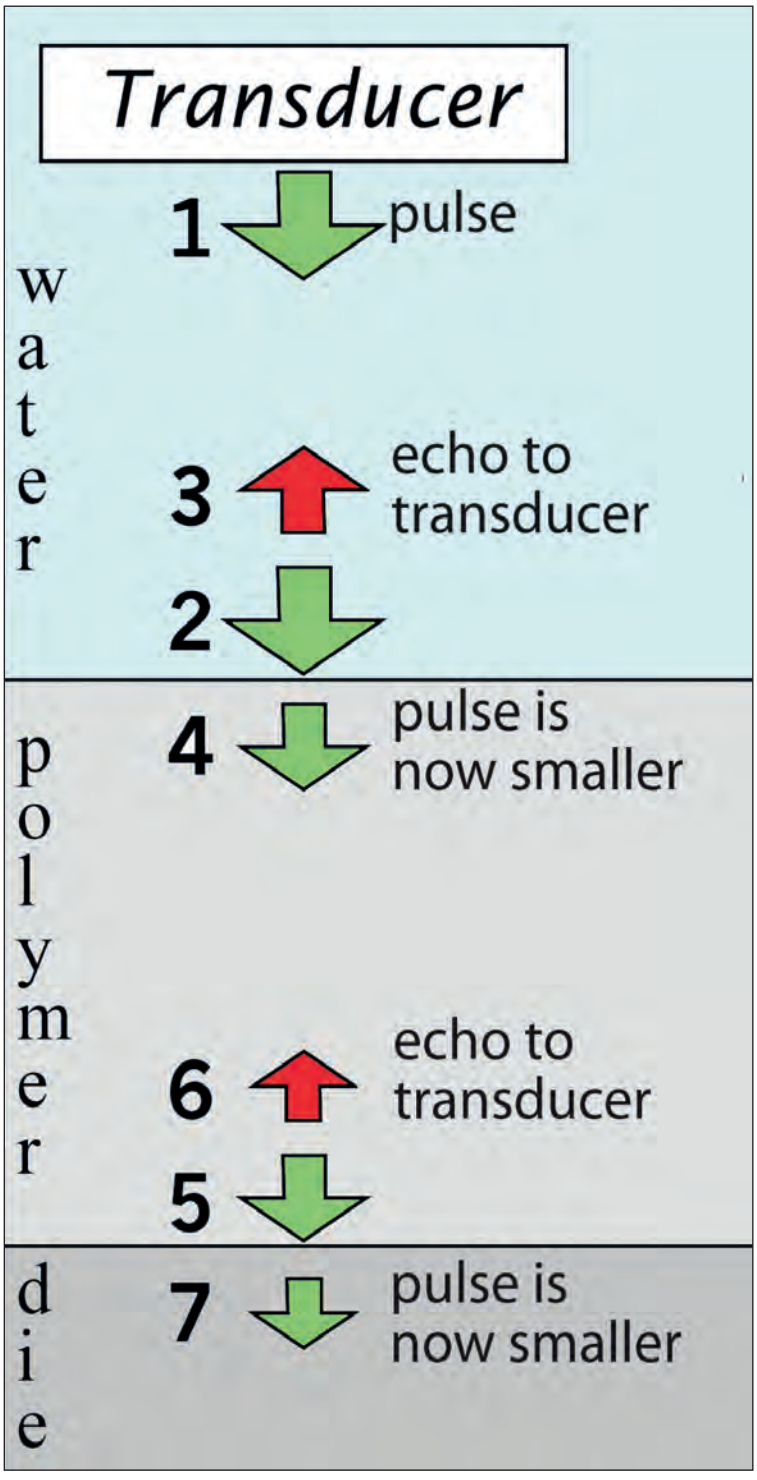
This echo returning from the interface, #6, arrives at the transducer and reports its travel time, and thus the depth of that interface. It also reports its amplitude, its ultrasonic frequency content, and the polarity (positive or negative) of the interface. These bits of data tell the user the depth of the interface and much about the two materials at the interface.

The transducer scans rapidly across the surface of the component and each second launches a pulse at each of tens of thousands of x-y locations, receiving the echoes from each location before launching the next pulse. Software will turn the returning echo from each location into one pixel in the acoustic image of the component. The pixel can be made to represent various aspects of the echo, for example, amplitude, frequency content, arrival time, etc.

The completed acoustic image may show the interface between the encapsulant and the silicon die as one color, and an interface between the encapsulant and copper as a different color.

But the AMI tool will image the interface between a solid material and air (through which ultrasound at these frequencies will not travel) most brightly because the solid-to-air interface reflects nearly 100% of the arriving pulse. AMI systems easily find hidden internal defects because most performance-threatening defects contain air and thus present a solid-to-air interface to the arriving pulse.
In black and white acoustic images, solid-to-air regions are typically imaged in bright white. In color images, red is often selected for these air gaps, which represent the voids, cracks, delaminations that often cause electrical failures in service.

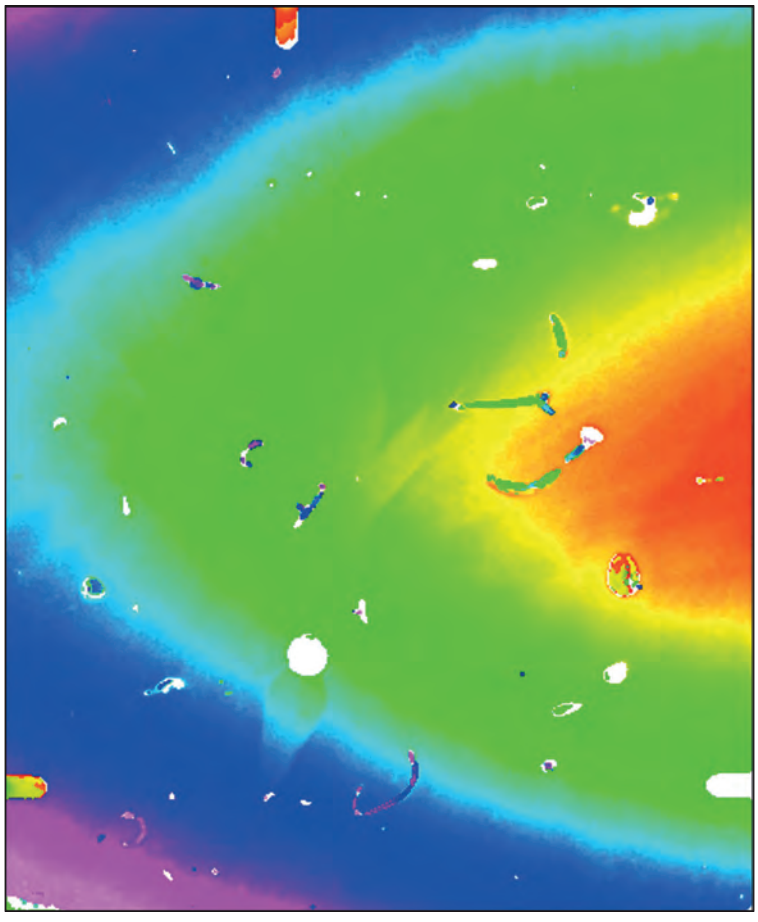
In some components, the user's interest may be only in a single depth within the component. In a given component type, if failures usually involve the die bond, a narrow electronic gate can be set that collects only those echoes that arrive at the transducer in the time slot matching the vertical extent of the die bond material.



➤ Figure 1. Sequence of events when a pulse is launched into a component.

Laboratory Analysis

From the basic technology briefly described above, acoustic micro imaging tools have been developed to ensure that electronic components installed in products are free from internal structural anomalies that could result in electrical failures in service. One of these is SONOSCAN's laboratory C-SAM® from



➤ Figure 2. IGBT imaged by Water Plume through the heat sink.

Nordson Test & Inspection. It does not handle multiple trays of components; instead, it was designed to image anything from a single component to a tray of components, but it is equipped with all of the C-SAM imaging modes, which total about 14.

C-SAM analysis may be used for one or more components of the same type. They may be components that failed in service or during environmental testing, or they may be a few sample parts from a new shipment of a component that is in constant use. Or they may be an entirely new component that will be introduced soon. All of these may be imaged to find anomalies or material changes that could lead to defects. Multiple acoustic imaging modes are frequently used to ensure that even hard-to-detect anomalies are found and imaged.

Components may also be analyzed without imaging to determine whether the mold compound in a new shipment differs from the mold compound used in previous shipments. Typically a small number of components receive a single pulse at five locations. If the acoustic impedance and acoustic absorption values are close to the values from previous shipments, very likely the materials are identical.

An IGBT module may be imaged in the C-SAM reflection mode, as shown in Figure 1. In this mode echoes are received from all depths to assemble the acoustic image. This method may provide an overall view, but if the purpose is to examine closely all depths, the user may find that some depths are out of focus and cannot be accurately assessed.

A better choice may be the PolyGate mode. In this mode, the transducer divides a stream of incoming echoes from each x-y location into, say, 5 groups by their arrival time, and is thus able to create 5 images showing five separate depths.

Figure 2 was made to reveal possible internal defects in an IGBT module. Unencapsulated IGBT modules must be imaged through their bottom surface because topside imaging might leave residue that could lead to an electrical failure in this high-power component.

Bottom-surface scanning is done with a type of C-SAM tool having the transducer inverted. It pulses ultrasound into the IGBT that is above it. Ultrasound from the transducer reaches the heat sink at the bottom surface of the IGBT through a column of water called the water plume.

The gate is often set to collect echoes from a depth beginning just above the inside of the heat sink and ending just above the surface of the ceramic raft. If it is desired to image the die themselves, which are on the top side of the raft, the gate is extended to include them.

But in Figure 2 the depth of interest was the solder layer between the heat sink and the raft. Two facts were immediately evident:

- The thin ceramic raft is warped. The Time Difference mode was used for this image. The color of a pixel is determined by the feature's distance from the transducer, or from a reference layer in the sample, but not its amplitude or some other property. The red region is farthest from the transducer; the barely visible white region at the lower left corner may actually lack solder and be in contact with the heat sink.

- The small variously shaped features within the solder are voids filled with air. The color reflected by a void is determined by the depth from which echoes are being returned. White voids are probably flat against the heat sink. There are green and blue and pink voids, and some multi-colored voids that extend through more than one depth color.

The message in this image is quite direct: there are significant differences in solder thickness, which will lead to uneven distribution of heat from the die above. There are in addition air-filled voids that will reflect heat back to the die. This IGBT may not be suitable for use in production.

All of the imaging modes (Figure 3) developed for C-SAM may be used in the laboratory analysis of components. One mode is Q-BAM, which enables the user to select a vertical plane of interest and perform a nondestructive cross-section through

the component along that line. The acoustic image shows details in the face of the component, as though the component has been sawn in two. Because the process its nondestructive, it can be repeated along as many other straight lines - of any orientation - as the user wishes. Q-BAM is sometimes followed by physical sectioning to compare the results. Using the nondestructive and destructive methods in sequence is known as Acoustically Guided Destructive Physical Analysis (AGDPA).

A quick look at some of the other modes:

Acoustic 3-D uses ultrasound to image non-vertical internal interfaces in colors that indicate each feature's depth.

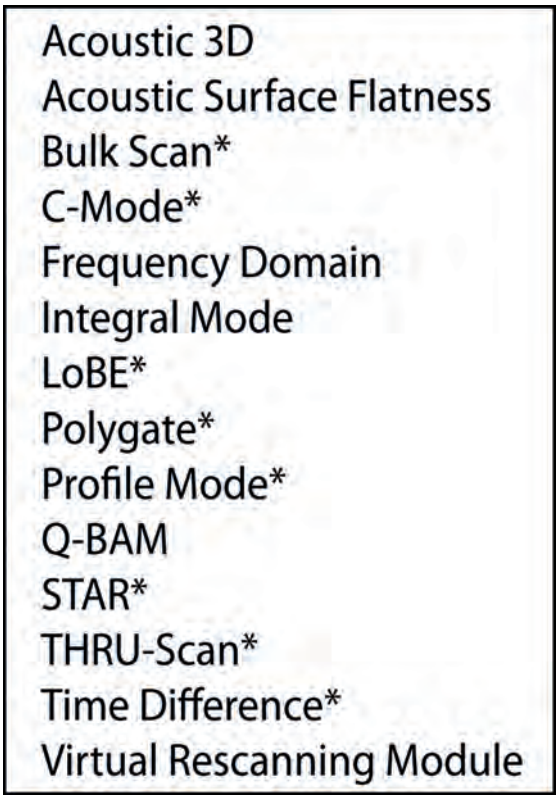
Acoustic Surface Flatness (ASF) uses color to reveal local departures from flatness in, for example, the surface of a BGA package or a 300mm wafer. Frequency Domain displays specific frequencies from the echoes to reveal internal features that are better revealed in this mode than by looking at the total echo amplitude. The echoes may contain a wide range of frequencies, say 75 to 125 MHz but the feature may only show up over a relatively brief frequency range - 93 MHz to 98 MHz, for example.

PolyGate lets the user create, during a single scan, multiple images, each of a specific vertical range. The result may be, for example, a sequence of 20 images each showing one of the 20 slices into which the returning echoes were divided.

THRU-Scan uses two transducers, one on top of the component and one beneath it. Each is coupled to the component surface by water. A C-shaped mount keeps both at the same x-y position at all times. The top transducer fires a pulse, but ignores echoes reaching it from all depths. A portion of the pulse passes through the back wall and is collected by the transducer below. No ultrasound passes through air gaps such as voids and delaminations, so these defects appear in the acoustic image as solidly black features.

STAR stands for "Simultaneous Transmission and Reflection Mode," in which images are made from echoes returning (reflected) from internal interfaces and from energy that has passed through the component and has been detected by the receiving transducer underneath.

VRM means "Virtual Rescan Mode," and permits re-imaging of a component that is no longer available to image because, for example, it may have been destroyed or lost. This could be important for establishing the root cause of a component failure that passed a screening test but failed anyway due to a previously unanticipated defect. The VRM mode records raw echo data from throughout the thickness of the sample and creates a matrix data file. If an FA engineer wants to rescreen the part acoustically using different modes of analysis the matrix file is rescreened instead of the missing component. In recent years some imaging modes that were once used only for analytical work have been adapted for use in screening. These modes are marked by an asterisk in Figure 3.



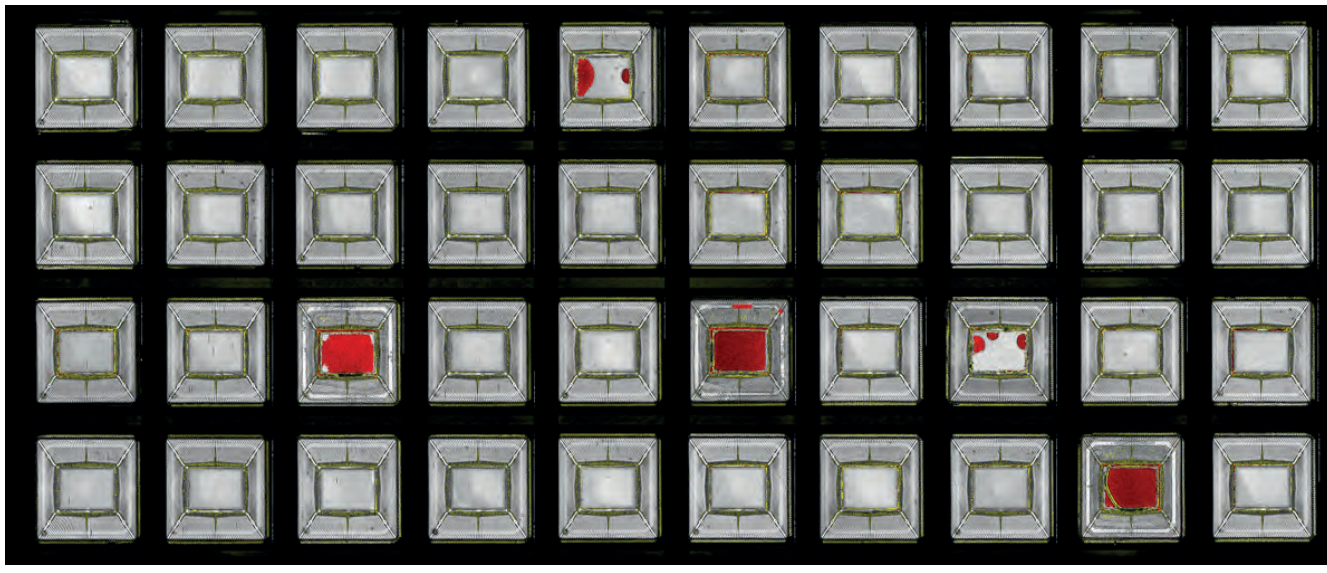
➤ Figure 3. Why ultrasound sees so much: the 14 acoustic imaging modes.

High-Throughput Screening

When the laboratory completes its detailed analysis of the chips that experienced similar failures, enough data has been collected to write the procedure for high-throughput acoustic screening of large numbers of a single component or component type.

The specific locations of known defects within the chip, and the most revealing parameters, are shared with all of the company's locations where this chip is being used in assembly. Some defects are elusive. The details of the optimum imaging method will be shared by the laboratory with the firm's assembly locations, which may be worldwide. This requires that each AMI tool be capable of achieving precisely the same image from the same component. Nordson Test & Inspection SONOSCAN makes this possible by supplying multiple matched tools that are in fact operational twins, triplets, etc., even if a component requires imaging using parameters that differ substantially from the usual menu. AMI tools with different operators speaking different languages and on different continents will produce precisely the same image from a single component.

Screening can take place both before and after components are mounted on a board. The purpose of screening is to identify and remove those components that possess internal features that the laboratory



➤ Figure 4. Acoustic screening image of a tray of plastic-packaged ICs.

has identified as anomalies that could generate field failures.

The result is a demanding environment. The components, which are already in trays used in the manufacturing process, are scanned by Nordson Test & Inspection SONOSCAN FastLine® high-throughput AMI tools. If there is more than one depth of interest, or if anomalies are suspected that may not all be imageable by the same means, then echoes from multiple gates are collected during the same scan. The screening tools must be highly automated in order to characterize thousands of components quickly.

The transducers must be able to focus automatically. They must be able to image in a dozen or more modes and must be able to use precisely the same parameters - imaging mode, frequency, amplitude, and depth range. They must be able to capture returning echoes within the same sub-millionths-of-a-second time period. And they must avoid permitting any residue or contamination to reach components being imaged. Even the analysis of the images to select which components must be scrapped is automated.

The acoustic frequency used is designed to give maximum resolution at the desired depths within the component. The frequency of ultrasound being pulsed into the components may range from 10 MHz (low resolution, but deep penetration) to 300 MHz (high resolution, but less penetration).

Because the laboratory's analytical work has identified the most likely locations where a given defect may occur, scanning may be simplified by using only those echoes arriving at the transducer within a specific time span. The time span defines the "gate," the vertical depth within which defects are most frequent. For example, if the most frequent depth for defects is at the interface between the die face and the encapsulant, it may not be judged necessary to process echoes from other depths in this component.

Figure 4 is the AMI 30 MHz reflection mode image of a tray filled with components. They were screened because the laboratory had found that similar defects in components caused failures during testing. The images were made with the SONOSCAN FastLine tool from Nordson Test & Inspection.

This image is one of several made during a single scan of the tray. Several gates were set, and echoes originating between two gates would be used to make a single image for that very thin horizontal slice of the component. This image was made from echoes originating at the interface between the mold compound and the top of the silicon die. This image's gate was set from just above the mold compound to die interface to just below that interface. Red was selected as the color to identify pixels at a solid-to-air interface.

The red defects are air-filled delaminations - flat air bubbles. In this location thermal excursions during use may cause them to move upward and downward, actions which may result in breaking wires attached to the die or in cracking the die itself. The result in either case is electrical failure.

Laboratory analysis can use any of the 14 imaging modes. There has been a gradual trend over the years of modes from the laboratory being modified for use in screening environments - PolyGate is one example. But some imaging modes are simply too time-consuming and data intensive for high-speed screening. Examples are Q-BAM nondestructive cross-sectioning and three-dimensional acoustic imaging.

Together, the laboratory C-SAM and the production floor FastLine find risky components before they can blossom into field failures. The key is the variety of imaging modes that can report many different data forms from diverse types of internal structural anomalies. The benefactors are end users whose electronic devices, vehicles, computers, telephones, appliances and tools fail to break down.

Four ways to properly purify the gases that power today's technologies

Precise and reliable gas delivery is a critical part of semiconductor manufacturing. And with the increased costs of manufacturing semiconductors – as well as the recent shortage that's affecting many industries around the world – there isn't a moment to waste on compromised gas purity.

BY APPLIED ENERGY SYSTEMS

DURING THE COMPLEX and delicate semiconductor manufacturing process, multiple gases in varying flow rates are carefully delivered to process chambers in order to produce critical features on silicon wafers that are used in manufacturing chips for a variety of uses. To support today's complex applications, these gases must not only be delivered in precise quantities and with repeatability, but also with strict purity levels.

As semiconductor technology continues to undergo an evolution of its own, adhering to stringent requirements for precise and pure gas delivery has never been more important. Even a trace level of contamination can render a chip useless – a significant issue with a multitude of direct and indirect costs. In the past few years, research and design costs for the development of a chip have increased from about $28 million at the 65 nanometer (nm) node to about $540 million at the leading-edge 5 nm node. And fab construction costs for the same nodes have increased from $400 million to $5.4 billion, according to McKinsey.

The importance of gas purity

For fabs, where the quality of gas used in a process is intrinsically tied to yield, the gas purifier is an integral part of the equipment landscape. If gases introduce contaminates during production, there can be severe ramifications for process quality and system integrity.

Gas contamination can, unfortunately, happen to any company. In July, Taiwan Semiconductor Manufacturing Co.'s Fab 18 plant – its most important plant for manufacturing Apple processors – was affected by a contamination of gas used in the chipmaking process. The company announced that several TSMC production lines in the South Taiwan Science Park received gases from suppliers that were at risk of contamination. These were quickly replaced with other gas supplies to mitigate impact on production. TSMC said it is carrying out stringent follow-up operations to ensure that there will be no quality issues. Choosing the right gas supplier and purifier is critical to avoiding a situation like this.

Selecting the right purifier for your high and ultra high purity applications is shaped by various specifications, like gas type, impurity, pressure, and flow rate. Let's explore four ways you can ensure your gas is pure and that you are utilizing the right kind of purifier for your unique applications.

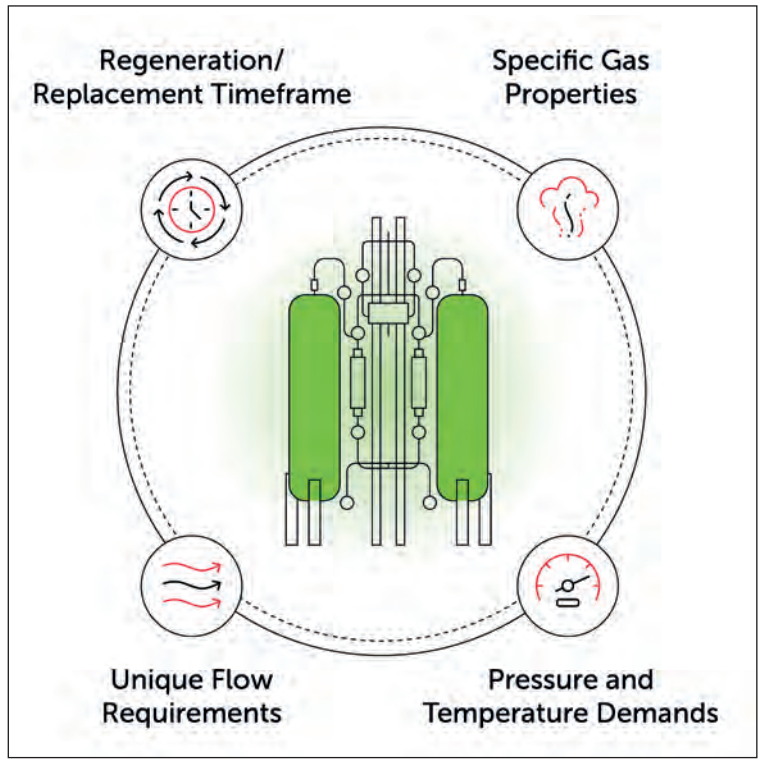
- **Determine the properties of each specific process gas involved**
  At its core, a gas purifier's role is to remove trace impurities from process gases to ensure contaminates do not impact production. Doing so requires gas purification technology that can remove impurities down to the parts per billion (PPB), or parts per trillion (PPT) level. Different

gases have different properties – with some that are highly flammable, hazardous, or toxic. Common process gases include NH_3, CO_2, H_2, SiH4, HBr, Cl2, BCl3, DCS, and PH3, and there's also a wide range of other gas types that can be used, including purge, passivation, and fluorinated gases. The ideal purifier solution is designed with the properties of each specific process gas in mind, accounting for factors that may impact the stability of gases during production. Applied Energy Systems' ARM Purification division delivers a versatile range of high and ultra high purity grade gas purifiers that reliably uphold mission-critical gas delivery requirements across applications, from the smallest point-of-use vessel to the most complex bulk system.

- **Optimize the purifier for your unique flow requirements**
  Pairing a gas purifier optimized for one flow rate with an application that demands another level of gas flow can result in subpar purification and compromise process safety. Your purifier solution should be tailored to your unique flow rate requirements in order to achieve the standards for purification, performance, and safety that your application demands. Once a fab has identified the volume of gas required, the next step is to consider the type of purifier – point of-use, micro-bulk, or bulk. Each purifier can be used in isolation or in a series with others based on gas stream, level of impurity, and outlet purity required. For example, bulk purifiers operate at the ultra high purity level, making them ideal for UHP applications like semiconductor fabrication. ARM Purifications' Bulk Purifiers offer large flow rates and are designed to meet the specific requirements of a multitude of gas delivery systems.

- **Ensure the purifier meets your pressure and temperature demands**
  You should be aware of your application's precise pressure and temperature demands as both impact your purifier selection. Pressure varies by gas type and process application. Additionally, requirements for use at elevated temperatures vary based on gas type, targeted impurity, and function. The right purifier solution should be tailored to the specific pressure and temperature requirements dictated by your application. In addition to ARM Purification's purifiers, which handle standard pressure requirements, ARM Purification works with customers to develop solutions for various temperature-driven and high pressure applications.

- **Note when to refurbish and revitalize gas purifiers at end-of-life**
  Gas purifiers don't last forever, as they are designed and specified for continuous operation and eventually reach end-of-life. Luckily, many gas purifiers can be refurbished, revitalized, and redeployed into existing systems, maximizing return on investment over the long run. But while aged purifiers may represent an opportunity for restoration, the latest advancements may offer greater efficacy from a net-new component. ARM Purification understands the need to maximize your investment while optimizing your equipment. It can assess your system and component health and provide recommendations for replacement or servicing. If needed, ARM Purification can refurbish older gas purifiers while adding new features to them that enhance future functionality – ultimately preventing investments from becoming obsolete.



➤ There are four key areas to consider in order to ensure you're using the right purifier for your unique applications.

Position your fab for success with the right purifier

Today's semiconductor fabs cannot afford for impure gases to disrupt their intense manufacturing operations. Choosing the right purifier for your needs is not only important – but it's absolutely critical in today's demanding and complex tech climate.

Gas purifiers are central to fabs' abilities to improve yield, ensure process integrity, and power innovation. ARM Purification recognizes that a gas purifier is more than just an isolated component – it has the ability to make or break your most delicate production processes. ARM Purification is a division of Applied Energy Systems that delivers a full range of point-of-use, micro-bulk, and bulk purifier solutions for high and ultra high purity applications. Its proven purifiers have been trusted by the world's innovators to uphold the most stringent purity requirements for more than two decades.

To learn more about how the right gas purifier can enable your semiconductor fab to meet today's rigorous industry demands, visit:
https://www.armpurification.com

ULVAC ENVIRO™ plasma ashing systems

With over 40 years of ashing experience, Ulvac has ENVIRO plasma ashing tools for R&D, pilot production and high-volume manufacturing.

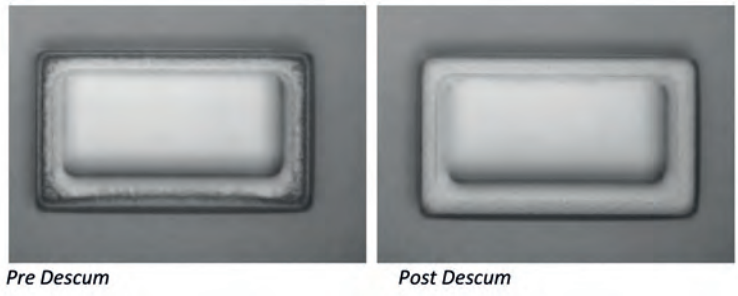
THE ENVIRO-1Xa photoresist removal equipment from ULVAC, offers superior performance at an exceptional price. The system is equipped with a versatile platform that can handle multiple wafer sizes, ranging from 100 to 200 mm in diameter. The system utilizes a high efficiency downstream plasma source and can achieve ash rates >10μm/min, with a throughput of 70+wph. This is all achieved on a minimal footprint of 1.57m². It offers high process flexibility that is required for demanding processes, such as: high-dose implanted resist removal, descum and surface modification, SU-8 and fluorinated resist removal, and MEMS sacrificial-layer removal.

ENVIRO -- High Speed Plasma Ashing Systems

- ENVIRO-1Xa – Single Chamber
- ENVIRO-1Xa 2C – Two Chambers
- ENVIRO-Optima – Three Chambers

ENVIRO™ features common process chambers mated to high-speed wafer handlers for R&D, pilot production and high-volume manufacturing; including thin wafer handling.

Post Deep Silicon Etch Resist Removal



Pre Descum *Post Descum*

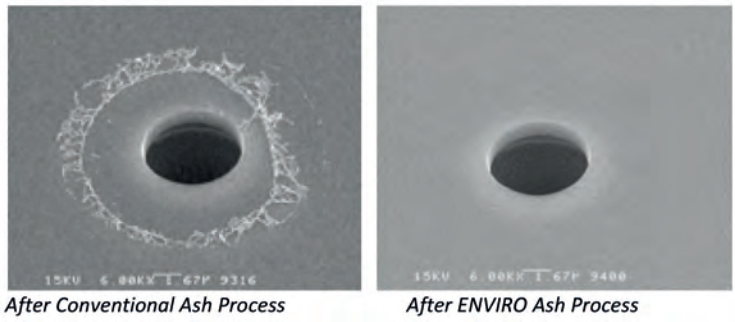
ENVIRO offers the flexibility for multiple applications, including:

- Descum
- Thick resist strip (including: SU-8, KMPR, silanated)
- Polymer and residue removal
- MEMS Release (organic sacrificial layer removal)
- Backside clean (bevel/edge)

ENVIRO offers a wide process operating range:

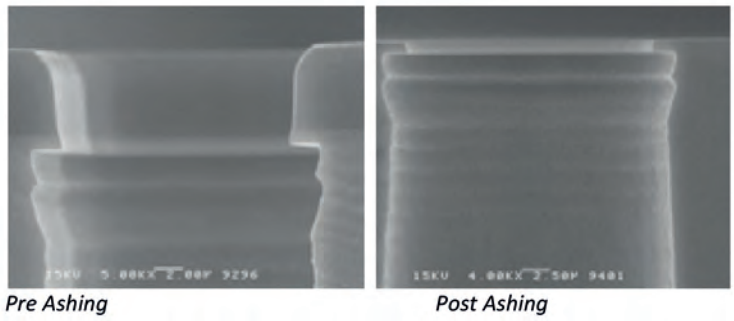
- Ashing Rate – Several nm/min to more than 10um/min
- Wide range of stage temperature control (hot plate or optional cold plate)
- High efficiency downstream plasma source
- Up to 4 MFC's, 2 standard, 2 optional
- Gas chemistries: various, including halogen bearing

Post Process Residue Removal



After Conventional Ash Process *After ENVIRO Ash Process*

MEMS Device Descum



Pre Ashing *Post Ashing*

About ULVAC Europe

ULVAC GmbH was established in 1987 as the European subsidiary of ULVAC, Inc. Headquartered in Munich, Germany. From Munich, our sales and service team serve the EMEA region. ULVAC provides a very broad portfolio of manufacturing equipment for the vacuum, materials, and thin film industries. ULVAC's solutions diversely incorporate equipment, materials, analysis, and services for semiconductors, MEMS, flat panel displays, electronic components, PCB, TFB and other vacuum equipment.

ULVAC offers state-of-art products and technologies for semiconductor and related processes. To support MEMS, power devices, and NVM fabrication, ULVAC offers equipment for sputtering, evaporation, plasma etch, ashing, ion implanting, oxidation/POA/nitridization, and activation annealing for both R&D, pilot line, as well as high volume manufacturing. A complete line of vacuum components is also offered which includes vacuum pumps of all types, helium leak detectors, UHV systems and gauges, RGA's and thermal analysis instrumentation.

At ULVAC we pursue leadership in vacuum technology to realize innovation for our customers.

Contact ULVAC today, and discover how we can work for you.
Visit: **www.ulvac.eu** or contact us at: **ulvac@ulvac.de.**

Semiconductor solutions from Pfeiffer Vacuum

Semiconductor fabrication takes place under clean-room conditions in the high and ultra-high vacuum range. To ensure that these conditions are met, reliable vacuum equipment is a must.

A TYPICAL semiconductor fab consists of four levels. At the top level, the cleanroom, the production line as well as special systems for contamination management are located. The level below the cleanroom – the so-called "subfloor" – is where the dry pumps for the evacuation of load-locks and transfer chambers are located. The next level below is where the cooling units, current supplies and RF-generators of the plant are located. The lowest level contains dry pumps and the exhaust gas treatment (abatement) equipment.

➤ The ASM 392 is the perfect leak detection solution adapted to the semiconductor and display industries as well as other demanding applications where rapid pump down and high sensitivity is key. It is fully Semi S2 compliant.

Explore our solutions for semiconductor fabs – in 3D and from a 360° perspective! Click through the different floors and components of our semiconductor fab model and learn which products Pfeiffer Vacuum offers to fulfill the diverse requirements!
https://www.pfeiffer-vacuum.com/en/solutions/vacuum-experience/semiconductor-fab-3d/

Deposition

Manufacturing of a semiconductor component is a very complex process, involving many steps under vacuum. The deposition process is one of them and consists of depositing a material on the wafer through several technologies: PVD (Physical Vapor Deposition), PECVD (Plasma Enhanced Chemical Vapor Deposition), SACVD (Sub-Atmospheric Chemical Vapor Deposition), LPCVD (Low Pressure Chemical Vapor Deposition) or more recently ALD (Atomic Layer Deposition). Each technology requires a different level of vacuum. We provide high vacuum turbopumps and primary dry pumps solutions dedicated to your deposition applications and designed for the lowest cost of ownership and highest process lifetime.

Applications

- PVD (Physical Vapor Deposition)
- PECVD, SACVD
- Diffusion, LPCVD
- ALD (Atomic Layer Deposition)

Etch & Clean

Manufacturing of a semiconductor component is a very complex process, involving many steps under vacuum. Dry etch process is one of them and consists of selectively removing a material on the wafer. This material can either be a conductor material, shaping the structure of the semiconductor component, or a dielectric material, insulating the conducting parts of the component. Strip & Clean processes are also used to remove selective materials from wafer surface, such

as photoresist film and residues that could impact the device performance. Each technology requires a different level of vacuum. We provide high vacuum turbopumps and primary dry pumps solutions dedicated to Etch & Clean applications and designed for the lowest cost of ownership and highest process lifetime.

Applications
- Dry Stripping & Cleaning
- Dielectric Etch
- Conductor & Polysilicon Etch
- ALE

Ion implantation

Manufacturing of a semiconductor component is a very complex process involving many steps under vacuum. Among them, ion implantation process consists of doping the silicon wafer surface with ions, to change the electrical characteristics of the material and increase device conductivity. Regardless of implanter technologies (medium current, high current or high energy), implanter tools layout includes three main vacuum areas: Ion source, beamline and end station. We provide high vacuum turbopumps and primary dry pumps solutions for all implant applications and are designed for the lowest cost of ownership and highest process lifetime.

Applications
- Source, beamline & end-station

Wafer handling

Manufacturing of a semiconductor component is a very complex process, involving many steps under vacuum environment. Wafers enter or exit a semiconductor tool through load-lock chambers to ensure the right vacuum level. Wafers are moved from process chamber A to B through transfer modules, which are also maintained under vacuum. We provide high vacuum turbopumps and primary dry pumps solutions dedicated to wafer handling applications and designed for the highest throughput and lowest operating costs.

Applications
- Load lock & transfer

Inspection & Metrology

As semiconductor device manufacturing become more and more complex with increased number of steps, wafer inspection and metrology are more critical than ever. Besides vacuum solutions for traditional inspection & metrology tools, we provide innovative in-line Airborne Molecular Contamination (AMC) systems for Front Opening Universal Pods (FOUP) and clean room environment analysis. With our AMC systems, wafers are analyzed through the production cycle, contributing to increase manufacturing yield.

Applications
- CD SEM
- AMC and particles monitoring in FOUP
- AMC monitoring in clean room

➤ The A3004 XN dry process pumps are made to meet the requirements of most corrosive processes. Innovative technologies reduce maintenance frequency and increases pumping lifetime.

Lithography

Manufacturing of a semiconductor component is a very complex process. Photolithography process is one of them and consists of defining and transferring patterns in each layer of the device. As chip node dimensions continuously shrink, traditional photolithography using Ultra Violet (UV) light has reached its limits. A new lithography process using Extreme Ultra Violet light (EUV) under vacuum has emerged. We provide high vacuum turbopumps and primary dry pumps solutions dedicated to EUV application, supporting advanced chip scaling below 10 nm node.

Applications
- EUV (Extreme Ultra Violet) lithography

Facilities & Maintenance

Any single leak present on a semiconductor tool and its related facilities can impact manufacturing throughput and yield. Consequences vary from loss of production due to process specs not met, to critical safety hazard. Therefore, leak detection is a critical and mandatory step of any new tool commissioning in the clean room or after any maintenance intervention. At the basement level, forelines & dry pumps are also regularly exchanged for cleaning or repair. We provide comprehensive leak detection solutions which guarantee vacuum integrity of your installation from process chambers down to gas abatement. Our goal: Maximize your production yield.

Applications
- Leak Detection

Pfeiffer Vacuum
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Semiconductor (Silicon/Compound)
Publications include: Compound Semiconductor, Silicon Semiconductor, CS China, SiS China

Power Electronics
Publications include: Power Electronics World

Future Mobility
Publications include: TaaS Technology, TaaS News

Data Centres
Publications include: DCS Europe, DCS UK, SNS International

SmartSolar UK & Ireland
Publications include: Solar and Power Management, Solar UK and Ireland

Sensors
Publications include: Sensor Solutions Magazine, Sensor Solutions International

Digitalisation
Publications include: Digitalisation World, Information Security Solutions, Managed Services

Photonics
Publications include: PIC Magazine, PIC Conference

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Dedicated technical and time-served experts/editors

MARK ANDREWS
Mark Andrews is technical editor of Silicon Semiconductor, PIC Magazine, Solar+Power Management, and Power Electronics World. His experience focuses on RF and photonic solutions for infrastructure, mobile device, aerospace, aviation and defence industries

PHIL ALSOP
Journalist and editor in the business to business publishing sector for more than 30 years currently focusing on intelligent automation, DevOps, Big Data and analytics, alongside the IT staples of computing, networks and storage

JACKIE CANNON
Director of Solar/IC Publishing, with over 15 years experience of Solar, Silicon and Power Electronics, Jackie can help moderate your webinar, field questions and make the overal experience very professional

DR RICHARD STEVENSON
Dr Richard Stevenson is a seasoned science and technology journalist with valuable experience in industry and academia. For almost a decade, he has been the editor of Compound Semiconductor magazine, as well as the programme manager for the CS International Conference

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ETCH

GAS DELIVERY SYSTEMS

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FLOW MEASUREMENT

GAS PURIFIERS

MATERIALS

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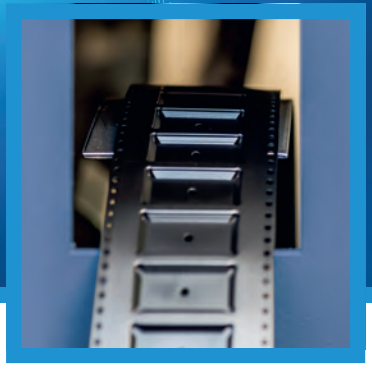
CARRIER TAPE ON-DEMAND

The new normal in semi-packing



Produce component carrier tape in-house as and when you need it, removing the need to store pre-formed reels. *Re-flex II* produces both standard and custom tape pockets either directly on to a tape and reel system in-line "On-Demand" or output to reel.

Best of all, the reduction in tape cost returns your investment within months, and ensures control over your own carrier tape supply and pocket quality.

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