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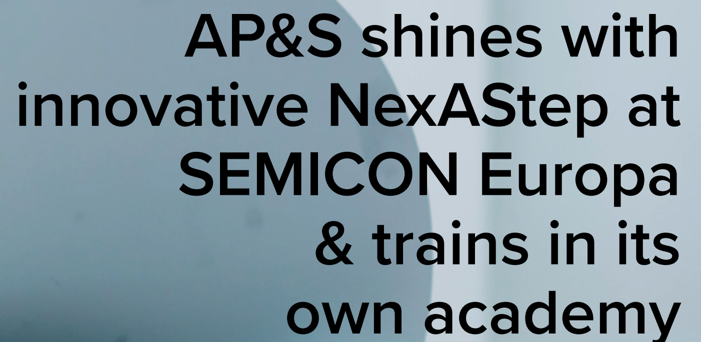

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Semiconductor ecosystems are on the cusp of significant changes in packaging technology

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VIEWPOINT

By Phil Alsop, Editor

Once again, the three Ss grab the headlines

I MAKE NO APOLOGIES for returning to the theme of my comment in the previous issue of Silicon Semiconductor. Sustainability, skills and the supply chain continue to dominate the news. However, there is one addition to be made to this list, and that's a very big I – an I which, to be fair, has always been at the forefront of the industry. I for Innovation.

In no particular order, the news stories that have caught my attention in recent weeks include: Infineon heading up the EECONE European research project for advancing the circular economy and sustainability of the electronics industry; the Semiconductor PFAS Consortium publishing its tenth and final white paper on the uses of PFAS in the semiconductor industry; The 2023 Dr. Lisa Su Woman of Innovation Award being given to Rani Borkar, Corporate Vice President for Azure Hardware Systems and Infrastructure at Microsoft; TSMC revealing a 'breakthrough' set to redefine the future of 3D IC; the Volkswagen Group reorganising its procurement of electronic parts and semiconductors to ensure supply over the long term to help secure it a leading position in terms of technology and competitiveness; the formation of Flanders Semiconductors – a new semiconductor hub in the heart of Europe; Vodafone working on new silicon photonic chips; and Intel celebrating the arrival of its Intel 4 technology, which uses extreme ultraviolet (EUV) technology, and the first use of EUV in high-volume manufacturing (HVM) in Europe.

The video interviews I have conducted over the same period confirm the importance of SSSI to the industry – and have also emphasised that two or more of these topics frequently coincide. For example, the water treatment technology companies are working with semiconductor manufacturers to provide innovative

solutions to sustainability issues around the industry's use of water. And, in the case of Volkswagen, the company has gone out and hired semiconductor experts to help it improve the efficiency of its supply chain – with technology innovation being a major focus, alongside sustainability – that's all four SSSI disciplines in one go! While the semiconductor industry is no different than any other in that it must wait and see how governments and industry regulation dictates what changes might need to be made, it is clear that much of the semiconductor supply chain is acting before it is made to do so. It wants to be in control of its future.

Geopolitical events of recent weeks might make this industry self-determination more vulnerable to outside influences than ever before, especially when combined with the environmental 'flip-flopping' that seems to have become a major feature of national politics across the globe. Yet, it is encouraging to see that from the top down, the semiconductor industry is stepping up to the challenges it faces in a positive, proactive manner. 2024 could just be a very exciting year for the industry – for all then right reasons.

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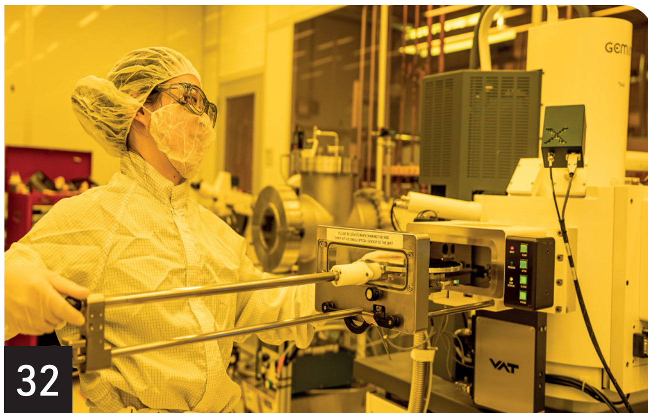

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Infineon coordinates electronics sustainability

Infineon heads European research project for advancing the circular economy and sustainability of the electronics industry.

INFINEON TECHNOLOGIES AG has taken over as head and coordinator of the broad-scope European research project EECONE (European ECOsystem for greeN Electronics), intended to make electronics in Europe more sustainable. The objective is to investigate the corresponding technologies along the entire value chain, from design, manufacture and use all the way to recycling. EECONE is one of the Key Digital Technologies research projects supported by the European Union as a Joint Undertaking. 49 partners are participating in the project, which has a volume of approximately 35 million euros total costs. The project is being funded by the European Union and the national governments of the participating companies with around 20 million euros.

"Electronics are fundamental to improving the sustainability of many applications. But this is not sufficient, electronics themselves have to become greener," says Constanze Hufenbecher, Infineon Management Board member and Chief Digital Transformation Officer. "Infineon is pleased to take on the lead role in the research project EECONE in order to advance the circular economy together with our partners along the value chain. The only way to achieve sustainability from design and use and all the way to recycling is by working together."

EECONE is aligned with the 6R concept (Reduce, Reliability, Repair, Reuse, Refurbish, Recycle); the amount of materials required by electronics is to be reduced, electronics are to be made more reliable, easier to fix and use again, and easier to recondition and to recycle. The project will investigate a total of ten application examples from the widest possible variety of fields in terms of developing green electronics. The applications are from the areas Automotive, Consumer Electronics, Health, Information and Communication Technologies, Aviation and Agriculture. Focus points are for example reducing the amount of material used by making circuit boards thinner or smaller, or improving sustainability by introducing materials which are easier to separate during recycling. Facilitating the replacement of not only circuit boards but also of semiconductors is to make it easier to repair devices. The technologies involved could also make it possible to reuse and recycle electronic components. The project will in addition develop technologies which for example generate and store their own power in IoT devices. New, ecologically friendly materials are to make it easier to recycle lithium-ion batteries.

Artificial Intelligence will be used to prolong the service lives of electronic equipment, while tools for more sustainable electronic design, including comprehensive impact assessments for the use of electronics, are to be developed as well. EECONE also covers the use, dissemination and standardization of electronics and will train specialists in handling electronic refuse.

The EECONE research project has a planned duration of three years. It will establish decisive foundations for the sustainable development, manufacturing and use of electronics in Europe. The on-site inaugural event of the project was held in Toulouse on 20 and 21 September.

The 49 EECONE Research Project Partners

4Mod Technology, Acorde Technologies Sag, Agencia Estatal Consejo superior de Investigaciones cientificas, Aniah SAS, Arcelik A.S., Atea Sverige AG, AT&S - Austria Technologie & Systemtechnik, Centre national de la Recherche scientifique, Charokopeio Panepstimio, Commissariat a l'Energie atomique et aux Energies alternatives, Dassault Systemes, Design and Reuse, EcoDC AG, Fraunhofer Gesellschaft zur Forderung der angewandten Forschung e.V., Get electronique, Infineon Technologies AG, Institut mikroelektronickych Aplikaci SRO, Institut polytechnique de Grenoble, Interactive fully electrical Vehicles SRL, Interuniversitair Microelectronica Centrum, Leonardo - Societa per Azioni, Luna Geber Engineering SRL, Melsen Tech A/S, Nerosubianco SRL, Orbotech Ltd., Ozyegin Universitesi, Premo, S.L., Research Institutes of Sweden AB, Robert Bosch GmbH, Siec Badawcza Lukasiewecz - Instytut Mikroelektronik i Fotoniki, Silicon Austria Labs GmbH, Smartsol SIA, Soitec SA, STMicroelectronics SAS, Synano BV, Technicka Univerzita v Liberci, Technische Hochschule Deggendorf, Tecnologias Servicios telematicos y Sistemas SA, Teknologisk Institut, Tetradis, Thales dis France SAS, Università degli Studi di Perugia, Université catholique de Louvain, Université Grenoble Alpes, Ustav teorie informace a Automatzizace AV CR VVI, Vitesco Technologies France, Weeecycling, Associated Partners Centre Suisse d'Electronique et de Microtechnique SA - Recherche et Developpement, Swiss Vault Systems GmbH.

Consortium publishes PFAS white paper

Following 18 months of research, surveys, working group meetings, and technical review, the Semiconductor PFAS Consortium published its tenth and final white paper on the uses of PFAS in the semiconductor industry.

THE PAPERS identify the essential performance attributes of different PFAS chemistries in various applications in the semiconductor manufacturing process and semiconductor manufacturing equipment and infrastructure, as well as the significant technical challenges the industry faces in replacing these substances in these various applications.

The white papers also consider workplace health and safety, in addition to environmental releases and controls.

This series of papers provides policymakers and industry experts a significant body of knowledge and technical data needed to contribute to the formulation of an industry-wide approach regarding the semiconductor industry's use of PFAS, as well as to better inform global, national, and state regulation and legislation. The topics of the 10 white papers are listed below and are available for download on the SIA website.

- Background on Semiconductor Manufacturing and PFAS
- PFAS-Containing Surfactants Used in Semiconductor Manufacturing
- PFOS and PFOA Conversion to Short-Chain PFAS-Containing Materials Used in Semiconductor Manufacturing
- PFAS-Containing Photo-Acid Generators Used in Semiconductor Manufacturing
- PFAS-Containing Fluorochemicals Used in Semiconductor Manufacturing Plasma-Enabled Etch and Deposition
- PFAS-Containing Heat Transfer Fluids Used in Semiconductor Manufacturing
- PFAS-Containing Materials Used in Semiconductor Manufacturing Assembly Test Packaging and Substrate Processes
- PFAS-Containing Wet Chemistries Used in Semiconductor Manufacturing
- PFAS-Containing Lubricants Used in Semiconductor Manufacturing
- PFAS-Containing Articles Used in Semiconductor Manufacturing

The white papers find that a variety of PFAS are used in thousands of essential applications in the semiconductor supply chain, including the complex tools needed to manufacture chips, in numerous process steps in the fab, and in the assembly and packaging process.

In the vast majority of instances, the PFAS chemistries used have unique properties and functionality for which there are no readily available alternatives or "drop-in" substitutes. Developing alternatives will require extensive research and new discoveries, and integrating and qualifying a non-PFAS substance with the necessary performance requirements can take between 5-25 years for use in high-volume manufacturing operations.

While there may eventually be viable alternatives in some cases, full replacement of PFAS-containing materials may not be possible for some of the most exacting applications without a change in the material systems that enabled scalability and reliability in high volume manufacturing.

For ongoing critical uses of PFAS in the industry, substantial work is needed on optimizing and minimizing the use of these substances and capture and abatement of discharges.

The Consortium also published a study on "The Impact of a Potential PFAS Restriction on the Semiconductor Sector," considering the effects of potential restrictions considering the lack of alternatives for these essential uses.

The Consortium now enters its next phase of collaboration, focused on release mapping and model development as well as assessing the industry's management of PFAS and identification of technologies that will minimize uses and releases by following the pollution prevention hierarchy.

GSA celebrates women's innovation

GSA Women's Leadership Initiative announces the Dr. Lisa Su Woman of Innovation Award recipient, Rani Borkar for WISH Conference.

THE GLOBAL SEMICONDUCTOR ALLIANCE (GSA) Women's Leadership Initiative (WLI) announces the recipient of the 2023 Dr. Lisa Su Woman of Innovation Award. This award will be presented at the Women in Semiconductor Hardware, WISH, Conference on October 12, 2023.

The 2023 Dr. Lisa Su Woman of Innovation Award recognizes an industry veteran who has dedicated her career to making exceptional contributions to drive the development, innovation, growth, and long-term opportunities for the semiconductor industry. GSA WLI will proudly present the Woman of Innovation award to Rani Borkar, Corporate Vice President for Azure Hardware Systems and Infrastructure at Microsoft.

"Rani Borkar's distinction as the first-ever recipient of the Dr. Lisa Su Woman of Innovation award perfectly embodies the award's core values, highlighting her outstanding leadership and contributions to our industry," said Jodi Shelton, GSA CEO. "I have had the privilege to work with Rani over the last several years and she has contributed much to the leadership of the GSA and to the GSA's Women's Leadership Initiative. Rani commands respect from her peers both inside Microsoft and in tech ecosystem for her exceptional leadership, technical prowess, and commitment to innovation as well as advocating for women within the industry and beyond."

Rani Borkar is the Corporate Vice President for Azure Hardware Systems and Infrastructure at Microsoft. In her role, Borkar leads the core organizations responsible for planning, architecting, developing, and deploying the hardware and infrastructure for Microsoft's leading cloud computing platform.

Over the last 35 years, Borkar has established herself as a pioneer in the semiconductor industry, a technology

executive, product visionary, and trusted leader. Borkar's leadership has intersected the most seminal platform shifts in the evolution of modern computing: the rise of the PC, the introduction of consumer mobile, the arrival of multi-core processors, and the proliferation of digital transformation via cloud, AI, and quantum computing. During her career at Intel, Borkar led silicon product development strategy for microprocessors that drove evolutionary shifts for the semiconductor industry, including the highly successful Intel Xeon, Atom, Core, Pentium, and Celeron product families. Managing large, complex, and diverse global engineering organizations, Borkar's leadership enabled technological innovation in servers, PCs, mobile phones, tablets, and the Internet of Things that drove major product shifts and transformed consumer behavior.

As the head of Azure Hardware Systems and Infrastructure at Microsoft, Borkar is responsible for the vision, strategy, and architecture of silicon and systems development, cloud supply chain as well as global capacity deployment for Microsoft's cloud data center infrastructure. Her organization develops technologies that empower the world to innovate and drive end-to-end business value for Azure's products and solutions, and today serves more than 95% of the Fortune 500. Leading with the philosophy of "mission first, people always," Borkar has inspired and transformed organizations by building close-knit communities. To produce great technology, Borkar believes in the power of combining technology assets and engineering talent with the values of collaboration, innovation, and risk-taking, thereby empowering teams to innovate and move the industry forward. Leading with the philosophy of "mission first, people always," Borkar has inspired and transformed organizations by building close-knit communities. To produce great technology, Borkar believes in the power of combining technology assets and engineering talent with the values of collaboration, innovation, and risk-taking, thereby empowering teams to innovate and move the industry forward.

Borkar is actively involved in the Global Semiconductor Alliance (GSA), where she serves on its board of directors and on the GSA Women's Leadership Council. She is also on the board of directors of Applied Materials. Borkar previously served as a Trustee and as Chair of the Board of Trustees at Oregon State University to help guide the state's effort to advance economic development and innovation. Borkar earned a bachelor's degree and a master's degree—both in physics – from the University of Mumbai, India. She went on to earn a second master's degree in electrical engineering from the Oregon Graduate Institute. Borkar also holds an Executive Program in Leadership (LEAD) certificate from the Stanford University Graduate School of Business.

"I am humbled and honored to receive the Dr. Lisa Su Award and to be recognized for all that it represents – the dedication, talent, and accomplishments that women have had and continue to have in an industry that drives incredible innovation to change the world for the better," said Borkar. "When we value and recognize the power of workplace diversity, we change what's possible for generations to come, inspire technical women to lead, and build supportive communities that will collectively fuel semiconductor growth," said Rani Borkar.

TSMC reveals 'breakthrough' set to redefine the future of 3D IC

TSMC has announced the new 3Dblox 2.0 open standard and major achievements of its Open Innovation Platform® (OIP) 3DFabric Alliance at the TSMC 2023 OIP Ecosystem Forum.

THE 3Dblox 2.0 features early 3D IC design capability that aims to significantly boost design efficiency, while the 3DFabric Alliance continues to drive memory, substrate, testing, manufacturing, and packaging integration. TSMC continues to push the envelope of 3D IC innovation, making its comprehensive 3D silicon stacking and advanced packaging technologies more accessible to every customer.

"As the industry shifted toward embracing 3D IC and system-level innovation, the need for industry-wide collaboration has become even more essential than it was when we launched OIP 15 years ago," said Dr. L.C. Lu, TSMC fellow and vice president of Design and Technology Platform. "As our sustained collaboration with OIP ecosystem partners continues to flourish, we're enabling customers to harness TSMC's leading process and 3DFabric technologies to reach an entirely new level of performance and power efficiency for the next-generation artificial intelligence (AI), high-performance computing (HPC), and mobile applications."

Introduced last year, the 3Dblox open standard aims to modularize and streamline 3D IC design solutions for the semiconductor industry. With contribution from the largest ecosystem of companies, 3Dblox has emerged as a critical design enabler of future 3D IC advancement.

The new 3Dblox 2.0 enables 3D architecture exploration with an innovative early design solution for power and thermal feasibility studies. The designer can now, for the first time in the industry, put together power domain specifications and 3D physical constructs in a holistic environment and simulate power and thermal for the whole 3D system. 3Dblox 2.0 also supports chiplet design reuse features such as chiplet mirroring to further improve design productivity. 3Dblox 2.0 has won support from key EDA partners to develop design solutions that fully support all TSMC 3DFabric offerings. Those comprehensive design solutions provide designers with key insights to make early design decisions, accelerating design turnaround time from architecture to final implementation.

TSMC has also launched the 3Dblox Committee, organized as an independent standard group, with the goal to create an industry-wide specification that enables system design with chiplets from any vendors. Working with key members including Ansys, Cadence, Siemens, and Synopsys, the committee has ten technical groups of different subjects and proposes enhancements to the specs and maintain the interoperability of EDA tools. Designers can now download the latest 3Dblox specifications from the 3dblox.org website and find more information about 3Dblox and its tool implementation by EDA partners.

As the first of its kind in the semiconductor industry, TSMC's 3DFabric Alliance has grown tremendously over the past year, working toward the goal of providing customers with a full spectrum of proven solutions and services for semiconductor design, memory modules, substrate technology, testing, manufacturing, and packaging. Now the Company has 21 3DFabric Alliance partners across the industry to collaborate and innovate with.

Memory Collaboration: Generative AI and large language model-related applications require more SRAM memory and higher DRAM memory bandwidth. To meet this requirement, TSMC has worked closely with its key memory partners including Micron, Samsung Memory, and SK hynix to drive rapid growth on HBM3 and HBM3e to advance generative AI systems by delivering more memory capacity.

Substrate Collaboration: TSMC has worked successfully with substrate partners IBIDEN and UMTC to define a Substrate Design Tech file to facilitate substrate auto-routing for significant efficiency and productivity gains.

The Company initiated a three-way collaboration with substrate and EDA partners with the goal to deliver 10x productivity gains from automatic substrate routing. The collaboration also includes design for manufacturing (DFM) enhancement rules to reduce stress hotspot in substrate design.

Testing Collaboration: TSMC is collaborating with automatic test equipment (ATE) partners Advantest and Teradyne to solve a variety of 3D test challenges to reduce any yield loss and improve power delivery efficiency for chiplet testing. To demonstrate high-speed test access for 3D stack testing through functional interface, TSMC is working with Synopsys and ATE partners on a silicon demonstrator to achieve the goal of 10x testing productivity boost. The Company is also working with all design-for-test (DFT) EDA partners to ensure effective and efficient interface testing.

Volkswagen Group reorganizes semiconductor procurement

The Volkswagen Group is reorganizing its procurement of electronic parts and semiconductors to ensure supply over the long term and, in doing so, securing itself a leading position in terms of technology as well as competitiveness.

TO THIS END, the Group has developed a new strategy for the procurement of parts with electronic components. "A high degree of transparency in the semiconductor value chain – the exact knowledge of the parts used – enables us to better determine the global demand and availability of these components. This is underscored by risk management which, in future, will extend to the level of individual electronic parts and help us detect bottlenecks early on and avoid them. For strategically important semiconductors and even the Group's own planned developments in the future, we will rely on direct purchasing from the semiconductor manufacturers," said Dirk Große-Loheide, Board Member for Procurement of Volkswagen Passenger Cars and member of Group management.

In the past, electronic components like control units were procured and the Tier 1 suppliers were largely free to decide which parts they used. Going forward, in close collaboration and partnership with Tier 1 suppliers, Group procurement will define which semiconductors and other electronic parts are to be used.

"Additionally, this is done across all brands by the Semiconductor Sourcing Committee (SSC) established especially for this purpose, with representatives from the procurement and development departments of the brands as well as from Volkswagen Group Components and CARIAD. Furthermore, the transparency regarding semiconductors means that technical alternatives can be identified and implemented more quickly in the event of bottlenecks. Another positive effect is that a reduction in the diversity of variants in the hardware results in a lower degree of software complexity," said Karsten Schnake, Board Member for Procurement at Škoda Auto and head of the cross-brand and cross-functional task force COMPASS (Cross Operational Management Parts & Supply Security), explaining the advantages.

Semiconductors are indispensable in the automotive industry: not only are they elementary for mass production, but they are also innovation drivers and key for launching new products on the market.

The greatest increase in demand for semiconductors is the result of the increasing electrification of vehicles and the trend towards the growing use of assistant functions through to fully autonomous driving. The corresponding innovations will also result in the use of cutting-edge semiconductors, while the demand for more common semiconductors will remain or even rise further. Vehicle innovations are heavily characterised by the use of semiconductors: in 1978, only eight semiconductors were installed in a control unit of a Porsche 911. Today, a Škoda Enyaq has around 90 control units with some 8,000 electronic components.

This development also has an impact on the value of electronic components in the vehicle, the value of which will more than double by the year 2030 from today's average of around 600 euros per vehicle. According to the Group's assessment and corresponding analyzes, the importance of the automotive sector as a customer of the semiconductor industry is also increasing. Today, the automotive industry is in 5th place among the major buyers with a global procurement volume for semiconductors of around 47 billion US dollars.

By 2030, our industry is expected to secure third place with a market volume of around 147 billion US dollars.

The after-effects of the COVID-19 pandemic and the associated chip crisis can still be felt. To solve these enormous challenges and ensure the semiconductor supply, the Volkswagen Group launched the COMPASS initiative at the beginning of 2022, initially with the operational focus of safeguarding the vehicle programme. Strategic action areas were identified on the basis of lessons learned during the semiconductor crisis and solutions were developed and implemented for the long term. (For more details see the article on Page 28).

Flanders Semiconductors - a new hub in Europe

A group of semiconductor companies in Flanders have come together to create Flanders Semiconductors, a new nonprofit organization representing the interests of the industry at local, European, and global levels.

THE ORGANIZATION is open to all qualifying companies, both in and outside of the Flanders region, that have semiconductor technology at the core of their business.

Flanders Semiconductors is a significant move for the Flemish semiconductor industry, which currently employs well over 3,000 people directly, has more than 50 companies with semiconductor as their core business, and over 100 companies defining, testing, and integrating advanced customized semiconductor devices or technologies. Flanders Semiconductors covers the whole supply chain, including infrastructure, equipment, materials, processing, testing, and devices. The Flanders region also boasts world-class research facilities such as IMEC, universities, and institutes providing semiconductor R&D, education, and training. The objectives of Flanders Semiconductors are to increase the talent pool, share industry roadmaps, maintain a yearly business events calendar, and represent members' interests at international levels.

The organization will also market the region and its members internationally, to promote cooperation between members and to cooperate with similar organizations in Europe.

Flanders Semiconductors is led by President Lou Hermans, who has over three decades of industry expertise, along with a team of seasoned semiconductor professionals. Together with the dedicated management team, their mission is to foster collaboration, drive innovation, and catalyze growth within the semiconductor ecosystem, both in Flanders and on a global scale.

"We are thrilled to officially announce the launch of Flanders Semiconductors, poised to be(come) another important European hub for semiconductor innovation, said Lou Hermans, President of Flanders Semiconductors.

"Our founding members, including BelGan, Caeleste, Cochlear, easics, ICsense, NXP, Pharrowtech, Sofics, and Spectricity, have united to create a platform that champions the semiconductor industry's interests at every level. I am deeply inspired and motivated by the drive, support, remarkable power and unity of the founding members. Our diverse community of present and future member companies, each bringing their unique solutions to the semiconductor industry, exemplifies the immense strength and boundless potential that collaboration holds."

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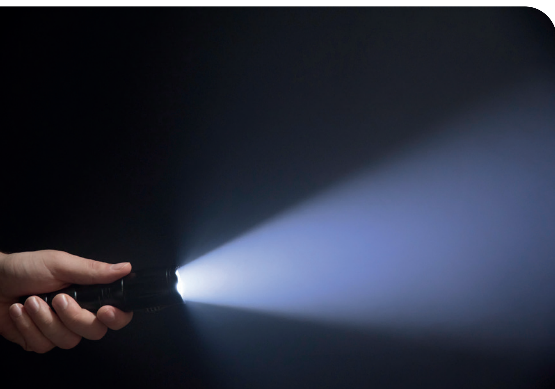
Vodafone shines light on new silicon photonic chips

Vodafone's engineers at its R&D centre in Málaga, Spain, are exploring the potential for new silicon photonic chips to become the hardware of choice to drive the customer-focussed mobile networks of the future.

THE NEWS THAT Vodafone is exploring this new technology comes as the company recently expanded its purpose-built campus in Málaga to house the more than 430 highly skilled engineers made up of over 30 nationalities already working there, along with the further 170 expected to join by 2025. In addition to advancements in silicon chip architecture, Málaga is home to Vodafone's pioneering work in edge computing, IoT and network APIs, among other disruptive technologies, all of which support the digital transformation of Europe's public sector and businesses of all sizes.



Far Faster Chips

Silicon photonic chips promise to be far faster, more efficient, and reliable than today's electronic equivalent found in most electronic devices, including smartphones and telecommunications infrastructure. They use light instead of electricity to compute mathematical operations and the computation time is measured by how long it takes the light to cross the microchip.

The photonic chips would sit at the heart of Vodafone's mobile base stations, providing an ultra-low latency, highly programmable and greener network. Their integration would support the massive advances in computation seen in new technologies like generative AI, cyber security (including quantum computing), and autonomous vehicles, to name but a few.

Vodafone's engineers can predict the speed of a calculation based on the fact that light can travel seven and half times around the equator within one second, or in a one trillionth of a second (a picosecond) across a chipset. According to the University of Oxford, photonic chips could be three hundred times faster than electronic ones.

Working with Salience Labs and iPronics

Among the first start-ups to collaborate with Vodafone's engineers at the expanded campus are two industry leading photonics companies - UK-based Salience Labs and iPronics, headquartered in Valencia, Spain. They join other vendors that are already working with Vodafone on the advancement of chip architecture to enhance new Open RANs.

Salience Labs and iPronics are assisting Vodafone in testing the latest silicon photonics, which has the potential to process and deliver huge amounts of data faster but still securely, without compromising the customer experience or requiring more masts.

Silicon photonics is becoming increasingly important because the increased demand for processing power from AI computer models requires more efficient and faster computer chips. AI computation alone is doubling around every three and half months, according to Salience Labs, and is outpacing what standard semiconductor technologies have left to offer.

Scaling up 5G

By taking a leading research role in silicon photonics today, Vodafone can ensure that it has the processing power baked into its network to match demand in years to come. It's not only AI; scaling up new 5G features also requires a step-change in processing power at the mobile base station, for example network slicing where a business, hospital or school is given their own fast connection on demand.

Even though most microprocessors have reached their computing limit, hey will more than adequately serve most electronic devices and networks for another 20 years. However, Vodafone is determined to stay ahead of the curve by looking to shape a new paradigm for compute with its partners.

Salience Labs is building silicon photonic solutions to overcome the challenge that the growth in AI presents to the movement of data in a world where traditional semiconductor technology can no longer scale higher to keep pace with innovation.

Vodafone's work with iPronics within the field of radio frequency beamforming – the ability to bend and direct a signal to its intended recipient such as a smartphone user – ensures that all aspects (the antenna and the actual baseband equipment) of a mobile base station are covered.

Driving Innovation in Europe

The just-in-time speed at which these silicon photonic chips make calculations will lead to fewer delays and far less heat generated in the transmission of data versus today's method, which is reliant on slower and heat susceptible electronic capacitors.

By collaborating with vendors such as Salience Labs and iPronics, Vodafone can drive silicon innovation in Europe and strengthen its position in the global market.

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AP&S shines with innovative NexAStep at SEMICON Europa & trains in its own academy

The semiconductor industry has made enormous strides in recent decades and plays a critical role in our modern world. A key component for the production of high-quality semiconductor devices is wet process equipment. These systems have been built by AP&S for 20 years and are essential for cleaning and treating wafers. The latest development from the company is the NexAStep wet bench, which is used for batch processing.

Alexandra Laufer-Müller (Shareholder & CEO)

Tobias Bausch (CMO&CTO)

Christoph Kluge (Managing Director tepcon GmbH)

THE COMPACT SYSTEM DESIGN here represents a fundamental advancement that allows optimal use of the clean room, as the system takes up less space. The efficient arrangement of chemical supply, drains, receiver tanks and control cabinets in the module footprint further reduces space requirements and facilitates access for maintenance and operation. The modular plant design allows the plant to be quickly assembled, disassembled and reconfigured, increasing flexibility in production. This allows companies to quickly adapt to market changes when necessary and scale the plant to expand production capacity if necessary.

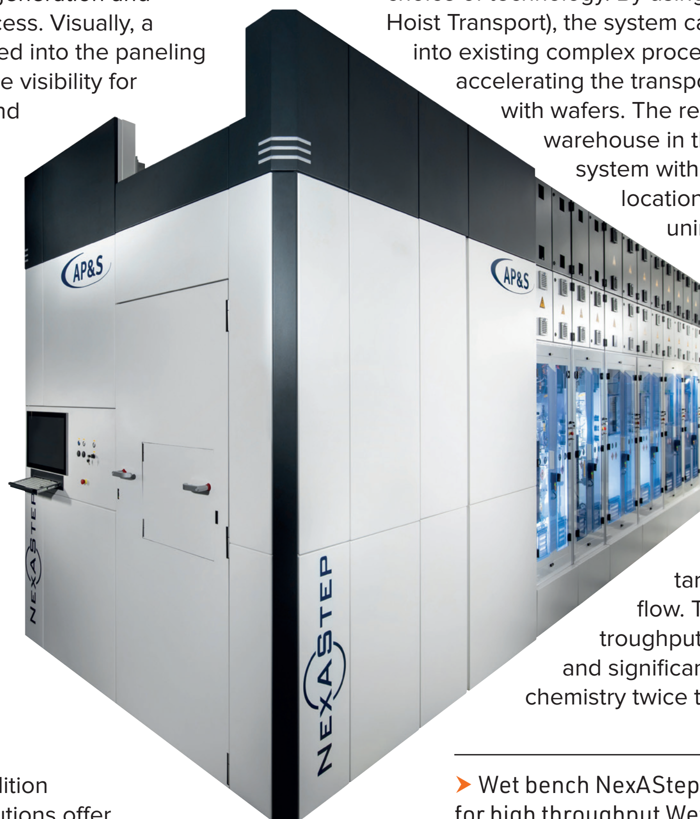
An integrated axis at the front of the NexAStep minimizes particle generation and simplifies direct access. Visually, a signal light integrated into the paneling provides 180-degree visibility for improved access and safety.

With its sister company tepcon GmbH, AP&S has a software company at its side that, among other things, assisted in the implementation of a user-friendly intuitive HMI. The simplified operation of the system, optimized monitoring and efficient control were the main focus here. This ensures efficient process control.

"In the area of condition monitoring, our solutions offer configurable visualization of real-time data in tables, graphs or flowcharts, monitoring of limit values and very timely alarming via email, SMS or WhatsApp. The customer can intervene flexibly at any time and from anywhere via his mobile device. Machine failures can be avoided in real time. The analysis of process data enables the recording and tracking of recipes. Operating errors become visible through comparison with historical data, which leads to optimization of recipe processes and efficient planning of service calls," explains Christoph Kluge, Managing Director of tepcon GmbH.

High throughput due to automatic control and loading also played an important role in the choice of technology. By using an OHT (Overhead Hoist Transport), the system can be integrated into existing complex process chains, thereby accelerating the transport of carriers loaded with wafers. The resulting integrated warehouse in the wet process system with its up to 75 storage locations guarantees an uninterrupted production flow.

The up to 12 LMC process carriers are thus supplied without interruption with 100 wafers/ halfpitch (8 inches) each, which supports an uninterrupted and targeted production flow. Thus, AP&S doubled troughput on the same footprint and significantly reduce TCO (same chemistry twice the throughput).



Wet bench NexAStep – Our new Batch Tool for high throughput Wet Processing

Up to 12 LMC carriers of 100 wafers/halfpitch (8 inches) each for efficient processing

"With the new NexAStep plant platform, we have been able to combine all the positive experience that we have built up as AP&S over the past 20 years with current customer and market requirements in one plant. The next level of "automation, throughput and functionality" in wet process plant engineering could be climbed. It fills us with pride to be able to generate data in the field with the first plants and to see the added value that the new concept represents for us and the customers," says Tobias Bausch (CMO&CTO).
The wet process plants of the future use a combination of established drying processes such as the Marangoni effect and NID hot drying (Nitrogen IPA Dispense-Drying). Both processes are examples of specialized drying techniques that have already found their proven and qualified application for various diverse semiconductor technologies.
In order to give customers as much freedom as possible in designing the filling and process recipes, these can be precisely programmed individually and selected depending on the product.

Further innovations of the NexAStep system are the optimized extraction of the process chamber and the resulting lower contamination as well as the high process temperature of up to 170°C, which allows a higher process speed.

Overall, these advanced wet process systems offer the semiconductor industry significant added value for customers. They enable more efficient, more flexible, more cost-optimized, more automated and higher-quality production of semiconductor components, thus contributing to the further development of the technology sector.

This is precisely what the AP&S Academy, which opened its doors in June of this year, also supports. "We have been successfully conducting training courses at customers' on-site semiconductor factories for a long time. In recent years, however, demand here has grown significantly. There were also increasing calls from customers for a central training center for wet process technology so that running production facilities would not be affected by training purposes. This coincided with our strategy for founding the AP&S Academy," explains COO and initiator of the AP&S Academy Tobias Drixler.

Steffen Hölderle (Head of Service) and André Menge (Senior Service & Training) were proudly presented with the key to the AP&S Academy. Managing Director Tobias Drixler (COO) sees the training center as a platform for preparing both new employees and customers individually and

Up to 75 storage locations guarantees an uninterrupted production flow

Highly dynamic axis system for wafer-friendly transport and fast empty runs

specifically for the respective uses of the machines. The interest in such training offers has increased enormously due to the current shortage of skilled workers and the need to adequately instruct and thus qualify non-specialist personnel in the world of chemical wet process technology.

Four training modules, which can be attended continuously, are offered by the company's employees, who have both the knowledge of the semiconductor industry and the pedagogical skills. The know-how of the employees of AP&S International GmbH, which has been accumulated over 20 years, is thus passed on to interested parties in a focused manner in order to teach the handling of wet process equipment in a practice-oriented manner.

Manual operation and loading possible for maximum flexibility

From left to right: Managing Director Tobias Drixler (COO), Steffen Hölderle (Director of Service) and André Menge (Senior Service & Training)

Shareholder and Managing Director Alexandra Laufer-Müller: "Our goal is to cover the entire spectrum of wet process solutions required in both the front-end and back-end production chains. For example, our products perform functions such as cleaning, etching, metal etching, PR strip, electroless plating, lift-off, drying and development processes. This is the beginning. Together with our customers, we are constantly developing new outstanding processes, such as the AP&S metal lift-off process, which is unique in today's market. We also offer manual, semi-automatic and fully automatic applications."

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Report focuses on value chain's carbon emissions

The SEMI Semiconductor Climate Consortium (SCC) has issued its first report of the semiconductor ecosystem's greenhouse gas (GHG) emissions profile, an in-depth analysis of the semiconductor value chain's carbon footprint and priority-ranked carbon emission sources for the industry to address.

TITLED TRANSPARENCY, Ambition, and Collaboration: Advancing the Climate Agenda of the Semiconductor Value Chain, the report provides the most comprehensive sustainability data available on the semiconductor ecosystem. Key takeaways from the report compiled by Boston Consulting Group (BCG), under the direction of the SCC Baselining, Ambition-Setting and Roadmapping (BAR) Working Group, include:

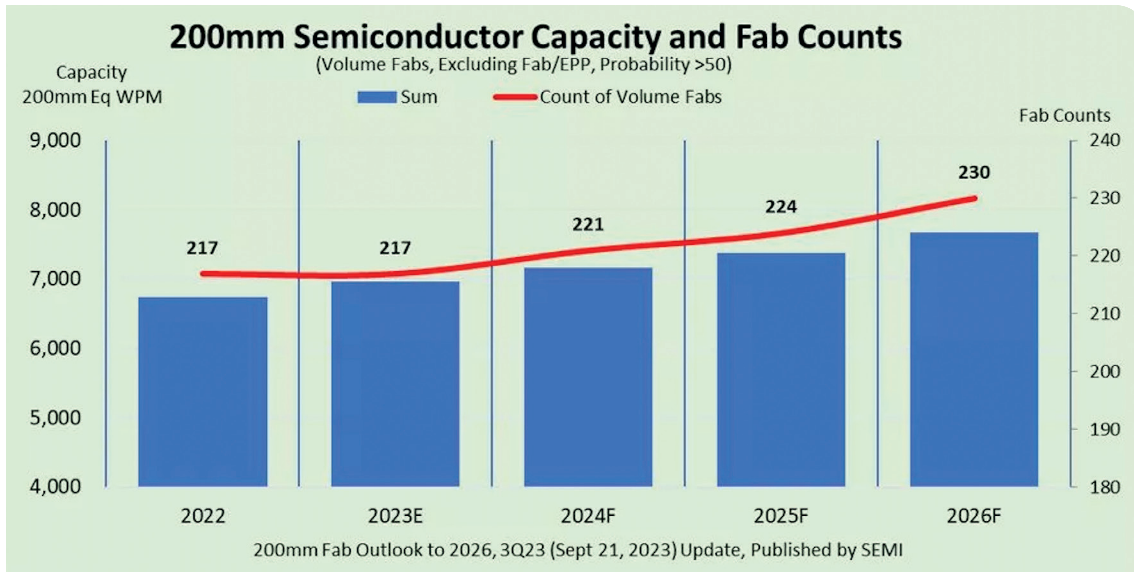
- **Baseline of value chain emissions**
  Semiconductor devices produced in 2021 have a lifetime CO_2e footprint of 500 megatonne (MT) – 16% from supply chain, 21% from manufacturing, and 63% from device use.
- **Low-carbon energy is a key lever**
  Bold and decisive investments in low-carbon energy sources can address more than 80% of industry emissions primarily by reducing the carbon footprint stemming from electricity usage for semiconductor manufacturing and for powering chips in electronics devices.
- **Investment and innovation to solve remaining 16%**
  Emissions from the supply chain and from manufacturing process gases will require considerable research and development to address, necessitating investments now.
- **Future manufacturing emissions scenarios**
  Current government and company commitments will substantially reduce manufacturing emissions, but they are still forecasted to overshoot the carbon budget for the 1.5°C pathway.
- **Dilemma of value chain emissions**
  Digital technologies that require semiconductors play a crucial role in reducing energy use and emissions across industries while simultaneously adding to the overall carbon footprint.

"While the SCC's work on behalf of the industry is just getting started, its sustainability report clearly outlines where chip industry efforts initially should be focused and how we can make the greatest impact for SEMI members and the semiconductor value chain at large," said Mousumi Bhat, Vice President of Sustainability at SEMI. "Thanks to the BCG team for their collaboration on this seminal work."

"For our industry to effectively accelerate climate action, it is crucial that we have a shared view on our industry's baseline carbon footprint, expected trajectory of future emissions, and available improvement levers," said Marijn Vervoorn, BAR co-lead and Director of Sustainability Strategy at ASML. "This report, including its clear view on data gaps and required data quality improvements, provides the foundation for an ambitious industry roadmap showing the tangible action required to achieve both short-term objectives and Net Zero emissions in 2050."

"Our work is far from finished," said Chris Jones, BAR co-lead and Business Development Manager at Edwards. "For the SCC to be successful, we need all three stages of baselining, setting our ambitions (targets) and curating the roadmap of how we will get there. Net Zero is our ultimate goal for SCC members, but the many steps to get there is the detail we are working out."

"The BCG team is proud to be part of this groundbreaking research to build the most comprehensive baseline of the industry's greenhouse gas emissions, helping to focus



our Climate Change and Sustainability efforts where they are most impactful," said Ramiro Palma, Ph.D., BCG Managing Director and Partner, Global Semiconductor Practice Area co-lead. "We thank the SCC and its member companies for all their engagement to make this study their own in a step toward a greener future."

200mm fabs to reach record high capacity by 2026

Semiconductor manufacturers worldwide are projected to increase 200mm fab capacity by 14% from 2023 through 2026, adding 13 new 200mm volume fabs (excluding EPI) as the industry reaches a record high of more than 7.7 million wafers per month (wpm), SEMI announced today in its 200mm Fab Outlook to 2026 report.

Power and compound semiconductors, which are vital for the consumer, automotive and industrial sectors, are the biggest drivers of 200mm investment. The development of powertrain inverters and charging stations for electric vehicles (EVs) in particular is expected to fuel increases in global 200mm wafer capacity as EV adoption continues to rise.

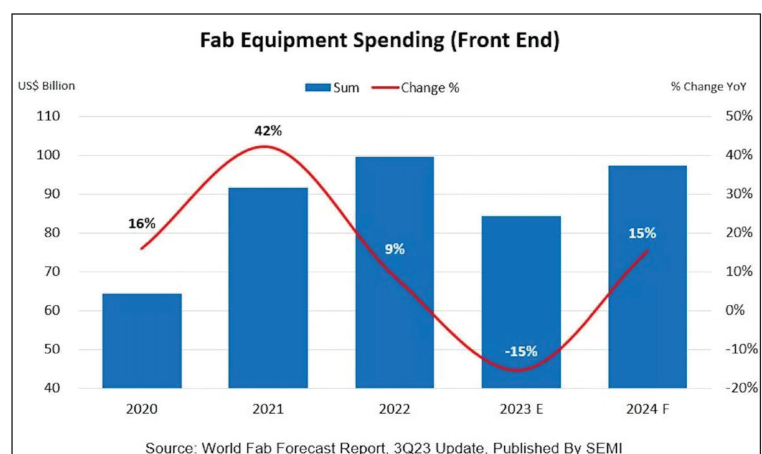
"The global semiconductor industry's ramp to record 200mm fab capacity highlights the bullish expectations for growth in the automotive market in particular," said Ajit Manocha, SEMI President and CEO. "While automotive chip supply has stabilized, the increased chip content in EVs and the drive to reduce charging time is spurring capacity expansions."

Chip suppliers including Bosch, Fuji Electric, Infineon, Mitsubishi, Onsemi, Rohm, STMicroelectronics and Wolfspeed are accelerating their 200mm capacity projects to meet future demand. The SEMI 200mm Fab Outlook to 2026 report shows fab capacity for power semiconductors growing 35% from 2023 to 2026, with Microprocessor Unit/Microcontroller Unit (MPU/MCU) ranking second at 21%, followed by MEMS, Analog, and Foundry at 16%, 8%, and 8%, respectively.

Accounting for most of the 200mm fab capacity are 80nm to 350nm technology nodes. Growth of 80nm to 130nm node capacity is forecast to expand by 10%, while 131nm to 350nm technology nodes are expected to register an 18% expansion from 2023 to 2026.

Regional outlooks

Excluding EPI, Southeast Asia is projected to lead 200mm capacity growth with a 33% increase from 2023 to 2026. China is expected to rank second with 22% growth. The biggest contributor to the 200mm capacity expansion, China is projected to reach more than 1.7 million wafers per month by 2026. Americas, Europe & Mideast, and Taiwan will follow at 14%, 11%, and 7% growth, respectively. In 2023, China is forecast to claim 22% share of 200mm fab capacity, while Japan is expected to account for 16% of total capacity, followed by Taiwan, Europe & Mideast, and America at 15%, 14%, and 14%, respectively.



The SEMI 200mm Fab Outlook to 2026 report tracks 335 fabs and lines (from R&D and volume). The report includes 99 updates across 85 facilities and lines, including 12 new lines since the previous update in March 2023.

2024 fab equipment spending to recover in 2024

Global fab equipment spending for front-end facilities in 2023 is expected to decline 15% year-over-year (YoY) to US$84 billion from a record high of US$99.5 billion in 2022 before rebounding 15% YoY to US$97 billion in 2024, SEMI announced today in its latest quarterly World Fab Forecast report. Softening chip demand and elevated inventory of consumer and mobile devices will contribute to the 2023 decline.

Next year's fab equipment spending recovery will be partly driven by the end of the semiconductor inventory correction in 2023 and strengthening demand for semiconductors in the high-performance computing (HPC) and memory segments.

"The 2023 decline in equipment investment is proving shallower and the 2024 rebound stronger than expected earlier this year," said Ajit Manocha, SEMI president and CEO. "The trend suggests the semiconductor industry is turning the corner on the downturn and on a path back to robust growth fueled by healthy chip demand."

Foundry segment continues to lead semiconductor industry expansion

The foundry segment is expected to lead the semiconductor expansion in 2023 with US$49 billion in investments, 1% growth, and US$51.5 billion in spending in 2024, a 5% increase as investment continues in leading-edge and mature process nodes. Memory spending is forecast to stage a strong comeback in 2024 with a 65% increase to US$27 billion after a 46% decline in 2023. Specifically, DRAM investments are expected to decline 19% YoY to US$11 billion in 2023 but recover to US$15 billion, a 40% annual jump, in 2024.

NAND spending is projected to mirror that trend, decreasing 67% to US$6 billion in 2023 but surging 113% to US$12.1 billion in 2024. MPU investments are expected to remain flat in 2023 and increase 16% to US$9 billion in 2024.

Taiwan Continues to Lead Equipment Spending
Taiwan is expected to retain the global lead in fab equipment spending in 2024 with US$23 billion in investments, a 4% YoY increase. Korea is projected to rank second in spending, with an estimated US$22 billion in investments in 2024, a 41% jump from this year reflecting a memory sector recovery.

With export controls expected to limit China's spending in leading-edge technologies and foreign investment, the region is forecast to place third in equipment spending worldwide in 2024 at US$20 billion, a decline from 2023 levels. Despite the constraints, Chinese foundry suppliers and IDMs are expected to continue investments in mature process nodes.

The Americas is expected to remain the fourth largest region in spending, reaching a historic high of US$14 billion in investments in 2024, a 23% YoY increase.

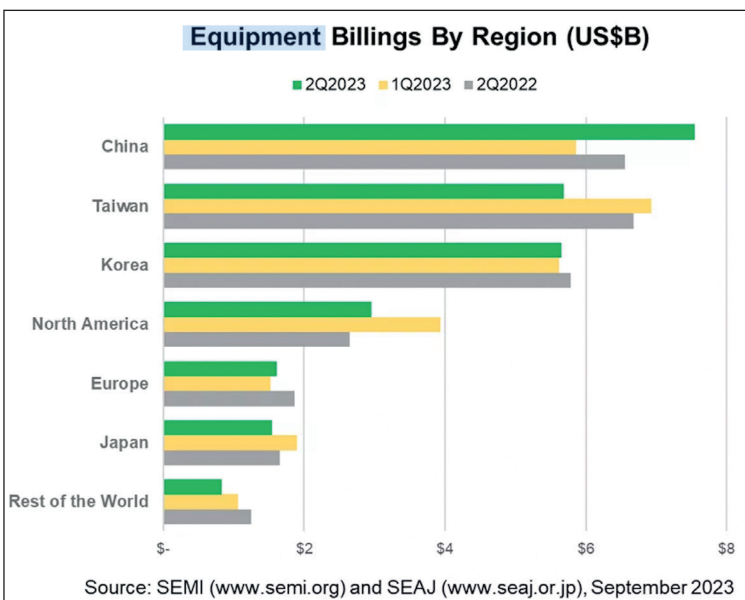
The Europe and Mideast region is also forecast to log record investments next year, increasing spending by 41.5% to US$8 billion. Fab equipment spending in Japan and Southeast Asia is expected to increase to US$7 billion and US$3 billion, respectively, in 2024.

Covering 2022 to 2024, the SEMI World Fab Forecast report shows the global semiconductor industry increasing capacity by 5% this year after an 8% rise in 2022. Capacity growth is expected to continue in 2024, climbing 6%.

The latest update of the SEMI World Fab Forecast report, published in September, lists 1,477 facilities and lines globally, including 169 facilities and lines with various probabilities expected to start operation in 2023 or later.

Billings dip 2% YoY

Global semiconductor equipment billings dipped 2% year-over-year to US$25.8 billion in the second quarter of 2023, while quarter-over-quarter billings slipped 4%, SEMI announced today in its Worldwide Semiconductor Equipment Market Statistics (WWSEMS) Report.



Compiled from data submitted by members of SEMI and the Semiconductor Equipment Association of Japan (SEAJ), the WWSEMS Report is a summary of the monthly billings figures for the global semiconductor equipment industry. Following are quarterly billings data in billions of U.S. dollars with quarter-over-quarter and year-over-year changes by region

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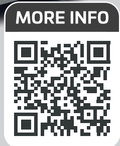

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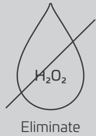
Ongoing supply chain disruptions impact the industry, leading to anticipated shortages and rising prices in cleaning chemicals, as forecasted by researchers like TECHCET. Smart utilization of ozone, along with the usage of minimal amounts of ammonia and acids, result in significant cost savings. This approach can replicate traditional cleaning steps and enhance organic cleaning efficiency in SC1, SC2, and DHF processes, with precise control by using inline spiking technology.



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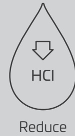
Reduce



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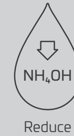

Reduce

Reduce

Chemical consumption: SicOzone vs. conventional cleaning applications

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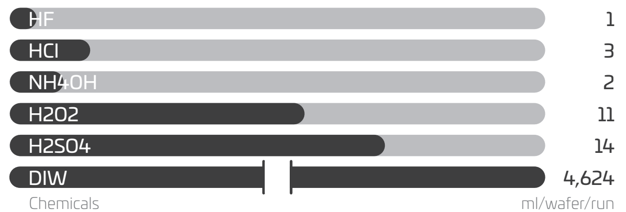

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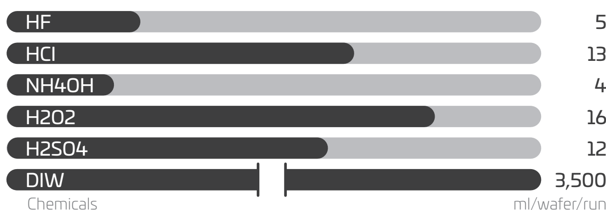
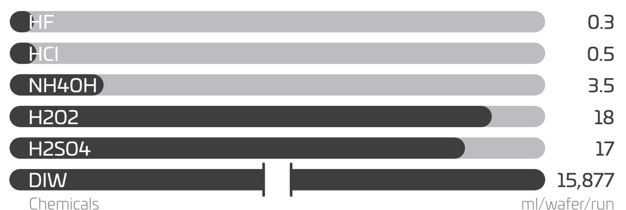


Wetbench



Efficient semiconductor thermal management

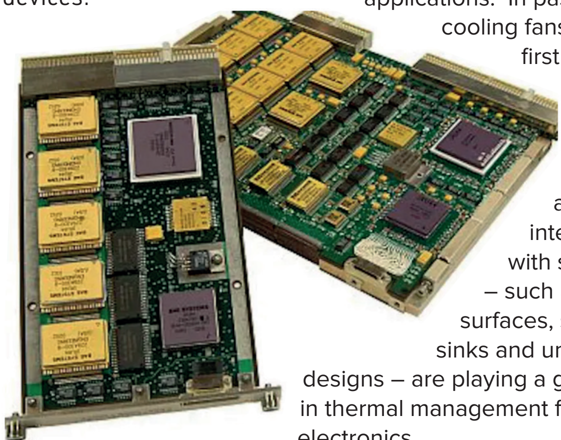
There is growing consensus in the semiconductor ecosystem that we are on the cusp of significant changes in packaging technology. Evolving semiconductor technologies are driven by new applications. These new technologies call for semiconductor materials that are highly efficient, smaller in size and highly reliable, with longer field life cycles and the ability to operate across all climate conditions.

BY RAMESH KOTHANDAPANI, TECHNICAL DIRECTOR, MICROELECTRONIC PACKAGING, MATERION CORPORATION

ELECTRONIC COMPONENTS have necessarily evolved since the late 1990s, yielding complex and compact designs with efficient performance for their intended applications. Companies are engaging in more research activities to develop new alloys and composite materials, ways to prolong the life of semiconductors, and suitable environments for semiconductor performance. Industry is capturing these developments in the technology roadmap.

Modern electronics pose several challenges during the design stage. One example is space constraints, which relate to the microelectronic packaging design process. The number of electrical connectors, the material selected, electrical resistances, weight and cost are just some of the factors that drive new technology.

Many devices within a microelectronic package may be operating simultaneously, which leads to thermal accumulation. This collected thermal energy or heat cause the semiconductor to perform inefficiently, or even to malfunction. Thermal energy is a constant threat to semiconductors, especially in critical applications. In past years, fins and cooling fans were often the first line of defense against high temperatures.



➤ Thermal management is a critical process step for the efficient operation of semiconductor-powered devices.

Today, advanced thermal interface materials with special features – such as wavy 3D surfaces, smaller heat sinks and unique enclosure designs – are playing a greater role in thermal management for advanced electronics.

Following is a partial list of sectors or industries in which advanced thermal management materials are required for reliable operation:

- **Space:** Understandably, the space sector has no room for failure. The technology road map for space must support planetary exploration, space tourism, space mineral mining for new materials and probes and vehicles to travel vast distances. Semiconductor material used here must be able to tolerate harsh environmental challenges while performing critical operations.

- **Aerospace, low-altitude mobility:** There can also be no failure with any type of flying vehicle. From passenger planes to war planes and even forthcoming low-altitude flying taxis, efficient electronics will be required for maximum performance. A future human-transporting drone must be equipped with sophisticated semiconductor chips. These chips must support uninterrupted communications, air current sensing and emergency landing. Thermal management is crucial to these semiconductors.

- **Uninterrupted communications:** Smoother communication is always expected despite various types of noise and disturbances. The electronics and their respective packaging must enable the semiconductor to serve its designed function.

- **Radio wave-based telecommunications:** Base station systems contain semiconductor devices operating within a multitude of different environmental conditions. They experience constant thermal management issues that can lead to interruption of communications. Inefficient electronics causes poor signal management and the need for frequent maintenance. The evolution of telecommunications has now reached its fifth

➤ Telecommunications devices risk poor signal management and decreased efficiency without proper thermal management.

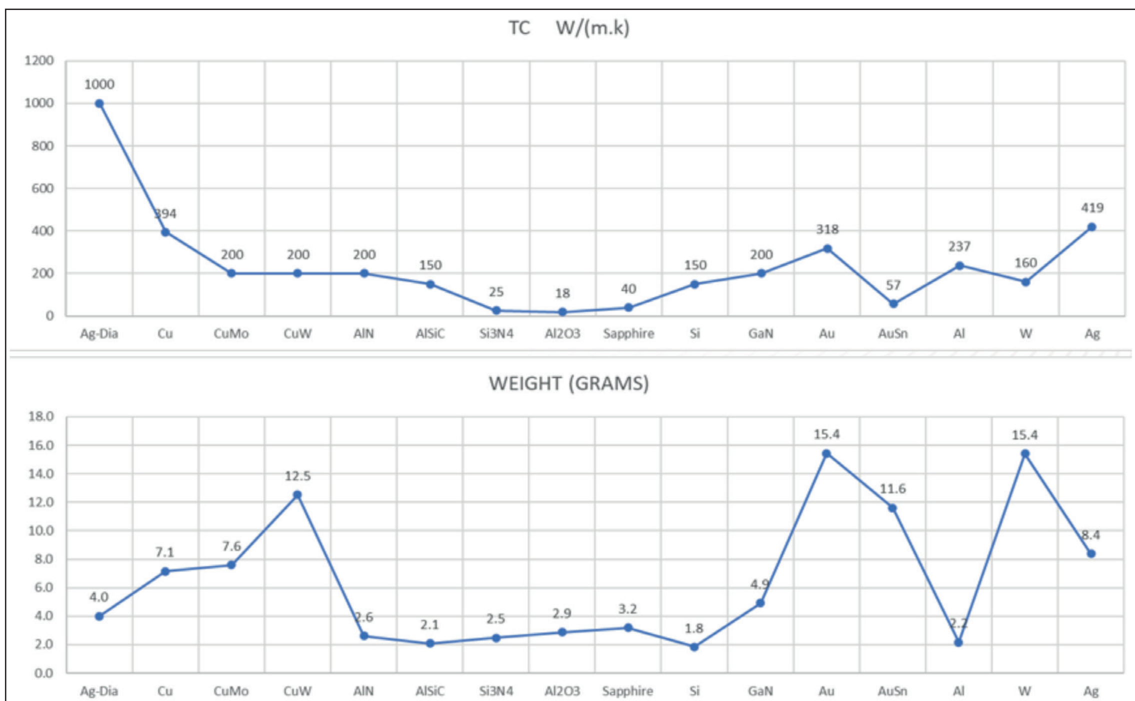
generation, with ongoing changes in design and device size. Each generation demands incrementally better thermal management of electronic packaging. Microelectronics are especially challenging in this regard, as these semiconductors experience enormous loads that require efficient thermal management material. From military communication and airliners to consumer mobile devices and smart home and office systems, these applications all require the highest-quality communication.

Automobiles and autonomous travel: Increasingly, automobiles are combining telecommunication electronics with safety and optical sensing devices. Environmental concerns over the use of petroleum products have led to the development of temporary energy storage or battery products. Efficiently managing power adds a layer of design complexity, with additional electronic modules being integrated into a single semiconductor. As multiple applications operate simultaneously, loads on these semiconductor units generate high levels of thermal energy. These batteries also charge and discharge frequently, putting a strain on the electronics governing their operation. Electric vehicles contain an estimated four to six times more electronic components than conventional vehicles.

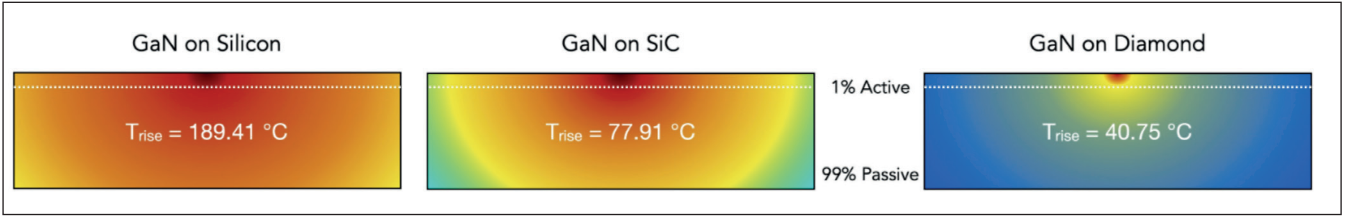
Human-wearable systems with efficient heat management materials: Human-wearable devices are challenging as a result of their small size, safety requirements and weight. Much like battery-operated devices, they are prone to heat generation that must be highly managed through material selection.

Again, these are only a few examples illustrating emerging thermal management demands on semiconductor materials. To date, silicon-based materials have been most widely used because of their efficient operation and wide availability. Silicon's cost, integration into established design and process flow, and favorable chemical and electronic properties also contribute to its popularity for semiconductor applications.

In new devices bundling multiple applications, however, the question arises whether existing semiconductor materials can deliver needed output. Newly developed and enhanced materials are rapidly coming onto the scene. These include



➤ Designers must balance the thermal conductivity and weight of materials used in their systems.



The effect of temperature on semiconductor efficiency is dependent on the materials being employed and their specific physical properties.

gallium nitride, gallium arsenide and silicon carbide, each of which has its own pros and cons as designers continually balance cost, weight and other factors in their material selection.

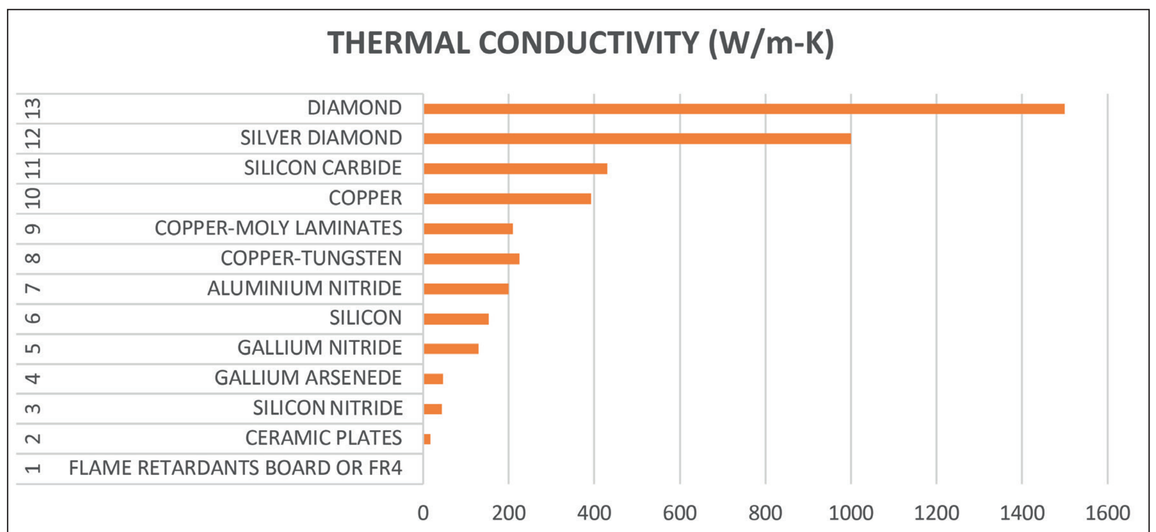
These designers must consider several factors, including the reality that the lower thermal conductivity of new materials often increases cost while traditional materials, which do not tend to enhance semiconductor efficiency, offer undeniable cost benefits.

As mentioned earlier, the electronic module has shrunk considerably and now contains many more components than it did previously. During operation, it is natural for these devices to generate heat that gets transferred to other assemblies. Bonding materials used to assemble the semiconductors are constantly challenged by poor heat transfer. If heat is not transferred quickly, the semiconductor cannot perform its role efficiently, leading to device or system failures. In certain applications, high humidity combines with heat to create even more severe failures.

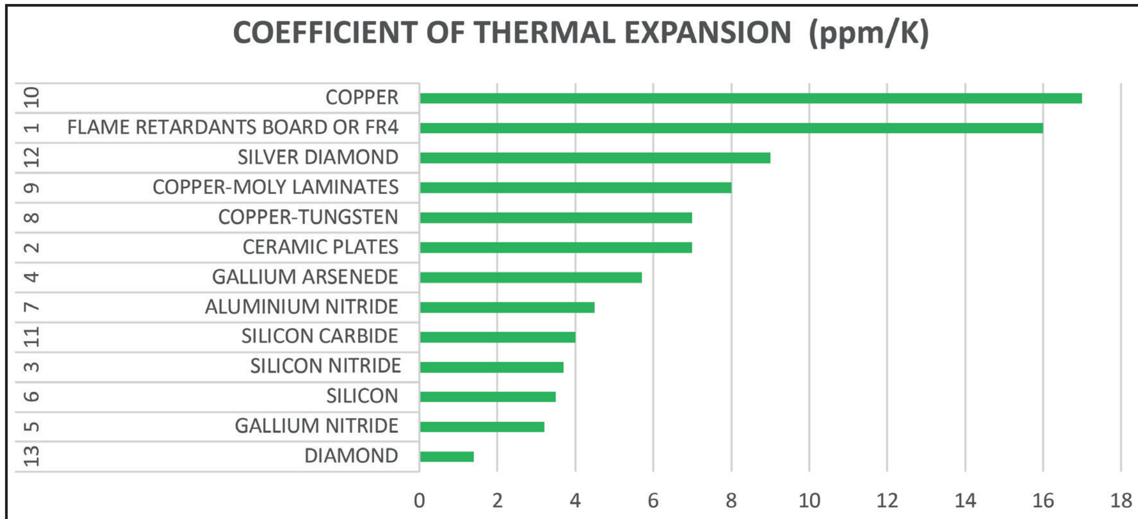
An efficiently designed semiconductor electronic system requires a good thermal management material to dissipate heat. Frequency switching, voltage handling capabilities and operating temperature are important considerations for future semiconductor materials. Gallium nitride (GaN) placed on silicon and silicon carbide are examples of materials gradually replacing silicon for this purpose. Thermal overstress is an important point to consider during the design stage. A good electronic design team will consider the thermal transfer processes that add weight to the design and enlarge electronic architectures accordingly. Design teams should introduce longer-term reliability test simulations and good bonding materials that are able to tolerate high levels of heat.

Figure 4 clearly illustrates the effect of temperature on semiconductor efficiency. The standard GaN on Si measures 189 degrees Celsius with 1% of the active device on silicon. The undesired heat transfer will be passed onto semiconductor bonding materials – which could be any eutectic die bond material or solders – causing a catastrophic failure over time. GaN on SiC is significantly better, reducing heat by more than 50% to 77 degrees Celsius. The illustration of GaN on diamond refers to a diamond composite material that manages the heat transfer process extremely well. It yields a reduction of about 50% compared with GaN on SiC and four times lower than GaN on Si.

Thermal transfer material selection is also crucial to packaging components. Silver particles and small diamond particles are combined to produce a diamond composite substrate that enables excellent heat transfer for any of the available semiconductor materials. In addition to the diamond composite, there are several other heat transfer materials from which to select. Thermal conductivity is measured in watts per meter Kelvin (W/mK). Materials with high thermal conductivity can transfer heat quickly, while materials with low thermal conductivity will insulate heat well. The larger the value, the better the performance. Not all materials with higher thermal conductivity values are useful substrate, however, because of the potential for greater expansion. One example is copper, which offers good thermal conductivity but also tends to expand significantly.



Thermal conductivity of various materials, as measured in watts per meter Kelvin (W/mK).



Coefficient of thermal expansion (CTE) for various materials (in ppm/K).

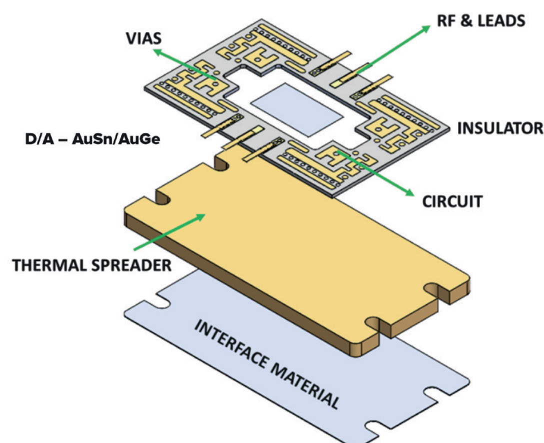
Figure 5 illustrates thermal conductivity values for several materials. It is important to match this value with Figure 6 listing CTE values.

The coefficient of thermal expansion (CTE) is a measure of how much a material expands or contracts when its temperature changes from a colder zone to a hotter zone. It is usually expressed as a fractional change in length or volume per unit temperature change. Unlike TC, CTE values must be lower for efficient thermal management. Apart from TC and CTE, inefficient heat transfer must be managed well with an appropriate material to dissipate heat. The illustration below is an example of the next-generation Laterally Diffused Metal Oxide (LDMOS) RF device GenPack®, which is constructed with a base capable of efficiently dissipating heat. An interface material with foil contacts could be added to enhance thermal transfer even further. These thin foils (MiM) offer more contacts to connect the base and substrates. Selecting semiconductor attachment or bonding material is also very important. The semiconductor or die is usually attached to its base using epoxies with higher melting temperatures that require curing before final hermetic or semi-hermetic packaging. Eutectic die attach solder materials such as gold-germanium (88Au/12Ge) alloy, which has a melting temperature of 361 degrees Celsius, or gold-tin alloy (80Au/20Sn), which has a melting temperature of 280 degrees Celsius, may also be considered. These are purely organic-free materials for the die bond process.

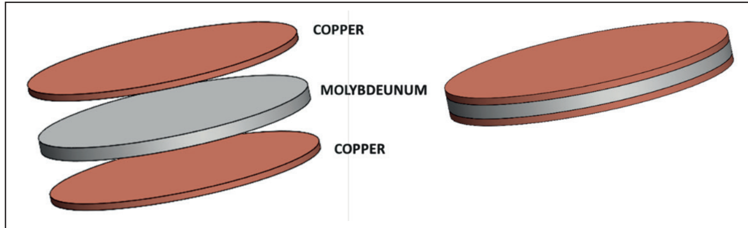
Conductive epoxies are very widely used for die attachment in silicon semiconductors. As mentioned, if these conductive epoxies contain organic material, it can lead to outgassing, which reduces die performance. Using gold-tin (80Au/20Sn) or gold-germanium (88Au/12Ge) as die attach materials eliminates organic content and reduces outgassing, thus enhancing the performance of the die. The package may then undergo hermetic sealing with either gold-tin or gold-germanium combined with a plated lid.

Again, it's important to emphasize that conductive epoxy-based die attach materials may release gases that become trapped during application and circulate within the hermetically sealed package. These gases are harmful to the semiconductor and can cause it to operate inefficiently. This leads to high heat generation, which in turn may cause further complications. Under these circumstances, additional materials (such as a getter material) must be included in the package to manage outgassing. Hermetic packaging with the Combo Lid® is a critical process step that prolongs the life of semiconductor materials in the package and facilitates operation free of environmental pollutants such as moisture or gases like hydrogen and oxygen.

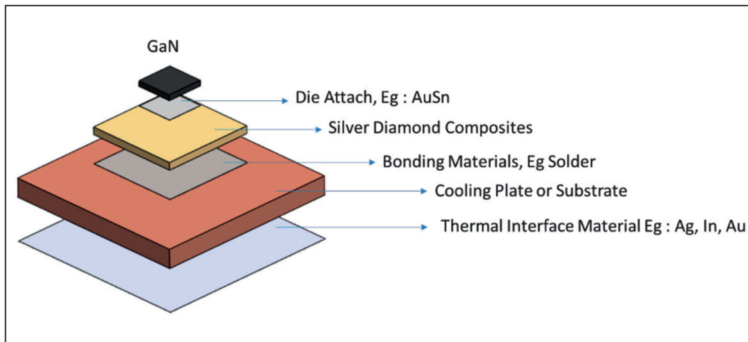
After the package is well sealed, units should be subjected to a series of reliability tests. Gross leak, fine leak, electrical performance, aging and other tests can confirm whether selected materials will truly enhance field performance. Electrical and temperature cycle assessments can be time consuming processes, so designers often employ accelerated tests that simulate the life of the package. Survival in these harsh test environments validates proper selection of materials for efficient



Exploded schematic view of the next-generation Laterally Diffused Metal Oxide (LDMOS) RF device GenPack®



Copper and molybdenum laminates are among the materials that lend themselves to efficient thermal management.



Schematic view of thermally managed package for a GaN semiconductor device.

thermal management. In summary, the following items should be considered during the electronic design stage:

1. TC and CTE values for various selected materials
   a. Higher TC and lower CTE values
2. Substrate or base material selection
   a. Diamond composite
   b. Copper-moly laminates
   c. Copper-moly alloys
   d. Silicon nitride substrates
   e. Ceramic materials
   f. Copper tungsten alloys
3. Die attach materials
   a. Silver epoxy
   b. AuGe
   c. AuSn
4. Hermetic lids
   a. Determine the seal cover
   b. What solder type to be used?
5. Post-die attach process to cure epoxies
   a. Curing temperature
   b. Any test to confirm effectiveness?
6. Outgassing
   a. Source of gases
   b. Containing them
   c. Correlate with electrical tests
7. Post-packaging reliability tests
   a. Gross leak (nondestructive)
   b. Fine leak (nondestructive)
   c. Temperature cycle tests (destructive)
   d. Electrical test (nondestructive)
8. Thermal interface materials
   a. Silver preforms with 3D surfaces for higher surface contacts
   b. Indium-based materials

Material selection and package design are both vital in creating reliable systems. It's also important to develop a plan to handle mass production. Cost roadmaps and manufacturing processes are reviewed in parallel at an early stage. Materials with affordable CTE and TC values may offer high levels of performance for specific applications. Adding special layers of materials with VIAS and pedestal mimics high-end packaging. The point, of course, is to prepare for volume production with a highly developed process.

Thermal expansion plays an increasingly important role in newer applications. The evolving challenge is to combine different materials to form a consolidated package housing. Many materials exhibit promising thermal management properties that put them on the designer's short list. Additional features could be added to materials to enhance operation. For example, improved heat dissipation can be achieved through braze alloys or copper.

Over time, this process will be explored in both organic and various amorphous materials such as glass substrates. Such materials may serve as both heat absorbers and as substrates for multiple chips. As substrates, they could be further enhanced with thermal interface materials to yield a larger contact area. The thermal interface material also contributes to greater electrical contact.

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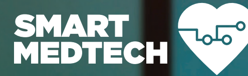

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Volkswagen Group reorganises semiconductor procurement strategy

Karsten Schnake, Board Member for Procurement at Škoda Auto and head of the Volkswagen Group's cross-brand and cross-functional task force COMPASS (Cross Operational Management Parts & Supply Security), explains to the Silicon Semiconductor Editor, Philip Alsop, the advantages of the reorganisation process, which include: a high degree of transparency, closer collaboration with key supply chain partners, improved risk management and a streamlining of component inventory, all under the auspices of a newly established Semiconductor Sourcing Committee.

PA: We're talking because the Volkswagen Group is reorganising your procurement of electronic components and semiconductors. It would be good to understand whatever you can share as to the background. Obviously, the whole industry had problems with COVID and there's the ongoing geopolitical situation, but, if you can, the reasons behind the decision to look at the reorganisation?

KS: For myself, so I'm now working for VW and also for the procurement, more than 25 years. And this is a continuous development. For us, the semiconductor issue is also, I would call it evolution, but it was accelerated by COVID and the chip crisis. So what we see clearly more or less the time horizon which we have is from the beginning 2025/2026 the new platforms we are planning to roll out there. That is the importance of semiconductors. Because

semiconductors contribute a lot, with energy savings for the new electric vehicles, and also for computing power, for autonomous driving and for controlling the car. So, this was clear that it's coming. But what was for us really an issue is that this was accelerated by the chip crisis, through the chip shortage, and it has become much more of an issue than we expected when we started with the new platform developments.

And today, after this crisis, or if you would ask me, in the crisis, what it was like to handle such things, it's like a nightmare. But at the end of the day, we have to say it's also like a present for us because we can be faster. We can, let me say, catch up two or three years earlier, instead of what the normal planning for the rollout of new platforms are.

So, it's a way of evolution. But we have to accelerate this much more than we expected it. And at the end of the day it is something that we learn faster. We have to learn and you can say we listen to the semiconductor industry because until this crisis, until the chip crisis and this changes, I would say our view more or less ended with our first tier partners on the electronic components for steering, for controlling and the like. We have not engaged directly with many semiconductor suppliers or semiconductor partners at this time. However, beginning last year, we initiated efforts to actively connect and listen to them, learn from them and deep dive in a partnership with them.

PA: And I believe you have, whether it's overseeing or as a result of this reorganisation, you've established a semiconductor sourcing committee. And to what you've alluded to there, I believe you're now looking to work more directly. I mean presumably previously you were working was it through distributors, more sourcing and now you're wanting to establish or develop relationships with the tier one semiconductor manufacturers, if you like, get work directly with them. Is that one of the key parts of this new strategy?

KS: Yes, let me describe this in this way. So, first issue is that we established for this item for supply chain, supply chain securing and developing. In the supply chain we installed new people which we hired and which are coming internally from our company. So, to fill up the teams in the technical department, quality, logistics and also in the procurement and these team together and we have these teams established in all platform developers so far.

There are teams established now which are handling this item directly with the semiconductor producers and with partners in the supply chain. What you pointed out, for example, distributors and what is our goal together is to achieve first transparency, the risk analysis and to make with them contracts and let me say projects where we can secure our supply. And we do this with the colleagues from the technical department in something what we so called category management where we together with our new partners decide which technology should be delivered in which category.

PA: You mentioned transparency. Clearly you worked already fairly closely with a lot of your supply chain partners but if I understand correctly, you're almost taking it to a new level of transparency. So you're going to be sharing, I guess it's a two way collaboration. They'll be telling you some of what they're up to and availability and you will be sharing your roadmap so that there are no surprises. You are hoping to much better manage or improve the management of the supply chain so that you won't end up thinking hang about, we need some chips and where are we going to get them from? Hopefully that won't arise in the future. Is that right?

KS: Yes, and for us what we've learned in the last two years that we have to influence and we can influence the quantity of, let me say, critical chips in a very early phase. So, on the Wafer level, you know, this is much better. And we decide together with the wafer producer which quantities at the end of the day we need to produce. Then coming from the wafer in the back end. The right dedicated chips. We need a couple of weeks or months later in the production to keep our factories running in the right way. It was for us extremely important to go two technical layers under our normal bill of material.

Normally our bill of material in the past ended up on the technical layer which we get as, let me say, assembly from our first tier partners. But we have achieved for us the view now with our new partners on the chip level and also on the wafer level that we know where the wafer is coming from, what supply chain we have from the wafer or from the crystal, I would say from the raw material over the wafer to the chip so that we can decide and control together with our new partners what chips should be produced when we have given example one wafer and we decide okay, should be DLP driver chips

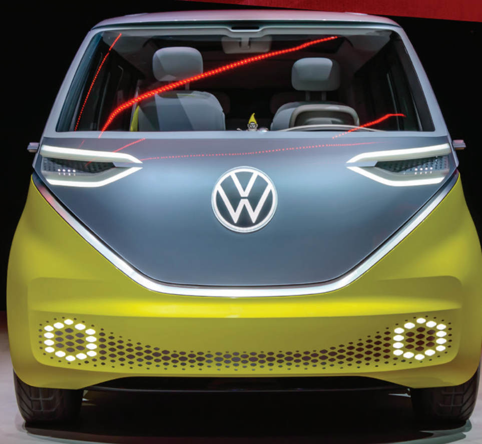
we are much more able to secure our supply chain in our factories and we can decide, okay, which cars, in which quantity we need and should be produced. And this has started for us now on the wafer level. And we have a lot of examples where we are now directly steering this

there or should be, let me say voltage controllers there.

And this we are deciding now actively because then we are much more able to secure our supply chain in our factories and we can decide, okay, which chips, in which quantity we need and should be produced. And this has started for us now on the wafer level. And we have a lot of examples where we are now directly steering this. What for us was also, I think to your question, important that we combine now the database for our semiconductors. So full transparency on the semiconductor level in the cars.

And this we connected with our demand systems coming from our sales area so that we can now not only calculate the demand on a unit level like, let me say a steering unit, which we have in the car. We now can calculate the quantities on the chip and on the wafer level because we connected the systems and we connected from the semiconductor industry well known risk analysing tools with this database so that we have now the full transparency over that and this is what we have learned from our partners from the semiconductor industry - very important for them because now we can discuss with them what we need in two, three or four years.

And it's much more better also for these partners to do the right investments. The intention is that we are more secure, but our partners can also in their own supply chain in their factory planning make much better investments and planning. With additional transparency, it is a win-win for both the semiconductor industry and for us in the car industry.



PA: And I think as well that standardisation is something you're also looking at doing - you're going to potentially use less components overall. And that helps in terms of reducing your inventory? And are you looking to consolidate the supply chain to work, if you like, more closely with fewer suppliers, or will you still work with the same amount of suppliers but just potentially less product variations along the way?

KS: I have a little bit of a smile on my face. Let me give you two examples. So, what we pointed out or what discussed together at the beginning, we hired a lot of new people. Coming from the semiconductor industry and I have some new colleagues which are, let me say 27, 28 coming from this industry and they told me 'Hey, Mr. Schnake, I see we have here semiconductors which are older than me, which are longer in the market'! They are still good, but now running out.

And the other thing is, I would say when you walk through this crisis, you have the feeling VW was more or less using every ever-produced semiconductor! And we have to have this control for the future which is so important. And then also let me say, to have always the newest technology and to reduce also the capacities you need for developing the right software for this hardware, you have to reduce the variance.

And this has started what we called category management with our technical colleagues from every platform developer in our group. So that our clear goal is to reduce the number of variants dramatically and then focus with our partners on these technologies and over the right roadmap, then to replace, let me say, after five, six years of running this semiconductor with the newest technology because we need it for energy consumption, to reduce energy consumption in the cars in the future and with new functions we are then adding with software updates.

PA: It would be good to understand whether you've got, if you like, official targets or you know in your head where you think you'd like to be with this, just anything you can share. Have you set objectives and time frames as to how you want to improve this process?

KS: It's clear if you're handling supply chain, then the clear target is to have zero losses in the supply chain. Because it is not only a loss for our customers who have to wait for the car, it's a loss for the VW group and it's a loss for our partners. Because also our partners, the suppliers in the supply chain, have losses when we are not able to let me say keep it running in a proper and perfect way. So this is the first overall target. It's clear that we have risks, it's clear that we have, let me say, negative impacts in the supply chain. But the daily job of the organisation is prepare yourself, be ready, that we have no losses overall. Then the other thing is what's coming with that, because then you are focused, then you are training the team in the right way, then you have the right people in place and then you are creating the strategy which supports this.

The other topic which I think is also very important - I'm working for procurement and normally it's always a question which is very important that we have commercial-wise to achieve the best result. And it's really important because we are doing this also for the customer. When you as a customer buy a new Golf, when you're buying a new Audi, when you're buying a new Skoda, a new Porsche, whatever in which range you are searching, you expect that you are getting a maximum value for your money. So, it's also for us to take as much care as possible with the costs. But you can only do this if your partners are also with you. And so to work on these partnerships in this open way, in the same way, is very important. And this is why we say we generated and we bring now in place new partners from the semiconductor industry. We have roughly 40 new partners where we are on weekly base in discussions, show our figures, be transparent, learning. But we are also staying with our first tier partners where we are working now over 50 years and it's a clear commitment from our side that we are working with both because otherwise you are unable to secure the supply chain in the right way.

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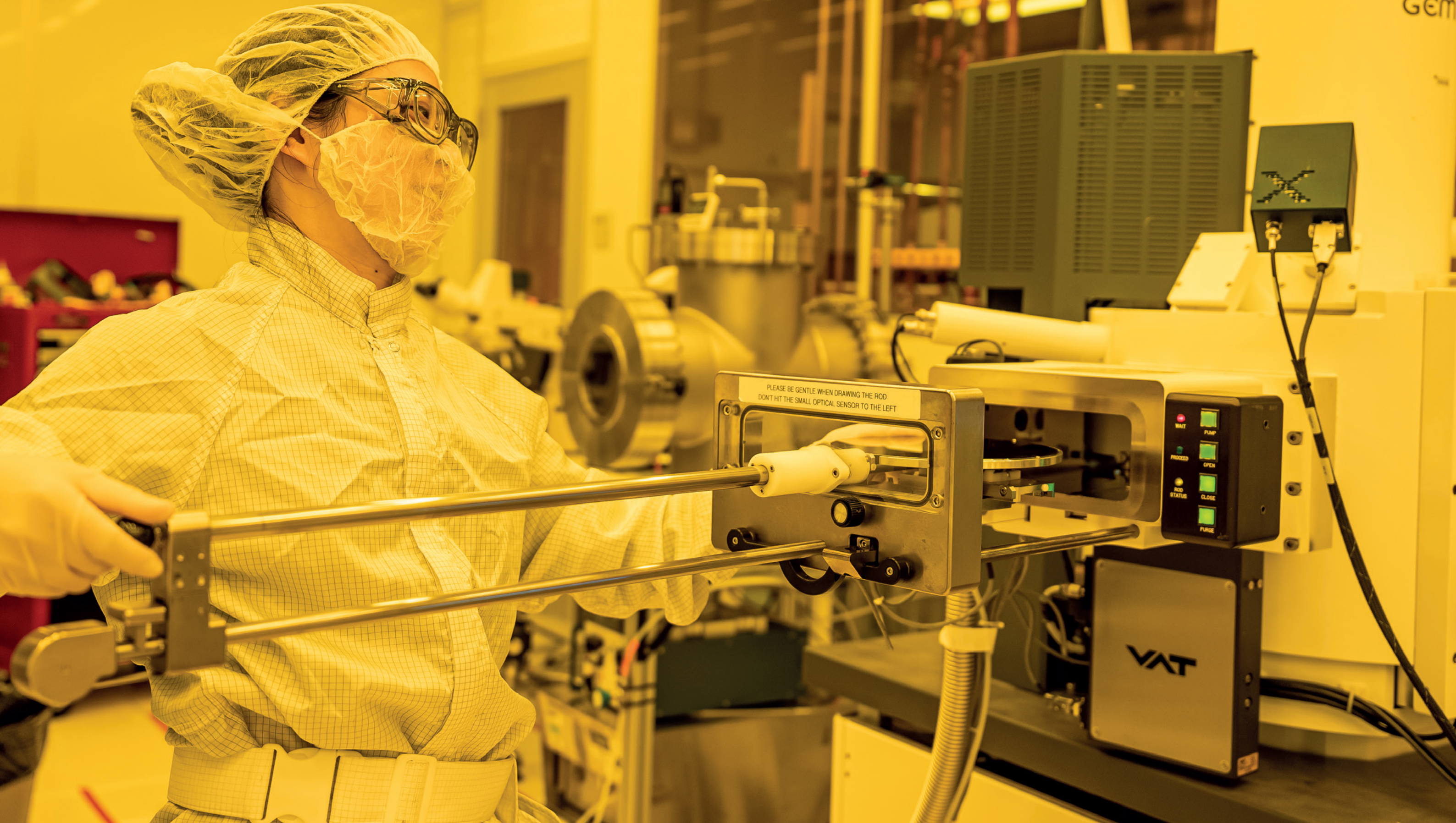

Beihang Yu preparing silicon wafers for inspection at the Molecular Foundry's nanofabrication facility. Marilyn Sargent/Berkeley Lab

How scientists are accelerating next-gen microelectronics

Multi-institutional team led by Berkeley Lab could help chip manufacturers race ahead of Moore's Law

BY THERESA DUQUE, SCIENCE WRITER, BERKELEY LAB.

A NEW CENTER led by Lawrence Berkeley National Laboratory (Berkeley Lab) could accelerate the next revolution in microchips, the tiny silicon components used in everything from smartphones to smart speakers, life-saving medical devices, and electric cars.

The new center, called CHiPPS – or the Center for High Precision Patterning Science – is led by Berkeley Lab microelectronics expert Ricardo Ruiz. He is also a staff scientist in Berkeley Lab's nanoscience user facility, the Molecular Foundry. "Advanced computer chips are essential to modern life. Staying at the forefront of this technology – and keeping pace with Moore's Law – is critical to our economic security and national defense," Ruiz said. Over the course of four years, Ruiz and his research partners will direct their diverse scientific expertise toward a common goal: Gaining new insight into the science of extreme ultraviolet lithography or EUVL, a revolutionary technique that enables the world's leading semiconducting manufacturers to pack more than 100 billion transistors – the tiny components that help a computer retain and process data – into a chip the size of a fingernail.

The team includes Berkeley Lab scientists from the Molecular Foundry, the Advanced Light Source, the Center for X-Ray Optics, the Chemical Sciences Division, and the Energy Storage & Distributed Resources Division, along with collaborators from Argonne National Laboratory, San José State University, Stanford University, the University of California at Santa Barbara, and Cornell University.

The researchers' work could help chip manufacturers make even smaller, more powerful chips, and support the goals of the Creating Helpful Incentives to Produce Semiconductors and Science Act, which aims to mitigate supply chain disruptions by helping the U.S. design and produce the world's most advanced chips domestically. (The CHIPS and Science Act was signed into law by President Joe Biden last summer.)

Last year, the U.S. Department of Energy awarded the CHiPPS research center a total of $11.5 million over four years through the Energy Frontier Research Centers program to pursue fundamental research in EUV lithography, including new materials and their interaction with EUV light. The CHiPPS center's efforts comprise four research "thrusts" focused on photomaterials synthesis, new "hierarchical" self-assembling materials, theory and modeling, and new techniques to characterize EUV lithography materials with atomic precision.

The CHiPPS research center not only aims to advance EUVL research, but it also places great emphasis on workforce development to nurture the next generation of scientists and engineers, Ruiz said. Through a collaboration with San José State University, the CHiPPS center offers an immersive work training program to four students every summer, consisting of two undergraduate students and two master's students. (The inaugural cohort commenced in June.)

Before joining Berkeley Lab in 2019, Ruiz worked as a research scientist in the microelectronics and data storage industry, specializing in polymer-based lithography techniques for magnetic data storage at Hitachi Global Storage Technologies, and alternative nanofabrication techniques for non-volatile memories at Western Digital. He earned his Ph.D. in physics from Vanderbilt University in 2003, and worked as a postdoctoral researcher at Cornell and IBM before joining Hitachi Global Storage Technologies in 2006.

He shares his perspective in this Q&A.

Q. *How will the new CHiPPS Energy Frontier Research Center advance microelectronics?*

Ricardo Ruiz: The mission of the CHiPPS center is to create new fundamental understanding and control of patterning materials and processes with atomic precision. The goal is to enable the large-scale manufacturing of next-generation microelectronics. To unpack that a little bit, that means that our focus lies in the scientific exploration of an advanced method known as extreme ultraviolet (EUV) lithography.

EUV lithography is key to creating integrated-circuit patterns on the scale of a billionth of a meter in the materials that are used to manufacture advanced microchips. It's the latest advance in lithography, a technique that uses light to print tiny patterns in silicon to mass produce microchips.

Over the past five decades, lithographic techniques have progressively evolved from the use of light in the visible range, where wavelengths are as small as 400 nanometers, to the latest advance: the extreme ultraviolet range with short wavelengths of 13.5 nanometers, about 40 times smaller than the wavelengths of visible light. Such advances in lithography have enabled the use of smaller and smaller wavelengths to fabricate smaller, denser microchips.

EUV lithography was just recently introduced in the production of microchips in 2019, and it still faces multiple challenges, particularly in the development of advanced patterning materials suitable for high-resolution and high-throughput manufacturing processes using light in the form of EUV radiation. The light-sensitive chemical films called photoresists or "resists" in use today for microchip production do not efficiently absorb EUV radiation, and little is known about how these photoresists interact with EUV light.

And that's where we come in.

At CHiPPS, we are taking this opportunity to design new photoresist materials specifically designed to work with EUV radiation. We aim to tackle fundamental scientific challenges to better

Members of the Center for High Precision Patterning Science (CHiPPS), a DOE Energy Frontier Research Center. (Photo Credit: Marilyn Sargent/Berkeley Lab) .

understand and control the chemical reactions arising from the interaction between EUV radiation and resist materials. These tiny, but localized, chemical changes inside the resist is what enables the fabrication of smaller patterns to print, for example, smaller transistors, facilitating the production of faster and denser microchips.

Q. *The microelectronics industry already has a wealth of 50 years of experience in lithography. How is the CHiPPS EFRC's approach to lithography different?*

Ricardo Ruiz: EUV radiation is fundamentally a very different light from the previous generations of light that the chip industry had used for the past 50 years.

And it wasn't too long ago when the chip industry used deep ultraviolet light (193 nanometers) to print transistor patterns on silicon, a key component in chip production.

EUV lithography uses a wavelength of light that is only 13.5 nanometers. That's a factor of 10 smaller than the previous generation, which makes EUV photons 10 times more energetic.

Unfortunately, conventional deep UV photoresists are very poor absorbers at EUV wavelengths. Furthermore, when EUV light does get absorbed, its high-energy photons kick electrons off the resist and substrate materials. This in turn pushes other "secondary" electrons around in a cascading event. And that is the issue with the photoresist materials in use today: It is the secondary low-energy electrons that are making chemical changes in the photoresist.

CHiPPS researchers Areza Sumitro and Beihang Yu in the nanofabrication facility at Berkeley Lab's Molecular Foundry." (Photo credit: Marilyn Sargent/Berkeley Lab.)

This is poorly understood and poorly controlled, because there is very little knowledge of how materials behave at the atomic level when they interact with EUV light.

This is a challenging problem to solve, but fortunately we have the strength of having a big interdisciplinary team. We paid special attention in selecting the brightest minds in all aspects of patterning science with a proven record of collaboration and team science.

Our interdisciplinary team of 13 principal investigators span the scientific disciplines, from synthetic chemistry to nanomaterials and physics to computer modeling. Our scientists come from some of the nation's leading national labs and universities, including Berkeley Lab, Stanford University, San José State University, UC Santa Barbara, Argonne National Laboratory, and Cornell University.

Everyone in the team is very excited to work together. We're exploring new physics and new chemistry, and we all have the same goal: Pushing the boundaries of patterning materials so we can help the microchip industry stay ahead of Moore's Law. (Moore's Law is named after Intel co-founder Gordon Moore, who declared in 1965 that the number of transistors placed on a chip would double every two years until the technology reached its limitations in miniaturization and performance.)

Q. *How are CHiPPS and Berkeley Lab uniquely positioned to advance EUV lithography with the microchip industry?*

Ricardo Ruiz: As a multidisciplinary national lab, Berkeley Lab offers a combination of research facilities; access to big, scientific instruments; and expertise in chemistry, materials science, physics, engineering, and computing – and proximity to industry and universities – that can't be found anywhere else.

Berkeley Lab is also home to the Center for X-Ray Optics and the Advanced Light Source.
The Advanced Light Source (or ALS) is a synchrotron user facility that produces very bright X-rays, including soft X-ray and extreme ultraviolet light, that are critical to characterizing photoresist materials. In very close proximity to the ALS is the Center for X-Ray Optics (or CXRO), which is dedicated to advancing science and technology by using short wavelength optical systems and techniques with a special emphasis on EUV technology.

CXRO houses a unique lithography platform called a "high numerical aperture EUV exposure tool," which offers a resolution capability that is significantly better than current state-of-the-art EUV platforms. CXRO is currently the only research facility in the world where industry partners can use this tool to test new patterning materials.

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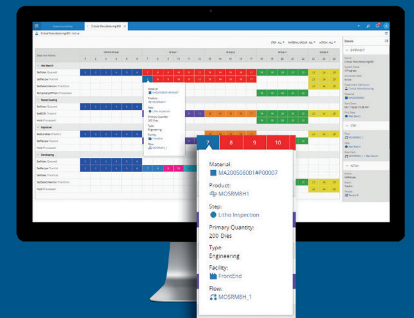

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There are only a few places in the world where people can do research with EUV light because it's very expensive and very difficult to make EUV light and EUV optics. For example, a first-generation EUV lithography tool costs more than $100 million. That's not something that research labs or even microchip industries can afford to buy just for research.

CXRO is strategically positioned to help chip manufacturers like Intel and Samsung do EUV lithography research without having to buy a $100 million EUV lithography tool.
Additionally, CXRO, along with its close neighbor the ALS, offers unique capabilities and scientific expertise that are critical in understanding how EUV light interacts with photoresist materials. But microchip patterning science requires much more than EUV exposure and characterization capabilities. We also need specialized instruments and world-class experts in materials synthesis.

To that end, we will heavily rely on Berkeley Lab's Molecular Foundry. Its Organic and Biological Nanostructure facilities are instrumental to making new nanostructured patterning materials that are more sensitive to EUV light.

The Molecular Foundry is also home to a 4,850 square foot clean-room facility dedicated to patterning, nanofabrication, and molecular self-

How mentoring can advance the next generation of scientists and engineers

IF YOU ASK CHiPPS Director Ricardo Ruiz, mentoring the next generation of scientists and engineers is just as important if not more so than advancing EUV lithography research for next-generation microelectronics. And that comes from someone who knows firsthand how mentoring can inspire and transform a budding interest in STEM (science, technology, engineering, and mathematics) into a flourishing and rewarding career.

"Since joining Berkeley Lab, I've been mentoring a good number of student interns in addition to the postdocs in my group. Mentorship has always been important to me. Over the years I've been lucky to work with inspiring mentors who shaped my career and now I try, as best as I can, to offer a similar experience to the next generation of scientists who bring a fresh perspective and energy for driving scientific progress. Working with them at Berkeley Lab has been a rewarding and fulfilling experience. Mentorship is a responsibility I take seriously, as it promotes a virtuous cycle of collaboration and knowledge while shaping future leaders in science," he said.
Below is an excerpt of our discussion with Ruiz on the importance of mentoring in STEM.

Q. *You have a Ph.D. in physics, and you're a leading expert in nanopatterning for microelectronics. Is microelectronics research something you dreamed of pursuing when you were growing up?*

Ricardo Ruiz: Not at all. When I was in high school, I thought I wanted to be an astronomer, but it was later during college and graduate school when I discovered my passion for physics, materials science, and soft matter through a project on organic electronic materials. These are an exciting class of electronic materials that can be deposited onto flexible or soft substrates, enabling flexible electronics and wearable technologies.

After I completed my Ph.D. at Vanderbilt, I continued to specialize in organic electronic materials as a postdoctoral scholar at Cornell University. After that I spent 15 years in the private sector at IBM Research, Hitachi Global Storage Technologies, and most recently at Western Digital where I did research on various nanofabrication and self-assembling techniques for semiconductor, magnetic storage, and memory technologies until I joined Berkeley Lab at the end of 2019. As I look back, it is easy to recognize that much of my career trajectory was shaped by influential and thoughtful mentors along the way who helped me build a career and get to where I am today. Mentors can make the biggest impact in motivating people to stay in STEM careers and do good quality science that matters not only for personal gain but for the good of society. I was very lucky. I benefited from having excellent mentors who served as role models for me throughout my career.

At CHiPPS, we all value the importance of mentorship, and that's why we pay special attention to creating opportunities and equitable experiences for the postdocs and students working at the center. We are also excited about the student training program we launched together with San José State University. Through this program, four students have the opportunity to learn and interact alongside Berkeley Lab scientists during the summer.

Q. *How does your experience in the private sector shape your approach to scientific research and leadership at Berkeley Lab?*

Ricardo Ruiz: My experience in the private sector has turned out to be a nice complement to my work at Berkeley Lab.

In the private sector, researchers are very focused on applications. And in my work at Berkeley Lab's Molecular Foundry, we are always trying to look for ways in which science can advance an application, even if it's fundamental science.

Another experience that shaped my career considerably in the private sector was the focus on team effort. Berkeley Lab is the birthplace of multidisciplinary team science, so it's a perfect fit.

25mm x25mm

Long range profiling for CMP characterization

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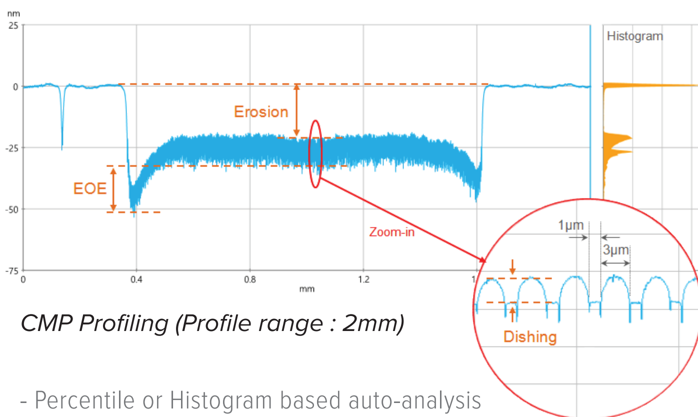

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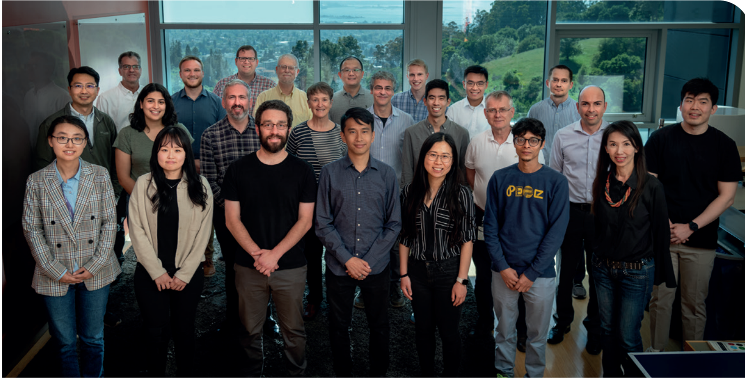

Members of the Center for High-Precision Patterning Science (CHiPPS), a DOE Energy Frontier Research Center, photographed at the CHiPPS all-hands meeting at Berkeley Lab last May. Ricardo Ruiz is in the middle row, second from right."(Photo credit: Thor Swift/ Berkeley Lab).

assembly. This facility is critical to developing atomically precise pattern-transfer techniques for new EUV materials.

In our pursuit of a comprehensive understanding of all chemical and physical phenomena, modeling and simulation research around EUV patterning is key. This work is supported by the computational capabilities and expertise at Berkeley Lab's Chemical Sciences and Energy Storage & Distributed Resources divisions together with computing resources at the Department of Energy's National Energy Research Scientific Computing Center (NERSC), which is also located at Berkeley Lab.

Q. ***Pushing the boundaries of Moore's Law was once considered unthinkable. How does the CHiPPS team aim to advance EUV lithography research in order to stay ahead of Moore's Law?***

Ricardo Ruiz: Developing high-performance materials capable of high EUV light absorption and precise lithography patterns formed through controlled, atomic-level chemical reactions are two goals that are crucial to our successfully advancing the limits of Moore's Law.

To achieve these goals, our CHiPPS researchers are making sure that we take advantage of working together in a team that is larger than the sum of its parts.

Brett Helms (Berkeley Lab), Chris Ober (Cornell), Rachel Segalman (UC Santa Barbara), and Stacey Bent (Stanford) are developing new photoresist materials that are specifically tuned to work with EUV radiation. In a multi-prong collaboration across institutions, Brett leads efforts on a new class of materials called organo-metal halides.

Chris and Rachel are advancing bio-mimetic, sequence-specific polymers. And Stacey is pursuing "dry" resists synthesized from layered organometallic materials.

At CHiPPS, we are also exploring "bottom-up" hierarchical materials and processes as a potential solution to overcome the limitations of photoresist materials. For example, Argonne's Paul Nealey is focused on developing highly customizable block copolymer materials for lithographic features as small as 4 nanometers. (To put that in perspective, a sheet of paper is about 100,000 nanometers thick.) Paul, Stacey, and I are collaborating to employ various self-assembly and pattern transfer methods.

Our teams are also collaborating to understand the thermodynamics of self-assembling polymers on "noisy" or defective EUV patterns. Additionally, we are working with Paul Nealey and CXRO Director Patrick Naulleau to identify and minimize defects in photoresist patterns. A joint effort – led by Stacey Bent's group at Stanford with my group at Berkeley Lab and Paul Nealey's group at Argonne – focuses on an area-selective deposition process that precisely transfers circuit patterns from the photoresist to the silicon wafer.

At CHiPPS, computer modeling and simulations are cornerstones to understanding the chemical and physical phenomena behind pattern formation with EUV radiation. Sam Blau and Frances Houle of Berkeley Lab are leading computer modeling and simulation experiments that aim to understand how patterning materials react to EUV light and low-energy electrons. Their work will also help us better understand the chemical and physical processes that take place after light exposure.

They are collaborating closely with Cheng Wang, Oleg Kostko, and Patrick Naulleau of Berkeley Lab and Dahyun Oh of San José State University to use relevant experimental data in their modeling. The team will also provide input to the synthesis efforts of Brett Helms, Chris Ober, Rachel Segalman, and Stacey Bent.

To effectively monitor and validate our materials and processes, CHiPPS will rely on a comprehensive characterization suite developed by Cheng Wang, Oleg Kostko, Patrick Naulleau, Weilun Chau (also of Berkeley Lab), and Dahyun Oh. This suite allows us to image buried features in resist materials, assess the impact of EUV exposure, study secondary electron behavior, measure interface roughness, and understand the role of interfaces in the patterning process.

As you can see, our highly integrated, collaborative team is our greatest asset. We are all motivated by the exciting developments of patterning science. And we are well aware that the challenges in front of us can only be overcome by team science.
The Advanced Light Source, Molecular Foundry, and NERSC are DOE Office of Science user facilities at Berkeley Lab.

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Taking testing to the next level

EMANUELE BARDO, VICE PRESIDENT FOR THE SEMICONDUCTOR AND MEMS TEST BUSINESS UNIT AT SPEA, talks to Silicon Semiconductor Editor, Philip Alsop, about the company's Automatic Testing Equipment expertise as it relates to the semiconductor sector, highlighting technology innovations, alongside the company's future growth plans.

SPEA was founded in North Italy in 1976. The founder worked for the famous Italian company, Olivetti, and later on with General Electric, before founding SPEA. The initial business was related to the production of ICT testers - testing of assembled PCBA boards.

In 1993, SPEA produced its first semiconductor tester, that went into the market a year later. Being European, the first installed base was with the major semiconductor IDM companies here in Europe. The company's first high volume semiconductor tester went out in the market in 1999 and later on with a second version in the 2002/2003. SPEA then penetrated the sensors' market in 2003/2004. At the time, there were not many applications. One early successful application was the Nintendo Wii, that contained the first three axial accelerometers - which were tested and calibrated with SPEA machines. Since then, the consumer business has driven a lot of innovation in the sensor business, followed by the automotive industry.

In 2009/2010 SPEA started to heavily penetrate the high voltage and high current business that today represents one of the biggest revenue shares of the company, driven again by automotive and electric cars. And in 2018, SPEA was able to introduce the second generation of what it calls the DOT device-oriented tester. And this has been one of the biggest 'revolutions' in the industry, introducing a new way of conceiving the ATE that represents an extremely successful business case for a lot of customers in Europe, in the United States, in Asia - in Korea, in Japan and in mainland China. Today, the company has a turnover that is over 200 million euros, and the target is to break the 300 million euro barrier in the next two years.

In terms of how the company positions itself within the automatic test equipment market, it is currently in the number four position. However, the company is dominant in two major markets. In the MEMS sensors market, the company has more than 60% of the market, and also has a significant presence in the high voltage and high current semiconductor product market. The big news is that, on the analogue mixed signal side, that was dominated by its two major competitors in the past, SPEA's market share has more than tripled in the last four years. With the company's machine designs bringing down the cost of test in a significant way, based on its four year roadmap, SPEA expects to move up to the overall number three market position.

In terms of how SPEA distinguishes itself in the market, what it does differently from the competition when it comes to semiconductor testing, Emanuele explains: "Measuring a voltage and measuring a current is equal for all the ATE vendors. Of course, if you have to measure five volts with a certain accuracy, or you have that spec, or you don't have, the key is how you do it and how you make this cost efficient. To make things cost efficient today, you have to work on two major topics - design architecture and distributed intelligence in the machine. So, the architecture of the machine brings to two major advantages - to have an equipment that is extremely modular and configurable in a way that the overall Capex cost is significantly lower than the competitor. The second topic is how you design your instrument, your backplane in order to get the

➤ The growing need for reliability in power semiconductor devices brought SPEA to develop a dedicated test system, able to fulfill the requirements to perform thorough AC, DC, ISO tests on the devices.

highest multi-site efficiency - semiconductor tests require multi-site testing for cost proposal. So, the key question is how much is the percentage of test time increased every time you add one site during the parallel test? So, if your efficiency is 99, that's an okay number, but if your efficiency is 99.95%, that's a different number and that represents cost saving. So, these two elements are driven by the architecture of this test."

Emanuele continues: "The other topic is the intelligence that you put inside the machines today. This type of equipment - they use their own intelligence to self-control their own calibration data in order that automatically the machines can recalibrate on the fly in the spare time they have on the production floor. This is coming away from the old model of working where you have the equipment and the tester operating for a certain amount of hours then going into a preventive maintenance operation, then doing diagnostic and calibration and so on.

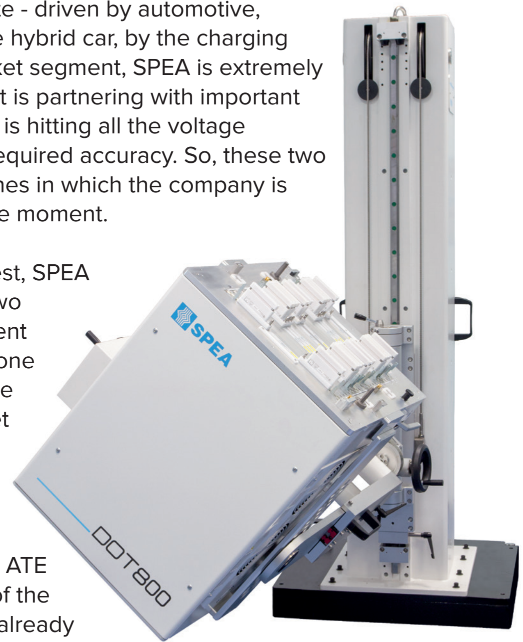
"The big advantages that we are introducing are exactly these three, the architecture, multi-site efficiency and intelligence in the equipment. Overall, this represents cost saving. And when you start to slice the cost in different portions and you act on all of this in parallel, you are able to cut those costs by a significant percentage. That's the competitive element and why a big customer would consider changing their test platform."

In terms of SPEA's product and services portfolio, the DOT tester is the biggest innovation. DOT means device-oriented tester and the name itself represents a big step forward for the company's architecture because the old ATE machines, they used to have purely analogue cards, purely digital cards, single processing cards, high voltage cards and so on. The customer was selecting equipment, it was coming out of the budget and it was demanding their application team to rail out a PCB interface to specialise the tester interface to the product.

With the DOT, SPEA has boards that are themselves configurable. So, the customer knows his product portfolio and he can configure one board with a logic mixing of analogue, digital, signal processing and power in a way that with one card the customer can test one, two, four or eight devices in parallel and then populate the tester with the required number of the same card. This is the big cost advantage and the technical element that brings us to multi-site efficiency. So, this is one of SPEA's major elements on the mixed signal tester side.

The company also has a very strong technological roadmap on everything relating to power - high voltage, high current. This market, that was a very low market until three years ago, is now booming. And even during 2023, in a year where generally the semiconductor industry market is going down, the only market segment that has two-digit growth is power and discrete - driven by automotive, by the EV car, by the hybrid car, by the charging stations. In this market segment, SPEA is extremely advanced because it is partnering with important IDM companies and is hitting all the voltage standards and the required accuracy. So, these two segments are the ones in which the company is investing more at the moment.

At the SEMICON West, SPEA introduced one or two innovations. The event was a very positive one for the company - the United States market that really 'requires innovation from a new supplier coming out from the monopoly of the old ATE suppliers'. In terms of the architecture aspect already mentioned, SPEA has developed ultra-high speed digital pins that will become an option for the low cost mixed signal tester, with the concept that you can configure one of the cards partially with a high speed digital pin. In terms of all the products that you have today, they have high speed interfaces like Ethernet, HDMI and so on.



The innovative DOT test platform addresses the test requirements of applications like BMS, SerDes, OpAmp, PMIC, MEMS and sensors, Microcontrollers.

To bring the cost of test low for high-speed digital testing has always been a big challenge and with this type of innovation, SPEA offers the option to configure a channel board with low speed digital, high speed digital, analogue and signal processing, at a very competitive cost . And this is related to the mixed signal.

The other big topic that the company discussed at SEMICON West was the emerging needs of the silicon carbide product testing, where the voltage ratings are going above 3000 volts and as possible roadmap above 6000 volts.

Another significant innovation that SPEA introduced recently focuses on auto maintenance. Emanuele explains: "The old ATE systems, they work in a way that they operate a certain amount of hours, then they go into a preventive maintenance mode and the machine has to do calibration adjustment and eventually also diagnostics. What we have been able to do is to know when the tester has idle time. If you do a calculation, this time is very significant during one month. Well, we are capable to understand when the tester is idle for a certain amount of time.

"At that point, we can run a subset of our calibration programme in order to verify the drift of the calibration data. We are able to keep track and memory of this data over the time. And we are capable to predict when an instrument potentially can go out from the calibration thresholds. And at

that point, when we have that prediction, instead of setting the tester in PM with an appropriate margin, we are able to auto recalibrate the machine."

This auto maintenance/calibration innovation is industry 4.0 in action – making the tester smart enough so it can automatically control drifting of the data and eventually recalibrate.

Another function that SPEA has introduced in terms of Industry 4.0 is to develop a tester that is capable of calculating the lifespan of relays. All ATE is full of mechanical and solid-state relays. These are parts that sooner or later will fail because they have a certain lifetime. Being able to understand what is the lifetime of the consumable parts that are mounted in a tester and being able to predict end of life represents a very important advance, because it helps customers to reduce downtime and to improve their manufacturing efficiency.

And from Industry 4.0 to artificial intelligence and machine learning is but a small step, as Emanuele acknowledges: "AI will bring a lot of potential in the future and I think the potential will be for a supplier like us to help our customers with migration of the test programme and the test application from one machine to another. As I said earlier, we are coming later to the market and we offer a competitive advantage, but one of the big headaches for our customer is oh, we have already many products running on machine A, we need to convert on the SPEA. Using AI to help during this test programme migration will be a big opportunity in the future.

"This will be the next step forward where we can give a huge advantage to our customer. And our design team and our software team are working on this topic, because it's not only matter of the AI itself, but it's also a matter of how we design our software architecture to make that friendly in a way that the migration can be done automatically using AI tools with the appropriate level of confidentiality the customer wants to have."

➤ The DOT800 test platform incorporates the elements of Industry 4.0, in terms of auto-maintenance capabilities, data collection and analysis, and artificial intelligence in the service of an easy test program migration from legacy testers.

While the ubiquitous confidentiality agreements which surround the semiconductor industry prevent Emanuele from sharing details as to how SPEA is helping specific companies, he is able to give a high-level view of the type of work which is being undertaken.

Emanuele says: "In the last two years, we have played an extremely important role in everything to do with BMS (Battery Management System) testing. We have helped a major customer to reduce more than 50% of their operating cost thanks to the use of dedicated instrumentation, with extremely high accuracy, that we have developed for this business. You can understand that doubling the output with our existing machine, together with all the advantages I mentioned before, is a huge cost saving, floor space saving and the like. This is one of the biggest successes that we have achieved.

"We have also supported another major customer with sensor testing, where they were able to gain an extremely big market share thanks to our multi-site capability that was ten times higher than our competitor. These are two very nice examples of partnerships that we have built over the years and which have brought a lot of advantages to two of our major customers."

Looking to the future, Emanuele expects SPEA's organic growth to continue across all sectors. The rate of growth is biggest in the analogue mixed signal space and in the power space – they are very big market segments and also the market segments where SPEA is focusing introducing the majority of its innovations.

The sensor business is still growing, but not at the same rate of previous years. That said, the sensor business is growing in an impressive way in mainland China where SPEA plays a dominant role and has recently set up partnerships.

The high growth in the analogue mixed signal and the high-power segments brings many challenges for the company. SPEA has recently approved a massive investment that will increase capacity by more than two and a half times the current output over the next two years and beyond.

Emanuele summarises: "This is a massive investment, not only in our headquarters here in Italy, but all over the world. Because, of course, we are growing our organisation in all the countries from Asia, China, Southeast Asia, United States and Europe. By growing our installed base, our customers need faster answer times, they need application capability, they need service capability, they need local repair centres. That's where all the investments will be focused - to be as close as possible to the customer."

In terms of the technology future, SPEA has a five year roadmap, from both a hardware and software perspective. The company shares its plans with, and receives regular feedback from its major customers as to their own plans – where they are going. It also works with individual customers to validate innovations. Emanuele explains: "Recently, we have also introduced the following practice: once we introduce a new piece of equipment or a new equipment feature, we work together with a customer to identify one of their products that has a specific technical requirement for the innovation and we work together to shorten the validation time and to speed up time to market in an improved way with a fully validated solution."

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Increase manufacturing quality with reliable liquid flow measurement

Reliable liquid flow measurement plays an important role in semiconductor process management. Flow meters can effectively monitor wet processes to ensure a constant flow of the liquid or manage volume dispensing at the points of use. By implementing an accurate and reliable flow measurement, fabs can significantly improve their process quality.

BY ANIKA BAUMHAUER, INTERNATIONAL STRATEGY AND SALES MANAGER AT SONOTEC

REPRODUCIBILITY and maintaining strict quality control throughout the entire wafer manufacturing process are top priorities in the semiconductor industry. Thus, stable and highly accurate flow measurement is essential for many semiconductor manufacturing steps. Non-contact clamp-on flow meters have proven to fulfill this demanding task reliably. The ultrasonic sensors measure through the wall of the tube or pipe and substantially reduce the risk of contamination or leakage of hazardous fluids. With the SEMIFLOW flow meter series, the ultrasound specialist SONOTEC has developed metal-free contactless flow meters particularly designed for the requirements in the semiconductor industry – also for hazardous environments. The compact sensors with integrated electronics board are available in multiple sizes suitable for all common rigid plastic tubes and pipes used in fabs. In order to guarantee continuous high product quality, a tight liquid flow monitoring is necessary. From liquid storage containers to the application in the process, the liquid flow must be monitored and tracked, e.g., to measure the volume flow in a transfer line or to control the volume output at the points of use. Ultrasonic flow meters can be implemented in low- and high-volume manufacturing settings and used reliably regardless of the type or blending of the chemicals in the tube.

Reliable monitoring of slurry consumption in CMP

Chemical-mechanical planarization or polishing (CMP) is one of the leading technologies to manufacture state-of-the-art microelectronic components and micro-electro-mechanical systems (MEMS). In order to produce modern integrated circuits with multiple wiring levels and smallest line widths, highly precise flat and smooth surfaces are needed. CMP processes have become also very important in the finishing of wafer-thinning

processes and the production of vertical contacts through the silicon wafer. Since the industry is persistently looking for further ways to reduce the structure width, the requirements in process design are becoming more detailed and stringent. Hence, CMP processes are getting more complex and quality standards grow constantly. As a consequence, process parameters have to be monitored very closely at various steps to avoid deviations in product quality that might lead to costly failures.

In CMP processes, flow meters accurately monitor the dispensing of slurry on the polishing plate. Additionally, they are installed to count the volume flow to calculate the amount of slurry used at this process step. Flow sensors also monitor precisely the consumption of slurry in supply tanks or in the pipe system to determine the transfer volume. Every fab uses its own slurry blending. Non-contact flow meters are well-suited for contamination-free flow or volume measurement of liquids, work independently of the slurry composition and are free of wear and tear.

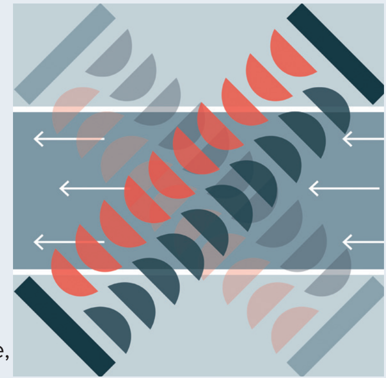
Efficient slurry blending and dispensing at each point of use

Large semiconductor manufacturing sites commonly implement slurry mixing and blending systems to ensure optimal slurry concentration for the specific process requirements. For the slurry preparation, the different components are mixed with DI-water. With regard to achieve exactly the predefined slurry concentration at the point of use, highly accurate flow meters monitor the volume flow rate of the components from buffer tanks to the mixing container. This real-time control with contactless flow sensors ensures proper blending of the chemicals at high production rates and specific mixing ratios.

Automatic slurry dispense platforms guarantee an efficient slurry distribution during continuous operations in CMP manufacturing environments. In order to have a redundant system monitoring, non-contact flow meters are installed in addition to each distribution pump to make sure that the defined product quality remains constantly at the same high level. Contactless ultrasound flow measurement guarantees that the slurry or chemical in the pipe or tube is not contaminated or influenced by the measurement device. Additionally, the flow sensor can conveniently be replaced or moved to another position without having to intervene in the closed pipe system.

By monitoring the slurry composition and concentration with automatic dosing and blend correction throughout the entire pipe system, precise metrology options are used. Via additional tank or mixing stations in the fab, blend corrections can be processed. For this step, highly accurate and reliable flow meters control the related pumps. Thus, the exact slurry blending can be ensured and efficiently used. Additionally, flow meters guarantee both system and component redundancy throughout the entire wafer manufacturing process.

Engineering Principle of Ultrasonic Flow Meters



Ultrasonic transducers are the heart of any ultrasonic flow sensor. They consist of piezoelectric ceramics or composites that expand or contract when a DC voltage is applied, depending on the sign of the voltage (inverse piezoelectric effect). By applying an alternating voltage, the piezoelectric expands and contracts periodically and emits a sound wave corresponding to the excitation frequency. This sound wave is sent out as a pulsating ultrasonic beam from an excitation transducer and is detected by a receiving transducer. The signal is evaluated electronically and output via various signal outputs (digital + analog).

Transit-Time Technology

There are different ways how ultrasonic signals can be utilized to calculate flow rates. SONOTEC's SEMIFLOW sensors work on the basis of transit-time technology.

With this method, the transit-times with and against the flow direction of a medium are measured with high precision by time-to-digital converters. In the direction of flow, the transit-time of an ultrasonic wave is shorter than against the flow. The time difference combined with geometrical information of the tubing allows to determine the flow rate and volume. This method causes neither a pressure drop in the tube nor a risk of leaks, as it can be applied in a completely non-invasive and non-intrusive manner. When appropriately calibrated, transit-time can work on almost all liquids, independent of viscosity, density, color or electromagnetic properties of the fluids. Ions and particulate matter are not required to calculate the measurement. Additionally, the contactless measurement method does not cause any wear or tear for the sensor. Thus, the clamp-on ultrasonic sensors are maintenance-free.

In large manufacturing facilities, transfer pumps control the slurry supply via fab-wide loop pipe systems. For redundancy reasons, implemented clamp-on flow sensors monitor the liquid flow or volume in the pipe system.

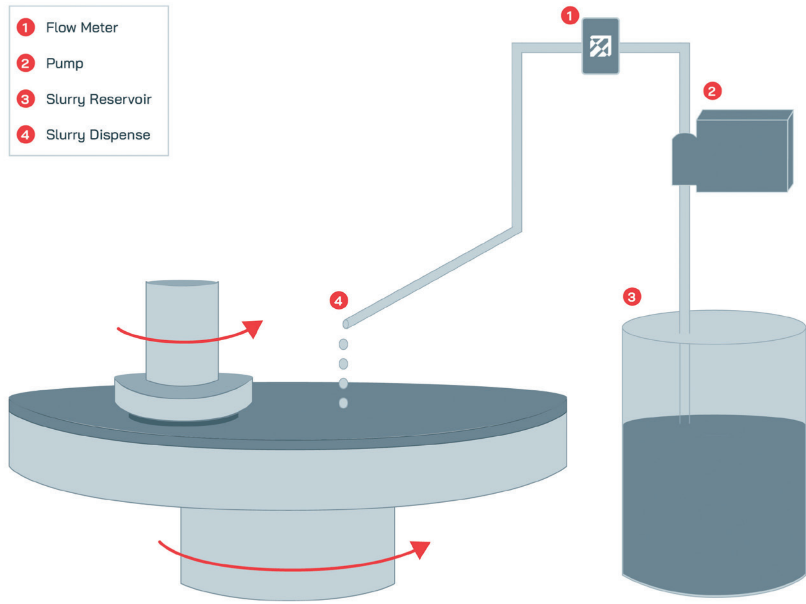
Precise distribution of photoresist in lithography applications

In semiconductor manufacturing, the process of photolithography describes the processing of circuit board designs on silicon wafers by means of light. The process starts with coating the wafer with a chemical layer called photoresist. The layer of the photoresist must be extremely precise. For the exact volume dosing of these photoresist layers, highly accurate flow meters are implemented to redundantly monitor the pump behavior. By implementing non-contact ultrasonic air bubble detectors from SONOTEC, even smallest air bubbles can be detected that might occur in the coating

Fundamentals on Chemical-Mechanical Polishing / Planarization (CMP)

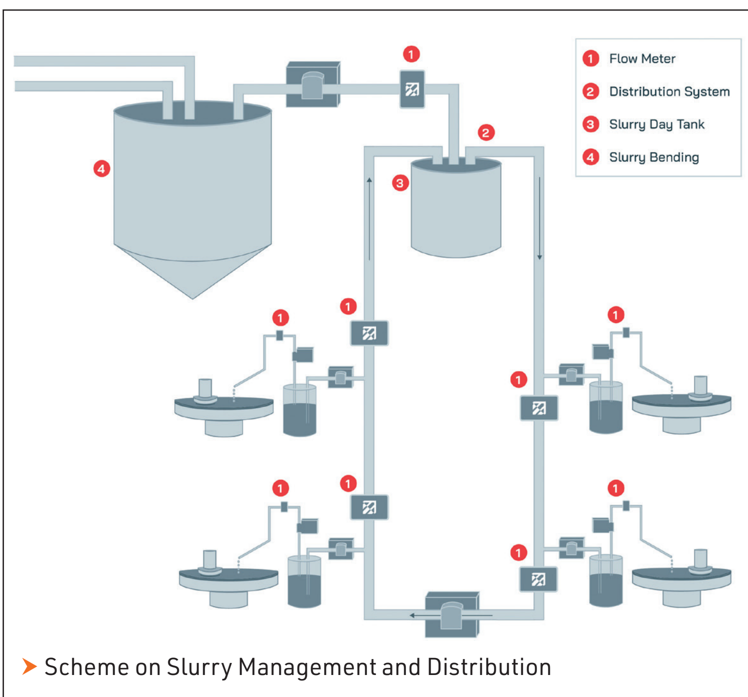
CMP is a key technology in any semiconductor fabrication. It is applied in both, substrate as well as device fabrication. Advanced semiconductor devices easily need more than 30 CMP processes to get to its final stage. CMP aims on perfect smooth surfaces with almost no remaining topography.

To that, the wafer surface is polished using a slurry and a polish pad. Slurry describes a chemical fluid that contains abrasive nanoparticles dispersed in acidic or basic solution. During the CMP process step the wafer is pressed on the rotating polish pad, while slurry is continuously dispensed. Specifically, the slurry chemically modifies the uppermost surface layer, which is then mechanically cracked and removed by slurry abrasives.



Scheme on Chemical-Mechanical Planarization

process. In a further step, light passes through a photomask and creates an optical image of the circuit layout on the wafer. The generated light reacts with the photoresist which is washed away in the next process step. Thus, the underlying oxide layer is exposed. By using certain acid baths, further oxide and residues of the underlying silicon layer are removed. As the acid baths have to be kept with an even filling level, non-contact flow meters precisely monitor the filling of the wet benches. Thanks to the non-contact measurement method it is not necessary to replace the sensor after cleaning procedures or servicing. The described process is repeated several times with different combinations of chemicals and masks, building up the layout structure of the later processor. Finally, the doping process is applied to the exposed silicon, changing its electrical properties. Current photolithography processes often include around 30 or more separate masks to layer circuit patterns on top of each other.



Scheme on Slurry Management and Distribution

Increasing manufacturing effectiveness and yield with fab-wide liquid transport management

Considering the efforts and costs of recently planned and established new fabs, it is crucial to implement and maintain efficient operations, keep equipment uptime as high as possible, and optimize the yield of high-quality products. Installing highly accurate and reliable flow meters for liquid process management as part of a tight production control system improves manufacturing efficiency, reduces manufacturing costs, and avoids downtime in the production cycle.

Latest sensor technology offers real-time data that gives feedback for real-time control systems to reduce cycle-time and improve yield. Independent from flow range and flow volume, SONOTEC offers a broad portfolio of compact ultrasonic flow meters and air bubble detectors suitable for various tube and pipe sizes to enable a fab-wide flow control system – also in hazardous environments.

The non-contact flow sensors operate cost-efficiently and reliably in low volume or bulk chemical distribution systems. Subsequently, highly reliable continuous chemical fab supply chains can be established to increase efficiency and yield.

ROUNDTABLE

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- Moderated by an editor, Phil Alsop, this can include 3 speakers
- Questions prepared and shared in advance
- There would be an opportunity to view and edit out any unflattering bloopers

This event would be publicised for 4 weeks through all our mediums including:

- A banner on the Silicon Semiconductor homepage for 8 weeks
- 4x weekly dedicated HTMLs
- 4x news pieces which would also appear on the weekly e-newsletters
- Promoted through our social media platforms for 8 weeks (pre and post event)
- Available as an on-demand asset through all mediums
- All registered attendees' details would be made available to you

Cost: €5995

Contact: Jackie Cannon at jackie.cannon@angelbc.com

ANGEL EVENTS

Revving up: the intersection of semiconductors and the automotive industry

The convergence of the semiconductor industry and the automotive market has brought about a wave of innovation and change. Over the few years, these two sectors have become more interconnected with semiconductors serving as the foundation for modern advancements in automobiles.

BY **SHALINI NAGAR, JR. CONTENT WRITER AT RESEARCH NESTER PVT**

WHETHER it's improving safety and performance or enabling self-driving cars semiconductors are, at the forefront of shaping the future of the automotive industry. In this article, we will delve into the role played by semiconductors in reshaping the automotive landscape.

Semiconductor industry overview

The semiconductor industry has been at the forefront of innovation for many years playing a crucial role in advancing fields like computing, telecommunications, and consumer electronics. With a market worth exceeding USD 500 billion and an estimated annual growth rate of 6.5%, it holds significance globally.

Semiconductors are building blocks in electronic devices that form the foundation for microprocessors, memory chips and other essential components. Since its inception in the mid-20th century this industry has experienced growth fueled by advancements in manufacturing processes and design techniques. Nowadays semiconductors are utilized in a range of products including smartphones and automobiles with continuously increasing demand, for these components.

Automotive market overview

The automotive industry has made progress since the invention of the first car in the late 1800s. Today, it is a sector that employs millions of people and generates billions of dollars in revenue annually. In times there has been substantial growth in the automotive market driven primarily by emerging economies like China and India. It is predicted that global sales of passenger cars will reach 100 million units by 2025.

A consumer's view of the automobile

Automobiles have become a part of our everyday lives providing us with the convenience of efficient transportation from one place to another. This is particularly vital in cities where access to public transport may be limited. Additionally, as the global

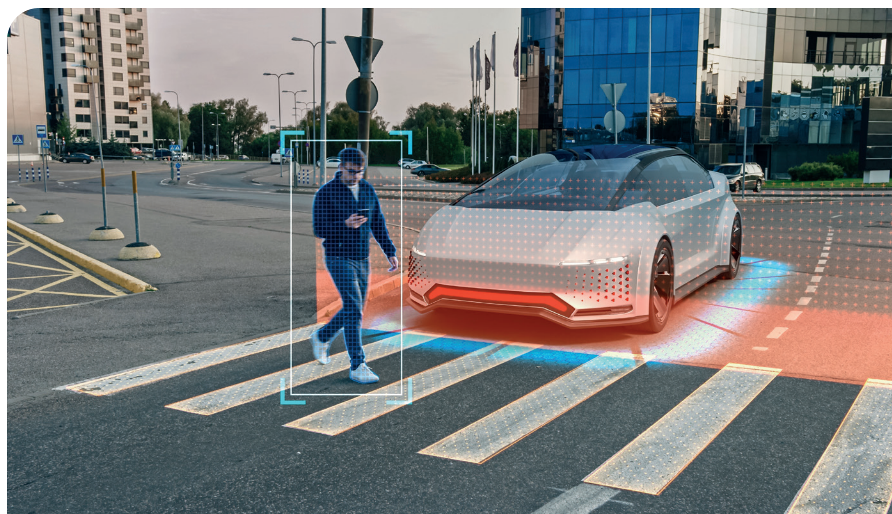
population continues to rise there is an increasing demand for cars making them a crucial element of our transportation infrastructure. Presently there are over 1.4 billion motor vehicles, on roads and this number is projected to grow to 1.9 billion by 2035. Passenger cars account for 75% of these figures while light commercial vehicles and heavy trucks, buses, coaches, and minibuses make up the remaining 27%.

Automotive manufacturers strive to develop vehicles that offer safe performance as they aim to provide customers with peace of mind and ensure their products withstand the test of time. That's why auto companies invest resources in researching, designing and testing their vehicles to ensure they meet the most stringent safety and reliability standards.

The evolution of semiconductors in the automotive industry

Semiconductors play a role in automotive electronics, including powertrains, infotainment, and safety systems. Therefore, semiconductors are vital for the operation of the automobile industry. Here are a few noteworthy developments, in semiconductors that are revolutionizing the sector.

- **Better Connectivity:** Our vehicles now have functionalities such as GPS-based route mapping, real-time traffic updates, and alerts for red lights. Additionally, they offer features like parking assistance and all the essential tools we require while driving. The semiconductors used in legacy nodes are specifically designed to handle the tasks involved in processing data from different sensors in the vehicle. This data is then utilized to make adjustments, to the existing systems enhancing their performance and ensuring a secure and dependable driving experience.
- **Performance Optimization:** Semiconductors have been instrumental in improving the performance of cars. Advanced engine control units (ECUs), with microprocessors are used to enhance fuel efficiency and minimize emissions. Furthermore, semiconductors enable systems that offer drivers and passengers a variety of entertainment, connectivity, and navigation options. These advancements have elevated the driving experience making it more enjoyable and efficient.
- **Electrification:** The shift towards electric vehicles (EVs) is a significant development in the automotive sector and semiconductors play a crucial role in driving this transformation. The advancement of powertrains, battery management systems, and charging infrastructure heavily depends on semiconductor technology. Additionally, semiconductors are vital for managing the intricate electrical systems, within electric vehicles guaranteeing their safety, efficiency, and durability.
- **Safety Enhancements:** One of the ways that semiconductors have positively impacted the automotive industry is by enhancing safety. Advanced driver assistance systems (ADAS) heavily rely on semiconductor components like sensors, cameras, and microcontrollers. These components play a role in enabling features such as adaptive cruise control, lane-keeping assistance automatic emergency braking, and blind spot monitoring. As a result, vehicles are now equipped with the capability to detect and respond to dangers more efficiently ultimately leading to a reduction, in accidents and saving lives.
- **Autonomous Driving:** The development of self-driving cars would be impossible without the use of semiconductors. These vehicles heavily rely on a range of sensors, processors, and AI algorithms to understand their environment and make quick decisions. The amount of power needed for these tasks is immense leading semiconductor manufacturers to continuously create more advanced chips to meet these requirements. As autonomous driving technology progresses it has the potential to revolutionize transportation by enhancing safety and accessibility.
- **Advanced Driving Assistance:** Various functionalities such as cruise control, braking system (ABS) Voice control GPS navigation OTA updates, active steering, etc. are all dependent on the integration of software within the vehicle. AUTOSAR plays a role in connecting and managing numerous electronic control units (ECUs). It provides a platform that facilitates consistent communication between ECUs and application software. This enables an array of functions to be controlled through a centralized system.
- **Connected vehicles:** Connected vehicles will require internet connectivity in order to receive real-time data about their surroundings like road conditions and traffic information. Additionally, they will need the capability to transmit data to vehicles and cloud servers for effective communication, with other autonomous vehicles and optimization of performance. Semiconductor technology plays a role, in safeguarding the



With advancements, semiconductors have become smaller yet more powerful enabling more efficient and innovative automobile designs and features. They are also integral in powering safety systems and navigation tools that enhance vehicle intelligence and safety

integrity and dependability of data produced by connected cars. Without semiconductors, the data generated by these cars would be exposed to tampering resulting in potentially disastrous outcomes.

- **Mobility as a Service:** MaaS, short for Mobility as a Service is a business model that combines various transportation options like ride-hailing and public transportation into one convenient platform. With an app, customers can effortlessly access and manage all their transportation needs. According to KPMG a significant 70% of Americans reside within a 10-minute radius of an Uber or Lyft pickup point. Not does MaaS offer convenience but it also has the potential to alleviate traffic congestion enhance safety measures and reduce harmful emissions. As the popularity of MaaS continues to grow there will be an increased demand for semiconductors that power the safety features and autonomous technologies in MaaS vehicles. Additionally, these vehicles will need connectivity with cloud services further driving the demand, for semiconductors.

The Future of semiconductors in the automobile sector

Semiconductors play a role in this transition by enabling the creation of smaller more powerful and more efficient hardware and software components. They empower automakers to develop driver assistance systems, electronic control units, infotainment systems and connected services. Moreover, semiconductors are also utilized in driving technology and the advancement of alternative energy sources like fuel cells, batteries and solar cells.

According to a market research report from Research Nester, the Automotive Semiconductor Market is projected to generate a revenue of USD 115 billion by the end of 2035 with an annual growth rate of 10% from 2023 to 2035. Additionally, the market already generated USD 40 billion in revenue in 2022. These figures underscore the role that semiconductors play in revolutionizing the automotive industry. With advancements, semiconductors have become smaller yet more powerful enabling more efficient and innovative automobile designs and features. They are also integral in powering safety systems and navigation tools that enhance vehicle intelligence and safety. In the future, there will be a surge in demand for semiconductors and their solutions. Collaboration, between OEMs (Original Equipment Manufacturers) and automobile manufacturers is crucial to avoid semiconductor shortages down the road. Moreover, reputable organizations and news agencies have projected a future, for the semiconductor industry indicating great opportunities for companies to experience accelerated growth.

Challenges and Opportunities

The semiconductor industry has brought about a wave of automotive advancements but it has also encountered its fair share of challenges. The global shortage of chips in 2020 and 2021 shed light on the industry's vulnerability to disruptions in the supply chain. This scarcity had an impact on the automotive sector causing delays in production and an increase in costs. However, this challenge has also emphasized the importance of diversifying supply chains and boosting semiconductor manufacturing. Both governments and industry leaders have recognized the need for investing in semiconductor production capacity to ensure a supply of chips across industries, particularly in automotive.

Furthermore, the convergence of these industries presents opportunities. With self-driving vehicles gaining popularity there will be a growing demand for advanced semiconductors. This growth will drive innovation resulting in efficient, affordable, and powerful semiconductor solutions. It will also foster collaboration between automakers and technology companies leading to new business models and ecosystems, within the automotive market.

Semiconductor chip shortage: How are auto manufacturers responding?

Automotive news has been dominated by reports of

a decline in vehicle demand during the initial stages of the COVID-19 crisis. This drop can be attributed to the global supply chain disruptions caused by the pandemic in relation to critical components like automotive semiconductors. The demand for these semiconductors has been steadily rising over the few years and the pandemic has only worsened this situation.

To ensure a supply of components original equipment manufacturers (OEMs) have been exploring alternate sourcing models. As a result, stronger partnerships are being formed between OEMs, Tier 1 suppliers, and semiconductor suppliers. These collaborations are expected to benefit the industry in the long term by reducing the risks associated with future shortages. By fostering partnerships, OEMs and other automotive manufacturers can sustain their innovation efforts and remain competitive in the global market. Furthermore, investing in companies that specialize in technologies can serve as a safeguard, against any potential disruptions that may occur in the semiconductor industry down the line.

Conclusion

The relationship between the semiconductor industry and the automotive market is unquestionably interconnected as semiconductors play a role, in driving modern vehicle technology. They have revolutionized the sector by enabling

safety enhancements, improving performance, facilitating electrification, and advancing autonomous vehicle development.

However, the difficulties caused by disruptions in the supply chain have highlighted the importance of building resilience and investing in the manufacturing of semiconductor chips. As the automotive sector continues to evolve it is crucial for collaboration and innovation between these two industries to take place. This will contribute to the creation of more efficient and environmentally friendly vehicles ultimately shaping the future of transportation for future generations. It is impossible to overstate the significance of the semiconductor industry's role in this transformation as its influence, on the market, will undoubtedly increase in the coming years.

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Contamination management solutions from Pfeiffer Vacuum

Pfeiffer Vacuum's many years of experience as a provider of vacuum technology have shaped our know-how and understanding of the processes, equipment and environment of production systems. Based on this knowledge, we have developed solutions to identify and minimize contamination and increase the yield at each step of the process.

SOLUTIONS for contamination management from Pfeiffer Vacuum improve the yield in the individual process steps of sensitive devices production. Innovative solutions from Pfeiffer Vacuum In-order-to-ensure the quality and a high yield in production, knowledge about the contaminants in the packaging of devices and their direct environment is important.

In the semiconductor industry, continuous analysis within the process cycle is possible with the APA 302. The fully automated process of the ADPC 302 localizes and counts particles on the inner surfaces of transportation carriers. The APR 4300 even goes a step further. The AMPC is the ideal solution for clean room and equipment front end modules monitoring (EFEM).

APA 302 - Pod Analyzer

The APA 302 is a unique in-line monitoring tool for advanced chip manufacturing in a clean room environment. This innovative equipment measures the airborne molecular contamination (AMC) in a FOUP in the sub ppbv- range. The measurement occurs in real-time with a high sensitivity in the ppbv-range.

ADPC 302 - Dry Particle Counter

The ADPC 302 is a unique in-process contamination management system for particle contamination monitoring in the semiconductor industry.

Efficient particle monitoring

The ADPC 302 measures the number of particles in wafer transport carriers (Front Opening Unified Pod, FOUP, and Front Opening Shipping Box, FOSB).

The fully automated patented process localizes and counts particles down to 10 nanometers size from the carrier surfaces, including the door. Qualified by leading fabs, this system can be used for both the serial production as well as R&D analysis. The main applications are the carrier characterization, cleaning strategy optimization and cleaning quality check.

Advantages

The dry process (Dry Particle Counter) of the ADPC shows clear benefits compared to the traditional wet method (Liquid Particle Counter). The main advantage of the dry process is that the particle measurement is completely automated. It is integrated in the production process and therefore does not require time outside the production period. The fully automated measurement process does not require an additional operator. The test time is only

➤ The Pod Analyzer APA 302 is a unique in-line monitoring tool for advanced chip manufacturing in a clean room environment.

six minutes. Traditional systems usually take about one hour for one FOUP and are not an automated process. It is possible to test 10 transport boxes in one hour.

APR 4300 - Pod Regenerator

The APR is a system for the decontamination of wafers and the protection during queue time. Airborne Molecular Contamination (AMC) lowers the yield and quality in the semiconductor production. The APR effectively prevents the adsorption of contaminated organic or organic, inorganic and humidity molecules on the surface of a wafer and the transport box. Through the evacuation of chambers in the APR, the adsorption probability is reduced dramatically. The yield of a fab can be increased significantly in this way and the queue times between the individual process steps can be optimized.

AMPC - Ambient Multi Port Controlling

Airborne molecular contamination (AMC) in IC fabs is known as the major factor of yield loss. To control and understand where contamination comes from, Pfeiffer Vacuum offers a unique solution to the semiconductor market to monitor clean rooms as well as EFEM (Equipment Front End Module).

Customer benefits

- Real-time compound measurement (acids, bases, organic compounds)
- Innovative software to manage sampling lines priority, quality check (QC) and alarms
- 96 samplings lines gathered onto one tool (up to eight analyzers)
- High throughput (analyzing and cleaning within three minutes)
- No cross-contamination from one sampling line to another

Systems for contamination management are our newest developments, specifically for the semiconductor and pharmaceutical industry.

How does contamination occur?

In the semiconductor industry, wafers emit reaction by-products during transport and waiting times. Moisture and molecular contaminants borne by air currents (Airborne Molecular Contamination, in short AMC), such as hydrogen fluoride (HF) react in the tight interstices of the transport boxes (pod systems) with oxidants from the ambient air (H_2O and O_2). During these reactions, undesired crystal growth on structured wafers is triggered which leads to a decline in quality and a decreased production yield.

Sub-micrometer particles can cause defects that may lead to considerable yield loss. Even the smallest particles measuring 0.1 µm may damage the structure of semiconductor chips.

The APR 4300 decontaminates 300 mm wafers and their transport boxes (FOUPs) on a molecular level and protects them during queue time. Reliable decontamination and protection from contamination

How does APR work?

The FOUP can be delivered either manually or through overhead hoist transportation (OHT) on the two load ports. The APR is a system with four stacked vacuum chambers for the decontamination of wafers and FOUPs, which is served from a reliable robot. All chambers are equipped with a vacuum pumping station, a gas box, an operating panel and a control with power supply. The chambers can be operated individually. After loading the chamber with a FOUP containing wafers, the pressure in the chamber is reduced to 0,05 mbar. Then the decontamination process is applied. After this, the chamber is purged with clean nitrogen and returned to atmospheric pressure. The wafers and the transport box are now protected from contamination for more than one day.

The AMPC is the ideal solution for clean room and equipment front end modules monitoring (EFEM).

The AMPC gathers the most advanced analyzers to detect and quantify acids, bases and organic compounds in up to 96 locations in a fab due to an innovative and integrated valves design. AMPC range includes two tools: AMPC S and AMPC L where external dimensions, number of lines and options are different. Additionally, the AMPC Extension Frame provides 39 U of space for extra analyzers. It can be used for upgrades of existing AMPC units or added to new AMPC S and AMPC L units.

Data management and fab communication

The tool software allows the end users to set various alarms when the levels of contamination exceed defined thresholds. All measurement results and tool parameters are stored in a database that can be transmitted to fabs' communication protocols to provide customers with a real-time picture of the fab's contamination levels. The customer is also able to remotely access the tool to modify tool parameters if necessary.

The Dry Particle Counter ADPC 302 is a unique in-process contamination management system for particle contamination monitoring in the semiconductor industry.

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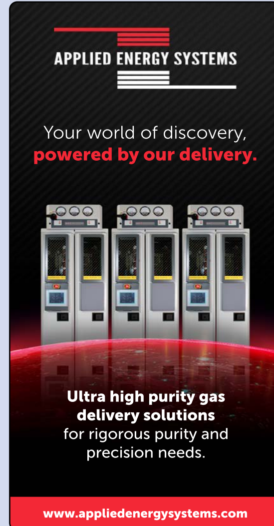
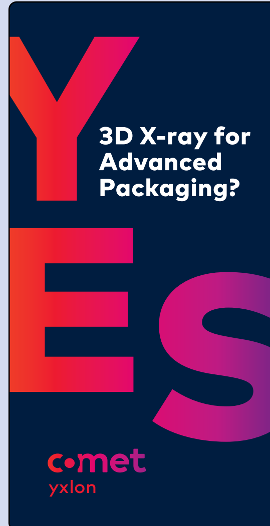
CLEAN ROOMS

GAS DELIVERY SYSTEMS



INSPECTION SYSTEMS



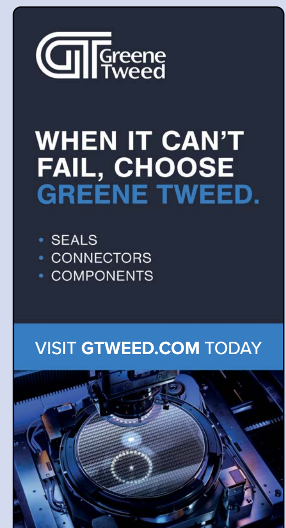
VACUUM EQUIPMENT

ETCH

GAS PURIFIERS

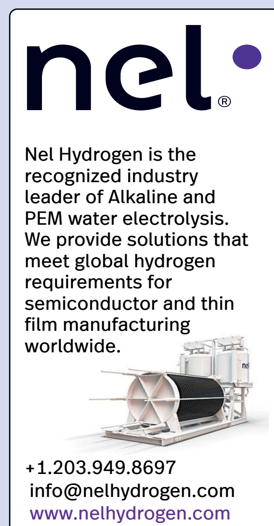
PLASMA TECHNOLOGY

COMPONENTS



FLOW MEASUREMENT

HYDROGEN GENERATORS



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