SILICON SEMICONDUCTOR
CONNECTING THE SILICON SEMICONDUCTOR COMMUNITY

ADDRESSING THE CHALLENGES OF ADVANCED ALD PROCESSES

VOLUME 45 ISSUE V 2024
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INSIDE

Silicon-based quantum computing processors

Contrary to popular belief, simply demonstrating quantum advantage is not the ultimate goal of quantum computing

Exploiting the new wave of semiconductors

Navigating the semiconductor revolution and identifies opportunities for growth

The challenges of advanced ALD processes

Addressing the potential problems of pump failure, process downtime and slow processing speeds

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VIEWPOINT

By Phil Alsop, Editor

When does a shortage become a crisis?

A COMMON THEME running across the three industry sectors in which I work – data centres, semiconductors and water – is the very real concern that there is a shortage of skilled individuals joining these industry sectors, as a significant quantity of the incumbent workforce are nearing retirement. A great deal of experience is leaving these important industries and it is not being replaced at anything near the required rate – especially when one considers the time it will take new recruits to themselves become 'experienced professionals'.

So far, the talk around this impending...well, what seems to be a crisis, but almost everyone I speak to across these three sectors goes out of their way not to use such a word, is very measured and calm. The talk is about all of the initiatives being introduced by individual organisations and the collective industries to develop tomorrow's workforce in the right numbers and with the right skills. Mention of the projects that have been delayed because there are not enough suitably qualified people to build a data centre, or to operate a semiconductor fab, is kept to a minimum.

Now, I am sure we can all sign up to the power of positive thinking, but, at some stage, such positivity does also have to take on board a healthy dose of realism. A workforce that is neither large enough nor skilled enough to help sustain the digital expansion predicted over the next few years is a serious problem.
And, more to the point, something of a self-inflicted one. Historians might argue that we were due a major global health disaster, and point out that global peace and stability is noted more by its absence than its observance, but few could have predicted the problems brought about by the pandemic or the war in Ukraine. However, the skills shortage has bee obvious for quite some time.

While AI sceptics might not lament the predicted shortage of AI chips in the near future at least, this potential bottleneck, with the guarantee of price volatility and some major winners and losers long the way, is not especially healthy. And there could be a knock on effect as all of the attention goes to expanding AI chip capacity, to the detriment of other chip types.

All of which leads me to the conclusion that, as far as is possible, the industry needs to go further and faster in terms of addressing the supply chain issues which it can control. The various Chips acts, and the expansion of national and regional semiconductor industries across many parts of the world, is an exciting development. Let's hope that industry is not putting all of its trust in a 'build it and they will come' belief.

Rather, we should hope to see the industry pushing at what is largely an open door. The financial incentives being offered by so many governments to the semiconductor industry demonstrates that the people in charge understand the importance of the sector. Not too difficult then to persuade them that an accompanying re-focusing of the education system is as equally important as the money?

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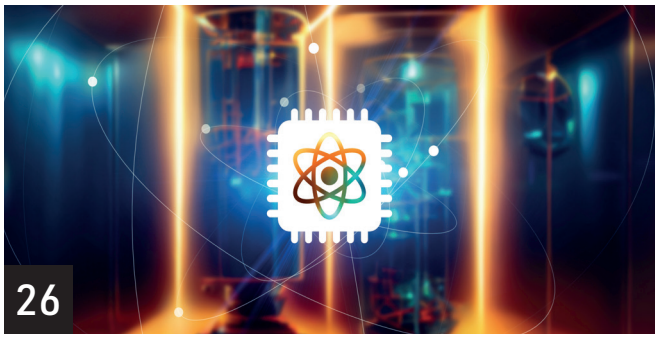
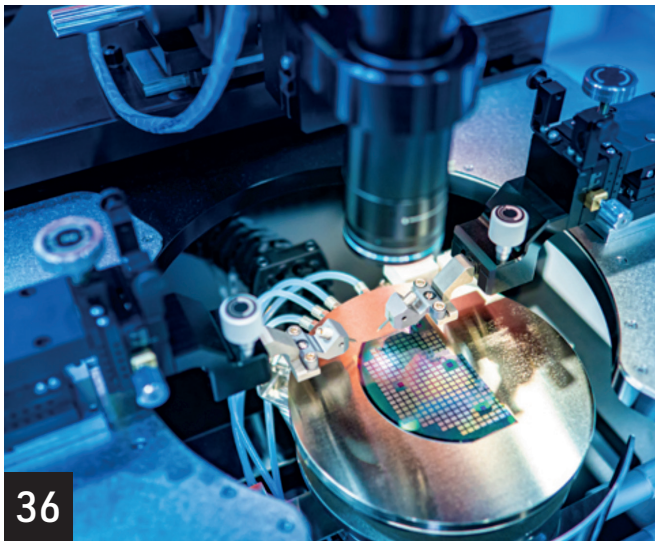
CONTENTS

VOL 45ISSUE V 2024

SILICON SEMICONDUCTOR





NEWS

Publisher Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Editor Phil Alsop phil.alsop@angelbc.com
Sales & Marketing Manager Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215
Marketing & Logistics Executive Eve O'Sullivan eve.osullivan@angelbc.com +44 (0)2476 823123
USA Representatives Tom Brun Brun Media tbrun@brunmedia.com +001 724 539-2404
Janice Jenkins jjenkins@brunmedia.com +001 724-929-3550
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214

Chief Executive Officer Sukhi Bhadal sukhi.bhadal@angelbc.com +44 (0)2476 718970
Chief Technical Officer Scott Adams scott.adams@angelbc.com +44 (0)2476 718970
Directors Jackie Cannon, Sharon Cowley

Published by Angel Business Communications Ltd,
6 Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970 E: info@angelbc.com

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Hyperscalers forge ahead with in-house semiconductor solutions

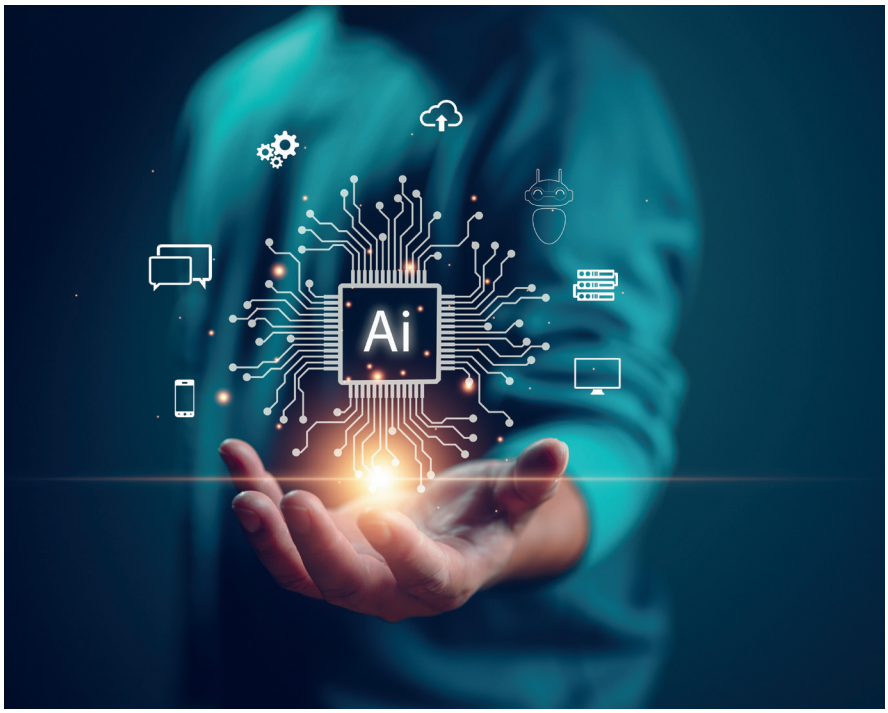
Hyperscalers such as Meta, Microsoft, Google, and Amazon are strategically shifting towards developing proprietary semiconductor technologies in response to the soaring demand for Nvidia's GPUs in the burgeoning generative AI (GenAI) market

THIS STRATEGIC MOVE is aimed at reducing dependency on Nvidia while fostering innovation and facilitating global expansion. Within this dynamic landscape, significant investments in AI technologies and strategic partnerships underscore the intense competition within the GenAI space, says GlobalData, a leading data and analysis company.

Nvidia, which sells graphic processing unit (GPU) semiconductors particularly suited to AI-specific workloads, has emerged as one of the clear winners in the nascent GenAI market as demand for its GPUs explodes. However, providers of GenAI services such as big cloud computing companies have been impacted by the massive financial burden of acquiring the expensive chips.

Beatriz Valle, Senior Enterprise Technology and Services Analyst at GlobalData, comments: "There is a significant imbalance between supply and demand when it comes to GPU processors, because GenAI models in general, and especially multimodal systems that produce images and videos, greatly benefit from the parallel processing capabilities of GPUs. As a result, the chips are expensive and in short supply.

"To counteract this trend, GenAI companies are coming to market with their own proprietary technologies to run these workloads. Google has its tensor processing unit (TPU) semiconductors and Amazon has its Inferentia and Trainium architectures.



Meta, the social media company behind Facebook and Instagram, recently announced the next generation of custom-made chips to help power AI-driven rankings and recommendation ads on social media platforms."

GlobalData analysis notes that money continues to flow in the lucrative GenAI space as hyperscalers jockey for position. Leading GenAI companies are ramping up investment in strategic partnerships across the world to remain competitive. Microsoft, now vying for a global presence to offer AI services across Microsoft Azure's infrastructure, has recently invested $1.5 billion in new technology group G24, an Abu Dhabi (UAE) AI consortium. AWS is completing its final round of $4 billion in funding to partner Anthropic, striving to gain a foothold following Microsoft's mega OpenAI investment.

Charlotte Dunlap, Research Director of Enterprise Technology and Services at GlobalData, comments: "Microsoft's investment signals the start of a much larger AI technology role for the UAE. G24 is targeting various sectors for its AI solutions, including healthcare and energy. The deal is not without its complications. In return for the mega investment by Microsoft, G42 severed ties to China by eliminating hardware provisioning by Huawei systems, among other efforts in recent months to appease US concerns."

To counteract this trend, GenAI companies are coming to market with their own proprietary technologies to run these workloads. Google has its tensor processing unit (TPU) semiconductors and Amazon has its Inferentia and Trainium architectures

CHIPS for America announces $285 million funding opportunity

The Biden-Harris Administration has issued a Notice of Funding Opportunity (NOFO) seeking proposals from eligible applicants for activities to establish and operate a CHIPS Manufacturing USA institute focused on digital twins for the semiconductor industry

DIGITAL TWINS are virtual models that mimic the structure, context, and behavior of a physical counterpart. The CHIPS for America Program anticipates up to approximately $285 million for a first-of-its-kind institute focused on the development, validation, and use of digital twins for semiconductor manufacturing, advanced packaging, assembly, and test processes. The CHIPS Manufacturing USA institute is the first Manufacturing USA institute launched by the Department of Commerce under the Biden Administration.

Unlike traditional, physical research models, digital twins can exist in the cloud, which enables collaborative design and process development by engineers and researchers across the country, creating new opportunities for participation, speeding innovation, and reducing costs of research and development.

Digital twin-based research can also leverage emerging technology like artificial intelligence to help accelerate the design of new U.S. chip development and manufacturing concepts and significantly reduce costs by improving capacity planning, production optimization, facility upgrades, and real-time process adjustments.

“Digital twin technology can help to spark innovation in research, development, and manufacturing of semiconductors across the country – but only if we invest in America’s understanding and ability of this new technology,” said Secretary of Commerce Gina Raimondo. “This new Manufacturing USA institute will not only help to make America a leader in developing this new technology for the semiconductor industry, it will also help train the next generation of American workers and researchers to use digital twins for future advances in R&D and production of chips.”

“Under President Biden’s leadership, we’re writing a new chapter in semiconductor manufacturing in America,” said Arati Prabhakar, Assistant to the President for Science and Technology and Director of the White House Office of Science and Technology Policy. “CHIPS R&D is about making sure American manufacturers can continue to succeed and thrive. Digital twin technology can accelerate the costly and time-consuming work to develop the next generation of robust manufacturing for this extraordinarily complicated product.”

Funded activities are expected to include, but not necessarily be limited to operational activities to run the Institute; basic and applied research related to semiconductor digital twin development; establishing and supporting shared physical and digital facilities; industry-relevant demonstration projects; and digital twin-related workforce training.

“Digital twin technology will help transform the semiconductor industry,” said Under Secretary of Commerce for Standards and Technology and National Institute of Standards and Technology (NIST) Director Laurie E. Locascio. “This historic investment in the CHIPS Manufacturing USA institute will help unite the semiconductor industry to unlock the enormous potential of digital twin technology for breakthrough discoveries. This is a prime example of how CHIPS for America is bringing research institutions and industry partners together in public private partnership to enable rapid adoption of innovations that will enhance domestic competitiveness for decades to come.”

Imec.xpand launches EUR 300m fund

Imec.xpand, an independent global venture capital fund, has launched a new EUR 300 million fund aimed at accelerating the growth of transformative semiconductor and nanotechnology innovations

ESTABLISHED as a collaborative effort with imec, the world-leading R&D and innovation hub in nanoelectronics, the fund will invest in startups that have the potential to be globally disruptive within their target domains. The fund is designed to fuel semiconductor innovation beyond traditional applications and drive the next-generation technologies that are 10 years ahead of their time.

Imec.xpand invests globally across all stages, transforming semiconductor and nanotechnology innovations into market-ready solutions. Focused on leveraging imec's expertise, the fund targets breakthrough technologies including artificial intelligence (AI), machine learning (ML), augmented reality/virtual reality (AR/VR) and photonics. In life sciences, imec.xpand is looking for opportunities to advance cell therapy, sequencing, neuromodulation and other applications that will revolutionize medical diagnostics and treatments.

"Imec.xpand is not just about funding startups, it's about building companies that can lead the next wave of technological transformation," said Tom Vanhoutte, partner at imec.xpand. "With this fund, we are dedicated to advancing the semiconductor industry by empowering startups to bring innovative technologies to market faster. The combination of our venture capital and international network helps unicorns grow amid the global race for semiconductor supremacy."

The first imec.xpand fund was launched in 2017 with the strong support of imec. Since then, imec.xpand has attracted a loyal base of international financial and strategic investors. Over the years, imec.xpand has built a strong track record of investing in game-changing companies.

The fund's unique positioning among the global venture capital community, and also in the U.S., is instrumental in attracting potential co-investors for its portfolio companies. Imec.xpand's stamp of approval often acts as a financial catalyst that enables startups to raise additional funding from other investors. To date, imec.xpand has invested in 23 companies that, so far, have raised nearly EUR 1.5 billion in financing and includes two unicorns.

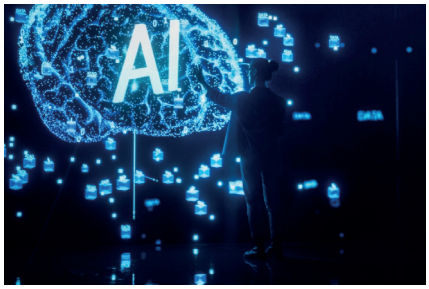
Imec.xpand portfolio companies are developing cutting-edge, differentiated technologies that give them a global competitive advantage in their respective markets. Noteworthy imec.xpand portfolio companies include Celestial AI, a Palo Alto-based company that recently raised $175 million USD to advance its optical compute and memory fabric solution for AI infrastructure; PsiQuantum, a frontrunner in the race to develop the first practical quantum computer; and Swave Photonics, developing a unique holographic extended reality chip technology designed to disrupt 3D holographic imaging and spatial computing.

AI chip market to become a $300 billion industry

THE GLOBAL AI renaissance, which started last year, only fuelled the market growth, helping it to reach a staggering value in the following years. According to data presented by AltIndex.com, the global AI chip market is expected to grow 10 times in the next ten years and become a $300 billion industry.

AI chips are specialized semiconductor devices that perform complex calculations and tasks required for artificial intelligence applications. They are designed to accelerate AI algorithms and processes, enabling higher performance, lower power consumption, and improved cost-effectiveness. Today, AI chips are used across industries, from healthcare and finance to automotive and manufacturing, and the global demand for these devices is expected to skyrocket in the following years. According to Statista and Market.us data, the global AI chip market will gross $30 billion in 2024, or $7 billion more than last year. Over the next three years, the market revenue will more than double and hit $67 billion by 2027. Still, that is nothing compared to growth projections in the years after that. By 2029, the entire market is expected to hit a massive milestone and become a $100 billion industry. Three years later, that $100 billion will grow into $260 billion, or eight times the expected revenue in 2024. Statistics show the global AI chip market will continue surging in 2033, with revenues rising to a whopping $341 billion, or 1,000% more than this year.

Although Nvidia is the absolute king in the AI chip industry with a massive



80% market share, both large and small businesses are searching for alternatives to diversify their AI chip options. That caused intense competition in the market, with both semiconductor giants and emerging startups heavily investing in AI chip research and development to gain a competitive edge. The surging need for AI chips has also created a huge space for VC investors, who have poured tens of billions of dollars into these startups.

Semiconductor giants add $1.1 trillion to stock values

After a challenging year in 2023, the global semiconductor industry is back on track for recovery, fuelled by a surging AI chip sale, especially in the generative AI field

GLOBAL SEMICONDUCTOR sales are expected to hit $588 billion in 2024, 13% more than last year and 2.5% higher than 2022's record industry revenues of $574 billion. This positive trend has also helped the largest players in the market add hundreds of billions of dollars to their stock values.

According to data presented by AltIndex.com, the five largest semiconductor companies have collectively increased their stock values by over $1.1 trillion year-to-date.

The surge in generative AI use continues fuelling global AI chip sales and rising stock prices of the biggest semiconductor companies. In January, the combined market cap of Nvidia, Taiwan Semiconductor Manufacturing, Broadcom, Samsung, and ASML Holding, the five largest semiconductor manufacturers globally, amounted to $2.99 trillion. Since then, this figure has jumped by an impressive $1.1 trillion and hit $4.1 trillion last week. And while most of these tech giants added tens and even hundreds of billions of dollars to their market cap over the past four months, none is even close to Nvidia (NVDA).

The world's third-largest tech company and the biggest semiconductor company by market cap is having another fantastic year. After ending 2023 as the best S&P 500 performer with a 236% gain, the Nvidia added more than one trillion dollars to its stock value in the first three months of the year, or 15% more than in the entire 2023.

In January, Nvidia's market cap amounted to $1.2 trillion. By the end of March, this figure soared to $2.3 trillion, showing an impressive 90% growth in just three months. Although the company`s market cap dropped by 10% since then and hit $2.06 trillion last week, Nvidia still added a whopping $833 billion to its stock value year-to-date, the biggest increase among the semiconductor giants.

Semiconductor Manufacturing (TSM) jumped by almost $170 billion, or 31%, in this period, the second-highest increase in this group. In January, the market cap of the Taiwanese tech giant stood at $539 billion; now, it's over $708 billion. Statistics show the US semiconductor manufacturer, Broadcom, added $77 billion to its market cap year-to-date and hit a market cap of almost 600 billion last week. The Duch-based ASML Holding follows with a $58 billion increase and $356 billion in stock value as of last week.

Rapidus and Esperanto Technologies sign memorandum of cooperation

Promote development and manufacture of more energy-efficient semiconductors for artificial intelligence and other high-performance datacenter applications

RAPIDUS has signed a Memorandum of Cooperation with Esperanto Technologies Inc, a leader in energy-efficient RISC-V based computing solutions. With the conclusion of the MOC, the two companies intend to promote the development and manufacture of low-power consumption AI semiconductors for datacenters, which will be indispensable in the coming full-fledged AI era.

Esperanto develops high-performance, energy-efficient computing solutions for artificial intelligence/machine learning based on the open standard RISC-V instruction set architecture. The company has semiconductor design technology that achieves high energy efficiency in the fields of generative AI and high-performance computing (HPC).

Last September, Rapidus began construction of IIM (Innovative Integration for Manufacturing) in Chitose City, Hokkaido. This will be Japan's first facility for the production of state-of-the-art logic semiconductors at 2-nanometers (nm) and beyond. At the same time, Rapidus has been dispatching researchers to the Albany Nanotech Complex in New York, USA, one of the world's most advanced semiconductor research centers, to work with IBM to develop technologies for the production of 2nm logic semiconductors. The company is also planning to acquire EUV lithography technology, which is essential for the production of cutting-edge semiconductors, from imec. Utilizing these technologies, the company plans to start operation of a pilot production line at IIM-1 in April 2025, and begin mass production in 2027.

As society enters the full-fledged AI era represented by generative AI, power consumption in data centers is

increasing. According to International Energy Agency, data centers are significant drivers of growth in electricity demand in many regions. After globally consuming an estimated 460 terawatt-hours (TWh) in 2022, data centers' total electricity consumption could reach more than 1,000 TWh in 2026. This demand is roughly equivalent to the entire electricity consumption of Japan. Updated regulations and technological improvements, including on energy efficiency, will be crucial to moderate the surge in energy consumption from data centers. (Source: "Electricity 2024" ©International Energy Agency)

The 2nm node semiconductors that Rapidus aims to manufacture will be more advanced than conventional semiconductors, enabling not only improved processing performance but also dramatically reduced power consumption. Esperanto, meanwhile, has been developing products with superior energy efficiency for generative AI, HPC and edge devices.

By collaborating early on the co-optimization between design and manufacturing of next-generation semiconductors, the two companies aim to better enable the development of energy-efficient products for the AI era.

"The strategic partnership with Rapidus plays a key role in our expansion plans for Japan," said Art Swift, CEO of Esperanto Technologies Inc. "Rapidus represents a new approach to leading-edge semiconductor manufacturing, and we are very impressed with the direction and speed at which they are operating. Along with our other partners in Japan, we hope our new relationship with Rapidus will extend the benefits of our energy efficient technology to a broader set of SoC designers."

"As part of our corporate philosophy, we will commit ourselves to further innovating toward a truly green society," said Dr. Atsuyoshi Koike, president and CEO of Rapidus Corporation. "As we enter the age of full-fledged AI, it is imperative to design and manufacture semiconductors with superior energy-saving performance, and we believe that this collaboration with Esperanto is a major step toward solving this issue."

Infineon reveals roadmap for energy-efficient power supply units in AI data centres

Artificial intelligence leads to increasing energy demand of data centres worldwide

THE INFLUENCE of artificial intelligence (AI) is driving up the energy demand of data centers across the globe. This growing demand underscores the need for efficient and reliable energy supply for servers. Infineon Technologies opens a new chapter in the energy supply domain for AI systems and unveils a roadmap of energy efficient power supply units (PSU) specifically designed to address the current and future energy need of AI data centers.

By introducing unprecedented PSU performance classes, Infineon enables cloud data center and AI server operators to reduce their energy consumption for system cooling. The innovative PSUs reduce power consumption and CO 2 emissions, resulting in lower lifetime operating costs. The powerful PSUs are not only used in future data centers but can also replace existing power supply units in servers and increase efficiency. In addition to the current PSUs with an output of 3 kW and 3.3 kW available today, the new 8 kW and 12 kW PSUs will contribute to further increasing energy efficiency in future AI data centers. With the 12 kW reference board, Infineon will offer the world's first power supply unit that achieves this level of performance and supplies future data centers with power.

"At Infineon, we power AI. We are addressing a critical question of our era – how to efficiently meet the escalating energy demands of data centers," says Adam White, Division President Power & Sensor Systems at Infineon. "It's a development that was only possible by Infineon's expertise in integrating the three semiconductor materials silicon (Si), silicon carbide (SiC), and gallium nitride (GaN) into a single module. Our PSU portfolio is therefore not only an example of Infineon's innovative strength, which leads to first-class results in terms of performance, efficiency and reliability for data centers and the AI ecosystem. It also reinforces Infineon's market leadership in power semiconductors."

Infineon is responding to the requirements of data center operators for higher system efficiency and lower downtimes. The growth of server and data center applications has led to an increase in power requirements, necessitating the development of power supplies with higher power ratings from 800 W up to 5.5 kW and beyond. This increase is driven by the growing power requirements of Graphic Process Units (GPU) on which AI applications are computed.

£3m grant for Glasgow chip research

A major new grant will allow the University of Glasgow to build one of the UK's most advanced research facilities for silicon chip integration and packaging

A MAJOR new grant will allow the University of Glasgow to build one of the UK's most advanced research facilities for silicon chip integration and packaging.

The Engineering and Physical Sciences Research Council's Strategic Equipment Grant scheme will provide £3m to help the University establish ANALOGUE – the Automated Nano AnaLysing, characterisatiOn and additive packaGing sUitE.

Clockwise from top left: Prof David Flynn, Prof Hadi Heidari, Dr Mahmoud Wagih and Prof Jeff Kettle of the James Watt School of Engineering

ANALOGUE will enable the rapid prototyping and characterisation of a wide range of semiconductor devices. New developments prototyped at ANALOGUE could find applications in biomedical implants, sustainable and biodegradable sensors, and quantum computing interfaces.

The facility, which will be based at the University's Mazumdar-Shaw Advanced Research Centre (ARC), brings together researchers from the University's James Watt School of Engineering with a strategic network of partners from industry, national semiconductor facilities, and academia, aligned with fast tracking disruptive new technologies into applications.

It aims to support the UK government's semiconductor strategy by providing access to new technologies to boost cutting-edge research and development. It will also play a role in expanding the country's semiconductor skills base through industry-led events and partnerships with Centres for Doctoral Training across the UK.

The suite will house chip probing equipment, advanced packaging capabilities, and additive electronics

manufacturing using state-of-the-art tools. The equipment will be automated as a single suite, making it the UK's first machine-driven integrated assembly and characterisation line for semiconductor devices. ANALOGUE's advanced automation will allow users to use the suite remotely, with support from on-site experts, helping to streamline the research process.

ANALOGUE will also provide support for ongoing efforts to decarbonise the electronics supply chain by helping researchers gather data on their product's environmental impact.

ANALOGUE will be open to academia and industry working on low-volume and high-value research and development projects, helping them to rapidly prototype advanced nanoelectronic devices.

Professor Hadi Heidari, Head of the University of Glasgow's Electronics and Nanoscale Engineering Research Division, is the project's principal investigator.

He said: "This grant is a significant milestone for semiconductor research in the UK, which is a key part of the country's economy. The electronics sector as a whole supports more than a million jobs in the country, and the UK government has ambitious plans to grow the sector in the years to come.

"The establishment of ANALOGUE represents a substantial advance in the UK's semiconductor research infrastructure for heterogeneous integration and advanced packaging.

"This initiative will help spark new innovations across the tech sector and cultivate valuable partnerships between academia and industry, helping to support breakthrough research which can drive economic expansion."

The suite is supported by 27 external project partners including national facilities such as the Manufacturing Technology Centre (MTC) and the National Physical Laboratory (NPL), academic networks (EPSRC eFutures and E-Textiles), and top research universities.

A team of 23 academics and more than 100 researchers and students will make regular use of the facility. ANALOGUE's industrial partners include Arm, PragmatIC, Inseto, Nano-Dimension, Vector Photonics, Touchlab, Printed Electronics, Kelvin Nanotechnology, Denchi Power, SeeQC, Quantum Science, Labman, Scotland 5G Centre, and CENSIS.

This multidisciplinary project is strongly supported by other colleagues at the James Watt School of Engineering from different areas of Quantum Technologies, Medical Implantables, Wearables and Diagnostics, Ultrasound Systems, and Sustainable Electronics including Prof Jeff Kettle, Prof David Flynn, Dr Mahmoud Wagih, Prof Martin Weides, Prof Muhammad Imran, Prof Edward Wasige, Prof Marc Sorel, Dr Chong li, Dr Kaveh Delfanazari, Dr Andrew Feeney, Prof Sandy Cochran, Dr John Mercer, Dr Daniel Mulvihill, Prof Margaret Lucas, Prof S Kumar, Prof David Cumming, Prof Manuel Salmeron-Sanchez, Prof Qammer Abbasi, Dr Morteza Amjadi, Prof Julien Reboud, Prof Jonathan Cooper, Dr Qingshen Jing, Dr Kwok Ho Lam and Dr Rair Macedo.

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High-speed, high-temperature pumps address the challenges of advanced ALD processes

Addressing the potential problems of pump failure, process downtime and slow processing speeds when it comes to atomic layer deposition.

BY ALLISTER WATSON AND YOUNG CHUNG, EDWARDS VACUUM

SEMICONDUCTOR DEVICE designs are going vertical. Some of the most exciting new devices use many-layered film stacks and incorporate high aspect-ratio (HAR) features that are themselves complex multilayered structures deposited with atomic layer deposition (ALD) processes. Some ALD processes generate condensable by-products that can accumulate in vacuum pumps.

If not addressed, the deposits can lead to pump failure and process downtime. Even when managed appropriately, these accumulations require periodic maintenance that increases cost-of-ownership and reduces productivity. While ALD is exquisitely precise, it is also inherently slow, limited to a large extent by the vacuum system's ability to cycle between precursor and reactant gases in the process chamber. Together, these considerations are driving the development of higher temperature, higher speed pumps to extend maintenance intervals and shorten ALD process cycles.

HAR structures

HAR features are becoming more common, and their aspect-ratios continue to increase. In some cases, such as the capacitors in DRAM, the increasing ratio results from pressure to pack more capacitors within a given footprint. In other cases, the pressure is in the vertical direction, as in 3D NAND, where increasing memory capacity means

more layers and longer channels. In both cases, tall, narrow, cylindrical cavities etched in the substrate are filled by concentric layers of various materials to create the functioning device.

ALD processes

Most conventional deposition processes were developed to deposit uniform films over shallow features. The processes are relatively fast, and the deposition continues as long as the surface is exposed to the process.

The thickness of the film is thus a function of the time the deposition time. These processes are not good at maintaining uniformly thick films in the presence of significant topography, especially the extreme topography of HAR features where the deposition process has restricted access to the internal vertical walls and deeply recessed bottoms of the features.

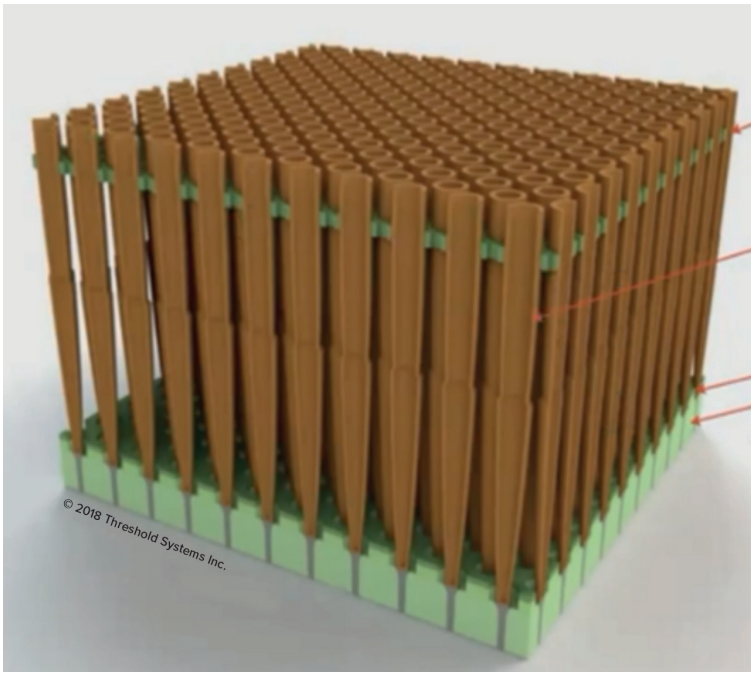
ALD offers an elegant solution for depositing highly conformal, precisely controlled thin films on complex, deeply recessed surfaces. The deposits accumulate one atomic layer at a time as the surface is exposed to a repeating cycle of precursor and reactant gases. In the first phase, the precursor reacts with specific sites on the surface.

The reaction is self-limiting – once all sites have been occupied by a precursor molecule, the reaction stops. Next, the precursor gas is removed, and a reactant gas is introduced. The reactant interacts with the previously deposited precursor, again in a self-limited way, to complete the deposition and recreate the original surface chemistry. The newly deposited monolayer is ready for another ALD cycle.

Because both reactions are self-limiting, film thickness is a function of the number of cycles, not exposure time. This gives process engineers the luxury of allowing each cycle of the process to continue as long as needed to be sure all surfaces are completely and uniformly covered.

The biggest drawback of ALD is its slow speed. It is best suited to the deposition of very thin films that require fewer deposition cycles. Wafer throughput is determined primarily by the time it takes to remove one gas from the process chamber and replace it with the other, which puts a premium on high pumping speed in the vacuum system.

Condensable Process Gases and By-Products



➤ Figure 1: The tube-shaped capacitors comprise concentric cylindrical TiN plates separated by dielectric materials. ALD of TiN from TiCl4 creates NH4Cl, a condensable by-product. $TiCl_4$ flows will increase as the capacitors grow taller and narrower. Reference: Threshold.

Some process gases and by-products condense on cooler surfaces. In extreme cases, accumulations can completely block vacuum lines and cause pumps to seize. Avoiding unwanted deposition is most critical in the pump itself where rapidly rotating parts must maintain very tight mechanical tolerances. Condensation can be reduced or prevented by maintaining sufficiently high temperatures within the vacuum system. The challenge is best addressed by specially designed high-temperature pumps and by heating the foreline and exhaust line.

DRAM capacitors (Fig 1) are getting taller and thinner to increase their aerial density. The half-pitch of the capacitor array is projected to decrease by half over the next decade. Inside each capacitor, concentric tubular plates are separated by a complex structure of layered dielectric materials. ALD is essential for depositing the TiN electrodes of the capacitors. It is produced by the reaction of TiCl4 and NH3. The reaction deposits TiN but generates NH4Cl, a condensable by-product. A carefully controlled, high-temperature profile throughout the vacuum

DRAM	2022	2025	2028	2031	2034
Min Half Pitch (nm)	15.5	13	14	11.5	10
Cell Size (µm²)	0.00165	0.00118	0.00085	0.00062	0.00044

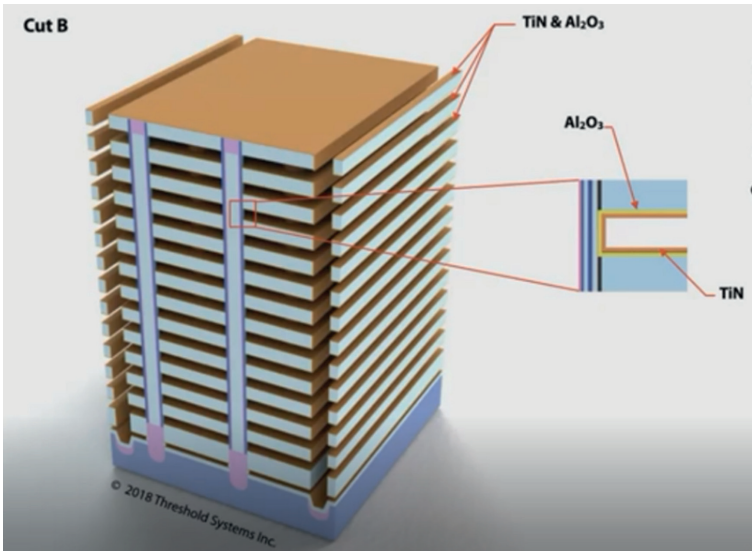
➤ Table 1. The cell size and half pitch of DRAM capacitor arrays are expected to shrink substantially in the next 10 years. (source: IRDS 2022)

Edwards' latest generation of high-speed, high-temperature pump (iXH6520HTXS+) was developed in collaboration with major semiconductor equipment suppliers to address the challenges presented by advanced ALD process

system, but especially in the pump, reduces unwanted deposition and the risk of pump seizure. As aspect ratios increase, so will TiCl4 flows.

Current generation 3D NAND devices have nearly 200 pairs of alternating oxide/nitride dielectric layers. Vertical memory strings are created along channels that penetrate these layers. The number of layers determines the number of memory cells along each channel and thus the memory density and capacity of the device.

The number of layers for multi-tiered devices will likely increase to 500 or more this decade. To create the memory cells, the channels are lined with an oxide/nitride (ONON) sandwich. The nitride layers become the charge traps that store information. The outermost oxide layer is needed to block a subsequent nitride etch that removes nitride from between the oxide layers of the original ONON stack.



➤ Figure 2. The number of layers in 3D NAND memory is predicted to double or more by 2031, requiring longer, higher aspect ratio channels. The ONON sandwich that lines each channel is deposited with ALD from HCDS. The nitride phase of the deposition creates condensable NH4Cl. The HCDS can also condense to a polymeric gel. (Source: Threshold Systems 2021)

ALD processes are used to deposit the ONON sandwich within the channels. Both the oxide (SiO2) and the nitride (SiN) are generated from hexachlorodisilane (HCDS). For nitride layers, HCDS + NH3 deposits SiN but also generates condensable NH4Cl as a by-product, requiring a hot pump to prevent unwanted condensation within the pump.

For oxide layers, HCDS + oxidant deposits the oxide without creating the NH4Cl by-product. However, the HCDS molecule itself may polymerize to form a condensable gel. Thus, a hot pump is needed to prevent NH4Cl in the nitride case and HCDS gel condensation in both cases. As the number of layers increases, so will the flows of HCDS and the need for hotter pumps.

The pump

Edwards' latest generation of high-speed, high-temperature pump (iXH6520HTXS+) was developed in collaboration with major semiconductor equipment suppliers to address the challenges presented by advanced ALD process. It incorporates several new critical high-temperature technologies that allow it to operate at surface temperatures as high as 260°C. High-temperature operation reduces by-product condensation on critical pump surfaces, significantly extending recommended service intervals. Compared to its predecessor this new pump also benefits from a 30% increase in peak pumping speed, up to 96,000 l/min; a 34% lowering in power consumption; and better achievable ultimate vacuum pressure performance (important for high cleanliness between ALD steps).

For advanced ALD processes where condensable by-products are a concern then less frequent maintenance, faster process cycles, and lower power consumption can offer substantial bottom-line returns by lowering cost of ownership and increasing productivity.

3D NAND	2022	2025	2028	2031	2034
Number of Memory Layers	128-192	256-384	384-576	576-768	768-1024
Number of Tiers	2	2	3	3	4
Bits/mm^2	2T	5.2T	8T	12T	16T

➤ Table 2. 3D NAND Layers, tiers and storage density will all increase substantially over the next ten years. (Source: IRDS 2022)

Exploiting the new wave of Semiconductors:

AI, trust & information overload

ROBERT MCKENZIE, VP OF SILICON SECTOR AT GLOBAL SOFTWARE SERVICES COMPANY, MOBICA navigates the semiconductor revolution and identifies opportunities for growth.

THE GLOBAL SEMICONDUCTOR INDUSTRY is experiencing huge growth and predicted to become a trillion dollar industry by 2030. That growth is being accompanied by an ongoing rediscovery of application approaches and step changes in design and development. It is not an understatement to say that we are seeing momentous changes happening at an unprecedented pace.

In this article we take a look at what's driving those changes, their adoption and the technology underlying this momentous change.

The scale of change

A keynote at Embedded World conference, March 2023, provided the following eye popping statistics about the level of growth in Internet of Things (IoT) business and installations:

- By 2030, the IoT could enable $5.5 trillion to $12.6 trillion in value globally
- In 2023 11.5bn connected devices will ship, bringing the installed base to 40bn units - 1.5bn home automation, 0.75bn inventory and asset tracking, 600m for lighting, 300m health and fitness

Thanks to the rapid adoption of AI, embedded solutions and the IoT, there is a new wave of chips coming along that can serve a broader range of applications. They can do so because of the increased capability to support security, safety, identity and privacy, all areas where the new architecture and semiconductor chip features add value.

Originally computers were designed for a particular purpose, for example, breaking cryptographic ciphers. The arrival of the first commercially available general purpose computer, the Ferranti Mark 1, led to general purpose applications for government, business and scientific challenges. But there was still an opportunity for 'application specific integrated chips' (ASICS). Companies such as LSI Logic played a significant role in changing the semiconductor market during the 1980s and 90s, with their ASICS for calculators etc.

Building on the foundations laid over the past 50 years

Today's industry builds on previous inventions to deliver a wide range of architectures and technologies that deliver the new applications. As well as the general purpose 'central processing units' (CPUs), those technologies include:

- **ASICS** for handling, amongst other things, compression, encryption and with features

like VRAN boost in Intel XEON based SmartNICS accelerating networking needs.
- **FPGAs -** fully programmable gate arrays - enabling feature updates on the semiconductor itself, making them as upgradeable as a software package
- **GPUs -** graphics processing units - accelerating graphics processing by enabling single instructions to operate in parallel on multiple data
- **xPUs -** the processing unit designed for a particular application

The 'system on chip' (SOC) approach brings together semiconductor designs to deal with I/O, power management, telecoms, including the iterations of mobile protocols 3-5g, WAN and Bluetooth.

We should mention the concept of the xPU: this is a catch-all for the 'processing unit', designed for a particular application e.g. most SOCs now include an NPU, or neural processing unit, designed for efficiently calculating the mathematics of neural networks, which feature in new products from Intel, Apple and Qualcomm. A further example is the VPU, or 'visual process unit', used in cameras, and designed for image processing.

Scaling up: trends and new developments

As well as being able to design all the systems on one chip, standardisation around 'chiplets' will increase the possibility and market for new semiconductor development.

The UCIe specification for the 'Universal Chiplet Interconnect Express' is focussed on building an open ecosystem of chiplets for on-package innovations. This market will take a decade to develop, but is part of the new wave of semiconductor innovation.

Before moving onto AI, trust and information overload, it's worth providing two more examples of scale. At the data centre end, Nvidia's GPU Technology Conference in 2022, Stephen Jones ran through the phenomenal increase in performance that has occurred at the high-end of silicon technology.

The A100 GPU, or Ampere architecture, used in the data-centres, runs at 9.7 TFLOP/s double precision performance. To put this in perspective, the world's leading supercomputer in 2001 was the Lawrence Livermore National Laboratory in the USA's ASCI White, had 7.9 TFLOPS/s. So the A100 chip has more than the equivalent performance.

At the recent GTC, Jensen Huang - Nvidia's CEO - announced its new Blackwell architecture to be released in 2024. Whilst double precision (FP16) performance figures weren't presented, the new chip does deliver 20k TFLOPS at FP4, or 1000x increase over the past 8 years.

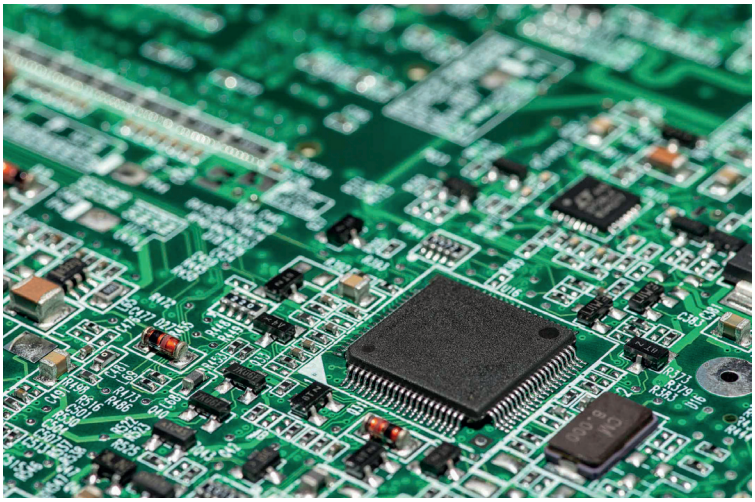
At the edge, the microcontroller (MCU) is becoming increasingly sophisticated and able to deliver more. Traditionally it has a few components such as RAM, ROM, and programmable I/O ports primarily designed to control and drive other electronic equipment. MCUs are designed to be embedded, often in a highly restrictive environment. They usually consume very little power, may run relatively slow, and typically execute individual task-specific programs. But now they are increasingly including features to ensure security and provide AI services.

TinyML is one movement that is enabling machine learning on these tiny devices. According to the TinyML foundation, it is broadly defined as a fast growing field of machine learning technologies and applications including hardware, algorithms and software capable of performing on-device sensor data analytics at extremely low power, typically in the mW range and below, which enables a variety of always-on uses for battery operated devices.

The NXP MCX N Advanced Series Microcontrollers, includes intelligent peripherals and on-chip accelerators. To balance performance and power efficiency, they incorporate NXP's eIQ Neutron neural processing unit (NPU) specifically for machine learning applications.

Similar devices are being produced by Infineon, STMicro, Sony, Espressif, often combining off the shelf IP CPU cores licensed from ARM and then adding these new features in order to support new applications. Whereas the latest data centre chips and boards cost tens of thousands of dollars, microcontrollers can be bought in quantity for under fifteen dollars - or less.

Further new innovations coming down the line will increase the performance and reduce the power consumption even further. A good example of this is being developed by EnchargeAI. They are designing a hybrid of analogue and digital chip technology due to ship at the end of 2024. Benchmarks demonstrate a 150 TOPS/W, which is 20x current market leader in power usage efficiency.



Inference: use cases and applications

Initial use cases for the EnchargeAI product will be in inference, not for training the Deep Neural Nets (DNN) and Large Language Models that Nvidia and newer entrants such as Tenstorrent and Cerebras are aiming at. The inference work will use these trained models for natural language processing and image recognition support. The product is likely to become integrated in SOCs for the phone, or battery powered devices. Currently, security systems are often wired in because the components won't operate for multi-year periods on batteries. These new technologies bring the promise that they will not only be able to operate for long periods of time, but that they will also be able to make decisions based on better training.

At the moment, standard commercial or domestic security systems will recognise intruders, capture the image and, if armed, inform the owner. With new features at an improved price point, it's a short step to having the system recognise that it's you, or someone else who lives or works at the premises, and disarm and open the door.

For the first time, the ability to get inferencing and then decision making right at the edge is becoming a reality. Perhaps more significantly, it is also becoming economically viable.

So much so that a number of companies such as Google's advanced projects and Levi and Nike have been championing the use of wearable technology. For Nike, this is in the sporting field, where its value in assessing fitness and performance is married with the far more important need to understand the long-term health of athletes, especially in contact sports.

Mobica has worked on SOLI for gesture recognition (radar) and Jacquard (gyro) for motion. Jacquard technology used by Levi's and Nike, Soli technology features in the Pixel phone.

Semiconductors form the bedrock for these applications but need the software and firmware above it in order to put an ecosystem in place that makes it a usable solution.

The two fundamental technological areas of artificial intelligence (AI) and trust, which is more typically referred to as security, have driven the demand for new semiconductor design and performance. The software and firmware part of the journey is also vital.

Connecting the hardware to the software

The capability of connecting the hardware to the software is at the core of Mobica - a Cognizant company - services. When a device needs a driver, whether it be GPU or Ethernet adapter, Mobica is often asked to assist and we cover all other aspects of connecting the hardware by developing and optimising systems software and firmware.

Our customers included industry leaders such as BMW, Jaguar Land Rover, Cariad in the automotive industry and ARM, Imagination Technologies as well as Samsung in the semiconductor industry.

The customers of these customers are demanding smarter products, which now means using AI and products they can trust, which means better security technology.

The new wave of chips - privacy, security and trust

This new wave of chips supports trust in new products and services, but includes well understood cryptographic theory as features in the chip set or SOC. The algorithm was initially devised by mathematician Clifford Cocks who, in the early 1970s, while working at the United Kingdom Government Communications Headquarters (GCHQ), developed public key cryptography (PKC). It was developed into a solution known as public key encryption (PKE), by Rivest, Shamir and Adleman (RSA) who established a company to commercialise it.

This algorithm and digital certificates infrastructure has been widely used since the 1990's - but it has been implemented at the network, (the IP layer) to deliver 'virtual private networks' (VPNs) with IPSec protocol and at the Transport layer, via the TLS implementation, to deliver security to web browsers, text messages and email for example. The problem is that neither of these prevents interception or 'man in the middle' attacks at the physical media level - that is the processor.

Mobica has worked on SOLI for gesture recognition (radar) and Jacquard (gyro) for motion. Jacquard technology used by Levi's and Nike, Soli technology features in the Pixel phone

Consequently semiconductor industry participants have developed frameworks and IP to ensure that customer information and data can remain private, not only when 'at rest' i.e in a storage medium, or when 'in flight' i.e. over communication protocols such as HTTP, but now when 'in use'. The expression 'secure, at rest, in flight and in use' has become commonplace over the last 3-5 years.

Two companies that have introduced semiconductor technology to support this are Intel and ARM. Intel is most famously associated with the PC and data centre, whereas ARM licences technology to companies such as Apple, Qualcomm and Samsung and, between these two ecosystems, the cloud to edge security is covered.

Intel delivered the Intel Trust Authority, offering a unified independent assessment of its Trusted Platform Module. TPM came from the Trusted Computing consortium and provides circuitry to implement PKI down to the processor level in both the PC and data centre. The Trust Authority provides a framework for independent attestation that nothing has touched, read, or in any way interfered with your data.

The key point is that the TA services will give users confidence that confidential information placed in the cloud remains secret, even from those that operate the cloud. There is nothing that they can do, at the container, hypervisor or OS level that gives them the privileges to access this. This is vitally important for many industries e.g. banking, pharmaceutical, for its drug research data chemical industries, for product recipes.

ARM provides its Platform Security Architecture (PSA) as a common industry framework for IoT devices. PSA helps developers define a consistent level of security by providing principles and deliverables, including threat models, architecture specifications and open source firmware.

For its Cortex A architecture, the heart of most mobile phone SOCs, it has created Trust Zone, which is commonly used to run trusted boot and trusted OS to create a Trusted Execution Environment (TEE). Typical use cases include the protection of authentication mechanisms, cryptography, mobile device management, payment, key material, and digital rights management (DRM).

These two frameworks add the semiconductor integrity to well understood trust algorithms, providing the integrity required for customer trust of the product. Naturally, even though these foundations are in place, it requires excellent and experienced software and firmware engineering to implement an error free solution. Mobica works with chip manufacturers and smart product manufacturers to ensure that the implementation includes all valid specifications and verifies that the specifications are implemented accurately.

To the consumer, they can have confidence that these products and services will prevent unauthorised access to property or theft of vehicles. If used for monitoring services - and if the provider transfers sole access and data to the consumer - then the same technology can be used to prevent 'big brother' scenarios, whether from government or organisations.

The future functions of AI PC

The AI features in the new semiconductor solutions work in tandem with trust features to combat information overload. The vast majority of work activity today requires handling large amounts of information and data.

Recently at Mobile World Congress (MWC) in Barcelona, a partner discussion posited a few examples of where AI assistants either help, or may help, reduce overload. The first example was for office productivity where the new AI PC - which was being promoted - would feature applications that could summarise and prioritise emails and the coming week's meetings, in conversation with the PC. This might be possible, but there is a lot of software engineering and LLM training and application development to be done before this would work faster and more accurately than doing it yourself.

As the diversity of document and file types and stores proliferate, this capability will be much needed - particularly thanks to phones, drives (Apple, Gdrive, Onedrive) mail (Gmail, Outlook, Thunderbird, Apple), messaging apps (Slack, WhatsApp, Messenger) and social media (Snapchat, Facebook, Instagram, TikTok).

This is particularly the case since the AI PC is taking the workload off the CPU, resulting in a more responsive and power efficient PC. For example, tests show that blurring the background for video conferencing (an AI task) takes up to 20% of CPU

cycles. This goes down to 1% with the AI NPU offload and gives a 38% power saving when tested with ZOOM. Further examples included translating sign-language to english in real-time which was not possible with earlier PC generations but is now a possibility, using CPU, GPU and NPU in the AI PC to deliver this.

Microsoft has co-opted the term 'Co-pilot' for embedding AI technology into OS's and applications. It's a good term, better than 'digital twin' as it confers the notion of assistance. As Mobica is a software and firmware solution provider, benefits from assistance in writing both are appreciated, but it's not a panacea, even for programming, where logic and algorithms are documented in Open Source repositories such as GitHub and GitLab.

The best illustration of the journey still to be taken was presented by Fireship - a popular technology YouTube channel. It's worth looking at 'Devin' - a product from Cognition AI labs - which accesses a terminal, browser, coder editor like a SW engineer and is designed to work like an SW engineering expert. It iterates, through from requirement, to code fragments similar to the issue and generates code, runs it, tests it and more, until the requirement is met.

As a product, it is comparable to AutoGPT, where LLM is also the base technology, but Devin gets the ability to perform actions and react to the feedback from those actions.

They demonstrated the product using the "SW Engineering Benchmark", which is closer to real SW engineering challenges, than what is commonly used for demonstrating other 'co-pilot' type products.

The benchmark provides an evaluation framework including 2,294 software engineering problems drawn from real GitHub issues and corresponding pull requests across 12 popular Python repositories. Given a codebase along with a description of an issue to be resolved, a language model is tasked with editing the codebase to address the issue.

The table below shows the results:
Whilst 13.85% is a step change compared to previous LLM products benchmark results, it is not the end of software and firmware engineering as a career. In fact the need for experienced engineers is likely to continue to grow.

The ongoing importance of software engineering

The new performant semiconductor products provide the foundation for these new solutions, both in the cloud (large scale) and at the edge (small scale), but engineering the complete stack requires skilled software engineering services.

It is imperative that we continue to train and develop engineers that understand the performance parameters, strengths and characteristics of new and developing software, whether that's AI technologies (LLMs, SLMs, DNN RNNs), cryptographic, compression or performance accelerators, which is something Mobica, and its parent Cognizant delivers.

Tool	% Issue Resolved
Claude2	4.8%
SWE Llama 13B	3.97%
SWE Llama 7B	3.01%
GPT-4	1.74%
ChatGPT-3.5	0.52%
DEVIN	13.85%

siconnex

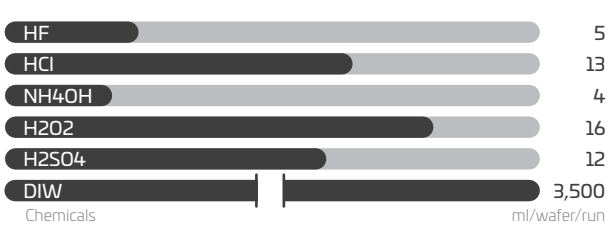
SOLUTION FOR CHEMICALS SHORTAGE

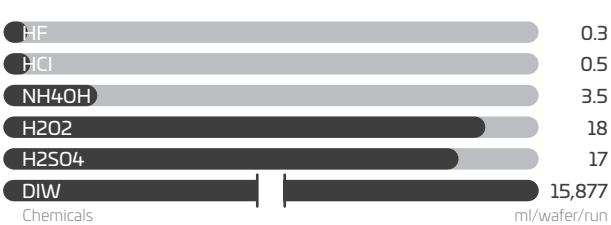
ELIMINATE H_2SO_4 AND H_2O_2 WITH OUR TECHNOLOGY

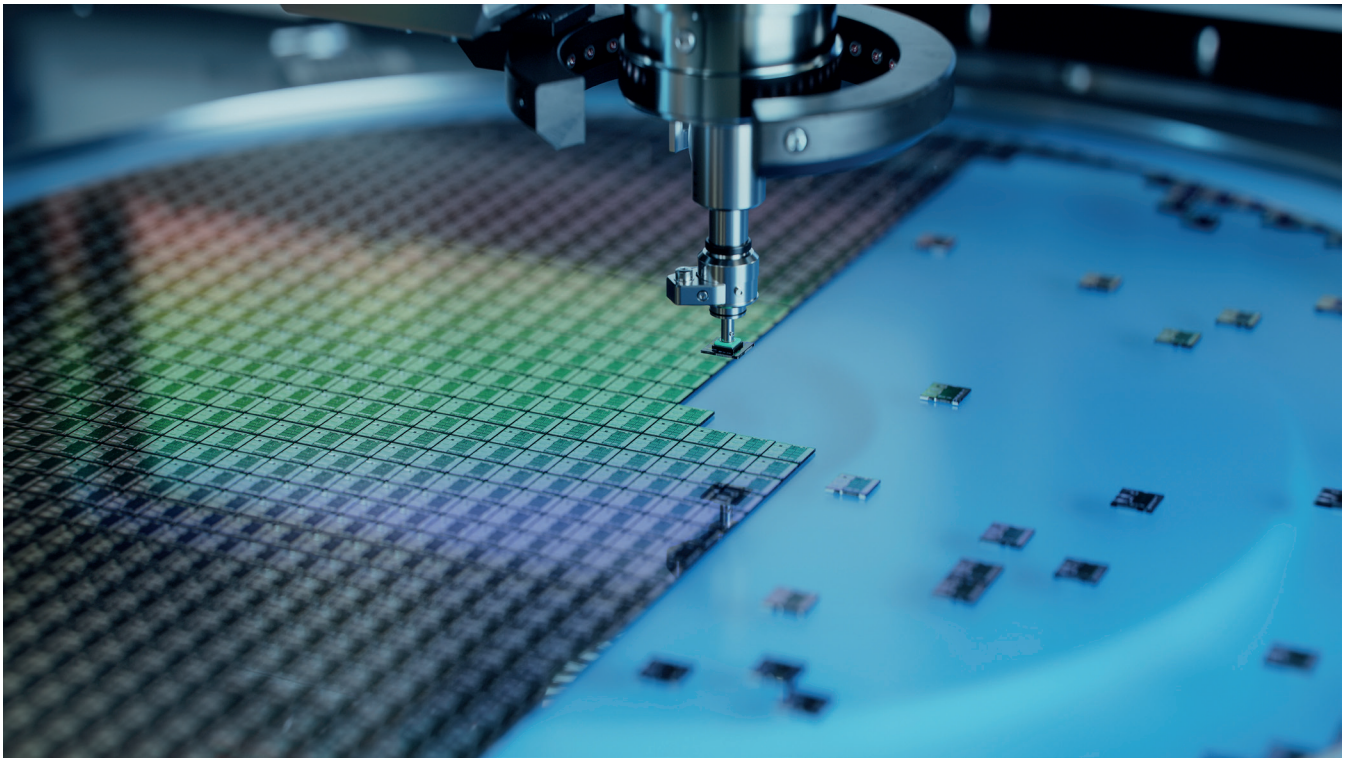
sicOzone by siconnex

Ongoing supply chain disruptions impact the industry, leading to anticipated shortages and rising prices in cleaning chemicals, as forecasted by researchers like TECHCET. Smart utilization of ozone, along with the usage of minimal amounts of ammonia and acids, result in significant cost savings. This approach can replicate traditional cleaning steps and enhance organic cleaning efficiency in SC1, SC2, and DHF processes, with precise control by using inline spiking technology.

Chemical consumption: SicOzone vs. conventional cleaning applications







Semiconductors in a world without PFAS

At the end of the day, the world's reliance on semiconductors isn't going away, but semiconductor manufacturers likely won't get to avoid PFAS requirements, even if their products are vital. They almost assuredly need to act now to avoid disruptions in their supply chain as PFAS restrictions tighten

BY NEIL SMITH, A REGULATORY AND SUSTAINABILITY EXPERT FOR ASSENT.

FROM THEIR USE in our smartphones and laptops, and video game systems and chips for our appliances and vehicles, semiconductors play a vital role in our economy and everyday lives. The increasing demand for semiconductors around the globe has a profound impact on both business and geopolitics, with manufacturers and governments positioning to protect their supply of these important materials.

One complication to future semiconductor production is the current and upcoming changes to legislation surrounding the use of perfluoroalkyl and polyfluoroalkyl substances (PFAS), particularly in North America and the EU. These changes will result in restrictions on PFAS, potentially creating supply issues for companies in the semiconductor industry. Procurement professionals are working vigorously to ensure they have a sustainable stockpile of semiconductors to keep their operations running smoothly and avoid supply chain disruptions.

Why would the regulation of PFAS have such a profound impact on semiconductors? The equipment and technology used to manufacture semiconductors are often reliant on PFAS, and there are no suitable alternatives readily available in the marketplace. The reality is that as PFAS restrictions continue to tighten, they will create severe disruptions for manufacturers in the areas of intellectual property and confidentiality; machine obsolescence, redesign, and derogation/exemption determinations; equipment maintenance and repair; and management of end-of-life e-waste.

Confidentiality & intellectual property

The importance of semiconductors is not lost on governments and NGOs. The EU's REACH Annex XVII PFAS restriction proposal initially suggested exemption periods (derogations) of five and 12 years, based on risk and socioeconomic assessments. Semiconductor manufacturing was a commonly referenced example of why such a process was necessary.

Although the U.S. Environmental Protection Agency's Toxic Substances Control Act (TSCA) PFAS reporting rule does not currently exempt

semiconductor manufacturers, state-level PFAS restrictions in Maine and Minnesota allow exemptions for unavoidable use.

Even in cases where exemptions exist, it's not likely the derogation/exemption period will give industry enough time to adjust without significant pain and disruption. This is due to the sheer volume of data that needs to be collected from the supply chain concerning PFAS use, and the long lead time involved in product redesigns if they are necessary. To put it simply, if companies want to get ahead of their requirements, the time to map PFAS use in the semiconductor manufacturing process is now.

Even if an extended use period is granted, it doesn't mean companies are exempt from submitting data on PFAS usage. Product-level reporting requirements have created new challenges for the semiconductor industry as well. Historically, downstream manufacturers that requested PFAS information from semiconductor manufacturers were denied on the basis that the data was confidential business information (CBI) or intellectual property (IP). Now, there is a growing understanding that these inquiries are based on regulatory pressures and reporting obligations associated with PFAS. This has resulted in a shift in the way these types of inquiries are handled. Companies that encounter true IP roadblocks may need to do joint filings with their suppliers, or the suppliers will need to work with customers so they can meet their obligations in a manner that protects supplier IP/CBI.

Machine obsolescence, redesign & derogation

Staying ahead of upcoming regulatory changes also means taking a hard look at the semiconductor manufacturing equipment that relies on PFAS.

Even if a company receives a 12-year derogation, there is a strong possibility that these machines will have a decades-long service life that stretches beyond the regulatory obsolescence period. As such, the company may face significant challenges if they have to routinely re-supply parts or other materials that contain PFAS as part of maintenance and repair. The machine may become a victim of unplanned obsolescence much sooner than intended.

A derogation/exemption could allow for continued PFAS use for maintenance and repair of equipment already on the market. But there is still a risk that the manufacturers of maintenance repair and operations (MRO) parts and materials see the market dry up because they are now only supplying pre-existing machines — a small amount of the market. That, coupled with heightened regulatory scrutiny and increased liability burdens, could easily lead them to significantly raise prices or, in a worst-case scenario, exit the market completely. In that worst case, their customer would then have an unplanned, non-regulatory supply chain obsolescence. In many cases, this will be the reality more so than the regulatory obsolescence. Companies have so many different moving parts to consider in a world where PFAS is restricted. Even if they're allowed to use those substances, will they still have access to them?

It is worth noting that the packaging side of semiconductor manufacturing could also be profoundly affected. Some of the semiconductor manufacturers use PFAS-containing protective coatings like films for shipping purposes, which would add another layer to their production challenges and potential supply chain disruptions.

End of life/e-waste

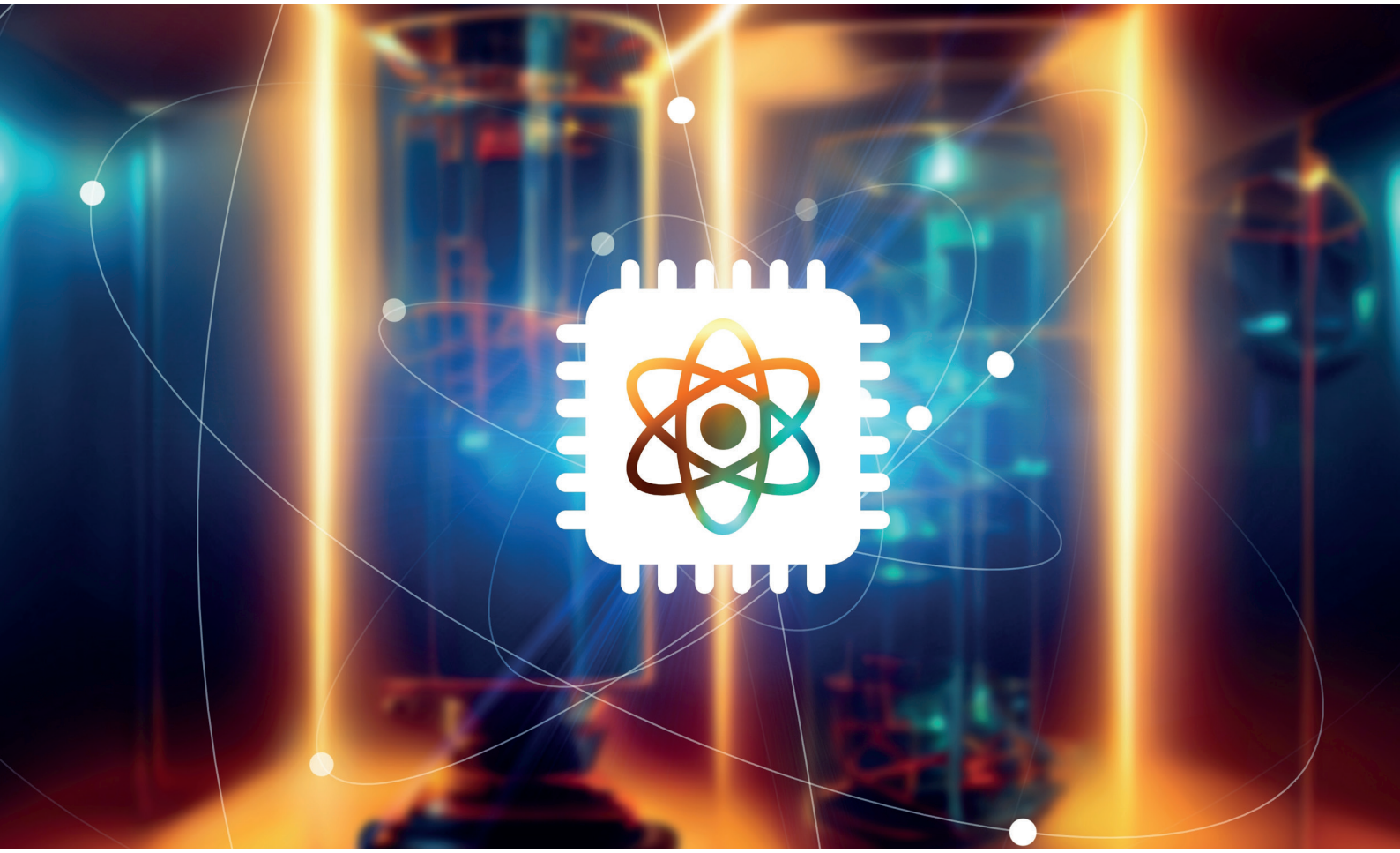
The EU is very committed to a green circular economy, including end of life. Many other jurisdictions globally also have e-waste extended producer responsibility programs in place. In the future, companies may have the challenge of figuring out a way to extract PFAS or "forever chemicals" from e-waste at end of life, which raises the question of how to treat and properly dispose of substances when there are no easy treatment technologies currently available. This derivative problem has to be solved, but it's not even being considered as an overhang yet.

Manufacturing engineers will be asking, "How do I know where PFAS are in my products and manufacturing operations?"

Product engineers will ask, "How do I remove those PFAS and what do I do with them after?"

Everyone reading this is asking, "How did I find myself in this PFAS disaster?"

At the end of the day, the world's reliance on semiconductors isn't going away, but semiconductor manufacturers have a lot of hurdles to overcome in the transition to a PFAS-regulated and PFAS-restricted world. They will need to collaborate effectively with their customers and suppliers, and rely on deep visibility into their supply chains to keep their operations running smoothly.



The crucial role of ADCs and DACs in scaling quantum computing

In recent years there has been a surge in interest surrounding the topic of quantum computing and heightened anticipation about its potential to revolutionise the technology world. However, its future relies heavily on the complex interplay with a broader set of factors. While qubits may steal the spotlight, the Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) operating behind the scenes play a vital role.

BY CHRIS MORRISON, DIRECTOR OF PRODUCT MARKETING, AGILE ANALOG

FIRSTLY, let's give a brief overview of what's involved with quantum computing.
At the heart of quantum computing lies the quantum elements such as qubits and gates.

Qubits are the fundamental units of quantum information. Unlike the classical bits we use in conventional computers, which can only exist in a binary state of 0 or 1 at a given moment, qubits can simultaneously occupy states of 0, 1, or even a combination of the two, thanks to a quantum phenomenon known as superposition.

This unique property of superposition allows qubits to perform parallel calculations, offering ground-breaking potential for quantum computing applications. Whereas classical bits can only represent one state at a time, qubits can exploit the richness of quantum mechanics to process a multitude of information simultaneously, offering exciting prospects for solving complex problems.

A quantum gate (or quantum logic gate) is a basic quantum circuit operating on a small number of qubits. Quantum logic gates are the building blocks

of quantum circuits, like classical logic gates are for conventional digital circuits. They manipulate qubits to perform quantum operations.

Below is a short description of different types of quantum computer.

Superconducting quantum computers use superconducting circuits to create qubits. In order to preserve their quantum characteristics, the circuits are cooled to incredibly low temperatures. Superconducting quantum computers are comparatively advanced and capable of carrying out a large number of computations. However, they are highly sensitive to their environment and can be difficult to scale to larger sizes.

Trapped ion quantum computers use trapped ions to produce qubits. Ions are atoms that have lost or gained electrons, and they can be trapped in an electromagnetic field. Though complex to construct and operate, trapped ion quantum computers are nonetheless a relatively mature technology.

Photonic quantum computers use photons (particles of light) to form qubits. These are still in the early stages of development but are thought to be scalable because photons can be easily delivered over great distances with the use of optical fibres. In addition to being challenging to build, photonic quantum computers require specialized hardware.

Neutral atom quantum computers use neutral atoms (atoms that have not lost or gained electrons) to create qubits. These too are in the early phases of development and have the potential to be highly scalable. This is due to the ease with which lasers may be used to trap neutral atoms. Neutral atom quantum computers are also complex to build and need specialized hardware.

Why are ADCs and DACs needed?

The control and measurement of qubits often involve converting between analog and digital signals. This is where ADCs and DACs come into play.

Role of Analog-to-Digital Converters (ADCs)

ADCs are instrumental in quantum control, converting analog signals from the measured qubits into digital data that can be processed by standard control systems. Advances in ADC technology have led to the development of high-resolution converters capable of accurately capturing quantum signals with minimal noise and distortion. These ADCs also enable precise measurement of quantum states, providing the feedback necessary for real-time control and error correction in quantum systems.

ADCs for sensitive readout

After performing quantum computations, the qubit states need to be read out. This involves measuring weak signals that are converted to digital form using ADCs. Each qubit needs between 1 and 3 ADCs depending on the implementation. Key considerations for ADCs in this context include:

- **High sensitivity and dynamic range**

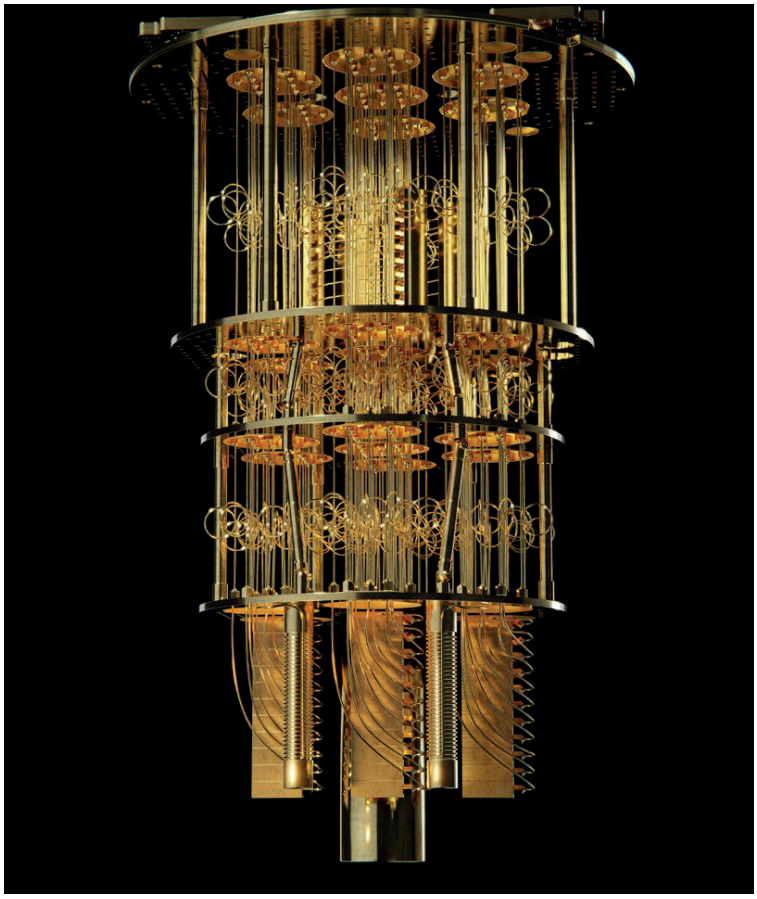
The ADCs must be highly sensitive to capture the faint signals from the qubits and possess a wide dynamic range to accommodate the full range of potential values. In general, these control signals need to be between 5 and 12 bits of resolution.

- **High speed**

Efficient readout relies on ADCs with fast sampling rates to capture the rapid changes in the qubit states. With today's technology, quantum computers are moving from ADC sampling rates of 10s of MSPS up to 100s of MSPS, or even 1GSPS.

Role of Digital-to-Analog Converters (DACs)

DACs play a key role in quantum control by converting digital control signals into analog voltages or microwave pulses used to manipulate qubits and implement quantum gates. Recent developments in DAC technology have focused on increasing speed and precision, allowing for faster and more accurate control of quantum operations. These DACs enable the implementation of complex pulse sequences and control algorithms, leading to improved gate reliability and quantum algorithm performance.



DACs for precise control

Quantum gates, the fundamental operations performed on qubits, are implemented through carefully designed control signals. There is typically a requirement for 2 to 5 DACs per qubit.
DACs with the following features are essential:

- **High resolution and speed**

Precise manipulation of qubit states requires DACs with high resolution (8-12 bits) to accurately represent the complex control signals and fast settling times (nanoseconds or faster) to ensure minimal signal distortion. Again, with today's technology, quantum computers are moving from DAC sampling rates of 10s of MSPS up to 100s of MSPS, or even 1GSPS.

- **Low noise**

Any noise introduced by the DAC can lead to errors in the control signals, compromising the fidelity of quantum operations.

> Maintaining low power consumption is absolutely critical to the overall energy efficiency of quantum computers. Taking the example of 8,000 or 8 million converters, if these all consume 1mW then this leads to a total consumption of 8 Watts or 8,000 Watts

Requirements of different qubit technologies

Whilst all forms of quantum computers make extensive use of ADCs and DACs, each particular quantum computing topology has its own specific requirements.

The requirements for ADCs and DACs can vary. For example:

Superconducting qubits

- **ADCs**

Low-noise, high-bandwidth ADCs are required to measure the weak signals from the resonators used for readout.

- **DACs**

High-fidelity voltage or current DACs are needed to generate the precise microwave control signals.

Trapped ion qubits

- **ADCs**

High-sensitivity, high-speed ADCs are needed to convert the weak fluorescence signals from the trapped ions during readout.

- **DACs**

High-speed, high-resolution DACs are used to modulate the intensity and phase of the laser beams for control.

Challenges of ADC and DAC integration

Integrating high-performance ADCs and DACs into quantum computing systems presents several challenges:

- **Miniaturization**

As the number of qubits increases, the need for compact and scalable ADCs and DACs becomes crucial. For example, if you need 3 ADCs and 5 DACs for each qubit and you want 1,000 qubits, you need 8,000 converters. So, 1 million qubits need 8 million converters!

- **Integration**

Seamless integration of these converters with the qubit control and readout electronics is essential for efficient system operation.
Power consumption

Maintaining low power consumption is absolutely critical to the overall energy efficiency of quantum computers. Taking the example of 8,000 or 8 million converters, if these all consume 1mW then this leads to a total consumption of 8 Watts or 8,000 Watts. This all generates significant heat and modern cryostats are only capable of maintaining their temperature with between 2 and 5 Watts of internal dissipation.

Control electronics

Control electronics interface with quantum systems to provide precise control and measurement capabilities.

- **Issues with external control electronics**

Currently, most quantum computers have their control circuitry, including ADCs and DACs, housed outside the ultra-cold cryogenic chamber (cryostat) where the qubits reside. This approach, while functional for small-scale systems, presents a significant bottleneck for scaling to thousands or even millions of qubits.

- **Limited scalability**

The number of qubits that can be controlled is restricted by the physical limitations of the cryostat. Routing numerous control cables for each qubit, including those for ADCs and DACs, becomes impractical and cumbersome as the number of qubits increases.

- **Signal degradation**

Long control cables introduce signal degradation and noise, leading to errors in qubit control and readout. These errors become more pronounced with increasing cable lengths, hindering the fidelity of quantum operations.

Increased complexity
Managing and routing numerous control cables outside the cryostat adds to the complexity of the system, making it difficult to maintain and scale.

Advantages of integrating control electronics within the cryostat

Integrating control electronics, especially ADCs and DACs, directly within the cryostat holds the key to overcoming the scalability bottleneck and paving the way for building larger and more powerful quantum computers. There are several advantages:

Reduced signal degradation
By placing the ADCs and DACs closer to the qubits, signal losses and noise are minimized, leading to improved control and readout fidelity.

Enhanced scalability
With on-chip analog control electronics, the number of qubits that can be controlled is no longer limited by the number of cryostat feedthroughs. This allows for the construction of larger and more complex quantum circuits. Digital control circuity can be integrated within the cryostat or, due to the inherent noise immunity for digital signals, remain outside.

Simplified system design
Integrating the analog control electronics within the cryostat reduces the complexity of the system, making it easier to manage and maintain.

Challenges and considerations

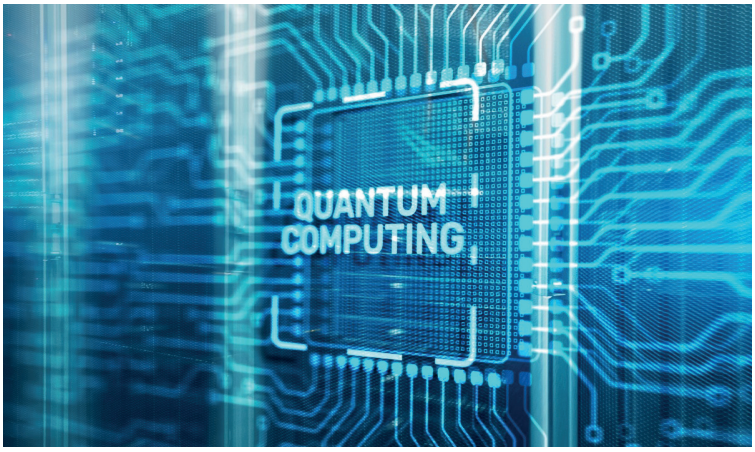
While integrating ADCs and DACs within the cryostat offers significant advantages, several challenges need to be addressed:

Harsh cryogenic environment
ADCs and DACs designed for room temperature operation need to be adapted to function reliably at cryogenic temperatures, normally around 4 Kelvin. This involves using specialized circuit design techniques.

Whilst semiconductor process technologies are typically characterized for operation from -40C to 125C, new models are required to design at these low temperatures. In addition, changes need to be made to the underlying transistors provided by the foundry to achieve optimal performance at these low temperatures.

Limited space
Integrating numerous ADCs and DACs within the limited space available near the qubits requires miniaturization and high-density packaging solutions.

Power consumption
Managing heat dissipation within the cryostat is crucial. Low-power ADCs and DACs are essential to avoid compromising the thermal stability of the system.



Scaling quantum computers

To achieve their true potential, there is a need to dramatically increase the number of qubits, from the several hundred that is possible today to millions.

These qubits have to be controlled, and by generating semiconductor IP that can operate at cryogenic temperatures, quantum computing developers can quickly design their own control ASICs that can be co-located with the qubits in the cryostat.

In the world of quantum computing, where operational qubits demand temperatures even lower than 4K, co-locating the analog control electronics close to the qubits within the cryostat is key for quantum computer scaling.

Advances in ADCs and DACs

As the field of quantum computing continues to evolve, the need for high-fidelity, low-noise, and high-speed analog components will only become more critical. Agile Analog is exploring opportunities to develop a range of cryogenic ADCs and DACs. The design team has acquired experience of some of the challenges involved during a project with sureCore, the ultra-low power embedded memory specialist, that delivered a cryogenic control ASIC in Global Foundries 22FDX technology, as part of an Innovate UK funded project.

Conclusion

The path towards a robust and scalable quantum computer is paved not only by advancements in qubit technology but also by the development of high-performance and reliable analog components. As quantum computers grow in size and complexity, the demands on the analog components increase. From generating control signals to amplifying weak qubit states, these components play a central role at various stages of the quantum computing stack. ADCs and DACs are poised to play a vital part in unlocking the full potential of quantum computing. The continuous development of high-performance analog electronics in tandem with advances in qubit technology will drive the evolution of quantum computing towards increasingly complex and powerful applications.

Silicon's dual role: Fueling AI's need for computation and connectivity

BY ALAN KEIZER, SENIOR TECHNOLOGY ADVISOR, AFL

SILICON IS THE BASIC building block of hyperscale technology. Pure silicon is highly reactive and, in nature, always combines with other elements – most commonly oxygen to form silicon dioxide (SiO_2), or silica, the material used in the construction of almost all optical fiber. Given their mutual material makeup, optical fibers and silicon semiconductors share similar timelines for innovation, miniaturization, and enhanced performance.

Co-design describes the collaborative approach to innovation across optical fibers and the system architectures configured for entire optical networks. More simply, performance optimization is made easier where the components and systems set up to improve scalability, efficiency, and resiliency undergo complementary refinements, benefitting the real-world applications of the dual technologies.

AI model training requires massive computational power (compute). AI's insatiable appetite for compute resources dwarves traditional computing workloads. The generative AI boom's growing need for seamless data processing ties R&D directly to silica optical fiber and silicon semiconductors.

Silicon's characteristic ability to selectively conduct electricity under controlled conditions makes it the preferred material for transistor fabrication – not only does AI connectivity rely upon advancements in silicon-based technologies, but advancements in the transistor world of switching, amplification, and digital logic operations also depends heavily upon miniaturized silicon structures to increase the transistors-per-microchip count. However, resolving the challenge evokes Moore's law.

Shrinking transistors and Moore's Law

In 1965, Gordon Earle Moore (co-founder of Fairchild Semiconductor and Intel) noted the predictable relationship between time passing and transistors per integrated circuit. Initially, Moore's observation stated transistor counts for microprocessors would double each year. In 1975, Moore revised this guidance, predicting the doubling in number of integrated circuit transistors every two years.

Interestingly, Moore's Law became an industry roadmap for long-term innovation, acting as a self-fulfilling prophecy for setting and realizing timeframes in technological advancement. Throughout the 1990s, Moore's Law settled on a doubling period of 18-24 months.

Lithographic advancements have given rise to precision component etching at the transistor component manufacture stage, enabling transistors to keep pace with Moore's Law. By steadily developing the process, modern lithography enables manufacturers to shrink transistor dimensions and improve performance. Over the decades, creative three-dimensional design and

high layer count have greatly contributed to higher density and lower power per unit of performance.

Let's take a closer look at real-world examples of chips with billions of transistors, progressing over time:

- **1971 - Intel 4004:** ~2,300 transistors, 10-micron process.
- **1995 - Intel Pentium Pro:** ~5.5 million transistors, 350-nanometer process.
- **2020 - AMD Ryzen Threadripper 3990X:** ~39 billion transistors, 7-nanometer process.
- **2024 - The Extreme Ultraviolet Lithography system** from ASML delivers 2nm features. Nvidia introduces the B100 accelerator with over 100 billion transistors based on 2nm technology.

The limitations and challenges in continuing this miniaturization trend indefinitely lie not only with the obvious physical boundary of silicon atomic size, but also in cooling – increasing component count in a decreased space brings considerable heat dissipation challenges, requiring research and investment into sophisticated cooling technologies. At the atomic level (where single digit nanometer technology is headed), the unpredictable presence of small dimensions can result in quantum tunneling, which when controlled is central to transistor operation but can have undesired outcomes when not intended. Quantum tunneling dictates that the atomic-scale proximity of components will see signal interference through uncontrolled electron sharing, rendering the processor ineffective.

Harnessing light at a miniature scale

The principle of total internal reflection underpins optical fiber technology. This phenomenon only occurs where the angle is shallow, much like skimming a stone on still water.

Innovations such as core-cladding and doping further enhance fiber's transmission of relatively lossless light signals. Utilizing the principle of total internal reflection, a less dense material forms the cladding around the denser fiber. Doping is used to control the numerical index of refraction (N) to create higher or lower N materials from which to fabricate the core and cladding elements of single mode fiber. The core typically has a slightly higher N than the cladding. Doping involves adding elements to both the cladding and fiber core, optimizing performance (especially over long distance). Specialized fiber types and doping techniques help to minimize signal loss. Optical fiber transmission speeds have increased from Mb/s to hundreds of Gb (and even Tb/s):

- **1980s:** Commercial systems at 565 Mb/s were state-of-the-art.
- **2000s:** 10 Gb/s links became standard for long-haul infrastructure.
- **2010s:** Coherent transmission techniques enabled 100 Gb/s and 400 Gb/s per fiber pair.

Today: Focus on terabit capacity per single fiber with advanced multiplexing and modulation.

Today, typical Single Mode Fiber (SMF) at 1550 nm wavelength has a loss of around 0.2 dB/km. Specialized Ultra-Low Loss fibers can achieve 0.15 dB/km or less, critical for extreme distances.

Wavelength-division multiplexing (WDM) multiplies fiber capacity. WDM can put 100+ wavelengths (colors) on a single fiber, each carrying tens or even hundreds of Gbps. Multiple colors of light can travel independently on the same fiber, significantly enhancing its bandwidth.

Optical components on silicon

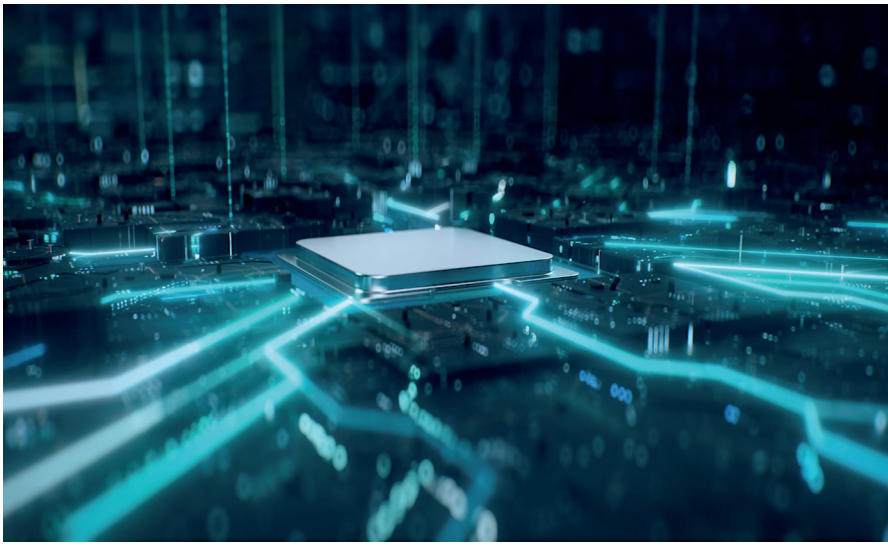
Advances in silicon photonics can help overcome the growing demand for high-speed connectivity. The technology enables electronic signal processing and light signal manipulation/transmission on the same chip. The reduced power consumption has applications across next-generation communication. Modern silicon photonic transceivers can achieve upwards of 1Tbps within a fingernail-sized package. The same manufacturing plants used for electronics can be adapted for silicon photonics, promising cost advantages.

Complementary Metal-Oxide-Semiconductor (CMOS) technology is the mainstay of integrated circuit construction. CMOS compatibility (e.g., high temperature threshold, using non-reactive materials such as silicon, and maintaining uniformity and performance when layering) is a consideration around optical waveguides, modulators, and detectors on silicon chips.

Electrical transmission on host printed circuit boards at very high data rates is limited in distance. 100G signals have a maximum transmission distance in high-performance circuit boards of 200mm or less.

Co-design: breaking boundaries for AI

Limitations in both semiconductor scalability and optical fiber capacity create system-level



bottlenecks. Where the interconnect speed is not matched, even the fastest GPU can be starved for data. Training machine learning (ML) models across multiple machines is essential to achieve reasonable processing times, emphasizing chip-to-chip and node-to-node communication to achieve high performance.

To illustrate the issue, consider the limitation placed on nanosecond computations where electrical data movement between chips becomes a bottleneck for AI. Co-packaged optics (CPO) provide viable market solutions.

CPO integrates optical communication components and electronic semiconductor chips, reducing both latency and power consumption. By creating a single package incorporating silicon and optics with high capacity and low energy consumption, the potential emerges for wider industry applications. Also, as silicon is not the optimal choice for some electro-optical devices, a different semiconductor platform represents a significant advantage (e.g., gallium arsenide phosphide or other III/V or II/IV compounds).
Examples include:

- **Telecommunications – 6G Radio Access Networks (RANs)**
  CPO will accelerate innovation across signal processing, integrated circuit architectures, and optical communications and packaging, leading to the emergence of 6G RANs – this includes AI-enabled Radio Access Network, Aerial Radio Access Networks (ARANs), and Open Radio Access Networks (O-RANs). Through greater use of RANs and the terahertz (THz) spectrum, 6G could launch commercially by 2030.

- **Medical – quantum dot lasers**
  Co-packaged optics systems enable the compact, energy efficient performance necessary for quantum dot lasers. Commercially available but not yet widely adopted, quantum dot lasers use quantum dot semiconductor particles measured in nanometers – much smaller than the bulk semiconductor material found in conventional lasers. Applications include precision laser surgery and tissue coagulation.

- **AI – training and inference**
  AI and machine learning require massive data processing and seamless data sharing between distributed computing systems. Integrating optical interconnects and packing more computing devices closer together can help reduce latency, enhance system performance, and accelerate data movement.

AI and machine learning require massive data processing and seamless data sharing between distributed computing systems. Integrating optical interconnects and packing more computing devices closer together can help reduce latency, enhance system performance, and accelerate data movement.

Hybrid switching brings together the benefits of both circuit and package switching to better accommodate diverse traffic (i.e., data centers can route latency-sensitive traffic such as video via circuit switching, whereas internet browsing can be routed via packet switching). Examples include:

- **Cloud networking**
  Hybrid switching enables greater connectivity between public cloud platforms and on-premises facilities.
- **Internet service providers (ISPs)**
  ISPs deploy hybrid switching to optimize service quality through networking resource allocation.
- **Data center networks**
  Data center hybrid switching may involve traditional core network ethernet switching for high-speed connectivity and network edge Software Defined Networking (SDN) switching for dynamic traffic management.

The holistic co-design approach breaks boundaries in support of AI system advances, resolving challenges across bandwidth, energy efficiency, and latency.

For example, instead of off-chip optical transceivers connected via electrical signals, silicon photonic chips could be placed directly next to AI processors, reducing the distance electrical signals must travel.

This reduced proximity is a consideration in electrical interconnect power consumption over various link distances. For example, consider a 100 Gbps link over 1 kilometer. In this scenario, electrical interconnects would consume a minimum

of 20 Watts where optical interconnects would consume less than 10 Watts.

The future: beyond silicon's limits

Co-design can help innovators to overcome the existing limitations of silicon. By incorporating emerging technologies, materials, and design ideas, co-design will revolutionize how we currently think about the inherent limitations of silicon-based solutions. Examples include:

- **III-V material integrations**
  Integrating silicon and elements from groups III and V in the periodic table to create semiconductor alloys can enhance carrier mobility, reduce power consumption, and enable previously unthinkable functionality.
- **Polymers and ceramics**
  Combining silicon with polymers and ceramics to create multi-functional, flexible, enhanced systems has potential commercial uses in bioelectronics and photonic integrated circuits. Wavelength splitters, comb filters, and modulators can be fabricated and integrated with waveguides to make compound optical devices.
- **Innovative design methodologies**
  Co-design facilitates technological integrations between silicon-based systems, enabling advanced modeling and simulation techniques used to enhance and optimize next-level manufacturability.

At this advanced stage, greater experimentation into wider materials – as mentioned above – is perhaps required to deliver on the promise of enhanced performance.

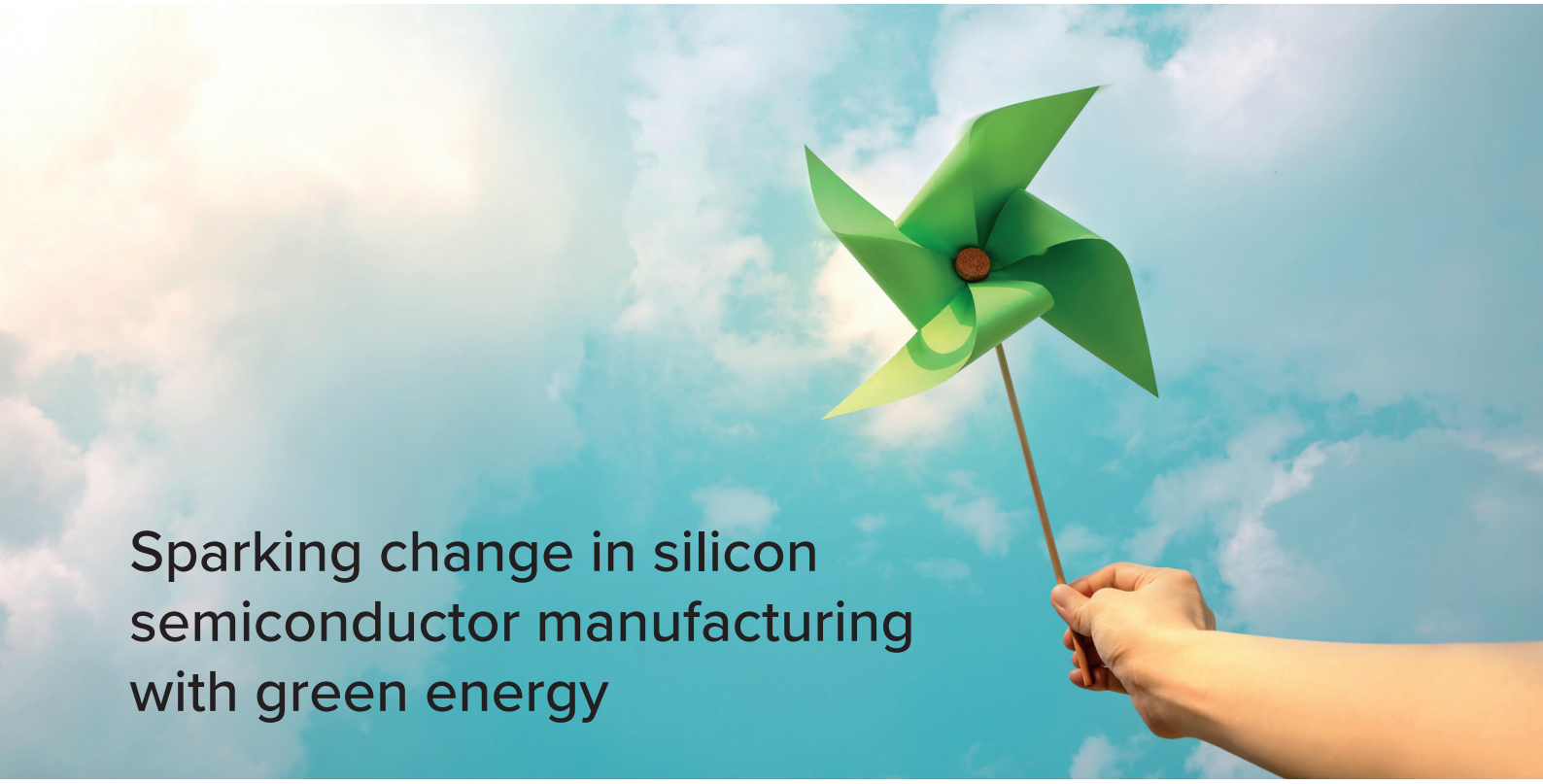
Conclusion

The journey from bulk silicon to sophisticated optical and computational components involves several complex stages, including wafer preparation, photolithography, and doping. The resulting high performance of silicon-based communication technologies pushes the limits of AI and connectivity.

Co-design between existing and new materials provides the logical next step in unlocking AI's potential. The industry – and indeed the wider world – awaits further innovation regarding quantum communication and photonic neural networks.

As these emerging technologies continue to mature, their convergence will bring new levels of security and increased processing power, along with the kinds of crucial energy efficiency upgrades necessary to revolutionize and scale AI applications.

From a scientific curiosity to everyday life, AI and the innovations that power its continued onward march are undoubtedly here to stay. Silicon is the common element.



Sparking change in silicon semiconductor manufacturing with green energy

In the ever-evolving tech landscape, few industries rival the energy demands of silicon semiconductor manufacturing. These energy-intensive businesses are the backbone of modern electronics, powering everything from smartphones to supercomputers. However, this vital sector faces a pressing dilemma: the soaring costs of energy amidst a global climate crisis.

BY PHIL THOMPSON, CEO OF BALANCE POWER

THE SEMICONDUCTOR INDUSTRY operates within a relentless energy consumption cycle, with dominant industry players consuming staggering amounts of power. Take Intel, for example. Its global energy use in 2022 amounted to 10.9 billion kilowatt hours. Nine billion of which marked electricity usage, reflecting how energy intensive the manufacturing of silicon chips is. As the price of energy has soared worldwide, the sector has faced eyewatering bills that have eaten into profits and in some cases, threatened the sustainability of their operations.

Compounding this challenge is the urgent need to decarbonise as governments worldwide implement stringent emissions reductions targets. With the manufacturing and production sector accounting for one-fifth of global carbon emissions, and with more than 80% of semiconductor industry emissions coming from the consumption of electricity, these companies are under mounting pressure to become more sustainable and transition to cleaner sources of energy.

A pathway to decarbonisation and profitability

Some of the biggest industry players have already taken strides towards making their operations more sustainable. Samsung, for example, announced its environmental strategy in 2022, where it pledged to join the global fight against climate change and achieve net zero emissions by 2050.

Despite these efforts, there's still a lot more that needs to be done. Semiconductor emissions are forecasted to overshoot the carbon budget for the 1.5C pathway by 3.5 times, and the industry is

predicted to fall short of net zero targets. There's a real need to accelerate sector-wide progress towards decarbonisation to ensure the viability of the semiconductor industry.

Decarbonising a business might seem like a complex ordeal. However, there is an attractive option that silicon semiconductor manufacturers have at their disposal – switching to renewable energy to power their operations. Not only does this align with global sustainability goals and targets, but it also offers other tangible benefits, including reduced operational costs, enhanced operational resilience and lower carbon footprints.

Business's that use clean energy from solar panels, wind turbines or other renewable sources free themselves from the volatility of the global energy market and benefit from more stable and predictable sources of power. And, as renewable energy is cheaper than fossil fuel alternatives, it can significantly slash a businesses' energy bills.

Behind-the-meter generation: a pioneering solution

Despite the clear benefits, many companies remain unaware of the feasibility of this transition. Instead, they remain locked into costly contracts with grid-dependent energy suppliers, perceiving renewable energy as an inaccessible luxury.

However, renewable energy has become increasingly accessible for businesses through 'behind-the-meter' generation. This usually involves a partnership between a business and a clean energy developer, who identifies the most effective method for generating renewable energy. This is typically through installing solar panels or wind turbines on the manufacturer's premises or in a field nearby. The power that is generated by the renewable energy source is fed directly to the business, avoiding many of the third-party costs and other charges that are normally added to an energy bill.

This approach has already been adopted by Samsung Semiconductor as part of its environmental strategy, which pledges a transition to 100% renewable energy-based electricity across all its global business sites by 2050. Since 2020, its US and Chinese business sites have been powered by clean energy through installing large-scale renewable facilities.

In the case of Balance Power, we help energy-intensive businesses, including manufacturers, identify the right solution for their specific size and needs, before financing and building a renewable energy project. So, all they need to do is buy the energy they use – it's that simple.

Strategically positioning renewable energy projects near semiconductor facilities offers a compelling alternative to traditional grid-based power sources. Not only does it represent a cleaner and more autonomous energy option, but it also promises substantial cost savings, easing the financial strain on businesses while reducing their carbon footprints. Plus, behind-the-meter generation doesn't rely on a one-size-fits all approach. It can be customised to suit each company's unique energy requirements and constraints, from the largest manufacturers like Samsung Semiconductor to those who operate on a smaller scale. These renewable energy projects are designed to seamlessly integrate into existing operations, putting cheaper and cleaner energy sources within reach.

Strategically positioning renewable energy projects near semiconductor facilities offers a compelling alternative to traditional grid-based power sources. Not only does it represent a cleaner and more autonomous energy option, but it also promises substantial cost savings, easing the financial strain on businesses while reducing their carbon footprints

The way to a greener future

As the semiconductor industry navigates the complex intersection of energy demand, sustainability, and profitability, the case for adopting renewable energy grows ever more compelling. Paradoxically, semiconductors themselves play a key role in facilitating the transition towards a decarbonised economy, with the increased use of electric vehicles and renewable energy technology driving demand for chips. But it's crucial for the industry to build sustainability into its manufacturing processes to properly support a net zero future.

By adopting renewable energy, silicon semiconductor manufacturers not only reduce their environmental impact but also bolster their bottom line, enhance their competitiveness and future-proof their business.

A sustainable semiconductor industry needs smarter water management

As the industry expands exponentially, so does its needs for water. **Dan LeCloux, SVP of Research, Development, and Engineering for Ecolab's Industrial division,** says responding to growing demand responsibly requires companies to look at sustainability, water stewardship and productivity through a circular lens. While **Mukul Girotra, vice president and general manager of Global High Tech for Nalco Water, an Ecolab company,** shares his perspective on how manufacturers can use smart water management to balance sustainability, productivity and reliability in their operations.

SIS: *Water stress is a growing issue worldwide. How does this impact semiconductor manufacturing, especially considering the water intensity of the industry?*

DL: Manufacturers are facing significant and seemingly paradoxical challenges. On one hand, water stress remains a critical reality, with global freshwater demand projected to outpace supply by up to 56% by 2030 (according to the World Resources Institute). At the same time, the need for water in manufacturing continues to grow exponentially. The United Nations estimates demand will have increased by 400% between 2000 and 2050.

The microelectronics industry makes up a significant proportion of manufacturing water use, and many companies are actively seeking opportunities to reduce their water footprint. The industry is expected to grow by 6-8% every year through 2030, and its water requirements will scale accordingly.

Some semiconductor fabricators turn to air-cooled technologies as an alternative, but air-cooling requires substantial energy that results in increased greenhouse gas emissions – a significant trade-off. To build resilient, responsible operations, manufacturers need to look at water, climate and productivity together through a circular lens so they can minimize environmental impacts while maximizing production output and quality.

SIS: *How would you characterize the complexity facing the microelectronics industry?*

MG: Demand for smart phones, wearable devices and other technology continues to surge. Regional policies support expansion of the industry to meet demand, such as the CHIPS and Science Act legislation in the United States. At the same time, the semiconductor components that power this technology have gotten smaller – a trend driven by innovation in the industry. As a result, manufacturers must reconcile growing production requirements with increasingly elaborate processes as they work with reduced feature sizes.

Semiconductor fabricators also face pressure related to the water intensity of their operations. As an example, estimates suggest a single smart phone requires more than 3,000 gallons (11,300 liters) of water to produce. In response, many manufacturers are looking for circular strategies to manage and minimize water consumption while meeting their productivity goals.

SIS: *How can a manufacturer evaluate their water intensity? What's a practical first step?*

DL: It starts with a plant assessment that results in a sustainability plan. Water use goes beyond linear treatment within the plant itself; it impacts the surrounding community. When conducting a plant assessment, semiconductor fabricators need to look inside and outside the facility fence to examine their water needs against available resources. Opportunities often exist to reduce, reuse, and recycle water from specific processes, or even from effluent sources, for utility applications, like cooling water make-up. By identifying these types of opportunities, manufacturers can build a smart water management approach that minimizes community strain and still prioritizes business objectives like yield, uptime and product quality.

SIS: *What makes the water demands of semiconductor manufacturing unique when compared to other industries?*

MG: As semiconductor components get smaller, the water requirements of manufacturing processes get more stringent. Fabricators rely on ultrapure water sources to produce semiconductors, and the quality of ultrapure water helps maintain the integrity of the delicate circuits on semiconductor wafers.

In addition to ultrapure water, semiconductor manufacturers also need to manage utility and wastewater operations like other industries. Cooling towers, chillers and boilers require treatment programs to minimize corrosion, scaling potential, and other risks, and wastewater streams can contain metals, fluoride and other contaminants that must be removed. Altogether, these water sources require a specialized approach — what we call 'smart water management' — to help semiconductor manufacturers minimize use, maximize quality, and reduce potential risks that could impact manufacturing assets.

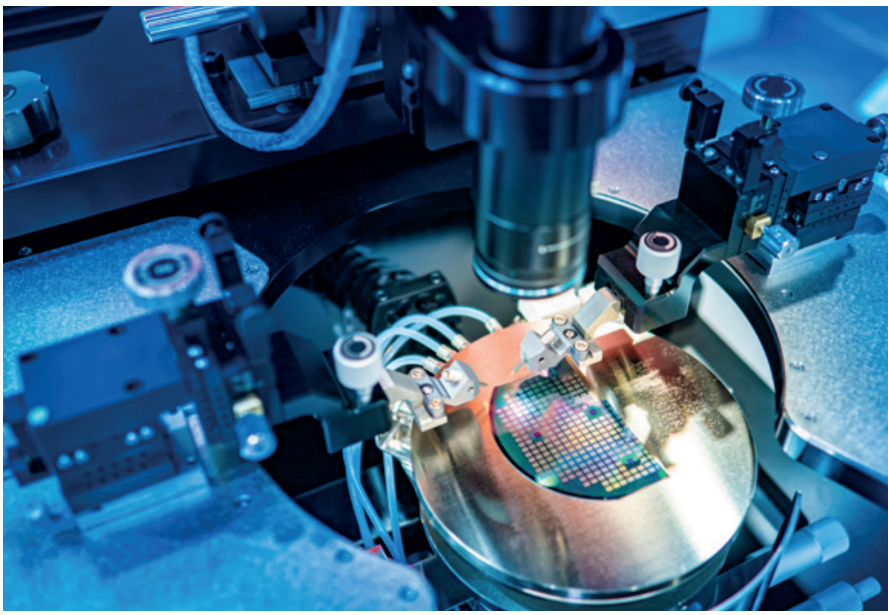
SIS: *Are there specific factors to consider when identifying water reuse opportunities?*

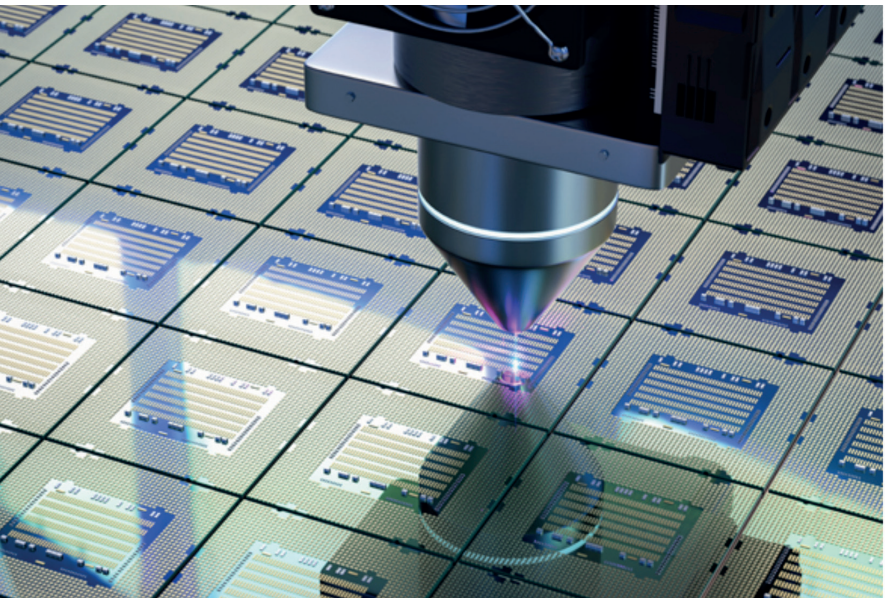
DL: Recycling water requires an understanding of the composition of each available water source, as well as its end use. Different water sources require specialized forms of treatment to remove containments that can cause fouling, scale potential, or other risks. For example, effluent wastewater requires a treatment program that addresses the most critical components in the water stream, such as metals or fluoride. An optimized program can help a fabricator recycle and treat water to meet specific quality requirements, allowing them to reuse the water as utility make-up water in their operations.

To give a specific example of our work in this space, we helped a Texas-based manufacturer, NXP Semiconductor, reclaim water from its fabrication processes for use in the utility center's cooling towers. We knew this solution would only work if we took steps to protect the assets from contaminants in the reclaimed water, such as phosphates, fluorides, sulfates, chlorides, ammonia and silica, as well as naturally occurring hardness caused by calcium and magnesium. These contaminants can increase corrosion, scale and other risks in the cooling water system.

By combining 3D TRASAR™ automation technology, Ecolab Global Intelligence Center monitoring and comprehensive on-site service, we delivered a real-time corrosion control solution that led to significant results. In a single year, the manufacturer saved 7.2 million gallons (27.2 million liters) of municipal water and reduced wastewater discharge by 8.5 million gallons (32.1 million liters).

SIS: *Can you explain the smart water management concept? What does it entail?*





MG: Smart water management looks at the water needs of a semiconductor manufacturer holistically. Our approach combines digital technology with innovative chemistry programs and institutional expertise to help companies address water use, productivity, and other sustainability levers — like energy and greenhouse gas emissions — all at once.

Digital solutions, like 3D TRASAR™ technology powered by the ECOLAB3D™ intelligence platform, can measure water system performance at the asset, site and enterprise level. With visibility to water consumption, quality conditions, and other insights, semiconductor manufacturers can keep a pulse on the health and reliability of their operations in real time. These solutions, in concert with innovative treatment programs and global expertise, help semiconductor manufacturers maintain efficient, optimized operations.

Smart water management starts with understanding the needs and risks inside and outside the manufacturing fence, as well as water's impact on other sustainability levers like energy and greenhouse gas emissions. Water must be moved, heated, cooled and treated during the manufacturing process, which consumes energy and generates greenhouse gas emissions. Efficient water management strategies can help semiconductor manufacturers reduce energy consumption, and in turn, minimize greenhouse gas emissions.

SIS: *You mention real-time monitoring and automation. To what extent do digital tools and innovation drive water savings opportunities, particularly for microelectronics?*

DL: Digital innovations can help manufacturers gain insight into water use and quality in real time. Through digitally enabled tools, manufacturers can take targeted corrective action quickly and address system upsets before they impact operations.

For example, 3D TRASAR™ technology detects out-of-spec conditions and determines the appropriate actions automatically. By using Connected Chemistry™ capabilities, 3D TRASAR technology can rapidly respond to conductivity, pH levels, turbidity, flow rates, corrosion risks, scaling potential and other issues. The technology integrates with digital services like Water Quality Intelligence – a solution that is powered by the ECOLAB3D™ platform, which visualizes water performance data to provide a real-time perspective of system health across individual assets, manufacturing sites, or entire organizations.

Demand for microelectronics will continue to grow and change, and the industry's water needs will only get more complex. Manufacturers will need to turn to innovative solutions to respond effectively in a dynamic and increasingly stringent environment.

SIS: *Can you demonstrate or quantify the types of results that come from this approach?*

MG: We can. In one example, we helped a manufacturer of data storage equipment achieve water and energy savings across multiple locations over 15 years. Using 3D TRASAR technology for cooling water, COIL-FLO coil cleaning programs, and a silica removal process, we addressed challenges like high scaling potential and fouling, which led to optimized heat transfer efficiency. Our approach helped the company save an estimated 7 million gallons (26.5 million liters) of water along with 5 million kilowatt hours of energy and 3 thousand tons of CO2 emissions annually, with a total value delivered of more than $450,000 per year.

In another example, we helped NXP Semiconductor, as outlined earlier in this Q and A. It's worth repeating that our solution helped save 7.2 million gallons (27.2 million liters) of water and reduce wastewater discharge by 8.5 million gallons (32.1 million liters) in a single year, delivering a total annual value of nearly $115,000.

SIS: *What steps are you taking to support semiconductor manufacturers who may not yet have a smart water management strategy in place?*

MG: For Nalco Water, supporting the industry is as much a climate responsibility as it is a strategic priority. We recently joined the Semiconductor Climate Consortium founded by SEMI, the global industry association representing electronics manufacturing and design. With a global network of water experts that span more than 40 different markets, we can contribute our expertise and unique perspective to help manufacturers build resilient operations by understanding the interconnected relationship between water and energy. Our collaboration with SEMI will allow us to highlight the importance of thinking globally while acting locally, driving manufacturers to think about enterprise business objectives while keeping site-specific water realities front-of-mind.

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The future of computing runs on silicon-based quantum computing processors

Contrary to popular belief, simply demonstrating quantum advantage is not the ultimate goal of quantum computing. It would be an amazing feat of science and engineering, but it is not sufficient to reach the goal of making quantum computing mainstream. As we approach the era of quantum advantage, demonstrated by the continuously increasing capabilities of quantum computers around the world, the ecosystem may pivot its focus from scientific experiments and demonstrations to prioritizing scalability in the real world.

BY HIMADRI MAJUMDAR, CHIEF EXECUTIVE OFFICER AND CO-FOUNDER OF SEMIQON

THE RACE to quantum supremacy will largely be solved by having scalable, reliable, and affordably manufacturable qubits that can get us to the million-qubit era to solve real-world problems.

Significant progress in the quantum computing communities all around the globe is already happening. After the first successful demonstrations of quantum computers in action, the next step is to integrate quantum computers or processors with high-performance computing (HPC) environments – supercomputers. This integration will demonstrate the benefits of coupling quantum computing with classical computing, which will be followed by further advancement in quantum computing capacity, all leading to the era of scalability in quantum computing.

But we are not there yet. Right now, we are at the crossroads where the global quantum computing ecosystem is primarily engaged in highly costly scientific experiments that focus on building stable qubits within the physical limits of superconductor, ion-trap, neutral atom or photonic technology – or identifying a new path.

The former keeps the status quo while the latter allows us to approach the next stages of quantum computing as difficult yet solvable engineering challenges. Most of the mentioned modalities are also working on the scalability aspects, even though aspects of practical and optimal module sizes, qubit connectivity and interconnect compatibility are still a work in progress.

The first-generation quantum computers have already convincingly demonstrated that harnessing the power of quantum phenomena for computation purposes is possible. The real challenge with further progress, if we can call it an era of practically useful quantum computing – or Quantum Computing 2.0 – is how it can be done in a scalable, sustainable, and affordable way.

Answers to the problems hindering the scalability and widespread adoption of quantum computing can be found much closer to home than most would think. To address the challenges of sustainability, scalability, and affordability, we must put the vast knowledge of semiconductor manufacturing to work to drive the future growth of the quantum computing industry.

Unlocking the full abilities of quantum computers can, at the moment, seem like a distant dream with many challenges, both from a hardware and software perspective. However, the history of technology and computing has taught us that what at one point in time seems almost impossible becomes a daily reality, even mundane, in the future.

Take, for instance, mobile phones. What began as a big, bulky machine has now turned into an incredibly powerful mini computer with mind-boggling computational ability that most of us have with us at all times – even young children. In fact, the astronauts who went to the Moon had far more primitive technology helping them navigate space and safeguard their lives.

So, what needed to happen for that phone that you use to send email, play games, and take photos with, to appear in your hand? It wouldn't exist without the invention of semiconductor (silicon) integrated circuits or IC chips that paved the way for computation as we experience it today on our phones, tablets, smart TVs, and home devices. We certainly wouldn't have AI – once a sci-fi concept that has now turned into a household topic – machine learning, metaverse, or the digitalization of many services, like healthcare and mail, which we take very much for granted.

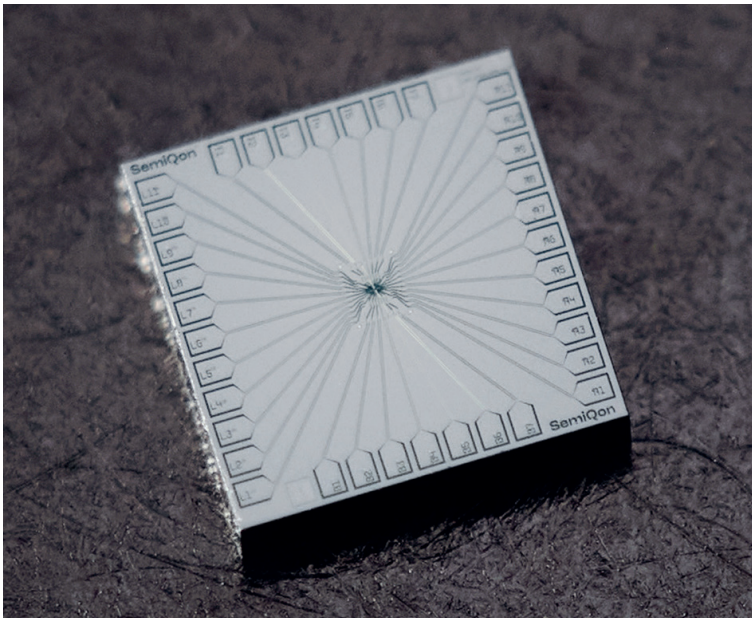
In the 1940s, early computers such as ENIAC took up a large room and a lot of effort to run. With hundreds of wires and, sometimes, vacuum tubes connecting different parts of the machine that had to be manually adjusted, ENIAC weighed about 30 tons and was almost 2.5 meters tall and 30 meters in length. Additionally, it consumed a huge amount of electricity to complete computational tasks – 174 kW to be exact.

Surely in the 21st century, quantum computers are much more sophisticated than this? You'd be tempted to think so, but the facilities a functional quantum computer requires are even more complex than ENIAC. The chandelier, as the quantum computer is often fondly called due to its appearance, has hundreds of wires, and the more qubits it has, the more wires it needs. They require specific, low temperatures to function, several millions in financial investment, and a highly qualified team of quantum physicists and computer scientists to work on them and run them.

What this all means is that like ENIAC, modern quantum computers are simply not scalable and we need to look to the future to a moment when quantum computers finally begin to scale and deliver on their promise to develop vaccines, new materials and solve the practical questions of more far-off ideas like space travel.

But how do we get there and bring the promise of quantum computing down from its ivory tower to a productized level and real-life applications? Instead of relying on non-standard, exotic material-focused approaches to build quantum machines, it is possible to use proven and reliable semiconductor manufacturing technology for building quantum computing processors.

SemiQon is already on the path to demonstrating this. SemiQon builds its hardware using a customized CMOS fabrication process. In it, SemiQon's team monolithically integrates silicon quantum dots and cryogenic CMOS on the same chip to build the full quantum processing unit or QPU. The benefit of this approach is that it allows the fabrication of significantly smaller qubit dimensions than what is typically used in current quantum computers, making it possible to pack more qubits into a smaller footprint. This in turn



reduces the need for large-scale cryogenics or cooling to perform computations at the low temperatures standard quantum computers require.

The requirement of extremely low temperature can also be solved: we aim to operate our silicon-based quantum chips at higher temperatures than the norm – at 1–4 Kelvin – which means that less energy is needed, helping us achieve scalability and cost savings at the same time. Development is ongoing for on-chip cooling solutions that can potentially allow such temperatures to be achieved without significant infrastructure, too.

We shouldn't stop there, however. We envision an era for a convenient plug-and-play processor that will allow integration of the processors into a highly scalable, full-stack quantum computer. We are on our way – we have our own fabrication operation at a national pilot line foundry and our own testing and measurement facility. We have now manufactured our first batch of processors and they are in use with our partners who are conducting different levels of testing around the world.

When it comes to the scalability of quantum computers, traditional quantum computing platforms are certainly ahead of the semiconductor-based platform. However, technological challenges are expected to bring the traditional approach to a plateau. The semiconductor quantum computing platform may have had a slower start, but once the scalability of manufacturing of semiconductor-based quantum processors is demonstrated, the approach can outpace all other platforms.

Scalability depends on several different aspects of the full stack of a quantum computer. This has been highlighted in various market reports and industry trends. The factors that come up often, and should be considered by all modalities are usually identified as fidelity at scale, control over individual qubits at scale, computation speed, multi-qubit networking,

cooling requirements, and manufacturability – as discussed by McKinsey and Global Quantum Intelligence.

Predicting the impact of emerging and novel technologies is always an exercise for the imagination. However, we can undoubtedly expect that the million-qubit era of quantum computing will expand our idea of what is and is not possible. As we discuss the future, it is valuable to note that developments in quantum do not exist in a vacuum, separate from other scientific discoveries. For example, during the last century, humanity witnessed exponential growth in computing power walk – and run – hand in hand with other discoveries, such as space travel and the onset of bringing AI into our daily lives.

New milestones achieved by the quantum computing ecosystem will encourage businesses, research organizations, and governments to venture deeper into the world of quantum computing and to partner with companies that are paving the way to the million-qubit era.

Exploring the opportunities of this previously unattainable computing power should not be left to quantum scientists alone. The quantum ecosystem will greatly benefit from engaging existing industries, potential end-users, and interested policy-makers to help build technologies that solve problems, add value, and are easy to adopt. Realizing the

promise of quantum requires strategic investments in both innovations and the existing semiconductor industry. The good news is that success in scaling up quantum will provide endless opportunities for industry and a competitive edge on the global scale.

(This article is based on the presentation and the paper “Future of Computing: Silicon-based Quantum Computing Processors”).

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SEMI focuses on **skills initiatives**

Skills, sustainability and market numbers are all covered in this SEMI news update

SEMI is inviting key industry stakeholders to participate in a survey designed to assess job skills in highest demand in Europe›s microelectronics industry in 2024. Responses are sought from professionals in various roles including senior engineers, professors, researchers and human resources representatives. The deadline for completing the survey is June 28. Results will be published in September 2024.

Supported by SEMI Europe and organized by DECISION - Études & Conseil, the survey was developed by the European Chips Skills Academy (ECSA), an EU-funded initiative launched by a consortium of 18 partners from 12 countries. The survey builds on the METIS project's in-depth analysis of skills in the European microelectronics sector from 2020 to 2023. The survey will enable the ECSA to evaluate relevant job profiles in the semiconductor industry, including new roles, positions in highest demand, and those with the highest skills shortage. DECISION Études & Conseil will use the survey to monitor hiring trends and craft public policy recommendations.

"The survey is essential to analyzing key workforce trends in Europe's semiconductor sector and giving us strategic insights that will enable the ECSA to update the EU Microelectronics Skills Strategy," said Léo Saint-Martin, Senior Consultant – Associate at DECISION Études & Conseil. "The results will also help us implement and operationalize the EU Pact for Skills."

The ECSA's mission is to help integrate the work of industry, research, and academia to develop innovative training and curricula in order to better meet the skills needs of Europe's chip sector.

"To increase its competitiveness and to achieve the ambitions of the EU Chips Act, the European microelectronics sector must overcome severe skills and talent shortages," said Christopher Frieling, Director of Advocacy and Public Policy at SEMI. "The survey is part of a holistic initiative under the European Chips Skills Academy that aims to involve partners across the entire semiconductor value chain."

The ECSA plans to repeat the survey in 2025, 2026 and 2027 to ensure that public policy recommendations reflect the semiconductor industry's most pressing workforce needs.

New online certification programs

Aiming to help the global semiconductor industry address its talent gap by training and upskilling workers, SEMI says that its SEMI University™ learning platform now offers online course certification programs designed to fast-track semiconductor career development. Tailored to help meet burgeoning industry demand for technicians, the first two SEMI University Semiconductor Certification Programs are designed for new talent seeking rewarding careers in the industry and experienced workers looking to keep their skills current.

"With semiconductor manufacturers investing heavily in new fabs backed in part by government incentives, SEMI projects the global industry will need 1 million new workers worldwide by 2030 to support the chipmaking expansion," said Shari Liss, Executive Director of the SEMI Foundation, which drives the SEMI Workforce Development program. "Technicians are in the highest demand, accounting for roughly 40% of the semiconductor workforce worldwide. The SEMI University Certification Program will help meet the industry's pressing need for a diverse range of training and certification programs to close the talent gap."

"SEMI University's new Semiconductor Certification Programs give the industry a fast way to train new talent while enabling current workers to keep pace with its expanding skills requirements," said SEMI University Director Naresh Naik. "The first two certification programs address critical technician roles. We look forward to adding new certifications to support the industry's growing workforce needs and career development for our learners."

The SEMI University Semiconductor Certification Programs include:

- **The Semiconductor Technician Certification** equips new semiconductor industry workers with the skills necessary to excel in chipmanufacturing. The certification program provides comprehensive training in the semiconductor process and on-the-job tasks. Courses cover the function of semiconductors and their manufacture, how electrical circuits work and the physical laws that apply to electrical current, as well as the various applications of electrical testing equipment.
- **The Pneumatics/Hydraulics Technician Certification** covers the use of vacuum technology in pneumatic systems and hydraulics theory. Courses address the properties of gases and vacuums, how various vacuum types are generated, and hydraulic systems and their components including actuators. The curriculum also compares hydraulic and pneumatic systems.

Keeping tabs on corporate climate disclosures

SEMI has released the report A Rising Tide: Building a Climate-Resilient Semiconductor Value Chain that spotlights the maturity of the semiconductor value chain as it strives toward greater climate resilience and develops climate risk mitigation strategies. Led by the SEMI Sustainability Initiative Environmental Risk Mitigation and Reporting (ERMR) working group, the study identifies strengths, gaps and challenges faced by the industry in implementing recommendations of the Taskforce on Climate-related Financial Disclosures (TCFD). The report also offers recommendations on industry best practices to enhance climate disclosure maturity. Download the report.

The report leveraged Nasdaq Sustainable Lens™, an AI-powered ESG intelligence platform, to analyze and assess the maturity level of each segment of the semiconductor value chain based on publicly available sustainability and climate information of 100 leading semiconductor companies against TCFD recommendations. Nasdaq Sustainable Lens™ reviewed over 2,200 corporate annual financial reports, sustainability reports, low-carbon transition and climate action plans and other sustainability and climate information released between 2021 and 2023. The platform uncovered five key takeaways: Maturity of semiconductor industry-level climate disclosures are in the Established phase as defined by Nasdaq. The semiconductor companies included in the assessment showed 40% higher TCFD alignment than the market average, represented by over 9,000 global companies across all industries beyond semiconductors.

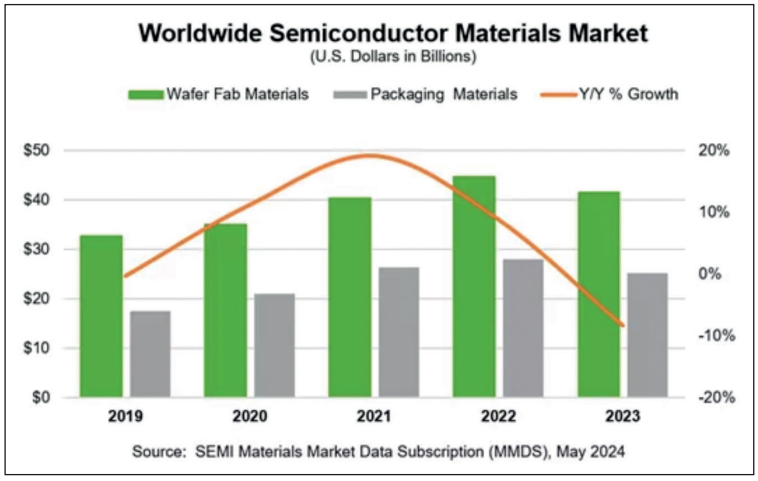
"With semiconductor manufacturers investing heavily in new fabs backed in part by government incentives, SEMI projects the global industry will need 1 million new workers worldwide by 2030 to support the chipmaking expansion"

Corporate climate reporting varies by semiconductor value chain segment largely due to different stakeholder expectations, jurisdiction-level reporting requirements, the level of resources dedicated to corporate climate work, as well as board- and executive-level engagement in climate initiatives. Companies prioritize near-term climate targets, though only some have set long-term net zero goals. On average, value chain segments demonstrated the most comprehensive TCFD alignment with the Metrics & Targets pillar, particularly as it relates to near-term greenhouse gas (GHG) emissions reduction targets.

Addressing organizational resilience to climate change appears to be the biggest industry-level challenge. The most underreported categories included climate scenario analysis, quantitative physical and transition climate risk assessments, and setting an internal carbon price. This indicates that the core question of how a company's business strategy will perform under various climate scenarios remains a major gap across all semiconductor value chain segments.

Ensuring climate resilience of the value chain is a business imperative for semiconductor companies. Industry-level recognition of the vulnerability of the semiconductor value chain to existing and potential climate-related risks and proactively building a path towards climate resilience are crucial for long-term business continuity.

"Our study aims to raise awareness of climate risk as a key business risk and demonstrate an important role that climate resilience plays in ensuring business continuity and long-term resilience of the semiconductor value chain," said Alua Suleimenova, Senior Sustainability Program Manager at Marvell and leader of the ERMR working group. "This analysis will inform business leaders' decisions around measuring and reporting on corporate climate action. Further, this study can help SEMI members enhance transparency of their climate disclosures in alignment with emerging reporting requirements, including the TCFD recommendations, which are now housed within the International Sustainability Standards Board (ISSB)."



"The analysis made possible by Nasdaq Sustainable Lens™ is a key step forward in understanding and improving sustainability risk assessment and reporting across the semiconductor value chain," said Dr. Mousumi Bhat, Vice President of Global Sustainability Programs at SEMI. "Marvell's leadership and the companies that provided case studies were crucial to delivering these important insights."

Mixed market messages

The global semiconductor manufacturing industry in the first quarter of 2024 showed signs of improvement with an uptick in electronic sales, stabilizing inventories and an increase in installed wafer fab capacity, SEMI announced in its Q1 2024 publication of the Semiconductor Manufacturing Monitor (SMM) Report, prepared in partnership with TechInsights. Stronger industry growth is expected in the second half of the year.

In Q1 2024, electronic sales rose 1% year-over-year (YoY), with Q2 2024 forecast to register a 5% YoY increase. IC sales posted robust 22% YoY growth in Q1 2024 and are expected to surge 21% in Q2 2024 as shipments of high-performance computing (HPC) chips increase and memory pricing continues to improve. IC inventory levels stabilized in Q1 2024 and are expected to improve this quarter.

Installed wafer fab capacity continues to increase and is projected to exceed 40 million wafers per quarter (in 300mm wafer equivalent), rising 1.2% in Q1 2024 with an expected 1.4% uptick in Q2 2024. China continues to log the highest capacity growth among all regions. However, fab utilization rates, particularly for mature nodes, remain a concern with little signs of recovery expected in the first half of 2024. Memory utilization rates were lower than expected in Q1 2024 due to disciplined supply control.

In line with fab utilization trends, semiconductor capital expenditures remain conservative. After falling 17% YoY in Q4 2023, capital expenditures continued to pull back 11% in Q1 2024 before eking out an expected 0.7% gain in Q2 2024. Sequentially in Q2 2024, the trend is turning positive with an expected 8% increase in memory-related capital expenditures as they see slightly stronger growth than non-memory segments.

"Demand in some semiconductor segments is recovering, but the pace of recovery is uneven," said Clark Tseng, Senior Director of Market Intelligence at SEMI. "AI chips and high-bandwidth memory are currently among devices in the highest demand,

Worldwide silicon wafer shipments decreased 5.4% quarter-over-quarter to 2,834 million square inches in the first quarter of 2024, a 13.2% drop from the 3,265 million square inches recorded during the same quarter last year, the SEMI Silicon Manufacturers Group (SMG) reported in its quarterly analysis of the silicon wafer industry

leading to increased investment and capacity expansion in these areas. However, the impact of AI chips on IC shipment growth remains limited due to their reliance on a small number of key suppliers." "Semiconductor demand in the first half of 2024 is mixed, with memory and logic rebounding due to surging generative AI demand," said Boris Metodiev, Director of Market Analysis at TechInsights.

"However, analog, discrete, and optoelectronics have experienced a slight correction due to the slow recovery of the consumer market coupled with a pullback in demand from the automotive and industrial markets."

"A full-on recovery is likely to take hold in the second half of the year with the projected boost in consumer demand by AI's expansion to the edge," Metodiev said. "Additionally, the automotive and industrial markets are expected to return to growth in the latter part of the year as interest rates fall – providing consumers more purchasing power – and inventory declines."

Sources: SEMI (www.semi.org) and TechInsights (www.techinsights.com), May 2024

Global semiconductor materials market revenue in 2023 contracted 8.2% to $66.7 billion from the market record of $72.7 billion set in 2022, SEMI has reported in its Materials Market Data Subscription (MMDS).

Wafer fabrication materials revenue declined 7.0% to $41.5 billion in 2023, while packaging materials revenue fell 10.1% to $25.2 billion last year. The silicon, photoresist ancillaries, wet chemicals, and chemical mechanical planarization (CMP) segments logged the biggest contractions in the wafer fabrication materials market. The organic substrates segment accounted for much of the packaging materials market contraction.

Demand for semiconductors softened in 2023 as the industry worked to reduce excess inventory, leading to lower fab utilization rates and, consequently, a drop in materials consumption.

Taiwan, at $19.2 billion in revenue, was the world's largest consumer of semiconductor materials for the 14th consecutive year. China, at $13.1 billion in revenue, continued to register year-over-year growth, ranking second in 2023, while Korea remained the third largest consumer with $10.6 billion in revenue. All regions except China posted high single- or double-digit declines in 2023.

Note: Summed subtotals may not equal the total due to rounding.*Rest of the World includes Singapore, Malaysia, the Philippines, other areas of Southeast Asia, and smaller global markets.*

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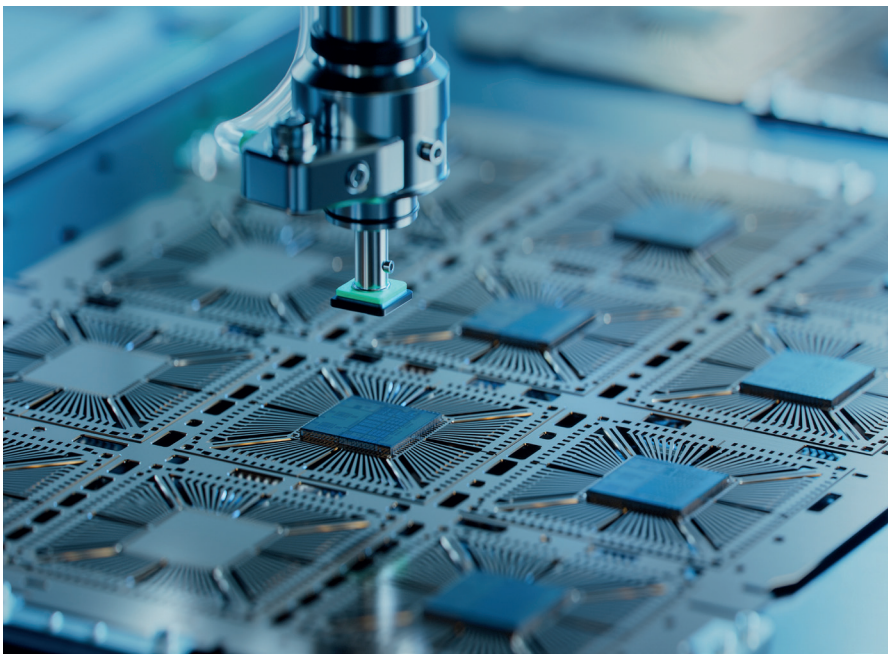
"The continuing decline in IC fab utilisation and inventory adjustment led to negative growth across all wafer sizes in Q1 2024, with polished wafer shipments falling slightly more year-over-year than EPI wafer shipments," said Lee Chungwei, Chairman of SEMI SMG and Vice President and Chief Auditor at GlobalWafers. "Notably, utilization by some fabs



bottomed out in Q4 2023 as growing AI adoption fueled rising demand for advanced node logic products and memory for data centers."

Silicon area shipment trends – Semiconductor applications only

Senator saluted

The SEMI North America Advisory Board has presented the annual SEMI Americas Government Leadership Award to U.S. Senate Majority Leader Charles (Chuck) Schumer in recognition of his extraordinary support of the U.S. semiconductor industry. SEMI Americas President Joe Stockunas and TEL Vice President Ben Rathsack presented Senator Schumer with the award this week at the U.S. Capitol Building.

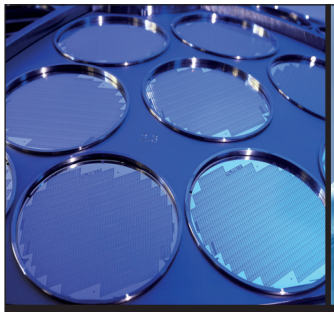
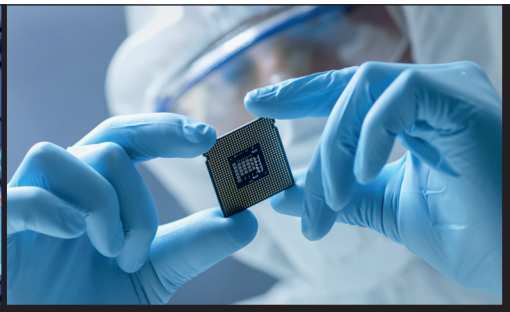
The SEMI North America Advisory Board selects SEMI Americas Government Leadership Award honorees based on their impact on policies and incentives to bolster semiconductor design and manufacturing in the Americas region and advance the growth of the global industry.

"Senator Schumer is the embodiment of a semiconductor industry champion," Stockunas said. "His visionary leadership was instrumental in the passage of the CHIPS and Science Act, paving the way for the creation of thousands of jobs and the infusion of billions of dollars into the U.S. chip ecosystem to help strengthen the resilience of the global semiconductor supply chain. The funding awards include recent grants for GlobalFoundries and Micron facilities in New York that will support research and development at the Albany NanoTech Complex critical to national security."

"Senator Schumer's steadfast support, from the drafting of the CHIPS Act to its implementation, continues to bring tangible benefits to communities, businesses and the U.S. as a whole, contributing to its national and economic security," Stockunas said. "We commend Senator Schumer for his outstanding contributions and tireless efforts to help ensure the semiconductor industry reaches its full potential."

The North America Advisory Board provides guidance on SEMI Americas programs designed to advance their business interests and address significant challenges in the electronics manufacturing and design supply chain.

The Board's mission is to strengthen the financial, market, and technology performance of SEMI member companies operating in North America.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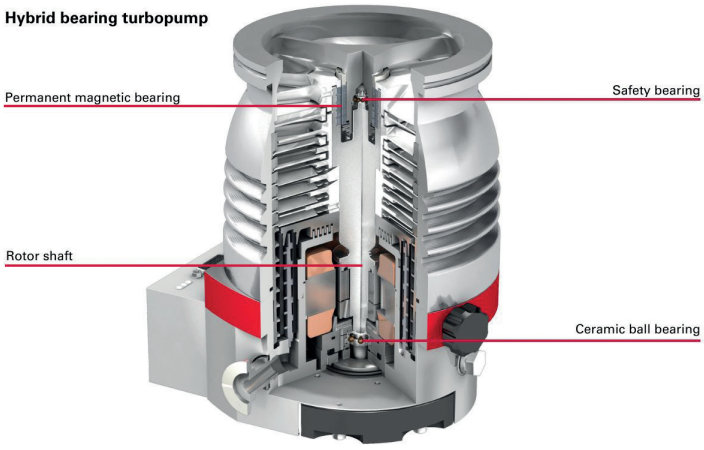
Problem

Today, the process of ion implantation is widely used for fabricating modern micro devices. This process requires high vacuum which can only be provided with high performance turbomolecular vacuum pumps. In the source chamber of the ion implantation tool several process gases will be introduced which causes the accumulation of many byproducts inside the turbopump. Due to the byproduct accumulation, the life expectancy of the turbopump can be negatively affected.



Pumping Speed Class	Implant Standard	Implant Heated
1200 l/s	HiPace 1200 I	HiPace 1200 IT
1500 l/s	HiPace 1500 I	HiPace 1500 IT
1800 l/s	HiPace 1800 I	HiPace 1800 IT
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HiPace-I series can be used for the source and beamline chambers of the implantation tool. For use with the source chamber, a heated pump version is recommended.

Platforms

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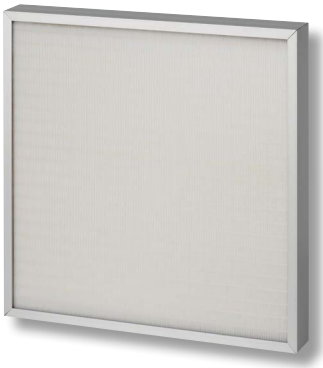

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Testing microchips for AI applications:
Unveiling the challenges

Microchips are the backbone of artificial intelligence (AI) applications, powering everything from self-driving cars to virtual assistants. With the growing complexity of AI algorithms and the need for faster processing speeds, testing these microchips has become a major challenge for semiconductor companies.

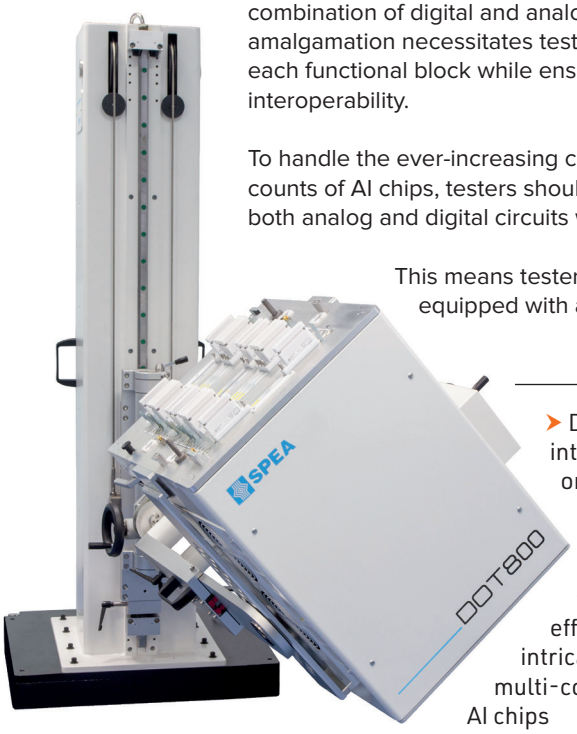
AI CHIPS are designed to process large amounts of data and make decisions in real-time, making them crucial for the success of final applications. Without proper testing, these chips may not function as intended, leading to errors and potentially dangerous consequences. This is especially true for applications that require real-time decision making, where any errors or malfunctions can have serious consequences.

In this article, we will explore the challenges in testing microchips for AI applications and the evolving capabilities required of mixed signal testers for robust AI microchip validation.

The challenge of testing complex AI chip designs
One of the main challenges in testing microchips for AI applications is the complexity of the algorithms they are designed to support. Modern AI chips often integrate diverse processing elements like CPUs, GPUs, specialized AI cores, and rely on a combination of digital and analog signals. This amalgamation necessitates tests that cater to each functional block while ensuring seamless interoperability.

To handle the ever-increasing complexity and pin counts of AI chips, testers should excel at testing both analog and digital circuits with high precision.

This means testers should be equipped with a variety of features and capabilities, including high-speed digital and analog testing, low-noise signal generation and analysis, high-speed digital pattern generation, and advanced data processing.



➤ Distributed intelligence based on a multi-core architecture makes new-generation mixed signal testers able to effectively test the intricate multi-die and multi-core architecture of AI chips

To keep pace with the evolving architecture of AI chips, testers need to boast increasingly sophisticated capabilities. As chip designers leverage technologies like 3D-stacking to enlarge bandwidth and facilitate the transfer of massive datasets in record time, new-generation testers must adapt accordingly. This necessitates a large quantity of high-speed digital channels, capable of handling frequencies ranging from 400MHz to tens of GHz. Additionally, large memory depth is crucial for accommodating the extensive test data these complex chips require.

The intricate multi-die/multi-core architecture of AI chips presents another challenge. Neural processing units (NPUs), for instance, often incorporate multiple cores. To effectively test these chips, testers require a new level of intelligence. Distributed intelligence based on a multi-core architecture enables the tester to perform multiple, simultaneous computations in an asynchronous manner. Imagine a tester with its instruments and components functioning as independent, intelligent modules capable of launching test patterns autonomously. This distributed processing power significantly enhances test efficiency and streamlines the validation process for complex AI chips, enabling the tester to mimic intricate real-world operating conditions.

The need for speed and efficiency

Another challenge in testing microchips for AI applications is the need for speed and efficiency. As AI applications become more prevalent, the demand for faster processing speeds and lower power consumption is increasing.

This puts pressure on semiconductor companies to develop microchips that can meet these demands while still being thoroughly tested. Traditional testing equipment and methods can be time-consuming

and may not be able to keep up with the pace of development, leading to delays in bringing products to market. To keep up with efficiency, testers should be capable of high multi-site capabilities, and should incorporate specific features aimed at maximizing the test execution speed. Distributed intelligence is a game-changer: multiple CPUs embedded within the tester and its instruments, all working simultaneously, allow the tester to run multiple test processes concurrently, significantly accelerating test execution.

Furthermore, multi-time domain capability is essential for maximizing test speed. This feature enables the tester to run digital signals with different time domains at the same time. This translates to testing concurrently the various blocks within the chip under test, decreasing dramatically the overall test-time.

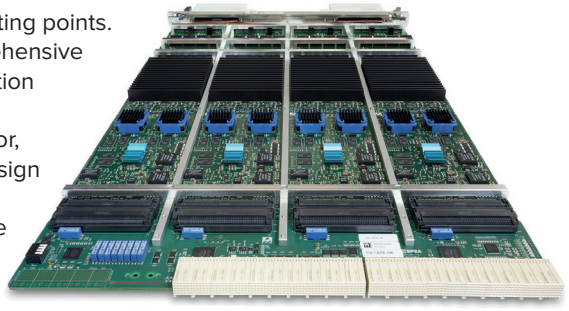
Other key features that contribute to test time optimization include embedded Digital Signal Processing (DSP) units on both analog and digital instruments. These on-board DSP units perform data de-coding and computations directly on the instruments, eliminating the need for data transfer back and forth to a central processing unit, which can slow down the testing process. Additionally, a protocol-aware instrument architecture is crucial. By understanding the communication protocols used by the DUT, the tester can streamline pattern complexity and optimize communication efficiency, further accelerating test execution.

Monitoring the chip power consumption

A hallmark of AI chips is their focus on power efficiency. This makes power management expertise one of the key characteristics that a new-generation mixed signal tester for AI microchips must possess. These chips often boast high-density layouts, integrating diverse processing elements with their own specific power requirements. This translates to a multitude of power domains, each requiring meticulous verification.

The tester needs to be adept at precisely controlling and monitoring power delivery across these domains, not just at the system level, but also for individual sections of the chip. This granular power management ensures that the chip operates under realistic conditions, allowing for accurate power consumption verification and the detection of power-related defects that might otherwise go unnoticed.

Furthermore, the immense processing power required by AI chips makes them inherently energy-consuming. This high-power draw translates to significant energy costs and thermal challenges for data centers, causing headaches for IT managers. To address this concern, mixed-signal testers must be equipped with a robust suite of power supplies capable of accurately stimulating the AI chips under test at various operating points. This enables comprehensive profiling and verification of the chip's power consumption behavior, ensuring it meets design specifications and contributes to a more energy-efficient overall system. By closely mirroring real-world power conditions, testers can help mitigate the data center power consumption woes associated with AI deployments. Additionally, the dynamic nature of AI chip operation necessitates new generation testers with a suitable number of high-current analog channels. Unlike traditional chips with steady power demands, AI chips exhibit fluctuating power consumption as workloads change.



The tester's analog channels need the capacity to deliver these high currents while maintaining precise control. Fast instrumentation is equally important for effectively modulating the current supplied in response to the chip's real-time requirements. This ensures that the chip receives the exact amount of power it needs at any given moment, mimicking real-world operating conditions and enabling comprehensive power integrity testing.

Conclusion

Testing microchips for AI applications is a crucial step in the development process, but it comes with its own set of challenges. The complexity of AI algorithms, the need for speed and efficiency, and the importance of power consumption monitoring all make testing these microchips a difficult task. Investing in the right test equipment is essential to maximize AI chip performance and stay ahead of the competition in this rapidly advancing field. The new generation of mixed signal testers, as the SPEA DOT800, includes features like:

- High-speed digital and analog testing capabilities
- Large memory depth
- Distributed intelligence on a multi-core architecture
- Multi-time domain operation
- DSP units on analog and digital instruments
- Protocol-aware instrumentation
- A robust suite of power supplies

These features enable testers to mimic real-world operating conditions, perform comprehensive power integrity testing, and streamline test execution. By embracing these advancements, semiconductor companies can ensure the robust validation of AI microchips, paving the way for the next generation of groundbreaking AI applications.

The future of AI microchip testing is bright, characterized by continuous innovation and a symbiotic relationship between cutting-edge chip design and powerful testing methodologies.

➤ To handle the ever-increasing complexity of AI chips, tester instrumentation should include high-speed digital and analog capabilities, low-noise signal generation and analysis, high-speed digital pattern generation, and advanced data processing.

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For more information contact:

Jackie Cannon **T:** 01923 690205 **E:** jackie@angelwebinar.co.uk **W:** www.angelwebinar.co.uk
Angel Business Communications Ltd, 6 Bow Court, Fletchworth Gate, Burnsall Road, Coventry, CV5 6SP. UK
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