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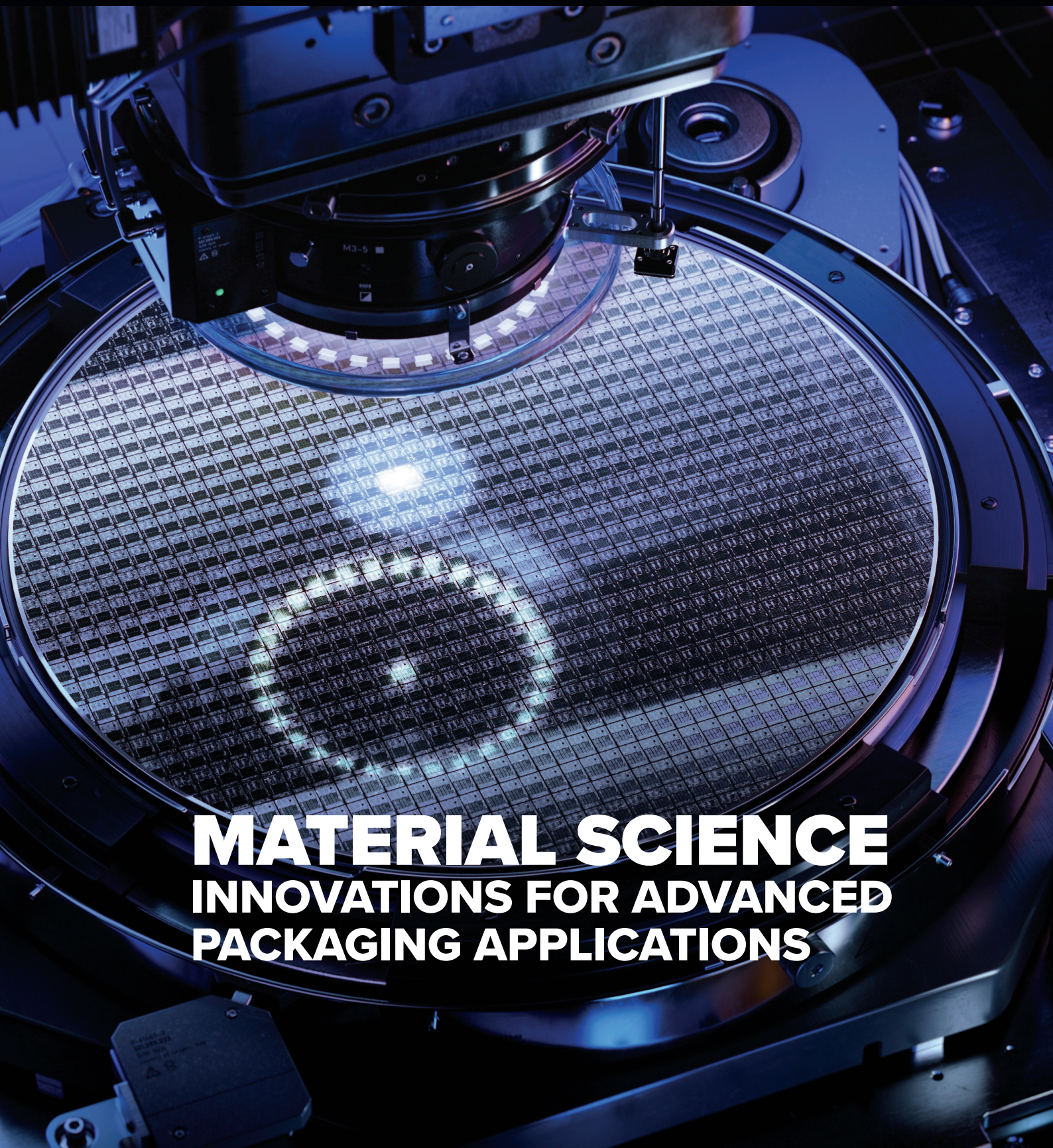

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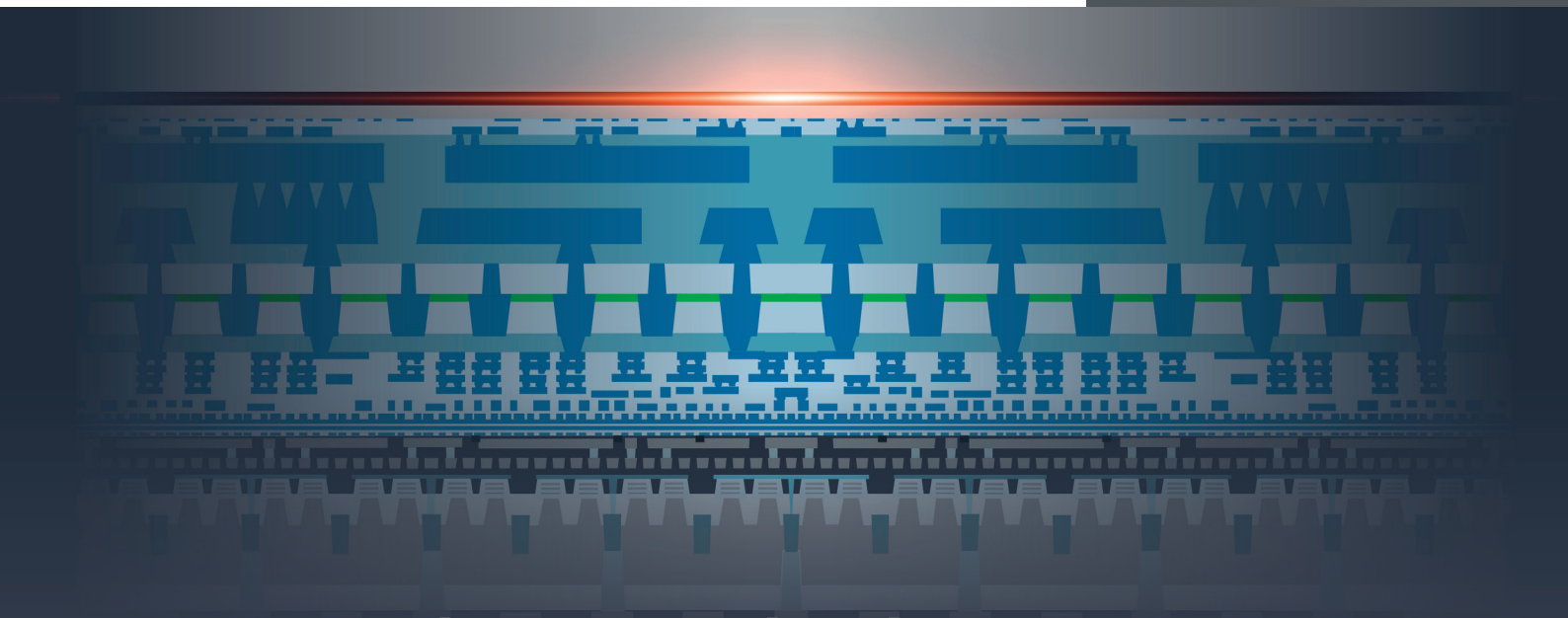

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VIEWPOINT

BY PHIL ALSOP
EDITOR

The cost of doing something versus the cost of doing nothing

The news pages in this issue of Silicon Semiconductor neatly encapsulate the ongoing dilemma facing individual countries, wider regions and the semiconductor companies themselves when it comes to how best to respond to the significant challenges facing the sector – with geopolitics top of the agenda. Reshoring/onshoring may well be an attractive proposition in terms of taking back control, but the cost of such a policy is colossal – whatever the mix of government and private company investment. Additionally, policies which are intended to promote the idea of local supply chain security might just backfire, as in the story on Page 8 – 'US export controls on AI chips boost domestic innovation in China'. And it is China that seems to dominate the semiconductor landscape at the current time. The Yole report on Page 9 outlines the likely, significant increase in Chinese foundries over the next few years.

Additionally, it would seem that Chinese foundries' ability to manufacture semiconductors at a low price level which others cannot match is having a significant impact on strategic decisions being taken by other players.
More generally, the simple presence of China in the semiconductor market is proving a catalyst for many new initiatives within the industry, which one could argue may or may not have happened in any case. So, China may be seen as a threat by many, but it is also focusing the minds of the competition.

The news on Page 10 – (UK) TechWorks and Canadian Semiconductor Council sign MoU – is a case in point. Would such collaboration have happened pre the current geopolitical uncertainties? And, as on Page 12, would Qatar now be interested in the semiconductor space if the status quo of a few years ago remained today?

What remains to be seen is just what the various semiconductor manufacturing countries and regions, mature and emerging, do want to do and what they don't want to do in terms of the overall supply chain. And, importantly, once they have made a plan, how can it be implemented effectively?

As the article on Page 46 makes clear, delivering on a strategy is not easy.

'It is very unlikely that the EU will meet its target of a 20 % share of the global market for microchips by 2030, according to a new report by the European Court of Auditors. While the 2022 EU Chips Act has brought new momentum to the European microchip sector, the investments driven by it are unlikely to significantly enhance the EU's position in the field'.

Intriguingly, the report points out that, whatever the EU does itself (and this applies elsewhere to other governments), it is largely at the 'mercy' of the semiconductor companies who, ultimately, will make the crucial investment decisions. Yes, of course, those in charge can offer various incentives (carrots and sticks!), but they cannot force private companies to invest if they do not wish to.

And that perhaps is why China is such a looming presence at the present time, as the link between its government and its semiconductor industry is incredibly close.

Looking ahead, it will be fascinating to see what transpires - to see who wants to play at the very top table, and who wants to identify and occupy smaller, more specialised parts of the semiconductor market.

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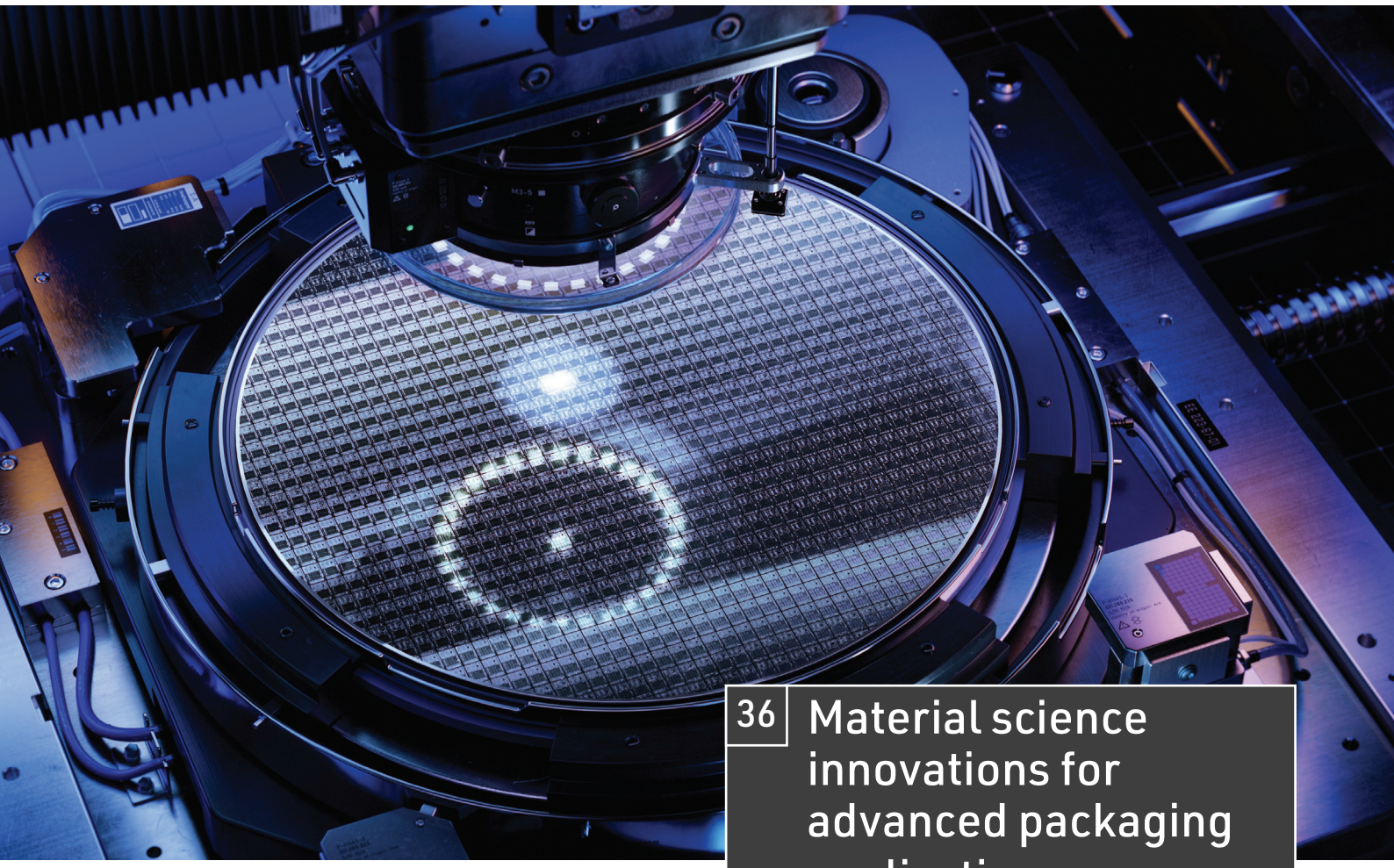

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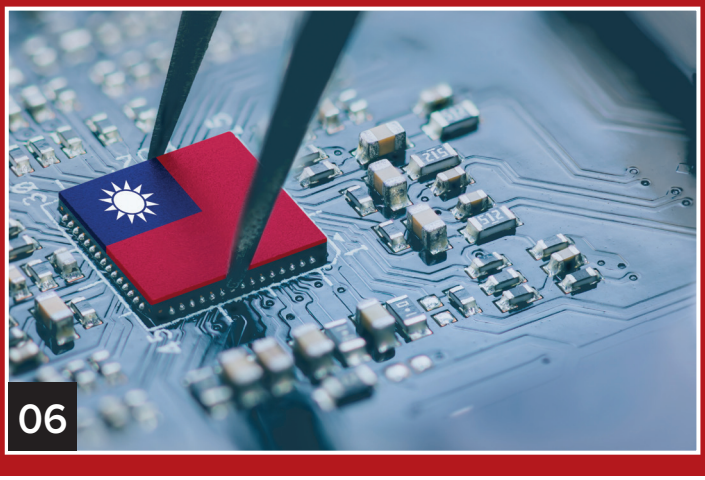

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Strategic silicon: how geopolitics is redirecting semiconductor investment

Geopolitical tensions are redirecting global investments in advanced semiconductor technologies, reshaping the semiconductor supply chain in pursuit of technological sovereignty, according to IDTechEx

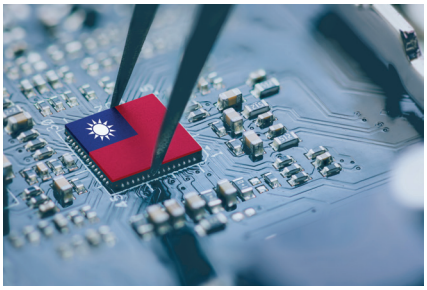
THE VAST MAJORITY of the world's most advanced silicon chips are manufactured in Taiwan by a single company - Taiwan Semiconductor Manufacturing Company (TSMC). These chips power everything from data centers to smartphones.

However, Taiwan's central role has become a geopolitical vulnerability. Mounting tension between China and Taiwan, paired with the growing strategic value of advanced semiconductors, has raised global concerns.

In response, governments and corporations have launched a sweeping wave of reshoring efforts. In the U.S. alone, over $480 billion in semiconductor-related investments were announced between 2024 and 2025. Major contributors include Texas Instruments ($60B), Micron ($200B), GlobalFoundries ($16B), TSMC ($165B), and Samsung ($40B), many supported by The Chips Act subsidies. These projects are strategically positioned to develop capabilities across advanced silicon nodes, high-bandwidth memory (HBM), advanced semiconductor packaging, and silicon photonics, all critical to the AI era.

Across Europe, the EU Chips Act is catalyzing local semiconductor ecosystems. TSMC, alongside Bosch, Infineon, and NXP, is co-investing in a 22/28 nm fab in Dresden, backed by the German government. Other key developments include Infineon's €3.5B MEGAFAB project and Silicon Box's €3.2B chiplet facility in Italy. These underscore Europe's ambition to reestablish sovereign manufacturing capacity.

In Japan, TSMC's Kumamoto fab (via JASM) has begun production, and a



second, more advanced fab is under construction. The government has pledged over $5.4B to Rapidus, aiming for 2 nm pilot production by 2027. South Korea continues expanding its HBM and logic production with strong state backing.

Meanwhile, Taiwan is reinforcing its leadership in advanced semiconductor technologies through strategic regulation. In March 2025, the National Development Council confirmed that TSMC's overseas fabs are subject to the "N-1" rule, which prohibits companies from transferring their most advanced process nodes abroad. Officials outlined three principles: the latest technology must stay in Taiwan, critical IP must not leave, and national security takes priority, ensuring Taiwan remains the hub of cutting-edge chipmaking.

TSMC continues to invest heavily at home, building seven new facilities in 2025, including six fabs and one advanced packaging plant in Taiwan. 2 nm production will ramp in the second half of 2025, and 3 nm output is set to grow 60% this year. The company projects AI-related wafer shipments will be 12× higher than in 2021, with large-die shipments up 8×.

While these investments may enhance national capabilities, they also fundamentally reconfigure the global semiconductor supply chain. Today's semiconductor ecosystem, particularly for AI chips, is deeply rooted in East Asia, with Taiwan at the center, not only for wafer fabrication but also for advanced packaging, testing, and final assembly. Manufacturing a chip with an advanced node is only the first step; without co-locating downstream processes, it makes little economic sense to fabricate in the U.S. only to ship wafers back to Taiwan for packaging.

Building a fab that manufactures advanced nodes already costs a fortune (Building a 2 nm wafer fab with high-volume output requires an enormous investment, often approaching tens of billions of dollars.), but replicating the entire supporting ecosystem adds substantially more. TSMC's Arizona project illustrates this complexity: to make it operate effectively, TSMC had to rebuild much of its supply chain from Taiwan to the US.

This kind of transition inevitably drives up the cost of advanced chips, and only wealthy nations with strong political and financial backing can afford to play. While the U.S. Chips Act has catalyzed onshoring, the road ahead remains long and difficult. Key challenges include:

- Skilled labor shortages, exacerbated by anti-immigration policies
- Capital intensity, especially amid worsening global economic conditions
- Geopolitical friction, including Taiwan's "N-1" regulation, which restricts export of the most advanced nodes and technologies
- Supply chain immaturity and fragility, as many upstream and downstream partners remain concentrated in Asia.
- Policy uncertainty, as government subsidies and permitting shifts, can delay or disrupt projects, especially over multi-year timelines.

High bandwidth memory market is projected to surpass $25.9 bn by 2034

The High Bandwidth Memory Market is set to grow from its current market value of more than $2.3 billion to over $25.9 billion by 2034; as reported in the latest study by Global Market Insights, Inc.

THE GLOBAL SHIFT toward data-centric technologies is reshaping the landscape of memory solutions, with high bandwidth memory emerging as a critical enabler for faster data processing and energy-efficient computing. As organizations across various sectors race to adopt next-generation technologies, the demand for high-speed, low-latency memory has seen a notable surge.

The growing influence of artificial intelligence (AI), machine learning (ML), advanced driver-assistance systems (ADAS), and 5G networks continues to fuel demand for powerful memory technologies. Enterprises are leaning heavily on HBM to support big data, high-resolution imaging, real-time analytics, and deep learning workloads. With digital transformation accelerating in sectors like automotive, healthcare, financial services, and media, HBM solutions are rapidly becoming foundational to the development of smarter, faster, and more connected systems. Companies worldwide are responding by investing in cutting-edge innovations and expanding manufacturing capabilities to stay competitive in this rapidly evolving space.

The market is segmented by technology node into below 10nm, 10nm to 20nm, and above 20nm. The 10nm to 20nm category accounted for USD 1 billion in 2024 and is projected to grow at a CAGR of 26.7% between 2025 and 2034. This node has proven ideal for applications requiring balanced performance and cost-efficiency, such as automotive electronics, IoT devices, and mid-range consumer products. Its scalability, coupled with high-yield production and reliable thermal management, continues to make it a go-to option for developers aiming to optimize performance without inflating manufacturing costs.

Based on application, the high bandwidth memory market is categorized into GPUs, CPUs, FPGAs, ASICs, AI, ML, HPC, networking, and

data centers. The GPU segment captured a 21.3% share in 2024, supported by soaring demand in professional and immersive gaming ecosystems.

As ultra-high-definition graphics, real-time rendering, and extended reality environments become mainstream, graphics processing units are integrating advanced HBM technologies such as HBM3E to meet rising bandwidth needs. This trend is particularly prominent in the gaming and animation sectors, where rapid refresh rates and responsive user experiences are essential.

Semiconductor market sustains momentum amidst evolving global dynamics

THIS FIGURE represents a considerable 19.8% increase compared to May 2024, when sales stood at $49.2 billion, and a 3.5% uplift from April 2025. This sustained upward trajectory offers critical insights for procurement pipelines and supply-chain agility within the electronics sector, particularly as defence industries globally seek advanced technological integration.

The consistent growth in chip sales indicates a robust underlying demand, which is a key consideration for strategic sourcing. According to John Neuffer, president and CEO of the Semiconductor Industry Association (SIA), “Worldwide chip sales remained strong in May, slightly exceeding April’s total and significantly outpacing last year’s performance.” This sustained performance signals a stable, if not expanding, supply landscape for fundamental electronic components.

Regional sales figures underscore a shifting global dynamic. Year-on-year expansion was observed across all major markets. The Americas led with a substantial 45.2% rise, followed by Asia Pacific/All Other regions at 30.5%, China at 20.5%, Japan at 4.5%, and Europe with a 4.1% increase.

Month-on-month growth also saw Asia Pacific/All Other (6.0%), China (5.4%), and Europe (4.0%) taking the lead, while the Americas and Japan registered more modest increases of 0.5% and 0.2% respectively. This regional disparity necessitates careful consideration for global procurement strategies, particularly concerning lead times and potential geopolitical influences on supply chains.

US export controls on AI chips boost domestic innovation in China

The discussion around advanced chips for artificial intelligence, driven by billions in investment, dreams of artificial general intelligence, and marred by political concerns over security, has entered a stage of intense competition between nations, says IDTechEx.

NVIDIA achieved revenues of over US$80 billion from data center GPUs alone in 2024; however, with significant stock going to nations outside of the US, the US government has mandated stringent measures to reduce this flow, citing national security concerns as the reason. China has been particularly affected by this change, with limited access to not only GPUs but also advanced tools required for manufacturing advanced semiconductor technologies.

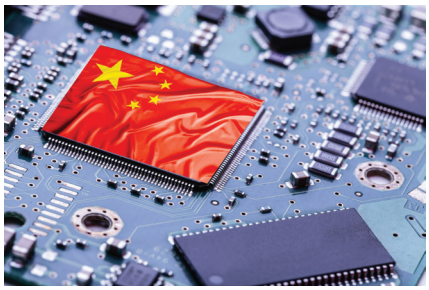
Whilst these measures create roadblocks for companies across the whole supply chain, they also create the necessity for innovation, with Chinese players demonstrating this already. IDTechEx explores innovations from companies across the AI chips landscape within its semiconductors, computing, and AI portfolio, including a full analysis of the regulations landscape and analysis of international AI chip players, and technologies in the recently released "AI Chips for Data Centers and Cloud 2025-2035: Technologies, Market, Forecasts."

AI chips for data centers, rely on international collaboration in design, manufacturing, and distribution, however the US has cornered China by restricting this collaboration. These AI processors see increasing demand in data centers, but this comes with high energy consumption and capital costs. Source: IDTechEx

Artificial Intelligence (AI) is continuously being adopted into workflows by enterprise and consumers alike, presented as know-it-all generative AI language bots and smart AI agents; however, this is only the final layer of what AI really is. Behind the screen, and on the other side of the internet, are tens of gigawatts of data centers' capacity, with millions of GPUs and other AI accelerators populating their racks. AI hardware sees governments and hyperscalers pouring hundreds of billions of dollars into building out AI data centers. These continue to be developed to facilitate the growing size of AI models required to deliver the likes of ChatGPT, Claude, Gemini, and other large AI models.

Demand has outstripped the famous Moore's Law scaling, with floating point operations per second (FLOPS) increasing at a rate of four and a half times per year since 2010. For perspective, Llama 3.1-405B, a leading AI model from Meta, requires 3.8x1025 FLOPS of training compute, which in turn requires 16,384 NVIDIA H100 SXM5 80GB nodes. This itself takes 2,142 hours with a power draw of 25,280 W to train, which is equivalent to powering 2,085 US households for a year, when running at 40.42% hardware utilization. This demand for computing is only expected to continue growing, with governments striving to lead in autonomous infrastructure, drug discovery, and military capabilities. IDTechEx forecasts that the AI Chips market will reach US$453 billion by 2030 at a CAGR of 14% between 2025 and 2030.

The US puts pressure on the global semiconductor supply chain to limit China and other arms-embargoed countries' access to advanced chips Despite US-based fabless chip designers, NVIDIA and AMD, leading in the revenues from AI chip sales, the supply chain is firmly international. Semiconductor manufacture has been dominated by production in Taiwan, with TSMC leading the production of the majority of advanced AI chips. Advanced memory technologies providers have been split between the US and South Korea, with high bandwidth memory (HBM) designed



by SK Hynix, Samsung, and Micron Technology. Lithography equipment, specifically extreme ultra-violet (EUV lithography), is firmly dominated by the Netherlands' ASML. However, the US has imposed various strategies to limit China's ability to not only access advanced chips, but also equipment.

The US's limitations on China's access to advanced chips are by no means a new story, but it is a tale that gets more rigid year on year. October 2022, during Biden's presidency, saw the Bureau of Industry and Security (BIS) introduce controls restricting China's ability to obtain advanced computing chips, develop supercomputers, and manufacture advanced semiconductors, on the grounds of preventing these technologies from being used for military applications and human rights abuses. The controls were updated to enhance effectiveness and close loopholes in October 2023, which were formed of stricter limitations destined for countries of concern, particularly China.

In December 2024, the BIS further strengthened these controls by adding 24 types of semiconductor manufacturing equipment and three types of software tools to the restricted list. Additionally, 140 Chinese entities were added to the Entity List, requiring special licenses for US businesses to supply them. This move creates a chokehold on Chinese manufacturers to produce advanced chips for AI.

Semiconductor foundry landscape to transform by 2030

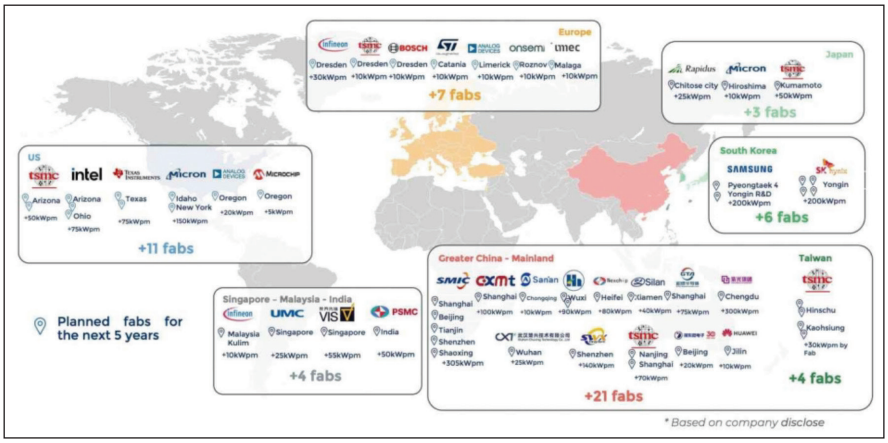
Yole Group's new report, Status of the Semiconductor Foundry Industry, explores the geopolitical, economic, and capacity realignments reshaping the semiconductor foundry industry.

YOLE GROUP unveils its latest Status of the Semiconductor Foundry Industry report, offering a comprehensive view into a sector undergoing profound transformation. At the crossroads of technology, geopolitics, and global market dynamics, this ecosystem is being reshaped by new capacity investments, regional power shifts, and long-term national strategies.

Yole Group's 2025 analysis highlights how the global semiconductor supply chain remains highly fragmented and increasingly vulnerable to geopolitical tensions. Since the U.S. launched a semiconductor-focused trade war, mainland China has ramped up efforts to build a self-sufficient domestic ecosystem. In response, governments worldwide have launched significant subsidy programs to re-localize and fortify their semiconductor infrastructure.

One of the most impressive contrasts identified is in the U.S. market. Pierre Cambou, Principal Analyst, Global Semiconductors at Yole Group, comments: "While American semiconductor companies account for 57% of global wafer demand, they control only about 10% of foundry capacity locally. Indeed, the U.S. ecosystem relies heavily on foundry players located in Taiwan, Japan, and mainland China."

In contrast, Taiwan controls 23% of global foundry capacity but accounts for only 4% of wafer demand, as highlighted by Yole Group in its 2025 foundry report. Taiwanese foundry players mainly supply the US fabless ecosystem through players like TSMC, UMC, and VIS. South Korea with players, such as Samsung, is mostly satisfying its domestic demand with an equal share of global capacity and wafer demand at 19%.



The Status of the Semiconductor Foundry Industry report reveals the worldwide capacity and its distribution as well as regional dependencies. It analyzes this dynamic landscape and how it is expected to evolve.

Mainland China is rapidly becoming a central player. In 2024, it held 21% of foundry capacity despite generating just 5% of global wafer demand. Much of this excess capacity is either foreign-owned or offered as open foundry services, although utilization rates remain below the global average. By 2030, China is projected to dominate the global foundry landscape, accounting for 30% of installed capacity, outpacing Taiwan, South Korea, and Japan.

Europe and Japan are holding steady in terms of the supply-demand balance, though much of their foundry capacity is tied to their own internal market. The Southeast Asian region, especially Singapore and Malaysia, owns 6% of global foundry capacity, although it lacks domestic players and therefore operates entirely on foreign-owned foundries.

Despite fears of overinvestment, Yole Group forecasts that the 4.3% CAGR in foundry capacity will not result in severe overcapacity. Global utilization is expected to hover around 70% through 2030. This relatively low utilization rate will become the new normal. Without a corresponding surge in wafer production and end-market demand, the return on these capital-intensive expansions may fall short.

"The foundry market is more of a capitalistic game than a product competition," explains Pierre Cambou from Yole Group. "Ownership, location, and utilization must now be read through national interests, economic security, and long-term technology strategy."

While U.S.-based players still control roughly 20% of global capacity, 10% locally and 10% abroad, China's domestic players are rapidly expanding own local capacity from 15% in 2024 to significantly more by 2030. This growing divergence between where capacity is built and who owns it points to future uncertainties in market access, supply chain transparency, and strategic leverage.

There's a clear geographical overweight toward Asia, and that will only deepen. The global foundry market will be decided less by where fabs are located and more by who owns them.

TechWorks and Canadian Semiconductor Council sign MoU

TechWorks, the UK industry association for semiconductor and deep tech innovation, has signed a landmark Memorandum of Understanding (MoU) with the Canadian Semiconductor Council (CSC) to foster strategic collaboration between the UK and Canadian semiconductor ecosystems.

THE AGREEMENT recognises the highly complementary strengths of both nations in areas such as advanced packaging, compound semiconductors, quantum technologies, AI, neuromorphic processors, sustainable materials, and more. While traditional high-volume digital CMOS production manufacturing has shifted eastward, the UK and Canada remain at the forefront of innovation across emerging technologies critical to future global competitiveness.

This coincides with the meeting this week in Ottawa between Sir Keir Starmer, Prime Minister of the United Kingdom (UK) and Mark Carney, Prime Minister of Canada to reaffirm the strength of the Canada-UK partnership, deepening trade ties as trusted partners and, in particular, agreeing to work together to enhance both nations' complementary strengths in semiconductors, photonics, emerging materials and chip design.

Their commitment underscores the vision set out in the MoU to build resilient supply chains and accelerate breakthroughs in this key economic growth sector, which is of great importance to both countries.

Charles Sturman, CEO of TechWorks, commented, "This partnership represents a significant milestone for our respective semiconductor industries. By connecting two innovation-rich ecosystems, we are opening the door to deeper collaboration in R&D, talent development, and commercial opportunity. Through shared strengths and common mind-set, we can help build resilient supply chains and accelerate the technologies that will define the next decade."

The MoU sets out a long-term collaborative framework based on:

- Sharing market intelligence, roadmaps, and best practices
- Promoting business-to-business collaboration and trade missions
- Supporting workforce development and academic partnerships
- Facilitating bilateral R&D initiatives, including participation in international innovation programs

Both countries aim to enhance their global competitiveness by increasing trade, foreign direct investment, and innovation output across the full semiconductor and microelectronics value chain—from design to manufacturing to end-use applications in AI, IoT, communications, mobility, and more.

"Canada and the UK have long shared a rich history of collaboration, and this agreement is a natural next step in addressing the growing need for deeper cooperation in the semiconductor sector – especially as global trade dynamics continue to shift rapidly," said Paul Slaby, Managing Director of Canada's Semiconductor Council. "By strengthening ties and leveraging our mutual strengths, we can create new opportunities and lasting impact for both nations."

The UK Science Minister, Lord Vallance said: "This new partnership reflects the UK and Canada's shared commitment to strengthening semiconductor supply chains and deepening international cooperation in critical technologies.

"It will help create new opportunities for businesses and researchers and support our Plan for Change through long-term economic growth."
The Honourable Mélanie Joly, Minister of Industry and Minister responsible for Canada Economic Development for Quebec Regions added:

"Canada and the United Kingdom's partnership demonstrates our shared commitment to advancing innovation and building economic resilience. We are strengthening our leadership in innovation, reinforcing secure supply chains, and creating new opportunities for businesses and researchers on both sides of the Atlantic."

TechWorks and CSC are also working with the UK and Canadian governments to support innovation and economic growth in this critical sector, supporting a jointly funded research and development program focusing on advanced packaging, photonics, and emerging materials. This was recently launched by Innovate UK and Canada's National Research Council Industrial Research Assistance Program (NRC IRAP).

The program aims to foster innovation and resilient supply chains: https://iuk-business-connect.org.uk/opportunities/canada-uk-semiconductors-2025/.

The call for proposals is open to Canadian and UK organisations who wish to form project consortia to collaborate on innovative products, processes, or technology-based services.

NY CREATES and Fraunhofer Institute to advance memory devices at the 300mm wafer scale

NY CREATES and Fraunhofer IPMS has announced at a signing ceremony a new Joint Development Agreement (JDA) to drive research and development focused on memory devices.

THE JDA will leverage and link the strengths of each organization to engineer, develop, and characterize these devices that are critical for advancing the memory development ecosystems of each respective organization.

"As we build upon the strong connections, we have with semiconductor R&D centers around the globe to create the technologies that the U.S. and the world will rely on in the future, we look forward to this collaboration with Fraunhofer IPMS to further develop next-generation ferroelectric memory devices at the 300mm scale," said Dave Anderson, President of NY CREATES.

"We are proud to work together to accelerate the processes and the evaluation and deployment of these materials which can lead to innovative breakthroughs, maintaining our global R&D leadership. With the Center Nanoelectronic Technologies (CNT), Fraunhofer IPMS maintains a leading international competence center for the development of ferroelectric memories based on hafnium oxide (HfO_2). These memory technologies are particularly promising for neuromorphic computing applications as they are very energy efficient, CMOS compatible and scalable down to very small technology nodes. We look forward to working with NY CREATES to develop new promising memory designs based on the expertise of both parties," said Dr. Wenke Weinreich, Deputy Director of Fraunhofer IPMS.

Leaders from the New York Center for Research, Economic Advancement, Technology, Engineering, and Science (NY CREATES), based in Albany, N.Y., and the Fraunhofer Institute for Photonic Microsystems IPMS, based in Dresden, Germany, formalized the JDA with a ceremonial signing by NY CREATES Vice President of Strategies, Partnerships, & New Ventures and Chief Operating Officer Paul Kelly and Fraunhofer IPMS Deputy Director Dr. Wenke Weinreich at NY CREATES' Albany NanoTech Complex on May 15, with a number of dignitaries from New York State and Germany in attendance. NY CREATES and Fraunhofer IPMS will embark on a joint development project for the co-development of advanced memory devices built at the 300mm wafer scale, the platform upon which chips are made.

In May of 2023, representatives from Fraunhofer IPMS met with counterparts at NY CREATES' Albany NanoTech Complex, the largest non-profit semiconductor research and development facility in North America.

There, Dr. Weinreich signed a Memorandum of Understanding between the two organizations and in the presence of Saxony's Minister President Michael Kretschmer with the aim of further advancing economic prosperity through innovation in both regions.

Invest Qatar partners with Ardian and Silian Partners

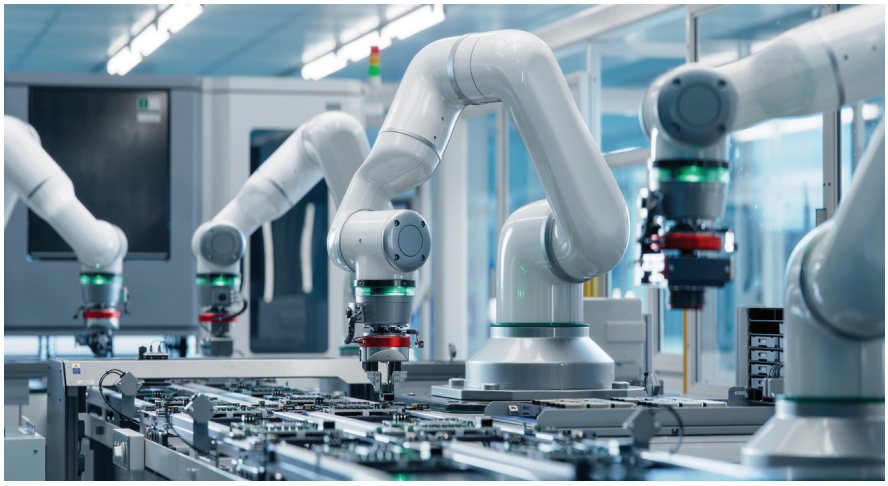
Plan is to foster AI and semiconductor ecosystems in Qatar and the wider region.

THE INVESTMENT PROMOTION AGENCY QATAR (Invest Qatar), Ardian, a world-leading private investment house, and Silian Partners, a unique strategic and operational value creation firm specialised in the global semiconductor industry that has formed a strategic partnership with Ardian to launch Ardian Semiconductor, a pioneering semiconductor private equity platform, have announced a partnership to collaborate on AI and semiconductors.

This initiative will contribute to drive digital innovation and to develop strategic technologies in Qatar. Invest Qatar, Ardian and Silian Partners will work together to attract companies in the AI and semiconductor technology ecosystems to explore opportunities and establish operations in Qatar. In line with these efforts, Silian Partners will establish an office in Qatar to bring significant semiconductor industry capabilities to the country. As part of this partnership, Invest Qatar will facilitate connections between Ardian Semiconductor's portfolio companies and local stakeholders, as well as provide aftercare services for current investors.

The collaboration is poised to introduce various initiatives to support the long-term growth of the technology sector in Qatar such as joint seminars, workshops and conferences to facilitate knowledge sharing and networking. Invest Qatar will also work closely with Ardian and Silian Partners to organise exploratory fact-finding trips for related companies to learn more about Qatar's welcoming and supportive business environment and to experience the country's high quality of life.

Announced during the Qatar Economic Forum in Doha, the MoU was signed by Sheikh Ali Alwaleed Al-Thani, CEO, Invest Qatar; Jan Philipp Schmitz,



Executive Vice President, Ardian; Paul Boudre, CEO, Co-Founder & Partner, Silian Partners.

Sheikh Ali Alwaleed Al-Thani, CEO, Invest Qatar, said: "This partnership with Ardian and Silian Partners exemplifies our commitment to attracting investment in enabling clusters such as IT & Digital in line with Qatar's Third National Development Strategy. By combining Qatar's world-class digital infrastructure and significant investments in RDI with Ardian's proven and successful private equity capabilities and Silian Partner's deep semiconductor industry experience and expertise, we are paving the way to further enhance Qatar's position as a global hub for innovation and piloting new technologies."

Jan Philipp Schmitz, Executive Vice President, Ardian said: "I would like to extend my heartfelt congratulations to all parties involved in the partnership between Invest Qatar, Ardian, and Silian Partners. This collaboration marks a significant milestone in our shared commitment to fostering AI and semiconductor ecosystems in Qatar and the wider region. Ardian Semiconductor, our pioneering private equity platform, will serve as a catalyst for digital innovation and strategic technology development in the region. We are thrilled to see Silian Partners establish an office in Qatar, which will not only bring substantial semiconductor industry expertise to the country but also create new opportunities for growth and investment. This initiative aligns perfectly with our vision to drive forward cutting-edge technologies and solidify Qatar's position as a global hub for innovation. We are eager to explore the new avenues this partnership will open and look forward to a prosperous future together."

Paul Boudre, CEO, Co-Founder & Partner, and Thomas Pebay-Peyroula, Co-Founder & Partner, Silian Partners said: "We are excited to announce that we will locate our global strategy team in Qatar. Our team in Doha will carry out high value-added semiconductor industry research and analysis, which is essential to underpin the investment strategy of the Ardian Semiconductor platform and support portfolio companies in their strategic positioning and growth. Having an on-the-ground presence will also accelerate our vision to participate in the emergence of a differentiated local semiconductor ecosystem, as well as further strengthening our long-term partnership with Qatar."

semi™

Connecting Semiconductors and Electronics

About SEMI:
SEMI connects more than 2,500 member companies and 1.3 million professionals worldwide to advance the technology and business of electronics design and manufacturing. The breadth and depth of our events, programs and services help members accelerate innovation and collaboration on the toughest challenges to growth.

ESDA Electronic System Design Alliance

FlexTech

FOA Fab Owners Alliance

MEMS & SENSORS INDUSTRY GROUP®

SOI Industry Consortium

Accelerating the green transition in the semiconductor industry

SEMI Europe has announced a new three-year Memorandum of Understanding (MoU) with Stockholm Environment Institute (SEI), which will serve as a knowledge partner in the green transition of the semiconductor industry.

The purpose of the MoU between SEMI Europe and SEI is to provide a framework of cooperation and understanding, and to facilitate collaboration to further shared goals and objectives linked to global challenges. These include, but are not limited to, pollution, climate change, decarbonisation, the sustainable development of the semiconductor industry, and the implementation and promotion of the European Green Deal.

"Our strategic collaboration with Stockholm Environment Institute is a key step in driving sustainability across the semiconductor value chain," said Laith Altimime, President of SEMI Europe. "By combining SEMI Europe's industry leadership with SEI's research expertise, we support the EU's goal of climate neutrality through climate action, circularity, and responsible innovation."

Areas of cooperation for the MoU include sustainable consumption and production; sustainable business and industry transition(s), critical metals and minerals, the science-policy interface, environment and human health, circular economy, climate change and atmospheric quality, pollution, artificial intelligence, and education for sustainable development.

"The partnership with SEMI Europe, with its over 3,000 global members, has great potential to be impactful and accelerate implementation of the green transition in the electronics and semiconductor industry," said Måns Nilsson, SEI Executive Director.

SEI is an international non-profit research institute that tackles climate, environmental and sustainable development challenges. It has a diverse research agenda including air pollution, climate change, sustainable consumption, and human health. Using a range of participatory approaches, such as citizen science, SEI helps policymakers around the world make informed decisions for a sustainable future.

Advancing sustainability and innovation

SEMI has released its official position paper on the revision of the European Union's REACH Regulation. The paper outlines the semiconductor industry's priorities for ensuring that the revised regulation supports sustainable manufacturing in Europe while protecting the technological resilience and competitiveness of Europe's semiconductor industry.

"Semiconductors are at the core of Europe's green and digital transition, and the REACH revision must reflect the unique role our industry plays in enabling this future," said Laith Altimime, President of SEMI Europe. "This paper highlights how a more tailored, risk-based approach to regulation can ensure continued access to critical materials, foster innovation, and uphold the EU's leadership in sustainable manufacturing."

The REACH revision proposal is expected in Q4 2025. With key regulatory decisions approaching, SEMI Europe is calling for a balanced and forward-looking framework that enables both environmental protection and technological progress.

Key recommendations from SEMI Europe include:

- Introducing sector-specific derogations and realistic transition timelines for complex industrial sectors such as semiconductors.

- Ensuring restriction decisions are based on full risk assessments that account for real-world use and exposure, rather than hazard alone.
- Avoiding mandatory polymer registration for proprietary process chemicals already governed under existing frameworks.
- Applying substance grouping and substitution planning with greater scientific precision, especially for critical-use substances.
- Clarifying and operationalizing the essential use concept in a transparent, proportionate, and industry-relevant manner.
- Strengthening nanomaterials regulation through targeted updates to safety data sheets, testing guidelines, and integration of the revised EU definition.

The paper also highlights the importance of ensuring that the REACH revision does not conflict with strategic EU initiatives, including the European Chips Act, and calls for deeper engagement between regulators and high-technology industries in shaping effective, innovation-compatible policy. "SEMI Europe stands ready to work with EU institutions, regulators, and relevant stakeholders to ensure the REACH revision reflects both scientific evidence and the operational realities of the semiconductor sector," said Altimime. "By aligning regulatory ambition with industrial capabilities, Europe can achieve its sustainability goals while preserving long-term strategic resilience."

Strengthening Europe's competitiveness and advancing innovation

Seeking to explore semiconductor policy measures that can strengthen Europe's industrial ecosystem, SEMI, the European Semiconductor Industry Association (ESIA), the Global Electronics Association (formerly IPC), and the European Association of Automotive Suppliers (CLEPA) have successfully held a roundtable in Brussels, bringing together representatives from the European Commission and national governments.

The 2023 European Chips Act marked an important milestone for Europe's semiconductor industry and overall industrial ecosystem, providing concrete measures to enhance competitiveness and technological capabilities. In order to build on the success of the Chips Act, the next 2028-2034 Multi-Annual Financial Framework (MFF) – the long-term budget of the European Union – must continue to deliver strategic investments to support manufacturing capabilities, research and development (R&D), supply chain resilience and access to critical raw materials.

"The creation of a new European semiconductor strategy was a focal point of the roundtable discussion, emphasizing on the increasing need to boost the technological capabilities and accelerate innovation across the European semiconductor ecosystem," said Laith Altimime, President, SEMI Europe. "We look forward to continuing our discussions with the European Commission to make sure the MFF effectively supports the semiconductor industry's pivotal role in technology advancement."

SEMI applauded the ongoing initiatives of European policymakers, together with the progress already made to bolster the European semiconductor ecosystem. Nevertheless, considering the existing concerns and challenges of industry raised during this forum, the European semiconductor ecosystem requires a holistic approach that decisively supports competitiveness while preserving supply chain resilience and security in the longer term.

SEMI will continue to engage with the relevant policymakers and stakeholders to create a policy framework that can strengthen the entire European semiconductor supply chain while preserving technological competitiveness.

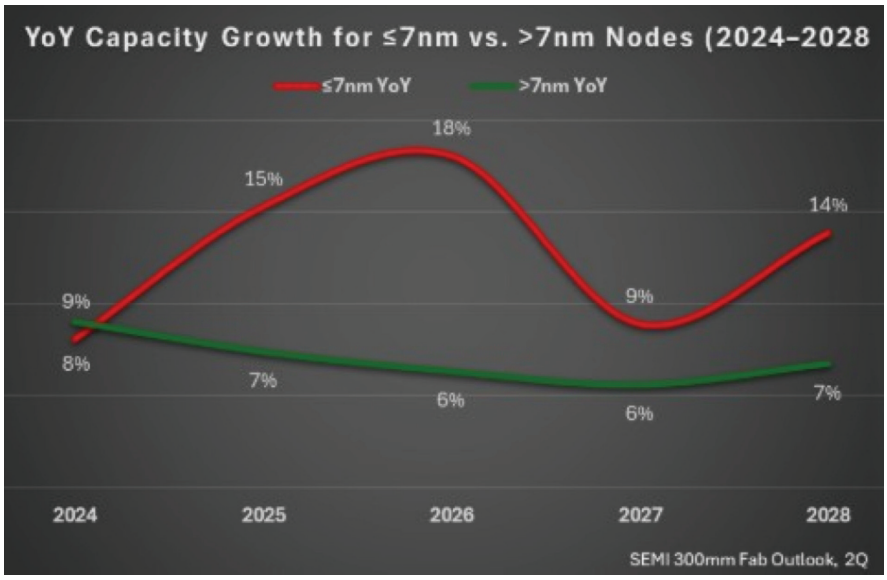
69% growth in advanced chipmaking capacity through 2028 due to AI

SEMI has reported findings from its latest 300mm Fab Outlook report. The report shows global front-end semiconductor suppliers are accelerating expansion efforts to support the surging demand for generative AI applications.

According to the 300mm Fab Outlook report, the global semiconductor manufacturing industry is expected to maintain strong momentum, with capacity projected to grow at a compound annual growth rate (CAGR) of 7% from the end of 2024 through 2028, reaching a record high of 11.1 million wafers per month (wpm).

A key driver of this growth is the continued expansion of advanced process capacity (7nm and below), which is expected to increase by approximately 69% – from 850,000 wpm in 2024 to a historic high of 1.4 million wpm in 2028 – representing a CAGR of around 14%, double the industry average.

"AI continues to be a transformative force in the global semiconductor industry, driving significant expansion of advanced manufacturing capacity," said SEMI President and CEO Ajit Manocha. "The rapid proliferation of AI applications is stimulating robust



investment across the semiconductor ecosystem, underscoring the industry's pivotal role in fostering technology innovation and meeting the surging demand for advanced chips."

AI Continues to Drive Demand for Advanced Nodes

Beyond the demand for increasingly powerful training capabilities to support larger AI model architectures, AI inference has emerged as another critical catalyst for growth. Market expansion is further fueled by AI's integration into system software for personal assistants and innovative applications.

Moreover, AI is also enabling new breakthroughs in virtual and augmented reality devices, as well as humanoid robotic sectors, which are expected to sustain strong demand for advanced semiconductor technologies over the next several years.

Advanced Process Capacity Expansion Maintains Double-Digit Growth

Advanced process capacity is projected to maintain a robust 14% CAGR from 2025 through 2028, beginning with 982 thousand wpm in 2025, representing 15% YoY growth. The industry is expected to achieve a significant milestone in 2026, surpassing one million wafers for the first time, with capacity reaching 1.16 million wpm.

2nm and below capacity deployment shows even more aggressive scaling throughout the forecast period, with production capacity expanding dramatically from less than 200 thousand wpm in 2025 to over 500 thousand wpm by 2028, reflecting the strong market demand driven by AI applications in advanced manufacturing.

Fab Equipment in Advanced Technology Soar in 2025 and 2027

The semiconductor industry's investment landscape remains firmly anchored in advanced process technologies. Capital expenditure on advanced process equipment is forecast to surge to over US$50 billion by 2028, representing a substantial 94% increase from the US$26 billion invested in 2024.

This trajectory underscores the industry's resolute commitment to next-generation manufacturing capabilities, reflecting a robust 18% CAGR.

The transition to cutting-edge nodes continues to accelerate, with 2nm technology projected to reach mass production by 2026, followed by the commercial deployment of 1.4 nm technology in 2028.

In anticipation of growing market demand, chip manufacturers are strategically expanding production capacity ahead of schedule, with growth rates of 33% in 2025 and 21% in 2027, respectively.

Investment in 2nm and below wafer equipment represents a particularly dramatic expansion, with funding more than doubling from US$19 billion in 2024 to US$43 billion in 2028.

A remarkable 120% increase that underscores the industry's aggressive pursuit of next-generation manufacturing capabilities.

Semiconductor manufacturing equipment market: endless potential in chip making

The global semiconductor manufacturing equipment market is currently at the forefront of a major technological shift led by the rapid rise of applications like AI, 5G, IoT, automotive electronics, and advanced packaging.

SEMICONDUCTOR manufacturing equipment (SME) has now burst into the limelight, which is paving the way for the future of mobility, healthcare, energy, and defense. Governments are investing heavily in reshoring, supply chain security, and innovation. As per a report published by Research Nester, the semiconductor manufacturing equipment market is projected to reach an impressive USD 350.3 billion by 2037.

The growth is driven by the global shift towards electric and autonomous vehicles and the increasing demand for advanced, smaller node semiconductor technologies like 5 nm and 3 nm chips. As the automotive sector embraces electrification and self-driving technology, the need for high-performance semiconductors has skyrocketed. This surge has prompted substantial investments in SiC chip manufacturing facilities. At the same time, the semiconductor industry is pushing for miniaturization. This is leading to a soaring demand for ultra-precise manufacturing equipment. Further, let's dive into the trends and market dynamics shaping this vibrant industry.

Rise of advanced packaging

The surge in advanced packaging technologies is becoming a key player in the growth of the semiconductor manufacturing equipment market. This has increased the need for specialized equipment for precise assembly, bonding, interconnection, and inspection. Additionally, the need to manage delicate, high-density interconnects and multi-layer structures is driving the demand for ultra-precise manufacturing systems. This trend is further fueled by the growing applications in areas like AI accelerators, 5G modules, IoT devices, and automotive electronics.

For instance, in September 2024, Tata Electronics announced a partnership with ASMPT Singapore for the development of semiconductor assembly equipment for its chip packaging units in Assam and Karnataka. This collaboration is all about R&D in areas like wire bonding, flip-chip technology, and advanced packaging. The goal of this partnership is to create a strong semiconductor assembly and testing infrastructure while prioritizing energy and material efficiency to promote sustainable growth and strengthen the semiconductor supply chain.

Incorporation of Artificial Intelligence (AI) and Machine Learning (ML)

As the process of chip fabrication gets more intricate, manufacturers are increasingly relying on AI and ML to boost operational efficiency. One of the standout uses of AI in semiconductor manufacturing equipment is predictive maintenance. This proactive approach cuts down on unexpected downtime, prolongs the lifespan of equipment.

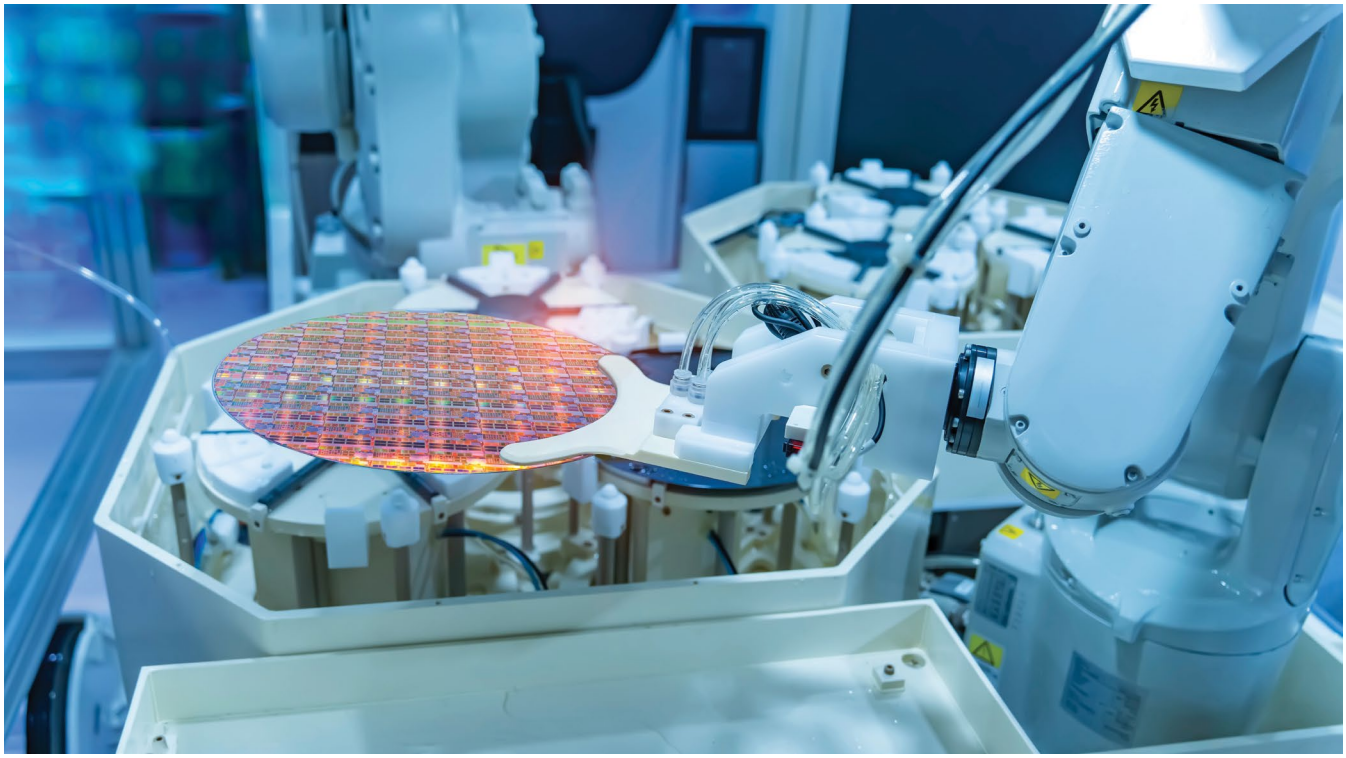
Moreover, AI and ML are also making waves in process optimization and defect detection. AI is revolutionizing smart automation in semiconductor fabs that boost yield and cut down on energy use. The integration of AI and ML is also transforming equipment design and functionality. Consequently, this is positioning it as a crucial factor for long-term growth in the market. In March 2025, YES, a leading manufacturer of process equipment for AI and high-performance computing (HPC) semiconductor solutions, announced the shipment of its very first commercial VeroTherm Formic Acid Reflow tool to a prominent global semiconductor manufacturer.

This showcases the first piece of equipment made in India for cutting-edge semiconductor applications like high bandwidth memory (HBM), which is essential for AI and high-performance computing (HPC) around the globe.

Adoption of advanced lithography

The rise of cutting-edge lithography techniques is reshaping the semiconductor manufacturing equipment market. EUV lithography has become crucial for making these next-gen processes a reality. This transition has led to a surge in demand for highly complex, high-value lithography equipment. In February 2025, DuPont announced that showcase its latest innovations through a series of technical presentations that will highlight the development of photoresists for EUV lithography.

The introduction of High-NA EUV systems is likely to further boost capital spending among major players like Intel, TSMC, and Samsung. Recently, in June 2025, ASML, the world's sole provider of extreme ultraviolet (EUV) lithography machines, declared to move forward with its next-generation High-NA (numerical aperture) EUV systems. Furthermore, a new wave of investment in R&D,



production capacity is solidifying advanced lithography as a key player in the expansion of the market.

Investments in semiconductor fabrication (Fab) expansion

The recent surge in investments aimed at expanding semiconductor fab plants is playing a pivotal role in boosting the semiconductor manufacturing equipment, such as lithography systems, etching machines, deposition tools, cleaning units, and metrology devices.

Fab expansion is a fundamental shift in the global manufacturing strategy. Key players like Samsung, Intel, and GlobalFoundries are pouring billions into next-gen fabs across the U.S., Taiwan, South Korea, and Europe.

Government initiatives like the U.S. CHIPS Act, the European Chips Act are providing robust policy support, funding incentives to enhance domestic semiconductor production. This movement is resulting in a promising growth trajectory that looks set to continue well into the next decade. Let's have a look at recent investments in semiconductor fab expansion by several regions.

- In June 2025, Texas Instruments announced a groundbreaking investment of over USD 60 billion in seven semiconductor fabs across the U.S. This marks the largest commitment to foundational semiconductor manufacturing in the nation's history. This expansion will significantly boost our manufacturing capacity to meet the rising demand for semiconductors.
- In March 2024, the Indian government gave the green light to a significant investment to feature the nation's very first cutting-edge semiconductor fabrication plant. A whopping USD 15 billion has been allocated for these ambitious projects.

In a nutshell

The semiconductor manufacturing equipment market is now a vital cornerstone of global innovation and economic stability. As various industries sprint towards digital transformation, the appetite for advanced semiconductors is skyrocketing.

The constant drive for smaller, more powerful chips, the emergence of advanced packaging and 3D integration, and the incorporation of AI and automation are expanding the semiconductor manufacturing equipment market.

Key players like Applied Materials, Lam Research, and Tokyo Electron are innovating rapidly to adapt to the shifting semiconductor landscape. At the same time, countries are pouring billions into policy initiatives to bolster domestic manufacturing capabilities. Looking ahead, the SME market will play a crucial role in driving the future of technology forward.

https://www.researchnester.com/reports/semiconductor-manufacturing-equipment-market/5058

As the process of chip fabrication gets more intricate, manufacturers are increasingly relying on AI and ML to boost operational efficiency. One of the standout uses of AI in semiconductor manufacturing equipment is predictive maintenance. This proactive approach cuts down on unexpected downtime, prolongs the lifespan of equipment

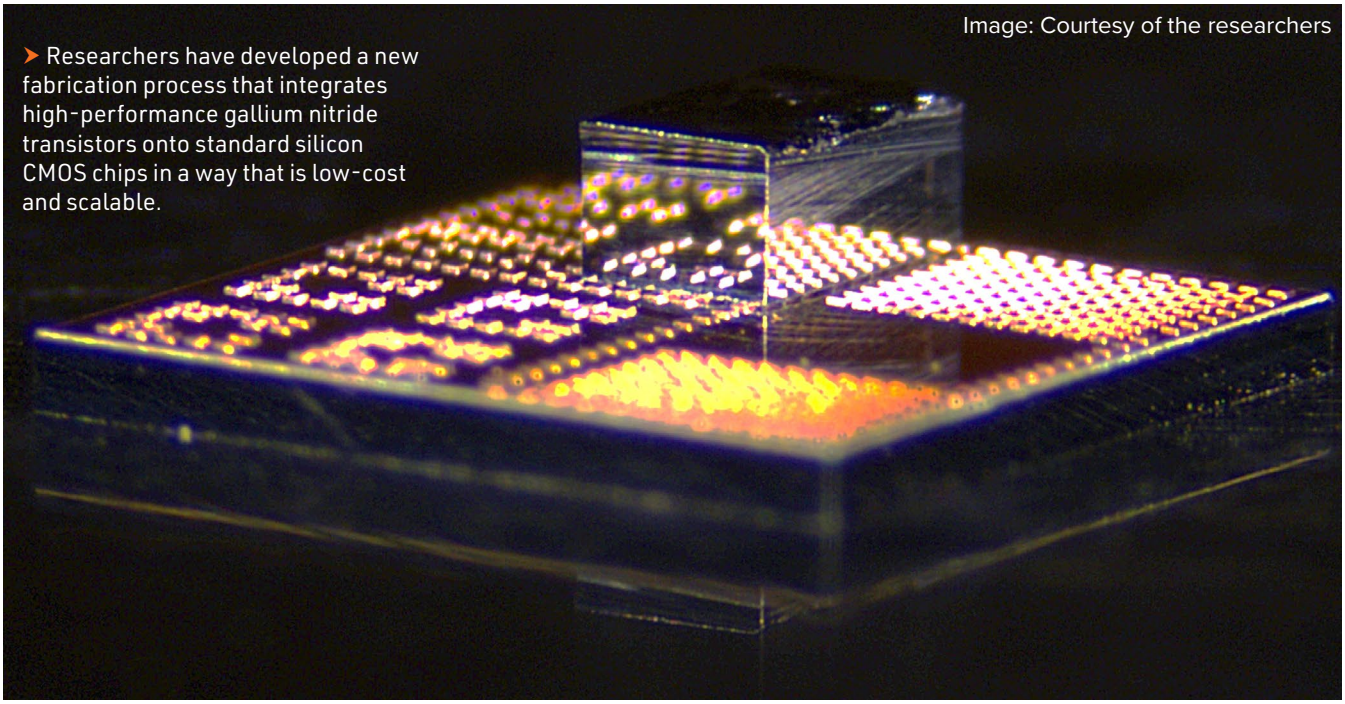


Image: Courtesy of the researchers

➤ Researchers have developed a new fabrication process that integrates high-performance gallium nitride transistors onto standard silicon CMOS chips in a way that is low-cost and scalable.

New 3D chips could make electronics faster and more energy-efficient

The low-cost, scalable technology can seamlessly integrate high-speed gallium nitride transistors onto a standard silicon chip.

BY ADAM ZEWE, MIT NEWS

THE ADVANCED semiconductor material gallium nitride will likely be key for the next generation of high-speed communication systems and the power electronics needed for state-of-the-art data centers.

Unfortunately, the high cost of gallium nitride (GaN) and the specialization required to incorporate this semiconductor material into conventional electronics have limited its use in commercial applications.
Now, researchers from MIT and elsewhere have developed a new fabrication process that integrates high-performance GaN transistors onto standard silicon CMOS chips in a way that is low-cost and scalable, and compatible with existing semiconductor foundries.

Their method involves building many tiny transistors on the surface of a GaN chip, cutting out each individual transistor, and then bonding just the necessary number of transistors onto a silicon chip using a low-temperature process that preserves the functionality of both materials.

The cost remains minimal since only a tiny amount of GaN material is added to the chip, but the resulting device can receive a significant performance boost from compact, high-speed transistors. In addition, by separating the GaN circuit into discrete transistors that can be spread over the silicon chip, the new technology is able to reduce the temperature of the overall system.

The researchers used this process to fabricate a power amplifier, an essential component in mobile phones, that achieves higher signal strength and efficiencies than devices with silicon transistors. In a smartphone, this could improve call quality, boost wireless bandwidth, enhance connectivity, and extend battery life. Because their method fits into standard procedures, it could improve electronics that exist today as well as future technologies. Down the road, the new integration scheme could even enable quantum applications, as GaN performs better than silicon at the cryogenic temperatures essential for many types of quantum computing. “If we can bring the cost down, improve the scalability, and, at the same time, enhance the performance of the electronic device, it is a no-brainer that we should adopt this technology. We’ve combined the best of what exists in silicon with the best possible gallium nitride electronics. These hybrid chips can revolutionize many commercial markets,” says Pradyot Yadav, an MIT graduate student and lead author of a paper on this method.

He is joined on the paper by fellow MIT graduate students Jinchen Wang and Patrick Darmawi-Iskandar; MIT postdoc John Niroula; senior authors Ulriche L. Rodhe, a visiting scientist at the Microsystems Technology Laboratories (MTL), and Ruonan Han, an associate professor in the Department of Electrical Engineering and Computer Science (EECS) and member of MTL;

and Tomás Palacios, the Clarence J. LeBel Professor of EECS, and director of MTL; as well as collaborators at Georgia Tech and the Air Force Research Laboratory. The research was recently presented at the IEEE Radio Frequency Integrated Circuits Symposium.

Swapping transistors

Gallium nitride is the second most widely used semiconductor in the world, just after silicon, and its unique properties make it ideal for applications such as lighting, radar systems and power electronics.

The material has been around for decades and, to get access to its maximum performance, it is important for chips made of GaN to be connected to digital chips made of silicon, also called CMOS chips. To enable this, some integration methods bond GaN transistors onto a CMOS chip by soldering the connections, but this limits how small the GaN transistors can be. The tinier the transistors, the higher the frequency at which they can work. Other methods integrate an entire gallium nitride wafer on top of a silicon wafer, but using so much material is extremely costly, especially since the GaN is only needed in a few tiny transistors. The rest of the material in the GaN wafer is wasted.

"We wanted to combine the functionality of GaN with the power of digital chips made of silicon, but without having to compromise on either cost of bandwidth. We achieved that by adding super-tiny discrete gallium nitride transistors right on top of the silicon chip," Yadav explains. The new chips are the result of a multistep process.

First, a tightly packed collection of miniscule transistors is fabricated across the entire surface of a GaN wafer. Using very fine laser technology, they cut each one down to just the size of the transistor, which is 240 by 410 microns, forming what they call a dielet. (A micron is one millionth of a meter.) Each transistor is fabricated with tiny copper pillars on top, which they use to bond directly to the copper pillars on the surface of a standard silicon CMOS chip. Copper to copper bonding can be done at temperatures below 400 degrees Celsius, which is low enough to avoid damaging either material.

Current GaN integration techniques require bonds that utilize gold, an expensive material that needs much higher temperatures and stronger bonding forces than copper. Since gold can contaminate the tools used in most semiconductor foundries, it typically requires specialized facilities.

"We wanted a process that was low-cost, low-temperature, and low-force, and copper wins on all of those related to gold. At the same time, it has better conductivity," Yadav says.

A new tool

To enable the integration process, they created a specialized new tool that can carefully integrate the extremely tiny GaN transistor with the silicon chips. The tool uses a vacuum to hold the dielet as it moves on top of a silicon chip, zeroing in on the copper bonding interface with nanometer precision. They used advanced microscopy to monitor the interface, and then when the dielet is in the right position, they apply heat and pressure to bond the GaN transistor to the chip. "For each step in the process, I had to find a new collaborator who knew how to do the technique that I needed, learn from them, and then integrate that into my platform. It was two years of constant learning," Yadav says.

Once the researchers had perfected the fabrication process, they demonstrated it by developing power amplifiers, which are radio frequency circuits that boost wireless signals. Their devices achieved higher bandwidth and better gain than devices made with traditional silicon transistors. Each compact chip has an area of less than half a square millimeter.

In addition, because the silicon chip they used in their demonstration is based on Intel 16 22nm FinFET state-of-the-art metallization and passive options, they were able to incorporate components often used in silicon circuits, such as neutralization capacitors. This significantly improved the gain of the amplifier, bringing it one step closer to enabling the next generation of wireless technologies.

This work is supported, in part, by the U.S. Department of Defense through the National Defense Science and Engineering Graduate (NDSEG) Fellowship Program and CHIMES, one of the seven centers in JUMP 2.0, a Semiconductor Research Corporation Program by the Department of Defense and the Defense Advanced Research Projects Agency (DARPA). Fabrication was carried out using facilities at MIT.Nano, the Air Force Research Laboratory, and Georgia Tech.
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Applied Materials and CEA-Leti expand joint lab to drive innovation in specialty chips

Based at CEA-Leti, collaboration focuses on materials engineering solutions to enable more energy-efficient AI Data centres.

APPLIED MATERIALS, INC. and CEA-Leti have outlined the next phase of their longstanding collaboration to accelerate innovation in specialty semiconductors. Through an expansion of their joint lab, the organizations plan to develop materials engineering solutions to address emerging infrastructure challenges in AI data centers.

The joint lab is focused on device innovations for chipmakers serving ICAPS markets (IoT, Communications, Automotive, Power and Sensors). These specialty chips are used in a wide range of applications – from industrial automation to electric vehicles – and they play a critical role managing data and power distribution within data centers. Growing resource demands in AI infrastructure have highlighted the need for a new wave of innovation in ICAPS chips to enable more energy-efficient computing.

Under the new agreement, Applied and CEA-Leti will expand the lab with new equipment and capabilities that move beyond individual process steps to include full-flow development of specialty devices. Additionally, the lab will be equipped with state-of-the-art advanced packaging tools to support heterogeneous integration of chips across different wafer types and process nodes – enabling entirely new classes of specialty devices for a range of next-generation applications.

The joint facility features several Applied Materials wafer processing systems together with CEA-Leti's world-class capabilities for evaluating performance of new materials and device validation. The upgraded lab will strengthen the chipmaking ecosystem in France by further expanding the technology hub in Grenoble, a leading site for collaborative innovation across government, academia and industry.

The lab also marks an extension of Applied's global EPIC Platform, a new high-velocity innovation model designed to accelerate commercialization of new chip technologies. Applied and CEA-Leti will be able to leverage the R&D work taking place across Applied's global innovation centers to drive progress in specialty semiconductor technologies.

"Applied Materials and CEA-Leti have a long history of successful collaboration, and we are excited to strengthen our capabilities for accelerating innovation and commercialization of next-generation specialty chips," said Aninda Moitra, corporate vice president and general manager of Applied Materials' ICAPS business. "Our combined expertise will help foster breakthroughs and push the boundaries of semiconductor innovation, contributing to sustainable advancements in a range of critical applications for the AI era." Sébastian Dauvé, CEO of CEA-Leti, said the first phase of the expanded collaboration laid important groundwork for addressing materials-engineering challenges of specialty semiconductor devices.

"Building on this momentum, the joint lab's new focus on energy-efficient solutions for AI data-center infrastructure reflects our shared commitment to making technological progress that meets both industrial

and societal needs. The extended partnership also leverages our complementary strengths to accelerate innovation at the system level, while supporting sustainable growth in France's semiconductor ecosystem," he said.

CEA-Leti and Soitec form strategic partnership

CEA-Leti and Soitec have formed a strategic partnership to enhance the cybersecurity of integrated circuits (ICs) through the innovative use of fully depleted silicon-on-insulator (FD-SOI) technologies.

This collaboration aims to position FD-SOI as a foundational platform for secure electronics by leveraging and extending its inherent resistance to physical attacks.

At the heart of the initiative is a joint effort to experimentally validate and augment the security benefits of FD-SOI—from the substrate level up to circuit design. The project aims to deliver concrete data, practical demonstrations, and roadmap guidance to meet the surging cybersecurity demands in critical markets such as automotive, industrial IoT, and secure infrastructure.

Combining expertise to secure the future of electronics

The partnership, which will utilize GlobalFoundries' advanced chip manufacturing capabilities, will address a growing need for trusted components in embedded and cyber-physical systems – systems that must deliver security services and withstand both software- and hardware-level attacks. With FD-SOI's proven advantages against laser fault injection (LFI) attacks due to its thin-film architecture and channel isolation, the technology presents a compelling foundation for next-generation secure IC design.

Key goals of the partnership include:

- Highlighting FD-SOI's existing strengths in cybersecurity.
- Co-developing innovations across the substrate-design stack to boost physical robustness and meet security requirements in automotive and other embedded systems.
- Demonstrating empirical security data to reinforce FD-SOI's credibility in certification contexts such as SESIP and Common Criteria.

> "Applied Materials and CEA-Leti have a long history of successful collaboration, and we are excited to strengthen our capabilities for accelerating innovation and commercialization of next-generation specialty chips"

- Context: Rising Threats, Rising Demand

"In an era marked by increasing attacks on connected systems and autonomous vehicles, the need for embedded hardware capable of resisting physical tampering has never been greater," said CEA-Leti CTO Jean-René Lequepeys. "FD-SOI's unique combination of performance, energy efficiency, and attack resistance offers an ideal answer for industries that demand both trust and efficiency. This project will leverage research results from the FAMES Pilot Line."

FD-SOI's critical benefits include:

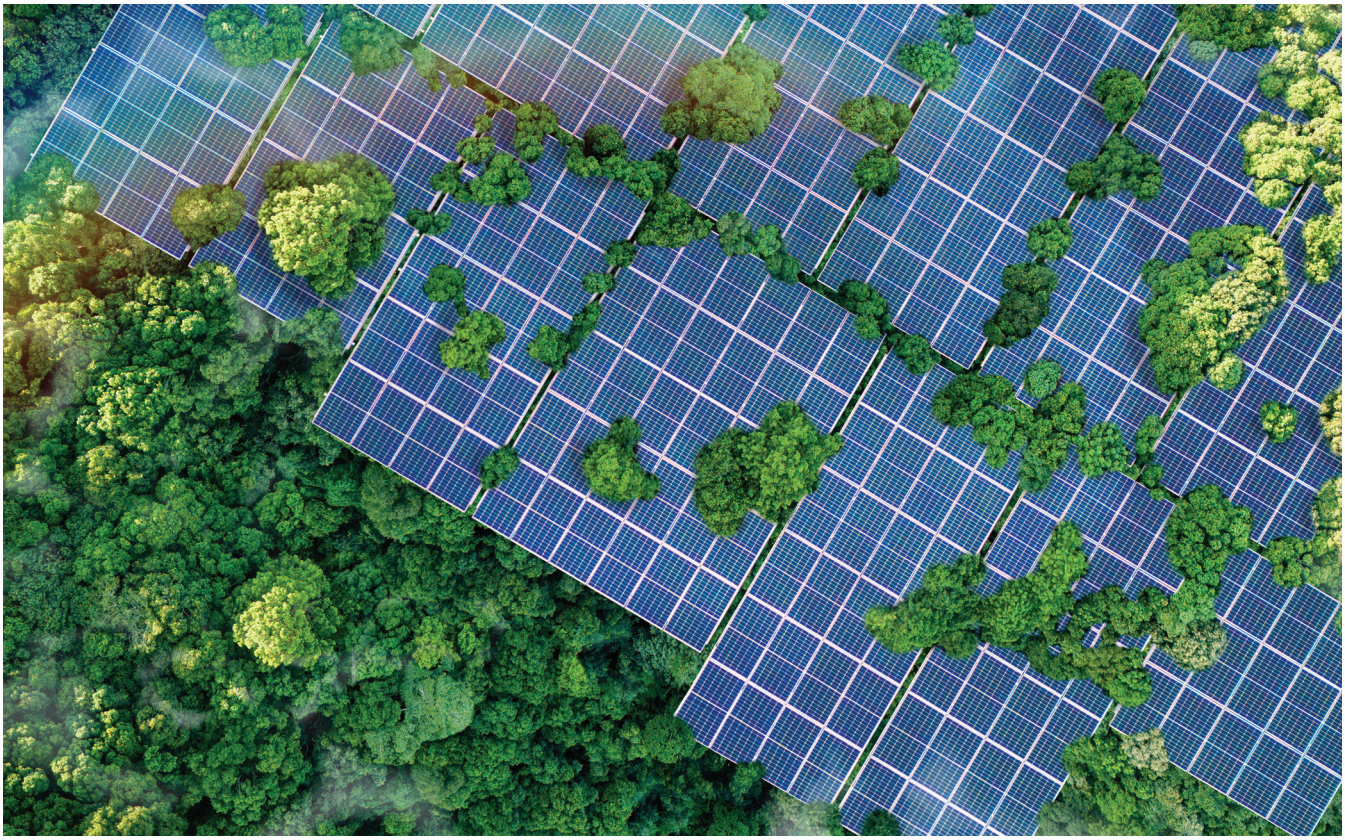
- Physical attack resistance, enabled by electrical isolation between the channel and substrate.
- Power-performance optimization, vital for battery-constrained applications like automotive ECUs and industrial sensors.
- Security design enablement, allowing tailored countermeasures such as fault detection and isolation of sensitive circuit domains.
- Long-Term Vision: Toward a New Cyber-Substrate

While the initial phase focuses on leveraging existing FD-SOI capabilities, the project sets the stage for long-term innovation. The envisioned next-generation cyber-substrate would expand upon FD-SOI's strengths by incorporating:

Enhanced protection against backside and invasive physical attacks. Embedded anti-tamper features and physical unclonable functions (PUFs) for hardware fingerprinting.

Dynamic response mechanisms to detect and counter emerging threats. This future-oriented work will address both cyber and supply-chain vulnerabilities – making FD-SOI not only more secure, but also more indispensable.

Soitec's Senior Executive Vice President in charge of Innovation and Chief Technology Officer Christophe Maleville said: "This partnership with CEA-Leti reflects our strategic ambition to position FD-SOI as a reference platform for secure and energy-efficient electronics. By combining our substrate innovation capabilities with CEA-Leti's research excellence, we aim to demonstrate the full potential of FD-SOI in addressing today's most pressing security challenges. Together, we are paving the way for a new generation of trusted technologies that are essential to the future of connected systems."



GENESIS Project launches to lead Europe's transition to sustainable semiconductor manufacturing

58 partners charged with implementing cutting-edge solutions for emission control, materials innovation, waste reduction and raw material reuse.

A PAN-EUROPEAN consortium dedicated to developing sustainable processes and technologies for the semiconductor-manufacturing industry has announced the launch of the GENESIS project.

This integrated, large-scale initiative aims to enable Europe's chip industry to meet its sustainability goals – from materials development to final waste treatment.

Coordinated by CEA-Leti, the three-year project brings together 58 partners spanning the entire European semiconductor value chain, from large enterprises and SMEs to research institutes, universities, and industry associations.

GENESIS will drive innovative solutions in emission control, eco-friendly materials such as alternatives to PFAS-based ones, waste minimization, and raw material reuse, directly aligned with the European Green Deal and European Chips Act.

"GENESIS is designed to address the complex challenges of building a truly sustainable semiconductor ecosystem," said Laurent Pain, Sustainable Electronics Program director at CEA-Leti. "Its structure reflects both the urgency and the opportunity of Europe's green transition, powered by the complementary expertise and close collaboration of its partners."

45 sustainability innovations driven by four strategic pillars

Pain, manager of the project, noted that the team expects to deliver approximately 45 sustainability-driven innovations covering the semiconductor lifecycle, guided by four strategic pillars that form the technological foundation of GENESIS's vision for a green European semiconductor industry:

- **Pillar 1 – Monitoring & Sensing:** Real-time emissions tracking, traceability, and process feedback systems,
- **Pillar 2 – New Materials:** PFAS-free chemistries and low-GWP alternatives for advanced semiconductor processes,
- **Pillar 3 – Waste Minimization:** Innovations in recycling (solvent, gas, slurries), reuse, and sustainable replacements, and
- **Pillar 4 – Critical Raw Materials Mitigation:** Strategies to reduce dependency on CRM and strengthen resource security.

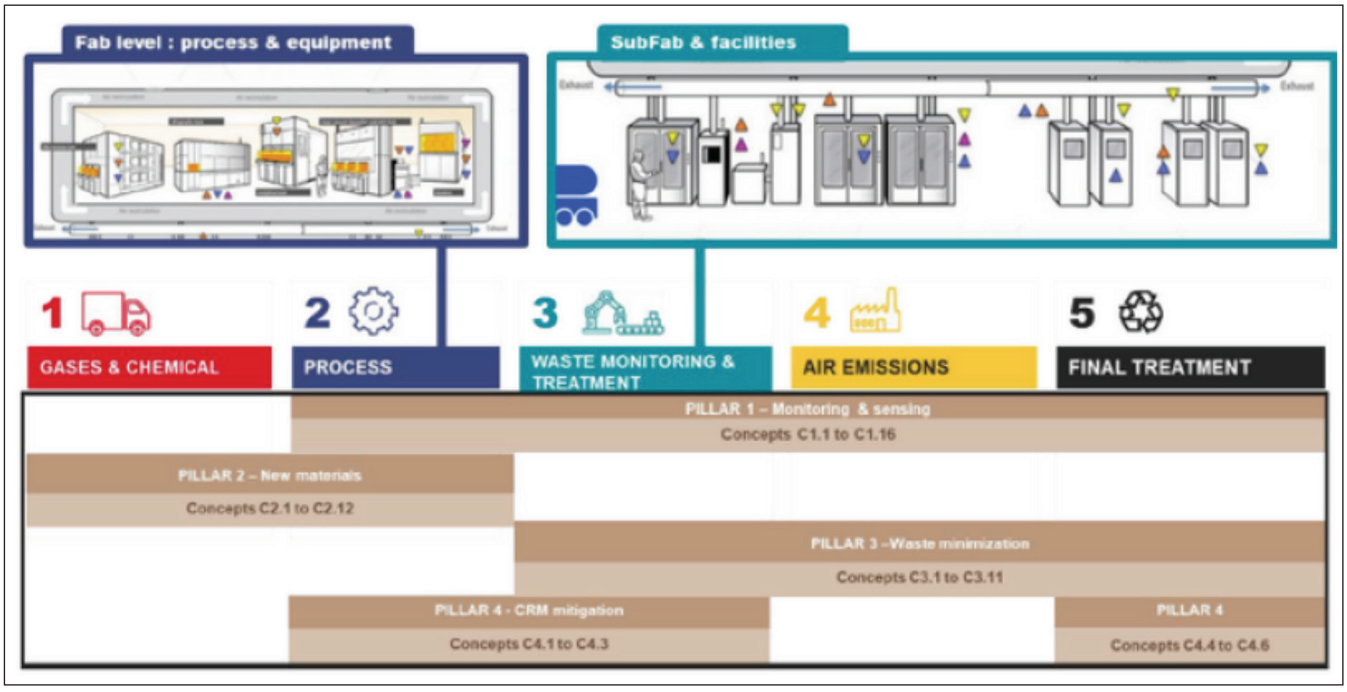
Complimenting these pillars, the project's objectives establish an overall framework that includes deploying sensor-integrated abatement systems to reduce PFAS and GHG emissions. It also aims to position Europe as a leader in green semiconductor innovation by aligning supply-chain practices with environmental regulations.

A green fit for Europe's chips agenda

"The launch of the GENESIS project marks a critical step toward aligning Europe's semiconductor ambitions with its climate commitments," said Anton Chichkov, head of programs at Chips Joint Undertaking (Chips JU), a public-private partnership created to bolster Europe's semiconductor industry by fostering collaboration between the EU, member states, and the private sector.

"As chips become the backbone of everything from AI to energy systems, their environmental footprint is rapidly growing," he said. "GENESIS responds to this urgent challenge by pioneering sustainable alternatives in materials, waste reduction, and resource efficiency. Through this initiative, Europe is not only investing in cleaner technologies—it's positioning itself as a global leader in green semiconductor manufacturing."

With a budget of close to €55 million, the GENESIS project is co-funded through the Chips Joint Undertaking by the European Commission, participating EU member states, and the Swiss State Secretariat for Education, Research and Innovation (SERI).



➤ The Five Critical Stages in Chip-Making Lifecycle Addressed by GENESIS: The GENESIS integrated roadmap outlines five critical stages in the semiconductor manufacturing lifecycle - materials (PFAS-free alternatives & gases and chemicals, processes, waste monitoring & treatments, air emissions and final treatments – wherer environmental impact can be minimised. This structured approach guides the project's efforts to reduce emissions, eliminate harmful substances and enable material recovery through innovation in sensing, materials, waste reduction and raw material reuse.

EU Project ELENA pioneers LNOI Platform for next-gen photonic circuits and Europe's first commercial supplier of LNOI wafers

Capacity to deliver millions of TFLN chips annually 'firmly positions Europe as a global leader in photonic chip manufacturing'.

A RECENTLY concluded 42-month EU project, ELENA, has announced the development of the first-ever, European-made lithium niobate on insulator (LNOI) substrates for photonic integrated circuits (PICs) – a breakthrough that establishes a fully European supply chain for thin-film lithium niobate (TFLN) technology.

TFLN is a breakthrough material platform enabling high-performance PICs through its thin-film structure, offering unique electro-optic, nonlinear optical, and acousto-optic properties. The advent of LNOI wafers allows micromachining of LN with high precision, integrating multiple optical functions within a footprint smaller than a fingertip. These attributes make LNOI particularly attractive for high-speed, low-power optical communications and quantum systems.

Until now, the LNOI ecosystem has been constrained by a limited supply chain reliant on a single commercial supplier outside the EU – and the absence of a commercial foundry capable of producing TFLN photonic chips at scale. The ELENA project directly addressed these critical gaps by establishing Europe's first commercial LNOI wafer supply and laying the groundwork for a TFLN photonic chip foundry.

The €5 million initiative united 10 partners across the PIC value chain –

from substrate innovation and photonic design to manufacturing, testing, and packaging. Key outcomes include the first process design kit (PDK) for the LNOI platform and advances in foundry-compatible processes to transition TFLN technology from research to commercial production. This effort significantly enhances European sovereignty in a strategically vital segment of the semiconductor supply chain.

Spinout launched to produce TFLN photonic chips on 150mm optical grade wafers

A cornerstone of the project is the creation of Europe's first open-access LNOI photonic chip foundry at the Swiss Center for Electronics and Microtechnology's (CSEM) certified cleanroom facility in Neuchâtel, Switzerland.

There, TFLN chips will be produced on 150 mm optical-grade LNOI wafers at industrial scale. As a result, CSEM, which coordinated the project, has launched CCRAFT, a dedicated spinout to scale up production.

"The spinout foundry is uniquely positioned at the core of the TFLN value chain, because it delivers production-grade service, a rare block in the supply chain," said Hamed Sattari, ELENA's project manager and CEO of CCRAFT.

"CCRAFT's roadmap includes expanding capacity to deliver millions of TFLN chips annually, firmly positioning Europe as a global leader in photonic-chip manufacturing."

The availability of a production-grade photonic chip foundry, combined with project members CEA-Leti and SOITEC's plans to commercialize LNOI wafers, also supports Europe's ability to manufacture the next generation of photonic chips across a broad range of markets and industries.

Meeting diverse market needs with demonstrator prototypes

To validate the platform, ELENA produced four demonstrator PICs targeting high-impact sectors:

- **Quantum:** ion trapping, optical clocks, entangled photon generation,
- **Telecom:** >400 Gbit/s modulators, DWDM, CMOS-compatible transceivers,
- **Space:** lightweight, low-power PICs for satellite communications, and
- **LIDAR/Sensing:** compact, efficient systems for automotive, medical, and environmental monitoring.

As demand surges for faster, energy-efficient electro-optic chips across AI, data centers, and telecommunications, ELENA's achievement firmly positions the EU at the forefront of global photonics innovation.

The partners, which include leading European research institutes, large industrial companies and SMEs (short names in brackets), are:

- Swiss Center for Electronics and Microtechnology (CSEM), Switzerland;
- CEA-Leti (Leti), France;
- SOITEC SA (Soitec), France;
- VPIphotonics GmbH (VPI), Germany;
- Eidgenössische Technische Hochschule Zürich (ETHZ), Switzerland;
- Vanguard Automation GmbH (VA), Germany;
- Thales SA (THALES), France;
- III-V LAB (III-V LAB), France;
- Rosenberger Hochfrequenztechnik GmbH & Co. KG (ROS), Germany; and
- L-up SAS (LUP), France.

Artificial intelligence in multimodal microscopy workflows for failure analysis: from 3D imaging to automated defect detection

Examining how the wealth of interconnected data will fuel the development of AI-based predictive models, capable of forecasting not only the occurrence but also the timing and underlying causes of failures from their earliest symptoms.

BY FLAVIO COGNIGNI, PRODUCT AND APPLICATION SALES SPECIALIST XRM & MULTIMODAL MICROSCOPY AND HEIKO STEGMANN, FIB-SEM APPLICATION EXPERT AND ADVISOR, CARL ZEISS MICROSCOPY

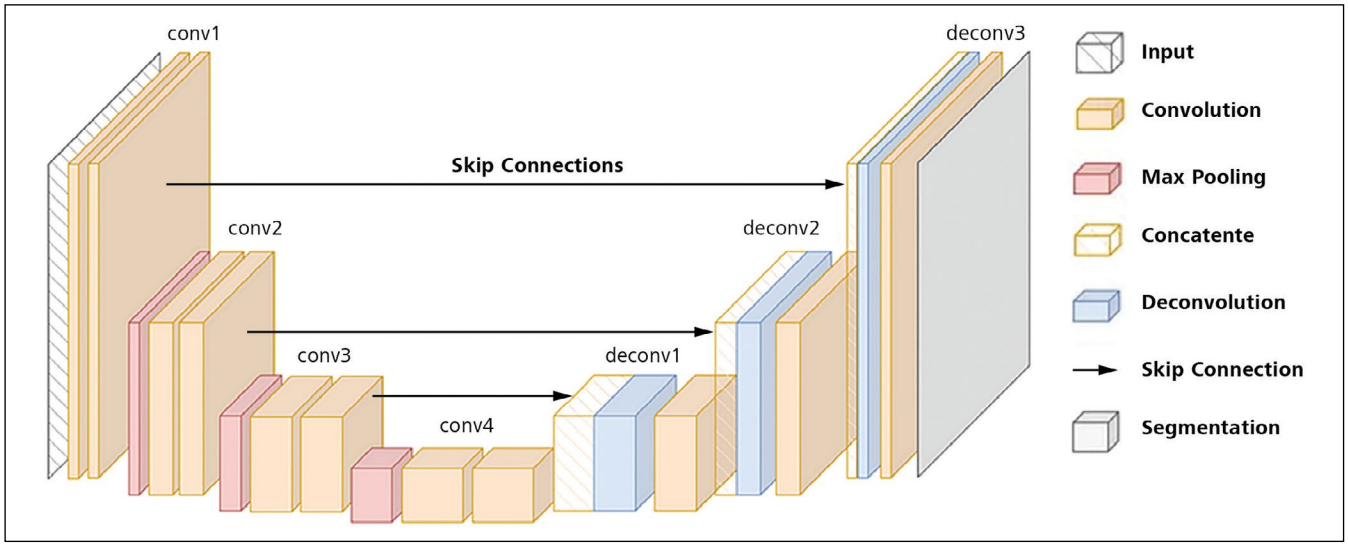
Evolution of imaging technologies and the need for artificial intelligence in failure analysis

In the fast-evolving world of electronics and semiconductors, image processing and analysis have become essential pillars of innovation, reshaping failure analysis workflows. As devices have grown more compact, complex, and densely integrated, the demand for three-dimensional (3D), high-resolution, and non-destructive imaging has increased exponentially.

Image processing and analysis constitute a distinct field of research and application, drawing upon contributions from multiple scientific disciplines such as computer science, physics, mathematics, and engineering.

The integration of knowledge from these areas has significantly advanced our capabilities in enhancing, interpreting, and extracting meaningful information from complex image datasets, thereby enabling breakthroughs across a wide range of technological and industrial domains. The increase in data volume, complexity, and dimensionality - particularly with the widespread adoption of 3D imaging and multimodal investigation workflows - has pushed traditional image analysis methods to their limits.

As a result, there is a growing need for smarter, more adaptive approaches capable of handling complex and large image datasets and automating repetitive analytical tasks.



➤ Figure 1. U-Net Explained: Understanding its Image Segmentation Architecture, author: Conor O'Sullivan.
link: https://medium.com/data-science/u-net-explained-understanding-its-image-segmentation-architecture-56e4842e313a

In this article, we explore how artificial intelligence (AI) is transforming the way image data is processed and analyzed in the context of failure analysis (FA) for electronics and semiconductors. We highlight the core benefits of AI-based approaches, examine practical applications, and discuss the future implications for research, quality assurance, and industrial reliability.

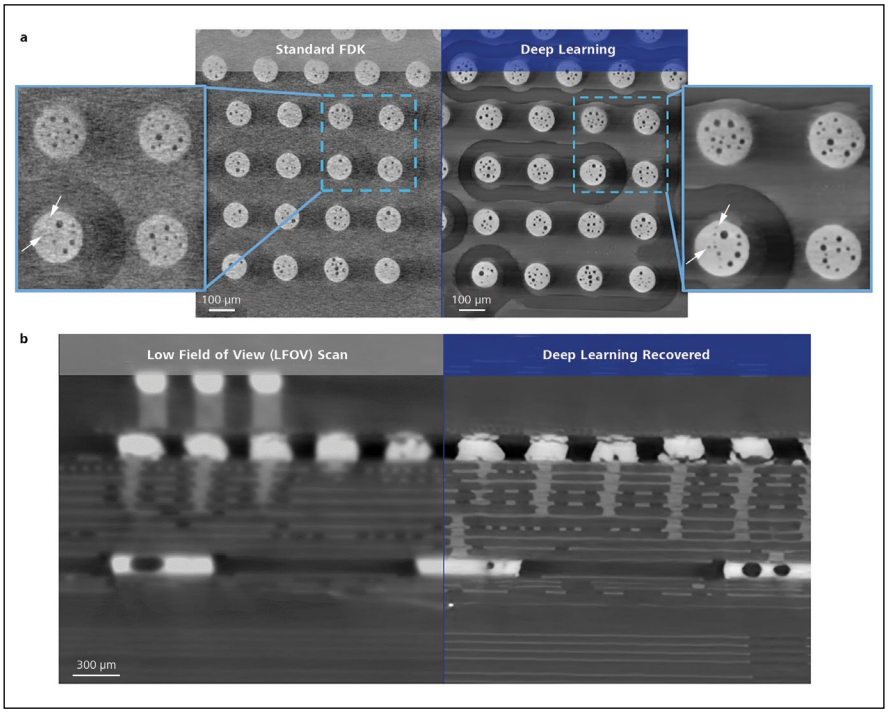
Fundamentals of AI, machine learning, and deep learning in image analysis

To understand advancements in AI applied to image processing and analysis, it is important to define key concepts. AI broadly refers to computer systems that mimic human intelligence. Machine learning (ML) is a subset of AI, where computers learn from data without explicit programming. Deep learning (DL), a further subset of ML, uses neural networks - interconnected layers of nodes inspired by brain neurons - to process information.

Among neural networks, convolutional neural networks (CNNs) are the most commonly used in image processing. The U-Net architecture is particularly prominent in the field of image segmentation and analysis, known for its high performance even with limited training data, mainly due to the presence of skip connections that help preserve spatial information during feature extraction and reconstruction (Figure 1).

Advancing image reconstruction with DL techniques

The growing need for smarter, more adaptive approaches to manage increasing complexity and dimensionality has paved the way for AI to become a powerful ally in FA. By learning from data and adapting to context, DL models can overcome hardware limitations in image quality and throughput - enhancing 3D reconstructions, enabling the detection of finer, more complex structures and hidden features, and significantly improving both the speed and accuracy of data acquisition and interpretation (Figure 2a). DL-based models have found wide application in the field of super-resolution, where AI is used to transfer the fine pixel size of a high-resolution XRM scan - characterized by a small field of view (FOV) - to a lower-resolution scan that captures a larger FOV [1] (Figure 2b).



➤ Figure 2. (a) Comparison between X-ray microscopy (XRM) datasets of a modern graphics card, reconstructed using the traditional Feldkamp-Davis-Kress (FDK) algorithm (left) and a DL algorithm (right). DL reconstruction reveals fine details that are not visible in the standard FDK reconstruction, as highlighted by the white arrows. (b) Application of a DL-based super-resolution model to transfer the fine pixel size of a high-resolution XRM scan (small FOV) onto a lower-resolution scan capturing a larger FOV [1].

AI-powered image segmentation and its impact on semiconductor FA

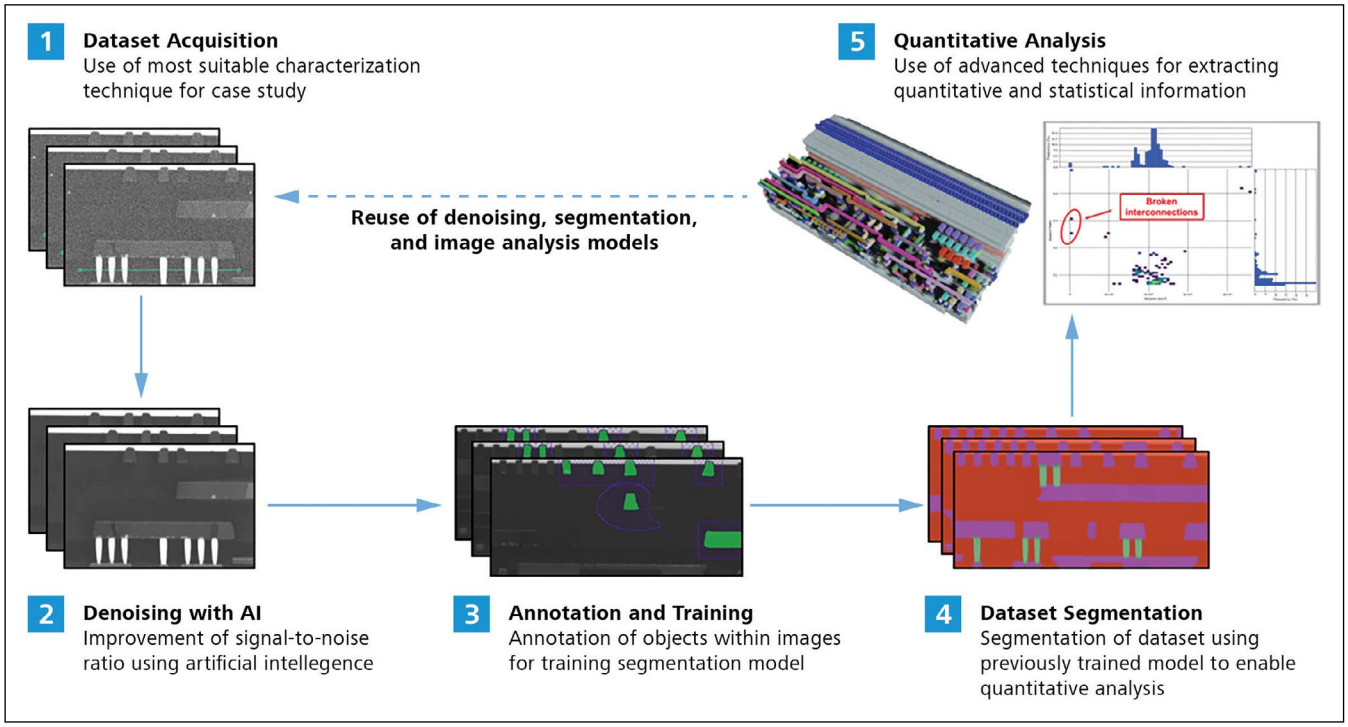
Following reconstruction and initial image processing - such as filtering - image segmentation plays a critical role as the first and fundamental step in the image analysis pipeline. It involves partitioning an image into meaningful regions or objects, such as interconnects, vias, cracks, voids, or delamination which are essential for identifying defects and understanding failure mechanisms. The schematic shown in Figure 3 illustrates a general example of an image processing and analysis workflow.

Accurate segmentation allows for precise localization and quantification of structural features, enabling analysts to focus on areas of interest and extract relevant measurements. Traditional segmentation methods, such as histogram-based thresholding, are simple and, in several applications, may be a suitable solution for accessing and revealing the desired information contained in the dataset. However, the features and characteristics, as well as both the image analysis purpose and tasks, of certain images can limit the efficacy of these methods.

Without effective segmentation, downstream tasks such as defect classification, statistical analysis, or 3D objects visualization may suffer from reduced accuracy or interpretability. As device architecture becomes increasingly complex and image datasets grow in size, dimensionality and complexity, advanced segmentation - particularly AI-powered - is becoming indispensable for enabling scalable, consistent and reproducible FA.

Overcoming computational barriers: Cloud-based training for DL models

Performing image segmentation with DL models has opened new opportunities in FA. This approach requires model training, which involves dataset annotation and significant computational effort. To be practical, training must be completed within minutes - or at most, a few hours - using a limited number of images, as extremely large training datasets and long training times hinder real-world application (Figure 4).

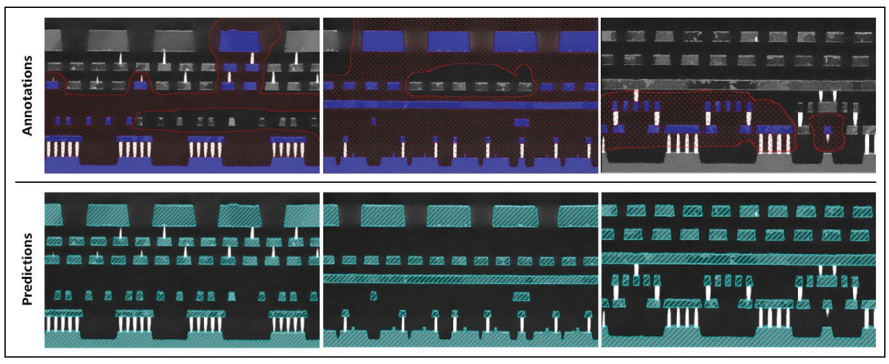


➤ Figure 3. AI-based workflow for image processing and analysis. The process includes dataset acquisition using the most appropriate characterization technique, AI-based denoising to enhance signal-to-noise ratio, object annotation for training segmentation models, automated dataset segmentation, and advanced quantitative analysis. Trained models can be reused for consistent and efficient analysis across similar datasets.

The training phase is the most resource-intensive step. While local computing resources, such as high-power workstations, are often constrained by hardware limitations - CPUs, GPUs, memory, and storage - resulting in long processing times and limited scalability, cloud computing offers a flexible alternative [2].

On-demand, pay-per-use platforms eliminate hardware barriers, provide elasticity to scale resources as needed, enable remote accessibility, and foster collaborative environments, all while reducing maintenance costs. These advantages make cloud solutions increasingly attractive for integrating DL into routine FA workflows.

Results reported in Figure 5 demonstrates how effectively DL models can segment noisy datasets - eliminating the need for extensive preprocessing - and images where different structures exhibit similar greyscale levels, making traditional methods such as histogram-based thresholding ineffective [3].



➤ Figure 4. Using modern cloud-based software solutions for annotation, training, and segmentation, the development of customized DL models becomes possible with only a limited number of annotated images and objects. For illustrative purposes, three representative images are shown in the figure [2].

Building automated multimodal pipelines with DL and Correlative Microscopy

The entire AI-powered image processing and analysis workflow can be automated within compact, integrated multimodal pipelines that combine data analysis functional units, code integration, and data storage into a single software environment, enabling complex analyses and routine operations.

For example, a Superjunction MOSFET was investigated by combining FIB-SEM tomography with 3D energy-dispersive X-ray spectroscopy (EDX), integrating nanoscale morphological information with elemental mapping. The two datasets were aligned, and their combination enabled the training of a DL model capable of segmenting the entire dataset, capturing both morphological and elemental features.

The case presented in [4] addressed a real-world industrial problem, demonstrating that this approach can automate the analysis of thousands of images from the same sample class (Figure 6).

AI algorithms can also be employed to reduce X-ray microscopy (XRM) scan time. Engineers have developed a multimodal characterization workflow that combines infrared imaging, multiscale XRM, and FIB-SEM tomography to investigate stealth laser dicing-induced defects in integrated radio frequency (RFID) devices [5].

In this study, a 10x reduction in scan time was achieved while preserving the quality of the dataset, as reported in Figure 7a. A DL segmentation model enabled the visualization of a color-coded network of metal layers within the device, as depicted in Figure 7b.

A second DL algorithm was used to guide and streamline the identification of potential defect site locations within the FIB-SEM tomography dataset volumes of interest (VOIs). Engineers observed that defects could manifest as low discharge between poly stripes and were often accompanied by small holes or voids within the first metal layer.

After two training cycles, the model demonstrated its ability to precisely identify these voids and holes, which may indicate the potential presence of a root cause of failure. Results are reported in Figure 7c,d.

The role of data management systems and AI in the connected laboratory of the future

As FA laboratories evolve, the implementation of robust data management systems (DMS) becomes critical for handling the large amount of data generated by multimodal characterization platforms. A DMS provides centralized storage, organization, and accessibility, enabling integration with AI-powered image processing and analysis workflows.

In the connected laboratory of the future, where instruments operate remotely and collaboration extends beyond physical boundaries, DMS platforms combined with multimodal microscopy and AI technologies will be essential.

They ensure efficient data management, support FAIR principles - at least within their own organizations - and accelerate the training of AI models for automated defect detection, thereby enhancing throughput, reproducibility, and innovation across semiconductor and electronics failure analysis [6].

Looking ahead, we foresee that the wealth of interconnected data will fuel the development of AI-based predictive models, capable of forecasting not only the occurrence but also the timing and underlying causes of failures from their earliest symptoms. By dramatically reducing time-to-result and empowering us to design more resilient and intelligent devices, these advances will open a new chapter for humankind - one where our technologies harmonize with the delicate systems of our world, propelling us forward while carefully minimizing our footprint on the Earth.

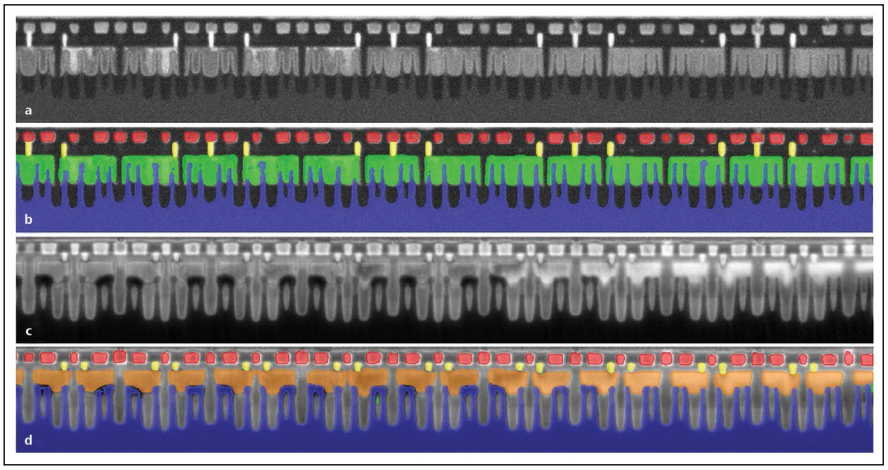


Figure 5. 2.45 x 0.29 µm² sections of a (a) BSE and a (c) SE images with their respective (b, d) segmentation with the following color codes – blue: fins, green: gates, orange: SD, yellow: contacts, red: M1 [3].

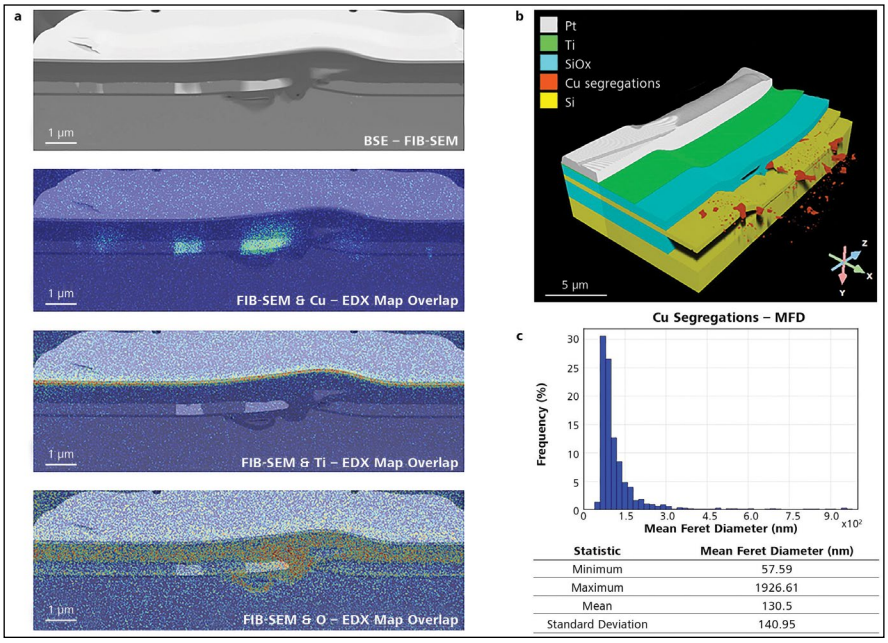
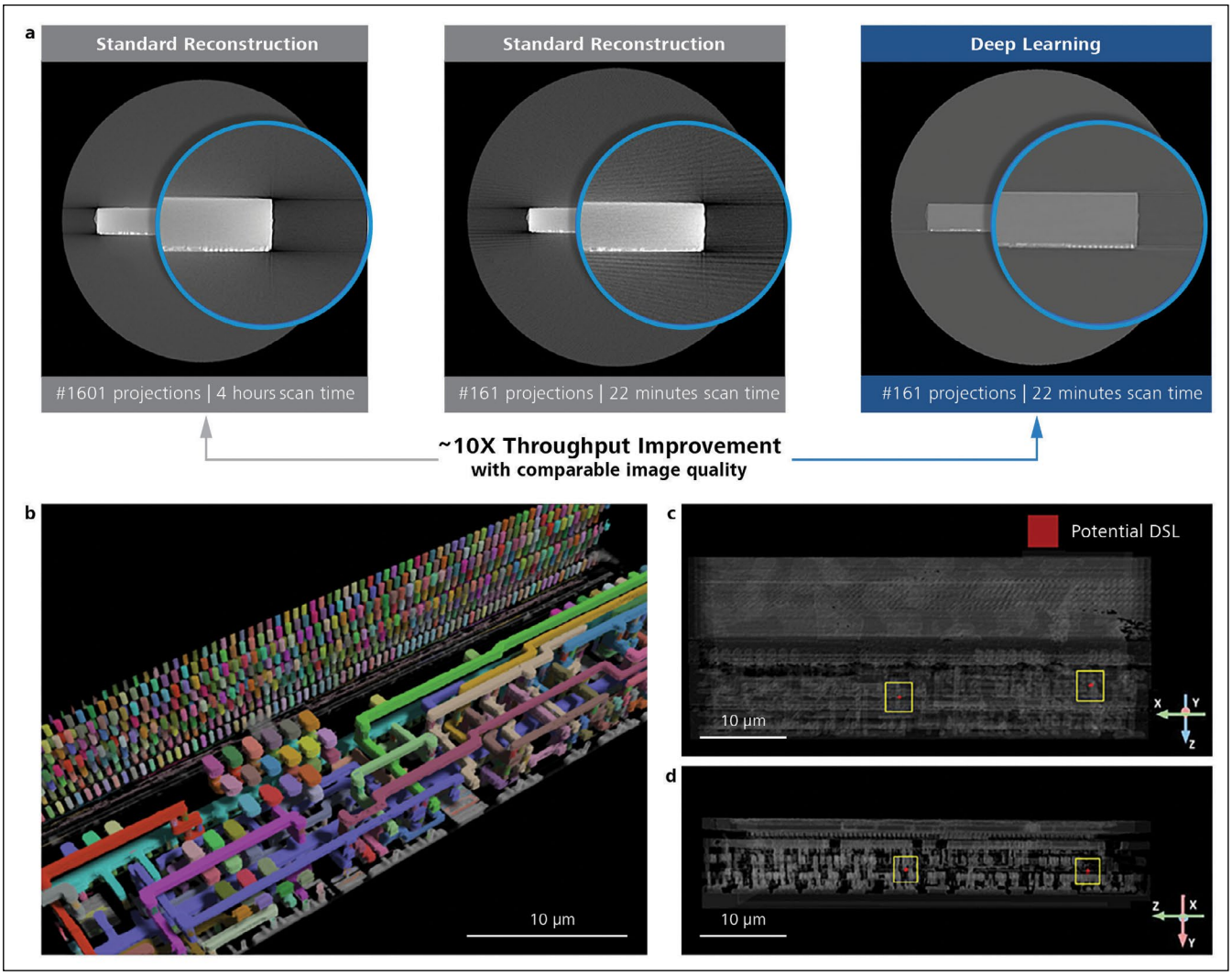


Figure 6. Example of an AI-powered integrated workflow for failure analysis. A Superjunction MOSFET was analyzed by combining FIB-SEM tomography and 3D EDX, enabling the alignment of morphological and elemental datasets. A DL model was trained on the combined data to segment structures based on both morphology and composition, allowing automated analysis across thousands of images from the same sample class. This approach demonstrates the power of multimodal data integration in real-world industrial applications [4].



➤ Figure 7 – (a) The reconstruction obtained using a DL reconstruction algorithm (right) allowed failure analyst to obtain XRM datasets in ~ 20 minutes, whilst the standard FDK reconstruction (left) required ~ 4 hours scan time. The standard FDK reconstruction (middle), obtained acquiring 161 projections, shows the typical radial artifact lines related to missing angle information. These artifacts are avoided using DL, while maintaining 161 projections, i.e., reducing the scan time by a factor of 10 [5].

For More Information
ZEISS Microscopy: www.zeiss.com/ai-multimodal-workflows

FURTHER READING / REFERENCE

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➤ **[2]** Carl Zeiss Microscopy, «ZEISS arivis Cloud Software,» [Online]. Available: https://www.zeiss.com/microscopy/en/products/software/arivis-cloud-ai.html

➤ **[3]** H. Stegmann e F. Cognigni, «Few-Shot AI Segmentation of Semiconductor Device FIB-SEM Tomography Data,» in ISTFA 2024: Conference Proceedings from the 50th International Symposium for Testing and Failure Analysis, San Diego, California, USA, 2024.

➤ [4] F. Cognigni, M. Rossi, H. Stegmann, G. Sciuto, G. Anastasi, M. Astuto, M. Bonadonna e D. Mello, «A Multiscale and Multimodal Correlative Microscopy Workflow to Characterize Copper Segregations Identified in Epitaxial Layer of Power MOSFETs,» in ISTFA 2023: Conference Proceedings from the 49th International Symposium for Testing and Failure Analysis, Phoenix, Arizona, USA, 2023.

➤ [5] F. Cognigni, G. Lamedica, D. Mello, P. Von Gunten, G. Fiannaca, H. Stegmann, A. du Plessis e M. Rossi, «Integrating Multimodal Microscopy and Artificial Intelligence Solutions for Laser Dicing Process Induced Defect Identification,» in ISTFA 2024: Conference Proceedings from the 50th International Symposium for Testing and Failure Analysis, San Diego, California, USA, 2024.

➤ [6] Carl Zeiss Microscopy, «ZEISS arivis Hub,» 2025. [Online]. Available: https://www.zeiss.com/microscopy/en/products/software/arivis-hub.html

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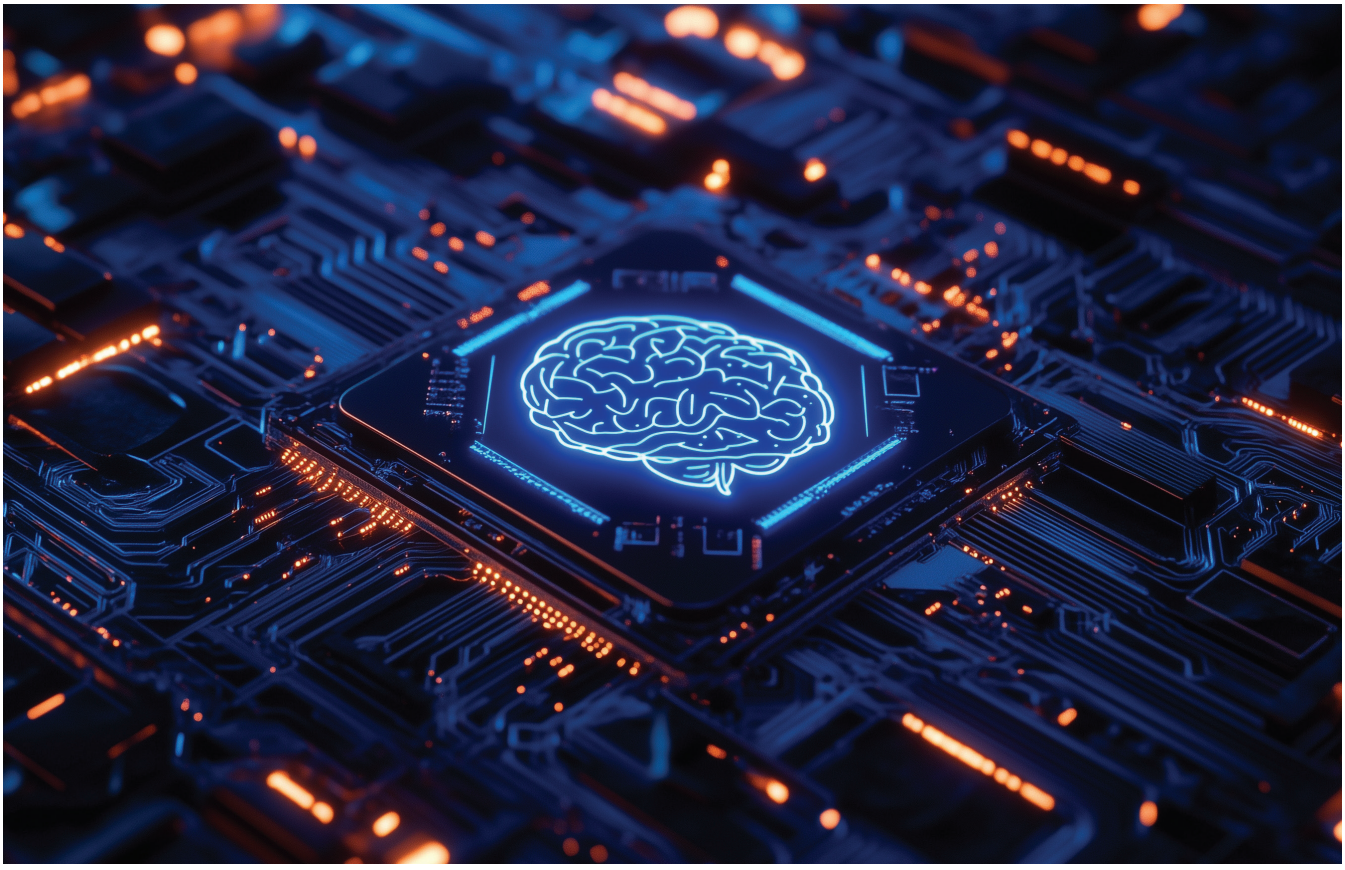
FlexTech

FOA Fab Owners Alliance

MEMS & SENSORS INDUSTRY GROUP®

SOI Industry Consortium



Building trust in GenAI for semiconductor design with IP lifecycle management

While Generative AI (GenAI) technologies are already transforming software development and have great potential to improve semiconductor design, their adoption in this industry remains hindered by the challenges around protecting highly sensitive intellectual property (IP), the vast costs associated with errors, and the critical need to manage data provenance and liability.

BY VISHAL MOONDHRA, VP OF SOLUTIONS ENGINEERING, PERFORCE.

THE POTENTIAL benefits of GenAI to accelerate and drive new efficiencies in semiconductor design means that there is a growing demand for these barriers and challenges to be overcome.

There is a critical need to create a solid strategy that protects IP while still enabling teams to use AI. One pillar that is being examined is to include IP lifecycle management (IPLM) processes — already part of many semiconductor design teams' ways of working — to ensure better control and traceability around how data is used to train GenAI models.

Benefits and risks of GenAI in semiconductors

To understand how that can work in practice, it helps to have some more context around the benefits and risks.

When applied appropriately, GenAI can contribute to accelerated design cycles, improved design quality, enhanced validation and verification, simplified IP reuse, and increased capacity for experimentation and innovation, as well as collaboration and knowledge sharing. GenAI can provide teams with a significant head start, helping them overcome the limitations of human time and experience. For instance, currently, understanding and debugging errors is a time- and labour-intensive process.

With effective use of AI, engineers could receive guidance about the source or reason for the error, as well as suggestions around how others have tackled similar issues. Another example could be having an AI agent look for the best IP or design block to satisfy a particular aspect of a design project, again saving the design team time and effort. However, the advantages must be carefully balanced against the challenges and risks:

- **Liability –** pertaining to IP ownership and licensing of data used for training. If GenAI models are trained on proprietary or third-party data without proper controls, sensitive IP could be leaked via the outputs generated by AI. Given the massive investments that IP vendors have made in creating and selling their designs, control over their use – including preventing third parties from using that data to train AI models or having it used in unauthorised locations — is of paramount importance.
- **Lack of traceability, data quality concerns –** it can be complicated to trace exactly how an AI model was trained. Yet traceability is essential to ensuring that the model is reproducible and that all data used in training is fully vetted for IP quality and maturity. If organizations don't fully understand exactly what data and IP versions have been used to train the model, debugging becomes nearly impossible.
- **High stakes –** the cost and potential time delays resulting from errors can be ruinous. In the domain of software applications, errors and problems, while challenging, have reasonable recovery mechanisms. However, in the semiconductor domain, the situation becomes much harder. The later an issue is detected, the more expensive it is to fix. Mistakes that reach tapeout can run into millions of dollars to address. This massive financial risk is one of the primary reasons the semiconductor industry has been slow to adopt generative AI techniques. A badly trained model, with unknown provenance of the training data set, can easily lead to generating designs that are unviable, hard to verify or otherwise error prone.

Therefore, having complete control over the process to know what and how data is being used for training, including its full provenance, has to be the foundation of any semiconductor design project involving GenAI. Semiconductor leaders who are tasked with incorporating GenAI into the design workflow must establish firm guardrails for the data used to train internal models in order to achieve the level of trust required to open the door to AI adoption, move forward, and reap the benefits of AI. Trust is the bedrock of AI adoption.

To establish trust in using AI to train internal models, it is critical to have the following:

- Clear and auditable data provenance for all training datasets
- Complete traceability of all IPs and IP versions
- Secure and compliant use of both internal and external IP.

Breaking designs into blocks

So, how do we ensure that teams do not use the wrong data — or use it incorrectly – to train their AI models? The starting point is to segment designs into a set of individual, manageable IPs or blocks. IP lifecycle management (IPLM) techniques and tools can then be utilized to manage the lifecycle of the individual IPs.

By breaking a design into individual IPs, organisations can train AI models with specific, known, vetted and trusted blocks, as opposed to an opaque, monolithic design that may contain unauthorized, poor quality, or otherwise inappropriate IP.

Increasingly deployed within the semiconductor business, IPLM follows data IP from acquisition or development through to qualification, distribution, and integration into design. IPLM makes it easier to see where each specific IP version has been used across all projects, as well as any outstanding bugs, derivative designs, and the status of verification. Fine-grained permissions can ensure that only IPs that has been authorised for use in AI models are available to include in model training, while geofencing protects IP from being used in an unauthorised country, even if user permission has been granted.

This end-to-end visibility, traceability, and IP security provides the control and transparency required to establish a trusted foundation for AI use in semiconductor design.

Ensuring data provenance and quality

With this comprehensive control and traceability, IPLM can also provide data provenance for AI training datasets. Data provenance is critical to ensuring full auditability of all designs. With IPLM, provenance can be established down to the IP version level, as well as for all associated metadata and even the design environment, ensuring that every possible variable contributing to the AI model is known, tracked, and auditable. Data can be modelled as a series of parent-child relationships to understand IP lineage, including the project(s) from which data was derived or copied.

Rules can be applied and enforced regarding the types of IP that can be used, as well as their source, to guard against contamination of the dataset and keep unauthorised IP from being incorporated into the training data. Rules can also be established to ensure certain standards for IP quality and maturity, as defined by organisations, are met before any data is used for AI training.

Consequently, semiconductor organisations can effectively build trust into their GenAI model training process, with the confidence to experiment and innovate more efficiently and safely. Furthermore, incremental training becomes possible, allowing users to see exactly what has changed since the last training set.

Training an AI model is a continuous process, not a one-time step. Users need to know: what happened in the past? How was that point reached? What is new, and what can be repeated?

These are all ways in which semiconductor teams can minimise the risks around AI use in semiconductor design while reaping the benefits. While the semiconductor industry has been cautious compared to others in its adoption to date of AI for design, the highly competitive nature of the semiconductor industry will soon force companies to move forward with AI to avoid falling behind, and organisations must be prepared.

Using IPLM helps establish and manage clear guardrails for safe, secure use of AI for semiconductor design teams. With AI's widespread adoption inevitable, now is the time to create the right foundations to safeguard IP, mitigate business risks, stay competitive, and be ready for AI's continued evolution.

Material science innovations for advanced packaging applications

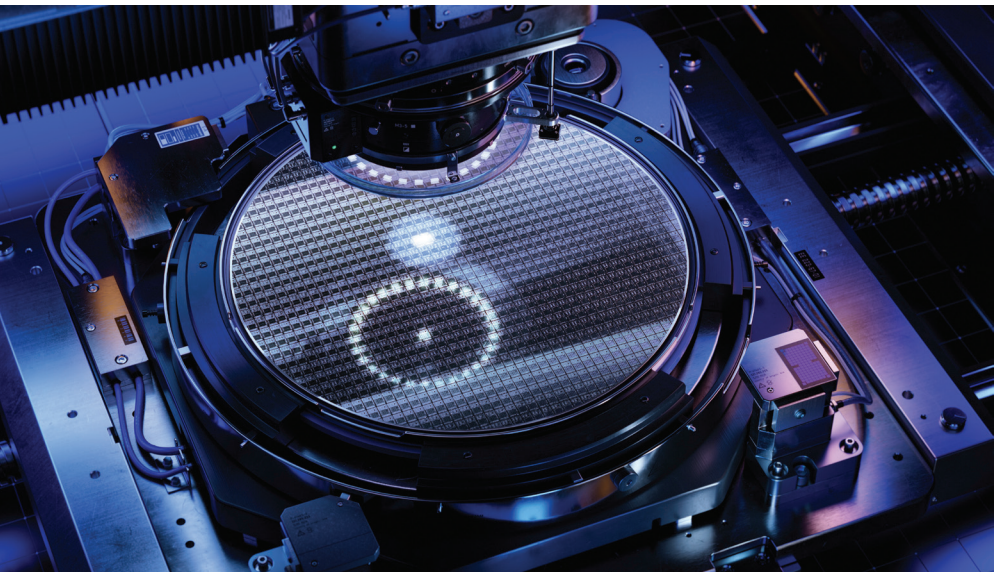
Wayne Rickard, Terecircuits CEO, outlines the company's decision to join the US's National Semiconductor Technology Center, contributing its considerable expertise in the synthesis, characterization and delivery of polymers, encapsulants and thin film coatings for advanced packaging. Wayne explains that, in working alongside industry leaders across the U.S. semiconductor ecosystem, Terecircuits can accelerate the development of advanced material solutions for heterogeneous integration and, in so doing, is helping to tackle critical challenges in high-density, high-performance chip manufacturing.

SIS: *It would be great if we can start with a little bit of background, a brief introduction to the company?*

WR:
Sure. Terecircuits was actually founded by Dr. Jaina Sheets, and we got our first funding in 2019. She was driven by the vision that, eventually, advanced packaging would become a driver of advancements in semiconductor manufacturing and processing to complement Moore's Law, and that when that happened, it would require new materials as well. As a physical chemist with a background of 20 years at HP Labs and a background in photolithography, Jaina was uniquely qualified to understand how that market might emerge.

SIS: *You've recently joined the National Semiconductor Technology Centre (NSTC). It would be good to understand a bit about why joining is important, the benefits you expect to get and also what you will contribute?*

WR: The National Semiconductor Technology Centre is an opportunity for a small company like us. As I mentioned, we're a startup. We have less than a dozen employees. In material science, you're only a small part of a larger ecosystem. Obviously, advanced packaging involves tool makers, it involves the ODMs, it involves the OSATs. Every part of the supply chain, every part of the interrelated infrastructure that's required to build a semiconductor has unique requirements. Without having the ability to go out and buy and purchase the entire tool chain that you need to build a semiconductor, having something like this technology centre gives us the opportunity to interact with our peers and with the people that own and control the upstream and downstream processes, which is critically important as a material provider.



Then a secondary benefit is it's very expensive as a material company to go out and qualify our material in different environments. Again, this brings everybody together under one roof where we can all interrelate and work on some of the problems the industry is facing together.

SIS: *in terms of the technology portfolio you've got, I think that the sweet spot is around polymer chemistry. there's a product solution called Terefilm and other things you do – please would you give us a bit more detail?*

WR: Terefilm is a unique material. It combines some of the qualities of a temporary bonding and debonding,

adhesive with the patternability of photolithography.

This is a very unique combination of characteristics. In temporary bonding and debonding, where you're connecting two wafers together or chips to wafers, you have a release process that acts on the entire surface area of the bonding material. And that means it's either bonded or it's debonded. With lithography, though, you're able to pattern an individual component. In the lithography, obviously, when we fabricate semiconductors, we're doing that down at the nanoscale. But what we envisioned was a process where you could use a temporary bonding, debonding adhesive, and then pattern individual components that are being held by that adhesive, and then release them in a controlled way. And what that lets us do are some very unique things. It lets us handle material for one that is very, very small. So one example is micro-LEDs, which can be about the size of a grain of pollen. Very difficult for a pick-and-place tool, you can imagine, or something with a vacuum head to pick up something on the scale of a red blood cell.

But we can do that with our material. We can pick up an entire EPI wafer of components, and then we can target the ones we want to release. Just using a little bit of light and heating, we can target the ones that we want to release and place them on a substrate. This gives us the ability to handle things that are very small, but we can also handle components that are very fragile. An example might be something like silicon carbide or gallium nitride.

These materials are much more brittle than silicon, and conventional handling techniques can actually damage them. Our material can hold these components securely and then release them accurately at the point that you want to place them on a substrate. And then the final use case is for materials that are also very fragile, like a thin silicon wafer. When it's silicon, the silicon is normally pretty rigid and easy to handle, but when it's thinned down to under 50 microns, now it becomes much more fragile and difficult to handle. Again, our material can act as a temporary bonding, debonding adhesive and hold that material securely until you're ready to release it and place it.

"Terefilm is a unique material. It combines some of the qualities of a temporary bonding and debonding adhesive with the patternability of photolithography. This is a very unique combination of characteristics. In temporary bonding and debonding, where you're connecting two wafers together or chips to wafers, you have a release process that acts on the entire surface area of the bonding material"

SIS: *In terms of where you are, is that solution readily available for partners and others? Or is it still in test phase? What's going on there?*

WR: We're sampling the material today. We have several partners that are evaluating the material for all three of the use cases I just mentioned, micro-LEDs for advanced display fabrication, for silicon carbide handling for die attach, and for thin wafer handling. All those use cases are actually being applied at various partners today. We also partner with tool companies. We're, as I said earlier, a material company, so our expertise is in the polymer chemistry side of the equation. We still need to work with tool partners in the case of micro-LED placement, for example, that requires a laser placement tool. There are several companies that are involved in the development of these tools, and we work with them.

SIS: *You also have expertise and innovation around lithography and process engineering. Is this 'incidental' to your main expertise, polymer chemistry, or are those separate major focuses or only in so far as they impact on the polymer chemistry that's your sweet spot?*

WR: That's a good question. These are very complementary skill sets to have. If you develop advanced materials, particularly for advanced packaging, which is a fast evolving sector in semiconductor manufacturing, you need to have exposure to the complementary skills that are involved in bringing that material to market. For example, I mentioned that to pattern our material, you need to have a tool very much like a lithography tool. For us to even demonstrate our material, we've had to develop expertise in optics and in fine positioning systems. This requires some mechanical engineering expertise. This is not to say that we want to be in the tool business, but to attract the tool companies to what our process is capable of, we need to demonstrate the material. We've actually built lab-scale tools that can do everything I've described, place components with micron accuracy on a substrate and release individual components with one micron between them. This is the type of thing that if you don't see it demonstrated, it's difficult to believe it's even possible. Again, process engineering skills, lithography skills, and skills in optics and lasers are all complementary skills we've had to develop.

SIS: *Without labouring the point, bearing in mind this expertise you have developed, is this something you think might turn into an opportunity - whether you just licence someone to produce these tools or is it just a means to an end, and once the polymer chemistries and Terefilms out there, you will no longer have a need to develop these tools?*

WR: That's a good question. I think from our standpoint, we want to enable as many tool vendors as possible to use a material like ours. It's good for the industry, and each of the verticals that I've described is probably going to have some nuance in the tool design. If you've ever talked to a tool vendor, in a perfect world, they'd build one tool and it would work for everybody. But the reality is there's a nuance to every deployment that requires the tool to be tweaked a little bit and optimised for the individual process flow. By working with a lot of tool vendors and helping them tune in their process with

whatever the process parameters are that need to be adjusted, we can attack multiple verticals in parallel. The tool vendor partner for display technology is going to be very different than the tool vendor that's focused on power semiconductors.

SIS: *You've referenced a couple of times advanced packaging, which is the end goal. As you said, it's fast moving. Your thoughts more generally as to the challenges and opportunities in terms of where you're at and the potential you see for yourselves within this exciting area would be great to understand?*

WR: Advanced packaging is indeed a fast moving, fast evolving area. And today, at the very peak of what's capable in advanced packaging, it's dominated by the large companies like Samsung and TSMC who have internal processes. Intel has a process. But to really get advanced packaging into the mainstream so that it can be adopted by the OSATs and so that we can drive the advanced packaging techniques down into the mainstream of semiconductor manufacturing for standard components, not just for the latest GPU from NVIDIA - this is something that's going to require a lot of process optimisation. It's going to require a lot of new materials.

It's also going to require us to reimagine and reinvent some of the ways we assemble semiconductors today. When you think of advanced packaging, in the past, packaging involved one die on a substrate, wire bonded to a lead frame and encapsulated. Today, advanced packaging involves tens, or in some cases, hundreds - in the case of a micro-LED panel, millions of components that need to be assembled in some type of a larger assembly. This can involve things like co-packaged optics. It can involve thin film batteries, passives, different process nodes.

The latest process node that you use for the GPU, for example, is not the same process node that's required for the memory. And that means that you've shifted from a problem that has been largely solved by integrating on a monolithic chip. Now you're distributing that problem across multiple different components. Of course, one of innovations is chiplets, which are small building blocks that can be used to build more complex assemblies. But again, chiplets also create a packaging challenge because they have to be placed on a substrate with high accuracy, in some cases, very close to each other, in some cases, even stacked in the third dimension.

All of these challenges involve... and when we think about the tools we have to do that, we really have pick-and-place tools, which, as I mentioned earlier, get increasingly challenged as components get small, thin, and fragile. And you have flip-chip die bonders, this is a tool that does things one at a time, or maybe five or six at a time on a multi-head tool. This does not give you the throughput and the yield that is required to go from where you can afford to pay for very expensive tools to something that can be acquired by an OSAT.

SIS: *In terms of the NSTC, you've explained the benefits of being part of a bigger collaborative organisation. Is this so important to you? The organisation's goals include the US's semiconductor industry, developing that and reducing the time from lab to fab. I guess what you've explained there, you've very much committed to that. But just in terms of the US semiconductor industry, are you keen to help that or do you regard yourself as part of the global semiconductor industry, if you like?*

WR: I think we're part of both. The challenges that the global industry is facing, the ones I mentioned about advanced packaging are common to the entire industry. As far as the US is concerned, the challenge the US has is, again, this push for independence of the supply chain is a consequence of increased specialisation across geographies. For example, the EDA tools and the design of semiconductors, this expertise is in the US. But when you get to lithography tools, some of the more advanced tools that are used in the process of manufacturing, Europe has a lot of the competency there.

Advanced materials, the competency is in Japan. And of course, packaging and assembly has traditionally been in Southeast Asia. This dispersion of competencies is something that makes the entire semiconductor industry more interdenpendent. I think what COVID taught us was that when supply chains are disrupted, you end up with a situation where for the lack of a semiconductor in a radio, you can't build a car. And that really was a wake-up call for the industry to say we need, if not complete reshoring, we need less interdependence.

We also need to move some of our supply chain dependencies from regions that may be more impacted, either by geopolitical situations or by supply chain disruptions like COVID, to something where we're less dependent on single points of failure.

That's part of what the National Semiconductor Technology Centre is trying to do for the US, which is flatten the supply chain a little bit through this type of reshoring and bringing some industries that have traditionally been located in other geographies back into the US.

SIS: *I was going to ask you about what I always call the three Ss. You've talked about the supply chain, but we've got skills, which everyone says there aren't enough people to go around and it's*

> "I think from our standpoint, we want to enable as many tool vendors as possible to use a material like ours. It's good for the industry, and each of the verticals that I've described is probably going to have some nuance in the tool design. If you've ever talked to a tool vendor, in a perfect world, they'd build one tool and it would work for everybody. But the reality is there's a nuance to every deployment that requires the tool to be tweaked a little bit and optimised for the individual process flow"

going to get worse. But as I always say, I don't see anyone break into a sweat about it, but, potentially, it sounds like quite a large problem. Then there's sustainability. There's maybe a bit of pushback at the moment geopolitically, but I think the industry is, to a certain extent, on a path towards sustainability anyway. It would be good to have your thoughts as to these challenges?

WR: Skills and workforce development is something that comes up all the time - when you have allowed some core competency to go to a geography where they've developed the expertise over the last couple of decades, and you've allowed that skill set to atrophy domestically.

Now you find, if you really want to do some level of reshoring, that you don't have the skilled workforce that's required. It may be that it's experiential because you haven't been doing manufacturing in the US, or it may be that you don't have the educational discipline in the institutions to do the type of job on preparing people for entering in the semiconductor field.

I see that changing a lot. Almost all the major organisations, like SEMI and even the individual companies that are involved in semiconductor manufacturing have workforce development programmes right now, outreach to universities, certificate programmes. It's becoming something that, while I think it will continue to be a problem for a while as you try to bring resources to different regions that don't have the base established, it's something that the industry is addressing.

A good example is TSMC building fabs in Arizona. One of their critical concerns was, would we be able to find a skilled enough workforce outside of Taiwan to actually run them?
There were some fits and starts, but I think the evidence now is pointing to the fact that it is possible to build a skilled workforce in a region that hasn't traditionally been part of the industry.

WR: Sustainability is something I think one of the areas that always comes up. I'm here in Arizona, and we always are asked about, what about if the centre of gravity for the US semiconductor industry is moving to Arizona, what about water? What you've seen in companies, I think Intel is a great example, is the ability to recycle a lot of the water that's used in the semiconductor process so that you really aren't using a lot of water.

You're not consuming a lot of water, you're reusing a lot of water. That's a big development in sustainability in the processing of manufacturer's semiconductors. This has happened in the last decade.

The other thing to remember about sustainability is that we're moving to an era where this is the electrification era, where we're looking at things like electrical vehicles, we're looking at non-traditional sources of power like solar and wind power. All these sources of energy that will generate and consume electricity, they're going to benefit from the transition from silicon to power semiconductors like silicon carbide and gallium nitride. I've seen statistics that say just by using silicon carbide in an electrical vehicle drivetrain instead of silicon for power conversion, you can get a 7% improvement in range in that electrical vehicle.

Because silicon carbide is more efficient, you'll also get a lighter powertrain, which also adds to the efficiency. You'll be able to eventually use higher voltages for charging stations. Power semiconductors will enable you to charge an electrical vehicle in the same amount of time it takes to fill a tank of gas, which is one of the last barriers to electrical vehicle adoption. All of this will drive less dependence on fossil fuels and more reliance on cleaner and more efficient sources of energy. A lot of that's enabled by these new advances in semiconductors.

SIS: *In terms of the industry's future, obviously, we live in uncertain times, shall we say. In terms of the reshoring*

and the more insular approach that different countries, regions are taking, do you think that is going to damage the industry to a worrying extent, or is it something the industry can adjust to? Because as you explained eloquently a few minutes ago, each region of the globe has expertise in certain areas, and altogether, as a global industry, it's fantastic. If each country or region has to start becoming more self-sufficient for that whole supply chain, there might be opportunities, but also challenges?

WR: Right. You mentioned the three S's, and I think there's also the three R's, which are resiliency, which we talked about, reshoring, which we talked about, and R&D, which is the third leg, which is where we've all fallen behind is in area. My company is a great example. The US is not really known for having a centre of competency in advanced materials for semiconductors. That's largely concentrated in Japan.

As we focus on closing the gaps that we have domestically, whether it's materials or whether it's packaging and assembly, as we focus on closing those gaps, and as other regions like Europe, and they have their own version of the Chips Act, as they focus on closing their own gaps and get better at chip design and EDA tools, we all end up becoming more competent, we become more competitive globally.

The fact is that we're never going to be 100% completely onshore. The supply chains are too interrelated and too complicated. The best we can do is hope to have strong partnerships with aligned communities of interest to avoid some of the geopolitical stress. But once we've done that, the fact that we've all tried to close these gaps in our own ability means that we're all stronger together.

I think that's a very positive sign for the future the industry.

SIS: *Maybe just finally, in terms of the company, Terecircuits, anything you can share on the company's roadmap?*

WR: Sure. Well, of course, Terefilm is our flagship product, and it has use cases across many aspects of advanced packaging assembly for precision placement and as a way to replace in some extreme cases what we can't do with pick-and-place tools.

There's lots of work still to do building up that product category and bringing more tool players into that world.

For Terecircuits beyond that, we have an IP portfolio that's fairly deep, and it includes other materials like encapsulants. We're doing some work with materials that have a negative coefficient of thermal expansion.

By using those as doping agents in traditional encapsulants and underfills, you can actually make a material that has better heat transfer characteristics because now you're not needing to load it with as much silica.

This is an area of investigation for us. We also are doing works with photoimageable masks, we're doing this with liquid metal amalgams. We have quite a dense portfolio of IP that we haven't even begun to exploit yet. Our plate is quite full with the one material that we're taking to market now!

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Scaling quantum

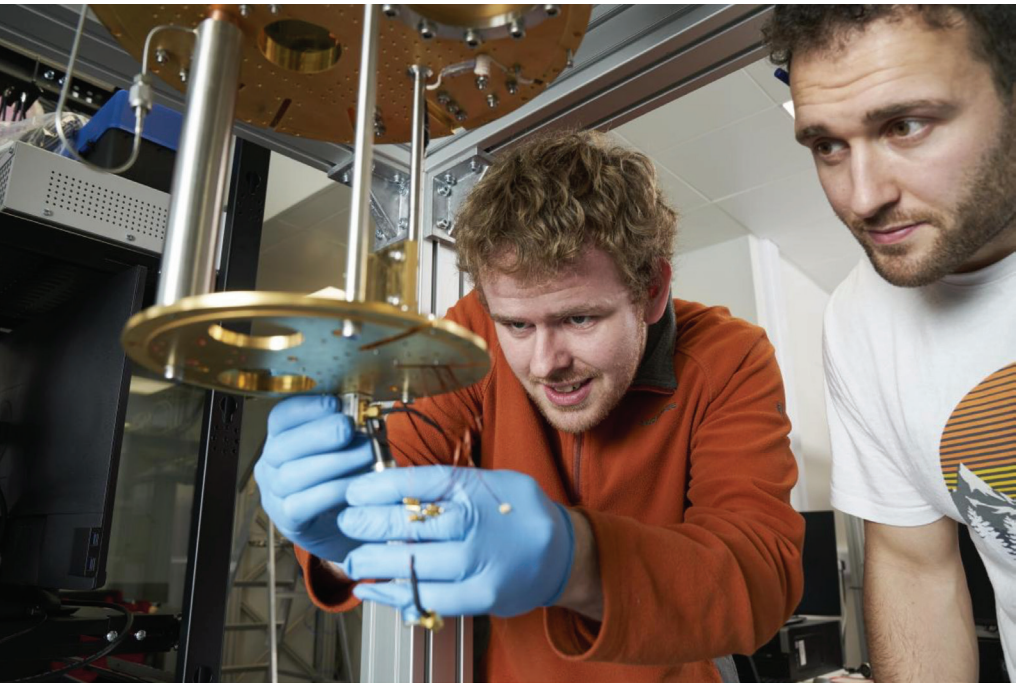
How Cryo-CMOS blueprints bridge the gap to scalable quantum computers.

BY RAY SPITS, COLLABORATION PROGRAMMES MANAGER AT OXFORD INSTRUMENTS NANOSCIENCE, PAUL WELLS, CEO AT SURECORE AND MARTIN WEIDES, PROFESSOR OF QUANTUM TECHNOLOGIES AT UNIVERSITY OF GLASGOW

LEADERS from industries all over the world are discussing the transformative benefits that quantum computers could deliver. There are multiple candidates for scalable quantum computing platforms, based on different qubit ("quantum bit") modalities. Solid state devices such as superconducting and spin qubits are attractive due to their overlap with well-understood and well-controlled semiconductor fabrication processes.

However, in constructing a quantum computer using ultra-low temperature solid-state qubits, it is not only the qubits that need to operate in such incredibly low temperature environments, but control and interface components also need to work in this regime.
The electronic control that we use in classical computing today operates at room temperature, in stark comparison to the extremely cold cryogenic environment of a quantum processor. Most quantum computing controllers currently sit outside that cryogenic environment. The aim of many university and industry researchers is to bring this control closer to the processor to increase speed and reduce electronic noise.

Enter: Cryo-CMOS, or Cryogenic Complementary Metal-Oxide-Semiconductors.



The Cryo-CMOS solution

CMOS process technology has been the bedrock of the semiconductor industry for over 30 years. It has enabled the transformative power of Moore's Law to revolutionise the modern world. CMOS typically operates between -40 °C and 125 °C which covers the vast majority of electronic products sold on the market today. By measuring and understanding how CMOS performance changes when temperatures are reduced into the cryogenic realm, a whole new design capability was discovered. In doing so the term 'Cryo-CMOS' was coined to characterise these specialist electronic circuits that can be designed to work at very low temperatures. Not only can Cryo-CMOS circuits survive the cold, but they also reduce the complex and bulky cabling currently used to connect quantum computer components. This is a way that we may be able to scale quantum computers more effectively.

One programme helping to facilitate the development of these essential components is an Innovate UK-funded consortium, led by sureCore with the support of Oxford Instruments NanoScience and the University of Glasgow among others.

Can you explain the Cryo-CMOS project? What is its goal?

To develop modern chips, designers need access to a range of key predesigned functions. These include logic gates, flip-flops and memories – the essential building blocks of any digital chip - as well as more specialist blocks.

Such blocks are only available for the standard operating temperature ranges. To be useful in the cryogenic quantum space, Cryo-CMOS is needed so that control chips can be designed for these harsh environments.

To help address this, the Innovate UK project developed the low-level transistor simulation models needed

to create the key building blocks. The project then created a range of cryogenic building blocks that will now facilitate the design of advanced cryogenic control chips, addressing a critical challenge in quantum computing: efficient qubit and system scaling.

The project kicked off in early 2021 and has run for 36 months, during which our primary goal was to develop cryogenic transistor simulation models (so called SPICE models) for silicon-based CMOS circuits that can operate at ultra-low temperatures. These models were then used to develop a range of key building blocks, essentially a comprehensive "toolbox" for semiconductor chip designers to help enable them to design integrated circuits.

The transistor models and the building blocks we have created will enable the design of control chips capable of qubit manipulation, data readout, and efficient data storage and processing at extremely low temperatures. This will in turn accelerate quantum computing development by making designing electronics for the cryogenic space easier and eliminating the need for extensive cabling.

What is Oxford Instruments' role?

One of the most critical challenges in this endeavour is managing heat generation. The obvious solution is to co-locate the control electronics with the qubits in the cryostat but this requires both to be kept at ultra-low temperatures. Not only is space limited in the cryostat, but the modern semiconductors that make up these chips only work down to -40° C.

We helped overcome this challenge by providing one of our specialised 3 K (-270 °C) cryostats with a custom temperature-controlled measurement plate, enabling precise transistor characterization between 3 and 200 K. We adapted this cryostat by implementing a custom designed stage that allowed the temperature-controlled evaluation of mounted test cryo-CMOS devices.
We offer the environments needed to understand and model why the operating characteristics of the electronics change when the temperature is reduced to absolute zero. From here, our partners in the project will be able to design a portfolio of cryo-CMOS IP, enabling the creation of custom chips that can interface to the qubits at cryogenic temperatures and support controller functionality.

By addressing the fundamental challenges of quantum system design, the consortium is bringing us closer to revealing the transformative potential of quantum technologies

Who else is involved in the project?

The project brings together a strong consortium of quantum research and industry leaders, led by sureCore, with the University of Glasgow, Synopsys, Universal Quantum, SEEQC, and Semiwise. This collaborative approach ensures a holistic solution to the quantum computing challenges. The more we collaborate, the faster we can implement quantum computing in real-world applications for life-changing projects, and head closer towards quantum's commercialisation.

We have strong ties with several of the organisations involved. SureCore, a low power semiconductor design specialist, is leading this project. Paul Wells, CEO at sureCore comments: "This is an extremely exciting project. Quantum computing has the potential to make a huge impact across the globe. Our goal is to accelerate quantum computing scaling by enabling the migration of the control electronics into the cryostat to be closer to the qubits. All the consortium members have made invaluable contributions, and we are really proud of the impressive results seen so far. We are now able to offer to the market, for the first time, a range of Cryo-CMOS semiconductor IP"

We are especially close to the University of Glasgow and Prof. Martin Weides' group with whom we have collaborated on a number of Innovate UK projects. One of these was a project exploring 'Reliable, high throughput production and characterisation of coherent superconducting devices', otherwise known as FABU, alongside Oxford Quantum Circuits: "The collaboration with Oxford Instruments NanoScience has been pivotal in advancing our research in quantum technologies" said Martin Weides, Professor of Quantum Technologies at the University of Glasgow. "The custom-made 3 K cryostat, equipped with a variable temperature stage, has become a cornerstone of our experimental setup. Its large volume and robust cooling power enable the simultaneous integration and testing of multiple devices under cryogenic conditions, significantly enhancing our research efficiency."

"Furthermore, this cryostat allows us to reliably and swiftly pre-test a wide range of devices, ranging from simple transistors to off-the-shelf and our bespoke application-specific integrated circuits (ASICs), from DC up to microwave frequencies. It serves as a critical enabler for the success of this Innovate UK-funded Cryo-CMOS project, streamlining the development of cryogenic control and readout electronics for scalable quantum computing technologies. Moreover, its unique capabilities play a vital role in bridging the gap between research outcomes and commercial applications, particularly through Kelvin Quantum, our startup focused on cryogenic electronics."

What are the next steps? What will happen now that the project is coming to a close?

SeeQC and Universal Quantum will now evaluate the Cryo-CMOS devices, potentially paving the way for commercial products. The developed intellectual property will be made available to quantum computing startups.

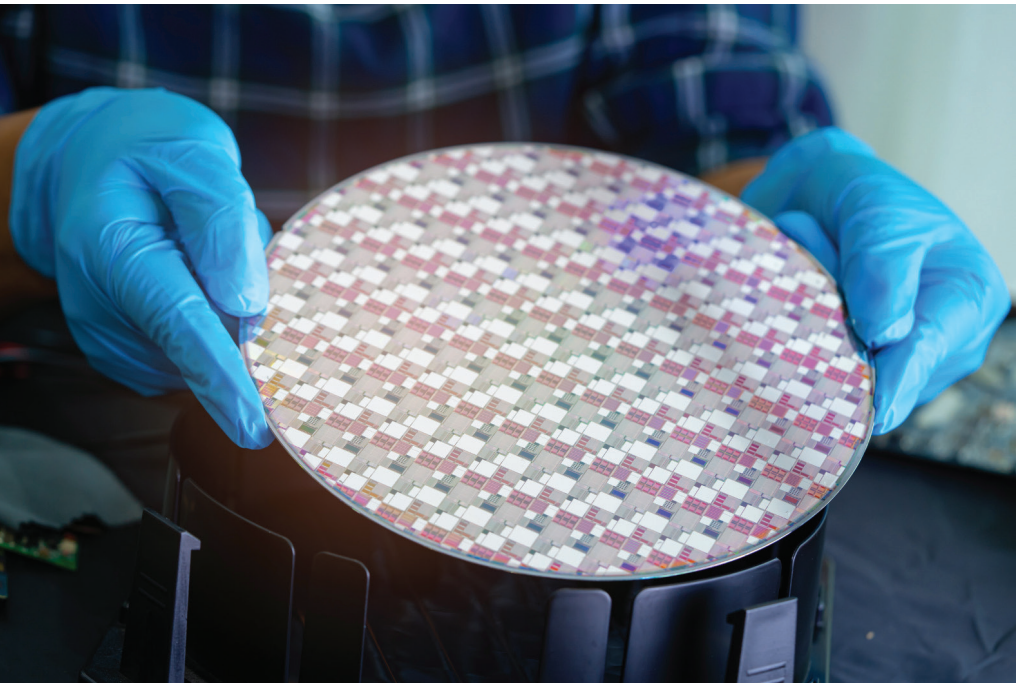
This collaborative effort represents a significant step towards making quantum computing more accessible, efficient, and scalable. By addressing the fundamental challenges of quantum system design, the consortium is bringing us closer to revealing the transformative potential of quantum technologies, promising a future where complex computational problems can be solved with unprecedented speed and efficiency.

Expert insights on choosing the right test methods for accurate thin film and semiconductor analysis

Kalle Niiranen, Technical Account Manager at Measurlabs, writes about method selection based on his experience managing analysis projects for dozens of clients working with thin films and advanced semiconductor components. Measurlabs is a laboratory testing provider with specialised services for the semiconductor industry, offering seamless access to all analytical techniques through a single point of contact.

IN THE semiconductor industry, precision is everything. When devices are scaled down to the nanometer range, the slightest impurity or structural inconsistency can compromise performance or cause the device to fail. Accurate testing is the key to avoiding such situations, and it requires selecting the right analytical method for each task.

Different techniques provide different types of data, and a combination of several methods is often needed to gather all required information.



The challenge lies in matching the techniques to the samples and the information needed, whether that is compositional detail, contaminant detection, or structural integrity.

The risks of going for convenience in compositional analysis

Even highly experienced product development engineers often default to familiar or readily available techniques, even when alternative methods could provide more accurate, relevant, or cost-effective results. One situation where we see this often is automatically opting for X-ray photoelectron spectroscopy (XPS) for compositional analysis of thin films. While XPS is an excellent choice for surface-level elemental analysis when quantifying heavier elements, it cannot detect hydrogen or helium. As one example, films deposited using atomic layer deposition (ALD) may be hydrogen-rich, and analyzing them with XPS can lead to deceptively “clean” data that underrepresents hydrogen content by several atomic percentages.

In such cases, a hydrogen-sensitive method like secondary ion mass spectrometry (SIMS) or time-of-flight elastic recoil detection analysis (ToF-ERDA) is needed to obtain a more accurate picture of the film’s composition. Out of these options, SIMS is often chosen simply because it is more well-known. This may introduce a new set of problems, as SIMS requires high-quality reference samples for calibration, and obtaining these for all materials of interest for a suitable matrix is not always straightforward. ToF-ERDA, on the other hand, yields quantitative results for elements from hydrogen to uranium without a need for references.

Picking the right tools for tracking trace contaminants

When analyzing trace-level contaminants on thin film surfaces, the distinctions between methods become even more critical. A common tendency

is to opt for a reasonably priced screening method, such as vapor phase decomposition ICP-MS (VPD-ICP-MS). While it is a cost-effective option for routine monitoring and has an excellent, often ppb-level detection limit, it cannot locate the exact spot where the contamination is located on the wafer.

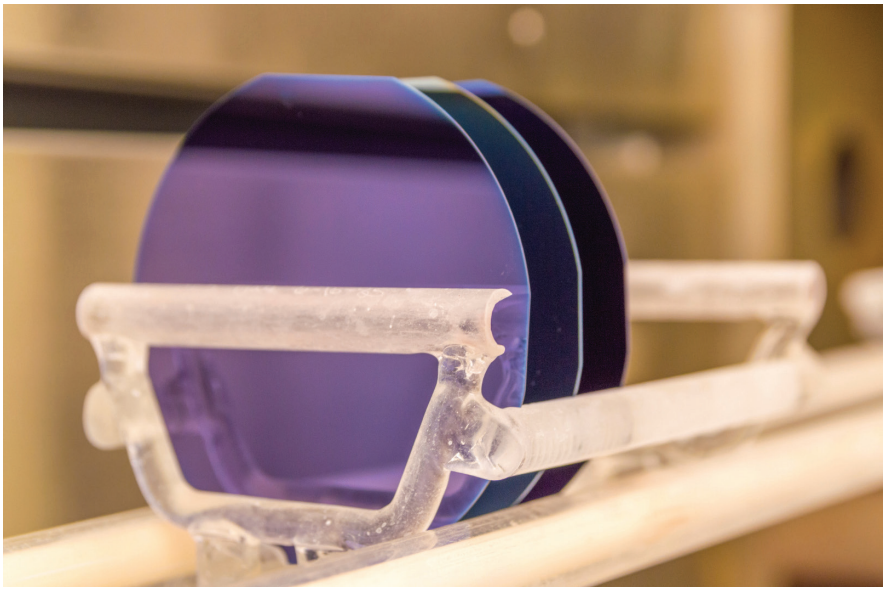
To complement data obtained with VPD-ICP-MS, total reflection X-ray fluorescence (TXRF) can be used to localize the contamination and facilitate a more targeted analysis of its root causes. Due to the higher cost, however, TXRF is typically used sparingly. A typical workflow might involve screening hundreds of wafers for contamination with VPD-ICP-MS and following up with TXRF on a smaller subset of samples.

When measuring trace element concentrations as a function of depth, SIMS is again often the first choice for many. While it does offer an excellent detection limit when references are available, its depth resolution is not always as good as that of medium energy ion scattering (MEIS) spectroscopy, which also has the added advantage of not requiring reference samples.

Depending on the target elements and the required detection limit and depth resolution, Rutherford backscattering spectrometry (RBS) might also be a solid choice. As a general rule, we would recommend ToF-ERDA or SIMS for light elements, MEIS for elements in the mid-range of the periodic table, such as manganese, tin, and gallium, and RBS for the heaviest elements.

Monitoring thin film thickness: why ellipsometry isn't always enough

Method choice matters even in seemingly routine tasks like measuring



thin film thickness. Here, ellipsometry is often used due to its speed and widespread in-house accessibility. However, it can be unreliable for complex multilayer structures or films grown by ALD, where growth-per-cycle values within the film stack may deviate from average results of thicker single-material films. In such situations, variations from the expected layer thickness can lead to inaccurate modelling and misleading thickness data.

X-ray reflectivity (XRR) often provides more accurate results for multi-layered films, especially when the layers have varied densities, which can also be determined with the technique. Additionally, transmission electron microscopy with focused ion beam preparation (FIB-TEM) can be used for visual confirmation of layer thickness in nanoscale films.

The importance of choosing the right testing partner

Availability bias may cause method selection to be guided by the availability of analytical equipment rather than the research question, leading to incomplete or even misleading data being collected. Measurlabs' service model, built around a wide network of partner laboratories, gets around this issue, as it removes the incentive to recommend a given method just because it is easily available.

Having a scalable testing infrastructure with multiple partners for all major thin film analysis techniques, Measurlabs is well-equipped to manage large-scale projects involving hundreds of wafers or complex multi-technique workflows. Not depending on a single instrument or facility also minimizes the risk of delays caused by equipment downtime or laboratory closures.

In a field where small errors can have large consequences, it is essential to have timely access to a comprehensive range of analysis methods and the expertise to choose the right ones for each purpose. This ensures that results are reliable, costs are kept in check, and incomplete information does not cause delays to product development or quality assurance processes.

When analyzing trace-level contaminants on thin film surfaces, the distinctions between methods become even more critical. A common tendency is to opt for a reasonably priced screening method, such as vapor phase decomposition ICP-MS (VPD-ICP-MS). While it is a cost-effective option for routine monitoring and has an excellent, often ppb-level detection limit, it cannot locate the exact spot where the contamination is located on the wafer

Microchips: EU off the pace in a global race

The target of 20 % global market share by 2030 appears out of reach. Member states and the private sector account for the lion's share of investment; the European Commission manages much smaller funds. Issues like access to raw materials, energy costs, and geopolitical tensions pose additional challenges. Here we set out the findings and recommendations of the European Court of Auditors' 'The EU's Strategy for Microchips' Special Report.

IT IS VERY unlikely that the EU will meet its target of a 20 % share of the global market for microchips by 2030, according to a new report by the European Court of Auditors. While the 2022 EU Chips Act has brought new momentum to the European microchip sector, the investments driven by it are unlikely to significantly enhance the EU's position in the field.

Microchips play a vital role in modern life, and the global shortage of microchips during the COVID-19 pandemic highlighted their critical importance to the economy. The EU's Digital Decade strategy set a target for the Union to gain a 20 % share of global production value in cutting-edge and sustainable microchips by 2030. The European Commission has made reasonable progress on implementing its strategy, but the auditors found that there is a gap to bridge between ambition and reality.

"The EU urgently needs a reality check in its strategy for the microchips sector", said Annemie Turtelboom, the ECA Member in charge of the audit. "This is a fast-moving field, with intense geopolitical competition, and we are currently far off the pace needed to meet our ambitions. The 20 % target was essentially aspirational – meeting it would require us to approximately quadruple our production capacity by 2030, but we are nowhere close to that with our current rate of progress. Europe needs to compete – and the European Commission should reassess its long-term strategy to match the reality on the ground".

The Commission is responsible for only 5 % (€4.5 billion) of the €86 billion in estimated funding for the Chips Act up to 2030. The remainder is expected to come from member states and industry. For comparison, the top global manufacturers budgeted €405 billion in investment over just a three-year period, from 2020 to 2023, which dwarves the financial firepower of the Chips Act.

Nevertheless, as the auditors point out, the Commission has no mandate to coordinate national investments at EU level to ensure they align with the Act's objectives. In addition, the Chips Act lacks clarity in its targets and monitoring, and it is difficult to know whether it takes proper account of the industry's current levels of demand for mainstream microchips.

Several other key factors affect the EU's competitiveness in the field, and the chances for successful implementation of the Chips Act. These include dependency on imports of raw materials, high energy costs, environmental concerns, geopolitical tensions and export controls, and a shortage of skilled workers.

Furthermore, the EU microchip industry consists of a few large enterprises focused on high-value projects, meaning that funding is concentrated. The cancellation, delay or failure of a single project can therefore have a significant impact on the whole sector. Overall, the auditors found that the Chips Act is highly unlikely to significantly increase the EU's share of the microchips market, or to meet the objective of 20 % of global output. Indeed, the European Commission's own forecast, published in July 2024, predicts that despite a significant expected increase in manufacturing capacity, the EU's overall share of the global value chain in a fast growing market would increase only slightly, from 9.8 % in 2022 to just 11.7 % by 2030.

The report in more detail

Over the years, the EU's output of microchips has increased, but its share of global manufacturing capacity has decreased significantly. In 2020 the EU's share was estimated at around 9 %[1]. In 2021, with the EU's existing production sites operating at full capacity, the EU's trade deficit for microchips was almost €20 billion[2]. In the context of a very complex and globalised microchip value chain, total autonomy in microchip production is impossible.

However, the COVID-19 pandemic highlighted dependencies of the EU in the global microchip market, and the risk it represents for EU industry. For example, in the pandemic's wake, the shortage of microchips for German carmakers caused car production to collapse to 1975 levels. This resulted in a recognition of the importance of security of supply (either manufactured within the EU or by reliable partners) in order to reduce dependency, and the need for an updated strategy on the EU's role in the global microchip market.

As an element of the EU's industrial policy, the EU Chips Act package[3] (hereafter referred to as the Chips Act) was introduced in February 2022 to respond to the global supply chain disruptions provoked by the COVID-19 pandemic, which also affected Europe. The aim of the Chips Act was to confront microchip shortages and strengthen EU's technological leadership. The Chips Act regulation entered into force in September 2023.

A range of public and private potential funding streams were identified for the microchip sector, with a minimum of €43 billion in policy-driven investments matched by a commensurate amount of private investment funding announced under the Chips Act.

The total can be estimated as at least €86 billion. Member states and industry stakeholders are expected to contribute substantial resources for the implementation of the Chips Act. The Commission adopted the EU's Digital Decade target of 20 % by value of world production in cutting-edge and sustainable microchips by 2030, as the overarching objective of the Chips Act.

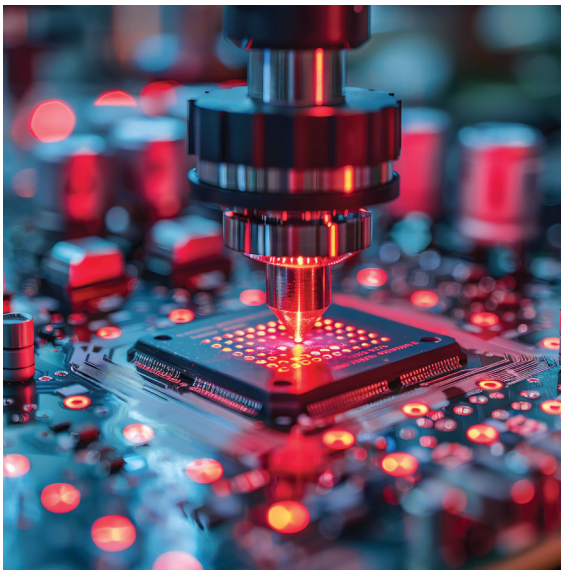
The objective of the audit was to examine how EU industrial policy supported strengthening the strategic autonomy of the EU microchip industry. We assessed the Chips Act's design against the outcomes of the 2013 Strategy on the micro- and nano-electronic sectors, the alignment of funding with the EU's strategic objectives, the timeliness and progress of the Chips Act implementation and reaching its overall objective, and other factors and risks affecting its success. This audit aims to contribute to crucial debates on the EU's strategic autonomy and industrial policy, complementing the previous work as set out in the ECA's special reports on circular economy, batteries, and hydrogen.

Findings and recommendations

Overall, we conclude that the Commission's current strategy (the "Chips Act") provided new impetus for action in the area. The Commission has already made reasonable progress in implementing its strategy, especially with regard to Pillar I, but we found weaknesses in its preparation, implementation and monitoring. Given the current level of investment in manufacturing capacity, the strategy is very unlikely to be sufficient to achieve by 2030 the very ambitious Digital Decade target of a 20 % EU share in the global market value chain by revenue. It is currently predicted that its share will be only 11.7 % by 2030. This target may also be considered overly ambitious for the Chips Act given the Commission's limited mandate and resources and the success of the strategy being largely reliant on member states' actions, investments of the private sector, and other crucial factors, such as the cost of energy.

The Chips Act package of 2022 was preceded by a 2013 Strategy that aimed to strengthen the micro- and nano-electronic sectors. While the EU's microchip capacity increased substantially as of 2013, it did not keep pace with global growth meaning the EU's share of the global market declined. The Chips Act picked up where the 2013 Strategy had left off, and responded to the microchip shortage crisis with a set of new actions. These included: reinforcement of technological and innovation capabilities and addressing gaps in the ecosystem (Pillar I); the principles to assess state aid support to investments in innovative "first-of-a-kind" (FOAK) production facilities (Pillar II); monitoring and response mechanisms to anticipate and react to crises (Pillar III).

However, the Chips Act was prepared in urgency, meaning the procedures usually applied when preparing legislation were not followed, such as evaluation of previous strategies, and an impact analysis of the proposal. Not fully analysing why the 2013 Strategy fell short of its goals and the resultant failure to draw lessons from the experience could mean that the Chips Act is susceptible to precisely the same problems. We found that the Chips Act lacks clarity regarding its targets and monitoring. In the absence of a full impact assessment, it is difficult to judge whether the Chips Act gives sufficient consideration to industry's needs in mainstream microchips.



Investment decisions in the microchip industry are predominantly driven by private sector companies. In the context of the 2013 Strategy and subsequently the Chips Act, a range of different public and private potential funding streams were identified for the microchip sector. The Chips Act announced a total investment of at least €43 billion, with expected further private investment of a similar amount. However, the majority of these funds consist of the industry's own resources or member state budgets, with the Commission being responsible for just a small part (approximately 10 % of public funding) of the total. The Commission has no mandate to coordinate national investments at EU level in order to align them with the Chips Act objectives. Overall, the Commission has only partial information on the total funding provided to, and used by, the industry, which reduces its ability to monitor progress and identify gaps and overlaps.

RECOMMENDATION 1

CARRY OUT AN URGENT REALITY CHECK ON THE STRATEGY AND TAKE THE NECESSARY SHORT-TERM CORRECTIVE ACTIONS

THE Commission should, in close cooperation with both the member states and the industry:

- Urgently carry out a reality check on the Chips Act to assess Whether the ambitions and targets that it contributes to remain realistic in view of the resources available to achieve them, global competition, as well as other crucial factors, such as energy cost and dependence on raw materials;
- Where applicable, take appropriate short-term corrective action needed to help achieve the strategic objectives;
- Introduce systematic monitoring to identify as early as possible any impediments to achieving the objectives of the current (and any future) microchip strategy, as well as mechanisms for prompt remedial action.

Target implementation date: 2025

While we found that the projects receiving co-funding directly from the Commission, or via the Chips Joint Undertaking (JU) (and its predecessors the Electronic Components and Systems for European Leadership (ECSEL) and the Key Digital Technologies (KDT) joint undertakings), were generally well-aligned with the goals of the respective strategies, the arrangements in place to measure their effect were incomplete. The Commission also has incomplete information on the state aid investments' contribution towards achieving the strategy's objectives.

We found that the timeline for implementing the Chips Act's three pillars is unclear, and their implementation is very unlikely to be sufficient to achieve the overarching objective. Pillar I is progressing well but suffering some delays. The uptake of FOAK investments under Pillar II is slow and unlikely to be sufficient for the overall digital target of 20 % to be met by 2030. Lastly, the coordination and crisis-monitoring mechanisms, which were expected to be available in the short term under Pillar III, are still in the very early stages.

Achievement of the Chips Act objectives does not depend solely on EU action, but is also determined by the level of private sector investment, the EU business competitiveness compared with competing global regions, and other crucial factors. The funding associated with the Chips Act may not be sufficient to support and stimulate the investment the industry needs to increase the EU's share, and so meet the objective of 20 % of global output. Indeed, the Commission's own forecast published in July 2024 predicts a slightly increasing market share to only 11.7 %. We also note that the industry is characterised by a relatively small number of large enterprises undertaking high value projects, meaning that funding is similarly concentrated. As such, the cancellation, delay or failure of an individual project can have a significant overall impact. Finally, as the semiconductor industry is global, the EU faces intense international competition, as well as other challenges. Countries around the world have their own strategies for attracting investment, increasing their market share and strengthening the security of their supply. There are also other factors, which also depends on coordination between the EU and member states, impacting the EU's competitiveness and the objectives of the Chips Act, such as export controls, access to the necessary raw materials, the cost of energy and environmental requirements.

RECOMMENDATION 2

START PREPARING THE NEXT SEMICONDUCTOR STRATEGY

THE Commission should, in close cooperation with both member states and the industry, start preparing the next semiconductor strategy. This strategy should:

- Build on the result of the above review and the successes and failures of the previous strategies;
- Set clear, timebound and realistic objectives taking into account the state of play of the EU's microchip sector, EU industry's short- and long-term needs, global competition, and other crucial factors, such as energy cost and raw material supply;
- Propose appropriate actions and funding, including if deemed necessary proposals to adapt the legal framework;
- Include a coordinated approach at EU level, including interactions with competing economies on a global scale.

Target implementation date: 2026

FURTHER READING / REFERENCE

- [1] Semiconductor Industry Association: Government Incentives and US Competitiveness in Semiconductor Manufacturing, 2020, p. 7 (exhibit 2).
- [2] Commission staff working document: A Chips Act for Europe, SWD(2022) 147, p. 57.
- [3] COM(2022) 45, COM(2022) 46, COM(2022) 47, C/2022/782.

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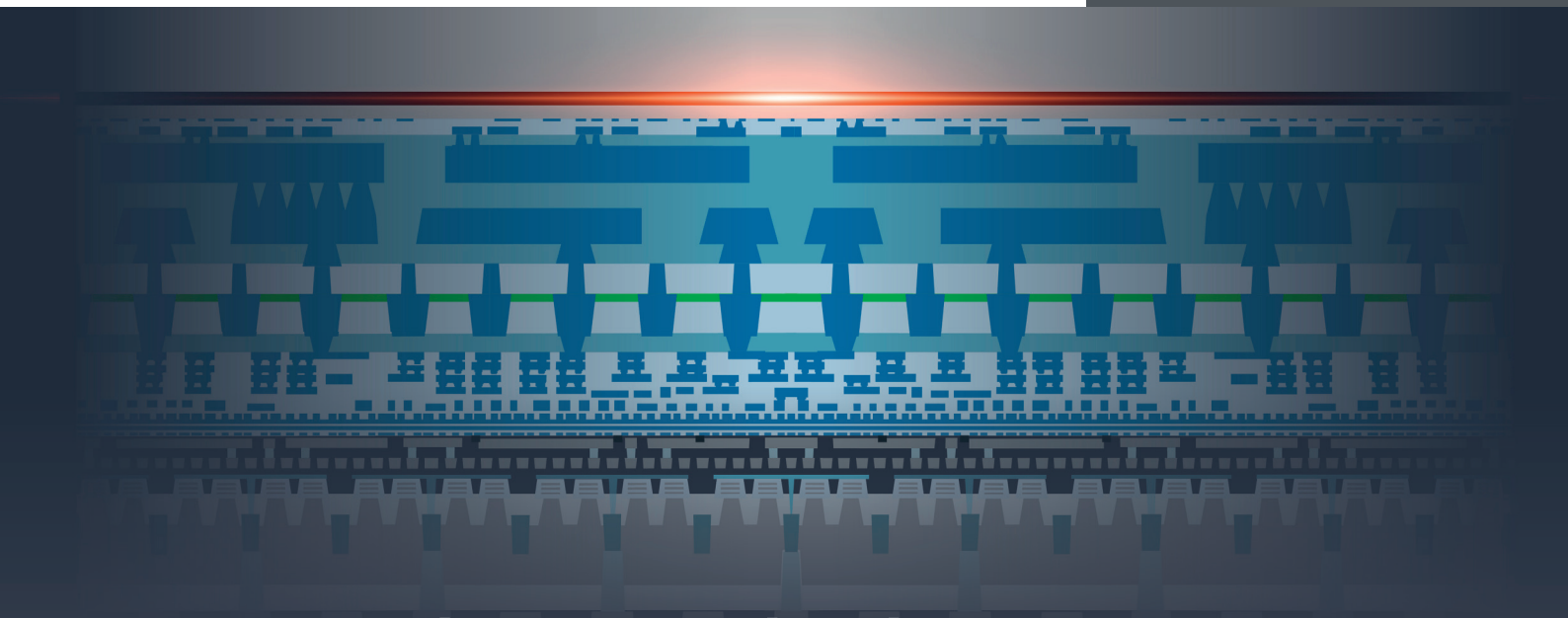

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GaN-on-Si transistor performance, single-chip microwave photonics and DAC

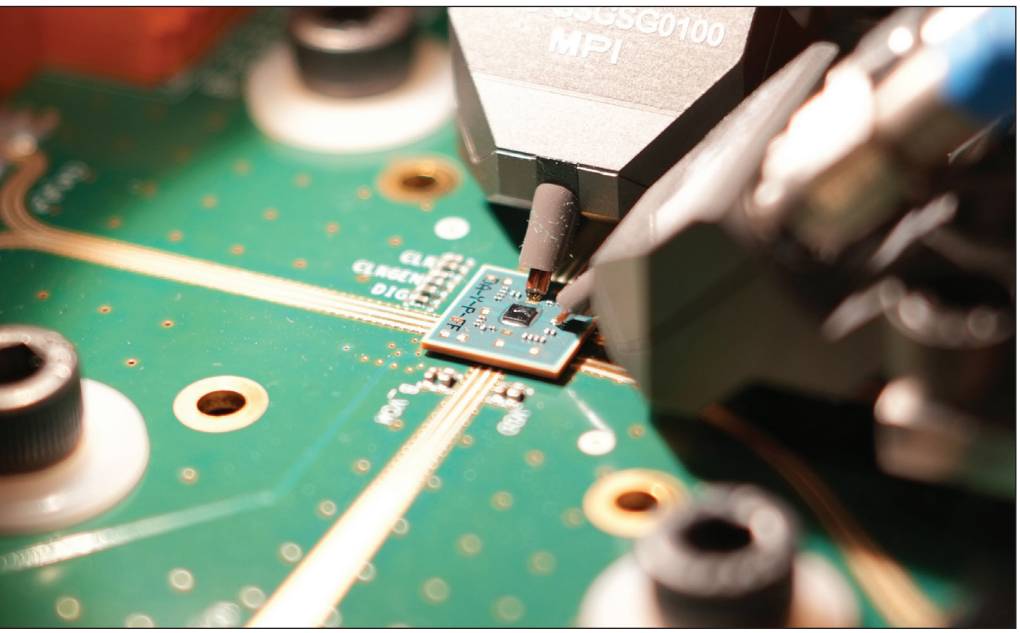
Recent imec research work includes record-breaking RF GaN-on-Si transistor performance for high-efficiency 6G power amplifiers, imec and Ghent University demonstrating a fully-integrated, single-chip microwave photonics system for compact and versatile signal processing and a significant breakthrough in high-speed digital-to-analogue conversion.

IMEC believes that it has set a new benchmark in RF transistor performance for mobile applications. They present a gallium nitride (GaN) MOSHEMT (metal-oxide-semiconductor high-electron-mobility transistor) on silicon (Si) that achieves both record efficiency and output power for an enhancement-mode (E-mode) device operating at low supply voltage.

In parallel, imec also demonstrated a record-low contact resistance of 0.024Ω· mm which is essential to further boost output power in future designs. The results mark a crucial step toward integrating GaN technology into next-gen mobile devices, particularly those targeting the 6G FR3 band between 7 and 24GHz. The results will be presented at the 2025 Symposium on VLSI Technology and Circuits in Kyoto, Japan.

Today's mobile networks largely operate below 6GHz, but to meet the data rate demands of future 6G systems, a shift to higher frequencies is needed. In these bands, current mobile solutions based on gallium arsenide (GaAs) HBTs (heterojunction bipolar transistor) struggle to maintain performance. Their efficiency and gain degrade significantly above 10 to 15GHz, leading to fast battery drain and poor energy use in user equipment.

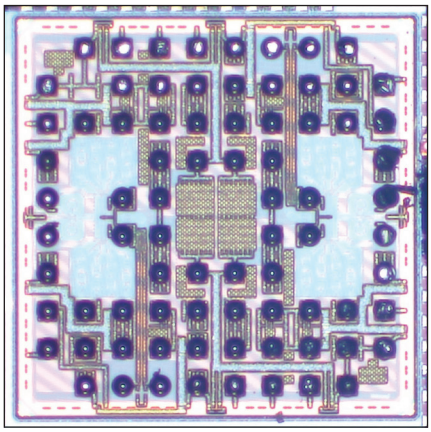
GaN is widely recognized as a promising alternative because of its higher power density and breakdown voltage. While GaN transistors on silicon carbide (SiC) have shown strong RF performance in high-frequency base station applications, the cost and limited wafer scalability of SiC remain barriers for the mobile market.



Silicon is a more scalable and cost-effective platform but building high-efficiency GaN transistors on it has been challenging due to the lattice and thermal mismatch between the two materials, which can compromise material quality and device reliability. The challenge is even greater for E-mode designs –which are preferred in mobile for their fail-safe operation and low power consumption – because it typically requires thinning the transistor barrier and channel under the gate. This limits the on-current and increases the off-state leakage, making it harder to achieve the power, efficiency, and gain needed for 6G.

Imec now demonstrates a GaN-on-Si E-mode MOSHEMT that reaches a record 27.8dBm (1W/mm). output power and 66% power-added efficiency (PAE) at 13GHz and 5V. The result was obtained in a single device with an 8-finger gate layout, providing the gate width needed for high output power without requiring the combined power of multiple transistors. The excellent performance was enabled by combining a gate recess technique, used to shift the device into E-mode, with an InAlN barrier layer that offsets the performance loss from the thinned channel.

In parallel to the device development, imec demonstrated a record-low contact resistance of 0.024Ω· mm using



a regrown n^+(In)GaN layer maximizing current flow and minimizing power loss. While the result was obtained in a separate module, it is fully compatible with the E-mode transistor architecture. Simulations indicate that integrating this contact module could improve the output power density by 70%, meeting the performance target for 6G user equipment.

"Reducing contact resistance is crucial for pushing output power while keeping efficiency high," said Alireza Alian, Principal Member of Technical Staff at imec. "Our next step is to integrate this contact module into the E-mode transistor and validate the expected gains in power and efficiency, bringing the device closer to real-world 6G applications."

A programmable solution for higher-speed wireless communication networks and low-cost microwave sensing

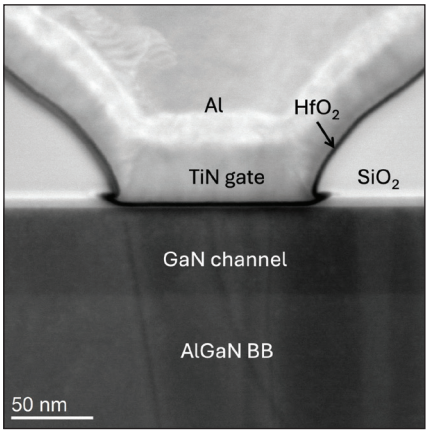
The Photonics Research Group and IDlab, two imec research groups at Ghent University, and imec, a world-leading research and innovation hub in nanoelectronics and digital technologies, have published the demonstration of a fully-integrated single-chip microwave photonics system, combining optical and microwave signal processing on a single silicon chip. The chip integrates high-speed modulators, optical filters, photodetectors, as well as transfer-printed lasers, making it a compact, self-contained and programmable solution for high-frequency signal processing.

This breakthrough can replace bulky and power-hungry components, enabling faster wireless networks, low-cost microwave sensing, and scalable deployment in applications like 5G/6G, satellite communications, and radar systems. The results have been published in Nature Communications.

Modern communication networks rely on both high-speed fiber-optic links and wireless radio-frequency microwave transmission, but as demand for higher data rates and operation at higher frequencies grows, new systems need much tighter integration between these two modes of communication to overcome the struggle with signal processing complexity, high transmission losses, and power-hungry electronics. Microwave photonics offers a promising solution by using optical technology to process high-frequency signals with lower loss, higher bandwidth, and improved energy efficiency. However, most microwave photonics systems rely on bulky, fiber-based architectures that limit scalability. In contrast, integrating microwave photonics onto a chip could enable more scalable and power-efficient systems, but early experimental demonstrations have either lacked key functionalities or required external components to achieve full performance.

Imec and Ghent University now demonstrate a silicon photonic engine that processes and converts both optical and microwave signals on a single chip. The key innovation in this new system lies in the novel combination of a reconfigurable modulator and a programmable optical filter enabling efficient modulation and filtering of microwave signals while significantly reducing signal loss. This unique combination enhances overall performance allowing the system to handle complex signal processing tasks with greater flexibility and efficiency for a wide range of applications.

The chip is built on imec's standard

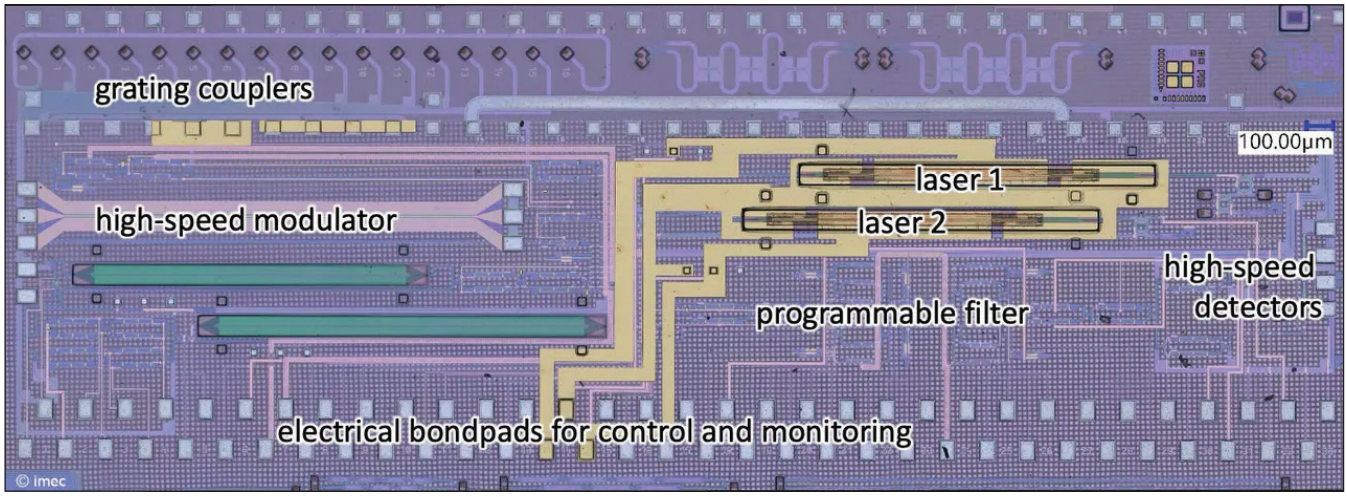


iSiPP50G silicon photonics platform, which includes low-loss waveguides and passive components, high-speed modulators and detectors, and thermo-optic phase shifters for tuning the optical response. To provide an integrated light source, the researchers incorporated an indium phosphide (InP) optical amplifier (developed by III-V Lab) on the chip using the microtransfer-printing technology developed at the Photonics Research Group (imec/Ghent University). In combination with on-chip tunable filter circuits, this allows the optical amplifier to function as a widely tunable laser, further enhancing the system's versatility.

"The ability to integrate all essential microwave photonics components on a single chip marks a major step toward scalable and energy-efficient high-frequency signal processing," said Wim Bogaerts, professor in the Photonics Research Group at Ghent University and imec. "By eliminating bulky external components, this technology paves the way for more compact, cost-effective solutions in next-generation wireless networks and advanced sensing systems."

High-speed DAC paves the way for faster and more energy-

"Imec and Ghent University now demonstrate a silicon photonic engine that processes and converts both optical and microwave signals on a single chip. The key innovation in this new system lies in the novel combination of a reconfigurable modulator and a programmable optical filter enabling efficient modulation and filtering of microwave signals while significantly reducing signal loss"



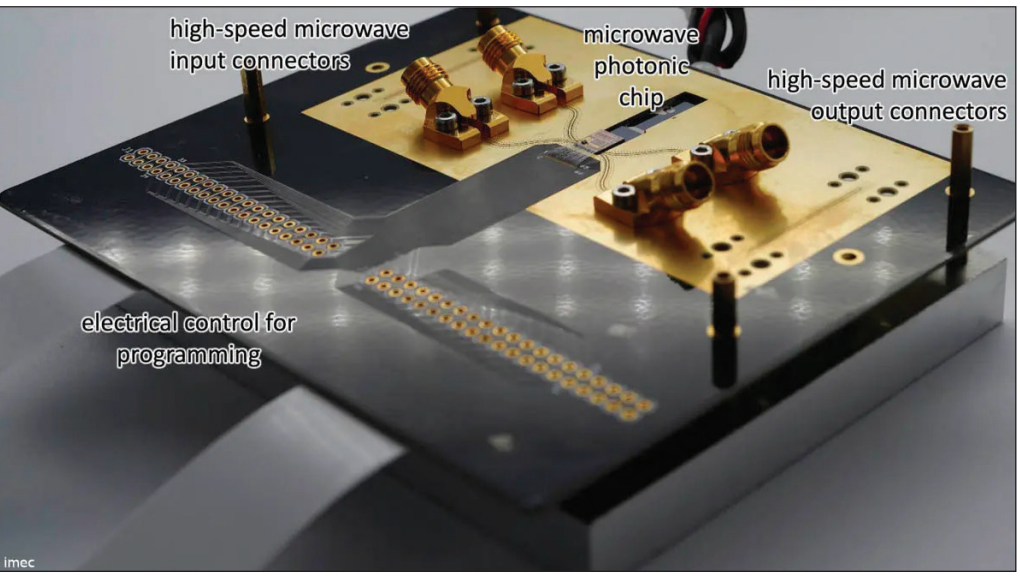
efficient optical and electrical links in data centRES

Imec has made a significant breakthrough in high-speed digital-to-analog conversion. The new 7-bit 150 GSa/s Digital-to-Analog Converter (DAC), fabricated in a 5nm FinFET CMOS process, achieves data rates of up to 300 Gb/s using PAM-4 modulation. Designed to address the growing demand for faster data center links, the DAC combines speed and power efficiency, setting a new standard for wireline data conversion.

The demand for higher data transfer rates in data centers continues to surge as data-intensive applications like machine learning and AI become more prevalent. To handle the vast amounts of data flowing through these centers, wireline communication systems rely on analog-to-digital converters (ADCs) and digital-to-analog converters (DACs) to convert analog signals to digital data and back, allowing the use of sophisticated signal processing supporting transmission over physical links. However, as data volumes continue to rise, ADCs and DACs must convert data at increasingly higher speeds to ensure efficiency.

Ultra-fast ADCs and DACs are therefore essential to ensure data flow in next-generation wireline systems. Conventional architectures often fall short, resulting in signal degradation and power inefficiencies. At the same time, power efficiency is becoming increasingly important, as the amount of interconnect deployed inside large-scale data center infrastructures grows at an even faster pace than the amount of compute.

Imec's latest DAC addresses these challenges by achieving a high-speed 150 GSa/s sample rate, capable of generating data rates up to 300 Gb/s using PAM-4. With increasing data rates, PAM-4 has emerged as the preferred modulation scheme in data centers, enabling faster data transfer without requiring more bandwidth. "This 7-bit DAC is designed for next-generation data center links, targeting data rates above 200 Gb/s and ultimately reaching 400 Gb/s per lane. In order to efficiently manage these speeds, the necessary signal processing is implemented in advanced CMOS nodes such as 5nm FinFET. Consequently, the DAC must also be realized within the same technology node. Integrating such complex architectures in scaled CMOS nodes draws on imec's unique expertise in advanced integrated circuit design," says Peter Ossieur, program manager for high-speed transceivers at imec.



To optimize power efficiency, imec has innovated the DAC architecture by drastically reducing the number of unit cells from 127 to 34. This has minimized switching activity, effectively lowering power consumption (to 621 mW at 0.9V and 0.96V supplies) without compromising speed. This reduction also decreases parasitic effects, enabling more accurate signal conversion at higher data rates.

Ossieur added: "Looking ahead, the team aims to address the growing demand for even faster data links by targeting the next generation of ADCs and DACs based on 3nm CMOS technology. The focus is on doubling the sampling rate to 300GSa/s and pushing bandwidth beyond 100GHz. To achieve such speed imec will draw on its expertise in analog design, and now also addresses the design of ultra-low-jitter clock generation circuitry targeting femtosecond-level accuracies."

From lab to fab

Solving systematic yield issues with next generation 3D X-ray

With the increasing adoption of 2.5D and 3D ICs in semiconductor manufacturing, the sophistication of packaging design is on the rise, highlighting the importance of robust quality assurance practices in bringing these complex architectures to market.

BY COMET YXLON

WITH TRENDS such as miniaturization, or the ever-growing hype around AI, driving demand for increased performance, the next generation of chips are pushing the boundaries of functionality within increasingly compact volumes. This shift raises a host of new challenges for manufacturers, not just in the speed required to stay ahead in a competitive market, but also in managing the higher manufacturing and material costs associated with more complex structures.

To tackle this, manufacturers must adopt comprehensive inspection strategies to maintain a competitive edge. Prompt identification and resolution of issues throughout the design and manufacturing phases are crucial for efficient production scaling, improved yield, and faster market entry.

Historically, non-destructive testing methods, such as 2D X-ray, have lacked both the speed and resolution to find defects within the highly specialized parameters of advanced packaging, particularly for applications that are production-ready, however, with the new generation of 3D X-ray, supported by AI-powered defect recognition, this is about to change.

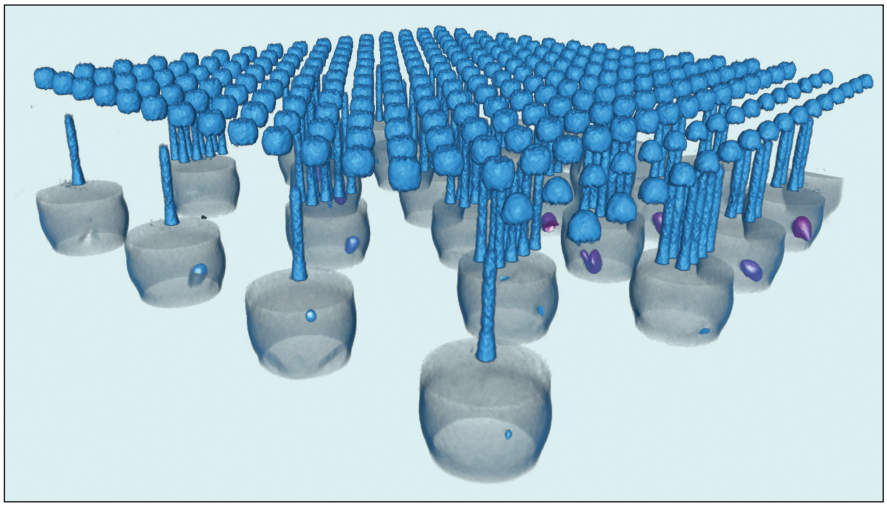
3D X-ray and AI Powered Defect Recognition: A dynamic duo

Advancements in 3D X-ray technology, and in the supporting software, such as those shown in the Comet Yxlon CA20, have the promise to revolutionize the inspection process for 3D ICs. The ability to detect even the smallest defects with precision and speed provides manufacturers with valuable insights to improve yield and quality, without sacrificing time on the production line.

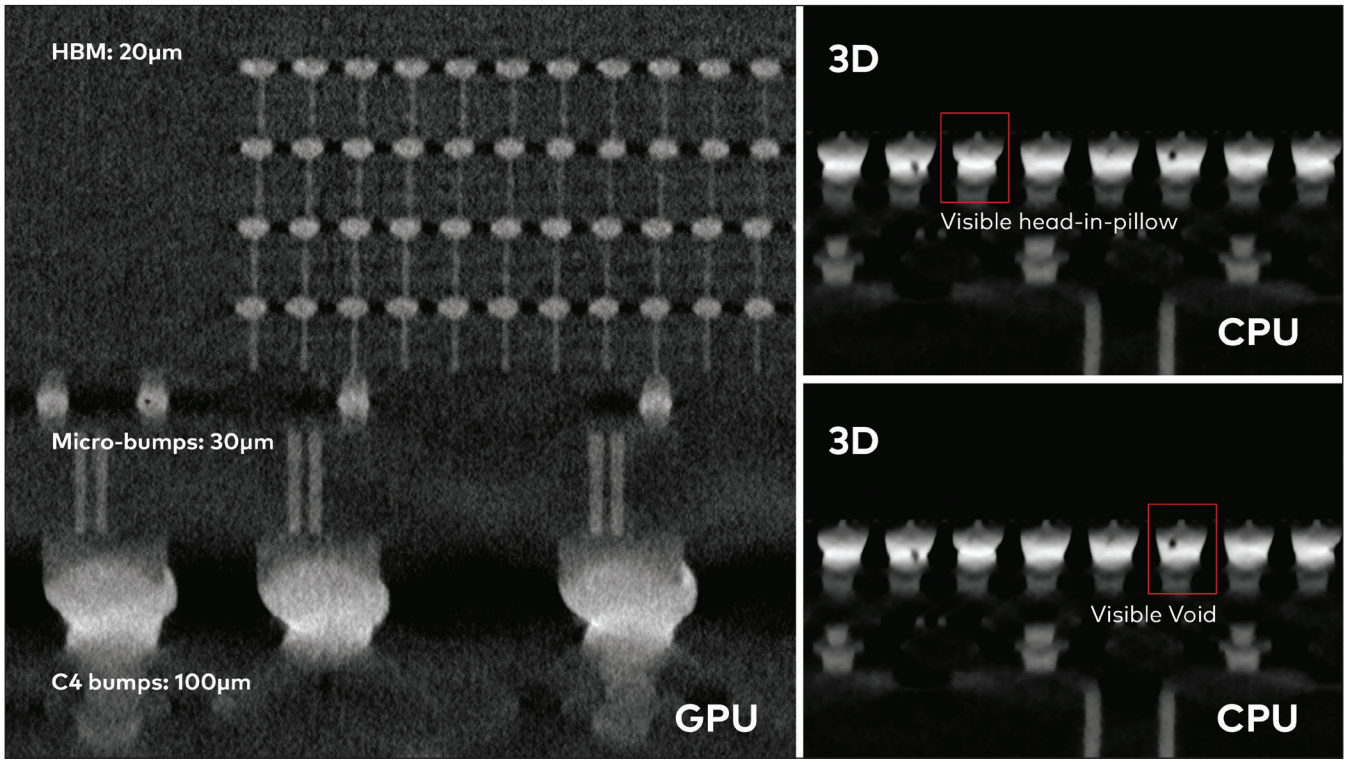
The detailed information extracted from captured images goes far beyond visual inspection, allowing for informed decision-making and enabling manufacturers to address systemic issues, such as voids in solder bumps or “head-in-pillow” defects, before they take hold.

The below example of a CPU captured with Comet Yxlon’s CA20 showcases the capability of modern 3D X-ray technology to reveal intricate details, including defects as small as 10 microns in diameter. The speed at which these scans can be performed highlights the efficiency of the technology in providing rapid and accurate results.

Moreover, the ability to generate “virtual slices” from reconstructed 3D volumes of multi-layered chips such as GPUs allows users to visualize cross-sections of the different layers within, such as C4 bumps, interposer bumps, and high-bandwidth memory (HBM)



➤ Figure 1. A rendering of a commercially available CPU showcasing C4 bumps (diameter: 65µm) with visible voids, TSVs and microbumps (diameter: 20µm). All image property rights remain with Comet Yxlon and images are not to be copied or distributed.



➤ Figure 2: Left, virtual slice of a reconstructed X-ray scan of a commercially available GPU with 100µm C4 bumps, 30µm microbumps and 20µm high bandwidth memory bumps. Right, virtual slice of a reconstructed X-ray scan of a commercially available CPU with ca 65µm C4 bumps. All image property rights remain with Comet Yxlon and images are not to be copied or distributed

bumps. This level of detail would be challenging to achieve with traditional optical inspection or 2D X-ray methods due to the stacked nature of the layers obscuring underlying features.

Although capturing high-resolution images is important, the real strength of today's 3D X-ray technology lies in its AI-powered software capabilities. Software tools like Comet Yxlon's CoS Insights package can quickly identify and assess defects, such as solder bump misalignments and head-in-pillow issues, analyzing their size and severity. By evaluating critical parameters such as bump shift, die tilt, and the probability of defect occurrence, this technology offers a thorough assessment of the component's status.

Integrating 3D X-ray into the Fab environment

All of this highly detailed information can provide incredible insight into a chip's potential performance, however, in the context of a new product introduction (NPI), even small optimizations early in the process can have a significant effect on yield further down the line. It is therefore crucial that any insights into product quality can be directly fed back into the production process to improve.

That is where the next generation Comet Yxlon CA20 comes in. Now updated with automatic loading and unloading capabilities with an integrated EFEM loader, the CA20 ensures a smooth and continuous operation without the need for manual intervention. By seamlessly integrating into the Fab production line, the CA20 offers manufacturers real-time monitoring of production quality, identifying trends and potential issues early on, allowing manufacturers to take proactive measures and ensure consistent product quality.

With wizard-guided functions and automated inspection workflows, including one-click operation, operators can quickly learn how to use the system effectively. At the same time, the advanced hardware ensures reliable measurements are given, even at the shortest scan times, delivering results in a machine-readable format for easy data analysis and interpretation.

These results are then analyzed for key defect parameters automatically using powerful AI-based software in compliance with SECS/GEM standards, ensuring consistency and accuracy in defect identification and reporting.

And there are further software innovations too. Alongside defect recognition, the CA20 comes equipped with smart tools such as our Batch Manager package, which enables the scanning of multiple chips at once, flexibly organizing scan results by part IDs, while the Dose Manager package continuously monitors and tracks the X-ray dose that the sample is subjected to, taking into account the tube power and the distance to the sample to avoid damage to sensitive components.

Main takeaways

Maintaining competitiveness, managing costs, and accelerating time-to-market within today's complex chip world relies on a comprehensive inspection strategy. By including advanced technologies like 3D X-ray inspection, especially coupled with AI-powered defect recognition, manufacturers can enhance yield, quality, and efficiency not just throughout the design and research phase, but even within on the production line.

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