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Greene Tweed

Greene Tweed Leads the Way

Precision Sealing for Advanced Semiconductor Manufacturing

VOLUME 45 ISSUE VI 2024

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

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INSIDE

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ATE testing of heterogeneous silicon chips

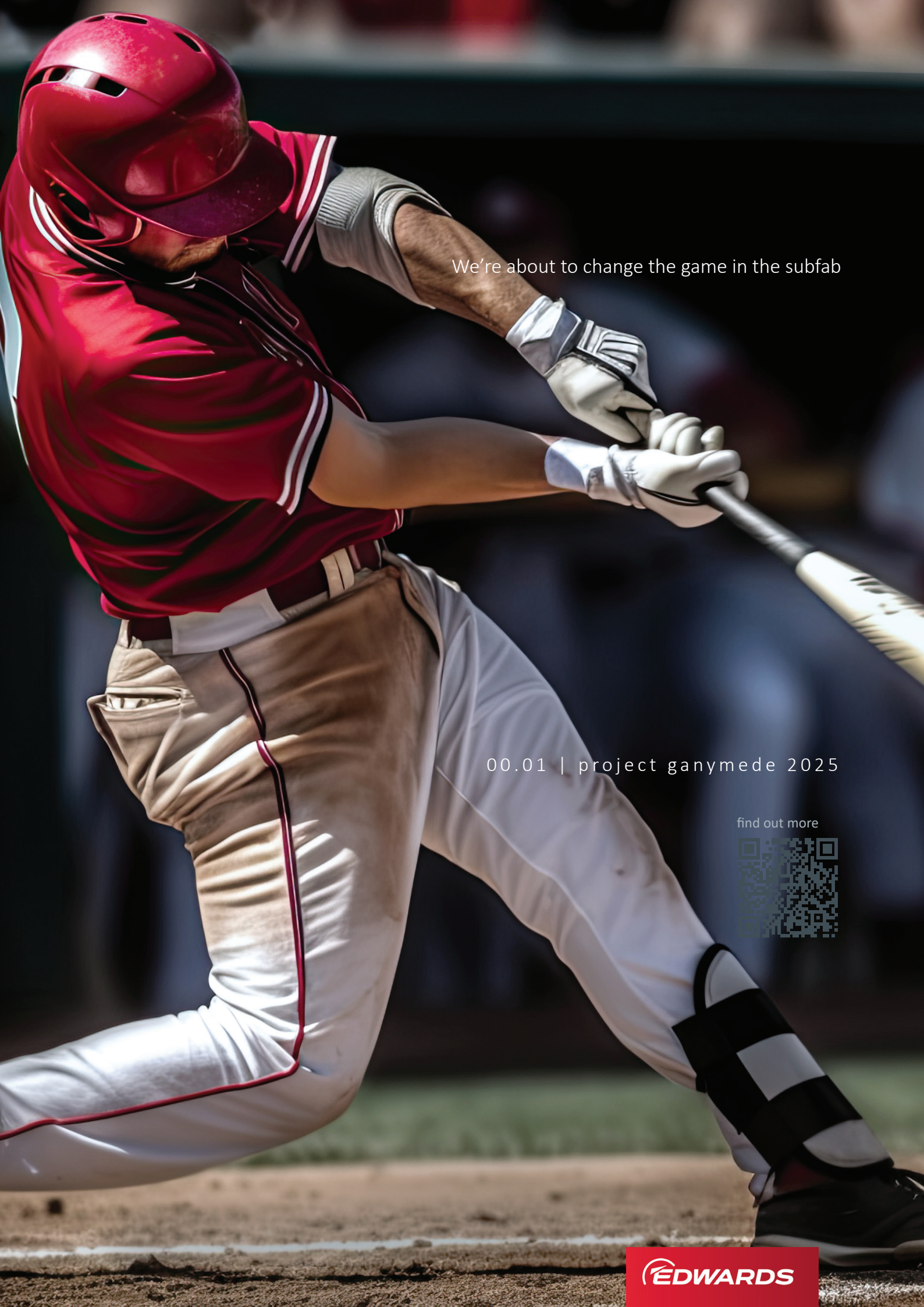
The semiconductor industry is rapidly evolving, driven by the demand for more powerful, efficient, and versatile devices

Active alignment engines for efficient photonics

Photonic markets are advancing rapidly, with substantial growth sectors incorporating this technology in the next decade

Why the mask world is moving to curvilinear

If you've been to a lithography or photomask conference lately, you've noticed many papers and talks on curvilinear formats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EDWARDS

VIEWPOINT

By Phil Alsop, Editor

Yield optimisation – the quest continues

A COUPLE of conversations during some of the recent video interviews I've been conducting served as a timely reminder (to me at least) that the never-ending quest for improving/optimising wafer manufacturing yields needs to be as wide-ranging as possible. That's to say that, as well as focusing on the big-ticket ideas and items – AI being latest example of this – organisations would do well to understand the importance of the often overlooked and underestimated aspect of the overall manufacturing process.

Understandably, AI's potential when it comes to impacting virtually all aspects of the semiconductor manufacturing cycle is grabbing the headlines for now. Fuelled by the right quantity and quality of relevant data, AI can add to the many years' of knowledge acquired by experienced semiconductor engineers and experts, to bring about production innovations providing significant operational and financial benefits to many organisations.

One word of warning, AI is not a magic wand which can be waved to solve every problem. Over time, there's no doubt of the contribution it will make to the industry, but in the short term, the lack of available meaningful data sets might just prove something of an obstacle which needs to be overcome. No need to panic! There are some very clever individuals and companies developing some very clever AI (and ML)-based software solutions for the industry, but whether or not the undoubted current hype lives up to the subsequent reality remains to be seen.

In the mean-time, there are plenty of currently overlooked areas of the fab where significant improvements can be made right now. For example, the thermal loop as a topic might not set hearts racing, but the proper specification, installation, operation, monitoring and maintenance of the component parts - chillers, heat exchangers, hoses, pumps and valves, monitoring and control and filtration and purification – allied to the correctly specified insulation quite literally has the ability to make or break the production line.

And yet, responsibility for such a potentially crucial part of the overall fab often falls through the gaps between various job titles and individuals.

Hopefully, the articles in this issue of SiS (including one on the thermal loop!), alongside the recent videos added to our website, will provide plenty of food for thought when it comes to yield optimisation – and serve as a timely reminder that the whole supply chain, with the fab at its heart, needs constant attention, not just the current buzz topics...

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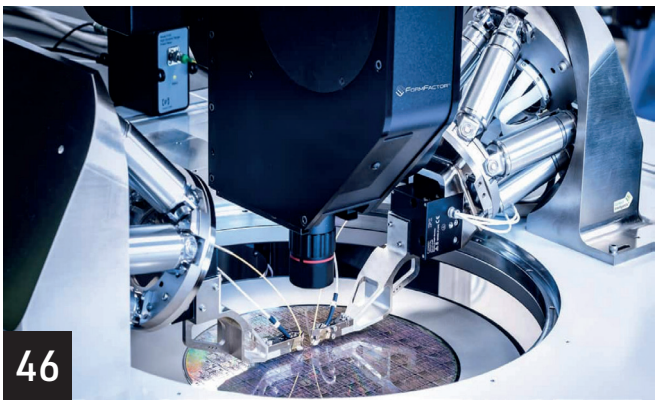

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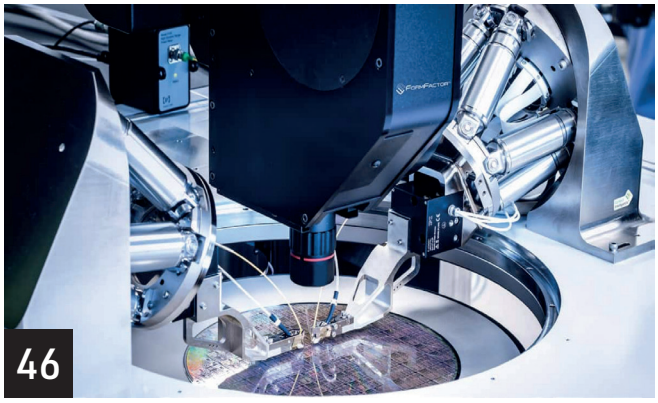
The automation of semiconductor test processes is a crucial factor in modern semiconductor production



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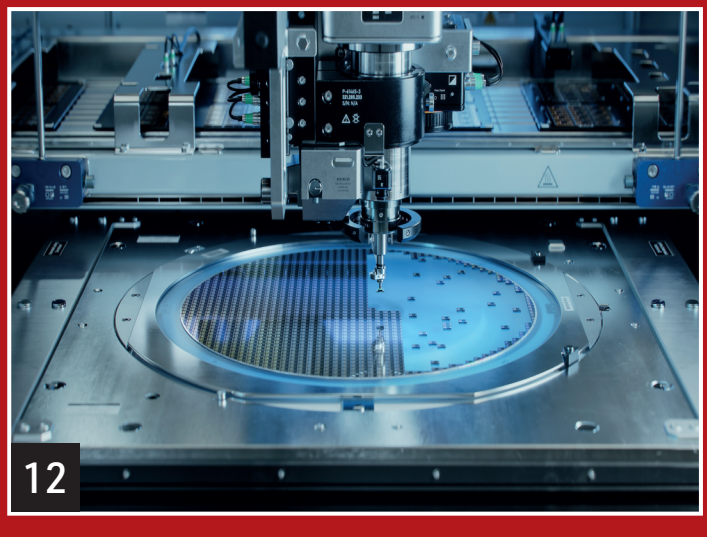

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Intel acts to 'accelerate progress'

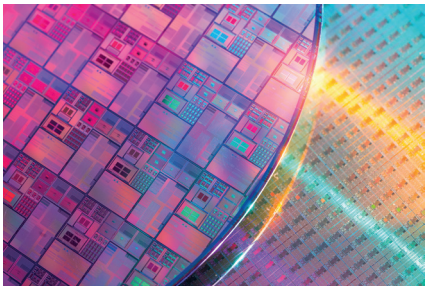
Intel CEO Pat Gelsinger has outlined plans for the future to employees after second-quarter 2024 earnings were published on Aug. 1, 2024.

INTEL PLANS to deliver $10 billion in cost savings in 2025, and this includes reducing head count by roughly 15,000 roles, or 15% of the workforce. The majority of these actions will be completed by the end of this year. The company is seeking to align its cost structure with its new operating model and fundamentally change the way it operates. Revenues have not grown as expected – and the company has yet to fully benefit from powerful trends, like AI. Costs are too high, and margins are too low. As a result, actions are being taken to address both – particularly given the financial results and the outlook for the second half of 2024, which is tougher than previously expected.

Since introducing its new operating model, Intel has taken a clean-sheet view of the business and assessed itself against benchmarks for high-performing foundries, fabless product companies and corporate functions. This work made it clear the company's cost structure is not competitive.

For example, annual revenue in 2020 was about $24 billion higher than it was last year, yet the current workforce is actually 10% larger now than it was then. There are a lot of reasons for this, but it's not a sustainable path forward. Beyond its costs, Intel is to change the way it operates. There's too much complexity, so there is a need to both automate and simplify processes. It takes too long for decisions to be made, so there is a need to eliminate bureaucracy. And there's too much inefficiency in the system, so there is the need to expedite workflows.
Key Priorities

Areas of focus include:
Reducing Operational Costs: Intel will drive companywide operational and cost efficiencies, including the cost savings and head count reductions mentioned above.



Simplifying the Portfolio: Intel will complete actions this month to simplify its businesses. Each business unit is conducting a portfolio review and identifying underperforming products. The company is also integrating key software assets into the business units to help accelerate the shift to systems-based solutions. And the plan is to narrow its incubation focus on fewer, more impactful projects.

Eliminating Complexity: Intel will reduce layers, eliminate overlapping areas of responsibility, stop non-essential work, and foster a culture of greater ownership and accountability. For example, the company will consolidate Customer Success into the Sales, Marketing and Communications Group to streamline the go-to-market motions.

Reducing Capital and Other Costs: With the completion of its historic five-nodes-in-four-years roadmap clearly in sight, Intel will review all active projects and equipment so it begins to shift its focus toward capital efficiency and more normalized spending levels. This will reduce 2024 capital expenditures by more than 20%, and the plan is to reduce non-variable cost of goods sold by roughly $1 billion in 2025.

Suspending its Dividend: Intel will suspend its stock dividend beginning next quarter to prioritize investments in the business and drive more sustained profitability. Maintaining Growth Investments: The company's IDM2.0 strategy is unchanged. Having fought hard to reestablish its innovation engine, Intel will maintain the key investments in its process technology and core product leadership.

Intel CEO Pat Gelsinger explained: "I have no illusions that the path in front of us will be easy. This is a tough day for all of us and there will be more tough days ahead. But as difficult as all of this is, we are making the changes necessary to build on our progress and usher in a new era of growth.

"When we began this journey, we set our sights high, knowing that Intel is a place where big ideas are born and the power of what's possible triumphs over the status quo. After all, our mission is to create world-changing technologies that improve the lives of every person on the planet. And at our best, we have exemplified these ideals more than any company in the world.

"To live up to this mission, we must continue to drive our IDM 2.0 strategy, which remains the same: re-establish process technology leadership; invest in at-scale, globally resilient supply chain by expanding manufacturing capacity in the U.S. and EU; become a world-class, leading-edge foundry for internal and external customers; rebuild product portfolio leadership; and deliver AI Everywhere.

"Over the past few years, we have rebuilt a sustainable innovation engine that is largely in place and on track. It's now time to focus on building the sustainable financial engine needed to drive our performance. We must improve our execution, adapt to new market realities and operate as a more agile company. That's the spirit of the actions we are taking – knowing that the choices we make today, as difficult as they are, will strengthen our ability to serve our customers and grow our business for years to come.

Major government investment to 'propel' Canada

FABrIC launched by CMC Microsystems thanks to strategic investment by the Government of Canada.

CMC MICROSYSTEMS, and Innovation, Science, and Economic Development Canada (ISED) have launched FABrIC, an initiative that secures Canada's future in semiconductors and advanced manufacturing. FABrIC is made possible thanks to an investment of $120M over five years from ISED's Strategic Innovation Fund (SIF), and is a crucial step to grow Canada's semiconductor industry, develop new Made-in-Canada semiconductor-based IoT products, manufacturing options, and create a resilient and sustainable semiconductor ecosystem in Canada.

"Semiconductors are the engines behind the digital economy. Chip-based technologies power applications in all areas of our lives to make us more productive and connected. FABrIC provides Canadian innovators with the resources they need to develop next-generation, high value semiconductor technologies, creates good jobs for Canadians, and strengthens Canada's semiconductor industry to build a stronger economy" said The Honourable François-Philippe Champagne, Minister of Innovation, Science and Industry.

Making the semiconductor products and technologies of tomorrow FABrIC will provide financial and technical resources, mentorship, and training for semiconductor businesses, engineers, and scientists in Canada.

From startups and established firms to post-secondary and research institutions, FABrIC supports innovators developing Made-in-Canada semiconductor-based IoT products in clean tech, electrified vehicles (EVs), artificial intelligence (AI), and much more. FABrIC also provides resources to create new manufacturing processes for Compound Semiconductors, Quantum Technologies, Photonics, and MicroElectroMechanical Systems (MEMS) – areas with high growth potential and value-add where Canadian expertise is well recognized. These are the applications and technologies that will power the semiconductor technologies of tomorrow.

Through a series of Challenge Calls – calls to small and medium sized businesses and researchers to innovate – FABrIC will ignite innovation to develop these strategically important, Made-in-Canada, semiconductor-based IoT products and manufacturing processes.

FABrIC will enable the training of 25,000 students, and 1,000 professors over 5 years, and provide Canadian universities and colleges with technical resources for students and researchers to design and manufacture advanced semiconductor devices during their studies. Graduates are then ready to enter industry in Canada with the skills and experience to continue their professional development and grow the ecosystem in Canada.

"FABrIC offers Canada's semiconductor professionals a wide array of training and upskilling opportunities in the newest tools and technologies to stay at the leading edge of the industry. With fierce competition around the world for top semiconductor talent, a workforce of highly qualified personnel (HQP) in Canada is critical for global competitiveness." Steve Bonham, Plant Manager, Teledyne MEMS and Chair of the Board of Directors of CMC Microsystems.

As global supply chains continue to adapt to meet increasing demand, FABrIC leverages Canada's innovation infrastructure and talent to grow the industry and become a global leader in semiconductor manufacturing. FABrIC ensures that new manufacturing options, developed in Canada, can be used to build the next generation of semiconductor-based IoT products in Canada thanks to our resilient, secure, interconnected supply chain.

"This investment is an important step to securing Canada's future in semiconductors and advanced manufacturing" said Gordon Harling, President and CEO of CMC Microsystems. "FABrIC gives Canadian entrepreneurs and researchers the resources they need to drive innovation and make the advanced semiconductor products of tomorrow here in Canada, thanks to our world-class talent and manufacturing capabilities. Investments in FABrIC will ensure Canada remains a globally competitive player in semiconductors and is well prepared to design and build the semiconductor products of tomorrow."

Powered by CMC Microsystems FABrIC is powered and managed by CMC Microsystems, Canada's leading semiconductor facilitator and accelerator. CMC has over 40 years of experience working with Canadian supply partners and is a trusted partner of companies in Canada and peer countries across the world.

Experts urge EU to increase investment in photonics or risk falling behind China

New research reveals that investments from government and regional clusters worth billions of euros have enabled China to become the world's biggest photonics powerhouse – prompting calls from EU photonics experts for increased funding to close the gap in critical technologies.

STUDY REVEALS how industrial development plans and unique regional clusters have helped China increase its global market share from 10% in 2005 to more than 30% in 2022 – dwarfing Europe and the US.

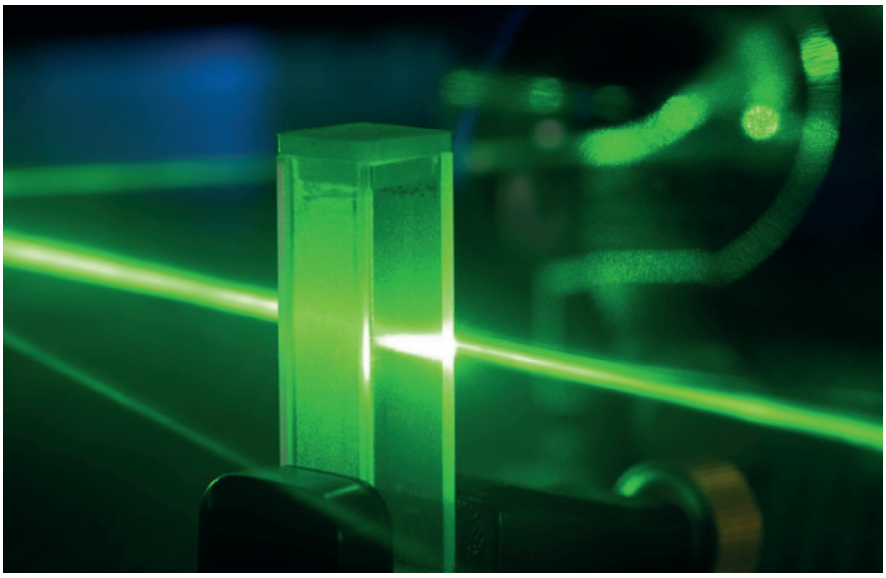
Local clusters are set to raise €5 billion to invest in China's photonics industry in the next few years.

China is currently in the third phase of the National Integrated Circuit Industry Investment Fund, the largest-ever semiconductor investment programme equivalent to nearly €39 billion. Photonics21 President Dr. Lutz Aschke says, "The future of Europe's innovation and industry rests on our ability to match China's strategic advancements."

A new study published by Europe's premier photonics technology platform, Photonics21, shows the tremendous growth of China's photonics industry, with a global market share increasing from 10% to more than 30% over the past two decades – dwarfing both the US and Europe each with 15% respective shares.

The research, called Political Steering Processes in China in Core Segments of the Photonics Industry, which was conducted by international management consultancy EAC reveals how China's political system steers and funds the industry.

Photonics – the science and technology of generating and harnessing light – is a linchpin that supports and enhances critical technologies like quantum, 5G, AI, IoT, biotechnology, aerospace, intelligent manufacturing, and life sciences and is crucial for applications in displays, lasers, lighting, ICT, and photovoltaics.



The new study shows despite China's GDP growth gearing down from a rapid ~7% to a steadier ~4% over the next few years, photonics production in China is still expected to reach €315 billion in 2025.

This global dominance has prompted calls by European experts to increase funding for optics and photonics technologies. Photonics21 President Dr. Lutz Aschke said: "Policymakers must take heed of China's market and technological leadership. China is penetrating sectors traditionally dominated by Europe, such as laser manufacturing, sensing, optical components and systems. Basic research and enabler processes need to be strenghthened and matched by investments in future markets such as Artificial Intelligence (AI). We have to take timely measures.

"While Europe currently holds the second position in the global photonics industry, there is a pressing risk of falling behind. Without significant investment, Europe faces the threat of losing ground in this crucial technology sector, which could undermine its economic competitiveness and technological independence.

"To maintain and defend this position, it is essential for national and European policymakers to prioritise this strategic sector. We need to implement a European strategy on critical materials and components for key industries and technologies to secure a resilient photonics supply chain in Europe. Specifically, research and development activities, as well as the production of photonic components in Europe that are critical to the industry supply chain, should be strengthened.

"The future of our innovation and industry rests on our ability to match China's strategic advancements and secure our place in the global market. We must urgently increase funding for Europe's photonics industry to keep pace and close the gap with China."

€5 billion in China's regional clusters According to the study, China's financial backbone consists of local governments, investment institutions, and enterprises. These entities are set to exceed national contributions with around €5 billion for photonics innovations over the next few years.

The research shows that public funds account for only 20%-30% of this regional revenue. In contrast, the remaining 70%-80% is composed of funds from investment institutions and enterprises. These clusters are based in eight different cities in major industrial areas across China, each with its own focus and strategy. In Suzhou, a 10 billion RMB (approx. €1.3 billion) photonics industry fund aims to establish the Suzhou Taihu Photonics Center, enhancing scientific innovation.

Wuxi plans the Taihu Optics Valley with significant investments, including a 3 billion RMB (approx €390 million) fund for silicon photonics and a 2 billion RMB (approx €260 million) industrial park. Wuhan, known as China's Optical Valley, boasts a 10 billion RMB (approx €1.3 billion) venture capital fund. Beijing plans a €30 million optoelectronics fund, while Xi'an's 750 million RMB (approx €97 million) fund supports its photonics industry. Chengdu offers incentives like 10 million RMB (approx €1.3 billion) grants for optoelectronics investments.

Shanghai identifies photonics as a future-leading industry, and the Guangdong-HK-Macao Greater Bay Area has received the equivalent of €1 billion in photonics investments since 2021.

Sydney council forges vital semiconductor agreement

THE MoU, digitally signed by both parties at formal ceremonies held simultaneously in Taiwan and at City of Ryde's Council Chambers on Tuesday 9 July, was approved by Council at its meeting on Tuesday 24 October 2023.

Along with City of Ryde Mayor Clr Trenton Brown and CEO Wayne Rylands, dignitaries at the ceremony included NSW Federal Senator Dave Sharma, The Hon. Jacqui Munro, Member of the NSW Legislative Council, Jordan Lane, Member of the NSW Parliament, Hugh McDermott, Member of the NSW Parliament, Stirling Wright, MPID Partnerships, Macquarie University, and Prof Sakkie Pretorius, Deputy Vice Chancellor (Research), Macquarie University.

Taipei Economic and Cultural Office, Sydney, Director-General David Chen-Wei Wu was also present, while Wayne Yeong-Junaq Wang, Director-General Hsinchu Science Park Bureau, conducted the signing in Taipei. Cooperation between Council and the Hsinchu Science Park – which houses the world's top two semiconductor companies among its more than 400 high-tech businesses – will focus on 'the advancement of the semiconductor industry, the biomedical industry, and the incubation of start-up companies'.

The historic agreement means that Macquarie Park Innovation District can play a key role for Australia in an essential global industry that produces the computer chips needed to run everything from household appliances, smartphones and cars to submarines, and medical equipment. Under the terms of the MoU, City of Ryde and Hsinchu Science Park will work together on information sharing and technology collaboration, bilateral contacts and partnership development, and the encouragement of knowledge-based industries in both regions.

It will further encourage assistance and collaboration in expanding other knowledge-based related industry clusters in both regions, and the encouragement of the exchange of faculty/staff or science park employees from the respective institutions.

"In the spirit of cooperation and friendship, the Hsinchu Science Park Bureau and the City of Ryde, share the common desire to expand and deepen their friendly ties of economic cooperation," said City or Ryde Mayor Clr Trenton Brown, who signed the MoU on Council's behalf. "As noted by the Australian Strategic Policy Institute in September 2022, Australia's lack of participation in the global semiconductor ecosystem has put us

at a geopolitical disadvantage and having unfettered access to microchips is a matter of economic and national security.

"Taiwan produces over 60 percent of the world's semiconductors and over 90 percent of the most advanced chips, so this collaboration is significant, not only for the City of Ryde but also for NSW and Australia."

In March 2023, delegates from the City of Ryde attended the Taipei Smart City Summit and Expo, visiting the Hsinchu Science Park and meeting officials from Hsinchu County and the Hsinchu Science Park Bureau. Council delegates held 39 meetings over three days with a range of business, academic, and government institutions.

"As noted by the Australian Strategic Policy Institute in September 2022, Australia's lack of participation in the global semiconductor ecosystem has put us at a geopolitical disadvantage and having unfettered access to microchips is a matter of economic and national security"

Government scheme helps UK chip start-ups raise £10 million

From new fertility treatments to improving the efficiency of AI, British semiconductor innovators are reshaping global technology.

ELEVEN SEMICONDUCTOR start-ups working on chips that make AI more efficient and create new lifesaving healthcare tech have joined a government-backed support service to help turn their research into business realities.

Semiconductor chips are fundamental to the technology that we interact with daily, underpinning everything from smartphones to AI and advanced medical devices.

The companies will be the second group to go through ChipStart, an incubator programme launched in October 2023 with £1.3 million of backing to nurture a new generation of chip designers and crowd in investment totalling nearly £20 million in commitments from private investment and grants to help drive economic growth.

POM Health is among the companies joining the second round of the programme. It is pioneering the use of semiconductors to create a wearable patch for continuous hormone monitoring. This technology could transform healthcare by enhancing fertility treatments, offering women precise, real-time insights into their hormonal health.

HeronIC, another new joiner to the programme, has developed a software design tool that quickly creates custom chips for AI applications, boosting their energy efficiency and increasing performance for complex tasks.

Minister for Science, Patrick Vallance said: “Innovation in semiconductors can underpin technological advancements in every field, from AI to consumer devices and healthtech. British researchers across the country are leading in R&D in this essential field and the support we are delivering through ChipStart is helping their ideas become reality.

“As well as the commercial success of the first cohort, the innovations ChipStart is supporting could help to change lives, from helping to develop new fertility treatments to optimising AI and extending the battery life of devices we use every day. We are making sure British science leadership converts to help address critical global challenges and drive economic growth.”

Following a first round that saw participants close over £10 million of funding from private investors and grants, with a total of nearly £20 million in commitments being finalised, ChipStart will continue to provide these early-stage semiconductor companies with:v Access to commercial design capability: Including the full Silicon Catalyst ecosystem, design tools, IP, and prototyping capability.

Commercial expertise and mentorship: Startups receive guidance from experienced semiconductor industry executives and connections to Silicon Catalyst’s global network.

Exposure to private capital: Access to over 270 Silicon Catalyst advisors, Strategic Partners, and an extensive network of investment groups.

On completion, the pilot will provide the UK’s semiconductor industry with a pipeline of new startups that have an innovative product, route to market, and are a foundation for future growth, including routes to future seed funding. Sean Redmond, Managing Partner, Silicon Catalyst UK commented: “ChipStart UK is leveraging the UK’s position as a global centre of semiconductor research to transform academic innovations into market-ready technologies.

“Nine of the eleven firms in the next group come from UK universities and are set to build on the success of the first cohort, which secured a strong position in the international semiconductor supply chain through private funding and global partnerships. After nine months of rigorous training, ChipStart has created over thirty new UK semiconductor executives, ready to scale their businesses towards global success.”

Total semiconductor equipment sales to reach record $109 billion

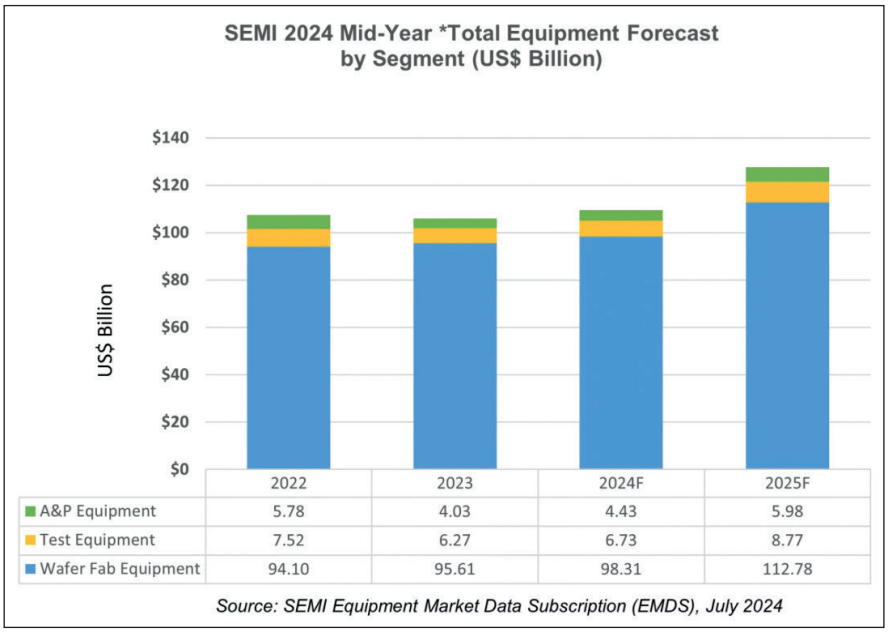
A round-up of some of the latest news announcements from SEMI, covering market intelligence, diversity, EU semiconductor strategy and flexible electronics.

GLOBAL SALES of total semiconductor manufacturing equipment by original equipment manufacturers are forecast to set a new industry record, reaching $109 billion in 2024, growing 3.4% year-on-year, SEMI announced today in its Mid-Year Total Semiconductor Equipment Forecast – OEM Perspective at SEMICON West 2024. Semiconductor manufacturing equipment growth is expected to continue in 2025, with sales forecast to set a new high of $128 billion in 2025, driven by both the front-end and back-end segments.

"The growth in total semiconductor manufacturing equipment sales already underway this year is forecast to be followed by a robust expansion of roughly 17% in 2025," said Ajit Manocha, SEMI president and CEO. "The global semiconductor industry is demonstrating its strong fundamentals and growth potential supporting the diverse range of disruptive applications emerging from the Artificial Intelligence wave."

Semiconductor equipment sales by segment

After registering a record $96 billion in sales last year, the wafer fab equipment segment, which includes wafer processing, fab facilities and mask/reticle equipment, is projected to increase 2.8% to $98 billion in 2024. This marks a notable increase from the previously forecasted $93 billion in SEMI's 2023 Year-End Equipment Forecast. Ongoing strong equipment spending in China and substantial investments in DRAM and HBM, driven by AI computing, drove the upward revision. Looking ahead to 2025, Wafer fab equipment segment sales are projected to expand 14.7%, reaching $113 billion due to increased demand for advanced logic and memory applications.



	2022	2023	2024F	2025F
A&P Equipment	5.78	4.03	4.43	5.98
Test Equipment	7.52	6.27	6.73	8.77
Wafer Fab Equipment	94.10	95.61	98.31	112.78

Source: SEMI Equipment Market Data Subscription (EMDS), July 2024

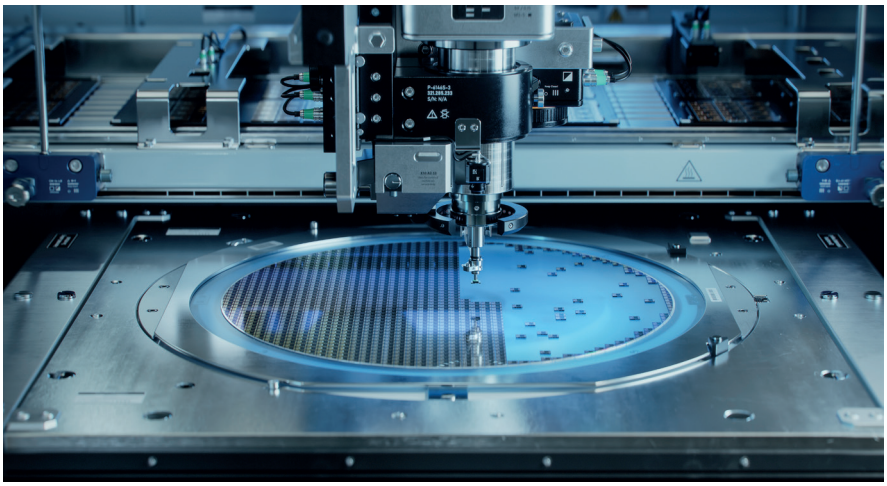
Following two years of contraction caused by challenging macroeconomic conditions and softening semiconductor demand, the back-end equipment segment is anticipated to start its recovery in the second half of 2024. Specifically, sales of semiconductor test equipment are projected to rise 7.4% to $6.7 billion in 2024, while assembly and packaging equipment sales are predicted to increase 10.0% to $4.4 billion in the same year.

Furthermore, back-end segment growth is expected to accelerate in 2025, with test equipment sales surging 30.3% and assembly and packaging sales increasing 34.9%. The segments' growth is supported by the increasing complexity of semiconductor devices for high-performance computing and the expected recovery in demand for automotive, industrial, and consumer electronics end-markets. Additionally, back-end growth is expected to increase over time to process ramping supply from new front-end fabs.

Wafer fab equipment (WFE) sales by application

The sales of Wafer Fab equipment for foundry and logic applications are expected to show a moderate contraction of 2.9% year-over-year to $57.2 billion in 2024 as a result of softening in demand for mature nodes and higher than expected sales for advanced nodes in the previous year.

The segment is forecast to grow 10.3% in 2025 to $63.0 billion, driven by increasing demand for leading-edge technology, the introduction of new device architectures, and increased capacity expansion purchases. Memory-related capital expenditures are projected to see the most significant increase in 2024 and demonstrate continued growth in 2025. NAND equipment sales are expected to remain relatively stable in 2024, with a 1.5% increase to $9.35 billion, as supply and demand normalize, setting the stage for a 55.5% expansion to $14.6 billion in 2025. Meanwhile, DRAM



equipment sales are projected to grow strongly at 24.1% and 12.3% in 2024 and 2025, respectively, supported by surging demand for high-bandwidth memory (HBM) for AI deployment and ongoing technology migration.

Semiconductor equipment sales by region

China, Taiwan and Korea are expected to remain the top three destinations for equipment spending through 2025. China is projected to maintain the top position over the forecast period as the region's equipment purchases continue to rise. Equipment shipments to China are projected to exceed a record $35 billion in 2024, solidifying its lead over other regions. While equipment spending for some regions is expected to fall in 2024 before rebounding in 2025, China is expected to see a contraction in 2025 following significant investments over the past three years.

The SEMI forecast is based on collective input from top equipment suppliers, the SEMI Worldwide Semiconductor Equipment Market Statistics (WWSEMS) data collection program and the industry-recognized SEMI World Fab Forecast database.

Worldwide silicon wafer shipments increase 7%

Worldwide silicon wafer shipments increased 7.1% quarter-over-quarter to 3,035 million square inches (MSI) in the second quarter of 2024, but saw an 8.9% decline from the 3,331 million square inches recorded during the same quarter last year, the SEMI Silicon Manufacturers Group (SMG) reported in its quarterly analysis of the silicon wafer industry.

"The silicon wafer market is recovering driven by strong demand related to products for data centers and generative AI," said Lee Chungwei (???), Chairman of SEMI SMG and Vice President and Chief Auditor at GlobalWafers. "While the recovery is uneven across different applications, 300mm wafer Q2 shipments indicated 8% quarter-over-quarter growth for the best performance among all wafer sizes. There are a growing number of new semiconductor fabs under construction or ramping production volume. This expansion, along with the longer-term trend toward a $1 trillion semiconductor market, will inevitably require more silicon wafers."

Data cited include polished silicon wafers, including those used as virgin test wafers, as well as epitaxial silicon wafers, and non-polished silicon wafers shipped by the wafer manufacturers to end users.

SEMI Europe-led consortium launches to boost diversity

SEMI has launched a consortium organized by the European Commission's Erasmus+ programme to enhance Diversity, Equity, and Inclusion (DEI) in the European microelectronics sector. SEMI Europe and the new 11-partner European Chips Diversity Alliance (ECDA) consortium will develop an innovative and robust partnership between academia and industry to lower barriers to joining the microelectronics workforce for underrepresented groups, with the goal of growing the competitiveness of Europe's broader electronics industry.

SEMI logoECDA will support the EU Chips Act to address microelectronics industry's skills shortage, attract new talent, and support the emergence of a trained workforce to enhance Europe's technological advancement. A €1.5 million grant provided will fund the alliance for three years. "The European Chips Diversity Alliance is a momentous endeavor with participation not only from companies, but also academia and social organizations to propel our industry forward.", said Laith Altimime, President of SEMI Europe.

European chips diversity alliance

ECDA aims to formalize DEI as a key tenet of the Pact f?r Skills and put it at the heart of economic, educational, and industrial policies for Europe. ECDA seeks to boost innovation through multidisciplinary, learner-centered curricula on DEI for the microelectronics sector.

"The European semiconductor industry will need to grow its workforce to reach manufacturing capacity expansion targets and seize innovation and market opportunities," said Cassandra Melvin, Senior Director of Business Development and Operations at SEMI Europe. "ECDA will be a key link to eliminate biases and promote a skilled workforce that is inclusive and reflective of the world we live in."

The European Chips Diversity Alliance consortium consists of the following organizations:
SEMI Europe - Germany
Comenius University - Slovakia
Comet Yxlon - Germany
ESCP - Germany
EudaOrg - Ireland
Innovazione Apprendimento Lavoro Friuli Venezia Giulia (IAL-FVG) - Italy
Learnovate - Ireland
Merck - Germany
MIDAS - Ireland
Platform Talent voor Technologie (PTVT) - Netherlands
X-FAB - France
The consortium will release a report on the current state of DEI in the European microelectronics industry later this year.

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CEA-Leti launches FAMES Pilot Line

CEA-Leti held the kick-off meeting in June of the FAMES Pilot Line, a pioneering project aimed at advancing semiconductor technologies in Europe.

THIS INITIATIVE aligns with the ambition of the EU Chips Act, which seeks to bolster EU semiconductor capabilities and ensure technological sovereignty.

The pilot line will develop five new sets of technologies:

- FD-SOI (with two new generation nodes at 10nm and 7nm),
- Several types of embedded non-volatile memories (OxRAM, FeRAM, MRAM and FeFETs),
- Radio-frequency components (switches, filters and capacitors),
- Two 3D integration options (heterogeneous integration and sequential integration), and
- Small inductors to develop DC-DC converters for Power Management Integrated Circuits (PMIC).

Invented by CEA-Leti, FD-SOI is a planar CMOS technology that offers the best PPAC-E (Performance, Power, Area, Cost and Environmental impact) for mixed circuits (mixing digital, analogue and radio-frequency blocks).

FD-SOI has been adopted by global semiconductor leaders due to its tight electrostatic control at the transistor level and because it is well suited for highly innovative power-management technologies.

The booming FD-SOI market is therefore anticipating the 10nm and 7nm next-generation nodes. No less than 43 companies throughout the electronic-systems value chain, from materials providers and equipment manufacturers to fabless companies, EDAs, IDMs, system houses and end-users from ITC, automotive, medical device or space and security markets, have formally expressed their support for the FAMES initiative, prefiguring a vibrant ecosystem of start-ups, SMEs and other global industry leaders.

"By integrating and combining a set of cutting-edge technologies, the FAMES Pilot Line will open the door to disruptive system-on-chip architectures and provide smarter, greener and more efficient solutions for future chips. The FAMES project will indeed pay special attention to semiconductor sustainability challenges," said Jean-René Lèquepeys, CTO of CEA-Leti.

"The Chips Joint Undertaking (Chips JU) is proud to contribute to this strategic initiative and strengthen the EU's sovereignty in a critical domain. This pilot line will advance essential semiconductor technologies, while maintaining a strong focus on sustainability, and foster the collaboration between several European actors. The Chips JU aims to act as a catalyst and a model for further public and private collaborations in key areas," explained Jari Kinaret, the Chips JU executive director.

The FAMES Consortium brings together an outstanding group of partners: the pilot line coordinator, CEA-Leti (France), imec (Belgium), Fraunhofer Mikroelektronik (Germany), Tyndall (Ireland), VTT (Finland), CEZAMAT WUT (Poland), UCLouvain (Belgium), Silicon Austria Labs (Austria), SiNANO Institute (France), Grenoble INP-UGA (France) and the University of Granada (Spain). The five new technologies will create market opportunities for low-power microcontrollers (MCU), multi-processor units (MPU), cutting-edge AI and machine learning devices, smart data-fusion processors, RF devices, chips for 5G/6G, chips for automotive markets, smart sensors and imagers, trusted chips and new space components.

The pilot line will be accessible to all EU stakeholders (universities, RTOs, SMEs and industrial companies) and all like-minded countries through annual open calls and upon request, following a fair and non-discriminatory selection process.

The project will benefit from funding that will be provided in equal parts by participating member states and the Chips JU.

CEA-Leti presents complementary developments in 3D Integration Technologies

CEA-Leti scientists presented three papers at the IEEE Symposium on VLSI Technology and Circuits detailing the institute's progress on 3D integration technologies, which are a promising approach for designing More than Moore systems, especially radio frequency (RF) integrated systems. 3D integration techniques enable high-density CMOS transistors to coexist with transistors made of III-V materials, which can reach power levels and frequencies

unattainable with conventional silicon technologies. Potential applications include communications, the internet of things, medical devices and automotive sensing.

RF performances are competitive with other 3d solution

The paper, "Hybrid Integration of 3D-RF Interconnects on AlGaN/GaN/Si HEMT RF Transistor featuring 2.2W/mm Psat & 41% PAE @28GHz using a Robust and Cost-Effective Chiplet Heterogeneous Bonding Technique", reports the stacking of an AlGaN/GaN/Si high electron mobility transistor (HEMT) on coplanar-waveguide (CPW) lines fabricated on 200mm silicon trap-rich substrate. The HEMT and CPWs lines were interconnected with copper pillars (CuPi) using a high-yield chiplet heterogeneous integration process.

"Thanks to the integration of low insertion loss CuPi interconnects – 0.1dB@28GHz and a careful management of the heat dissipation within the 3D structure – the HEMT transistor features an output power density of 2.2W/mm @10V & a peak PAE of 41 percent," the paper reports.

"These RF performances are competitive with other 3D solutions found in the literature," said Alexis Divay, lead author of the paper. "Our industrial-grade 3D assembly approach is highly promising for fabricating efficient and cost-effective 3D-RF III-V systems."

Results lay the groundwork for using 3D technologies to enable RF applications

The paper, "First Radio-Frequency Circuits fabricated in top-tier of a full 3D Sequential Integration Process at mmW for 5G applications", details how for the first time 5G-compatible (30GHz) RF circuits have been stacked directly above a working digital circuit. The analog silicon RF circuits, sequentially fabricated at 500°C above a digital circuit layer with a 28nm FD-SOI industrial platform, presented performance in line with standard, thermal-budget FD-SOI devices.

"Both top- and bottom-tier circuits are fully functional with good performance after the 3D-SI process," said lead

authors José Lugo and Jean-Baptiste David. "Moreover, we explored a worst-case scenario to assess potential detrimental impacts of the ultra-thin proximity between analog-RF circuits and the digital layer. The work demonstrated the feasibility of vertical co-integration without any degradation, despite the close vicinity of both tiers. These results lay the groundwork for using 3D technologies to enable to RF applications."

CEA-Leti creates a path toward a second step in 3D silicon-integration development

The paper, "Breakthrough processes for Si CMOS devices with BEOL compatibility for 3D sequential integrated More than Moore analog applications", reports unlocking low-temperature "showstoppers" in versatile analog high-voltage (>2.5V) BEOL (400°C) devices.

"We demonstrated for the first time the nanosecond laser annealing, solid-phase epitaxial regrowth on a complete device, which surpasses the low-temperature, dopant activation technological showstopper," said Daphnée Bosch, lead author of the paper.

With this paper, CEA-Leti creates a path toward a second step in 3D-silicon integration development with 400°C top devices stackable above a less resilient bottom tier

The paper notes that the work also "demonstrated monocrystalline silicon devices with a CMOS-compatible poly gate thanks to nanosecond laser annealing in melt regime and junction dopants activation without diffusion at 400°C." This preserves the engineered junction profile. "HPD2 final anneal cures low-temperature gate stack, achieving performances in line with planar analog CMOS technology."

Co-author Perrine Batude said some of CEA-Leti's industrial partners already have introduced a part of its vision: a second device layer integrated sequentially using monocrystalline channel bonding above a bottom device. However, the top pixel MOSFETs are currently processed at 1,000°C.

"With this paper, CEA-Leti creates a path toward a second step in 3D-silicon integration development with 400°C top devices stackable above a less resilient bottom tier," she said.

Fourth Paper

A fourth paper presented by the institute at the conference covered "A Current-Source-Free Constant-Current Wireless Adiabatic Neural Stimulator Achieving a 5.5-27.7x Improved RF-to-Electrode Stimulation Efficiency Factor".

Paving the way for the semiconductor future

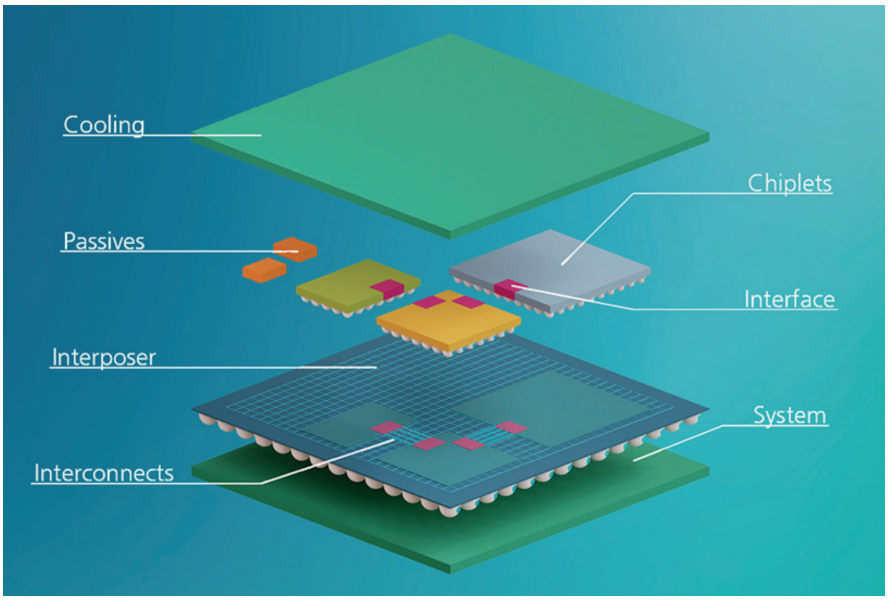
The Chiplet Center of Excellence commences operations.

THREE FRAUNHOFER INSTITUTES have launched a forward-looking research initiative in Dresden: the Chiplet Center of Excellence (CCoE). Its purpose is to partner with industry to drive forward the introduction of chiplet technology. Researchers at the CCoE are working on several fronts for the automotive industry, developing the first workflows and methods for electronics design, demonstrator construction, and the evaluation of reliability.

"Chiplets will play a critical role in the global semiconductor industry in the years ahead because this technology offers the greatest freedom possible for customizing the design of electronics systems. This makes it all the more important for European industry to have a coordinated roadmap for the incorporation of chiplets into its own products," says Andy Heinig, department head at Fraunhofer IIS/EAS and head of the Chiplet Center of Excellence (CCoE). "That's why it's essential for companies to be able to assess the feasibility of chiplet-based system solutions early on. For this reason, at the CCoE we take the wide range of requirements and constraints these products have and convert them into practical workflows and new evaluation processes."

The aim of the CCoE is to do all it can to support the competitiveness and technological sovereignty of strong European industrial sectors. For the first two years, the CCoE will therefore focus on applications in automotive electronics. These efforts will bring together a range of key partners all along the value chain – from car manufacturers to semiconductor companies.

The Fraunhofer researchers want to provide these partners with methodological approaches, architectural concepts, reusable basic components, and roadmaps for the development, manufacture, and robust



design of chiplets. In addition, the CCoE assesses a variety of chiplet solutions in terms of their performance, cost, and reliability. The research findings will flow into international standards and play a role in shaping a multi-vendor chiplet ecosystem.

What sets the CCoE apart is Fraunhofer's expansive portfolio in electronics development and manufacture, as well as the close interdisciplinary collaboration with industry. The CCoE is operated by the Dresden-based Engineering of Adaptive Systems EAS division of the Fraunhofer Institute for Integrated Circuits IIS, the Fraunhofer Institute for Reliability and Microintegration IZM and its division All Silicon System Integration Dresden – ASSID as well as the Fraunhofer Institute for Electronic Nano Systems ENAS.

Companies interested in participating in the CCoE's pre-competitive activities and shaping its research agenda have until fall 2024 to sign up. For more information about the CCoE and ways to get in touch, visit **https://www.chiplet-center.fraunhofer.de/en.html**

EU project ARCTIC joins forces towards the era of scalable control technology for quantum processors

Quantum computing is currently seen as the most promising contender to efficiently solve problems which are completely out of reach for classical computers. Whereas research on qubits is long established, developing the control machinery is at least as important for scaled systems, yet is still in its infancy. Project ARCTIC brings together 36 partners from industry, academia and leading RTOs to establish a complete and comprehensive European supply chain for and develop scalable, reliable, innovative control infrastructure for cryogenic quantum processors. The EU is funding the project with over € 11 million for a duration of three years.

A quantum computer requires an enormous amount of control and interfacing to function. For quantum computers based on qubits operated close to absolute zero Kelvin inside a cryostat, the number of possible signal lines fed from the machinery into the cryostat is currently limited due to the restricted space, the heat transported

through the wires and the signal integrity due to long wires.

"The performance requirements asked from electronic devices and circuits at cryogenic temperatures are quite different compared to those at room temperature. Especially when interfacing very sensitive applications such as quantum processors, all aspects of microelectronic technologies need to be optimized," says Alexander Grill, scientific leader of ARCTIC ("Advanced Cryogenic Technologies for Innovative Computing") at imec.

The expected project outcomes are considered as important enablers for highly demanded technologies that can resolve existing problems in areas such as computational chemistry, bio and life sciences, cryptography needed for data protection and cyber security.

To overcome these constraints, ARCTIC brings together 36 partners from industry, academia and leading RTOs to establish a complete and comprehensive European supply chain for cryogenic photonics, microelectronics, and cryo-microsystems around the emerging quantum computing industry and different cryo-enabled ICT applications.

Fraunhofer IPMS will contribute competencies in characterization of commercial semiconductor devices The Center Nanoelectronic Technologies (CNT) at the Fraunhofer IPMS focuses on the characterization and modelling of bipolar and CMOS-transistors as well as memory elements at cryogenic temperatures.

The emphasis will be put on high frequency, noise and defect characterization and modelling of commercial transistors in 22FDX FDSOI technology as well as the development of optimized non-volatile ferroelectric memories. For this, it is crucial to improve characterization methods in cryogenic environment and on full wafers and to generate a deep understanding of how field-effect transistors and memory devices behave at untypically low temperatures.

"We want to gain new insights into the energetic position and number of electrical defects in the transistors. This will allow the industry to offer new cryo-designated products and Fraunhofer to offer unique characterization methodologies for industry products. The reduction of defect induced noise in electronics is an important factor for increasing the coherence time of qubit states, that is why the developed methodologies are directly relevant for cryogenic quantum computing approaches.

Regarding the non-volatile memories it is furthermore important to minimize the power consumption of the devices, since the cooling power is very limited inside of cryostats" explains Dr. Maik Simon, researcher within the Quantum Technologies group at the CNT in Dresden, Germany.

Another demonstration of IPMS's competences is investigating the applicability of non-volatile ferroelectric three-terminal memories for a cryogenic environment by electrical characterization and physical modelling. This pioneering study will reveal how the devices perform at low temperatures and what parameters can be altered to enhance switching characteristics, integration density and reliability.

The project at the Fraunhofer IPMS is co-financed by the German Federal Ministry of Education and Research (BMBF) and the Saxon State Ministry for Economic Affairs, Labour and Transport (SMWA).

CROSSHEAD
Fraunhofer IPMS remains important research partner for GlobalFoundries Dresden

The Fraunhofer Institute for Photonic Microsystems IPMS is expanding its long-standing collaboration with the leading international semiconductor manufacturer GlobalFoundries and launches several research projects on innovative integrated memory concepts.

The Center Nanoelectronic Technologies (CNT) at Fraunhofer IPMS is researching new processes and concepts for memory modules in GlobalFoundries chip technologies within several research projects on behalf of GlobalFoundries. In addition to the development of processes for the 22nm FDX® technology, the focus of the development projects that have now been launched lies on the optimization of magnetic, ferroelectric and resistive embedded data storage. An important goal is to develop scalable and energy-efficient memory solutions. This is particularly advantageous for the Internet of Things and automotive sectors.

The research projects are being implemented on behalf of GlobalFoundries as part of the "Important Project of Common European Interest" (IPCEI), which is funded proportionately by Saxony and the federal government and was launched in 2023.

Reasons for GlobalFoundries' cooperation with the CNT at Fraunhofer IPMS are the excellent technical expertise of its more than 100 employees, the immediate vicinity in the north of Dresden and the research clean room with standard industrial equipment on 300mm wafer size, which is unique in Germany. Only this unique selling point makes a fast and efficient exchange of wafers and research results with fabs such as GlobalFoundries possible.

Wenke Weinreich, Head of CNT and Deputy Director of Fraunhofer IPMS, is pleased with the continuation of the cooperation with GlobalFoundries Dresden alongside the new projects and proudly emphasizes: "It is an honor to continue to be an important research partner of GlobalFoundries Dresden. With these projects that have now been launched, we are working together to ensure that Dresden continues to occupy a leading position in global microelectronics."

Dr. Manfred Horstmann, General Manager of GlobalFoundries Dresden, adds: "The teams at the Center Nanoelectronic Technologies at Fraunhofer IPMS and GlobalFoundries are perfectly attuned to each other. We are therefore delighted to be continuing our proven collaboration in the field of research under the umbrella of IPCEI. The results will make a significant contribution to the further strengthening of the Central German semiconductor cluster."

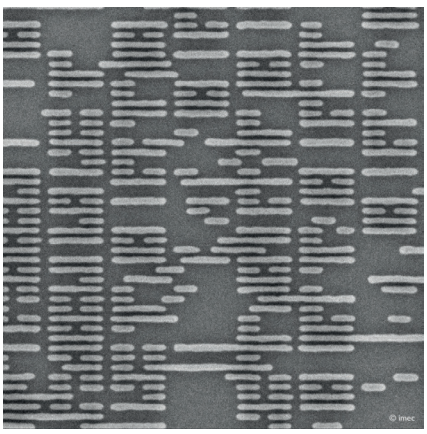
Imec demonstrates logic and DRAM structures using high NA EUV lithography

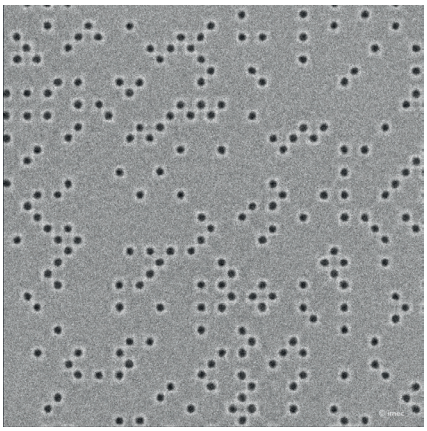
Results confirm readiness of the High NA EUV patterning ecosystem for enabling future logic and memory use cases.

IMEC PRESENTS patterned structures obtained after exposure with the 0.55NA EUV scanner in the joint ASML-imec High NA EUV Lithography Lab in Veldhoven, the Netherlands. Random logic structures down to 9,5nm (19 nm pitch), random vias with 30nm center-to-center distance, 2D features at 22nm pitch, and a DRAM specific lay out at P32nm were printed after single exposure, using materials and baseline processes that were optimized for High NA EUV by imec and its partners in the framework of imec's Advanced Patterning Program. With these results, imec, confirms the readiness of the ecosystem to enable single exposure high resolution High NA EUV Lithography.

Following the recent opening of the joint ASML-imec High NA EUV Lithography Lab in Veldhoven, the Netherlands, customers now have access to the (TWINSCAN EXE:5000) High NA EUV scanner to develop private High NA EUV use cases leveraging the customer's own design rules and lay outs.

Imec has successfully patterned single exposure random logic structures with 9,5nm dense metal lines, corresponding to an 19nm pitch, achieving sub 20nm tip-to-tip dimensions. Random vias





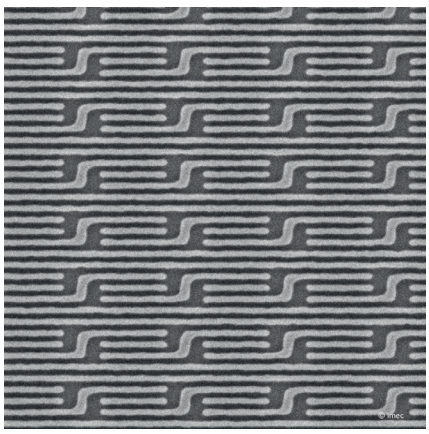
with a 30nm center-to-center distance showcased excellent pattern fidelity and critical dimension uniformity. Furthermore, 2D features at a P22nm pitch exhibited outstanding performance, highlighting the potential of High NA Lithography to enable 2D routing.

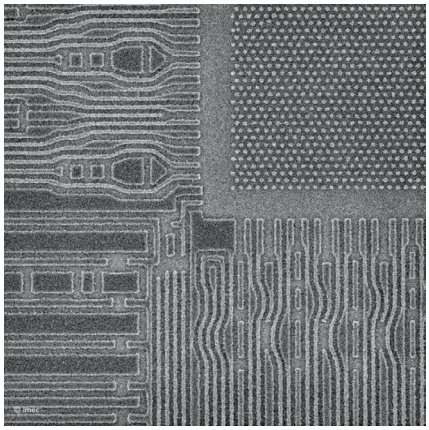
Beyond logic structures, imec successfully patterned, in a single exposure, designs that integrate the storage node landing pad with the bit line periphery for DRAM. This achievement underscores the potential of High NA technology to replace the need of several mask layers by 1 single exposure.

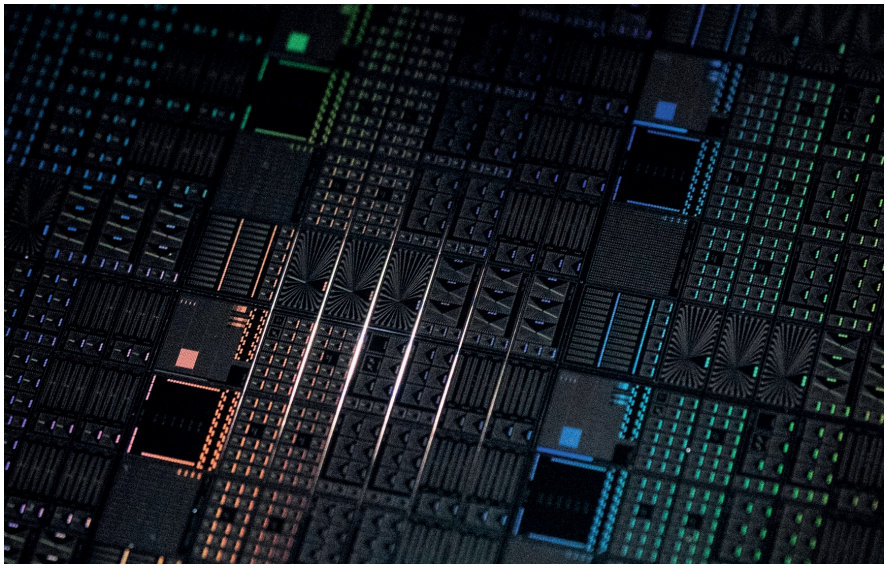
These breakthrough results follow intensive preparatory work by imec and ASML – in close collaboration with its partners – to ready the patterning ecosystem and metrology for the first generation of High NA EUV Lithography. Prior to the exposures, imec prepared dedicated wafer stacks (including advanced resists, underlayers and photomasks), and transferred High NA EUV baseline processes (such as optical proximity correction (OPC), integrated patterning and etch techniques) to the 0.55NA EUV scanner.

Steven Scheer, senior vice president of compute technologies & systems / compute system scaling at imec: "We are thrilled to demonstrate the world's first High NA-enabled logic and memory patterning in the joint ASML-imec lab as an initial validation of industry applications. The results showcase the unique potential for High NA EUV to enable single-print imaging of aggressively-scaled 2D features, improving design flexibility as well as reducing patterning cost and complexity. Looking ahead, we expect to provide valuable insights to our patterning ecosystem partners, supporting them in further maturing High NA EUV specific materials and equipment."

Luc Van den hove, president and CEO of imec: "The results confirm the long-predicted resolution capability of High NA EUV lithography, targeting sub 20nm pitch metal layers in one single exposure. High NA EUV will therefore be highly instrumental to continue the dimensional scaling of logic and memory technologies, one of the key pillars to push the roadmaps deep into the 'angstrom era. These early demonstrations were only possible thanks to the set-up of the joint ASML-imec lab allowing our partners to accelerate the introduction of High NA lithography into manufacturing.".







Imec achieves record-low charge noise

Imec has also announced the demonstration of high quality 300mm-Si-based quantum dot spin qubit processing with devices resulting in a statistically relevant, average charge noise of 0.6µeV/ÖHz at 1Hz. In view of noise performance, the values obtained are the lowest charge noise values achieved on a 300mm fab-compatible platform. Such low noise values enable high-fidelity qubit control, as reducing the noise is critical for maintaining quantum coherence and high fidelity control. By demonstrating those values, repeatedly and reproducibly, on a 300mm Si MOS quantum dot process, this work makes large-scale quantum computers based on Si quantum dots a realistic possibility.

Si quantum dot spin qubits are promising building blocks to realize large-scale quantum computers for two main reasons. First, Si spin qubits with long quantum coherence times (a metric reflecting their ability to store quantum information for a long time) and high-fidelity quantum gate operations have been repeatedly demonstrated in lab environments and are therefore a well-established and tested technology with realistic prospects.

Second, and potentially more importantly for the long-term viability, the underlying technology is compatible and intimately linked with CMOS manufacturing technologies and as such offers the possibility of wafer-scale uniformity and yield with the required advanced back-end-of-line interconnection of the Si quantum dot structures that are needed for truly large scale quantum chips, with millions or even billions of qubits operating in synchrony.

Several types of Si quantum dot spin qubits exist and are being pursued at imec. In this work, the quantum dot spin qubits were defined by metal-oxide-semiconductor (MOS) quantum dot structures that resemble modified transistor structures to trap a single spin of an electron or hole. To achieve long quantum coherence times, the noise, and in particular the charge noise of the quantum dot should be as low as possible. That noise generally results from residual charges, trapped nearby or even inside the quantum dot, removing those is key to increase the performance of the spin qubits.

Ultimately, this is determined by the full processing stack of the quantum dot qubit structure, since any defects introduced there need to be minimized. While this can be realized through lab-based techniques such as very gentle lift-off processes that reduce process damage, industrial manufacturing techniques like subtractive etch and lithography-based patterning have shown to easily result in degradation of the device and interface quality, particularly at the Si/SiO2 interface nearby the quantum dot qubits. As a result, the charge noise of Si/SiO2-based quantum dot structures manufactured in professional fabrication facilities is typically higher than the values obtained using lab-based processing.

By careful optimization and engineering of the 300mm Si/SiO2-based MOS gate stack, imec achieved a record-low average charge noise level of only 0.6µeV/ÖHz (at 1Hz), across 300 mm wafers and characterized using statistical methods. Kristiaan De Greve, imec Fellow and Program Director Quantum Computing at imec: “We demonstrated charge noise levels that, depending on the source, are between half an order of magnitude to one order of magnitude lower, when compared to current state-of-the-art fab-based Si quantum dot structures and achieved remarkably uniform quantum dot operation. Our results confirm that 300mm Si MOS is a compelling material platform for quantum dot spin qubits and highlight the maturity of industrial fabrication techniques for qubit development.”

In addition, the statistical analysis methods used to characterize the low charge noise devices revealed fundamental insights into their origin. “Knowing the source of the charge noise will give us directions to further optimize the quantum dot structures,” De Greve adds. “The low-noise qubit environment and demonstrated uniformity of the CMOS manufacturing are just the start of a series of enabling technology developments for upscaling quantum chips towards eventual practical quantum computing, which, with current understanding, will require millions of physical qubits.”

The results above were published in a Nature Partner Journals paper.

Precision sealing for advanced semiconductor manufacturing:
Greene Tweed leads the way

The semiconductor industry is poised to double to $1 trillion in six years, putting pressure on manufacturers to scale up. As a global leader in FFKM Chemraz® sealing solutions, Greene Tweed knows that second-best seals won't cut it in an industry as complex and challenging as semiconductor manufacturing. Discover how the company is stepping up its game to ensure that chipmakers have everything they need to thrive in this era of unprecedented growth.

HISTORIANS could call the 2020s the 'new Roaring 20s' — the decade of artificial intelligence (AI). The AI boom started when the world woke up to the promise of generative AI. Momentum is building as 2024 is promising to be the year of adoption for several AI applications. McKinsey research shows that the trend will continue, and generative AI could enable automation of up to 70 percent of business activities by 2030, adding trillions of dollars in value to the global economy.

These AI applications and their insatiable demand for data heavily rely on semiconductors for processing and storage. Unsurprisingly, McKinsey expects the global semiconductor market to double to $1 trillion by 2030, raising the stakes for manufacturers who need to scale up to keep up with the demand. On top of that, the growth in AI is also pushing them toward more powerful smaller processor nodes so that they can fit more increasingly complex transistors on a single chip, resulting in more intricate designs.

This complexity translates to more advanced manufacturing processes with harsher conditions. Manufacturing processes often require extremely high temperatures and aggressive chemicals and harsh plasmas, posing significant risks to materials and components in the equipment. The entire operation occurs in cleanrooms where

even microscopic particles of dust or slight chemical contaminant can cause defects and compromise the performance and reliability of the chip being made.

When it can't fail

In this dizzying race to build new fabs, semiconductor manufacturers are not only exploring advancement in chip design, materials, and architectures but also need a steady supply of several inconspicuous yet indispensable components, such as Greene Tweed's Chemraz® seals, critical for manufacturing new advanced chips.

Greene Tweed, a global leader in Perfluoroelastomer (FFKM) Chemraz® sealing solutions, is leading the way in this rise with its own multi-million-dollar investments in facilities and several new products and manufacturing automation technologies.

"Several prominent chipmakers depend on Chemraz® seals to fabricate their most powerful chips and second-best seals aren't good enough for their challenging manufacturing environments," says Shawn McCloskey, Chief Commercial Officer of Greene Tweed. "We are fully committed to supporting our customers and ensuring that they have the sealing solutions they need to meet the soaring needs for semiconductors."

This criticality of Chemraz® sealing solutions is growing as chipmakers turn to more demanding processes. Thyag Sadasiwan, General Manager of Chemraz® at Greene Tweed explains why, "Our Chemraz® o-rings and sealing solutions meet the critical demands of modern chip fabrication by preventing contamination while withstanding aggressive chemicals and extremely high temperatures. As a result, these sealing solutions outperform and outlast in the world's harshest semiconductor manufacturing applications."

Another factor making Chemraz® seals indispensable is the increased need for ultraclean processing in the more advanced manufacturing applications. Being the first sealing solutions company to use cleanroom manufacturing in the US, Greene Tweed fully understands the significance of ultraclean operations in the semiconductor industry and ensures that our seals control particle excursions that could cause contamination while improving uptime and boosting wafer yield.

Rising to the challenge

Scaling up to provide chipmakers the solutions they will need during the anticipated boom won't be easy. But the recent industry-wide supply crunch gripping the FFKM materials that coincided with a global surge in demand for chips gave us valuable insights into how to meet the burgeoning demand and minimize the impact of possible disruptions.

Building on the insights, Greene Tweed is rolling out six major initiatives to ensure that we are able to promptly deliver their high-performing Chemraz® sealing solutions, as the customer needs evolve to meet the growing demand for semiconductors:

1. New manufacturing facility in Korea

Greene Tweed is investing to expand its global manufacturing capacity and capabilities for the semiconductor market. An excellent example is the newly constructed 70,000 square feet (6,500 sq m) facility in Ochang, Cheongju-si, Chungcheongbuk-do, Korea. This factory is equipped with end-to-end manufacturing process capabilities – from initial extrusion of raw materials to warehousing of the finished products. We have started producing samples and will transition to commercial production later this year.

Featuring cleanroom space to maintain a pristine environment vital for components supporting chip fabrication, the facility will initially focus on Greene Tweed's flagship Chemraz® product line known for its superior performance in demanding semiconductor applications. It doesn't just increase the global capacity but also underscores the company's commitment to supporting customers based in Korea and the surrounding region, including notable semiconductor leaders. It will help improve lead times, build stronger co-development strategies with key customers, and enhance business continuity plans, implementing a healthier global supply chain.

The state-of-the-art plant is equipped with advanced manufacturing technology as well as solar panels and greywater recycling facilities to mitigate environmental impact.

What's more, the new facility is designed with scalability in mind and offers ample room for growth, enabling us to expand our production capabilities as demand increases. We will be implementing a phased rollout of new production lines. In the next few years, we will increase capacity and add automated equipment to enhance our production processes and reduce lead times. In the next phase, we will focus on further expansion, including an

additional cleanroom, and integrating cutting-edge manufacturing technologies and processes.

This long-term strategy ensures that we remain agile and responsive to our customers' evolving needs as the demand for semiconductors grows over the rest of the decade and beyond.

2. New innovations designed for harsh conditions and expansion

As a global leader in FFKM seals, Greene Tweed knows that Chemraz® seals are critical for the most advanced semiconductor fabrication processes. To support our customers' growing needs, Greene Tweed has introduced two new high-performing, price-competitive products – Chemraz® G38 and G57.

"With an unwavering focus on performance and supply chain resiliency, we are developing several new Chemraz® products to meet the evolving needs of various plasma applications while being highly price competitive and delivering world-class lead times. The additions demonstrate our commitment to continuously innovating and responding to the demands of the market, ensuring that our customers have the best solutions at their disposal," says Thyag Sadasiwan.

Custom-engineered to meet the demands of aggressive dry plasma systems, Chemraz® G57 provides improved plasma resistance and minimizes contamination, resulting in less downtime and higher wafer processing yields in both static and dynamic oxide etch wafer processing applications. It offers excellent chemical resistance and can withstand temperatures up to 572°F (300°C) and is ideal for several applications, such as endpoint windows, window seals, slit valve seals, bell jar seals, isolator valve seals, chamber seals, valve seals, lid seals, KF fitting seals, and gas inlet seals.

Chemraz® G38 is developed for high-density plasma systems where seal reliability and minimal contamination are essential. It provides excellent chemical compatibility and withstands a variety of aggressive chemicals. Recommended for bonded gate seals and chamber seals, it delivers exceptional value in applications such as deposition, remote plasma cleans, oxidations, diffusion, ion implant, implant anneal, and rapid thermal processing.

This journey of innovation continues, and another Chemraz® sealing solution is ready to roll out in the next six to 12 months. In addition, our existing sealing solutions, including Chemraz® and Fusion® F07 fluoroelastomer, are being adopted by customers to meet the increasing needs of semiconductor fabrication and subfab plants being built around the world.

3. Next-Gen manufacturing to accelerate growth

Greene Tweed is committing significant resources to automate manufacturing processes to scale capacity and quickly meet the growing needs of semiconductor customers as they evolve.

By supplementing core manufacturing processes with robotics and digital solutions, the company is supporting production floor employees to eliminate process bottlenecks and enable shorter lead times. The largest investments have been made for high-

impact process steps, like compression molding, inspection, and packaging, to maximize efficiency and productivity gains. For compression molding, operators are currently responsible for moving and servicing molds between every cycle.

An automated solution has been developed that uses a 6-axis robot to move molds, allowing the operator to focus only on the value-added activities and service more molding presses. Similarly, for current packaging operations, operators are responsible for bagging and labeling parts individually which is slow and tedious.

An automated solution has been developed that utilizes multiple SCARA robots and an automatic bagging machine to improve throughput and standardize bagging quality. Additionally, digital twins are being built and utilized to proactively evaluate the new innovative technologies and how to best introduce them into existing manufacturing facilities.

These technologies and dedicated technical resources are transforming production lines, making them more adaptable, and allowing us to scale up quickly to meet our customers' needs without compromising on excellence.

4. Secured resources

Expanding manufacturing capacity is just one prong of the multifaceted strategy to prepare for an upturn in a market as cyclical as semiconductors. To support world-class lead times, Greene Tweed has secured a reliable supply of raw materials from multiple suppliers to cover the anticipated ramp over the next two years.

Running four factories with balanced workloads, the company has significantly increased the workforce to stabilize the production process and bolstered manufacturing capabilities with multiple new equipment in the Korea, Taiwan, and Selma plants. These strategic moves are designed to not just keep up with growth, but also enhance production capabilities, minimize delays, and excel in delivery times.

5. Fortified supply chain resiliency

As Greene Tweed works to secure a steady supply of raw materials, the company is proactively reducing reliance on a single vendor or a market. Here's why: The industry-wide FFKM supply crunch during the pandemic-led surge in demand for semiconductors taught us the significance of diversifying and strengthening the supply chain. That's why Greene Tweed has carefully selected multiple sources of raw materials located in separate regions.

Proactively identifying and mitigating potential risks ranging from geo-political to regulatory and climate change events, Greene Tweed has built a comprehensive supply chain resiliency and business continuity plan and shared it with customers to ensure transparency.

Running four factories with balanced workloads, the company has significantly increased the workforce to stabilize the production process and bolstered manufacturing capabilities with new equipment in the Korea, Taiwan, and Selma plants. These strategic moves are designed to not just keep up with growth, but also enhance production capabilities, minimize delays, and excel in delivery times

By securing raw material and building supply chain resiliency, Greene Tweed enables its customers to reduce downtime and meet the incredibly tight production schedules needed to meet the fast-increasing demand during the anticipated boom. That can be critical in the semiconductor industry, where missing a time-to-market window can shrink revenues considerably.

6. Ready for the new design at tool OEMs

Major semiconductor capital equipment manufacturers are upgrading their tools to move to smaller processor nodes and the resultant complex processes. Whether it's the latest innovations in lithography or etching, they are creating an increased demand for wafer equipment seals and Greene Tweed is taking proactive steps to keep up with this growth. Greene Tweed's patented LF10 coating has allowed equipment manufacturers to meet the stringent performance of the next-generation semiconductor nodes.

At the same time, our bonded slit valves, lip seal, seals for electroplating solutions, vacuum line solutions, cryogenic seals and many other sealing solutions continue to be widely adopted by equipment makers. Most recently, our Xyfluor® materials were qualified in electrostatic chuck solutions requiring temperatures below - 40C.

Ready for growth

Building cutting-edge semiconductor chips is a challenging and cost-intensive process that hinges on small yet essential components such as Chemraz® sealing solutions.

Working closely with its customers and partners, Greene Tweed is ready to address the burgeoning need for its Chemraz® sealing solutions from chipmakers, ensuring the scalability and sustainability of their operations for the rest of the decade and beyond.

Powering progress:

sustainability initiatives driving change in the semiconductor industry

As the global demand for electronic devices, artificial intelligence, machine learning, and high-performance computing continues to surge, the semiconductor industry faces escalating pressure to address its carbon footprint. Although semiconductor companies are making sustainability commitments, more action is needed to achieve net zero.

BY JIM STRAUS, VICE PRESIDENT OF SALES AND SERVICE, ACM RESEARCH

THE ENVIRONMENTAL COST of semiconductor manufacturing is becoming increasingly problematic as the need for advanced technology accelerates. The energy demand is rising as chip design grows more intricate, with semiconductor fabrication facilities operating as some of the most energy-intensive facilities in the world.

Decarbonization efforts also serve as another driver for chip production. Semiconductors are a key component of green technologies such as renewable energy and electric vehicles, facilitating the transition toward a greener economy. On average, electric cars contain about 2,000 chips, roughly double the number of chips in a non-electric car. The number of power semiconductors used in the global renewable energy market is expected to grow with a compound annual growth rate of 8% to 10% from now through 2027.

Many end customers are also putting pressure on suppliers, including semiconductor companies, to step up their efforts to reduce greenhouse gas emissions to achieve net-zero carbon emissions along their entire supply chain. Suppliers and stakeholders are taking heed of these requests, voicing and prioritizing sustainability to accelerate the transition toward a more environmentally responsible future.

To find key strategies and innovations that will drive positive change, companies within the semiconductor industry are pursuing innovative sustainability initiatives to help reshape the landscape of semiconductor manufacturing. From resource-efficient production processes to the development of eco-friendly materials, the semiconductor sector is embracing sustainability as a core principle for future growth.

Closely engaging with customers on developing and refining process technologies that promote the three R's—reduce, reuse, and recycle – is critical to advancing the industry's next-zero trajectory. ACM Research embraces this shift toward more environmentally friendly manufacturing processes and facilities by incorporating chemical reduction, defect reduction, and yield improvement into its proprietary technologies.

Reduction of sulfuric acid and hydrogen peroxide mixture (SPM) usage and raw materials management

Many of the chemicals involved in the production of semiconductors are hazardous and have environmental implications if not handled and disposed of properly. Managing the procurement, storage, and safe disposal of these chemicals adds to the complexity and cost of the manufacturing process.

To help customers reach sustainability goals, leading semiconductor chipmakers have embraced the circular economy concept, which focuses on reducing, recycling, and reusing materials in a closed loop. With chip production requiring many scarce natural resources, the reduction or reuse of chemicals and materials can significantly

decrease its environmental impact. Companies are setting ambitious sustainability goals with the aim of improving waste-management practices and lowering CO_2 emissions through product usage. Efforts to reduce CO_2 emissions extend to semiconductor fabrication and beyond.
For example, ACM Research promotes the reduction of SPM usage with cutting-edge cleaning systems. Sulfuric acid, mixed with peroxide, is used primarily for the removal of organic materials, such as photoresist. It is considered one of the most widely used chemicals in semiconductor manufacturing and largely impacts the cost of manufacturing/production and the environment. The global electronic-grade sulfuric acid market is projected to reach $415M by 2026.

ACM Research's Ultra C Tahoe cleaning system implements a two-step approach to optimizing the advantages of wet-bench and single-wafer cleaning, thereby reducing energy usage and minimizing waste. About 80% of the sulfuric acid can be reduced, leading to approximately $12M saved in sulfuric acid usage annually for a 100K wafer production line. Other strategies to consider for handling raw materials involve collaborating with suppliers to source materials with lower emissions, promoting sustainable mining and extraction practices for essential materials like rare-earth elements, and streamlining supply chain logistics to reduce transportation-related emissions.

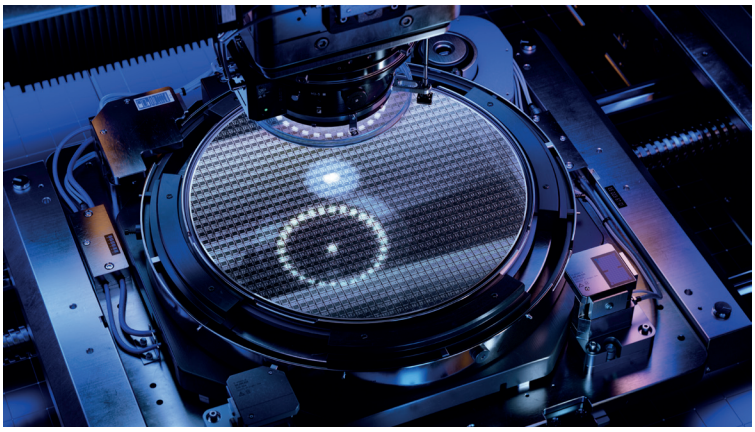
Water conservation and energy efficiency

During chip production, several million gallons of water are consumed daily, including ultrapure water (UPW) for multiple cleaning steps, cooling, and other applications. During chip production, water is used to rinse and clean silicon wafers, removing debris left from the manufacturing process. This operation requires UPW, which is thousands of times more pure than drinking water. It takes roughly 1,400 to 1,600 liters of municipal water to make 1,000 liters of UPW.

Water conservation and recycling have become necessary to avoid any interruptions in production. Water strategies typically target conservation and reclamation and may include investing in local water treatment.

Chip production at 28nm technology node requires nearly 6 liters of water per square centimeter of wafer, but in the advanced technology node (e.g., nanosheet levels), this figure rises to more than 14 liters. About 75% of the water in a semiconductor fab is used in the manufacturing process, primarily in chemical mechanical planarization and wet clean and etch.

Companies like ACM Research reduces its chemical usage through its H_2 functional water and SAPS Megasonix technology. These efforts help protect valuable water resources through effective water



usage and reduced processing time. The SAPS Megasonix cleaning technology initiates the formation of H radicals from H_2 functional water (dissolved H_2 gas bubble), generates surface passivation, and leads to better particle-removal efficiency with reduced deionized water usage.

Energy-efficient semiconductor manufacturing can manifest in a multitude of ways, such as implementing energy-efficient manufacturing processes and technologies, optimizing equipment and machinery to minimize their energy consumption, utilizing advanced cooling systems to reduce energy-intensive heat dissipation, and investing in renewable energy sources, such as solar or wind, to power manufacturing facilities. By developing semiconductor technologies that rely on lower power consumption, customers can create energy-efficient chips and devices that consume less electricity during use. Implementing product design strategies that prolong the lifespan of semiconductor devices also reduces the need for replacements. The recycling and reuse of semiconductor components and materials encourages long-term resilience.

Advancing customer sustainability goals and initiatives

Manufacturers and suppliers dedicated to helping customers achieve sustainability goals and reach their zero-waste-to-landfill goals can do so with tools and technologies designed to reduce, reuse, and recycle the chemistries used in wafer processing. As the semiconductor industry continues to play a pivotal role in powering the digital revolution, it is imperative that stakeholders prioritize sustainability to mitigate environmental impacts. Overall, sustainability is becoming a driving force in the semiconductor industry, with companies actively pursuing eco-friendly practices and solutions to reduce their carbon footprint.

The manufacturing chain for semiconductors is remarkably complex and relies on hundreds of different participants. A cohesive and collaborative approach to responsible environmental sustainability relies on efforts by suppliers, manufacturers, end-users, and regulators advocating for a fundamental change in the industry.

Why the mask world is moving to curvilinear

If you've been to a lithography or photomask technology conference lately, you've likely noticed a trend: many papers and talks on curvilinear masks, curvilinear OPC, curvilinear ILT, curvilinear mask process correction (MPC), and curvilinear mask formats. The photomask industry is experiencing a fundamental shift from Manhattan masks to curvilinear masks. Part 1.

BY LEO PANG, D2S, INC.

SO, WHAT IS the motivation for this shift? After decades of Manhattan mask design, what are the benefits of moving to curvilinear? First, let's look at some background on the technologies that set the stage for this shift to curvilinear masks.

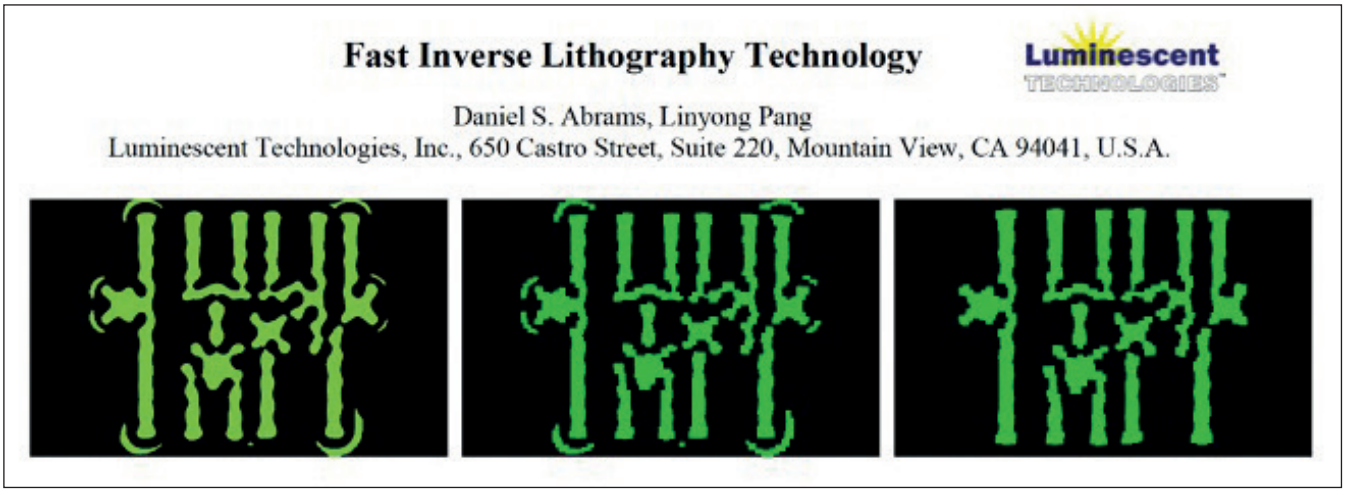
ILT started the shift

Curvilinear masks started with inverse lithography technology (ILT). ILT treats mask optimization as an inverse problem, starting with the desired wafer target and calculating the mask that will produce the desired wafer target. Wafer scanners have band-limited optics which cannot produce 90-degree corners, so any 90-degree corners (especially the tip of the corner, which has infinite frequency) will be filtered by scanner optics, and so are not included in ILT solutions. For this reason, ILT mask patterns were naturally curvilinear.

At the 2006 SPIE Advanced Lithography Conference, Dan Abrams and I presented the first ILT paper from Luminescent, "Fast Inverse Lithography Technology."[1] Luminescent and its partners published numerous papers that showed that ideal, fully curvilinear ILT mask patterns produced the largest process window[2-9].

Figure 1 shows the mask pattern created by this first ILT solution on the left. In the middle, is a "Manhattanized" version adapted to variable shaped beam (VSB) mask writers, which can only write rectilinear shapes. On the right of Figure 1 are the Manhattanized ILT mask patterns without sub-resolution assistant features (SRAFs).

Writing curvilinear mask shapes or their "Manhattanized" versions presented a very real



➤ Figure 1. Mask pattern created by this first ILT solution (left). "Manhattanized" version of the same pattern (center), Manhattanized ILT mask patterns without SRAFs. (right) [1]. Source: Luminescent/Synopsys.

roadblock, as the number of shots required to represent curvilinear shapes was prohibitively high. Since the VSB mask write time is proportional to the number of shots, it was not practical to write curvilinear masks with VSB mask writers.

Multi-beam mask writers, GPU computing change the game for curvilinear masks

The advent of multi-beam mask writers removed the mask write-time roadblock to adoption of curvilinear masks. Multi-beam mask writers have an array of hundreds of thousands beams, each of which can be turned on, off, or in fractional dose.

Since the write time is only proportional to area, it can write curvilinear masks without any penalty in write time, as shown in Figure 2.

The initial use of ILT in production was mainly in limited, "hotspot," areas. The reason was another roadblock: the difficulties in computing full-chip ILT solutions. One difficulty is runtime, but runtime can be handled by using GPU-accelerated computing. Feeding chip partitions into a GPU-accelerated computing system can speed the processing of each partition. However, when the partitions are "stitched" back together, errors occurred along the partition boundaries. These stitching errors and the re-computation required to address them were still show-stopping issues (Figure 3).

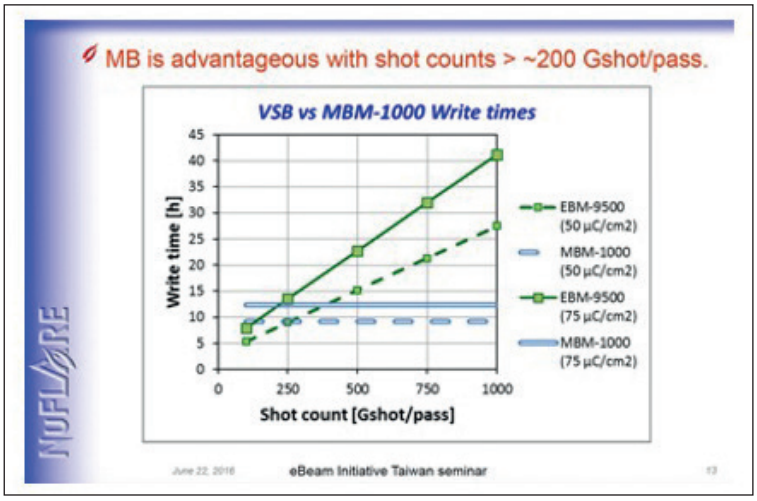
To avoid the time-consuming recursive correction passes necessary to resolve these stitching errors, in 2019, D2S presented [12] a new hardware/software co-designed solution that had the ability to process the entire chip at once: a computational platform that behaved as a single, giant GPU/CPU pair that could optimize full-chip data seamlessly, without partitions (Figure 4).

Today, with these roadblocks removed, the photomask industry's confidence in their ability to create curvilinear masks is very high. In 2023, a survey by the eBeam Initiative, an industry group that surveys industry leaders each year, asked about high-volume manufacturing of curvilinear masks.

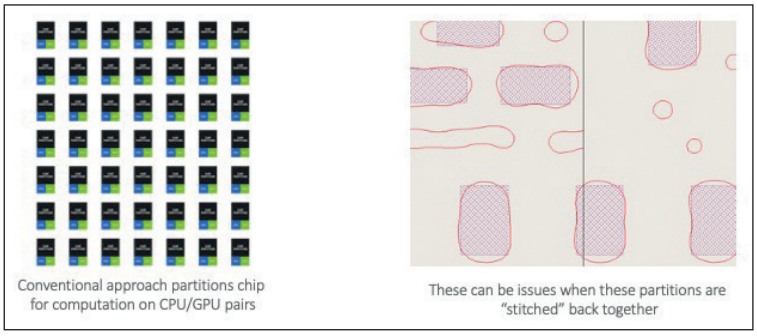
Figure 5. Results of the 2023 eBeam Initiative Luminaries Survey showing that 87% of the respondents are ready for at least a limited number of curvilinear masks. 33% can handle as many masks as there is demand[14].

The motivation for curvilinear masks: Improved process window at every node

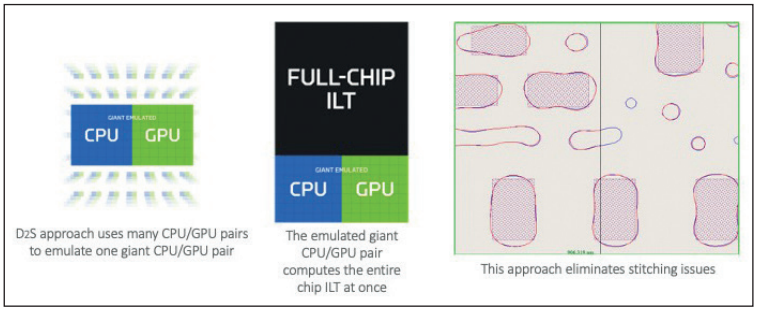
What has motivated to photomask industry to prepare for these changes is the demonstrated benefits of using curvilinear mask features. Dating back to the first ILT papers in 2006, numerous studies have shown curvilinear masks can improve process window for all technology nodes and lithography technologies, from



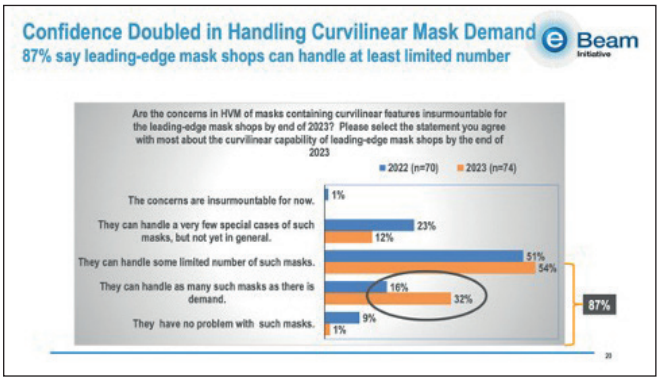
➤ Figure 2. Write times for VSB mask writers are proportionate to the number of shots required to create the mask shapes. Multi-beam mask writers are shape-agnostic, with a constant write time regardless of mask shapes[11]. Source: NuFlare.



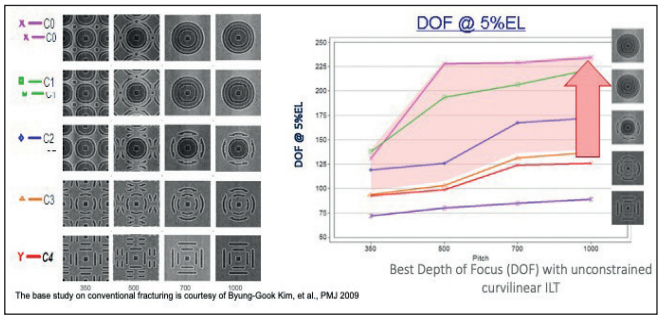
➤ Figure 3. The conventional full-chip approach partitions chips for computation on CPU/GPU pairs. Issues arise when the partitions are stitched back together[12]. Source: D2S.



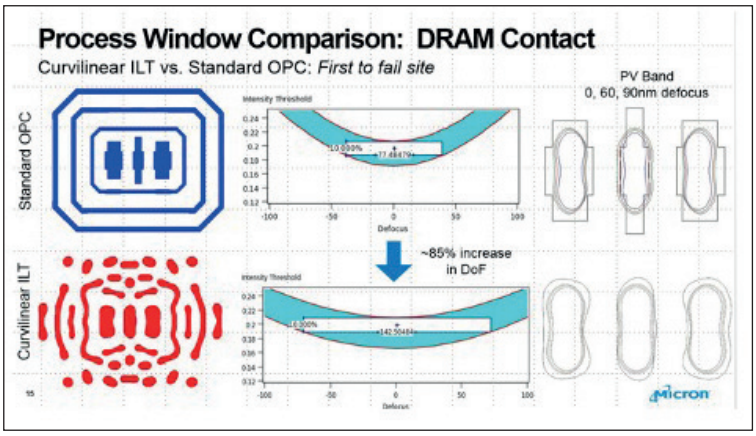
➤ Figure 4. A novel approach emulates a giant CPU/GPU pair that computes the entire chip at once, eliminating stitching issues[12]. Source: D2S.



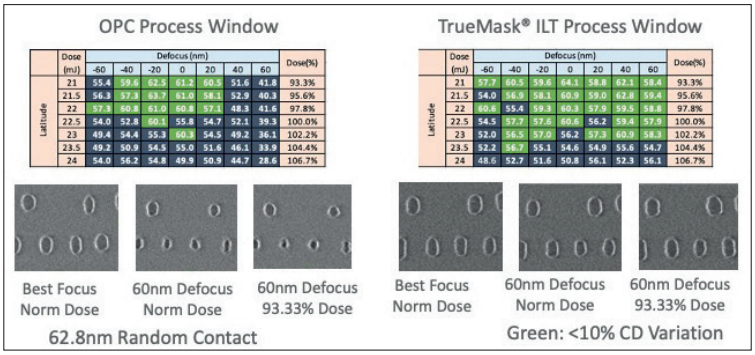
➤ Figure 5. Results of the 2023 eBeam Initiative Luminaries Survey showing that 87% of the respondents are ready for at least a limited number of curvilinear masks. 33% can handle as many masks as there is demand [14]. Source: eBeam Initiative.



➤ Figure 6. A study of a contact array using varied levels of curvilinearity. The best depth of focus was achieved by the unconstrained curvilinear ILT [9]. Source: Samsung.



➤ Figure 7. Curvilinear ILT provides an 85% increase in depth of focus compared to standard OPC [13]. Source: Micron.



➤ Figure 8. Curvilinear ILT provides over 100% increase in process window on random contact layer compared to standard OPC using a multi-beam mask writer [12]. Source: D2S and Micron.

193 dry, 193 immersion, to EUV. One such study was conducted by Luminescent with Samsung[9] in 2009. As shown in Figure 6, curvilinear mask patterns for a contact array were generated with different pitches.

For each pitch, there was an unconstrained curvilinear ILT mask pattern and then simplified ILT mask patterns, all the way to just horizontal and vertical scaling bars very close to OPC. Then the wafer was printed with dose and focus matrix, and CDs were measured. When we look at the process window, you can see for every pitch the unconstrained curvilinear mask pattern always gives the largest depth of focus.

More recently, in 2020, Ezequiel Russell from Micron [13], showed that for the three contacts shown in Figure 7, using full curvilinear ILT can improve the depth of focus by 85%.

In 2019, I presented with Micron an over 100% improvement over OPC on process window using curvilinear ILT patterns created by the full-chip stitchless ILT solution described above and written using a multi-beam mask writer. (Figure 8) [12].

Curvilinear also enables smaller pitches, simpler mask rules

Some additional benefits of using curvilinear mask patterns are related to mask rules. First, curvilinear mask shapes can enable smaller pitches. A simple example representing part of a contact array is shown in Figure 9.

Minimum corner-to-corner mask rules limit how tightly you can pack the contact array. Just by changing the target mask shape of the contact from square to circular, using the same mask rules, the pitch can be reduced by 14%. Simply put, curvilinear contacts can be packed tighter than Manhattan contacts.

Curvilinear mask features also present the opportunity for greatly simplified mask rules, with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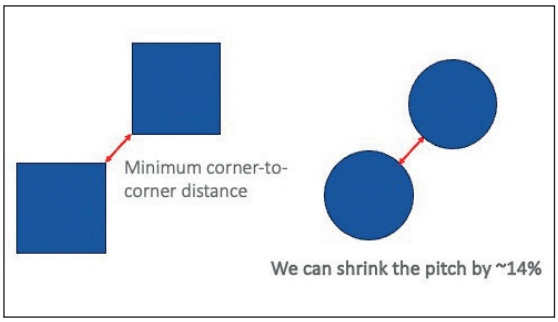
only minimum curvature, minimum CD, minimum space, and a minimum area required [15]. Figure 10 illustrates this using an intuitive example.

In this example (Figure 10), the size of the green ball represents the minimum CD. If the ball rolls along the contour inside a given pattern, and it doesn't get stuck, that means it satisfies the minimum CD rule. If it gets stuck somewhere, as shown with the red ball, that means the pattern violates the minimum CD rule.

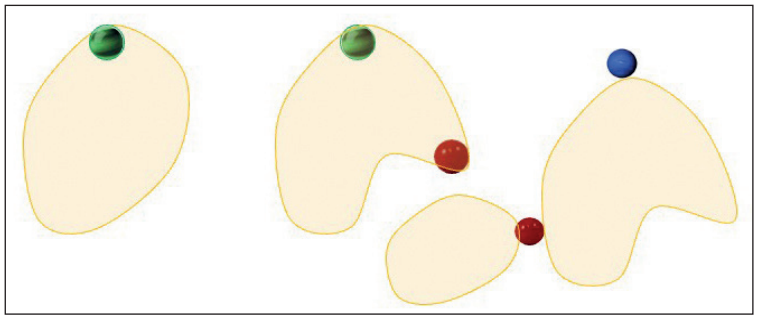
Similarly, you can roll the ball outside of the pattern to determine minimum spacing, as shown with the blue ball in Figure 10. Any overlaps into other patterns, as shown with the red ball, would be spacing violations. Of course, in practice, a fast, pixel-based algorithm tailored for GPU would be used to execute this concept.

Note: *This article is based on a paper from the author presented at SPIE Advanced Lithography 2024*[22].

Part 2 of this article will appear in SiS Issue 8, published in October.



➤ Figure 9. By moving from rectilinear to curvilinear mask features, pitches can shrink by 14%.



➤ Figure 10. A conceptualization of how design rules might be simplified for curvilinear masks, using only minimum curvature, minimum CD, minimum space, and a minimum area[15]. Source: D2S.

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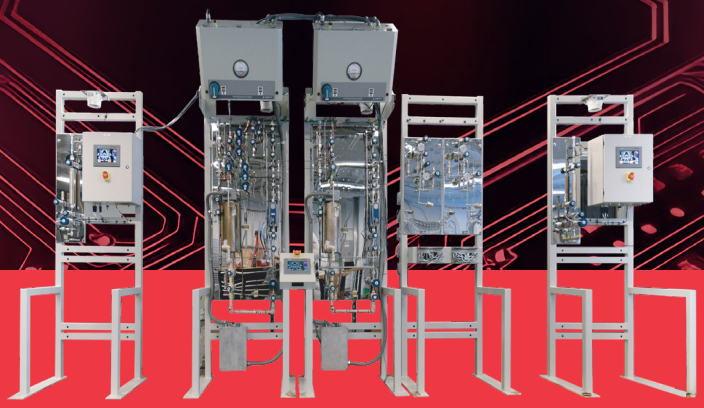

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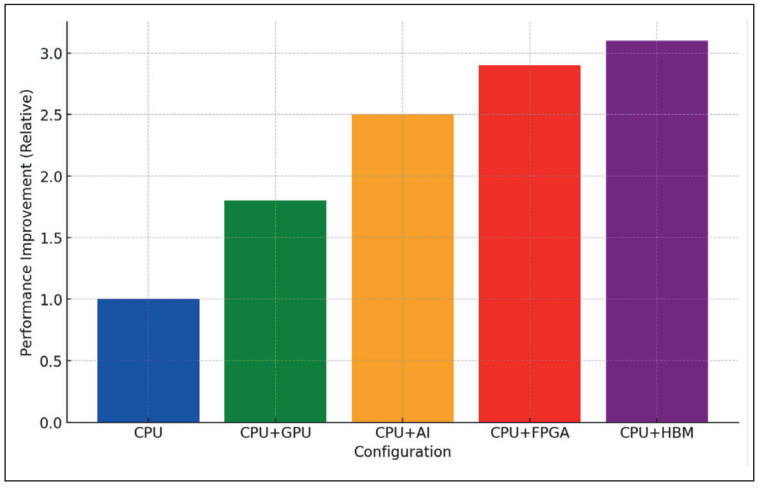
ATE testing challenges of heterogeneous silicon chips with advanced packaging

The semiconductor industry is rapidly evolving, driven by the increasing demand for more powerful, efficient, and versatile devices. This evolution has led to the development of complex heterogeneous semiconductor chips with ultra-high density and advanced silicon packages. These cutting-edge designs integrate various functionalities, materials, and technologies onto a single chip, making them incredibly powerful but also posing significant testing challenges in the manufacturing flow.

BY SRIHARSHA VINJAMURY, PRINCIPAL ENGINEER, SOPT, ARM INC

THE PUSH for heterogeneity in silicon packages is aimed at enhancing computational performance, energy efficiency, and system adaptability. By integrating various types of processors—such as CPUs, GPUs, FPGAs, and AI accelerators—these packages can optimize task execution. Heterogeneous integration enables specific processors to handle workloads they are architecturally optimized for, resulting in significant energy savings and performance boosts. Additionally, it facilitates system upgrades and customization, allowing new functionalities to be added without necessitating a complete system redesign. Enhanced thermal management techniques distribute the computational load more evenly, maintaining lower operating temperatures and improving component reliability.

This approach drives innovation, enabling bespoke solutions for applications ranging from hyperscale data centers to portable consumer electronics.



Silicon Performance improvements with heterogeneous Integration.

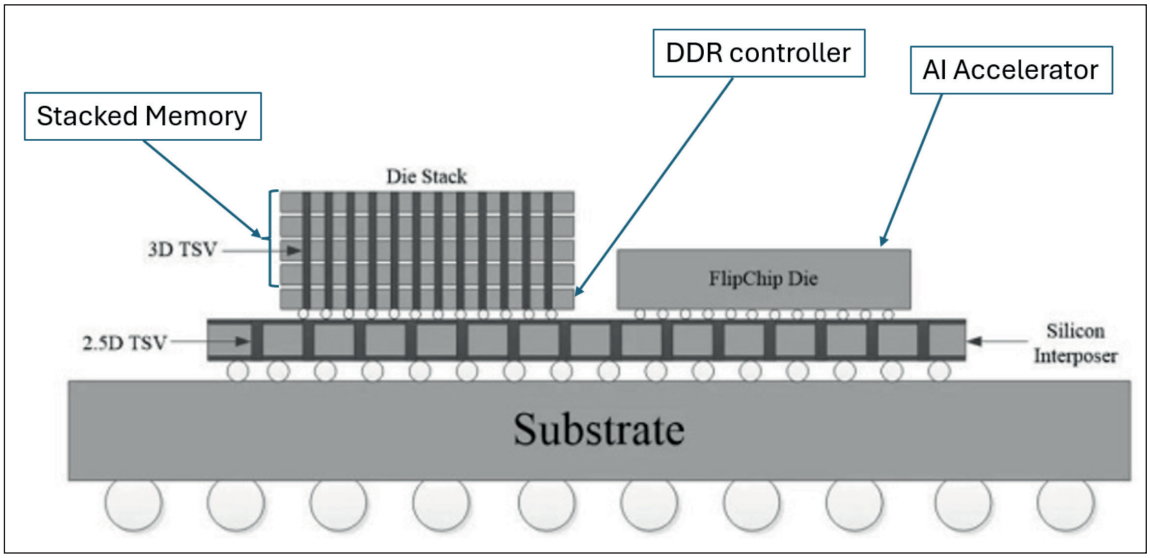
Furthermore, it is cost-effective, extending the operational lifespan of technology and minimizing the frequency and cost of updates.

A heterogeneous package with 3D HBM memory stacking and an AI accelerator chip

Challenges faced in Advanced Packages:
One of the primary issues in advanced packaging is material compatibility and selection. Ensuring strong adhesion between diverse materials such as organic substrates, silicon dies, and metal interconnects is critical. Poor adhesion can lead to delamination, impacting device reliability. Additionally, different materials have varying coefficients of thermal expansion (CTE), which can cause mechanical stress during thermal cycling, potentially resulting in cracks or warpage.

Lithography and patterning also pose significant challenges. Achieving precise patterning for redistribution layers (RDLs) and interconnects at sub-micron scales is difficult. Variations in these processes can cause electrical performance issues and reduce yield. Accurate alignment between multiple layers in multi-die or 3D ICs is crucial, as misalignment can result in connectivity failures and diminished performance.

The nano-scale lithography for the RDL layers pose issues for reduced line widths, requiring precise electromigration control. Integrating low-k dielectrics and novel metals demands strong adhesion and diffusion barriers. Efficient thermal management and stress-relief structures are crucial for differential CTE-induced stress. Maintaining high-frequency signal integrity and controlling defects in photolithography, etching, and plating are essential for yield and reliability in complex, high-density interconnects.



➤ A Heterogeneous Package with 3D HBM memory stacking and an AI accelerator chip.

Thin wafer handling is nothera major challenge in advanced packaging because thinning wafers to just a few hundred micrometers for 3D stacking makes them fragile and prone to breakage and warpage, necessitating special handling during processing. Through-silicon vias (TSVs) add another layer of difficulty with their complex etching and filling processes; defects here can seriously compromise performance and reliability. Additionally, TSVs can introduce stress that degrades silicon performance over time, especially under thermal cycling.

Thermal management is crucial as high-density interconnects and multiple dies generate significant heat, which needs to be efficiently dissipated to prevent overheating. This requires appropriate thermal interface materials (TIMs). Ensuring interconnect reliability is also tough, as high current densities can lead to electromigration, causing connection failures. Repeated thermal cycling adds stress that can crack interconnects over time.
In assembly and bonding, achieving reliable flip-chip bonding with micro-bumps demands precise control over bump formation, alignment, and reflow. Optimizing the underfill process is critical to protect solder joints from environmental stresses.

Managing yield and defects throughout the stages of lithography, etching, and bonding is vital, as any defects can significantly affect production efficiency. Environmental concerns like moisture sensitivity and outgassing must be managed to ensure long-term reliability. Finally, balancing cost and scalability is essential. Advanced packaging processes are inherently complex and expensive, requiring constant innovation and collaboration to maintain high yield and commercial viability.

These issues impact yield and introduce latent defects. Variations in these processes can lead to electrical performance issues, misalignments, and stress-induced failures, which are difficult to detect during Automated Test Equipment (ATE) testing. Defects like delamination, warpage, and electromigration often manifest under operational stresses, making early detection and effective fault isolation challenging, ultimately affecting the overall reliability and yield of the devices.

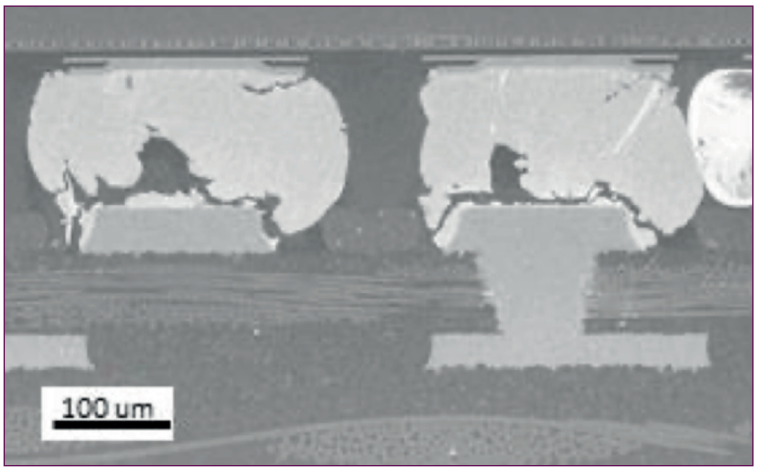
ATE testing overview

Automated Test Equipment (ATE) plays a pivotal role in evaluating large samples and is essential for the production testing of newly fabricated silicon chips. As a cornerstone of semiconductor manufacturing, ATE's primary job is to offer an automated, cost-effective testing solution that boosts device throughput significantly. By automating the testing process, ATE not only slashes the time and costs linked with manual testing but also enhances the accuracy and reliability of these tests. When combined with System-Level Testing (SLT), ATE creates a robust testing framework that supports the mass production of chips while upholding high quality standards.

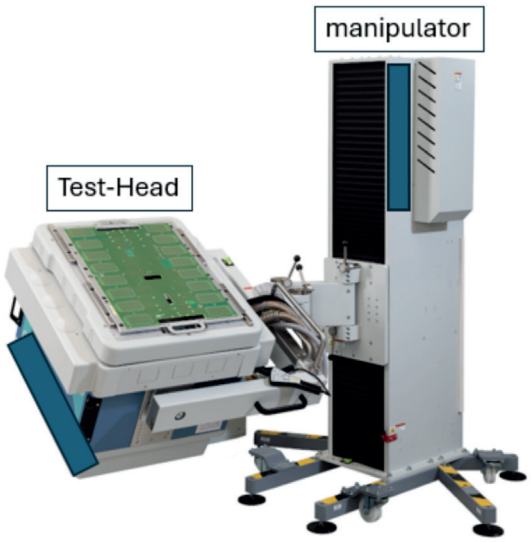
Types of Tests Conducted by ATE

Structural Testing:

- **Purpose:** Identify manufacturing defects in silicon chips.
- **How It Works:** DFT engineers use fault modeling to create test patterns for various faults.
- **Examples:** ATPG for Stuck-At Faults (SAF),



➤ Mechanical failure in RDL, source AMKOR.



➤ A Generic ATE test system.

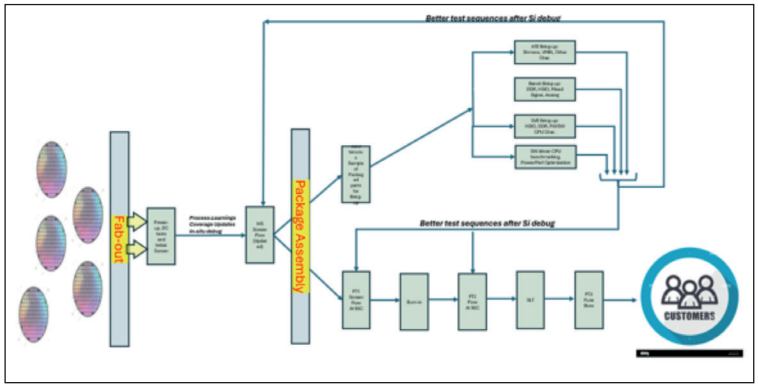
Transition Delay Fault (TDF), Boundary-Scan Description Language (BSDL)/Boundary Scan (BSCAN), Logic Built-In Self-Test (LBIST).

Functional testing:
- **Purpose:** Ensure the electronic device operates according to specifications.
- **Examples:** Testing a microcontroller to verify data processing and signal generation.

Parametric testing:
Purpose: Measure specific electrical parameters like voltage, current, and resistance.
Example: Checking power supply voltage levels within the specified range.

Integration flow: Tests are combined into a flow influenced by factors like wafer stage or final test stage, temperature conditions, and board complexity.

Additional testing for system-level performance and reliability:
- **System-Level testing (SLT):** Evaluate overall system performance.
- **Stress testing:** Assess robustness under extreme conditions.
- **Burn-In testing:** Identify early-life failures by running devices at elevated temperatures.
- **Environmental testing:** Evaluate performance under various conditions like humidity, temperature, and vibration.



➤ ATE testing NPI and Production Flow.

Key phases in Device Bring-up on ATE

The Bring-Up or New Product Introduction (NPI) phase is the initial but the most crucial stage in the lifecycle of Automated Test Equipment (ATE) operations, crucial for accurate and efficient testing of newly developed semiconductor devices before mass production. Key activities include system configuration and setup, test program development, debugging and validation across platforms, Internal part distributions, Providing Engineering and Customer Samples to the End customer and finally, flow optimization and production release. The Production Phase is the second and ongoing stage in ATE operations, focusing on high-volume testing and continuous improvement to ensure consistent high-quality and efficient manufacturing. Key activities include high-volume testing, ongoing calibration and maintenance, yield monitoring and improvement, test program updates, cost reduction and efficiency enhancements, and quality assurance and reliability testing.

Key process parameters are meticulously tracked at various stages and fed back to the fabs. The fabs provide Wafer Acceptance Test (WAT) parameters, allowing us to compare these metrics against design targets and make informed decisions. Given that Automated Test Equipment (ATE) operates in a volume-driven environment, advanced data analysis tools are essential for identifying systematic and random process-related patterns on the wafers. However, these issues can be latent, only manifesting during later stages of device aging. Detecting such latent defects during the testing phase is challenging, as it requires sophisticated fault isolation techniques and predictive analytics to ensure long-term chip reliability.

Challenges and recommendations faced in testing advanced packages

A single multi-die configuration constitutes different special-purpose components including CPUs, GPUs, memory arrays, analog/RF circuits, specialized accelerators, and so on. This increased complexity increases the functional verification and debugging requirements. The traditional methodologies developed for 2D testing are more likely to be inadequate and thus call for advanced techniques like hierarchical test methodologies and advanced Design-for-Testability architectures to increase Fault coverage and observability.

Low accessibility to deeper nodes
The vertical and horizontal integration of different dies in a heterogeneous package makes the access of internal nodes difficult for proper testing and debugging. The access mechanisms for all those nodes, without disturbing the functionality of the device, come through innovative solutions such as boundary scan testing, advanced BIST circuits, and micro-probing technologies. These techniques have enabled non-intrusive monitoring and diagnosis of embedded components with very little degradation of device performance.

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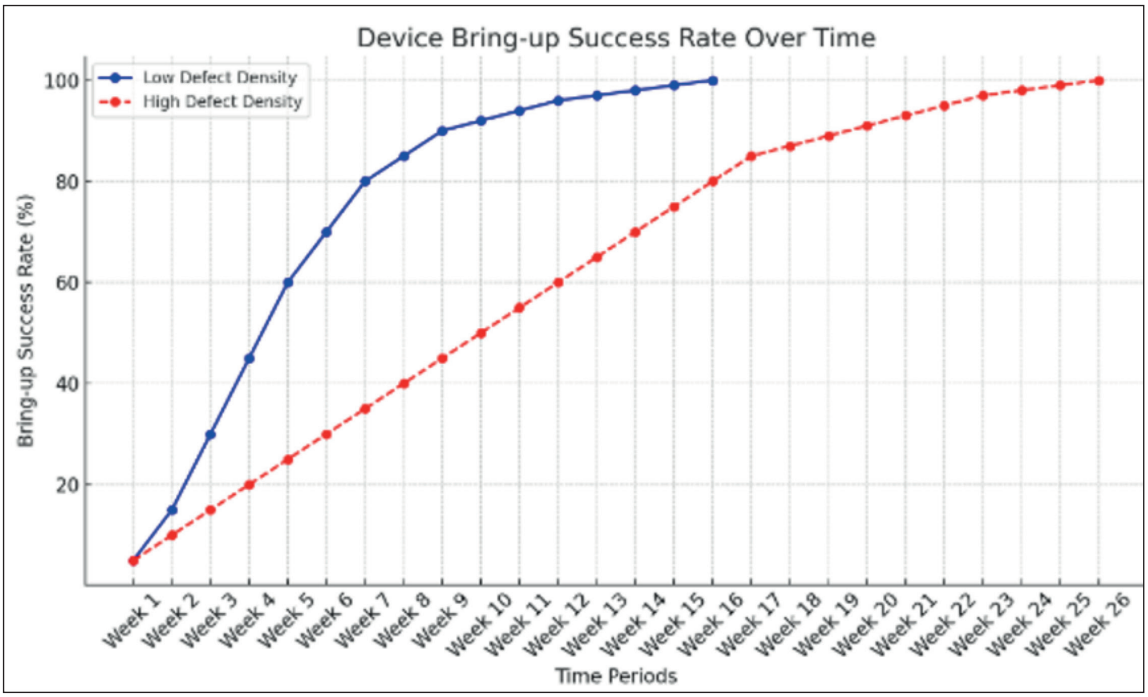


➤ ATE ramp-up timelines based on defect density.

Advanced ATPG algorithms, such as dynamic compaction, X-filling, and fault simulation, enhance test efficiency by generating highly compact test patterns, reducing test time, and improving fault coverage. Techniques like SAT-based ATPG leverage satisfiability solvers for complex fault detection, ensuring robust testing of intricate semiconductor designs. These methods address challenges in heterogeneous packages, ensuring high reliability and performance

Heat dissipation

The larger the number of high-performance active components that are integrated into heterogeneous packages, the greater the thermal management problems are. Advanced methods of heat dissipation shall be needed with thermal vias, microfluidic channels, and high conductivity TIMs. Efficient management of heat transfer minimizes thermal hotspots and ensures a constant distribution of temperature that does not result in thermal-induced performance degradation or device failure.

> “Key process parameters are meticulously tracked at various stages and fed back to the fabs. The fabs provide Wafer Acceptance Test (WAT) parameters, allowing us to compare these metrics against design targets and make informed decisions. Given that Automated Test Equipment (ATE) operates in a volume-driven environment, advanced data analysis tools are essential for identifying systematic and random process-related patterns on the wafers”

Thermal profiling

The bring-up phase itself is a critical part of discovering and mitigating potential thermal issues. Sophisticated thermal simulation tools such as Computational Fluid Dynamics and Finite Element Analysis are further combined with infrared thermal imaging to provide valuable details of thermal maps. These help in designing an effective cooling solution and instructing on where the die should be placed and what kind of materials to use for packaging.

Power delivery network design

It should ensure that there is stable and efficient power delivery with minimal IR drop and noise and power integrity issues for all the integrated components in heterogeneous packages. Advanced materials with superior electrical properties, on-die decoupling capacitors, and hierarchical schemes of power distribution could be applied to avoid higher current densities and intrinsic reduced noise margins in more densely integrated structures.

Advanced board designs

Designing advanced boards for next-gen silicon packages faces challenges like achieving ultra-high routing density with micro-vias and buried vias, maintaining signal integrity with controlled impedance traces, differential pair routing, and low-loss dielectrics, and ensuring power integrity with dedicated power/ground planes and decoupling networks. Effective thermal management requires integrated heat spreaders, thermal vias, pads, and metal-core PCBs. Precision manufacturing tolerances and enhanced inspection techniques like AOI and X-ray are essential for reliability.

High-speed design features such as via-in-pad technology and backdrilling reduce parasitic effects,

while embedded/co-packaged components improve performance. Advanced simulation tools for electromagnetic and thermal analysis optimize the design, and test sockets facilitate robust and repeatable testing of high-performance devices.

Defect density during production testing
Compared with traditional 2D chips, heterogeneous packages may involve more process-induced defect density because of an increased number of fabrication steps, additional die-to-die bonding, and more inter-component connections. Advanced defect inspection techniques, like e-beam inspection or AOI, must be combined with SPC for detecting defects and reducing them to improve yield rates.

Time-to-market challenges
High defect density in advanced silicon packages delays device bring-up and extends development timelines. Complex testing and debugging, including advanced ATPG, DDR, and high-speed I/O (HSIO) bring-up, require sophisticated protocols and extensive validation, significantly prolonging the process. Efficient thermal management and signal integrity maintenance demand detailed analysis and optimization, adding to development time.

Debugging intricate issues, such as timing violations and cross-talk in HSIO, can be time-consuming, further delaying deliverables. Power integrity challenges and ensuring robust manufacturing tolerances also contribute to extended timelines.

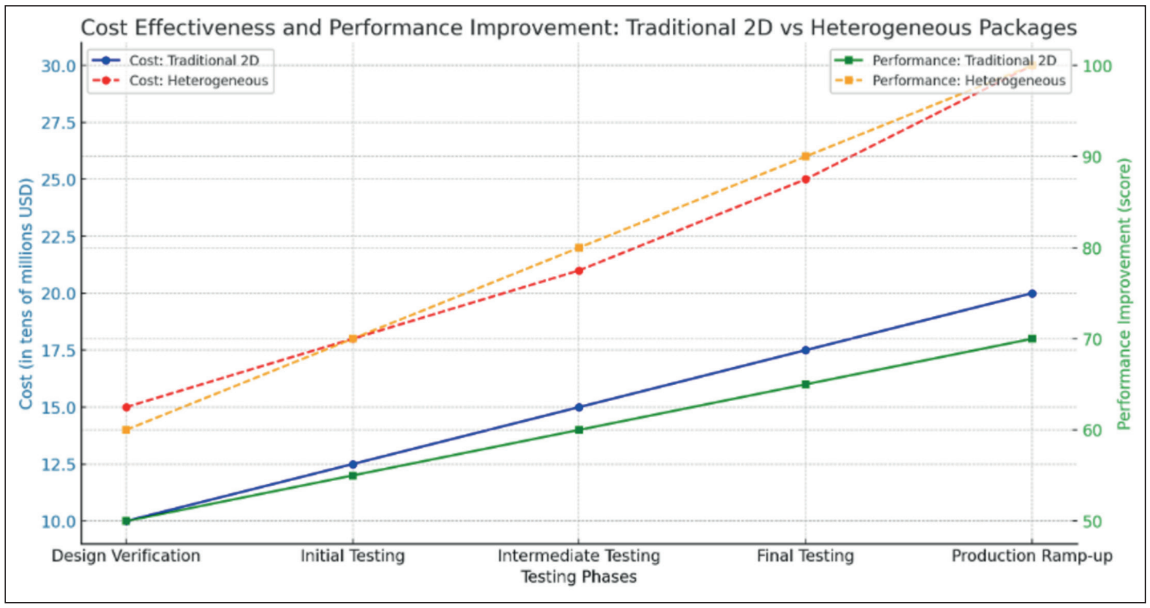
Inter-component reliability
To ensure the reliability of interconnections in heterogeneous packages, implement self-healing interconnects using conductive polymers or nano-composites that autonomously repair minor cracks. Utilize AI-driven predictive maintenance by analyzing real-time data from embedded sensors to anticipate and prevent failures. Integrate quantum dot-based stress sensors within interconnects for highly sensitive, real-time monitoring of stress and temperature. Develop adaptive thermal management systems that dynamically adjust cooling strategies using phase-change materials and microfluidic channels based on real-time thermal profiling. Employ advanced nanomaterials like graphene to create interconnects with superior electrical, thermal, and mechanical properties, significantly enhancing durability and performance under extreme conditions.

Cost effectiveness
The complex fabrication process and reduced yields at the start for heterogeneous packages can make them more expensive to produce. In order to have an economic package, balancing production costs against the market requirements includes enhancing the fabrication process, introducing lower cost-effective materials, and economies of scale. However, the Performance benefits Heterogenous integration offers precedes the cost of producing these chips.

Scalability
Increased demand for heterogeneous packages makes scalability an essential criterion. This means developing manufacturing techniques to be scaled up, like advanced lithography methods, wafer-level packaging, and automated assembly lines, so large-scale production can be attained without sacrificing quality or yield, answering the demand of the market. Increased demand for heterogeneous packages makes scalability an essential criterion. This means developing manufacturing techniques to be scaled up, like advanced lithography methods, wafer-level packaging, and automated assembly lines, so large-scale production can be attained without sacrificing quality or yield, answering the demand of the market.

Conclusion

The evolution of heterogeneous silicon chips with



➤ Cost versus performance between 2D monolithic and Heterogenous packages.

advanced packaging presents both significant challenges and unparalleled opportunities.

Addressing issues such as high defect density, complex thermal management, and ensuring inter-component reliability requires innovative solutions like advanced ATPG algorithms, AI-driven predictive maintenance, and self-healing interconnects.

While the initial cost and complexity of producing these advanced packages are higher, the substantial performance improvements and long-term benefits justify the investment. By leveraging cutting-edge technologies and methodologies, the semiconductor industry can achieve scalable, high-yield production, meeting the growing demand for more powerful, efficient, and adaptable devices.

Ultimately, these advancements will drive the next wave of innovation in fields ranging from data centers to consumer electronics, paving the way for a future where technology continues to evolve at an unprecedented pace.

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Advanced thermal control techniques to improve wafer manufacturing yield

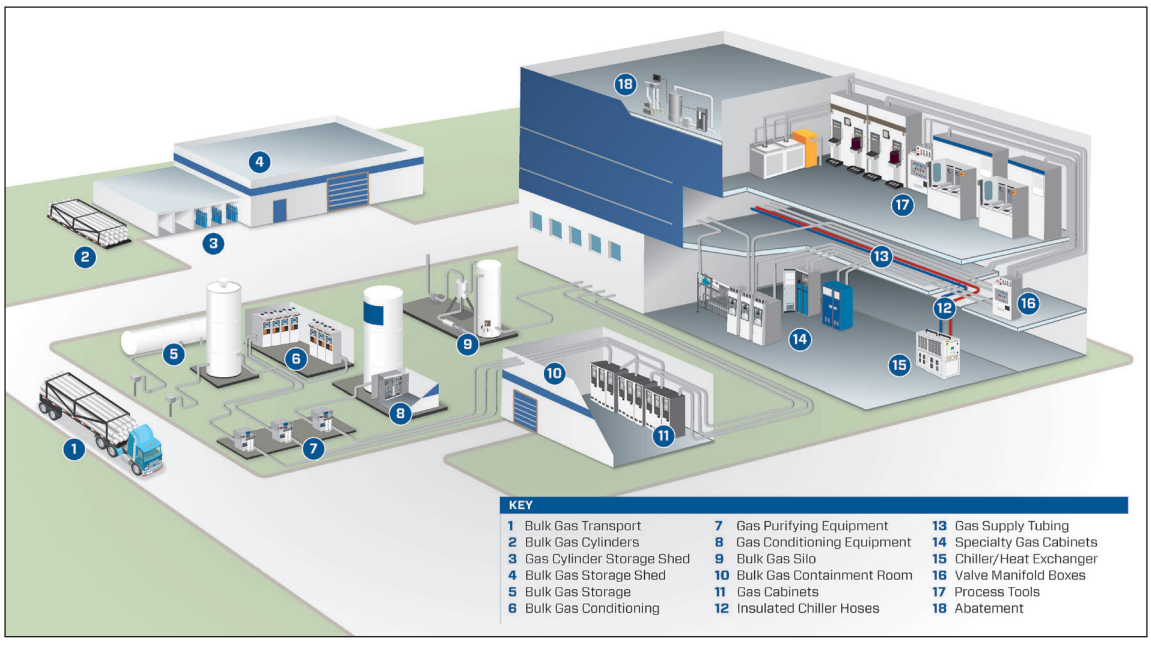
Finding hoses with proper insulation can mean the difference between success and failure.

BY MARGARET BRENNAN, PRINCIPAL ENGINEERING LEAD, APPLICATION SOLUTIONS, SWAGELOK COMPANY

Demand for high-quality semiconductor wafers has grown exponentially as artificial intelligence and other technological advances require more sophisticated chips. The process of creating the chips has never been more complex, and fabrication plants, OEMs, and all parts of the value chain are seeking new ways to maximize efficiency and improve profitability.

To maximize chip yields, the thermal loop is designed to keep deposition chambers at optimal temperatures throughout the manufacturing process. Ultralow temperatures are often used to regulate precise temperatures in the chamber. The challenge is that these temperatures, which can often be as low as -40°C, put additional pressure on each component of the thermal loop. This critical loop consists of chillers, pumps, heat exchangers, and all the components that keep them connected. A single malfunctioning component within that system can reduce fab efficiency and output.

Precision and cleanliness are also intersecting priorities in the world of semiconductor chip production. Temperatures inside the deposition chamber must be kept at optimized levels to ensure process stability. Simultaneously, the chamber must be kept entirely free of potential contaminants to maximize the throughput of chips during the delicate fabrication process.



➤ Figure 1. The lower area of a typical semiconductor fabrication operation houses key components of the facility's thermal loop, including insulated chiller hoses (12), gas supply tubing (13), specialty gas cabinets (14), plus a chiller and heat exchanger (15).

Because significant engineering and design go into creating and maintaining an ideal fabrication environment, it can be easy to overlook the importance of selecting some of the more "basic" components that support the chip production process. Consider an industrial hose, which is used in countless applications throughout manufacturing facilities. In the semiconductor fabrication process, hoses play an important role, as they are commonly used to help the chillers regulate the environment necessary for production processes.

Getting hoses and other system components right means paying attention to three critical areas that affect how components will function in the thermal loop, including:

- Choosing the right components
- Finding the right insulative balance
- Using proper installation and performance testing

Before constructing a thermal loop for a semiconductor wafer fab, it is crucial to understand the importance optimal temperature control. Finding suppliers who can guide engineers through this critical area and support the design and implementation of thermal loop construction will help fabricators optimize thermal management and maximize the number of high-quality chips produced.

How to keep fluid temperatures stable

Keeping temperatures at precise levels in the deposition chamber is essential to produce the highest-quality semiconductor chips. To regulate them, powerful chillers pump coolants into and out of the machine. The hoses that transfer coolants must be properly insulated to ensure temperatures remain stable throughout the fabrication process.

For example, if the natural temperature increase that occurs as fluid moves through the system is not accounted for when determining the cooling temperature and amount of insulation needed, it can cause out-of-tolerance temperature fluctuations within the chamber. These fluctuations may result in wafer defects, which can reduce yields.

Semiconductor manufacturers use water containing glycol to prevent freezing because it can withstand temperatures as low as -40°C. It is energy intensive to keep temperatures ultralow, so using insulated industrial hoses can help fabricators control temperatures more effectively. Semiconductor manufacturers are particularly sensitive to keeping the temperatures at precise levels to produce high-quality chips and keep energy costs down.

Choosing the right components

With temperature management during semiconductor manufacturing being essential, system designers must specify the right components to build a thermal loop that can withstand harsh operating conditions. Each component—hoses, valves, fittings, filters, and more—must meet the minimum requirements, including handling modern pressure and flow rates in addition to extreme temperatures (Figure 1).

Chiller hoses represent a particularly critical example because of the need for insulation (Figure 2). Enabling greater chiller efficiency with insulated hoses will keep temperature variations to a minimum, reduce heat transfer, and prevent condensation. Selecting components with these characteristics can help keep the fab running more efficiently and reduce overall downtime.

Though condensation is a threat to most industrial applications, it can halt production in a fab. In addition to dripping water potentially damaging critical equipment, unidentified leaks or puddles are always assumed to be toxic, which requires evacuation until the media is identified and determined to be safe. This unnecessary downtime and resource allocation can hinder a facility's chip production, which is why having properly insulated hoses is critical (see Figure 3).

➤ Figure 2. Chiller hoses should be properly insulated to help maintain desired temperatures and to prevent condensation.

Key elements of the thermal loop

The thermal loop is made up of:

- Chillers, which cool the fluid that circulates through the equipment
- Heat exchangers, which enable heat transfer
- Insulated hose assemblies and weldments, pumps, and valves, which help distribute temperature-controlled fluid throughout the entire cycle
- Monitoring and control systems, which adjust the flow rates and temperature
- Filtration and purification systems, which prevent contamination and remove impurities

Finding the right insulative balance

The solution for proper thermal performance is more complex than simply adding insulation to components. The longer the length of the hose, the more insulation is necessary, which can become costly. Therefore, installing the optimal amount of insulation will enhance the system's efficiency and minimize unnecessary costs.

A study of a fab's thermal loop system was conducted to demonstrate the efficiency gains that properly insulated hoses can provide. The tool needed -30°C chilled water to achieve the desired temperature in the process. To do this, the chiller upstream had to supply temperatures colder than -30°C so that the media would land at -30°C by the time it entered the tool. In this case, the tool was 40 feet away from the chiller.

Had an uninsulated hose been used to transport media across this distance, the chiller would have needed to provide much colder temperatures than it would if hoses were insulated because of the cooling loss (or heat gain) that would occur during the media's journey to the tool.

This overworks the chiller, leading to excessive energy costs, higher maintenance frequency, and possibly a shortened equipment life cycle. With an insulated hose, the chiller can provide temperatures closer to -30°C because it won't need to overcompensate as much for any cooling lost throughout the transport to the tool. In this example, every reduction of 1°C costs about 27 cents (USD) per hour. Saving 44 degrees of chilling requirements, for example, could save $11.80 (USD) per hour in cooling costs. While insulated hoses cost more, they can pay for themselves in energy savings.

➤ Figure 3. Selecting the right insulated hose is critical to mitigating condensation issues in fab production operations and may involve selecting vacuum-insulated metal hoses, which provide excellent insulation against extreme media temperatures.

Proper installation techniques and performance testing

Once designers and engineers choose the right components to maintain effective thermal management, the next step to building a high-performance system is the installation and implementation of those components. It is crucial to follow these protocols precisely to ensure each system is installed consistently, repeatably, cleanly, and moisture-free.

Review the basics before starting to install a system in the fab. As with most other industrial fluid systems, leak-tight performance is essential. Achieving leak-free systems requires technicians to understand tube fitting and valve installation. Misunderstanding these essential steps in the process can cause critical fluid systems to fail, which can hamper the efficiency and effectiveness of a production facility.

System failures lead to unplanned downtime, decreased production, safety issues, and lower profitability. For these reasons, proper installation of leak-tight fluid systems in semiconductor manufacturing facilities is critical.

In addition to proper installation, designers and engineers must carefully consider how they route chiller lines. Cold chiller lines should be kept far enough away from each other, so the hoses' surface temperatures do not fall below the dew point and cause condensation – or even icing.

The closer together the hoses are, the more likely they will cool the surrounding air to the chilled media's temperature in the hose and cause condensation problems. Generally, well-insulated hoses should be at least 12 inches (31 cm) apart. If the configuration of the system does not allow such spacing, additional layers of insulation on the lines to maintain performance integrity may be required.

Stagnant air can also affect the surface temperature of cooling lines. As airflow increases, surface temperatures can trend more toward the ambient environment temperature. Consider a hose that is routed through a confined area, such as a subfloor. In the case of cold media flowing through the hose, this could cause condensation to form on the outside, which may drip onto sensitive equipment as discussed before.

Finally, while a hose's minimum bend radius does not change when it is insulated, bending the hose

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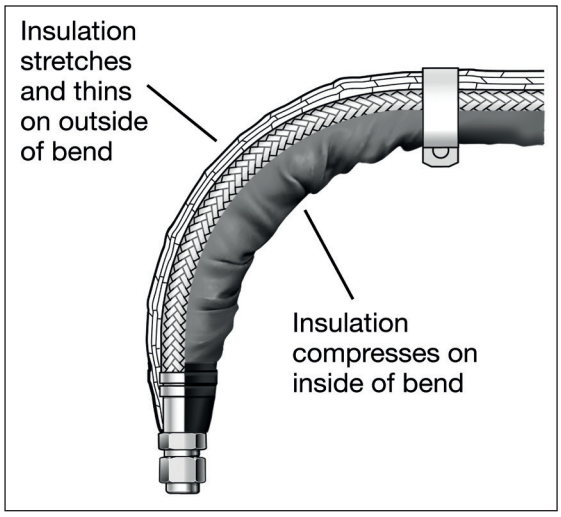
ESDA Electronic System Design Alliance

FlexTech

FOA Fab Owners Alliance

MEMS & SENSORS INDUSTRY GROUP®

SOI Industry Consortium



➤ Figure 4. Be careful not to bend insulated hoses too much to avoid crimping the hose and affecting the insulation properties.

How to choose insulated hoses

DURING THE DESIGN and installation of semiconductor manufacturing chiller applications, the most important consideration is choosing insulated hoses designed specifically for the application. While some manufacturers insist their insulated hoses can be used in both hot and cold fluid transfer applications, they often perform differently depending on what type of insulation is used.

For example, a hose featuring a flexible polyolefin heat shrink cover has been demonstrated to perform better in cold applications than insulated hoses with fabric coverings, which are more suited for high-temperature fluid applications.

Choose a hose supplier who has the expertise to help determine which materials will work most effectively for an application to avoid performance problems down the road.

Another key is that hoses must remain flexible regardless of which insulation type is used. Without maintaining flexibility, engineers may not be able to route and install the hoses on optimal paths. A hose's minimum bend radius, for example, should not change with insulation, nor should that bending capability compromise its insulative properties.

Look for options that properly maintain the target temperature of the transported fluid, do so flexibly, and are also not too bulky, such as a hose featuring low thermal conductivity aerogel insulation material.

Finally, an insulated hose that brings true efficiency to an application is one that uses only as much insulation as is required. Rather than a one-size-fits-all approach, a good hose supplier can offer different layering options that can cost-efficiently meet the temperature requirements of specific applications. In the best-case scenario, they will request the parameters of the application and use an equation to determine exactly how much insulation will be right for the specific hose needs.

may affect the insulation properties. To minimize these effects, it is generally recommended to make softer bends with a larger bend radius (Figure 4). If this is not possible, consider supplementing the hose with additional layers of insulation. See the sidebar to find out how to choose insulated hoses most effectively.

Building effective partnerships

As semiconductor manufacturing becomes increasingly important to the world economy, the race to lower costs has intensified. It is often difficult to trim costs on the expensive manufacturing tools that make high-quality chips possible to power future technological innovations. As a result, it makes sense to evaluate overall systems throughout the facility by looking for other less intrusive ways to lower manufacturing costs.

Evaluating whether the cold-temperature fluid transfer systems have the appropriate hoses is one such place to find unanticipated savings. Determining the precise level of necessary insulation can save money over time and help the system perform at peak efficiency over its lifespan – but operators, engineers, and technicians cannot be expected to know everything about thermal management. That is why finding a trusted supplier who can consult on these decisions is critical.

Finding a partner with the necessary experience in semiconductor manufacturing can provide valuable counsel about which components will meet the needs of particular applications. This guidance can mean reduced installation and operating expenses, improving profitability along the way. In the case of insulated hoses, an experienced partner can help determine how much insulation is necessary to keep chillers and other equipment operating properly. The more competitive the market becomes, the more important it will be to trim unnecessary expenses wherever possible.

The benefits of working with a supplier that can offer these tools and expertise can be significant, including:

- Reduced downtime via condensation prevention
- Increased semiconductor chip yields via minimized thermal variation and efficient media transfer
- Increased efficiency and reduced energy costs via improved chiller performance

Maintaining optimal functionality of the thermal loop is essential to consistent, maximized chip yield in semiconductor wafer manufacturing settings. Work with a supplier who can dive deeply into specific applications and offer innovative solutions to semiconductor wafer manufacturing operations. Find a partner with broad reach who can not only advise on proper hose choices but other components as well. Working together, semiconductor fabs can keep moving the world forward and running smoothly as technology continues to improve.

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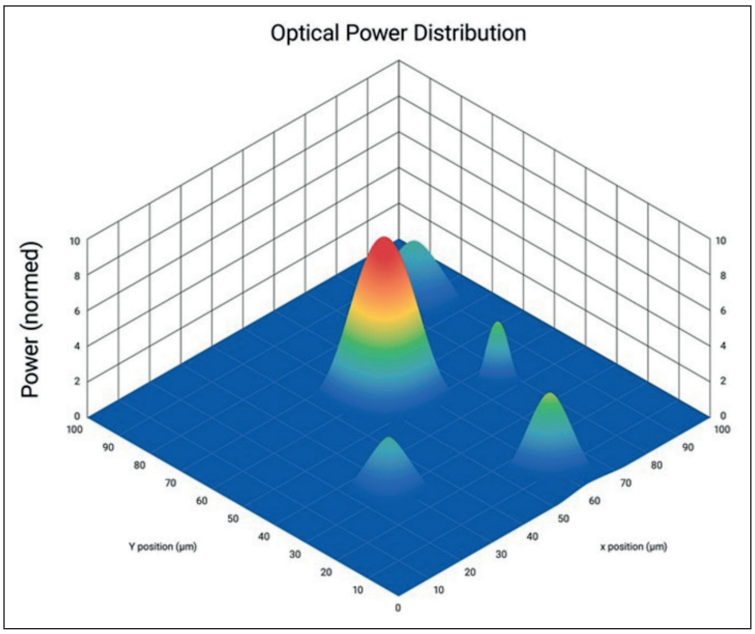
Advances in active alignment engines for efficient photonics device test and assembly

The photonics market is advancing rapidly, with projected substantial growth in a large number of sectors incorporating this technology in the next decade. Anticipating devices with hundreds or even thousands of individual components and connections, manufacturers face the necessity of parallel optimization, making active alignment an optimal choice to meet production demands.

BY SCOTT JORDAN, STEFAN VORNDRAN AND WARREN HARVARD, PHYSIK INSTRUMENTE L.P. (PI)

OVER MORE than a half century, the pace of innovation in electronic communication and computing has consistently increased, giving rise to progressively smaller silicon microchips with enhanced processing power. This achievement is attributed to the exponential growth in the density of integrated circuit (IC) transistors, a development predicted by Gordon Moore, Intel confounder, in 1965 and commonly called Moore's Law. However, there are inherent limits to reducing the physical feature size of silicon structures before quantum effects start influencing their functionality.



➤ Optical power distribution of a photonic component and simulated hill-climb algorithm (gradient search). (Image courtesy PI).

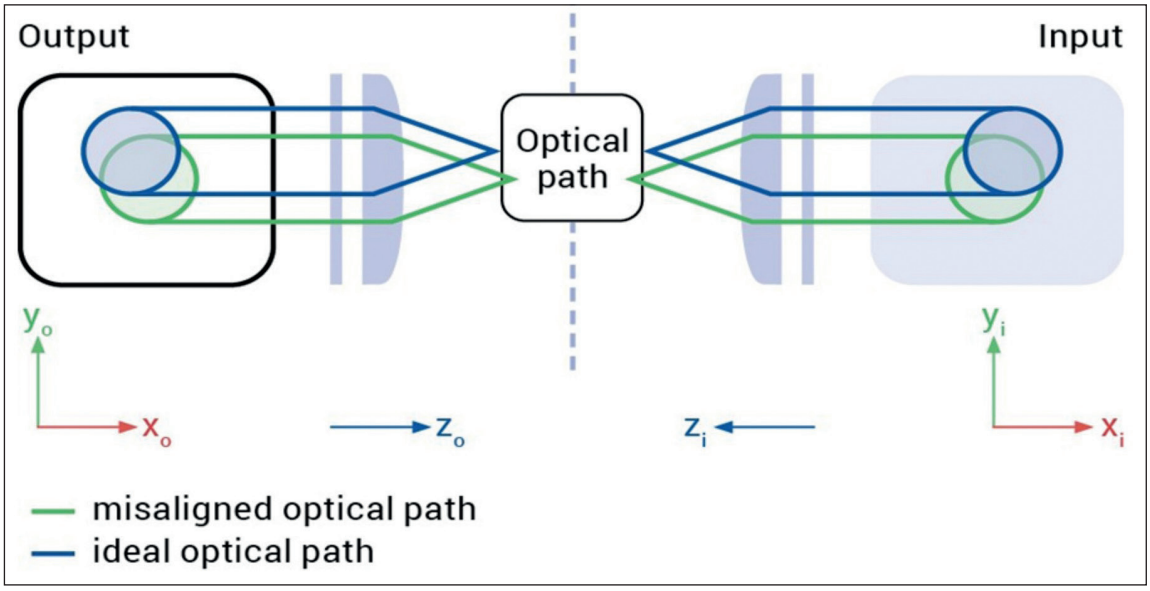
Fortunately, photonics has come to the aid of electronics, enabling the integration of miniaturized optical devices into various applications, from sensors in wearable devices, to LiDAR and ADAS cameras in autonomous vehicles. Photonics has the potential to surpass traditional electronics combining data throughput and efficiency with miniaturization, sparking a true revolution in the telecommunications and data communication sector. To sustain this growth, it is essential to address the remaining challenges and bottlenecks in photonic device manufacturing. The implementation of additional automation solutions, especially those ensuring fast and precise component alignment, is crucial to meet the demands of future advancements.

Limitations of labor-intensive device assembly

The assembly process of photonic devices typically includes meticulously aligning, gluing, and curing a combination of light sources, fibers, lenses, arrays, waveguides and chips. Each of these individual components must be accurately positioned to ensure the intended functionality and performance of the final product, as even slight misalignments on the orders of less than a millionth of a meter can severely impact device efficiency.

Despite technological advancements, many manufacturers still rely on manual alignment techniques, using shims for error compensation or securing hardware with retaining rings. Beyond being time-consuming, these methods often involve specialized labor that is both costly and challenging to find.

The manual assembly of complex devices can take up to 20 minutes, creating a significant bottleneck

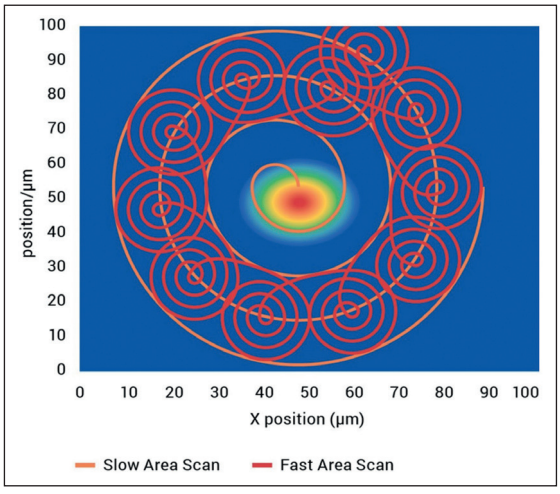


➤ Testing and packaging of modern photonic devices can be a huge challenge across multiple degrees of freedom. The alignment of multi-channel devices, such as fiber-optical arrays, used to be a slow, repetitive process before modern parallel algorithms were developed. (Image courtesy PI).

in the production process at the component positioning stage. Additionally, traditional assembly tools like shims and jigs may struggle to meet the increasingly stringent tolerances required for manufacturing modern devices. An alternative alignment strategy is necessary to precisely indicate component positioning.

Optical feedback to guide automatic alignment engines

A key characteristic of photonic devices is their efficiency's direct correlation with the alignment of individual components. This means that the output strength dynamically changes in real time with component positions. The varying signal strength serves as a guide for an iterative positional adjustment process, resulting in a precisely aligned assembly. To assess component drift, the fluctuation in photonic output strength can be monitored during the gluing and curing process. However, manually performing this method on complex devices with numerous inputs and outputs becomes impractical. Optimizing one connection can lead to movement affecting others, necessitating constant readjustment for a global consensus. An automated solution is essential to address this challenge, enabling a practical production process that eliminates the need for time-consuming back-and-forth adjustments.



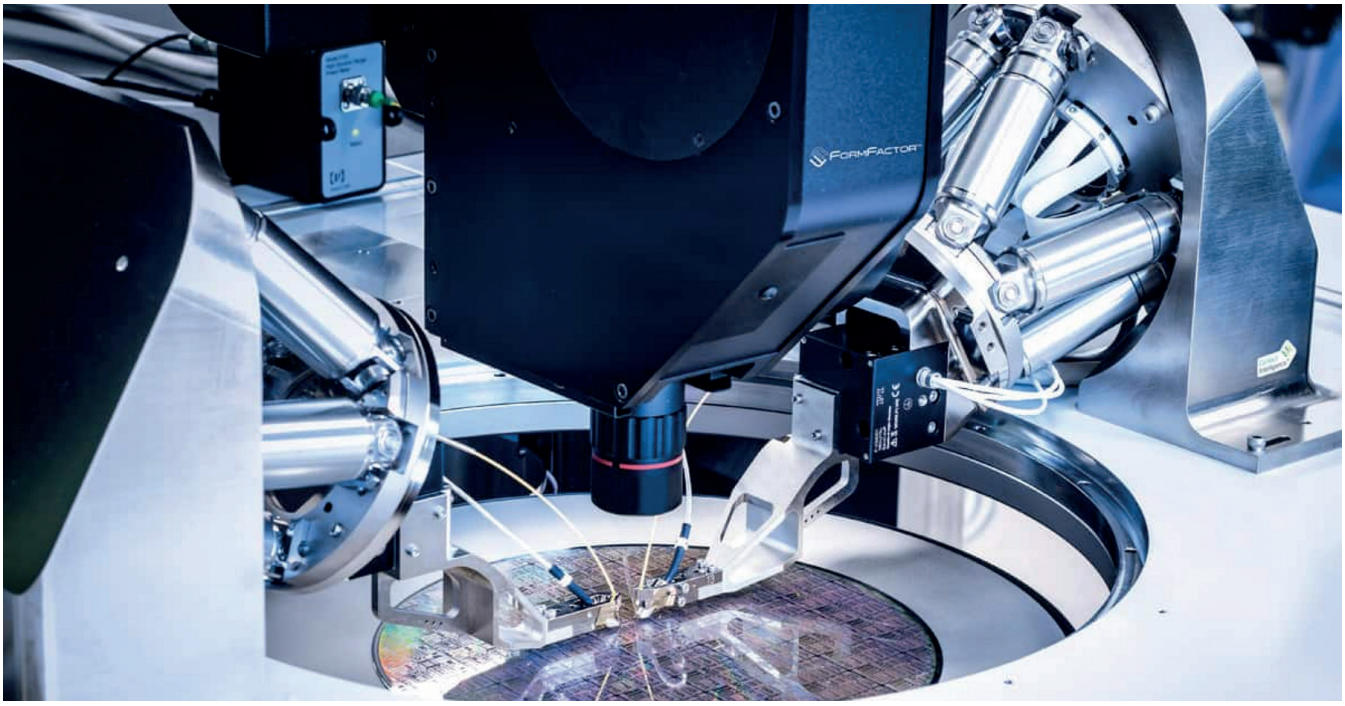
➤ Optical feedback is the key to automated alignment. A fast, traditional way of finding first light followed by a gradient search for optimum coupling efficiency is shown above – a double spiral scan using a hexapod/piezo approach. The hexapod runs a coarse spiral scan (coarse meaning single digit microns), while the piezo stage fills in the gaps with high-speed sub-micron scans. Both fine and coarse scans can be executed simultaneously. (Image courtesy PI)

Automating the adjustment process involves closing the feedback loop between device output and positioning hardware, allowing intelligent software solutions and control modules to handle fine-tuning. These systems utilize areal scan algorithms to characterize the assembly, identifying the approximate location of peak photonic output. Multiple gradient searches are then conducted to precisely determine the global optimum. Specialized piezo nano-positioning devices, capable of adjusting several connections simultaneously, guide the components into perfect alignment in an innovative process known as active alignment. Integrated features, including compensation factors, eliminate the need for constant iterative readjustment.

Complete modular solutions are now available, significantly reducing photonic device manufacturing times while maintaining sub-micron precision. Physik Instrumente's Fast Multichannel Photonic Alignment (FMPA) technology, for instance, can perform multiple alignments, such as in and outputs, across multiple-degrees of freedom, in parallel, reducing assembly time by a factor of 100 or more.

Solving the first light capture problem

Since alignment is the top cost driver for photonics device manufacturing, addressing it has been PI's



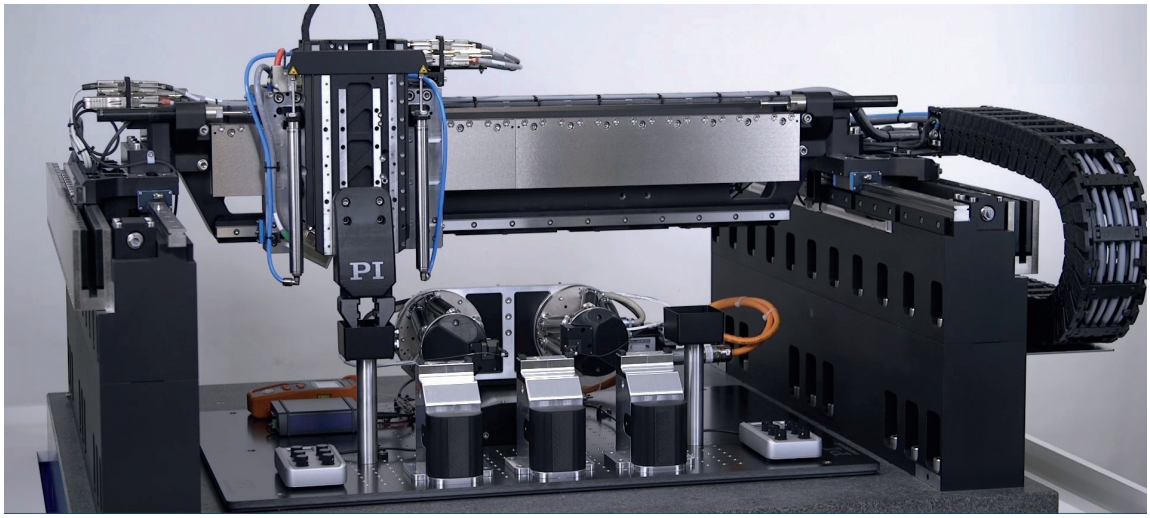
➤ The F-712, double-sided 18-axis fast multi-channel photonics alignment engine provides fast NxM alignment of SiP devices in wafer probers. The hexapods provide 6 degrees of freedom, while a compact 3-axis piezo scanner achieves nanometer resolution and scanning frequencies to 100Hz for fastest possible alignment. Cascade Microtech's pioneering CM300xi photonics-enabled engineering wafer probe station integrates PI's Fast Multichannel Photonics. Alignment engines for high throughput, wafer-safe, nano-precision optical probing of on-wafer Silicon Photonics devices. (Image courtesy FormFactor).

focus since the award-winning Fast Multichannel Photonics Alignment (FMPA) technologies in 2016. By performing optimization in parallel across multiple channels, components and degrees of freedom and achieving coupling repeatabilities to typically 0.02dB, FMPA reduces the time and cost of manufacturing and testing of photonic devices and improves yield. But before the optimization process can even start, an optical signal, above the noise level, needs to be detectable – this process is called first light capture, and it is particularly time-consuming in devices with inputs and outputs where both sides must be lined up for even a threshold amount of coupling to be achieved. Finding first light has been a time-consuming procedure in all industrial photonics alignment applications, including wafer probing and device packaging.

➤ A PILightning-algorithm enabled dual sided air-bearing-based alignment system. The new algorithm reduces the first light finding process in single-sided applications by 10X or more and in dual-sided applications by several 100X. (Image courtesy PI).

Now, a breakthrough has arrived in the form of a novel, built-in search-and-alignment algorithm (patent applied for), promising to revolutionize this field. The algorithm, dubbed PILightning runs embedded on PI's advanced controller. It enables highly dynamic mechanics such as piezo scanners or direct-drive air bearing stages to achieve significant production-economics gains over previous first light search algorithms. This new process is fully automated and virtually instantaneous, eliminating the need for extensive calibration or manual intervention. PILightning is based on a new search method with integrated AI-based real-time executive function. It also replaces fine pitch scanning by high frequency data sampling, raising alignment speeds significantly. It drastically reduces the time required to acquire first light in single- and double-sided couplings and in loopback (omega) waveguide configurations.

Once first light is detected, the FMPA fast gradient search algorithm takes over, utilizing real-time feedback control to swiftly optimize the alignment in parallel across the degrees-of-freedom and



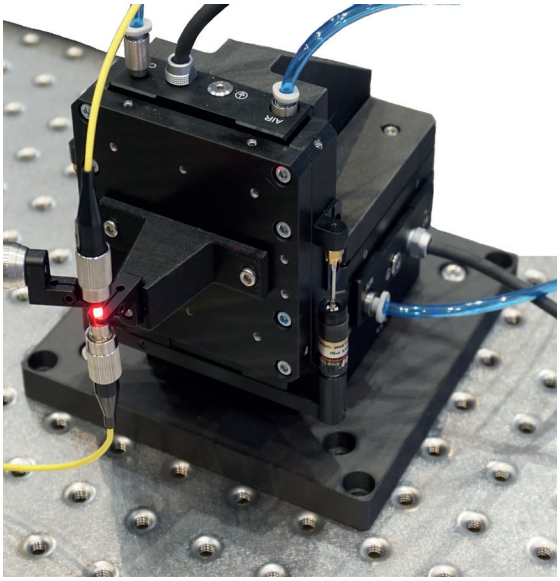
➤ Image 6: A gantry pick-and-place system with two hexapod 6-axis high-speed automated alignment stations for fast SIPh component test. (Image courtesy PI)

channels. Depending on the application, a tracking algorithm can also be activated to maintain maximum coupling efficiency – important, for example, in curing situations.

Ensuring future success through modular solutions based on multiple drive technologies

The photonics market is advancing rapidly, with projected substantial growth in a large number of sectors incorporating this technology in the next decade. Anticipating devices with hundreds or even thousands of individual components and connections, manufacturers face the necessity of parallel optimization, making active alignment the optimal choice to meet production demands.

Additionally, as photonic devices gain traction across various sectors, the development of increasingly specialized devices requires bespoke production processes. Manufacturers aiming to stay competitive and adapt to evolving demands require flexible combinations of hardware and software that can be easily reconfigured.



➤ A compact, multi-axis air-bearing based photonics alignment system. Advantages of air bearings are frictionless, high-speed motion with virtually unlimited lifetime as well as the lack of particle generation. (Image courtesy PI).

In addition to “monolithic” hexapod-based 6-axis alignment engines, modular alignment solutions, exemplified by those developed by PI, excel in providing the flexibility and scalability necessary for production operations. These solutions include friction-free air-bearing-based motion systems that require zero maintenance and provide superior speed and lifetime, as well as linear and torque motor driven solutions with precision mechanical bearings, and economical systems based on traditional screw drives and stepper motors.

➤ PI’s automation controller uses ACS controller and driver modules and embedded high-performance alignment algorithms for the highest data-throughput and shortest alignment times. EtherCat® connectivity allows seamless integration of third-party devices. (Image courtesy PI).

Common to all these modular systems is a high-performance EtherCat®-based motion controller with embedded, advanced alignment routines and integrated, high-speed optical power meter, for a quick path to success.

Automation in semiconductor test processes: **a key factor in modern production**

The automation of semiconductor test processes is a crucial factor in modern semiconductor production. It promises not only increased efficiency and cost reduction but also improved test accuracy and reliability. Despite the numerous advantages, manufacturers face various challenges, ranging from technical hurdles to organizational barriers. This article highlights the current issues in semiconductor testing and how these challenges can be addressed through innovative solutions and proven strategies.

BY THOMAS SEIDL, TECHNICAL SALES MANAGER, ESMO AG

DURING CHIP DEVELOPMENT, various revision stages are undergone. New developments and prototypes are produced in small batches, making them expensive and rare. The limited number of components makes the use of a high-parallel production handler impractical, as these handlers are often too expensive to procure, too complex to operate, and too time-consuming to reconfigure.

For these reasons, engineering tests are usually conducted manually, which ties up valuable employee resources and test capacities.

Additionally, modern microchips tend to get smaller, presenting extra handling challenges. One can imagine how mentally exhausting and concentration-intensive it is to correctly place and test a certain number of 1x1mm components over time, not to mention the potential for placement errors and damage.

➤ The esmo talos automates microchip engineering test procedures easily and reliably.

Automating this process with an engineering handler, such as the esmo talos, is advantageous. An operator loads the machine with components (trays/tubes/tape), installs a component-specific conversion kit, and initiates automatic testing. With a fully tri-temp capability and an integrated Active Thermal Control System (ATC), such a handler is ideal for effortless characterization.

Switching from one package to another is possible within minutes, which is crucial when dealing with a high number of different packages. Engineers can start testing quickly without lengthy setup adjustments. The system's high flexibility often allows the use of existing test setups, avoiding additional costs.

Automation in production

In production, the focus is on maximizing test cell utilization. Any test failure or delay is extremely costly and jeopardizes test goals. Here some common tasks and how to overcome them.

Semi-automatic board exchange via DIB changer

When a board needs to be replaced, trained personnel are usually required. The test head is undocked, manually moved outward, and returned after a successful board swap. Depending on how

carefully personnel handle this process and how securely the docking solution is implemented, there can be potential tension or damage to the board or components.

An automated board exchange system from esmo can handle this process automatically. The command can come either from an operator's push-button or directly from the test cell. The system disconnects the tester from the handler, and the board is moved outward via a drawer. It can then be easily swapped by an operator or automatically by an AGV. This ensures no damage occurs during the docking process and the connection is always secure and reliable.

Auto-setup manipulator + automated board locking

Taking automation a step further is the fully automatic docking and undocking of the tester using an automatic manipulator. A key feature is that the test head acts as the cell's master, controlling the manipulator. If issues arise, a signal can be sent to automatically undock the test head and move it to a service position.

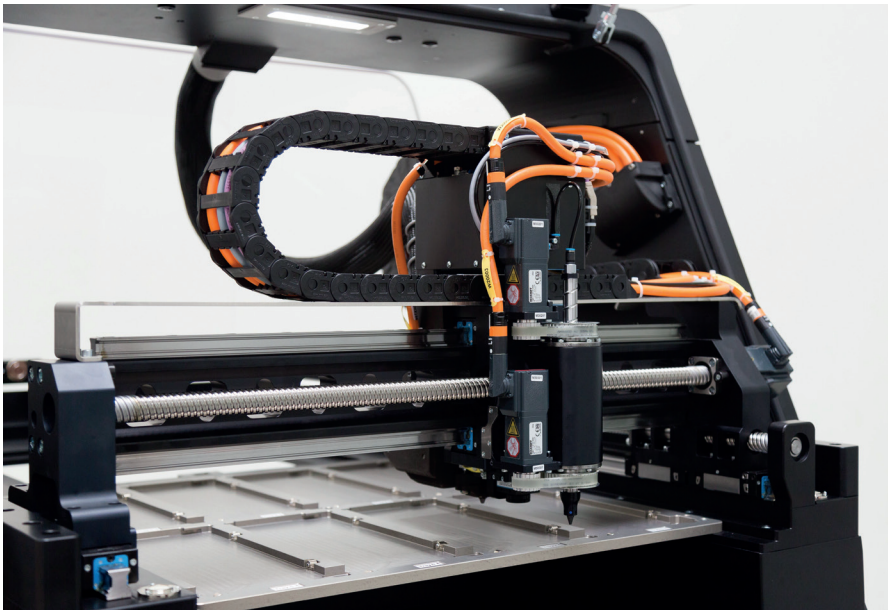
The esmo ares auto setup (Final Test Manipulator) and Titan (Universal Manipulator) have a patented integrated camera that recognizes the handler's position and precisely aligns the tester during docking. This advantage means that if the handler is moved, no precise realignment or extensive retraining is necessary. The positioning provided by the vision system allows for the use of a CUH and an auto-lock feature on the handler, eliminating the need for traditional docking.

The board and CUH remain on the tester and, once positioned and brought to the handler, are locked in place. Many handlers already feature this capability, and if not, esmo offers retrofit solutions.

Future outlook

In conclusion, the automation of final microchip testing not only plays a crucial role today but will also be of central importance in the future. As technology advances and microchips become more complex, automated test systems will become increasingly sophisticated and powerful.

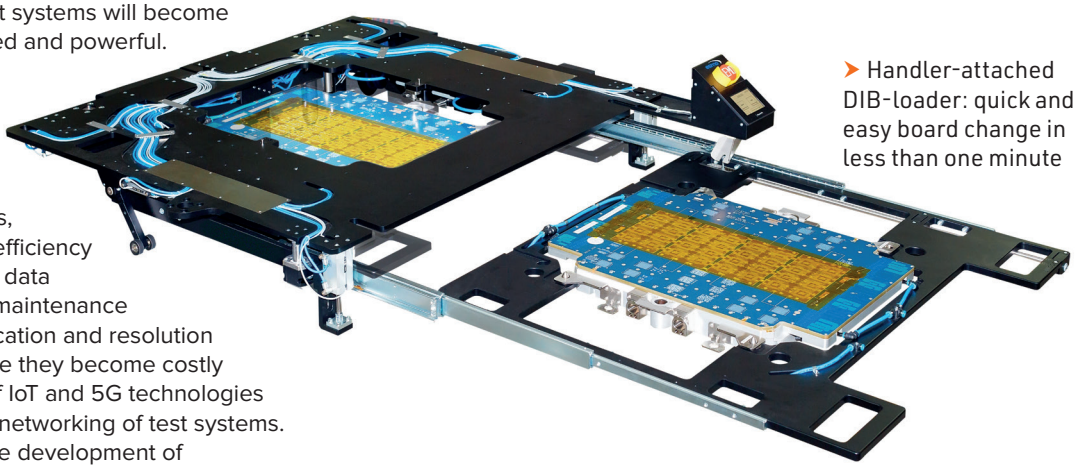
We can expect the integration of artificial intelligence and machine learning into final test procedures, significantly enhancing efficiency and precision. Real-time data analysis and predictive maintenance will enable early identification and resolution of potential issues before they become costly problems. The advent of IoT and 5G technologies will further optimize the networking of test systems. A promising aspect is the development of autonomous test systems that can adapt to new requirements independently and continuously learn. These systems will be able to develop and implement complex test strategies that surpass those of human engineers.



➤ The esmo ares auto setup is a unique final test manipulator capable of automated test head positioning.

With the ongoing automation of final microchip testing, the innovation cycle will accelerate, product quality will improve, and time-to-market will shorten. Companies that embrace these technologies early will gain a significant competitive advantage and be better equipped to meet future challenges.

The future of final microchip testing is undoubtedly exciting and promising. We are at the beginning of a new era where automation will fully unlock the potential of microchips and revolutionize the semiconductor industry.



➤ Handler-attached DIB-loader: quick and easy board change in less than one minute

ULVAC ENVIRO™ Plasma Ashing Systems

With over 40 years of ashing experience, ULVAC has ENVIRO plasma ashing tools for R&D, pilot production and high-volume manufacturing.

The ENVIRO-1Xa photoresist removal equipment from ULVAC, offers superior performance at an exceptional price. The system is equipped with a versatile platform that can handle multiple wafer sizes, ranging from 100 to 200 mm in diameter. The system utilizes a high efficiency downstream plasma source and can achieve ash rates >10µm/min, with a throughput of 70+wph. This is all achieved on a minimal footprint of 1.57m^2. It offers high process flexibility that is required for demanding processes, such as: high-dose implanted resist removal, descum and surface modification, SU-8 and fluorinated resist removal, and MEMS sacrificial-layer removal.

➤ ENVIRO-Optima – Three Chambers

ENVIRO -- High Speed Plasma Ashing Systems

- ENVIRO-1Xa – Single Chamber
- ENVIRO-1Xa 2C – Two Chambers
- ENVIRO-Optima – Three Chambers

ENVIRO™ features common process chambers mated to high-speed wafer handlers for R&D, pilot production and high-volume manufacturing; including thin wafer handling.

ENVIRO offers the flexibility for multiple applications, including:

- Bulk ashing (including thick resist such as SU-8, KMPR)
- High Dose Implant resist strip
- Descum
- Polymer and residue removal
- MEMS release (organic sacrificial layer removal)
- Backside ashing, bevel/edge cleaning

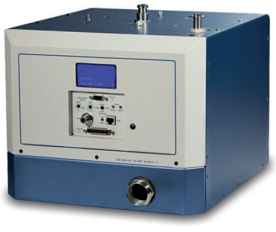
ENVIRO offers a wide process operating range:

- Ashing Rate – Several nm/min to more than 10 µm/min
- Wide range of stage temperature control (hot plate or optional cold plate)
- Choice of high efficiency downstream plasma sources: ICP or MW
- Choice of RF bias plasma source
- Up to 4 MFC's, 2 standard, 2 optional
- Gas chemistries: Oxidizing, reducing, halogen bearing

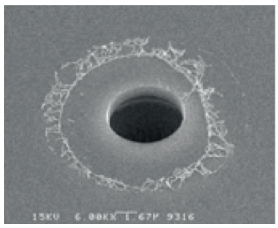
Plasma Source Options for ENVIRO

ICP Source

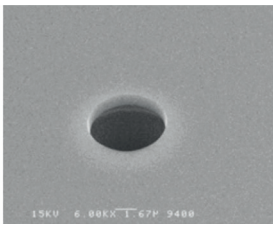
The original Optima was designed for high throughput and high reliability utilizing a compact, inductively coupled plasma (ICP) source. To meet the demands for high productivity, the process focus was on high film removal rates, MEMS applications, and high dose implant strip (HDIS).



Post Bosch Process Residue Removal



➤ After Conventional Ash Process



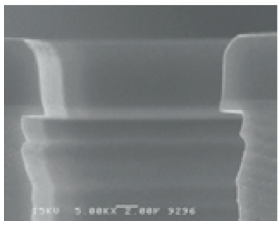
➤ After ENVIRO Ash Process

MEMS Device Descum

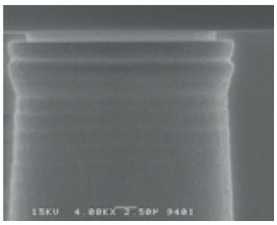
➤ Pre Descum

➤ Post Descum

Post Deep Silicon Etch Resist Removal



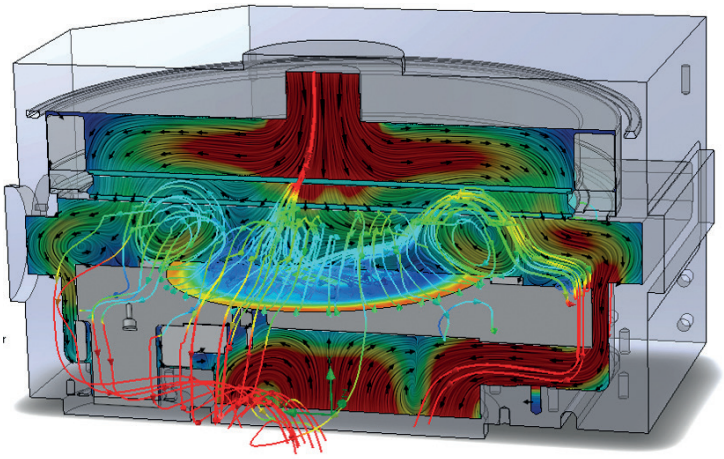
➤ Pre Ashing



➤ Post Ashing

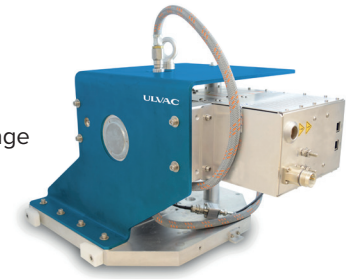
MW Source: Expanded Process Capabilities

With the addition of microwave frequency plasma source technology, the Optima can support a wider range of process chemistries to address low temperature polymer removal and low oxidation of substrate materials. The microwave energy provides low plasma induced damage with test results indicating approximately 50% reduction from the ICP source.



➤ Configured with either Microwave or ICP as downstream plasma option, and RF Bias as an independent plasma option, the Optima continues to support the needs for high volume production with its ability to replace multiple legacy systems with a single Optima tool. ULVAC customers have put into mass production one Optima system to replace from three to seven legacy dry strip systems.

- Wider range of process chemistry
- Low temperature polymer removal
- Low oxidation of substrate materials
- 50% reduction in plasma induced damage



RF Bias Source: More Expanded Process Capabilities

RF Bias source is the latest addition to Optima's plasma options, which further expands Optima's process capabilities. RF Bias plasma can act on its own, or be used in conjunction with MW or ICP downstream plasma source. Chemical and physical ashing/etching can be achieved at the same time, to address a wider range of processes:

- Carbonized skin layer removal in high dose implant strip
- Anisotropic low temperature descum
- Light etching
- High aspect ratio cleaning

ULVAC

About ULVAC Europe

ULVAC GmbH was established in 1987 as the European subsidiary of ULVAC, Inc. Headquartered in Munich, Germany. From Munich, our sales and service team serve the EMEA region. ULVAC provides a very broad portfolio of manufacturing equipment for the vacuum, materials, and thin film industries.

ULVAC's solutions diversely incorporate equipment, materials, analysis, and services for semiconductors, MEMS, flat panel displays, electronic components, PCB, TFB and other vacuum equipment.

ULVAC offers state-of-art products and technologies for semiconductor and related processes. To support MEMS, power devices, and NVM fabrication, ULVAC offers equipment for sputtering, evaporation, plasma etch, ashing, ion implanting, oxidation/POA/nitridization, and activation annealing for both R&D, pilot line, as well as high volume manufacturing. A complete line of vacuum components is also offered which includes vacuum pumps of all types, helium leak detectors, UHV systems and gauges, RGA's and thermal analysis instrumentation.

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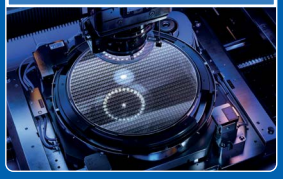

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