SILICON SEMICONDUCTOR

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PREDICTIVE MAINTENANCE IN THE SEMICONDUCTOR SECTOR:

HOW EDWARDS VACUUM IS SHAPING THE FUTURE OF RELIABILITY

EDWARDS

EDWARDS

[enabling environments where innovation thrives]

Ganymede

Performance without compromise

VIEWPOINT

BY PHIL ALSOP
EDITOR

The Semiconductor industry at a crossroads — growth, risk, and geopolitics

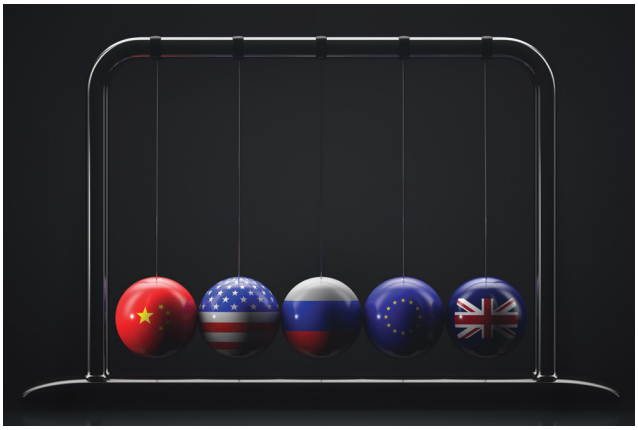
The semiconductor industry is surging ahead, yet it is also stumbling into risks that will define its future. In the second quarter of 2025, global foundry revenues hit a record $41.7 billion, driven by seasonal demand and China's subsidy-fuelled consumption. TSMC's dominance has never been clearer, securing over 70% market share. At the same time, AI adoption is reshaping both chip design and manufacturing: the AI-in-semiconductor manufacturing market is forecast to grow sevenfold by 2033, while AI-powered data centres are expected to nearly double their semiconductor spend by 2030.

But behind the growth charts lies a more fragile picture. Security risks are mounting. Every semiconductor company in the S&P 500 has now disclosed AI-related vulnerabilities - ranging from intellectual property theft to prompt-driven data leaks. In a sector where a single schematic or line of code represents billions in R&D, such breaches are existential threats. Innovation is colliding with exposure. Geopolitics adds another layer of volatility. The US–China chip rivalry has hardened into a long-term structural divide.

Export controls have deprived China of leading-edge GPUs and advanced manufacturing tools, but they have also spurred domestic innovation, with SMIC, Huawei, and others doubling down on homegrown capabilities. Yole Group forecasts China could control 30% of global foundry capacity by 2030 - a shift that would rival Taiwan's dominance and reshape global dependencies.

Meanwhile, Europe, Japan, and even the UK are each attempting their own sovereignty plays. The UK's Council for Science and Technology has urged the creation of a sovereign AI chip design industry, while the US is pouring billions into workforce training through regional education nodes.

This competition isn't just about market share, it's about who controls the future of AI. Hyperscalers like Google, Amazon, and Microsoft are developing AI-specific ASICs to



reduce reliance on Nvidia, while startups push boundaries on cost and energy efficiency. Fraunhofer's collaboration with DIVE shows how sustainability and efficiency can still be achieved, cutting emissions and metrology waste in fabs. Yet even this innovation must be seen through the lens of ownership and control: who builds the fabs, who owns the IP, and who sets the guardrails for AI integration.

The semiconductor industry is now a theatre where three forces collide: explosive technological growth, escalating security vulnerabilities, and geopolitical manoeuvering. Revenue highs cannot mask the fragility of a system dependent on a few chokepoints of capacity, tools, and talent. The industry is richer than ever, but also more exposed than ever.

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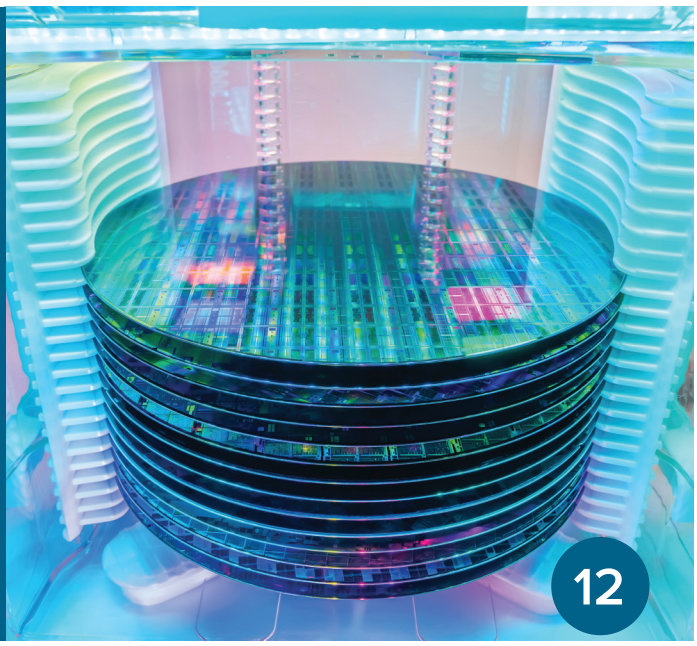

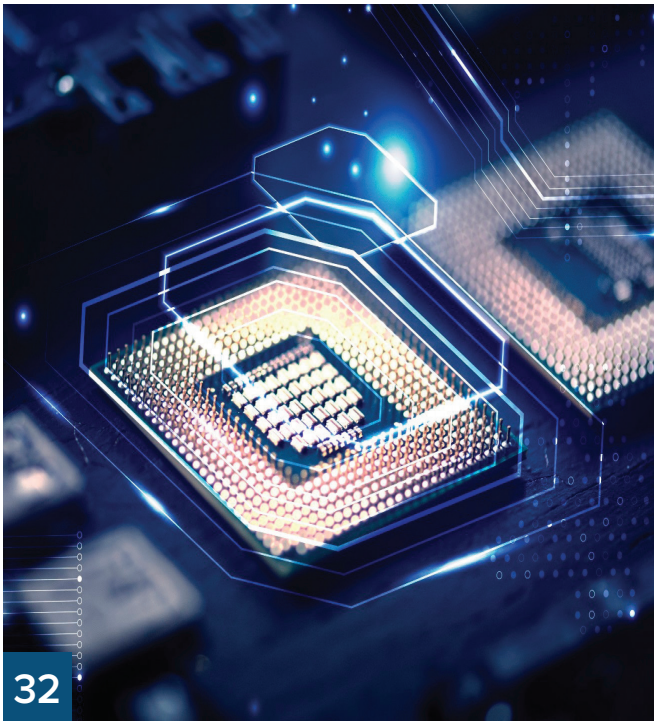

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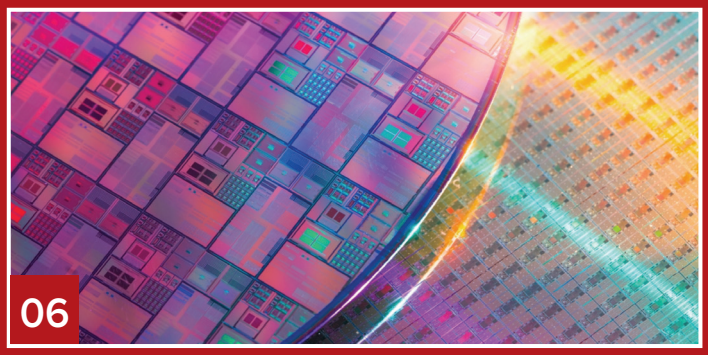

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Tech, software, and semiconductor companies face the highest AI security risk in the S&P 500

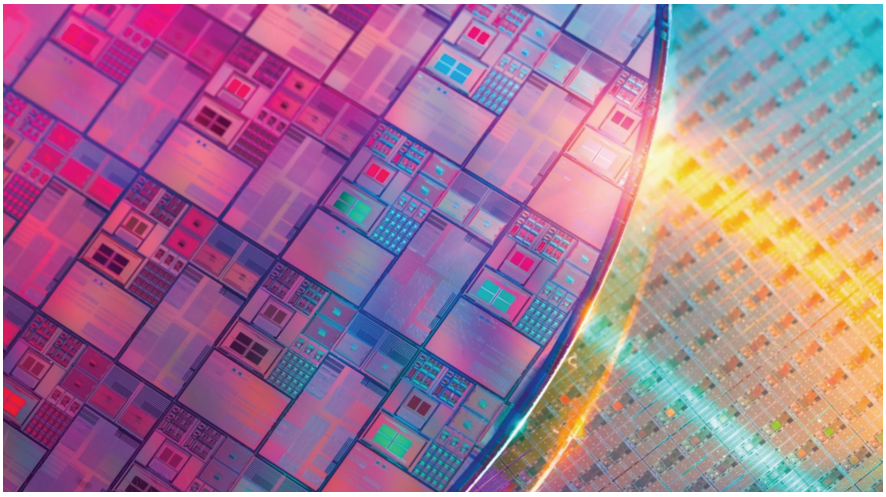
nexos.ai highlights sector-leading exposure to IP theft, insecure AI outputs, and data leakage, and outlines practical controls to protect code and chip-design intellectual property (IP).

AI RISK is no longer just a hypothetical concern for America's largest companies. Autonomy Institute's new analysis shows that 3 out of 4 S&P 500 firms increased their AI risk disclosures this year, highlighting how deeply AI security issues are transforming corporate strategies. The technology, software, and semiconductor industries face the greatest exposure. According to Cybernews research, this sector alone has 202 documented AI security risks across 61 companies – the highest in the index.

These risks include 40 flagged cases of potential intellectual property theft, 34 insecure AI outputs, and 32 instances of data leakage. The Autonomy Institute's accompanying analysis underscores how widespread the issue is: 1 in 5 companies in the S&P 500 now list proprietary data or IP exposure as a top AI risk, and every single semiconductor company in the index updated its filings in 2025 to acknowledge significant AI threats.

Cybernews' investigation reviewed public disclosures of AI use across 327 S&P 500 companies, finding nearly 1,000 real-world AI deployments, from internal analytics tools to customer-facing chatbots, and identifying 970 potential AI security issues in total. Each case included specific examples and was categorized into risks such as prompt injection, model extraction, and accidental data exposure.

For tech and semiconductor companies, the risk isn't hypothetical. One malicious prompt can trick a model into revealing confidential code or unreleased design files. A continuous model-extraction attack can reconstruct algorithms and expose trade secrets. Cybernews warns that since these companies hold "a high concentration of proprietary algorithms and sensitive code," they



are "especially vulnerable to both data leaks and IP theft."

"AI is now a core business driver. Without the right guardrails, it carries strategic risks, especially in tech and semiconductors," says Žilvinas Girėnas, head of product at nexos.ai. "IP theft, insecure outputs, and prompt-driven leaks are no longer theoretical. The solution is proactive: policy-first design, prompt redaction at the edge, strict model access controls, and audit-ready logs. This is how companies can protect their most valuable asset, their innovation, while still moving fast with AI."

For technology and semiconductor companies, intellectual property isn't just valuable — it is the core of the business. A single leak of source code, chip schematics, or proprietary algorithms can wipe out years of competitive advantage.

Recent incidents demonstrate how quickly things can go wrong. At Samsung, engineers pasted confidential code into ChatGPT, and that code became part of the model's training data — leading to a corporate ban on generative AI. In 2024, an EDA (Electronic Design Automation) software company encountered a serious exposure: internal design automation prompts, used to guide the AI-assisted design of chip layouts and verification logic, were found circulating in developer forums after being entered into an unsecured third-party AI model. In multiple semiconductor companies, misconfigured AI assistants have exposed unreleased product specifications during internal testing.

These aren't isolated mistakes. They indicate that without enforced AI policies, redaction during use, and strict model oversight, every AI query risks becoming a security breach.

"Tech companies are racing to ship AI features. That pace often skips the guardrails protecting code and designs. Centralized controls like policy, redaction, routing, and clear audit trails are the only way to keep innovation from becoming an IP liability," says Girėnas.

Girėnas recommends that organizations handling sensitive code, algorithms, or design files adopt: Centralized policy enforcement to block risky prompts and apply consistent output filters.

AI in semiconductor manufacturing market to surpass $14.2 billion

According to Research intelo's latest research, the AI in Semiconductor Manufacturing market size reached USD 1.95 billion in 2024 globally.

THE MARKET is demonstrating robust momentum, supported by a strong compound annual growth rate (CAGR) of 22.7% projected from 2025 to 2033. By the end of the forecast period in 2033, the market is expected to attain a value of USD 14.2 billion.

This substantial growth is primarily driven by the increasing adoption of artificial intelligence technologies to enhance process efficiencies, reduce defects, and optimize yield in semiconductor fabrication and assembly.

As per the latest research, the market's expansion is further fueled by the growing complexity of semiconductor devices and the need for advanced analytics to maintain competitiveness in a rapidly evolving industry landscape.

The semiconductor industry forms the foundation of the digital age, powering everything from smartphones to supercomputers. As chips grow smaller, faster, and more complex, traditional manufacturing processes face significant challenges.

Artificial Intelligence (AI) has emerged as a transformative tool, enabling smarter production, faster innovation, and enhanced efficiency in semiconductor manufacturing.

Semiconductor manufacturing involves hundreds of intricate steps, including wafer fabrication, lithography, etching, and packaging. With each new generation of chips, transistors shrink to nanoscale levels, pushing the limits of physics and precision engineering.

AI helps overcome these challenges by providing predictive insights, automating defect detection, and optimizing process efficiency.

Key Applications of AI in Semiconductor Manufacturing

1. Predictive Maintenance

Manufacturing equipment in semiconductor fabs is highly complex and prone to wear.

AI-powered predictive maintenance detects anomalies in machines, reducing downtime and preventing costly failures.

2. Yield Optimization

AI algorithms analyze vast amounts of production data to identify defects, improve yields, and enhance product quality. This ensures minimal wastage and greater cost efficiency.

3. Process Automation

From wafer inspection to testing integrated circuits, AI-driven automation reduces manual intervention and speeds up production cycles.

4. Supply Chain Management

AI models forecast demand, optimize inventory, and enhance logistics efficiency, ensuring semiconductor manufacturers remain resilient in times of global shortages.

Benefits of AI Adoption in Semiconductor Manufacturing

- **Higher Production Efficiency:** Reduced errors and faster production cycles.
- **Cost Reduction:** Lower downtime, reduced scrap, and optimized resource allocation.
- **Improved Quality:** Enhanced defect detection and precise manufacturing.
- **Innovation Acceleration:** Faster design-to-manufacturing transitions.
- **Sustainability:** Optimized use of energy and raw materials.

AI in Wafer Fabrication and Inspection

Wafer fabrication is one of the most critical steps in chip manufacturing, where even microscopic errors can impact chip performance. AI-based imaging systems enable:

- Real-time defect detection.
- Improved lithography pattern recognition.
- Accurate alignment of nanoscale structures.

These advancements help manufacturers achieve higher yields and improve the reliability of finished chips.

Challenges in AI Integration

Despite its promise, AI adoption in semiconductor manufacturing faces hurdles:

- **Data Privacy Concerns:** Handling proprietary design and manufacturing data.
- **High Implementation Costs:** AI infrastructure requires significant investment.
- **Skilled Workforce Shortage:** Combining AI expertise with semiconductor domain knowledge is rare.
- **System Integration:** Ensuring AI tools align with existing manufacturing processes.
- **Future Outlook:** AI-Powered Semiconductor Ecosystem

The future of semiconductor manufacturing lies in intelligent automation and adaptive processes. AI will continue to evolve with advancements in:

- **Generative AI for Chip Design:** Automating early-stage circuit design.
- **Digital Twins of Fabs:** Creating virtual replicas of manufacturing plants for simulation and optimization.
- **Edge AI:** Deploying smart chips that manage their own performance.
- **Sustainable Manufacturing:** Using AI to minimize energy and water consumption in fabs.

2Q25 foundry revenue surges 14.6% to record high

TrendForce's latest investigations reveal that global foundry revenue in 2Q25 reached a record US$41.7 billion, up 14.6% QoQ, thanks to China's consumer subsidy program spurring early stocking, along with upcoming demand for new smartphones, notebooks/PCs, and servers launching in the second half of the year. Both capacity utilization and wafer shipments improved significantly across the top ten foundries.

LOOKING ahead to 3Q25, seasonal demand for new products will drive order momentum. Advanced nodes will benefit from strong demand for flagship chips, while mature nodes will be supported by peripheral IC orders. As a result, industry-wide utilization rates are expected to rise further, supporting continued revenue growth—albeit at a more moderate pace.

The revenue performance of the top 10 foundries in the second quarter is as follows: TSMC reported outstanding performance, with major smartphone clients entering their ramp-up cycle and strong shipments of AI GPUs, notebooks, and PCs pushing wafer shipments and ASPs higher. Revenue climbed 18.5% QoQ to $30.24 billion, lifting its market share to a record 70.2% and cementing its leadership position.

Samsung Foundry also posted solid results, benefiting from smartphone demand and the ramp-up of the Nintendo Switch 2. Shipments were weighted toward high-value advanced nodes, driving revenue up 9.2% QoQ to $3.16 billion to give the company a 7.3% market share as it ranked second. SMIC, while still supported by U.S. tariffs and China's subsidies, struggled with lingering issues from its advanced-node production lines in the first quarter, which led to shipment delays and lower ASPs. Its revenue slipped 1.7% QoQ to $2.21 billion, with market share dipping slightly to 5.1%, though it retained third place.

Ranking	Company	2Q25	1Q25	QoQ	2Q25	1Q25
1	TSMC	30,239	25,517	18.5%	70.2%	67.6%
2	Samsung	3,159	2,893	9.2%	7.3%	7.7%
3	SMIC	2,209	2,247	-1.7%	5.1%	6.0%
4	UMC	1,903	1,759	8.2%	4.4%	4.7%
5	GlobalFoundries	1,688	1,585	6.5%	3.9%	4.2%
6	Huahong Group	1,061	1,011	5.0%	2.5%	2.7%
7	VIS	379	363	4.3%	0.9%	1.0%
8	Tower	372	358	3.9%	0.9%	0.9%
9	Nexchip	363	353	2.9%	0.8%	0.9%
10	PSMC	345	327	5.4%	0.8%	0.9%
Total of Top 10		41,718	36,413	14.6%	97%	97%

UMC performed well, with gains in both shipments and ASPs lifting revenue by 8.2% QoQ to $1.9 billion, securing a 4.4% market share and ranking fourth. GlobalFoundries followed closely, benefiting from new product stocking and modest ASP improvements. Its revenue increased 6.5% QoQ to $1.69 billion, placing fifth with a 3.9% share. Shipments of Tier 2 foundries improved, supported by orders for peripheral ICs used in new products.

TSMC reported outstanding performance, with major smartphone clients entering their ramp-up cycle and strong shipments of AI GPUs, notebooks, and PCs pushing wafer shipments and ASPs higher. Revenue climbed 18.5% QoQ to $30.24 billion, lifting its market share to a record 70.2% and cementing its leadership position

Amid China's consumption subsidies and the push for IC localization, HHGrace, a subsidiary of HuaHong Group, saw its capacity utilization improve in the second quarter, which drove a sequential increase in total wafer shipments. While this was partly offset by a slight decline in ASP, revenue still rose by 4.6% QoQ. Including HLMC and other affiliated businesses, HuaHong Group's consolidated revenue grew by around 5% to reach approximately $1.06 billion, securing a 2.5% market share and holding steady at sixth place.

Vanguard reported revenue growth of 4.3% QoQ to nearly $379 million, ranking seventh, while Tower improved utilization as clients resumed stocking for second-half launches, pushing revenue up 3.9% QoQ to $372 million, maintaining eighth place.
Nexchip also benefited from subsidy-driven demand and higher orders for peripheral ICs, though low pricing limited upside. Its revenue grew nearly 3% QoQ to $363 million, ranking ninth. Finally, PSMC achieved revenue of $345 million, up 5.4% QoQ, securing tenth place.

Regional nodes to ramp up education

The SEMI Foundation has launched the application process for organizations seeking to become Regional Nodes in the National Network for Microelectronics Education (NNME), a nationwide initiative funded by the U.S. National Science Foundation and supported by the U.S. Department of Commerce that aims to advance education, training, and employment pathways in the U.S. microelectronics sector.

THIS RELEASE marks the first step in the review and selection process designed to identify and support regional ecosystems that are ready to lead and scale workforce development efforts aligned with the growing talent needs of the semiconductor and microelectronics industries.

The SEMI Foundation is serving as the NNME's Coordinating Hub, which includes development, coordination, and scaling of Regional Node activities nationwide. NNME expects to support up to eight nodes, each with up to $20 million over five years.

SEMI Foundation"We've spent years listening, collaborating, and building trust, and the NNME is where all of that work takes flight," said Shari Liss, Vice President of Global Workforce Development and Initiatives at SEMI. "In an industry that's shaping the future, investing in people isn't just important, it's everything. This is our moment to build the national workforce infrastructure our ecosystem needs, one that matches the scale of our ambitions and the promise of what we can achieve together."

NNFME"A key component of our nation's technology strategy has to be talent — specifically, ensuring our nation has a world-class workforce that is qualified and equipped to compete globally in the technology sectors we know will drive the economy of the future," said Erwin Gianchandani, NSF Assistant Director for Technology, Innovation and Partnerships. "NSF is thrilled to be investing in the National Network for Microelectronics Education, which will coordinate and expand access to workforce training opportunities for America's semiconductor industry. Together with

the private sector, NNME will bolster opportunity for all Americans and strengthen our competitive advantage in a technology sector critical to our economic future and national security."

"NNME is more than a workforce initiative — it's a national call to collaborate," said Michelle Williams, Executive Director of the SEMI Foundation. "We believe the greatest breakthroughs in microelectronics workforce development will come not from isolated efforts, but from strong, coordinated partnerships rooted in communities across the country. Through NNME, we're creating a framework where industry, education, and local leaders can work hand-in-hand to make a lasting impact."

Regional Nodes are expected to be collaborative, location-based partnerships that anchor workforce development strategies for the semiconductor industry. They will bring together employers, education providers, and community organizations to: Coordinate talent development aligned with local and national industry needs,
Expand access to training and work-based learning for all populations across a full range of job types and educational attainment levels, and
Support employer engagement in the co-design of programs.
The Regional Nodes will serve as innovation hubs, building replicable models for scalable impact across the ecosystem.

Regional Nodes are expected to be collaborative, location-based partnerships that anchor workforce development strategies for the semiconductor industry

Data centre semiconductor trends 2025: AI reshapes compute and memory markets

Yole Group publishes its new report, Data Center Semiconductor Trends 2025, offering an in-depth analysis of how AI, HPC, and hyperscaler demand are driving a new semiconductor paradigm.

THE SEMICONDUCTOR backbone of global cloud and AI infrastructure is undergoing a profound shift. Yole Group's Data Center Semiconductor Trends 2025 reveals a market at an inflection point, driven by explosive AI growth and fundamental architectural change.

In 2024, the total semiconductor TAM for data centers reached $209 billion, spanning compute, memory, networking, and power. By 2030, that figure is projected to grow to nearly $500 billion. AI and HPC are now the dominant use cases, with generative AI alone reshaping demand across processors and accelerators.

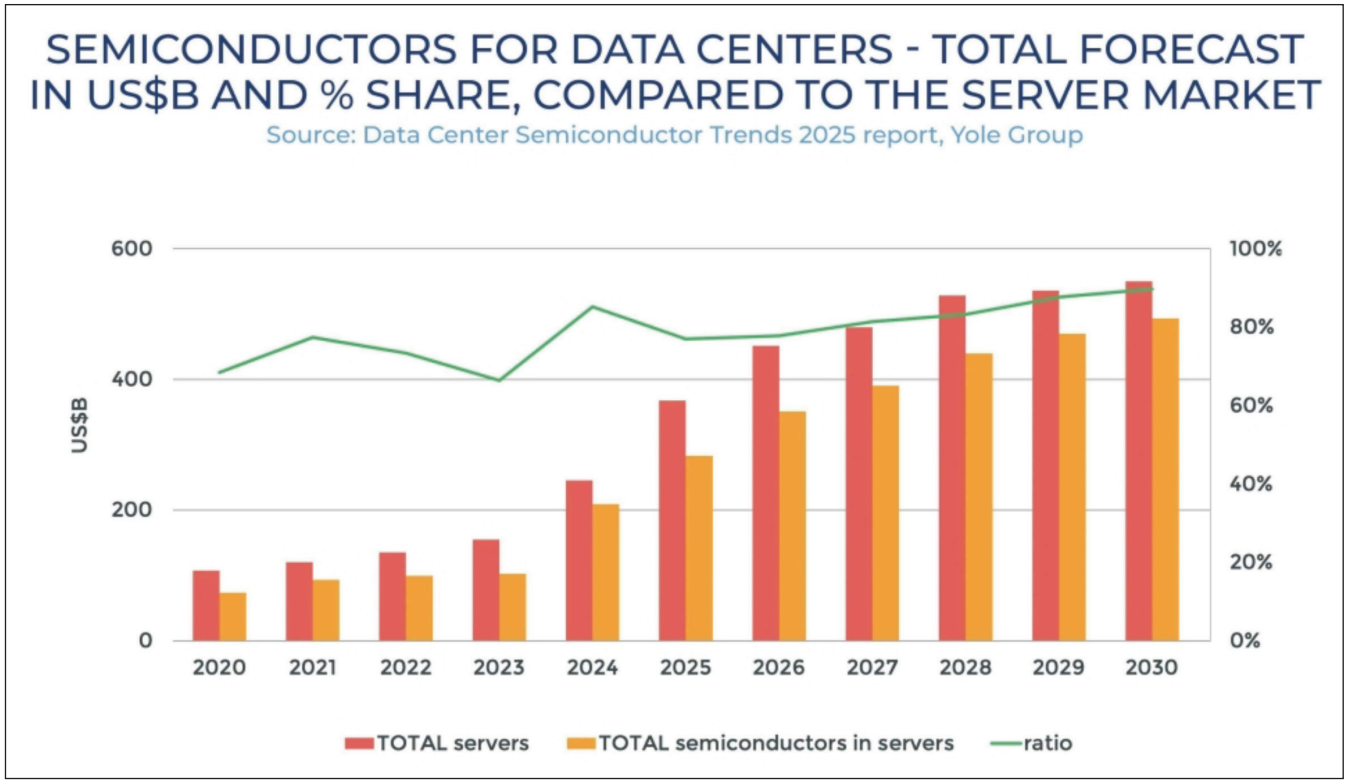
GPUs remain the cornerstone of AI infrastructure, with Nvidia capturing 93% of the server GPU revenue in 2024. Yole Group, the market research & strategy consulting company, forecasts GPU revenue will grow from $100 billion in 2024 to $215 billion by 2030. Despite their high ASPs, GPUs are indispensable for AI training and are increasingly used in inference.

In this dynamic environment, AI ASICs are gaining momentum. Google, Amazon, and Microsoft are investing in domain-specific silicon to optimize performance and reduce dependence on Nvidia. Based on the entrance of these leading companies, AI ASIC revenue is expected to skyrocket to $84.5 billion by 2030.

Compute is not the only bottleneck. Memory architecture is also evolving rapidly. DDR5 adoption continues. HBM is seeing exceptional demand, especially for AI training. CXL is gaining traction to solve memory disaggregation and latency challenges in new server architectures.

Leadership in data center silicon is also shifting. US players remain dominant, especially Nvidia, AMD, and Intel. But Yole Group's analysts point out that China is scaling up its domestic capabilities through strategic investment and policy. Export controls continue to impact supply chains but also reinforce sovereign development goals in China and beyond.

Startups and newcomers are also part of the game and shaping the market. From Groq to Cerebras and Tenstorrent, innovation in chip design is pushing the frontier of what AI inference hardware can do. Sometimes, novel solutions challenge established players on cost, performance, or energy efficiency.



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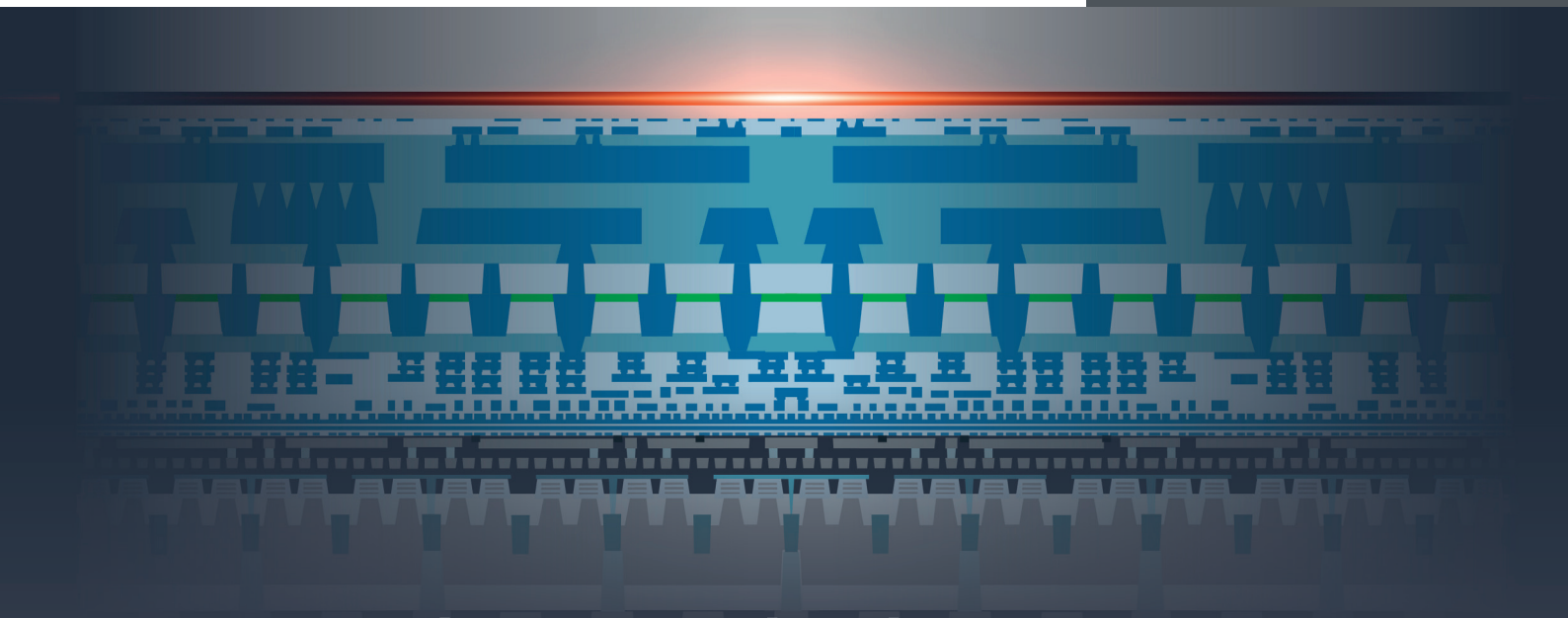

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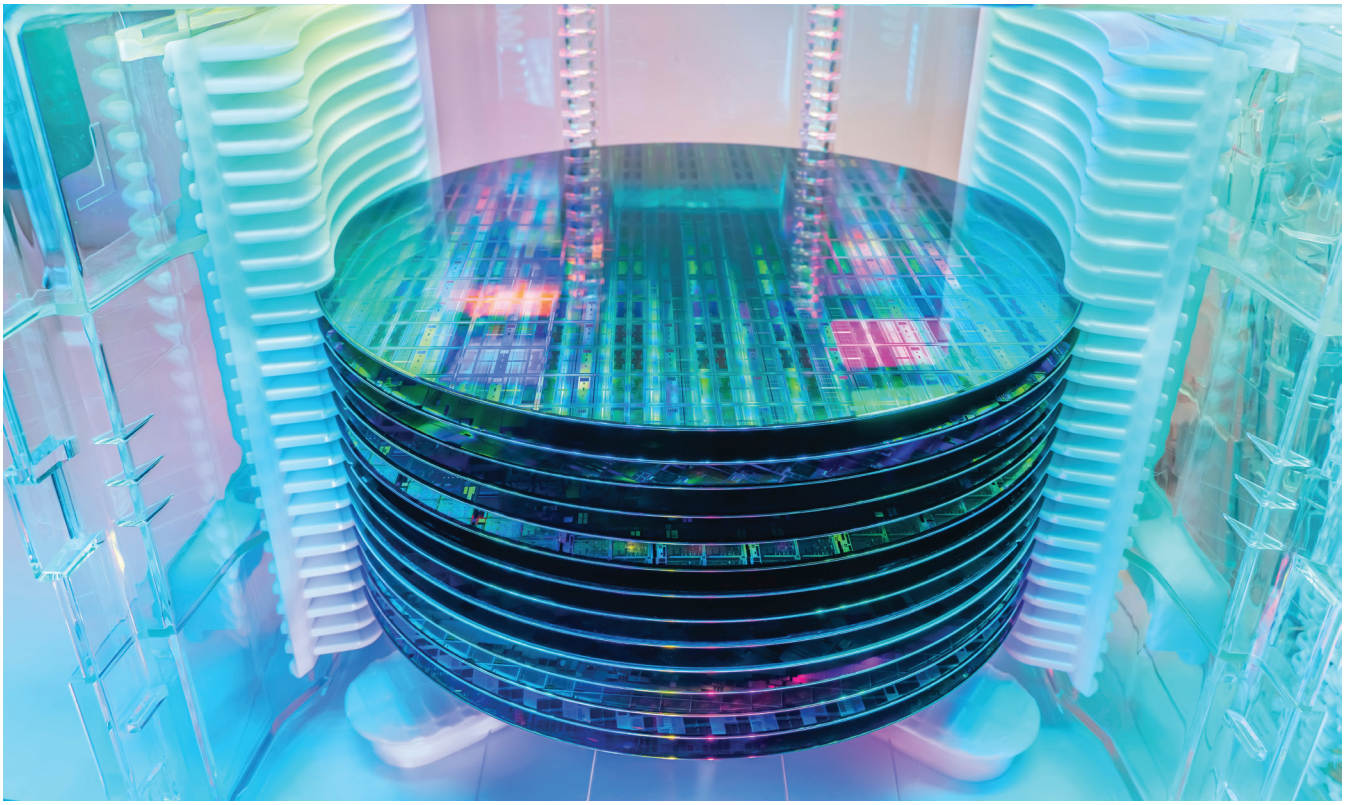


Predictive maintenance in the semiconductor sector: how Edwards Vacuum is shaping the future of reliability

Predictive maintenance for vacuum pumps is no longer an experimental idea — it is a proven value driver in semiconductor fabs worldwide. By marrying decades of vacuum science expertise with cutting-edge data science and AI, Edwards Vacuum has built a leadership position in this critical domain.

SEMICONDUCTOR manufacturing is an unforgiving business. The complexity of the processes, the astronomical value of wafers, and the constant pressure to drive down cost while scaling up performance mean that every piece of equipment in a fab must operate with absolute precision. Among these critical systems are vacuum pumps, the often-overlooked workhorses that underpin etch, deposition, and other fundamental processes.

When a vacuum pump fails unexpectedly, the consequences can be catastrophic. A single wafer can be worth tens of thousands of dollars; in batch processes, an entire lot could represent millions in scrapped product. In an industry where margins are thin and throughput is paramount, the ability to predict and prevent vacuum pump failures is no longer a nice-to-have — it is a strategic necessity.

This is where predictive maintenance comes in. While preventive maintenance schedules have long been a feature of fabs, the ability to forecast failures before they happen, based on real data rather than arbitrary calendars, has transformed expectations. And at the forefront of this transformation is Edwards Vacuum, a global leader in vacuum and abatement solutions for semiconductor manufacturing.

This article explores the evolution of predictive maintenance in the semiconductor sector — from pre-AI roots to the latest machine learning and digital twin models — and examines how Edwards Vacuum is deploying data science, domain expertise, and IoT technology to deliver game-changing value to its customers.

From preventive to predictive - an historical perspective

Before the rise of AI and machine learning, predictive maintenance largely relied on rules-based approaches. Engineers would monitor key parameters — vibration, temperature, power draw, exhaust composition — and set thresholds for when interventions should occur. Using decision trees and other statistical models, these early predictive maintrenance systems achieved respectable accuracy, often outperforming time-based schedules.

The foundations of machine learning were laid decades ago, but it is only in the last 15 years that computing power has caught up with the theory. Edwards and other advanced manufacturers were already experimenting with digital twins and rule-based models well before AI became a buzzword.

On vacuum abatement equipment, these models proved particularly effective; for dry pumps, accuracy was more challenging but still offered tangible benefits compared to rigid maintenance calendars.

The real game-changer, however, came when better data capture and higher-quality sensor inputs met the rise of advanced machine learning. By investing heavily in data acquisition infrastructure, Edwards set the stage for a step change in predictive accuracy. With high-resolution time-series data streaming from pumps, machine learning models could spot subtle signatures that precede failure — signatures invisible to rules-based systems.

The cost of failure - why prediction matters

In semiconductor fabs, two basic maintenance strategies historically dominated:

- **Run-to-fail –** Pumps and abatement are operated until they break. This is common in single-wafer processes where the loss of one wafer is painful but manageable.
- **Scheduled replacement –** Pumps and abatement are swapped at conservative intervals to prevent catastrophic failures during batch processing, where dozens or even hundreds of wafers are at stake.

Both strategies carry heavy costs. In run-to-fail scenarios, every failure risks unplanned downtime and lost product. In scheduled replacement regimes, pumps are often serviced or replaced long before their useful life is exhausted. Edwards engineers routinely find pumps that are “clean as a whistle” internally, removed only because the schedule said it was time.

Predictive maintenance provides a third path: run-to-predict. Instead of guessing, fabs can use real data to make informed decisions. Vacuum systems can be operated closer to their true limits without crossing them, minimizing both scrap risk and unnecessary replacements. The Edwards approach is tailored.

Tailored models for specific failure modes

A key insight from Edwards’ work is that not all pump failures are created equal. Vacuum pumps in semiconductor fabs are exposed to hostile environments - corrosive gases, deposition byproducts, and extreme duty cycles.

Different processes lead to different degradation mechanisms. For example, corrosion occurs gradually as corrosive gases attack pump internals. These are relatively easy to detect, as degradation trends are slow and steady. In contrast, when it comes to deposition byproducts accumulating inside the pump, leading to blockages or seizure, these failures are more abrupt and therefore harder to predict.

Rather than attempting a “one size fits all” predictive model, Edwards builds specific models for each failure mode and pump family, tuning them to the customer’s process conditions.

remarkable results, with prediction accuracies north of 95% for corrosive processes and 70-90% accuracy for depositive processes, depending on the customer and the specific process. These accuracies are 30 -40% higher than attempts to use generic models. The lesson is clear - domain expertise and failure-mode specificity matter just as much as raw machine learning power.

The data advantage – needles and haystacks

Machine learning thrives on data — but without domain knowledge, models can mistake noise for signal. Edwards’ advantage lies not only in the sheer volume of pump performance data it has accumulated over decades, but in its deep vacuum science expertise. Building predictive models is a little like looking for a needle in a haystack. AI can sift the hay faster, but Edwards knows what a needle looks like. By combining physics-based insights with statistical analysis, this avoids false positives and delivers actionable intelligence.

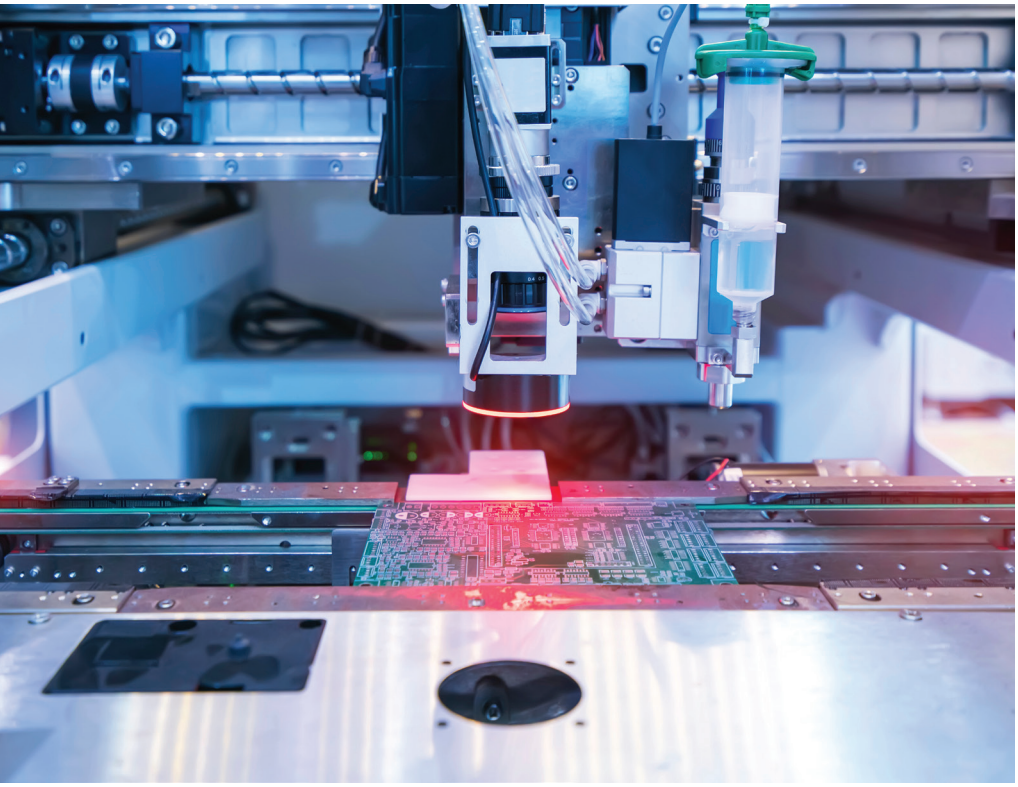
This fusion of human expertise and algorithmic insight is what makes Edwards’ predictive maintenance solutions robust in real-world fabs.

Dollars and downtime

Ultimately, fabs care about total cost of ownership (TCO) and yield protection. Predictive maintenance delivers on both fronts.

While Edwards guards its proprietary ROI calculators, the company can quantify benefits for each customer by analyzing historical pump failures, wafer scrap events, and unplanned maintenance. For many fabs, the savings run into hundreds of thousands of dollars per year, by moving breakdown maintenance to corrective maintenance.

But the benefits extend beyond customer savings. Predictive insights



allow Edwards itself to optimize its service network. For example, if the company can forecast a quantity of potential pump failures across a region weeks in advance, it can stock the right spare parts, schedule the right number of technicians, and streamline logistics. This not only reduces Edwards' operating costs but ensures faster, smoother service for customers.

Beyond prediction - optimization and self-tuning

Predictive maintenance is not just about avoiding failure; it also opens the door to optimizing vacuum system performance.

By analyzing operational data, Edwards' teams often discover simple configuration tweaks — for example, adjusting pump temperature by a few degrees — that dramatically reduce failure risk. These insights, delivered as part of Edwards' service packages, represent an additional layer of value beyond prediction.

Looking ahead, Edwards envisions a future where pumps may be able to reconfigure themselves autonomously in response to changing process conditions. While industry conservatism and safety concerns make this a longer-term goal, the trajectory is clear: predictive maintenance is evolving into prescriptive maintenance, and eventually toward self-optimizing equipment.

Building and deploying the models

Edwards' predictive maintenance models are structured around standard models for pump families and failure modes and customer-specific tuning, enabled by a sophisticated simulation environment.

By replaying years of pump data in a matter of hours, Edwards can test and refine models before deploying them live. This rapid iteration allows them to demonstrate predicted hit rates with confidence and customize solutions without prolonged trial-and-error on the fab floor.

Deployment is flexible. Edwards' data platform is designed cloud-first, offering scalability, real-time monitoring, and fleet-level visibility. For customers wary of the cloud, edge deployments are possible — either on-site or within the customer's own private cloud.

Alerts and decision-making can be handled by Edwards' service teams, integrated into fab management systems, or both. The flexibility reflects a key principle, that customers choose the level of autonomy they want, while Edwards protects the proprietary core of its models.

Next-generation pumps - Ganymede and IoT in action

Edwards' upcoming Ganymede platform exemplifies the convergence of predictive maintenance and IoT. Unlike previous pumps, where the control and communication functions were bundled on a single microcontroller, Ganymede introduces a dedicated gateway controller with substantial compute power.

This allows predictive models to run directly on the pump itself, reducing latency and dependency on external systems. Data still flows into EdCentra for fleet-level oversight, but the pump becomes more autonomous, embodying the long-promised vision of industrial IoT. The IoT hype cycle has passed through its 'trough of disillusionment', what remains is a mature, pragmatic use of connected devices — and Ganymede is poised to be a flagship example.

The role of digital twins

Digital twins — virtual replicas of physical systems — are another AI frontier for Edwards. The company's service centre teams are already using twins of maintenance facilities to simulate pump flows and optimize operations.

For predictive analytics, the challenge is tougher: accurately modelling the physics of a vacuum pump in real time is enormously complex. Edwards is tackling this incrementally, starting with subsystems like cooling circuits. The long-term goal is to combine physics-based twins with machine learning models, yielding hybrid approaches that are both interpretable and accurate. Full pump digital twins may be several years away, but the trajectory is set - twins will complement AI by embedding physical causality into predictive systems.

Toward deeper fab integration

One exciting prospect is integrating pump data with process tool data. In theory, knowing process gas flow rates or chamber conditions could make predictive models even more accurate. In practice, fabs are fiercely protective of recipe data, and OEMs guard their equipment telemetry closely.

This is a longstanding cultural barrier, rooted in the semiconductor industry's

history of secrecy and 'paranoia'. Yet there are signs of progress. Edwards can already show how combining pump and abatement system data — both under its umbrella — improves prediction accuracy. Extending this logic to fab-level integration may be inevitable, especially under the combined pressures of sustainability, yield, and cost efficiency.

The challenge will be coordinating collaboration across OEMs, fabs, and suppliers while maintaining confidentiality. Initiatives like SEMI standards and third-party data platforms may provide the neutral ground needed.

Overcoming human and cultural barriers

Predictive maintenance is as much a people challenge as a technical one. Operators with decades of experience often pride themselves on their "gut feel" for when equipment is failing. Far from displacing this expertise, Edwards' models often validate it, providing data-driven confirmation. Resistance does exist, but results speak louder than scepticism. Once engineers see higher uptime and fewer scrapped wafers, they tend to embrace the technology.

At a broader level, the semiconductor industry's caution toward cloud adoption remains a barrier. Concerns about data leaving the fab walls are deeply ingrained. Yet as Edwards points out, the very IT security technologies developed by the semiconductor industry underpin the safety of cloud systems used in banking, pharma, and other critical sectors.

For Edwards, the vision is clear - a 'control room' model (similar to the Rolls-Royce aerospace approach), where specialists monitor pump performance worldwide in real time and proactively guide maintenance. Achieving this requires industry-wide comfort with cloud-based data sharing — a cultural shift that is gradually unfolding.

The road ahead

Edwards' predictive maintenance journey is still evolving. The near-term roadmap includes:

- Wider deployment of cloud-first data platform.
- Rollout of Ganymede pumps with onboard predictive capability.
- Continued progress on digital twins for subsystems.
- Exploration of deeper fab integration under secure data-sharing frameworks.
- Leveraging predictive insights for Edwards' own service network optimization.

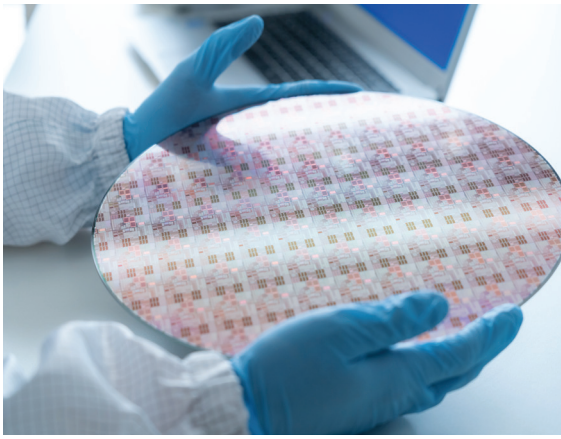
Longer-term, the possibilities include autonomous self-tuning pumps, AI-driven operational efficiency across regions, and hybrid models combining machine learning with digital twins. In every case, the goal is the same: to reduce downtime, extend pump lifetimes, and protect yield in one of the most unforgiving industrial environments that exists.

Conclusion

Predictive maintenance for vacuum pumps is no longer an experimental idea — it is a proven value driver in semiconductor fabs worldwide. By marrying decades of vacuum science expertise with cutting-edge data science, Edwards Vacuum has built a leadership position in this critical domain.

From tailored failure-mode models to IoT-enabled next-generation pumps, from service-centre digital twins to visions of real-time global monitoring, Edwards is demonstrating how predictive maintenance is evolving into a broader paradigm of predictive operations.

In the relentless pursuit of yield, uptime, and efficiency, predictive maintenance is not just about pumps — it is about the future of semiconductor manufacturing itself. And Edwards is helping to write that future, one (AI-enabled) pump at a time.



SEMICON West reaches new heights in Phoenix

A comprehensive overview of the forthcoming SEMICON West 2025 event, held for the first time in Phoenix, Arizona. The show floor has grown from 1,100 exhibitors in 2024 to more than1,500 this year, and the packed conference programme boasts just under 600 presentations covering the sector's current challenges and opportunities, including AI and quantum computing, cybersecurity, the skills shortage, sustainability, supply chain, heterogeneous integration, and more.

SILICON SEMICONDUCTOR INTERVIEW WITH JOE STOCKUNAS, PRESIDENT, SEMI AMERICAS

SIS: *The obvious place to start is that we have a brand new venue for SEMICON West - Phoenix, Arizona. How much was the decision influenced by the fact that Arizona is a big semiconductor ecosystem and growing. Why Phoenix?*

JS: I made the decision shortly after coming into this role in 2022, and things were really just getting started in Arizona, but it certainly turned out to be a very good decision as a result of Arizona being successful in attracting over $200 billion worth of investment. Now, an awful lot of that's just with TSMC, but there's plenty more. I've been to countless ribbon cuttings in the Phoenix area over the last few years and I've got three during SEMICON week. So, it really has worked out very well. The decision goes back to the fact that I feel very strongly about hosting SEMICONs where there's a semiconductor community. I wanted to do something a little bit different.

I looked at where that community exists. We looked at San Jose, Portland, Austin and, of course, Phoenix. The Phoenix Convention Centre really was the one that was most attractive because it was large enough to handle our growth. That's worked out very well. We sold out the show floor. We've never done this before. We sold out the show floor almost a year in advance. The show's in October this year. By the end of last November, we were completely sold out on the show floor. We kept taking waitlist requests from companies. In March, we had 280 companies on the waitlist. I looked at this and said, we've got to do something, I don't want to turn away 280 companies. The main show floor is similar to Moscone in San Francisco, one level below street level. Adjacent to where the keynote stage will be, that auditorium is where we will have additional exhibition space. We've opened that up, and we sold that out now as well. Last year, we had just over 1,000 booths at Moscone. And as of yesterday, we were at 1,535 booths. We've got a 50% increase in exhibitors this year, and we've got a great exhibition.

And content at the show will be fabulous. We'll actually have four days of content. The exhibition will only be open Tuesday, Wednesday, Thursday. But Monday afternoon, we've got our Market Symposium, and that is very

attractive to many. We get a huge crowd for that. During this session, SEMI's own analyst along with others that we collaborate with through the year will provide different perspectives on what to expect in the semiconductor market. Overall, right now, we have 567 speakers lined up in those four days across 63 different content sessions. Again, last year, I think we had about 450. We're up nicely on the number of speakers.

SIS: *I was going to ask if you could point out what you think might distinguish the new location from the traditional home in San Francisco. You've already partly answered it because clearly the show is going to be bigger. Is there anything else you think that's going to distinguish it being in Phoenix as opposed to San Francisco?*

JS: It's really interesting just how many companies are involved in semiconductors in Phoenix. There's a very large number of big companies like Intel and TSMC, certainly. But there's an awful lot of infrastructure in the industry based there as well. A number of our equipment and materials suppliers have located their headquarters in the area and have been there for a long time.

Companies like ASM and EV Group and a company I used to work for. I ran the electronics materials business at Air Products. Now, that division was sold off to Merck KGaA, Darmstadt, Germany and goes by EMD Electronics in the US. And again, they've got their headquarters for US now in Phoenix as well. So, a really great opportunity.

And what I think will be different is, I'll be honest, I'm a little jealous of my peers in Asia, the shows in Asia are just unbelievable. We had 180,000 people in China in March at SEMICON China in three days, and Japan broke 100,000 people. And the difference is in Korea, Samsung and SK hynix combined bus 17,000 employees to come to SEMICON Korea. And that's the difference for us in Phoenix this year - we've got those operating companies, the fabs, the equipment suppliers, material suppliers, the rest of the infrastructure that makes up semiconductor.

People are going to come and kick the tires this year. It'll be a great show. Again, being in Phoenix, I'm expecting that our crowd will increase. Last year, we had about 25,000 people, I think maybe 27,000. But this year, I'm very confident that we'll be over 35,000 and probably closer to 40,000 people this year. Being in Phoenix, where that infrastructure is established and people go to work every day in semiconductors, will bring more people into the convention centre, and we're really excited about that. It'll have a real buzz. Since the CHIPS Act, our shows had a real buzz. The show floors are crowded. There's a lot of folks there. This year, I think it'll even be bigger and better with us being in Phoenix where so much is going on.

SIS: *You referenced some of the shows in Asia. Do you still view SEMICON West as very much a global event, bringing people from around the world to come and discuss some of the industry challenges and obviously the momentum? I still think the $1 trillion mantra is somewhere out there, isn't it? But do you think you're going to get that global audience and this forum to discuss what's needed?*

JS: I think you asked me three questions there!

So, your first question, the global show. SEMICON West was the original show, the first SEMICON we ever had, and that was in 1970 and back in Silicon Valley. And SEMI is headquartered in the US. The view of West is it's both the Americas show, so SEMICON for the Americas business, but it's also the headquarters show as well. As a result, it has always been very well-attended. We don't have the numbers that China has, but all the movers and shakers

are at SEMICON West, and that will continue.

We do a really good job of tackling the issues that are facing our industry. That is very key to it. We are very much on the path to $1 trillion. To give you some feel for that, the semiconductor sales revenue, that's $1 trillion in global semiconductor sales. Last year, we finished the year at $619 billion and we're seeing very significant growth this year, maybe to $720 billion.

We had double-digit growth, high over 20% last year. And this year, most of the market analysts are projecting at least 15%. We're well on track to $1 trillion. That was your second question. And that's really exciting for us. It is a good time to be in semiconductors.
And your third question, I think it was, will we tackle the issues? And as I said, we very much tackle the issues at this event. We've got a great keynote schedule. We'll have keynotes Tuesday, Wednesday, and Thursday morning.

Last year, we just did all day Tuesday and all day Wednesday. And what I did was I focused on the Americas

issues on Tuesday, which was really the growth in America. It was really celebrating how much investment was happening in the US. Then on Wednesday, we took a look at the global opportunities and issues and split it up that way. My only regret was, if you go later in the day like we did, you're competing with the show floor. I had wonderful speakers in the afternoon, and my only complaint was they deserved a bigger audience.

This year, I'm limiting it. The show floor doesn't open until 10:00 a.m., and we'll be finished with the keynotes on Tuesday and Thursday at 10:30 a.m. And on Wednesday, we're going a little bit longer till 11:30 a.m. And the reason is on Wednesday, it will be AI day. We will start off with NVIDIA, and we will have all presentations focusing on how AI impacts and creates opportunity for the semiconductor industry. We've got great presentations on AI.

We'll go a little bit longer. But for the most part, I don't want to see us competing with the show floor. Again, we will be tackling all the opportunities and issues, which today, great growth opportunities, driven principally by AI, but then the other markets that we're very excited about, automotive, manufacturing, industry 4.0, 5.0, as you see it, MedTech, the continued demand for communications and computing capability, and the advancement into quantum computing in the future. All those opportunities will be covered in great detail, both with the keynote presentations and the other 62 sessions that provide the over 560 speakers I mentioned earlier.

We'll also have a lot to talk about on talent. Our industry is very much self-governing right now in wanting to make these investments and do them the right way and be environmentally sensitive with it. Growing issues with cybersecurity. Cybersecurity has really been the new issue that we're putting more effort into. So, it is very much the headquarters show, and we will cover all the opportunities and issues that are present for the industry today and for the next five years as we move forward on that path to $1 trillion.

SIS: *That's answered a couple of my next questions. You're ahead of me there. I know that the main theme is, 'Stronger together', which is, I guess, looking at the cross-industry collaboration. I'm just interested how far you think that can go because I've talked to a couple of people, you referenced AI, and clearly a large part of that is the data. I know traditionally, semiconductor companies are reluctant to share data for obvious reasons. But if the full potential of AI is going to be realised, they maybe will have to do something around that. Just your thoughts, I suppose, as to how far collaboration needs to go in the industry?*

JS: I think we've really seen changes in collaboration. The SEMI supply chain initiative is very much led and engaged by us, but we've had Intel and TSMC partnering with us from day one in establishing that supply chain initiative. I've worked in the industry for 40 years and it was very difficult to get data, very difficult to get forecasts, even more difficult to get accurate forecasts. Then we have chip shortages, and that's recognised now. I do think there's a whole lot more collaboration in general.

I can point to that, but I'll also point to when you talk about the technology demands now, it's a number of entities working together. It's certainly the tradition of the device manufacturers, the equipment manufacturers, and the material suppliers, and others. Now, again, design companies are coming into it as well in that, to make the most advanced chips, no one's doing it alone today. And that collaboration is recognised. A number of the large companies are speaking openly about this, I've actually heard one of them talk about the fact that 'we recognise we have to collaborate with our competitors now'.

I worked in the chemical/semiconductor industry for many years. And in the chemical industry, it's a common practise. In some cases, we have a relationship where we're competitors, in others, we're suppliers, in others, we're buying from each other. I think that's coming to fruition now in the semiconductor industry as well, principally driven by the needs for a reliable and resilient supply chain, and then also the demands of the technology going forward.

SIS: *In terms of a quick overview of what's going on, you've mentioned the CEO Summit, but I think there are executive panels, workforce development. I think the SEMI University is there, and there are lots of technology sessions, and then there's the show floor. I've probably asked you about three questions in one, but can you give us a flavour of content, both in terms of the speakers, the conferences, and then what people can see on the show floor?*

JS: As I mentioned a little bit earlier, the CEO Summit will be Tuesday, Wednesday, and Thursday. I've got anchor presentations on Tuesday. We'll start off with the Governor of Arizona, and we'll end up with TSMC. And in between, there's another three or four presentations that are equally powerful. On Wednesday, it's AI, and we start off with an NVIDIA presentation.

I'm hoping they bring the dog! It's a programme around AI and robotics and

tied to semiconductor opportunities for AI, but I'm really hoping they bring the dog - I hope at least some videos! And then the last session will be very interesting. Our friends from Merck KGaA, Darmstadt, Germany are actually bringing the global people officer and head of strategy in the US, and they're going to do a presentation on how they see AI impacting their workforce, how they'll gain advantages, where their concerns lie. And then on Thursday morning, we've invited Department of Commerce to speak. We've invited Intel to speak about their foundry business and where that's going.

And then we finish up with a presentation on cybersecurity. And that presentation will be by Keith Krach. Keith was the CEO of DocuSign, so very well-versed in security. And he also served in a previous administration in the Department of State, so very much a global view as well. And again, one of our biggest challenges now is protecting our data in this big data AI world that we're all in.

I walked away from SEMICON West last year and looked at what were my big takeaways? The number one on my list was my last position in industry, I worked in back-end packaging and test equipment. I had seven different product lines for test and high-speed dispense for packaging applications. For the last 10 years, I've been working on advanced packaging, and advanced packaging was the future. I walked away from the show last year, and my view was that the future is now for advanced packaging. We will have an awful lot more content, and that's very prevalent today, as you see all the things that are being discussed on the packaging that's used for the most advanced chips, the stacking, the memory. You will see a whole lot more content in our agenda that focuses on advanced packaging, heterogeneous integration.

In terms of workforce development, we're really proud at SEMI to have been selected to operate the National Network for Microelectronics Education, and we'll look to shepherd the implementation of a national programme. You'll see and hear a whole lot of what's going on in workforce development with SEMI in the US and globally, during the presentations and also on the show floor where we'll have

a workforce development pavilion. Over the last few years, there's been a real buzz in the show. We've had wonderful attendance, we've had a large number of speakers, great content and great exhibit show floor.

This year, the thing I'm trying to bring to it is a bit more recognition and celebration. On Monday evening, we will have our first ever gala. It's called the Legends and Leaders Honors event, where we will recognise Lisa Su, the CEO of AMD, as our first award recipient for the SEMI Silicon Medal. First time we've ever done that so it will be a big time celebration on Monday evening. On Tuesday evening, we will have a street fair. We've got a country western band, and we've got a bunch of new activities on Third Street, which separates the two buildings in the Convention Centre, and we're going to have fun on Tuesday night.

We're not going to compete with many of our large customers at SEMI who host hospitality from 5:30 p.m. to 8:00 p.m. So, from 8:30 p.m. till about 11: 00 p.m., we're going to have this street fair, and it'll be fun folks.

Additionally, during the CEO Summit, each day we'll have at least two presentations recognising technology advancement. We have a 20 Under 30 recognition where we recognise 20 people under 30 years of age. We'll present the SEMI Catalyst Award to one of the global companies that's been in Phoenix for a long time and still today is providing enabling technology for the advancement of our industry. We'll have a host of different presentations where we're recognising people on stage as well.

SIS: *In closing, I guess it'd be good to understand if there was one thing you wanted people to take away, that might be difficult, so it might be two or three things, but what you want them to go away with, and then, in my tradition of asking you at least two questions in one, for people who are attending for the first time, would you have any advice? You've given us the numbers. They can't, I expect, get round all 1,500 stands or listen to all of the presentations. Any tips as to how best to get stuck into SEMICON West?*

JS: First thing is, visit our website, www.semiconwest.org. You need to visit our website, first of all to register for the event. Our agenda is organised in many different ways. You can see the full agenda and decide what presentations you must hear. The show floor map is there. You can search on specifically what exhibitors you might want to see when you go to visit. You can see where the social happenings are occurring all on that same website.

Overall, what I'd like to leave everyone with is we're clearly on the path to $1 trillion, but it's not going to come to you. It's a very competitive world right now. If you want a part of that $1 trillion, come to SEMICON West, have a plan. There's tremendous opportunities for you to network, develop business contacts, figure out where you can most advance your opportunities in the semiconductor world. It's a very exciting world right now. It's happening all over the... well, not quite all over the world, but we've got eight SEMICONs and pretty much wherever there's a SEMICON, there's a lot of activity right now in the semiconductor world. Come to SEMICON, make the contacts, do the networking, and come ready with a plan so you can maximise your opportunities in three days.

www.semiconwest.org

Innovative partnership for resource-efficient wafer inspection

Fraunhofer IPMS and DIVE optimise semiconductor processes with ‘cutting-edge’ measurement system.

THE FRAUNHOFER INSTITUTE for Photonic Microsystems IPMS, in collaboration with DIVE imaging systems GmbH, has achieved a major milestone in resource-efficient semiconductor manufacturing. With the successful installation of an optical measurement system by DIVE in the cleanroom of Fraunhofer IPMS, the effort required for quality control during wafer production has been significantly reduced. This collaboration paves the way for a more sustainable and efficient semiconductor production process.

Semiconductor manufacturing involves up to 1,500 process steps, including etching, deposition and lithography. Due to their complexity of structures, finished wafers must be nearly defect-free, which requires rigorous quality control. As a result, up to 50% of process steps are dedicated to metrology and thousands of additional control wafers are produced each month. This requires substantial additional financial and material expenditures as well as energy and time resources.

The project “NEST” (New Screening Tool for Efficient Semiconductor Manufacturing) directly addresses this issue. Over the past 1.5 years, DIVE, together with Fraunhofer IPMS and Fraunhofer IZM has conducted an environmental potential analysis. The study revealed that targeted inspection tools could reduce control wafer usage by at least 25%, while also saving more than 118,000 kilograms of CO_2 emissions during production every month.

➤ Quality inspection in the wafer manufacturing process. © Fraunhofer IPMS

DIVE’s solution uses an innovative combination of spectroscopy and imaging technologies capable of identifying defects even in deeper wafer layers. The analysis was based on a 28 nm manufacturing process and 25,000 wafer starts per month. The project was funded within the “Green ICT Space” by the Research Fab Microelectronics Germany (FMD).

In addition to CO_2 savings, the system offers further ecological benefits, such as the reduction of water and chemicals used in control wafer production.

Furthermore, the reduction of metrology steps also improves energy efficiency by freeing up tool capacity; an early detection of process deviations avoids misproduction and improves the overall productive wafer yield, which results in an economic advantage as well.

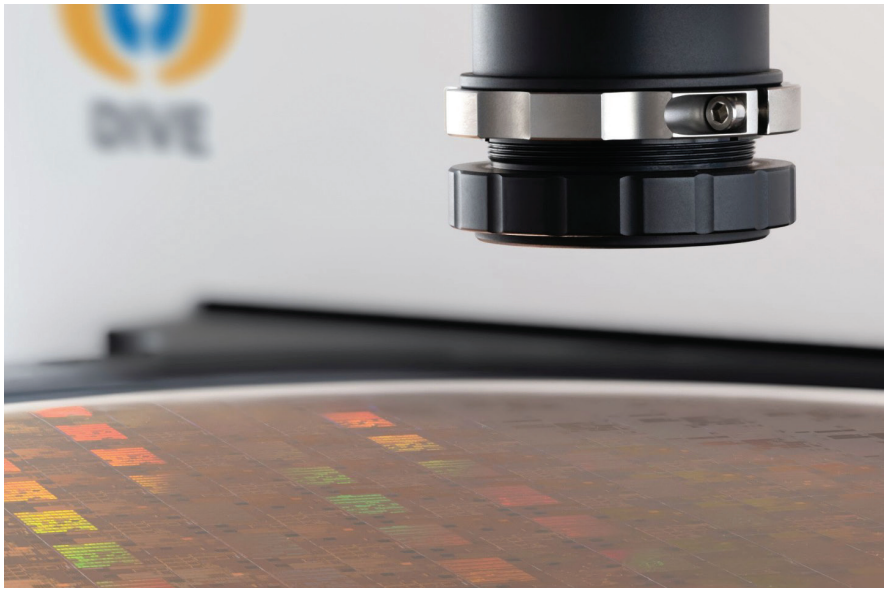
Industry-ready evaluation in cleanroom Environment at Fraunhofer IPMS

DIVE imaging systems GmbH develops advanced inspection tools that combine the benefits of optical spectroscopy with imaging. The DIVE VEpioneer® is the first of its kind to operate under cleanroom conditions.

It rapidly assesses surface properties, contamination and deviations from

production specifications in just 20 seconds. The integration of AI algorithms enables comprehensive process control while significantly reducing testing efforts. “DIVE’s hyperspectral imaging systems offer a new way of non-destructive wafer inspection. With the support of Fraunhofer IPMS, this innovative technology is now available for use in standardized industrial cleanrooms – enabling significant productivity gains and cost savings for semiconductor fabs,” says Martin Landgraf, R&D Manager at Fraunhofer IPMS.

After the successful conclusion of the project, the DIVE VEpioneer® system will remain at Fraunhofer IPMS’s Center Nanoelectronic Technologies (CNT) for continued wafer measurement and evaluation for customers and partners. Further joint projects are planned to enhance the system with wafer handling automation and equipment integration for an automatic data transfer. With the acquisition of DIVE imaging systems GmbH by PVA TePla AG, the start-up now gains new opportunities for evaluation and development – particularly through the expertise of the material and metrology specialist.



Imaging Systems from DIVE for a non-invasive wafer control. © DIVE imaging systems GmbH

Pure water for sustainable semiconductor production

AlixLabs and NSS Water are pleased to announce a strategic collaboration to develop sustainable and cost-effective ultrapure water (UPW) management solutions for chip production. Amid rising concerns over the semiconductor industry’s ever-increasing water consumption the two Swedish companies will team up to address this challenge.

The project value is approximately 28,000 euros, with funding coming from the European Union’s ASCENT+ program and is overseen by the Fraunhofer-Institute for Photonic Microsystems IPMS.

By integrating Fraunhofer IPMS’s state-of-the-art metrology expertise in advanced defect and contamination control, the partnership aims to improve and elevate water recycling methods, reduce chemical usage, and optimize overall process efficiency – paving the way for smarter water solutions in a water-constrained future.

Nano-pure water for sustainable water consumption

According to industry data, the semiconductor sector has experienced a 20–30% increase in water consumption in recent years, with the average chip manufacturing facility using up to 10 million gallons of UPW daily – an amount equivalent to the daily water needs of a city of 300,000 people. Producing UPW traditionally comes at a significant cost: it can be 60 to 350 times more expensive than drinking water due to the intensive energy and chemical processes required.

This is the challenge NSS Water addresses with its nano-pure water (NPW). The semiconductor industry’s water consumption is projected to keep increasing due to more advanced plants with higher consumption coming online in the coming years.

Additionally, 40% of chip production facilities are projected to be located in high-water-risk areas by 2030, meaning the need for data-driven, circular water strategies has never been more critical.

“Water is the lifeblood of our planet and the backbone of the semiconductor industry,” says Reza Jafari Jam, Research Director at AlixLabs. “This collaborative research on water conservation not only safeguards a finite resource but fuels innovation, ensuring sustainable growth and technological advancement. We push the semiconductor industry to be more sustainable with our APS™ patterning process technology and our collaboration with NSS Water will further solidify our position as an enabler tomorrow’s green semiconductor production.”

By integrating Fraunhofer IPMS’s state-of-the-art metrology expertise in advanced defect and contamination control, the partnership aims to improve and elevate water recycling methods, reduce chemical usage, and optimize overall process efficiency – paving the way for smarter water solutions in a water-constrained future

Cooperation for advanced semiconductor manufacturing

"We are happy to expand our collaboration with AlixLabs and Fraunhofer IPMS," says Björn Holmström, CEO at NSS Water. "The importance of advanced metrology will help us provide a platform that improves the water infrastructure used by AlixLabs and other advanced semiconductor players. With this project, we get to benchmark our NPW on 300-millimeter wafers as well as have the wafers cleaned with NPW by Fraunhofer IPMS."

➤ Experts from DIVE and Fraunhofer IPMS in the cleanroom at Fraunhofer IPMS in Dresden. © Fraunhofer IPMS.

Through this partnership, AlixLabs and NSS Water are combining their respective strengths in innovative water treatment, advanced analytics, and semiconductor manufacturing know-how to develop solutions that significantly reduce water usage, lower operational costs, and bolster sustainability. Fraunhofer IPMS's involvement ensures precise contamination and defect control, further enhancing the effectiveness of the recycling and purification processes. Co-financed by the European Nanoelectronics Access program ASCENT+, which provides a direct gateway to Europe's global-scale Nanoelectronics Research Infrastructure, granting researchers, SMEs, and PhD candidates access to state-of-the-art capabilities. The project is an important step in positioning AlixLabs, NSS Water and the European Union at the forefront of sustainable semiconductor manufacturing innovations.

ARM PURIFICATION
BY APPLIED ENERGY SYSTEMS

Empower Your Purity

Proven Gas Purifiers That Enable Total Process Excellence

ARM Purification's purifier solutions are equipped for the precise purification of gases and uphold the most stringent application requirements across industries. **Discover why we're trusted by the world's innovators to meet today's mission-critical gas purity demands.**

Our Complete Purifier Solutions:

Point-of-Use Purifiers

Frame-Mounted Purifiers

Bulk Purifiers

Nova™ Series In-Line Gas Purifier

BROUGHT TO YOU BY APPLIED ENERGY SYSTEMS

Explore our Gas Purification Solutions

SCREEN

Wafer Cleaning System

No.1 Global Share

* Based on SCREEN in-house research

Wet Station | Spin Scrubber | Single Wafer Cleaner

15,000+

units shipped

SCREEN Semiconductor Solutions Co., Ltd.

SEMICON® WEST October 7-9, 2025 SCREEN Booth #6545

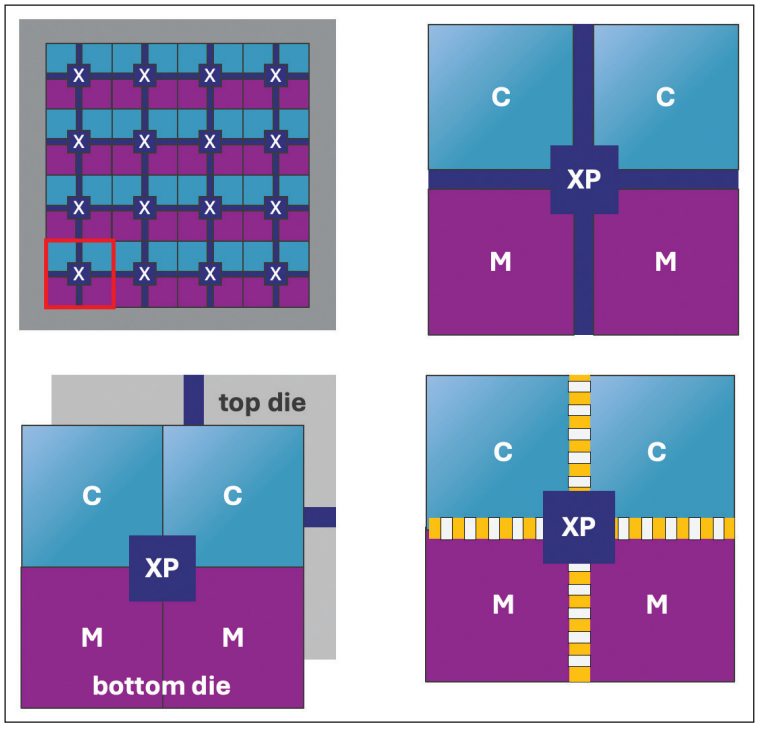
Innovative approaches to scaling network-on-chip architectures

The evolution of cloud computing has sparked a pressing need for advanced solutions that maximize computational efficiency while minimizing physical and energy constraints. Modern data centers depend heavily on multi-core processors, often packing over 100 cores into a single chip.

BY MORITZ BRUNION, RESEARCHER DESIGN-TECHNOLOGY CO-OPTIMIZATION AND JAMES MYERS, PROGRAM DIRECTOR SYSTEM TECHNOLOGY CO-OPTIMIZATION, BOTH AT IMEC.

THESE PROCESSORS are designed to handle the growing demands of cloud-based applications by sharing network, memory, and storage resources, transforming each core into a rentable unit of processing power.

However, as processors grow more powerful, the network-on-chip (NoC) has emerged as a critical bottleneck in scaling. The NoC, tasked with routing data among CPU cores and memory, relies on metal interconnects that present unique challenges when scaled down. Higher resistance in these interconnects increases power consumption and necessitates additional signal repeaters to maintain performance over long distances.



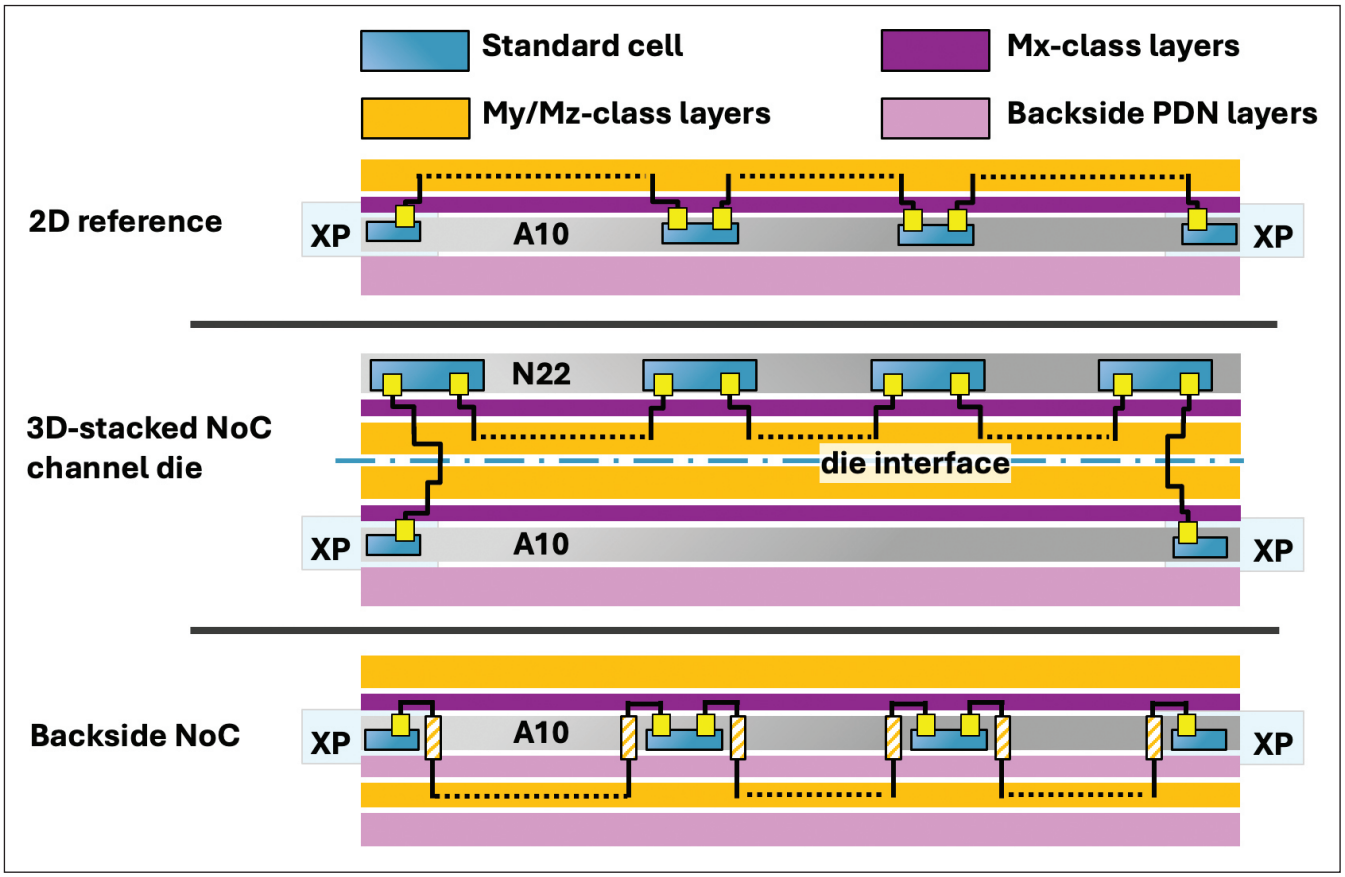
➤ Figure 1. 2D reference system (top left) and tile (top right) with NoC channel routes and logic within a single FEOL and BEOL stack. In the bottom are the two new approaches depicted: (left) 3D stacking design, showing the separation of NoC channel routes into a dedicated routing die bonded to the A10 logic die, and (right) the backside integration approach, showing NoC channel routes integrated into the backside metal layers of the BSPDN.

Adding to this, the increasing core count and HD logic scaling, while maintaining the same NoC dimensions, drive a significant rise in NoC area. These factors add complexity and compromises the goal of achieving smaller and more efficient designs.

Addressing these challenges has led to a variety of innovative solutions, though none without trade-offs. 2D mesh topologies, while straightforward and scalable, struggle with communication latency as the number of cores increases.

Other approaches, such as routerless configurations or workload-specific optimizations, can improve performance but are often impractical for general-purpose systems like those used in cloud computing. While scaling the NoC link throughput by an increase in the number of signals per channel can increase the throughput, it often results in higher costs and resource demands, further complicating the NoC landscape.

In response to these constraints, imec researchers have pioneered two transformative approaches: relocating NoC channels to a dedicated die and integrating them with the backside power delivery network (BSPDN). These strategies, guided by system-technology co-optimization (STCO) principles, aim to overcome scaling limitations while balancing cost and performance. Of these, the co-integration of NoC channels with the BSPDN offers particularly promising results for future design of such high core-count systems.



➤ Figure 2. (Top) The technology stack cross-section for the 2D reference shows both NoC channels and crosspoints (XP) in the A10 logic frontend. (Middle) The NoC routing is entirely offloaded to a dedicated die freeing up placement and routing resources on the main logic die. In this case, channels in the separate die are manufactured in older technology while the crosspoints reside in the A10 logic. (Bottom) The NoC channels sharing routing resources with the power delivery network and repeaters located on the logic die front-end. NoC buffer islands occupy 1-2% of a high-performance CPU core (compared to up to 10% of the silicon area being dedicated to the NoC in the 2D reference), with the addition of two dedicated backside metal layers for NoC channels.

Dedicated NoC routing on a separate die

One novel approach proposed by imec involves offloading the NoC channel routes to a dedicated die, independent of the main logic layers. Using wafer-to-wafer face-to-face hybrid bonding, this architecture can leverage the high-bandwidth data transfer in the vertical direction with minimal energy usage per bit. The NoC die can be fabricated using a less advanced manufacturing process, such as N22, significantly reducing production costs.

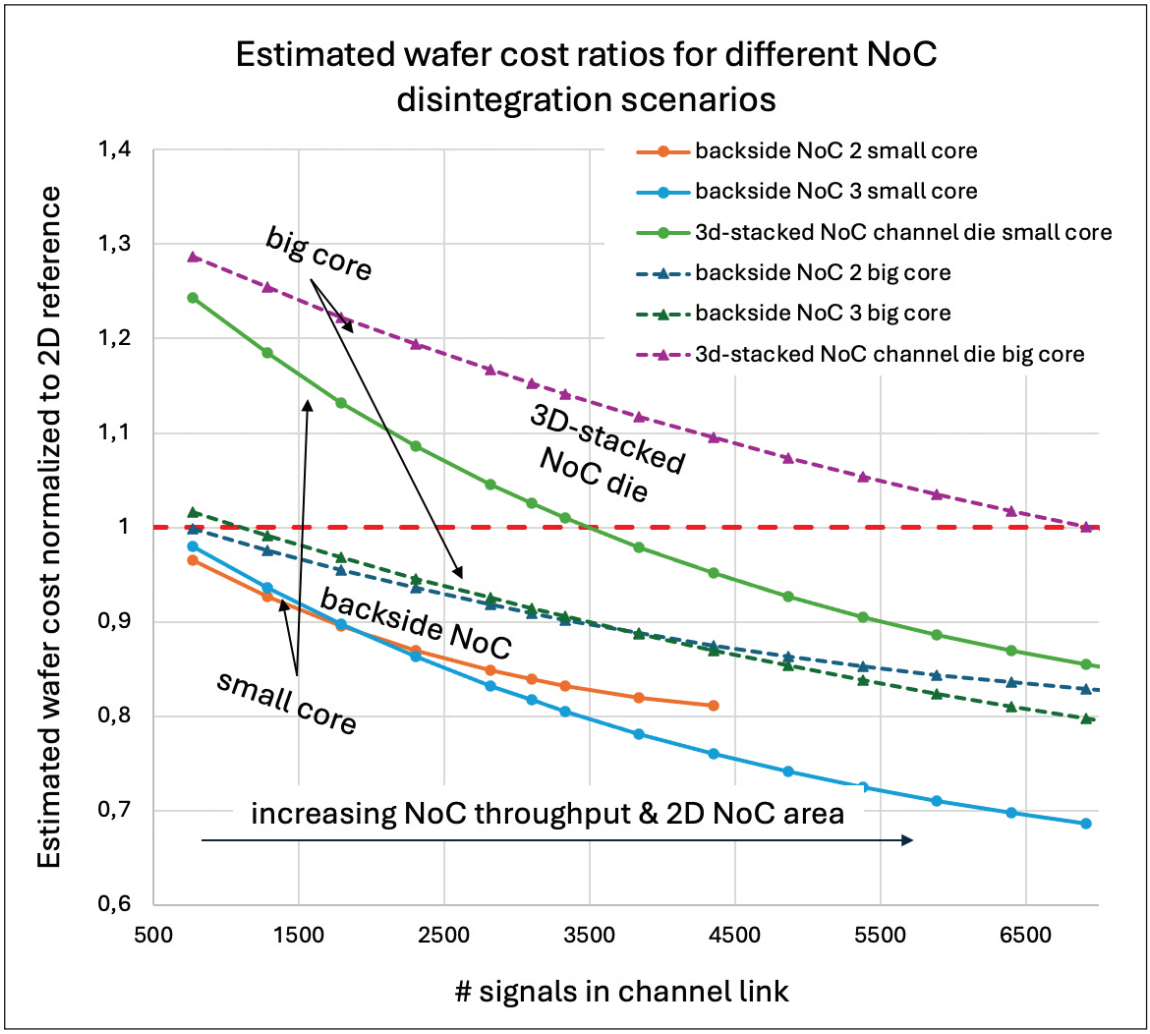
This design also simplifies the back-end-of-line (BEOL) configuration by using fewer metal layers, thereby optimizing functional integration efficiency. The NoC routers, which make real-time routing decisions, remain on the main logic die, ensuring that latency is kept to a minimum.

This design, however, is not without its challenges. Power distribution becomes more complicated, as the additional die requires its own power infrastructure. Physical design experiments also revealed an 8% increase in propagation delay and a 15% rise in energy per bit transferred across a channel link compared to conventional 2D NoC systems.

Backside integration with the BSPDN

A second solution involves co-integrating NoC channels with the BSPDN on the backside of the wafer. The BSPDN's existing metal layers, optimized for power delivery with wider pitches and lower resistance, provide an ideal foundation for routing NoC channels over long distances at high clock speeds. This integration takes advantage of the relaxed design constraints of backside interconnects to achieve efficient signal transmission.

To implement this approach, the researchers made several design adjustments. First, they devised a bidirectional wiring scheme, enabling both horizontal and vertical NoC channels to share the same metal layer. This reduces the total number of required layers, lowering both costs and the overall chip footprint. Second, since BSPDN currently doesn't support active devices on the backside, signal repeaters were placed as compact "islands"



➤ Figure 3. Estimated wafer cost ratios of different NoC integration schemes, normalized to the 2D baseline. As the width of the NoC channel increases, the cost advantage of backside integration becomes more evident.

on the main logic die. These repeaters ensure robust signal strength at a small area overhead, while freeing up the channel routing footprint in the main logic die for other logic components. Finally, integrating NoC channels with the BSPDN required addressing the shared routing resources between data and power delivery, which increases the risk of IR drop and can affect performance. To mitigate these challenges, the researchers traded-off the PDN pitches and IR drop against the area overhead of the repeater islands, maintaining the benefits of the BSPDN and ensuring stable voltage levels, while also supporting reliable data transmission across the NoC.

Cost-benefit analysis favours NoC backside integration

When comparing the two approaches, not only their technical trade-offs but also cost-effectiveness is important to identify the best solution for growing demands. The dedicated die method offers greater flexibility and customization options but incurs higher manufacturing costs due to the need for an additional fully processed wafer. By contrast, integrating NoC channels with the BSPDN reuses existing infrastructure, adding only a few extra metal layers. This significantly reduces costs and optimizes the use of front-side silicon, making it an attractive option for applications requiring high core densities, such as cloud server CPUs.

Backside integration also excels in scalability. As core counts per processor continue to rise, the demand for wider NoC channels increases. By leveraging the backside metal layers, this approach minimizes congestion and enables higher data throughput without substantially increasing the silicon footprint. These attributes make it a compelling solution for next-generation chip architectures.

To mitigate these challenges, the researchers traded-off the PDN pitches and IR drop against the area overhead of the repeater islands, maintaining the benefits of the BSPDN and ensuring stable voltage levels

Broader implications and future directions

While backside NoC integration is highly applicable for cloud server CPUs, its relevance to other applications, such as GPUs and accelerators with coarse-grained, regular topologies, is still being explored. However, widespread adoption of this technology depends on advancements in Electronic Design Automation (EDA) tools. Currently, implementing backside NoC channels requires specialized workflows, which can be labor-intensive and costly. As EDA tools evolve, they are expected to streamline the design process, making backside integration more accessible and practical for a variety of use cases.

In conclusion, the integration of NoC channels with the BSPDN represents a significant breakthrough in chip design. By addressing routing and power delivery challenges simultaneously, this approach exemplifies the power of STCO principles. As the demand for scalable, high-performance architectures continues to grow, innovations like backside NoC integration will play a pivotal role in shaping the future of semiconductor technology and driving the next wave of computational advancements.

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James Myers
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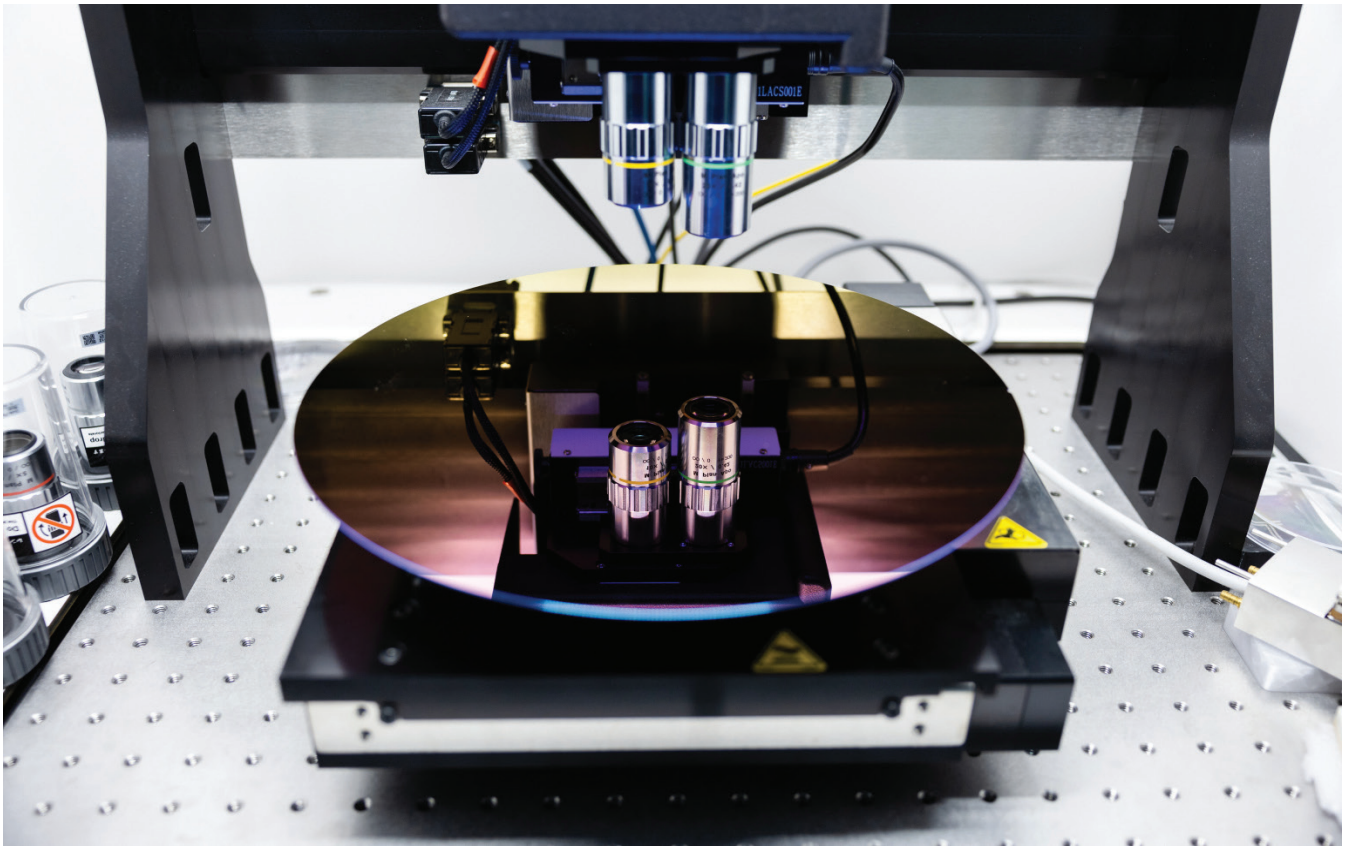
James Myers holds a MEng degree in Electrical and Electronic Engineering from Imperial College in London. He spent 15 years at Arm, leading research from low power circuits and systems, through printed electronics, to DTCO activities. He joined imec in 2022 to lead the System Technology Co-optimisation program, with the aim of building upon established DTCO practices to overcome the numerous scaling challenges foreseen for future systems. James holds 60 US patents, has taped out 20 SoCs, has presented at ISSCC and VLSI Symposium, and has published in IEDM and Nature.



Thin film thermal metrology and its implications for electronic devices

How a new technology addresses the limitations of traditional measurement methods.

BY LASER THERMAL

SEMICONDUCTOR MANUFACTURING is an industry defined by ever-increasing demand and a constant quest for higher yield and throughput, and more fine-tuned testing processes play an important role in improving the yield and efficiency of the manufacturing process. The earlier and more precisely that defective chips or sub-standard materials can be identified, the more time and money can be saved. Once identified, defective chips can be excluded from subsequent processing that costs equipment capacity, money, and labor time. The key is identifying these defective materials, processes, and chips as early and as far upstream in the manufacturing process as possible.

In this context, our experience suggests that enhanced thermal testing capabilities for the thin film materials used in many semiconductor devices represent a valuable avenue for improvement. Furthermore, accurately measuring the thermal properties of thin films is essential for eliminating deleterious temperature rises, understanding operating limits, and designing cooling systems capable of maintaining performance while avoiding both thermal failure and costly over-specification. Understanding the thermal properties of thin film materials is crucial to maximizing performance, reliability, and manufacturing yield.

Accurately measuring the thermal properties of nanoscale thin films, however, is a substantial metrology challenge. Due to demands on throughput, a thermal resistance measurement technique must be amenable to rapid material screening along with integration into semiconductor manufacturing cycles to achieve maximal impact.

However, most traditional thermal testing methodologies cannot dependably provide exact measurements of thermal resistances on the length scales needed for semiconductor chips, nor meet the integration and throughput constraints necessary for integration into the semiconductor testing market.

In this article, we explore how a new optical measurement technique (Steady-State Thermoreflectance in Fiber Optics) can directly address the limitations of traditional thin film thermal measurement techniques.

Limitations of Traditional Thin Film Thermal Metrology Methods

Sustained thermal stress can drive a variety of different failure modes in thin film materials, which must be carefully engineered to operate within specified thermal limitations. To limit failures and accurately assess the reliability of components, semiconductor manufacturers institute rigorous procedures to test for thermal resistances. Potential modes of failure include:

- Oxide-layer faults
- Metallization defects
- Die-substrate attachment issues
- Seal failures
- Different materials with mismatched thermal expansion coefficients
- Packaging defects

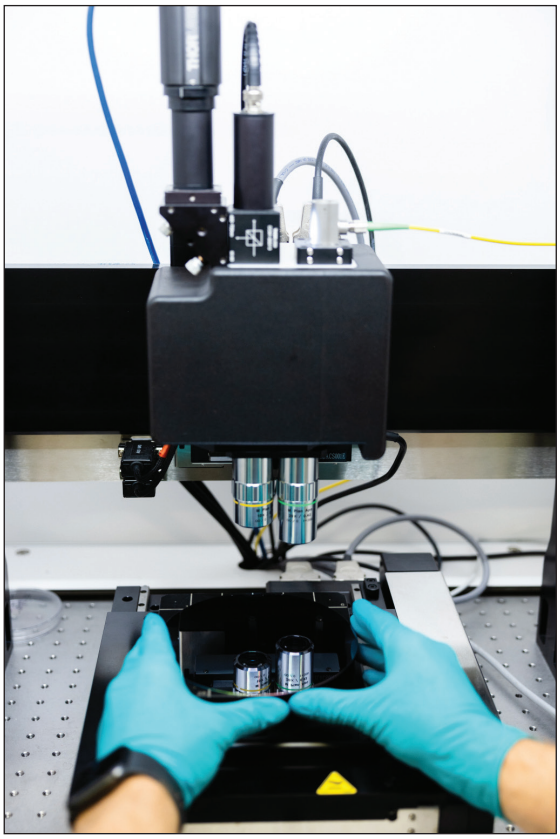
While stress screening can help establish operating limits and filter out defective devices, it does not generate precise data on how a component can dissipate heat from electrical loads. Doing so requires measuring crucial properties such as thermal resistances, but measuring these properties in the nanoscale thin films used in semiconductor devices is a substantial metrology challenge requiring specialized equipment.

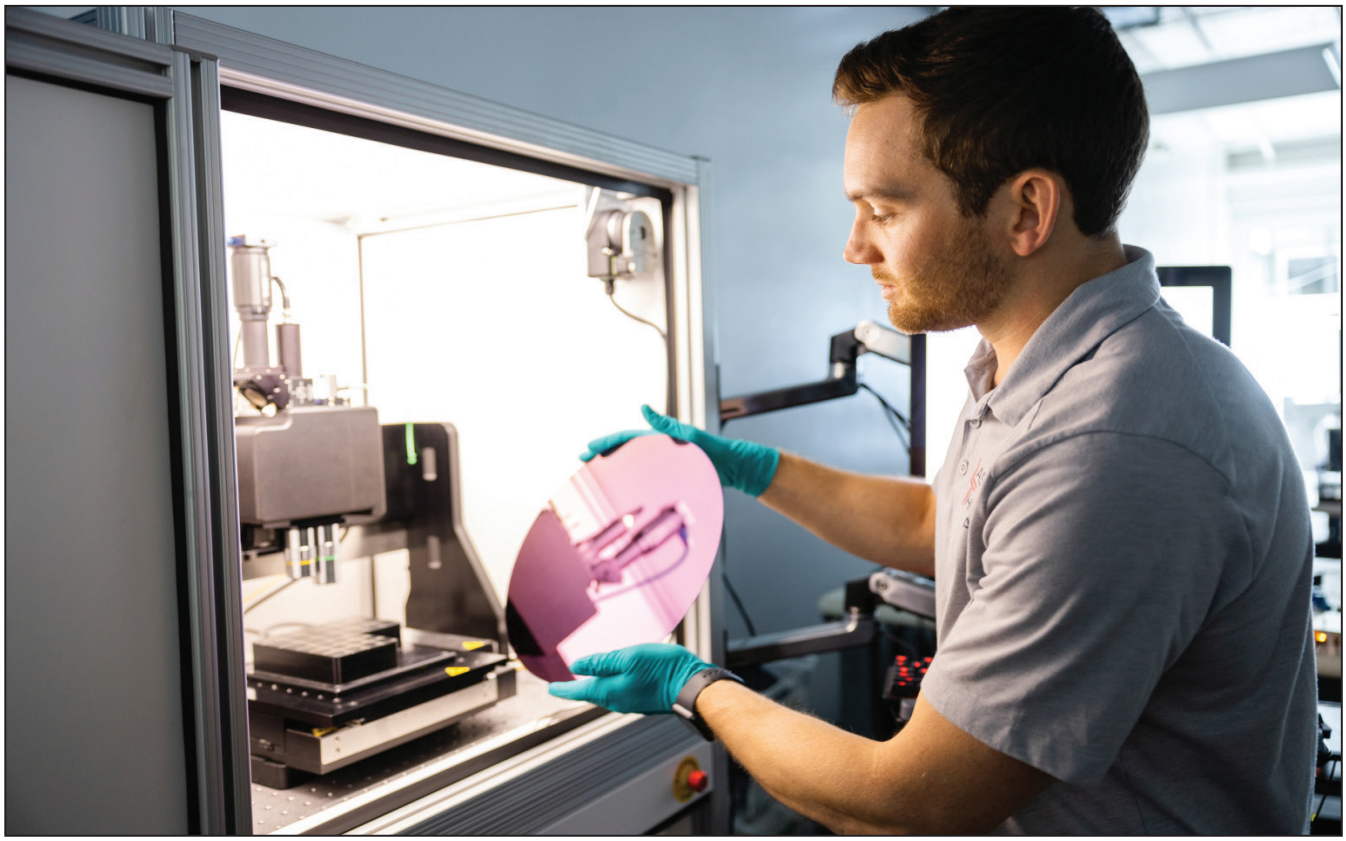
Ranging from several micrometers to less than a single nanometer in thickness, thin films create unique challenges for measuring basic thermal properties like thermal conductivity. In short, these materials are simply too thin to rely on traditional thermal measurement techniques. To make matters even worse, the thermal conductivity of thin films is strongly dependent on the film thickness and processing conditions, meaning one cannot simply "look up" the thermal conductivity of thin films in the back of a textbook. In thin films, defects and interfaces may arise during growth and heterogeneous integration that change the electron and phonon scattering events, resulting in drastically lower thermal conductivities in materials relative to their bulk counterparts. Therefore, to truly understand the thermal conductivity of a thin film in a device, one must measure the thermal conductivity of a film of the same thickness, grown under the same conditions.

In most traditional applications, sensors such as thermocouples or resistive thermometers can be used to capture measurements of the temperature gradients or changing heat flux that result as heat is applied to a material (measurements which can be directly related to thermal conductivity via Fourier's law or the heat equation). Thin film materials, however, are often substantially thinner than the dimensions of the heaters and sensors used to induce the temperature gradients and capture temperature changes, respectively. This fact renders these measurement platforms unsuitable for these applications. Furthermore, the physical testing probes used in traditional measurement techniques are not amenable to the high-throughput screening techniques necessary in today's semiconductor fabrication facilities.

> Accurately measuring the thermal properties of nanoscale thin films, however, is a substantial metrology challenge. Due to demands on throughput, a thermal resistance measurement technique must be amenable to rapid material screening along with integration into semiconductor manufacturing cycles to achieve maximal impact

For example, the material in the thermal sensor itself will contribute more to the recorded thermal resistances and temperature changes than the thin film of interest! The accurate measurement of thermal resistance and thermal conductivity of thin films requires a different approach to thermal metrology, which must achieve the substantially higher temporal/spatial resolutions demanded by these nano-meter scale materials.





With substantial margins for error on traditional thin film thermal resistance measurements, semiconductor manufacturers have traditionally resorted to derating (operating a device at less than its maximum rated power dissipation) to establish an additional margin of safety. Consequently, more accurate, precise thermal resistance measurements can directly enable semiconductor device designs that are higher performing, reliable, and more predictable.

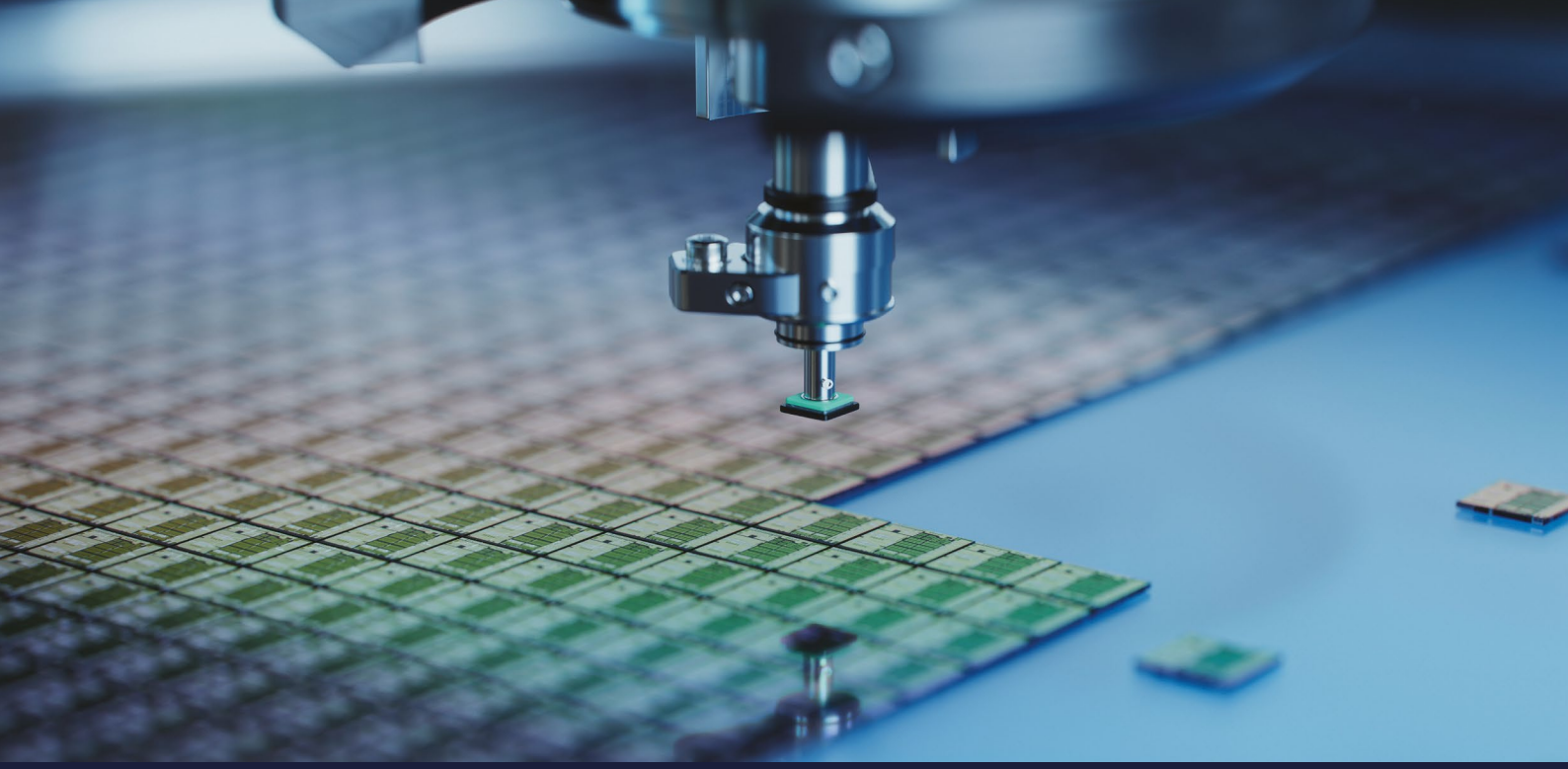
Steady-state thermoreflectance in fiber optics: A novel approach to measuring thermal properties of thin films

Optical measurement techniques can directly address these key limitations of traditional thin film thermal metrology techniques. For example, Laser Thermal's products and testing services are anchored in Steady-State Thermoreflectance in Fiber Optics (SSTR-F), a non-contact, laser-based pump-probe technique.

This approach works by utilizing a laser to create a nano-to-microscale heating event on the surface of a sample, resulting in a steady-state temperature gradient in the sample. A secondary probe laser is then used to measure the temperature on the surface of the sample, which is altered by incrementally increasing pump powers to induce incremental temperature rises. The spot laser used in this process can be tuned to be as small as a few microns 1/e2 diameter, which, given the nanoscale localized absorption of the laser, enables SSTR-F to be used effectively to measure in-plane and through-plane (cross-plane) thermal resistances and thermal conductivities– even for nanometer-scale thin films and atomically thin interfaces. Defects, stresses, compositional differences, and changes in density and microstructure that occur during film growth and alter the subsequent thermal properties can be easily and rapidly identified via SSTR-F.

SSTR-F can provide accurate, repeatable (+/- 1.0 %) and reproducible (+/- 2.0 %) thermal conductivity measurements. This approach is also capable of fully automated, high-throughput measurements, which are crucial for the large volumes of testing required by the ever-growing semiconductor industry. Our automated, high throughput, turnkey implementation of SSTR-F can measure the thermal conductivity of materials with values ranging from 0.05 to 3,000 W/m/K. And high-throughput SSTR-F testing of multiple samples facilitates, for example, screening the thermal conductivity of different thin films processed under different conditions. Thermal mapping of planar devices can be performed to look at the spatially varying thermal resistance of chip level structures.

Looking forward, we expect that enhanced thermal metrology capabilities will only become more critical for semiconductor manufacturers. As System-on-Chip's become more tightly integrated and less repairable, pressure will only mount to improve reliability wherever possible. To keep up with global demand, new measurement techniques must be amenable to automated, high-throughput manufacturing operations. SSTR-F is strongly suited to this challenge, and plays a valuable role in helping semiconductor manufacturers continue to push engineering boundaries.



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The geopolitics of the semiconductor industry: navigating a global power struggle

Nations are racing to control the semiconductor technologies that power everything from consumer gadgets to defence systems. With supply chain issues, national security concerns, and economic goals all at play, the competition to lead this sector has never been more intense.

BY DUNSTAN POWER, DIRECTOR OF EMBEDDED DESIGN CONSULTANCY BYTESNAP DESIGN

HERE we explore the dynamics shaping the semiconductor industry, from the intensifying US-China rivalry and Taiwan's pivotal role to the global push for supply chain resilience, the rise of AI and EVs, and the challenges faced by regions like Europe and India in carving out a foothold in the sector.

US-China tensions and the semiconductor race

At the centre of semiconductor geopolitics lies the rivalry between the United States and China. While Washington seeks to maintain its technical and economic dominance, Beijing is rapidly growing its semiconductor capabilities. Allegations of intellectual property theft and questionable practices are further fuelling tensions.

While US sanctions, which block China's access to advanced manufacturing equipment, have slowed its progress, they have not dented its long-term goal of becoming a global leader in chip production.

Despite its efforts, China remains 5–10 years behind in the most advanced semiconductor technologies. The gap between its global market share in semiconductor equipment supply (3.2%) and its share of demand (34.4%) further underscores the significant challenge it faces in achieving self-sufficiency.

To counter China's semiconductor ambitions, the US enacted the CHIPS Act, a key initiative aimed at boosting domestic production and restricting China's access to advanced manufacturing equipment.

However, the future of the legislation is uncertain following President Donald Trump's sharp criticism during his campaign, which has raised doubts about the continuity of projects funded by the Act. This includes a £6.29 billion grant finalised by the Biden administration for Intel's semiconductor plant in Ohio, which some GOP lawmakers are keen to protect despite broader Republican support for cost-cutting measures.

Taiwan plays a pivotal role in the semiconductor industry, with TSMC producing over 50% of the world's chips. This dominance has raised concerns from governments and businesses like Apple about geopolitical risks from potential conflict with China. In response, TSMC is diversifying its operations by constructing new fabs in Arizona and Japan, though these facilities will contribute only about 10% of its total silicon output. Despite these initiatives, the majority of production will remain in Taiwan, highlighting the challenges of reducing reliance on a single region – a process that will take years to fully materialise.

The Netherlands has also been drawn into this geopolitical struggle, with its leading lithography equipment company, ASML, facing pressure to limit exports to China. These lithography machines, especially those using extreme ultraviolet (EUV) technology, are critical to advanced chip production and represent a linchpin in the semiconductor ecosystem. Although the Dutch government has taken steps to align with US sanctions, questions remain about the extent of its compliance.

Supply chain challenges and the road to recovery
The COVID-19 pandemic laid bare the fragility of global semiconductor supply chains. A surge in demand for electronics and automotive components created an acute shortage, with lead times stretching beyond a year. During this crisis, China absorbed a significant share of global demand. However, as the pandemic's supply chain pressures eased in early 2023, the industry faced a new problem: overproduction and excess inventories. Companies, having overordered during the crisis, found themselves saddled with surplus chips, dampening innovation and creating market instability.

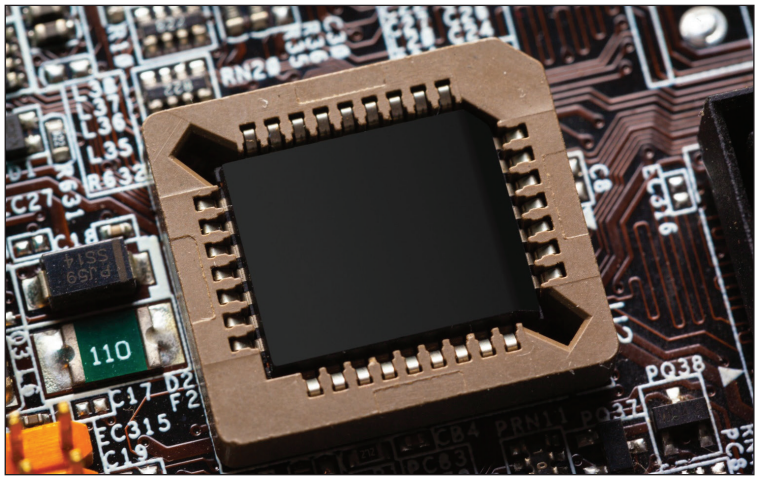
Despite the challenges, the semiconductor industry is rebounding, largely driven by the surging demand for artificial intelligence (AI) applications. AI-specific chips, such as those produced by Nvidia, have experienced explosive growth, marking a significant shift in market priorities. The AI chip market, valued at £49.1 billion in 2023, is projected to grow at a compound annual rate of 29.4%, reaching £496.9 billion by 2032.

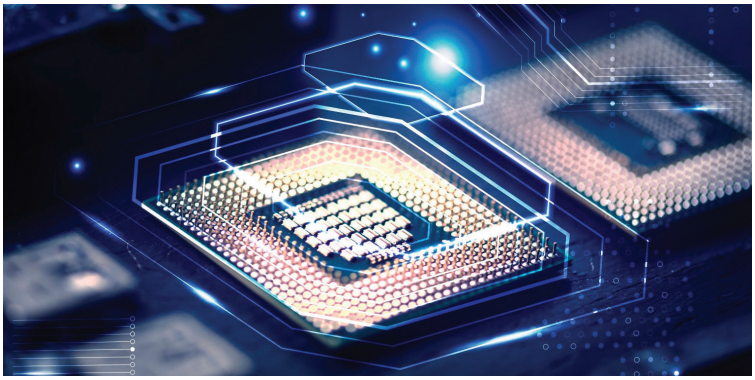
Another key driver is the rising integration of semiconductors in electric vehicles (EVs). Globally, 15.2 million EVs were sold in 2024, reflecting a 25% year-to-date increase, according to Rho Motion. China leads the charge, setting a record with 1.3 million units sold in November 2024 alone, almost entirely from battery electric vehicles (BEVs). Brands like Geely, Tesla, and Changan were among the top sellers, further cementing China's dominance in the EV market. China's high EV sales have profound geopolitical implications for the semiconductor industry, as EVs rely heavily on advanced chips for critical systems. By leading global EV adoption, China is solidifying its influence in the semiconductor sector, even as it remains dependent on foreign technology. This dynamic heightens competition with the US and Europe, driving their efforts to secure supply chains and reduce reliance on Taiwan for chips and China for EV technologies. At the same time, China's integration of domestic semiconductor development into its booming EV industry strengthens its position in the global tech race, making semiconductors a focal point of both economic strategy and geopolitical power conflicts.

Europe's struggles in the semiconductor landscape
Europe, while home to significant players like NXP and STMicroelectronics, has long been overshadowed by its US and Asian counterparts. The region faces several challenges, including a lack of large-scale investment and a struggling automotive sector. Germany, the largest electronics market in Europe, exemplifies these difficulties, with its car manufacturers grappling with the transition to EVs. Meanwhile, China is taking the lead in EV technology, putting further pressure on Europe's traditional industries.

In response, the European Union has pledged billions in subsidies to bolster its semiconductor sector. For instance, Germany recently announced a €2 billion investment aimed at strengthening chip manufacturing. While this is a step in the right direction, the scale of investment pales in comparison to the costs of building state-of-the-art fabs. There is, however, a need for greater financial commitments to reduce reliance on non-European manufacturers and foster more innovation. Europe's progress is, however, hampered by bureaucratic red tape and political vacillation.

Unlike the US, which has adopted a more aggressive approach to reshoring manufacturing, Europe appears to be on the sidelines of this global competition. The UK, in particular, has little influence, with limited government investment and a reliance on allies for strategic direction. Efforts to block Chinese acquisitions, such as the attempted purchase of a fab in Wales, highlight the UK's defensive posture but do little to address its lack of domestic manufacturing capability.





Global trends reshaping the semiconductor industry
The semiconductor industry is navigating a critical period of transformation. Diversification of manufacturing, while necessary to mitigate risks tied to Taiwan's dominance, highlights the sheer complexity and cost of redistributing global supply chains. The strategic investments in fabs across the US, Japan, and Europe signal progress, but achieving meaningful independence will require years of sustained effort and collaboration.

AI and electric vehicles are reshaping semiconductor design and production, driving demand for specialised chips that power these transformative technologies. This shift creates opportunities for regions like India, with its £12 billion investment in chip-packaging plants and its first modern chip fab, and Europe to carve out niches. However, realising this potential will also require solutions to critical talent shortages. The expertise required for semiconductor design and manufacturing is concentrated in regions like Taiwan and South Korea, where decades of focused development have cultivated a highly skilled workforce. New entrants to the industry, such as India, face significant challenges in building this specialised talent pool, with red tape and bureaucratic hurdles adding further delays. Even with AI assisting in aspects of chip design, the deep, specialised knowledge needed for tasks such as coding, placement, and fabrication remains irreplaceable by automation.

At the heart of these trends is a renewed emphasis on resilience. Nations and corporations are beginning to view semiconductors as strategic assets, integral to both economic stability and national security. This recalibration is fostering an ecosystem where long-term innovation and cross-border collaboration may ultimately outweigh competition. If governments and industries align their priorities effectively, the semiconductor sector could emerge not only stronger but also more decentralised and inclusive, offering a more secure foundation for future technological growth.

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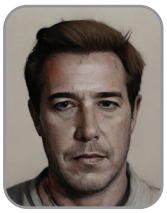
Today's fabs are highly complex environments that demand precision, reliability, and real-time adaptability. Industry success will depend on a stable workforce with specialised skills, a keen eye on processes and efficiencies, and a commitment to embracing innovative facility management partners and solutions.

BY JOSEPH CESTARI, VICE PRESIDENT, SEMICONDUCTOR OPERATIONS AND NEHA DHINGRA, VICE PRESIDENT, SEMICONDUCTOR STRATEGY AT ABM



THE U.S. domestic semiconductor manufacturing is fueled by record-high investment and federal incentives like the CHIPS and Science Act. The manufacturing capacity is poised for a massive expansion in the United States.

According to the Semiconductor Industry Association (SIA), U.S. fab capacity will triple its domestic semiconductor manufacturing capacity in the next decade.

Nonetheless, this manufacturing resurgence faces some significant obstacles. Many facilities need to be built from the ground up, which requires highly specialized skills and training – from pipe fitters to plumbers, electricians, and welders all the way to equipment installation as well as operation and maintenance.

Once up-and-running, keeping these fabs operating at peak efficiency while meeting stringent quality, safety, and environmental standards brings a unique set of challenges. Managing them is a monumental task due to the complexity of the processes, the precision required, and the scale of operations involved. As processes continue to advance (toward 3nm, 2nm nodes), the margin for error drops even further. Tiny deviations in temperature, pressure, or chemical composition during manufacturing can lead to systemic failures, especially with cutting-

edge technology like Extreme Ultraviolet (EUV) lithography.

These complex facilities require highly specialized cleaning and facility management solutions, a push toward more digitization, and sustained investment in workforce development.

Impact of facility downtime

Semiconductor facility outages can stem from a myriad of issues from power disruptions, equipment failures, human error and — as evidenced during the pandemic – supply chain shortages.

An unplanned outage lasting 4 hours in a leading-edge fab could cost anywhere from $833,000 to $3.3 million (a massive $3,472 per minute). This means a full day could range from an astounding $5 million to $20 million. Smaller or older facilities producing less advanced chips might see lower costs but can still reach upwards of $500,000 to $2 million per day.

While the actual cost may fluctuate based on the facility's output value and product type, one thing is certain. Any downtown is unquestionably costly. To further complicate matters, finished products can also fail after shipment due to contamination or inconsistent processing leading to costly recalls or even injury to consumer leading to huge fines and penalties, forced work stoppages, lost profit from returned goods, or costly lawsuits.

The clean continuum

Cleanrooms must have one consistent goal – keep contaminants out and remove what's generated inside. This requires a "clean continuum" of establishing, certifying and sustaining the necessary environment. This meticulous process – leverages a combination of competencies of specialized controlled environment cleaning as well as particulate measurement, air flow test and balance, and compliance certification to standards.

A breached filter, a leak in a material supply line, or a careless tech can lead to contamination and yield loss. And a single particle significantly smaller than a micron (one-hundredth the width of a human hair) can ruin an entire wafer.

ISO standards provide the framework necessary to maintain these sterile conditions, defining acceptable particle levels in the air and establishing guidelines. Contamination control from Class 1 to 10,000 scales with particle limits, airflow rigor, and procedural stringency. The primary contaminants are airborne contaminants (dust, microbes, aerosols) introduced by personnel, equipment, materials, or processes. Each step up in cleanliness amplifies the challenge and the stakes.

Managing particular problems

Air pollution, dirt and dust, ferrous metal particles, human hair, skin particles — just to name a few — all must be kept at bay. It's also important to remember that all operations and systems are interconnected and affect each other. Particulates in HVAC systems can increase cooling energy costs. Airborne gases can lead to corrosion and failures. Particles and build up can interfere with critical equipment and cause failures.

Contamination from humans such as skin flakes, hair, and breath can be a major source. A single uncovered cough in Class 1 can undo hours of filtration.

The good news is this type of contamination is mitigated with upgraded contamination and control procedures including entry, gowning and air showers. Strict SOPs must be adhered to within the overall clean environments – encompassing both routine cleaning along with "after action cleaning" such as tool installation or servicing.

Air filtration, flow and exhaust are also critical within these complex environments. A rigorous preventative maintenance schedule is essential to maintain the necessary unidirectional flow critical for Class 1-100.

Digitisation of facility management

Digitising facility services involves leveraging advanced technologies to optimize operations, enhance efficiency, and ensure the stringent conditions required for semiconductor manufacturing are consistently met. It can transform facility services in key areas such as automation, data integration, and environmental control.

Semiconductor fabs generate massive amounts of data from equipment, environmental controls, and production processes. Digitizing facility services means harnessing this data for actionable insights. A data intelligence platform, such as ABM Connect™, can streamline and display analytics tailored for immediate answers to questions. With an integrated

IoT hub for visibility and task validation, examples of front-line team data can include:

- Work completion against planned routes
- Quality performance & inspections
- Recognition patterns & performance trends
- Training compliance
- Safe workplace observations

This technology allows greater accuracy and efficiency with real real-time actionable metrics, robust reporting, and up-to-date KPIs.

In highly regulated industries like semiconductor manufacturing, the solution can help meet compliance and audit challenges, while enabling continuous improvement.

Incorporating predictive maintenance

As innovation on the fab floor increases, tech-based solutions can be applied to equipment maintenance. Predictive maintenance (PdM) offers the promise of transforming semiconductor fabs by shifting from reactive or scheduled maintenance to a data-driven, just-in-time approach.

Highly specialized, expensive tools like photolithography machines, etchers, and deposition systems are prone to breakdowns. A laser misfire in an EUV system or a vacuum pump failure can stop a line. Leveraging a PdM model can minimise disruptions and extend the life of equipment. It's basically the difference between changing a specific part on a sensible schedule and knowing when it is optimal for operations and lifecycle costs.

Real-time monitoring can be achieved with connected sensors. Wireless and wired sensors (along with AI) can monitor for conditions and report to a centralized information system. These types of sensors can be used to monitor key assets such as:

- **Heat Monitoring -** Detects heat caused by insulation issues or conduction problem so you can act before discharge events or arc faults.
- **Partial Discharge Monitoring -** Partial discharge usually isn't visible, but it destroys insulation over time, which will cause a full and destructive discharge.
- **Circuit Monitoring -** Measures power and power quality data, including harmonic disturbance in the wave forms and voltage transients (sags and swells) that can damage to sensitive equipment.

This data is then analyzed using AI and machine learning algorithms to detect patterns or anomalies that signal impending failures. For example, a spike in vibration levels in a pump could indicate wear and prompt preemptive action. Recording this type of data over time gives you the ability to identify asset anomalies and provide advance warnings of equipment failures before they occur. Where just-in-time maintenance strategies have been implemented, the result typically is higher overall equipment efficiency. According to Nucleus Research, PdM initiatives can reduce downtime by between 35 and 50 percent, extend asset lifespan by between 20 and 40 percent, lower costs, improve safety, and enhance product quality.

Yet, effective implementation is not without challenges. Success relies on high-quality, accessible data, and integration with existing systems. It is also critical to define the right parameters for failure prediction models. And as with any connected system, robust security measures are needed to protect sensitive production data. However new solutions are making the process easier and scalable across facilities. An experienced team with the right skillset can help implement PdM to enhance efficiency, reduce costs, and maintain product quality.

Power resilience

Semiconductor fabs are energy-intensive, consuming vast amounts of electricity and water for cooling, processing, and cleanroom operations. They also demand uninterrupted, ultra-stable electricity – with 24/7 uptime with zero flicker. Even a millisecond-long outage can disrupt processes like etching or doping, ruining wafers mid-process.

Yet, the U.S. electric grid is under strain. Projections indicate that the demand for electricity will surge by 50% during the next two decades, with no signs of slowing down. According to Grid Strategies, the U.S. electric grid is not prepared for this level of significant load growth. This poses a key risk for reliability, and could have detrimental effects on fabs, particularly in more drought prone or high-cost areas.

On the bright side, new methods of energy management are now available to increase energy reliability and resiliency. Localized power grids (or microgrids) can provide a decentralized approach to energy distribution to bolster on-site energy capacity, avoid high-cost, peak timeframes, and ensure power resiliency.

In the simplest terms, a microgrid is a local collection of distributed energy resources that also can interact with the broader electrical grid to provide peak load shaving and system resiliency. This autonomy enhances resilience, energy security, and efficiency. Thanks to increased affordability and shifting regulations, more of these microgrids are being powered by renewable energy methods. What makes a microgrid "intelligent" is the set of control systems that can manage, store, charge, and discharge the entire system at any given time. These controls can be programmed to monitor the supply versus demand of power being pulled from the central grid and the real-time cost of power on the market.

While monitoring, if the control system detects low energy prices, it can switch to purchasing power from the grid to supplement the consumer's needs while using battery systems to store self-generated power from solar panels for future use. Subsequently, the controller can discharge these batteries when prices increase, ensuring more stable energy costs. The system can also operate autonomously, ensuring an uninterrupted power supply even during grid outages or disruptions. This level of real-time energy management improves the energy performance, control costs and increases predictability.

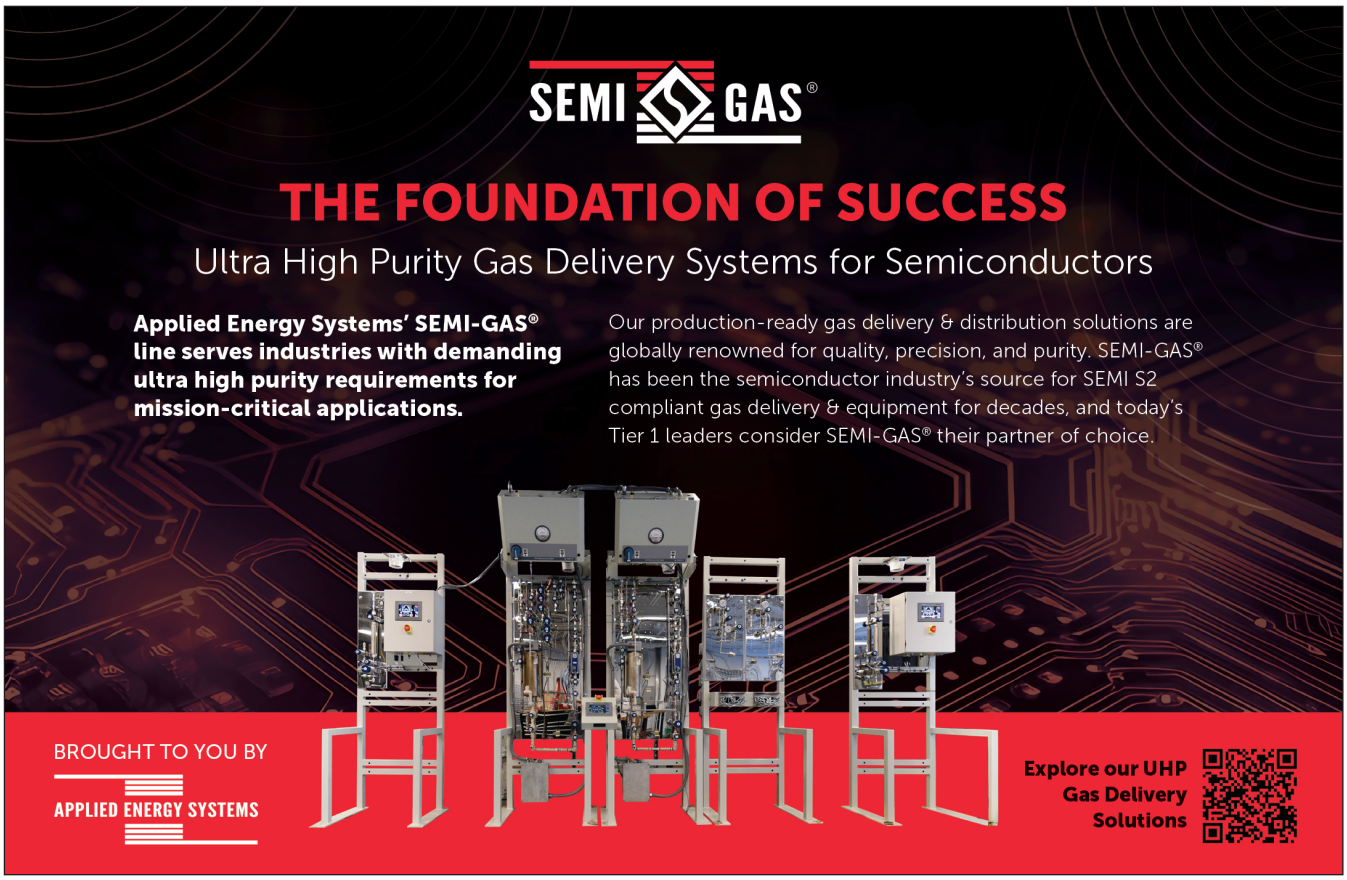
Skilled workforce

The SIA predicts that by 2030, there will be a shortage of approximately 67,000 skilled engineers and technicians in the industry. In addition, a third of the workforce is nearing retirement. More extensive training, upskilling and sustained workforce development is urgently needed. The good news is that many of these roles do not require a four-year degree. Rather, they can be fulfilled with a certification or 2-year training program.

Industry stakeholders must look to develop a national training structure, utilizing government funding and industry momentum to build critical in-house expertise. In the meantime, embracing outsourcing may be the answer to expand the labor pipeline as demand for skilled labor outpaces supply. This is particularly true if the outsourcing partner has in-depth expertise working within these highly specialized and complex environments.

Facilities management partners can help fill talent gaps in construction, operations, and maintenance, provide valuable tribal knowledge, and help ensure safety and quality. Leveraging these types of experts may hold the key to revitalization of the U.S. manufacturing industry.

Today's fabs are highly complex environments that demand precision, reliability, and real-time adaptability. Industry success will depend on a stable workforce with specialized skills, a keen eye on processes and efficiencies, and a commitment to embracing innovative facility management partners and solutions.



Why the global semiconductor industry needs SEMI EDA standards

By improving data throughput and seamlessly integrating with modern analytics and artificial intelligence-driven solutions, standards enable real-time process optimisation, predictive maintenance, and more adaptive manufacturing operations.

BY DR. FAHAD GOLRA, DIRECTOR OF PRODUCT INNOVATION, AGILEO AUTOMATION

SINCE THE development of SEMI Equipment Communications Standard 1 (SECS-I) in the early 1980s, SEMI has continually advanced the standardization of semiconductor manufacturing. SECS-I laid the groundwork for communication between semiconductor manufacturing equipment and factory systems.

Over the years, SEMI has expanded its portfolio with SECS-II, GEM (Generic Equipment Model), and the GEM300 standards suite. These standards provide a common language for communication, data exchange, and control between shop-floor equipment and IT systems. By standardizing these interactions, SEMI has enabled seamless integration of equipment from multiple vendors, an essential requirement in wafer fabrication facilities. SEMI standards now underpin key activities such as equipment communication, process control, material management, and data collection.

The evolution from SECS/GEM to EDA

More recently, SEMI introduced Equipment Data Acquisition (EDA), often referred to as Interface A, to expand its standards suite and address the semiconductor industry's increasingly diverse and complex needs. EDA standards facilitate and streamline communication between a factory's data collection applications and manufacturing equipment.

The evolution from SECS/GEM to GEM300 and now EDA is a natural progression that reflects the increasing complexity of semiconductor manufacturing. The original SECS/GEM standards established a robust framework for equipment-to-host communication and standardized equipment behavior, enabling reliable interactions and laying the foundation for automation. With the move from 200mm to 300mm wafers, GEM300 was introduced to address higher throughput requirements and advanced process control. Building on SECS/GEM, GEM300 added features such as job management, automated material handling, and material tracking that were critical to support larger wafers and increased production volumes.

As industry scaled up, the importance of data collection and utilization became paramount. The EDA (Interface A) suite emerged as a solution for high-speed, high-volume data acquisition. Complementing SECS/GEM and GEM300, EDA enables real-time data analysis, process optimization, and predictive maintenance which are vital for data-driven manufacturing.

Together, SECS/GEM, GEM300, and EDA provide a comprehensive roadmap for improving efficiency,

yield, and quality control. This evolution ensures that semiconductor fabs remain competitive, highly automated, and ready to innovate in an ever-evolving market.

Leveraging equipment data for fab efficiency

Modern semiconductor equipment generates large volumes of real-time data that underpin a wide range of critical applications, including:

- **Run-to-run control (R2R):** Dynamically adjusts equipment settings to maintain consistent output quality between production runs.
- **Fault detection and classification (FDC):** Monitors data to detect and classify anomalies, preventing defects.
- **Virtual metrology:** Predicts process parameters using sensor data, reducing the need for physical measurements and improving throughput.
- **Condition monitoring:** Analyses equipment and sensor data to predict and prevent failures, minimizing unexpected downtime.
- **Data analysis:** Identifies patterns and trends to optimize processes, improve yields, and increase overall efficiency.

These data-driven applications illustrate the transformative impact of harnessing equipment data. By implementing robust data collection standards, fabs can operate with greater agility, solve problems proactively, and continually refine their processes to stay competitive.

EDA standards

As Moore's Law continues to drive higher transistor densities, semiconductor manufacturing processes have become more complex. The EDA suite provides standardized data structures, formats, and protocols to enable the efficient data exchange between sophisticated equipment and IT systems. Building on earlier SEMI standards, EDA adds capabilities for managing high-speed, high-volume data.

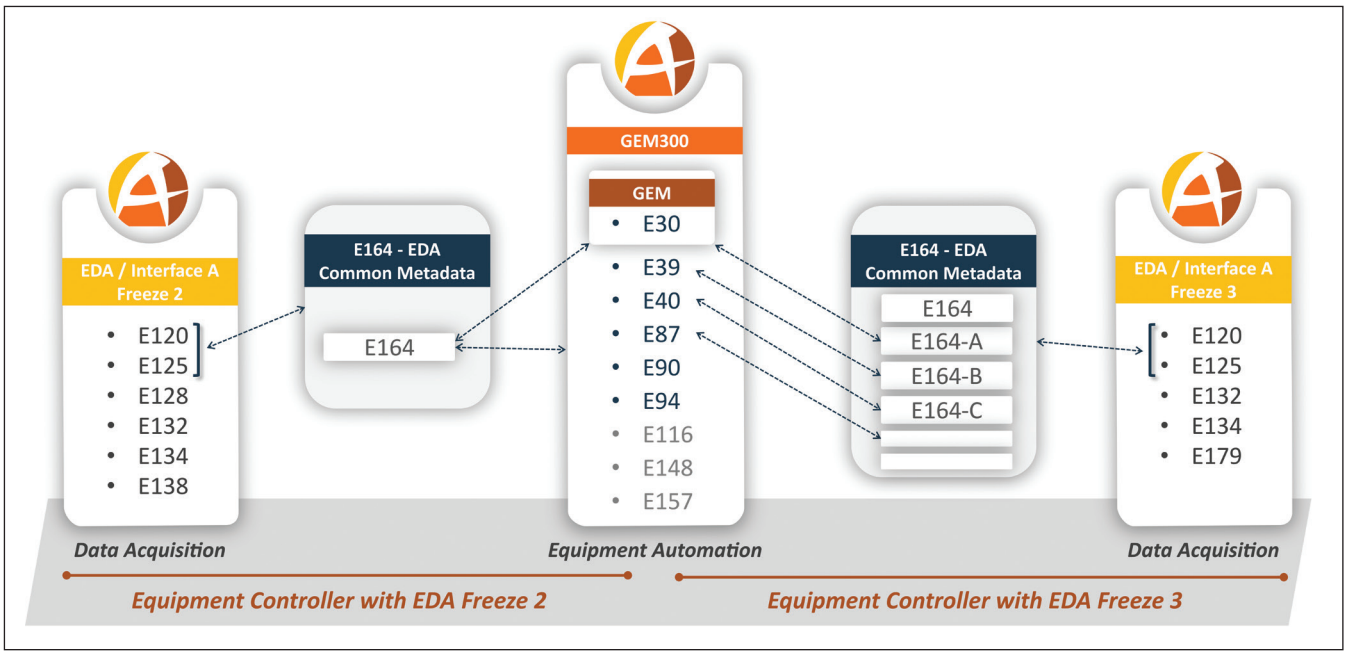
These standards address several critical capabilities such as equipment structure, communication, security, data modeling, and collection planning to enable fabs to gain actionable insights both securely and efficiently.

SEMI E164 bridges EDA and GEM/GEM300 by hierarchically modeling equipment metadata and enabling standardized access to equipment states, regardless of the underlying protocols. This integration ensures seamless data collection from increasingly complex, automated equipment.

The role of freezes

The concept of a "freeze" stabilizes SEMI standards by designating mature, reliable versions that collectively form the standards suite. SEMI E178 governs freeze versions for EDA, with Freeze 2 serving as the current stable framework for high-speed, high-volume data acquisition. As part of the ongoing evolution, the industry is preparing for Freeze 3, which will introduce support for HTTP/2, gRPC, and protocol buffers, among other enhancements.

A key element of Freeze 3 is SEMI E179, the specification for Protocol Buffers Common Components. This standard establishes a unified approach to representing errors, data types, data value types, units, and operators through protocol buffers. It will replace SEMI E138 and SEMI E128 in Freeze 3, moving the industry from XML-based structures to next-generation data exchange formats. While Freeze 3 continues to evolve, SEMI EDA Freeze 2 remains a reliable, proven standard that drives data acquisition and integration in today's semiconductor manufacturing. This evolution underscores the industry's commitment



STANDARD	DESCRIPTION
SEMI E120 – Common Equipment Model (CEM)	It provides a unified high-level structure for equipment.
SEMI E125 – Equipment Self-Description (EqSD)	It standardises how equipment capabilities and operational states are presented.
SEMI E128 – Specification for XML Message Structures	It defines XML-based message structures for consistent data exchange.
SEMI E132 – Specification for Equipment Client Authentication and Authorisation	It addresses session management and standardises authentication and authoriszation for secure data access.
SEMI E134 – Specification for Data Collection Management	It outlines the process for planning, managing, and executing data collection.
SEMI E138 – XML Semiconductor Common Components (Freeze 2 only)	It provides XML components tailored for semiconductor communication.
SEMI E179 – Protocol Buffers Common Components (Freeze 3 only)	It specifies a standardized approach to representing errors, data types, data value types, units, and operators through protocol buffers.

to embracing cutting-edge technologies for data-driven semiconductor manufacturing.

With each new process node and the growing adoption of advanced packaging techniques, the global semiconductor industry faces a steep increase in data complexity. With the upcoming Freeze 3 enhancements such as HTTP/2, gRPC, and protocol buffers, SEMI EDA standards are positioned to more efficiently handle these increasing data demands. By improving data throughput and seamlessly integrating with modern analytics and artificial intelligence-driven solutions, these standards enable real-time process optimization, predictive maintenance, and more adaptive manufacturing operations.

Fabs that embrace this evolution will realize superior yields, faster innovation cycles, and a sustainable competitive advantage in an ever-accelerating market.

Dr. Fahad Golra is Director of Product Innovation at Agileo Automation, a French firm specializing in equipment connectivity, control, and supervision solutions for the global semiconductor manufacturing industry. Since joining in 2019, he has driven practical innovations in connectivity technologies, data modeling, and communication architectures. Actively involved in SEMI and the OPC Foundation, Dr. Golra advocates Industry 4.0 adoption, focusing on interoperability, digital twins, and edge-to-cloud architectures. Over his 15-year career, he has served in academia, research, and industry. He is a recognized speaker at global semiconductor events and an accomplished author of conference papers and articles, contributing extensively to the field's ongoing evolution.

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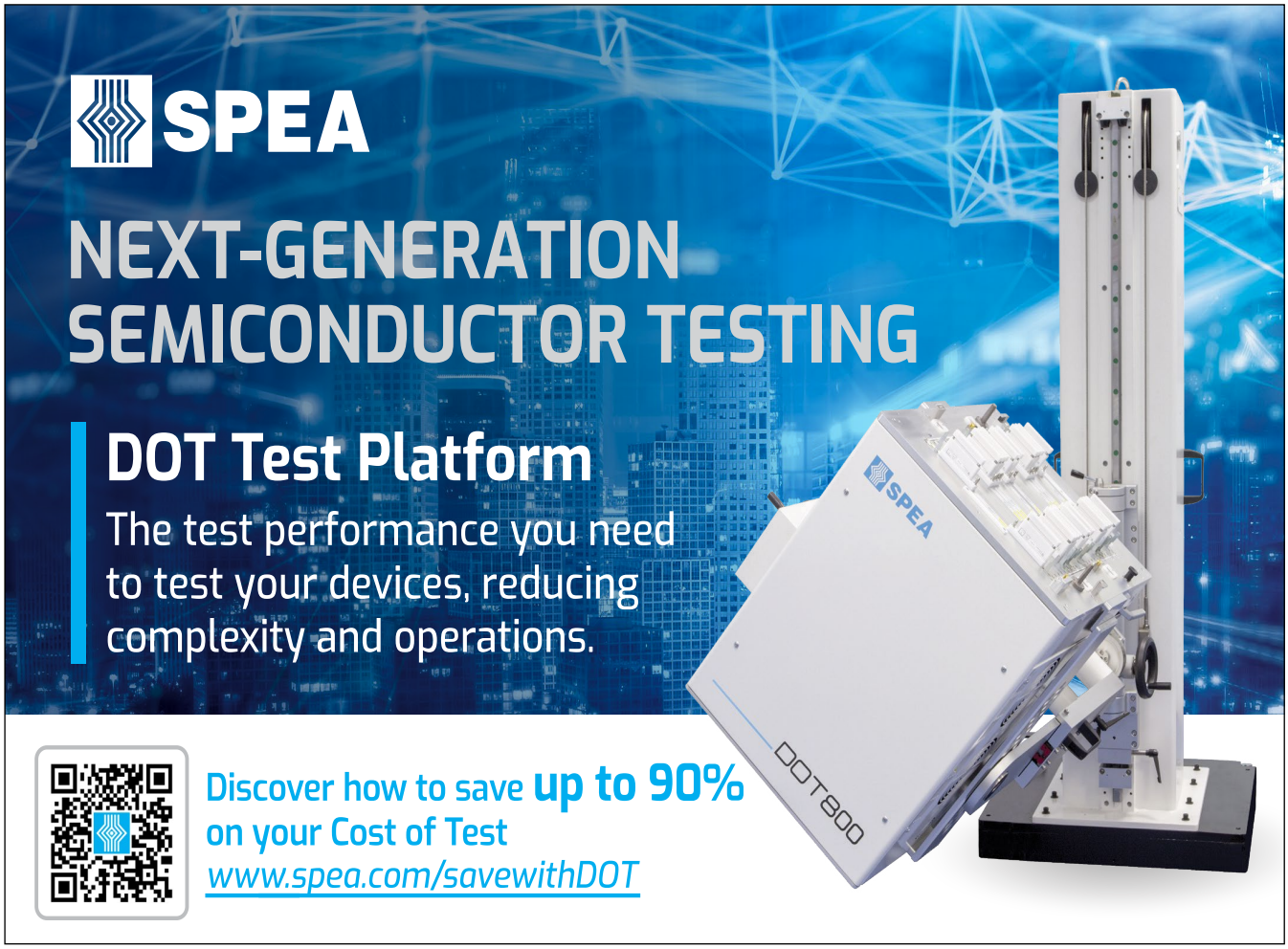
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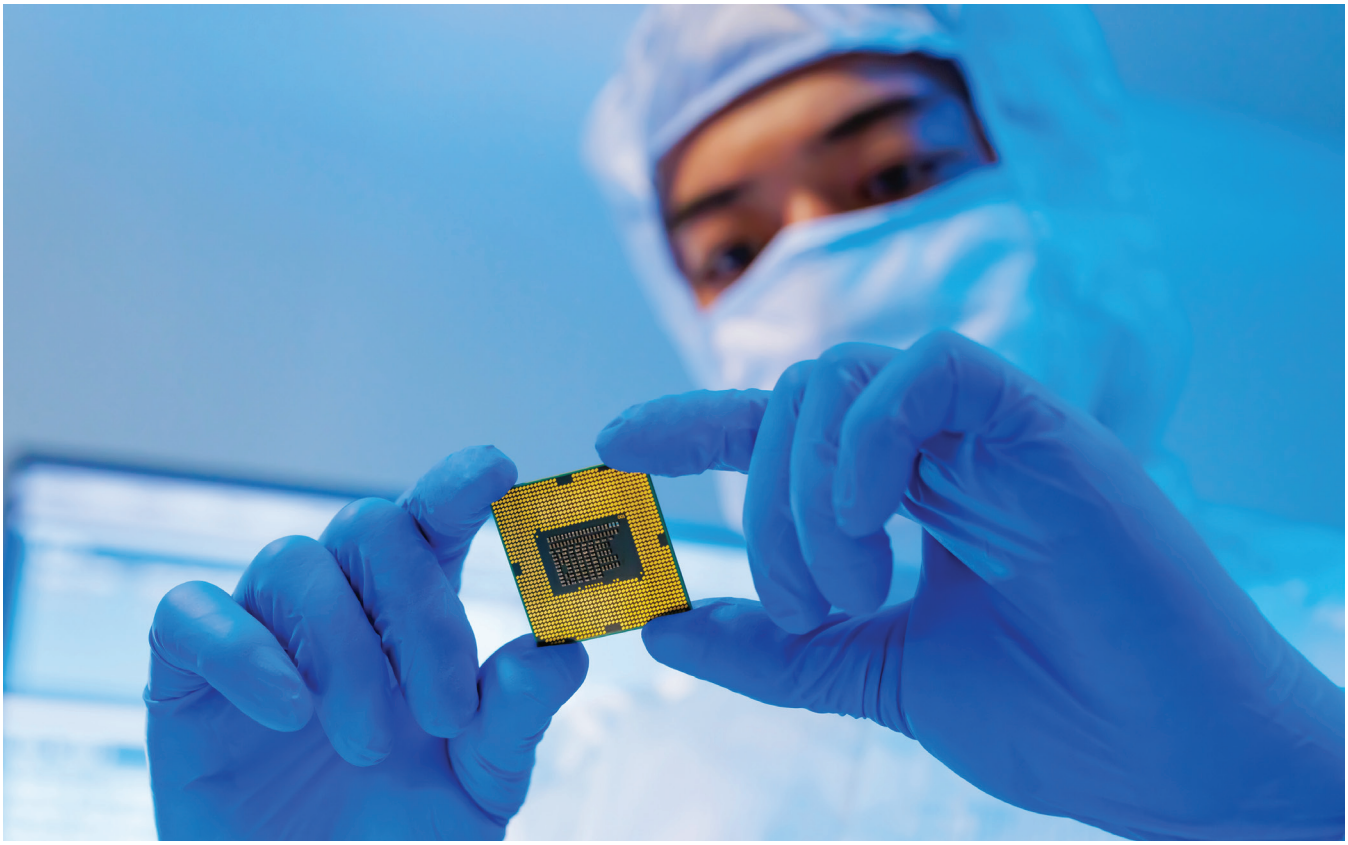


Ensuring gas purity for complex semiconductor manufacturing

As demand for chips grows, the semiconductor industry is pushing the limits of current manufacturing capabilities. Companies that invest in cutting-edge QA/QC tools will not only keep pace with demand, but also gain a competitive advantage in a fiercely competitive global market.

BY DANIEL MERRIMAN, SEMICONDUCTOR CONSULTANT AT THERMO FISHER SCIENTIFIC

SEMICONDUCTOR CHIPS are the driving force behind modern electronics. Any electronic device – from the cell phone in your pocket to the LED lights in your home or office – uses semiconductor technology, and many of these devices are becoming smarter and more connected with each iteration. There's expanding use of advanced semiconductor technology across a wide range of applications, such as artificial intelligence (AI), wearable technology and advanced data centers. In fact, Deloitte projected that the industry is on track to reach $1 trillion in chip sales by 2030, largely driven by the demand for generative AI.

As the global semiconductor industry grows to an estimated $1 trillion by 2030 and semiconductor manufacturers transition to advanced, three-dimensional chip designs that support society's technological advancement, there's a critical need for a consistent supply of ultra-high purity (UHP) gases during production. Gas impurities can result in poor device performance, production delays and revenue loss. While tools like electron microscopes can help identify micro-scale physical defects that impact production, innovative analytical technologies, such as UHP electronic gas analyzers that combine atmospheric pressure ionization mass spectrometry (API-MS), can help ensure that semiconductor manufacturers have the UHP gases they need to achieve the precision required for these semiconductors.

API-MS sets a new benchmark in gas analysis by enabling the continuous detection of impurities at exceptionally low levels. This sensitivity ensures even the tiniest contaminants are identified,

addressing the industry's need for extreme precision for manufacturers. The industry needs next-generation gas analyzers to streamline and optimize quality control (QC) processes to meet he stringent demands of semiconductor manufacturing.

Challenges in quality control for semiconductor manufacturing

Challenges in quality control remain even with the most advanced semiconductor production processes. Because chips are susceptible to impurities, which can absorb through the surface of the wafer and affect the properties of subsequent layers, even trace levels of contaminants in the gas supply can result in costly defects, production delays and revenue loss.

To maintain wafer integrity, semiconductor manufacturers need tools for greater precision in electronic specialty gas (ESG) composition, which includes nitrogen, oxygen, argon, hydrogen, helium and carbon dioxide, among others. UHP gas analyzers allow each bulk gas to be monitored for a range of potential contaminants at parts per trillion (ppt) level detection, which meets the most stringent quality requirements.

Historically, techniques such as gas chromatography and thermal desorption have been used to monitor the purity of ESGs. However, as industry focuses on producing smaller, more complex chips, these methods become inadequate for industry demands, where contamination limits must be far lower and more precise. When impurities go undetected in manufacturing, it can result in scrapped wafers, wasted resources and production line suspensions. The financial and reputational stakes are higher than ever in a growing industry under pressure to deliver flawless devices.

Adopting API-MS into workflow for QC

For continuous impurity monitoring, manufacturers should look to adopt innovative analytical technologies, such as API-MS analyzers. When coupled with sophisticated electronics and software, API-MS analyzers can help overcome the limitations of technologies like gas chromatography.

With real-time feedback, manufacturers are able to quickly address quality issues and avoid costly disruptions. API-MS analyzers can also detect a wider spectrum of impurities, such as combining oxygen and moisture with hydrocarbons, hydrogen, carbon monoxide and inert gases. This information ensures manufacturers can confidently meet evolving standards for gas purity.

Another benefit of adopting API-MS analyzers is that the technology can reduce capital and operational costs by providing multi-component and multi-stream solutions. These analyzers have built-in automated calibration capability which further reduces user intervention and drives down cost of ownership. To ensure that complex semiconductor manufacturing is optimized for maximum yield, gas manufacturers and semiconductor companies should turn to API-MS to identify, reduce and avoid defects and contamination that make high quality output a reality.

Combining analytical techniques to ensure quality

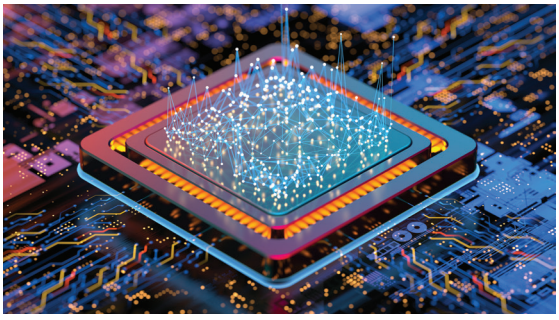
Innovation across the value chain is required to meet the demands of today's semiconductor industry. While API-MS ensures ultra-high purity gases, advanced imaging techniques, such as scanning electron microscopy (SEM), can help manufacturers identify atomic-level structural defects in semiconductors for a comprehensive approach to quality control. SEM tools use low-voltage imaging to analyze miniaturized device features without causing damage, complementing API-MS by addressing physical fault detection.

Additionally, automation in SEM workflows streamlines data collection and enhances precision, reducing production downtime and improving efficiency in fault analysis. Integrating data from API-MS and SEM provides a holistic view of the quality assurance (QA) and QC process, enabling manufacturers to quickly identify and resolve issues, ensuring seamless semiconductor production.

The path forward led by innovative technologies

As demand for chips grows, the semiconductor industry is pushing the limits of current manufacturing capabilities. Companies that invest in cutting-edge QA/QC tools will not only keep pace with demand, but also gain a competitive advantage in a fiercely competitive global market.

Semiconductor manufacturers can create a powerful and cost-effective workflow by adopting next-generation gas analyzers and advanced analytical technologies. They can significantly reduce contamination risks, minimize production delays and maintain the integrity of their products. Precision and accuracy are imperative for quality control and quality assurance in chip manufacturing and innovative tools allow companies to address the growing complexity of devices and meet market demands. With continuous technological advancements, manufacturers are better positioned than ever to deliver high-quality, flawless devices that meet expectations across industries.



Artificial intelligence in multimodal microscopy workflows for failure analysis: from 3D imaging to automated defect detection

Examining how the wealth of interconnected data will fuel the development of AI-based predictive models, capable of forecasting not only the occurrence but also the timing and underlying causes of failures from their earliest symptoms.

BY FLAVIO COGNIGNI, PRODUCT AND APPLICATION SALES SPECIALIST XRM & MULTIMODAL MICROSCOPY AND HEIKO STEGMANN, FIB-SEM APPLICATION EXPERT AND ADVISOR, CARL ZEISS MICROSCOPY

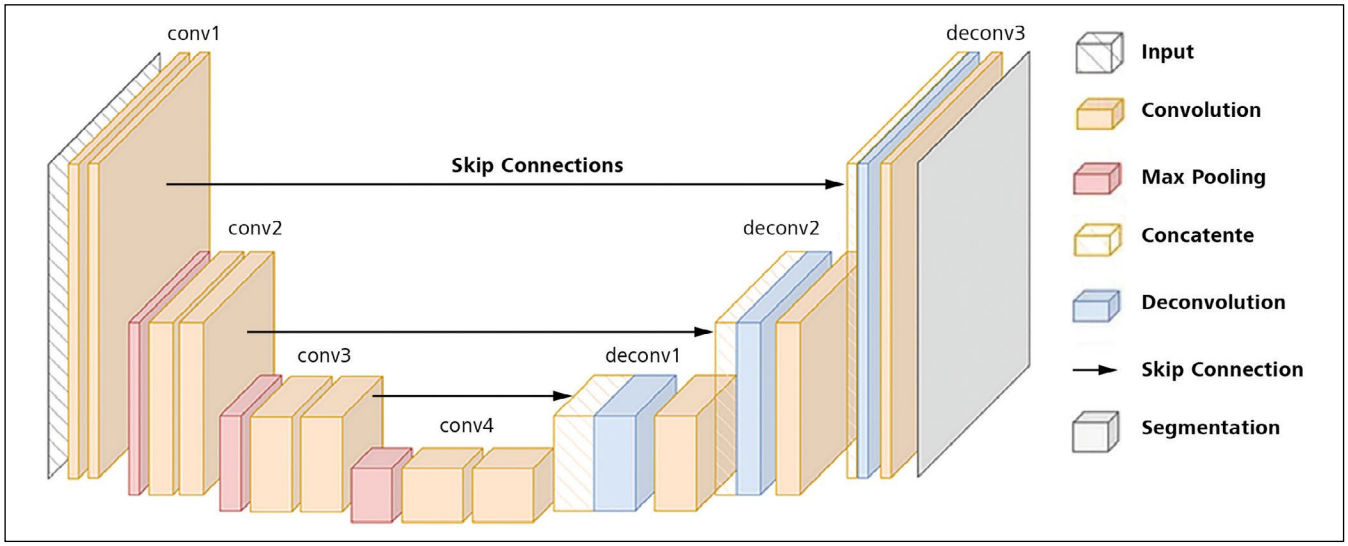
Evolution of imaging technologies and the need for artificial intelligence in failure analysis

In the fast-evolving world of electronics and semiconductors, image processing and analysis have become essential pillars of innovation, reshaping failure analysis workflows. As devices have grown more compact, complex, and densely integrated, the demand for three-dimensional (3D), high-resolution, and non-destructive imaging has increased exponentially.

Image processing and analysis constitute a distinct field of research and application, drawing upon contributions from multiple scientific disciplines such as computer science, physics, mathematics, and engineering.

The integration of knowledge from these areas has significantly advanced our capabilities in enhancing, interpreting, and extracting meaningful information from complex image datasets, thereby enabling breakthroughs across a wide range of technological and industrial domains. The increase in data volume, complexity, and dimensionality - particularly with the widespread adoption of 3D imaging and multimodal investigation workflows - has pushed traditional image analysis methods to their limits.

As a result, there is a growing need for smarter, more adaptive approaches capable of handling complex and large image datasets and automating repetitive analytical tasks.



➤ Figure 1. U-Net Explained: Understanding its Image Segmentation Architecture, author: Conor O'Sullivan.
link: https://medium.com/data-science/u-net-explained-understanding-its-image-segmentation-architecture-56e4842e313a

In this article, we explore how artificial intelligence (AI) is transforming the way image data is processed and analyzed in the context of failure analysis (FA) for electronics and semiconductors. We highlight the core benefits of AI-based approaches, examine practical applications, and discuss the future implications for research, quality assurance, and industrial reliability.

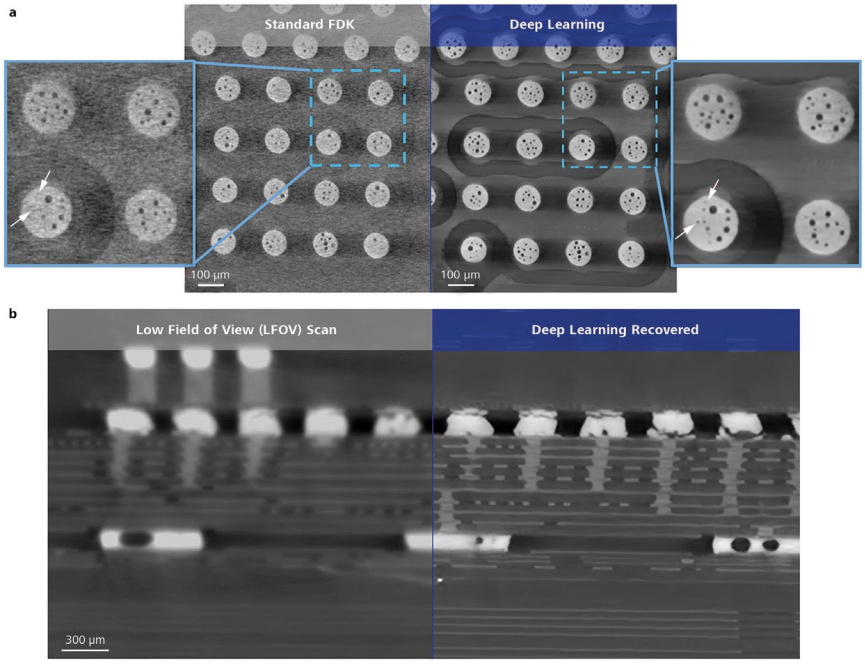
Fundamentals of AI, machine learning, and deep learning in image analysis

To understand advancements in AI applied to image processing and analysis, it is important to define key concepts. AI broadly refers to computer systems that mimic human intelligence. Machine learning (ML) is a subset of AI, where computers learn from data without explicit programming. Deep learning (DL), a further subset of ML, uses neural networks - interconnected layers of nodes inspired by brain neurons - to process information.

Among neural networks, convolutional neural networks (CNNs) are the most commonly used in image processing. The U-Net architecture is particularly prominent in the field of image segmentation and analysis, known for its high performance even with limited training data, mainly due to the presence of skip connections that help preserve spatial information during feature extraction and reconstruction (Figure 1).

Advancing image reconstruction with DL techniques

The growing need for smarter, more adaptive approaches to manage increasing complexity and dimensionality has paved the way for AI to become a powerful ally in FA. By learning from data and adapting to context, DL models can overcome hardware limitations in image quality and throughput - enhancing 3D reconstructions, enabling the detection of finer, more complex structures and hidden features, and significantly improving both the speed and accuracy of data acquisition and interpretation (Figure 2a). DL-based models have found wide application in the field of super-resolution, where AI is used to transfer the fine pixel size of a high-resolution XRM scan - characterized by a small field of view (FOV) - to a lower-resolution scan that captures a larger FOV [1] (Figure 2b).



➤ Figure 2. (a) Comparison between X-ray microscopy (XRM) datasets of a modern graphics card, reconstructed using the traditional Feldkamp-Davis-Kress (FDK) algorithm (left) and a DL algorithm (right). DL reconstruction reveals fine details that are not visible in the standard FDK reconstruction, as highlighted by the white arrows. (b) Application of a DL-based super-resolution model to transfer the fine pixel size of a high-resolution XRM scan (small FOV) onto a lower-resolution scan capturing a larger FOV [1].

AI-powered image segmentation and its impact on semiconductor FA

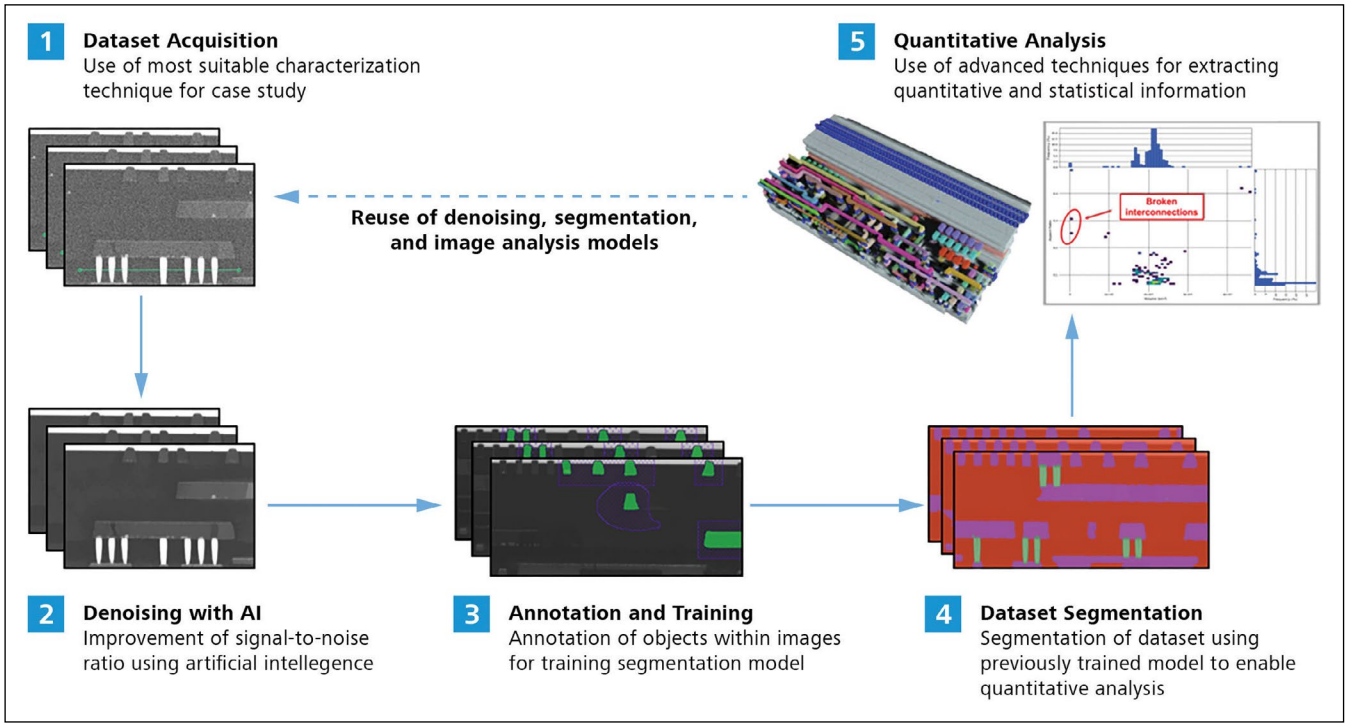
Following reconstruction and initial image processing - such as filtering - image segmentation plays a critical role as the first and fundamental step in the image analysis pipeline. It involves partitioning an image into meaningful regions or objects, such as interconnects, vias, cracks, voids, or delamination which are essential for identifying defects and understanding failure mechanisms. The schematic shown in Figure 3 illustrates a general example of an image processing and analysis workflow.

Accurate segmentation allows for precise localization and quantification of structural features, enabling analysts to focus on areas of interest and extract relevant measurements. Traditional segmentation methods, such as histogram-based thresholding, are simple and, in several applications, may be a suitable solution for accessing and revealing the desired information contained in the dataset. However, the features and characteristics, as well as both the image analysis purpose and tasks, of certain images can limit the efficacy of these methods.

Without effective segmentation, downstream tasks such as defect classification, statistical analysis, or 3D objects visualization may suffer from reduced accuracy or interpretability. As device architecture becomes increasingly complex and image datasets grow in size, dimensionality and complexity, advanced segmentation - particularly AI-powered - is becoming indispensable for enabling scalable, consistent and reproducible FA.

Overcoming computational barriers: Cloud-based training for DL models

Performing image segmentation with DL models has opened new opportunities in FA. This approach requires model training, which involves dataset annotation and significant computational effort. To be practical, training must be completed within minutes - or at most, a few hours - using a limited number of images, as extremely large training datasets and long training times hinder real-world application (Figure 4).

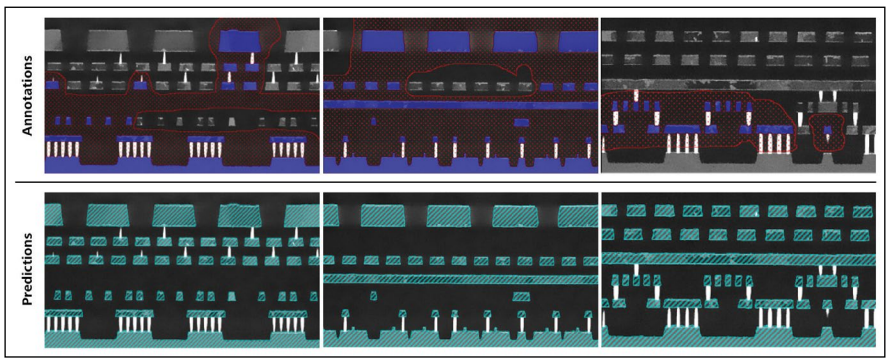


➤ Figure 3. AI-based workflow for image processing and analysis. The process includes dataset acquisition using the most appropriate characterization technique, AI-based denoising to enhance signal-to-noise ratio, object annotation for training segmentation models, automated dataset segmentation, and advanced quantitative analysis. Trained models can be reused for consistent and efficient analysis across similar datasets.

The training phase is the most resource-intensive step. While local computing resources, such as high-power workstations, are often constrained by hardware limitations - CPUs, GPUs, memory, and storage - resulting in long processing times and limited scalability, cloud computing offers a flexible alternative [2].

On-demand, pay-per-use platforms eliminate hardware barriers, provide elasticity to scale resources as needed, enable remote accessibility, and foster collaborative environments, all while reducing maintenance costs. These advantages make cloud solutions increasingly attractive for integrating DL into routine FA workflows.

Results reported in Figure 5 demonstrates how effectively DL models can segment noisy datasets - eliminating the need for extensive preprocessing - and images where different structures exhibit similar greyscale levels, making traditional methods such as histogram-based thresholding ineffective [3].



➤ Figure 4. Using modern cloud-based software solutions for annotation, training, and segmentation, the development of customized DL models becomes possible with only a limited number of annotated images and objects. For illustrative purposes, three representative images are shown in the figure [2].

Building automated multimodal pipelines with DL and Correlative Microscopy

The entire AI-powered image processing and analysis workflow can be automated within compact, integrated multimodal pipelines that combine data analysis functional units, code integration, and data storage into a single software environment, enabling complex analyses and routine operations.

For example, a Superjunction MOSFET was investigated by combining FIB-SEM tomography with 3D energy-dispersive X-ray spectroscopy (EDX), integrating nanoscale morphological information with elemental mapping. The two datasets were aligned, and their combination enabled the training of a DL model capable of segmenting the entire dataset, capturing both morphological and elemental features.

The case presented in [4] addressed a real-world industrial problem, demonstrating that this approach can automate the analysis of thousands of images from the same sample class (Figure 6).

AI algorithms can also be employed to reduce X-ray microscopy (XRM) scan time. Engineers have developed a multimodal characterization workflow that combines infrared imaging, multiscale XRM, and FIB-SEM tomography to investigate stealth laser dicing-induced defects in integrated radio frequency (RFID) devices [5].

In this study, a 10x reduction in scan time was achieved while preserving the quality of the dataset, as reported in Figure 7a. A DL segmentation model enabled the visualization of a color-coded network of metal layers within the device, as depicted in Figure 7b.

A second DL algorithm was used to guide and streamline the identification of potential defect site locations within the FIB-SEM tomography dataset volumes of interest (VOIs). Engineers observed that defects could manifest as low discharge between poly stripes and were often accompanied by small holes or voids within the first metal layer.

After two training cycles, the model demonstrated its ability to precisely identify these voids and holes, which may indicate the potential presence of a root cause of failure. Results are reported in Figure 7c,d.

The role of data management systems and AI in the connected laboratory of the future

As FA laboratories evolve, the implementation of robust data management systems (DMS) becomes critical for handling the large amount of data generated by multimodal characterization platforms. A DMS provides centralized storage, organization, and accessibility, enabling integration with AI-powered image processing and analysis workflows.

In the connected laboratory of the future, where instruments operate remotely and collaboration extends beyond physical boundaries, DMS platforms combined with multimodal microscopy and AI technologies will be essential.

They ensure efficient data management, support FAIR principles - at least within their own organizations - and accelerate the training of AI models for automated defect detection, thereby enhancing throughput, reproducibility, and innovation across semiconductor and electronics failure analysis [6].

Looking ahead, we foresee that the wealth of interconnected data will fuel the development of AI-based predictive models, capable of forecasting not only the occurrence but also the timing and underlying causes of failures from their earliest symptoms. By dramatically reducing time-to-result and empowering us to design more resilient and intelligent devices, these advances will open a new chapter for humankind - one where our technologies harmonize with the delicate systems of our world, propelling us forward while carefully minimizing our footprint on the Earth.

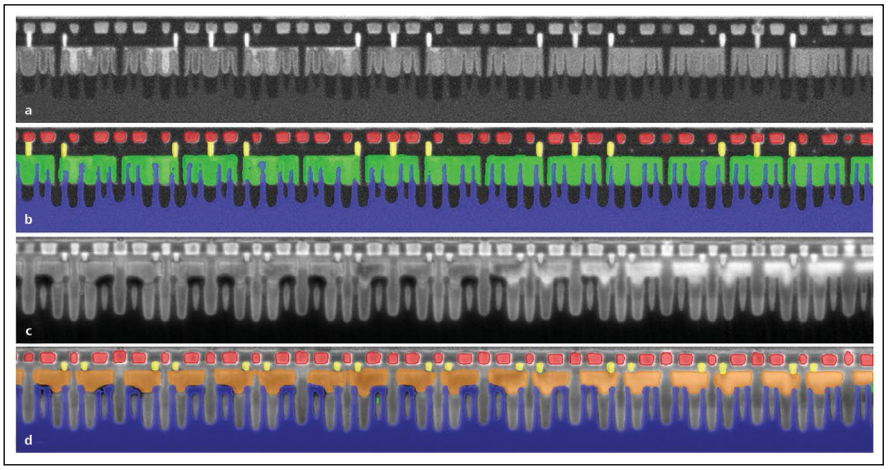


Figure 5. 2.45 x 0.29 µm² sections of a (a) BSE and a (c) SE images with their respective (b, d) segmentation with the following color codes – blue: fins, green: gates, orange: SD, yellow: contacts, red: M1 [3].

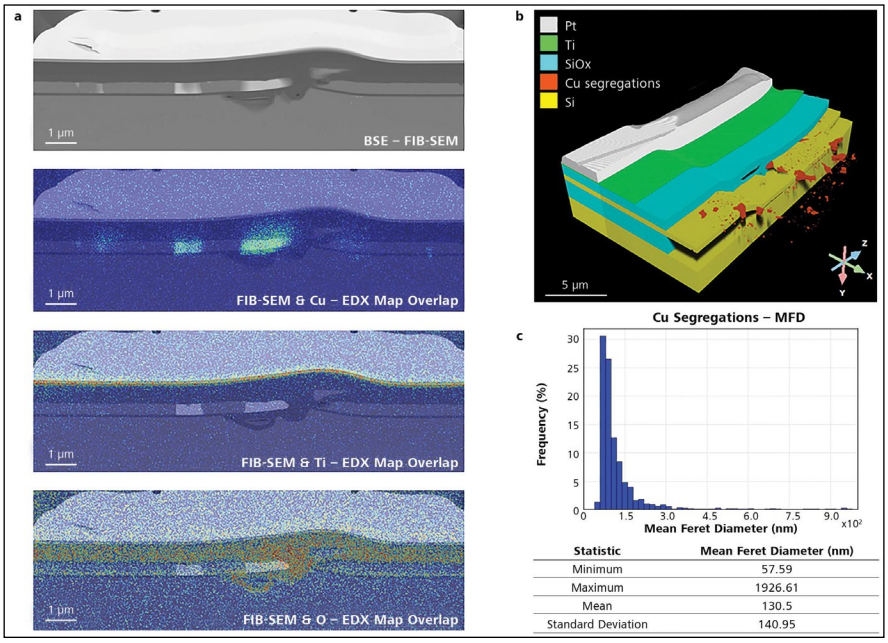
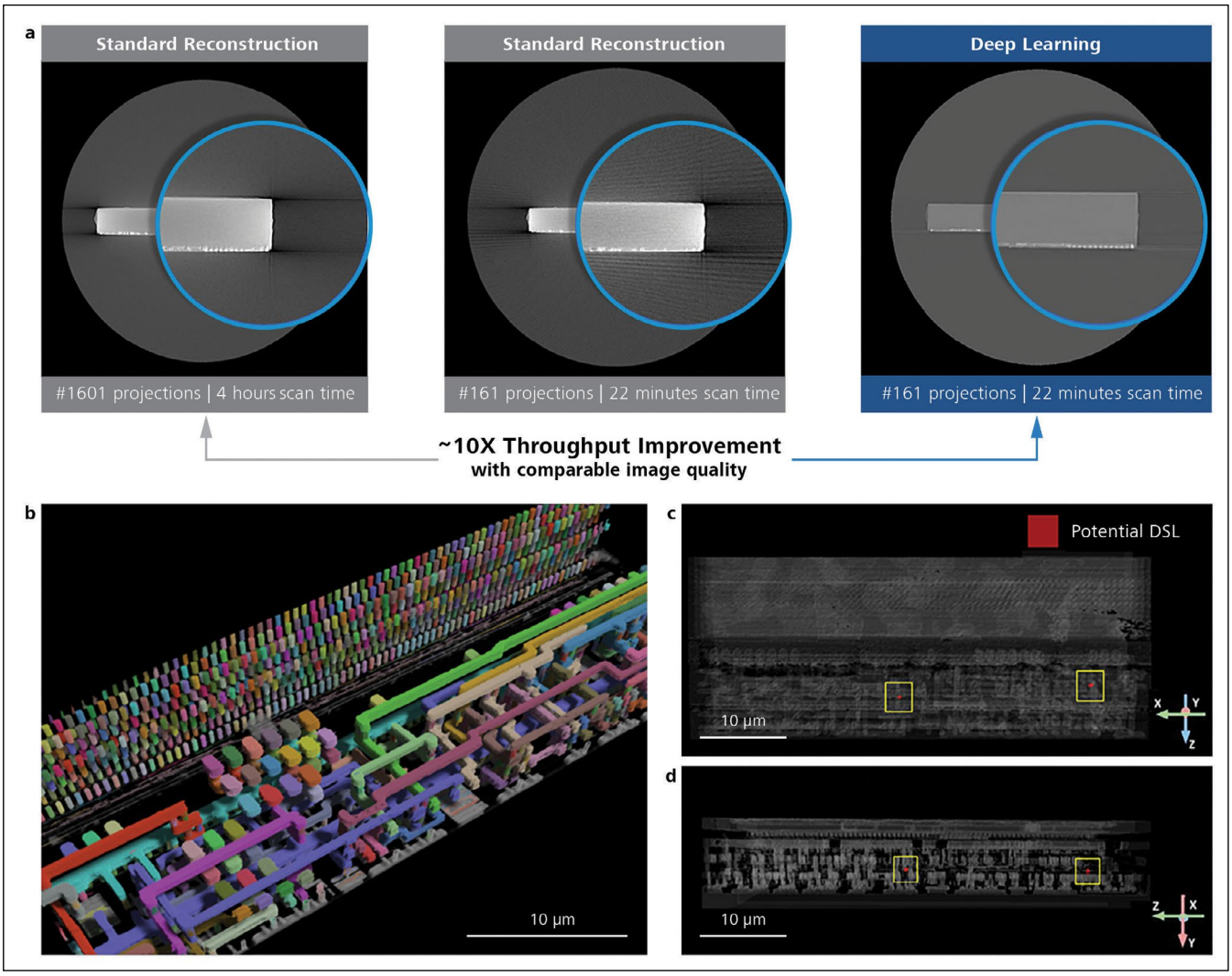


Figure 6. Example of an AI-powered integrated workflow for failure analysis. A Superjunction MOSFET was analyzed by combining FIB-SEM tomography and 3D EDX, enabling the alignment of morphological and elemental datasets. A DL model was trained on the combined data to segment structures based on both morphology and composition, allowing automated analysis across thousands of images from the same sample class. This approach demonstrates the power of multimodal data integration in real-world industrial applications [4].



➤ Figure 7 – (a) The reconstruction obtained using a DL reconstruction algorithm (right) allowed failure analyst to obtain XRM datasets in ~ 20 minutes, whilst the standard FDK reconstruction (left) required ~ 4 hours scan time. The standard FDK reconstruction (middle), obtained acquiring 161 projections, shows the typical radial artifact lines related to missing angle information. These artifacts are avoided using DL, while maintaining 161 projections, i.e., reducing the scan time by a factor of 10 [5].

For More Information
ZEISS Microscopy: www.zeiss.com/ai-multimodal-workflows

FURTHER READING / REFERENCE

➤ **[1]** Carl Zeiss Microscopy, «Advanced Reconstruction Toolbox,» 2025. [Online]. Available: https://www.zeiss.com/microscopy/en/products/software/advanced-reconstruction-toolbox.html

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➤ [4] F. Cognigni, M. Rossi, H. Stegmann, G. Sciuto, G. Anastasi, M. Astuto, M. Bonadonna e D. Mello, «A Multiscale and Multimodal Correlative Microscopy Workflow to Characterize Copper Segregations Identified in Epitaxial Layer of Power MOSFETs,» in ISTFA 2023: Conference Proceedings from the 49th International Symposium for Testing and Failure Analysis, Phoenix, Arizona, USA, 2023.

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➤ [6] Carl Zeiss Microscopy, «ZEISS arivis Hub,» 2025. [Online]. Available: https://www.zeiss.com/microscopy/en/products/software/arivis-hub.html

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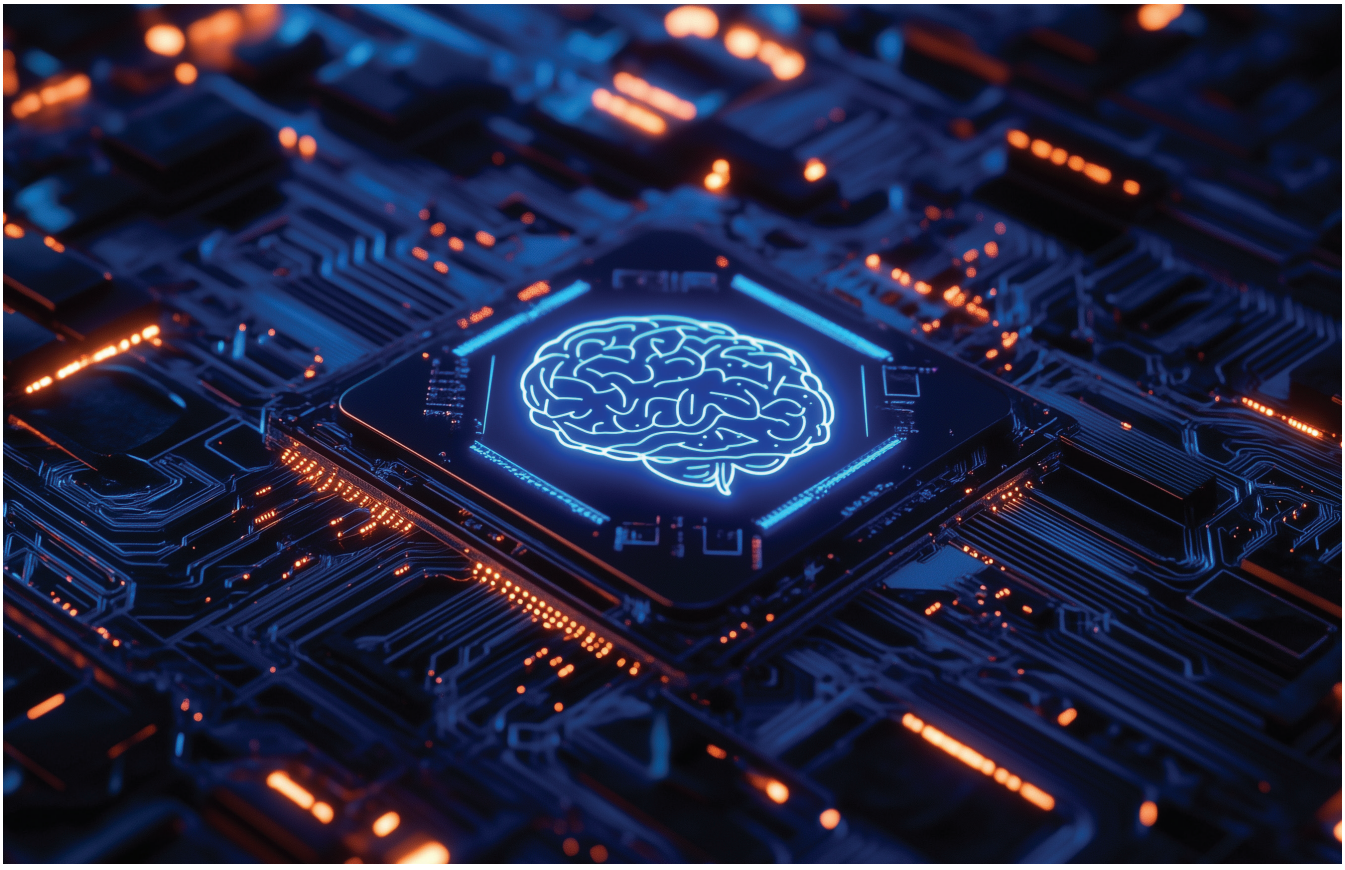


Building trust in GenAI for semiconductor design with IP lifecycle management

While Generative AI (GenAI) technologies are already transforming software development and have great potential to improve semiconductor design, their adoption in this industry remains hindered by the challenges around protecting highly sensitive intellectual property (IP), the vast costs associated with errors, and the critical need to manage data provenance and liability.

BY VISHAL MOONDHRA, VP OF SOLUTIONS ENGINEERING, PERFORCE.

THE POTENTIAL benefits of GenAI to accelerate and drive new efficiencies in semiconductor design means that there is a growing demand for these barriers and challenges to be overcome.

There is a critical need to create a solid strategy that protects IP while still enabling teams to use AI. One pillar that is being examined is to include IP lifecycle management (IPLM) processes — already part of many semiconductor design teams' ways of working — to ensure better control and traceability around how data is used to train GenAI models.

Benefits and risks of GenAI in semiconductors

To understand how that can work in practice, it helps to have some more context around the benefits and risks.

When applied appropriately, GenAI can contribute to accelerated design cycles, improved design quality, enhanced validation and verification, simplified IP reuse, and increased capacity for experimentation and innovation, as well as collaboration and knowledge sharing. GenAI can provide teams with a significant head start, helping them overcome the limitations of human time and experience. For instance, currently, understanding and debugging errors is a time- and labour-intensive process.

With effective use of AI, engineers could receive guidance about the source or reason for the error, as well as suggestions around how others have tackled similar issues. Another example could be having an AI agent look for the best IP or design block to satisfy a particular aspect of a design project, again saving the design team time and effort. However, the advantages must be carefully balanced against the challenges and risks:

- **Liability –** pertaining to IP ownership and licensing of data used for training. If GenAI models are trained on proprietary or third-party data without proper controls, sensitive IP could be leaked via the outputs generated by AI. Given the massive investments that IP vendors have made in creating and selling their designs, control over their use – including preventing third parties from using that data to train AI models or having it used in unauthorised locations — is of paramount importance.
- **Lack of traceability, data quality concerns –** it can be complicated to trace exactly how an AI model was trained. Yet traceability is essential to ensuring that the model is reproducible and that all data used in training is fully vetted for IP quality and maturity. If organizations don't fully understand exactly what data and IP versions have been used to train the model, debugging becomes nearly impossible.
- **High stakes –** the cost and potential time delays resulting from errors can be ruinous. In the domain of software applications, errors and problems, while challenging, have reasonable recovery mechanisms. However, in the semiconductor domain, the situation becomes much harder. The later an issue is detected, the more expensive it is to fix. Mistakes that reach tapeout can run into millions of dollars to address. This massive financial risk is one of the primary reasons the semiconductor industry has been slow to adopt generative AI techniques. A badly trained model, with unknown provenance of the training data set, can easily lead to generating designs that are unviable, hard to verify or otherwise error prone.

Therefore, having complete control over the process to know what and how data is being used for training, including its full provenance, has to be the foundation of any semiconductor design project involving GenAI. Semiconductor leaders who are tasked with incorporating GenAI into the design workflow must establish firm guardrails for the data used to train internal models in order to achieve the level of trust required to open the door to AI adoption, move forward, and reap the benefits of AI. Trust is the bedrock of AI adoption.

To establish trust in using AI to train internal models, it is critical to have the following:

- Clear and auditable data provenance for all training datasets
- Complete traceability of all IPs and IP versions
- Secure and compliant use of both internal and external IP.

Breaking designs into blocks

So, how do we ensure that teams do not use the wrong data — or use it incorrectly – to train their AI models? The starting point is to segment designs into a set of individual, manageable IPs or blocks. IP lifecycle management (IPLM) techniques and tools can then be utilized to manage the lifecycle of the individual IPs.

By breaking a design into individual IPs, organisations can train AI models with specific, known, vetted and trusted blocks, as opposed to an opaque, monolithic design that may contain unauthorized, poor quality, or otherwise inappropriate IP.

Increasingly deployed within the semiconductor business, IPLM follows data IP from acquisition or development through to qualification, distribution, and integration into design. IPLM makes it easier to see where each specific IP version has been used across all projects, as well as any outstanding bugs, derivative designs, and the status of verification. Fine-grained permissions can ensure that only IPs that has been authorised for use in AI models are available to include in model training, while geofencing protects IP from being used in an unauthorised country, even if user permission has been granted.

This end-to-end visibility, traceability, and IP security provides the control and transparency required to establish a trusted foundation for AI use in semiconductor design.

Ensuring data provenance and quality

With this comprehensive control and traceability, IPLM can also provide data provenance for AI training datasets. Data provenance is critical to ensuring full auditability of all designs. With IPLM, provenance can be established down to the IP version level, as well as for all associated metadata and even the design environment, ensuring that every possible variable contributing to the AI model is known, tracked, and auditable. Data can be modelled as a series of parent-child relationships to understand IP lineage, including the project(s) from which data was derived or copied.

Rules can be applied and enforced regarding the types of IP that can be used, as well as their source, to guard against contamination of the dataset and keep unauthorised IP from being incorporated into the training data. Rules can also be established to ensure certain standards for IP quality and maturity, as defined by organisations, are met before any data is used for AI training.

Consequently, semiconductor organisations can effectively build trust into their GenAI model training process, with the confidence to experiment and innovate more efficiently and safely. Furthermore, incremental training becomes possible, allowing users to see exactly what has changed since the last training set.

Training an AI model is a continuous process, not a one-time step. Users need to know: what happened in the past? How was that point reached? What is new, and what can be repeated?

These are all ways in which semiconductor teams can minimise the risks around AI use in semiconductor design while reaping the benefits. While the semiconductor industry has been cautious compared to others in its adoption to date of AI for design, the highly competitive nature of the semiconductor industry will soon force companies to move forward with AI to avoid falling behind, and organisations must be prepared.

Using IPLM helps establish and manage clear guardrails for safe, secure use of AI for semiconductor design teams. With AI's widespread adoption inevitable, now is the time to create the right foundations to safeguard IP, mitigate business risks, stay competitive, and be ready for AI's continued evolution.

Ensuring the reliable and long-lasting operation of cutting-edge semiconductor fabrication with thermoplastic Pipe Stress Analysis

Plastic piping systems are crucial for High Purity Water applications and a highly capable alternative to metal when it comes to transporting chemicals and other fluids. However, their implementation requires a number of key considerations as thermoplastics have unique material properties. Conducting a comprehensive pipe stress analysis helps to prevent issues and increase reliability, safety, and longevity.

In the microelectronics industry, piping materials play an important role to ensure mission-critical fluid handling. Water in particular is an essential natural resource for semiconductor manufacturing facilities which use millions of gallons every day.

Extensive piping systems are therefore required for the transport of high-purity-, specified- water and wastewater as well as a variety of chemicals. Here, thermoplastics have established themselves as a popular option.

This popularity is due to several factors. Materials of construction such as PVC-(C), PP-H, PE, PVDF, or ECTFE feature a high chemical and corrosion-resistance, making them a long-lasting and cost-effective option. At the same time, thermoplastics provide a number of benefits that streamline projects and simplify the installation process. Jointing technologies such as contact-free infrared fusion with a completely machine-controlled process enable efficient and high-quality pre-fabrication, while the low weight of thermoplastics makes handling and logistics easier.

➤ Many modern production plants are complex and require extensive piping systems. To successfully implement thermoplastics, a wide range of factors need to be considered during PSA, including the type of media flowing through the pipe, ambient conditions, and the length of the pipe. Source: GF.

Moreover, thermoplastic piping systems directly support today's most pressing industry challenges: a shortage of skilled labor, fast-paced facility ramp-ups, and the need to keep existing fabs operating reliably for longer periods. With faster installations, safer handling, and reduced need for rework, thermoplastics can enable semiconductor manufacturers to meet demand with greater agility and confidence.

Understanding thermoplastics

Traditionally, guidelines for the design of piping systems are mostly based on steel as a piping material. However, the standards and material properties of steel cannot be simply applied to thermoplastics. One of the most striking differences is thermal expansion: A material such as PVDF, for example, has a thermal expansion that is ten times greater than steel (≈0.13 mm/(m*K) compared to ≈0.012 mm/(m*K). In practice, a wide range of factors need to be considered to ensure accurate results, including temperature differences between the installation and operation, the type of media flowing

through the pipe, ambient conditions, and the length of the pipe.

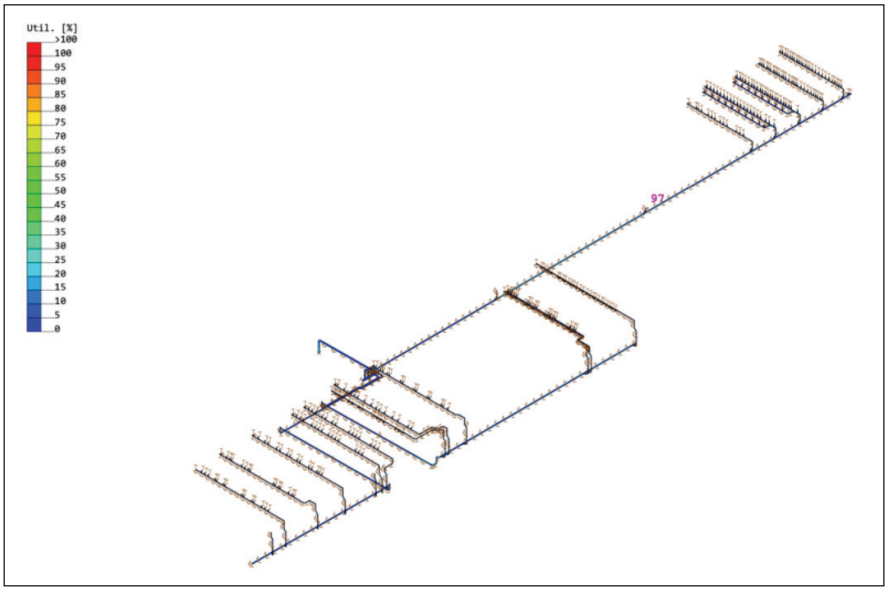
Looking at the microelectronics sector, many modern production plants are complex and require extensive piping systems with transitions between buildings. As some sections might run through temperature-controlled interior spaces while others are subjected to the elements, these systems can experience significant temperature fluctuations. This is a crucial consideration during planning as thermal expansion can lead to pipe deformation, peak-stress areas, long-term creep failures or support damage if it is not managed correctly.

Another key consideration is the material behavior of thermoplastics, meaning the short- and long-term reaction to stress experienced by these materials. Similar to steel piping systems, short-term stress factors include pressure changes, water hammer effects, seismic activity, etc. At the same time, thermoplastics have unique long-term properties. For example, these materials exhibit creep behavior at higher temperatures or under long-term loading, reducing their elastic modulus over time. If planners are not aware of the specific material properties of thermoplastics or disregard some best practices, this might lead to catastrophic failure. In order to ensure the desired operational life span of ≥25 years for industrial piping systems, controlling the long-term creep behavior by a designed support concept is key.

Why conduct a pipe stress analysis?

The goal of Pipe Stress Analysis (PSA) is simple: To predict and mitigate mechanical stress in piping systems, ensuring their structural integrity over time. The analysis process takes all relevant parameters into account, from thermal expansion to welding factors, modulus of elasticity, creep behavior, etc. This is especially important for an industry like microelectronics manufacturing which not only challenges planners with aggressive chemicals and high quality standards but is also experiencing rapid growth while facing talent shortages at the same time.

To meet demand, existing plants are being operated for longer durations and new plants are being built faster than ever. Pipe Stress Analysis enables optimum design for secondary support steel and supports planners in avoiding technical issues/claims as well as unplanned and costly downtimes.

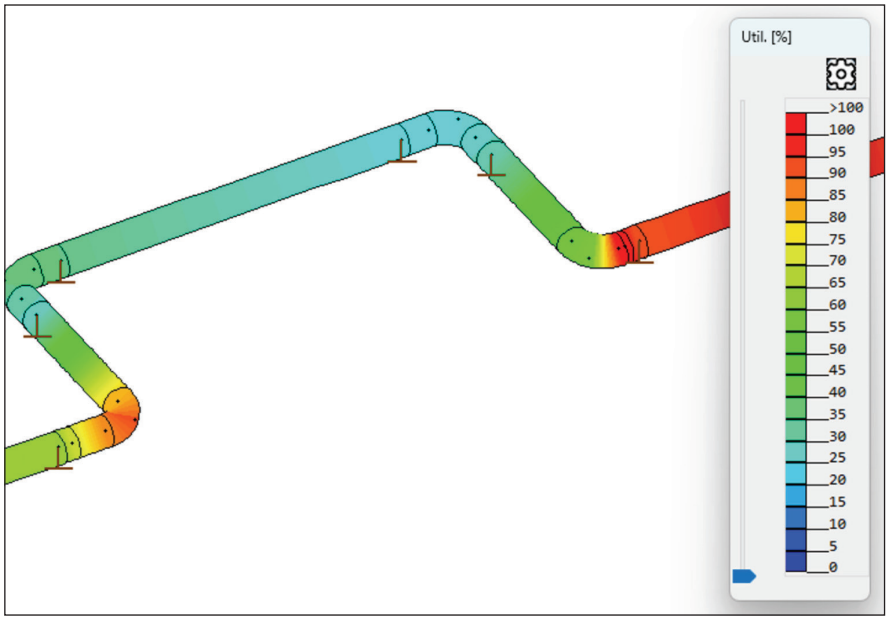


➤ PSA is particularly important for long piping systems as they experience unique stresses. Thanks to a thorough analysis, a Malaysian semiconductor plant was able to achieve a max. utilization of 62% and a safety factor of C > 1.6 over a length of nearly 20 kilometers. Source: GF.

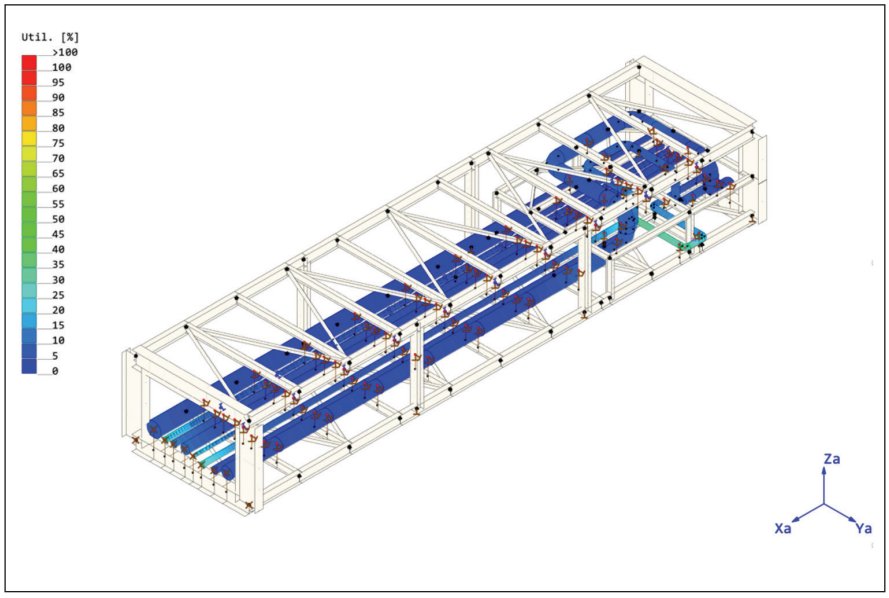
Equally important, pipe stress analysis helps teams avoid inefficiencies during fast-paced facility builds. By identifying potential problem areas early, project leaders can proactively address stress factors to keep timelines on track — even when engineering resources are stretched thin. This makes pipe stress analysis not just a safety measure, but a powerful enabler for productivity and uptime.

PSA – Some best practices

1. Accurate Stress Calculations:
To ensure a reliable, long-lasting, and safe operation, it is not only important to take all relevant parameters into account. Planners must also calculate



➤ PSA following a pipe rupture during a pressure test at a US semiconductor plant. The analysis showed peak stress due to large reaction forces and displacement, leading to a revision of the pipe support concept. Source: GF.



➤ As prefabrication is a popular choice in the microelectronics sector, unique stresses like acceleration forces during transport also need to be taken into account. Shown here is a prefabricated module with a size of ~ 6x6x21 meters (~ 20x20x70 Feet). Source: GF.

short-term stress and long-term deformation as thermoplastics react differently to temperature and stress over time.

2. Understanding your tools:
Many popular software options such as Caesar II are not optimized for thermoplastics. Alternatives like ROHR2 have been designed to correctly map both short- and long-term properties of thermoplastic piping systems.

However, software is only a tool, and the relevant parameters need to be defined by the structural engineer.

3. Load Case Mapping:
Over their lifetime, piping systems may experience a wide range of load cases that go beyond their intended operational parameters and can put significant stress on components, such as water hammer or seismic activity.

4. Engineered Pipe Support Concepts:
An engineered and designed pipe support concept is essential, as it takes the specific properties of the pipe material into account. While traditional clamps for metal systems are rigid, thermoplastic require specialized supports that allow the pipes to move naturally without damaging them. There are many different support types to choose from (e.g. guide and slide bearing options, spring hangers, expansion joints, etc.).

5. Adherence to standards/guidelines:
A static evidence according to DVS 2210-1 et al, using correct parameters for thermoplastic piping systems, meets or exceeds the ASME B31.3 guidelines for process piping and ASME NM.3.1 standard for nonmetallic materials. Some countries require a static proof by law (e.g. AwSV § 43 for double containment piping systems in Germany)

6. Analyzing existing systems:
Ensuring a reliable service life of 25 years or more is not just a matter of getting the initial planning right. Existing piping systems should be tested non-destructively in regular intervals. Should any stress peaks or deformation occur, it is advisable to conduct a condition assessment in collaboration with the manufacturer.

Taking prefabrication into account

Like other modern industries, projects in the microelectronics sector often face challenges such as a shortage of skilled labor, time constraints, cost overruns, quality concerns, or physical space limitations. Off-site prefabrication has therefore become a popular choice as flow solutions are assembled in a controlled environment by specialists, which significantly streamlines projects.

Additionally, thermoplastic materials are ideally suited due to their low weight and versatile jointing options. However, prefabrication is yet another factor that should be accounted for in the planning phase.

This particularly applies to the transportation of components to the job site. Temperature variations and the lack of operating pressure can put significant stress on thermoplastic pipes. At the same time, transportation can cause acceleration values of ≈ 0,5g to 0,8g which may lead to impact damage. Including these load cases in the initial stress analysis ensures the structural integrity of the pipe spools, while additional, designed supports can mitigate issues like displacement during transport.

Solving failures with pipe stress analysis

Pipe stress analysis is also a valuable tool when it comes to analyzing and resolving claims. This is best illustrated by an example from the field which occurred at a semiconductor manufacturing facility in the US: During a pressure test after a pipe installation at elevated temperatures of around 60°C, the system experienced a pipe rupture with a violent break as a result of slipping off the slide bearings.

After conducting a pipe stress analysis, it was confirmed that this area of the piping system was experiencing peak stress due to large reaction forces and displacement. The issue could be solved by revising the pipe support concept and retrofitting guide bearings that prevent lateral as well as vertical movement and are better suited for maintaining alignment in this scenario.

Best practices from the field

Swiss flow solutions provider GF was chosen as a supplier for a state-of-the-art microelectronics fabrication plant in Malaysia. The plant required an extensive piping solution for ultrapure water and wastewater with a total length of nearly 20 kilometers, necessitating a thorough PSA.

Rather than merely supplying products, GF was able to support the customer as a collaborative engineering partner, and contributed technical insights as well as problem-solving expertise across the project lifecycle.

To meet the demands of the application, the pipe stress analysis focused heavily

on the unique stresses associated with the considerable length. Among the most important parameters were peak stress and forces, peak displacement, as well as water hammer. These calculations resulted in the installation of ≈18 kilometers of polypropylene ranging from d20 to d500, and ≈1 kilometer of PVDF ranging from d20 to d160. In addition, the support concept and structural interface was optimized based on the results of the PSA. By conducting a thorough analysis, selecting suitable materials in the correct dimensions, and developing a compatible support concept, it was possible to achieve a safety factor of C > 1.6.

As part of the defined pipe support concept, selecting appropriate support types was key. Based on the results of the pipe stress analysis, the decision was made to change slide supports in certain sections of the piping system to guide supports. During the project, the customer selected Stress Less® supports by GF, a product family designed for PP, PE, PVC, CPVC, ABS, and PVDF pressure, waste, and double-contained piping systems. Stress Less® covers multiple installation configurations incl. guides, vertical supports, hangers, and valve mounting inserts.

The Stress Less® guide supports that were selected for the Malaysian Semiconductor FAB feature a metal bracket with a plastic insert. The clamp provides strength, e.g. during seismic events, while the plastic insert protects the surface of the pipe.

A consistent engineered gap between the insert and pipe diameter allows free movement and controlled friction in the axial direction during thermal expansion. Stress Less® also includes valve supports with threaded mounting inserts that allow valves from GF to move up to +/- 3 inches (≈ 7,6 cm).

Conclusion

Pipe stress analysis is an integral part of planning any industrial piping system, and especially for state-of-the-art semiconductor manufacturing. In order to ensure a long-lasting, reliable, and safe operation, understanding the characteristics of the piping material is key.

Due to a large variety of different thermoplastic resins being used, it is the responsibility of the calculation engineer to use correct material parameters. As a consequence, the specific life-time verification of a thermoplastic piping system can only be realized by using correct calculation parameters approved by the system manufacturer.

Despite the differences compared to steel, thermoplastics provide a wide range of significant benefits for applications in the microelectronics industry. Adhering to PSA best practices designed for thermoplastic piping systems not only streamlines the planning phase, but also enables the optimization and expansion of existing systems. This ensures maximum performance and peace of mind for operators.

50 years of innovation, shaping a sustainable future

In 2025, SCREEN Semiconductor Solutions Co., Ltd. (SCREEN SPE) celebrates a major milestone—its 50th anniversary. Since entering the semiconductor manufacturing equipment sector in 1975, SCREEN SPE has consistently pursued technological innovation and enhanced customer value.

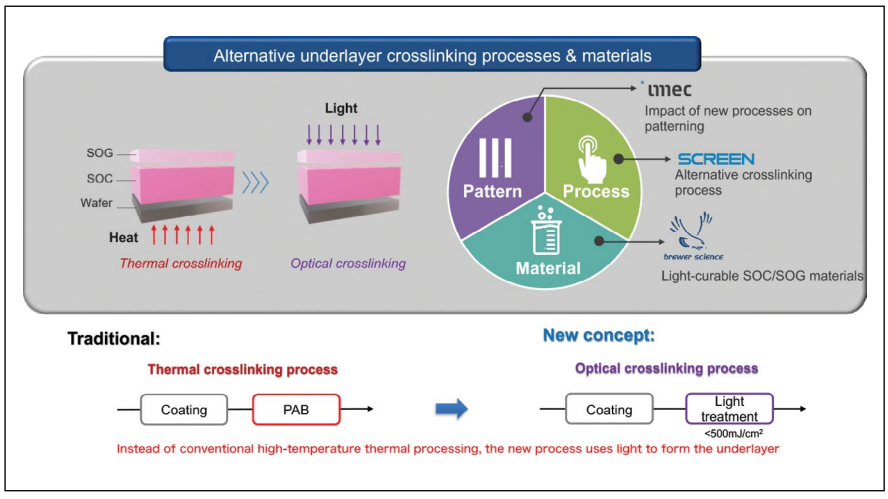
TO DATE in 2025, SCREEN SPE has shipped over 15,000 cleaning systems, including the SU series single-wafer cleaning systems, FC series batch cleaning systems, and SS series spin scrubbers. This achievement demonstrates not only the high level of trust and recognition from customers for SCREEN's performance and reliability but also the company's strong competitive position in the global market. We believe that this obligates us to strive for quality that will honor our legacy, and we believe that we must pursue sustainability to fortify our future.

The challenge toward carbon neutrality: Striving for harmony between environment and technological innovation

In recent years, the growing demand for advanced semiconductors has made the environmental impact of manufacturing processes a pressing social issue. To achieve sustainable growth, the SCREEN Group promotes sustainable management and has established "Sustainable Value 2026" as a non-financial target under its medium-term management plan, "Value Up Further 2026."

This plan aims to achieve carbon neutrality by 2050, with a goal of reducing greenhouse gas emissions by 58.1% compared to 2019 levels by March 2030.

In addition to in-house development, SCREEN SPE collaborates with world-leading research institutions and industry partners such as imec, Leti, and IBM to accelerate technological innovation in the semiconductor industry and deliver solutions that maximize added value for device manufacturers. Furthermore, SCREEN SPE contributes to building a sustainable society by providing equipment with superior environmental performance.
SCREEN SPE has long been committed to reducing water usage, energy consumption, and chemical usage in its cleaning equipment, significantly reducing the environmental impact of semiconductor manufacturing.
The same sustainability principle is now being extended to coater/developer systems, where SCREEN SPE is advancing innovative technologies to dramatically reduce power consumption. By enhancing the environmental performance of its equipment, SCREEN SPE aims to realize sustainable semiconductor manufacturing.



Case study: Photo-crosslinking technology in coater/developer systems

As demand for advanced semiconductors grows, the environmental burden of manufacturing processes is becoming increasingly severe.

In particular, the coating and developing processes face major challenges due to chemical waste treatment and the high energy consumption of thermal processes. Traditional approaches to reducing chemical usage have reached their limits, prompting SCREEN SPE to focus on reducing power consumption. The company replaced conventional processes requiring heat treatment at over 300°C with "photo-technology," which uses light energy to cure coatings. This technology significantly reduces standby power consumption because light is applied only when needed.

For this technology, SCREEN SPE delivered its DT-3000 coater/developer to imec for reliability testing and performance visualization.

Through joint development with imec, SCREEN SPE has commercialized materials and systems compatible with photo-crosslinking. Evaluations confirmed a 65–85% reduction in power consumption, a 24% reduction in CO_2 emissions, and improved productivity through shorter processing times.

Going forward, SCREEN will continue collaborating with material manufacturers and other industries to

create new technologies and value, aiming to achieve a better environment and contribute to society.

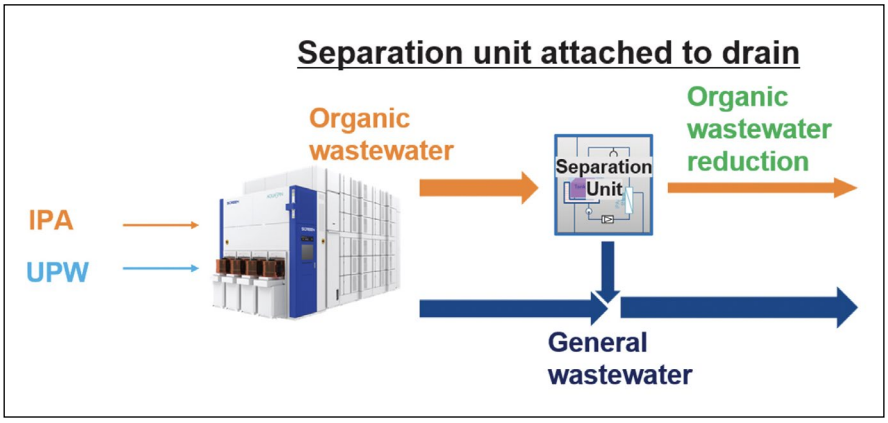
Case study: Reduction of organic wastewater using a separation membrane

In a matter of a few minutes, most anyone can use a simple web-based search or AI prompt to provide essentially unlimited amounts of interesting information about water.

Its chemical and physical properties are not only fascinating, but crucial for life on earth and a global economy comprised of sports, agriculture, and commodities transport, etc. It is no surprise that recent years have seen an increase in the amount of activity targeted at protecting this precious resource. Due to water usage rates in the semiconductor industry, this has been particularly pressing for the entire supply chain. While there are many individual processing steps and disciplines in the flow required to complete a single chip, the many dedicated cleaning steps consistently account for the largest consumption of water in a fab when compared, for example, to lithography or dry etching. For this reason, SCREEN SPE has engaged in many efforts to reduce water usage while still meeting the demands of crucial cleaning operations. One such effort is the reduction of wastewater output from single wafer cleaning equipment.

When a single wafer cleaning process is occurring, there are many potential cleaning chemicals, or mixtures of chemicals, that are applied to the wafer. However, at the end of the cleaning process a traditional water rinse with spin dry is typically performed. For many years past in manufacturing this was sufficient, but device architectures have become very challenging in part due to their extremely high aspect ratios. Very high aspect ratio features are susceptible to collapse due to capillary forces, and to overcome this, it is common to use IPA (isopropyl alcohol) to rinse the water from the wafer. The lower surface tension of the IPA assists in mitigating the collapse that is observed when using water alone.

This method of rinsing, however, creates a liquid waste stream that contains water and IPA mixed in the drain, commonly referred to as an organic wastewater drain. At this point, the waste stream will typically undergo a distillation in some type of industrial wastewater treatment facility. This process is typically very expensive and consumes a great deal of energy and time. SCREEN researchers have recognized the need for a more simple, cost-effective solution for separating such wastewater and have engaged in research which is targeted at providing a solution to this problem.



If organic wastewater containing IPA and water can be sufficiently separated then it is feasible to anticipate that each of the two components could be reused for purposes that have less demanding purity requirements or, in an optimal scenario, be reused in the cleanroom for additional wafer processing. Following this logic, our team identified effective filtration media with ideal pore sizes for separating water and IPA which can be integrated into a reasonably sized unit located in the organic wastewater drain line. Our calculations indicate that with 90wt% IPA being recovered this represents a total volume reduction of ~75% being discharged from the organic wastewater line after the separation unit. Furthermore, if a recirculation system (reuse unit) is added adjacent to the separation unit, it is reasonable to expect that purities near semiconductor grade could be recovered from the system.

An experimental lab unit was assembled with 50wt% IPA as a starting mixture for separation testing, and it was shown that with a fixed temperature, flow rate, and filter pressure, the mixture could be concentrated sufficiently to produce >99wt% IPA. In parallel with these bench tests, our engineers also conducted an analytical modeling simulation for 50wt% IPA. With other process parameters held constant, the circulation time and IPA concentration were varied in the modeling test, which yielded results within 5% of the benchtop tests.

These promising results have provided the justification for additional testing which will close the remaining gap to provide beneficial inline separation units for all sustainability-focused customers.

Conclusion

The last 50 years have invoked countless radical changes to the semiconductor industry, its requirements, and the hardware solutions that we have provided to meet these challenges. At SCREEN, we are confident that we will continue to surpass industry and customer requirements by providing intelligent solutions that are truly world class, and we will do this while maintaining an uncompromising commitment to the environment. We eagerly anticipate the arrival of all future opportunities that will allow us to provide Innovation for a Sustainable World!

Additional details:
Photo-crosslinking Technology in Coater/Developer Systems
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Test methodologies for high-performance ADC and DAC converters

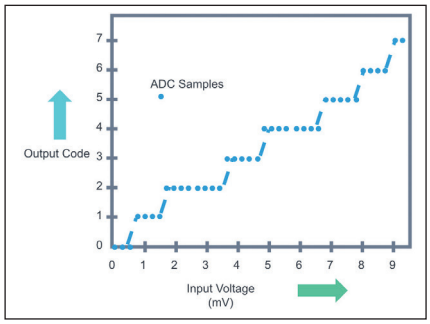
In today's increasingly interconnected world, the performance of Analog-to-Digital Converters (ADCs) and Digital-to-Analog Converters (DACs) is more critical than ever before. These ubiquitous devices form the crucial link between the analog signals of the real world and the digital data processed by electronics, underpinning applications from high-fidelity audio and advanced telecommunications to sophisticated data acquisition and control systems.

AS DEVICE complexity and performance demands continue to escalate, ensuring the accuracy, reliability, and efficiency of ADCs and DACs through rigorous testing has become paramount for semiconductor manufacturers.

The indispensable role of ADCs and DACs

ADCs are the cornerstone of data acquisition systems, transforming continuous analog signals into digital streams suitable for processing, storage, and analysis. The precision of this conversion directly impacts the integrity of downstream data, making even subtle inaccuracies unacceptable.

Conversely, DACs are vital for applications requiring the precise reconstruction of analog signals from digital data, such as digital audio. Both types of converters are defined by critical performance metrics, including maximum sample rate, bit resolution, Total Harmonic Distortion (THD), Signal-to-Noise Ratio (SNR), Integral Non-Linearity (INL), Differential Non-Linearity (DNL), Effective Number of Bits (ENOB), and jitter. Thorough testing across these parameters is essential to guarantee optimal device performance in their intended applications.



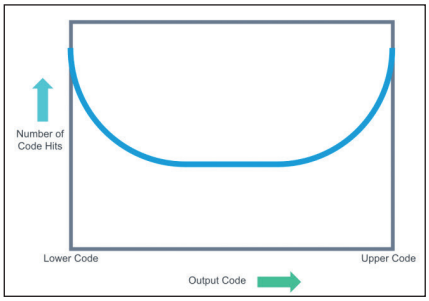
➤ Figure 1. Histogram test with linear ramp on ADC: test principle.

Navigating ADC testing complexities

Testing ADCs presents unique challenges due to the inherent sensitivity of analog measurements. Test equipment must deliver high-quality digital signals with fast edges and minimal jitter, alongside analog sources characterized by high spectral purity (high SNR and low THD). High-precision analog sources are also indispensable for accurate linearity tests like INL and DNL.

Key static testing methodologies for ADCs include the histogram test with a linear ramp and the histogram test with a sinusoidal input. The linear ramp histogram, also known as the code density test, is widely used to evaluate DNL and INL by analyzing the occurrence of each output code. Deviations from an ideal uniform distribution reveal linearity errors. While a linear ramp provides a straightforward approach, the sinusoidal input histogram offers an alternative, often simpler, method for generating a pure input signal, allowing assessment of the converter's performance across its full voltage range.

Dynamic ADC testing, on the other hand, necessitates careful consideration of various noise sources that can significantly degrade performance. Jitter on digital signals introduces errors in acquisition timing, impacting SNR. The quality of the waveform generator used for testing is also critical; it must offer a higher SNR than the Device Under Test (DUT) to ensure valid results.

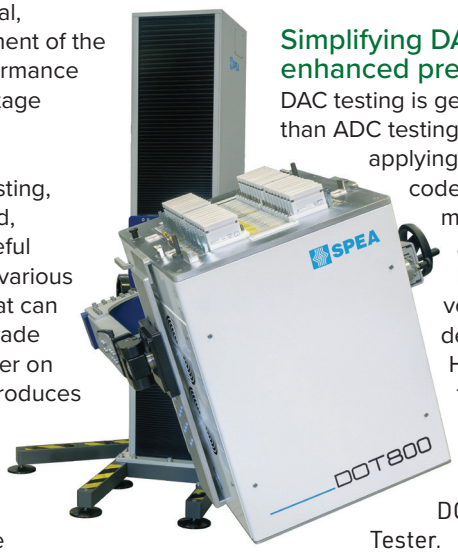


➤ Figure 2. Histogram test with sinusoidal on ADC: test principle.

Furthermore, noise originating from the ADC's voltage reference or power supplies can manifest as output noise, offset, and gain errors. Utilizing external voltage references and meticulously controlling power supply noise through parameters like Power Supply Rejection Ratio (PSRR) are crucial for accurate characterization.

Simplifying DAC testing with enhanced precision

DAC testing is generally less complex than ADC testing. It primarily involves applying a series of digital codes to the DAC and measuring the resulting analog output with a high-precision digital voltmeter (DVM) to determine DNL and INL. However, achieving the required level of



➤ Figure 3. SPEA DOT800 Mixed Signal Tester.

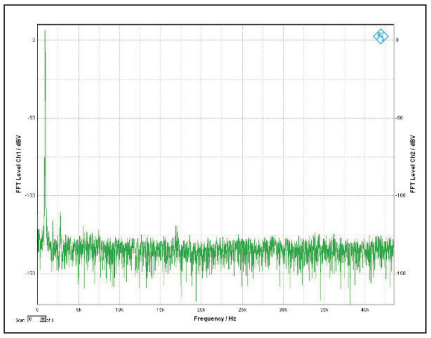
accuracy for modern high-performance DACs still demands highly precise digitizers.

To overcome limitations in digitizer accuracy, advanced strategies can be employed. The Pedestal Test enhances precision by subtracting a known pedestal voltage from the DAC output, allowing the digitizer to operate within a smaller, more resolute range. This method leverages the ramp generator of the digital processing instrument as a pre-characterized pedestal. For even greater precision, the Bucking Source Differential Amplifier technique employs a high-stability voltage source to "buck" against the DAC under test. A high-stability, low-drift Programmable Gain Amplifier (PGA) then amplifies the small difference between the DAC's output and the bucking source, enabling highly accurate measurement of DNL and INL by focusing on point-by-point differences.

SPEA DOT800: The performance edge in converter testing

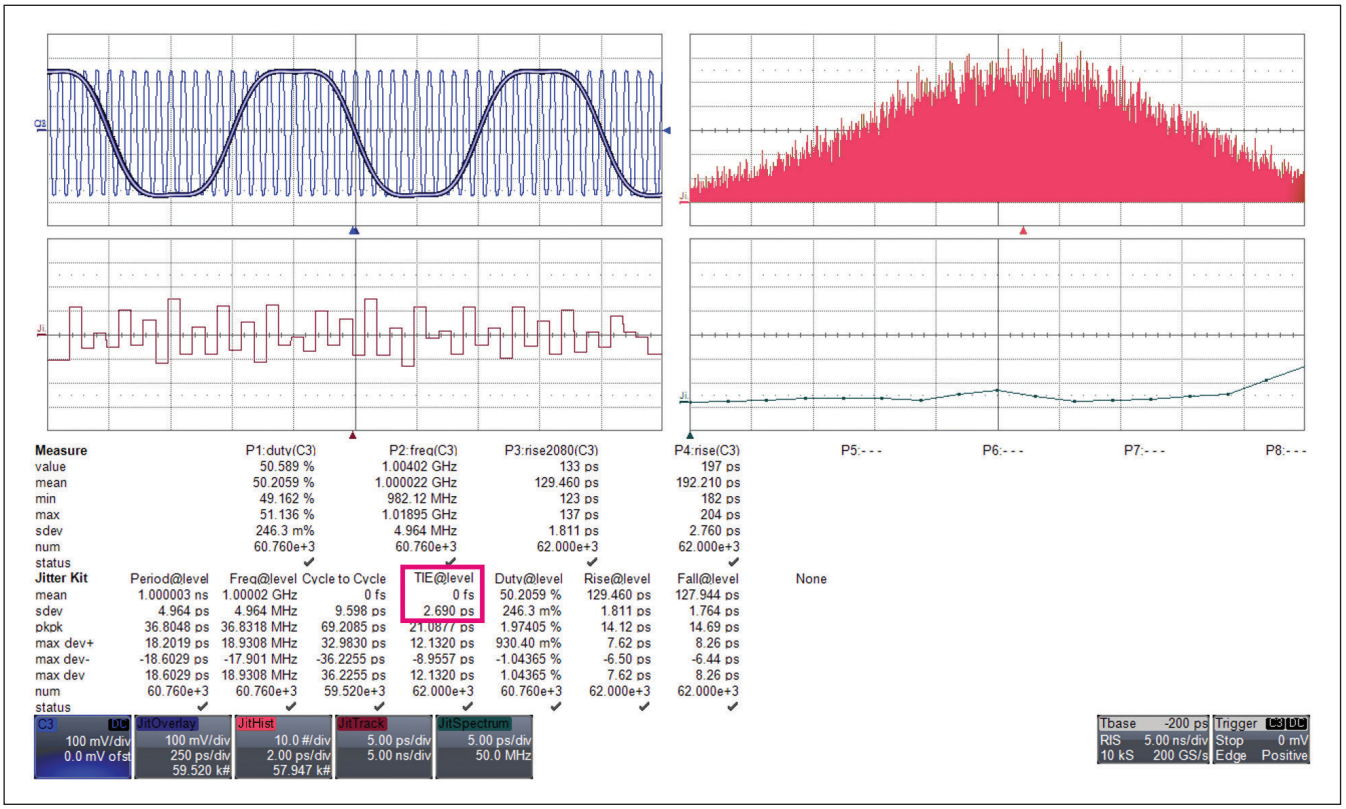
Meeting the stringent demands of both ADC and DAC testing requires sophisticated Automated Test Equipment (ATE) capable of delivering unparalleled signal integrity and measurement precision. The SPEA DOT800 tester is engineered to provide the ideal performance mix for comprehensive converter characterization. Its High-Speed Digital Channels are critical for ADC testing, offering fast edges and exceptionally low jitter (typically <2ps for a 1GHz clock). These channels feature user-programmable FPGAs, enabling the generation of standard or custom test vectors, including algorithmic patterns like PRBS, and supporting concurrent testing with digital multi-time domain capabilities. This ensures precise digital stimulus for ADCs and efficient protocol awareness.

For analog signal generation and acquisition, the High-Accuracy, Low-Noise Signal Generator within the DOT800 platform provides analog sources with superior spectral purity. It boasts a very high SNR tone (greater than 110 dB), crucial for accurate noise analysis and dynamic testing of ADCs. Its capability to generate standard and user-defined waveforms with low THD is essential for linearity tests. Furthermore, features like coherent sampling between digital signal generation and acquisition, on-board voltage references for improved measurement accuracy in low-voltage ranges, and wide synchronization capabilities across instrument resources optimize test efficiency and precision for both ADC and DAC applications.



➤ Figure 4. Voltage Spectrum of 1kHz tone generated with SPEA DOT800 signal generator shows high SNR, essential for ADC and DAC testing.

The SPEA DOT800's combination of high-accuracy digital channels, high signal-to-noise ratio, and low total harmonic distortion in signal generation makes it an ideal solution for comprehensively testing ADCs and DACs. By leveraging such advanced ATE, semiconductor manufacturers can ensure the reliable data conversion that is essential for the next generation of electronic innovations.



➤ Figure 5. Jitter measurement on 1GHz clock signals generated with SPEA DOT800 digital channels.

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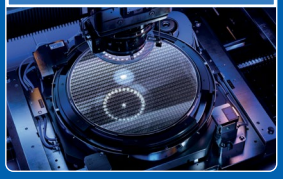

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