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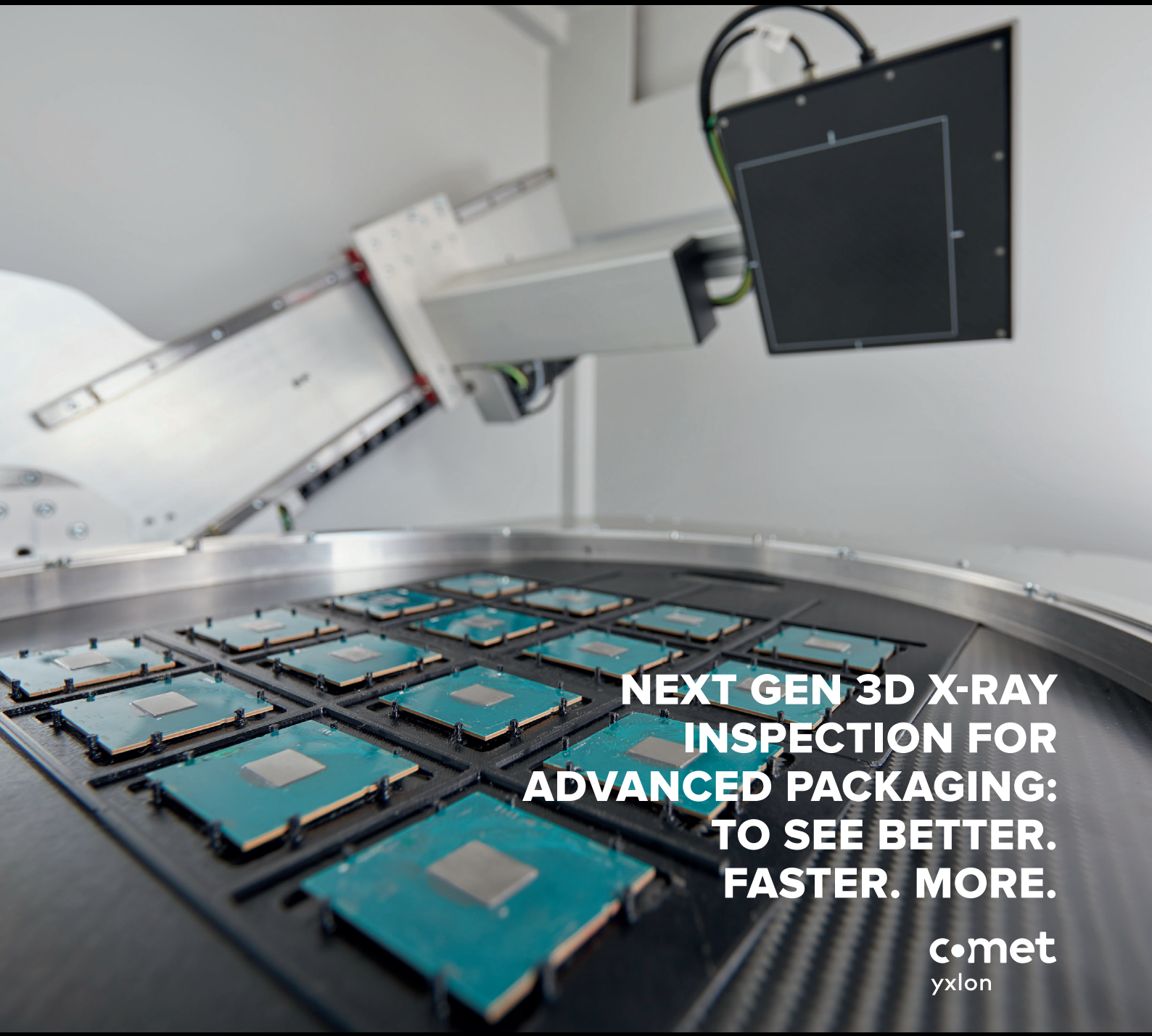

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INSIDE

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VIEWPOINT

By Phil Alsop, Editor

Plenty of reasons to celebrate the semiconductor industry's success

THE NEWS PAGES in this issue of Silicon Semiconductor demonstrate an industry in good health, with plenty of grounds for optimism over the next few years, whether or not that $1 trillion target is reached in 2030 of beyond.

One could reasonably argue that semiconductors are the most important components of the modern vehicle – whether that's the ADAS which continue to evolve, EVs themselves, or the Internet of Vehicles. Yes, many will still think of the transport future as a little bit too science fiction for their liking, but there's no doubting the general direction of travel or the massive role which semiconductors will continue to play in adding more and more intelligence to vehicles for safety and/or sustainability reasons.

Onshoring, reshoring, whatever name we give to the process of countries taking back control of their manufacturing activities, continues to be a major consideration for many nations. At the very least, countries want to ensure a safe and secure semiconductor supply chain. How much of this can be established in country, and how much relies on collaboration with other like-minded nations, remains to be seen. But the UK, Germany (and the wider EU) and India/Singapore news in this issue are just some of the latest developments in this ongoing process.

No one wants to have to worry about their chip supply chain. Alongside supply chain security, sustainability remains a major focus for the industry – and the 'Carbon dioxide capture success' story provides plenty of food for thought. Quite how our digital world can also be truly sustainable remains to be seen (without some radical consumption restrictions at some future date), but it's great to see that much work is being done in this area.

Visitors to SEMICON Europa will have the chance to see and hear how the industry is addressing the sustainability challenge, as well as, of course, witnessing how the industry continues to innovate in so many ways.

Which brings us neatly to Infineon's announcement that it has developed what it says is the world's first 300 mm power gallium nitride (GaN) technology. The silicon semiconductor industry remains the bedrock of the semiconductor sector, but it is fascinating to see the development of the new compound semiconductors, and to try and understand how they will fit alongside existing materials and solutions and where they will likely replace them.

In summary, the semiconductor industry seems to be in a good, if not great, place right now. Let us hope that this momentum continues, whatever the geopolitical climate, and however the 'great' AI story unfolds.

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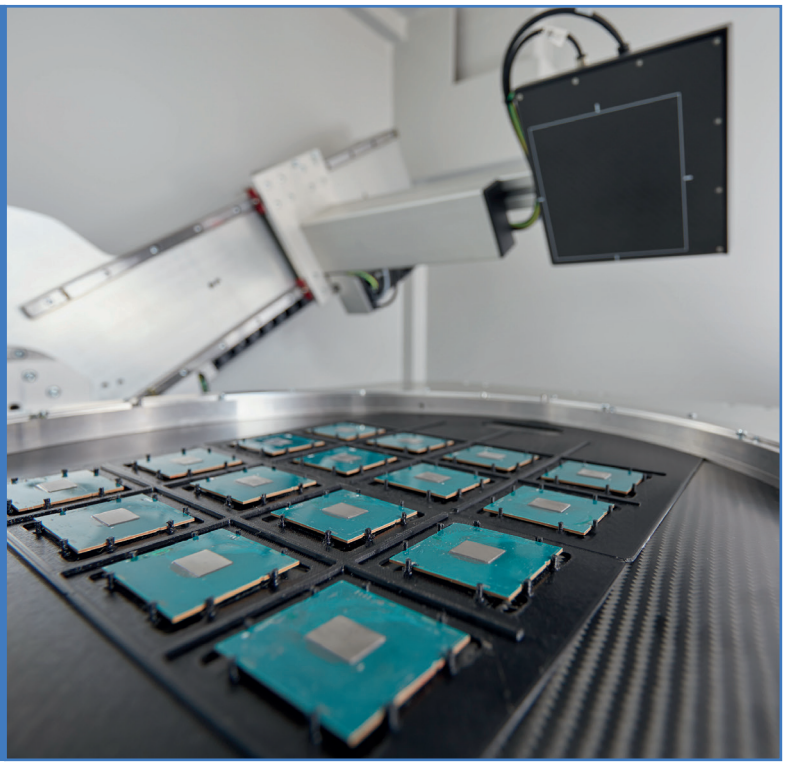

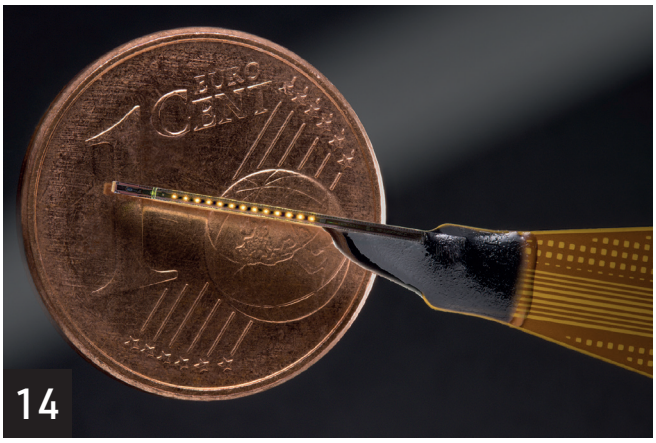

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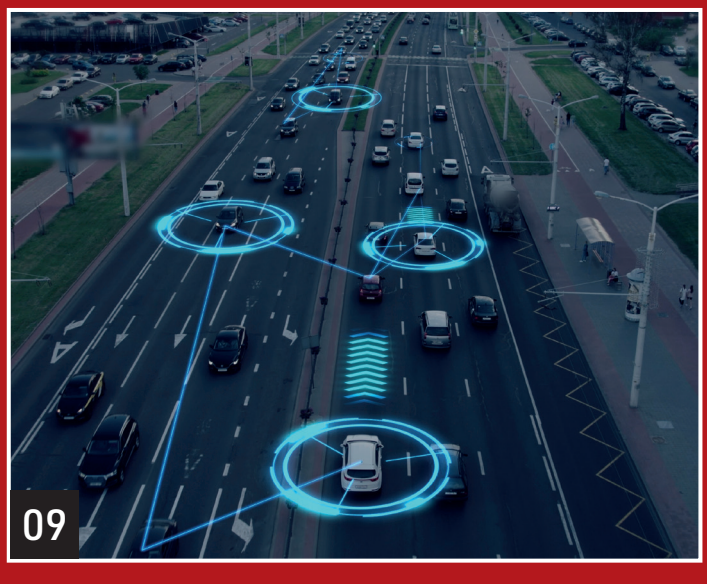
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Automotive semiconductor market poised for $88 billion by 2027

The global automotive semiconductor market is on track to surpass $88 billion by 2027, driven by the surging demand for high-performance computing (HPC) chips, graphics processing units (GPUs), radar chips, and laser sensors.

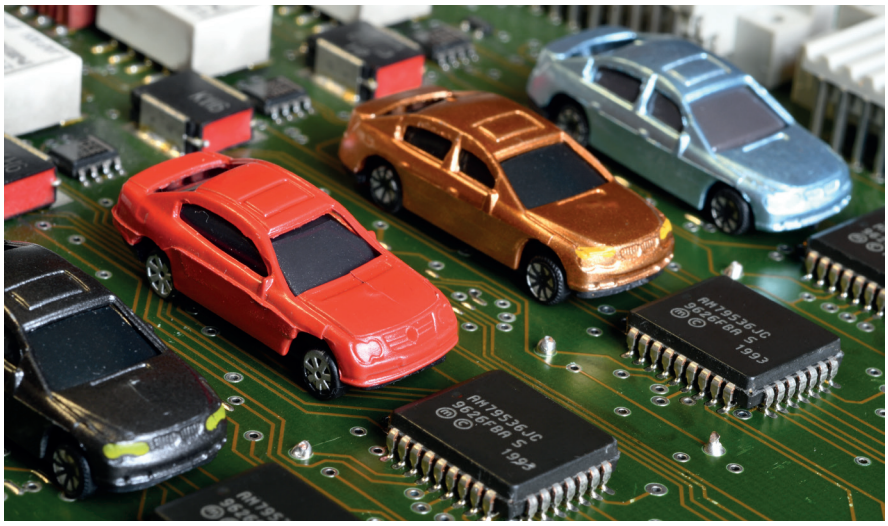
THIS GROWTH is fueled by the increasing adoption of the advanced driver assistance system (ADAS), electronic vehicles (EVs), and Internet of Vehicles (IoV), bringing new growth opportunities for the automotive semiconductor sector, according to a recent report titled 2023 Worldwide Competitive Landscape of Automotive Semiconductor.

IDC predicts that as the value of semiconductors per vehicle continues to rise, semiconductor companies will become increasingly critical to the automotive supply chain.

Leading semiconductor companies such as Infineon, NXP, STMicroelectronics, Texas Instruments (TI), and Renesas Electronics are investing heavily in developing solutions for next-generation microcontrollers, system on a chip (SoC), and high-resolution radars.

To meet the needs of automobiles for higher volume, higher performance, and higher safety of semiconductors, they continuously enhance ADAS, autonomous driving systems, and cockpit and networking features and integrate complex electronic control units (ECUs) and sensor fusion technology.

According to International Data Corporation (IDC)'s recently released report, 2023 Worldwide Competitive Landscape of Automotive Semiconductor (Doc #US50917724, July 2024), the top five vendors in the automotive semiconductor market captured over 50% of the market share in 2023. Infineon led the market with a share of 13.9%; it was followed by NXP and STMicroelectronics, holding a market share of 10.8% and 10.4%, respectively; TI and Renesas Electronics also demonstrated strong performance, accounting for 8.6% and 6.8%,



respectively, of the total share. The market landscape is as follows:

- Through ongoing technological innovation, strategic acquisitions, robust supply systems, and close cooperation with automotive original equipment manufacturers (OEMs), Infineon consistently elevated its market position in the field of power electronics and advanced control systems, establishing itself as a leader in the power semiconductor market.
- NXP possesses deep expertise in vehicle-to-everything (V2X) communication and security technologies and continually innovates and iterates. It is a frontrunner in this field as a supplier of comprehensive product solutions through close cooperation with automotive OEMs and Tier 1 suppliers.
- STMicroelectronics offers innovative solutions for the automotive industry by virtue of its specialisation in micro-electromechanical systems (MEMS) and power semiconductors.
- TI, with a wide range of analog chips and embedded solutions, delivers product portfolios that meet customers' needs. Meanwhile, it has a robust supply chain management and product quality management system to support it.
- Renesas Electronics offers a comprehensive collection of microprocessors and SoCs to ensure functional safety and reliability. Meanwhile, it employs strategic acquisitions and cooperation to maintain its leading edge in the industry.

Advancements in the automotive sector have fueled the demand for high-performance, high-safety semiconductors. As EVs and autonomous driving technologies evolve, those semiconductor companies will continue to play a key role in the global automotive semiconductor market.

According to Adela Guo, Research Director at IDC Asia Pacific, "The common strengths of these leading semiconductor vendors include substantial R&D investment and strong technological leadership, comprehensive product portfolios, solid strategic partnerships, efficient global operations, as well as safe and reliable product performance."

Support for semiconductor firms to grow, powering growth in £10bn UK industry

Science Minister Lord Vallance unveils new support for UK semiconductor scale-ups to advance innovations, from phone screens to medical tech.

UK SEMICONDUCTOR firms producing vital technology from phone screens to surgical lasers are being backed in their efforts to scale up into large businesses and drive economic growth.

The science Minister Lord Patrick Vallance has announced the 16 projects that will win a share of a £11.5 million pot – provided by Innovate UK – that will help drive innovation, as he opened an industry conference of G7 nations today (Thursday 26 September).

Pioneering projects across the country will help take the UK's thriving semiconductor industry to the next level as it further enhances everyday life – from more efficient medical devices to energy saving phone screens – and kickstart economic growth.

This comes shortly before the Government's International Investment Summit which will showcase the UK as a place to do business. Today's move is yet another reason for business to choose the UK as a place to invest – as it is backing the industries of the future. A new report by Perspective Economics reveals the UK semiconductor sector, which includes over 200 companies in research, design, and manufacturing, is valued at almost £10 billion and could grow up to £17 billion by 2030.

Semiconductors are small chips at the core of everyday technology from smartphones to renewable energy systems and this support will help to scale up domestic manufacturing and strengthen supply chain resilience, so the UK is fit for the future in a global industry.

The funding comes as the G7 Semiconductors Point of Contact group kicks off with a stakeholder forum at major UK tech company Arm's HQ in Cambridge, where member states, research organisations, and industry representatives are discussing key issues affecting the global semiconductor industry, like supporting early-stage innovation and sustainability.

Science Minister, Lord Vallance, said: "Semiconductors are an unseen but vital component in so many of the technologies we rely on in our lives and backing UK innovators offers a real opportunity to growth these firms into industry leaders, strengthening our £10bn sector and ensuring it drives economic growth.

"Our support in these projects will promote critical breakthroughs such as more efficient medical devices that could significantly lower costs and faster manufacturing processes to improve productivity.

"Hosting the G7 semiconductors Points of Contact group is also a chance to showcase the UK's competitive and growing sector and make clear our commitment to keeping the UK at the forefront of advancing technology."

Among the funded projects, receiving a share of £11.5 million, is Vector Photonics Limited in collaboration with the University of Glasgow, which aims to enhance the power and cost-effectiveness of blue light lasers in everyday technology by using gallium nitride, a high-performance material. Blue lasers are key in devices like medical equipment, quantum displays and car headlights.

Another project, led by Quantum Advanced Solutions Ltd with the University of Cambridge, is developing advanced shortwave infrared (SWIR) sensors which improve vision in critical sectors like defence, by supporting surveillance in challenging conditions

in low-visibility environments, such as during adverse weather conditions or atmospheric disturbances. The project looks to simplify production using innovative quantum dot materials – tiny semiconductor particles that emit light at specific wavelengths – offering higher sensitivity and performance, cutting costs and making this advanced technology more accessible to multiple sectors including manufacturing and healthcare.

The G7 Semiconductors Point of Contact Group, established under Italy's G7 Presidency earlier this year, continues its mission to address issues impacting the semiconductor industry, including early-stage innovation, crisis coordination, sustainability, and the impact of government policies and practices.

This meeting immediately follows the OECD Semiconductor Informal Exchange Network gathering, where countries and stakeholders shared strategies for strengthening global semiconductor supply chains and addressing shared challenges in the semiconductor industry.

The UK is playing a key role in the OECD's efforts to unite government and industry in navigating the complexities of the global chip supply chain.

Commission approves €5 billion German State aid measure to support ESMC

The European Commission has approved, under EU State aid rules, a €5 billion German measure to support European Semiconductor Manufacturing Company ('ESMC') in the construction and operation of a microchip manufacturing plant in Dresden.

ESMC is a joint venture between Taiwan Semiconductor Manufacturing Company ('TSMC'), Bosch, Infineon, and NXP. The measure will strengthen Europe's security of supply, resilience and digital sovereignty in semiconductor technologies, in line with the objectives set out in the European Chips Act Communication. The measure will also contribute to achieving the digital and green transitions.

Germany notified the Commission of its plan to support ESMC's project to build and operate a new semiconductor production facility in Dresden, Germany. The project aims at serving the demand for automotive and industrial applications.

The new large-scale manufacturing facility supported under the measure will deliver high-performance chips, based on 300mm silicon wafers with node sizes covering 28/22nm and 16/12nm, using field-effect transistor ('FinFET') technology and allowing the integration of several additional features in one chip. The produced chips will offer better performance while at the same time reducing total power consumption. The plant, which is planned to be operating at full capacity by 2029, is expected to produce 480,000 silicon wafers per year.

The facility will operate as an open foundry, meaning that any customer – including but not limited to the three other shareholders besides TSMC – can place orders for the production of specific chips. This operating model is important for the wider EU ecosystem, especially in view of ESMC's commitments to provide dedicated support to European small and medium enterprises ('SMEs') and start-ups, to strengthen their knowhow and competences. The facility will also provide special access to its production

capacities for SMEs and European universities, further supporting research and knowledge creation within Europe.

The Commission's assessment

The Commission assessed the German measure under EU State aid rules, in particular Article 107(3)(c) of the Treaty on the Functioning of the European Union ('TFEU'), which enables Member States to grant aid to facilitate the development of certain economic activities subject to certain conditions, and based on the principles set out in the European Chips Act Communication.

The Commission found that:

- The measure facilitates the development of certain economic activities, by enabling the establishment of a new mass-production facility for innovative technologies and chips in Europe.
- The facility is first-of-a-kind in Europe, as there currently is no comparable mass-production facility for the specific technology features offered. ESMC will be the first open foundry that will produce silicon wafers with 28/22nm and 16/12nm technology nodes, using FinFET technology with logic, mixed-signal, radio frequency and embedded non-volatile memory technology processes. These specific technologies differentiate it from other existing capacity and complement the production capacities needed by European customers.
- The aid has an 'incentive effect', as the beneficiary would not carry out this investment without public support.
- The measure has a limited impact on competition and trade within the EU. It is necessary and appropriate to ensure the resilience of Europe's semiconductor supply chain. In addition, the aid is proportionate and limited to the minimum necessary based on a proven funding gap (i.e. the aid amount necessary to attract the investment that otherwise would not take place). Finally, ESMC has agreed to share with Germany potential profits beyond current expectations.
- The measure has wide positive effects for the European semiconductor ecosystem and contributes to strengthening Europe's security of supply, in particular by setting up an open foundry providing access for European customers, including SMEs and start-ups. It will also enable additional support for European universities. Furthermore, ESMC has committed to comply with priority rated orders to produce crisis-relevant products in Europe in case of a crisis, as defined in the EU Chips Act Regulation. The Commission also took note that ESMC has committed to apply to be recognised as an Open EU Foundry under the EU Chips Act Regulation and will comply with all obligations linked to this status, including the commitment to invest in continued innovation in the EU with a view to achieving concrete advances in semiconductor technology, by preparing next-generation technologies as well as investing in the Union's talent pipeline.

On this basis, the Commission approved the German measure under EU State aid rules.

ESMC breaks ground on Dresden fab

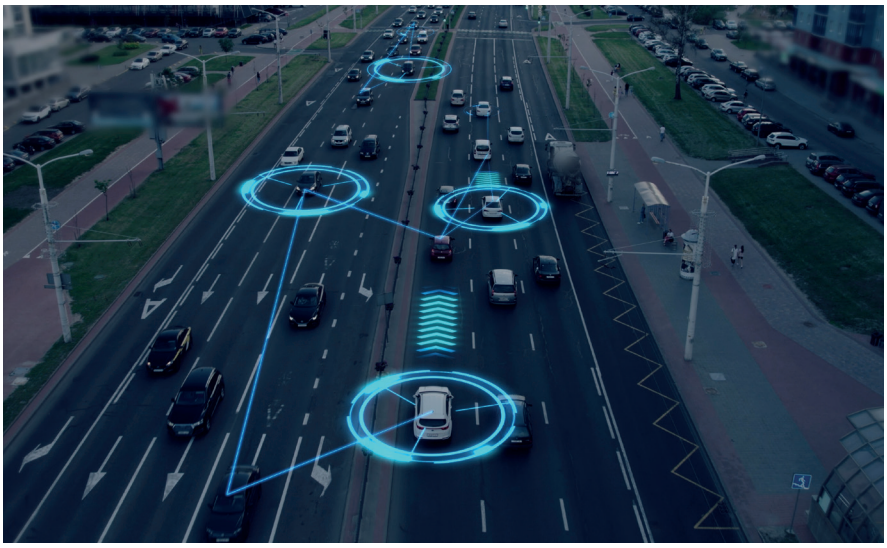
ESMC – a joint venture between TSMC, Robert Bosch GmbH, Infineon Technologies AG and NXP Semiconductors N.V. – recently held a groundbreaking ceremony to officially mark the initial phase of land preparation for its first semiconductor fab in Dresden, Germany.

THE EVENT brought together government officials, customers, suppliers, business partners and academia to celebrate a milestone in establishing what will be the EU's first-ever FinFET-capable pure-play foundry. Distinguished guests included president of the European Commission Ursula von der Leyen, German Chancellor Olaf Scholz, and Saxony Minister President Michael Kretschmer and Lord Mayor of Dresden, Dirk Hilbert.

In a demonstration of dedicated support, during the event, President von der Leyen announced that the European Commission has approved, under EU State aid rules, a €5 billion German measure to support European Semiconductor Manufacturing Company (ESMC) in the construction and operation of the semiconductor fab.

"Together with our partners, Bosch, Infineon and NXP, we are building our Dresden facility to meet the semiconductor needs of the rapidly growing European automotive and industrial sectors," said TSMC Chairman & CEO C.C. Wei. "With this state-of-the-art manufacturing facility, we will bring TSMC's advanced manufacturing capabilities within reach of our European customers and partners, which will stimulate economic development within the region and drive technological advancements across Europe."

When fully operational, ESMC is expected to have a monthly production capacity of 40,000 300mm (12-inch) wafers on TSMC's 28/22 nanometer planar CMOS and 16/12 nanometer FinFET process technology, further strengthening Europe's semiconductor manufacturing ecosystem with advanced FinFET transistor technology. Total investments are expected to exceed 10 billion euros consisting of equity injection, debt borrowing, and strong support from the European



Union and German government. The new facility is expected to generate around 2,000 direct high-tech professional jobs. Additionally, each direct job created by the project is expected to stimulate the creation of numerous indirect jobs throughout the EU supply chain, bolstering the region's economy. ESMC will uphold TSMC's standards of sustainability and environmental protection. In line with this mission, ESMC and its partners are dedicated to constructing a green fab that utilizes both existing and cutting-edge techniques to optimize conservation. This includes energy-efficient construction, water reclamation, and obtaining LEED certification.

The establishment of ESMC exemplifies the strength of TSMC's Grand Alliance, a cornerstone of innovation within the semiconductor industry. This alliance has driven groundbreaking advancements, bringing together TSMC's partners for a new level of collaboration. The investment in ESMC signifies not just a deeper commitment to this strategic partnership, but also underscores TSMC's unwavering dedication to nurturing innovation across Europe. Construction is expected to start later this year.

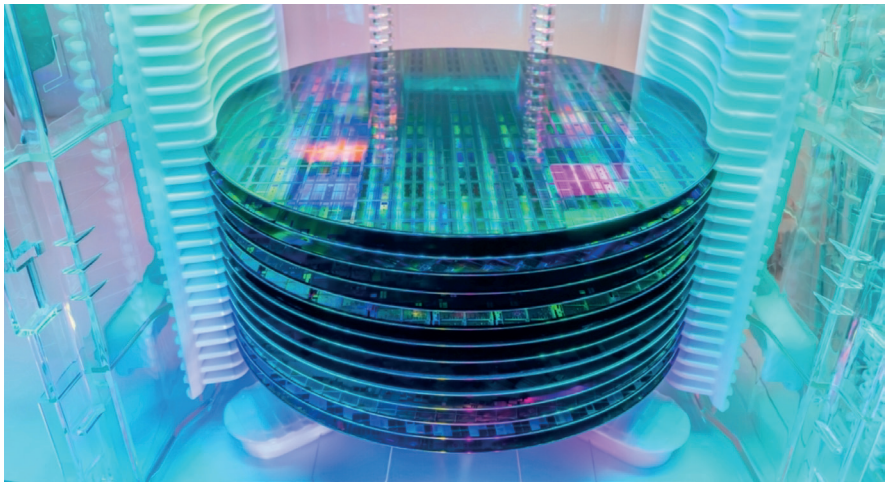
"The ESMC wafer fab is to be built right next door to our own Bosch wafer fab in Dresden. So now we will be able to watch it emerge and grow with our own eyes. We're looking forward to that, just as we are to collaborating closely with our partners TSMC, Infineon, and NXP. Together, we will take Europe a decisive step forward in a key industry, and ensure that advanced chips are available for industrial enterprises here," said Dr. Stefan Hartung, chairman of the board of management of Robert Bosch GmbH.

"Our joint investment in Dresden once again highlights the enormous significance of Silicon Saxony as a magnet for leading international semiconductor manufacturers," said Infineon Technologies AG CEO Jochen Hanebeck. "The construction of another semiconductor manufacturing facility in Dresden by ESMC constitutes a major success for the region. We are bringing to Europe a particularly important semiconductor technology which is used in the most modern digital chips. This investment will create additional jobs and will permanently strengthen the semiconductor ecosystem in Silicon Saxony, Germany and Europe as a whole."

Singapore and India sign MOU on semiconductor ecosystem partnership

Singapore and India exchanged a Memorandum of Understanding (MOU) to partner and cooperate in the field of semiconductors.

THE MOU aims to support India's growing semiconductor industry while facilitating Singapore's ecosystem of semiconductor companies and related supply chains to participate in the fast-growing Indian market.
The MOU was exchanged in the presence of India's Prime Minister Narendra Modi and Prime Minister Lawrence Wong during Prime Minister Modi's Official Visit to Singapore. It was signed earlier by Deputy Prime Minister and Minister for Trade and Industry, Gan Kim Yong and India Minister of Electronics and Information Technology, Ashwini Vaishnaw, on the sidelines of the India-Singapore Ministerial Roundtable on 26 August 2024.



MOU on India-Singapore
Semiconductor Ecosystem Partnership India aims to establish itself as a global node for semiconductor manufacturing, driven by strong domestic demand in the electronics, electric vehicles, and manufacturing sectors. Singapore's established semiconductor ecosystem has produced a strong cluster of semiconductor companies which are keen to participate in the growth of India's semiconductor industry.

Under the MOU, Singapore and India will leverage complementary strengths in their semiconductor ecosystems and tap on opportunities to build resilience in their semiconductor supply chains. This will include governmentled policy exchanges on ecosystem development, supply chain resilience, and workforce development. The Ministry of Trade and Industry (MTI) and India's Ministry of Electronics and Information Technology (MeitY) will establish a Policy Dialogue to facilitate discussions, oversee the implementation of the areas of collaboration, and exchange best practices. A parallel business-to-business Cooperation Forum will be established and led by Enterprise Singapore and the India Semiconductor Mission (ISM) to encourage and catalyse more private sector partnerships between both countries.

Deputy Prime Minister and Minister for Trade and Industry Gan Kim Yong said, "This MOU signals India's and Singapore's commitment to work together in the field of semiconductors to address the demand from industries around the world. This will also strengthen semiconductor supply chain resilience and create new markets and opportunities for businesses in our countries."

"Singapore plays an important role in the global semiconductor supply PRESS RELEASE chain. Our companies bring with them extensive expertise through their collaborations with global semiconductor players, and can value-add by providing services, solutions, components and more to global chipmakers and large equipment manufacturers. These capabilities and track record position them well to cement and strengthen the partnership between Singapore and India in the semiconductor space," said Deputy Managing Director, Enterprise Singapore, Tan Soon Kim. "Through our series of semiconductor delegations to India this year, EnterpriseSG has also seen positive reception from the engagements between Singapore companies and Indian officials and partners. We encourage more companies to leverage this latest MOU to tap on the growing opportunities in India."

Growing momentum between India's and Singapore's semiconductor ecosystems
During his visit in Singapore, Prime Minister Modi was hosted to a site visit by Singapore semiconductor ecosystem player, AEM Singapore. He was accompanied by Prime Minister Wong and Minister for Home Affairs and Minister for Law K Shanmugam. The visit comprised a sharing led by Singapore Semiconductor Industry Association (SSIA) on the development of Singapore's semiconductor industry and opportunities for mutual collaboration between Singapore and India partners, and a tour of AEM's facilities. Prime Minister Modi also engaged with ecosystem players and institutions such as APP Systems, Century Water, Ecsal Technologies, NexGen Wafer Systems, PEP Innovation and Temasek Polytechnic.

Carbon dioxide capture success

WACKER successfully tests carbon dioxide capture from the silicon production process.

WACKER has successfully captured carbon dioxide (CO_2) generated from silicon production. The project, which was enabled by the technology and expertise of the SLB and Aker Carbon Capture Joint Venture (SLB-ACC JV), involved a pilot test of the capture process at WACKER's production site in Holla, Norway, where quartz and carbon are combined to produce silicon for use in its silicone products. This reaction generates a considerable share of the CO_2 emissions relevant to WACKER and its products. The newly tested capture process makes it possible to reuse or store this greenhouse gas and prevent its release into the atmosphere – a critical step on the road to net-zero chemicals production.

Holla is where WACKER manufactures roughly one-third of the silicon metal that it needs for its production. The company carried out a successful carbon-capture pilot project here. Combined with green electricity and the use of renewable charcoal, this will open the door to future climate-neutral silicon value chains (photo: WACKER) SLB-ACC JV specializes in capturing CO_2 from flue gases from large-scale industrial processes, including unavoidable CO_2 such as that generated in the production of metallurgical-grade silicon. WACKER's production plant in Holla produces this important raw material, which serves as the basis for microchips, solar modules and the full range of silicones.

SLB ACC JV's mobile test unit (MTU) was installed at WACKER's site in Holla. The MTU is a complete CO_2 capture plant on a small scale. The waste gas generated from silicon production was piped directly into the pilot plant, where carbon dioxide was captured via a chemical process known as amine scrubbing. This makes use of an amine-containing solvent that selectively extracts CO_2 from the gas mixture. In large-scale industrial processes, the CO_2 is then released from the solvent by desorption before it is cooled, condensed under pressure and purified.

On the road to closed carbon cycles

For the first time, WACKER has demonstrated the amine scrubbing method for removing carbon dioxide in one of its own processes. The pilot test campaign, which was successfully concluded in late June, achieved capture rates of over 95%. The project team also thoroughly studied and validated the process parameters, delivering important information needed for large-scale implementation.

At the same time, WACKER and SLB-ACC JV conducted an engineering feasibility study as well, which involved drafting a design for a plant that would capture 180,000 metric tons of CO_2 annually. These calculations have now been supplemented with the data obtained in actual practice.

"The results of the pilot study are a huge success for us. We've shown that this technology makes it possible to remove CO_2 effectively," says WACKER CEO Christian Hartel. Capturing carbon dioxide prevents its release into the atmosphere as a greenhouse gas. It can then be put to other uses, such as creating synthetic fuels (e-fuels) or synthesizing methanol as a starting material for other chemical processes.

Storing it underground (carbon capture and storage, CCS) is also an option. The project represents an important step on the road to closed carbon cycles. "What we need now are customers that will buy the CO_2 from us and a regulatory framework that can help us build the business case," Hartel goes on to say.

Net Zero by 2045

WACKER has set ambitious sustainability goals for itself. By 2030, the company's absolute greenhouse gas emissions are to be 50% lower (compared to 2020). By 2045, WACKER intends to achieve net zero, which means it would no longer emit any net CO_2 whatsoever. Silicon production in Holla is a major piece of that puzzle.

The objective for this site is full CO_2-neutral production. The energy-intensive manufacturing processes here began running on 100% green electricity from sources such as hydroelectric power back in 2022. And the gradual switch from bituminous coal to biogenic sources of carbon is to be complete by 2030. Green electricity, sustainable carbon and carbon capture will one day make climate-neutral silicon value chains a reality.

The amount of carbon dioxide released during silicon production is the most critical factor in the carbon footprint of silicones. The use of CO_2-neutral metallurgical-grade silicon from Holla could significantly reduce the carbon footprint of the company's silicone products.

An industry game-changer?

Infineon pioneers world's first 300 mm power gallium nitride (GaN) technology.

INFINEON TECHNOLOGIES has succeeded in developing the world's first 300 mm power gallium nitride (GaN) wafer technology. Infineon believes that it is the first company in the world to master this groundbreaking technology in an existing and scalable high-volume manufacturing environment.

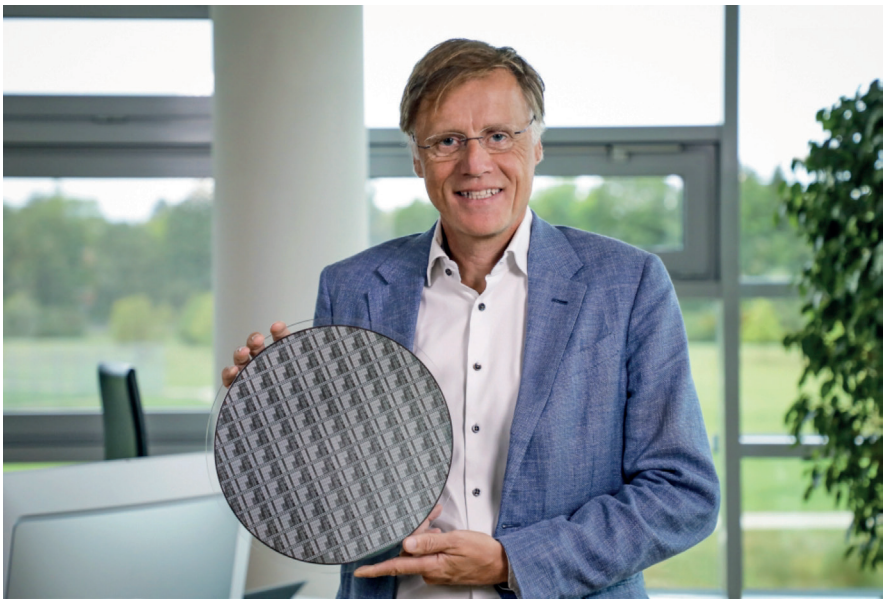
The breakthrough will help substantially drive the market for GaN-based power semiconductors. Chip production on 300 mm wafers is technologically more advanced and significantly more efficient compared to 200 mm wafers, since the bigger wafer diameter offers 2.3 times more chips per wafer.

GaN-based power semiconductors find fast adoption in industrial, automotive, and consumer, computing & communication applications, including power supplies for AI systems, solar inverters, chargers and adapters, and motor-control systems.

State-of-the art GaN manufacturing processes lead to improved device performance resulting in benefits in end customers' applications as it enables efficiency performance, smaller size, lighter weight, and lower overall cost. Furthermore, 300 mm manufacturing ensures superior customer supply stability through scalability.

"This remarkable success is the result of our innovative strength and the dedicated work of our global team to demonstrate our position as the innovation leader in GaN and power systems," said Jochen Hanebeck, CEO of Infineon Technologies AG.

"The technological breakthrough will be an industry game-changer and enable us to unlock the full potential of gallium nitride. Nearly one year after the acquisition of GaN Systems, we are demonstrating again that we are determined to be a leader in the fast-growing GaN market. As a leader in power systems, Infineon is mastering all three relevant materials: silicon, silicon carbide and gallium nitride."



Infineon has succeeded in manufacturing 300 mm GaN wafers on an integrated pilot line in existing 300 mm silicon production in its power fab in Villach (Austria). The company is leveraging well-established competence in the existing production of 300 mm silicon and 200 mm GaN.

Infineon will further scale GaN capacity aligned with market needs. 300 mm GaN manufacturing will put Infineon in a position to shape the growing GaN market which is estimated to reach several billion US-Dollars by the end of the decade.

This pioneering technological success underlines Infineon's position as a global semiconductor leader in power systems and IoT.

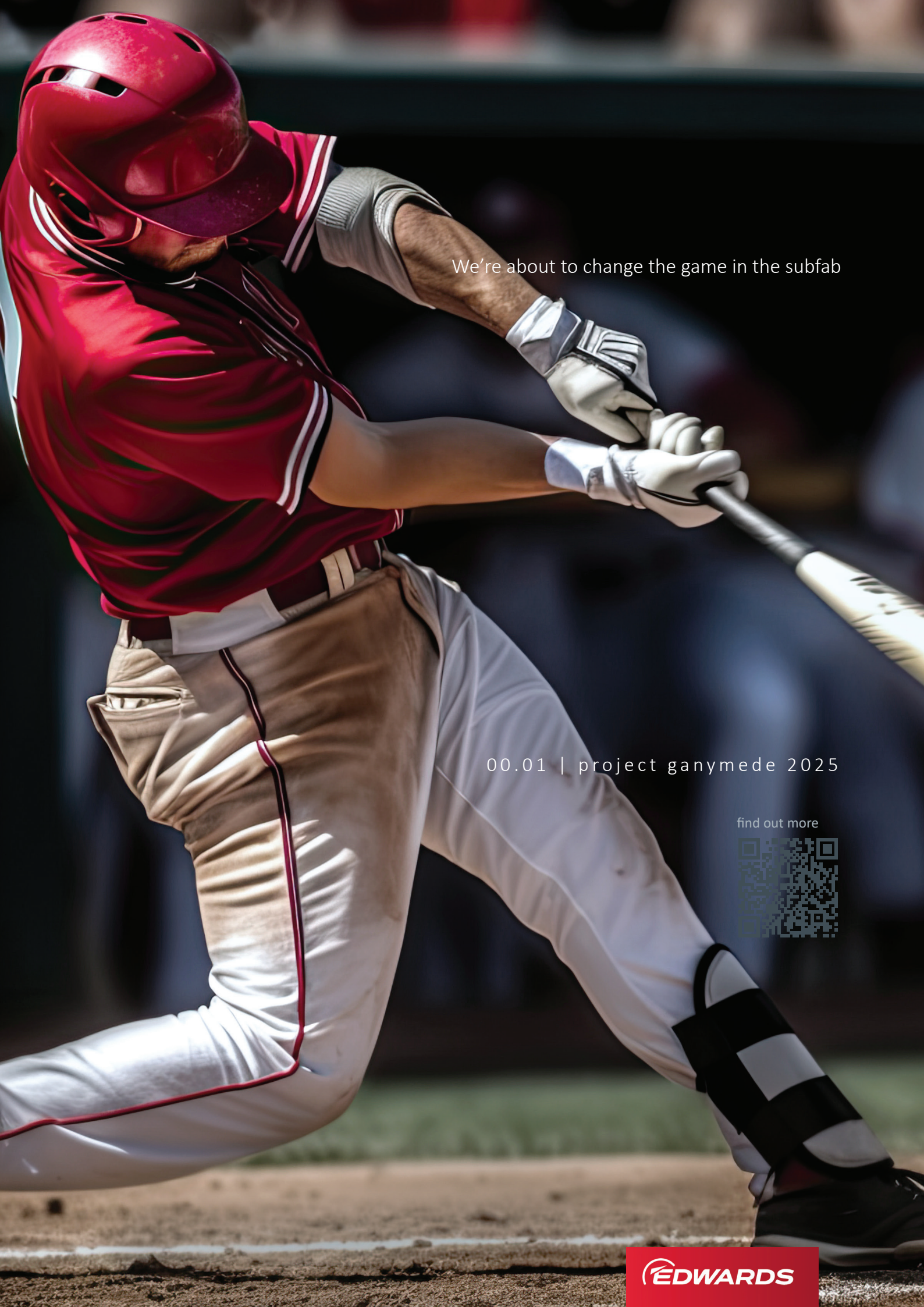
Infineon is implementing 300 mm GaN to strengthen existing and enabling new solutions and application fields with an increasingly cost-effective value proposition and the ability to address the full range of customer systems. Infineon will present the first 300 mm GaN wafers to the public at the electronica trade show in November 2024 in Munich.

A significant advantage of 300 mm GaN technology is that it can utilize existing 300 mm silicon manufacturing equipment, since gallium nitride and silicon are very similar in manufacturing processes.

Infineon's existing high-volume silicon 300 mm production lines are ideal to pilot reliable GaN technology, allowing accelerated implementation and efficient use of capital.

Fully scaled 300 mm GaN production will contribute to GaN cost parity with silicon on R DS(on) level, which means cost parity for comparable Si and GaN products.

300 mm GaN is another milestone in Infineon's strategic innovation leadership and supports Infineon's mission of decarbonisation and digitalisation.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Optogenetic OLED-on-CMOS stimulators for neurosensory therapies

Researchers from the Fraunhofer Institute for Photonic Microsystems IPMS and the Max Planck Institute for Multidisciplinary Natural Sciences (MPI-NAT) have researched optical stimulators for future cochlear implants as part of the "NeurOpto" project (funded by the Fraunhofer-Max-Planck Cooperation Program: 601001).

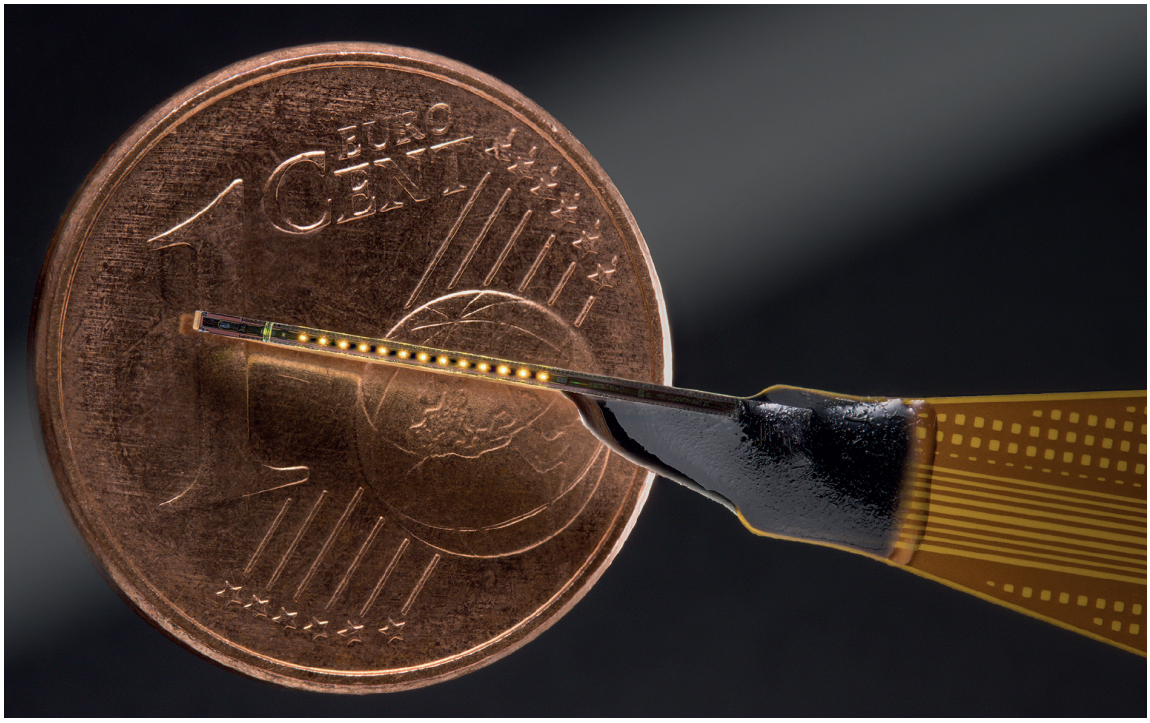
OPTOGENETICS is a method that uses light to control genetically modified cells in living tissues. By introducing light-sensitive proteins into cells, their activity can be precisely turned on and off with light pulses. This technique is commonly used in neuroscience to study the functions of nerve cells and to activate or inhibit specific neuronal populations. To deliver light precisely to stimulate tiny cells, small and locally selective light sources are therefore needed now.

Dr. Uwe Vogel, Head of business unit "Microdisplays and Sensors" at Fraunhofer IPMS, explains: "With OLED-on-silicon technology, we can bring tiny, locally controllable light pixels onto a chip. This chip can be flexibly designed to reach the desired locations even in curved structures like the cochlea. This allows light to be used precisely where electrical stimulation alone is insufficient."

Prof. Tobias Moser from MPI-NAT adds: "The development of optical cochlear implants promises better hearing for the severely hearing impaired. MPI-NAT and University Medical Center Göttingen (UMG) are working closely with partners such as Fraunhofer IPMS on the technological solutions required for this. Intelligent implantable stimulators based on optical stimulation could also be used for other medical therapies such as laryngeal pacemakers, cardiac pacemakers, pain relieve, retinal implants, or deep brain stimulation."

How does optical cell stimulation work?

Current electrical cochlear implants (eCIs) restore speech comprehension in quiet environments for most of the approximately 1 million users worldwide. However, speech recognition in background noise and enjoyment of music are often severely limited. The reason for this is the inadequate frequency resolution of electrical sound coding: each electrode contact also stimulates more distant nerve cells that code different frequencies due to the broad current spread. Since light can be controlled much more



➤ OLED-on-Silicon Technology for Optogenetics. © Fraunhofer IPMS

precisely, an optical cochlear implant (oCI) could overcome this problem. The number of independent frequency bands could be increased by spatially-targeted optical stimulation of light-sensitive auditory nerve cells (SGNs). This would be possible through dozens of microscale light emitters along the frequency axis of the cochlea, ideally individually controllable.

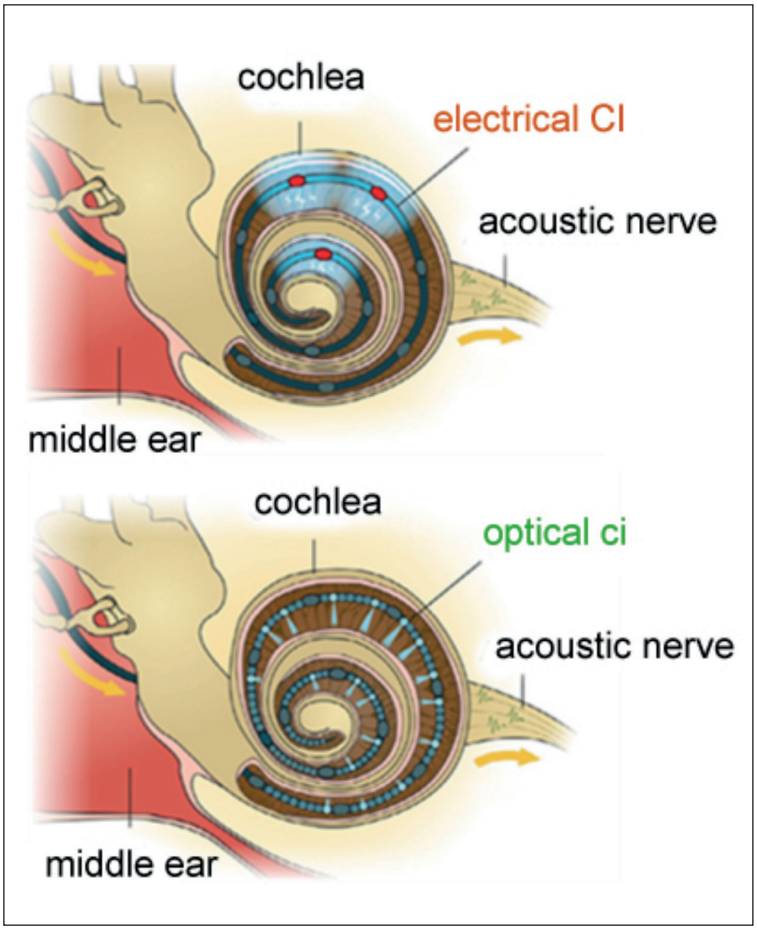
UMG/MPI-NAT have been working for many years with academic and industrial partners on the development of the oCI and gene therapy. The current collaboration with Fraunhofer IPMS focused on evaluating OLED technology for use in oCIs. Fraunhofer IPMS has leveraged its experience from OLED-on-silicon technology for microdisplays to bring CMOS-integrated light sources of the highest pixel density and brightness, as well as the lowest power consumption, to a pixelated OLED microsensor that can individually control spatially distributed light channels assignable to corresponding audio frequencies in the cochlea via a serial interface.

Where was the challenge in developing the technology?

Although Fraunhofer IPMS has already introduced unique features with its OLED-on-silicon technology for microdisplays that are also important for optogenetics, there are still some challenges: The necessary brightness and degree of integration have been successfully demonstrated during the project. However, flexibility and biocompatibility are not yet verified. The silicon microtechnology used has shown that these properties are generally achievable. With further research and development effort, they also appear feasible here.

When will the technology be market-ready?

The project laid the first foundations for the use of OLED-on-silicon technology in optogenetics. The results are promising. The scientists will continue to work on this technology and remain open to other areas of application.



➤ Electrical vs. Optical Cochlea Stimulation - Above: The current from each of the 12 electrode contacts of a conventional electrical cochlear implant spreads widely. Below: The light from nearly one hundred independent micro-light-emitting diodes of an optical cochlear implant can be projected onto a small area.

Semiconductors:

Unstoppable growth in a billion-dollar market

Both companies and governments are investing heavily in semiconductor technology to stabilise supply chains and meet demand through innovation drivers such as AI. An analysis of the market potential based on current figures.

BY PHILIPP SCHLÜTER, PARTNER M&A, PAVA PARTNERS GERMANY

THE INTERNATIONAL semiconductor industry has been at the centre of global attention during the significant supply chain disruptions between 2021 and 2022. What industry insiders have already been aware of for quite a while has now come to light: the semiconductor market is both complex and essential to the global industry.

According to analysis by IC Insights and Semiengineering.com, more than €190 billion has been invested in the semiconductor market in 2022 alone. A further USD 300 billion has been announced by leading semiconductor companies for the coming years.

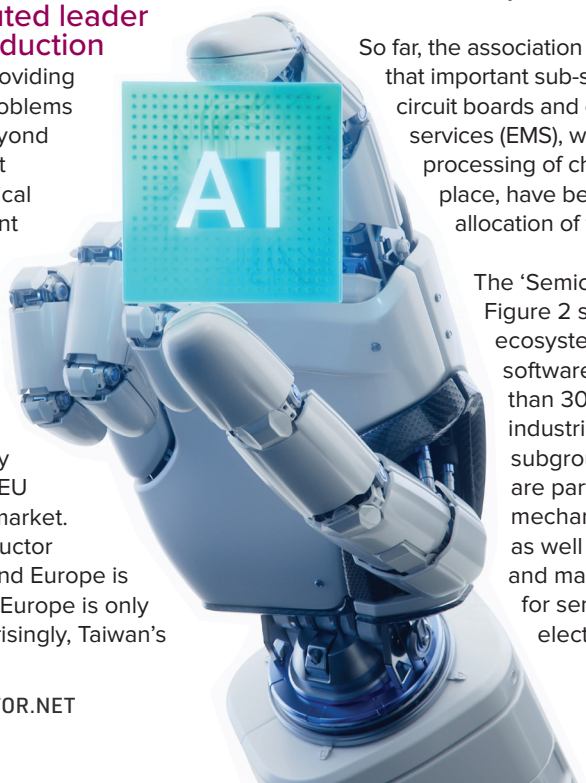
By way of comparison, this is roughly equivalent to the amount the global automotive industry plans to invest in research and development by 2028, driven in particular by the megatrends of electrification and autonomous driving.

Taiwan is the undisputed leader in semiconductor production

Government policy is also providing a boost. The supply chain problems during the pandemic and beyond have highlighted the fact that semiconductor chips are critical infrastructure. With the current shortage, politicians in Europe and the US have decided to boost local production again. As a result, billions of taxpayers' money are being pumped into establishing FABs. How badly subsidies are needed in the EU shows its positioning in the market. The world's top 10 semiconductor foundries show how far behind Europe is in chip production (Figure 1). Europe is only listed under 'others'. Unsurprisingly, Taiwan's semiconductor production is the undisputed leader. The chart from the latest Semicon Report illustrates Taiwan's immense lead.

The fact that industrial policy is now being implemented, and more subsidies are being channelled into semiconductor production, is an important sign for Europe and Germany in particular. Over the past 30 years, the region of Saxony and Saxony-Anhalt has succeeded in establishing the region as an attractive location for international players through the strategic development of production sites and expertise at universities and research centres.

An investment that has paid off, as confirmed by the international companies that have already settled in the region. However, the industry association ZVEI has criticised the fact that German funding is too selective and does not sufficiently support the entire semiconductor ecosystem.

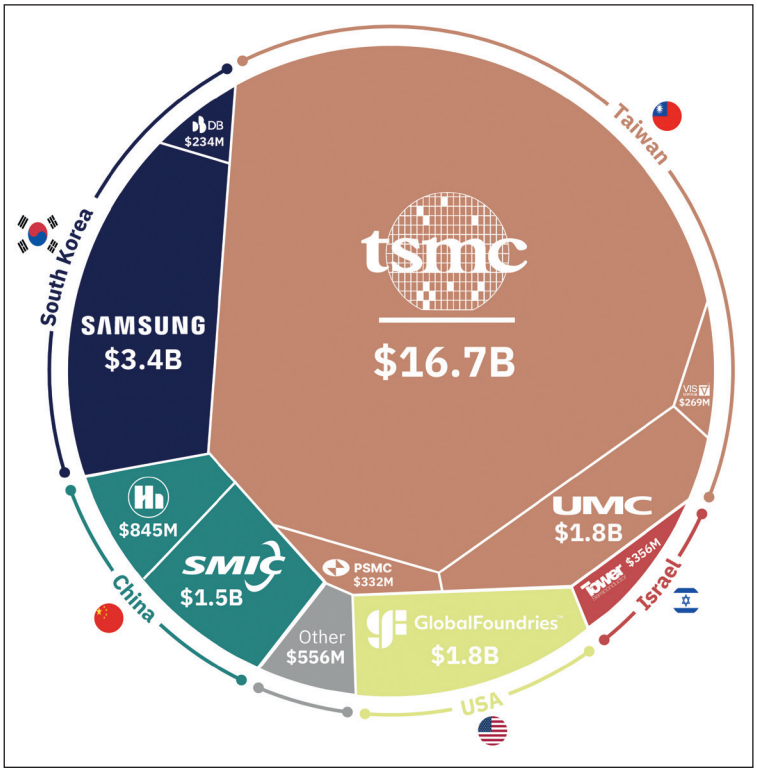


So far, the association has criticised the fact that important sub-sectors such as printed circuit boards and electronic manufacturing services (EMS), which make the further processing of chips possible in the first place, have been excluded from the allocation of funding.

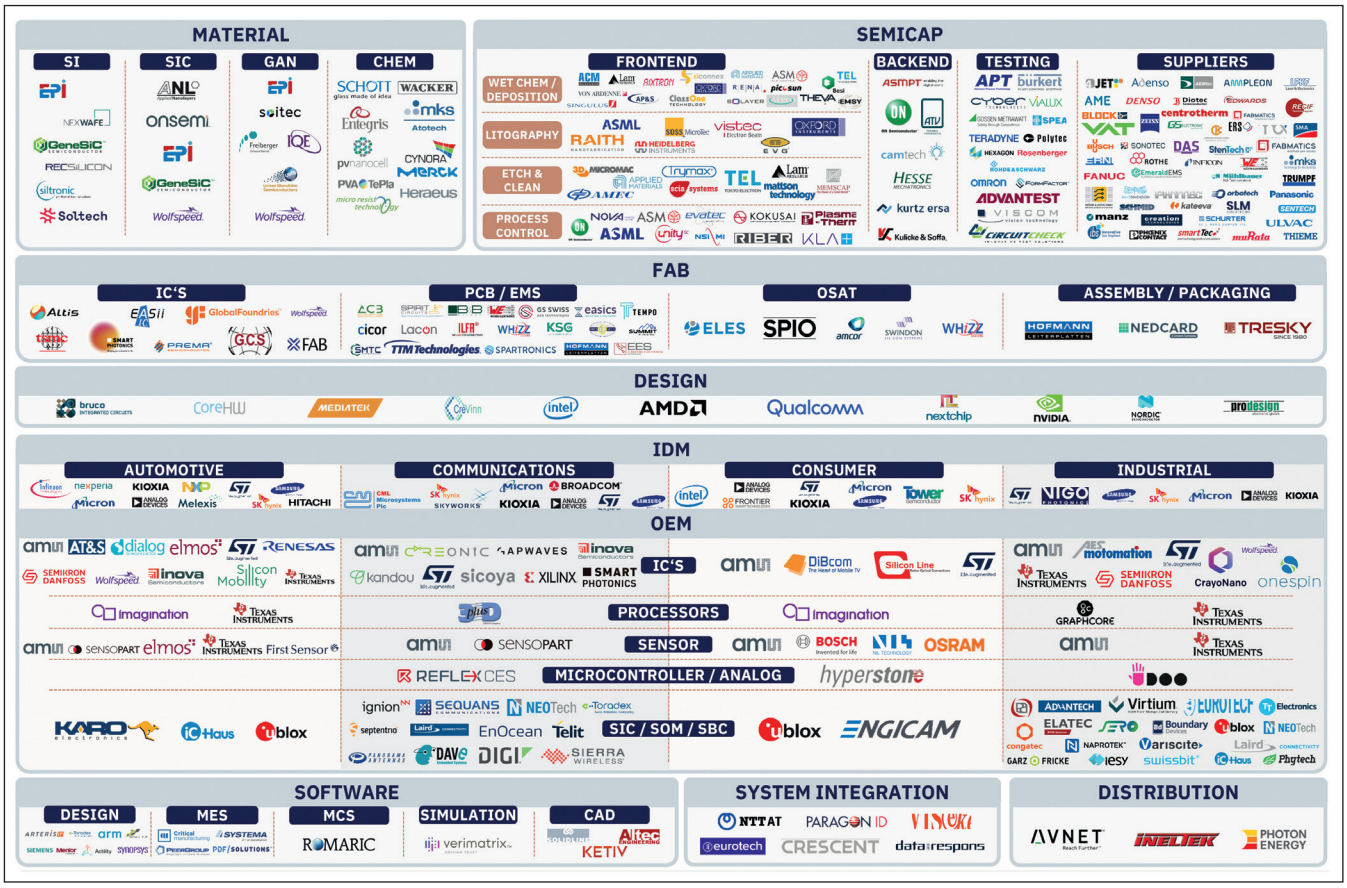
The 'Semicon Landscape' in Figure 2 shows that the entire ecosystem, from materials to software, comprises more than 300 companies in new industrial sectors with various subgroups. European suppliers are particularly strong in mechanical engineering, as well as in the design and manufacture of chips for sensors and power electronics.

Artificial intelligence drives demand for chips
However, a look at the main drivers of growth in the semiconductor industry shows that the market is set for strong growth in the future. Data storage, wireless communications and automotive electronics are the biggest growth drivers in the semiconductor industry, accounting for more than 70 percent of the sector's growth (Figure 3). In particular, the electrification of the automotive industry and advances in autonomous driving are driving growth, as is the expansion of the Internet of Things in industrial and consumer environments. The future topic of artificial intelligence, in particular Generative Artificial Intelligence (GenAI), which has achieved enormous leaps in innovation in a very short period of time, is increasing the demand for intelligent chips to an unprecedented extent. According to current analyses, the demand for logic chips for GenAI applications will increase to up to 3.6 million additional wafers (Fig. 4). Meeting this demand will require a corresponding increase in production capacity, requiring up to eight new FABs by 2030.

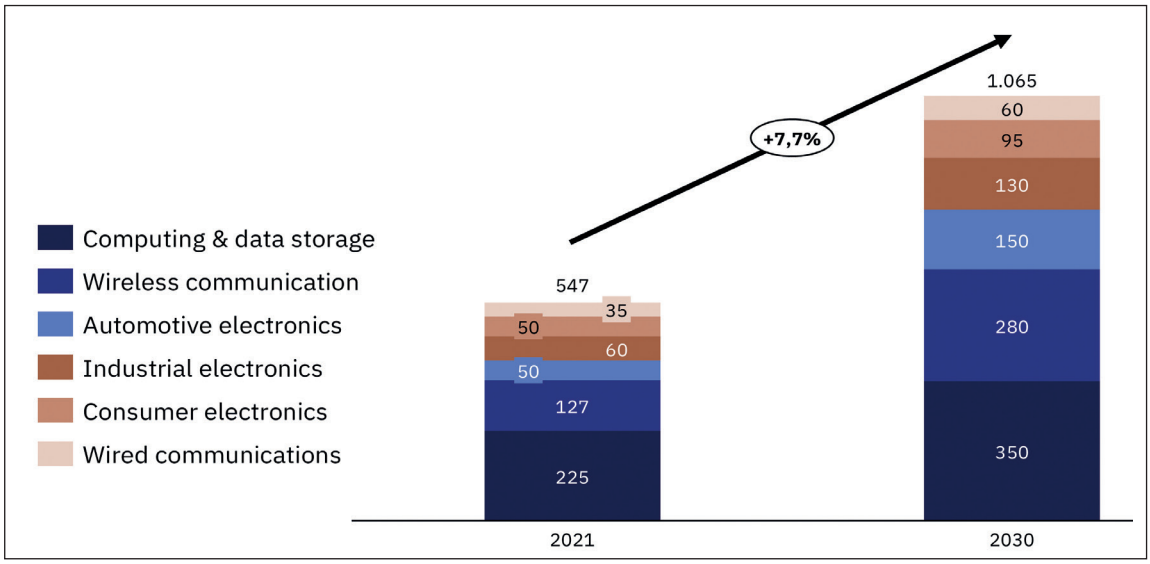
The graph in Figure 4 also clearly shows that NAND and DRAM chips in the tens of millions will be needed in the memory technology sector. This demand is primarily driven by the increasing requirements for computing power and the increasing rack density in specialised data centres as a result of the growing number of complex GenAI



➤ Figure 1. Data based on Q1 2023 revenue in USD.



➤ Figure 2.Pava's semicon landscape.



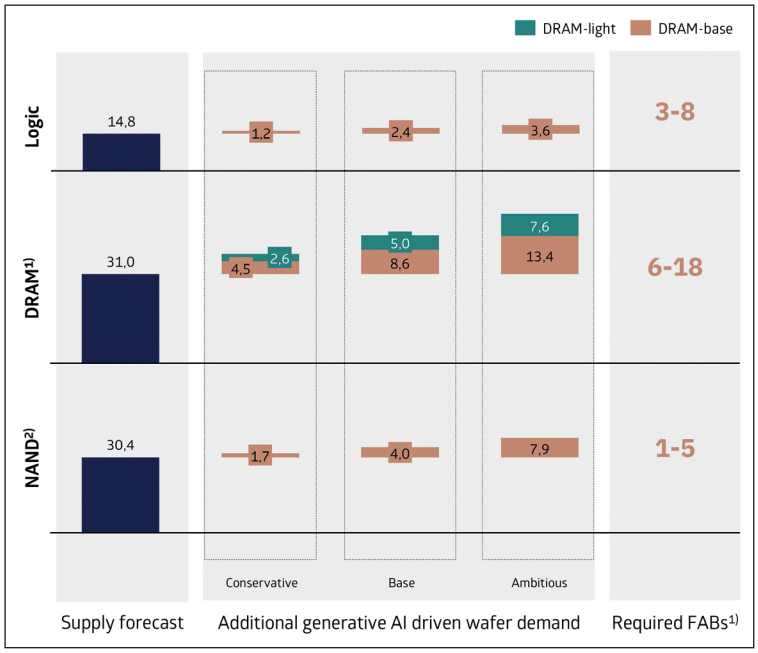
➤ Figure 3. Global growth of semicon market, in bn EUR.

applications. Manufacturers are already investing to massively increase production.

New construction and optimisation: Meeting demand

79 new FABs are currently planned by 2025 to meet growing demand. All major OEMs - from Globalfoundries, Intel and Micron to Samsung, TSMC and Texas Instruments - are planning to build highly efficient and powerful new factories.
There are currently 486 FABs worldwide, of which 289 produce 200mm wafers and 197 produce 300mm wafers. There is a strong demand for new 300mm fabs, especially from industries that require new processors, larger memories and billions of transistors. Therefore, 54 of the new FABs will produce 300mm wafers, while 25 will produce 200mm chips, specifically for silicon carbide-based semiconductors. The expansion of the new chip factories takes time, so the existing facilities are being optimised and a higher degree of automation is being introduced. Legacy Fabs optimise material flow through optimised handling, transport and storage processes. Process improvements such as these help to expand existing production capacity and meet current demand.

➤ Figure 4. order to fulfil additional wafer demand until 2030.



The semiconductor market: Growth market and outlook for Europe

The figures show a clear trend: the demand for chips will continue in the medium term. They underpin the most important technologies of our time, and government subsidies for semiconductor production are correspondingly high. In recent years, supply chain problems have shown how fragile the global ecosystem can be. Nearshoring to the US and Europe will mitigate this risk somewhat, but building a complete, complex ecosystem in a region remains a challenge. For every job at a FAB, five jobs are created at suppliers.
In the medium term, OEMs need to be able to meet demand at all. They are therefore focusing on both building new factories and optimising existing ones to increase capacity in the short term.

The rapid development of data centres for AI has not yet been taken into account in most studies and plans. The importance of the key technology of semiconductors is not likely to diminish. The market for AI chips seems to be dominated by the US and China for the time being. Time will show, if Europe will be able to play to its historical strengths in Industrial IoT. Europe is also at the forefront of quantum computing research, productizations are driven by US companies, though for the time being.

Philipp Schlüter is a partner and semiconductor expert at Pava Partners, one of Europe's leading M&A Advisory firms, where he advises companies in the semiconductor industry on sales, strategic acquisitions, financing and succession.

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SEMI Consortium to develop cybersecurity strategy and roadmap

Seeking to strengthen the semiconductor industry's resilience to cybersecurity threats, the global association SEMI is to create of a strategic roadmap for cybersecurity implementation throughout the industry.

THE SEMI Semiconductor Manufacturing Cybersecurity Consortium (SMCC) has partnered with the National Institute of Standards and Technology (NIST) to develop a semiconductor manufacturing industry profile for NIST Cybersecurity Framework 2.0 (CSF 2.0) that will serve as the foundation for the aforementioned roadmap. NIST plans to publish the profile in mid-2025.

According to research by the Identity Theft Resource Center, cyberattacks rose by 72 percentage points in 2023 over the previous all-time high in 2021. As semiconductor factories become increasingly connected and autonomous, the industry must respond to the growing security vulnerabilities associated with this next level of digital reliance and align with broader government efforts to secure the building blocks of technologies vital to society.

"Semiconductors are integral to both national security and the global economy – we need to do everything in our power to protect the industry," said Cherilyn Pascoe, Director of the National Cybersecurity Center of Excellence (NCCoE) at NIST. "NIST is pleased to partner with SEMI SMCC for the development and adoption of a NIST Cybersecurity Framework 2.0 Profile for Semiconductor Manufacturing. This collaboration is important to identify and reduce cybersecurity challenges in semiconductor manufacturing."

"It's important to recognize and address the unique cybersecurity challenges facing the semiconductor industry," said Jennifer Lynn, SMCC Working Group Chair and Semiconductor Cybersecurity Lead at IBM Research. "This community profile could allow us to better identify and execute a path forward."

In support of the 2023 National Cybersecurity Strategy's strategic objective to secure global supply chains for information, communications and operational technology products and services, the White House Office of the National Cyber Director (ONCD) included a Cybersecurity Framework Profile as part of initiative 5.5.5 in the National Cybersecurity Strategy Implementation Plan Version 2. SMCC recognized the need for a cybersecurity community profile specific to semiconductor manufacturing and worked with the federal government to develop one.

"Unlike air, space, land, and sea, cyberspace is the only battle domain created entirely by human hands," said Anjana Rajan, Assistant National Cyber Director for Technology Security at ONCD, during the Global Executive Cybersecurity Forum at SEMICON West 2024. "This means we have both the power and the responsibility to shape it. The future of cyberspace where defenders have an inherent advantage over attackers starts with preparation, and that preparation must begin with securing the building blocks."

Prior to completion, the community profile will open for public review and commentary in accordance with NIST's official process. The review period has

yet to be announced. The community profile is part of a broader NIST strategy to further standardize cybersecurity protocols for the semiconductor sector, in line with profiles for other industries. "With the committed resources and support from NIST to support SMCC working groups, we'll be able to accelerate the development of this semiconductor manufacturing industry community profile creation," said Brian Korn, Director for SMCC and Staff Technologist focused on Cybersecurity and Automation at Intel Foundry.

SMCC will provide cybersecurity recommendations for semiconductor manufacturing equipment, information on implementation, and updates on the development of the community profile. For more information, visit the project webpage or contact **cybersecurity@semi.org**

SMCC working groups are engaged with the SEMI Standards program to create a standards-based approach supporting the semiconductor ecosystem by leveraging the program's 50-year history of industry alignment. SMCC is currently working on developments to two cybersecurity standards:

- **E187:** Specification for Cybersecurity of Fab Equipment
- **E188:** Specification for Malware-Free Equipment Integration

Industry plans to invest $400 billion in 300mm fab equipment

IMAGE WEB PAGE:
https://www.semi.org/en/semi-press-releases/global-semiconductor-industry-plans-to-invest-%24400-billion-in-300mm-fab-equipment-over-next-three-years-semi-reports

Global spending on 300mm fab equipment is expected to reach a record US$400 billion from 2025 to 2027, SEMI has highlighted in its quarterly 300mm Fab Outlook Report to 2027 report. The robust spending is being driven by the regionalization of semiconductor fabs and the increasing demand for artificial intelligence (AI) chips used in data centers and edge devices.

Worldwide, 300mm fab equipment spending is projected to grow by 4% to US$99.3 billion in 2024, and further increase by 24% to US$123.2 billion in 2025, surpassing the US$100 billion level for the first time. Spending is forecast to experience 11% growth to US$136.2 billion in 2026 followed by a 3% increase to US$140.8 billion in 2027.

"The magnitude of the expected ramp of global 300mm fab equipment spending in 2025 sets the stage for a record-setting three-year period of semiconductor manufacturing investments," said Ajit Manocha, SEMI President and CEO. "The world's ubiquitous need for chips is boosting spending on equipment for both leading-edge technologies addressing AI applications and mature technologies driven by automotive and IoT applications."

Regional growth

China is projected to maintain its position as the top spending region on 300mm equipment globally until 2027, investing over US$100 billion in the next three years driven by its national self-sufficiency policies. However, spending is anticipated to gradually decrease from a peak of US$45 billion in 2024 to US$31 billion by 2027.

Korea is projected to rank second and invest US$81 billion in the next three years to further its dominance in memory segments including DRAM, high-bandwidth memory (HBM), and 3D NAND Flash. Taiwan is forecast to spend US$75 billion on 300mm equipment over the next three years, ranking third as the region's chipmakers build some new fabs overseas. Leading-edge logic below 3nm is the primary driver of Taiwan fab investments.

The Americas is projected to invest US$63 billion from 2025 to 2027, while Japan, Europe & Mideast, and SE Asia are expected to spend US$32 billion, US$27 billion, and US$13 billion, respectively, over the three-year period. Notably, these regions are anticipated to more than double their equipment investment in 2027 compared to 2024 due to policy incentives earmarked to alleviate concerns on the supply of crucial semiconductors.

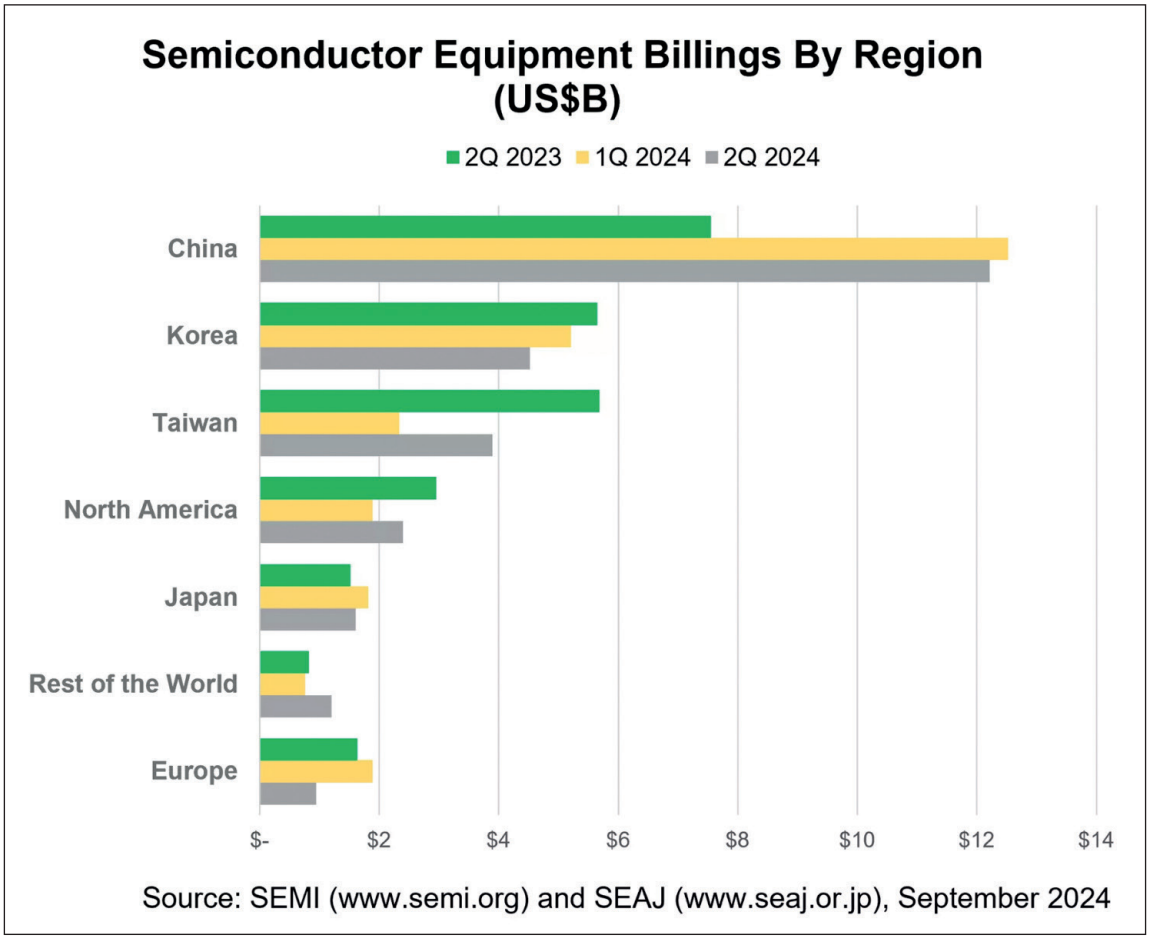
Segment growth

Foundry equipment spending is projected to reach approximately US$230 billion between 2025 and 2027, fueled by investments in sub-3nm cutting-edge nodes as well as continued spending on mature nodes. Investment in 2nm logic processes and development of key technologies at 2nm, such as gate-all-around (GAA) transistor structure and back-side power delivery technology, is crucial to meet future high-performance and energy-efficient computing needs, particularly for AI applications. Cost-effective 22nm and 28nm processes are expected to see growth due to increasing demand for automotive electronics and IoT applications.

The Logic and Micro segment is projected to spearhead the equipment spending expansion over the next three years, with an anticipated total investment of US$173 billion. Memory comes in second, expected to contribute over US$120 billion in spending during the same period, marking the beginning of another segment growth cycle.

Within Memory, investment in DRAM-related equipment is projected to surpass US$75 billion, while investment in 3D NAND is expected to reach US$45 billion.

The Power-related segment ranks third, with an expected investment of over US$30 billion over the next three years, including around US$14 billion for compound semiconductor projects. The Analog and Mixed-signal segment is projected to reach US$23 billion during the same period followed by Opto/Sensors at US$12.8 billion.



Q2 2024 equipment billings increased 4% YoY

Global semiconductor equipment billings increased 4% year-over-year to US$26.8 billion in the second quarter of 2024, while quarter-over-quarter billings edged up 1% during the same period, SEMI has published in its Worldwide Semiconductor Equipment Market Statistics (WWSEMS) Report.

"Global semiconductor equipment billings totaled $53.2 billion for the first half of 2024, reflecting a healthy year so far for the industry overall," said Ajit Manocha, SEMI President and CEO. "The semiconductor equipment market has returned to growth driven by strategic investments to support continued strong demand for advanced technologies and regions seeking to bolster their chipmaking ecosystems."

Compiled from data submitted by members of SEMI and the Semiconductor Equipment Association of Japan (SEAJ), the WWSEMS Report is a summary of the monthly billings figures for the global semiconductor equipment industry. Following are quarterly billings data in billions of U.S. dollars with quarter-over-quarter and year-over-year changes by region:

Wojciech P. Maly inducted into the Phil Kaufman Hall of Fame

Dr. Wojciech P. Maly, a pioneer in broad spectrum research in electronic system design who died in 2021, today was inducted posthumously into the Phil Kaufman Hall of Fame.

The honor, co-sponsored by the Electronic System Design (ESD) Alliance, a SEMI Technology Community, and the IEEE Council on Electronic Design Automation (CEDA), acknowledges his significant and innovative contributions to the electronic system design industry. Founded in 2021, the Phil Kaufman Hall of Fame honors deceased members of the industry who made major contributions but did not receive the Phil Kaufman Award during their lifetime.

A distinguished professor at Carnegie-Mellon University (CMU) in Pittsburgh, Penn., Dr. Maly's research interests focused on interfaces between very-large-scale integration (VLSI) design, testing and manufacturing with an emphasis on the stochastic nature of phenomena relating to these three VLSI domains. He authored, co-authored and edited numerous books, journal and conference papers, as well as patents, which have attempted to promote integration of design, test and manufacturing.

"Professor Maly was ahead of his time and demonstrated amazing creativity and out-of-the-box thinking," said Andrzej Strojwas, Chief Technology Officer at PDF Solutions, and a former student of

Dr. Maly. “Our industry is only now realizing the potential of his pioneering work especially in the area of three-dimensional ICs.”

“Dr. Maly’s name may not be as well recognized as other industry giants, but his contribution is unmistakable and valued,” said Bob Smith, executive director of the ESD Alliance. “With this honor, he is not forgotten and will remain in the annuls of the ESD industry.”

Dr. Maly received the Master of Science degree in electronic engineering from the Technical University of Warsaw, Poland, in 1970, and a Ph.D. degree from the Institute of Applied Cybernetics, Polish Academy of Sciences, also in Warsaw, in 1975.

From 1970 to 1973, he was with the Institute of Applied Cybernetics. In 1973, he joined the Technical University of Warsaw, where he was appointed Assistant Professor in 1975. From 1979 to 1981, he was a Visiting Assistant Professor of Electrical and Computer Engineering at CMU. Beginning in 1983, he was the Whitaker Professor of Electrical and Computer Engineering at CMU.

Professor Maly was the recipient and/or co-recipient of various awards. He received Carnegie Mellon’s Benjamin Richard Teare Teaching Award; AT&T Foundation Award for Excellence in Instructing Engineering Students; Eta Kappa Nu CMU Sigma Chapter Excellence in Teaching Award; and the Semiconductor Research Corporation’s 2007 Aristotle Award.

His list of awarded research accomplishments includes honors for his Ph.D. thesis from Ministry of Higher Education of Poland; SRC’s 1992 Technical Excellence Award; the Best Paper Awards from the International Test Conference in 1990 and 1997; ESREF’s 1994 Best Paper Award; the 1994 Best Paper Awards from IEEE Transaction on Semiconductor Manufacturing; and Best Paper Award from 1996 European Design and Test Conference. He was a recipient of a Fellowship from Deutsche Forschungsgemeinschaft and Humboldt Research Award.

Dr. Jason Cong to be honoured with 2024 Phil Kaufman Award

Dr. Jason Cong, Distinguished Professor and Volgenau Chair for Engineering Excellence at the University of California, Los Angeles (UCLA), will be honored with the 2024 Phil Kaufman Award for distinguished contributions to Electronic System Design (ESD).

The annual award from the Electronic System Design Alliance (ESD Alliance and the Council on Electronic Design Automation (CEDA) of the Institute of Electrical and Electronics Engineers (IEEE) will be presented at the Phil Kaufman Award presentation and banquet, November 6 in San Jose, Calif. The organizations are honoring Dr. Cong for his sustained fundamental contributions to Field-Programmable Gate Array (FPGA) design automation technology, from circuit to system levels, with widespread industrial impact.

“Dr. Jason Cong is highly regarded in the industry for his work in FPGA synthesis and interconnect optimization and is recognized as a top researcher in the field,” said Dr. Anirudh Devgan, President and CEO of Cadence Design Systems and the 2021 Phil Kaufman Award honoree. “Along with his passion for teaching and mentoring the next generation of innovators, Jason has had a significant impact on the FPGA and EDA industries.”

“Jason Cong has made sustained, seminal contributions to design automation for FPGA designs, from chips to systems, across logic, layout, compilation, and applications, over a remarkable 30-plus-year span,” said Rob Rutenbar, Senior Vice Chancellor for Research, Distinguished Professor of CS and ECE at the University of Pittsburgh, and the 2017 Phil Kaufman Award recipient. “He is an inspiring and well-accomplished educator, mentor, and role model for generations of students who became successful faculty members, co-founders of startups, and key contributors to major EDA and semiconductor companies.”

“Dr. Cong has been a key innovator and EDA educator with outstanding technical contributions in design automation for FPGA designs, including logic, layout, compilation, and applications,” said Georges Gielen, Professor at KU Leuven and past Chair of the IEEE Council on EDA Awards Committee. “He has founded numerous successful startups, and with over 30 years on the faculty of UCLA, he and his numerous Ph.D. students continue to enhance the semiconductor industry.”

“The EDA industry would not be where it is today without Dr. Cong’s fundamental contributions to design automation for FPGA design and his strong role as an educator and mentor,” said Bob Smith,

“Dr. Cong has been a key innovator and EDA educator with outstanding technical contributions in design automation for FPGA designs, including logic, layout, compilation, and applications,” said Georges Gielen, Professor at KU Leuven and past Chair of the IEEE Council on EDA Awards Committee. “He has founded numerous successful startups, and with over 30 years on the faculty of UCLA, he and his numerous Ph.D. students continue to enhance the semiconductor industry.”

Executive Director of the ESD Alliance. “On behalf of SEMI and the ESD Alliance, I congratulate Dr. Cong on being honored with the 2024 Phil Kaufman award.”

SEMI and IESA join

In a strategic move to further solidify India’s position in the global semiconductor value chain, SEMI has announced a strategic agreement with the India Electronics and Semiconductor Association (IESA), the leading industry body representing the electronics and semiconductor sectors in India. IESA will become part of the global SEMI family and represent SEMI in India. IESA will continue to use its current brand while beginning to implement SEMI’s processes and select initiatives.

This unification is set to bolster India’s ambition to become a “Semiconductor Powerhouse” by advancing its design and manufacturing ecosystem. Together, the associations will enhance domestic manufacturing in line with India’s “Make in India” initiative, support workforce development, improve global competitiveness, and foster greater technological self-reliance. Additionally, SEMI members will now have direct access to India’s growing semiconductor market, tapping into new growth opportunities.

Ajit Manocha, President and CEO, SEMI, expressed his excitement about this milestone, stating, “India holds immense potential in the semiconductor space, and many global companies are already exploring the opportunities within the country’s semiconductor industry. This partnership will help SEMI grow a strong presence in this critical emerging market and enable both organizations to identify tangible strategies that leverage our combined strengths to enhance supply chain resilience.”

Dr. Veerappan, Chairperson, and Ashok Chandak, President, IESA, emphasized the strategic significance of the partnership, saying, “This milestone is a major win for India, SEMI, and IESA. It positions India to become a global semiconductor powerhouse, accelerates economic growth, and fosters innovation. By combining our capabilities with SEMI’s global standards, network, and resources, we are fortifying India’s ambitions and attracting global partnerships and investments to scale up design, manufacturing, and production capacities.”

This agreement will also pave the way for joint policy advocacy efforts, with IESA and SEMI working closely with both Central and State governments to drive incentives for product development and manufacturing, leveraging key programs such as the Production Linked Incentive (PLI) and Design Linked Incentive (DLI) models.

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Connecting Semiconductors and Electronics

About SEMI:
SEMI connects more than 2,500 member companies and 1.3 million professionals worldwide to advance the technology and business of electronics design and manufacturing. The breadth and depth of our events, programs and services help members accelerate innovation and collaboration on the toughest challenges to growth.

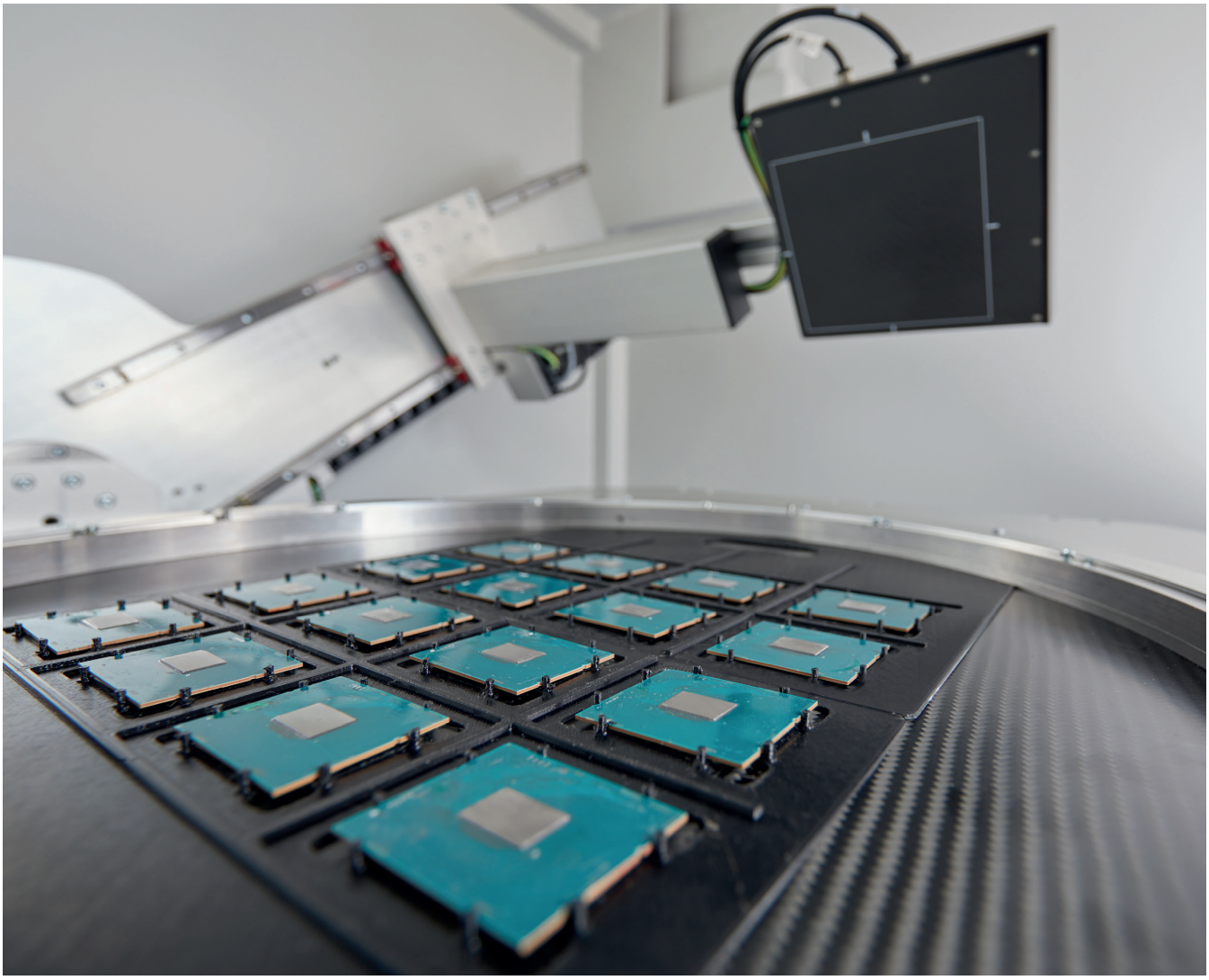
ESDA Electronic System Design Alliance

FlexTech

FOA Fab Owners Alliance

MEMS & SENSORS INDUSTRY GROUP®

SOI Industry Consortium



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As 3D IC packaging becomes ever more intricate and demanding, traditional inspection techniques are struggling to keep up. 3D X-ray inspection, powered by AI, is transforming how manufacturers view their products, offering a higher resolution without sacrificing speed or damaging valuable samples.

BY JOSCHA MALIN, DIRECTOR PRODUCT MARKETING SOFTWARE SOLUTIONS, COMET YXLON

AS THE DEMAND for miniaturization grows, semiconductor packaging design is rapidly evolving. Manufacturers are now incorporating 2.5D and 3D ICs into their production, pushing the boundaries of functionality within increasingly compact volumes. This shift brings new challenges, not only in designing robust initial prototypes but also in managing the higher manufacturing and material costs associated with more complex structures. To maintain a competitive edge, manufacturers must adopt comprehensive inspection strategies that help increase yield and accelerate time-to-market without compromising on reliability.

Crucial to the success of these inspection strategies is the ability to detect defects early within the design and manufacturing process. The sooner manufacturers can identify and resolve issues, the faster they can scale up production, ultimately leading to improved yield and a faster path to

market success. This is where advanced inspection technologies, particularly 3D X-ray inspection, come into play.

Bridging the Gap with 3D X-Ray Inspection

Historically, inspection methods for 3D ICs have relied on three primary technologies: optical inspection, 2D X-ray, and focused ion beam scanning electron microscopy (FIB-SEM). Each technology brings its own strengths and weaknesses. Optical inspection offers speed and repeatability but lacks the level of detail necessary for comprehensive 3D analysis. FIB-SEM provides unmatched resolution, but it's a slow, destructive process. Meanwhile, 2D X-ray falls in between—offering non-destructive insight but often lacking the speed or resolution required for today's complex 3D IC structures. 3D X-ray inspection fills the gap between these technologies, delivering detailed, non-destructive insights in a fraction of the time required for a FIB-SEM analysis. What's driving its rise now, especially for advanced semiconductor packaging, isn't just the improvement in X-ray hardware, but the breakthroughs in software and AI that support it.

As 3D IC packaging becomes ever more intricate and demanding, traditional inspection techniques are struggling to keep up. 3D X-ray inspection, powered by AI, is transforming how manufacturers view their products, offering a higher resolution without sacrificing speed or damaging valuable samples. By harnessing AI-driven image analysis, 3D X-ray technology can detect even the smallest defects, like voids or misalignments, with incredible precision. These systems use advanced reconstruction algorithms and data segmentation techniques to reveal fine details inside complex structures. AI further accelerates this process, providing insights at a scale and speed that were previously unattainable, ultimately boosting yield and quality.

The Three Pillars of Effective Inspection: Clarity, Efficiency, and Insight

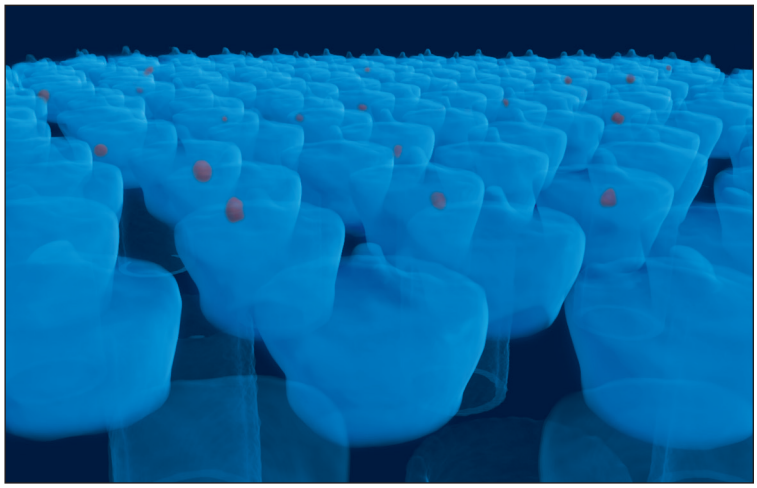
For any inspection technology to be successful, it must excel in three key areas, all heavily dependent on software:

- **Clarity:** This refers to the quality of the captured image, particularly how well the technology can visualize small details within complex structures. In the case of 3D X-ray, the combination of high-quality hardware and advanced reconstruction algorithms ensures exceptional image clarity, making even minute defects visible.
- **Efficiency:** Automation plays a vital role here. The ability to quickly gather and process images into usable data can significantly reduce inspection times and improve throughput. AI enhances this by automating much of the defect recognition process, allowing operators to focus on critical decision-making rather than manual inspection.
- **Insight:** Beyond what is visible to the eye, the real value lies in the data derived from the images. Advanced software can interpret this data to provide actionable insights, allowing manufacturers to make informed decisions. For instance, defects such as voids in solder bumps or "head-in-pillow" issues can be precisely measured and categorized, offering clear guidance on whether they fall within acceptable parameters.

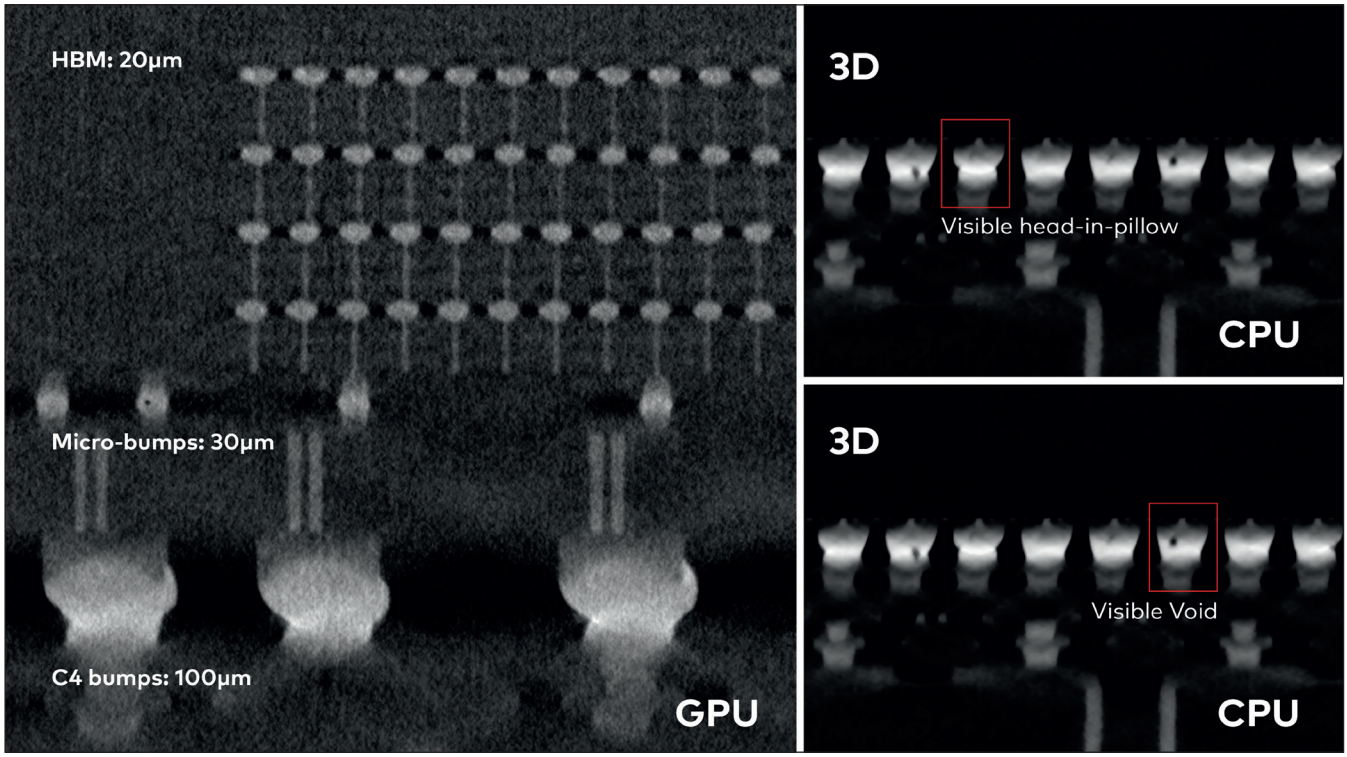
The below scan of a commercially available CPU (figure. 1), captured with Comet Yxlon's CA20 inspection solution, highlights what is already possible with today's technology, revealing detailed information about C4 bumps, including defects such as voids of only 10 microns in diameter. These scans take just minutes, highlighting the speed and precision of modern 3D X-ray technology

In another example, a "virtual slice" is taken from a reconstructed 3D volume of a GPU, allowing users to view 2D cross-sections of different layers within the chip, including C4 bumps, interposer bumps, and high-bandwidth memory (HBM) bumps (figure 2). This type of detail would be highly challenging to obtain with optical inspection or 2D X-ray due to the stacked nature of the layers obscuring underlying features.

While capturing high-resolution images is critical, the true power of 3D X-ray lies in the AI-powered software behind it. Assisted defect-recognition software such as Comet Yxlon's CoS Insights package can rapidly detect and analyze the size and severity of defects, such as solder bump misalignments, and head-in-pillow issues. By measuring key parameters, like bump shift, die tilt, and the likelihood of defects forming, this technology provides a comprehensive understanding of the part's condition, allowing manufacturers to spot these defects early and prevent costly issues down the line.



➤ Figure 1: A close up rendering of C4 bumps (diameter: 65µm) within a commercially available CPU. All image property rights remain with Comet Yxlon and images are not to be copied or distributed.



➤ Figure 2: Left, virtual slice of a reconstructed X-ray scan of a commercially available GPU with 100µm C4 bumps, 30µm microbumps and 20µm high bandwidth memory bumps. Right, virtual slice of a reconstructed X-ray scan of a commercially available CPU with ca 65µm C4 bumps. All image property rights remain with Comet Yxlon and images are not to be copied or distributed.

Insights: Taking stock of what's within

Even early in the ramp-up process, where initial designs are being manually tested in small batches to a late stage before entering mass production, assisted defect recognition can be a valuable asset, providing repeatable, transferable results based on captured data.

As with any software to be used within an industrial context, the focus lies in delivering critical information as efficiently and as clearly as possible, to ensure a variety of experts across different levels can maximize the value of the solution and understand the results. Comet Yxlon have worked closely with Dragonfly, Comet's AI brand with roots in Montreal, Canada, to develop a range of software-assisted workflows within the semiconductor space that utilize deep learning to streamline inspection workflows. Training the bump inspection within the software takes just four simple steps:

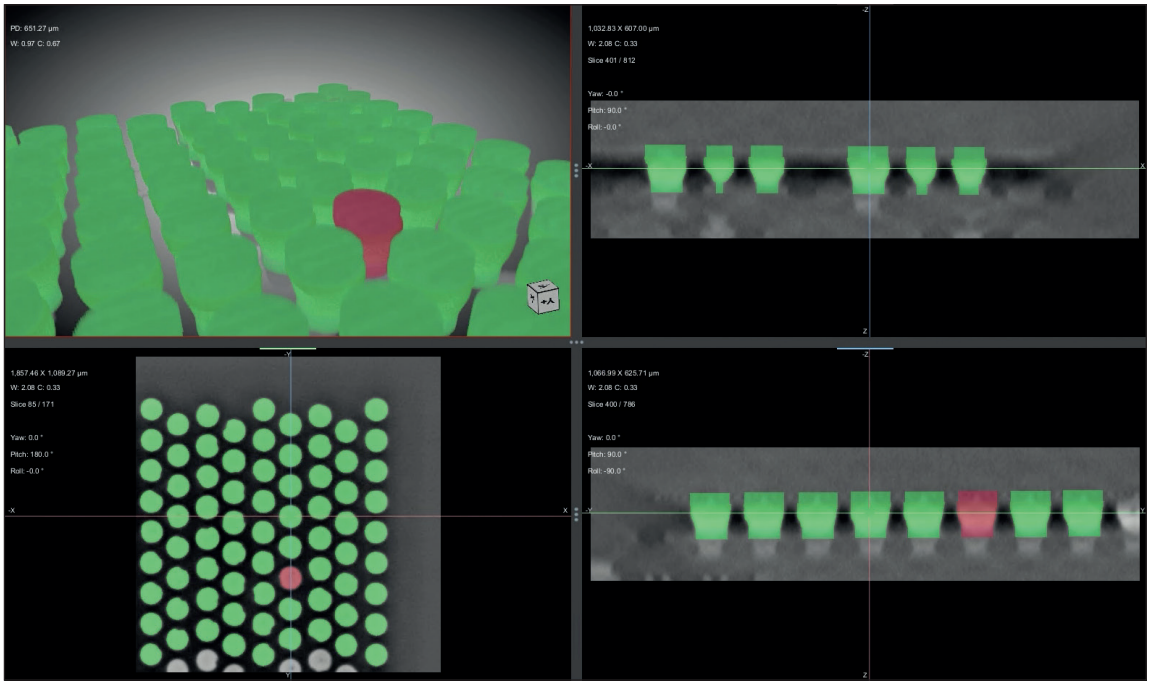
- **Step 1:** The user chooses the desired solder plane for analysis. The software can suggest which solder planes might be of interest based on previous data and adapts to previously set preferences.
- **Step 2:** The software is trained to recognize the bumps within the chosen sample. After manually defining the first few examples, the software will then analyze the entire sample and find all relevant bumps within the defined parameters.
- **Step 3:** As with step 2, the software first needs to be told the parameters it is working with to find the connection to a substrate or interposer die. Once defined, it will identify these connections automatically.
- **Step 4:** Once the parameters have been defined, the results are provided as a report, and in a machine-readable format.

This set-up, of just a few minutes, only needs to be defined once for a particular batch/part type.
The outcome of this process is shown in figure 3. In this image, taken from the software, the segmentation of a particular plane is shown, with green and red indicators used to visualize the performance of each bump within pre-defined limits. This particular example is the result of the shift and tilt and head-in-pillow evaluation, where it is clearly visible that all bumps have shifted slightly, with the bump shown in red exceeding the given limits for maximum shift.

To determine this shift, the software precisely evaluates every recognizable bump across several key metrics, analyzing the direction and the length of the shift. To determine die tilt, the stand-off height is measured, and for the head-in-pillow, an indicator is provided for the likelihood within each bump. These values, if used correctly, can be vital for identifying trends even before actual head-in-pillow defects appear.

Optimizing New Product Introductions (NPI) with 3D X-Ray

Alongside providing value in the lab, a thorough inspection strategy that includes 3D X-ray can



➤ Figure 3: Bumps automatically inspected by CoS Insights including a bump highlighted due to the violation of maximum shift allowed. All image property rights remain with Comet Yxlon and images are not to be copied or distributed.

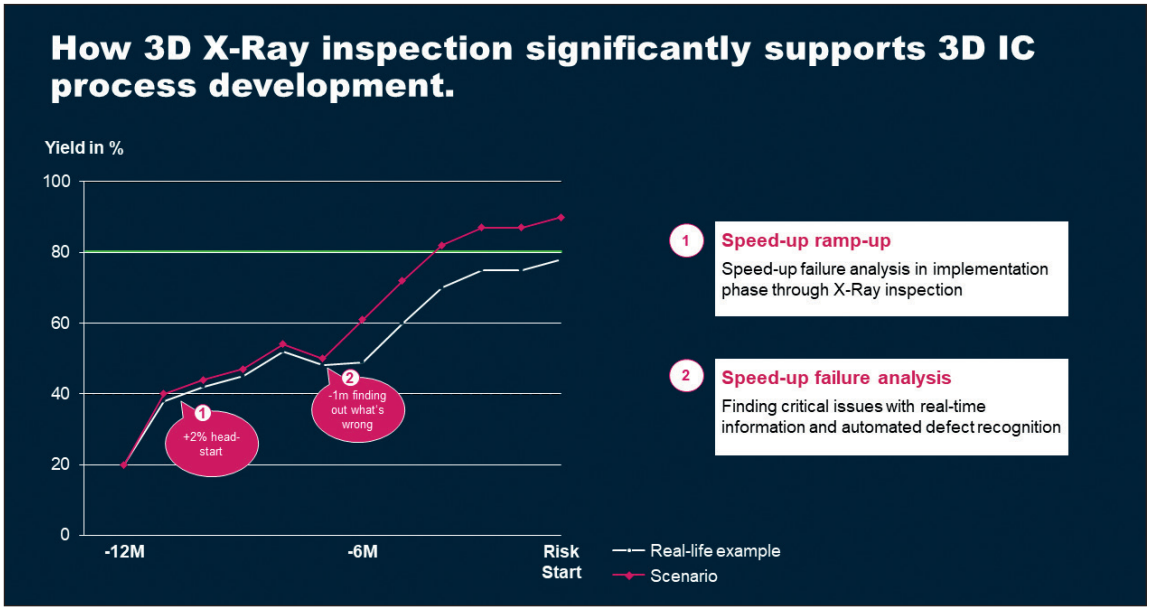
lead to significant yield improvements during the new product introduction phase. By detecting and addressing defects early in the ramp-up process, manufacturers can rapidly optimize their production line and achieve higher yields. In the hypothetical scenario shown below (Figure 4.), incorporating 3D X-ray into the inspection process resulted in a noticeable improvement in yield within just six months.

A dip in the yield curve can be seen around month 5, representing a major production issue. 3D X-ray technology can be beneficial in helping to speed up learnings from this expected setback, providing real-time monitoring across the production samples and sharing key information regarding their performance, helping identify the early signs of a developing trend before it becomes a problem.

Key Takeaways

3D X-ray inspection, especially when combined with AI-driven software, is revolutionizing semiconductor manufacturing. From early design and prototyping to mass production, this technology provides critical insights into defects that were previously difficult or impossible to detect. By integrating 3D X-ray into their inspection strategies, manufacturers can improve yield, reduce time-to-market, and ensure higher reliability in their products. This powerful combination of hardware and software, in this case Comet Yxlon and Dragonfly, is not just a tool for today but a key enabler for the future of semiconductor production.

Eager to discover more? Then join us in Munich at the SEMICON EUROPA 2024, in hall C2, Booth: 555.



➤ Figure 4: A real-life yield curve and hypothesized gains using 3D X-ray inspection. All image property rights remain with Comet Yxlon and images are not to be copied or distributed.

Bringing tomorrow's photonics to life with fully automated photonic wire bonding and facet-attached micro-lenses

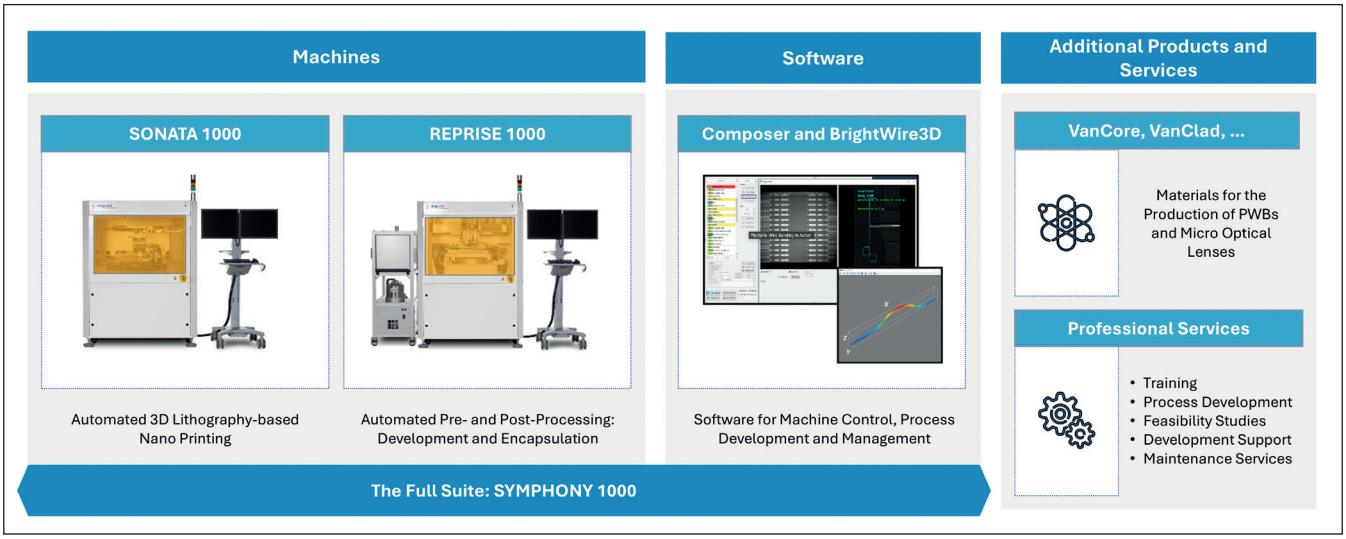
Vanguard Automation is enabling a bright future for photonic packaging and integration with scalable industry-ready 3D nano-printing solutions.

BY LAURA HORAN AND THORSTEN MAYER FROM VANGUARD AUTOMATION GMBH

OUR TECHNOLOGY DRIVEN world of AI (Artificial Intelligence), cloud computing and 5G networks is demanding more data at even greater speeds. Manufacturers are looking for new ways to produce products that are more efficient, compact and offer new functionalities. In the light of these demands the limitations of traditional electronics become very apparent. Photonic integration will be the game-changer to develop and scale the technologies of tomorrow.

The new role photonics shall play in the semiconductor market promises a paradigm shift offering the potential for significantly higher data transmission rates, reduced power consumption and increased density of component integration. While traditional photonics solutions have been bulky, expensive and required complex alignment and integration processes, ongoing innovations in integrated photonics are driving a significant reduction in size and are paving the way for their integration into various advanced technologies and everyday devices. However, overcoming scalability and production yields remain a limiting challenge.

Advanced manufacturing methods are needed to unlock the potential of integrated photonics for next generation optical devices.



➤ Figure 1: Vanguard Symphony, Vanguard Automation's fully automated photonic integration and packaging solution comprising of the automated 3D lithography based nano fabrication unit Sonata 1000 and the automated pre- and postprocessing unit Reprise 1000. The systems are equipped with Vanguard's BrightWire3D software enabling highly precise detection and on-the-fly trajectory calculations. Vanguard's own photoresists (vanguard VanCore series), standard process development, as well as product support and engineering services complete Vanguard's solution from prototyping to high-volume production.

➤ Figure 2: List of Vanguard Automation's technology users and ecosystem partners which can be disclosed at the time of publication.

Packaging of photonic devices is one key hurdle to overcome. Costs can soar to 80% of the final product price, representing a significant cost barrier to manufacturing.

At Vanguard Automation we believe that we hold the key to solving many of these issues by simplifying and automating the manufacturing process for photonic integration. Headquartered in Karlsruhe, Germany, Vanguard Automation develops unique process technology based upon 3D nano-printing technology. Now a part of Mycronic, a global supplier of high precision manufacturing tools for the electronics industry based in Sweden, Vanguard Automation are uniquely positioned to deliver advanced manufacturing tools that are enabling the innovation and scalability needed to unlock the full potential of photonic technologies.

Today's challenges, tomorrow's solutions

The future of high-performance, energy-efficient devices lies in photonic technologies. By leveraging photonic integrated circuits and optical components, product developers have achieved breakthroughs in data transmission speed, energy efficiency, power consumption, and device miniaturization. However, the industry is facing technical and commercial challenges, and one of these challenges is photonic integration and packaging. Current packaging technologies struggle to seamlessly integrate arrays of photonic components, creating a major barrier for wider adoption in product development.

Today's incumbent solutions use active alignment techniques. While this is suitable for single channel integration, scaling to the complex high-density 1D and 2D optical channel arrays demanded by the industry at high volumes is proving challenging. The challenges arise from the necessity to integrate various optical components from different material platforms, while ensuring efficient light coupling and signal transmission.

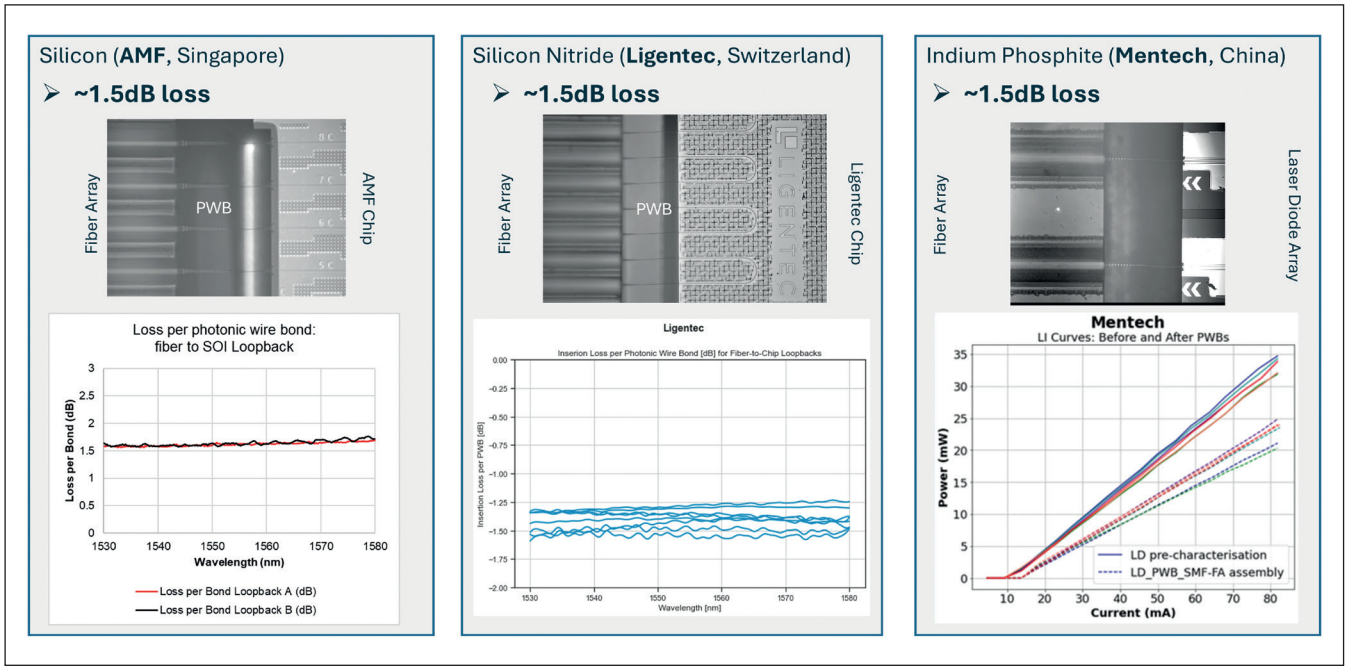
Optical modules can consist of active devices, such as indium phosphite lasers, passive devices made from silicon, silicon nitride, or lithium niobate, as well as single mode or polarization maintaining fiber arrays. This imposes an integration challenge due to the very specific optical properties of each component. Packaging or integration solutions which are viable for industrial mass production must solve challenges arising from these specific optical properties.

Additionally, to reduce coupling loss when combining different photonic devices, the specific mode field profiles must be matched, and the devices must be aligned very precisely. In industrial mass production, processes such as mode matching and alignment must be fast and reproducible since speed and yield determine the cost of the product. Additionally, the packaged assemblies need to be reliable under various environmental conditions which are specific to their field of application.

Furthermore, the mode field sizes are in the order of microns, pushing the alignment accuracy requirements for each component to less than one (1) micron. This complexity results in higher manufacturing costs for photonic devices (in comparison to traditional electronics) and lower yields. Tomorrow's solutions need a vastly different approach. By embracing simplified passive alignment procedures, machine vision and additive manufacturing techniques, mass production and packaging of high-density integrated photonic devices shall become viable.

Vanguard Automation's solution: Passive alignment & 3D nano-printing

Vanguard Automation solves these photonic integration challenges by simplifying the connectivity of integrated photonics using additive manufacturing via 3D nano-printing and passive alignment. The technique relies on highly precise direct-write 3D laser lithography to print 3D freeform single-mode waveguides called Photonic Wire



➢ Figure 3: Examples of photonic wire bonds demonstrating low loss connectivity solutions for active and passive devices from various foundries. (left) AMF (Si) chip with 1.5dB loss and (center) Ligentec (SiN) chip with 1.5dB loss per Photonic Wire Bond. (right) Mentech (InP) laser diode array with 1.5dB loss per Photonic Wire Bond.

Bonds to passively assembled photonic devices. Built on advanced 3D nano-printing technology, Photonic Wire Bonding is an inherently fully automated process and provides a high degree of design flexibility. Additionally, 3D nano-printing has been used for several years to fabricate facet-attached micro-lenses on optical chips and fibers, enabling low-loss coupling with relaxed alignment tolerances and wafer-level probing of optical devices. With both Photonic Wire Bonding and facet-attached micro-lenses in their technology portfolio, Vanguard Automation's mission is to advance photonic packaging and assembly by providing scalable 3D nano-fabrication solutions, allowing seamless transitions from prototyping to volume production.

Vanguard Automation offers a fully automated solution, the vanguard SYMPHONY comprising of two systems, one for the fabrication of Photonic Wire Bonds as well as facet-attached micro-lenses (vanguard SONATA 1000), and one for postprocessing of optical assemblies completing the fully automated packaging process (vanguard REPRISE 1000).

Vanguard's SYMPHONY includes Vanguard's Brightwire3D software for automated, highly precise interface detection (accuracy < 50 nm) as well as on-the-fly calculation of optimal Photonic Wire Bonding trajectories, dedicated photoresists tailored to meet strict industrial reliability requirements (vanguard VanCore series), standard fabrication processes as well as engineering service and support to enable customers to advance quickly from prototyping to production (see Figure 1).

Early adopters are qualifying Vanguard's solution

Over recent years, the number of adopters of Vanguard's technology has rapidly increased. This also gave rise to an eco-system of companies which provide services on Vanguard's 3D nano-printing solution (see Figure 2). Our customers and partners have successfully used Vanguard's Photonic Wire Bonding and facet-attached micro-lens technology in many applications solving the various challenges of hybrid module packaging and integration.

In the data center, telecommunication, and artificial intelligence markets, innovative Photonic Wire Bonding processes have been utilized by Vanguard's users [1] working on various material platforms, such as silicon, silicon nitride, indium phosphite, and lithium niobate to advance the concept of hybrid integration [1] (see Figure 3). Offering the unique advantage of using only one coupling PDK to couple to other types of optical components, Vanguard's technology portfolio is compatible with all academic and commercial foundries.

Consequently, foundries can be relieved from the burden of creating complex spot size converters [2]. Since the Vanguard technology can work with simple inverse tapered edge couplers realized by stepper lithography, the chip real estate used for sophisticated couplers can be reduced substantially, paving the way towards a novel and more universal standard for optical coupling. Photonic Wire Bonding has been utilized for self-injection-locked Kerr soliton microcombs and lasers with sub-100Hz linewidth [3, 4]. In the field of quantum applications,

Photonic Wire Bonding has been successfully tested in ultra-low temperature experiments [5]. Furthermore, Vanguard Automation's facet-attached micro-optical elements technology has demonstrated improved efficiencies for High-Bandwidth Coherent Driver Modulators (HB-CDM) [2]. Vanguard's dedicated photoresists series VanCore, tailored to meet strict industrial Telcordia reliability requirements, is proven to be reliable under the harshest environmental conditions [2] (see Figure 4).

The facet-attached micro-lenses have created a powerful platform for electro-optical engines to build transceivers, co-packaged optics, light engines, and sensing devices [6]. Incorporating Vanguard's technology improves the coupling efficiency of light as it passes from one photonic device to another, which in turn reduces the power consumption of the combined solution (see Figures 3 & 4).

The precise alignment and printing of the facet-attached micro-lenses at the wafer-level enables significant scalability and enhances the ability to address new applications [6, 7, 8, 9]. Vanguard's facet-attached micro-lens technology was successfully utilized in LiDAR applications for beam shaping elements [10] and in quantum applications to increase the effective collection area of superconducting nanowire single-photon detectors (SNSPD), thereby overcoming a fundamental design conflict of such devices [11].

A scalable path to integrate 3D lithography into the production chain

Due to its complementary technology portfolio comprising Photonic Wire Bonding and facet-attached micro-lenses, Vanguard Automation offers volume production customers a simplified path for incorporating the Vanguard technology into their production chain (see Figure 5). In a first step, Vanguard technology can be included in hybrid approaches together with conventional technologies such as active alignment [2] to improve coupling efficiencies and yield.

The facet-attached micro-lenses have created a powerful platform for electro-optical engines to build transceivers, co-packaged optics, light engines, and sensing devices. Incorporating Vanguard's technology improves the coupling efficiency of light as it passes from one photonic device to another

This approach does not imply any major changes to the chain of process steps in production. In a second step, beam-expanding micro-lenses can be implemented in products to ease the positioning tolerance of PICs (Photonic Integrated Circuits) and other optical components such as InP-lasers and fibers, thus relaxing alignment tolerances to such a degree that passive assembly becomes a viable process [9].

Finally, the full disruptive potential for photonic integration and packaging can be introduced by incorporating Photonic Wire Bonding into the product design, thus moving to standard pick and placing of all components of a hybrid multi-chip assembly with very relaxed placement tolerances while simultaneously ensuring high coupling efficiency, high yields as well as fast manufacturing and high package density [12].

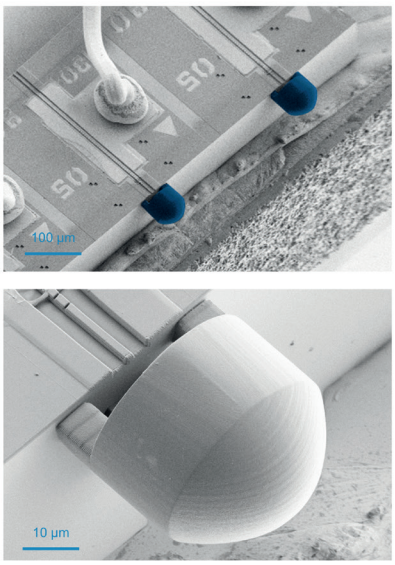
Compatible components
- Laser (DFB and other)
- PIN and APD diodes
- SMF, PMF and MMF fiber arrays
- PIC: SOI, SiN, InP, LiNb and more

Standard building blocks:
- Lenses with focal length up to centimeters and mode-field diameters of 2.0 µm to 100 µm (@1/e^2 intensity)
- Total-internal-reflection mirrors
- 3D-printed mode-size converter

Coupling, depending on laser and chip
- Laser-to-Chip: 0.6 to 2.5 dB
- Chip-to-Fiber: 1.5 to 2.5 dB

Alignment tolerances @ 1 dB penalty:
- ±1.5 µm (single lens on one component) to ±15 µm (beam expander)

Tested operational range
- 530 nm to 2000 nm



Reproducibility
- Below σ = 0.2 dB coupling variation
- Below 10% mode-field and focus length variation/deviation

Accuracy
- Below σ = 50 nm detection accuracy
- Below ±100 nm shape accuracy
- Less than 10 nm RMS-roughness

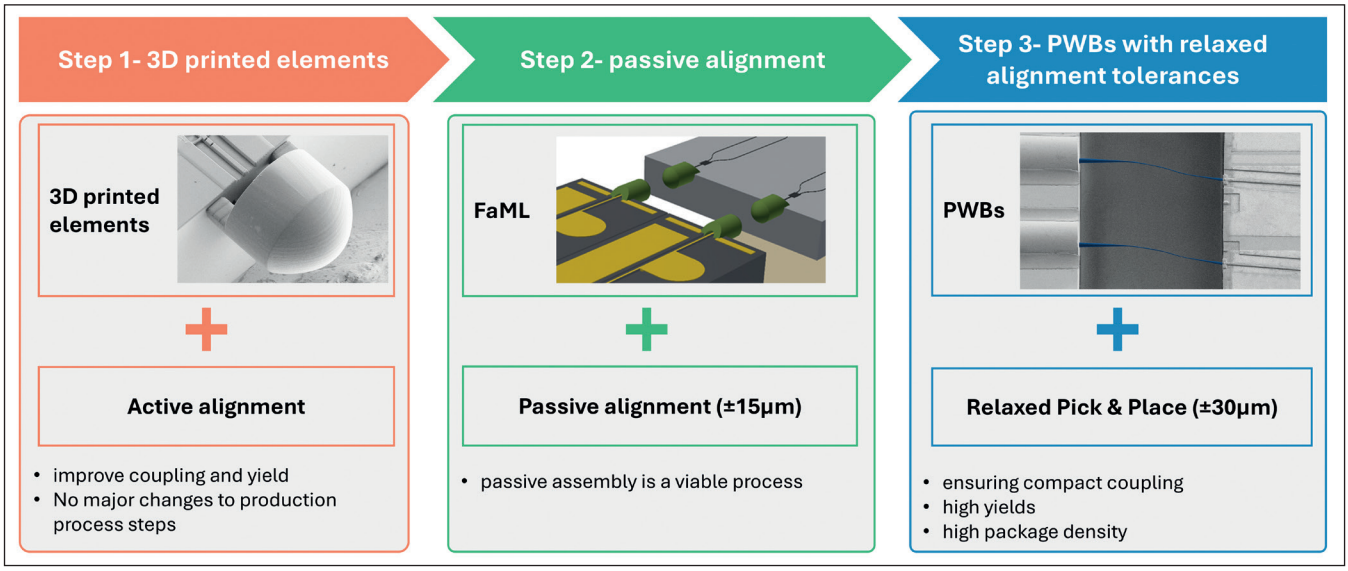
Reliability testing
- > 4000 h 85°C/85% rel. hum
- > 250 cycles -40°C to 85°C
- Reflow soldering, 3 cycles, 270°C
- Die bonding, 310°C

Shock testing
- Acceleration of up to 1500 g
- Vibration, 20g, all axis

High power operation
- >1 W @ 1550 nm

Cryogenic operation
- > 10 cycles 4K to room temperature

➤ Figure 4: Vanguard Automation's industrial grade facet-attached micro-lens technology compatible with a large variety of applications and widely tested under industry standards.



➤ Figure 5: Vanguard Automation's path to implement photonic integration into the production chain using 3D lithography.

Unlocking the benefits of throughput, cost and yield

Photonic integration offers significant benefits for the industry, but with current manufacturing methods there is a trade-off between throughput and cost. Many photonic integration approaches rely on established technologies like active alignment. These methods work well for single-channel devices, however they can lead to bottlenecks in production and higher costs per device when dealing with complex, high-density arrays. For example, attaching a single fiber is relatively straightforward, however, scaling to eight fiber channels and more significantly increases complexity. Traditional techniques often struggle with this complexity, leading to a drop in yield. Consider a high-performance system with eight data channels, each transmitting at 100 Gbps

(Gigabits per second). These data channels connect to expensive components like laser bars, which can have 4 or more channels. As the number of channels grows, and photonic integration density increases, achieving high yield becomes critical.

This is especially important because photonic components, like lasers, can be costly. In this scenario, yield issues can become the primary reason for discarding expensive components, significantly impacting production costs.

Leveraging passive alignment and 3D nano-printing holds the key to achieving a breakthrough in photonic integration of multi-channel devices - enabling production of complex devices with higher yields and lower costs. This solution will ultimately pave the way for wider adoption of photonic devices across various industries and is a technology that Vanguard Automation and their users have already shown to work for a variety of different integration and packaging challenges [2, 12].

Leveraging 3D nano-printing of optical components for integration and photonic packaging can offer faster turnaround times and eliminate the need for costly traditional tooling. Unlike traditional volume manufacturing's reliance on product specific physical tooling, 3D printing operates on a software-defined model, enabling the complete removal of long lead times associated with tooling preparation. This significantly accelerates the development and production cycle of complex freeform optical components and waveguides from prototyping phase to volume manufacturing.

The software-defined approach of Vanguard Automation's 3D nano-printing enables 100% reusability, allowing systems to be easily adapted to different product requirements and production lines.

In summary, Vanguard's photonic integration solution portfolio of industry ready machines, Telcordia proven materials and simplified 3D printed optics coupled with passive alignment of photonic assemblies is poised to enable the industry to achieve its targets of high yield, low loss, high density photonic integration.

Photonic Wire Bonding technology enables the combination of the complementary strengths of different optical integration platforms in advanced photonic multi-chip modules leading to compactness with high performance and great design flexibility.

Vanguard's photonic integration solution portfolio is completed by facet-attached micro-lenses on optical chips and fibers, allowing for low-loss coupling with high alignment tolerances and for wafer-level probing of optical devices. The fully automated, highly reproducible, and reliable vanguard SYMPHONY solution is already used by research and industry customers targeting next generation photonic integration and packaging.

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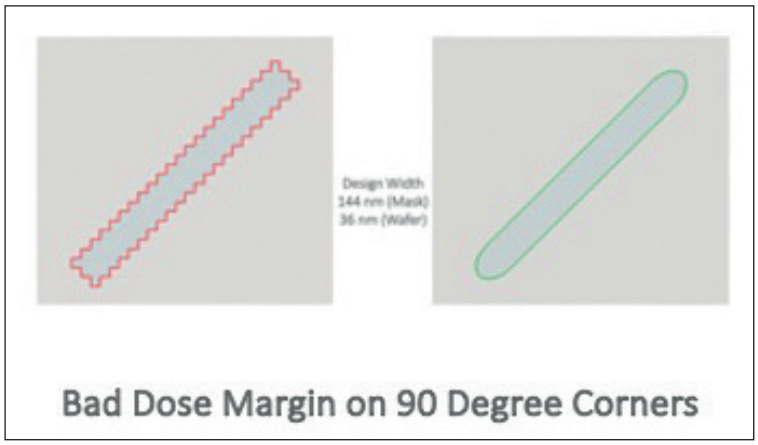
Why the mask world is moving to curvilinear

If you've been to a lithography or photomask technology conference lately, you've likely noticed a trend: many papers and talks on curvilinear masks, curvilinear OPC, curvilinear ILT, curvilinear mask process correction (MPC), and curvilinear mask formats. The photomask industry is experiencing a fundamental shift from Manhattan masks to curvilinear masks. Part 2.

BY LEO PANG, D2S, INC.

MANHATTANIZING CURVILINEAR ILT mask shapes creates two issues. First, there is the issue with VSB shot count discussed in Part 1 of this article in *SiS Issue 6*. The other issue is mask dose margin. Just as the wafer print on the scanner has process window, mask writing on an eBeam mask writer also has process window. In the case of wafer process window, the two variables are focus and dose. In mask writing, since the eBeam writer has infinite or very large depth of focus, the main variable is dose. Instead of calling it dose latitude (as they do in the lithography world), the mask world calls it dose margin. Dose margin is particularly bad for 90-degree corners. Manhattanizing curvilinear mask shapes creates a lot of 90-degree corners, as shown in Figure 11.

In Figure 12, on the right, we show the dose margin for Manhattan and curvilinear contact arrays. Dose margin is represented by a pseudo color: the red represents bad dose margin and the green represents good dose margin. The 90-degree corners of the Manhattan contacts clearly have worse dose margin than the smooth curvilinear contacts. On the left of Figure 12, is a study done in 2019[16], demonstrating that while the edges of the square contact had good dose margin, the corners had unacceptable dose margin. At the same time, it shows that circles at any angle have good dose margin.



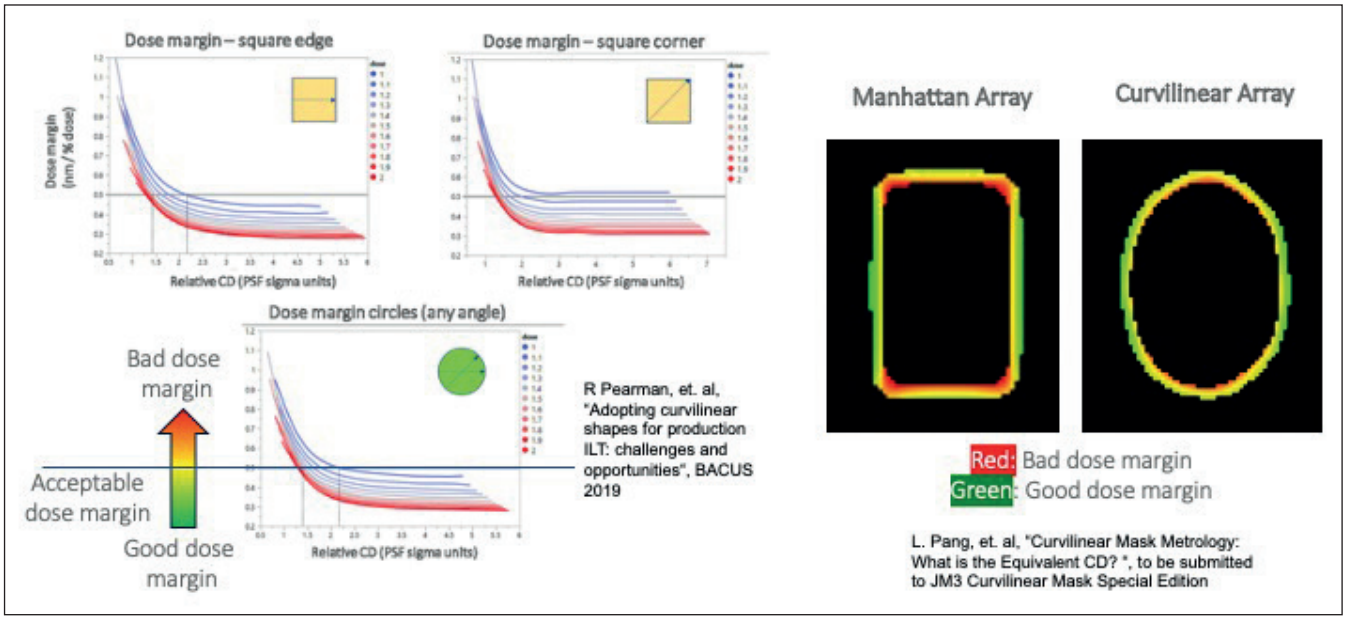
➤ Figure 11. Dose margin is poor for 90-degree corners. Manhattanized curvilinear shapes have many 90-degee corners and so have poor dose margin in comparison to the smooth curvilinear shape.

In addition, curvilinear shapes have less variation on wafer or smaller mask error enhancement factor (MEEF). A 2022 study found that in comparing the MEEF of a Manhattanized diagonal line to a curvilinear diagonal line, the smooth curvilinear line had ~28% improvement in MEEF over the stair-stepped Manhattanized line [17] (Figure 13).

This is the fundamental reason why curvilinear is better. Imagine moving the edge of a shape by a unit of 1, as shown in Figure 14. If it is a Manhattan shape, such as a square, the edges in the X and Y direction are moved by 1, but the corners are moved by 1.4. In a curvilinear shape, such as a circle, the edge in every place on the circle is moved by 1. This means the same change on mask will cause more variations on wafer with the Manhattan shape than the curvilinear shape.

For the same reason as the explanation above, curvilinear shapes have less variation in the mask process as well. In the mask process, which involves bias processes such as etching, curvilinear shapes are created more faithfully. Figure 15 summarizes the findings of a joint study of contact arrays with Micron and D2S. We created contact arrays, both curvilinear and Manhattan [18], and made 6 copies on each array on the mask. We took measurements every four nanometers from four locations on each contact array (left edge, center, a corner, and the bottom), including hundreds of contacts each for a total of millions of measurements.

First, we collected SEM images for all 6 copies of contact array at the same 4 locations (left edge, center, a corner, and the bottom), then we used proprietary software to align the 6 copies of the images for each location. The alignment considered the distortions that the SEM image could



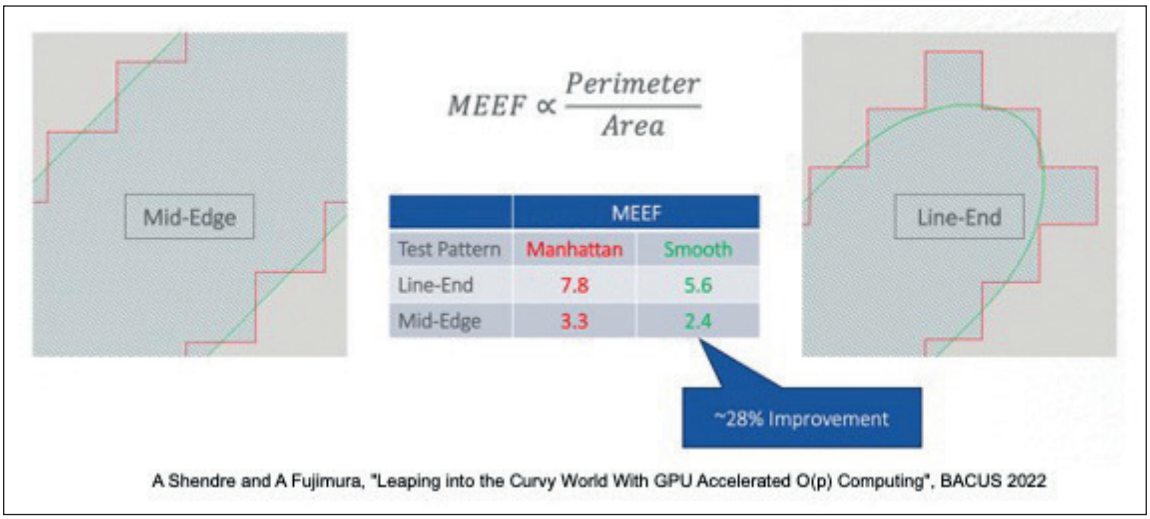
➤ Figure 12. While edges of Manhattan features have good dose margin, 90-degree corners have very poor dose margin, as shown by the red pseudo color. Circles have acceptable dose margin at any angle, as shown by the green/yellow pseudo color[16]. Source: D2S.

introduce, including shift, rotation, and scaling. Once the images were aligned, the contours were extracted using proprietary software. The multiple contours on each contact formed a variation band, and the bandwidth was measured every 4nm. Then we looked at the statistics to measure the mask variation band in the plot on the right, with curvilinear represented in blue and Manhattan represented in orange. We can see that the blue curve is shifted to the left compared to the orange, meaning that it's closer to zero. We can also see that the distribution of the blue curve is narrower, showing less variation.

Figure 16 shows the mean, standard deviation, and max variation for both the Manhattan (in orange still) and the curvilinear (in blue). In all cases, curvilinear contacts show significantly less variation, especially those in the corners with more SRAFs. Recall, these are measurements from the same mask written by the same multi-beam mask writer. The only difference is the pattern. One is a curvilinear pattern, the other one is the Manhattan pattern, but the curvilinear pattern on mask has a 20% smaller variation than Manhattan pattern. That is very significant, because with MEEF, this will translate to the smaller variation on wafer as well.

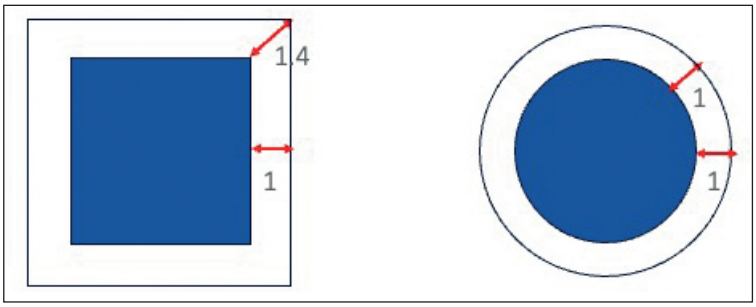
MWCO enables curvilinear benefits for VSB-written masks

We previously covered how the multi-beam mask writer solved the write time problem for curvilinear masks and we have shown that Manhattanized versions of curvilinear shapes do not yield the same benefits as true curvilinear shapes. But many mask shops use VSB mask writers today and will continue to do so. Is there any hope that VSB-written masks can reap the full benefits of true curvilinear shapes?

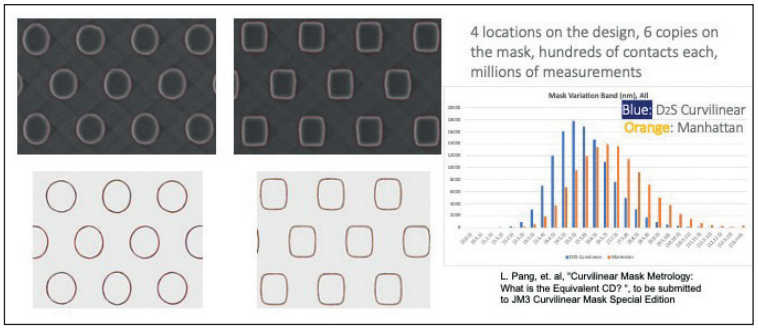


➤ Figure 13. Both the mid-edge and line-ends of Manhattanized patterns have worse MEEF than the smooth curvilinear patterns[17]. Source: D2S.

Yes, there is. As we've seen, the key to reducing mask variation is to reduce the number of corners. Using fewer shots helps the write time problem, and it means there are fewer corners, which will reduce the mask variation. In 2021, this author and colleagues at D2S and Micron introduced the concept of mask wafer co-optimization (MWCO) [19]. Starting with an ILT solution, then using overlapping shots to reduce shot count, MWCO uses double simulations – the mask simulation, and then the wafer simulation – and based on the wafer result, iteratively moves those shots to minimize edge-placement error (EPE) on wafer, as shown in Figure 17. MWCO uses overlapping shots on small SRAFs, which generally comprise the majority of shots. For main features we use fewer larger shots that are not overlapping.



➤ Figure 14. Moving a rectilinear shape by a unit of 1 causes the corners to move by 1.4, causing greater wafer variation, as compared to the circle, which is moved by a unit of 1 in every place on the circle.



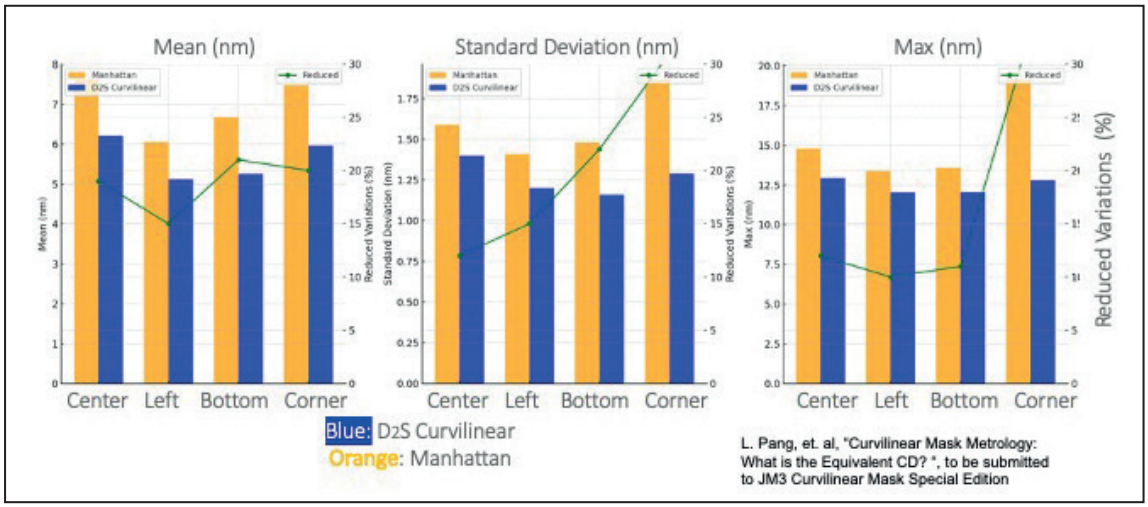
➤ Figure 15. Curvilinear mask patterns (blue on the graph at right) have less variation and a tighter distribution of variation in comparison to the Manhattan mask patterns (orange on the graph at right) [18]. Source: D2S and Micron.

As seen in Figure 18, an ILT pattern fractured with conventional shots (left) uses almost 5X the number of shots as an OPC solution (far right, shots not shown). By using overlapping shots alone, the number of shots can be halved (center left). However, using MWCO with overlapping shots (center right) yields a curvilinear solution that uses fewer shots than the OPC solution. Using fewer shots also means that the write time for the MWCO solution is shorter than for the OPC solution. In this case, the entire curvilinear mask was written in less than 12 hours on a VSB mask writer. Figure 19 shows the curvilinear mask patterns from Figure 18.

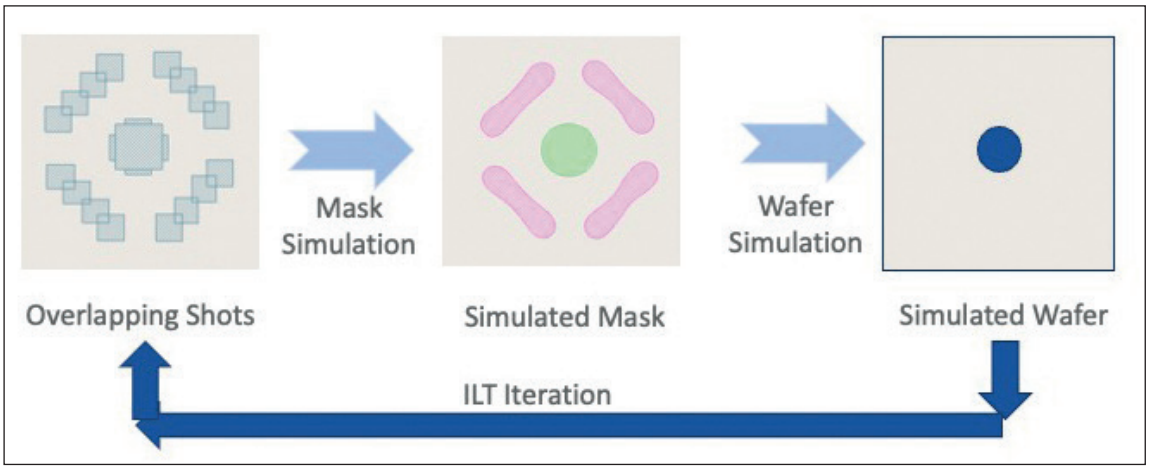
Figure 20 is the process window plot produced from this experiment. The x-axis is the focus, the y-axis is the dose change. Since there are 61 sites, the ratio of the number of sites meeting the process window requirement to the total number of sites was plotted [13]. A CD variation of 10% is used as the process window criteria. The pseudo color from green to red represents process window from good to bad. Overall, curvilinear ILT using overlapping shots without MWCO and curvilinear ILT using overlapping shots with MWCO enlarged the green (or non-red) region by over 2X, especially the depth of focus (DoF). Comparing overlapping shots without MWCO and with MWCO, the MWCO is slightly better, showing the benefit of optimizing wafer EPE instead of mask EPE while only using half the number of shots as the overlapping shots without MWCO case.

The mask industry has been preparing for curvilinear

Curvilinear masks provide multiple, substantial benefits for both mask and wafer quality. Knowing



➤ Figure 16. Mask variation for Manhattan (orange) and curvilinear (blue) mask patterns. Mean, standard deviation, and max all show less variation for the curvilinear mask features [18]. Source: D2S and Micron.



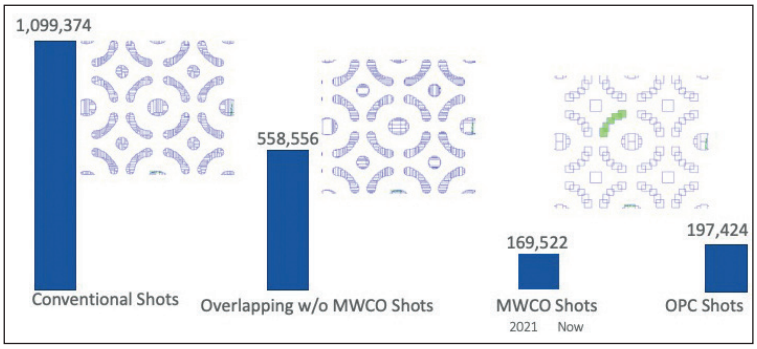
➤ Figure 17. MWCO creates overlapping shots to reduce the shot count of SRAFs. Mask and wafer simulations are performed and the wafer results are used to move the overlapping shots to optimize wafer EPE.

this, the photomask industry has been preparing and is now ready to create curvilinear masks in production. There are still some challenges to resolve, as shown in Figure 21 [14], which presents the responses of industry luminaries in the eBeam Initiative 2023 survey, ranking the concerns about producing curvilinear masks. Datapath was the top concern, a sentiment which was reflected in the work on the Multigon format standards. None of these concerns is insurmountable and many, such as datapath and mask metrology, have proposed solutions in the works already.

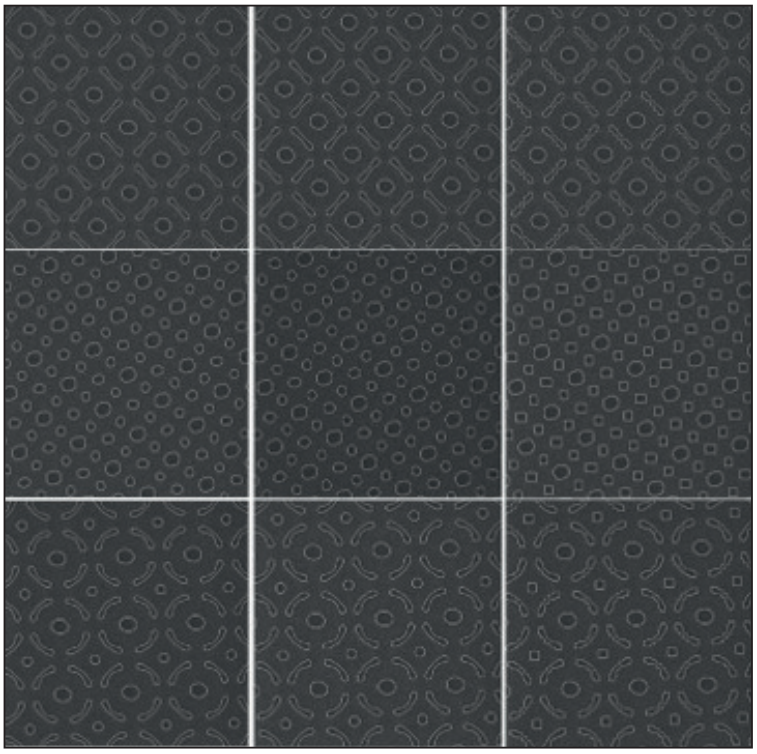
OPC, mask rule checking (MRC), mask process correction (MPC), mask data preparation (MDP), and other data processing steps have traditionally inherited the polygon-based geometry manipulation from EDA which had been primarily focused on manipulating Manhattan rectangles efficiently on CPUs by moving or analyzing vertices and edges. The pixel is ideal for processing curvilinear shapes (or any shapes – pixels are shape-agnostic) [17]. This is not a new finding. All the mask and wafer equipment related to imaging are already pixel-based, including mask and wafer inspection, SEM machines, and mask repair tools.

Although OPC is edge based, or polygon based, ILT is pixel based. Now, multi-beam mask writers are also pixel-based. So, it makes sense that MRC, MPC, etc., all could become pixel based. MPC has already been introduced in the pixel domain, as pixel-level dose correction (PLDC). Since PLDC can be done in real time, the turnaround time needed for MPC becomes zero [21]. This opens opportunities to have the entire tapeout flow in the pixel domain. It is important to note that pixel data does not mean the data volume will be bigger than polygon data, since pixel data can be compressed.

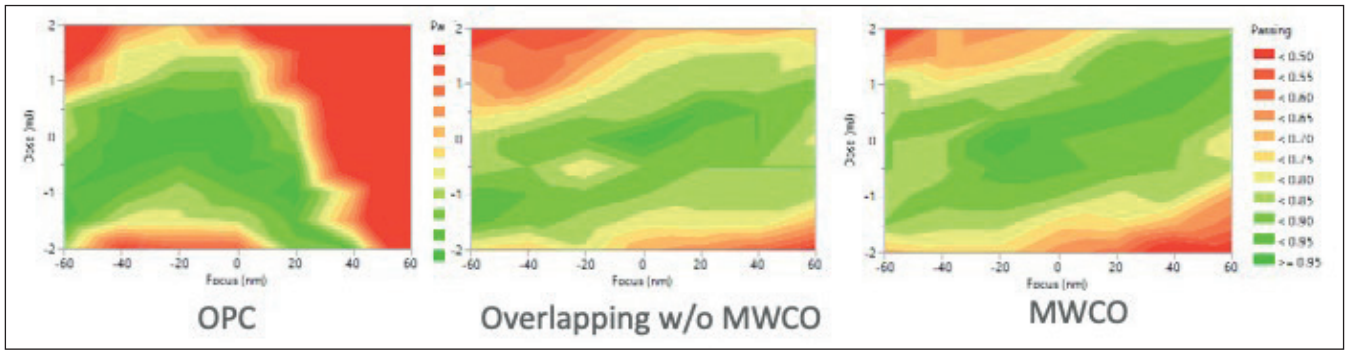
Curvilinear masks are good for semiconductor manufacturing because 1) they significantly expand the wafer process window; and 2) they produce manufacturable mask targets, which are more reliably manufacturable and produce fewer nuisance defects.



➤ Figure 18. An ILT pattern for a contact array is fractured using conventional shots (left), overlapping shots without MWCO (center) and overlapping shots using MWCO (right). The MWCO solution had fewer shots (and therefore a shorter write time) than the OPC solution. Source: D2S.



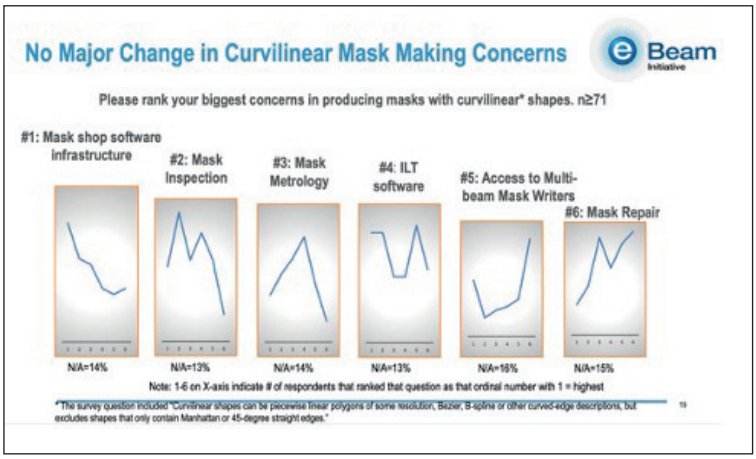
➤ Figure 19: Mask SEM images of VSB shot for three contact arrays with (a) conventional shots, (b) overlapping without MWCO, and (c) MWCO [19] (Source: Micron).



➤ Figure 20. Process window plot produced from the wafers. The red pseudo color represents areas outside the process window; the green pseudo color represents areas inside the process window. The MWCO solution has more than 2X the process window as the OPC solution. Source: D2S and Micron.

But the most remarkable effect of curvilinear masks is that curvilinear masks enable curvilinear design, i.e., curvilinear wafer targets. Just as manufacturable shapes are more reliably manufacturable on masks, manufacturable curvilinear designs are more reliably manufacturable on wafer as well. Curvilinear designs hadn't been manufacturable until recently, so study is just beginning [20] on the potential benefits in power, performance, area, yield, and cost that could come with judicious applications of curvilinear designs. It will be exciting to see how this unfolds on the design side.

- This article is based on a paper from the author presented at SPIE Advanced Lithography 2024[22].
- *Part 1 of this article appeared in SIS Issue 6, published in September 2024.*



➤ Figure 21. Responses from eBeam Initiative Luminaries Survey 2023, showing that the biggest concern about curvilinear masks is the mask shop datapath [14]. Source: eBeam Initiative.

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Beyond AOI:

An AI-driven revolution in visual inspection

In the relentless pursuit of quality and yield in manufacturing, visual inspection plays a crucial role. As industries strive to produce flawless products, the need for accurate, efficient, and adaptable inspection processes has never been more pressing. In response to this challenge, Averroes.ai seeks to redefine visual inspection in manufacturing, which will ultimately replace outdated AOI inspection methods.

The Quality Imperative: Quality control isn't merely a buzzword; it's a financial imperative.

According to a study by the American Society of Quality, the cost of poor quality in manufacturing organizations amounts to a staggering 15-20% of total sales revenue.

This statistic underscores the critical importance of effective inspection processes across various manufacturing sectors, including electronics, semiconductors, and automotive industries. The impact of poor quality on a company's bottom line highlights the need for advanced inspection techniques that can significantly reduce defects and improve overall product quality.

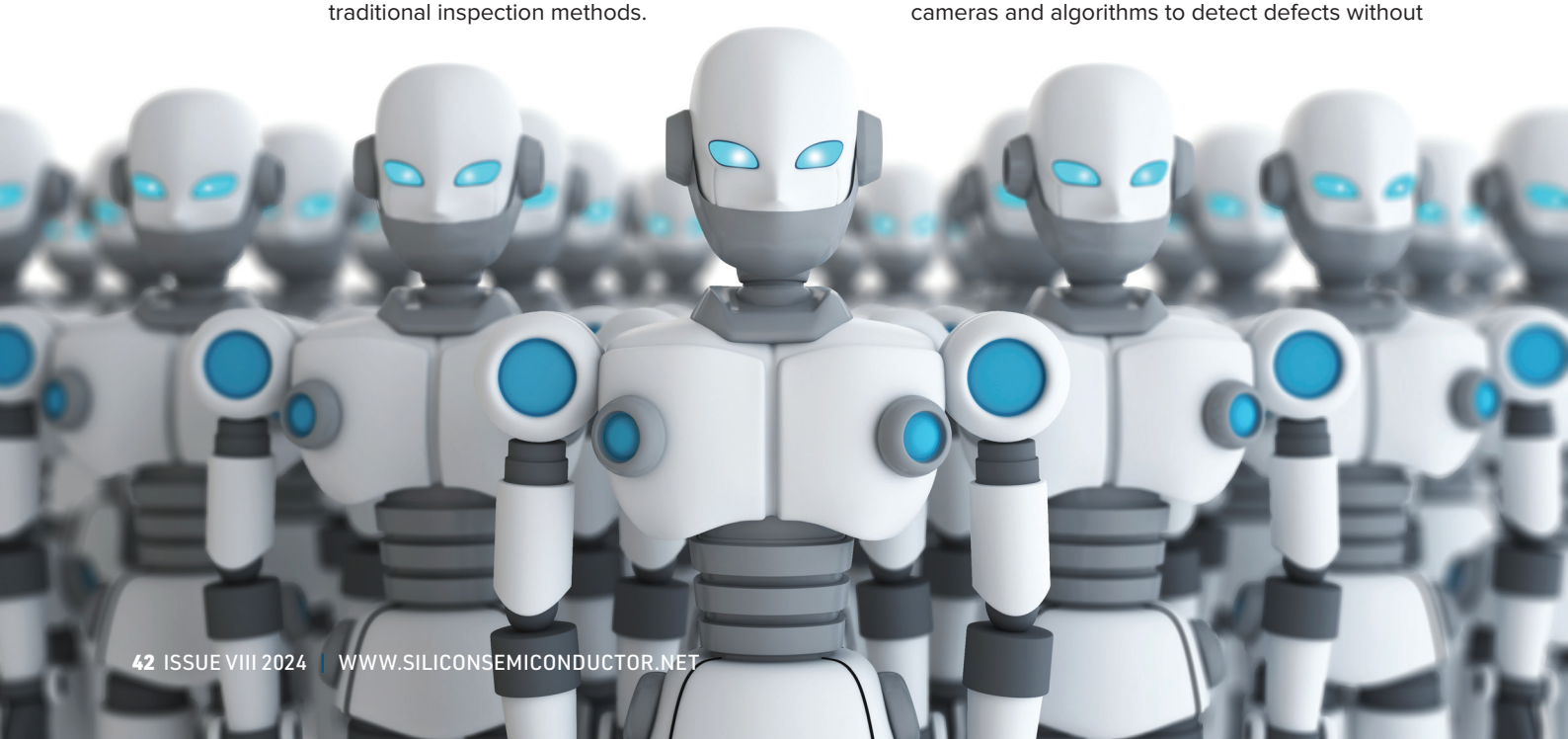
The evolution of visual inspection

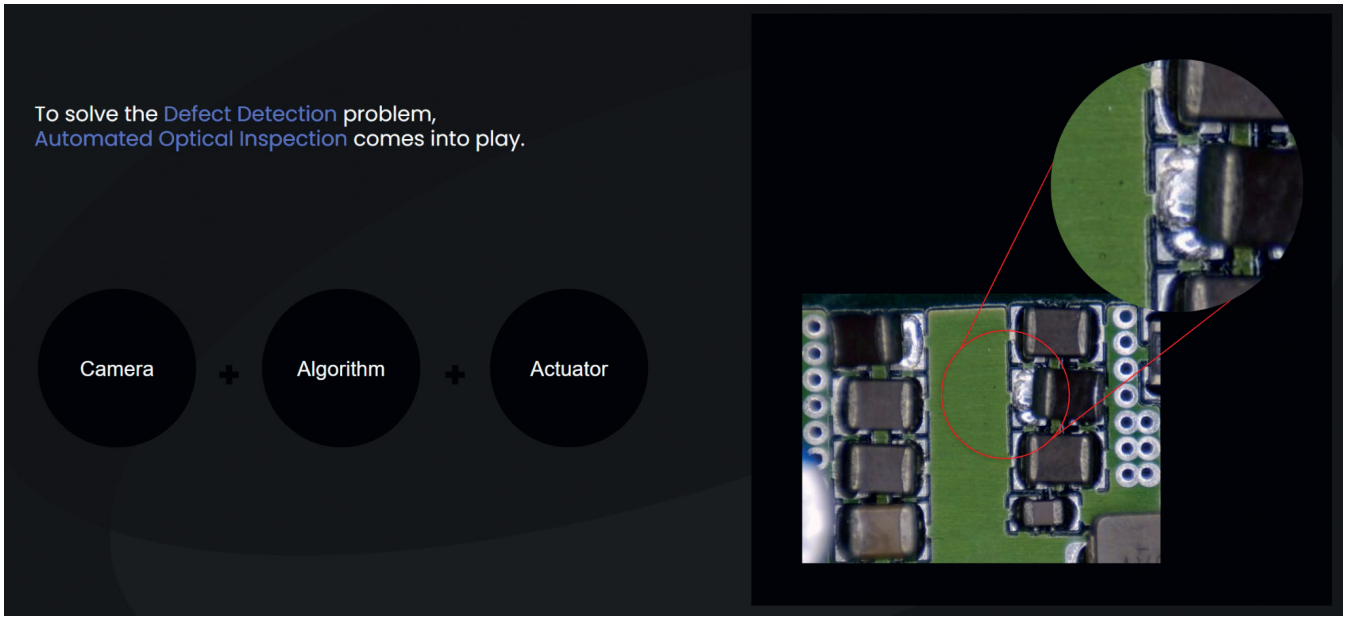
Visual inspection has come a long way from its humble beginnings, but the rapid pace of technological advancement has outstripped traditional inspection methods.

Manual Inspection: The Beginning
Initially, manufacturers relied heavily on manual inspection processes, where human workers visually examined each product for defects. While this method allowed for detailed inspection, it was time-consuming and prone to human error, especially over long periods of repetitive work.

Semi-Automated Inspection: A Hybrid Approach
As technology advanced, semi-automated inspection methods were introduced. These provided workers with specialized tools to make more informed decisions and accelerate the inspection process. This hybrid approach combined the discernment of human inspectors with the efficiency of technological aids.

Automated Optical Inspection (AOI)
The next significant leap came with the introduction of Automated Optical Inspection (AOI) systems in the early 2000s. These fully automated systems use cameras and algorithms to detect defects without





human intervention. AOI represented a major step forward in terms of speed and consistency, allowing for high-volume inspection in industries where manual methods were no longer feasible due to the scale and complexity of production.

The limitations of traditional AOI in modern manufacturing

However, the manufacturing landscape has changed since AOI was first introduced. Products are becoming increasingly smaller, more compact, and more complex. Defects are now harder to catch and often more subtle. The AOI systems designed for the technology of the early 2000s are struggling to keep up with these changes. What worked two decades ago is no longer sufficient for today's manufacturing challenges.

The Need for a New Paradigm

As everything in manufacturing gets smaller and more intricate, the limitations of traditional AOI become more apparent. Complex defects that were once rare are now common, and the systems built for earlier technologies are proving inadequate. This gap between inspection capabilities and manufacturing realities is driving the need for a new approach to visual inspection – one that can adapt to the increasing complexity and miniaturization of modern products.

How Does AOI Systems Work?

Traditional AOI systems typically consist of three key elements: the camera, the algorithm, and the actuator. While each component is crucial, the algorithm stands out as the most critical element, serving as the brain of the system.

Why traditional AOI Falls short in today's manufacturing landscape

Accuracy: One of the primary issues with traditional AOI systems is accuracy. These systems often produce a high rate of false positives, flagging defects where none exist. This oversensitivity can significantly lower production yield, as perfectly good products may be unnecessarily rejected or subjected to additional inspection. The problem of false positives not only impacts efficiency but can also lead to increased costs and reduced overall productivity.

Flexibility: Adapting the algorithm to accommodate new product designs or detect new types of defects often requires a complete overhaul of the system. This inflexibility can be a major drawback in industries where product designs evolve rapidly or where new types of defects may emerge due to changes in manufacturing processes.

Changes in the inspection environment: Changes in the inspection environment, such as variations in brightness or increased noise levels, can severely impact the algorithm's effectiveness.

Even small changes in product design or positioning can lead to unreliable results, necessitating frequent recalibration and adjustment of the system.

Domain expertise required & resource intensive: Implementing and maintaining traditional AOI systems is a resource-intensive process requiring significant domain expertise. Unlike AI-based systems, traditional AOI relies on programmed rules and parameters that need to be manually set and calibrated for each specific inspection task.
This process demands:

- Extensive knowledge of the manufacturing process and potential defects.
- Programming skills to create and adjust detection algorithms.
- Time-consuming calibration to ensure accurate detection.
- Ongoing adjustments to account for even minor changes in products or production processes.

The time-intensive nature of setup and recalibration can lead to production delays and increased costs, especially in industries with rapidly evolving products or frequent changes in manufacturing processes.

Averroes.ai: A paradigm shift in visual inspection

Averroes.ai has developed a deep learning engine to address these challenges. Their platform is designed as a no-code, no-technology-required solution that seamlessly integrates advanced AI into existing manufacturing processes.

This innovative approach allows manufacturers to leverage the power of cutting-edge AI without the need for extensive technical knowledge or significant changes to their existing hardware setup.

Integration with Existing Systems: The Averroes.ai solution operates as a software layer on top of existing hardware, utilizing images from current cameras to enable better-automated decisions. This software-based enhancement means that manufacturers can improve their inspection processes without the need for costly hardware upgrades or replacements.

The system takes in images from existing cameras and processes them through advanced AI models, displaying the results in a user-friendly graphical interface for review and analysis.

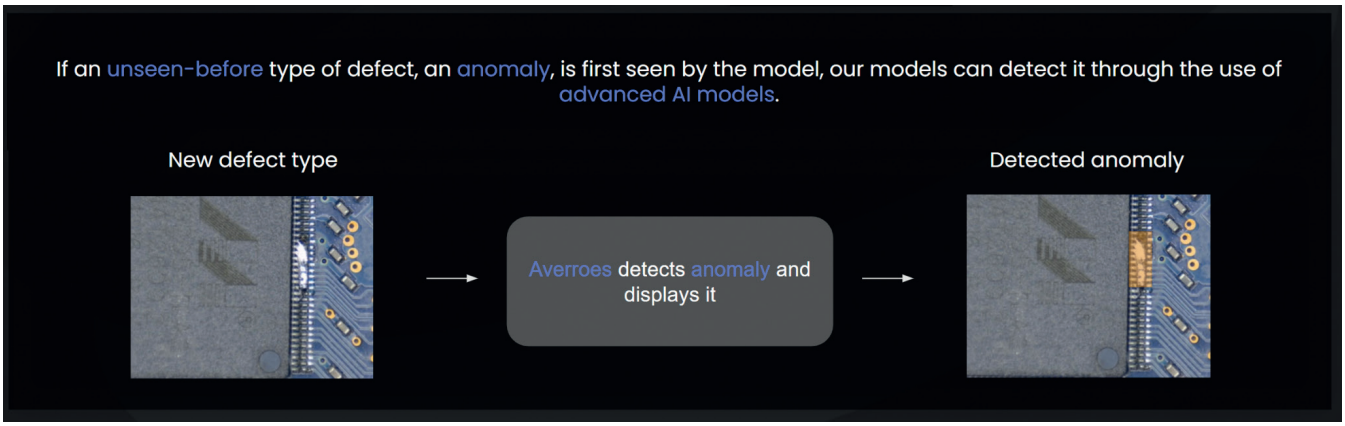
Exceptional Accuracy and Continuous Improvement
One of the standout features of Averroes.ai's platform is its ability to produce custom-built AI applications tailored to each customer's specific use case, achieving high accuracy with very little data. In one case study, the platform increased inspection accuracy from 63% (with the client's previous tool) to an impressive 97%. This dramatic improvement in accuracy translates directly to higher production yields, fewer false rejections, and ultimately, better quality products reaching the end consumer.

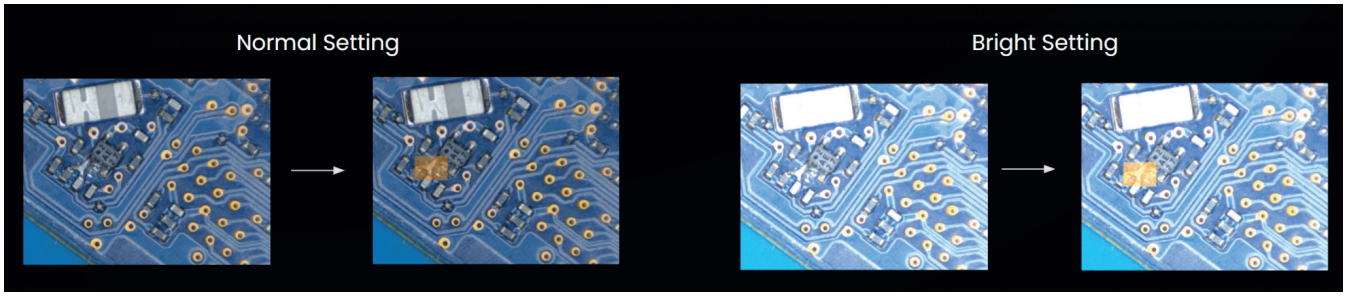
The system's ability to continuously improve sets it apart from traditional AOI solutions. Through active learning, the model suggests interesting images for human feedback, allowing it to evolve and further improve its accuracy over time. This means that the longer the system is in use, the more accurate and efficient it becomes. Starting with a model that may have 95% accuracy, the system can grow to 98%, then 99%, and eventually approach near-perfect accuracy through this iterative learning process.

Advanced defect detection and environmental adaptability: Another key advantage of Averroes.ai's solution is its ability to detect anomalies and new defect types. The advanced AI models can identify previously unseen defect types - a capability that is particularly valuable in industries where new types of defects may emerge due to changes in materials, processes, or product designs.

When the system encounters a new type of defect, it can flag it as an anomaly, allowing human operators to review and classify it. Once classified, the system immediately learns from this input and begins to identify similar defects in future inspections.

Environmental adaptability is another strength of the Averroes.ai platform. Unlike traditional AOI





systems that may struggle with variations in lighting or product positioning, this solution maintains high accuracy despite changes in the inspection environment.

Differences in brightness or placement do not significantly impact the system's performance, ensuring consistent results across various manufacturing conditions.

The engine behind the innovation

At the heart of Averroes.ai's capabilities is its proprietary engine, a sophisticated deep learning algorithm that designs and creates models tailored to specific use cases. This engine, boosted by the company's in-house DefectGPT model, can auto-generate complex models within hours while ensuring top-quality results.

The use of advanced AI in model creation allows for rapid deployment and adaptation to new inspection requirements, a crucial advantage in fast-paced manufacturing environments.

The Four-Step Process: Averroes.ai's approach to transforming datasets into high-performance AOI models follows a straightforward four-step process.

The journey begins with data collection, where a small sample of images (preferably 10 or more per defect type) is gathered from the client. This initial dataset forms the foundation upon which the AI model will be built.

Next comes the model generation phase, where Averroes.ai's proprietary engine utilizes this data to create high-quality AI models within hours. This rapid turnaround time is a significant advantage, allowing for quick deployment and testing of new inspection models.

Once the model is trained, it moves to the deployment phase, where it is integrated into the client's inspection process. This integration is designed to be seamless, working with existing AOI equipment to minimize disruption to ongoing operations.

The final step in the process is continuous improvement. Leveraging human-based feedback, the model continues to learn and adapt, driving towards 100% accuracy. This ongoing refinement ensures that the inspection system remains effective and up-to-date, even as manufacturing processes or product designs evolve.

Flexible Integration Options: Understanding that different manufacturers have varying needs and constraints, Averroes.ai offers flexible integration options for its solution. The platform is designed to work seamlessly with existing AOI equipment, offering both cloud and on-premises deployment options to suit different operational requirements and security protocols.

Cloud Solutions: For clients seeking rapid deployment with minimal hardware requirements, cloud solutions provide an ideal option. These are compatible with major cloud platforms including Azure, AWS, GCS, and Apple Cloud, allowing for easy integration with existing cloud infrastructure.

Cloud deployment offers the advantages of scalability, accessibility, and reduced on-site IT requirements.

On-Premise Solutions: On the other hand, on-premises solutions are available for clients that prioritize data security and in-house control. These can connect directly to local cameras or file systems, ensuring that sensitive manufacturing data never leaves the client's facility.

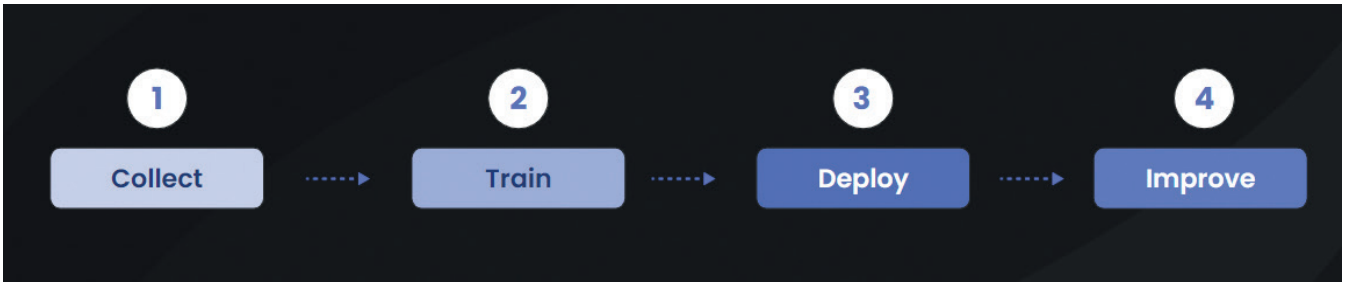
This option is particularly appealing for industries dealing with proprietary designs or those subject to strict data protection regulations.

Real-World impact: A case study

The effectiveness of Averroes.ai's solution is perhaps best illustrated through a real-world application.

In one instance, a client's existing inspection tool was missing 50% of defects, yielding only 63% accuracy. This level of performance was significantly impacting product quality and production efficiency. By simply connecting Averroes.ai's solution to the existing tool's camera, the process was automated and enhanced, resulting in a remarkable improvement to over 97% accuracy.

This dramatic increase in accuracy demonstrates the transformative potential of AI-enhanced AOI. Not only does it lead to better defect detection, but it also reduces false positives, improves production



yield, and ultimately contributes to higher-quality products.

The Averroes.ai platform: A closer look

The Averroes.ai platform offers a user-friendly, project-based approach to visual inspection. Each project serves as a container for related tasks, including data, models, monitors, and connectors. This organizational structure allows for easy management of multiple inspection processes or product lines within a single interface.

Team Collaboration Features: Team collaboration features are built into the platform, allowing project owners to invite collaborators and assign roles with varying levels of access. This facilitates seamless cooperation between different departments or team members involved in the inspection process, from quality control specialists to process engineers.

Versatile Dataset Creation: The platform supports versatile dataset creation, accommodating various task types including classification, object detection, and segmentation. This flexibility allows the system to be adapted to a wide range of inspection requirements, from simple pass/fail assessments to complex defect localization and characterization.

Intuitive Labeling Tools: An intuitive labeling tool is provided for easy annotation of images. Users can resize bounding boxes, change labels, and enhance image properties such as brightness, contrast, and saturation. These features make it easier to label defects accurately, especially in cases where defects may be subtle or difficult to discern.

Advanced Model Training Options: When initiating model training, users have access to advanced options that can significantly enhance model performance.

These include active learning, which allows the model to identify and request feedback on the most informative images; anomaly detection (referred to as Watchdog), which enables the identification of new defect types; and smart augmentation, which uses AI to generate additional training samples based on existing labeled images.

Model performance and monitoring

Comprehensive Analytics Tools: The Averroes.ai platform provides comprehensive tools for monitoring and analyzing model performance. Users can view detailed accuracy metrics, track training progress over time, and access type-specific information such as the number of defects, true positives, false positives, and false negatives. This wealth of information allows for continuous assessment and improvement of the inspection process.

Flexible Deployment Options: Deployment options are flexible, with models able to be connected to cameras for real-time streaming or to cloud/local storage for automated predictions on newly uploaded images. This versatility ensures that the system can be integrated into various production environments and workflows.

API Integration for Custom Pipelines: For seamless integration with existing systems, the platform generates API keys for custom prediction pipelines. This feature allows manufacturers to incorporate Averroes.ai's advanced inspection capabilities into their broader manufacturing execution systems or quality management processes.

Batch Prediction Capabilities: The platform also supports batch prediction, enabling users to manually upload large sets of images for analysis. This capability is particularly useful for large-scale testing and validation, allowing quality control teams to assess the model's performance across a wide range of scenarios or product variations.

Conclusion

As manufacturing pushes the boundaries of precision and complexity, traditional AOI systems are proving inadequate for modern challenges. Designed for early 2000s technology, these systems struggle with today's smaller, more complex products and defects.

Averroes.ai is not just enhancing visual inspection – it's revolutionizing it. By leveraging advanced AI and deep learning, Averroes.ai aims to replace outdated AOI methods with a more powerful and adaptable solution. The company's innovative approach, combining custom-built AI applications with high accuracy from limited data, positions it at the forefront of next-generation quality control. As manufacturers strive to minimize defects and maximize yield in an increasingly demanding market, Averroes.ai's technology promises to be crucial in shaping the future of manufacturing quality assurance, enabling higher quality, greater efficiency, and increased competitiveness.

In sensitive industries like semiconductor manufacturing, numerous cleaning steps are required throughout the production process.

Sustainable cleaning solutions for a greener microelectronics industry

The microelectronics industry powers the devices that define modern life, from smartphones and computers to vehicles and medical equipment. However, this rapidly advancing field also faces considerable environmental challenges, particularly regarding its cleaning processes. Each year, the industry uses around 500 million liters of chemical cleaning agents, many of which are petroleum-based solvents like N-Methyl-2-pyrrolidone (NMP). While effective, these chemicals pose significant environmental and health risks.

BY CHRISTIAN RÖMLEIN, CEO AT INTELLIGENT FLUIDS

FORTUNATELY, sustainable alternatives that offer a great substitute for traditional chemical solutions are emerging. Water-based cleaning agents are both effective and eco-friendly, offering a viable replacement for conventional solvents. Yet, despite their benefits, these alternatives still remain underutilized in the microelectronics sector. Now is the time for the industry to reconsider its reliance on aggressive chemicals and embrace greener solutions that meet both technical and environmental standards.

In this article, we will explore the unique cleaning challenges of the microelectronics industry, examine the harmful effects of traditional solvents, and highlight the promise of water-based alternatives.

The unique cleaning challenges of microelectronics

The microelectronics industry operates on an incredibly small scale, with manufacturers working on components measured in micrometers and nanometers.

This extreme miniaturization – seen most notably in the billions of transistors packed into a single microchip – requires equally precise cleaning processes. Any contamination left on these

components can degrade performance or cause total product failure, making cleanliness a top priority. Microchips undergo hundreds of individual processing steps, each of which may leave behind residues that must be removed before the next step.

A single computer chip, for example, can require up to 500 processing steps, with cleaning required after almost every stage. The complexity of these cleaning tasks increases as chips become smaller and more advanced, leading the industry to traditionally rely on chemical solvents that are believed to offer the most effective results.

However, this reliance on aggressive solvents comes at a significant cost – not only to the environment but also to human health.

The environmental and health costs of petroleum-based solvents

Petroleum-based solvents such as NMP, DMSO, and acetone have long been favored in the microelectronics industry due to their ability to efficiently dissolve contaminants. Yet, their extensive use carries serious consequences.

Once chemicals like NMP make their way into the environment, they can cause long-lasting harm, particularly to aquatic ecosystems. Acetone belongs to the group of volatile organic compounds (VOCs), which contribute to air pollution and can leach into soil and water sources if the disposal isn't properly taken care of.

In addition to environmental concerns, petroleum-based solvents pose significant risks to workers who handle them. Studies show that prolonged exposure to solvents like NMP cause a variety of health problems, including neurological disorders, respiratory issues, and skin irritation. Some chemicals are also known to cause reproductive health issues, with women exposed to them facing a higher risk of birth defects.

Despite the risks, the general opinion still holds on to the belief that only strong, traditional chemicals can deliver the necessary precision in cleaning microelectronics. However, this assumption is increasingly being challenged by the development of green alternatives that are both effective and safe.

A green alternative: water-based cleaning agents

Water-based cleaning agents are emerging as a promising, eco-friendly alternative to petroleum-based solvents. Companies like the German deep-tech firm intelligent fluids are leading the way in developing these solutions, offering products that can replace conventional solvents without compromising on cleaning performance.

These water-based agents use microemulsions, which are stable mixtures of water, oil, and surfactants. Microemulsions operate through physical mechanisms rather than chemical reactions, with micelles – tiny, net-like structures – forming to lift off dirt and residues from surfaces. This physical removal process makes the cleaning action both effective and gentle.

A key innovation of companies like intelligent fluids lies in their ability to stabilize these microemulsions for industrial use. Their proprietary formulations maintain the effectiveness of these water-based solutions across a wide range of temperatures and storage conditions, addressing some of the limitations that have historically hindered the implementation of water-based cleaners

A typical intelligent fluids formulation consists of water, oil, surfactants, and small amounts of additives like activators, or fragrances. The careful balance of components allows the water-based cleaner to achieve similar results to aggressive solvents but with a significantly lower environmental and health impact.

➤ Water-based cleaning agents can be applied for photoresist stripping and metal lift-off.

Applications in microelectronics: photoresist stripping and metal lift-off

Water-based cleaning agents are being tested and applied in various stages of semiconductor manufacturing, with two key applications standing out: photoresist stripping and metal lift-off.

In the production of semiconductors, photoresist materials are applied to a substrate and then exposed to light to create precise patterns. After the desired pattern is formed, the remaining photoresist must be thoroughly removed to ensure a clean surface for subsequent processing steps. Any leftover residue can compromise the chip's functionality.

Traditional solvents chemically break down photoresist materials to remove them. In contrast, water-based agents developed by intelligent fluids physically lift off the photoresist using their phase fluid technology. This results in effective cleaning without the health and environmental risks associated with traditional solvents.

Similarly, in the metal lift-off process, metal which layers over a patterned photoresist must be removed. Water-based agents can break down the underlying resist, allowing the metal layer to be removed cleanly and without harmful chemicals. This method reduces the risk of chemical damage to both the delicate components and the environment.

The path to a greener future for microelectronics

The microelectronics industry is now at a turning point. While petroleum-based solvents have long been the default choice for cleaning, the environmental and health consequences of their use can no longer be ignored. Water-based cleaning agents present a viable, sustainable alternative that meets the rigorous standards of precision demanded by the industry.

Real-world applications have demonstrated that these green alternatives can deliver results on par with traditional solvents while significantly reducing the associated risks. As companies and regulators become more aware of these innovations, the adoption of sustainable cleaning solutions is inevitable. For the microelectronics sector, embracing water-based cleaners is not only a responsible choice but also a practical one. The technology is ready and available, and with it comes the opportunity to significantly reduce the environmental footprint of one of the world's most essential industries.

The shift towards sustainable cleaning in the microelectronics industry is not just about compliance – it's about leading the charge toward a greener, healthier future. By adopting water-based solutions, the industry can continue to innovate while safeguarding both human health and the planet.

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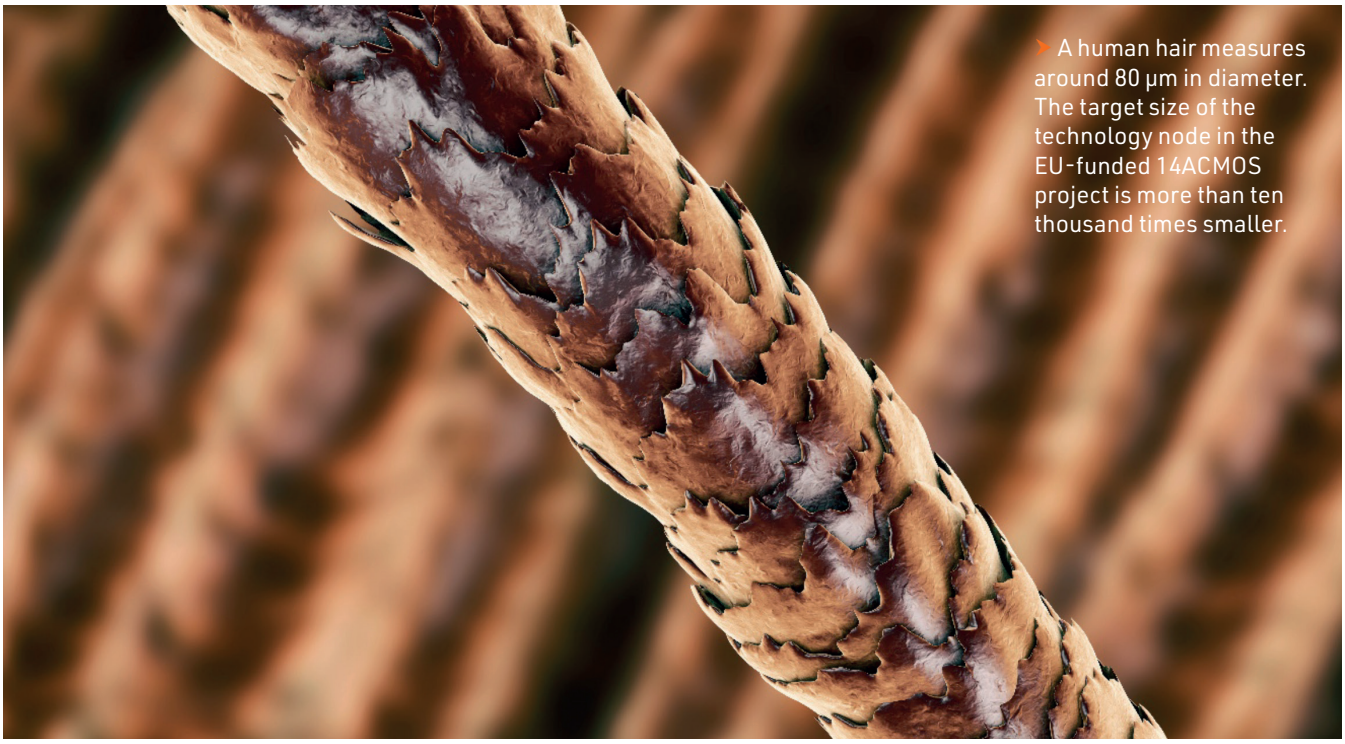


A human hair measures around 80 µm in diameter. The target size of the technology node in the EU-funded 14ACMOS project is more than ten thousand times smaller.

Splitting hairs to ten to the power of four

14ACMOS: EU project for the next technology node in semiconductor manufacturing

BY MATHIAS WINTER, HEAD OF PIEZO DRIVES & SYSTEMS TECHNOLOGY, GLOBAL RESEARCH AND MARKUS WIEDERSPAHN, CORPORATE COMMUNICATIONS, PHYSIK INSTRUMENTE L.P. (PI)

THE 14ACMOS project is part of Horizon Europe, the EU's key funding program for research and innovation for the period of 2021 to 2027 with a volume of more than € 95 billion. It tackles climate change, helps to achieve the UN's Sustainable Development Goals, and boosts the EU's competitiveness and growth.

Horizon is divided into six clusters, of which cluster 4 addresses "Digital, Industry & Space", funded with more than € 15 billion. With a total of currently 127 projects cluster 4 aims to strengthen the competitiveness of European companies in semiconductor and photonics industries.

The 14ACMOS project (14ACMOS = 14 Angstroem Complementary Metal-Oxide-Semiconductor) within Horizon aims to develop solutions for the 1.4 nm process technology node. Project activities address four key pillars: lithography, metrology, mask-infrastructure, and process technology.

Lithography solutions will be pushed to meet 1.4 nm capability, and extreme UV plasma physics will be studied to optimize optics transmission and lifetime. In the metrology pillar, advanced methods will be developed to improve measurement sensitivity and uncertainty and to assess reticle degradation induced by extreme UV light. Mask-infrastructure will cover the development of mask repair strategies based on particle removal technology and will assess durability. Process technology involves the development of patterning solutions, active device selection, and new interconnect technology, which are suitable for the 1.4 nm technology node.

The 14ACMOS project started in December 2022 and is set to end in November 2025. Total cost of the project sums up to € 94.6 million with an EU contribution of € 21.8 million. The project is coordinated by ASML. Participants are among others Carl Zeiss SMT, Trumpf, Applied Materials, KLA, Physikalisch-Technische Bundesanstalt (PTB). European players like ASML, Carl Zeiss SMT, and PI have contributed to every step of miniaturization in semiconductor manufacturing along the way from several microns down to the 1.4 nm node. To reach precision of 1.4 nm, new actuator and motor concepts, sensors and (control) algorithms for the drives must be developed, besides advancements in process technology, improved optics, and materials.

This project is co-funded by the European Union under grant agreement No 101096772 and is supported by the Chips Joint Undertaking and its members.

“Funded by the European Union. Views and opinions expressed are however those of the authors only and do not necessarily reflect those of the Chips Joint Undertaking. Neither the European Union nor the granting authority can be held responsible for them.”

PI offers 50 years of experience in piezo technology and nano positioning, a broad technological spectrum, and a high level of vertical integration in order to develop and provide components and systems that are optimally tailored to the respective process: From the very beginning, the basis for this consisted of mechanical motion systems (actuators and motors) and the appropriate bearing technology, sensors for recording the distance traveled and for determining the absolute position, algorithms for the firmware and an extensive collection of software interfaces and control technology. As a decade-long system partner of semiconductor equipment manufacturers and in particular the main participants in the 14ACMOS project, PI contributes its expertise and experience to the development of innovative motion solutions. The focus here is on very demanding motion and positioning tasks that require precision in the nanometer and sub-nanometer range. A particularly important aspect of some of the applications is the need to operate the systems under vacuum conditions. PI also offers suitable technologies and options for this.

A wide range of drive technologies

The field of semiconductor manufacturing, and the 14ACMOS project in particular, presents a unique challenge for motion systems: the combination of long travel distances (up to hundreds of millimeters) with high dynamics, speed, and precision down to the nanometer range. PI meets these challenges head-on with a comprehensive portfolio of drive technologies.

Electromagnetic drives

In the class of electric motors, PI offers rotating electric motors such as DC or stepper motors. These are used in connection with screw or worm drives. Stepper motor systems with high-resolution encoders can perform minimum incremental motions of 10 nm with high reliability and repeatability.

➤ Application examples of magnetic direct drive technology.

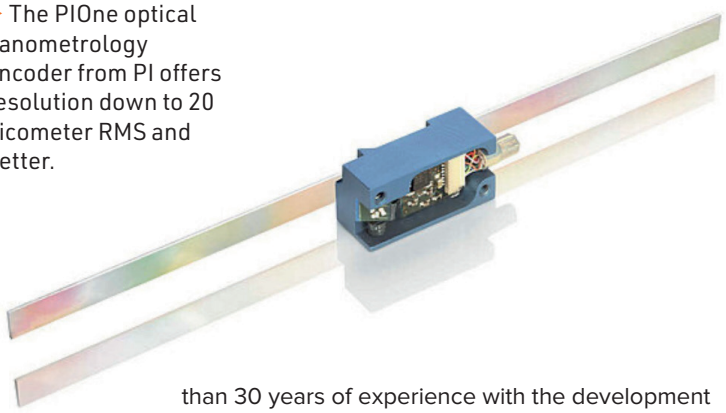
Also, in the field of magnetic direct drives, a wide range of technologies is at hand, namely voice coil motors, iron-core and ironless linear motors, and torque motors.

Piezo-based actuators and drives

The motion of piezo actuators is based on solid-state effects, giving them unlimited resolution in principle. Their stiffness is very high, enabling high force generation and dynamics. Their rapid response time in the microsecond range is a result of their high resonant frequency which can reach more than one hundred kilohertz. Actuator travel in the range of several ten micrometers can be mechanically amplified to reach more than 1 mm. The combination of extremely high resolution and small travel ranges requires the use of suitable guiding elements which are typically flexures that enable highest accuracy by avoiding friction, play and backlash.

Piezo actuators, that are preloaded against a guided runner can be utilized to build linear motors with motion resolution of far below one nanometer. PiezoWalk® piezo motors from PI offer unique capabilities which perfectly match with the needs of semiconductor manufacturing. This nonmagnetic, vacuum-compatible, and clean-room-compatible technology is based on more

➤ The new N-332 linear stage utilizes the PiezoWalk® technology.



➤ The PIOne optical nanometrology encoder from PI offers resolution down to 20 picometer RMS and better.

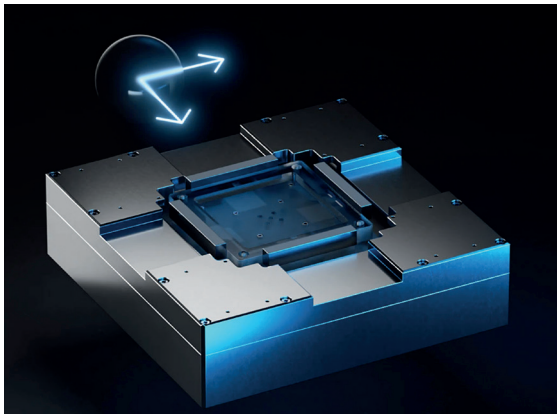
than 30 years of experience with the development and production of piezoceramic components. PI received the SEMI Technology Innovation Showcase Award for the PiezoWalk® technology in 2005. The drives are continuously developed further, and a large number of variants are now available for different areas of application.

Resolution of these drives goes down to 30 picometer, travel ranges are scalable due to scalable runner length. Feed forces are in the range of 50 N to several 100 N. These drives are self-locking when switched off thus saving energy and reducing the generation of heat.

The latest addition to this product family, the N-332 linear stage, is configurable for use in multi-axis setups involving the X, Y, Z axes, and the XY, XZ, and XYZ planes. For applications that require operation in vacuum, the N-332 stages are available in configurations suitable for pressures as low as 10-9 hPa. The PICMAWalk piezo motor inside the N-332 stage is based on PI's proprietary PICMA® piezo actuators.

A highly specialized application of piezo-based components are so-called PIRest actuators. With a load capacity of up to 4000 N per actuator and micrometer displacement with nanometer resolution, these components are ideally suited for drift compensation in machines, for alignment of optical components and static precision positioning.

Sometimes it is even necessary to combine motion systems that enable long-stroke movements, such as linear drives or piezo motors, with piezo-based actuators. Actuator and drive technologies are only one aspect considering the overall system properties. Optimal performance as required in applications targeted in the 14ACMOS project can only be achieved by implementing new and sophisticated control algorithms and the next generation of high-resolution sensor technology.



➤ Magnetic levitation is a promising technology for high-precision motion in six degrees of freedom.

The right position sensor technology

Position sensing systems are required to provide feedback to the motion controller. Linearity and repeatability of motion and positioning tasks are not possible without highest-resolution measuring devices. Accuracies in the range of a few nanometers and below require a position measurement method that can also detect motion in this range. PI can also draw on extensive experience and a comprehensive portfolio of technologies developed in-house in this discipline. Examples comprise capacitive sensors and optical nanometrology encoders. The latter achieve a resolution of 20 picometer and better due to their small signal period of 500 nm and the optimized signal processing.

New magnetic levitation stages

The PI Group is committed to meeting the demanding objectives of the 14ACMOS project through the enhancement of existing technologies and the creation of novel and transformative new solutions. PI is also engaged in the development of new technologies beyond the scope of the 14ACMOS project. One illustrative example is that of magnetic levitation (maglev) stages with six degrees of freedom. One major benefit of this technology is the avoidance of any friction in the process chamber, eliminating the risk of particle contamination.

To employ this principle for the execution of high-precision movements, the magnets in the base are designed as electrically controllable coils. In order to enable movements in all six degrees of freedom, a corresponding number of magnet pairs is required. In a multitude of practical applications, Halbach arrays are employed to reduce energy consumption, augment load capacity, and diminish heat dissipation.

The combination of magnetic guidance and dedicated high-precision drive and sensor technologies provides high dynamics and the highest resolutions down to the picometer range. Active control and definition of guiding characteristics in up to six degrees of freedom can enable additional correction tasks such as focusing in Z or adjusting tip/tilt during operation. The frictionless guiding principle, which is free of rolling elements, lubrication, and air flow, will ensure the highest precision over the entire service life and allows use in cleanroom environments.

Controller technology

As demands on the precision, dynamics, and speed of mechanical motion systems increase, so too does the complexity of the control systems. The selection

of an appropriate control technology is therefore of paramount importance. In particular, the control of piezo actuators and piezo-based positioning systems requires a high degree of specialization. PI has gained extensive experience in this field over decades. The characteristic properties of piezo actuators include the generation of large forces and fast response. In electrical terms a piezo element corresponds to a capacitance. A rapid change to the operating voltage brings about a rapid displacement of the actuator and thus a change in position.

When the control voltage suddenly increases, the piezo actuator can achieve its nominal displacement in only a few microseconds. A prerequisite for this is that the power supply provides sufficient current to charge the capacitance. For steady state operation, i.e., when holding a certain position, the stability of the power supply is crucial, as the piezoelectric actuators already respond with motion to the slightest voltage changes. Noise or drifting must therefore be avoided as far as possible.

With all these special features, PI benefits from more than 30 years of experience in the manufacture of piezo elements and the development of piezo-based positioning systems. PI is one of the few companies in the world with access to the entire value chain: from piezo development and production to the development of piezo-based motion systems and control technology.

PI can also look back on an even longer history of innovation in electric motor control technology. In addition to own cutting-edge solutions, PI leverages the expertise of ACS Motion Control, a wholly owned member of the PI Group based in Israel. Magnetic levitation stages exemplify the necessity for sophisticated control technology. In this context, the linear stage platform is not constrained by mechanical bearings, allowing for unimpeded movement within a single degree of freedom. Consequently, a robust multi-axis controller with a high bandwidth is essential to maintain control over all other degrees of freedom.

Conclusion

The 14ACMOS project presents completely new challenges and tasks for all involved. Precise positioning plays a key role in many processes. For example, in the manufacture, inspection (quality control) and repair of lithography masks. In wafer inspection, it supports the detection of structural failures, defects and particles. Precise positioning is also essential in the lithography process, and in wafer metrology, for example for measuring layer thicknesses and overlay offsets.

With a comprehensive portfolio of precision positioning technologies and complementary expertise in sensor, control, motion and force transfer technologies, PI is well positioned to support this technology node.

TSMC enables semiconductor fabrication expansion with AMD

Better cost-performance with fewer servers by deploying 4th Gen AMD EPYCprocessors.

TSMC is widely considered to be the leading foundry of semiconductor wafers in the world, but the foundry giant has bold plans for further expansion. This will require even more computational power to run its production, research, development, and general IT infrastructure. AMD EPYC processors were already playing a key role for TSMC, but 4th Gen AMD EPYC CPUs have provided the additional increase in capabilities required for the company to achieve its growth goals.

"TSMC is expanding very quickly," said Simon Wang, director of Infrastructure and Communication Services Division at TSMC. "We are expanding our global manufacturing footprint and have new fabrication plants being built in Taiwan, Japan, Germany, and the U.S. That means we are going to require a lot of computing power for fab production, research and development simulation, and business operation."

For its upgraded infrastructure, TSMC wanted to maximize computing performance while limiting power consumption. "When we evaluate servers and storage, we look at the computing performance per unit of power consumed, the space it takes, and the cost," said Wang. "Our workloads roughly fall into three categories. The first one is for automated fab production. The second is for research and development including simulation and design, working with Cadence and Synopsys Electronic Design Automation.

Mask-making also requires a lot of computing power, as does pathfinding. We are also searching for new materials and new technology for next-generation products. The third category is for business operation, supporting units like taking orders, HR, and legal." Empowering TSMC across three workload types. "Most of our fab automation is CPU based, using a Linux platform with virtual machines or Kubernetes," said Wang. "This is supported by a large quantity of storage. For R&D, we use CPUs with GPUs. In the third category of business operation, the quantity is limited compared with the other two because these are systems used by our supporting units and they mostly use CPU servers."

Although TSMC is the manufacturing partner for the AMD EPYC processor range, internal regulations meant that Wang had no special knowledge of forthcoming products, although his experience with previous generations had been very positive. Knowledge of the roadmap came from the AMD country manager in Taiwan, but Wang still needed to ensure the new generation would serve TSMC's requirements.

"The IT department has an additional responsibility to prove that our products are good," he said. "I wanted to prove that the latest AMD processors produced by TSMC have better performance at lower power consumption than the previous generation." "The IT department first defines the configuration that we want based on workload," said Wang. "We define the specifications for the CPU, clock rate, memory, and solid-state drive (SSD). Every year we define five to seven models, which we send to the vendors and ask for their feedback. It's an open bidding process where we decide the ultimate vendor. We are vendoragnostic. We decide on the vendor based on pricing, performance, and power efficiency."

Better cost-performance with AMD EPYC CPUs
"For the 4th Gen AMD EPYC rollout, we considered two options: a singlesocket CPU with more cores or dual CPUs with fewer cores each but the same overall total," said Wang. "We evaluated the cost performance of these two configurations. Originally, we thought that two CPUs with fewer cores would come out better, but one socket with more cores did."

"For performance testing, we use generic tools available on the market," said Wang. "In addition to those tools, we also use our pre-production environment, to see how the workload would perform and to see the response time. That was tested in our fab production and the R&D design center as well. In addition to testing performance and power consumption, we also test the server operability, which includes auto provisioning, so we work with the vendors for this."

"Compared to the previous generation, we found that 4th Gen AMD EPYC CPUs delivered more than a 30 percent gain in cost performance," said Wang. "Migration was very easy for fab production and automation. The IT department had a smooth transition, too. The only thing that we spent more time on was the R&D mask making because this process requires very high precision, but in the end, the team certified the AMD CPUs."

"In January of this year we were looking at the total number of CPUs that we bought last year and the plans for this year," said Wang. "We realized that by deploying 4th Gen AMD EPYC CPUs, we could buy fewer servers while increasing the computing performance by 30 to 40 percent. So migration was something that we must do." The increased performance per server also means that TSMC needs less space in the data center to deliver the same performance.

Better performance, lower cost, reduced power
Power consumption was also reduced thanks to the server density. "Computing performance has increased by 10 to 20 percent per watt of power consumed," says Wang. "The greater number of cores per CPU and support for more memory are the best features of AMD processors.

Cost performance per socket is better too. For the same number of cores, we found that one socket performs almost 10 percent better and the cost is lower. In our experience, the energy efficiency is more than 30 percent better when running 4th Gen AMD EPYC processors. With the most advanced TSMC fab, more than 90 percent of the workload now runs on 4th Gen AMD EPYC CPUs.

The TSMC IT department now has close to 20,000 servers powered by AMD EPYC CPUs across our three workload areas, with 6,600 already powered by 4th Gen AMD EPYC CPUs."

TSMC is using 4th Gen AMD EPYC 9124 and 9354P processors for its Kubernetes general worker nodes, 9254 for Kubernetes database nodes, and 9254 or 9454P for Cassandra nodes. "We will continue to deploy AMD CPUs in our data centers because in our experience they are better in terms of cost, performance, and computing power per watt," said Wang. "More than 90 percent of the X86 servers we are purchasing now use 4th Gen AMD EPYC CPUs. We will keep a close eye on the next-generation products from AMD."

ESMC breaks ground on Dresden Fab

ESMC – a joint venture between TSMC, Robert Bosch GmbH, Infineon Technologies AG and NXP Semiconductors N.V. –held a groundbreaking ceremony this summer to officially mark the initial phase of land preparation for its first semiconductor fab in Dresden, Germany. The event brought together government officials, customers, suppliers, business partners and academia to celebrate a milestone in establishing what will be the EU's first-ever FinFET-capable pure-play foundry.

"Together with our partners, Bosch, Infineon and NXP, we are building our Dresden facility to meet the semiconductor needs of the rapidly growing European automotive and industrial sectors," said TSMC Chairman & CEO C.C. Wei. "With this state-of-the-art manufacturing facility, we will bring TSMC's advanced manufacturing capabilities within reach of our European customers and partners, which will stimulate economic development within the region and drive technological advancements across Europe."

When fully operational, ESMC is expected to have a monthly production capacity of 40,000 300mm (12-inch) wafers on TSMC's 28/22 nanometer planar CMOS and 16/12 nanometer FinFET process technology, further strengthening Europe's semiconductor manufacturing ecosystem with advanced FinFET transistor technology. Total investments are expected to exceed 10 billion euros consisting of equity injection, debt borrowing, and strong support from the European Union and German government.

The new facility is expected to generate around 2,000 direct high-tech professional jobs. Additionally, each direct job created by the project is expected to stimulate the creation of numerous indirect jobs throughout the EU supply chain, bolstering the region's economy. ESMC will uphold TSMC's standards of sustainability and environmental protection. In line with this mission, ESMC and its partners are dedicated to constructing a green fab that utilizes both existing and cutting-edge techniques to optimize conservation. This includes energy-efficient construction, water reclamation, and obtaining LEED certification.

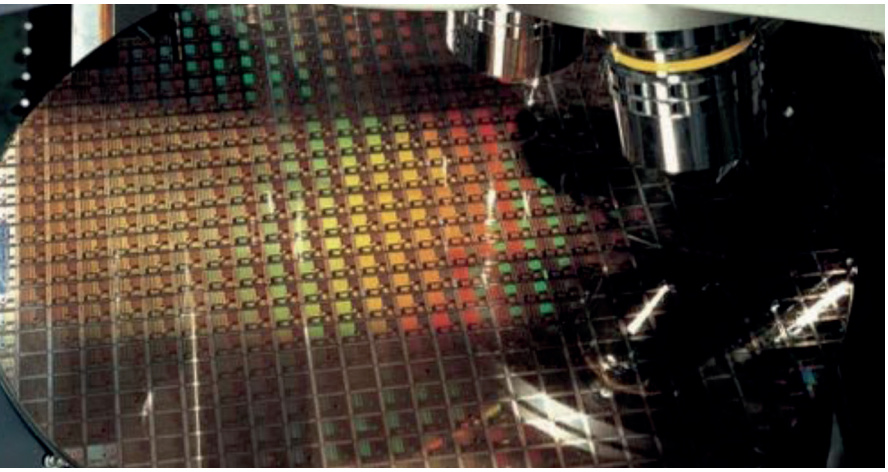
The establishment of ESMC exemplifies the strength of TSMC's Grand Alliance, a cornerstone of innovation within the semiconductor industry. This alliance has driven groundbreaking advancements, bringing together TSMC's partners for a new level of collaboration. The investment in ESMC signifies not just a deeper commitment to this strategic partnership, but also underscores TSMC's unwavering dedication to nurturing innovation across Europe. Construction is expected to start later this year.

TSMC collaborates with Ansys and Microsoft

ANSYS and TSMC have announced a successful pilot with Microsoft that significantly speeds-up the simulation and analysis of silicon photonic components. Together, the companies achieved over 10X speed-up of Ansys Lumerical FDTD photonics simulation via Microsoft Azure NC A100v4-series virtual machines, powered by NVIDIA accelerated computing running on Azure AI infrastructure. PICs are integral to applications across industries, including data communications, biomedical tools, automotive LiDAR systems, artificial intelligence, and more.

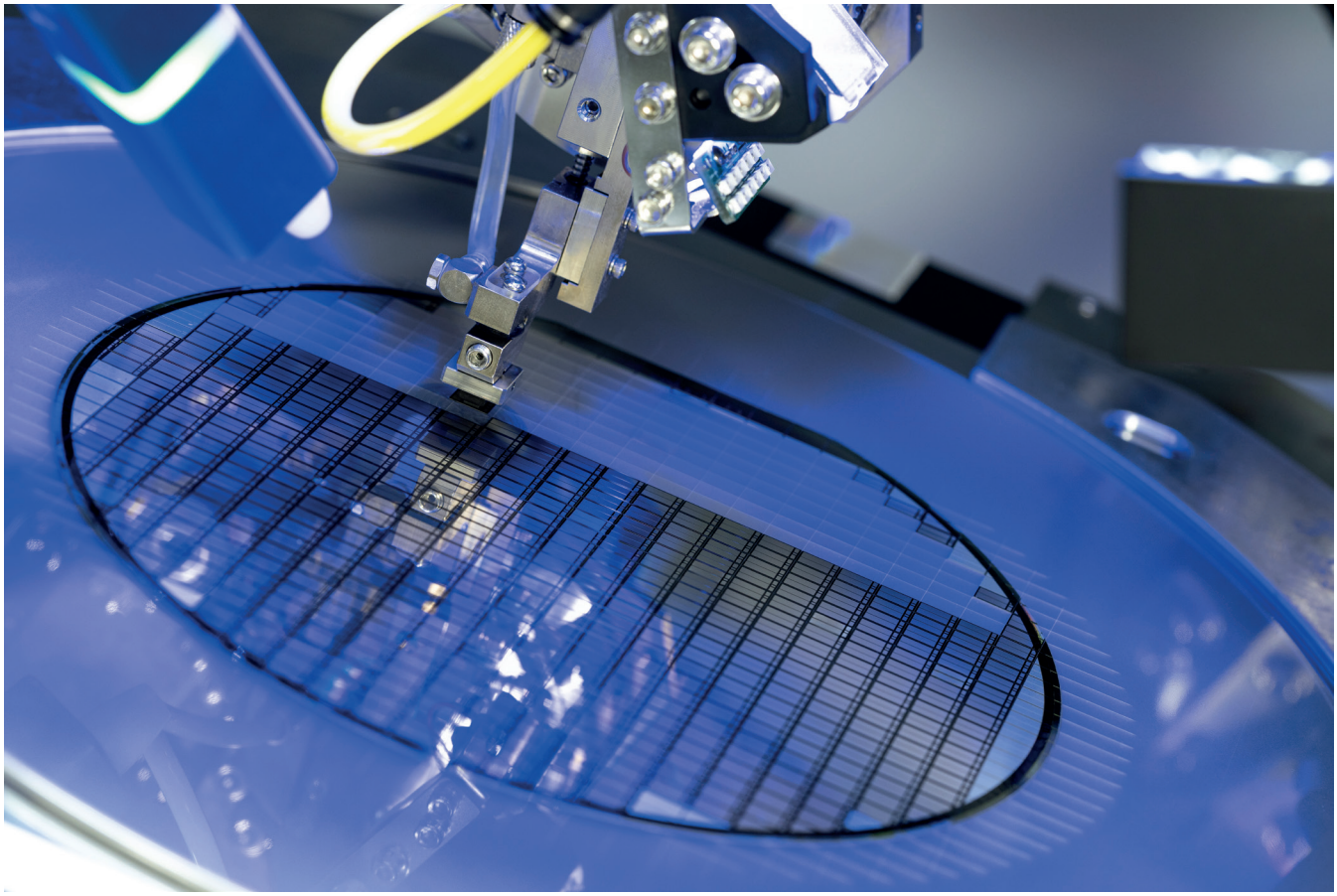
Silicon PIC, a type of optical communications that enables data to travel farther and faster, is integral to hyperscale data centers and Internet-of-Things applications. Combining photonic and electronic circuits is a painstaking task requiring precise multiphysics design and fabrication. A minor misstep can create continuity challenges within chips, which can result in added cost and timeline setbacks up to several months. To alleviate challenges and unlock the ultra-bandwidth capabilities of silicon PIC, TSMC collaborated with Ansys to speed-up Lumerical FDTD simulations using highly efficient Azure virtual machines that use NVIDIA GPUs. Azure NC A100v4 VMs executed the simulations and identified optimal resources that balance cost with performance. The overall result is seamless deployment, graphical interface access, scaling of distributed simulations, and post processing for large datasets in cloud environments. For a consistent end-to-end digital engineering workflow, Azure Virtual Desktop provided a seamless transition to the cloud by delivering the same user experience as on a desktop.

"The size and complexity of our multiphysics silicon solutions makes the process of simulating all possible parameter combinations challenging," said Stefan Rusu, head of silicon photonics system design at TSMC. "This latest collaboration again highlights that Ansys effectively harnesses the latest cloud infrastructure and techniques to deliver powerful, predictively accurate solutions that produce results in a fraction of the time." Deploying Lumerical FDTD on the cloud enables designers to swiftly identify optimal chip designs that account for the multiphysics challenges related to combining photonic circuits with electronic circuits.



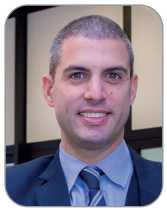
"It has always been the policy of the TSMC IT department that we use the latest products to enhance the performance of our data centers," said Wang. "AMD products are ideal for cloud-native environments because of the core density and support for large amounts of memory. It's ideal for multi-tenant and multi-tasking environments. The cost is not high, either."

"We have a very smooth collaboration partnership with AMD," concludes Wang. "These products meet our performance and cost requirements very well. We are looking forward to the latest GPUs from AMD, including the Instinct MI300X with faster speed and higher performance. Then we can deploy AMD technology to even more of our workloads."



Test early and test often

EMANUELE BARDO, VICE PRESIDENT FOR THE SEMICONDUCTOR AND MEMS TEST BUSINESS UNIT AT SPEA, talks to Silicon Semiconductor Editor, Philip Alsop, about the importance of power semiconductor testing. He also explains the company's expansion plans in Asia, and outlines SPEA's ongoing track record for innovation, sharing some fascinating future roadmap plans.



PA: *Power semiconductors are very much in the spotlight as the global focus on electrification is increasing, I won't say exponentially, but very significantly?*

EB: Yeah, this is exactly what SPEA is seeing. We are seeing an exponential global growth in the power segment, driven by three major factors - electrification, so EV and hybrid cars - as well as all of the business related to energy saving for consumers, as well as for solar panels. We see this trend growing all over the world, so in the United States, in Europe. But the biggest growth that we have seen is in Asia, and China in particular. I think this is well known. The investment made by Chinese companies in terms of power, with the support of the Chinese government, has been extremely significant in the past years. And this has been reflected in the amount of capital equipment that has been purchased and delivered.

PA: *Alongside this electrification and the growing importance of power semiconductors, it follows that power semiconductor testing is becoming increasingly important in this world. In simple terms, we're looking at performance and reliability when it comes to power modules or wider solutions?*

EB: Correct. Being a brand new business, there was not the culture of high power testing consolidated in the same way it is today consolidated for memory or for mixed signal or for high performance digital. For us, this was a big challenge because first of all, we have to educate our customers in terms of the need for testing and how to test the products. The second big challenge, as you correctly mentioned, power modules - our products can go up to 10K volt, 20K volt, 10K amp. So, it is a completely different way of conceiving the test equipment because the reliability and the safety become two of the major items on which we need to focus as well

as, of course, the performance, because all these products that are used - especially in the automotive market and especially the silicon carbide products - are extremely high voltage products with an extremely very fast switching time. The challenge is on all the elements - the reliability of the equipment, the safety of the equipment, as well as the technical performance. On top of this, educating the customer that testing is needed in all these areas.

PA: *A single fault or a faulty component can ruin a power device or power solution - there are a range of damaging consequences?*

EB: Absolutely. A faulty component can cause an explosion. This is the reason why testing is needed from the very beginning. We don't want the customer to assemble a full module and then discovering that the module is failing with consequences of, say, an explosion and with a cost that is significantly high. If you compare the average cost of a semiconductor chip and the cost of a power module, there is a factor of 100. It is absolutely vital to start testing in all the steps of the production. Testing on the wafers, testing at a single die level, the so-called KGD, testing on the DBC, so on the substrate, and finally testing the module and the package, in order to have the maximum yield in every step and in order to move the chips that have passed the test to the next step of the process.

PA: *You've explained the need for continuous testing throughout the process. The traditional tests would include static parameter testing? Do you want to say anything about the benefits and any drawbacks of this?*

EB: Historically, with this type of product, they were always doing the so-called static test. Also on the wafer, the majority of the tests are purely static. They simply verify that the component has not suffered major damage. When we say static test, it means applying high voltage in a static way and to measure a leakage current or to apply a high current and measure a voltage, as well as measuring the gate threshold voltage of the chip. These are tests that give you good information about the reliability of the process. However, static parametric test is not a functional test. We are not putting the device in real working conditions. If you think that these are IGBTs or MOSFETs, which are switches, the real working condition is to switch using the gate and to switch on and off. And when you switch on and off, you have a high voltage and high current that are flowing simultaneously in the device through the test equipment. And of course, at that point you have to measure all the parameters of the switching. The time that is necessary to switch from low current to high current and vice versa.

This brings the challenge which is the next step - the so-called dynamic test or switching test with the top performance that is the short circuit test. The problem, the technological problem, is that when you test on the wafer, some types of dynamic testing are not possible due to the environment, especially due to the parasitic element that is the chuck where the wafer is placed on. And this brings the need, the special need for this product to have an additional step of testing that is the bare die, the so-called KGD. Being able to extrapolate the single die from the wafer, at that point, it is possible to test static and dynamic directly on the die, to really check 100% the functionality of the product. Of course, this brings a big issue in real capability - you can imagine if one die is failing, you have a probe card with needle contacting and, if the equipment is not properly designed, you risk melting the needle as well as the wafer and all the conducting portion. That is the big challenge.

PA: *You've explained the need for the dynamic performance evaluation. There's a need for isolation testing as well. Can you say a little bit about where that comes into play?*

EB: The isolation test is a test that is not performed at high level because it's a test that measures the isolation through the external packing. But for sure, when you go in the final stage, so in the assembling the packaging, that can be a standard package like in the past or a more complex power module, the production line has to be equipped with isolation testing that has to be independent due to the fact that all the pins of the device have to be shorted together. This brings a challenge for our customers, because it's a separate station with an additional cost, of course, and both static and dynamic testing, not necessarily only done at ambient, but, in certain situations, also done at temperature because we are talking of electrification and the majority of this business is related to automotive. And, as a whole, for the automotive requirement, the temperature testing is becoming much, much more important to guarantee the reliability over the time of the final product.

PA: *To re-emphasise, you've outlined the steps of the testing, but the most important thing overall is to ensure that the testing is carried on throughout the process, as the solution is built up You're testing at every stage and your message is 'Test early and test often'?*

EB: Correct. So, don't just test the final product, because you cannot guarantee the performance as well as the reliability over the time of the full process, and it will absolutely not be cost-effective. Test early and test as much as you can in all the steps in order to have the better yield and in order to have a product that has a high reliability in the field and doesn't risk premature failing.

PA: *Presumably, the basic problem is if you only test at the end and you find a problem, it's very difficult to then chain back to find out where the problem might lie, whereas if you're testing frequently, you will hopefully come across a problem early on, and therefore you can deal with it so that you can then carry on building the solution, confident that it's going to be working, as opposed to, suddenly at the end it doesn't work, and then how do we find the problem?*

EB: Exactly. Because, if you only do the final testing of the model and you discover that it has a yield of 60% or 70%, you don't know which step(s) of the previous processes are causing this low yield. It's very difficult to feedback on your internal process. Having the testing on wafer, on single die, on substrate, on so-called DBC, and finally in the module, you are able to feedback each step of your process and to understand which one has to be improved.

PA: *In terms of the solutions available to do the testing that we've discussed, I guess SPEA is very well positioned for testing power semiconductors. I know you have the slogan or your concept is reimagining semiconductor testing. Can you just talk us through the solution or solutions that you think are particularly well suited to the situations we've discussed?*

EB: If I look at the data, SPEA is number one in this specific field of high power testing. High power testing is knowledge that you cannot build in a very short time. We have departments that have studied the high power instrumentation of our equipment almost since the foundation of SPEA, because high power equipment has to be conceived and designed as high power since the first drawing and the first schematic of the equipment. It cannot be a mixed signal equipment where you add a certain power instrumentation. It will not work. The flexibility of the solutions we have in the field, gives our customers the possibility to have a single model of machine extremely scalable, so capable to be configured for each step of the testing, with even a single software and a single test programme that can run from wafer level until the package test. This is extremely important for our customers because they have the same machine that can perform all the steps of testing, and they can easily compare data, limits, and capability of testing. This has placed SPEA as a leader in the market for high power testing. For example, almost 40% of the EV market in China is tested on our machine.

PA: *So far we've concentrated on power semiconductor testing. I know that's a major focus for yourselves, but you are doing other things as well. Perhaps we can have a brief look at some of those - areas like automatic probe card testing, I think there's some MEMS, environmental sensors testing, and we can't ignore that the world is going 'AI mad' and there's a need for testing for microchips for AI applications. Clearly, they're big subjects in their own right. But can you at least give us a flavour of what you're involved with in terms of each of these?*

EB: There are two market segments where SPEA is leader. It is related to high power, as we correctly mentioned, and everything is sensor and MEMS. You mentioned environment. It is just one of the latest challenges that we are faced with. We have been awarded by many companies as a supplier to test, accelerometer, gyroscope, pressure sensor, high-g sensors, and so on.

These two represent almost 50% of the turnover for SPEA. Then, we are growing all over the world, the business related to analogue mixed signal, as well as high computing digital devices. If you think, all the AI chips are chips that must have a big capability to transfer data at high speed with a lot of power supply. And this is a market segment that for us is growing significantly. On top of this, we have recently approached the market with some, let's say, very innovative equipment. For example, with a wafer prober it is no longer just a single probe card, as is already well known in the market.

There are certain devices, and this is one application, for some power chips like IGBTs or diodes, where there can be a certain technological advantage to probe both sides of the wafer, so top and bottom. We have also introduced equipment that has multi-probe cards, up to eight probe cards that can fly on the wafer and contact top and bottom. It's a new technology that we strongly believe will grow in the future.

PA: *Before we finish, I know SPEA Thailand is a new-ish venture, so it'd would be good to understand what's going on there. And, if memory serves, I think it's the 10th anniversary of your presence in China. I believe as part of the celebrations for this, you've actually expanded*

The big business of the analogue mixed signal is the area where SPEA has the biggest potential, we are currently coming on the market with the next generation analogue and digital card with a disruptive innovation in terms of cutting cost by a factor of four. And we are working with several customers in benchmarking mode because we are extremely confident that we can play an extremely important role for them for the future in terms of cost of test reduction

significantly the Suzhou facility. If you can talk us through a little bit about Thailand and then China?

EB: SPEA Thailand was opened at the beginning of May of this year. Thailand is one of the biggest installed bases for SPEA in Southeast Asia. SPEA has been present in Singapore for more than 20 years, and we also have service centres in Thailand, in Philippines, and in Malaysia. The decision of the company has been for a massive investment, first in Thailand and the Philippines will follow, to create offices, but especially to create the hub for all of our repair centres for Southeast Asia. So, the opening of SPEA Thailand is really important and strategic for the growth of all the businesses in Southeast Asia in order to better serve our tremendous installed base.

In terms of China, all the SPEA management was in Suzhou recently. SPEA has been present in China for 10 years and we celebrated this anniversary. Alongside this celebration, we also had a ceremony to open a new facility in Suzhou, a 2000 square metre facility with a demo room with more than 30 machines, a repair centre that will support all the mainland China business, and a plan to grow our personnel up to 200 people in China in terms of customer support, application and sales.

Today, China is the number one market in terms of revenue for SPEA. Historically, the relationship between Italy (we are an Italian company, of course!), and China has always been extremely good. And this positions SPEA extremely well for partnership with a major Chinese company. As you know, investment in China for independence on the semiconductor side is extremely high at the moment. We already have partnerships with a lot of companies, and we believe that this market will be an additional booming market for us in the next 10 years.

PA: *What we've discussed, you're clearly very busy at the moment already. There's plenty to keep you occupied. But, looking ahead, is there anything on the roadmap you're able to share?*

EB: Our R&D team is extremely busy in all of the market segments, I have to say. There are a lot of evolutions that are going on in the power segment, as we discussed before. The new challenges of the new generation of silicon carbide products, 3.3 kV, 6 kV, and even more, consequentially brings a new instrumentation that has to be brought to market – ideally, by offering our customers the possibility to use the big investment that they did in the past year, just by upgrading their machines.

The sensor business is a consolidated business that has a demand of cost of test reduction every year. And we are working with all our customers in order to always be able to offer them competitive advantages from that point of view.

The big business of the analogue mixed signal is the area where SPEA has the biggest potential, we are currently coming on the market with the next generation analogue and digital card with a disruptive innovation in terms of cutting cost by a factor of four. And we are working with several customers in benchmarking mode because we are extremely confident that we can play an extremely important role for them for the future in terms of cost of test reduction.

Let me say one more thing. 2024 for sure will not be remembered as the best year for the semiconductor industry in terms of revenue. But it's a very good moment for all our customers to have the possibility to re-evaluate and to select a new supplier. We have already won several benchmarks during this 2024, and we think that the second half will be as good as the first half from that point of view. So soon the book will be full of orders for the growth that we expect to come in Q1 of 2025.

PA: *One more thought, if I may. We've obviously talked about silicon a little bit, and you've mentioned silicon carbide, particularly relevant in power. What about gallium nitride? I have no idea whether that's on your roadmap or you're already doing it. If it requires a whole new level of testing, just anything you can perhaps share as to what gallium nitride means to you?*

EB: Let's say the base of the standard silicon carbide high power products continues. But of course, the GaN products are emerging. We are already testing several GaN devices at wafer level. We have the challenge of the high frequency and the high voltage mixed together that makes the testing extremely interesting from that point of view. Higher density and multi-site in terms of cost reduction is for sure the challenge we are facing, and that's what we will offer in the future.

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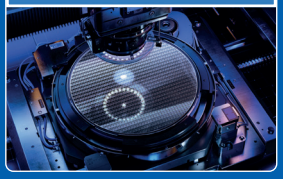

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