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VOLUME 46 ISSUE VIII 2025

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VIEWPOINT

BY PHIL ALSOP
EDITOR

Robotaxis and the AI opportunity: sorting the hype from the reality

A couple of recent episodes have served to highlight for me the continuing excitement and uncertainty that surrounds the future of our digital world as AI looms ever larger.

I was lucky enough to travel to Phoenix for the recent SEMICON West event, which seems to have been universally acknowledged as the biggest and best of these events for quite some. It will be interesting to see where else this event will visit in the coming years, or if San Francisco and Phoenix will remain the alternate year homes for some time to come.

Anyhow, arriving late on the Sunday, we had a day's leisure on the Monday, the day before the event, and so my colleague, Shez, and I decided to visit one of the out of town shopping malls. Uber ordered, and excitement from Shez as he realized that a Waymo robotaxi would be picking us up from our breakfast location. From the picking us up, the journey and the arrival at our destination the whole experience seemed faultless, although when I WhasApped my wife during the ride, she did scream at me to 'get out now'!!

For the rest of our stay, Shez summoned Waymos via their app and it all seemed very normal and safe.

Pre this direct experience of robotaxis, I was extremely sceptical as to the future of the driverless vehicle, but I am now a convert to the technology – although not quite as big a fan as Shez, who can't wait for them to arrive in the UK next year and seems likely to start up the first official Waymo fan club!

I shall leave the profound implications of the driverless vehicle future for another time, but there seems little doubt that robotaxis and fully autonomous vehicles for private citizens are here to stay.

Episode number two, a recent interview with a power grid expert who opined, with sound reasoning, that, in the UK at least, the required data centre capacity for AI – training and

inferencing – may well be somewhat over-estimated. The suggestion being that there are many data centre owners/operators chasing the same business, so the size of the anticipated market is significantly exaggerated. The good news would seem to be that the energy required to power the AI era is not nearly as much as currently anticipated. The less good news...maybe the number of chips, power electronics solutions and the like required to support the AI explosion will not be as high as currently expected.

Add in the ongoing geopolitics and the impact of tariffs – actual and threatened – and the semiconductor industry continues to face an exciting, if volatile, future. And if AI numbers do dip, then the autonomous vehicle market could just make up some of this shortfall.

I'll spare you my Third Man/Harry Lime quote about Italian turmoil leading to the renaissance and hundreds of years of peace in Switzerland leading to the cuckoo clock (I paraphrase somewhat), but there's no doubt that the pace and scope of innovation in our industry is increasing to meet the challenges of our time.

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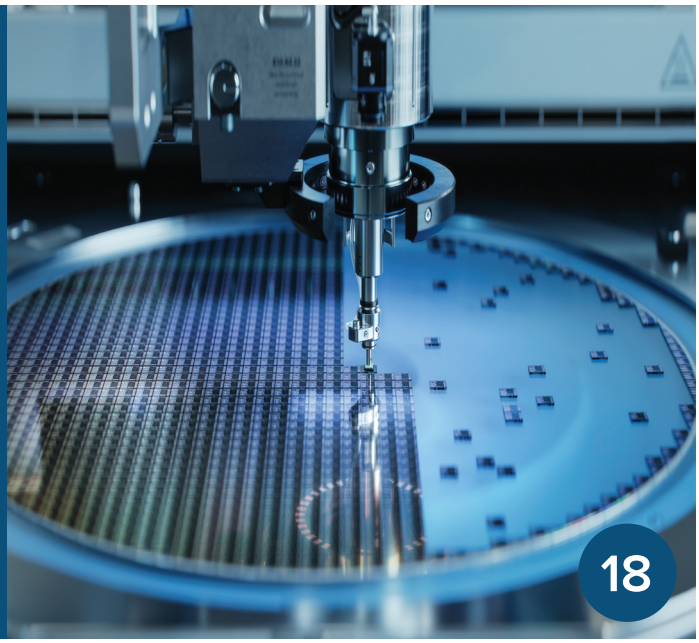
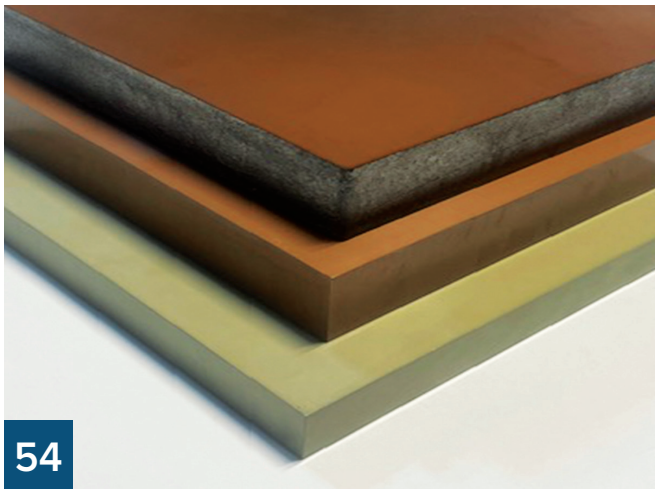
COVER STORY

Trends and drivers for next-generation process vacuum

Edwards Vacuum examines several emerging production processes with an eye towards identifying trends that will drive the development of next-generation vacuum systems.





NEWS

Publisher Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Editor Phil Alsop phil.alsop@angelbc.com
Sales & Marketing Manager Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214
Chief Executive Officer Sukhi Bhadal sukhi.bhadal@angelbc.com +44 (0)2476 718970
Chief Technical Officer Scott Adams scott.adams@angelbc.com +44 (0)2476 718970

Directors Jackie Cannon, Sharon Cowley

Published by Angel Business Communications Ltd,
6 Bow Court, Fletchworth Gate, Burnsall Road,
Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970 E: info@angelbc.com

Silicon Semiconductor is published ten times (6x print and 4x video issues) a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £50.00 per annum (UK) , €60.00 per annum (Europe), $90 per annum (air mail)(USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher. Every effort has been made to obtain copyright permission for the material contained in this publication. Angel Business Communications Ltd will be happy to acknowledge any copyright oversights in a subsequent issue of the publication. Angel Business Communications Ltd © Copyright 2025. All rights reserved. Contents may not be reproduced in whole or part without the written consent of the publishers. The paper used within this magazine is produced by chain of custody certified manufacturers, guaranteeing sustainable sourcing. US mailing information: Silicon Semiconductor, ISSN 1096-598X, is published 5 times a year by Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Rd, Coventry CV5 6SP. UK. Airfreight and mailing in the USA by agent named World Container INC 150-15, 183rd St, Jamaica, NY 11413, USA. Periodicals Postage Paid at Brooklyn, NY 11256. POSTMASTER: Send address changes to Silicon Semiconductor, Air Business Ltd, c/o World Container INC 150-15, 183rd St, Jamaica, NY 11413, USA.

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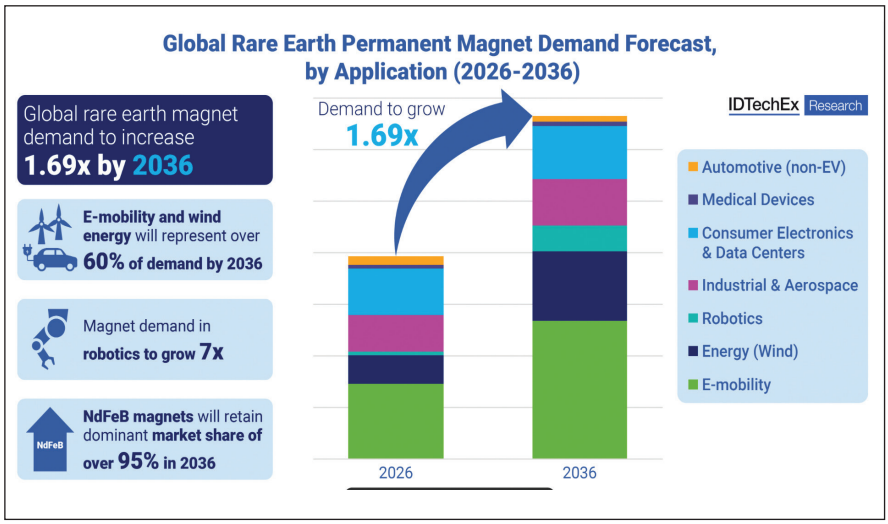
US-China trade war drives investment in domestic rare earth supply

Rare earth elements and critical minerals are now frequently featured in global news cycles due to the national security and economic impacts of increasing supply disruption.

Growing export restrictions placed on defense-related rare earth materials from China at a time of multiple international conflicts underscores growing demand in the US and Europe to develop alternative supply.

2025 is set to be an inflection point, as a year of tariffs and trade wars drive record investment into strategic Western rare earth supply chains. IDTechEx's latest research, 'Rare Earth Magnets 2026-2036: Technologies, Supply, Markets, Forecasts' explores rare earth investment and supply chain partnership trends driven by increasingly restrictive global rare earth supply.



China's latest export restrictions on critical rare earth elements applies yet more pressure to what are already tightly controlled materials. The latest round of restrictions extends to erbium, europium, holmium, thulium, and ytterbium, targeting defense and semiconductor chip applications. This announcement follows controls placed on neodymium magnet materials in April 2025, which sent the automotive industry scrambling for alternative supply and notably caused Ford to temporarily shut down some of its production plants.

Market disruption caused by export restrictions is unavoidable due to a lack of alternative rare earth sources and an absence of viable alternative materials in many integrated applications.China mines 69% of rare earth minerals, processes 88% of rare earth concentrates, and refines 90% of rare earth metals globally, with limited additional capacity available from other regions. On the demand side, rare earth magnets remain a dominant technology in applications such as high performance electric motors. Despite developments in rare earth-free motor technologies, IDTechEx forecasts that over 70% of electric vehicle motors will rely on rare earth permanent magnets over the next decade.

The US is the first (and best positioned) player addressing rare earth supply risks, announcing significant public investment into domestic production. In July 2025, the US Department of Defense (DoD) entered a public-private partnership with MP Materials, North America's only major rare earth mine. The partnership includes capital investment of over $400M and important rare earth purchase price commitments to ensure the mine's profitable operation.

The US is in a strong position to leverage its established rare earth mining base to expand downstream refining and production capacity, with investment and partnership trends beginning to reflect this. USA Rare Earths announced it will acquire UK-based rare earth refiner Less Common Metals for approximately $220M, securing supply of crucial feedstock for its planned 5,000 tonne magnet production facility in Stillwater, Oklahoma. In August, Noveon Magnetics also announced a multi-year supply agreement with General Motors to deliver rare earth magnets for its SUVs and trucks. The US rare earth ecosystem is moving fast to capitalize on its key advantage: the potential to insulate every supply chain stage from external dependence on China and mitigate the impact of future export controls.

The European rare earth market looks to be keeping pace with the US, despite the absence of established domestic rare earth mines. French-based Carester has secured €216M in financing from the French government and Japanese investors to build its separation plant capable of processing 5,000 tonnes of mineral concentrates and 2,000 tonnes of recycled magnets annually. Carester will join Solvay to offer separated rare earth products to European magnet producers Vacuumschmelze and Neo Performance Materials Silmet, the latter of whom began magnet production at its site in Estonia in 2025. Without primary mineral supply within Europe, the key to success will be securing offtake agreements with external partners while developing new secondary rare earth sources, such as recycled waste magnets and mining tailings.

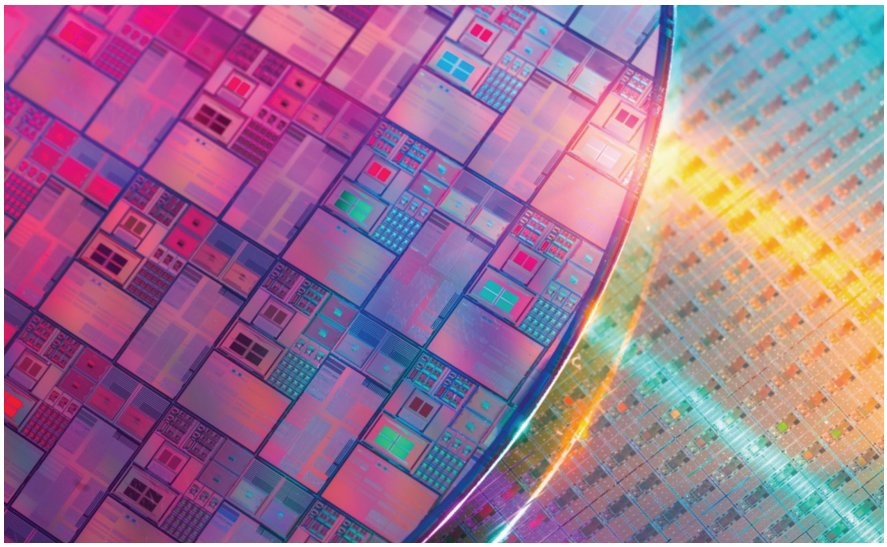
TechInsights announces 2026 Semiconductor Market Outlook Report Series

Reports provide forward-looking insight into the state of the semiconductor sector across a number of technologies and markets.

TechInsights has released its 2026 Outlook Report Summary that covers key technology and vertical market trends and forward-looking expectations for next year.

According to David MacQueen, TechInsights' director, executive insights, "Datacenters will continue to drive growth in 2026, particularly for accelerators and processors and support for large language models (LLMs), resulting in a bottleneck for power. Despite on-device inference benefits like lower costs, power efficiency, and privacy, cloud AI will be the key market driver, and the shift to autonomous edge machines will not become a mass-market trend in 2026."

The industry will reach a pivotal moment in 2026 as it transitions from FinFET to gate-all-around (GAA) transistors with next-generation 2nm manufacturing processes, promising lower power consumption and improved performance. High-bandwidth memory (HBM), the most high-margin memory product ever, used almost exclusively for artificial intelligence (AI) accelerators, continues to drive the memory market upward. In the future, it could be replaced by high-bandwidth Flash (HBF) memory; TechInsights expects to see the release of HBF prototypes in 2026. Additionally, next year promises to be the inflection point for silicon photonics, in the form of co-packaged optics (CPO), and glass substrates, which help to improve data transfer performance while addressing heat dissipation and power usage.



"The rapidly shifting technology landscape seems almost slow compared to the pace of change happening at a global political level, with tariffs and trade restrictions creating a fluctuating business environment," MacQueen added. "The industry will have to navigate an increasingly fractious and fragmented geopolitical landscape. Tariffs and export restrictions, particularly affecting trade involving the US and China, are more likely to escalate than abate in 2026."

TechInsights will release its semiconductor market outlook report series, which covers memory, advanced packaging, artificial intelligence (AI), automotive, PC/laptop, mobile and more, from October through November, according to the release schedule below. The TechInsights Outlook Summit Webinar Series will provide attendees with a summary of the reports and will be held from October 15, 2025 through January 21, 2026.

Access all reports for free here. The 2026 Market Outlook Report release schedule is as follows:

- LIVE: Advanced Packaging report release
- LIVE. Memory report release
- LIVE. AI report release
- LIVE: Compute report release
- LIVE: Power report release
- LIVE: Sensor report release
- Oct. 22: Automotive report release
- Oct. 29: Manufacturing report release
- Nov. 5: PC/Laptop report release
- Nov. 5: Connectivity report release
- Nov. 12: Mobile report release
- Nov. 19: Consumer electronics report release

The rapidly shifting technology landscape seems almost slow compared to the pace of change happening at a global political level, with tariffs and trade restrictions creating a fluctuating business environment

Bosch, Volkswagen, Nokia and Europe's Tech Giants unite to secure photonics future in FP10

Bosch, Volkswagen, Nokia, ZEISS, TRUMPF and other industry giants urge the EU to create a €2 billion photonics programme in FP10.

SOME of Europe's biggest industrial names, including Bosch, Volkswagen, Mercedes-Benz, Nokia Bell Labs, ZEISS, TRUMPF, and EssilorLuxottica, have joined forces to urge the European Commission to place photonics at the heart of the next EU Framework Programme (FP10).

In a Joint Statement released, leaders from across Europe's defence, automotive, healthcare, manufacturing, and telecoms sectors warn that without a bold and dedicated strategy, Europe risks falling further behind China and the US in the global race for photonics – the light-based technologies that underpin 20% of the EU economy.

With FP10 set to shape Europe's research and innovation agenda for 2028–2034, industry leaders argue that only a dedicated programme can ensure Europe's photonics sector remains globally competitive – powering breakthroughs in AI, quantum, energy, healthcare, mobility, and beyond.

"Photonics is the invisible force behind everything from AI and quantum computing to secure communications, energy, healthcare, defence, and mobility," said Dr Lutz Aschke, President of Photonics21.

"But Europe is at risk of losing its critical, competitive edge unless FP10 delivers a stand-alone €2 billion photonics programme, capable of unlocking €6-8 billion in industrial co-investment."

The signatories stress that photonics is one of the few digital technologies where Europe has long been a leader, but warn that China's share of the global photonics market has surged from 10% in 2005 to 32% in 2022, while Europe's has slipped to 15%.

"Photonics is a strategic technology for Europe's prosperity, autonomy, and security. This joint statement shows that Europe's industrial leaders stand united," said Dr Aschke.

The joint statement calls on the EU to:

- Establish a €2 billion stand-alone photonics programme under FP10.
- Launch Photonics Grand Challenge Proposals in fields such as AI, space, quantum, and defence.
- Strengthen resilient European supply chains for critical photonics components and materials.

The request brings together voices from across the European economy – from defence leaders such as Diehl Defence and WB Electronics, to automotive innovators at Volkswagen, Scania, and Mercedes-Benz, to healthcare pioneers ZEISS and EssilorLuxottica, and research powerhouses Nokia Bell Labs and ams-OSRAM.

The Robotaxi race is heating up globally in 2025

2025 has been a massive year so far for SAE level 4 autonomous vehicles, including the first foray outside of robotaxis.

MARKET INTELLIGENCE firm IDTechEx's report, "Autonomous Driving Software and AI in Automotive 2026-2046: Technologies, Markets, Players", analyzes the progress of robotaxi services to date, and forecasts the software revenue attributed to robotaxis up to 2046, split by region. The role of these different players and their approaches are analyzed, compared, and used to forecast the overall autonomous driving software market.

Increased competition in the US

Waymo has established itself as the leader of robotaxi services, operating in Phoenix, San Francisco, Los Angeles, Atlanta, and Austin, and has even established partnerships with Uber and Lyft, the two major ride-hailing companies, which could be considered competitors to Waymo's business model. With testing being done in Tokyo, it has also recently begun its first activities in international markets.

Tesla launched its robotaxi service in June 2025 and later increased its operational area to approximately 170 square miles in Austin, Texas. In September, these rides were opened to the public, and no longer have an onboard human supervisor, while maintaining the remote operators that all robotaxis have. However, more time is required to ascertain whether the technology is mature enough to scale.

Two other companies have opened robotaxi services in the US this year: Zoox and May Mobility. Unlike other companies, Zoox's robotaxi has been built from the ground up to be an autonomous vehicle. While Waymo's robotaxis are currently retrofitted Jaguar I-PACEs, and Tesla uses its Model Y, Zoox's robotaxi doesn't have a steering wheel, pedals, or a driver's seat. May Mobility began operating a robotaxi pilot program in September 2025 in collaboration with Lyft,

using modified hybrid Toyota Sienna minivans. Since the exit of Cruise in December 2024, the only company operating robotaxis commercially was Waymo. In the past two months, the activities of other companies suggest that robotaxis could be set to take off. IDTechEx forecasts that by 2046, the US will make up almost a quarter of the software revenue from the robotaxi market globally.

China's Market Continues to Grow, Europe Will Expand

With the second-largest population in the world, the addressable market for robotaxis in China is massive. In terms of scale, Waymo's only current competitor is from Apollo Go, owned by technology giant Baidu. Apollo Go is operational in over twelve Chinese cities, including Beijing, Shanghai, Shenzhen, and Wuhan. With a fleet of over one thousand vehicles, it has indicated its intention to serve foreign markets, targeting the UK and Germany by 2026. Considering the current state of the European market and the activities of European companies such as Wayve and Motor AI, Europe could become a key battleground for technology superiority in the future.

The domestic market also has players with hundreds of vehicles, such as Pony.ai and WeRide, and upcoming companies such as Momenta and Black Sesame that are developing autonomous vehicle technology.

With such a competitive domestic market, IDTechEx expects China to make up over half of the robotaxi software revenue in 2046.

Another player, AutoX, has come out with the world's first private SAE level 4 autonomous vehicle, under the new brand name Tensor. Under the name AutoX, the US-based company closed its robotaxi service in China two years ago. It remains to be seen whether this vehicle will enter the market, what it would cost, and how it would handle different responsibilities and liabilities associated with a private autonomous car.

IDTechEx's projections for software revenue from autonomous vehicles over the next twenty years, by region. Source: Autonomous Driving Software and AI in Automotive 2026-2046: Technologies, Markets, Players.

ESIA discusses Europe's semiconductor future

Semiconductor leaders unite to shape the next policy framework in support of Europe's chip ambitions.

THE EUROPEAN SEMICONDUCTOR INDUSTRY ASSOCIATION (ESIA) recently hosted a high-level policy event in Brussels, bringing together key voices from industry and government to discuss the future of Europe's semiconductor strategy. The event, entitled "Next-level policy blueprint for Europe's chip ambitions", marked a timely intervention as the review of the EU Chips Act officially gets underway.

Frédérique Le Grevès, STMicroelectronics EVP Public Affairs Europe and President of ST France, who serves as Vice-President of ESIA, declared: "Europe has the technologies, the talent, and the ambition to lead in key segments of the semiconductor industry in Europe – but we must move faster.

The revision of the EU Chips Act is an excellent chance for the EU to develop a vision for an industrial strategy and implement it in a way that strengthens the European semiconductor ecosystem. Europe's strengths – in sensors, microcontrollers, power semiconductors, edge AI – align perfectly with the needs of key end markets such as AI infrastructure and applications, automotive, factory automation, robotics, connectivity, energy infrastructure, aerospace, and defence. If a second EU Chips Act helps us scale those strengths, we will be in a better position to lead in key technologies underpinning the next wave of global growth."

During the high-level event, policymakers, industry leaders, and stakeholders engaged in a forward-looking dialogue on how the semiconductor ecosystem in Europe can be strengthened. The event featured keynote speeches from Member of the European Parliament Matthias Ecke (Socialists & Democrats, Germany), and Dr Andreas Schumacher, Executive Vice-President and Head of Strategy, M&A at Infineon Technologies.

The subsequent panel discussions explored how Europe's semiconductor policy framework must evolve to meet the challenges of global competition, technological sovereignty, and supply chain resilience. It featured perspectives from the manufacturing side through Ms Le Grevès, as well as up- and downstream views from CEA-Leti Chief Executive Officer Sébastien Dauvé and Pierre Millette, Chief Technology Officer at the European Automobile Manufacturers' Association (ACEA). Furthermore, Dr Tim Schulze, Senior Policy Officer at the German Federal Ministry for Economic Affairs and Energy, provided policymakers' insights from the EU's most populous Member State. Discussions focused on the need for a more agile, innovation-driven approach that supports both industrial growth and strategic autonomy.

The event concluded with closing remarks from Pierre Chastanet, Head of Unit for Microelectronics and Photonics at the European Commission, who reaffirmed the Commission's commitment to working closely with stakeholders to shape the next phase of semiconductor policy. As Europe revisits its Chips Act, ESIA's event served as a timely exchange for aligning public and private sector ambitions, ensuring that the continent remains competitive and resilient in a rapidly evolving global landscape.

During the high-level event, policymakers, industry leaders, and stakeholders engaged in a forward-looking dialogue on how the semiconductor ecosystem in Europe can be strengthened. The event featured keynote speeches from Members of the European Parliament, and Infineon Technologies

Vacuum-sealed semiconductor tray market to hit $2.3 billion by 2033

According to Research intelo, the Global Vacuum-Sealed Semiconductor Tray market size was valued at $1.2 billion in 2024 and is projected to reach $2.3 billion by 2033, expanding at a robust CAGR of 7.5% during the forecast period of 2025–2033.

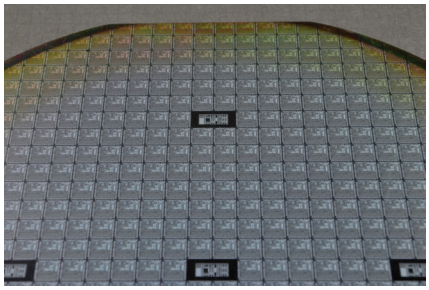
THE primary growth driver for the vacuum-sealed semiconductor tray market globally is the surging demand for advanced semiconductor packaging solutions, propelled by rapid advancements in consumer electronics, automotive electronics, and industrial automation.

As the semiconductor industry continues its transformation to support next-generation devices with higher precision and reliability, vacuum-sealed trays have become indispensable for safe wafer handling, chip packaging, and component storage. This market is witnessing increased investments in automation and material innovation to ensure contamination-free transportation and storage of sensitive semiconductor components, thereby fueling sustained growth worldwide.

The global semiconductor industry continues to grow rapidly, driven by rising demand for consumer electronics, automotive electronics, and advanced computing systems. As chips become smaller, more complex, and highly sensitive, protecting them during transportation and storage has become a critical challenge.

This is where vacuum-sealed semiconductor trays play a pivotal role. Designed to provide a controlled environment, these trays prevent contamination, moisture intrusion, and electrostatic damage, thereby ensuring chip reliability and performance.

The vacuum-sealed semiconductor tray market is witnessing steady expansion as manufacturers and suppliers align with the needs of semiconductor fabrication plants, assembly units, and packaging facilities. The growing focus on efficiency, sustainability, and advanced packaging technologies is further shaping the market landscape.



Key Drivers
Miniaturization of Semiconductors
The shift toward smaller and more powerful chips, such as those used in smartphones, wearables, and IoT devices, has increased the vulnerability of components. Vacuum-sealed trays safeguard these delicate semiconductors from dust, static, and oxidation.

Rising Global Chip Demand
With the semiconductor shortage exposing supply chain vulnerabilities in recent years, manufacturers are investing heavily in protection and logistics solutions. Vacuum-sealed trays ensure that chips reach their destinations without compromising quality.

Adoption in Automotive Electronics
The automotive industry's shift toward electric vehicles (EVs), autonomous systems, and advanced driver-assistance systems (ADAS) has spurred demand for high-reliability semiconductors. To maintain consistent quality standards, vacuum-sealed trays are becoming a crucial packaging solution.

Challenges
Despite promising growth, the market faces challenges such as high production costs and the need for customization. The design of trays varies based on chip type, size, and packaging style, making it difficult for manufacturers to standardize production. Additionally, the increasing emphasis on eco-friendly materials poses challenges for companies reliant on plastics and non-recyclable materials.

Technological Advancements
Technological innovation is reshaping the vacuum-sealed semiconductor tray market. Modern trays incorporate:
Electrostatic Discharge (ESD) Protection: Many trays are designed with conductive or dissipative materials to prevent electrostatic buildup, which can damage semiconductor circuits.

Moisture Barrier Films: Advanced sealing technologies ensure chips are shielded from humidity, crucial for devices used in medical and aerospace industries.

Automation-Friendly Designs:
Trays compatible with robotic handling and automated assembly lines streamline production and reduce operational errors.

The future of the vacuum-sealed semiconductor tray market looks promising, fueled by:
Growth of AI and IoT Devices: As billions of connected devices hit the market, the demand for semiconductors and consequently secure packaging will rise.

Sustainable Packaging Trends:
Companies are exploring recyclable and biodegradable tray materials, aligning with global sustainability goals.

Expansion of Global Semiconductor Supply Chains:
As governments and corporations invest in new fabs, tray manufacturers will find growing opportunities worldwide.

Semicon Coalition and industry: a united front to power Europe's semiconductor future

In a clear signal of unity and shared ambition, the 'Semiconductor Coalition Europe' has unveiled its Joint Declaration that seeks to strengthen and revitalise Europe's position in the global semiconductor industry

ALONGSIDE a broad alliance of semiconductor industry leaders issued its Endorsement, calling for bold action, proper preconditions, and a market-driven business case for Europe.

On the sidelines of the EU Competitiveness Council meeting, the Semiconductor Coalition Europe (or Semicon Coalition), supported by the EU Member States, presented their Declaration calling for a revised EU Chips Act, a little over six months since the initial formation and first Common Statement.

Their message is clear: semiconductors are vital to our society, our competitiveness, and our security. Also in attendance supporting this pivotal initiative was a broad alliance of over seventy semiconductor companies, industry associations, and research & technology organisations (RTOs) spanning the European and global value chains that have joined forces to back the Coalition's vision.

The signatories of the Industry Endorsement welcome and support the Coalition's initiative and urge them to immediately start the process of defining clear goals that are underpinned with a measurable execution strategy and developed in closest partnership with industry. More concretely, the undersigned call for bold action and clear ownership from the European Commission and Member States, the establishment of necessary regulatory, societal, and economic pre-conditions, and the development of a compelling, market-driven business case by the end of 2025.

As global demand for semiconductors accelerates, Europe's future competitiveness will de-pend on timely, coordinated action among public authorities and private players to address sector challenges and align industrial strategy with market needs.

ESIA urges the European Commission and EU Member States to immediately launch the necessary process to turn these ambitions into concrete results.

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Global 300mm fab equipment spending expected to total $374 billion over next three years

In its latest 300mm Fab Outlook, this robust investment reflects fab regionalization and surging AI chip demand for data centers and edge devices, while underscoring the growing commitment to semiconductor self-sufficiency across key regions through localized industrial ecosystems and supply chain restructuring.

WORLDWIDE 300mm fab equipment spending is expected to surpass $100 billion for the first time in 2025, growing 7% to $107 billion. The report projects investment will increase 9% to $116 billion in 2026, 4% to $120 billion in 2027, and 15% to $138 billion in 2028. "The semiconductor industry is entering a pivotal era of transformation, driven by unprecedented demand for AI-enabled technologies and a renewed focus on regional self-sufficiency," said Ajit Manocha, President and CEO of SEMI. "Strategic global investments and collaboration are driving robust, advanced supply chains and faster deployment of next-generation semiconductor manufacturing technologies. The global expansion of 300mm fabs will enable progress in data centers, edge devices, and the digital economy."

Segment Growth

The Logic & Micro segment is projected to lead equipment expansion with $175 billion in total investments from 2026 to 2028. Foundries are expected to be the primary drivers of this growth, fueled by sub-2nm capacity build-outs. Key enablers include advanced technologies such as gate-all-around (GAA) architecture and backside power delivery, which are essential to enhancing chip performance and power efficiency for increasingly demanding AI workloads. More advanced 1.4nm process technology is expected to enter volume production by 2028-2029. Additionally, AI performance improvements are anticipated to drive massive growth in edge-devices including automotive electronics, IoT applications, and robotics. Beyond advanced processes, demand across all nodes and various electronics devices is expected to surge significantly, fueling mature process equipment investment.

The Memory segment is projected to rank second with $136 billion in spending over the three-year period, marking the beginning of a new growth cycle for the segment. DRAM-related equipment investment is expected to exceed $79 billion from 2026 to 2028, with 3D NAND investment reaching $56 billion over the same period. AI training and inference have driven comprehensive demand increases across various types of memory.

AI training requires greater data transmission bandwidth and extremely low latency, significantly boosting high bandwidth memory (HBM) demand. Moreover, model inference generates higher quality and more diverse AI digital content, creating substantial demand for end storage capacity and driving 3D NAND Flash requirements. This robust demand has sustained elevated levels of supply

chain investment in memory over the medium to long term, helping to mitigate potential downturns from traditional memory cycle fluctuations. Analog-related segments' anticipated investment is projected to exceed $41 billion over the next three years.

Including Compound semiconductors, the power-related segment is expected to invest $27 billion from 2026 to 2028.

Regional Growth

China is expected to continue to lead in 300mm equipment spending with $94 billion in projected investments from 2026 to 2028, sustained by national self-sufficiency policies.

Korea is projected to rank second in global 300mm equipment spending over the three-year period with $86 billion invested, supporting industries worldwide in generative AI demand. Taiwan is expected to invest $75 billion in 300mm equipment over the three years, ranking third. Investment will concentrate primarily on 2nm and sub-2nm capacity to maintain dominance in advanced foundry capacity and technology leadership.

The report projects Americas to invest $60 billion from 2026 to 2028, rising to fourth position. U.S. suppliers are expanding advanced process capacity to meet surging AI application demands while catalyzing domestic industrial and investment upgrades to maintain global technology development leadership.

Japan, Europe & Middle East, and Southeast Asia are projected to invest $32 billion, $14 billion, and $12 billion, respectively, over the three-year period. Policy incentives aimed at alleviating critical semiconductor supply concerns are expected to increase equipment investment by more than 60% in these regions by 2028 compared to 2024.

Global silicon wafer shipments to rebound 5.4%

Global shipments of silicon wafers are projected to increase 5.4% in 2025 to 12,824 million square inches (MSI)

followed by steady growth through 2028 when the market is expected to reach a new industry record of 15,485 MSI, SEMI reported today in its annual silicon shipment forecast.

In 2025, the increase in silicon wafer shipments has been supported by strong AI-related growth, including advanced epitaxial wafers for leading edge logic devices and polished wafers for high bandwidth memory (HBM). Wafer shipments for non-AI applications, however, are just beginning to demonstrate a gradual recovery from the recent downcycle. The steady growth is expected to continue through 2028, driven by AI's expanding compute footprint in data centers and at the edge.

Silicon wafers are the fundamental building material for the majority of semiconductors, which are vital components of all electronic devices. The highly engineered thin disks, produced in diameters of up to 300 mm, serve as the substrate material on which most semiconductor devices, or chips, are fabricated.

All data cited include polished silicon wafers and epitaxial silicon wafers shipped by wafer manufacturers to end users. The data does not include non-polished or reclaimed wafers.

SEMI updates International Board of Directors

SEMI has announced updates to the SEMI International Board of Directors. Tetsuro (Terry) Higashi, Chairman of the Board of Directors for Rapidus, has been elected and began his three-year term on the SEMI International Board.
The following six board members have been reelected and were announced during the SEMI annual membership meeting on October 8, 2025, at SEMICON West:

- Tim Archer, President and CEO, Lam Research
- Doris Hsu, Chairperson and CEO, GlobalWafers
- Toshiki Kawai, Representative Director, President and CEO, Tokyo Electron
- Jon Kemp, President, Electronics and Industrial, DuPont
- Yong Han (YH) Lee, Chairman, Wonik
- Sue Lin, Vice Chairman, Hermes Epitek

The 18 voting directors and 10 emeritus directors on the SEMI International Board represent companies from across the global microelectronics supply chain, positioning SEMI to best support innovation in all areas of the industry. SEMI directors are elected by the general membership as voting members of the Board and can serve a

China is expected to continue to lead in 300mm equipment spending with $94 billion in projected investments from 2026 to 2028, sustained by national self-sufficiency policies

total of five, three-year terms.

NNME debuts ChipPath

To help meet the growing demand for skilled workers in the U.S. semiconductor and microelectronics industry, the National Network for Microelectronics Education (NNME), operated by the SEMI Foundation, has launched ChipPath, a first-of-its-kind, AI-enabled career platform that connects individuals directly to real opportunities across the industry.

With over 90,000 live job postings and counting, ChipPath is already one of the most comprehensive semiconductor workforce tools in the country. Unlike traditional job boards, ChipPath autonomously scrapes and aggregates open positions from the websites of SEMI member companies, capturing tens of thousands of roles across the full microelectronics supply chain, from design and manufacturing to automation, facilities, and materials.

"ChipPath is more than a job board, it's a bridge to opportunity," said Shari Liss, Vice President of Workforce Development and Initiatives at SEMI. "It's a movement to make the semiconductor workforce accessible to all Americans. This platform opens doors for students, veterans, career changers, and seasoned engineers, helping to see themselves in this industry and take real, actionable steps toward building their future in it."

Building the Bridge Between Talent and Opportunity

The semiconductor industry is expanding at record speed, yet many potential job seekers don't know how to start an industry career. ChipPath bridges that gap by helping users explore, prepare, and connect through an integrated set of tools designed specifically for semiconductor careers.

The platform includes four powerful components:

- **Smart Resume Builder: Creates** professional, industry-aligned resumes in minutes using AI-driven prompts that highlight relevant skills, certifications, and experience.
- **Career Mapping & Exploration:** Helps users discover the breadth of opportunities in semiconductors and visualize clear pathways to advancement.
- **Training & Development Resources:** Connects learners to certificate programs, apprenticeships, and degree pathways offered by NNME partners across the country.
- **Live Job Openings** Nationwide: Features over 90,000 active roles scraped directly from SEMI member company websites, providing a real-time view of the industry's hiring landscape.

"For too long, semiconductor careers have been somewhat invisible, seemed out of reach or hard to navigate," said Michelle Williams, Executive Director of the SEMI Foundation. "ChipPath changes that. It illuminates opportunities, empowers people to see where they fit, and gives them the tools to get there. No gatekeeping, no guesswork."

Next Up: Employer Dashboard Launching in 2026

The NNME and SEMI Foundation are already developing the next phase of ChipPath: a robust Employer Dashboard set to debut in early 2026. This feature will enable companies to curate and prioritize the skills and qualifications most important to their workforce needs, search and connect directly with job seekers, and gain data-driven insights into national workforce trends. The platform already operates autonomously, capturing tens of thousands of opportunities in real time.

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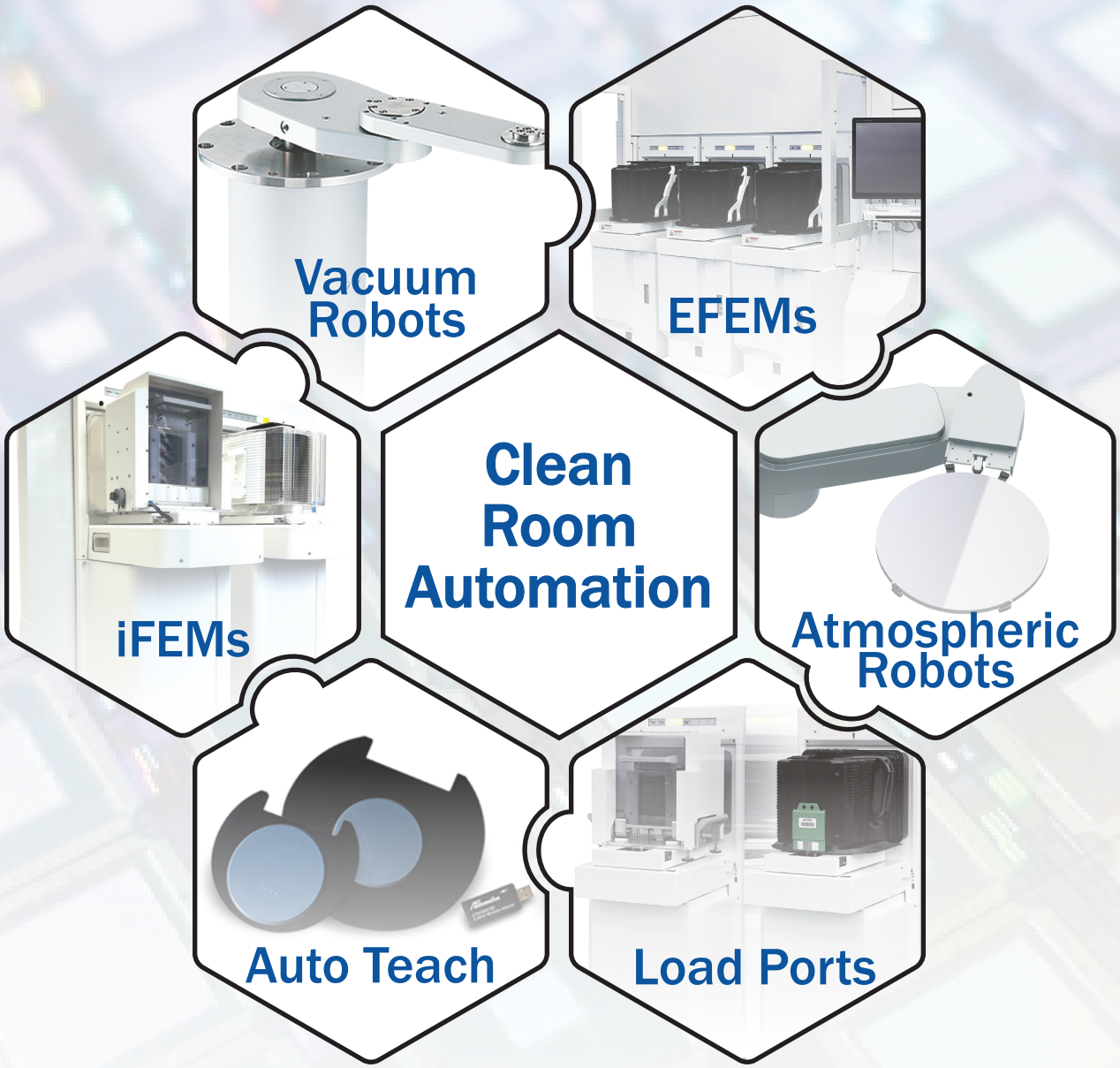

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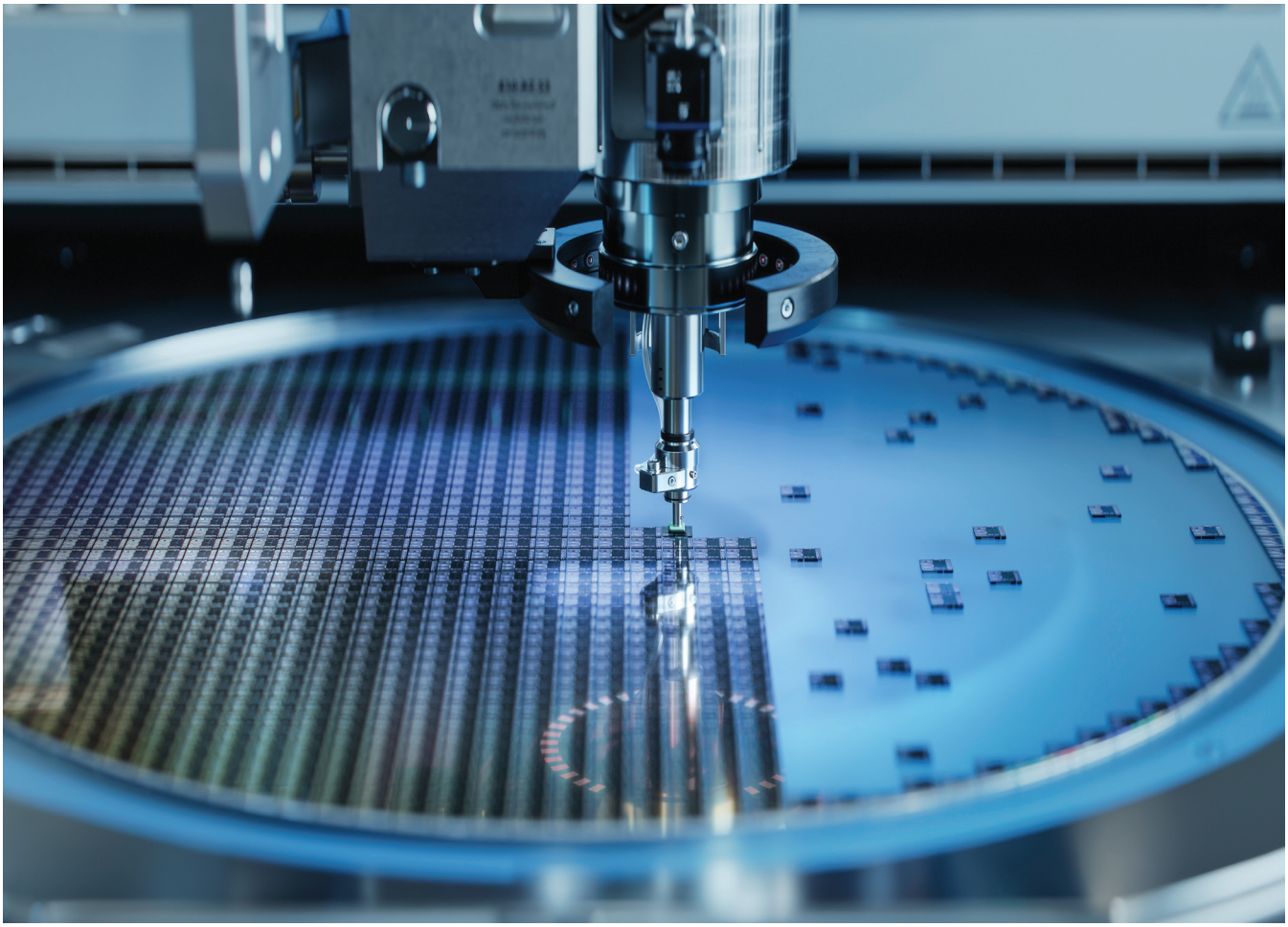


Trends and drivers for next-generation process vacuum

Edwards Vacuum examines several emerging production processes with an eye towards identifying trends that will drive the development of next-generation vacuum systems.

MOST semiconductor manufacturing processes require a vacuum in the process chamber to provide the pristine environment needed to ensure fault-free production and to remove excess process gases and reaction by-products. A modern fab with 60,000 wafer starts per month may contain 1000 or more vacuum process tools.

To support them the fab may need as many as 3500 dry vacuum pumps, most located below the fab in the sub-fab, and perhaps another 1200 turbomolecular pumps, located either in the sub-fab or attached directly to the process chamber/airlock to provide rapid wafer exchange and chamber pump-down. As process complexity continues to increase, the impact of vacuum system performance on process performance and productivity is also growing. Without vacuum the process stops, making overall reliability, especially the avoidance of unplanned downtime, the first priority. Minimizing total cost of ownership by extending the mean-time-between-service (when a pump is normally replaced from spare inventory and sent off-site for refurbishing) is a close second. As new processes and new materials are brought into high volume production, other details of vacuum system design and operation become more complex and more important. Here we will look at several emerging production processes with an eye towards identifying trends that will drive the development of next-generation vacuum systems.

A look back

Although the integrated circuit (IC) was invented in 1958, it was 1971 before the first processors based on now-familiar CMOS technologies were mass-produced (Intel's 4004). The manufacturing process, involving the sequential deposition and

patterning of multiple layers, was fundamentally the same then as it is now; though minimum feature sizes then measured in the tens or hundreds of micrometers, many thousands of times larger than today's nanometer-scale features. Then, as now, most process steps required vacuum conditions in the process chamber to control the chemical composition of the process environment. Most vacuum pumps in use in the first generations of integrated circuits (IC) were oil-sealed rotary vane pumps.

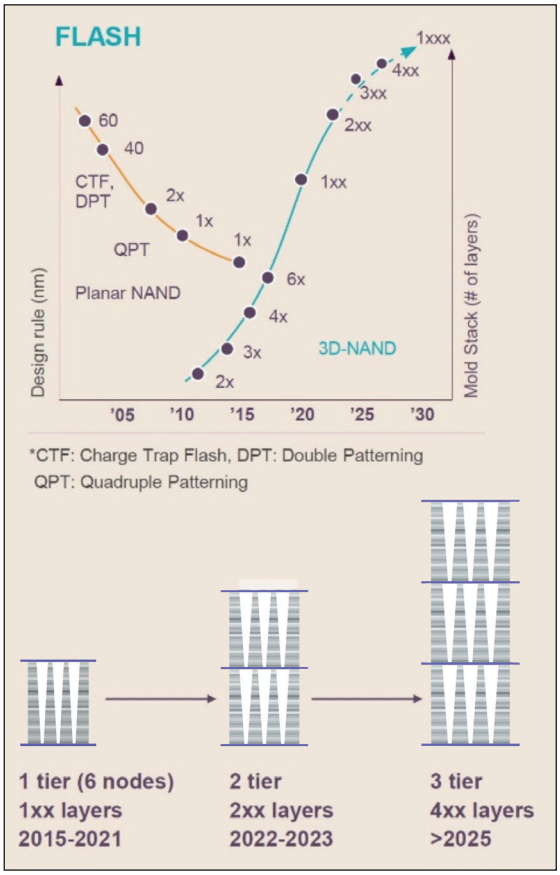
By the 1980s, IC production was expanding rapidly. New processes and increasing gas flows led to problems caused by aggressive chemicals and solids collecting in the pump oil. Frequent maintenance procedures to change very expensive specialty pump oils interrupted production, reduced productivity, and increased cost-of-ownership. In addition, new processes with more stringent requirements for contamination and cleanliness were intolerant of oil back-streaming from the vacuum system.

In 1980 Edwards introduced the first viable "dry" (oil-free) pump. The key innovation was a unique arrangement of roots and claw mechanisms in a multi-stage configuration that delivered clean vacuum with no need for oil to seal and lubricate the pump. Dry pumps were quickly adopted by semiconductor manufacturers and were arguably a critical enabler for the continuing development of increasingly complex semiconductor processes. Continuous innovation ever since has resulted today in a range of dry pumps, each tailored to address the specific challenges of new processes and process chemistries. In many cases, processes that are now commonplace would not have been possible without major innovations in vacuum systems.

Significant innovations since the dry pump include:

- New designs that prevent the accumulation of powders or the deposition of condensable by-products inside the pump
- Sophisticated data collection and analysis systems that optimize performance, coordinate maintenance schedules, monitor system health and predict maintenance requirements.
- Special coatings for pump components that resist attack by harsh process chemicals
- Green mode operation that reduces energy consumption by putting the pump in a low power mode when the process tool is idle

New developments in vacuum technologies have also significantly impacted the environmental profile of semiconductor manufacturing. Improving energy efficiency has been a persistent focus. Process-vacuum pumps can represent 12% or more of the total energy consumed by a semiconductor manufacturing facility. Current generation semiconductor dry pumps use less than half the energy consumed by their predecessors, while providing higher levels of performance, extended service intervals, and smaller footprints that improve sub-fab space utilization. In addition to reducing operating costs, the improved energy efficiency also reduces greenhouse gas emissions that result from energy production.

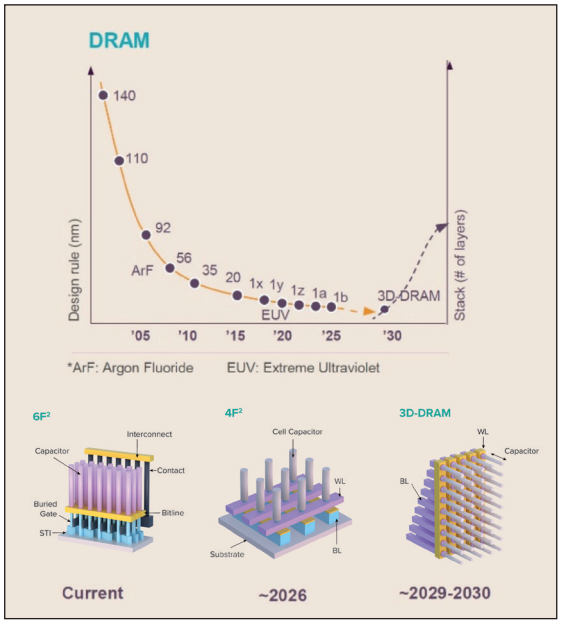


➤ Figure 1. 3D NAND flash memory uses very high aspect-ratio holes to create memory lines. The channels, and other HAR features must be lined with multiple thin conformal layers of various materials.

Looking ahead

As manufacturers develop new processes and introduce new materials, vacuum technologies must continue to evolve. The overall pressure in the process chamber as well as the partial pressure for each reacting gas will remain primary considerations. Pumping speed determines how fast the chamber can be brought to the required vacuum level and thus impacts process throughput and productivity. This effect is multiplied by processes such as atomic layer etch and deposition, which require frequent exchanges of gases in the chamber. Stability of the vacuum environment is also critical as it affects process variation, defect creation, and consequently process yield.

A brief survey of expected developments in several mainstream device technologies illustrates the challenges next-generation vacuum systems will need to address. For decades device manufacturers focused their efforts to pack more capability into less space on increasing aerial density, i.e., shrinking the size of individual components in an essentially two-dimensional layout. Those efforts resulted in the remarkable progress first observed by Intel's Gordon Moore: that the number of transistors in an



➤ Figure 2. Current DRAM designs use vertically-oriented capacitors to store information. Manufacturers must reduce the diameter and pitch of the capacitors to increase memory density. Future designs will adopt a 3D architecture that arranges horizontally oriented capacitors in many layers.

integrated circuit doubles about every two years. In recent generations, as transistors have become much smaller, further shrinking has become more difficult and more costly, resulting in a general slowing of the doubling rate. The last decade has seen the emphasis in many applications shift from two-dimensional layouts to more complex three-dimensional architectures that exploit the vertical dimension to pack more computing power into less space. The examples below illustrate this transition in 3D-NAND memory, DRAM, and logic.

New Architectures

3D NAND memory – 3D-NAND flash memory provides non-volatile data storage. It is used extensively in applications like solid state storage, where it replaces magnetic storage on disk drives. The defining characteristic of 3D-NAND is its storage of data in vertical strings of memory cells, thus multiplying, relative to conventional planar designs, the amount of data that can be stored in a given area on the wafer. Current generation 3D-NAND uses stacks (tiers) of around 200 layer-pairs. Some devices stack multiple tiers to increase capacity. Manufacturers' roadmaps predict significant increases in the number of layers per tier and the number of tiers per module over the next decade.

DRAM – DRAM (dynamic random-access memory) is faster than 3D-NAND, but also more expensive. And it is volatile – it loses the stored information when power is turned off. Its speed suits it well for operational applications, but its higher cost and volatility make it unsuitable for long-term storage of large amounts of data. Each memory cell may comprise only a single transistor and a single capacitor, with the absence or presence of charge on the capacitor determining the logical state of the cell. Current DRAM designs are essentially planar with a tubular capacitor oriented vertically above each transistor. Beginning as vertical holes, the capacitors are fabricated by depositing concentric layers of conductive and dielectric materials. To increase memory density, manufacturers must make the capacitors taller and thinner. The diameter and pitch of the capacitors are expected to shrink substantially over the next ten years, and heights to increase. The most significant change in DRAM will be a predicted transition to 3D architectures, in which multiple transistors and horizontally oriented capacitors are stacked vertically.

Logic – Logic, the network of variously interconnected, on-or-off transistors that actually performs computations is also becoming more complex as it transitions to three-dimensional architectures. The transistors are generally field effect transistors (FET). In a conventional planar FET, a gate is positioned above a semiconducting channel that connects a source and a drain. A voltage applied to the gate generates an electric field in the channel. The presence or absence of the field controls the flow of current through the channel, turning the transistor off or on. To improve performance of the transistor while reducing its size, designers have sought to provide better gate control over the channel. FinFETs, now widely produced with high-volume processes, feature a vertical fin structure surrounded on three sides by the gate. Gate-all-around (GAA) transistors take this further by wrapping the gate entirely around the channel, improving electrostatic control. The next innovation, complementary FET (CFET) stacks n-type and p-type transistors one atop the other. In most GAA transistors the channels are formed from very thin "nanosheets" of semiconducting material. New channel materials, such as transition metal dichalcogenides (TMD), could enable transistor gates as thin as a single molecular monolayer.

New Processes

HAR etch – More complex architectures incorporate novel features such as tall, narrow (high-aspect-ratio) holes and trenches. HAR features, such as the holes for memory strings and trenches in 3D-NAND and capacitors in DRAM begin with a specialized etch process. These highly directional (anisotropic) processes use complex chemical and physical interactions among the etched material, etching gases, and energetic ions/radicals to create features with tightly controlled sizes and profiles. The great depths and small etch fronts at the bottoms of HAR features extend etching times and reduce throughput. Longer etch steps require innovative mask materials that can resist the etching action to preserve the desired layer pattern. Highly reactive gases and process by-products are removed from the chamber by the vacuum system.

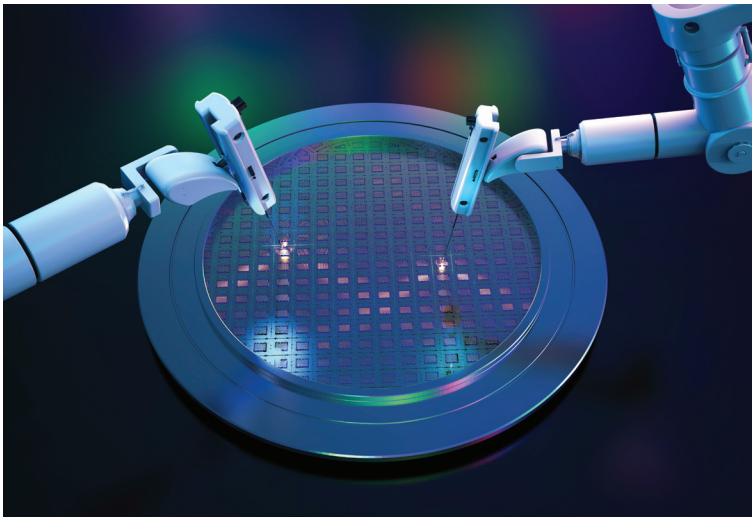
Chemical Vapor Deposition (CVD) – CVD uses chemical reactions to create thin films of solid materials on a heated surface. There are many variants, including atmospheric pressure CVD, but most processes used in semiconductor

manufacturing (PECVD, LPCVD, SACVD) proceed under vacuum conditions. In a CVD process the heated substrate is exposed to process gases containing precursors of the desired material, which react in the gas phase and accumulate on the wafer surface to form the deposited layer. The processes are relatively fast, and the deposition continues as long as the surface is exposed to the process. The thickness of the film is a complex function of flow rate, partial pressure, temperature, plasma settings (frequency, power, etc.), and process time.

To increase productivity, manufacturers are demanding higher flow rates and increased utilization (the ratio of production to capacity). At the same time, they are introducing new chemistries and materials that may have unexpected impacts on process equipment. Excess process gases and by-products can be toxic, corrosive, or explosive, raising significant safety concerns. Process windows are narrowing for film properties and uniformity. Thermal budgets must be carefully managed to avoid damage to the device being fabricated.

Advanced device architectures pose specific challenges. In particular, CVD processes are not good at maintaining uniformly thick films in the presence of significant topography, especially the extreme topography of HAR features, where the deposition process has restricted access to the internal vertical walls and deeply recessed bottoms of the features.

Atomic Layer Deposition (ALD) – ALD may be considered a variant of CVD. It offers an elegant solution for depositing highly conformal, precisely controlled thin films on complex, deeply recessed surfaces. The deposits accumulate one atomic layer at a time as the surface is exposed to a repeating cycle of precursor and reactant gases. In the first phase, the precursor reacts with specific sites on the surface. The reaction is self-limiting – once all sites have been occupied by a precursor molecule, the reaction stops. Next, the precursor gas is removed from the chamber, and a reactant gas is introduced. The reactant interacts with the previously deposited precursor, again in a self-limited way, to complete the deposition and recreate the original surface chemistry. The newly deposited monolayer is ready for another ALD cycle. Because both reactions



are self-limiting, film thickness is a function of the number of cycles, not exposure time. This gives process engineers the luxury of allowing each cycle of the process to continue as long as needed to be sure all surfaces are completely and uniformly covered. The biggest drawback of ALD is its slow speed. It is best suited to the deposition of very thin films that require fewer deposition cycles.

New Materials

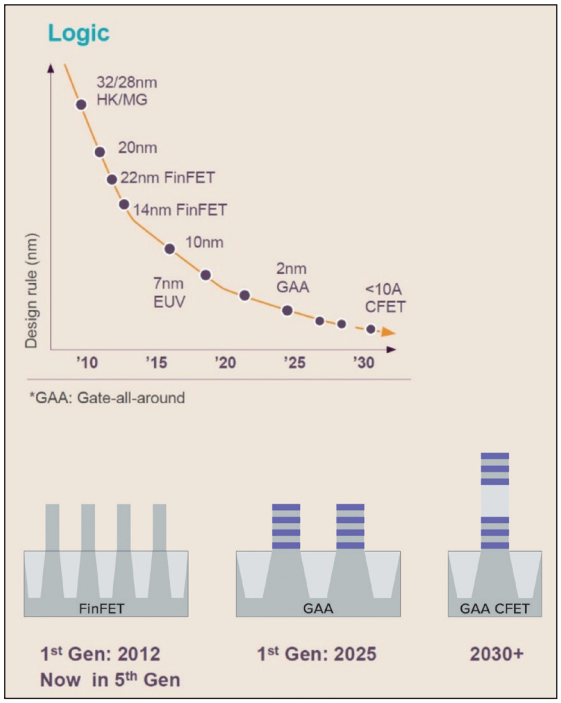
The development and integration of new materials have played an essential role in semiconductor innovation throughout its history. Through 1990, most fabrication schemes used process chemicals containing no more than a dozen elements: H, B, N, O, F, Al, Si, P, Cl, Ar, As, and Sb. The nineties saw the incorporation of 5 more: Ti, Cu, Br, Ta, and W.

The aughts added a whopping 43 elements: He, C, Ca, V, Cr, Fe, Co, Ni, Zn, Ge, Sr, Y, Zr, Nb, Mo, Ru, Rh, Pd, Ag, In, Ba, La, Hf, Re, Os, Ir, Pt, Au, Pb, Bi, Ce, Pr, Nd, Pm, Eu, Gd, Tb, Dy, Ho, Er, Tm, Yb, and Lu. And since 2010, 8 more: Mg, Mn, Ga, S, Se, Te, I, Xe. Fully 68 of the first 83 elements have now found their way into the production process. Most of these materials pass through the vacuum system, and each requires careful consideration to ensure safe, efficient handling.

New Vacuum Requirements

What effects do evolving device architectures and fabrication processes have on the vacuum systems tasked with removing excess process gases and by-products from process chambers?

To increase productivity, manufacturers are demanding higher flow rates and increased utilization (the ratio of production to capacity). At the same time, they are introducing new chemistries and materials that may have unexpected impacts on process equipment. Excess process gases and by-products can be toxic, corrosive, or explosive, raising significant safety concerns



➤ Figure 3. Logic transistors began the transition from planar to 3D more than a decade ago. FinFETS are in their 5th generation. Advanced devices are now adopting gate-all-around designs that stack multiple gates. Complementary CFET will position stacks of n-type and p-type GAA transistors one over the other.

Footprint – Process tools are trending toward larger platforms with more chambers, fitting more production capacity into less fab space. This increase in the density of chambers in the fab and demands commensurate footprint reductions in the sub fab, where supporting pumps and abatement systems must fit within the shadow of the process tool above.

Speed – New process technologies need higher flow rates, lower pressures, and faster pump-down times, all of which increase demand for higher speed and capacity from pumps and abatement systems. This is especially true for processes such as ALD, which require frequent exchanges of all gas in the process chamber.

Efficiency – Energy efficiency is one of the rare instances when the economic and environmental priorities of semiconductor manufacturers align. Vacuum systems account for as much as 25% of the energy consumed by a modern fab. Improving efficiency reduces both operating costs in the fab and any greenhouse gas emissions associated with power production.

Adaptation to new processes and materials – If the vacuum fails, the process stops. Avoiding unplanned downtime and maximizing process equipment availability require careful attention to the impacts of new materials and processes on supporting vacuum systems. Etch gases are highly corrosive. Some process gases and by-products can condense and solidify, blocking vacuum lines and seizing pumps – these deposits can be managed by controlling temperature along the lines and through the pump. Some gases generate powders that must be moved through the system and properly disposed of. Still others may be flammable, explosive, pyrophoric, or toxic, constituting health and safety hazards.

Collaboration and customization – The semiconductor industry has seen a fundamental change over the last decade as the era of lock-step two-dimensional shrinks has given way to innovative approaches that continue to pack more power into less space. The shared industry roadmap that efficiently guided manufacturers for decades has become less clear, and manufacturers are less open about their internal roadmaps. In diversification lies great opportunity. Innovation – new architectures, new processes, new materials – continues to emerge. Everyone wants innovation, but no one really wants to be first. The onus has shifted to individual manufacturers and suppliers to collaborate in developing customized solutions. Close relationships that encourage information exchange and early involvement in application-specific vacuum system design will be essential, and supplier knowledge and expertise based on broad engagement across the industry will acquire new value.

Stay tuned

We have looked here at the growing complexity of semiconductor device manufacturing as the industry transitions from simple two-dimensional shrinks to complex three-dimensional architectures, including examples from logic, 3D NAND and DRAM. New architectures have generated the need for new processes and materials, e.g. ALD and HAR etch, which in turn have placed new demands on process tools and the vacuum systems most of those tools depend on. We have reviewed the requirements for vacuum systems, both fundamental: reliability and MTBS; and emerging: footprint, speed, efficiency, adaptation, customization, and collaboration. These and more are driving our efforts to develop the next generation vacuum platform. Stay tuned, there is much more to come.

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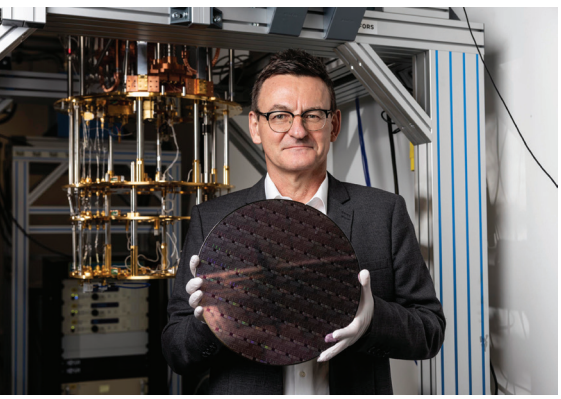
Imec technology lights the path to utility scale for Diraq's quantum chips

Silicon qubits made using advanced industrial manufacturing methods have met key performance criteria, paving the way to mass production of functional quantum computers.

IMEC and Diraq, a pioneer of silicon-based quantum computing, have demonstrated that industrially made silicon quantum dot qubits consistently show error rates that surpass the values needed for quantum error correction.



The results, reported in Nature, show that Diraq's qubits can be manufactured reliably with the tools of the silicon microchip trade, confirming the potential of imec's industrial manufacturing techniques for developing large-scale silicon-based quantum computers.

Leveraging nearly a decade of careful optimization and engineering of spin-qubit fabrication at imec, Diraq-designed devices were shown to consistently achieve over 99% fidelity in operations involving two quantum bits (or 'qubits'). This feat, made possible by imec's advanced spin qubit technology platform, is a crucial step in Diraq's roadmap toward utility scale — the point at which a quantum computer's value exceeds its cost.

Diraq's CEO and Founder, Andrew Dzurak, said, "Achieving utility scale in quantum computing hinges on finding a commercially viable way of producing high-fidelity qubits at scale. Diraq's collaboration with imec makes it clear that silicon-based quantum computers can be built by leveraging the mature semiconductor industry, which opens a cost-effective pathway to chips containing millions of qubits while still maximizing fidelity."

Technical summary

The fidelity of a quantum operation quantifies how close the actual operation is to its ideal version and is a key metric for enabling large-scale quantum computers. Ideally, fidelities must (far) exceed 99% across all operations. Only then are errors rare

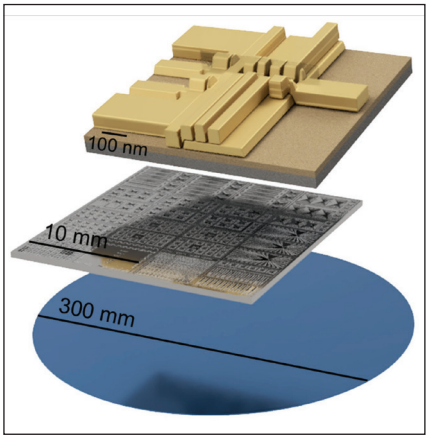
enough for quantum error correction methods to work successfully. In this work, fidelities were reproducibly measured for a set of silicon quantum dot spin qubit operations across multiple devices state preparation and measurement of the qubits (SPAM), and one- and two-qubit gate operations performed on the qubits to control their state and entangle them — the elementary operations required for a utility-scale quantum computer.

Fidelities above 99.9% were achieved for SPAM operations, and fidelities systematically exceeding 99% were shown for one- and two-qubit gate operations, making quantum error correction of industrially fabricated quantum dot qubit devices now a realistic prospect.

Typically, quantum devices fabricated in academic clean rooms are selected for measurement on the basis of their quality, a process that produces 'hero' devices, obscuring the reproducibility of the results. In the Nature publication, Diraq measured devices that were selected at random, obtaining reproducible data on sets of two-qubit devices, each consisting of a double quantum-dot structure. The devices were fabricated using imec's 300mm spin qubit platform for silicon quantum-dot structures, which is optimized for low electrical noise and high uniformity.

In order to also suppress the magnetic noise from residual nuclear spins in the substrate, the quantum-dot structures were fabricated on an isotopically enriched 28Si layer.

Kristiaan De Greve, fellow and program director for quantum computing at imec: "For the first time, silicon MOS based quantum-dot spin-qubit devices realized with industrial manufacturing techniques perform as well as academic hero devices. This shows that imec's 300mm process flow for MOS based quantum-dot structures enables a low-noise qubit environment, resulting in high fidelity values for a set of critical qubit operations. The methods used and insights gained from it also show us that there is further room for fidelity improvement, as higher fidelities can be achieved through even further isotopic enrichment of the silicon-channel layer with 28Si."



➤ Figure 1. Schematic of a Diraq two-qubit device on a 300mm wafer, showing the full wafer, single die and single device level (Dumoulin Stuyck et al, Nature – 2025).

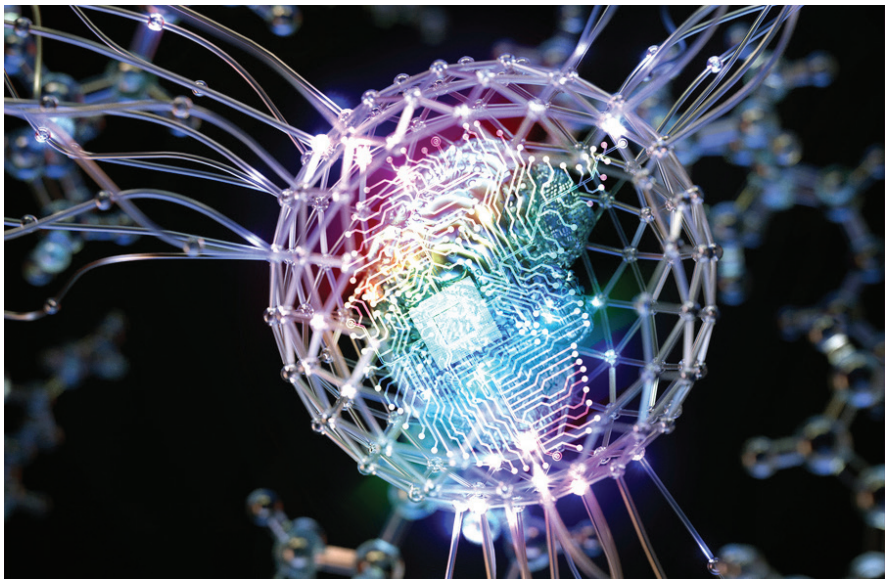
Checking the quality of materials just got easier with a new AI tool

Acting as a "virtual spectrometer," SpectroGen generates spectroscopic data in any modality, such as X-ray or infrared, to quickly assess a material's quality.

BY JENNIFER CHU, MIT NEWS

MANUFACTURING better batteries, faster electronics, and more effective pharmaceuticals depends on the discovery of new materials and the verification of their quality. Artificial intelligence is helping with the former, with tools that comb through catalogs of materials to quickly tag promising candidates.

But once a material is made, verifying its quality still involves scanning it with specialized instruments to validate its performance — an expensive and time-consuming step that can hold up the development and distribution of new technologies.



➤ The circle with the chip symbolizes SpectroGen, with the connecting threads depicting the process of generating a material's spectrum. Credit: Courtesy of the researchers.

Now, a new AI tool developed by MIT engineers could help clear the quality-control bottleneck, offering a faster and cheaper option for certain materials-driven industries. In a study appearing today in the journal Matter, the researchers present "SpectroGen," a generative AI tool that turbocharges scanning capabilities by serving as a virtual spectrometer. The tool takes in "spectra," or measurements of a material in one scanning modality, such as infrared, and generates what that material's spectra would look like if it were scanned in an entirely different modality, such as X-ray. The AI-generated spectral results match, with 99 percent accuracy, the results obtained from physically scanning the material with the new instrument.

Certain spectroscopic modalities reveal specific properties in a material: Infrared reveals a material's molecular groups, while X-ray diffraction visualizes the material's crystal structures, and Raman scattering illuminates a material's molecular vibrations. Each of these properties is essential in gauging a material's quality and typically requires tedious workflows on multiple expensive and distinct instruments to measure.

With SpectroGen, the researchers envision that a diversity of measurements can be made using a single and cheaper physical scope. For instance, a manufacturing line could carry out quality control of materials by scanning them with a single infrared camera. Those infrared spectra could then be fed into SpectroGen to automatically generate the material's X-ray spectra, without the factory having to house and operate a separate, often more expensive X-ray-scanning laboratory.

The new AI tool generates spectra in less than one minute, a thousand times faster compared to traditional approaches that can take several hours to days to measure and validate. "We think that you don't have to do the physical measurements in all the modalities you need, but perhaps just in a single, simple, and cheap modality," says study co-author Loza Tadesse, assistant professor of mechanical engineering at MIT. "Then you can use SpectroGen to generate the rest. And this could improve productivity,

efficiency, and quality of manufacturing." The study's lead author is former MIT postdoc Yanmin Zhu.

Beyond bonds

Tadesse's group at MIT develops AI-informed optical and spectroscopy systems that aim to advance disease diagnosis, therapy, and global health, in efficient, sustainable ways. "Diagnosing diseases, and material analysis in general, usually involves scanning samples and collecting spectra in different modalities, with different instruments that are bulky and expensive and that you might not all find in one lab," Tadesse says. "So, we were brainstorming about how to miniaturize all this equipment and how to streamline the experimental pipeline."

Zhu noted the increasing use of generative AI tools for discovering new materials and drug candidates, and wondered whether AI could also be harnessed to generate spectral data. In other words, could AI act as a virtual spectrometer?

A spectroscope probes a material's properties by sending light of a certain wavelength into the material. That light causes molecular bonds in the material to vibrate in ways that scatter the light back out to the scope, where the light is recorded as a pattern of waves, or spectra, that can then be read as a signature of the material's structure. For AI to generate spectral data, the conventional approach would involve training an algorithm to recognize connections between physical atoms and features in a material, and the spectra they produce. Given the complexity of molecular structures within just one material, Tadesse says such an approach can quickly become intractable.

"Doing this even for just one material is impossible," she says. "So, we thought, is there another way to interpret spectra?"

The team found an answer with math. They realized that a spectral pattern, which is a sequence of waveforms, can be represented mathematically. For instance, a spectrum that contains a series of bell curves is known as a "Gaussian" distribution, which is associated with a certain mathematical expression,

> With SpectroGen, the researchers envision that a diversity of measurements can be made using a single and cheaper physical scope. For instance, a manufacturing line could carry out quality control of materials by scanning them with a single infrared camera

compared to a series of narrower waves, known as a "Lorentzian" distribution, that is described by a separate, distinct algorithm. And as it turns out, for most materials infrared spectra characteristically contain more Lorentzian waveforms, while Raman spectra are more Gaussian, and X-ray spectra is a mix of the two.

Tadesse and Zhu worked this mathematical interpretation of spectral data into an algorithm that they then incorporated into a generative AI model.

"It's a physics-savvy generative AI that understands what spectra are," Tadesse says. "And the key novelty is, we interpreted spectra not as how it comes about from chemicals and bonds, but that it is actually math — curves and graphs, which an AI tool can understand and interpret."

Data co-pilot

The team demonstrated their SpectroGen AI tool on a large, publicly available dataset of over 6,000 mineral samples. Each sample includes information on the mineral's properties, such as its elemental composition and crystal structure. Many samples in the dataset also include spectral data in different modalities, such as X-ray, Raman, and infrared. Of these samples, the team fed several hundred to SpectroGen, in a process that trained the AI tool, also known as a neural network, to learn correlations between a mineral's different spectral modalities. This training enabled SpectroGen to take in spectra of a material in one modality, such as in infrared, and generate what a spectra in a totally different modality, such as X-ray, should look like.

Once they trained the AI tool, the researchers fed SpectroGen spectra from a mineral in the dataset that was not included in the training process. They asked the tool to generate a spectra in a different modality, based on this "new" spectra. The AI-generated spectra, they found, was a close match to the mineral's real spectra, which was originally recorded by a physical instrument. The researchers carried out similar tests with a number of other minerals and found that the AI tool quickly generated spectra, with 99 percent accuracy.

"We can feed spectral data into the network and can get another totally different kind of spectral data, with very high accuracy, in less than a minute," Zhu says.

The team says that SpectroGen can generate spectra for any type of mineral. In a manufacturing setting, for instance, mineral-based materials that are used to make semiconductors and battery technologies could first be quickly scanned by an infrared laser. The spectra from this infrared scanning could be fed into SpectroGen, which would then generate a spectra in X-ray, which operators or a multiagent AI platform can check to assess the material's quality.

"I think of it as having an agent or co-pilot, supporting researchers, technicians, pipelines and industry," Tadesse says. "We plan to customize this for different industries' needs." The team is exploring ways to adapt the AI tool for disease diagnostics, and for agricultural monitoring through an upcoming project funded by Google. Tadesse is also advancing the technology to the field through a new startup and envisions making SpectroGen available for a wide range of sectors, from pharmaceuticals to semiconductors to defense.

- ***Paper:*** *"Universal Spectral Transfer with Physical Prior-Informed Deep Generative Learning.*
- www.cell.com/matter/abstract/S2590-2385(25)00477-1

Imec achieves new milestones in single patterning High NA EUV lithography for both damascene and direct metal etch metallization processes

The results underscore the strength of imec's High NA EUV ecosystem in pushing the boundaries of High NA EUV patterning technology to A10 and beyond logic nodes.

AT the recent 2025 SPIE Photomask Technology + EUV Lithography Conference (Monterey (CA)), imec presented two breakthrough achievements in single print High NA EUV lithography: (1) line structures at 20nm pitch with 13nm tip-to-tip critical dimension (CD) relevant for damascene metallization, and (2) electrical test results of Ru lines at 20nm pitch obtained with a direct metal etch (DME) process.

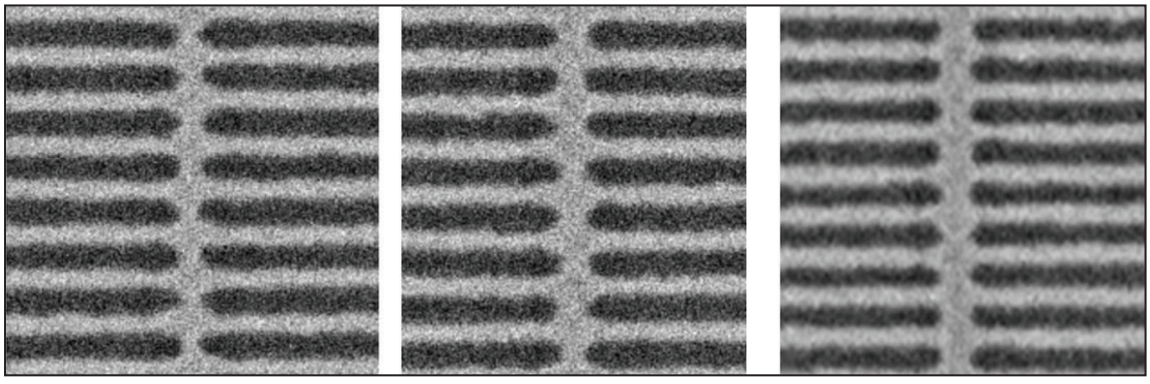
These results, enabled in part by the EU's NanoIC pilot line, not only mark a major milestone in advancing the single print capabilities of High NA EUV patterning. They also underscore the pivotal role of the imec-ASML partnership in enabling the broader ecosystem that drives the High NA EUV transition to high volume manufacturing, unlocking the sub-2nm logic technology roadmap.

After demonstrating 20nm pitch metallized line structures at the 2025 SPIE Advanced Lithography and Patterning in February 2025, imec now achieves 20nm pitch line structures with 13nm tip-to-tip (T2T) critical dimension (CD) with a single-exposure High NA EUV lithography step. For the 13nm T2T structures, a local CD uniformity (LCDU) as low as 3nm was measured, marking an industry milestone. The results were obtained with a metal oxide resist (MOR), which was co-optimized with underlayer, illumination pupil shape and mask selection.

Steven Scheer, Senior Vice President Compute System Scaling at imec: "Achieving these logic designs with single print High NA EUV lithography reduces processing steps compared to multi-patterning, lowering fabrication costs and environmental impact, and improving yield. These results support damascene metallization, the industry standard for interconnect fabrication.

T2T structures are an essential part of the interconnect layers, as they allow for interrupting the one-dimensional metal tracks. To meet the logic roadmap at 20nm metal pitch, the T2T distance is expected to scale to 13nm and below. while maintaining functional interconnects. Developments are ongoing to further scale T2T dimensions, with promising results for 11nm T2T, and to transfer the structures into an underlying hard mask – enabling true (dual-)damascene interconnects."

To enable metallization below 20nm, industry will likely move to alternative metallization schemes. As a second achievement, imec demonstrates the compatibility of direct metal etch (DME) of ruthenium (Ru) with single exposure High NA EUV lithography. We achieved Ru lines at 20nm and 18nm pitch, including 15nm T2T structures and functional interconnects with low resistance. For the 20nm pitch metallized line structures, an electrical test yield of 100% was obtained.



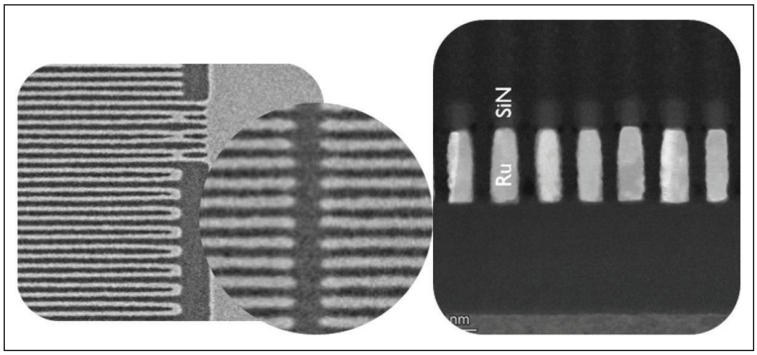
➤ Figure 1. Line structures at 20nm pitch with (left) 11nm T2T CD, (center) 13nm T2T CD and (right) 18nm pitch with 16nm T2T CD.

Steven Scheer: "After the opening of the joint ASML-imec High NA EUV lab in Veldhoven, the Netherlands, imec and its ecosystem of partners made great strides in advancing High NA EUV lithography and launching the industry into the angstrom era – backed by three years of ecosystem preparation.

The presented results mark a new milestone, underscoring imec's leadership in litho R&D. They also play a critical role in realizing the European Chips Act's ambitions for enabling sub-2nm logic technology nodes.

In close collaboration with the imec-ASML High NA EUV ecosystem, which includes leading chip manufacturers, equipment, material and resist suppliers, mask companies, and metrology experts, we continue to jointly optimize High NA EUV lithography and patterning in support of the logic and memory roadmaps."

The results, enabled in part by the EU's NanoIC pilot line, were be presented in the following paper at the SPIE Photomask Technology + EUV Lithography Conference: *Paper 13686-4 - Advances of dry resist towards next-generation lines-spaces patterning in high NA EUV lithography.*



➤ Figure 2 – 18nm pitch Ru lines obtained with DME after single exposure High NA EUV lithography.

ACKNOWLEDGEMENT

➤ This work has been enabled in part by the NanoIC pilot line. The acquisition and operation are jointly funded by the Chips Joint Undertaking, through the European Union's Digital Europe (101183266) and Horizon Europe programs (101183277), as well as by the participating states Belgium (Flanders), France, Germany, Finland, Ireland and Romania.

➤ For more information, visit nanoic-project.eu

Metrology for the 2 nm era and beyond

Infinitesima bets on high-speed atomic force microscopy to keep advanced silicon on track.

BY REBECCA POOL, TECHNOLOGY EDITOR

WITH Taiwan's lead chipmaker, TSMC, set to begin full-scale production of 2 nm technology, silicon chip design is entering uncharted territory - and pulling metrology along with it.

As ever-more complex 3D architectures, complementary-FETs, hybrid bonding and advanced packaging emerge, metrology and inspection tools will be vital to robust chip fabrication. But with transistor dimensions shrinking to just a few atoms, the workhorse of defect detection - optical inspection – is hitting its limits.

Deep UV lithography at 193 nm wavelength has already given way to extreme UV (EUV) lithography at 13.5 nm. Yet the smallest etch patterns now measure as small as 9 nm. Factor in intricate buried structures with remarkably high aspect ratios and more than 100 stacked layers on a single chip, and the challenge of detecting defects becomes staggering.

One company that remains undeterred is UK-based Infinitesima, which has just joined forces with photolithography systems giant, ASML, of The Netherlands, and Belgian R&D powerhouse, IMEC, to hone its in-line metrology platform for increasingly complex device architectures.

Instead of the usual optical methods, 'Metron3D' relies on atomic force microscopy (AFM), where a probe tip oscillates above the silicon wafer surface and measures the atomic forces, to detect defects. The platform combines AFM with interferometry and other optics innovations to increase inspection throughput of structures by at least 100 times compared to standard AFM - critical for defect detection on a high volume semiconductor manufacturing line.

Together the partners now intend to optimise and drive Infinitesima's unconventional metrology tech further into the silicon semiconductor market. "Industry is operating at the atomic-scale to control transistors – for example, to store electrons in a capacitor, very complex 3D structures are being [fabricated] and that's creating a need for sub-nanometre 3D metrology," says Infinitesima CEO, Peter Jenkins. "AFM is good at this, but traditionally very slow. So solving the speed problem means customers have the metrology to move these structures from R&D and into volume manufacturing."

From lab roots to fab floors

Founded in 2001 by University of Bristol professor, Andrew Humphris, to commercialise fast scanning probe microscopy for biological samples, Infinitesima quickly switched to semiconductors – given the greater market potential. The company's rapid probe microscope (RPM) soon followed - essentially a high-speed AFM that uses optical interferometry, instead of laser beam deflection, to track the AFM probe tip's motion and enable faster sample scanning.

Come 2010, photothermal actuation had replaced mechanically or piezoelectrically-driven actuation in the RPM set-up, to reliably drive probe tips at higher frequencies.

This helped to cut surface analysis and defect detection from minutes to seconds while still delivering sub-nanometre vertical resolution - proving the technique viable for semiconductor fabs. RPM technology was later integrated to Carl Zeiss' photomask repair tools as well as the scanning electron microscope platforms of a leading US chipmaker.

"It's the optics that give RPM its speed and enable unique modes of operation, helpful for looking at small, high aspect ratio structures on semiconductors," highlights Jenkins. "We currently dither [oscillate] the probe at 600 kHz and will extend this to more than a megahertz in the future to enable even faster speeds."

Scaling to volume production

With RPM in tow, Infinitesima partnered with IMEC to integrate its technology with wafer-handling software, robotics, and a high-speed wafer stage, to provide in-line metrology for next-generation logic, DRAM and 3D NAND. Metron3D was delivered in late 2021, and backed by Asia-based investors as well as Applied Ventures, the venture arm of US semiconductor equipment heavyweight, Applied Materials, Infinitesima has been ramping production ever since.

Right now, R&D and core module manufacturing takes place in the UK, with system assembly in Taiwan. "We don't have to invest in building a factory and it's going to be much faster to scale [manufacturing]," says Jenkins.

The system has already shipped to a significant - but unnamed - Taiwan-based foundry as well as to high bandwidth memory chip maker, SK Hynix of Korea - also a supplier to AI giant Nvidia - for advanced DRAM inspection. As Young-Hyun Choi, Head of Defect Analysis, Metrology and Inspection Technology, has said: "3D process control at the nano-scale level is becoming increasingly important to ensure high yield in advanced DRAM processes. Metron3D has demonstrated excellent sub-nanometre 3D metrology with the required cost-of-ownership necessary for high volume manufacturing implementation."

Next steps

Building on this traction, Infinitesima is now working with IMEC and ASML to hone Metron3D for in-line metrology of complex devices, in volume production. ASML in particular has a vested interest in optimising the platform for high-numerical aperture EUV lithography, having shipped these first resist imaging systems in early 2024.

Meanwhile, Jenkins sees other key market opportunities in 3D logic device structures such as complementary field-effect transistors (CFETs), and in hybrid wafer bonding.

"Nearly every future device will use hybrid wafer bonding, and measuring these extremely very flat [structures] is an ideal application for AFM," he says. "AFM is one of the ground-truth metrology methods that can give you sub-nanometre, 3D information, which is why we're confident industry will need this technology as it moves forward – and we can do this so much faster with Metron3D."

As part of a three-year development project, the partners will focus on taking in-depth 3D surface detection, high-speed imaging and interferometric accuracy further.

By way of example, Jenkins notes they will refine the RPM probe tip and AFM operating modes to measure the smaller patterns and strut features formed on wafers during high-NA EUV lithography. "We won't be redesigning our system," he explains. "This is about enhancing operation within the software, codes and types of probes that we use, and the data analysis that we run."

➤ Infinitesima's Metron3D metrology system is designed to measure challenging nanoscale structures in semiconductors at high speed. [Infinitesima]

Jenkins is hopeful that come the project-end, AFM technology market growth will be well and truly on the rise. He estimates the value of today's AFM market at around $200 million, but based on a steady semiconductor industry CAGR of 8%, expects this figure could reach $1 billion come 2030. "AFM will become increasingly complementary to certain process control steps, and the number of those steps will increase as fabrication processes evolve," he says.

But will industry demand for Metron3D also rise? Jenkins thinks so, highlighting Infinitesima's two existing contracts, and also noting how the technology is under evaluation with industry's other key players – that includes Intel, Samsung and Micron. "We're pretty hopeful that we will see additional contracts with other players in the coming 12 to 24 months," he says.

"Time to market is critical and we already have some strong IP protecting our core technology," he adds. "I would imagine we'll get an [acquisition] offer from one of the lead firms down the road, which we'll evaluate at that point in time. But for now, we're happy doing our thing."

iDEAL charts a new course for silicon

Will the latest MOSFET from iDEAL Semiconductor redefine silicon chip performance?

BY REBECCA POOL, TECHNOLOGY EDITOR

IN SEPTEMBER this year, a new kind of silicon MOSFET entered mass production. Developed by iDEAL Semiconductor, the 150V and 200V devices are based on the so-called SuperQ architecture, which the US-based firm claims is the first major advance in silicon MOSFET technology in more than 25 years.

Drawing on elements of the legacy HEXFET and Superjunction topologies, the SuperQ-based MOSFET concept was first conceived more than a decade ago. While built mostly on established CMOS processes, the device is said to break through long-standing silicon barriers in switching and conduction.

“The number one question I get from applications and systems engineers is what’s the catch?” says Ryan Manack, Vice President of Marketing at iDEAL Semiconductor. “I see competitors making devices with a lower resistance and double the switching loss, but we’re providing the next level of performance without a trade-off.”

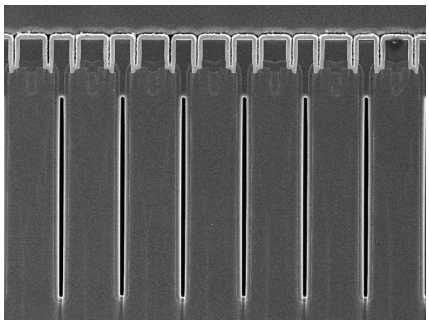
The 150V and 200V MOSFETs are just the beginning. iDEAL Semiconductor intends to soon provide a 650 V device, and has bold plans to take its SuperQ architecture up to 1200 V.

“We’ve already demonstrated that the performance of our [structures] is either equal or better than the industry-leading super-junction structures that industry has been optimising for the last twenty years,” highlights Manack’s colleague, Philip Rutter, Vice President of Development at iDEAL Semiconductor. “We’re just getting started.”

A different approach

The SuperQ architecture follows a long history of MOSFET innovation. The legacy HEXFET architecture was launched by International Rectifier back in late 1978. Its hexagonal cell geometry in a vertical MOSFET design boosted transistor density, shrank die size, and proved pivotal to the miniaturization of electronic devices. A wide *n*-type conduction region helped the device to excel at low and medium voltages, but performance became inefficient at higher levels, as blocking more voltage in this drift region drove up on-resistance.

Come 1998, Infineon Technologies (then Siemens Semiconductor) changed the game with its superjunction MOSFETs, which were based on the Reduced Surface Field - RESURF - structure and could operate at higher voltages more efficiently. The drift region of this power transistor comprised pillars of p-type and n-type layers, in contrast to purely n-type material in the HEXFET, yielding a less resistive structure that could still block higher voltages.



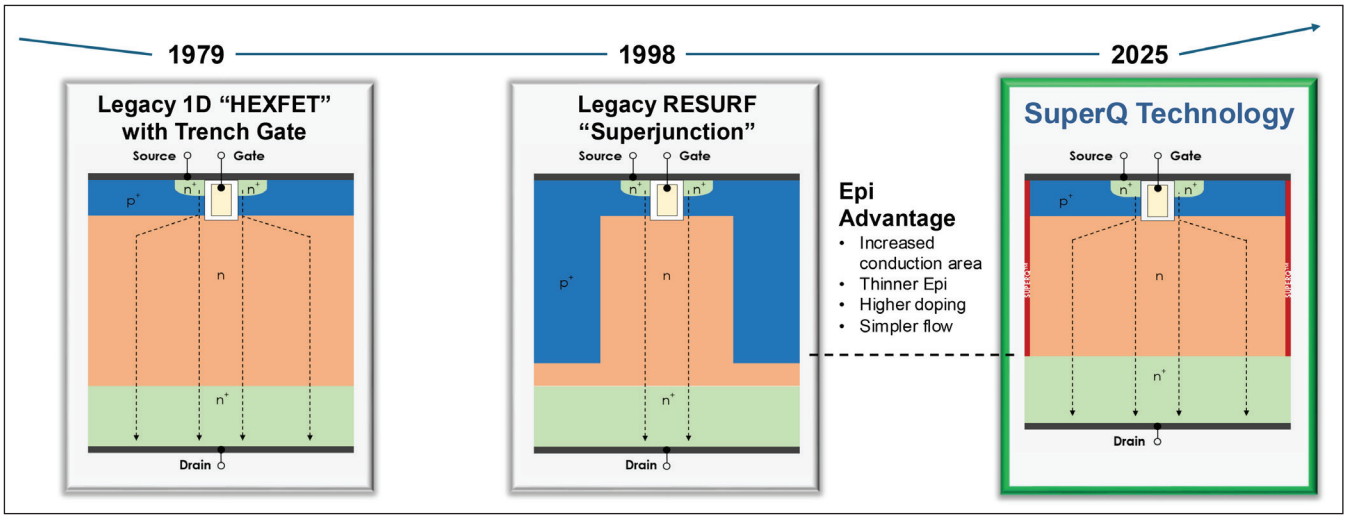
➤ SuperQ trench technology promises near-ideal charge balance, allowing thinner epitaxy. It also allows a higher doping concentration in the conduction region, helping to reduce channel resistance and lowering power loss. [iDEAL Semiconductor]

But while this superjunction approach became the gold standard for silicon MOSFETs, higher voltage operation has demanded thick, high resistance drift regions, that can stifle silicon performance and generate excess heat. Given this, Mark Granahan, now CEO of iDEAL Semiconductor, had the idea to bring back HEXFET’s wide n-type conduction region but introduce dielectric-filled deep trenches. This novel design minimized the need for p-type layers and reduced on-resistance whilst maintaining the all-important high voltage blocking capabilities.

iDEAL Semiconductor launched in 2017, with Granahan and colleagues spending some time finding the best way to etch high aspect ratio trenches and create functional structures. They settled on atomic layer deposition, a gas-phase chemical process in which thins films are deposited one atomic layer at a time. Following several investment rounds that brought in more than $75 million, including funds from Applied Ventures, the venture capital arm of Applied Materials, so-called SuperQ technology was introduced in 2023.

“We have extremely good process control that costs less [than superjunction fabrication],” highlights Rutter. “We etch our trench and then deposit a charged layer, using atomic layer deposition.”

“So as our competitors have kept on shrinking the n-type region, they’ve lost part of the benefits [of silicon] but



➤ MOSFET architectures include the 'HEXFET' and Super-junction. SuperQ is designed to maximize the n-conduction region. [iDEAL Semiconductor]

with SuperQ, we've kept the n-type region wider and have in effect just shrunk the p-region," he adds. "From an architectural point of view, there are no limits to doing this."

Delivering devices

Working with US-based independent foundry, Polar Semiconductor, iDEAL Semiconductor's first devices, both 150 V and 200 V MOSFETs entered full production within weeks of each other, this Summer, and higher voltage devices are set to follow soon.

"We've got 300 V and 400 V MOSFETs entering the fab right now, and 650 V [devices] are in the works," says Manack. "And [to deliver these], we're talking quarters not years."

Both devices are said to reduce switching losses by at least 2X compared to competing devices, and improve resistance and power losses – whilst maintaining the benefits of silicon, including its high-volume manufacturability. The company's latest lowest-resistance 200 V devices achieve a maximum RDS(on) of just 5.5 mΩ, delivering resistance that is said to be 1.2x lower than the current market leader, and 1.7x lower than its next-best competitor in silicon. Target applications include motor drives and AI servers, as well as LED lighting, battery protection, isolated DC/DC power modules and USB-PD adapters.

But there's more to SuperQ than silicon MOSFETs. The technology is also designed for IGBTs, diodes, power ICs - and even other semiconductor materials, including SiC and GaN. Manack also notes that iDEAL Semiconductor's silicon roadmap takes the technology to 1200 V.

"To reach higher voltages with the superjunction MOSFET, you grow additional epi-layers to get that thicker drift [region], which just gets more and more expensive as you get charged based on the numbers of process steps in the fab," he says. "But we're different. If you want a higher voltage, you need a deeper trench, so we look at how deep can we dig that trench - what aspect ratio can we reach? We believe that one day SuperQ will deliver a 1200 V MOSFET."

Etching ever-deeper, high-aspect-ratio trenches for higher-voltage MOSFETs is no small feat, but it's one that Rutter and colleagues believe they have mastered. With a newly acquired state-of-the-art trench etcher driving progress, they are now focused on integrating these deeper trenches into the MOSFET design - with qualification to follow. But how has the market responded to a new, high voltage MOSFET platform that is not based on wide bandgap semiconductors? High performance, energy efficient SiC and GaN devices from the likes of Wolfspeed, Infineon, EPC, Transphorm and more, have already made many in-roads into traction inverters, power supplies, fast chargers and myriad other applications. And despite recent upheavals, such as Wolfspeed's bankruptcy and TSMC pausing GaN production, market forecasts remain robust. Still, high performance and forecasts aside, these materials remain relatively expensive and can face supply bottlenecks compared with standard silicon used in most chips. Both Manack and Rutter are keen to emphasise how SuperQ MOSFETs can be cost-effectively manufactured with tools and processes commonly standard to CMOS fabs. Rutter points out that around 90% of SuperQ's production relies on established techniques used to fabricate vertical power trench devices while Manack notes that initial development took place on 300 mm CMOS.

"Having SuperQ on a silicon platform leverages a tremendous amount of existing tool-sets, and makes it very scalable," adds Manack. "We're not just increasing performance, we're also keeping costs under control." Recent partnerships with semiconductor distribution firms indicate that industry players agree. In July this year, iDEAL Semiconductor signed a global distribution agreement with Mouser Electronics, and also partnered with Richardson Electronics to gain access to its design and sales teams to expand the reach of its SuperQ MOSFETs.

"Some of the rhetoric in the industry has been that silicon is dead and you need to change materials and invent new tool-sets to improve performance," reflects Manack. "But this couldn't be further from the truth – what was dead was the new ideas and the R&D dollars."

CMOS: Not just for silicon

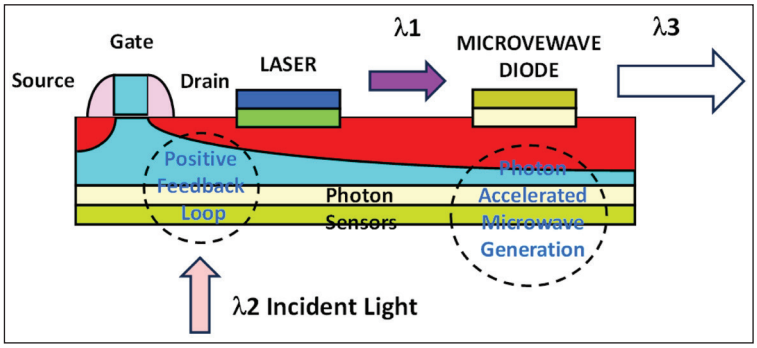
While CMOS may be synonymous with the manufacture of silicon ICs, it's a versatile process can also be applied to the production of photonic and microwave circuits employing compound semiconductors

BY JAMES PAN FROM NORTHROP GRUMMAN

SILICON ICs – invented in 1950s – are used in almost everything. Better known for their deployment in smartphones and computers, they are also integral to the operation of automobiles, washing machines, air conditioners, vacuum cleaners and so on. In all these cases, the ICs operate in total darkness, because silicon has an indirect bandgap. Due to this characteristic, silicon can absorb light, but it cannot emit it.

In our daily life, electrons and light are intertwined. We use electrons to generate light and other forms of electromagnetic radiation, such as microwaves. And while we might think of photons when we think about lasers and LEDs, they are electron devices – as are radar and lidar.

Now we need to start applying the principle of working with electrons and photons, which are intertwined, in ICs. Development is already underway, as compound semiconductors, such as GaAs, InP, and other III-V and II-VI compounds, are now used with silicon. Consider, for example, microwave photonic CMOS, which includes III-V or II-VI materials for lasers or millimetre-wave diodes, in the CMOS drain region, through a process called 'selective epitaxy'.



➤ Figure 1. Microwave photonic CMOS and image sensors. Positive feedback loops convert light to light currents. Photon-accelerated microwave generation produces modulated light wave and millimetre wave signals.

It's possible that these ideas might strike you as a little odd. I'm sure you have heard of the acronym CMOS – its full name 'complementary metal-oxide semiconductor' – and you'll know that it's a process employed to make billions of silicon ICs. But it's quite possible that this is the extent of your knowledge. And, to be fair to you, why should you know any more than this, given that many will believe that CMOS is not of any relevance to the compound semiconductor industry.

Well, I understand your position – but you are in danger of falling behind the times. Change is now afoot, thanks in part to our work at Northrop Grumman, a leader of lasers, millimetre-wave devices, and ASICs (Application Specific Integrated Circuits). We are developing a CMOS process for light-emitting structures and microwave circuits. It's a revolutionary breakthrough that will enable the integration of both compound semiconductors and silicon for almost 'all products' in the $500 billion CMOS industry, which is growing rapidly.

Our efforts are not the first to unite silicon and the compounds in ICs. Long gone are the days when silicon photonics is a new entity, having been pioneered by companies such as IBM and Intel, with products forming a small part of the IC industry. Today silicon photonics has already entered ULSI (Ultra Large-Scale Integration) markets, a point well-illustrated by the delivery of a webinar last August by Global Foundry's Anthony Yu, who gave a presentation entitled *Bringing Silicon Photonic Technology to the Forefront*). Within this development there's microwave photonic CMOS, involving modern processors that include hundreds of billions or trillions of CMOS transistors.

Based on such activities, a new trend is emerging – most, or even all of these many billions of CMOS transistors are no longer going to be fabricated only in silicon. Instead, they will incorporate GaAs, InP, or other compound semiconductors used in lasers and LEDs.

Behind this revolution is the move in modern societies to replace wireless tools with non-wireless tools, a migration observed in the uptake of smartphones, and changes to the connectivity of computers. In this particular case, the advantages of implementing compound semiconductors with silicon are wireless ULSI, and eliminating heating of the copper wires, and delays associated with their resistance and capacitance. There's the promise of replacing billions of copper wires in ULSI with wireless photonic CMOS technologies.

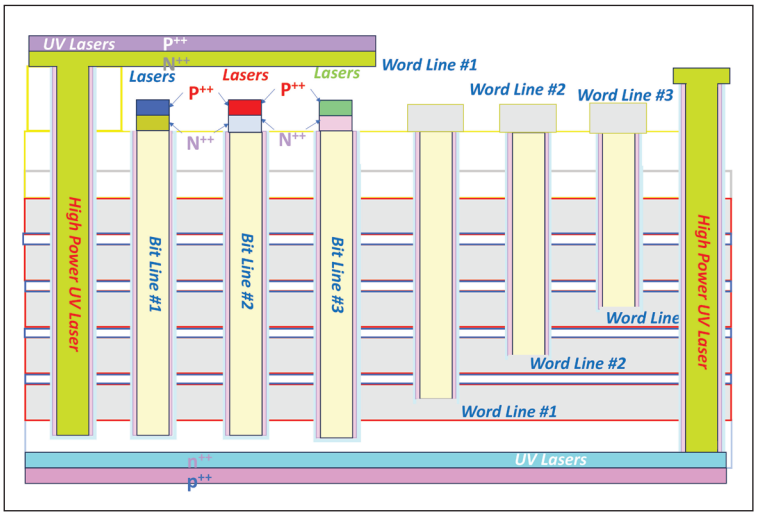
You may be wondering how III-Vs are introduced using a CMOS process. One illustrative example is the addition of GaAs in the CMOS silicon drain region, using either low-temperature selective CVD or selective epitaxy. For the former, the CVD tool includes an *in-situ* chamber in ultra-high vacuum, where native oxides on silicon are sputtered and etched, prior to sending the wafer to the CVD chamber for GaAs epitaxy. Note that all these processes proceed under high vacuum.

As GaAs is deposited right before the silicide process, in the BEOL (Back End of the Line), there are no contamination concerns, enabling the use of silicon lines (see Figure 1 for an illustration of the process integration of photonic CMOS).

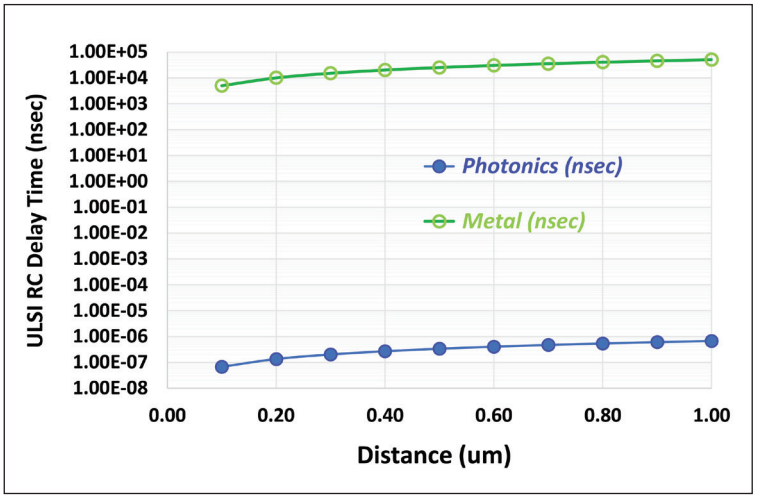
Thanks to the introduction of III-Vs, the era of microwave photonic CMOS is within our grasp. For this technology, options for the optical source include GaAs LEDs, emitting in the 800 nm to 900 nm range, threshold-less tunnel lasers on silicon, and microwave-generating devices. Note that microwave photonic CMOS can outperform traditional laser diodes, due to improved thermal reliability, higher external quantum efficiencies, and superior lasing powers.

To produce microwave photonic CMOS, an ultra-low-resistance threshold-less tunnel laser or LED is crafted in the drain region; and in either the well, channel or below the drain region, narrow-bandgap photon sensors or avalanche photodiodes are added, made from SiGe or other compound narrow bandgap materials. In addition, microwave diodes, made from silicon, SiGe, or other compound semiconductors, are added in the drain region. Note that the MOSFET, lasers, microwave diodes, and photon sensors are fabricated as one integral transistor.

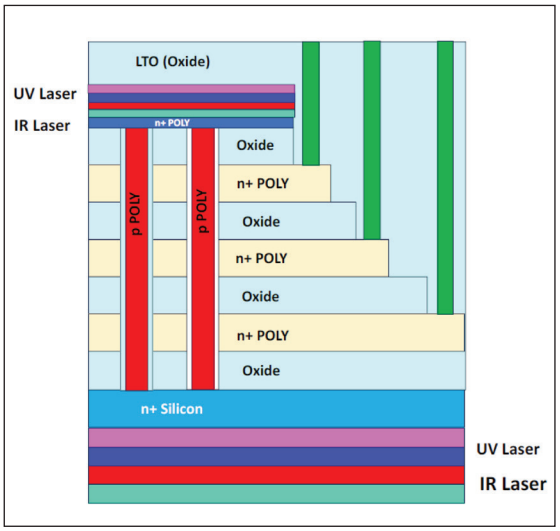
Alongside the optical sources, dielectric micro-optical waveguides are transferred that are suitable for sub-1 nm CMOS technology nodes. The dimensions of the micro-optical waveguides can be less than 100-300 nm, with guided optical signals confined with total reflection, despite the wavelength being longer than the width of the waveguide. For the sub-1 nm nodes, channel length is typically 5-20 nm, but the 'width' of the CMOS can be in the range of hundreds of nanometres, or even a few microns.



➤ Figure 2. Ultra-High-Speed Microwave Photonic Vertical NAND FLASH.



➤ Figure 3. Wireless ULSI with Photonic CMOS – significant reduction of RC delays and heat.



➤ Figure 4. An alternative method of fabricating Ultra-High Speed Microwave Photonic Vertical NAND FLASH (Vertical NAND FLASH, which has replaced NOR FLASH.

There is no doubt that these new forms of CMOS have great potential. One of their greatest assets is that the laser microwave CMOS process is 100 percent compatible with existing CMOS fabrication, and there is no threat of cross contamination. Another exciting opportunity is the introduction of far more sophisticated nonlinear optical computing. However, there are challenges – compared with photonics computing, which is already available and implemented, microwave computing needs advanced knowledge, and the development of micro-antenna, microwave filters, multiplexers, and designs.

I'm not saying that applying CMOS to the compounds is easy. But the rewards justify the endeavour.

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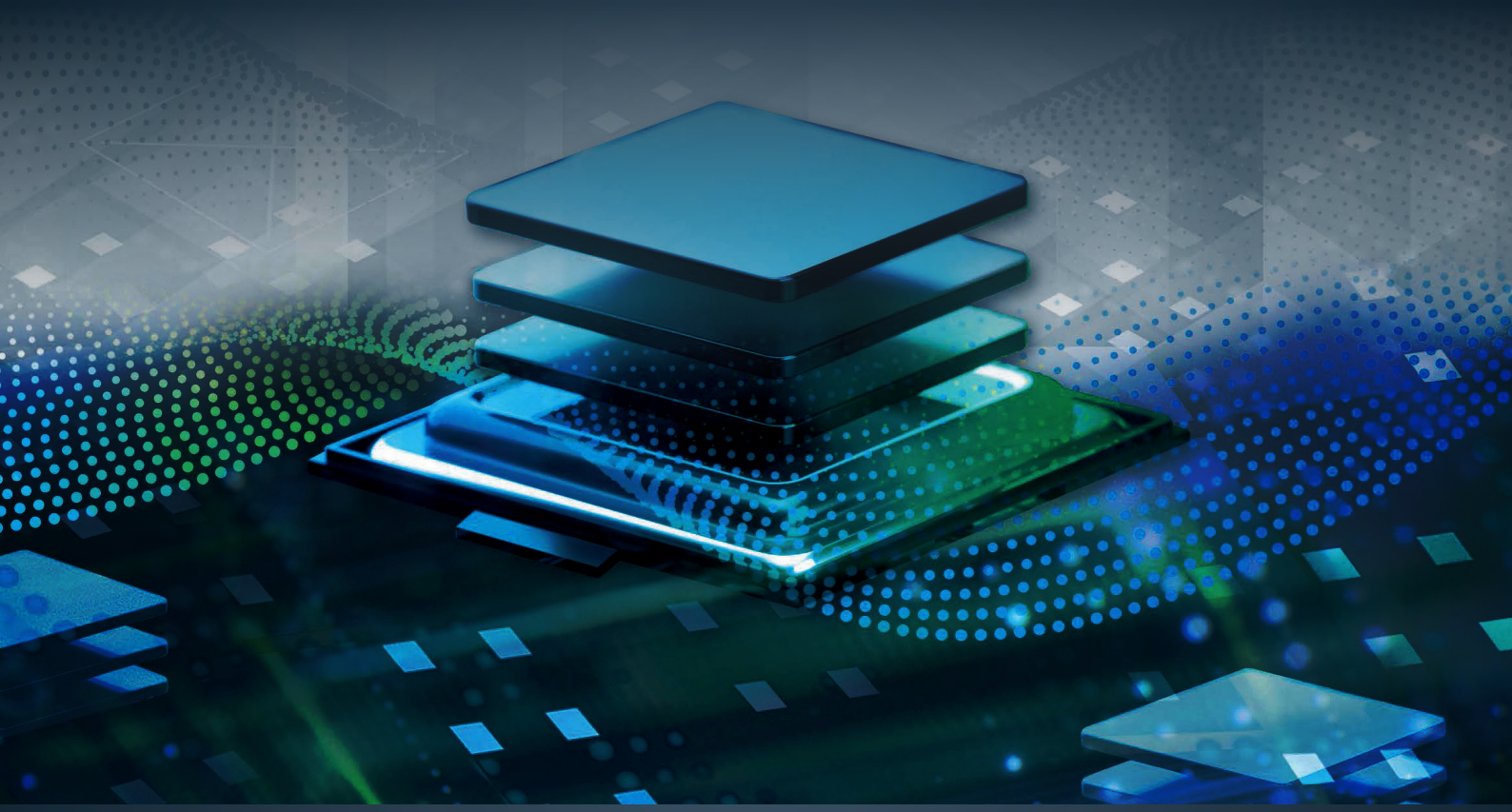
MKS Advanced Packaging Handbook



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Targeting semiconductor packaging pain points with multiphysics simulation

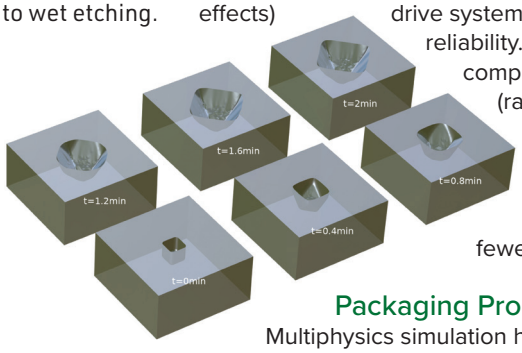
Multiphysics simulation can be used in semiconductor packaging to predict performance and ensure packaging reliability. This article goes over the areas of packaging where simulation can improve R&D.

BY ANDY CAI, COMSOL, INC.

THE PERPETUAL DRIVE to shrink semiconductor components means ever-increasing complexity — the need for denser integration, tighter thermal margins, and stricter reliability requirements has become more severe. In advanced packaging, especially for emerging 3D chip architectures, this complexity is amplified by vertical stacking, high-density interconnects, and diverse material interfaces. Challenges like warpage, interconnect fatigue, and thermal stress aren't isolated issues; they're tightly coupled and difficult to manage through testing alone. Modeling and simulation has become more common in packaging for addressing such challenges. However, even with the growing adoption of simulation, there remains a general hesitancy to fully embrace it.

It's true that parameters like material behavior carry uncertainty, so numerical models must rely on additional physics assumptions and simplifications. It's also true that no model can capture every detail of the physical world, but the goal of simulation isn't to mirror reality perfectly. Simulation is meant to help teams address design challenges and gather critical insight that can guide development decisions. When built thoughtfully, models can reveal dominant effects and clarify cause-and-effect relationships.

Multiphysics simulation is particularly powerful in semiconductor packaging, where coupled effects (e.g., thermal, mechanical, and sometimes electrical effects) drive system performance and reliability. Moreover, simulation complements testing (rather than replacing it), helping teams reduce iteration cycles and make better decisions with fewer surprises.



➤ Figure 1. The development of an etched groove shape over time due to wet etching.

Packaging Process Simulation

Multiphysics simulation has made a difference in various areas of semiconductor packaging. Below, we highlight some of these application areas.

Wet and Dry Etching

Both wet and dry etching are essential for the creation of features in advanced packaging, and both processes can be simulated accurately despite their complexities.

When simulating wet etching, chemical reactions as well as mass transport need to be considered. The interaction between fluid transport, diffusion, and reaction kinetics can be simulated and optimized to ensure etch uniformity or minimal undercutting. Conversely, dry etching can require significantly more complex physics couplings, as it involves plasma chemistry, ion transport, and directionally dependent material removal. Regardless, the right tools will enable you to model this process accurately.

Figure 1 shows an example of anisotropic wet etching of silicon, based on the different etching rates of silicon's crystal planes in a KOH solution. In the model, a small initial groove on the wafer surface comes into contact with the KOH solution, and pyramid-shaped grooves gradually form over time due to the crystal-plane–dependent chemical etching reaction.

Soldering Process

Solder joints and the reflow process used to create them are crucial in semiconductor packaging but can also be sources of significant reliability challenges, including thermal fatigue and warpage. To give one example, warping of a die from internal stresses can build up during the reflow process (Figure 2) and adversely affect a component's performance or cause early failure.

The melting and solidification behavior typical in the soldering process is often hard to predict, but it can be accurately simulated to provide insight into how thermal loads will evolve and

how stress will develop as materials transition from liquid to solid. Multiphysics modeling can replicate the metallurgical phase transitions and the residual stress state with multiple metal phase transformations. These visualizations can offer insight into the mechanical reliability of the solder joints and the operating conditions in which they will succeed. Solder joints are typically modeled with temperature- and rate-dependent viscoplastic (creep) constitutive laws, since stresses evolve during reflow and thermal cycling. Elastic–plastic and fatigue/damage models are added as needed to capture irreversible deformation and predict life.

Underfill

Underfill adhesives often exhibit non-Newtonian flow behavior, requiring rheological models and temperature-dependent properties. When these adhesives cure, they create residual stress and warpage. To get a complete understanding of underfill phenomena, it's best to use a multiphysics approach to assess both the chemical kinetics of the curing process and the resulting mechanical deformation within the same simulation space.

Grinding, Dicing, and Molding

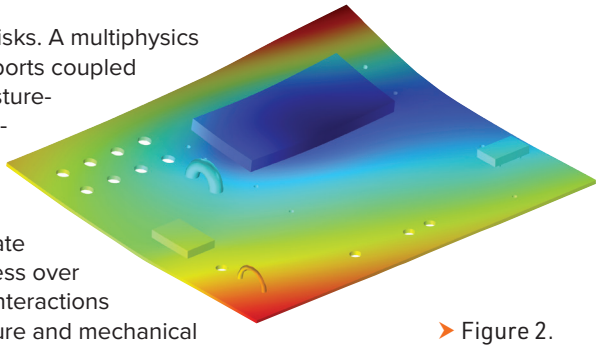
Mechanical operations in semiconductor packaging usually involve grinding, dicing, and molding (Figure 3). While these are routine steps, they introduce stresses and carry a risk of cracking in the packaged product. In particular, the risk of cracking is highest near edges and interfaces. Multiphysics simulation can be used to assess the impact of cutting forces and thermal effects on structural integrity.

Package Reliability Simulation

When testing package reliability, it's critical to consider environmental factors such as ambient humidity and moisture ingress through diffusion into materials. Let's talk about the areas where multiphysics simulation can play a role in ensuring packaging reliability.

Humidity and Moisture Ingress

The presence of moisture has damaging consequences: hygroscopic swelling, corrosion, and delamination risks. A multiphysics approach supports coupled heat- and moisture-transfer (hygro-thermal) modeling, allowing users to simulate moisture, ingress over time, and AC interactions with temperature and mechanical stress. This modeling is particularly useful for predicting failure during preconditioning or accelerated life testing, as it can reduce the amount of prototyping and testing.



➤ Figure 2. Warpage in a semiconductor after reflow soldering.

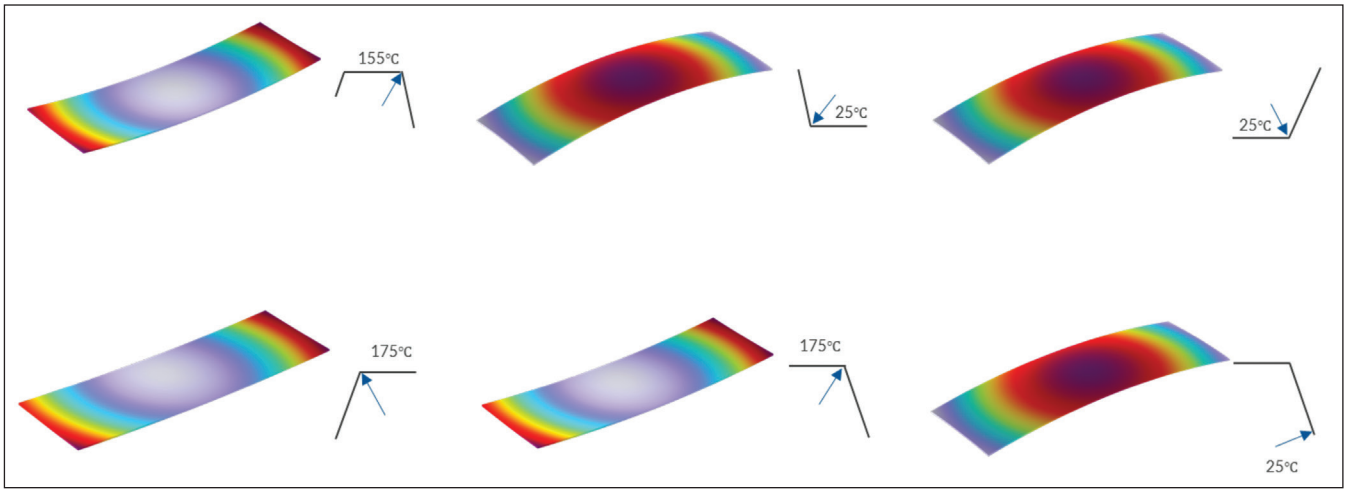
Structural Damage and Failure

When things go wrong, multiphysics simulation can be used for detailed failure analysis. Whether the failure is due to interfacial delamination, crack initiation and growth, or even thermal fatigue of solder joints, there are methods for virtually assessing what went wrong and how it can be prevented. Users can create models that include fracture mechanics for crack risk estimation as well as simulate progressive crack growth. In Figure 4, you can see a stress singularity at the crack tip in a sample plate geometry.

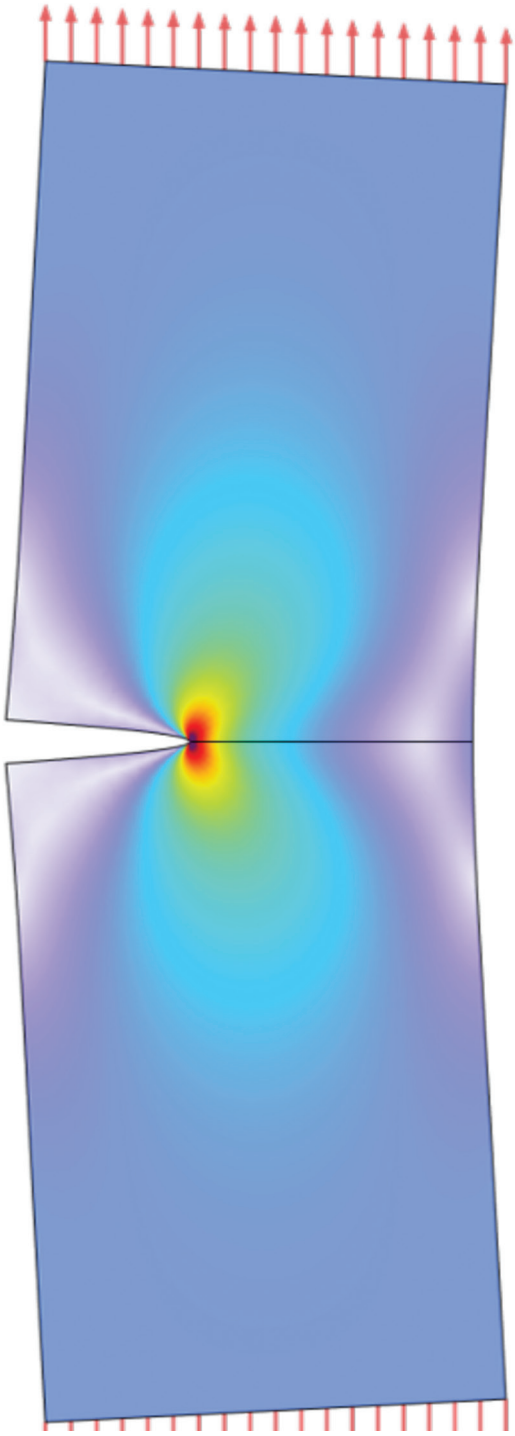
Shock, Vibration, and Static Loads

When modeling semiconductor packaging, it is important to account for mechanical shock and vibration and evaluate how these loading conditions affect package reliability. Models can be used to analyze the vertical displacement of a motherboard from a response spectrum evaluation, as shown in Figure 5. This need is especially heightened for mobile or automotive applications where semiconductor packages must withstand various dynamic stresses.

Users can perform a variety of dynamic mechanical analyses, including frequency-domain studies, impact simulations, response spectrum evaluations, and random vibration modeling. Similar approaches can be applied to assess package response to static



➤ Figure 3. Warpage evolution during the epoxy molding compound (EMC) molding process.



➤ Figure 4. A geometry showing the von Mises stress and the deformed shape of a cracked plate. Note that the displacement is exaggerated to illustrate the deformation under the applied load.

mechanical stresses, such as bending, torsion, or compression. These evaluations support design validation for a range of scenarios, such as a four-point bending test.

Thermal Management in Packaging

Thermal management is a multiphysics process that requires thermoelectromechanical simulation and CFD simulation. In advanced packaging specifically, these models require significant computational resources for computation. This is particularly true when working with 3D stacked layers or, in general, when including designs with a large number of components.

Simulation users benefit by coupling the three primary heat transfer modes in the same model: conduction, convection, and radiation. This coupling gives users the option to decipher the individual impact on different pieces of the overall system. For example, for a device in a package with air gaps, heat sinks, and a surrounding enclosure, users may want to include all three heat transfer modes but find that only one or two of the mechanisms will be the dominant dissipation or heating mechanism. Simulation enables users to easily turn on and off each mechanism and test it until they have a better understanding of how each one impacts the results.

In electronic packages, heat sources often arise from electromagnetic loss mechanisms such as resistive (ohmic) heating, eddy current losses, or dielectric heating in RF components. Simulation can couple these electrical and magnetic effects with thermal and mechanical responses, incorporating temperature-dependent material properties for metals and substrates.

Electromagnetic Performance in Packaging

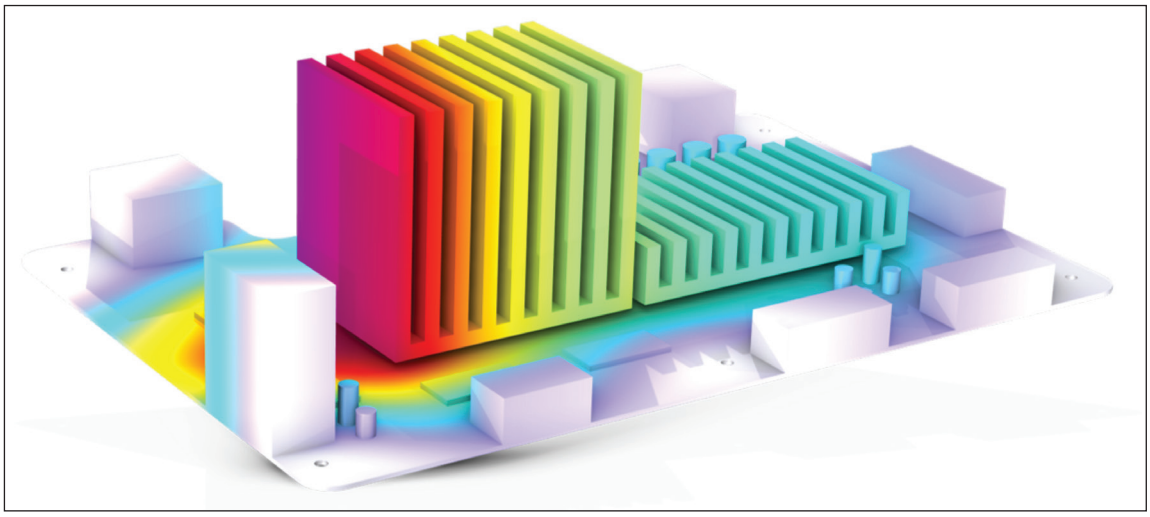
Electromagnetics simulation can be used to analyze how packaging affects signal propagation, including high-frequency effects such as skin and proximity effects. It can also evaluate how different geometries or materials influence transmission-line performance. This capability is valuable for predicting and mitigating signal integrity issues early in the design process, before hardware fabrication, to help rule out potential problems. A multiphysics approach enables coupling of detailed finite element (FEM) electromagnetic models with circuit-level simulations, supporting mixed-domain modeling in which part of the signal path is analyzed in full-wave detail while the remainder is represented by circuit elements. Users can automatically generate SPICE-compatible circuit models from extracted data and simulate signal reflections, losses, or noise to trace their origins to specific physical structures, which can be useful for both design and verification.

Bringing Simulation to the Factory Floor

Let's switch gears and discuss a specific modeling tool and how it can spread the use of simulation throughout organizations.

Through simulation apps, models can be brought into the field or onto the factory floor. These custom-made simulation tools can present team members with the information most relevant to their work, as opposed to presenting a full software user interface or unrelated data. App users can easily modify input parameters and study the computational results, even if they don't have foreknowledge of the underlying model or simulation software.

In semiconductor packaging, complex models can be compiled into apps and shared with team members who are not simulation experts. Figure 6 shows a thermoelectric cooler simulation app



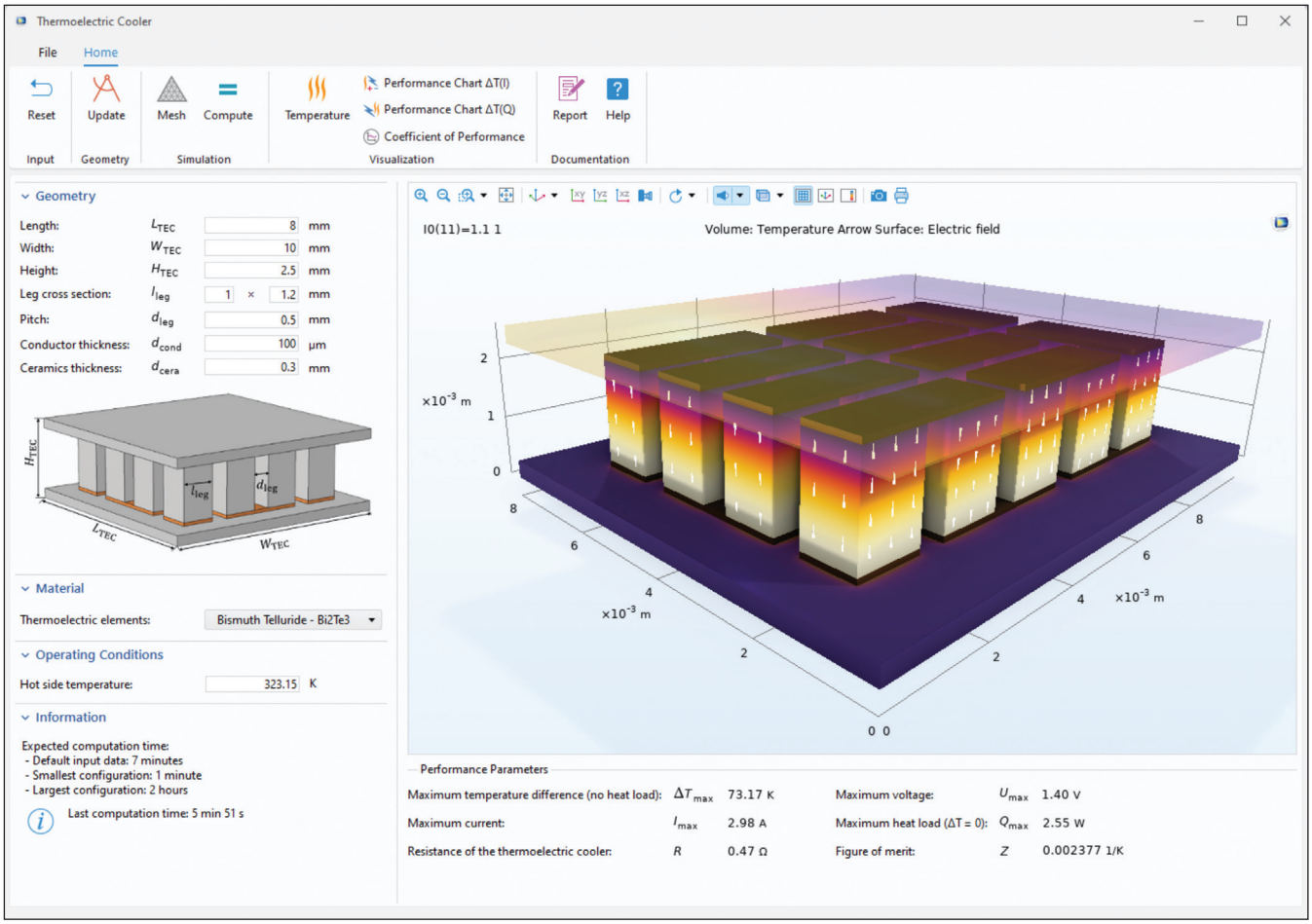
➤ Figure 5. A motherboard's vertical displacement as a result of a response spectrum evaluation.

with a specialized interface that contains only the parameters needed for specific analysis cases. This type of app can be used to examine current and temperature distributions for different inputs, enabling critical analyses to be performed easily and without the help of a simulation expert.

In this article, we have touched on common application areas within semiconductor packaging where multiphysics simulation can be used.

Multiphysics is how the world works, and semiconductor packages are proof of this point. With devices only getting more complex, it's only right that the tools we use to assess their design and operation have powerful, growing functionality.

Multiphysics simulation can help give R&D departments an understanding of where they need to move their design in tandem with their real-world experimentation.



➤ Figure 6. A simulation app that enables users to analyze single-stage thermoelectric cooler designs by testing various geometries, thermocouple configurations, and materials.

AI enables co-optimisation of devices and materials

In an interview with Silicon Semiconductor, **Vijay Narasimhan, Director of R&D Collaboration, EMD Electronics**, the North American electronics division of Merck KGaA, explains how AI for materials discovery and intelligence is helping the company to push the boundaries to revolutionize materials discovery by identifying new materials and optimising materials intelligence for greater efficiencies.

IN AN ERA when artificial intelligence, augmented reality, and hyper-connected devices are redefining the world's technological ambitions, the invisible foundation of it all remains the same: materials. Behind every chip that powers a data centre, every OLED display, and every AI accelerator lies an intricate ecosystem of chemical compounds, thin films, and engineered layers that enable performance, power, and precision. And a key contributor to this materials revolution is EMD Electronics, the electronics business of Merck KGaA, Darmstadt, Germany - a company whose history of scientific innovation stretches back almost 360 years.

It's quite possible that most people have never heard of EMD Electronics, yet it's almost certain that everyone has touched or used one of its materials today. Whether scrolling on a smartphone, checking an OLED display, or connecting to the cloud, EMD's chemistry underpins the electronics that define modern life. Now, as the semiconductor industry enters an age where scaling in two dimensions is reaching its physical limits, EMD Electronics is helping to lead the way into a new paradigm: a world where materials intelligence - an AI-driven fusion of digital and physical discovery -accelerates the creation of the next generation of electronic materials.

From shrinking to stacking

For decades, the semiconductor industry's trajectory followed a simple principle: make everything smaller. Through relentless miniaturisation, engineers were able to double transistor density and performance roughly every two years, in line with Moore's Law. In those early phases, only a handful of core materials were needed, and innovation centred on lithography precision and silicon purity.

But as feature sizes dipped into the single-digit nanometer range, traditional scaling began to falter. To keep pace with computing demands, engineers had to look beyond simple geometry. "We entered an era where we needed to go beyond those traditional scaling limits," explains Vijay Narasimhan, Director of R&D Collaboration at EMD Electronics. "We introduced a lot of new materials - at the interfaces between layers, within the layers themselves, and in the way we pattern those layers."

This shift marked a profound change in how materials were perceived. No longer passive enablers, they became active performance drivers. Even the materials that never make it onto the final chip, those used in patterning, etching, and deposition, became essential to enabling ever-smaller dimensions and more complex architectures.

Now the industry stands at the threshold of yet another leap: the vertical revolution. Rather than continuing to squeeze circuitry onto a single plane, chipmakers are building upwards, stacking chips like skyscrapers to pack more power into the same footprint. These three-dimensional designs, already visible in leading AI processors and advanced memory systems, demand materials that can meet increasingly conflicting requirements - mechanical strength, electrical conductivity, and thermal stability - simultaneously. "You're manipulating electrons in devices that have very strict requirements," says Vijay. "Materials engineering, and therefore the chemicals that underlie them, are more critical today than ever if we want to keep the pace of computing power scaling."

From intuition to intelligence

Historically, materials development has been an exercise in creativity, craftsmanship, and persistence. Chemists with deep domain expertise devised new formulations, often inspired by intuition and the nuanced needs of customers. Each concept moved through a meticulous process of synthesis, characterisation, and testing. Promising candidates were then sent to semiconductor manufacturers for evaluation - a feedback loop that could take months or even years.

This model, though rigorous, struggles under the weight of modern complexity. Each new chip generation requires not just one or two new materials but dozens, each with its own performance constraints and interdependencies. "Just with the number of layers and materials we need to develop today," notes Vijay, "we really need a shift in how we're doing this research."

That shift is already underway, driven by what EMD Electronics calls materials intelligence. It's a vision that unites human creativity, artificial intelligence, and automated experimentation into a continuous loop of learning and optimisation.

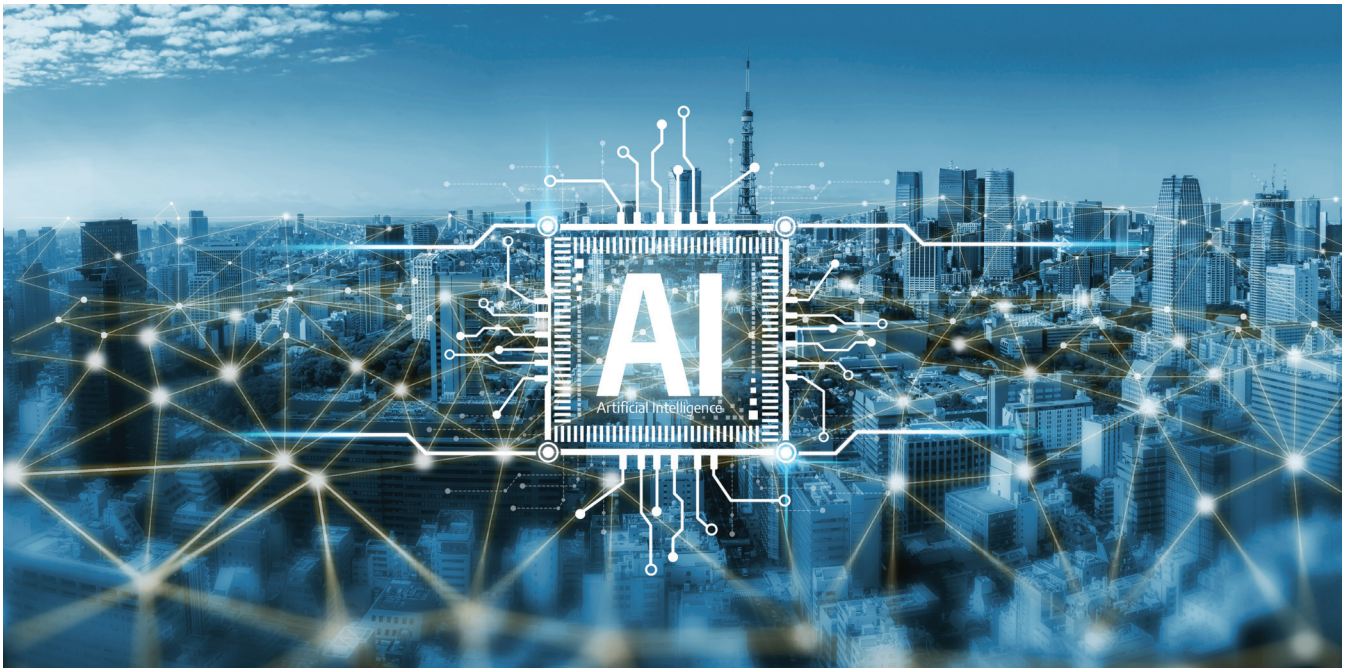
Imagine, as Vijay suggests, an infinity symbol. On one side lies the digital world: a realm of simulations, models, and virtual materials, where data and algorithms can explore chemical spaces at machine speed. On the other side lies the physical world: the realm of experimentation, synthesis, and validation. The two halves continuously inform and refine each other, closing the loop between imagination and implementation.

This dual-world approach allows EMD to move from a slow, sequential model of discovery to an agile, parallel one. Digital exploration suggests new materials; automated labs test them; data flows back into digital twins, refining predictions with every iteration. The result is a self-improving system that learns not just from success but from every experiment conducted.

Digital Twins: the virtual laboratories of the future

At the core of materials intelligence lies the concept of the digital twin, a digital representation of a physical material or process that behaves, as closely as possible, like the real thing. In EMD's world, a digital twin can predict a material's properties, such as conductivity, adhesion, or thermal performance, before it is ever synthesised in a lab.

To build such a twin, EMD begins with decades of experimental data. But as with most industrial research organizations, that data exists in countless formats: spreadsheets, lab notebooks, imaging systems, and academic publications. Extracting knowledge from this heterogeneous sea of information is a monumental challenge. Here, large language models (LLMs) and vision-language models (VLMs play an unexpected but powerful role.



"These models are incredibly effective at pulling out important assets and bringing them together in a searchable way," explains Vijay. "That gives us a foundation for building our digital twins." Once the data is structured, predictive algorithms, based on advanced physics and machine learning, can estimate material properties with increasing accuracy.

This predictive capability fundamentally changes the pace of innovation. A scientist with a new idea can now "plop" a virtual molecule into a model and receive a prediction of how it might perform, without spending months in the lab. Only the most promising candidates proceed to synthesis and testing, saving vast amounts of time and resources.

Generative chemistry: when AI designs molecules

The predictive power of digital twins is only part of the story. The next frontier lies in generative AI for chemistry - algorithms that can design new molecules or formulations from scratch.

Much like a writer prompts a language model with a question, a chemist can now prompt a generative model with a set of desired properties: for example, 'a dielectric material with high thermal stability and low leakage current'.

The AI then generates molecular structures or formulations that meet those criteria, guided by the predictive models' scoring functions. This feedback ensures the system explores only the most fruitful regions of chemical space.

The implications are profound. Chemical space is unimaginably vast - so vast that even supercomputers struggle to comprehend its scope. In one example, EMD described film stacks with 60 layers, each offering three possible materials - a combinatorial explosion amounting to 10^38 possible configurations. "It's such an impossibly large number that even ChatGPT couldn't give a good analogy for it," Vijay jokes. Searching that space through brute force is unfeasible; guiding the search intelligently through AI is transformative.

The rise of the Smart Lab

The physical counterpart to this digital innovation is EMD Electronics' high-throughput experimentation facility, Intermolecular, located in San Jose, California. Here, autonomous and semi-autonomous systems carry out synthesis, deposition, and characterisation at scales no human team could match. Robots handle materials, run experiments, and record results in structured databases - all feeding back into the digital loop.

Yet even this automation benefits from AI's analytical prowess. By applying Bayesian optimization and active learning, EMD's systems can adapt in real time, learning which experiments are most valuable and discarding unproductive paths. Rather than systematically testing every possible combination, the AI throws a few 'random darts', evaluates outcomes, and then focuses on the most promising areas of the search space. This approach mirrors how human scientists think - forming hypotheses, testing them, and refining based on intuition - but at a scale and speed that humans alone could never achieve. Crucially, human creativity remains central. EMD sees AI not as a replacement for scientists but as an exoskeleton for the mind, an augmentation that amplifies insight and intuition. "Humans are incredibly efficient heuristic thinkers," Vijay emphasises. "The creativity that comes from a conversation, a talk, or a spark of curiosity - that's really hard to replicate in silicon. We don't want to lose that."

In practice, that means every development cycle includes both machine-generated and human-suggested experiments. Each contributes unique value: the machine for speed and scale, the human for intuition and inspiration. Every data point, successful or not, helps refine the model. The process becomes not a handoff between man and machine, but a dialogue.

Structuring the past to build the future

No AI system, however sophisticated, can thrive without high-quality data. The semiconductor materials ecosystem, with its long legacy of discovery, faces a major challenge: decades of invaluable research stored in unstructured

formats. To address this, EMD Electronics is collaborating across academia and industry through initiatives like the Oasis Centre, a partnership with Intel and leading European universities.

These projects aim to create open-source methods for transforming scattered knowledge into structured, machine-readable formats. “We’ve discovered how effective large language models and vision-language models are at extracting information,” Vijay explains. “But going forward, we also need researchers to publish and store data in flexible, standardised formats, whether through electronic lab notebooks or open knowledge graphs.”

The goal is not just better data management but a cultural shift toward openness and collaboration. When researchers structure their findings in interoperable ways, every new experiment adds value to the collective digital ecosystem. As Vijay puts it, “You never quite know where science is going to go, and different pieces of the puzzle are filled in by different types of studies.” A flexible data framework ensures those pieces can always fit together.

The future of AI in materials research

As materials intelligence matures, one debate is emerging: should the field rely on vast, generalist AI models, capable of tackling multiple chemical domains, or on smaller, specialised models that excel at specific tasks? The tension mirrors discussions across the broader AI landscape. “There’s this push and pull between large foundational models and smaller domain-specific ones,” says Vijay. “It’s going to be very true in the chemical industry as well.” Some applications may demand comprehensive models that capture the nuances of diverse materials systems; others may benefit from modular architectures stitched together through agentic behaviour, where different AIs call on each other as needed.

Either way, the trend points toward greater integration - between algorithms, data types, and even disciplines. The company envisions a future where digital representations of materials flow seamlessly into digital representations of processes, allowing suppliers and chipmakers to co-develop and co-test innovations entirely in silicon before a single physical sample is exchanged. That, EMD believes, is the real promise of materials intelligence: smarter collaboration, faster feedback, and more sustainable innovation.

The next frontier of materials science

The convergence of AI, advanced materials, and semiconductor engineering is opening vast new opportunities, but also introducing new complexities. As devices stack vertically and functionalities intertwine, traditional trade-offs are being rewritten. Properties once considered acceptable compromises - between thermal conductivity and mechanical strength, for instance - must now be optimised simultaneously.

Emerging processes like area-selective atomic layer deposition and atomic layer etching illustrate this shift. These techniques enable self-patterning, placing materials precisely where needed without extra lithographic steps. The result is greater efficiency and fewer process layers, but also tighter tolerances and more demanding material behaviours.

At the same time, computing itself is evolving. Neuro-inspired architectures, where memory and computation coexist closely to mimic brain-like efficiency, are reshaping chip design priorities. The boundaries between memory, logic, and interconnects are blurring. “We’re going to have to target properties that are very different from what we’ve been targeting before,” Vijay observes. “There are trade-offs we could once accept that we can no longer tolerate.”

This convergence demands not only new materials but new ways of thinking about them. AI will help navigate this complexity, but human expertise remains the compass guiding discovery. By combining machine precision with human creativity, EMD envisions an innovation cycle faster and more collaborative than anything in the industry’s history.

Fusion at the frontier

While semiconductors form one pillar of EMD’s work, another lies in optronics - the science of how we manipulate and perceive light. EMD’s legacy in this space is visible everywhere, from liquid crystals in displays to the organic light-emitting diodes (OLEDs) in smartphones and TVs. Increasingly, the line between electronics and optronics is fading, as devices that once handled information or light separately now do both.

A striking example is augmented and virtual reality (AR/VR). These systems depend simultaneously on high-performance electronics for processing and on precision optics for rendering. “We’re moving toward a world where this doesn’t happen in a big helmet you strap on,” Vijay explains, “but in smaller and smaller footprints.” Shrinking AR systems from bulky headsets to lightweight glasses requires breakthroughs in every dimension: computing density, power management, heat dissipation, and optical efficiency. The challenge is as much materials-based as it is architectural.

Similarly, EMD is exploring neuro-inspired computing, where hardware mimics the brain’s ability to process and store information simultaneously. This paradigm affects every layer of the technology stack, from the memory cells that store data to the interconnects that shuttle information, and even the optical links that may soon replace traditional electrical connections at short distances. “It’s convergent,” says Vijay. “It brings together all the threads we’ve been working on - electronics, optronics, thermal management - and that just means more complexity, more requirements, and more need for innovative AI tools.”

Toward a smarter, more collaborative future

The semiconductor industry has always been defined by collaboration - between suppliers, foundries, and equipment makers - but materials intelligence promises to elevate that collaboration to a new level. With digital twins and shared data ecosystems, partners can now explore, test, and refine materials and processes virtually, long before a wafer hits the fab. This reduces waste, shortens development cycles, and opens the door to sustainable innovation at scale.

The vision EMD Electronics lays out is one where humans remain at the centre, not replaced by AI, but empowered by it. Scientists become orchestrators of intelligent systems, guiding discovery rather than grinding through repetition. Data becomes a shared language across disciplines, enabling insights that no single lab could achieve alone. And innovation becomes not just faster, but fundamentally smarter.

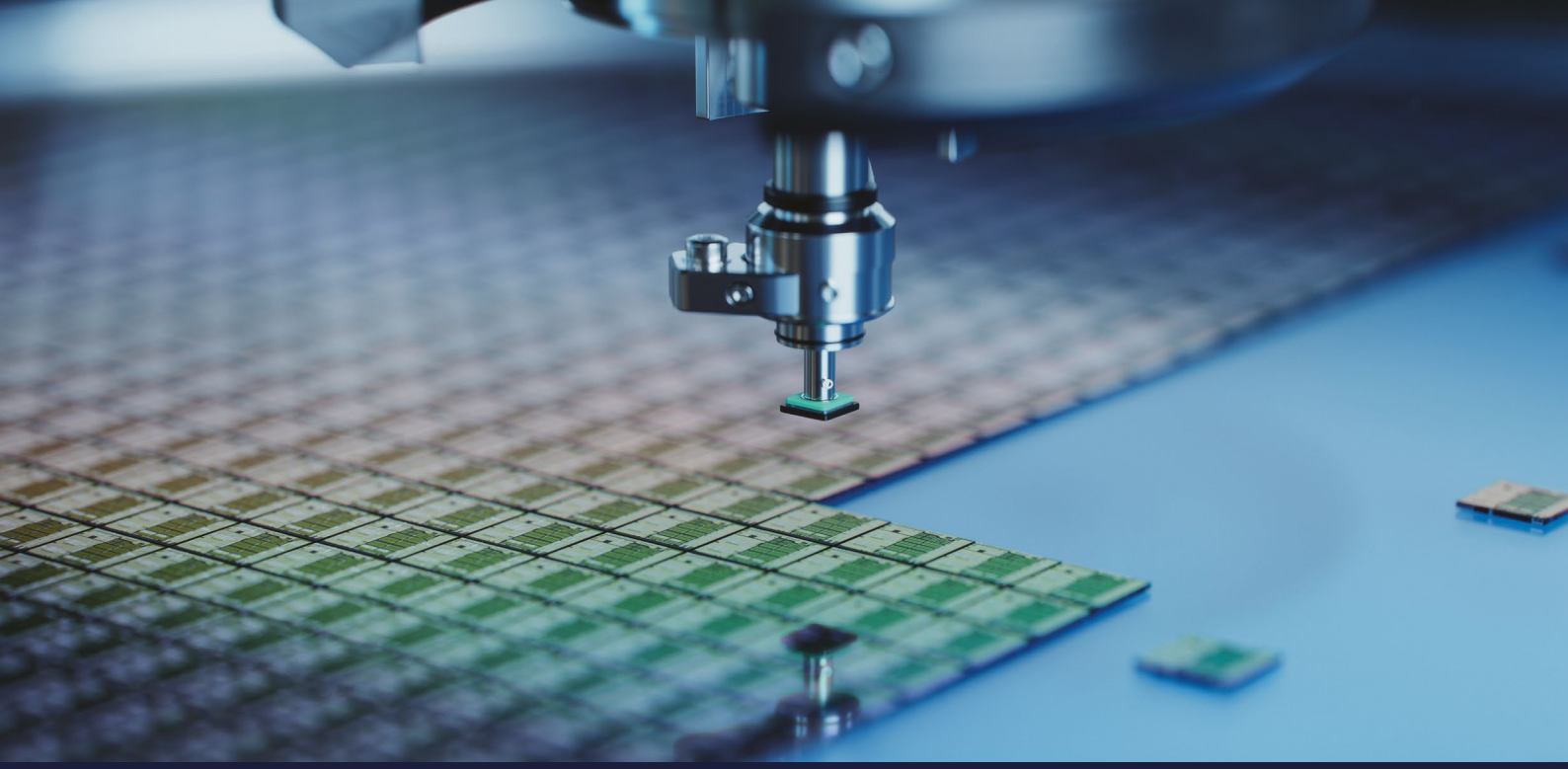
“We’re really in an era where, if we leverage these tools properly, we’ll be driving innovations faster than ever before,” Vijay outlines. “But more importantly, in a way that’s more collaborative than ever before - where digital representations of materials flow seamlessly into digital representations of processes. That’s the real promise of materials intelligence - to include humans in the loop, to improve collaboration, and to make the human innovation engine more capable for the future.”

The chemistry of the next revolution

As the boundaries of Moore’s Law blur and the semiconductor roadmap branches into new dimensions, one truth remains constant - progress depends on materials. The transistors of the AI age will be defined not only by their geometry but by the molecules that shape their behaviour, the algorithms that design them, and the humans who imagine them.

In EMD Electronics’ vision, the laboratories of the future will look as much like data centres as they do like chemistry benches. Virtual molecules will be tested before they exist; robots will conduct experiments guided by active learning algorithms; and scientists will collaborate through shared digital ecosystems that turn centuries of knowledge into instant insight.

It’s a vision that bridges past and future - a company founded in the 17th century harnessing 21st-century AI to shape the 22nd-century world. From molecules to machines, the journey of materials continues - and with materials intelligence as its compass, it shows no sign of slowing down.



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How simulation-driven engineering optimises sealing performance for semiconductors

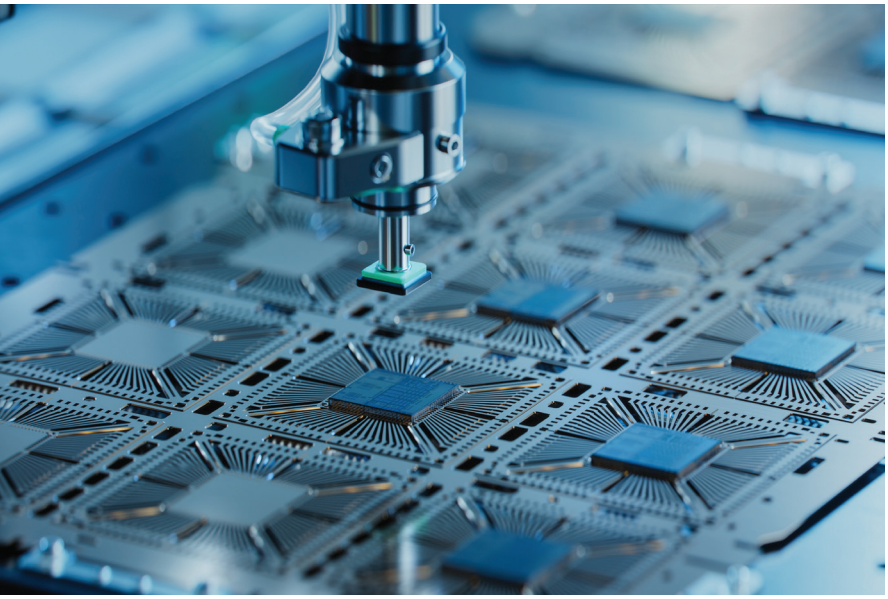
The semiconductor industry operates under extreme precision requirements where even microscopic failures can result in significant yield losses and costly downtime. Traditional testing methods, while reliable, often require months or years to validate seal performance under real-world conditions. Offered by component partners like Trelleborg Sealing Solutions, simulation-driven engineering is an approach that can predict seal behavior years into the future within hours of computational analysis.

BY ALAN ASTBURY, SIMULATION METHODS DEVELOPER, TRELLEBORG SEALING SOLUTIONS

THIS advanced methodology combines material science expertise with sophisticated computational tools to optimize sealing solutions before they reach production environments. By leveraging simulation technology, engineers can now predict compression set behavior, analyze dynamic responses and optimize seal designs to maximize performance in semiconductor applications.

Understanding Simulation Capabilities in Sealing Applications

Modern simulation technology extends far beyond basic stress analysis. Advanced simulation platforms can model complex material behaviors including hyperelastic properties, viscoelastic responses and long-term aging effects that directly impact seal performance.



Material Behavior Modeling

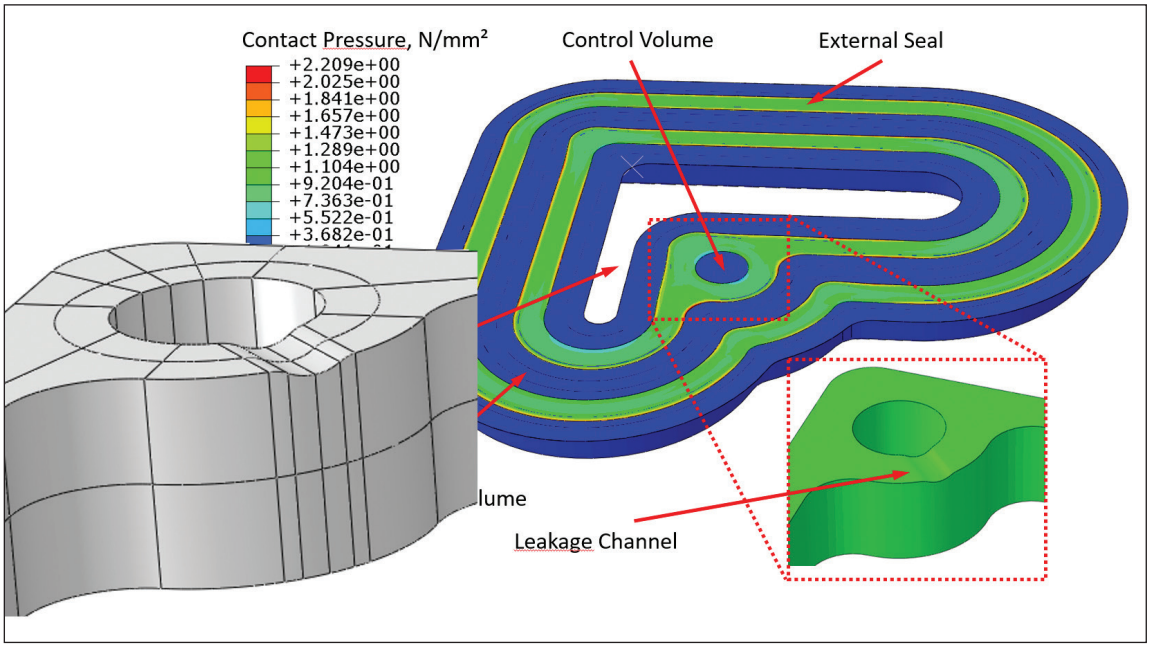
Elastomer seals exhibit nonlinear behavior under various conditions. Simulation software accounts for these complexities by incorporating hyperelastic material models that accurately represent how seals respond to deformation, temperature changes and dynamic loading conditions. This includes modeling the Mullins effect, where loading and unloading cycles on a material follow different stress-strain paths.

The simulation process begins with comprehensive material characterization using standard tensile testing equipment and dynamic mechanical analyzers (DMA). The DMA generates frequency sweeps at various temperatures, providing essential data for calibrating simulation models to match real-world material behavior.

Multi-Stage Analysis Approach

Expert seal suppliers like Trelleborg approach seal simulation with a multi-stage analysis. The process typically begins with thermomechanical analysis, where engineers couple mechanical responses with temperature effects and thermal expansion. This is followed by aging simulation using specialized subroutines that predict long-term material property changes. Finally, the analysis concludes by bringing the model back to normal conditions to assess final seal performance.

One of the most valuable applications of simulation-driven engineering is predicting compression set



Compression set control volume detecting leakage after a period of time, which is talked about in the article.

behavior over extended periods. Compression set occurs when elastomer seals lose their ability to return to original dimensions after prolonged compression, directly impacting sealing effectiveness.

At the molecular level, elastomers consist of long polymer chains connected by cross-links. Under sustained compression and elevated temperatures, these cross-links break and reform at shorter distances, preventing the seal from returning to its original shape. Simulation models replicate this behavior by tracking bond breaking and reformation processes over time.

Temperature and time are the primary drivers of compression set. Higher temperatures accelerate the process, which simulation engineers leverage through time-temperature shifting principles. This approach allows validation of years-long predictions using accelerated testing at elevated temperatures.

Practical Applications in Semiconductor Equipment

Consider a dual seal arrangement in semiconductor processing equipment designed to operate for seven years. Through aging simulation, engineers can predict when contact pressure will drop below critical thresholds, enabling proactive maintenance scheduling. The simulation might reveal that a pressure relief channel will lose contact after seven years while maintaining primary sealing function, providing an early warning system for maintenance needs. This predictive capability eliminates the need for extensive long-term testing while providing confidence in seal performance throughout the equipment's operational life.

Dynamic Response Analysis and Optimization

Semiconductor manufacturing equipment often involves dynamic conditions including vibrations, pressure fluctuations and mechanical movements. Nonlinear viscoelastic simulation addresses these challenges by modeling both elastic and damping properties of seal materials. In a nonlinear viscoelastic simulation, the material's response to stress or strain is not directly proportional to the applied load. This means that the relationship between stress and strain is more complex and can change depending on the magnitude and duration of the applied forces.

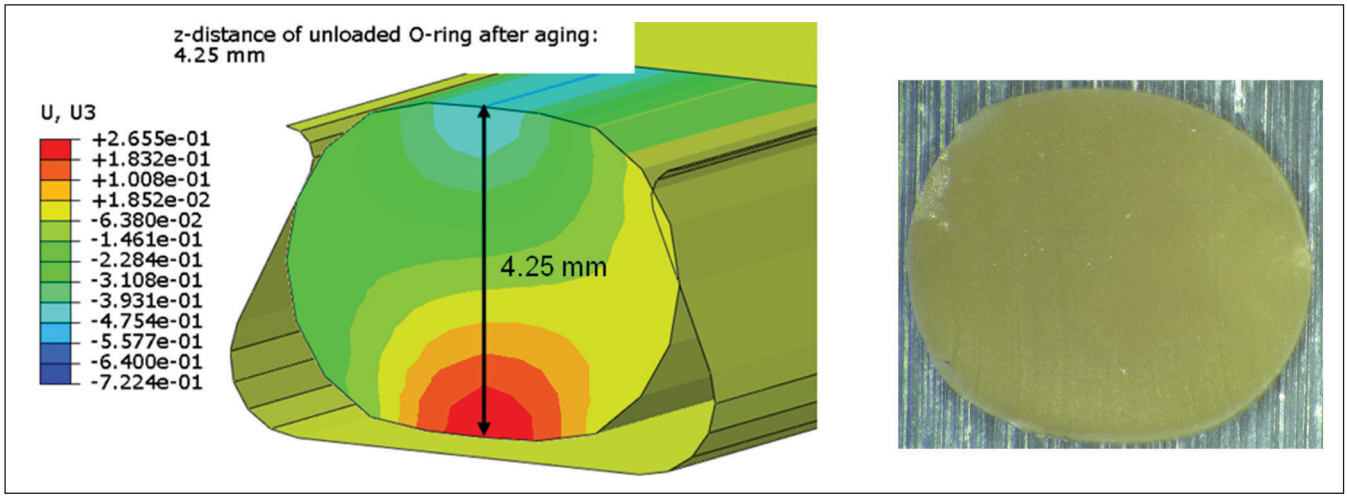
Vibration Isolation and Damping Optimization

Dynamic simulation enables engineers to optimize seal designs for specific frequency responses. For applications requiring vibration isolation, such as protecting sensitive measurement equipment from environmental disturbances, simulation can identify optimal material properties and geometric configurations. The analysis considers natural frequencies and damping characteristics to achieve desired isolation performance. By testing multiple material formulations virtually, engineers can select the optimal combination before manufacturing prototype parts.

Advanced Simulation Capabilities

Simulation extends beyond seal performance to manufacturing process optimization.

- **Wear Prediction Modeling**
  Seals in semiconductor equipment experience continuous wear throughout their service life. Advanced simulation techniques can predict wear patterns over months of operation, showing how sharp seal edges gradually wear to flat surfaces. This capability enables engineers to optimize seal geometries for extended service life. Wear simulation correlates well with real-world measurements, providing confidence



➤ Compression set after 37 years compared to a real O-Ring.

in predicted maintenance intervals and helping prevent unexpected failures.

- **Design Optimization Techniques**
  Modern simulation platforms offer both parametric and non-parametric optimization capabilities. Parametric optimization adjusts specific dimensional parameters to achieve performance targets, such as reducing stress concentrations by 11 percent through heel geometry modifications. Non-parametric optimization, while less applicable to sealing applications due to its tendency to create holes in components, proves to be a valuable technique for structural elements and assembly tooling design.

- **Manufacturing Integration and Quality Assurance**
  Simulation also ensures part quality from production. Injection molding simulation optimizes heating channel designs, gate locations and process parameters to achieve uniform material flow and minimize defects. It enables proactive quality management by identifying potential failure modes before they occur in service. Simulations account for material shrinkage, enabling precise tolerance control in final parts. This capability is particularly important for semiconductor seals where dimensional accuracy directly impacts performance.

- **Preventative Maintenance Scheduling**
  Advanced aging simulation provides specific timelines for seal replacement, enabling equipment operators to schedule maintenance during planned downtime rather than responding to unexpected failures. This approach significantly reduces overall maintenance costs and improves equipment uptime.

- **Material Selection Optimization**
  Simulation facilitates rapid comparison of different seal materials for specific applications. Engineers can evaluate how various elastomer formulations respond to temperature cycling, chemical exposure and mechanical stress without extensive physical testing.

The Future of Simulation in Sealing Technology

Emerging trends in simulation technology point toward molecular-level modeling capabilities that will enable virtual chemical compatibility testing. While these advanced techniques remain several years from practical implementation, they represent the next frontier in predictive seal engineering. Multi-scale modeling approaches will eventually bridge molecular behavior with macroscopic seal performance, providing unprecedented insight into material behavior under various service conditions.

Maximizing Value Through Simulation Partnership

Simulation-driven engineering delivers the greatest value when integrated early in the design process. It also requires close collaboration between a seal supplier like Trelleborg, equipment manufacturers and end users, to ensure models accurately represent real-world operating conditions. Engineers can explore multiple design alternatives and optimize performance before committing to tooling and production.

This partnership approach maximizes the predictive value of simulation analysis and ensures optimal seal performance throughout the equipment lifecycle.

Modern semiconductor manufacturing demands precision and reliability that traditional design approaches cannot guarantee. Simulation-driven engineering provides the predictive capabilities necessary to meet these demanding requirements while reducing development time and costs. As simulation technology continues advancing, its role in sealing optimization will only grow more critical to industry success.

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Why the automotive industry is the perfect use case for AI

When it comes to everyday life, artificial intelligence is already changing the world around us; if the most ambitious predictions are correct, it promises to transform our lives even further. For all the excitement about what it can do, some approach AI with caution, especially when it comes to its integration into the automotive industry.

BY PASCAL LEMASSON, AVP BUSINESS DEVELOPMENT AND SALES - EUROPE AT MEDIATEK

However, the opportunities AI presents for the automotive industry are limitless. It has the capability of not only making driving safer but also completely transforming the driving experience altogether. Whether it's advancements in AI-powered voice control or predictive maintenance, the future points to a driving experience that is seamless, personalised and always connected.

The way we interact with cars is set to change. The future in-cabin experience will involve a car getting to know its drivers, both their habits and preferences, via a hybrid approach of edge and cloud-based AI. This ensures that the drivers will experience the optimum experience without compromising their personal privacy.

Safety comes first

There's no doubt; safety has to be the priority. After all, it is an essential element of fostering consumer trust and acceptance of AI in vehicles. In fact, AI is set to revolutionise how we view safety in the automotive industry, both from a person-centric and car-centric perspective.

But what does this actually mean? Safety features that focus on person-centric elements involve monitoring the behaviours, responses and habits of the individual inside the car. A fantastic example of this is drowsiness detection — AI sensors and cameras inside the vehicle can detect if the driver is falling asleep by detecting differences in facial expression, head position, or tracking

eye movement. If the AI detects that the driver is becoming drowsy, the car will alert them. It will even adjust the temperature of the car, the volume of the radio or recommend that the driver should pull over. There has already been a mandate by the European Union that all cars made after 2024 are installed with driver drowsiness and attention warning (DDAW) systems, so we can expect to see a rising demand in this technology — AI will be crucial in supporting it.

This can be taken a step further; vehicles can use AI to recognise emotion or cognitive patterns. This means that, if someone shows a sign of being stressed, the vehicle could play relaxing music. It will also be able to detect if someone has sustained an injury or is having a medical episode and alert the authorities.

However, this is just one element of safety. AI will also boost safety systems specifically for the vehicle. This encompasses a range of different elements, from predicting maintenance issues before they arise to automatically adjusting your mirrors if someone is shining their full beam into your eyes. Adopting AI into the automotive industry will make driving a safer experience overall, but it also has the potential to completely transform the driving experience as a whole.

A personal assistant on wheels

Voice activation should no longer be viewed as just a safety feature but as a personal assistant, providing drivers access to an AI-powered chatbot.

This could be something as simple as asking an intelligent assistant to move your seat, turn on your wipers, adjust audio or change the navigation settings based on your commands. However, advanced features will allow the AI inside of the vehicle to be more like a concierge. It will be able to provide the user with information about areas you drive through, or if you drive past a nice restaurant, you will be able to ask your vehicle to book a table without disrupting the flow of your journey. It will also revolutionise what we consider to be in-car entertainment — it can provide tutoring sessions for children or tell stories which are tailored to their specific interests.

The integration of innovative AI and multimedia technologies into next-gen autonomous vehicles will redefine how we view automotive travel. We will start to view vehicles as an extension of our home rather than just a mode of transport. Passengers can take advantage of advanced video conferencing features that are supported by AI gaze correction and AI-based audio enhancement, allowing them to stay seamlessly connected with family, friends or even work colleagues whilst on the road. Ray tracing graphics will elevate the monitors even further, creating a high-quality and immersive experience, whether this is calling a friend, watching a film or even gaming.

Bringing edge to the automotive industry

Whether it's inside or outside the vehicle, cameras and sensors will be critical in allowing AI to improve both safety and entertainment features. Despite the benefits of detecting that the driver could be falling asleep or identifying an obstruction in the road, there are likely to be privacy concerns amongst consumers if there are cameras facing inside and outside the vehicle.

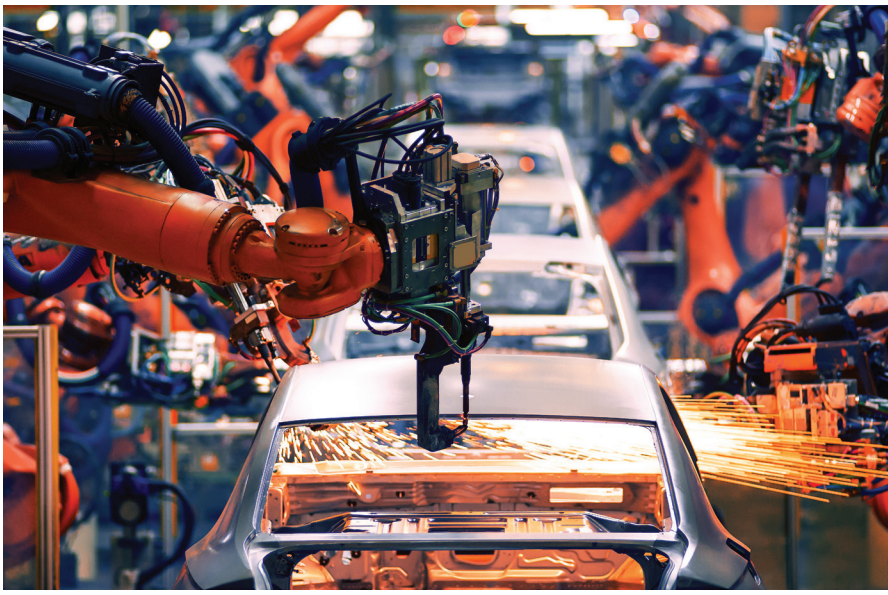
Consumers won't want this information being sent to and from the cloud, as it leaves potentially private information or conversations more vulnerable to being exploited. Fortunately, developments in edge AI mean that this information will remain on-device and never leave the vehicle. This eliminates the need for third parties to store sensitive data remotely and mitigates the danger of malicious actors accessing this information.

However, there are still benefits of cloud-based AI when it comes to fleet management and improving overall safety. AI is capable of predictive maintenance and will be able to report issues back to manufacturers securely. This provides invaluable insights into the overall safety of a make and model of a vehicle. If recurring maintenance issues are highlighted, they can alter the design of future models or, in extreme cases, even recall faulty product lines.

This is just the beginning

With so many capabilities to be realised, much of the predictions around AI and the automotive industry are merely scratching the surface. Consumers can expect to see their transport experience transformed, making journeys safer, personalised and more entertaining.

The everyday car will not just be viewed as a means of transportation but as a digital living room where passengers can continue to be productive, game or connect with friends and family on the move.



Next generation polyimide material for test socket applications

We live in an age seemingly defined by advancement in artificial intelligence technologies. To meet the demands of these cutting-edge developments, microchip architecture is rapidly increasing in complexity. This has implications for all processes involved in the manufacture of integrated circuits as well as in testing them.

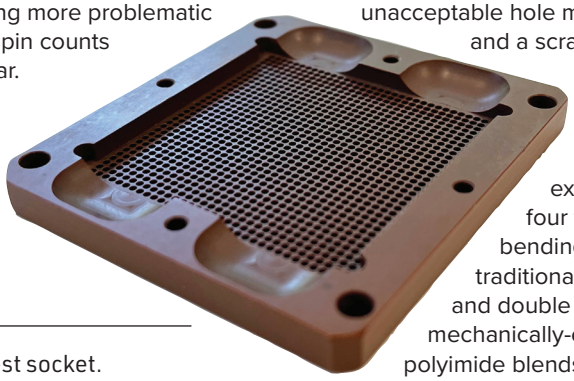
BY DAVE SEILER, SENIOR BUSINESS DEVELOPMENT MANAGER, CURBELL PLASTICS, INC.

THE MORE complex the chip, the more difficult it is to test it. Test sockets with over 10,000 pin holes are already in production and all signs point to counts increasing drastically in the near future. As a result, test socket designers are turning to new plastic composites with performance and machinability characteristics beyond the capabilities of legacy materials.

Machined socket materials have been steadily evolving for decades. Polyimides initially emerged as an enhanced stability alternative to more moisture-sensitive PAI and thermally-sensitive PEEK and PEI polymers. PEEK composite materials with filler packages that reduce their coefficients of thermal expansion are still popular in the finer pitch market due to their lower per pound cost relative to polyimides; however, their higher burr and blow-out rate is becoming more problematic (and costly) as pin counts continue to soar.

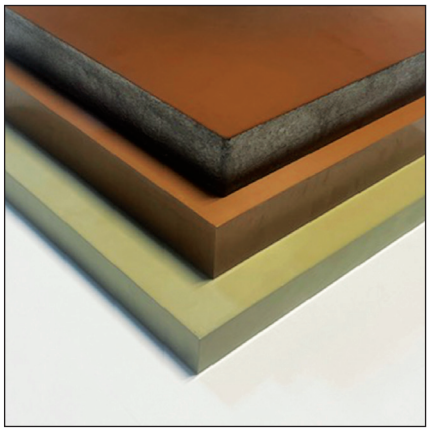
I sympathize with those who personally know the displeasure of machining thousands of ultra-precise holes in a socket plate only to discover during a scope-aided multi-hour manual inspection that something was askew and the socket would be scrapped. In such instances, the machine time and labor costs (and headaches) can greatly outweigh the costs of the raw material.

New polyimide composites have been developed to address the next generation of socket design challenges. As chip sizes grow, preventing flexure near the center of a would-be socket during machining operations becomes more difficult. Traditional unfilled plastic materials tend to be significantly less rigid than reinforced grades, which can lead to undesirable bowing near the center of a large part while holes are being drilled. With new age tolerance and pitch requirements, even a slight deflection may yield an unacceptable hole misalignment and a scrapped part.



➤ Polyimide test socket.

These latest polyimide composites exhibit roughly four times the bending stiffness of traditional polyimides and double that of mechanically-enhanced polyimide blends.



➤ Pictured from top to bottom: Vespel® SP-1, Vespel® SCP-5000, and the new polyimide composite Vespel® SCS-5700.

Meanwhile, they retain comparable strength characteristics to traditional unfilled polyimide socket materials to ensure tool wear is kept to a minimum. In service (and transport), these novel materials offer improved dimensional stability over traditional polyimide materials boasting both lower coefficients of thermal expansion and moisture absorption levels.

A table comparing key properties of three leading grades of polyimide socket materials is included here for reference.

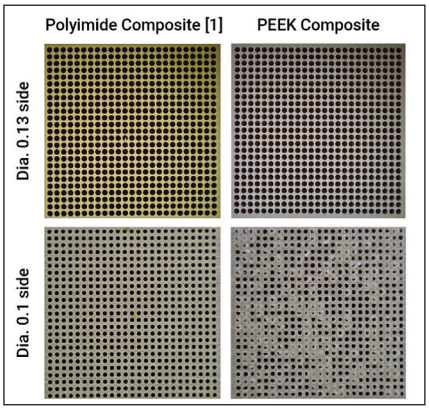
Comparison of Key Properties of Industry-Leading Polyimide Materials				
Material	**Flex Modulus**	**Tensile Strength**	**Coefficient of Thermal Expansion** (x-y direction)	**Moisture Absorption** (@ 24 hours)
Polyimide	449.6 ksi	14,500 psi	2.8 x 10^{-5}/°F	0.24%
High Strength Polyimide	826.7 ksi	25,200 psi	2.1 x 10^{-5}/°F	0.08%
New Polyimide Composite	1,711.4 ksi	16,500 psi	1.0 x 10^{-5}/°F	0.02%

➤ Data extracted from DuPont™ Vespel® Parts: Innovative Solutions for Semiconductor Testing Data correlate with Vespel® SP-1, Vespel® SCP-5000, and Vespel® SCS-5700 [1], respectively.

Property data only gets us so far. Real-world performance is often another matter entirely. Fortunately, these composite polyimides became commercially-available earlier this year and extensive machining studies have been conducted. In one such instance, step holes of 0.1 – 0.13mm were drilled in samples of the new polyimide composite and an industry-standard PEEK composite. The results were quite telling with the PEEK composite sample exhibiting significant quantities of burrs on the 0.1mm diameter hole side and the polyimide composite sample appearing quite clean.

Greater processing power places more responsibility on testing. And new polyimide composites are likely going to be utilized by designers assuming these responsibilities for the next generation of artificial intelligence testing solutions.

Their combination of extreme machinability, dimensional stability, and thermal capabilities will provide socket designers with a polymeric option for the incoming ultra-precise testing requirements that traditional materials simply cannot handle.



➤ Vespel® SCS-5700 composite material compared with a PEEK composite.

As chip sizes grow, preventing flexure near the center of a would-be socket during machining operations becomes more difficult.

How inorganic resists are redefining standards in electron beam lithography

Demands for resolution, process stability, and material performance are continuously increasing. In electron beam lithography, conventional polymer-based resists are reaching their physical limits. New materials based on HSQ are closing this gap and currently shaping key innovations – from mask fabrication to micro-optics.

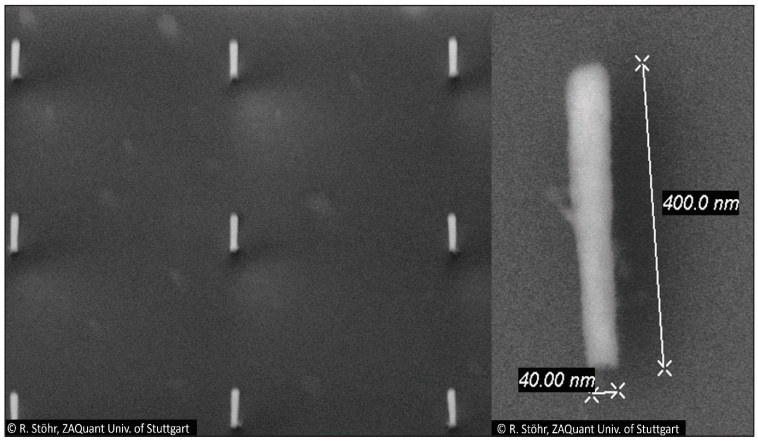
BY PATRICK SCHULZE, JOURNALIST FOR WORDFINDER

ELECTRON BEAM lithography (E-beam lithography) is a key technology for directly patterning the finest geometries. It is used in the fabrication of semiconductor components, diffractive optical elements, and MEMS structures. Unlike mask-based processes, the electron beam writes directly into the resist on the wafer, enabling high flexibility and resolution – but at the cost of slower processing speeds.

"Since the electron beam writes point by point, the resists must be highly sensitive to achieve acceptable process times," explains Harry Biller, customer advisor at Allresist GmbH, a manufacturer of innovative resists for lithographic applications. At the same time, extremely high resolutions are required – down to the sub-10 nm range. Many polymer-based resists reach their limits here due to issues like poor edge roughness and low etch resistance.

Why HSQ?

Hydrogen silsesquioxane (HSQ) is a purely inorganic material composed of silicon, oxygen, and hydrogen. Upon exposure to electron beam irradiation, it forms a compact, silica-like structure with high etch resistance. "A major advantage is that the reaction occurs only where the beam hits," says Biller. "This results in very high contrast and enables sharp edges." Especially in applications requiring narrow ridges rather than conical profiles, HSQ proves superior.



➤ Nanorods spaced 1 µm apart, written on silicon with 2000 µC/cm² at 50 kV and developed using AR 300-44 (2.38% TMAH). (image: Allresist)

In addition to these structural advantages, Allresist's HSQ-based resist, Medusa 84, offers significantly higher plasma resistance than organic resists. This enables deeper and narrower etch profiles at lower layer thicknesses – a crucial benefit for many high-end applications.

Technological progress made visible

One example of HSQ-based resists' performance is mask fabrication for extreme ultraviolet lithography (EUVL). "Here, structure sizes of up to 10 nm are required. Without HSQ, many mask manufacturers could hardly meet these demands," Biller says. The material is also used in the production of diffractive optical elements, MEMS structures, and hardmask processes.

Improved shelf life and process reliability

Another advantage of Medusa 84 is its improved shelf and process stability thanks to the use of butyl acetate instead of MIBK as a solvent. "Using butyl acetate in VLSI quality not only increases shelf life but is also safer than MIBK, which has been classified as potentially carcinogenic in the EU," notes Biller. Internal tests at Allresist show that Medusa 84 can be stored for over a year at -18°C without significant changes in layer thickness. The special purification of the HSQ polymer also plays a key role in long-term performance. "Gelation is significantly slowed when long-chain molecules are removed beforehand," explains Biller. This production process is essential for enhanced durability.

Grayscale lithography and post-treatment

HSQ also offers unique opportunities for shaping

structures: “By adjusting the dose, the structure height can be controlled. This enables the creation of lens-like or sloped structures, which is ideal for meta-optics and VR applications,” says Biller. Post-baking is optional but recommended: it nearly fully converts the structure into silicon oxide, further increasing stability. While process pauses are less critical due to the inorganic nature, they should still be kept short or performed under vacuum. “One to two days of air exposure can negatively affect contrast, but under vacuum or inert gas, pauses are unproblematic,” Biller adds.

HSQ technology resurgence – driven by availability

The planned market withdrawal of DuPont’s FOx16 and XR-1451 products by the end of 2025 raised concerns about a future shortage of high-performance HSQ resists. “Many users previously avoided HSQ due to limited availability and short shelf life. This is exactly where Medusa 84 steps in as a stable, ready-to-use alternative,” explains Biller. A key benefit is compatibility: existing processes do not need to be changed. “Users can maintain their existing processes, doses, and exposure parameters.”

According to Biller, this is particularly beneficial for research institutions with limited resources: “Users, especially those with limited resources, depend on the seamless transferability of existing processes.” Flexible customization and planned enhancements In addition to four standard versions, customer-specific layer thicknesses are also available.

Limitations exist mainly regarding solvents or additives due to unpredictable interactions with HSQ. “In such cases, a research partnership may be necessary. At present, we cannot guarantee that alternative additives are compatible with the HSQ system,” says Biller.

An expansion to include photoactive components is also planned. The goal is to make HSQ resists suitable for high-throughput UV lithography, thus greatly expanding the potential user base and enhancing the appeal of HSQ’s resolution-speed combination.

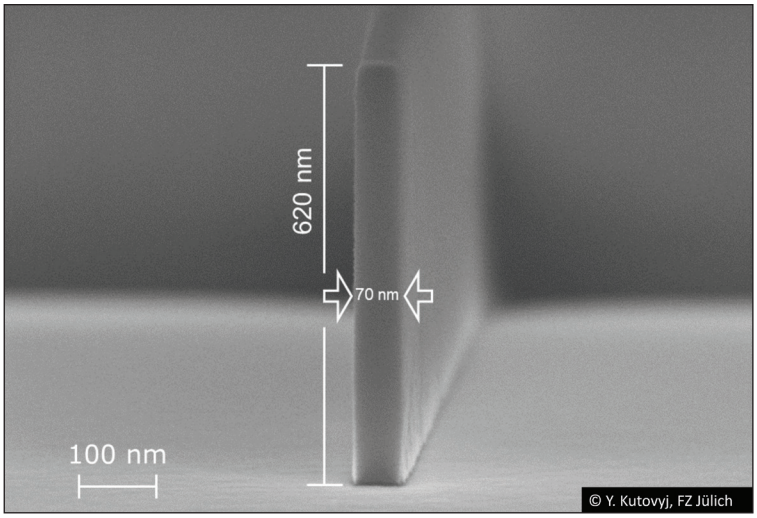
Support, datasheets, and practical expertise

To ensure the full innovation potential of HSQ-based resists like Medusa 84, Allresist offers users individual support in addition to safety and technical datasheets. “We support Medusa 84 users via video calls and provide access to a large application scenario database,” Biller explains. Extensive image documentation, such as electron microscopy images, is also available and can be used for quality control and process optimization.

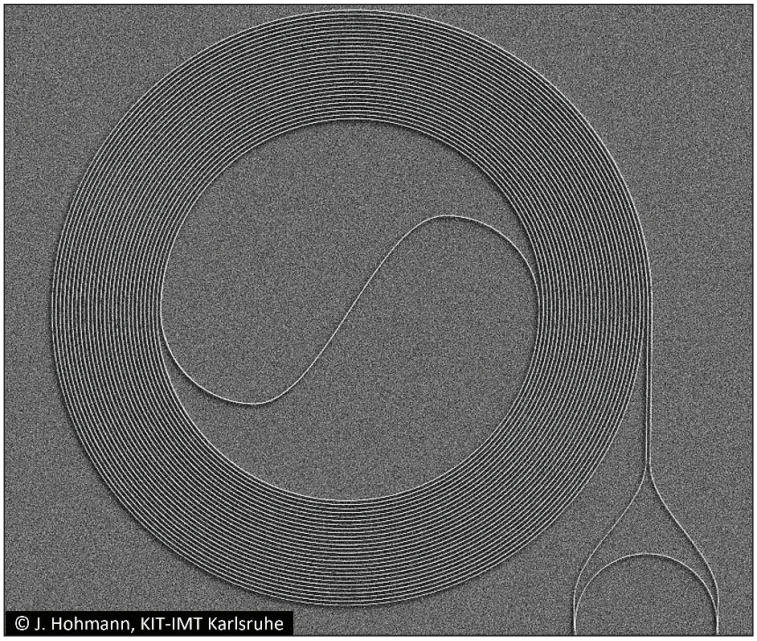
Conclusion

With the HSQ resist Medusa 84 from Allresist, electron beam lithography gains access to a powerful material that surpasses conventional organic polymers in many ways. Especially in terms of resolution, etch resistance, structural control, and shelf life, this modern HSQ formulation sets new standards. Thanks to its easy integration into existing processes and flexible configuration options, it presents a future-proof solution for research, development, and industrial use.

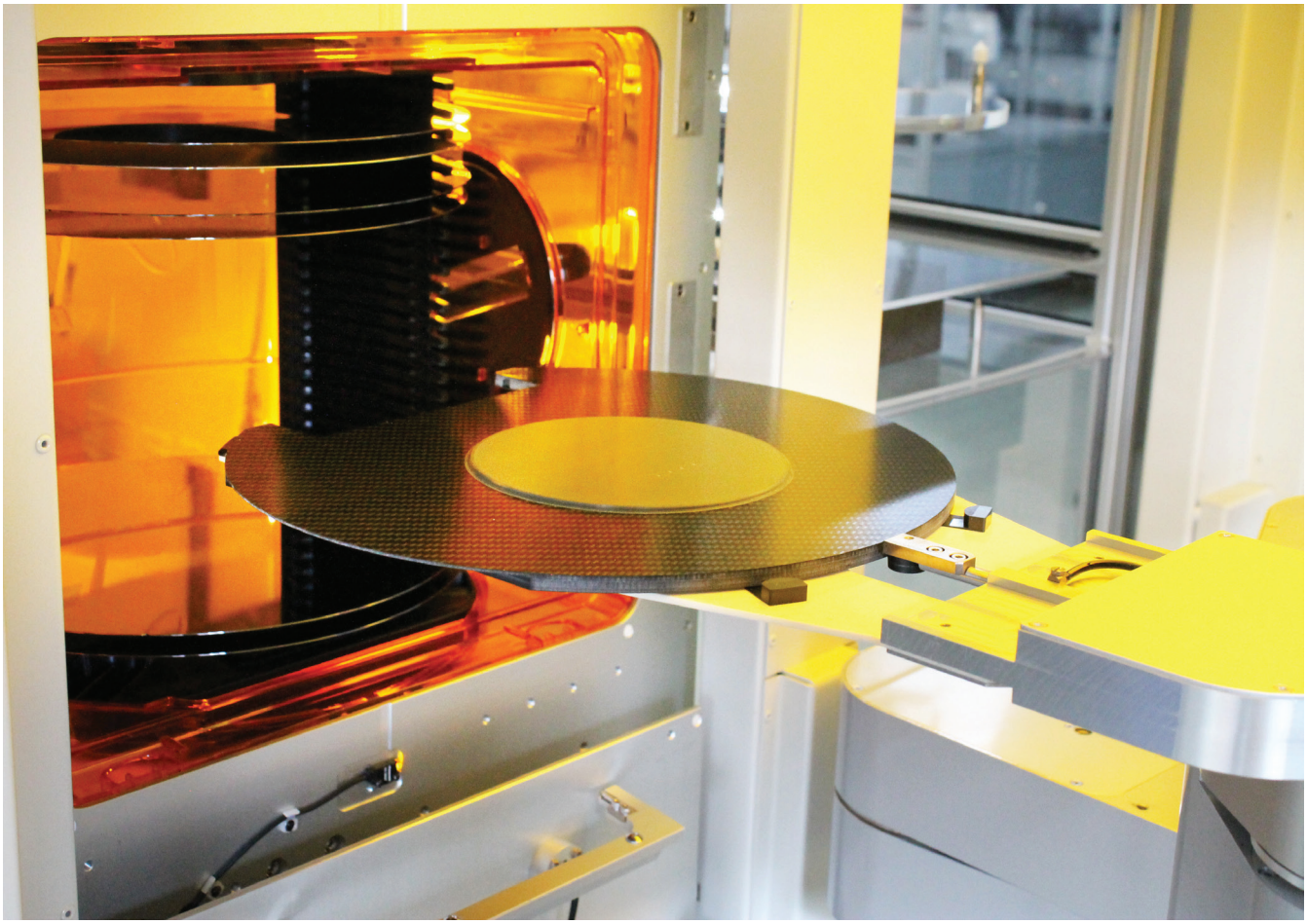
Ongoing efforts to enable UV sensitization may further broaden the adoption of HSQ resists among new user groups seeking these advantages.



➤ “Shadow wall” structures for quantum computer fabrication. Written at 100 kV, 200 pA beam current, dose: 600 µC/cm². Developer: AR 300-73 (6.5% TMAH). (image: Allresist)



➤ Circular 100-nm line/space structures, written on silicon with 100 kV and developed using AR 300-73 (6.5% TMAH solution). (image: Allresist)



AES motomation: Advancing Semiconductor Automation Worldwide

AES MOTOMATION has established a strong reputation in automated material handling solutions for the semiconductor industry by leveraging strategic partnerships, global expertise, and versatile portfolio of robotic and handling technologies.

Through close collaboration with JEL Corporation, Nidec Instruments Corporation, and Sinfonia Technology, AES motomation delivers integrated, high-precision systems such as iFEMs and modular EFEMs that optimize performance, reduce footprints, and enhanced cleanroom efficiency. With a commitment to innovation, flexible auto-teaching solutions, and comprehensive support across the entire product development cycle, AES motomation continues to provide scalable reliable and cost-effective automation solutions tailored to the evolving needs of clean and sterile manufacturing environments worldwide.

Founded in 1998, AES motomation provides specialized automated material handling solutions, primarily serving the semiconductor industry. With corporate roots in Germany and operations in North America (Fremont, California) as well as Asia (Taichung, Taiwan), AES motomation maintains a global presence to support their customers in the ever-growing global Semiconductor market.

Through key partnerships with JEL Corporation, Nidec Instruments Corporation and Sinfonia Technology, AES motomation offers a broad and customizable portfolio of modules and tools including load ports, robots, pre-aligners and full-handling platforms that ranges from 100 mm to 300 mm and coupling with extensive application engineering services ranging from feasibility studies and cycle testing to integration planning.

The synergy between JEL Corporation, Nidec Instruments Corporation, Sinfonia Technology, and AES motomation enables

their partnership to deliver comprehensive front and back-end solutions to their customers.

JEL Corporation provides robotic handlers designed for technologies such as MEMS and LED, supporting wafer sizes from 50 mm and up as well as advanced vacuum robot systems. Their robots are also engineered to operate reliably in wet environment.

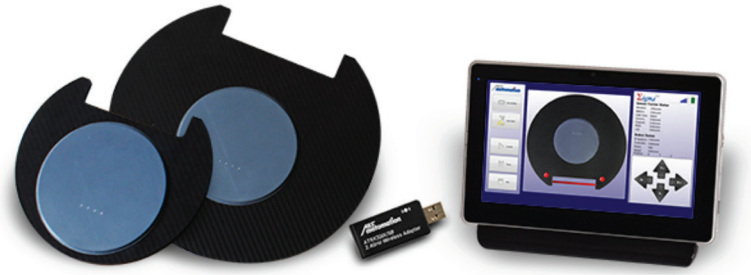
Meanwhile, Nidec Instruments Corporation offers handling robots for 300 mm wafers and FPD applications, capable of managing substrates as large as Generation 11. Sinfonia Technology, one of the leaders if not the leading supplier of FOUP opener provides a comprehensive portfolio of load ports ranging from 100 mm to 300 mm wafers, tape frames, flat panels as well as complete EFEMs for N2 environment and vacuum linear transportation units. Their EFEMs and platforms incorporate advanced technologies from all of our partners. They have already carried out the critical, but time-consuming work of evaluation, integration, testing, and data gathering. The result is a portfolio of solutions built on more than 100 years of combined semiconductor experience.

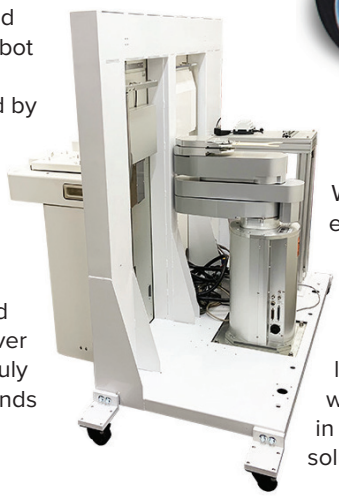
One example is their integrated Front-End Module (iFEM), a complete front-end handling solution that combines Sinfonia Technology's load ports with robotics from Nidec or JEL, all controlled by AES motomation's software. In terms of performance, the iFEM delivers the functionality of the EFEM, but with a smaller footprint. By utilizing the tool's existing FFU, façade, and interlocks, the iFEM offers a more cost-competitive alternative to a full EFEM.

AES motomation offers versatile auto teaching solutions compatible with any robot system handling round or square substrates, including wafers, reticles, LCDs, or solar panels. The system uses a substrate-shaped sensor carrier with wireless connectivity, enabling complete automatic re-teaching at any time. Standard sensor carriers are available for 200 mm and 300 mm wafers and can be interchanged between different tools using cassettes (FOUPs). They are wirelessly charged, either automatically inside the tool or manually outside, and can be controlled via the robot controller, tool controller, or handheld unit, all supported by an intuitive graphical user interface.

AES motomation's strength lies in its ability to combine global expertise, advanced technologies, and trusted partnerships to deliver automation solutions that truly adapt to the evolving demands of the semiconductor and laboratory industries.

The synergy between JEL Corporation, Nidec Instruments Corporation, Sinfonia Technology, and AES motomation enables their partnership to deliver comprehensive front and back-end solutions to their customers





With proven experience across clean and sterile environments, a broad portfolio of customizable tools, and a commitment to supporting customers from concept through full0scale production, we continue to drive efficiency, scalability, and innovation worldwide. As we look toward the future, we invite you to join us, whether as a partner, collaborator, or customer, in shaping the next generation of automation solutions together.

From wafer processing to packaged chip. Next Gen X-Ray opens up new possibilities for semiconductor inspection

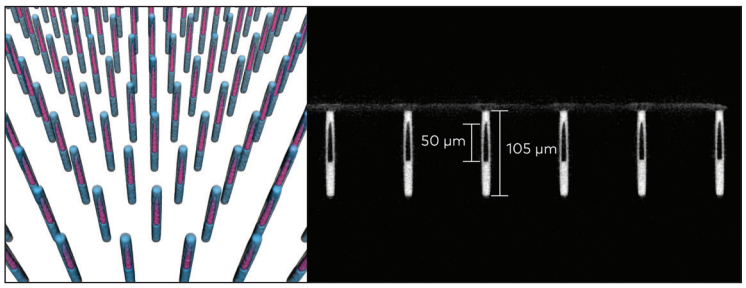
In the post-moore era, advanced packaging continues to play a critical role in meeting the ever-increasing demands of electronics production for more powerful performance in smaller and cheaper packages. As semiconductor manufacturers race to invest in this pivotal technology, they find themselves under pressure to deliver in a competitive landscape where even marginal yield improvements can have significant impact on profitability and time-to-market.

THE FAILURE of a single chip within the stack can affect the entire package, causing costly production-line adaptations and delays. Staying ahead of the curve requires the adoption of comprehensive inspection strategies to identify potential defects in these ever-more complex structures quickly and reliably. Thanks to innovative developments into both hardware and the supporting software, Comet's 3D and 2D X-ray inspection solutions are well placed to accelerate semiconductor quality inspection throughout crucial production phases in both the lab and the fab – now for the first time including processed wafers.

2D & 3D X-ray in the Lab environment

Before entering commercial production, 3D X-ray technology can provide a significant benefit for semiconductor manufacturers looking for deeper insight into their prototype designs, helping identify areas of potential defects faster and earlier. Systems such as our FF35 CT and CA20 can capture precise details in nano-level resolution, from coupons, dies, or even complete wafers and packaged chips. Thanks to significant breakthroughs in image capture and reconstruction, high-resolution 3D volumes can be captured in minutes, enabling manufacturers to measure and view TSVs or bumps from all angles, and extract 2D slices from anywhere within the volume. Critical attributes are captured in crystal-clear resolution presenting a full 360° view of buried features (vias, interconnects, solder bumps, microbumps, die-attach layers, TSVs, etc.), while preserving valuable early-stage prototypes for repeated analysis.

ADR software packages like CoS Insights X 3D make defect detection and analysis even faster and more intuitive. Powered by Dragonfly's AI capabilities, these tools enable automatic recognition of critical defects for bumps such as voids, head-in-pillow, bridges and for TSVs such as voids, cracks and fill-level. Alongside clear visual indicators, these software packages capture critical metrological data for further analysis.



➤ Reconstructed 3D image of a wafer sample showcasing the TSVs and visible voids, captured by the Comet FF35 CT and visualized in Dragonfly 3D World. Image right: 2D slice detail view taken from the 3D volume. Wafer designed for Comet by Fraunhofer IZM_ASSID, it contains voids for illustrative purposes. All image property rights remain with Comet.

Bringing X-ray technology to the production line

In 2024, the launch of the next-generation CA20 brought this progressive technology out of the research lab environment and directly on to the production line. Featuring an automatic EFEM loader and enhanced ADR software powered by Dragonfly, the next-generation CA20 offers seamless integration (compliant to SECS/GEM standards) and next-level automated insights for smooth process optimization. This year, the CA20 line has expanded further, with crucial design adaptions and new software options broadening the range of applications to cover wafer inspection. The CA20 is now able to comply with strict cleanroom standards of up to ISO Class 3 (within the interior cabinet

directly above the sample) and handle delicate wafers with precision. With this latest release, Comet's portfolio has grown to cover all crucial inspection phases across the manufacturing chain.

Example Workflow: TSV Insights X 2.5D

Expanding the application scope of the CA20 system to handle wafer inspection has only been made possible through significant advancements within Comet's AI-powered software, DirectInspect, and the introduction of TSV Insights X 2.5D. A single wafer can contain thousands or even millions of TSVs, tightly packed together and nearly identical in size and shape. Segmenting the individual elements and determining their position on the wafer reliably and consistently has, until now, presented a significant challenge for most inspection software.

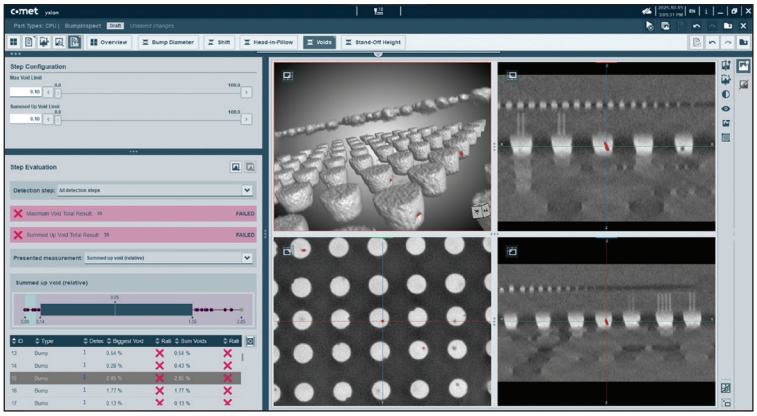
While 3D X-ray offers a full 360° view, perfect for the inspection of overlapping structures, for simpler TSV structures a 2D method can be sufficient, especially when captured across several positions at a specific angle that retains adequate depth information. This helps to determine positioning, requires less contrast to visualize any voids, and significantly reduces scan time while still presenting a statistically relevant picture of the entire wafer.

Through this approach, TSV Insights X 2.5D is able to automatically segment individual TSVs within captured X-ray images, extracting critical metrological data, detecting voids and categorizing this information based on predefined thresholds – all in a machine-readable format for swift process enhancement. Users have the option to utilize a pre-trained neural network for automatic TSV and void segmentation. In cases requiring customization, the model can be fine-tuned to match specific wafer designs for optimal accuracy. Whether employing a generic or tailored model, the analysis process is rapid and suitable for inline production use.

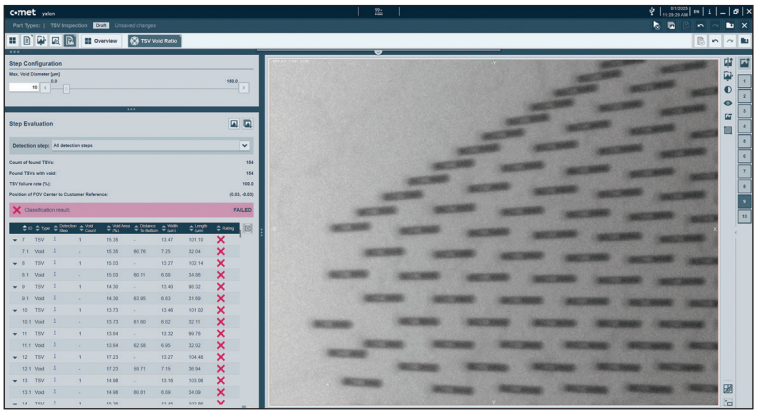
During inspection, the wafer is scanned at multiple key positions, with segmentation of TSVs and voids conducted on the acquired images. The software automatically collects various measurements for both the segmented TSVs and voids within, including length, width, and quantity. Subsequently, failure rates are calculated based on these measurements and specified thresholds. A structured and detailed report is generated and seamlessly shared with the host system before the next wafer is automatically inspected.

Key Takeaways

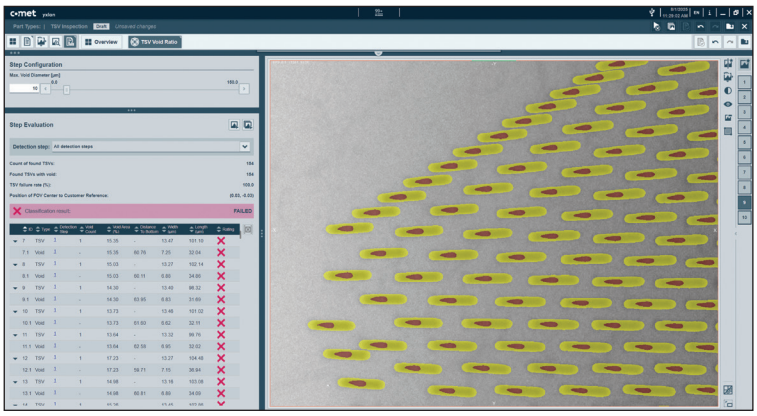
As chips become more complex and semiconductor manufacturers continue to chase even marginal improvements to their yield, a varied and robust quality inspection strategy is a crucial advantage in a highly competitive sector. Steady advancements in 3D and 2D X-ray have unlocked this technology for applications across critical steps in the manufacturing chain, from wafer processing to finished package. The latest systems, such as the CA20 are fully compliant with modern industry standards for cleanrooms and production-line integration, ensuring seamless set-up, while AI-powered software brings incredible visual quality and automatic recognition and classification of most critical defects.



➤ A screenshot taken from Comet's CoS insights X 3D package. The image showcases scans taken from a commercially available GPU, with voids clearly visible within the bumps. All image property rights remain with Comet.



➤ Screenshot taken from our TSV Insights X software showcasing the 2.5D scan before segmentation has been performed. Wafer designed for Comet by Fraunhofer IZM_ASSID, it contains voids for illustrative purposes. All image property rights remain with Comet.



➤ Screenshot taken from our TSV Insights X software after segmentation, with TSVs (yellow) and voids (red). Wafer designed for Comet by Fraunhofer IZM_ASSID, it contains voids for illustrative purposes. All image property rights remain with Comet.

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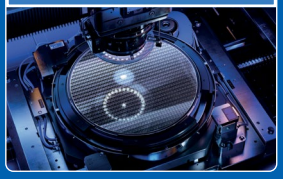

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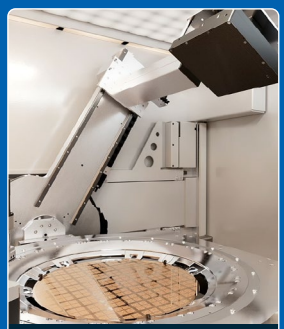

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