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INSIDE

News Review, Features
News Analysis, Profiles
Research Review
and much more...

Playing politics: the semiconductor supply chain

How should nations be looking to use their semiconductor assets in a market dependant on cooperation?

Hybrid optimises semiconductor development

Human-machine collaboration for improving semiconductor process development in the semiconductor chip processes

Current scenario of the semiconductor wafer industry

Demand for electronic devices in consumer and industrial settings has led to substantial growth in the wafer industry

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VIEWPOINT

By Phil Alsop, Editor

1984 on the horizon?

George Orwell's famous novel was published in 1949, not too many years before the semiconductor industry as we now know it began to take shape. One of the book's main features is the existence of three super-states: Oceania, Eurasia and Eastasia – constantly at war with one another, and constantly shifting their allegiances with one another. I mention this in passing as our main news story describes the latest in the 'Chip Wars' saga, whereby the European Commission has approved 8.1 billion euros of public support for microelectronics and communications technologies development within the EU region. A relatively small sum by semiconductor industry standards. Nevertheless, just one more reminder that the US, Europe and (a not so united) Asia are currently engaged in all manner of geopolitics when it comes to developing the foundational technologies that already underpin so much of the digital age, and will likely lead to its rapid acceleration (AI 'restrictions' withstanding) in the near future.

The semiconductor race is, at one level, completely logical and sensible. The pandemic-induced realisation as to the fragility of global supply chains was closely followed by the shattering of any illusions we might have had that, by and large, peace and prosperity for the developed world at least, was here to stay. And, if it was possible to fall out quickly and seriously with previously close trading allies and partners, then it was time to ensure that self-sufficiency for life's essentials became a major focus. Energy, food and semiconductors top this list. Countries and regions all over the world have adjusted many of their objectives around these three 'essentials'.

And yet, prior to this recent political volatility, there had been a long period of relatively trade stability and cooperation, whereby it was perfectly 'reasonable' to outsource even critical supply chains, products and services.

All of which brings me to a perhaps not very helpful main point! At one level, the present intense activity to onshore and thus ensure as near as possible national self-sufficiency makes complete sense, whether we're talking energy, food or semiconductors and digital technologies more generally.

At another level, given the lessons of history, this frenetic reaction to some 'mild' political turbulence, is something of an over-reaction. And, if the war in Europe is resolved quickly, and relations between China and the other global supra-trading blocks thaw, then future historians might well wonder what was all the fuss about back in the 2020s!

Especially as collaboration has become another major focus, alongside the ideas of energy and food security, and semiconductor autonomy. Yes, more and more organisations and businesses, countries and even global regions, have realised that collaboration and cooperation is the only way forward to achieve so much of what is required – not least on the road to Net Zero.

In summary, while we all seem to recognise the need to work together, for now at least, we want to be very selective as to the partners we choose to trust. Only time will tell whether this 'sheltered' approach is the right one.

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EU approves IPCEI ME/CT backing

European Commission approves up to €8.1 billion of public support by fourteen Member States for an Important Project of Common European Interest in microelectronics and communication technologies.

THE COMMISSION has approved, under EU State aid rules, an Important Project of Common European Interest ('IPCEI') to support research, innovation and the first industrial deployment of microelectronics and communication technologies across the value chain.

The project, called "IPCEI ME/CT", was jointly prepared and notified by fourteen Member States: Austria, Czechia, Finland, France, Germany, Greece, Ireland, Italy, Malta, the Netherlands, Poland, Romania, Slovakia and Spain.

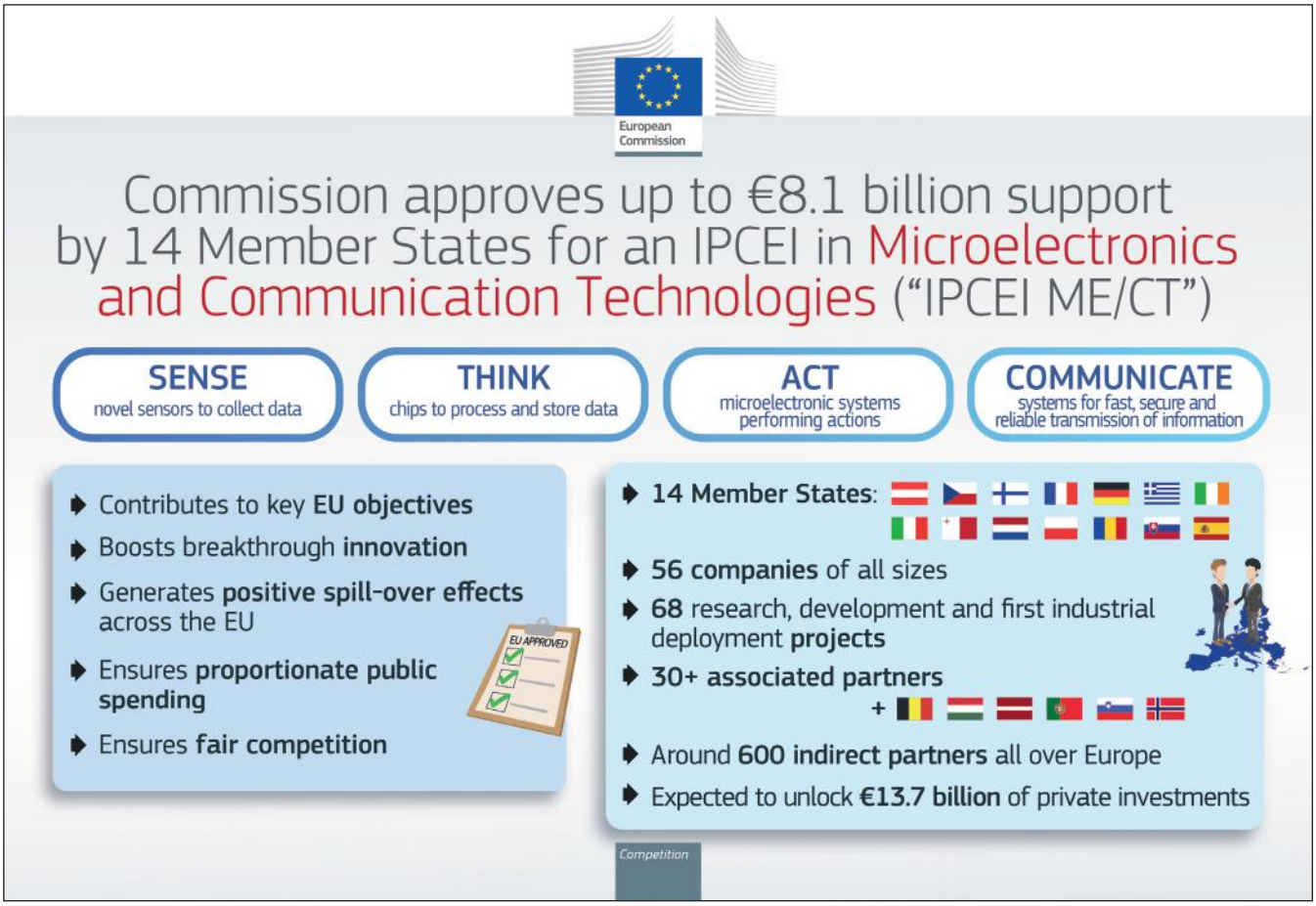
The Member States will provide up to €8.1 billion in public funding, which is expected to unlock additional €13.7 billion in private investments. As part of this IPCEI, 56 companies, including small and medium-sized enterprises ('SMEs') and start-ups, will undertake 68 projects.

IPCEI ME/CT

The IPCEI ME/CT concerns research and development projects covering microelectronics and communication technologies across the whole value chain from materials and tools to the chip designs and manufacturing processes.

These projects aim at enabling the digital and green transformation by: (i) creating innovative microelectronics and communication solutions, and (ii) developing energy-efficient and resource-saving electronics systems and manufacturing methods. They will contribute to the technological advancement of many sectors, including communications (5G and 6G), autonomous driving, artificial intelligence and quantum computing. They will also support companies active in the energy generation, distribution and use in their green transition.

First novel products may be introduced to the market as early as 2025 and the completion of the overall project is planned for 2032, with timelines varying in function of the project and the companies involved. Around 8.700 direct jobs are expected to



be created, and many more indirect ones. IPCEI ME/CT follows and complements the first IPCEI to support research and innovation in the field of microelectronics, approved by the Commission in December 2018.

The Commission assessment

The Commission assessed the proposed IPCEI under EU State aid rules, more specifically its 2021 Communication on Important Projects of Common European Interest ('IPCEI Communication').

Where private initiatives supporting breakthrough innovation fail to materialise because of the significant risks such projects entail, the IPCEI rules enable Member States to jointly fill the gap to overcome these important market failures. At the same time, the IPCEI rules ensure that the EU economy at large benefits from the supported investments and limit potential distortions to competition.

The Commission has found that the IPCEI ME/CT fulfils the required conditions set out in its Communication and is in line with State aid rules. In particular, the Commission concluded that:

- The IPCEI ME/CT directly contributes to achieving several EU objectives of a greener, digital, more secure, resilient and sovereign economy set out in key EU policy initiatives, such as the Europe's Digital Decade and the European Green Deal.
- All 68 projects part of the IPCEI are highly ambitious, as they aim at developing technologies that go beyond what the market currently offers and will allow major improvements, notably in the areas of sensors, high performance processors, microprocessors including artificial intelligence, actuators and communication means for secure data exchange.
- The IPCEI also involves significant technological and financial risks. Therefore, public support is necessary to provide incentives to companies to carry out the investment.
- Aid to individual companies is limited to what is necessary, proportionate and does not unduly distort competition. In particular, the Commission has verified that the total planned maximum aid amounts are in line with the eligible costs of the projects and their funding gaps. Furthermore, if large projects covered by the IPCEI turn out to be very successful, generating extra net revenues, the companies will return part of the aid received to the respective Member State (claw-back mechanism).
- The results of the project will be widely shared by participating companies benefitting from the public support with the European scientific community and industry beyond the companies and countries that are part of the IPCEI, including through conferences, publications, access to pilot and production facilities or licensing of intellectual property rights. As a result, positive spill-over effects will be generated throughout Europe.

Funding, participants and structure of the IPCEI

The IPCEI involves 68 projects from 56 companies. These direct participants will closely cooperate through more than 180 envisaged cross-border collaborations.

The figure below presents the overall structure of IPCEI ME/CT, including the individual workstreams:

The 68 projects are part of the wider IPCEI ME/CT ecosystem involving over 30 associated participants, including universities, research organisations and companies located in five additional EU Member States (Belgium, Hungary, Latvia, Portugal, and Slovenia) and Norway. Public support to projects handled by research organisation do not require the Commission's approval, as it does not qualify as aid.

The companies, which seek limited aid amounts, can obtain the public support under General Block Exemption Regulation, which therefore does not need to be notified to the Commission for approval. Their innovative projects are not considered part of the IPCEI as such. The figure below presents the IPCEI ecosystem showing the direct participants and the associated participants:

In addition, there are around 600 indirect partners which are companies or organisations that hold collaboration agreements with one or more direct participants of IPCEI ME/CT and that can therefore benefit from the various dissemination activities.

Several Member States (Austria, Czechia, Finland, France, Germany, Italy, Latvia, Romania, Slovakia and Spain) included their participation in the IPCEI ME/CT in their Recovery and Resilience Plans. These Member States have the possibility to partly fund their projects through the Recovery and Resilience Facility.

More information on the amount of aid to individual participants will be available in the public version of the Commission's decision, once confidentiality issues have been resolved with Member States and third parties.

Margrethe Vestager, Executive Vice-President in charge of competition policy, commented: "Microelectronics and communication technologies are the backbone of any modern electronic device from mobile phones to medical equipment."

"This Important Project of Common European interest is the largest approved so far and the second on microelectronics. Innovation is essential to help Europe economy become greener and more resilient. But innovation can come with risks that the market alone is not ready to take. This is why State aid should be made available to fill such a gap."

Thierry Breton, Commissioner for Internal Market, added: "This latest IPCEI approved today is yet another demonstration of the EU Chips Act already triggering considerable public and private investment across the European semiconductor value chain: from materials to design, from equipment to advanced packaging."

"By investing in our innovative companies, we are investing in Europe's technological and industrial leadership in semiconductors, as well as our security of supply and economic security."

Forging a dream material with semiconductor quantum dots

Researchers from the RIKEN Center for Emergent Matter Science and collaborators have succeeded in creating a "superlattice" of semiconductor quantum dots that can behave like a metal, potentially imparting exciting new properties to this popular class of materials.

SEMICONDUCTING colloidal quantum dots have garnered tremendous research interest due to their special optical properties, which arise from the quantum confinement effect. They are used in solar cells, where they can improve the efficiency of energy conversion, biological imaging, where they can be used as fluorescent probes, electronic displays, and even quantum computing, where their ability to trap and manipulate individual electrons can be exploited.

However, getting semiconductor quantum dots to efficiently conduct electricity has been a major challenge, impeding their full use. This is primarily due to their lack of orientational order in assemblies. According to Satria Zulkarnaen Bisri, lead researcher on the project, who carried out the research at RIKEN and is now at the Tokyo University of Agriculture and Technology, "making them metallic would enable, for example, quantum dot displays that are brighter yet use less energy than current devices."

Now, the group has published a study in Nature Communications that could make a major contribution to reaching that goal. The group, led by Bisri and Yoshihiro Iwasa of RIKEN CEMS, has created a superlattice of lead sulfide semiconducting colloidal quantum dots that displays the electrical conducting properties of a metal.

The key to achieving this was to get the individual quantum dots in the lattice to attach to one another directly, "epitaxially," without ligands, and to do this with their facets oriented in a precise way. The researchers tested the conductivity of the material they created, and as they increased the

carrier density using a electric-double-layer transistor, they found that at a certain point it became one million times more conductive than what is currently available from quantum dot displays. Importantly, the quantum confinement of the individual quantum dots was still maintained, meaning that they don't lose their functionality despite the high conductivity.

"Semiconductor quantum dots have always shown promise for their optical properties, but their electronic mobility has been a challenge," says Iwasa. "Our research has demonstrated that precise orientation control of the quantum dots in the assembly can lead to high electronic mobility and metallic behavior. This breakthrough could open up new avenues for using semiconductor quantum dots in emerging technologies."

According to Bisri, "We plan to carry out further studies with this class of materials, and believe it could lead to vast improvements in the capabilities of quantum dot superlattices. In addition to improving current devices, it could lead to new applications such as true all-QD direct electroluminescence devices, electrically driven lasers, thermoelectric devices, and highly sensitive detectors and sensors, which previously were beyond the scope of quantum dot materials."

News in Brief

MICRON TECHNOLOGY, INC. has launched the U.S.-Japan University Partnership for Workforce Advancement and Research & Development in Semiconductors (UPWARDS) for the Future. Aimed at cultivating a more robust and highly-skilled semiconductor workforce for the two countries, the partnership will drive emerging research while increasing the pipeline of students studying a semiconductor curriculum.

SIGMASENSE has licensed technology to NXP, and the companies will collaborate on high-performance sensing products for specific applications with demands for faster, more robust, fully immersive software-defined experiences.

MICRON TECHNOLOGY will be introducing extreme ultraviolet (EUV) technology to Japan, tapping this sophisticated patterning technology to manufacture its next generation of DRAM, the 1-gamma (1γ) node. Micron will be the first semiconductor company to bring EUV technology to Japan for production, with its Hiroshima fab playing a critical role in the company's development of the 1-gamma node. Micron expects to invest up to 500 billion yen in 1-gamma process technology over the next few years, with close support from the Japanese government, to enable the next wave of end-to-end technology innovation such as rapidly emerging generative artificial intelligence (AI) applications.

ANALOG DEVICES has announced a new €630 million investment at its European regional headquarters in the Raheen Business Park in Limerick, Ireland. The investment enables the construction of a new, state-of-the-art, 45,000 sq-ft Research & Development and manufacturing facility.

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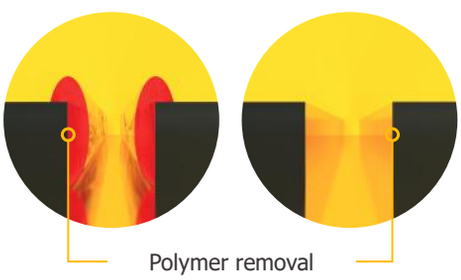

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Intel implements backside power delivery in silicon

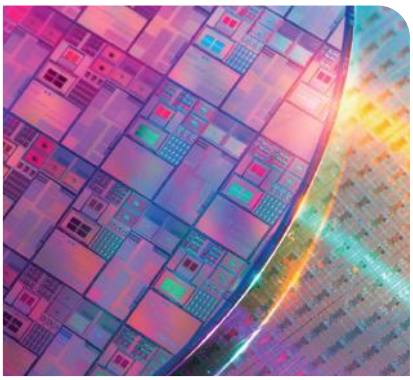
Product-like test chip shows PowerVia's ability to deliver over 90% cell utilization, solve growing interconnect bottlenecks and bring competitive advantages to customers – including foundry.

INTEL says that it is the first in the industry to implement backside power delivery on a product-like test chip, achieving the performance needed to propel the world into the next era of computing. PowerVia, which will be introduced on the Intel 20A process node in the first half of 2024, is Intel's industry-leading backside power delivery solution. It solves the growing issue of interconnect bottlenecks in area scaling by moving power routing to the backside of a wafer.

Ben Sell, Intel Vice President of Technology Development comments: "PowerVia is a major milestone in our aggressive 'five nodes in four years' strategy and on our path to achieving a trillion transistors in a package in 2030. Using a trial process node and subsequent test chip enabled us to de-risk backside power for our leading process nodes, placing Intel a node ahead of competitors in bringing backside power delivery to market."

Intel decoupled development of PowerVia from transistor development to ensure its readiness for silicon implementation based on Intel 20A and Intel 18A process nodes. PowerVia was tested on its own internal test node to debug and ensure good functionality of the technology before its integration with RibbonFET in Intel 20A. After fabrication and testing on a silicon test chip, PowerVia was confirmed to bring a remarkably efficient use of chip resources with greater than 90% cell utilization and major transistor scaling, enabling chip designers to achieve performance and efficiency gains in their products.

Intel believes that PowerVia is well ahead of competitors' backside power solutions, giving chip designers – including Intel Foundry Services (IFS) customers – a faster path to valuable



energy and performance gains in their products. Intel has a long track record of introducing the industry's most critical new technologies, such as strained silicon, Hi-K metal gate and FinFET, to propel Moore's Law forward. With PowerVia and RibbonFET gate-all-around technology coming in 2024, Intel continues to lead the industry in chip design and process innovations. Intel says that PowerVia is the first to solve the growing interconnect bottleneck issue for chip designers. Surging use cases, including artificial intelligence and graphics, require smaller, denser and more powerful transistors to meet ever-growing computing demands. Today and for the past many decades, power and signal lines within a transistor's architecture have competed for the same resources. By separating the two, chips can increase performance and energy-efficiency, and deliver better results for customers. Backside power delivery is vital to transistor scaling, enabling chip designers to increase transistor density without sacrificing resources to deliver more power and performance than ever.

Intel 20A and Intel 18A will introduce both PowerVia backside power technology and RibbonFET gate-all-around technology. As a completely new way of delivering power to the transistors, backside power implementation raised new challenges for thermals and debugging designs. By decoupling development of PowerVia from RibbonFET, Intel could work through those challenges quickly to ensure readiness for implementation in silicon based on Intel's 20A and 18A process nodes. Intel engineers developed mitigation techniques to prevent the thermals from becoming an issue. The debug community also developed new techniques to ensure the new design structure could be appropriately de-bugged.

As a result, the test implementation delivered solid yield and reliability metrics while demonstrating the intrinsic value proposition of the technology well before it joins new RibbonFET architecture.

The test also leveraged design rules enabled by EUV (extreme ultraviolet) lithography, which produced results including standard cell utilization of more than 90% over large areas of the die, enabling greater cell density which can be expected to lower costs. The test also showed more than 30% platform voltage droop improvement and 6% frequency benefit. Intel also achieved thermal characteristics in the PowerVia test chip in line with higher power densities expected from logic scaling.

In a third paper to be presented during VLSI, Intel technologist Mauro Kobrinsky will explain the research into more advanced methods to deploy PowerVia such as enabling both signaling and power delivery on either the front or the back side of the wafer. Bringing PowerVia to customers ahead of the industry and continuing to innovate into the future is in keeping with Intel's long history of being first to bring new semiconductor innovations to market while constantly innovating.

Evonetix delivers first chip-synthesized DNA to the University of Cambridge

First delivery and use of DNA manufactured using Evonetix's unique thermally controlled synthesis technology.

EVONETIX LTD, the company bringing semiconductor technology to DNA synthesis, says that DNA synthesized using its unique semiconductor chip technology was delivered to the Department of Chemical Engineering and Biotechnology at the University of Cambridge. This milestone marks the start of the next stage of development of the Company as it expands the range and scale of DNA synthesized on its desktop platform.

The DNA was delivered to Dr Jenny Molloy, Co-chair of the Engineering Biology Interdisciplinary Research Centre at the University of Cambridge. The successful testing of the DNA in Dr Molloy's laboratory further validates Evonetix's patented thermally controlled semiconductor technology and supports the further development of the Company's desktop DNA synthesis platform, which is being developed to enable scientists to synthesize long DNA in their own lab, enabling the biology revolution.

Dr Jenny Molloy, Department of Chemical Engineering and Biotechnology at the University of Cambridge, said: "I'm delighted to have received the first DNA synthesized on Evonetix's semiconductor chips.

Rapid access to custom-designed DNA is a key challenge for us and Evonetix's technology is an exciting new approach to meet the growing demand from researchers. Having the capability to quickly synthesize accurate, gene-length DNA in our own lab will revolutionize our ability to experiment and accelerate results across engineering biology."

Colin McCracken, Chief Executive Officer at Evonetix, commented: "We are proud to be collaborating with scientists at the University of Cambridge as part of our early access programme, delivering our high-fidelity DNA for use in research activities. Synthesizing the first user-ready DNA using our desktop platform is a huge accomplishment and a big step towards the development of our platform. Following our recent fundraise, this achievement continues our work towards full commercialization of our technology."

Democratising access to silicon technology

Advantest Corporation, together with other members of the Research Association for Advanced Systems (RaaS), including the Graduate School of Engineering at the University of Tokyo, Toppan Inc., Hitachi Ltd., Mirise Technologies Corporation, and Japan's RIKEN scientific research institute, has begun research and development on new, advanced system technology that aims to democratize of access to silicon technology by enabling anyone to quickly design a dedicated chip and manufacture it with leading-edge semiconductor technology.

THE KEY to the digital transformation, which promises to revolutionize every aspect of our lives through information processing technology, is the utilization of data that seamlessly connects physical and virtual spaces. Data-driven societies require support systems that collect data sensed by IoT devices via 5G communications, apply advanced analysis using AI, and provide the results to users in the form of a service.

Since digital technology and the products and services that utilize them develops and spreads through platforms--business models that gain market advantages by gathering users into a single place, and share technology across multiple products or product groups—not only cost performance but time performance is an important feature.

Platform-based products and services need to provide high performance at low cost, and they need to provide it quickly. High performance can be obtained by manufacturing dedicated chips using advanced processes, but developing these types of devices takes a great deal of money and time.

RaaS, led by Professor Tadahiro Kuroda, director of the Systems Design Lab at the Graduate School of Engineering of the University of Tokyo, was founded to democratize access to silicon technology by accelerating the efficiency of this design process. The association, whose acronym can also be read as "Research as a Service,"

advocates providing semiconductors not as parts (products) but as units of knowledge (a service). The association aims to develop an agile design platform and deploy open architecture that can increase the development efficiency of dedicated chips by 10x.

At the same time, it will improve energy efficiency by 10x by using advanced (7nm or smaller) CMOS processes developed by the world's great foundries to fabricate chips.

Development cost is a critical issue in designing and manufacturing dedicated chips. RaaS's new initiative, led by the six maembers of the association's systems research division--Advantest, the University of Tokyo, Toppan, Hitachi, Mirise Technologies, and RIKEN--will democratize chip design and manufacturing by developing a next-generation advanced semiconductor design and development platform that can be shared among the association's members. Other participants in the semiconductor industry, such as EDA vendors and foundries, will also support this project.

Advantest and the other members of the association will utilize the energy-efficient semiconductor chips developed in this way to develop and commercialize their own products and solutions. Ultimately, the project will democratize access to silicon technology by enabling anyone to quickly design a dedicated chip and manufacture it with leading-edge semiconductor technology.

Advantest and the other members of the association will utilize the energy-efficient semiconductor chips developed in this way to develop and commercialize their own products and solutions

GlobalFoundries, Samsung Electronics, and TSMC join Imec's "Sustainable Semiconductor Technologies & Systems" (SSTS) Program

The expansion of SSTS' partner network with three of the world's top foundries marks an important milestone in bringing together the entire IC ecosystem.

K, Samsung Electronics, and TSMC have joined imec's Sustainable Semiconductor Technologies & Systems (SSTS) research program. Launched in 2021, the SSTS program rallies stakeholders from across the semiconductor industry – including systems companies, (equipment) suppliers, and now also three of the world's leading semiconductor foundries – to help reduce the ecological impact of the IC value chain.

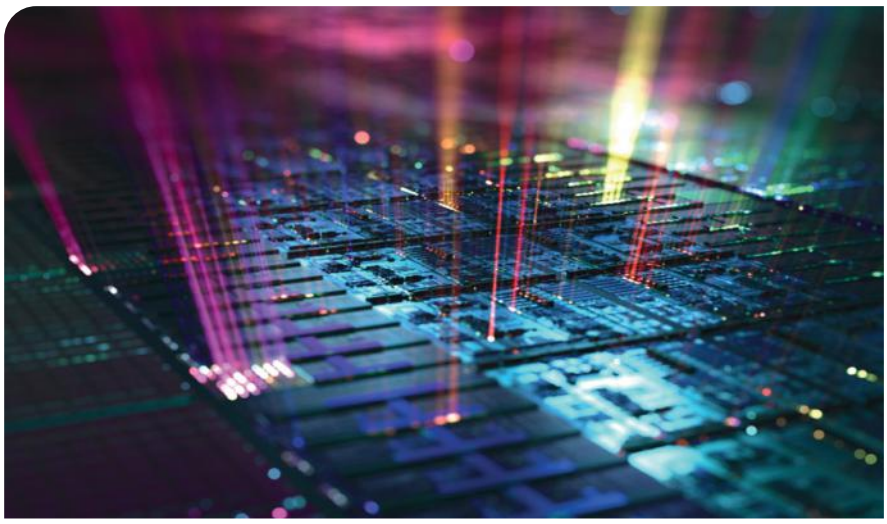
In response to mounting concerns about climate change, tech companies around the world are accelerating the efforts to complete carbon neutrality for their supply chains and products. The semiconductor industry recognizes its pivotal role in this endeavor. Studies have found, for instance, that almost 75percent of mobile devices' CO2 emissions can be traced back to the underlying manufacturing process – with chip production being responsible for nearly half of that footprint. Against this backdrop, the SSTS program provides detailed information on the environmental impact of choices made during semiconductor technology's definition phase.

Luc Van den hove, CEO of imec: "SSTS' success hinges on the active involvement of players from across the IC value chain. Hence, I am delighted to announce that GlobalFoundries, Samsung Electronics, and TSMC, have now entered the program as well as our new core program partner Rapidus – following the earlier enrollment of renowned systems companies such as Amazon, Apple, Meta and Microsoft, as well as equipment suppliers including Applied Materials, ASML, Edwards, Kurita, SCREEN and Tokyo Electron. Having secured the buy-in from foundries across the globe marks an important milestone in effectively bringing together the entire semiconductor ecosystem."

"By benchmarking our models at GlobalFoundries, Samsung Electronics, and TSMC, we will be able to further refine and optimize the imec.netzero tool, the web application that is at SSTS's very heart and that allows us to assess energy consumption, water/mineral usage, and greenhouse gas emissions associated with the various aspects of chip making. In the longer term, the partner program will also develop recommendations on how to improve the ecological footprint of chips by suggesting novel processes and technology optimizations," added Lars-Åke Ragnarsson, the program director of SSTS.

"As part of GF's longstanding commitment to environmentally responsible manufacturing and operations, we are constantly looking for new ways to minimize our impact on the environment. This includes enhancing manufacturing emission controls, further improving energy efficiency, sourcing renewable and lower-carbon energy, and engaging through key partnerships including imec's SSTS program," said Stacey Barrick, head of global ESG at GF. "As the first semiconductor manufacturer to join the SSTS, we look forward to partnering with imec and others in the semiconductor ecosystem and helping develop innovative technologies that drive change across the entire supply chain in a holistic, meaningful way."

"Our commitment to imec's SSTS program stems from Samsung Electronic's firm belief that we should not solely focus on meeting the mere technical requirements of the semiconductor industry. Being one of the world's top foundries and memory supplier, we want to lead the way in developing innovative technologies that ensure the preservation of our planet for generations to come. Teaming up with imec and the other SSTS partners allows us to translate this commitment into tangible actions," said Dooguen Song, Executive Vice President of the Environment, Health and Safety (EHS) Center at Samsung Electronics.



Global billings grow nine percent year-on-year

Global semiconductor equipment billings increased 9% year-over-year to US$26.8 billion in the first quarter of 2023, SEMI announced in its Worldwide Semiconductor Equipment Market Statistics (WWSEMS) Report. Quarter-over-quarter billings slipped 3%.

"SEMICONDUCTOR equipment revenue in the first quarter was robust despite macroeconomic headwinds and a challenging industry environment," said Ajit Manocha, SEMI president and CEO.

"The fundamentals remain healthy for the long-term strategic investments needed to support major technology advancements for AI, automotive, and other growth applications."

Compiled from data submitted by members of SEMI and the Semiconductor Equipment Association of Japan (SEAJ), the WWSEMS Report is a summary of the monthly billings figures for the global semiconductor equipment industry. Following are quarterly billings data in billions of U.S. dollars with quarter-over-quarter and year-over-year changes by region.

Region	1Q2023	4Q2022	1Q2022	1Q (QoQ)	1Q (YoY)
Taiwan	6.93	7.98	4.88	-13%	42%
China	5.86	6.36	7.57	-8%	-23%
Korea	5.62	5.80	5.15	-3%	9%
North America	3.93	2.60	2.62	51%	50%
Japan	1.90	2.25	1.90	-16%	0%
Europe	1.52	1.46	1.28	4%	19%
Rest of World	1.06	1.32	1.29	-20%	-18%
Total	**26.81**	**27.78**	**24.69**	**-3%**	**9%**

Sources: SEMI (www.semi.org) and SEAJ (www.seaj.or.jp), June 2023
Note: Summed subtotals may not equal the total due to rounding.

Moderate industry contraction

The current global semiconductor manufacturing industry contraction is expected to moderate in the second quarter of 2023 and give way to a gradual recovery starting in the third quarter, SEMI announced in its Q1 2023 publication of the Semiconductor Manufacturing Monitor (SMM) Report, prepared in partnership with TechInsights.

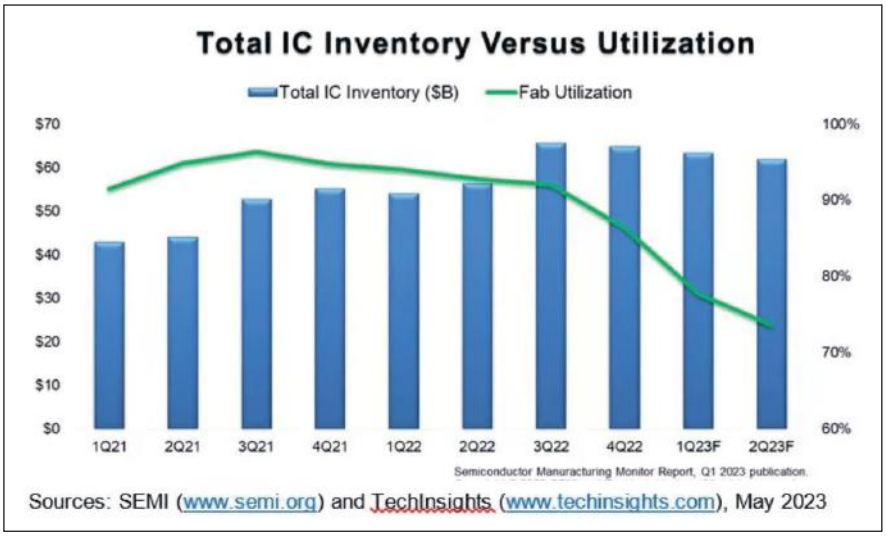
In the second quarter of 2023, industry indicators including IC sales and silicon shipments – both partly supported by seasonality – point to quarter-over-quarter improvements.

However, despite the gains, elevated inventories continue to dampen silicon shipments and fab utilization rates remain significantly lower than levels registered last year. In addition, semiconductor equipment sales continue to decline in parallel with capital expenditure adjustments by major industry stakeholders.

The indicators point to a likely bottoming of the current downturn in the second quarter of 2023 with a slow recovery expected to begin in the year's second half.

"The current market downturn is compounded by soft consumer demand and elevated inventory levels and has led to a sharp decline in semiconductor fab utilization," said Clark Tseng, Senior Director of Market Intelligence at SEMI. "However, as the inventory correction comes to an end in mid-2023, a mild recovery is expected in the second half of the year driven by a pickup in demand for inventory and the holiday season."

"Despite ongoing uncertainties and risks, we expect continuing production cuts and capex reductions, especially in the memory market, will start having a positive impact on market fundamentals in the latter part of the year, resulting in a more balanced market environment," said Risto Puhakka, VP of Market Analysis at TechInsights.



Packaging materials market to near $27 billion

Powered by strong demand for new electronics innovations, the global semiconductor packaging materials market is expected to reach US$29.8 billion by 2027, a compound annual growth rate (CAGR) of 2.7% from the US$26.1 billion in revenue it logged in 2022, SEMI, TECHCET and TechSearch International announced in their new Global Semiconductor Packaging Materials Outlook report.

High-performance applications, 5G, artificial intelligence (AI) and the adoption of heterogeneous integration and system-in-package (SiP) technologies are increasing demand for advanced packaging solutions. The development of new materials and processes to enable chips with higher transistor density and greater reliability are also contributing to market growth.

"The semiconductor packaging materials industry is undergoing significant changes as new technologies and applications are driving demand for more advanced and diverse materials," said Jan Vardaman, President and founder of TechSearch International. "Advances in dielectric materials and underfill are driving strong demand for fan-in and fan-out wafer level packaging (FOWLP), flip chip, and 2.5D/3D packaging. New substrate technologies such as silicon interposers and organic interposers using RDL (Re-Distribution Layer) are also key growth drivers of packaging solutions. At the same time, research on laminate substrates with finer features continues with the development of glass cores for build-up substrates."

Materials market revenue reaches record $73 billion

Global semiconductor materials market revenue grew 8.9% to $72.7 billion in 2022, surpassing the previous market high of $66.8 billion set in 2021, SEMI reported in its Materials Market Data Subscription (MMDS).

Wafer fabrication materials and packaging materials revenue in 2022 reached $44.7 billion and $28.0 billion, respectively, increasing 10.5% and 6.3%. The silicon, electronic gases, and photomask segments showed the strongest growth in the wafer fabrication materials market, while the organic substrates segment largely drove packaging materials market growth.

	2021**	2022	Year-Over-Year
Taiwan	$17,715	$20,129	13.6%
China	$12,082	$12,970	7.3%
South Korea	$12,134	$12,901	6.33%
Rest of World*	$7,896	$8,627	9.3%
Japan	$7,275	$7,205	-1.0%
North America	$5,713	$6,278	9.9%
Europe	$3,961	$4,580	15.6%
Total	**$66,776**	**$72,691**	**8.9%**

Source: SEMI (www.semi.org), June 2023
Note: Summed subtotals may not equal the total due to rounding.
* Rest of World includes Singapore, Malaysia, Philippines, other areas of Southeast Asia and smaller global markets.
** 2021 data reflects current updates.

For the 13th consecutive year, Taiwan, at $20.1 billion, was the world's largest consumer of semiconductor materials on the strength of its foundry capacity and advanced packaging base. China continued to register strong year-over-year results, ranking second in 2022, while Korea finished as the third largest consumer of semiconductor materials. Most regions registered high single- or double-digit growth last year.

Global 300mm fab equipment spending to reach $119 billion in 2026

Global 300mm fab equipment spending for front-end facilities next year is expected to begin a growth streak to a US$119 billion record high in 2026 following a decline in 2023, SEMI highlighted in its quarterly 300mm Fab Outlook Report to 2026. Strong demand for high-performance computing, automotive applications and improved demand for memory will fuel double-digit spending in equipment investments over the three-year period.

After the projected 18% drop to US$74 billion this year, global 300mm fab equipment spending is forecast to rise 12% to $US82 billion in 2024, 24% to US$101.9 billion in 2025 and 17% to US$118.8 billion in 2026.

"The projected equipment spending growth wave underscores the strong secular demand for semiconductors," said Ajit Manocha, SEMI President and CEO.

Regional Growth

Korea is expected to lead global 300mm fab equipment spending in 2026 with US$30.2 billion in investments, nearly doubling from US$15.7 billion in 2023. Taiwan is forecast to invest US$23.8 billion in 2026, up from US$22.4 billion this year, and China is projected to log US$16.1 billion in spending in 2026, an increase from US$14.9 billion in 2023. Americas equipment spending is expected to nearly double from US$9.6 billion this year to US$18.8 billion in 2026.

Segment Growth

Foundry is projected to lead other segments in equipment spending at US$62.1 billion in 2026, an increase from US$44.6 billion in 2023, followed by memory at US$42.9 billion, a 170% increase from 2023. Analog spending is forecast to increase from US$5 billion this year to US$6.2 billion in 2026. The microprocessor/microcontroller, discrete (mainly power devices), and optoelectronics segments are expected to see spending declines in 2026, while investments in logic is forecast to rise. The SEMI 300mm Fab Outlook Report To 2026 report lists 369 facilities and lines globally, including 53 high-probability facilities expected to start operation during the four years starting in 2023.

siconnex

Green Goals. Yellow Solutions.

Sustainability and environmental health are in our DNA. BATCHSPRAY® technology delivers energy-, media- and water-saving processes throughout the chip manufacturing cycle. With two decades of experience in batch spray and its hardware, Siconnex has grown to be the leading supplier of sustainable wet processing equipment.

The production of semiconductors consumes a considerable amount of resources. By embracing sustainable products and processes, the semiconductor industry can mitigate its environmental impact and work towards a more sustainable future.

Siconnex has been dedicated to efficient and resource-saving solutions for years, with its BATCHSPRAY® technology leading the way. The company continuously enhances its expertise in sustainable processes, driven by both its own mission statement and the sustainability goals of its customers. One such advancement is the perc™ process for Post Etch Residue Clean, which represents our latest sustainable offering.

Big challenge: Polymer removal

"My experience with perc™ is that after sending wafers through several dry etch steps, we successfully found a recipe to remove all polymers and achieve better sidewall roughness. After conducting electrical checks, we even discovered improved performance compared to the existing process. I genuinely appreciate the excellent cooperation and collaborative work with Siconnex to find solutions for both new and existing processes."

The statement by Dr. Julien Ladroue, STMicroelectronics, highlights the successful implementation of perc™ in addressing the challenge of polymer removal and achieving improved performance in chip production. In the context of device scaling and the difficulties associated with removing polymers using solvent-based processes, perc™ offers a solution that avoids the need for additional solvent media.

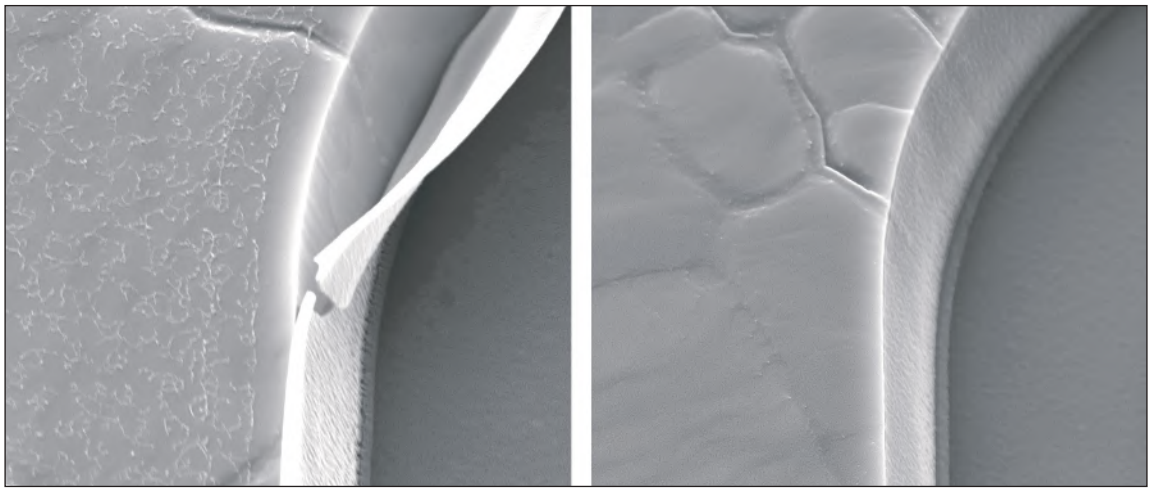
perc™, the process innovation from Siconnex, is specifically designed for Post Etch Residue Clean. This innovative application allows for the removal of several types of polymers by adjusting the process recipe. Siconnex's unique spiking technology ensures that only a limited quantity of acid is required within the DIW stream, resulting in a significant reduction in acid flow.

In addition to polymer removal, the perc™ process provides the ability to control metal loss within the recipe. This brings numerous advantages, including guaranteed polymer removal, reduced metal loss, considerable reduction in chemical consumption and water usage, efficient waste treatment, and other benefits.

Overall, perc™ represents a significant advancement in chip production, offering a sustainable and efficient solution for polymer removal and contributing to the overall goal of achieving more sustainable and cost-effective processes.

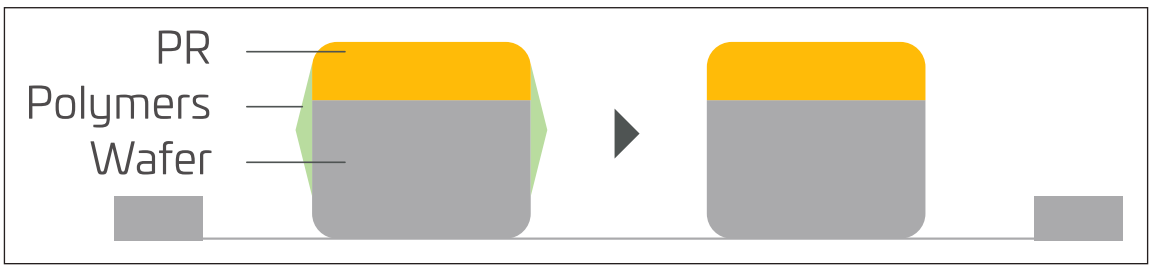
Post Plasma Dicing Clean

Plasma etching for wafer dicing is a dry etch process that is becoming increasingly significant and will have a growing impact on the industry in the future. This approach offers the advantage of saving considerable space in the planar direction of dicing, while also minimizing residues compared to mechanical or laser dicing.



Courtesy of STMicroelectronics

➤ After dry etch process (left) and after perc ™ process (right)



➤ Polymer removal with Post Plasma Dicing Clean

Benefits of perc™ process

Metal loss:
- Aluminum-Copper: <20 Å
- Titanium-Nitride: <15 Å
- No loss of Silicon-Oxide

Throughput per chamber:
- 136 wph
- Process time: 21 min

Chemical consumption:
- DIW: 110 liters
- H_2SO_4: 100 ml
- H_2O_2: 700 ml
- HF: 70 ml

Advantages:
- Adjustable for each polymer
- Flexible parameter adjustment
- Very low chemical usage
- Point-of-use media usage
- Stable media concentration
- Open process time
- Single-use media
- Recontamination is avoided
- High throughput
- Solvents are obsolete
- Easy waste treatment
- 4 chamber system available
- 25W/50W chamber
- Available for 2“ - 12“ wafers

However, there are challenges associated with plasma etch dicing. Thicker top photoresists become more difficult to remove after treatment, and the removal of sidewall polymers becomes even more complex since the wafer is already diced.

To address these challenges, Siconnex has developed a process called Post Dicing Clean, which effectively removes polymers, photoresist, and residues in a single process step. By treating the entire frame and sticky tape where the diced wafer is positioned, the post dicing clean efficiently removes polymers from the sidewalls.

Additionally, plasma-treated photoresist can be easily removed, and residues can be cleaned from the surface.

The post dicing clean process effectively mitigates the drawbacks associated with plasma dicing, providing a sustainable and environmentally friendly solution. The technology used to handle these frames has been in operation for several years, ever since Siconnex initially delivered systems for fully automated 300 mm fabs.

Excellence in 300 mm wafer processing

Wet etch and clean processes performed in batch spray systems have long been essential in 200 mm fabs. However, the assumption that what works for 200 mm may not be applicable to 300 mm is

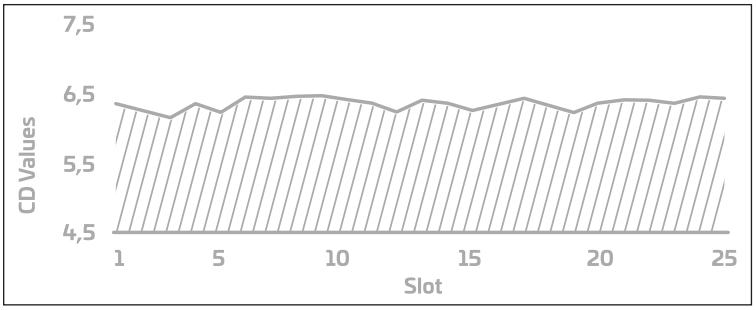
incorrect. The results achieved in 300 mm wafer processing are equal with those achieved in 200 mm.

Traditional wet processes conducted in wet benches or single wafer tools, which have been in use for many years, have not delivered leading-edge results concerning within-wafer uniformity, wafer-to-wafer uniformity, batch-to-batch uniformity, cleanliness, and sustainable execution.

Siconnex's BATCHSPRAY® equipment can significantly enhance all these specifications and more. Multiple processes can be performed within a single system, eliminating the need for multiple tools. Complex process sequences, such as AlSiCu etch followed by Freckle etch to remove any remaining silicon grains, and then a barrier etch to etch materials like Ti, TiN, TiW, and W, along with subsequent photoresist strip, can all be accomplished in one system. Furthermore, even dry etch processes, like the barrier etch mentioned earlier, can be replaced and executed sustainably.

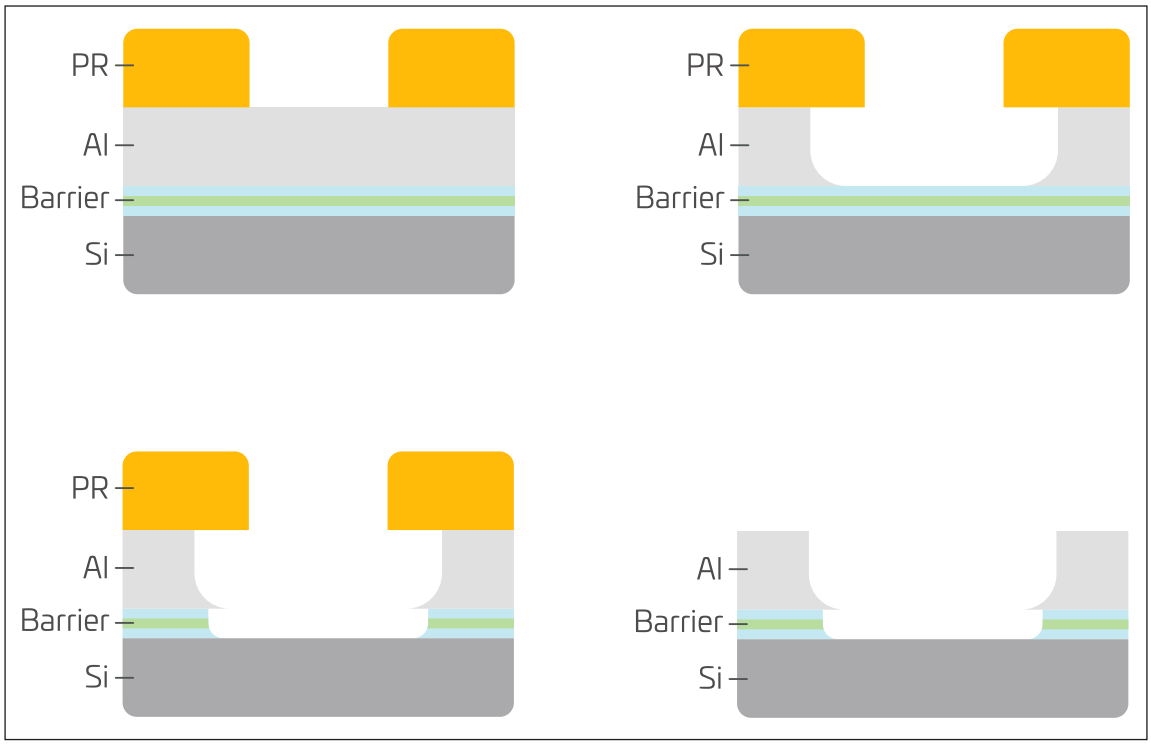
With its fully automated BATCHSPRAY® systems, Siconnex provides leading-edge results for wet processing, making it an ideal match for the 300 mm wafer world. Siconnex offers a complete platform of hardware and processes for sustainable 300 mm wafer manufacturing. Through the development of new sustainable processes and the delivery of cutting-edge results for wet processing, Siconnex has experienced rapid growth in its installed base.

With a focus on sustainability and continuous innovation, Siconnex is at the forefront of semiconductor manufacturing. The perc™ process addresses the challenge of polymer removal, while the Post Dicing Clean process tackles the complexities of plasma etching. The BATCHSPRAY® technology offers exceptional results for wet processing in 300 mm fabs, promoting uniformity, cleanliness, and sustainability. Siconnex's commitment to developing new, sustainable processes contributes to a more sustainable and efficient future for the industry.

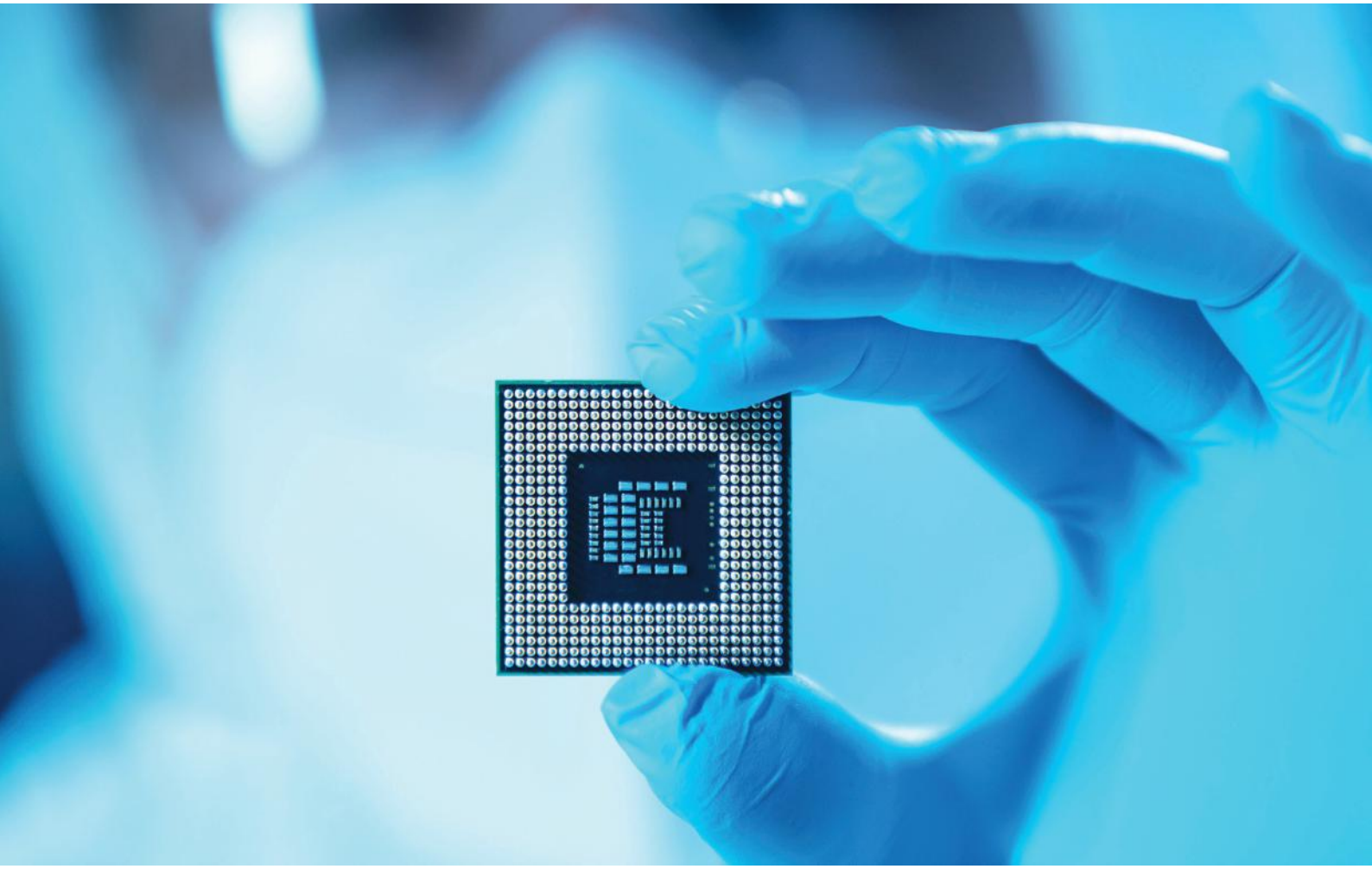


➤ Uniformity in batch processing of 300 mm wafers

> "After conducting electrical checks, we even discovered an improved performance compared to the existing process."
>
> Dr. Julien Ladroue, STMicroelectronics



➤ Process flow examples for Al etch, barrier etch and photostrip resist



Microelectronics Academy emphasizes the importance of education

The Microelectronics Academy, located at Fraunhofer's Research Fab Microelectronics Germany (FMD), launched in December 2022, and has the task of developing and testing concepts with the aim of offering up-to-date teaching content and methods in the field of microelectronics.

THE GLOBAL CHIP and semiconductor crisis, which was mainly triggered by the pandemic and its consequences for international supply chains, has led Europe and Germany to focus more closely on efforts for domestic production in microelectronics.

In addition, military crises in Europe and realistic threat scenarios from Asia have fueled concerns that the global supply chain for microchips could come to a standstill.

All these factors have led to increased awareness of domestic production of microelectronic systems. This is also linked to the drastically increasing demand for the most important production factor: the resource of well-trained specialists, without whom concrete implementation is unthinkable. Against this background, the economic importance of training and qualification in microelectronics quickly becomes clear.

Field of work: Orchestrating microelectronics
The Microelectronics Academy, launched in December 2022, has the task of developing and testing concepts with the aim of offering up-to-date teaching content and methods in the field of microelectronics. This also includes target group-specific communication to increase the attractiveness of the microelectronics profession. For this purpose, cooperation with other educational

institutions as well as research and industrial partners is planned, which expresses the core idea of the microelectronics academy: to create a network of equal players who orchestrate training and qualification together. It's not about reinventing the wheel; Rather, the focus is on a jointly coordinated approach in the field of training and qualification in one of the most important future technologies of our time. The need is based on the wishes and requirements of companies from the microelectronics sector in order to ensure effective support for business and industry.

Background information

The Microelectronics Academy is funded within the framework program for microelectronics of the federal government, the funds for which are made available by the Federal Ministry of Education and Research (BMBF). The implementation will initially take place in two projects: the cross-site competence center for resource-conscious information and communication technology „Green ICT@FMD" and the FMD module quantum and neuromorphic computing „moduleQNC".

Focus: Recruiting young people

Due to the worldwide developments described above, the European Union aims to increase the world market share of chip production to 20% by 2030. The share of European chip production is currently around 9%. At the same time, global microchip production is forecast to double by 2030. For Europe, this means that domestic capacities must increase by more than 400% in order to achieve the ambitious goal in Europe. This will also require four times as many workers in the microelectronics sector by 2030. However, without targeted measures, the targeted workforce will very likely not be available.

The number of young people who are interested in professions in the so-called MINT subjects (mathematics, computer science, natural sciences, technology) does not even begin to cover the need for workers. This also applies to microelectronics, in research as well as in business and industry. Overall, the number of young people who are interested in relevant professions is declining.

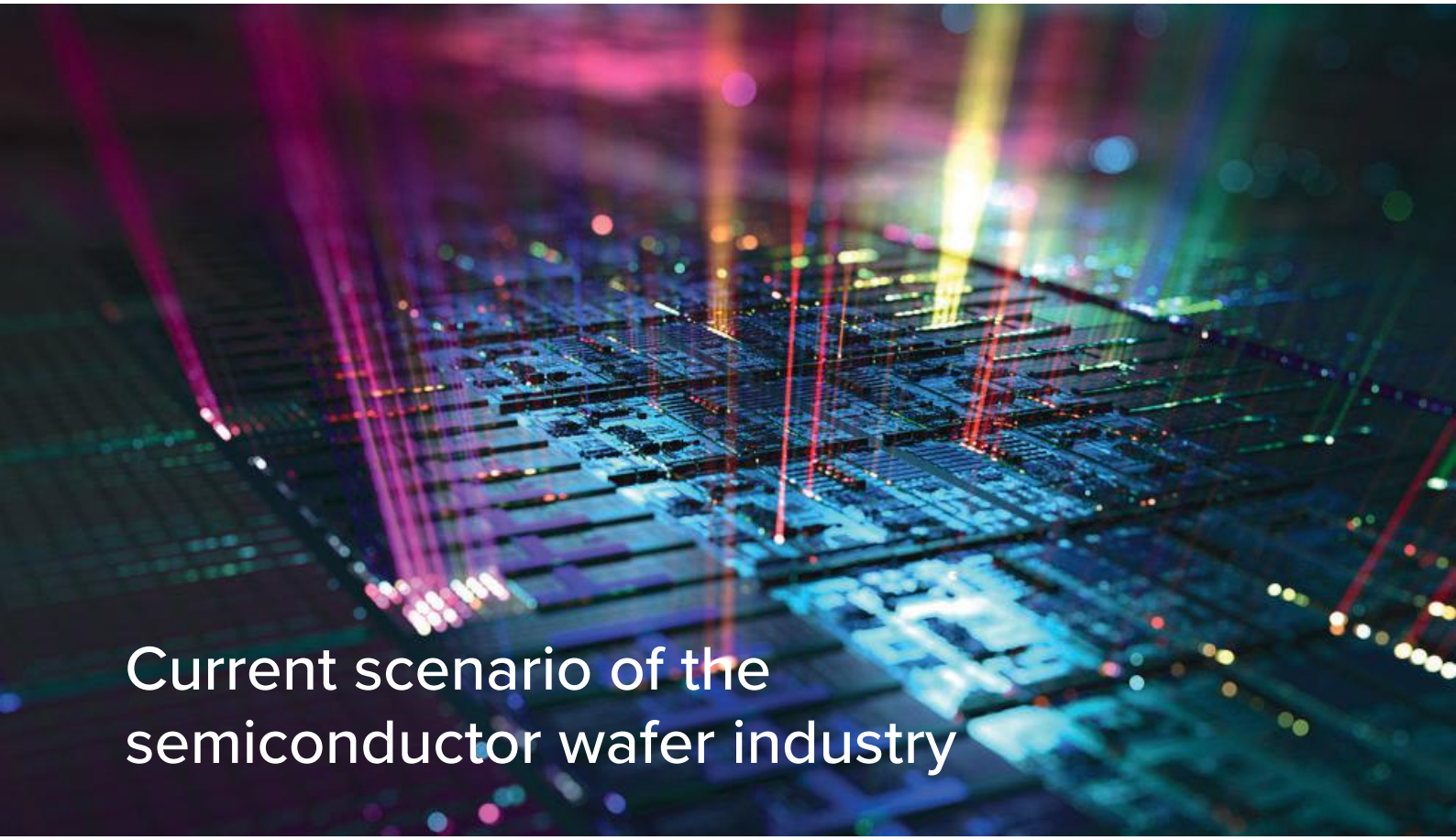
At the same time, dealing with microelectronic systems is part of everyday life for young people from an early age. Gaming and social media, which would be unthinkable without microelectronics, are also an integral part of cultural life today.

Why are relatively so few interested in "hiring" a career in microelectronics? How can the gap – large points of contact with microelectronics on the one hand and relatively little professional interest on the other – be closed? Finding answers to these questions and pointing out concrete solutions are the tasks of the Microelectronics Academy.

Structure and policy

The responsibility for the program as well as the organizational management of the Microelectronics Academy is located at the Research Fab Microelectronics Germany (FMD). The technical support of the work of the Microelectronics Academy is guaranteed by a high-ranking committee, which includes several institute directors from Fraunhofer and Leibnitz institutions, chaired by Prof. Gerhard Kahmen.

The Microelectronics Academy has just started its work, which is met with great interest at various levels of society. For the FMD, coping with the upcoming tasks of the Microelectronics Academy is a challenge, also in view of the needs outlined. At the same time, the Microelectronics Academy offers the great opportunity to play a decisive role in setting the course for the central future technology "microelectronics" and to use the existing skills of the FMD association to secure Germany as a business and industrial location.



Current scenario of the semiconductor wafer industry

Recent developments that have impacted the market's landscape.

By Koyel Gosh, Team Lead, Allied Market Research.

THE INCREASING DEMAND for electronic devices in consumer and industrial settings has led to substantial growth in the semiconductor wafer industry. The market's landscape has changed significantly due to the introduction of new products, mergers, acquisitions, and other recent developments.

One noteworthy development in the industry is the growing demand for 5G technology. As the world moves toward a more connected future, 5G technology is expected to be the backbone of this network. As a result, demand for semiconductors used in 5G technology has grown exponentially. Companies such as TSMC (Taiwan Semiconductor Manufacturing Company) and Samsung have already started producing 5G chips on their 7nm process node.

Another recent development is the increased demand for electric vehicles (EVs). As the world moves toward cleaner energy solutions, EVs are becoming more and more popular. Semiconductors are necessary components to operate vehicles, especially in power electronics where Insulated Gate Bipolar Transistors (IGBTs) are commonly used. This growing demand has resulted in a shortage of semiconductors, particularly those used in the automotive sector.

Growing demand for digitization has propelled the industry in more than one way-

The semiconductor industry plays a crucial role in driving innovation across various sectors such as electronics, automobiles, and automation. The core component of many microelectronic devices, the semiconductor silicon wafer, has become increasingly important with the rising demand for digitization and electronic mobility. As gadgets become smaller, there is a need for more functionalities from a single device, which means that integrated circuit (IC) chips should have more transistors to support additional features.

To keep up with these demands, foundries are investing in advanced packaging techniques, particularly those based on silicon wafers. Researchers are currently investigating the use of two-dimensional materials in the development of Monolithic 3D Integrated Circuits as a possible alternative to silicon, with the goal of improving

transistor density. For example, TSMC has developed a technology called "chip on wafer on substrate," which features the world's largest silicon interposer, measuring nearly 2500mm2. This interposer can accommodate two 600mm2 processors and eight HBM memory devices in a 75mm2 package. These advancements and innovations in the semiconductor industry are significantly impacting downstream technologies. Keeping in tab with a recent report by Allied Market Research, the global semiconductor wafer market is anticipated to exhibit a considerable CAGR from 2021 to 2030.

Wearable devices are set to provide significant growth opportunities for the market vendors too, especially in the industrial sector, where they have the potential to improve quality and safety. Siemens predicts that the market for industrial wearables will be substantial. Zebra Technologies Corporation forecasts that 40-50% of global manufacturers will have adopted wearable technology by 2022. In addition, there has been a rise in the desire for compact electronic devices, leading to an expectation for increased capabilities and features within a single gadget. As a result, IC chips will need to incorporate more transistors to support these additional features.

Emerging economies such as China have implemented government policies that are favorable to the semiconductor industry. This has created significant growth opportunities in the semiconductor silicon wafer market, which is expected to continue expanding in the forecast period. One example of such policies is the framework issued by the State Council of the People's Republic of China, which prioritizes the development of advanced semiconductor packaging solutions within the industry.

The Consumer Technology Association's study on US consumer technology sales and forecast predicts that 5G-enabled smartphones will see significant growth in 2021, with 2.1 million units sold and over USD 1.9 billion in revenue. Meanwhile, Apple has announced plans to contribute USD 350 billion to the US economy by 2023 and create 2.4 million jobs over the next five years through new investments and spending with domestic companies. Apple's recent announcement is expected to drive up the demand for semiconductor silicon wafers, given their significant presence in the consumer electronics industry.

Innovative product launches by companies

The Singapore-MIT Alliance for Research and Technology (SMART) has recently made an announcement regarding their successful development of a way to manufacture integrated silicon III-V chips that contain high-performance III-V devices. While silicon-based CMOS chips are widely used for computing purposes, they are not as efficient when it comes to communication and illumination. This results in lower efficiency and increased heat generation, causing 5G mobile devices to become hot and shut down quickly. In order to deal with the issue, it is essential to integrate III-V semiconductor devices with silicon. However, this has been a complex challenge for the semiconductor industry to overcome. SMART's accomplishment represents a significant step towards solving this issue in a commercially viable manner.

The semiconductor wafer market is characterized by rapid innovation, and companies are continually launching new products to meet the demands of the market. One recent product launch worth mentioning is Intel's 11th Gen Core Processors. The processors use Intel's 10nm SuperFin technology, which allows for improved performance and power efficiency. The launch of these processors has caused a shift in the market, with other companies rushing to release similar products.

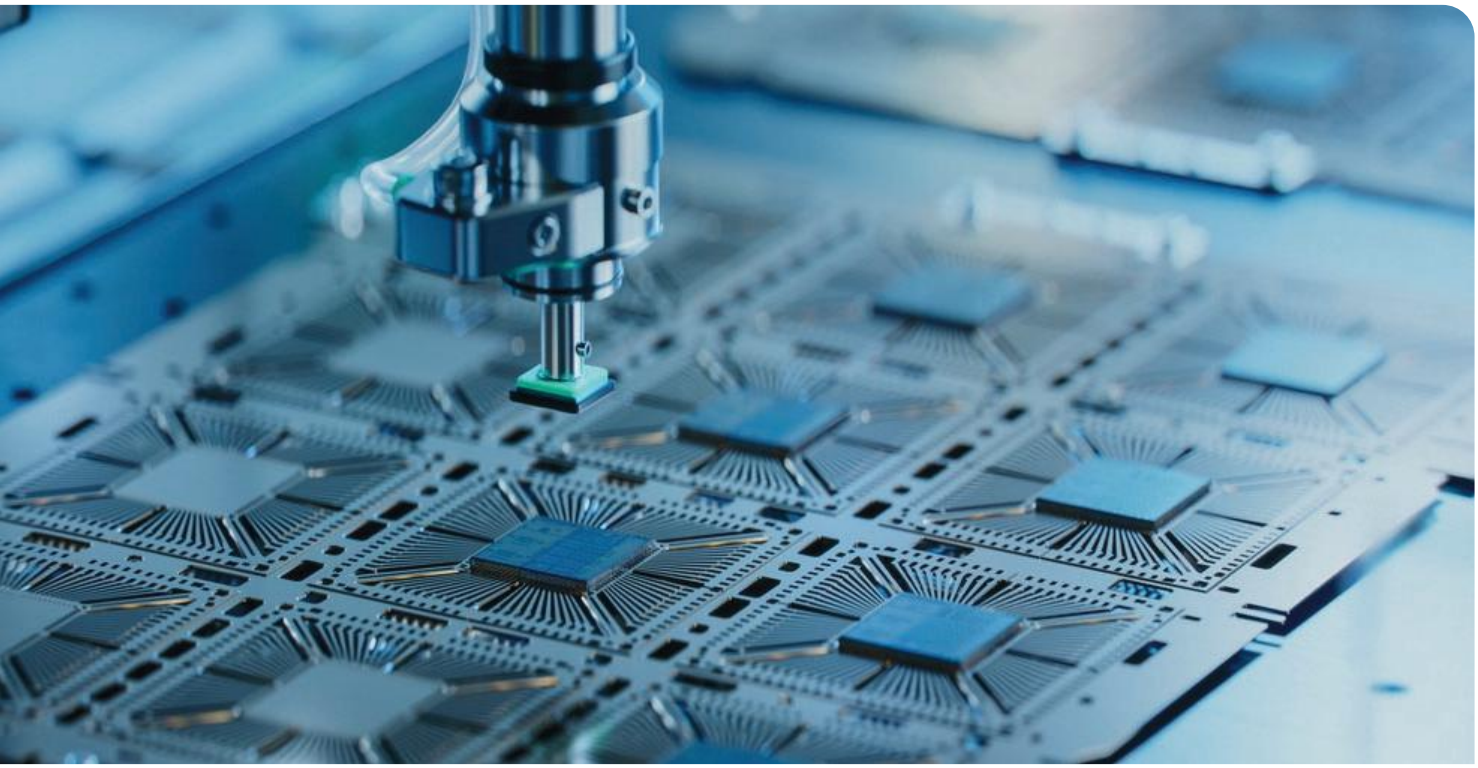
TSMC, a major semiconductor manufacturer, recently announced its plans to invest USD 12 billion between 2021 and 2029 towards constructing a 12-inch wafer plant that will produce chips using the advanced 5 nm process. This indicates a positive trend towards the growth of the semiconductor industry in North America. Additionally, the relocation of tech supply chains from foreign countries to North America is expected to continue, even after the change in political leadership from Donald Trump to Joe Biden, who had previously encouraged foreign companies to invest and create employment opportunities in the United States. Furthermore, the United States has some of the world's major players in the automotive industry, who are investing in electric vehicles and the self-driving potential of cars. This is fueling the demand for high-performance Integrated Circuits (ICs) in the semiconductor silicon wafers market.

The notable mergers and acquisitions in the industry

Mergers and acquisitions have also become prevalent in the semiconductor wafer market, as companies aim to broaden their product range and enhance their technological capabilities. One notable example of such a merger is the acquisition of Arm Holdings by NVIDIA. Arm Holdings is a major provider of semiconductor intellectual property, and NVIDIA's purchase of the company will enable it to extend its footprint in the data center and AI sectors.

Intel's recent acquisition of GlobalFoundries, one of the leading semiconductor foundries, is worth noting indeed. By acquiring GlobalFoundries, Intel aims to bolster its manufacturing capabilities and better compete with key players in the industry such as Samsung and TSMC. The acquisition is expected to be completed by the end of 2021.

On the other hand, SK Siltron Co. has recently announced that it plans to invest 1.05 trillion in the



next three years to expand its facilities for 300 mm wafers located in Gumi National Industrial Complex 3. GlobalWafers Co., a top-notch silicon wafer supplier in the world, is set to begin expansion work in 2022, with mass production slated to start in 2024. The company anticipates adding roughly 20,000 state-of-the-art 12-inch wafers per month from its local fabs as a result of this expansion. The company anticipates that this expansion will increase its capacity by 10-15% at its plants in South Korea, Japan, Taiwan, and Italy, thereby meeting the robust demand for its products.

Shin-Etsu Chemical Co. Ltd has recently declared a 10 percent increase in the pricing of all its silicone goods, and one of its business areas will be expanded in Japan and worldwide. As a result, there has been a significant surge in prices, along with increased transportation costs for raw materials procurement and finished goods distribution.

Experts at the Massachusetts Institute of Technology have developed a method for creating thin transistors directly on top of computer chips using automation technology-

MIT researchers have developed a new technology that can “grow” ultrathin 2D materials directly on top of a fully fabricated silicon chip, enabling the creation of denser and more powerful computer chips. This is a significant development as semiconductor chips traditionally use bulk materials that are difficult to stack to create denser integrations. The challenge has been that the process of growing 2D materials on a silicon wafer requires temperatures of about 600 degrees Celsius, which can damage the silicon transistors and circuits that cannot be heated above 400 degrees. The interdisciplinary team of MIT researchers has overcome this challenge by developing a low-temperature growth process that does not damage the chip. This process allows 2D semiconductor transistors to be directly integrated on top of standard silicon circuits. The latest technology has the capability to grow a consistent layer of TMD material on an entire 8-inch wafer in less than 60 minutes, which represents a substantial reduction in the time required to cultivate these materials uniformly. This new process of developing 2D materials directly onto a silicon wafer is a major advancement as it avoids imperfections that can occur when transferring the material from elsewhere and enables the creation of denser and more powerful computer chips.

The researchers focused on a 2D material called molybdenum disulfide, which has excellent electronic and photonic properties and is suitable for use in semiconductor transistors. This material is made up of a layer of molybdenum atoms sandwiched between two layers of sulfur atoms, and it is flexible and transparent.

To grow thin films of molybdenum disulfide, a process called metal-organic chemical vapor deposition (MOCVD) is often used. The process involves subjecting two organic compounds containing molybdenum and sulfur atoms to temperatures exceeding 550 degrees Celsius.

This leads to their decomposition into smaller molecules that subsequently combine to form chains of molybdenum disulfide on a surface. However, the use of such high temperatures poses a challenge, as

it can cause the degradation of silicon circuits, which begin to break down above 400 degrees.

A new furnace has been devised for the MOCVD (metal-organic chemical vapor deposition) process, which consists of two chambers: one for placing the silicon wafer at a low temperature, and the other for heating the precursors to a high temperature (above 550 degrees Celsius). The molybdenum precursor is kept in the low-temperature region to prevent damage to the silicon wafer and is decomposed at a temperature below 400 degrees Celsius. Meanwhile, the sulfur precursor is allowed to flow into the high-temperature region, where it is decomposed, and then returns to the low-temperature region for the chemical reaction that facilitates the growth of molybdenum disulfide on the surface of the wafer.

The specialists also developed a new method for growing molybdenum disulfide on silicon wafers using metalorganic chemical vapor deposition (MOCVD). They found that placing the wafer vertically in the low-temperature area of the furnace allowed for better material uniformity, as the gas molecules swirled around the chip and improved the growth of the material. This method was also much faster than traditional MOCVD processes, with a layer being grown in less than an hour compared to a full day. The vertical placement of the wafer ensured that no part of it was damaged by the heat, as neither end was too close to the high-temperature region. The scientists have utilized the advanced MIT. Nano facilities to exhibit excellent quality and uniformity of materials over an 8-inch silicon wafer. This achievement holds significant importance for industrial applications that require larger wafers. The process used to achieve this outcome is highly efficient, as it reduces growth time and can be easily incorporated into industrial processes. Additionally, the process is compatible with low-temperature silicon, which makes it feasible to extend the use of 2D materials in the semiconductor industry.

The technologists aspire to improve their techniques and apply them towards the development of multiple layers of 2D transistors stacked on top of each other, with the goal of enhancing their functionality and performance. They also plan to explore the use of the low-temperature growth process for flexible surfaces such as polymers, textiles, or papers. The successful application of this process could enable the integration of semiconductors into everyday objects like clothing or notebooks.

The funding for this project has been provided by a diverse range of organizations including the National Science Foundation Center for Integrated Quantum Materials, Ericsson, the U.S. Department of Energy, the U.S. Army Research Office, MITRE, and the MIT Institute for Soldier Nanotechnologies. The project has also received support from TSMC University Shuttle.

The potential of AI

Realising impact for businesses and consumers.

By Leo Charlton (research interests are in quantum technologies and nanophotonics) is a Technology Analyst with IDTechEx.

THE EMERGENCE of generative AI over the past five years – the most famous examples of which being OpenAI's DALL-E 2 image generator and ChatGPT – has been a key milestone for the ongoing AI boom.

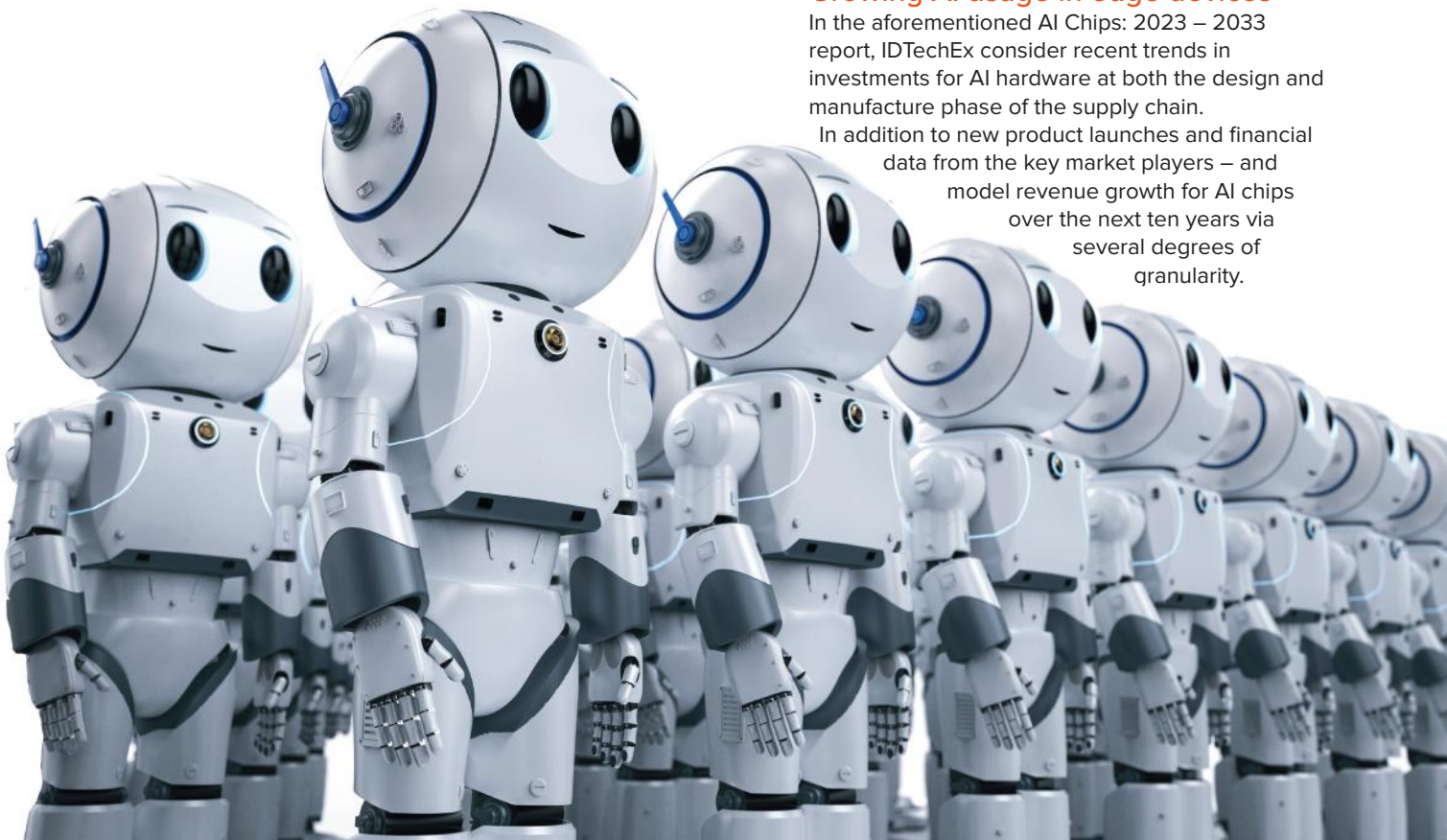
The robust predictive abilities of ChatGPT in particular have given a glimpse into the transformational power of AI across numerous industry verticals, where companies will be faced with the dilemma of how to effectively utilize AI tools for maximum business impact as the breadth and depth of AI models grow.

While by and large software has received more media attention of late than hardware – a not unnatural occurrence, given end-users and those that analyse the impact of such technologies care ultimately about what a tool can do, not how it can do it – the promise of AI models would remain unrealized were it not for the design and manufacture of hardware that can run these models in a cost-effective manner. As software develops in complexity (the most advanced AI models being more computationally intensive than those from yesteryear), advanced hardware is needed in order to facilitate growth.

According to a recently published report by IDTechEx on AI chips – the semiconductor circuitry that enables such AI functionalities as natural language processing, object detection and classification, and speech recognition – the global AI chips market will grow to more than US$250 billion by 2033, with the IT & Telecoms, Banking, Financial Services and Insurance (BFSI), and Consumer Electronics industries being key beneficiaries of emerging AI technologies.

Growing AI usage in edge devices

In the aforementioned AI Chips: 2023 – 2033 report, IDTechEx consider recent trends in investments for AI hardware at both the design and manufacture phase of the supply chain. In addition to new product launches and financial data from the key market players – and model revenue growth for AI chips over the next ten years via several degrees of granularity.



A key finding from the report is related to the revenue split over the forecast period between chips used for inference purposes versus those used for training.

Training and inference are the two stages of the machine learning process, wherein computer programs utilize data to make predictions based on a model, and then optimize the model to better fit with the data provided by adjusting the weightings used. The first stage of implementing an AI algorithm is the training stage, where data is fed into the model and the model adjusts its weights until it fits appropriately with the provided data.

The second stage is the inference stage, where the trained AI algorithm is executed, and new data (that was not provided in the training stage) is classified in a manner consistent with the acquired data. Of the two stages, the training stage is more computationally intensive, given that this stage involves performing the same computation millions of times.

The training for some leading AI algorithms can take days to complete, with ChatGPT using around 10,000 Nvidia A100 GPUs to train the GPT-3.5 large language model (LLM) on which it is based. Yet, despite these already impressive numbers, IDTechEx forecast that chips used for inference purposes will grow to contribute to more than two-thirds of total AI chip market revenue as of 2033.

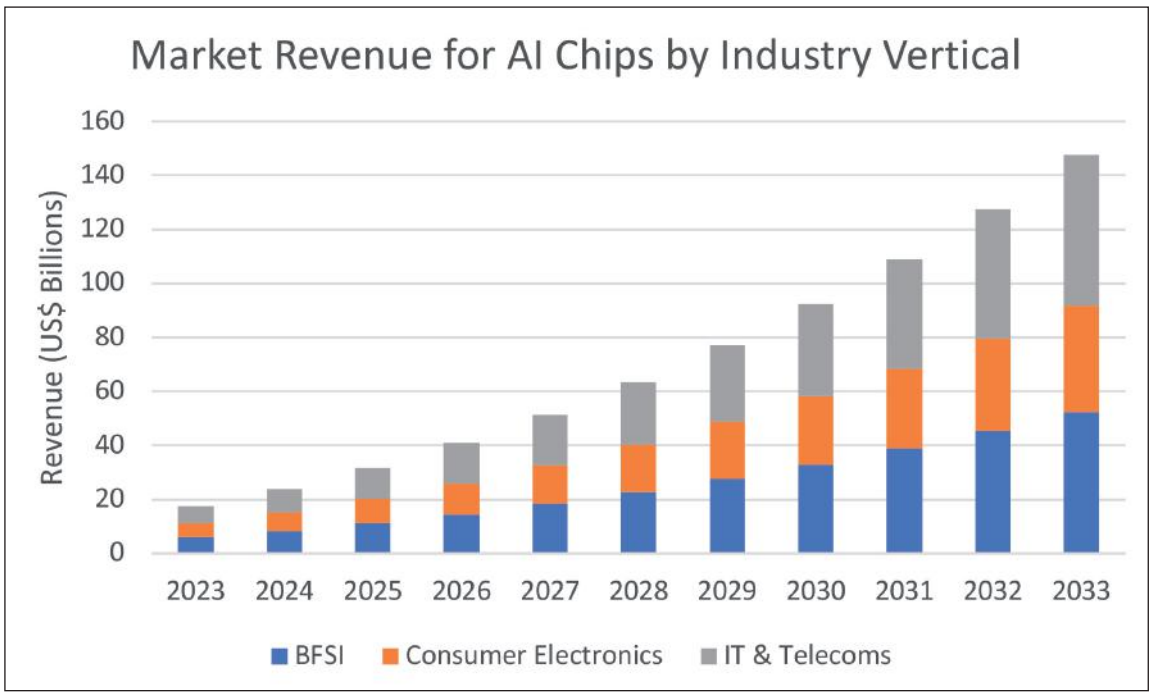
As all AI training takes place within the data centre in a cloud computing environment, this speaks to not only the continued use of inference chips in a cloud environment, but also the higher growth rate of AI chips used in edge devices than in a cloud environment (given that AI chips within edge devices are used for inference purposes) over the next ten years.

Adoption of AI-capable chips within edge devices is imperative to certain applications – such as fully-autonomous vehicles – and increasingly commonplace in others (such as in mobile phones). However crucial AI is to a particular application, effective deployment has the potential to create 'new normals' across industries.

The transformative powers of AI

While the birth of ChatGPT in 2022 delivered the most compelling example to date of what generative AI is capable of, many years of development – into this and other tools– preceded it. Google DeepMind's AlphaGo victory over Go world champion Lee Sedol in 2016 could feasibly be argued to be the AI landmark that kicked off the current boom, as it was generally considered prior to this that Go was just too difficult a game for AI to achieve victory within the time constraints of a tournament game.

IDTechEx take the view that this latest epoch in artificial intelligence began slightly earlier, with the introduction of the Siri virtual assistant to Apple phones in 2011. Siri is a virtual assistant that uses speech recognition to answer queries or follow directions from the user. By triggering the virtual assistant with the words 'Hey Siri', users speak into the phone, the speech recognition software translates what is spoken into computer code, and outputs text and/or a voice response from Siri. Siri's capabilities have been expanded over the years, from simple phone commands such as 'read my new messages', to handling payments through Apple Pay.



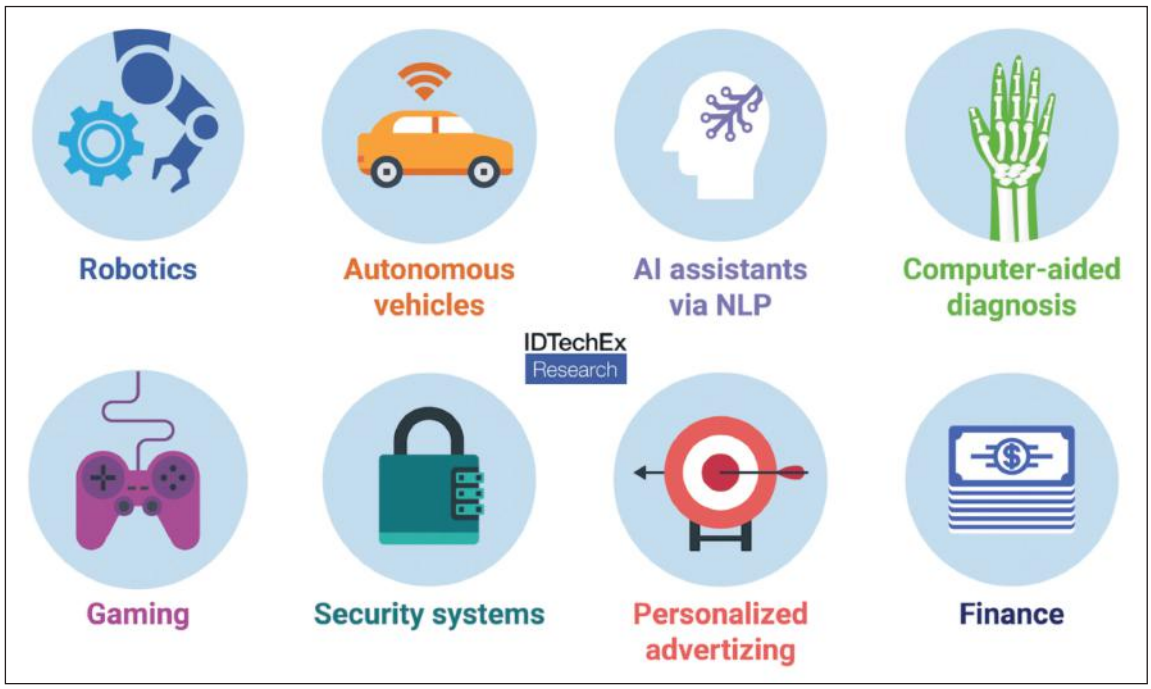
➤ The BFSI, Consumer Electronics, and IT & Telecoms industry verticals are forecast to lead the way in terms of revenue generated by the sale of AI chips up to 2033. Source: IDTechEx.

➤ The differing characteristics between AI at the edge and AI in the cloud. An edge computing environment is one in which computations are performed on a device – usually the same device on which the data is created – that is at the edge of the network (and, therefore, close to the user). This contrasts with cloud or data center computing, which is at the center of the network. Source: IDTechEx.

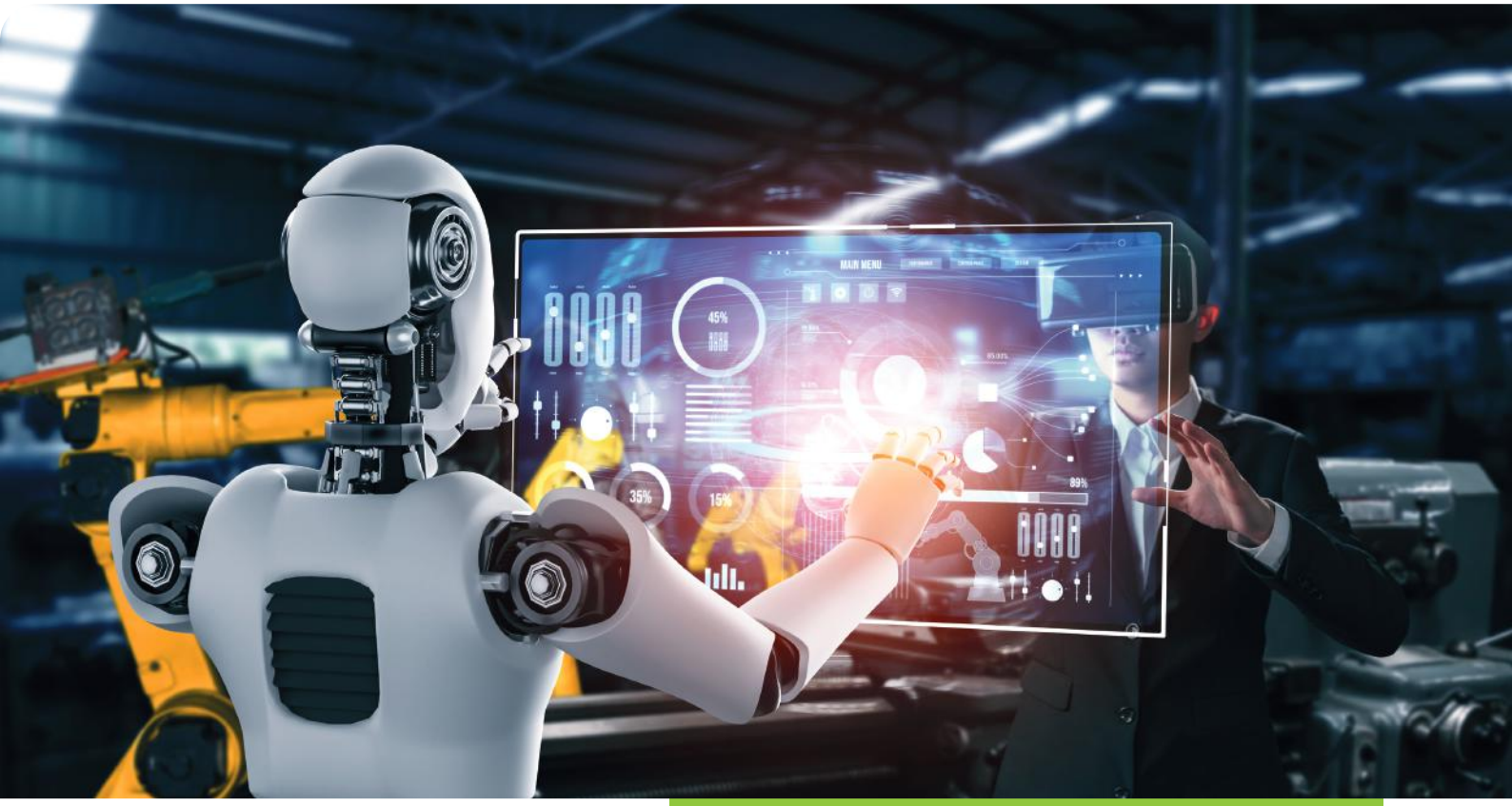
While the first instance of a virtual assistant, it is not the only one, with Microsoft Cortana and Amazon's Alexa also now widely known. Voice assistants effectively showcased the early potential of AI as applied to consumer electronic devices, where they were (and are) able to provide hands-free control and a greater range of accessibility options for users.

Since then, AI has been deployed across several different areas within consumer electronic devices to improve the user experience. Personalized recommendations are given through smart TVs and music platforms via the analysis of consumer behavior, allowing both the end-user to receive an experience tailor-made to their own tastes, while also increasing advertiser revenue.

In recent years, AI-capable smartphone chipsets have become fairly ubiquitous in leading products of major smartphone brands.



➤ AI chip applications. Source: IDTechEx



The image and object detection capabilities of these chipsets has enabled a more robust approach to photography and video on mobile phones, where camera settings are automatically adjusted according to objects in frame, and objects are able to be deleted/adjusted in post.

In the Banking, Financial Services, and Insurance industries, AI is already being put to effective use in high-frequency trading; GPU's currently account for the majority of the market for cloud AI, where the ability to parallel process allows for the handling of large amounts of data with effective latency masking (where stalled threads are switched for threads that have data, so that computation occurs concurrently).

The hardware capabilities have enabled fraud detection in high-frequency trading, where large volumes of financial transactions are analyzed for patterns that could indicate fraudulent activities. In addition, chatbots and virtual assistants are being used across industries (not just BFSI) at the customer end, where they handle initial enquiries and automate routine tasks, improving operational efficiency for the companies that utilize these tools.

These latter examples show that the benefits of AI to companies and consumers are not mutually exclusive; personalized recommendations enhance the user experience while also bolstering company revenue via more effective marketing. In another vein, the use of AI to streamline processes via automation (as well as assist with product design based on user feedback and the analysis of potentially unstructured data) represents long-term cost-savings for companies that can identify areas of their business that can benefit from automation, and thereby free employees up for more high-value tasks. The cost savings can then have a downstream effect on product price points.

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IDTechEx envision that the next ten years will see widespread AI implementation, given the fast-paced nature of developments in software and hardware, and the potential that is yet to be unlocked by the effective use of AI tools at the operational level within most companies.

eBeam Initiative: A voice for the photomask industry during rapid evolution

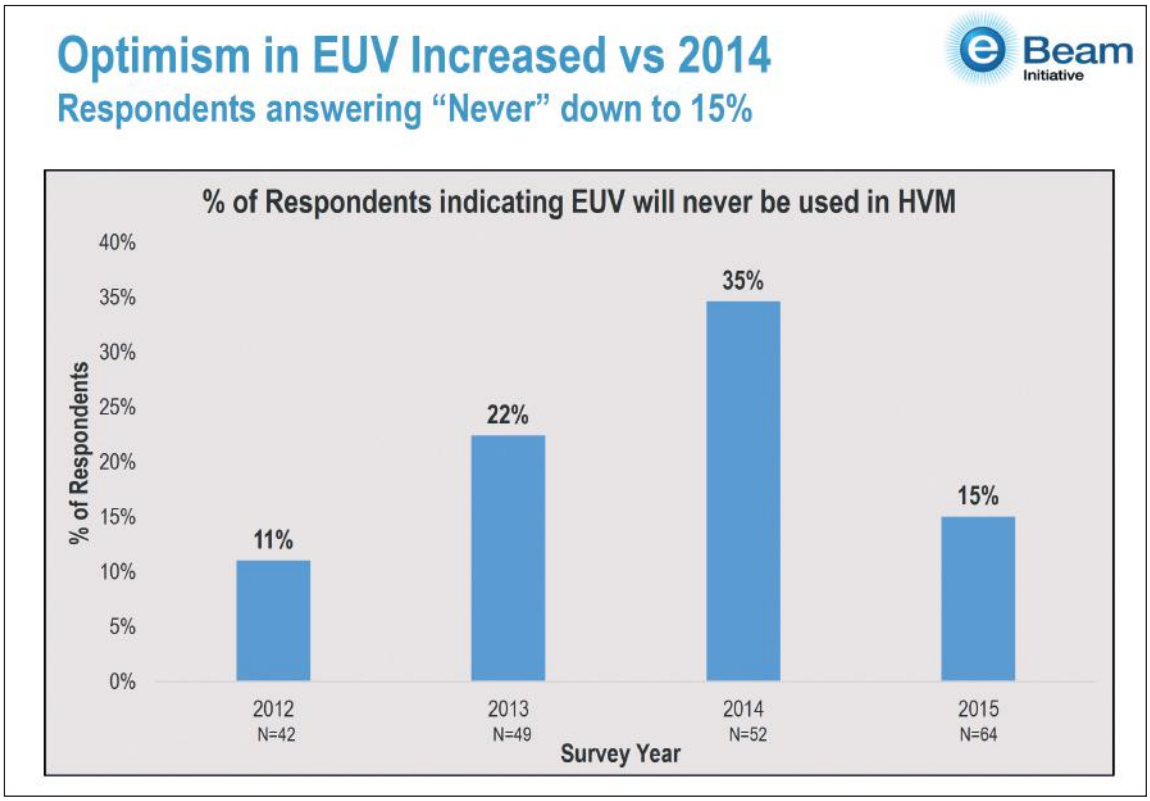
As the group approaches its 15th anniversary, the shift to curvilinear masks tops the agenda.

By Jan Willis, Co-Founder, eBeam Initiative

FOUNDED IN EARLY 2009, the eBeam Initiative is an industry group that provides a forum for educational and promotional activities regarding new design-to-manufacturing approaches that help reduce photomask costs for semiconductor devices based on electron beam (eBeam) technologies. The eBeam Initiative quickly established itself as a powerful collaborative forum for the semiconductor manufacturing community, with member companies presenting papers starting in late 2009.

While the early focus of the eBeam Initiative was on eBeam direct write (EBDW) where designs are written directly to wafer using advanced eBeam technology, the group quickly shifted to focus on the mask industry and to the technologies that could improve mask quality and lower mask cost. Historically, the mask industry has been depended upon to provide the accuracy needed for advanced nodes (though it has tended to be underappreciated), and with the scaling challenges

Figure 1: Logos of current eBeam Initiative member companies and design advisory team

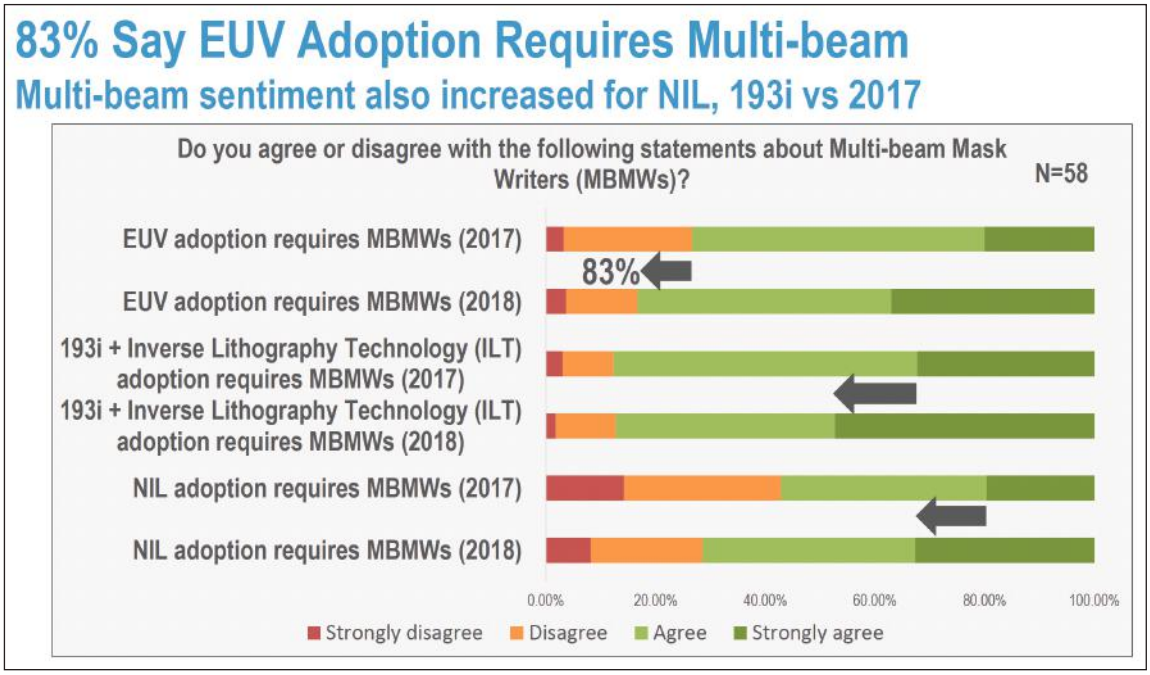


➤ Figure 2: eBeam Initiative 2015 Luminaries Survey results on the use of EUV in HVM

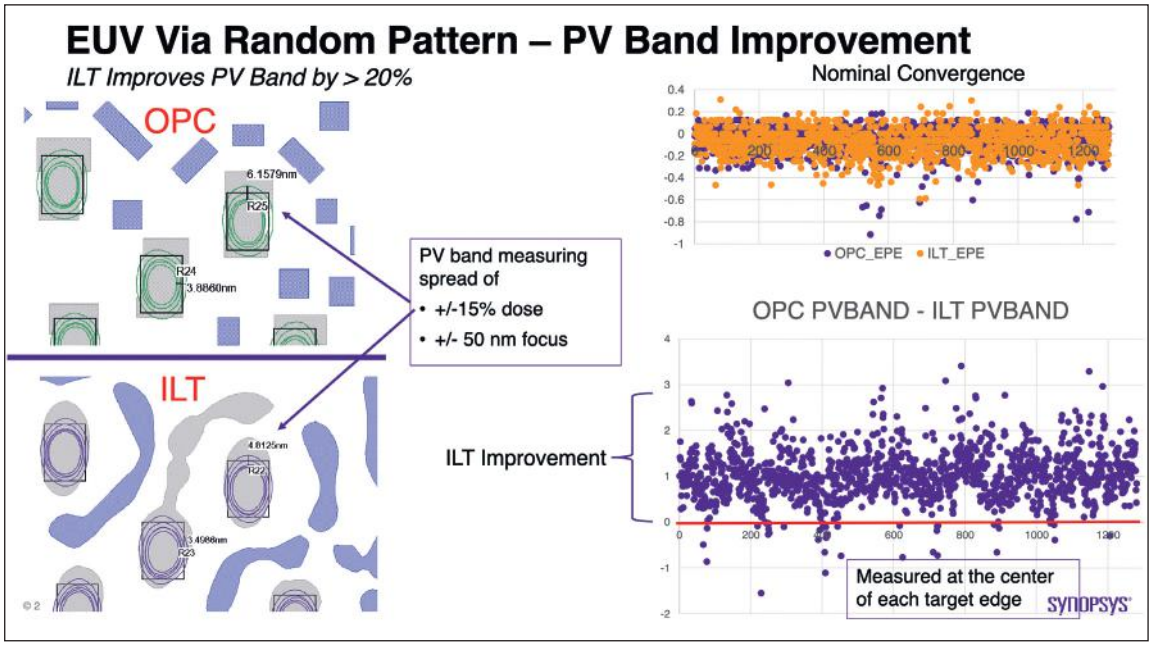
facing the semiconductor industry starting in the early 2000s, the mask industry was positioned to play an even larger role. Within a few years of its inception, the eBeam Initiative had become a voice for the mask community, helping to communicate its interests and achievements to the rest of the ecosystem.

To support the mission of education and promotion for the mask industry, the eBeam Initiative established multiple annual meetings, which take place each year during the SPIE Advanced Lithography Conference (usually held in February) and the SPIE Photomask Technology Conference (organized by BACUS, usually held in September). In the years since its founding with 20 members, the organization has expanded its membership to include more than 50 member companies across the semiconductor manufacturing and design ecosystem (see Figure 1).

Over the years of the eBeam Initiative's existence, the mask industry has seen multiple major shifts in technologies as the industry worked to keep



➤ Figure 3: eBeam Initiative 2018 Luminaries Survey results regarding adoption of multi-beam mask writers



➤ Figure 4: 2017 presentation to the eBeam Initiative on the resurgence of ILT. Source: Synopsys

advanced semiconductor node roadmaps viable as 193-nm immersion (193i) lithography was pushed to its limits and implementation of extreme ultra-violet (EUV) lithography was delayed. The eBeam Initiative's philosophy is to work closely with industry luminaries to curate technical and business insights for the mask community as it works with the rest of ecosystem to keep roadmaps in place. As the eBeam Initiative approaches its 15th anniversary in 2024, it is poised to help the mask industry make the next big shift coming for masks: curvilinear mask targets.

In the beginning: Extending 193i while waiting for EUV

As the semiconductor industry entered the 2010s, anxiety was high regarding extending 193i lithography through new advanced nodes while the industry was waiting for EUV lithography to reach maturity. The mask industry had a key role to play in providing solutions that would bridge this gap and produce masks that could meet the technical requirements of new advanced nodes and deliver them at a practical cost.

Mask customers were interested in making a balanced trade?off between the wafer quality achievable with complex optical proximity correction (OPC)/inverse lithography technology ILT)/source-mask optimization and the turnaround time of mask manufacturing. At 20-nm-and-below process nodes, both the main features of photomasks and the sub?resolution assist features (SRAFs) – which help preserve depth of focus (DOF) and critical dimension uniformity (CDU) for the main mask feature they support, but which do not print themselves – need to be increasingly complex in shape to ensure optimal patterning.

However, the number of eBeam shots required using variable-shaped beam (VSB) eBeam mask writers to create these complex features caused mask write-times – and mask costs – to increase significantly.

Technology	Write		PEB/Develop		CD Metrology		Etch		Strip/Clean		Inspection		Repair		AIMS (TM)		Phase/Trans Metrology	
	Svc	Parts	Svc	Parts	Svc	Parts	Svc	Parts	Svc	Parts	Svc	Parts	Svc	Parts	Svc	Parts	Svc	Parts
</=20nm	Adv e-b				CD SEM		Dry				Adv DUV		e-b					
40/28nm	Std e-b				CD SEM		Dry				Std DUV		e-b					
90/65nm	Mature e-b				CD SEM		Dry				Adv UV		FIB/e-b					
180/130nm	Std laser				Optical		Dry				UV		FIB					
>/=250nm	Mature laser				Optical		Wet				Visible		Laser					

➤ Figure 5: Mask manufacturing tool prognosis for 2020. Source: Toppan Photomasks

For several years, the eBeam Initiative focused its educational programming on the potential of using overlapping shots with VSB writers. One of the key solutions for this challenge was the addition of model-based mask data preparation (MB-MDP) to mask makers' technology toolkits.

Conventional mask data preparation simply fractured target mask shapes into adjoining rectangles, each representing a single eBeam shot of the same dosage. MB-MDP models enabled the use of overlapping shots that resulted in accurate mask shapes with fewer eBeam shots, and therefore faster write times.

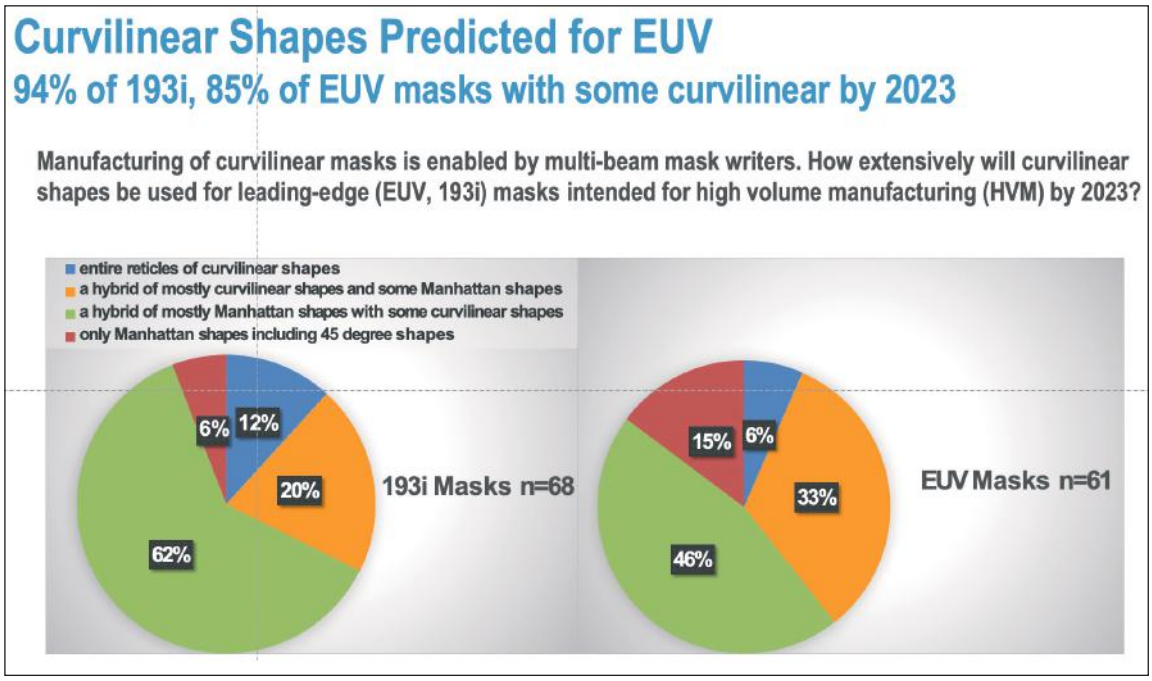
In 2012, the question of whether EUV would ever be ready for high-volume manufacturing (HVM) was still on the minds of leaders in the mask community. That year, the eBeam Initiative embarked on its first industry survey of business and technology experts throughout the semiconductor ecosystem, which has become known as the Luminaries Survey and conducted annually. The idea was to capture the opinions of the luminaries to provide early insight into key market and technology trends. In the fourth survey[1] conducted in 2015, the Luminaries' opinions on EUV provided the insight that the turning point on EUV had been reached (see Figure 2) and signaled to the entire community the need to prepare for EUV masks.

In 2012, the question of whether EUV would ever be ready for high-volume manufacturing (HVM) was still on the minds of leaders in the mask community. That year, the eBeam Initiative embarked on its first industry survey of business and technology experts throughout the semiconductor ecosystem, which has become known as the Luminaries Survey and conducted annually

A Milestone innovation: Readying the ecosystem for multi-beam mask writers

More than ten years ago, multiple companies were working on several technologies that split eBeams into multiple beams of constant size to effectively form a pixel array of eBeams to speed up mask write times and address the mask turnaround time issue. IMS Nanofabrication presented printing results of their multi-beam mask writing solution as early as the eBeam Initiative meeting at the 2012 SPIE Photomask Technology Conference[2]. NuFlare Technology followed with the introduction of their multi-beam mask writer at the eBeam Initiative's meeting at the 2016 SPIE Advanced Lithography Conference[3].

As development of EUV lithography progressed, it became clear that VSB mask writers would not support the resolution requirements of EUV, so multi-beam mask writer development became a strategic imperative for the entire industry. In the 2018 eBeam Initiative Survey[4] (see Figure 3), the majority of luminaries surveyed were signaling that the resolution needs of EUV would make multi-beam mask writers a requirement for both EUV and for 193i lithography at very advanced nodes.



➤ Figure 6: eBeam Initiative 2020 Luminaries Survey results about the use of curvilinear mask shapes

The eBeam Initiative becomes a forum for introduction of emerging trends

Over the years, eBeam Initiative member companies – and even some non-member companies – have used the forum provided by the eBeam Initiative to introduce emerging trends to the mask industry. Several times – as with multi-beam mask writer development – an eBeam Initiative meeting was the venue for the first introduction of an idea or technology.

One trend introduced through an eBeam Initiative event was the resurgence of ILT in part due to multi-beam mask writers' capability to deliver constant write time, independent of mask complexity and density. Tom Cecil, now a principal engineer at Synopsys, described this at the 2017 eBeam Initiative meeting at SPIE Advanced Lithography. His presentation[5] provided some of the very first insights on how ILT could improve EUV process variability (PV) bands as shown in Figure 4.

Another example of eBeam Initiative meetings being a forum for discussion of emerging technology was provided by David Lam, Chairman of Multibeam Corporation, at the annual meeting at SPIE Advanced Lithography Conference in 2023. Dr. Lam's presentation6 focused on new applications for eBeam direct-write technology, including internet of things (IoT) security applications. IoT security is a topic of concern for the entire semiconductor ecosystem, and it was interesting to see how eBeam technology could play a role in addressing this challenge.

A Wake-Up Call: Mask Equipment for Mature Nodes

At the 2018 eBeam Initiative meeting at the SPIE Photomask Technology Conference, Franklin Kalk of Toppan Photomasks presented a talk[7] in which he painted a picture of mask equipment shortfall by 2020, especially for mask writers at 90-nm nodes and above (see Figure 5). This became known as the "Franklin Kalk Effect."

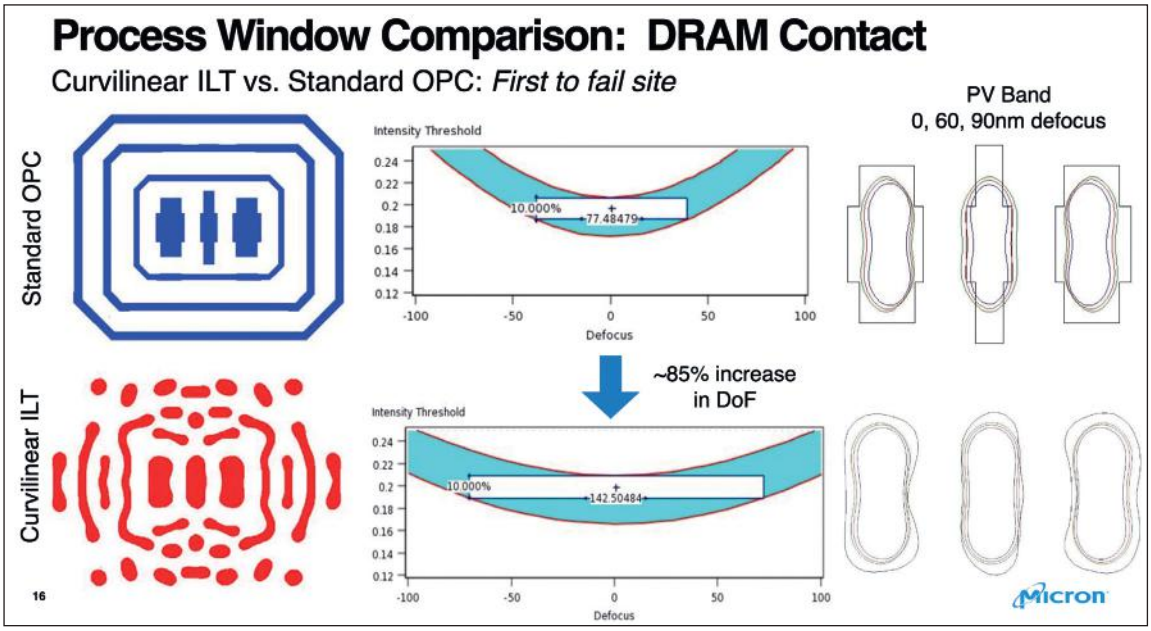
"One of the things that we didn't contemplate in the past was the resurgence of legacy products," Franklin Kalk was quoted as saying[8] at the time he was executive vice president of technology at Toppan Photomasks. "That's anything 90nm and above. The problem is that the industry is really structured to respond and chase the high end. We are not really prepared to cope with this mature resurgence."

While the mask industry was focused on the simultaneous introduction of multi-beam mask writers and EUV masks, the need for cost-effective new laser mask writers was becoming apparent. By the end of 2019, Mycronic answered the need by re-entering the semiconductor mask market with the introduction of their new SLX laser mask writers. They discussed their path back to semiconductors and their investment in deep learning in a talk at the eBeam Initiative meeting at the 2020 SPIE Advanced Lithography Conference[9]. As of the end of April 2023, Mycronic had announced orders for 40 SLX machines, validating the "Franklin Kalk Effect" was real.

The next frontier: Curvilinear mask targets

Looking forward, the course of rapid change for the mask industry seems to be running true. With EUV lithography coming into high-volume-production use and the introduction of the 3-nm process node – and the continuing development of the 2-nm and 1-nm nodes – curvilinear mask shapes are a topic of increasing focus for the mask industry. But curvilinear masks are not just for EUV.

As the non-EUV leading-edge looks for ways to extend 193i to more advanced nodes, curvilinear



➤ Figure 7: Curvilinear mask designs for advanced memory. Source: Micron

masks may be part of the solution. eBeam Initiative Luminary Surveys[10] for the past few years have pointed to the increased use of curvilinear mask features as a top trend for both EUV and 193i. In fact, the graphic from Figure 6 has been used repeatedly at conferences in the past three years to project the trend.

Nothing in nature has 90-degree angles, and manufactured shapes on the mask have always been curvilinear because of the corner-rounding physics of light. Targeted curvilinear mask features have been shown not only to print more accurately, but also to print more reliably, which is good for both mask and wafer quality.

However, until the advent of multi-beam mask writers, only VSB mask writers were available, so mask shapes were made rectilinear to be compatible with these mask writers. With multi-beam mask writers now widely deployed, there is an opportunity to take advantage of their ability to print any mask shape within the same write time and target more pervasive curvilinear mask shapes. In addition to Tom Cecil's 2017 presentation, several presentations and panels at eBeam Initiative meetings have focused on ILT and curvilinear masks. At the 2020 eBeam Initiative meeting during SPIE Advanced Lithography, Ezequiel Russell, Senior Director of Mask Technology at Micron Technology, provided evidence on the process window benefits[11] of ILT for advanced memory design as shown in Figure 7.

In a panel discussion during the virtual eBeam Initiative meeting at the 2021 SPIE Advanced Lithography Conference, Ezequiel Russell of Micron Technology, Noriaki Nakayamada of NuFlare Technology, and Danping Peng of TSMC, discussed curvilinear masks[12] and industry readiness to produce them.

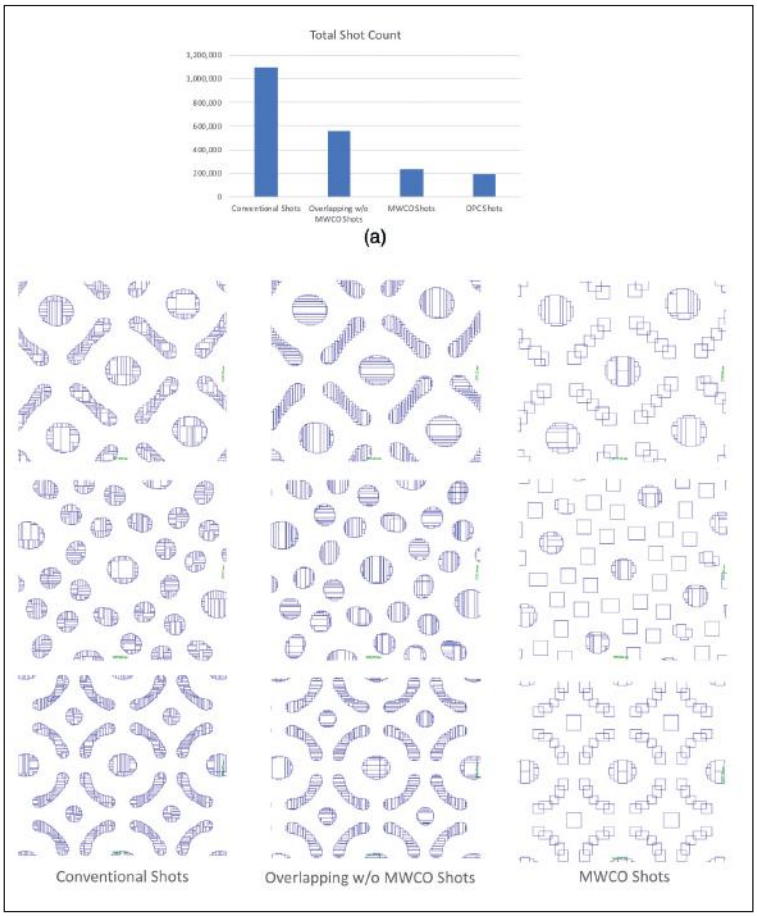
Given their potential for improving wafer quality, it was great to hear that curvilinear masks may not be just for EUV leading-edge masks or masks written by multi-beam mask writers after all. In 2020, Leo Pang from D2S introduced eBeam Initiative members to a technique called mask-wafer co-optimization (MWCO) for 193i and described it in his 2021 SPIE Journal review paper[13] on the 30-year history of ILT. MWCO marries curvilinear ILT with MB-MDP for VSB writers, using overlapping shots. MWCO incorporates overlapping shot generation and mask-wafer double simulation into the ILT process, so the output of the OPC shop is already optimized for shot count (see Figure 8).

In 2019, at the eBeam Initiative meeting at the SPIE Advanced Lithography Conference, Yu Cao, now President and Country Manager of ASML US and CEO of HMI, an ASML company, , presented on the use of machine learning[14] in computational lithography (ILT is a form of computational lithography). Deep learning and GPU acceleration play a key role in curvilinear mask making and are currently garnering a lot of attention with NVIDIA's support[15]. A new curvilinear format being developed under the auspices of the SEMI standardization process to support an optimized mask data infrastructure is a high priority for mask makers as expressed in the 2022 Luminaries Survey[16]. There's an opportunity on the chip design side to take advantage of what the mask industry has enabled for the first time in 40 years: a wholesale change in what future chips could look like by manufacturing curvilinear features. Curvilinear designs would run faster, yield better, use less power, decrease chip size and have better performance yield, too.

However, most of the chip design community is not yet aware that curvilinear manufacturing is now possible. Therefore, the eBeam Initiative is also working with the design community to encourage research in this area. The eBeam Initiative looks forward to continuing its mission of curating education and technical communication as the semiconductor industry moves toward this newest change.

Today's eBeam Initiative

Today, the eBeam Initiative includes more than 50 member companies spanning the semiconductor



➤ Figure 8: Curvilinear Masks for 193i using VSB writers and MWCO. Source: D2S

ecosystem, from small research operations to large, multi-national companies. A Design Advisory Team provides business and technical insights to myself and my co-founder, Aki Fujimura, CEO of D2S. D2S is the managing company sponsor of the eBeam Initiative. Currently, the Design Advisory Team includes John Chen of NVIDIA, Hugh Durdan formerly of Marvell, Jean-Pierre Geronimi of ST Microelectronics, Colin Harris formerly of PMC-Sierra, and Riko Radojcic, formerly of Qualcomm.

At the group's meetings, the eBeam Initiative curates technical presentations by various member companies and panel discussions of critical technical challenges, drawing ever-growing audiences of attendees at the prestigious SPIE Advanced Lithography and Photomask Technology conferences. During the COVID-19 pandemic, as conferences went virtual, the eBeam Initiative meetings went virtual as well – and drew significant participation with robust technical panels.

The group's virtual event in 2022 also provided a way to celebrate Dr. Harry Levinson[17], principal lithographer at eBeam Initiative member HJL Lithography, for being recognized with that year's SPIE Frits Zernike Award for Microlithography. At the first live eBeam Initiative meeting since the pandemic, at the 2022 SPIE Photomask Technology Conference, the group was able to honor[18] Naoya Hayashi for his many contributions to the mask industry and to the eBeam Initiative as he retired from 40 years at Dai Nippon Printing as a Fellow. The goodwill and camaraderie shown to these luminaries by their peers was a demonstration of what a group like the eBeam Initiative can provide for an industry: a gathering place, not only to share knowledge and technical concerns, but also to celebrate achievements and mark milestones as a community.

The group's website (www.ebeam.org) has become a treasure-trove of technical information, with archived presentations, videos of past eBeam Initiative events, and dozens of short videos on technical subjects and interviews with industry luminaries. The news section contains links to numerous articles and blogs commissioned by the eBeam Initiative and published in industry journals. "I think the most important thing about the eBeam Initiative is that that while it is a marketing group and has promotion as a goal, it has always been solidly grounded in curating technical knowledge," said Aki Fujimura. "It has been, and will always seek to be, first and foremost a strong technical voice for the mask industry."

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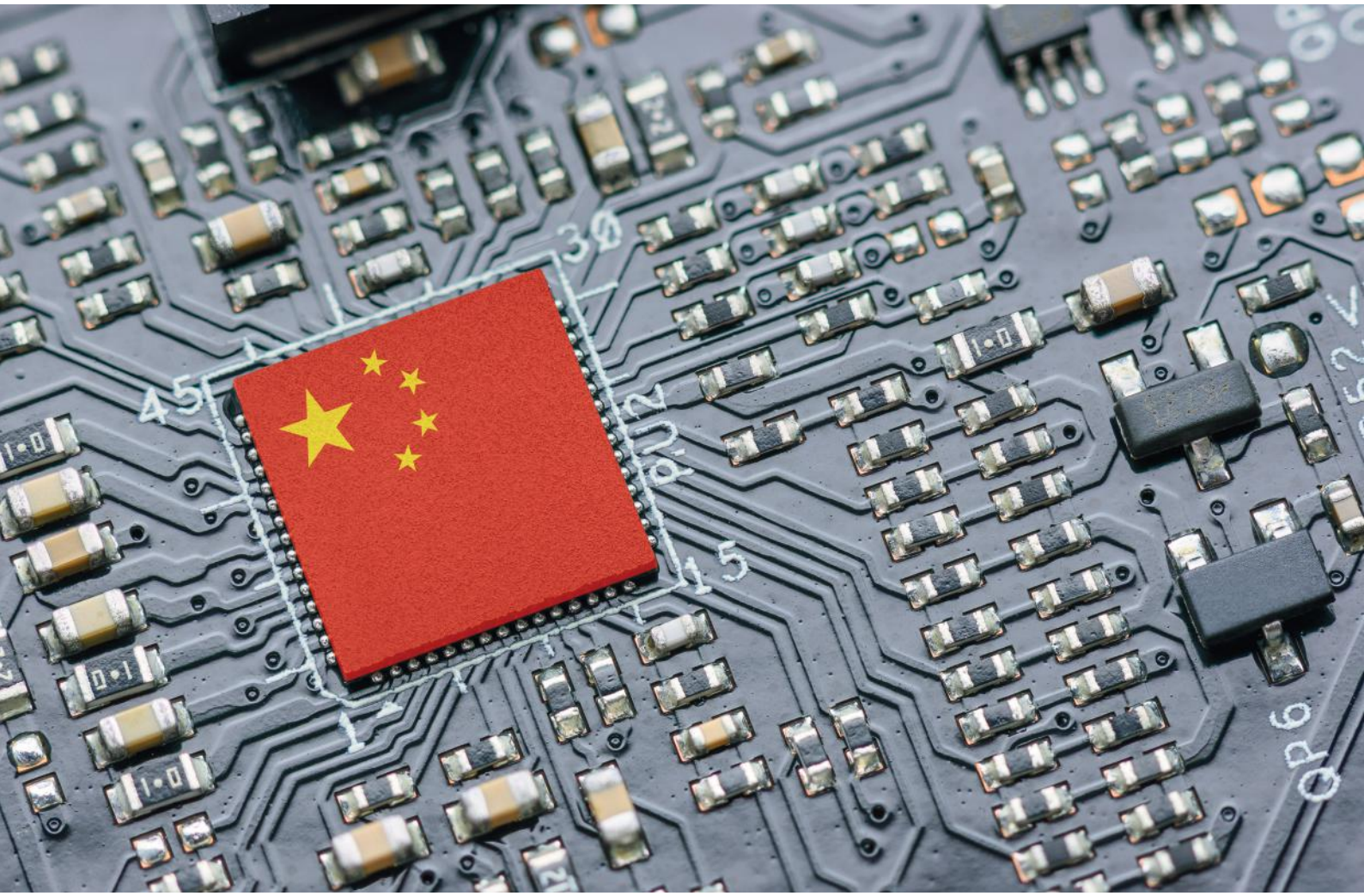


Playing politics:
The semiconductor supply chain

How should nations be looking to strengthen their semiconductor assets instead? And what's the purpose of barbed speeches, over-aggressive competition, and international tariffs in a market that seems to depend upon cooperation?

By Mark Lippett, CEO, XMOS.

"IT SHOULD BE CLEAR that no country – and even no continent – can be entirely self-sufficient. This is impossible."

Thus spoke Ursula von der Leyen, President of the European Commission, when announcing the EU's adoption of the European Chips Act in February 2022. The President was referring to the semiconductor supply chain: a complex concatenation of technologies and processes, from raw materials and extending all the way to fully produced chips with integrated IPs.

With each dependent upon others in the chain, and so many semiconductor niches to fill, placing meaningful investment in the supply chain is a huge challenge. Whereas manufacturers could once pour resources into producing chips for large, predictable, and pre-defined markets, like digital cameras, there are now so many diverse applications for chips that 'general' production is no longer realistic.

Consequentially, nations can't simply throw money at the problem. Between the speed at which

technology is advancing, the multi-year cycle required to produce semiconductors, and the shifting sands of trade restrictions and tariffs, total self-sufficiency on a national level is undeniably impossible.

So: why is this the case? How should nations be looking to strengthen their semiconductor assets instead? And what's the purpose of barbed speeches, over-aggressive competition, and international tariffs in a market that seems to depend upon cooperation?

Half a world away

To paraphrase Chris Miller's book, Chip War, a conventional computer chip could be based on blueprints designed by Californian and Israeli engineers and owned by the UK-based but Japanese-owned company, Arm. That device may be constructed in Taiwan, using specialised tools from one of five companies in the Netherlands, Japan, or back in California. After testing and packaging in South-East Asia, it's finally shipped to China for assembly.

If any link in that chain fails, the process falls apart. No final device, and no sale.

One familiar example is the automotive industry, which incidentally triggered the global run on chips as it scrabbled for supply. You may remember brands like Alfa Romeo and Audi pausing UK production with almost-finished vehicles languishing on the production line during the pandemic. Markus Duesmann, Audi's Chief Executive, specified an inability to address the "massive" shortage of computer chips" required to complete their manufacture.

In a conventional business environment, and especially one squeezed by the pandemic, a constrained supply would normally invite investment to plug the gap – just make more of what you need, right? But for a market as global, interconnected, and complex as the semiconductor supply chain, there is no financial panacea.

Money for nothing

Between the time it takes to build a fab and then produce production silicon, the best part of a decade could have passed between identifying a problem and establishing a self-sufficient solution.

During that period, technology will continue to advance at blistering pace. TSMC has announced its intention to begin producing 3nm wafers in 2026, and has teased 'key features' of 1nm chips. But most technologies, and businesses, don't rely upon these bleeding-edge technologies. So, if you spin up a new fab, it's impossible to guarantee that your target audience is there on arrival. Will you be too early, too late, or otherwise redundant by the time the facility is operational?

Beyond that, the market is changing, too. The sparring between the US and China when it comes to securing their respective supply chains has seen tariffs applied to both sides, extra funding granted to domestic ventures, and smaller countries in between being pressured to pick sides. Market forces could make certain technologies or businesses redundant or surplus to requirements by the time they can be brought to bear.

It's no surprise to see some of the biggest automobile brands in the world – BMW, Ford, Mercedes, Volkswagen, and more – continue to report frustrations eighteen months on from Alfa and Audi in the throes of COVID. Investment is being proffered, but timescales are long and the outcome may be a supply chain capacity that is overkill in some areas and absent in others. Von der Leyen's announcement specifically states that the US' $52bn CHIPS Act, and China's reported $143bn investment in its domestic semiconductor industry, have similar goals despite the political bullishness – will the outcome of these investments cover all bases?

Trailblazing

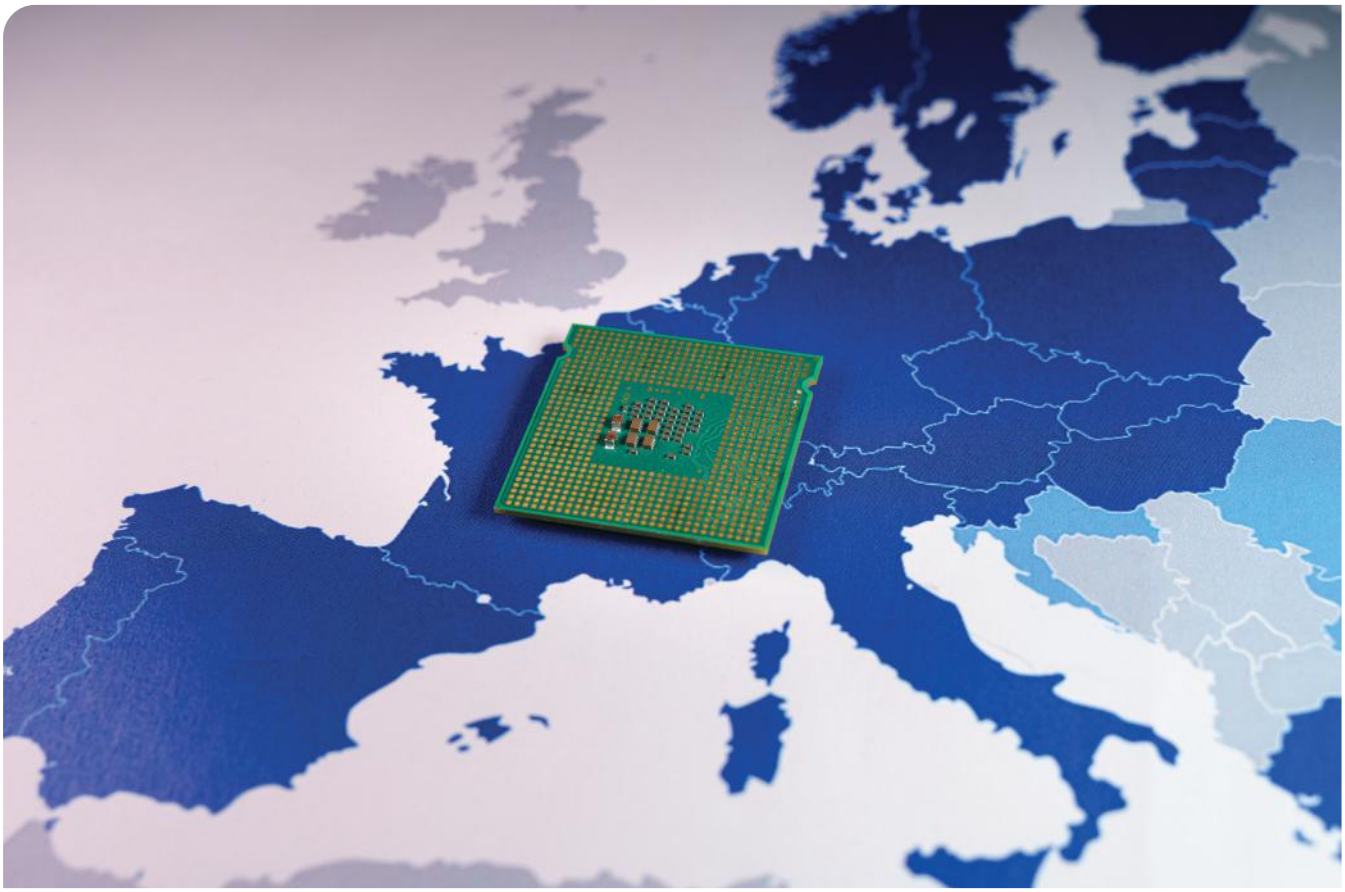
So: if independence is impossible, why such heady investment?

If intercontinental outsourcing is necessary, we must have a seat at that global table – earning that seat by bringing something unique in terms of technology or IP that other nations need. While funding in the US and China is more about getting as close to self-sufficiency as possible, for smaller nations, the goal is to synonymise themselves with a small but pivotal link in the global semiconductor value chain.

The Netherlands is one such example. With the EU's semiconductor capabilities distributed throughout the bloc, smaller nations tend to have specialisations rather than broad capabilities. The jewel in the crown of the Dutch is ASML, which has a worldwide monopoly upon the production of Extreme Ultraviolet Lithography (EUV) machines – without which the production of advanced chips is virtually impossible.

As a result, the small European country has been at the centre of a tug-of-war between China (which

The Netherlands is one such example. With the EU's semiconductor capabilities distributed throughout the bloc, smaller nations tend to have specialisations rather than broad capabilities



accounts for 15% of ASML's annual revenue) and the US (which seeks to take advantage of that supply for itself.) It has modest natural resources and chip production capabilities, and yet it is universally acknowledged as a crucial element of semiconductor production.

This is hypothetically possible for any nation – indeed, the UK's failure to deliver an investment strategy has been a point of longstanding frustration. Whether it's chemical and materials, the development of IP and components, the manufacturing of equipment, or the actual production of chips, there are a whole host of niches that countries can pursue in order to guarantee their voice at the table.

But the success of that investment goes beyond funding. You need the right environment for businesses to thrive.

Playing politics

The political rhetoric surrounding investment in semiconductors continues to reflect the twin themes of self-sufficiency and national security. With huge amounts of money being deployed, politicians need to be seen to understand and care about the semiconductor space – which leads to bullish catchphrases, and a tendency to act tough toward one's rivals.

China, for example, is often positioned as a security threat. Despite the reality that entire nations depend on trade with China for profitability, the prevailing sentiment is that opening yourself up to business with China risks an invasion of spyware. Rishi Sunak has said, for example, that China "poses a systemic challenge to our values and interests… that grows more acute as it moves towards even greater authoritarianism."

However, policies intended to ease supply chain and national security concerns are being applied far too generally. For the companies involved in the IoT (Internet of Things) – as opposed to those developing server-side systems, and the advanced computing that might be deployed nefariously – there's a frustratingly unnecessary impact upon our business that threatens our ability to remain competitive on a global stage.

Conversations between leaders of state are all-inclusive, failing to reflect the diversity of the semiconductor market. There's a need, ultimately, to move these discussions away from the politicians and towards the experts who understand the nuance.

A failure to do so perpetuates a lack of specificity and slows our progress – as the UK is currently experiencing with the stasis surrounding Newport Wafer. With far less investment capital to deploy, we must be smarter than those that content themselves with chest-thumping and sabre-rattling – we must pragmatically and thoughtfully deploy our resources where they can make the most impact, and deliver the most leverage on the global stage.

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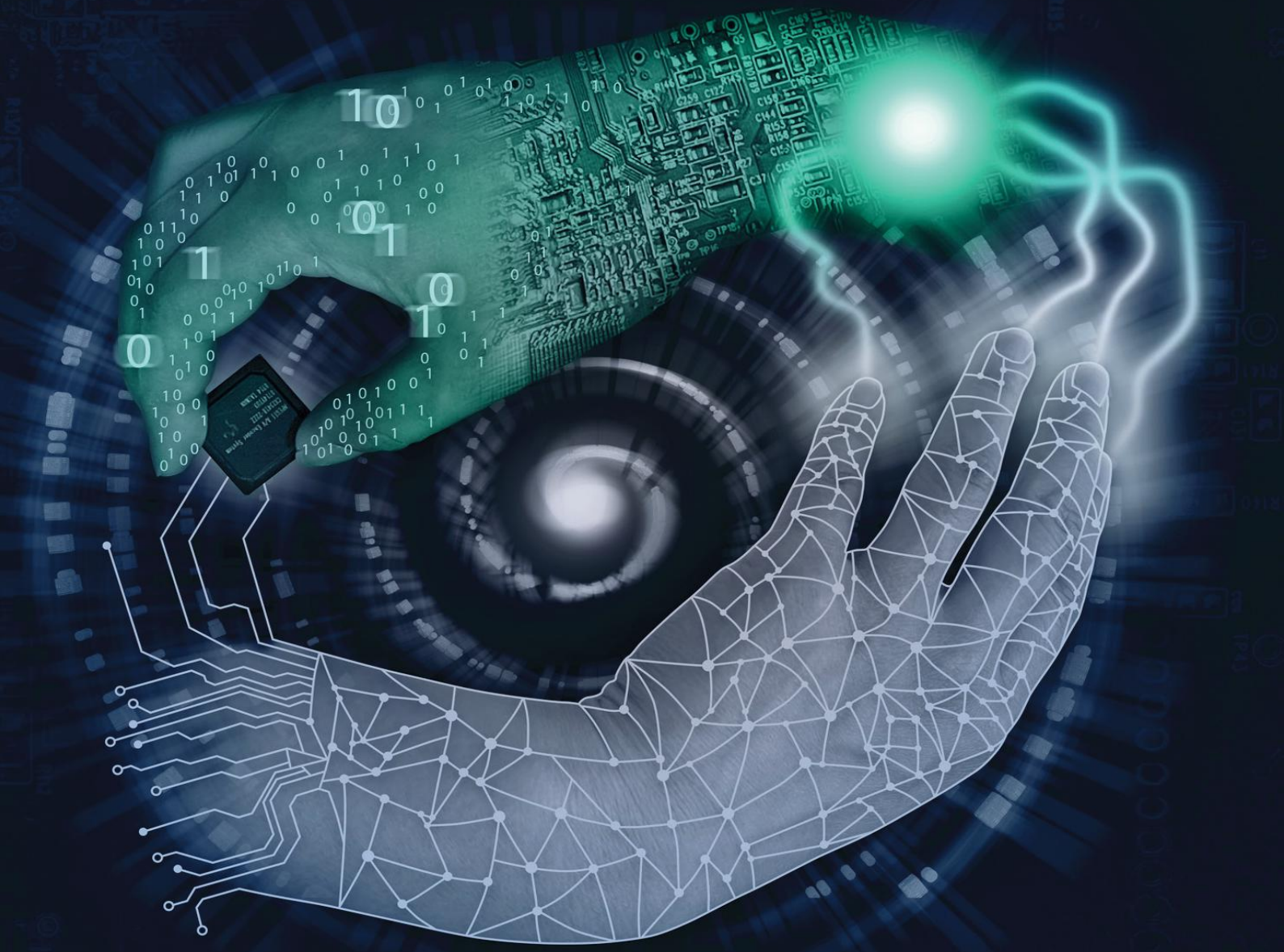


A hybrid approach optimises semiconductor process development

Keren Kanarik, Technical Managing Director in the Office of the CTO at Lam Research, and co-author of the Nature-published article: Human-machine collaboration for improving semiconductor process development, discusses with SiS editor, Philip Alsop, the organisation's research into what combination of human and artificial intelligence might best decrease the cost of developing complex semiconductor chip processes.

PA: *Lam Research recently published a paper which, in simple terms, was looking at AI and humans in terms of designing process engineering for semiconductor applications. Perhaps you can just give us a flavour of the paper and then we'll drill down into what actually went on in terms of from start to finish?*

KK: Our paper addresses a challenge, and one of the bottlenecks, really, of chip making, and that's the process engineering, the cost and time of process engineering, which is developing the processes that make the chip. And for the past 50 years, that's been done by humans, but it's taking longer and it's costing more, especially as we're moving to EUV.

And so the question that we wanted to answer in this paper is whether AI could help accelerate those efforts and reduce the cost of process engineering. So we went about trying to answer this question by running a competition, basically a game, to benchmark the different AI and different human approaches.

PA: *Intuitively, one would imagine, just the way that AI is taking over the world, that AI would automatically be better than humans because it can just process more information more quickly. But I'm suspecting that it may not be as simple as that. Is that correct?*

KK: Yeah, I like this question a lot. So, on one hand, as you say, intuitively, you think that AI should be able to handle this process engineering, tuning a process. On the other hand, process engineers like me, we know how much we rely on experience to do the process engineering. And so really, beforehand, we were sceptical of what AI could help or not help. So what the issue comes down to is that we're dealing with little data due to the high cost of data acquisition. And what that means is that we're not just asking the AI to develop a process, we're asking it to do so at the lowest possible cost. And it's that cost constraint from the little data. That's what really makes this problem interesting. Because really it wasn't clear from the beginning who was going to win.

PA: *Okay, so that was the background to how you decided to investigate AI versus human process engineering. Did you have any preconceptions at all? I know it's very difficult when you start with studies. Often, even if you say you don't, you have some kind of idea of where it might go. Did you have any thoughts or it was literally a blank piece of paper and you were going to be interested to see where it went?*

KK: Well, I came about this very objectively. The data scientists were coming to me and claiming that AI could help reduce the cost and kind of solve this problem. But as I mentioned, I was very sceptical. So that's where we came up with this idea because I didn't really know whether to believe them or not. So that's where we came up with this idea of doing the competition.

PA: *And in terms of the competitions, I understand that you developed a virtual process game. So can you talk us through it? Sounds exciting. What was involved in doing it and what was the thinking behind what you wanted to achieve with it?*

KK: I wanted to give the data scientists a chance to show what AI could do. And so originally I thought to run this game, this competition, on real wafers. And I brought up this idea to my boss at the time, Rick Gottscho. He's a co author on the paper, and he's the one that suggested that we do it virtually so that we wouldn't have to deal with the noise and the variability of real wafers, which could maybe muddy the results. So once we thought of doing it virtually, the advantages of doing it virtually became pretty apparent. We were able to run as many games as we wanted over and over again on the same process, apples to apples comparison. Actually, we ended up running hundreds to thousands of games, which really helped with the statistics for the AI performance. And then how we ran this competition. So like in a real lab, the participants would pick the recipe conditions and then it'd be run through a simulator. We'd give back the results. And so effectively, at the end of the day, it had the look and feel of a real demo.

PA: *Okay, in terms of the participants, they were the humans and then the AI, the computers. So first up, it would be good to understand how the humans came out in terms of how they performed in the game?*

KK: So we found that the humans were able to make cost effective decisions with the little data. And if you think about it, this makes sense because apparently humans have evolved to make decisions without all the information. For example, what college do we go to? What house do we buy? What are we going to eat for lunch? And we call this intuition. But in process engineering, the way I think of this is the engineers have formed some sort of mental map of how the space looks like and it helps us navigate through the processes. So in contrast though, for the humans, we observe that in the fine tuning stage, it didn't matter how much experience or whether they had a mental map in their head or not, whether they were Senior Engineer, junior Engineer, HR, it was almost as if they were shooting in the dark. They would change one or two parameters at a time and almost it appeared almost randomly.

PA: *And in terms of the contrast for the, for the computer participants, where did they fall down or and where did they maybe shine?*

KK: Okay, so the computers, fortunately, we found what I would call the opposite behaviour. So their advantage was in the fine tuning stage. And there the computers, they're able to move all of the parameters at once in such ways to find winning recipes rather quickly, as long as they were given guidance from the human where to look. In contrast, flipping it around, when the process space was too large. So at the beginning of development, they just got lost. We could see they were not making good progress towards the target. It makes sense that they lack the experience, they don't have the mental model, but they also don't have a computer map model to rule out maybe unlikely spaces or promising regimes. So the way I think of it, they didn't have this map to follow.

PA: *But as you say, once they'd been given a reasonable size of accurate data, they were better, and I guess faster in particular at coming up with*

possible fine-tuning options and then coming up with the winning recipe. Is that right?

KK: Yeah, they were able to. But, fortunately and reassuringly to us, we found that the humans are essential for that to happen. So they weren't able to do it completely on their own. Actually, the algorithms they could find, like I mentioned before, they could find the target on their own. So I just want to clarify that. But again, they couldn't do so at a low cost, which was the essence of the competition and the little data problem that we talked about. So in the end, I kind of think of the data scientists were right and they were wrong. So AI could help, but only after given guidance from the experts.

PA: *Okay. And then I believe that the next step. And fairly logical, based on what you've explained about the relative strengths and weaknesses of the humans and the AI computers, you came up with a hybrid game or scenario where you describe it as humans first, computers last. So talk us through what you did at that stage.*

KK: Okay, so we would give the computer and when I say computer, the computer or the machine or the AI, so we'd give the computer data from the human up until what we called the transfer point, along with a constrained space for them to look. And then the human effectively would step away. You can picture the human went out for coffee. By the way, I want to mention that it might look obvious in retrospect that we tried this hybrid approach of human first and computer last. But if you really think about it, we could have tried the other way around. We could have done computer first and human last, if we had assumed instead that the computer would do better at the beginning of development when the number of options is the highest. Right. But as we saw and with the concepts that we've been talking about, we chose the other way around because we could see pretty clearly that the algorithms with their trajectories, they were struggling early in development.

PA: *And just to throw in a question, did you run any of the scenarios where money was no object and did that just to see whether in that scenario, if computers, if you could spend millions or billions and billions on computers, they'd eventually come up with the right result?*

KK: A lot of the trajectories we truncated just because of time and cost, of just why keep running? But we did allow one of the trajectories to go for as long as it wanted, like you said, as if there was no cost involved. It took don't remember the exact number, but about $750,000 in order to find the process on its own. And that is relative to the expert benchmark, which was $105,000.

PA: *In terms of what you discovered, whether we're sort of re-emphasizing, that experienced humans were very important for the overall success of the process engineering, and the findings very much supported that, is that correct?*

KK: Yes. So, again, I do want to emphasise that we did find that the humans are essential. And again, being a former process engineer myself, which is why I ran this competition and was interested in this, that was very reassuring in terms of not only did we find them essential. But as you're getting at, the more experience seemed to be better. And the way you can see this, I think really clearly in the paper there's this figure three and extended data, and where we teamed up the computer algorithm with each of the process engineers and one of the inexperienced players, which you can assume is someone from HR department, let's say, and we found pretty clearly there that when you team up the computer with the more senior engineers, the overall costs were reduced. Now, there was kind of one exception there. There was one junior engineer that when they teamed up with the computer, did as well as the senior engineers. And when the reviewers were going through this paper, they joked that we should promote that junior engineer. She's doing quite well!

PA: *And in terms of the contrasting finding, you discovered or confirmed that uneducated computers are not very suited to the task. They are only really useful when they have access to, shall we say, the refined data. Is that fair to say?*

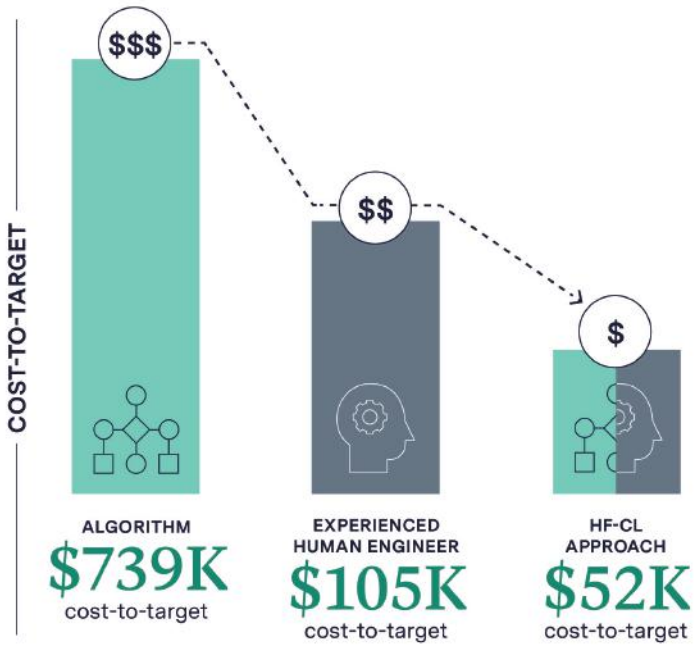
KK: Yeah, that's essentially so. Again, you saw with the example where we let the computer go until it wanted to and it cost 700 something thousand dollars, right? So the AI could, like the data scientists claim it could find the target. But again, the essence of this was could it find it at lower cost? And so in that sense, the data scientists, again, they were right and they were wrong. The computer could find the target, but it needs the guidance from the expert. And I think what this does, the results really highlight the importance of domain knowledge and experience, specifically in these little data type of problems, especially in our process engineering little data problem.

PA: *In terms of bringing that work together and optimising the chosen, if you like, or the preferred hybrid strategy. The crucial bit, and I don't know again, whether the game was able to reveal that, is at what point the humans stop, hand over their expertise and let the computer, the algorithms, take over to finish the process. Was that easy to identify?*

KK: Yeah, that's a good point. And when you're doing this hybrid strategy, how do you know when to switch over from the human to the computer? And the simple answer is don't do it too early and don't do it too late. But how do you find that point? So I would say if you wanted the absolute lowest cost, there should be this optimal point that we identified at the bottom of the V, but we identified it in retrospect, right? So if you don't know ahead of

TESTING EXPERTS AGAINST ALGORITHMS

In a controlled study, we compared the outcome and performance of three different process engineering models: **one driven by human engineers, another driven by computer algorithms with artificial intelligence (AI) and a hybrid model leveraging the strengths of both.**



The results showed that the hybrid model was able to *reduce chip development costs by*

50%

Our hybrid model uses a Human First-Computer Last (HF-CL) approach where an expert engineer begins the process and a computer algorithm completes it.

WHY HF-CL WORKS

Human engineers excel in the early stages of development because they have **prior knowledge of process trends and dependencies.**

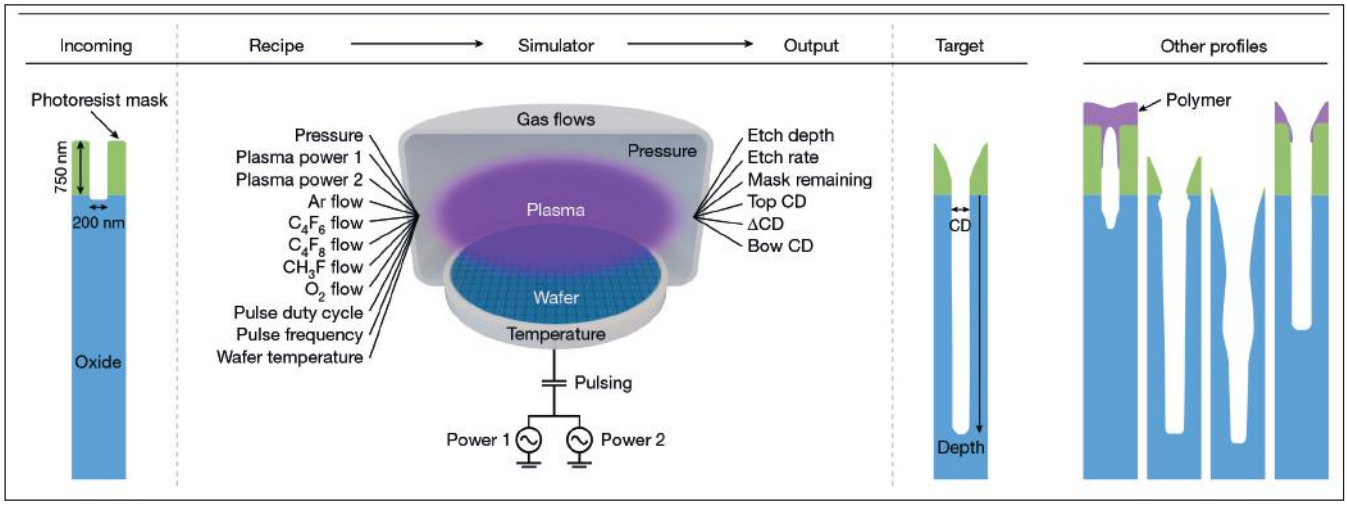
Algorithms excel in the late stages of development because they are **far more cost-efficient near the tight tolerances of the target.**

By transferring the development process at the right time in an HF-CL approach, we're able to *capitalize on the strengths of both humans and algorithms.*

SHAPING A FASTER, SMARTER FUTURE

The results of our research show great promise for the application of the HF-CL strategy in process development. By continuing to advance this field, we hope to make the jobs of process engineers easier while reducing costs and accelerating a critical link in the semiconductor ecosystem.

Visit lamresearch.com to learn more about the study and to see how else we're proving that innovation can power the future of our industry – and our world.



➤ Figure 1. Schematic of the virtual process used in the game. The input of the virtual process is a 'recipe' that controls the plasma interactions with a silicon wafer. For a given recipe, the simulator outputs metrics along with a cross-sectional image of a profile on the wafer. The target profile is shown along with examples of other profiles that do not meet target. The goal of the game is to find a suitable recipe at the lowest cost-to-target. CD, critical dimension.

time where that point is going to be, and we show that it depends on the process engineer, it depends on the computer algorithm, it will depend on the process. You may not always know that. That said, I think what we also finding is that you don't need the transition to be exactly right to still get the cost benefits of this approach. There was quite a wide range of that V of transition points that would still provide cost savings over doing a human alone.

PA: *And in terms of perhaps slightly stepping back a bit for more general findings, although this combined, this hybrid solution is the preferred one, you identified, I think, or you're suggesting that there might be some cultural issues with that sort of combination. So did that come out in the test or is this just anecdotal this is what you think might be the problems if this was enacted in the real world?*

KK: Well, first let me explain because I do, I really like that aspect of the paper hunt, this people, cultural side. Because what's happening here is we're proposing to partner humans with machines and that's foundationally changing the way processes are being developed since the last 50 years and not making that change. It's not easy to make that change. So really what we are seeing and we're watching the computers, we're watching the humans, that the AI does not behave like the humans. And there's what I'll call potential trust issues. To me, the really most clear example is that we found, and this is some in the extended data, we found that when it was handed over to the computer, the first thing that happened is often the computer would make these unusual, maybe non-traditional moves, moving all the parameters at once. And that means that the human needs to have faith that even though the computer is exploring, eventually it will hit target, preferably faster than the human would have. And there's no guarantee that that's actually going to happen.

And so I think of it like I looked at my phone the other day on the weather app and it had been predicting the rain pretty nicely. And then one day I look outside and it's raining and my phone is not saying that it's raining. And that doubt, that wonder is the AI working or not? Sometimes when there's no guarantee that there's some issues there that are known. We put some references, I did some references there. It's known that it's difficult to sometimes work with computers that way.

PA: *And did you at an even more basic level, did you get some of your more experienced process engineers just kind of say, well, I've got a whole career's worth of knowledge and I don't buy the idea that the AI can actually improve what I'm capable of doing. Was there a level of scepticism?*

KK: Yeah, that's really interesting. So I would say overall, the people, the engineers, they are actually really open to this AI help in the way in this approach that we're showing because we identified these two regimes, the rough tuning and the fine-tuning and really this confidence of the process engineer and it's really in the rough tuning phase. That's where they do well. That's where they see a lot of progress. The truth is that when they get to the fine-tuning phase, there is some frustration there, and they are more than happy to have the computer go and tidy up their work. It's like they do that 80:20 rule. They do 80% of the process, and they are happy to hand off that 20% to the computer.

PA: *In terms of where we are now with AI's usefulness or not with semiconductor process engineering, it would be good to understand where you think we are. But also talking to yourself. What is Lam Research currently doing in terms of maybe, as a result of this research, is AI becoming more important to you -where we are with AI and where yourselves in particular?*

KK: Yeah, that's good. So let me step back one moment and just explain to the audience why Lam is even interested in this study and in process engineering at all. We're in an equipment supplier, and we make the equipment that makes the chips, but we need to show our customers, the chip makers, that these processes work, that our equipment is capable of doing that. And so we have a whole bunch of process engineers in the labs working on this, and that's why we're at the front line. So that's why Lam's interested in it now, and that's why we did this study. In terms of using AI to help that process engineering, it's important to Lam, but really it's important to the whole industry. We just happen to be at the front lines using this AI. We believe this is in its infancy. We're just getting started. We believe this paper is representing what we see as the beginning of the use of AI in process engineering.

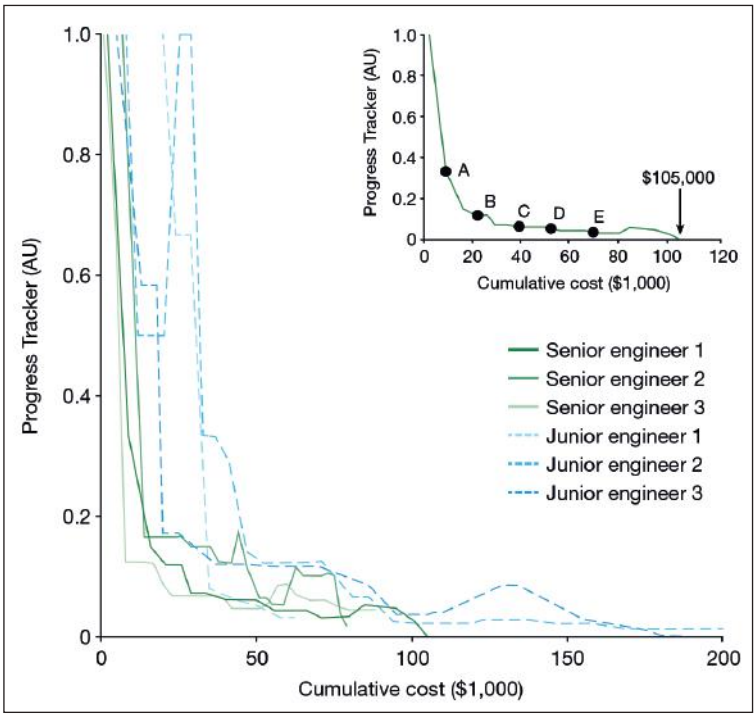
I also want to give just a little context, perhaps for your audience. When you build a chip, you first have to design it, and then you go in and physically build it. The designing part that has already been computer aided and even using AI for decades, actually, at least computer aided - the design part. But just because you can design a chip doesn't mean you can make it, right? So this paper really is focusing on the making part, and that process engineering, developing the process to physically make the chip. And that, I believe we are just getting started. And that's what we believe this paper is representing.

PA: *In terms of you said getting started, the obvious question might be, where do you think and I know it's a bit of a sort of crystal ball gazing, but where do you think AI might get to? And I'm wondering, we mentioned the little data problem. Is it just a question that if you can run machine learning algorithms, for example, and just absorb vast amounts of information and real-world examples, and once all that data has been absorbed, then AI takes over. Or because there are, as I understand it, so many variables in every time you're designing a process to manufacture a chip, that it's almost impossible that a computer will ever be able to contemplate all the different nuances. And we're back to a human's experience where they will just instinctively know what to do, where a computer won't be able to learn what to do?*

KK: Yeah, I think you're actually hitting on something important here that's been brought up and we've debated it ourselves. So I would say this - I'll give you a couple ideas that we've thought through in this debate. So you're asking if we had all the historical data in the world, all the processes out there, would that even help? Right. The thing is that even if you had all historical data, it doesn't mean you have enough data in the tiny little corner of the process space that you have of interest. And I'm not sure that everyone realises this, but every process is different in some way. It's a different stack or it's a different tool to run on. And so, for example, if you ran the exact same process recipe three years ago and then you run it today, you'll likely not get the same exact result. Because what's happening is there's all these latent you mentioned lots of variables. There's latent variables, there's hidden variables. And so we believe that at the end of the day, even as much as the AI will help, that there will always be a little data problem, to some extent at least, and in the limit of tight tolerances and that the data is costly.

PA: *And presumably the industry is moving so fast as well, so we've got more exotic materials being introduced and other innovations. So, again, that's a problem because again, when that starts happening, then the AI is back to square one. It's got no reference information, it's back to human. If I understand it, you think AI has more of a role to play, but it's never going to be able to replace that human experience because it just will never be able to absorb the required data sets. Is that right?*

KK: So I would say that the algorithms I think there's relative to what we published in the paper, I do think there's definitely room for improvement. Definitely there's some more teaching you can do to the AI, but I do agree with what you're saying, is that first of all, there's a bunch of new processes with new materials, but I would even go so back as old processes. You think you've done a mask, open etch



➤ Figure 2 Game trajectories for human engineers. The trajectories are monitored by the Progress Tracker as defined in Methods. The target is met when the Progress Tracker is 0. Trajectories of senior engineers are in green and junior engineers in blue. The trajectory of the winning expert (senior engineer 1) is highlighted in the inset, showing transfer points A to E used in the HF–CL strategy. AU, arbitrary units.

before and you think you've done it for the past 50 years and you get a new one and it's almost like you have to do it again. Although you can transfer some of the humans, transfer some of their experience, but then again, you have to still do some amount of process engineering to dial it into whatever new stack or new tool it happens to be on next. So somehow we still have to do it over and over and over again and so will the computers.

PA: *In terms of the hybrid, the human first, computer last, it would appear to be the main benefit is financial? You can hit the object target for the optimised cost if you like or the lease cost, whatever. Is that the main benefit? And did you compare the costs of doing human only and computer? Well, we found out the computers only ended up costing an astronomical amount. But were there other benefits that accrued alongside just the purely financial one?*

KK: Yes, in the paper we did focus on the financial one, which is the cost reduction, the cost savings. But along with that there is a really important benefit which is the time reduction that goes along with that cost reduction and with how fast this chip industry is evolving and changing that, speeding up that cost, I mean that time reduction to innovation effectively that's really important as well. You might even argue more important.

PA: *Were you able to put vague percentages or numbers on either the cost optimization, how much you might be able to save or in the time?*

KK: That's good. Off the top of my head, I would say if you reduce the cost by half, you might reduce the time by half because you're doing that many fewer. We did have a cost function that included number of experiments and the batch of experiments but roughly speaking you would translate that to time.

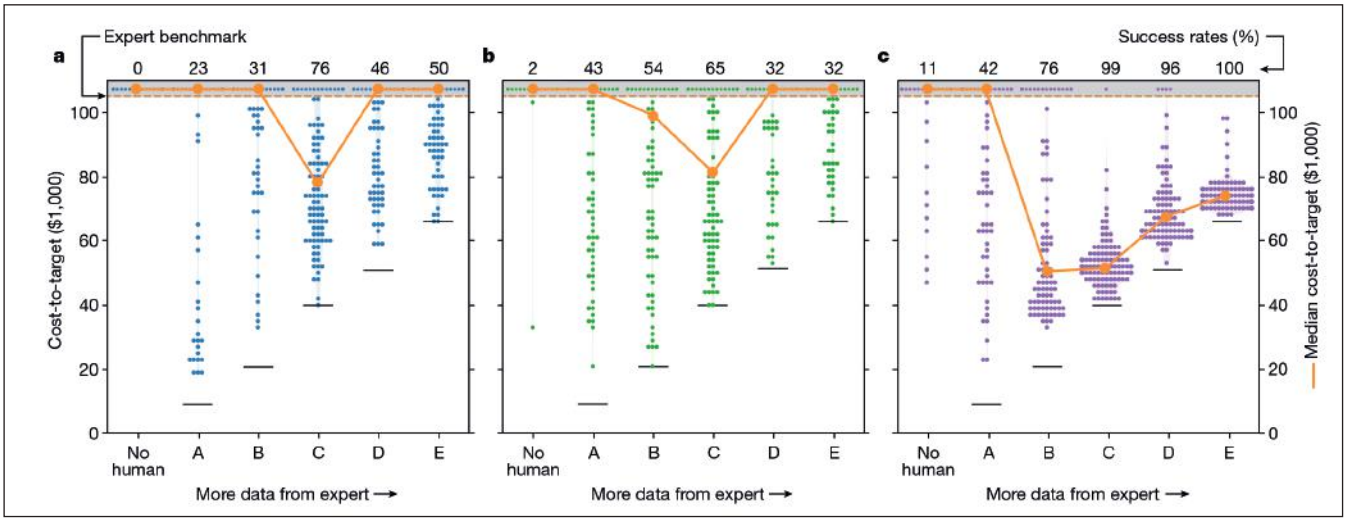
PA: *In terms of moving from a virtual process game to real world, is that the logical next step? Is that something you're looking at or does virtual give you all that you need - thoughts as to what's the next step I guess having done in the virtual process game?*

KK: Yes, so actually this is already happening in the real world. We are using this AI in the process engineering with real processes at Lam with good results. And that's partly when you asked the question before about how the humans were accepting. They are excited and for me it's exciting to see it working. I would still call it infant stages, but it is being used.

PA: *I know you've obviously published the paper, so it's in the public domain, but have you worked with any of your key customers, partners to share this knowledge and had any feedback from them as to how confident they are and that what you're doing is going to make a difference for them, chip manufacturers and stuff? Or is it too early to be doing that work?*

KK: Well, I will say we have been talking to customers and they also seem to be quite excited about this work.

PA: *In terms of the future. I guess one other variable I didn't ask about is particularly, I suppose, to do with cost, because quantum computing is on the horizon. And I'm just wondering, might there be a future where the processing power is improved so astronomically, and the price of it has come down correspondingly? That what you've discovered in this paper might be somewhat challenged because the financial equations changed or because of the problems we've outlined just absorbing all the data sets, or lack of them, that computers will always*



➤ Figure 3. Cost-to-target using the HF-CL strategy. a–c, Results for three algorithms: Algo1 (a), Algo2 (b) and Algo3 (c). The 'no human' results are without any help from humans, as reference. Columns A to E are the transfer points shown in Figure 2. Each dot represents one of 100 independent trajectories. Cost-to-target is the sum of cost from both the human and the computer algorithm; orange lines indicate median cost-to-target; dots aligned at the top exceed the cost-to-target of the expert alone ($105,000); black horizontal lines represent the cost of data provided by the human.

struggle? So there will be this hybrid solution that always wins out.

KK: Well, I think anything that a computer can go faster and more powerful will help if we're using computers. But I think really the main challenge for the computers is kind of a little bit what you've alluded to is, can we improve them from what we've already published that they can do? How much room for improvement is there in these algorithms to, for example, we mentioned in the paper some future directions where perhaps we could encode domain knowledge to reduce the costs even further. So how far can that go? I think that's what I'm looking for from the direction of computers in this problem.

PA: *Just as a matter of interest, do you have any specific roadmap or time frame as to various stages of this? Or is it very much you're doing the research and as and when something interesting, important crops up, then that will be taken out and used appropriately, or are there any sort of deadlines.*

KK: My boss would say, go as fast as possible. That's what I would say. We're testing it out.

I can also recap just a couple of the main points. It really is about process engineering, which I hope through this paper, the audience can appreciate just how critical process engineering is for making chips. Because without that process engineering, the phones wouldn't work and the chips couldn't be built. And that's not always really visible to most people. But the cost and time of designing those processes, those are increasing. And that's really what this paper is trying to address. I also wanted to emphasise that this problem that we're talking about, this process engineering problem, although Lam is interested in it, as with our equipment, it's not really just a problem for Lam. It is a problem for our whole industry. And our role in it is that we're just super laser-focused on the process engineering so that our equipment could work for the chip manufacturers. And then lastly, emphasise again that the human engineers continue to be essential for the chip making and for the creation of semiconductor chips. Although this hybrid approach does alleviate some of the more tedious aspects of process engineering.

And as we talked about, while the AI application to the process engineering, it's still in its infancy, we do think the results point us to a path to foundationally change the way processes are developed in semiconductor chips.

PA: *One thought occurred to me, and again, it might be a non-starter, but the way the industry is moving so that where we might characterise it, perhaps unfairly, but where there were slightly smaller amounts of process, there were mobile phones, computer chips and stuff. But the suggestion is that the future of the semiconductor is many more, but small, if you like smaller sized markets. So will this have a particular role to play there? Because rather than designing something that you're going to bang out vast amounts of chips for a mobile phone or whatever, you're going to have relatively shorter runs. Therefore, the process engineering development is even more important that you can optimise or minimise the cost of that. Is that fair to say?*

KK: Yeah. So I would say anywhere that you need a process engineer, that this has the potential to impact and provide cost savings and help develop that process just that much faster and that much less cost. So I think what we found even in this process here, we had the high aspect ratio, plasma etch case study that wasn't the most complicated etch out there and we saw that it applied to that etch.

So I do think that there's plenty of room for it to apply to kind of the more day to day process engineering for wherever process engineering is needed. This point, if you go to too difficult of a process, you need to make sure that the human can direct the computer. Because if the human can't even figure out where to go, it's not clear the computer will either.

How advanced cleaning helps achieve optimal wafer yields at advanced semiconductor nodes

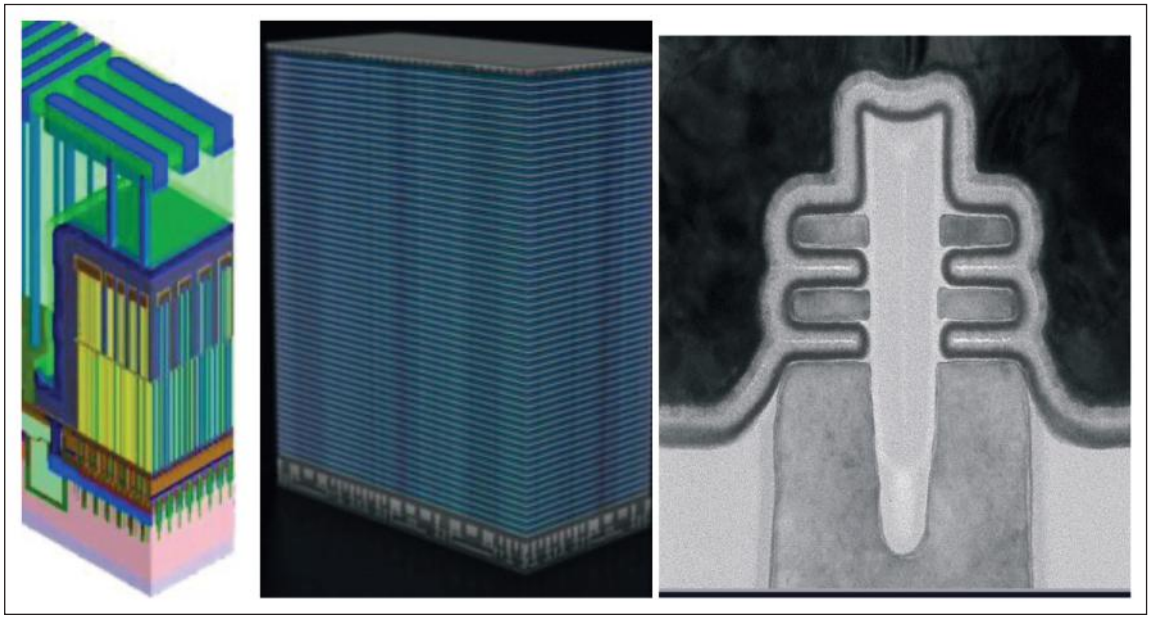
With the introduction of SAPS and TEBO technology in a megasonic system, semiconductor manufacturers now have new tools in their fight to achieve optimal wafer yields.

By ACM Research.

SEMICONDUCTOR chip features continue to shrink at a rapid pace. Dynamic random access memory (DRAM) manufacturers are now manufacturing 16GB chips in the 12nm range with an aspect ratio of 60:1 in the capacitor. NAND structures are reaching 232 layers with an even larger etch aspect ratio, and logic is moving into the first phase of gate-all-around (GAA) transistors at the 3nm node.

As these structures continue to shrink, the process technology becomes more challenging and removing contamination and random defects becomes extremely difficult. With minimum feature sizes and film thicknesses reaching the 10nm level (100 Ångstroms), a particle as small as 1nm (10Å) can be a killer defect causing a transistor not to function. Removing particles and other contaminants to reach acceptable yields in the manufacturing process will be one of the major process challenges for semiconductor manufacturers as chip features continue to shrink to below 10nm.

Wafer cleaning is sometimes considered low-tech in a semiconductor fab filled with advanced lithography, etch, and deposition equipment. However, the need to remove particles and other contamination that could change transistor characteristics, as well as contact and interconnect line resistance, has elevated wafer-cleaning technology to a higher level in the semiconductor manufacturing process. In fact, cleaning technology is now one of the most critical components of a semiconductor manufacturing line. In leading-edge factories, there can be more than 200 cleaning steps in the manufacturing process. Before each lithography process, thermal process, or deposition step, the wafer is typically cleaned to remove any defects and improve the material's surface quality. Cleaning systems have evolved beyond hand-operated dip-and-dunk systems, which use chemicals poured from bottles followed by a physical scrub/spray, as well as megasonic tank particle removal. Today's systems comprise



➤ Figure 1. Advanced Process Technology DRAM cell, NAND structure, and forksheet transistor (Source Micron Technology Day, IMEC)

sophisticated process equipment that accurately measures out cleaning chemistries and removes microcontamination and defects after etch, lithography, chemical mechanical planarization (CMP), and other semiconductor manufacturing steps. Conventional particle-removal cleaning is challenged by today's advanced technologies' smaller and finer features. The pressure levels needed when using a spray cleaning technology are too strong; the physical force will damage the surface features of the transistor and capacitor structures, potentially knocking them off the wafer. Spray technology also cannot reach into the trenches with deep aspect ratios.

Conventional megasonic cleaning also struggles with the small, deep features, as the energy cannot reach deep into the structures evenly. Conventional megasonics cannot guarantee even surface coverage across the wafer, which often results in insufficient cleaning in some wafer areas. This leads to yield loss. These processes can also create surface roughness and material loss, which could significantly impact advanced device performance when 1 Å is crucial for chip performance. Essentially, megasonic wafer cleaning and conventional cleaning approaches have reached their limits and can no longer remove the smallest killer defects without damaging the features on the chip.

Removing particles from today's patterned semiconductor is becoming a focused science. As chip features continue to shrink and move into the third dimension, the brute-force cleans using brush scrubbers and spray scrubbers, ultrasonics, and megasonic energy are evolving to avoid damaging the structures. New single-wafer cleaning process technologies address the critical nature of cleaning the current and next generation of patterned structures on the semiconductor chip.

The NEXT generation cleaning technology

To address the cleaning challenges facing semiconductor equipment manufacturers, ACM Research developed Smart Megasonix™—a smarter, more innovative suite of single-wafer wet cleaning technologies that can be used at existing and future process nodes across the range of processing steps to achieve more thorough, comprehensive cleaning without damage to device features. These proprietary technologies can control both the power intensity and the distribution of megasonic cleaning.

Two key technologies have been introduced to enhance the cleaning abilities of megasonic systems. The first is Space Alternated Phase Shift (SAPS™) wafer cleaning technology. The SAPS technology is an advanced megasonic process that uses alternating phases of megasonic waves in the gap between the megasonic transducer and the wafer. The SAPS technology moves or tilts the transducer while the wafer rotates, delivering megasonic energy uniformly across all points on the wafer, even if the wafer is warped. This ensures optimum energy delivery, which, when combined with the proper dilute chemistry, creates the right environment for removing wafer defects. The precision of the SAPS technology enhances the mass transfer rate of dislodged defects and improves efficiency of the system's particle removal. Implementing SAPS results in faster throughput and more efficient particle removal, which translates to higher yield as well as lower wafer cost of ownership.

➤ New single-wafer cleaning process technologies address the critical nature of cleaning the current and next generation of patterned structures on the semiconductor chip.

The second innovative development in megasonic technology is Timely Energized Bubble Oscillation (TEBO™). Conventional megasonics use cavitation to generate bubbles that are the active cleaning energy. In a conventional system, these bubbles can implode or collapse, which can then damage finely patterned features. With TEBO, the cavitations become stable without bubble implosion or collapse. The result is successful defect removal without damage to sensitive patterns such as high-aspect-ratio capacitors in DRAM and high-aspect-ratio trenches and holes in 3D NAND. The technology also removes defects from advanced fin field-effect transistor (FinFET) and GAA structures. As chip features shrink and aspect ratios increase, removing etch and photoresist residue as well as CMP particles becomes more challenging. Features are more fragile, and the atomic forces causing the defects to adhere to the wafer are significantly stronger. New clean chemistries and mechanical methods for defect removal that do not damage critical features are needed for advanced processing. With the introduction of SAPS and TEBO technology in a megasonic system, semiconductor manufacturers now have new tools in their fight to achieve optimal wafer yields.

The benefits of AI to the semiconductor industry supply chain

A Q and A with **Skyler Chi, Head of Enterprise Accounts, Exiger,** discussing the impact of AI on the microelectronics manufacturing supply sector, the benefits it can provide and offering some advice as to how best to integrate the technology into supply chain operations.

SS: *How is AI impacting the microelectronics manufacturing sector in terms of supply chain management / operations?*

SC: AI is revolutionising everything from normal data entry, to art, to just about all our jobs and functions. The microelectronics space is no different as AI and machine learning have also taken certain manufacturing sector processes by storm by streamlining the supply chain management and operations. For example, AI-powered supply chain management software has recently been deployed to assist manufacturers in monitoring and optimising their entire production process, from procurement to logistics.

On the risk side, AI is automatically scouring billions of open-source records per day and stitching together disparate documents to automatically illuminate previously opaque supply chains. Through this evolution, AI has enabled manufacturers to capture and analyse data in real-time, allowing them to make incredibly informed and optimised decisions that increase efficiency and reduce waste (while increasing time to value).

SS: *What benefits can AI technology provide to the microelectronics manufacturing sector supply chain? Are there any drawbacks?*

SC: AI has clearly provided several benefits to the microelectronics manufacturing sector's supply chain, including predictive maintenance, demand forecasting, quality control, and inventory optimisation. Predictive maintenance algorithms have today been deployed to prevent equipment downtime by identifying potential problems before they occur. AI-enabled demand forecasting algorithms provide accurate sales predictions, allowing manufacturers to optimise inventory and production planning. And AI-powered quality control systems analyse data from sensors and cameras to detect defects in real-time, reducing scrap and rework. Finally, AI has helped optimise inventory management by predicting demand, reducing waste, and avoiding overstocking.

The main drawback of AI technology is the potential for cyber-attacks or data breaches. Not to mention AI appears to give incredibly false answers with confidence. Or, as I prefer to tell my team, "Just

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assume in these early stages that the tools are often wrong, but never in doubt". Like any tool, it's important to rely on them but to check and challenge their outputs in the same way that we would any other tool. AI in many ways is not as accurate in the same way that, today, we rely on calculators to add 2+2. Since AI algorithms rely on vast amounts of data to learn, any compromise of the data could have significant consequences for the entire supply chain. Additionally, the integration of AI technology requires significant investment, training, and organisational change, which can be a challenge for some manufacturers and software companies.

Quality control systems are relatedly enhanced as they allow users to immediately analyse vast (read: trillions) of data records from sensors and cameras to detect defects in real-time, reducing scrap and rework across all manufacturing sites

SS: *How do microelectronics manufacturing businesses utilize AI technology in their supply chains?*

SC: Microelectronics manufacturing businesses are using AI today in various ways to optimise their supply chain management and operations. For example, manufacturers use predictive maintenance algorithms to minimise equipment downtime and optimise maintenance schedules. They also use AI-enabled demand forecasting algorithms to predict sales and optimise inventory and production planning. Quality control systems are relatedly enhanced as they allow users to immediately analyse vast (read: trillions) of data records from sensors and cameras to detect defects in real-time, reducing scrap and rework across all manufacturing sites. Finally, AI has helped optimise inventory management by predicting demand, reducing waste, and avoiding overstocking while highlighting risk of disruption in near-real time.

SS: *Do you have any tips/best practice advice on how microelectronics manufacturing companies should integrate AI technology into their supply chain operations?*

SC: In short, to integrate AI successfully into any system or supply chain operation function, microelectronics manufacturing companies can consider some of these best practices: Start with a very clear understanding of the business objectives and identify the specific supply chain processes that AI technology can improve. Without a roadmap, most evolution is destined to fail at the implementation stage.

Firms can and should develop a data strategy that defines the data requirements, data sources, and data governance policies needed to support AI-powered supply chain management. As noted above, garbage in means garbage out and strategic and tactical training of AI models is critical to accuracy. Companies can also choose to partner with technology vendors – like Exiger who have worked in the AI and supply chain management space for over a decade - with a track record of developing and deploying solutions in the microelectronics manufacturing industry.

Companies should ensure that all algorithms and training models are transparent, explainable, and auditable to build trust with stakeholders and ensure regulatory compliance. A single inaccurate response can immediately destroy all trust across the teams. Lastly, companies should look to train employees to use any AI supply chain management tools effectively and subsequently monitor their performance regularly to identify areas for improvement. As noted above, "just assume in these early stages that the tools are often wrong, but never in doubt".

CLEAN ROOMS

GAS DELIVERY SYSTEMS

INSPECTION SYSTEMS

VACUUM EQUIPMENT

ETCH

GAS PURIFIERS

PLASMA TECHNOLOGY

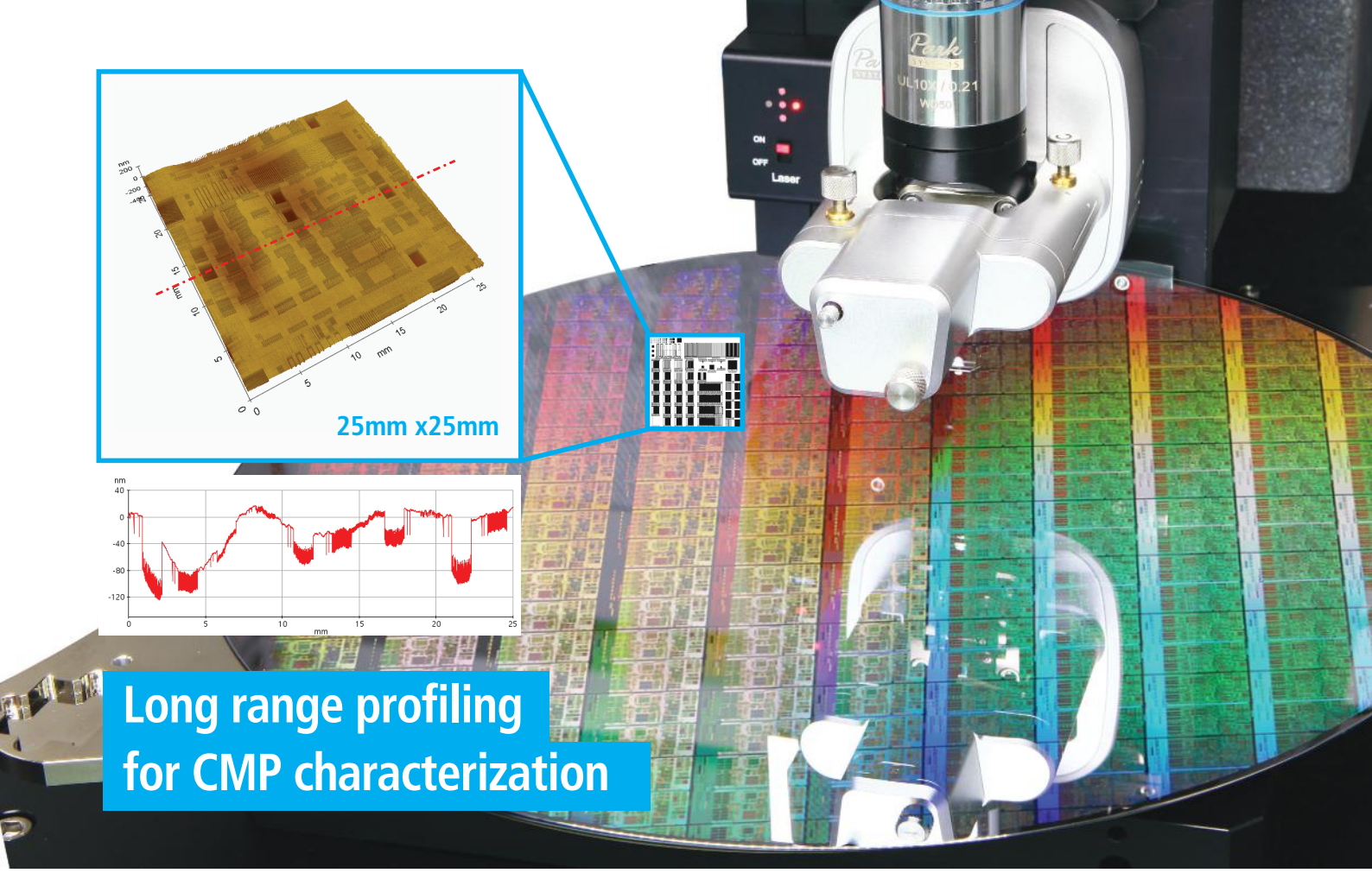
VACUUM EQUIPMENT

FLOW MEASUREMENT

HYDROGEN GENERATORS

TEST

WAFER SERVICES



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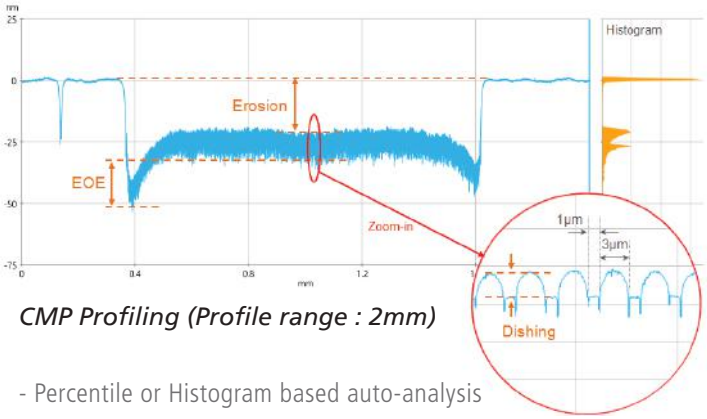

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