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Volume 16 Number 1**Editor-in-Chief**David Ridsdale dr@angelbcl.co.uk
+44 (0)1923 690210**Consultant Editor**Richard Stevenson PhD
richardstevenson@angelbc.co.uk
+44 (0)1291 629640**Publisher**Jackie Cannon jc@angelbcl.co.uk
+44 (0)1923 690205**Account Handlers**Shehzad Munshi sm@angelbcl.co.uk
+44 (0)1923 690215
Tommy Beazley tb@angelbcl.co.uk
+44 (0)1923 690222**Design & Production Manager**Mitchell Gaynor mg@angelbcl.co.uk
+44 (0)1923 690214**Circulation Director**Jan Smoothy js@angelbcl.co.uk
+44 (0)1923 690200**Subscriptions Manager**Debbie Higham dh@angelbcl.co.uk
+44 (0)1923 690220**Commercial Director**Stephen Whitehurst stephen@angelbc.co.uk
+44 (0)2476 718970**Directors**Stephen Whitehurst, Jan Smoothy
Bill Dunlop Uprichard**Published by**Angel Business Communications Ltd,
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Watford, Herts WD17 1JA, UK
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Calamitous Copenhagen

The failure of the world's leaders to agree on enforceable targets for CO₂ reductions is bad news on many fronts. Not only does it highlight the reluctance of humanity to care for its most vulnerable - it delays the introduction of new technologies that could both reduce global warming and reduce dependence on oil.

If a legally binding agreement had been signed, then it could have spurred tremendous investment in various compound semiconductor technologies. That's because reducing CO₂ emissions requires a two-pronged attack - generating more electricity from renewable sources and using it more efficiently - and the compounds can help in both cases. CdTe and multi-junction cells can provide a valuable contribution to a portfolio of renewable sources, and energy savings are possible by switching from incandescents to LEDs and from silicon power electronics to wide bandgap equivalents.

But there is no need to get too despondent about the missed opportunity at Copenhagen. Although the nations can't agree on a roadmap for slashing greenhouse gas emissions, many still have their own targets, and their governments are funding the development of a portfolio of clean technologies, including more-efficient, lower-cost LEDs and novel, ultra-high efficiency solar cells.

One attraction of turning to more efficient products is that it reduces energy bills. Local governments and companies are well aware of this - the widespread conversion of conventional traffic lights to those lit with LEDs is just one example. And we can expect similar cost-cutting initiatives in years to come, such as the growth of LED-lit parking lots and more efficient base stations employing GaN transistors.

The role of the individual should not be ignored, either. More and more people are factoring environmental issues into their decision-making, and this too could help the growth of LED sales. Using these devices to backlit TVs currently commands a small premium over the incumbent technology, but many may be willing to pay a few more hundred dollars for reduced power consumption, while enjoying the benefits of a better picture.

The high profile of green issues in the media will also help our industry's future. Rewind the clock by a decade or two, and a career in the III-Vs could often mean the development of faster, more powerful RF chips for the military. Helping to fight a war would have turned-off many talented physics and engineering graduates, who would have looked for a job elsewhere.

But today it's possible to help to save the planet with a career in the compounds. This makes our industry an attractive one to be involved with, and although Copenhagen didn't deliver, it will not prevent the compounds from playing an important role in reducing greenhouse gas emissions in the future.

Richard Stevenson PhD
Consultant Editor



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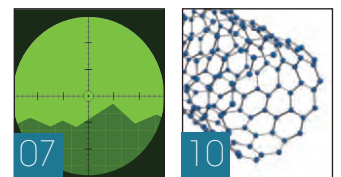
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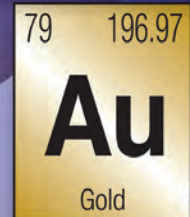
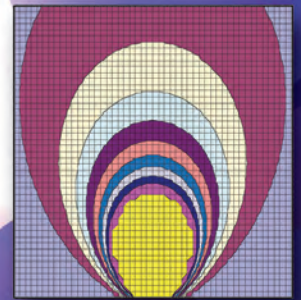
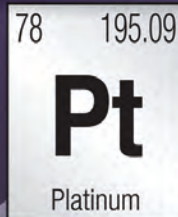
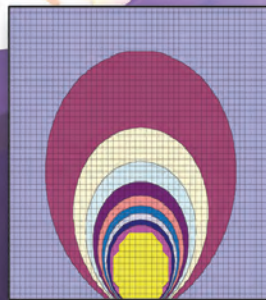
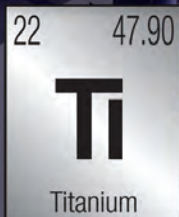
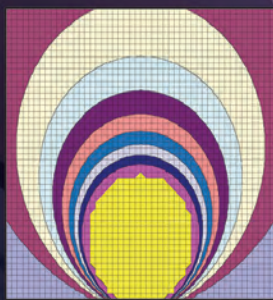


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First phase targets met for European CMOS photonics project

The pan European consortium HELIOS has announced its first update. Leti, coordinator of the consortium announced that the 19 partners have met or exceeded their phase-one goals for the large-scale CMOS photonics project. Launched by the European Commission in 2008, the €8.5 million project is designed to develop microelectronics fabrication processes for integrating photonics with CMOS circuits and to make the technology available to a wide variety of users. The participants include the major European CMOS photonics and electronics research centers and companies and potential users of the technology. The project will drive the European RTD in CMOS photonics and pave the way for industrial development.

First-phase achievements of HELIOS have concentrated on light photodetection and light coupling/routing; the related successfully completed milestones include:

- Characterization of vertical and lateral PIN Ge and III-V MSM photodetectors, showing low dark current, high optical responsivity and high optical bandwidth compatible with 40 Gb/s operation
- Demonstration of germanium photodiode bandwidth of 90GHz
- Demonstration of inverted taper coupling structure with 1dB coupling loss
- Design and fabrication of a transition between rib/strip waveguides with less than 0.2dB measured losses
- Demonstration of a high-efficiency grating coupler showing a coupling efficiency of -1.6dB and a 3dB bandwidth of 80nm
- More than 30 publications in international conferences or journals
- Organization of a winter school and two international events

"Europe has a well-established photonics-components industry and it is strategically important for us to maintain photonic chip design and chip-integrating functions that provide new opportunities for our microelectronics companies and enable us to compete with other countries," said Laurent Malier, CEO of Leti. "HELIOS combines the advanced, upstream research on CMOS photonics from leading research laboratories and universities with the commercialization expertise of some of

Europe's leading technology companies that will make this technology commercially viable."

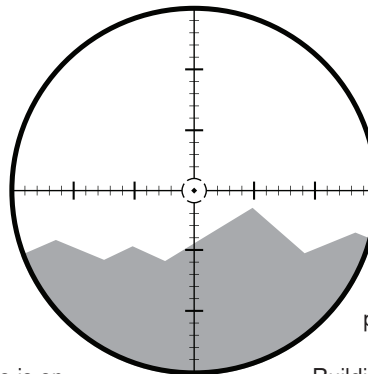
CMOS photonics is an intensely active research topic in many countries around the world, which increases the urgency for innovative results from HELIOS.

The project's success in developing microelectronics fabrication processes for integrating photonics with CMOS circuits would cement Europe's role as a global leader in this emerging technology. It will also have a major impact on the industry by, for example, leading to low-cost solutions for a range of applications: optical communications, optical interconnections between semiconductor chips and circuit boards, optical signal processing, optical sensing, and biological applications.

By co-integrating optics and electronics on the same chip, high- functionality, high-performance and highly integrated devices can be fabricated, while using a well-mastered microelectronics fabrication process. In addition, advances in CMOS photonics will move the emphasis from device component to architecture. Industrial and RTD efforts then could be focused on new products or new functionalities rather than on the technology level.

The four-year HELIOS project includes the development of such essential building blocks as efficient sources (silicon-based and heterogeneous integration of III-V on silicon), fast modulators and, more long term, the combination and packaging of these building blocks for the demonstration of complex functions to address a variety of industrial needs.

These include a 40Gb/s modulator on an electronic IC, a 16x10 Gb/s transceiver for WDM-PON applications, a photonic QAM-10Gb/s wireless transmission system and a mixed-analog and digital transceiver module for multifunction antennas.



Development of high-performance generic building blocks that can be used for a broad range of applications, ranging from WDM sources by III-V/Si heterogeneous integration, fast modulators and detectors, passive circuits and packaging.

Building and optimizing the entire supply chain to fabricate complex functional devices. Photonics/electronics convergence will be addressed at the process level and also at the design level as HELIOS helps develop an adequate design environment.

Investigating promising approaches that offer clear advantages in terms of integration on CMOS for next-generation CMOS photonics devices.

Road mapping, dissemination and training to strengthen European activities in this field and to increase awareness of new users about the potential of CMOS photonics. As coordinator of HELIOS, which includes nearly 60 researchers from member organizations, Leti is responsible for the technical, administrative and financial management of the project and for the day-to-day technical monitoring, direction and progress on the project. Leti also is a key contributor to the development of building blocks and integration processes that are part of HELIOS.

In addition to Leti, the HELIOS partners are:

- IMEC (Belgium)
- CNRS (France)
- Alcatel Thales III-V lab (France)
- University of Surrey (UK)
- IMM (Italy)
- University of Paris-Sud (France)
- Technical University of Valencia (Spain)
- University of Trento (Italy)
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- Photline Technologies (France)

Nitrogen cannot dope ZnO p-type, say UCSB researchers

COMPUTATIONAL scientists at the University of California, Santa Barbara (UCSB), have provided convincing evidence that nitrogen, which is widely believed to be a shallow acceptor in ZnO, is in fact a very deep acceptor and cannot lead to p-type conductivity.

ZnO has been intensively pursued as an optoelectronic material, in hopes of developing it into a wide-band-gap light emitter that would compete with GaN-but with the advantage that large single-crystal substrates are commercially available. A large part of the effort has been directed at establishing p-type doping, which is very challenging in wide-band-gap oxides in general. Dozens of papers claiming observations of p-type conductivity have appeared in the scientific literature.

However, independent verification of these reports has been lacking, as have convincing demonstrations of pn junctions.

The UCSB team, consisting of John Lyons, Anderson Janotti, and Professor Chris Van de Walle, performed calculations based on the hybrid functional methodology. In an Applied Physics Letter published online it is reported that nitrogen acceptors have an ionization energy of 1.3 eV-much too large to enable p-type doping.

They also address why the behaviour of nitrogen has been misinterpreted in so many of the previous investigations. In optical studies, the photoluminescence line most commonly associated with nitrogen is now known to be caused by stacking faults. Optical absorption and emission associated

with the nitrogen deep acceptor in fact occurs at much lower energies, at wavelengths that have been all but ignored in prior studies. When it comes to electrical measurements of acceptor-doped ZnO, the researchers point out there are many potential pitfalls, casting doubt on the p-type conductivity reports published to date.

"We are convinced that none of the substitutional acceptors (including Li, N, P, As, or Sb) will yield p-type conduction" commented Project Scientist Anderson Janotti. "Interstitial doping still looks promising, although it may be difficult to accomplish in actual device fabrication."

"Our finding that nitrogen is not a shallow acceptor will come as a disappointment to many who are excited about ZnO as an optoelectronic material" said Van de Walle. "However, we hope it will contribute to resolving the conflicting results that have plagued the literature, and will refocus ZnO research efforts on the many exciting applications that do not require ambipolar doping, such as transistors and sensors."

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Iron-arsenic compounds sought for quantum critical point

THE ABILITY of electrons to conduct electricity with no resistance is linked to their magnetic properties, new research has revealed.

A recently-discovered class of iron-based superconductors have undergone experiments by a team of Chinese and US physicists who discovered that the ability of electrons being able to conduct electricity with no resistance is specifically linked to their magnetic properties.

Rice University revealed in a recent edition of Physical Review Letters that close examination of several iron-arsenide compounds found that the strength of the magnetic order was reduced when smaller phosphorus atoms were introduced and replaced the arsenic atoms.

Qimiao Si, a Rice physicist, said this highlights evidence that a

magnetic quantum critical point can be found in these materials, something which could prove essential to the future development of semiconductors.

The researchers noted that high-temperature superconductors could be used to progress MRI scanners, high-speed trains and electric generators.

Mr Si stated: "The evidence from this study bolsters the hypothesis that high-temperature superconductivity in the iron pnictides originates from electronic magnetism."

Low temp superconductivity is caused by ionic vibrations. Last year, Ames Laboratory research revealed that iron-arsenide semiconductors' ability to carry a viable current could hold potential for the future development of much sought after zero-resistance power transmission.

Research presses ahead for vertically grown silicon nanowires

GROWING SILICON nanowires vertically can allow for more transistors to be placed on to a chip, resulting in more powerful electronics. However, the smaller the nanoscale used, the more difficult it becomes for researchers. At the end of November, it was revealed that researchers had learned how to create nanowires with different semiconducting materials sharply defined at the atomic level, bringing the industry one step closer to a new generation of ultrasmall transistors.

The team from IBM, the University of California at Los Angeles and Purdue University said the development was critical for making efficient transistors out of nanowires, which can also lead to more powerful computer chips.

Indeed, the semiconductor industry is constantly striving to meet the challenge set by Moore's law, which states that the number of transistors on an integrated circuit will double approximately every two years without it increasing in size. The nanowires consist of sharply defined layers of silicon and germanium. Researchers managed to grow the silicon nanowires vertically, meaning more transistors could fit on to a chip - this could help realise the challenge of Moore's law.

"But first we need to learn how to manufacture nanowires to exacting standards before industry can start using them to produce transistors," stated Eric Stach, an associate professor of materials engineering at Purdue.

Realising the need for more powerful chips, Intel recently announced a concept chip containing 48 cores on a single Intel processor, allowing for more power being available in a limited space. Following on from the research, the organisation said it was continuing to develop this to make smaller and more efficient consumer

electronics. The single-chip cloud computer (SCC) - which has up to 20 times more processing power than its current Intel Core processors - is still a prototype but has significant potential.

Speaking to Daily News & Analysis India, Vasantha Erraguntla, senior engineering manager at Intel Labs, said: "The second generation 48-core chip - SCC - has half the number of cores of its earlier generation chip, 1.3 billion transistors and dynamic

voltage scaling that has made it conducive for research and power efficient."

Intel is now looking at 32nm technology allowing for more semiconductors to be placed on an integrated circuit. This will be the third-generation SCC, already moving on from the current 45 nanometre-technology used for the prototype. However, scientists could have to overcome future problems of working with silicon at a nanometre scale smaller than 15.

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Growing Europe's nanowires

EUROPEAN researchers have developed state-of-the-art nanowire 'growing' technology, opening the way for faster, smaller microchips and creating a promising new avenue of research and industrial development in Europe. Nanowires are a promising new technology that could meet rapidly rising performance requirements for integrated circuit design over the next ten years. They are tiny wires just tens of nanometres in diameter and micrometers in length. They could mean smaller, faster and lower power electronics, and lead to entirely novel architectures such as 3D microchips – a vertical stack of circuitry that can massively increase the size of circuits for the same footprint.

Nanowires are so narrow they are often called 'one-dimensional' structures because the width of the wire constrains the sideways movement of electrons as they pass through the wire. Also, the cylindrical geometry allows the most efficient electrostatic gating technology.

Unsurprisingly at this scale, nanowires demonstrate many characteristics that offer the potential for novel circuits and architectures, and physicists are very excited. The Japanese pioneered the field with the USA taking up the work, and with a few European teams entering soon after.

But the Europeans are on their way. Recent work at the NODE project led to world-class technology and 40 patents. "Silicon technology becomes very challenging when you get down to 10-15nm," explains Lars Samuelson, director of the Nanometer Structure Consortium at Lund University and coordinator of the NODE project.

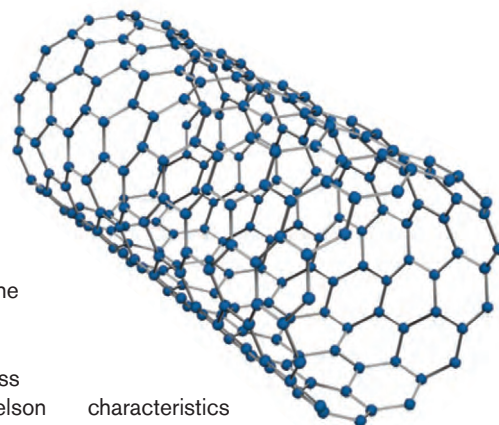
"One of the problems of the [current] top-down approach is that it introduces harsh environments and you end up with devices that may be dominated by defects."

NODE's nanowires are 'grown' from the bottom up, like crystals, into vertical structures. "We call it 'guided self-assembly', and it is a 'bottom-up' process that can result in fewer defects," Samuelson says. Vertical nanowires can consist of different materials, by simply altering the depositing material, so the wire takes on layers with different characteristics. "There are many potential opportunities for developing new technologies," he says. "This vertical arrangement may be the route to 3D circuit design as well as to realise monolithic on-chip optoelectronics."

NODE focused on combining silicon with indium arsenide (Si:InAs) and silicon with silicon germanium (Si:SiGe), two very promising materials. "Indium arsenide is inherently very fast and, as such, it was of particular interest to our work," remarks Samuelson.

The project looked at every link in the nanowire production chain, from growth, processing on an industrial scale, to characterisation and integration. "And one of the big challenges of the project was the integration of our work with current silicon processing technology, so there was a big effort on processing," Samuelson stresses.

For this, characterisation studies were important to examine the different materials used and the effects induced by the nanowire structure. NODE also examined



characteristics of potential devices, such as field effect transistors (FET). Finally, the team looked at integrating these devices into circuits.

It is a huge body of work and led to some real breakthroughs. "One of the breakthroughs was the perfect deposition of high-K dielectrics coating the nanowires and serving as a dielectric in the wrap-gate transistors," reveals Samuelson. "We developed a very good technique for this."

High-K dielectrics overcome some of the limits of silicon dioxide at very small scales and are a promising strategy for further miniaturisation of integrated circuits.

"As part of this research, we have also encountered problems and possible roadblocks [to further] development, such as quite severe problems in growing Si nanowires using gold catalysts", adds Samuelson.

"This technology is not ready for industrial applications, and whether it will be three, six or nine years before it appears industrially, I cannot say," Samuelson warns. "But we established the state of the art, we have the best results."

Yale researchers use benzene as single-molecule semiconductor

WHILE it has been revealed as a scientific breakthrough - and not a practical application - only, researchers have found a benzene molecule attached to gold behaves like silicon. Researchers have revealed that a benzene molecule attached to gold contacts behaves like a silicon transistor, which could open up the progression of single-molecule semiconductors.

The team from Yale University and the Gwangju Institute of Science and Technology in South Korea manipulated the molecule's different energy states by applying various voltages through the contacts, controlling the current passing through it. Traditional transistors are

not feasible at small scales in computer circuits and, as such, scientists want to use molecules as semiconductors, although Mark Reed, the Harold Hodgkinson professor of engineering and applied science at Yale, said the practical application of faster and smaller "molecular computers" could be decades away.

"We're not about to create the next generation of integrated circuits. But after many years of work gearing up to this, we have fulfilled a decade-long quest and shown that molecules can act as transistors," he stated. Benzene is widely used in the production of rubbers, dyes and plastics and is highly flammable.

Spire gets go ahead for GaAs expansion

SPIRE CORPORATION has announced that its wholly owned subsidiary, Spire Semiconductor, LLC, has successfully completed Phase I of its High Efficiency Concentrator Solar Cell program with the Department of Energy's National Renewable Energy Laboratory (NREL) and has been notified the NREL will authorize Phase II of the program. Under the 18-month, \$3.7 million cost share subcontract, Spire Semiconductor is developing technology to cost-effectively manufacture 42% efficient, 500 sun, concentrator solar cells for concentrator photovoltaic (CPV) systems.

Spire Semiconductor passed through the NREL Stage Gate Review, a go/no go decision point to validate the progression of

the project and assure that progress meets contract objectives. These objectives include estimates of key performance parameters of competitive Levelized Cost of Energy; annual manufacturing capacity potential; direct manufacturing cost; and cell Mean Time Between Failure (MTBF). PV cell performances of greater than 39%

efficiency were achieved during Phase I.

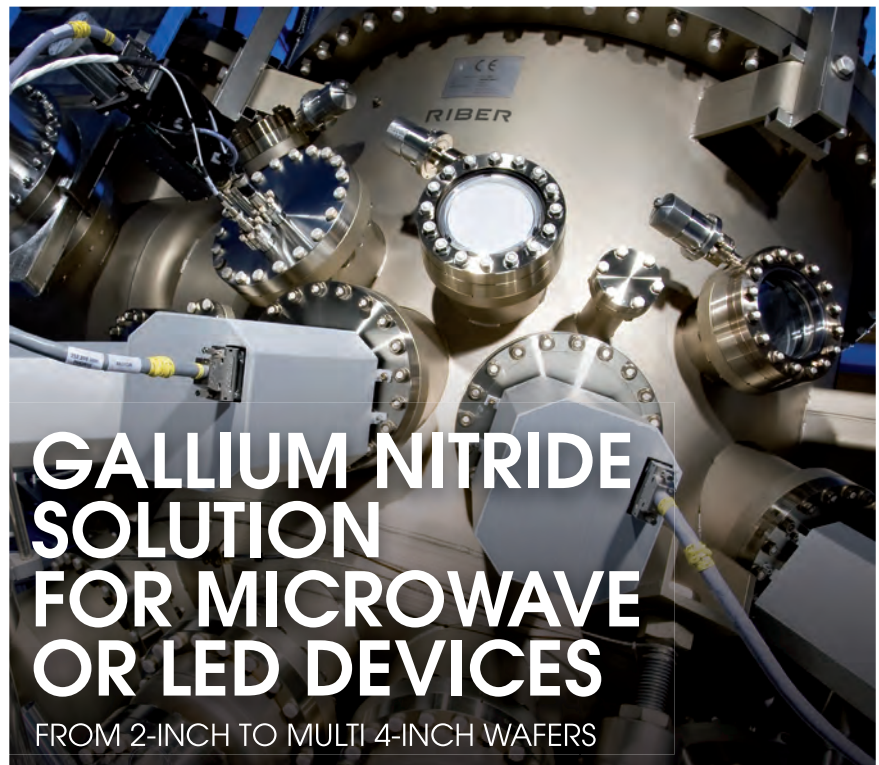
"We are very happy to be given the go ahead with our program," said Roger G. Little, Chairman and CEO of Spire Corporation. "It validates our efforts toward developing a proprietary GaAs concentrator solar cell that exceeds anything available."

Highest power output for 638 nm red LD

MITSUBISHI has revealed a 638-nanometre wavelength red LD which could prove ideal for the increase in popularity of pico projectors. A 638-nanometre wavelength red laser diode (LDs) has been revealed and its maker asserted that it offers the world's highest power output for this band of LDs.

Mitsubishi announced the launch of the 638-nanometre LD, with a power output of 500 milliwatts that makes it ideal for devices such as pico projectors and portable display systems that need a red light source with high brightness. The semiconductor industry could be interested in this development as pico projectors are often embedded in or connected to laptop computers and mobile telephones, with LDs and light emitting diodes mainly used as the light source.

LDs deliver higher output power with less consumption than LEDs, meaning the efficiency of semiconductors may constantly be addressed to ensure optimal performance. Furthermore, LDs offer a wider range of colours compared to lamp-based projectors. Pico projectors require miniaturised semiconductors as while sufficient storage is needed, it needs to fill as little space as possible to accommodate an attached display screen.



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INNOVATIVE SOLUTIONS FOR SEMICONDUCTOR INDUSTRY

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First Solar increases development with acquisition

FIRST SOLAR has completed the acquisition of a portion of Edison Mission Group's (EMG) solar project development pipeline. The utility-scale solar projects are located in California and the Southwest and manufacture solar modules that employ a thin layer of cadmium telluride semiconductor material to convert sunlight into electricity.

"Acquiring the EMG development pipeline extends First Solar's leadership in the U.S. utility market," said Lisa Bodensteiner, First Solar vice president of business development for North America. "It builds on our strategy to cultivate robust and predictable module demand in utility-scale applications."

The acquisition complements and diversifies First Solar's existing portfolio of utility-scale thin film photovoltaic solar projects. First Solar's existing projects are largely sited on public land, range to 550 megawatts (MW) in size, and are mostly under contract with utilities. The EMG projects that First Solar is acquiring are sited largely on private land, range from 20 to 150MW, and are not yet contracted with utilities.



First Solar and EMG have worked together since 2008 on the EMG projects, with First Solar providing engineering, procurement and construction services while EMG was responsible for land acquisition and permitting. First Solar will handle all development for these projects.

"First Solar is a good partner and the obvious purchaser of our interest in these projects which we have jointly developed," said Gerry Loughman, senior vice president of Development for EMG.

German OLED research project secures new member

A NEW national R&D project has recently been started in Germany focusing on the development of OLED displays and lighting applications. AIXTRON will participate in this 14.7 million Euro project together with ten other partners with the target to strengthen Germany's leading position in the fast growing OLED market.

Funded by the German Federal Ministry of Education and Research (BMBF) for a total period of three years, So-Light (Special organic Light) will focus on specific OLED applications, such as special lighting systems and displays. The technological focus will be on novel materials (transport materials, triplet emitter, redox dopants and matrix materials), improved optical systems and on process technologies for small molecule based OLEDs.

As part of the latter element, AIXTRON will take the lead in this area through the optimization of its proprietary OVPD (Organic Vapor Phase Deposition)

technology. Other project deliverables will be application studies and demonstrator devices for specific applications such as automotive or architectural lighting and backlights for large displays.

"We are very happy to participate in this project", says Prof. Michael Heuken, Vice President R&D at AIXTRON. "OLEDs and its application for special lighting and signage purposes is one of our strategic research targets. The So-Light project partners share the vision that OLEDs will play an important role to provide environmentally friendly light sources combined with novel design opportunities."

AIXTRON's partners in the So-Light project are Novald AG Dresden, Sensient Imaging Technologies GmbH, Westfälische Wilhelms University of Münster, Fraunhofer IPMS Dresden, Symbolo GmbH, Fresnel Optics GmbH, Hella KGaA Hueck & Co, Siteco Beleuchtungstechnik GmbH, AEG-MIS mbH and the University of Paderborn.

Samsung Partners With Luminus Devices

LUMINUS DEVICES has announced that its PhlatLight LED PT-120 is the light source in Samsung's new XGA (1024 x 768 pixels) LED data projector. It is the projection display industry's first LED-powered data projector. Today, PhlatLight LEDs are the solid-state light source of choice across all projection technologies, including 3LCD, DLP and LCOS.

The new Samsung LED data projector marks a milestone in the industry by validating that LEDs will start replacing conventional arc lamps in mainstream front projectors used in business, education and commercial applications. This market is forecasted by market research company Pacific Media Associates, Inc., to be in excess of 6 million units in 2010.

LEDs are a compelling light source for front projectors since their high reliability eliminates the need for expensive lamp replacement, which typically ranges from \$250 to \$400 including parts and labor. This drives down the total cost of ownership and reduces the administrative burden to

manage stocks of replacement lamps and disposal of used lamps.

"Samsung's new LED data projector is a great illustration of how Luminus works in close partnership with its customers to create a new multi-million unit market for PhlatLight LEDs and demonstrates that our unique large chip technology is a great fit for mainstream data projectors," said Keith T.S. Ward, CEO, Luminus Devices. "In today's challenging economic landscape, the marketplace is asking for affordable, long-lasting, lower total cost of ownership projectors in the business and education markets. Luminus and Samsung are fulfilling this demand while also creating new value for our customers with next-generation technology advancements such as amazing color depth and instant start and restart functionality."

"Leveraging PhlatLight LEDs, Samsung's new front data projector expands our line of LED projectors for business and education markets," said Jeong-Ho Nho, vice president of the visual display division, Samsung.

Hitachi Cable Develops High Power 55-Lumen Red LED Chips

HITACHI CABLE has announced the development of a high-power red LED chip offering a maximum luminous flux of 55 lumens. This was enabled by increasing the size of the LED chip and use of a fine line electrode structure.

Hitachi Cable manufactures supplies aluminum gallium arsenide (AlGaAs) epitaxial wafers and aluminum gallium indium phosphorus (AlGaInP) epitaxial wafers, both of which are compound semiconductor wafers for red LEDs. In response to demand for LEDs of higher luminous efficiency, the company has also developed a high-brightness red LED chips (hereafter referred to as an "MR-LED chips") that form a metal reflector (MR) under the light emitting layer. This product is currently being supplied to LED package manufacturers and other customers.

Through its LED business, Hitachi Cable has recognized the growing demand for higher output LED chips. The company has incorporated fine electrode structures and enlarged chip dimensions to develop high-power red LED chips offering outputs as

high as 55 lumens. One of the methods of improving per-chip light output is to increase the chip dimensions. However, larger chips increase the difficulty in distributing a uniform current across the entire light emitting layer. If large electrodes are positioned in the upper layer of the chip for a more uniform current dispersion, light from the light emitting layer will be blocked, reducing the light extraction efficiency.

To resolve these problems in developing a new LED chip, instead of using larger electrodes, Hitachi Cable has utilized two pad electrodes for receiving power, a backbone electrode connecting the two electrodes, and multiple fine line electrodes that extend from the backbone electrode on the upper chip layer.

By employing fine line electrodes, Hitachi Cable has achieved uniform dispersion of current across the chip surface without blocking light from the light emitting layer, attaining a maximum luminous flux of 55 lumens in a large LED chip measuring 1 mm by 1 mm—equivalent to the combined output of 21 MR-LED chips (0.33 mm x 0.33 mm).

OLED wallpaper could replace traditional lights

SEMICONDUCTOR TECHNOLOGY in the form of OLEDs could replace conventional light fittings by being coated on to film which acts as wallpaper. Semiconductor technology has been used to develop the potential for light bulbs to be replaced with thin film that can cover walls like wallpaper.

Organic light emitting diodes (OLEDs) have been used by Welsh company Lomox to create next-generation and low-carbon lighting for homes and businesses. OLEDs are coated on to thin flexible films to create the wall panels, although they can also be applied to mobile telephone displays, flat screen televisions and computers. The Carbon Trust has awarded a £454,000

grant to the firm so that the semiconductor technology can be used in both commercial and residential premises, as well as on the roads to light barriers and signs without the need for mains electricity.

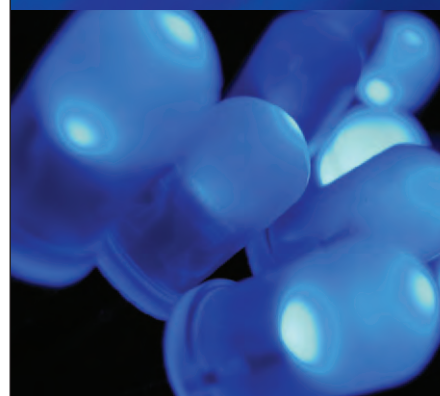
Ken Lacey, chief executive of Lomox, said the company has developed a chemical which reduces the cost and overcomes the lifespan issues associated with OLEDs. "This is a chemical that in a flat panel display screen you can put it in the device and it emits light. In a light you can put it anywhere. You can paint it on a wall or wallpaper," he stated.



Photo credit: Samsung

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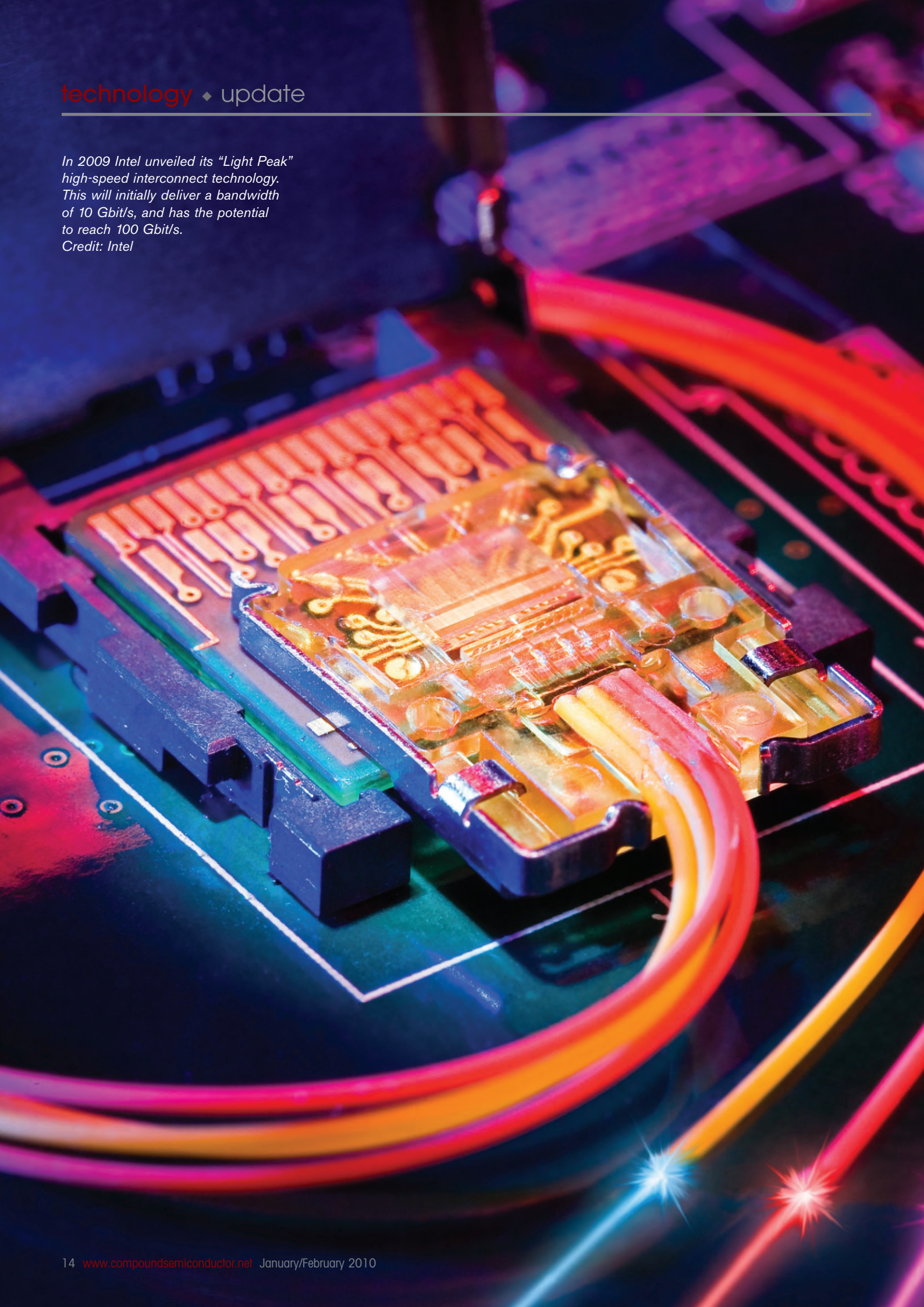


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*In 2009 Intel unveiled its "Light Peak" high-speed interconnect technology. This will initially deliver a bandwidth of 10 Gbit/s, and has the potential to reach 100 Gbit/s.
Credit: Intel*



IQE prepares to thrive in a buoyant market

Soaring sales of VCSELs for optical links in PCs and handsets, coupled to the launch of ultra-efficient multi-junction solar wafers and the introduction of next-generation wireless products could bolster IQE's revenue in the coming years.

Richard Stevenson reports.

For IQE there is good reason to look forward to the future. It is serving a compound semiconductor industry that is expected to enjoy double-digit growth in the coming years, and some of its products are operating in sectors that could grow even faster.

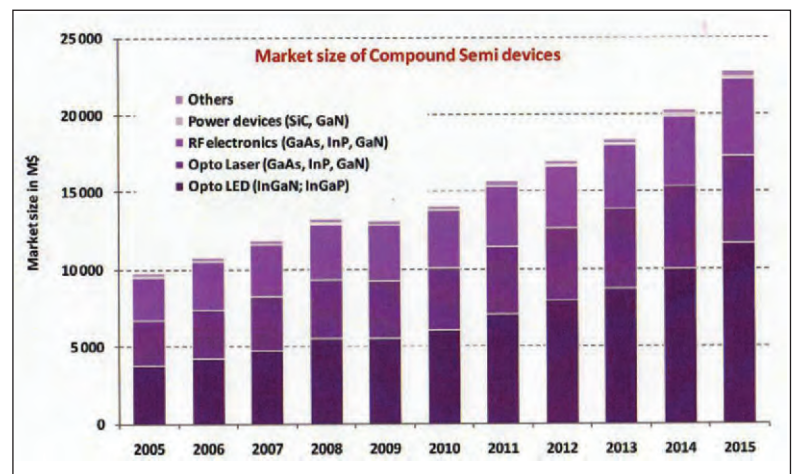
Both of these trends were discussed on 15 December at a Technology Update meeting attended by IQE at College Hill, London. Philippe Roussel from Yole Développement kicked-off the presentations with an overview of the state of the compound semiconductor industry, and this was followed by presentations from several players in the supply chain, including UK solar start-up Quantasol and the US-based manufacturer of GaAs-based wireless products, Anadigics.

Roussel had some good news for everyone involved in the compound semiconductor community: revenues will grow in all the major sectors, and total global sales for compound semiconductor chips will increase from \$12-13 billion in 2008 to just over \$20 billion in 2014.

According to him, the LED market is outpacing overall growth, and by 2014 it will be worth \$10 billion, almost twice the value that it is today. The main driver behind this high compound annual growth rate of 15 percent is the increasing deployment of LEDs in automobile headlamps, forms of solid-state lighting and types of displays. Roussel says that these applications require ultra-high-brightness LEDs with an output of at least 1W, and he predicts revenue from this particular class of LED to rocket from \$280 million in 2009 to \$3.1 billion by 2014. These high-performance emitters will command a very hefty price tag: in 2014 their market share, in terms of volume, will be less than 2 percent, but they will account for more than 30 percent of total LED revenue.

Up until recently, IQE has had minimal involvement in the LED sector, but it could now start to tap into this market thanks to its acquisition of UK start-up NanoGaN. The University of Bath spin-out has a novel nanotechnology for making GaN substrates, and the promise of low-cost production processes may allow this platform to be used for high-power LED manufacture.

Today IQE generates a substantial proportion of its revenue from the sale of epiwafers for wireless products, a market that Roussel tips for growth, thanks to the roll out of new wireless applications. He did not evaluate this growth in terms of the dollar, but he said that the volumes of GaAs semi-insulating substrates that are used exclusively for manufacturing these types of products will enjoy a compound annual growth rate of 15 percent.



The French market analyst Yole Développement is predicting growth for all the major sectors within the compound semiconductor industry. Credit: Yole Développement

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Roussel sees an opportunity for GaN and SiC devices in the power electronics market. One of the attractions of turning to these wider bandgap materials is their ability to handle far higher current densities: silicon devices must be operated at less than 1 A mm^{-2} , while those made from GaN can be driven at $3\text{-}5 \text{ A mm}^{-2}$. In addition, SiC and GaN devices can operate at far higher temperatures than their silicon brethren.

The French analyst told the attendees that the attractive attributes of SiC and GaN devices have caught the eye of all the leading silicon power electronics manufacturers. Market leader Infineon has pioneered the commercialization of SiC Schottky diodes, and its closest rival, Fairchild, dabbled with SiC before exiting this part of the business in 2009. The next biggest silicon power electronics manufacturer, International Rectifier, is developing GaN products, and ST Microelectronics and Toshiba are pursuing both types of material technologies.

Roussel expects the market for GaN and SiC devices to be worth just \$27 million in 2010, but will rocket to over \$800 million by 2019. He believes that the main driver behind this tremendous growth is the uptake of wide bandgap diodes and transistors in hybrid electric vehicles. Switching from devices made from silicon to those based on SiC or GaN increases the power electronics bill, but the far higher operating temperature of the wide bandgap chips allows the removal of a second water cooling system that leads to significant cost and weight savings.

The wide bandgap power electronics market offers a great opportunity for epiwafer providers, according to Roussel. He said that many of the companies operating in this arena tend to already work with external silicon foundries, and they will not want to invest in their own growth facilities. IQE is yet to offer any products in this area, but there is no reason why it could not move into this sector over the coming years.

A quantum leap for PV

The economic crisis took its toll on the solar market in 2009, and according to market analyst Display Search, global demand experienced a year-on-year fall of 13 percent to 5.2 GW. However, a rebound is expected, with demand predicted to hit 26.5 GW by 2013.

Today systems based on concentrating photovoltaics (CPVs) are a negligible fraction of the current solar market, but deployment of this technology is expected to grow strongly throughout this decade. Quantasol, a spin-out of Imperial College London, hopes to profit from this growth. "Our company is now ready for production and commercial manufacture," claimed Chris Shannon, who has been the CEO of the company since fall 2009.

If CPV technology is to enjoy significant commercial success, then its power generation costs must fall. Shannon claimed that there are three ways to do this:

increase cell efficiency; reduce the cost of the cell; or cut system costs.

Quantasol has chosen the first of these options, and has developed a novel solar cell technology that features quantum well layers in the cells. The cells in a triple-junction device are connected in series, and this means that the current densities generated by every cell must be matched, which limits overall efficiency. In a conventional device the middle cell produces the least current, and the other cells are modified to reduce their current density.

"What most people do to optimize this is to make the top cell thin, but this is a compromise," explained Shannon, who went on to reveal that it is possible to increase the density in the middle cell from 12.5 A cm^{-2} to 14 A cm^{-2} by adding quantum wells.

He believes that this increase in current density will make a significant impact on the overall solar cell conversion efficiencies, and backed this claim up with data from recent trials that revealed an increase from 34.9 percent to 39.6 percent, thanks to the addition of multiple quantum wells.

This efficiency is still below that produced by the leading developers of traditional multi-junction cells, such as Spectrolab and Fraunhofer Institute for Solar Energy Systems (ISE), which both reported values of more than 41 percent in 2009. And the target for Quantasol is going up, because this record tends to increase at about one percent per year. However, Shannon claimed that commercial device efficiencies trail the record-breaking values by about 3 percent, and he believes that customers will be attracted to Quantasol's launch of devices with 41.5 percent efficiency in 2010.

Shannon estimates that the potential revenue for Quantasol's cells will rise over the next few years, and will be over \$300 million by 2012. By then the efficiency of its cells is expected to be over 43 percent, rising to more than 46 percent by 2015. This gain will result from the introduction of quantum wells to the top cell.

If these efficiencies can be reached, then the benefits are not limited to just lowering the cost of the CPV systems – they will also increase the addressable market, thanks to



Research in Motion, the manufacturers of BlackBerry portable devices, employs GaAs MMICs made by Anadigics. Credit: Research in Motion



IQE has a growth facility at St Mellons, Cardiff, UK, which majors on the growth of epiwafers for optoelectronic devices, including VCSELs. Credit: R. Stevenson

an increase in the proportion of the world where the cost of this technology is viable. Shannon explained that today it only makes sense to consider CPV systems in areas where direct normal irradiance (DNI) is greater than 6, such as Spain, Australia and California. However, as efficiencies improve, this technology can compete financially in many other parts of the world, including all of continental US, southern Europe, and India.

Opportunities for VCSELs

A Japanese optoelectronics industry expert, Takeshi Nakamura, provided an insight into the opportunities in the VCSEL market. He explained that datacoms is the biggest market for VCSELs today, generating sales of about 20 million units.

The light source for optical mice is the only other significant market for VCSELs, and total shipments for this application are 10-20 million a year. Despite the small size of this particular sector, competition is fierce with about 10 manufacturers competing for sales, including Finisar, Avago Technologies and JDSU.

Although the current market for VCSELs is relatively small, Nakamura believes that volumes will go through the roof over the next few years, thanks to the emergence of this class of laser in consumer applications. He tips this device for deployment in PCs and mobile phones, where it will be used in conjunction with optical fiber to fulfill the demand for high speed routing of data. Intel is leading the introduction of this technology, and last year it unveiled its development of "Light Peak", which is claimed to combine

fewer, smaller connectors with longer, thinner cables to deliver higher bandwidth and multiple input/output protocols on a single cable.

Light Peak interconnects could replace copper links between the PC and the screen, facilitate video downloading from the network, transfer data from a gaming machine to its display, and improve data transfer within a PC. Intel's Light Peak technology would be backward compatible to USB 1.0-3.0, and be capable of data rates in the Gbit/s range. The cost-per-Gigabit is relatively low – about one-tenth of 8G Ethernet.

Nakamura pointed out that cell phones could also benefit from VCSEL-based optical links. He detailed the advantages of an optical approach, which include the removal of electromagnetic interference issues, the size of the technology (the thin-film waveguides can have a diameter of 0.1 mm, and pass through 3 mm diameter hinges), and the opportunity to simplify design layout.

Wireless prospects

One of IQE's key growth sectors over the last few years has been the outsourcing of epiwafers to the wireless market, and Mario Rivas, the new CEO of Anadigics, the US manufacturer of GaAs-based MMICs, gave the keynote wireless presentation.

Rivas is a firm believer in the outsourcing model. He pointed out that the silicon industry has adopted this approach over the last few years, and the only large in-house manufacturers today are Intel, IBM and TSMC.

Anadigics does not just outsource epiwafers. It also works with the Taiwanese firm WIN Semiconductors, a company that Rivas expects to become the TSMC of the GaAs foundry business. This relationship with WIN has helped Anadigics to increase its share of a GaAs market that should be worth \$5 billion in 2011.

Just over four-fifths of this is wireless products, an area that accounts for 70 percent of Anadigics' sales. Cable TV is the other significant sector for the company, and Rivas describes the products for this market as "very profitable".

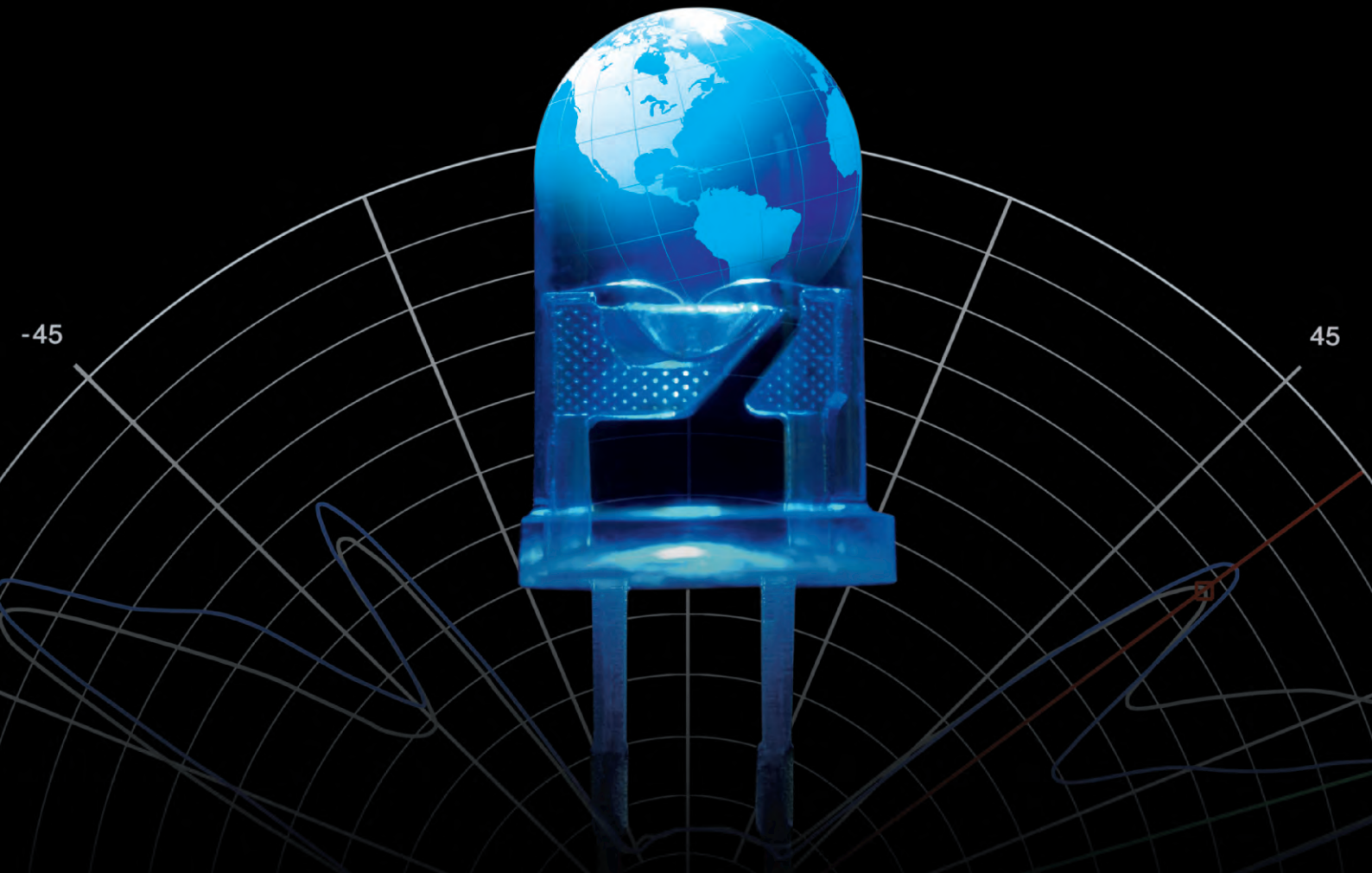
He explained that the short-term goals for Anadigics include operating at "cash-neutral", and generating quarterly revenues of \$80-100 million. According to him, the key behind the company's recent success is its agility, and this should help it to enjoy further success in emerging applications based on 4G/LTE, mobile WiMax and femtocells technologies. If it executes on these fronts, then Anadigics will enjoy the spoils. And if IQE can garner powerful relationships with growing fabless companies, then it too shall reap rewards in years to come.

● Declaration: the author of this article, Richard Stevenson, holds a small number of shares in IQE



In the fall of 2009 IQE strengthened its substrate technology portfolio by acquiring NanoGaN, a spin-out of Professor Wang Nang Wang's group at the University of Bath, UK. This start-up produces a GaN platform for device growth by using a variant of the epitaxial lateral overgrowth technique that is based on nanometer holes in a GaN template. Credit: R. Stevenson

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Stretching from the blue to the green

Osram has been a front-runner in race to make a green-emitting nitride laser, and its attempts to reduce dark spots in the active layer have enabled the company to be the first to break the 500 nm barrier. **Stephan Lutgen, Uwe Strauß and Michael Schmitt** detail device development and the wide variety of applications that promise to benefit from it.

Green lasers can serve many applications. Thanks to an emission wavelength that is close to the peak sensitivity of the human eye, they are ideal for aiding positioning and leveling tasks in the construction industry. If they are united with red and blue sources, they can form full color projectors that can form an image on a screen. And they can also be used for medical treatments, such as addressing a common form of blindness.

The ideal laser for all these tasks is a single, small compound semiconductor chip. These are not commercially available today, but lasers based on the nitride family of materials have recently reached these wavelengths, and they promise to combine a very stable output over a wide temperature range with fast modulation speeds and high efficiency. These attractive attributes have driven the development of longer wavelength nitride lasers for many years: the 405 nm lasers that are employed in BluRay players and recorders were commercialized in 2000; and chipmakers were selling 440-460 nm lasers by the middle of that decade. However, further commercial progress has been incremental, and the longest wavelength nitride laser that can be ordered from a manufacturer emits at 488nm [1].

Commercial limits

If commercial nitride lasers can be extended to the green, they could replace the far more cumbersome designs that are currently in use. These are either based on diode-pumped solid-state lasers, or frequency-doubled semiconductor lasers. Regardless of what approach is used, these commercial offerings tend to be complex systems requiring additional electronics and optics for stabilization within a reasonably broad operating range.

Two common examples of the diode-pumped solid-state laser are neodymium-doped yttrium aluminum garnet (Nd:YAG) and neodymium-doped yttrium orthovanadate

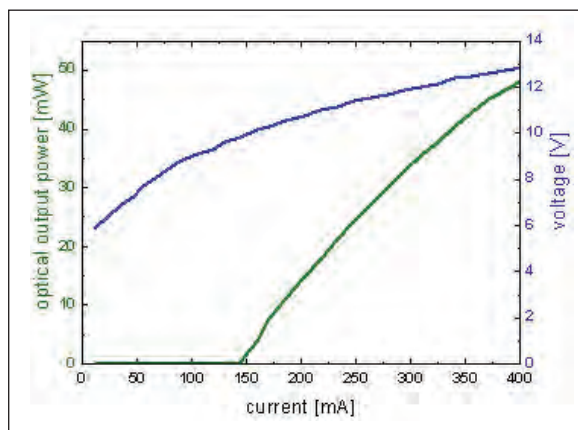


Research engineers at Osram Opto Semiconductors have recently developed a series of green InGaN laser diodes that emits at wavelengths up to 526 nm

(Nd:YVO₄) lasers. Both operate by employing a 808 nm GaAs-based laser diode to optically pump a 1060 nm solid-state laser, and then frequency doubling the emission produced by this laser to 530 nm with a non-linear optical up-conversion process, using lithium niobate (LiNbO₃), lithium triborate (LiB₃O₅), or similar crystals.

If the temperature of the pump diode shifts, its emission wavelength changes considerably. This is highly undesirable because the solid-state laser has a narrow absorption range, and this in turn restricts its operating temperature, which can be increased through the costly addition of external stabilization. To make matters worse, there is a strong intensity noise issue that can require additional elements within or outside the laser cavity for stabilization. Another downside of this type of laser is that its modulation speed is limited to the kHz range, due to the long lifetime of the charge carriers, and this means that the diode-pumped solid-state laser cannot be deployed for scanning beam projectors without an additional external modulator. However, in its very simple configuration this type of lasers can be used as a laser pointer, and more complex versions delivering a stable output power can serve medical and bio-technical applications. And by increasing the output power, these emitters can also be used in laser shows.

Fig. 1 Osram's 520 nm ridge waveguide laser, which has a 2 μm broad stripe with a 600 μm resonator length, can deliver an optical output power of 50 mW in pulse operation. To limit thermal effects the laser was measured in pulse mode with a duty cycle of 1 percent and a pulse length of 1 μs

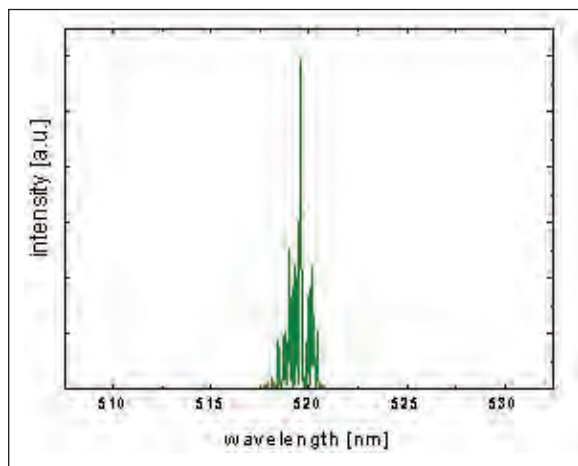


The other form of commercial green laser features either intra-cavity or extra-cavity frequency doubling. Both variants deliver fast switching times thanks to a 1060 nm, GaAs-based semiconductor laser source that is either electrically or optically pumped. Stable laser output over the operating temperature range results from maintaining the semiconductor emission at the frequency conversion wavelength.

This can be realized by adding a DBR structure to the electrically pumped laser, or using filter elements for the optical pumped laser. For intra cavity frequency doubling a periodically poled LiNbO₃ bulk crystal can be used. For the conversion outside of the cavity a several mm-long periodically poled SHG-crystal with additional narrow channel waveguide structure is used in order to reach the necessary power density for efficient laser light conversion.

Intra-cavity and extra-cavity approaches can produce MHz modulations speeds and operate over a wide temperature range. However, complex driving electronics are needed to drive these lasers efficiently.

Fig. 2 Ridge laser emission can support several lasing modes at 520nm in pulsed operation at 50mW output power at room temperature



The problems with nitrides

If nitride lasers are to replace the more complex diode-pumped, solid-state lasers and frequency doubled semiconductor lasers, then researchers must overcome the challenge of routinely producing high-quality InGaN-quantum wells with sufficiently high indium content. Extending emission from the blue to the green demands an increase in indium content in the InGaN wells, but this is hampered by a deterioration of the thermal stability of this layer, alongside higher compressive strain due to larger lattice mismatch [2, 3].

Our team of researchers at Osram has made an important breakthrough in this area - we were the first to break the 500 nm barrier [4]. Since then we have progressed to even longer wavelengths, including the realization of 515nm and 520 nm pulsed laser operation from broad, gain-guided test laser structures [5, 10]. Other researchers have also enjoyed success, such as Nichia, which has produced 8 mW continuous-wave operation at 515 nm from small ridge waveguide lasers.

Our lasers, and those developed by Nichia, are produced by growth on the c-plane of gallium nitride. One weakness of this approach is that high internal piezoelectric fields in the polar growth direction hamper the device performance. These fields can be either minimized or eliminated by turning to semi-polar and non-polar planes, respectively. Rohm has adopted this approach, and reported the longest lasing wavelengths for a laser on a non-polar m-plane GaN-substrate. It has developed a 499.8 nm laser with a very high junction temperature and 97% out-coupling mirror reflectivity [7]. Progress has also been realized by Sumitomo, which announced a 531nm broad gain guided test laser in summer 2009 that was driven in pulsed operation and grown on the semi-polar plane [2021]. Later that year this company reported continuous-wave operation up to 2mW from small ridge waveguide laser at 520nm on [2021]-plane [9]. Regardless of the growth plane, producing high material quality with a low defect density is a big challenge.

More recently we have managed to push our lasers to even longer wavelengths, and realized 526 nm emission from broad-area, test laser structures on c-plane GaN. Additional results include a 520 nm ridge waveguide laser with a record optical output power of 50 mW in pulse operation (Figs. 1 and 2). This optical power level is suitable for second-generation, red-green-blue scanning projection technology that can deliver an illumination level of about 10 lumen on the screen.

Our direct green 520 nm ridge laser was processed as a 2 μm broad stripe with a 600 μm resonator length, and it includes natural, cleaved laser facets with dielectric mirror coatings. The epitaxial structure consists of AlGaIn

cladding layers, GaN waveguide layers and an active region containing InGaN layers with different indium content on a c-plane GaN-substrate (Fig. 3). The laser characteristics include a threshold current of about 125mA, which is only four times the threshold level of currently available blue InGaN laser diodes.

Several hurdles had to be overcome to extend our lasers to 500 nm and beyond. Probably the biggest of these was improving the crystal quality of the high-indium-content quantum wells needed for green emission. The quality of this layer can be assessed with micro-photoluminescence mappings (fig. 4). The black spots in the left image of fig. 4 are areas of weaker green spontaneous photoluminescence emission, due to segregation of indium atoms.

A strong correlation exists between the formation of low spontaneous emission areas and high densities of non-radiative defects. The right image in fig. 4 shows an incredibly uniform green photoluminescence from a laser structure with higher crystal quality. Employing improved growth parameters and designs on c-plane GaN substrates formed this structure. No black spots can be seen, indicating improved crystal quality. This material produces devices with a higher peak gain for lasing.

The behaviour of our lasers is influenced by the strong piezoelectric fields within the quantum wells. The strain-induced piezoelectric fields and tilted energy potentials reduce the band gap. This is the so-called Stark-Effect. The lower band gap helps to reach the long emission wavelength without changing the material composition. However, lasers operate at current densities that are typically orders of magnitude higher than LEDs, which partially screen the internal fields, leading to a blue shift of the laser emission wavelength (Fig. 5 right). However, if the laser threshold current can be reduced, the Stark-Effect in the polar growth direction can be used to shift the laser towards longer wavelengths without increasing the indium-content in the $In_xGa_{1-x}N$ quantum wells.

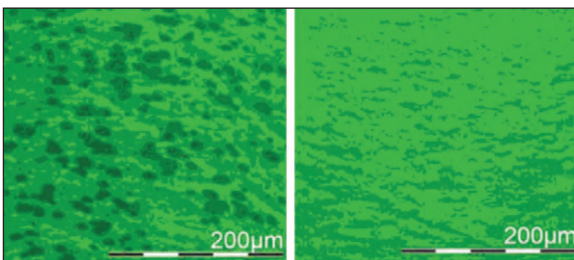


Fig.4. Micro-photoluminescence mappings reveal the quality of the quantum well layers. Left: Lower material quality, including dark spots due to indium-segregation. Right: Uniform green photoluminescence emission of InGaN quantum wells with higher material quality

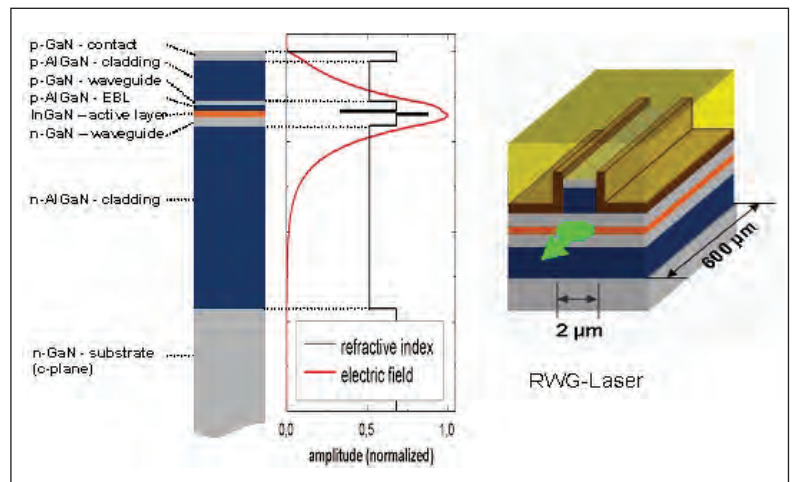


Fig.3. Osram's green-emitting laser is a conventional ridge laser design that includes GaN waveguides, an AlGaIn electron-blocking layer and AlGaIn cladding layers

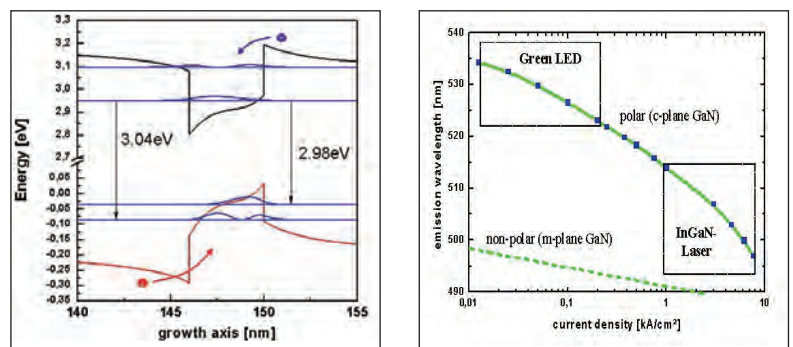


Fig. 5 Left: The piezoelectric fields in polar material alter the conduction and valence band profiles of the within InGaIn-quantum wells (left). Carrier separation at the quantized band states is indicated by the calculated carrier envelopes, which show a reduced electron-hole overlap compared to a rectangular quantum well profile (not shown here). Right: Increasing the current density of a polar green InGaIn-based LED to values needed to drive a laser produces a large blue-shift in the spontaneous emission wavelength. Nitride lasers with similar indium-content in the quantum wells that are grown on non-polar substrates produce a far smaller variation in emission at shorter wavelengths (dashed line)

Alternative approaches to reducing the internal built in piezoelectric fields are based on semi-polar or non-polar GaN substrates. However, lasers grown on non-polar m-plane GaN substrates currently suffer from poor material quality of the high indium-content layers needed to produce green emission.

Although there are issues affecting all forms of nitride laser, this should not obscure the tremendous progress made with green lasers over the last year or so - it is now

possible to produce directly emitting green lasers at wavelengths of 515nm and beyond on polar and semi-polar planes. Future goals include improvements in the material quality of the quantum wells. If success follows, small laser chips could replace the bulky, complex devices currently used to provide a green laser source.

● The German Federal Ministry for Education and Research (BMBF) supports the research activities on blue and green InGaN lasers within the project MOLAS (FKZ 13N9373)

Applications served by green lasers

With a photopic response of about 600lm/W, the green wavelength is ideal for applications where a laser beam or beam pattern is used to visually align, level or position. In comparison, commonly used red laser diodes have a significantly inferior photopic response, and this that means that roughly four times the laser output power is necessary to achieve the equivalent level of brightness of a green laser, which is a major impairment to eye safety. Although high absolute output power is not that critical in these applications, a large operating temperature range, high efficiency, ruggedness and simple control are key requirements, especially for portable, battery-powered leveling or positioning in construction and industrial environments.



Embedded laser projector with red, green and blue lasers. Credit: MVIS

image can be displayed on arbitrary surfaces without focusing. Further advantages of laser based projection displays are high system efficiency, because lasers emit polarized light and have, by nature, a very low etendue. Optics can also be less complex compared to other light sources enabling significantly smaller display engines. Due to the monochromaticity of lasers the color gamut is superior to any other projection technology. Implementations of laser projection displays can be found in pico projectors and rear-projection TVs, and they will soon appear in head-up displays in cars.

Color displays

Green lasers are also an essential component in any form of full color projector. Here red, blue and green lasers are used together to either directly scan a picture, or to project a picture by backlighting a micro display. If a micro-display approach is used, the imager is sequentially illuminated by these three laser sources and the monochromatic picture (color by color) is projected through an optical system. Usually it takes 4 ms to produce a single frame, which is one monochromatic picture, so it follows that the laser must be modulated in the kHz range.

Another display technology is the laser scanning beam projector, which is based on a fast deflecting MEMS-based micro mirror. The system works by scanning the entire picture a pixel at a time and modulating the laser directly at 10-100 MHz, much like the electron beams in a cathode ray tube used in a home TV. "Gray scales" are realized by amplitude modulation of the lasers. Lasers with excellent beam quality are needed to serve this type of projector, due to the small diameter of the micro mirror and the influence of the spot size on picture quality. No conventional imaging optics is needed, so the

Medical treatments

Green lasers are ideal for a wide variety of medical applications because this wavelength is absorbed by oxyhemoglobin and melanin, and by pulsing this source it is possible to ensure that thermal damage is confined to the targeted tissue or vessel by selecting a pulse length and duty cycle that enables the targeted area to cool down between pulses.

In Europe and North America the most common cause for blindness is diabetic retinopathy, which results from diabetes mellitus, and can be controlled with laser eye treatment. This eye condition is caused by a lack of oxygen in the retina, which stems from vessel damage associated with poorly controlled blood-sugar levels. Unwanted new blood vessels can then start to spread onto the retina and into the vitreous humour - the clear gel that fills the space between the lens and the retina of the eyeball - but this can be prevented by treating the eye with a green laser.

A technique known as panretinal laser coagulation is used on a large area of the retina to create 1000-3000 burn spots that can reduce the overall oxygen demand, thus supporting the still healthy parts of the retina.

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*Multi-junction solar cells are being deployed in concentrator photovoltaics systems, such as the one that is being built by Concentrix.
Credit: Concentrix*

Stacking sidesteps the strain in multi-junction cells

If terrestrial concentrator photovoltaics are to enjoy significant commercial success then electricity generation costs must fall. One way to do this is to improve the design of the cell with a stacked architecture that eliminates strain and current matching issues, according to **IMEC's Giovanni Flamand**.

The solar industry is changing. Although silicon is still the dominant material for solar cell manufacture, alternative technologies like thin-film and concentrator photovoltaics (CPV) are emerging. The latter of these promises to excel in sunnier climes and involves the focusing of incident sunlight onto cells with a typical area of just 10-100 mm². By focusing the light by a factor of several hundred, it is possible to minimize the total expenditure on these relatively expensive cells, and ultimately realize an acceptable cost-per-Watt at the system level.

Generating costs for CPV systems are also influenced by the efficiency of the cell. Single-junction solar cells are inappropriate, because they are limited to a theoretical maximum efficiency of about 30 percent, due to thermalization and transmission losses. In comparison, multi-junction cells can produce far higher efficiencies, because they cut thermalization losses by using several cells to absorb different parts of the solar spectrum.

Today the dominant multi-junction solar cell technology is the monolithic triple-junction (InGaP/(In)GaAs/Ge) solar cell that was originally developed and commercialized for space applications. These devices feature In_{0.5}Ga_{0.5}P, In_{0.01}Ga_{0.99}As and germanium cells that are lattice-matched to a germanium substrate to ensure excellent material quality and photovoltaic performance.

The conversion efficiency record for a multi-junction cell under concentrated irradiation has been broken on several occasions over the last few years. Spectrolab has made the most recent claim for the record, and in August 2009 it announced an efficiency of 41.6 percent, which was achieved under a concentration of 364 suns. But this record may not last for long because further improvements in monolithic multi-junction cells are expected. These could come through either adding more junctions to the stack, or using lattice-mismatched solar

cells. In the latter case, cell compositions are modified to yield a superior combination of bandgap energies. The downside of this approach is that each cell differs in its crystal lattice spacing, so additional buffer layers are needed to pin the crystallographic defects and prevent them from degrading the performance of the active layers.

Regardless of the form of monolithic multi-junction solar cell, current matching between different cells is essential, due to the inherent series connection of these integrated devices. In addition, there is a need for tunnel junctions, which are applied to electrically connect the different cells in the stack. These junctions can handle the high peak tunneling currents.

In real-life CPV applications there is an additional complication too - non-uniform illumination levels on the solar cell. This may lead to local current densities exceeding the tunnel junction design value, and ultimately higher resistances and voltage losses. Deviations in the spectral distribution of the incident sunlight occur all the time, because they depend on changes in geographical, seasonal, daily and climatic conditions. This makes it very tough to current match cells for optimal energy yield, and

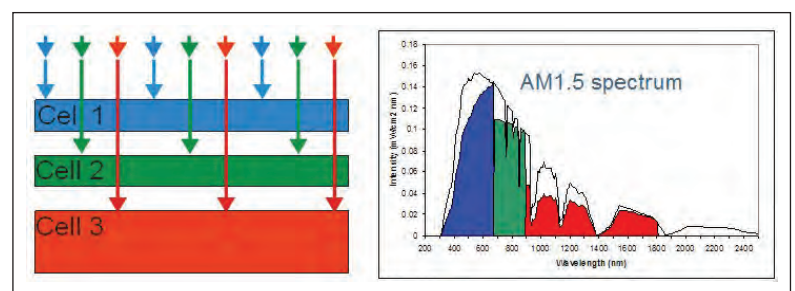
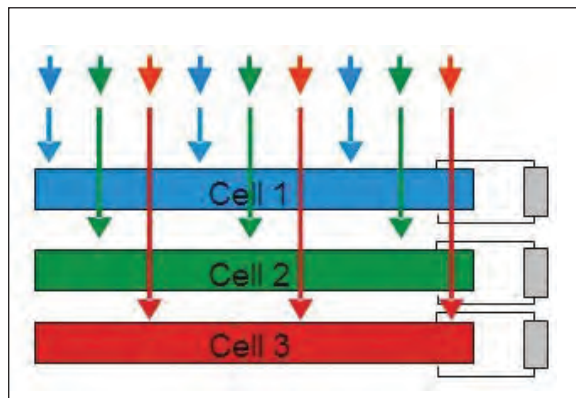


Fig.1. Multi-junction cells deliver higher efficiencies than single-cell equivalents by using materials with differing bandgaps to absorb different parts of the solar spectrum. This approach reduces thermalization losses

Fig. 2. Mechanically stacked junctions employ an electrical contact for every junction. Thanks to this approach, there is no need to current-match the junctions, or use tunnel diodes



imposes very stringent requirements on cell design for specific operating conditions and locations. The latter of these also needs to be very well documented.

Stacking cells: pros and cons

A promising alternative to these monolithic cells is a mechanically stacked multi-junction architecture. With this approach, different single-junction solar cells are integrated by mechanically placing them into a stack, such that each cell absorbs a different part of the incident spectrum (figure 2). Each of these cells has a separate electrical contact. This means that they do not have to be connected in series, which is a massive benefit because it removes the need for tunnel junctions and current matching.

Eliminating the need for current matching also produces additional, important advantages – it allows full exploitation of the power generated by every cell within the device, and it creates an inherent robustness against variations in the spectral distribution of the incident light. What's more, this approach offers the freedom to realize any combination of cells with different energy bandgaps, without the need to worry about lattice-matching issues.

However, all of these advantages have to be weighed against three specific challenges associated with mechanically-stacked solar cells that have hampered progress by their developers, and prevented commercialization: bulkiness; a complex electrical architecture; and optical coupling requirements.

Bulkiness is to a certain extent inevitable, due to the use of different solar cells and their associated substrates in a mechanical stack. In addition, multiple substrates push up

costs. Specifically for CPV applications, the thermal mass of the full mechanical stack also offers a major challenge concerning heat dissipation.

The second issue, the complex electrical architecture, stems from the need to provide individual electrical interconnections to every cell. This can be addressed at the system level with an intelligent string and inverter design (a string is a number of individual cells that are series connected by external circuits to obtain a larger DC output voltage, which can then be converted to an AC source for the grid with an inverter). However, this does not eliminate the need to integrate electrical leads on every cell in the stack, which has a major impact on cell and stack development and technology. This is especially a concern for cell interconnects that need to be placed on one of the intermediate cell surfaces within the stack.

Compared to its monolithic cousin, a mechanically stacked multi-junction solar cell has additional surfaces and interfaces, and it requires additional adhesive layers in between the different cells. These increase the number of sources of optical loss, which might have an important impact on the final performance of middle and bottom cells in such a stack. Moreover, in order to fully transmit the non-absorbed light from an upper cell to the ones beneath it in the stack, the higher cell must be optically transparent to its sub-bandgap radiation.

Efforts at IMEC

At IMEC, which is based in Belgium, I am working with several other researchers to develop mechanically-stacked solar cells that address the above-mentioned problems. We hope that our efforts will ultimately enable these devices to fulfill their high-efficiency potential and deliver the benefits associated with their inherent robustness to spectral variations.

The technologies used to produce these cells are compatible with high-throughput manufacturing. Specifically, a mechanically stacked triple-junction InGaP/GaAs/Ge cell is under development, exploiting the same sub-cells employed in current state-of-the-art monolithic cells.

In the proposed configuration, the InGaP and GaAs subcells are processed such that the germanium substrate, onto which the epitaxial layers are deposited, is removed. In this way, an InGaP cell with a typical thickness of about 1 μm and a 3-4 μm thick GaAs cell

Bulkiness is to a certain extent inevitable, due to the use of different solar cells and their associated substrates in a mechanical stack. In addition, multiple substrates push up costs. Specifically for CPV applications, the thermal mass of the full mechanical stack also offers a major challenge concerning heat dissipation

can be stacked on a separately realized germanium bottom cell. This architecture will allow the extraction of the full current generated by the germanium cell, which is not the case in a monolithically stacked triple-junction cell.

Removing the substrates from the top and middle cells should lead to easier transport of excessive heat towards the heat sink. A further benefit is that it allows interconnection of the contact grids of the different cells from the stack's front or rear side. This makes the electrical design less complex, opening the door to stacked cell processing on the wafer scale, which is a key element in upscaling this technology for the production of high-efficiency concentrator cells.

Final integration of the individual cells into a mechanical stack also requires know-how and tools from the semiconductor manufacturing industry, specifically 3D-stacking expertise, an area of technology where IMEC has considerable strength. Adopting this approach will produce high-quality bonding, integration and interconnection processes, while also offering the possibility to perform high-accuracy alignment of the different cells in the stack. This should result in a good alignment of the different contact grids applied to the front and backside of the individual cells, such that optical coupling between the different cells in the stack is not hampered by unwanted additional shadowing losses due to the contact structures.

Prototype progress

One significant step towards the fabrication of this triple-junction stacked cell has been the fabrication of a dual-junction version based on GaAs and germanium. This has been made by combining 4 μm , one-side-contacted GaAs solar cells and separately connected germanium solar cells. The thinned-down GaAs solar cells were bonded on top of the germanium solar cells using silicone sealant. Transmission measurements on a layer of this sealant with relevant thickness ($\sim 20 \mu\text{m}$) revealed that the transmission loss through this layer is limited to 3.5 percent in the 900-1800 nm wavelength range.

The presently realized mechanical stack (figure 3) employs individual GaAs and germanium cells that have a non-matched cell area and contact grid design. This means that the longer-wavelength portion of incident light that passes through the GaAs cell is not optimally coupled to the underlying germanium cell. Performance is also compromised by the absence of an anti-reflective coating at the rear of the GaAs cell that limits the transmittance of infrared radiation to the bottom cell. But the good news is that the applied technologies for thinning down the GaAs cell and bonding it on top of an active germanium solar cell are readily applicable in an optimized, stacked-cell design.

We have found that thinned-down, one-side-contacted GaAs cells integrated in the mechanical stack exhibit

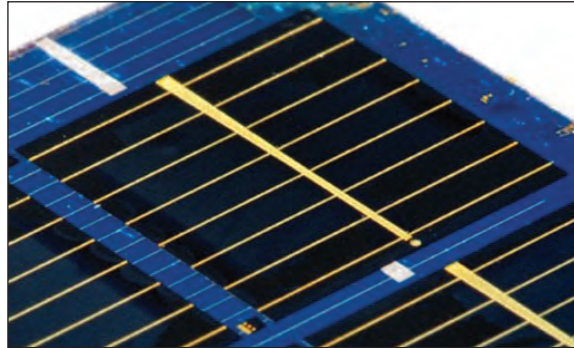


Fig.3. IMEC has already built a mechanically stacked dual-junction cell based on GaAs and germanium. The next goal is the addition of an InGaP top cell

identical results to those obtained previously on similar stand-alone cells. They can produce conversion efficiencies exceeding 23 percent (1 sun, AM1.5), close to our institution's best results for regular GaAs solar cells on a germanium substrate of 24.7 percent. The main limiting factor for the one-side contacted GaAs cells is the relatively low fill factor. This is caused by the use of the two-point measurement method during 'I-V' characterization, which is imposed by the small available area for contacting the rear-side grid in the present configuration.

The separately contacted germanium bottom cell in our stack exhibits a conversion efficiency of almost 2 percent (1 sun, AM1.5). The low efficiency can be attributed to the absence of an anti-reflective coating at the rear of the GaAs cell, and the use of a non-optimized coating on the front side of the germanium cell. Applying an optimized coating to both these surfaces should lift the efficiency of the germanium bottom cell to approximately 3-3.5 percent, which is well above the contribution of the germanium cell in conventional triple-junction cells.

Future work

Efforts will now be directed at increasing solar cell performance through the reduction of reflective losses at different cell surfaces and matching of the area and contact grid of the III-V and germanium cells. The bonding process demands high-accuracy alignment of the different cells' contact grids, which can be realized with flip-chip bonding, according to scanning acoustic microscopy measurements. When an ultra-thin, one-side contacted InGaP top cell is added to the structure, this should yield mechanically stacked triple-junction solar cells for CPV applications that feature efficiencies of around 40 percent and enhanced spectral robustness.

Finally, it should be noted that the application of a contacting layout that makes the contacts of all cells in the stack accessible from the stack's front and rear surfaces - as demonstrated in the present work - is instrumental in allowing wafer-scale processing of the full mechanical stack right up to the final step. This way, dicing to individual solar cells can be performed as a last step, right before cell laydown and interconnection.

Larger wafers can spur further growth of the LED industry

LEDs are making inroads into the backlighting of LCD TVs and general illumination. Further success hinges on reducing the cost per lumen, and this can be realized through a move to growth on larger sapphire or silicon substrates, argues **Aixtron's Rainer Beccard**.

Today, the high-brightness LED market is enjoying its strongest boom since the market first emerged. After initially being used for mobile phone illumination, it is now appearing in the back light units (BLUs) required for notebook PCs and, more recently, it is being deployed in large area LCD TVs, which will shortly become the dominant application for the market. Furthermore, even the holy grail of lighting applications appears at long last to be becoming accessible, thanks to the rapid improvement of white LED efficacies.

The continuation of this success story, however, still requires significant improvements of LED cost (or, to be more precise, an improvement of cost per lumen). Consequently, LED manufacturing processes have to be continuously improved in order to reduce the production cost and related to that need, MOCVD development also has to focus on reducing the operating cost when growing LED structures.

This cost reduction can be achieved by various means. One route is to develop MOCVD reactors that accommodate even more wafers of the same size, thus increasing the throughput. This is precisely what has been done in terms of reactor development since the early 1990s. As a result, each new reactor generation has been significantly larger than the previous one while the purchased cost has increased only moderately. However, there are some practical limitations to this scale-up process that encourage MOCVD reactor manufacturers to look for other, more intelligent ways, to reduce the LED production costs.

To understand the anticipated future development of the III-V industry - and in particular the LED part of it - it is helpful to take a look at the history of the silicon industry. In that industry larger and larger wafer sizes have played a crucial role in reducing the manufacturing cost of silicon devices and fundamentally this should be very similar in LED manufacturing.

What could be the benefits of moving to larger wafers in LED processes? First of all, using larger wafers in MOCVD reactors results in an increase in the usable wafer area per run. Looking at the typical geometry of an MOCVD reactor, it becomes obvious that a bigger part of the available reactor area can be better utilized when switching to large wafers. Furthermore, a relative reduction of the unusable edge area that has to be excluded from further processing is also achieved. The costly metal organics and hydrides would also be better utilized and finally all the subsequent process steps beyond the MOCVD process will enjoy improved yields.

The advantage of employing large wafers can be revealed with some simple calculations (Table 1). Looking at one of

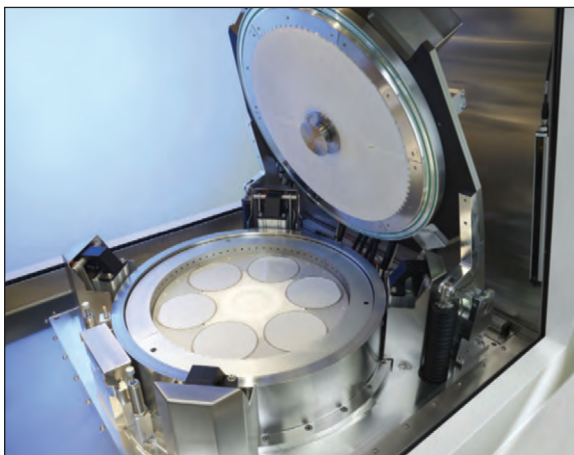


Fig. 1: Aixtron 2800G4 HT reactor in 6x6-inch configuration



SICK C 2000

CRIUS reactor after the growth of an LED structure on a 200 mm sapphire wafer

the MOCVD workhorses of the LED industry today, the AIXTRON 2800G4 HT, one may first calculate the total wafer area that can be loaded into the reactor (for the “standard” configuration of 42x2-inch wafers and the respective 4-inch and 6-inch configurations). In a second step, a certain amount of rim area (which is usually excluded from the usable area) is taken into account additionally. Finally, the gained usable area is calculated compared to the initial 42x2-inch configuration.

The potential result is impressive – 53% of the usable wafer area can be gained by simply moving to larger 6-inch wafers and most importantly – there is not a significantly high cost related to the conversion of a 2-inch reactor to a 4-inch or 6-inch configuration. Although the prices for 4-inch substrates today are now in an acceptable commercial range, the prices of 6-inch wafers are only just beginning to move downwards as the initial volumes begin to rise.

Looking at these economics, it may appear surprising that most of the GaN epitaxy is still performed on 2-inch sapphire wafers and indeed recently, many of the larger GaN LED manufacturers have started to convert their volume production over to 4-inch substrates when buying new systems for increased capacity.

Whereas we know that changing to 6-inch substrates clearly will be the next step for the industry, the decision to initiate this transition will depend on sufficient substrate availability and commercially viable prices. However, when that time arrives, the reactor technology needed is already

Configuration	42x2"	11x4"	6x6"
Total wafer area (cm ²)	851	891	1094
Total usable area (cm ² , 3 mm rim excluded)	662	789	1009
Gain compared to 42x2"		19.3%	52.6%

Table 1. The benefits of larger wafers

there when customers decide to convert or buy 6-inch wafer configurations.

For those who do decide to convert; all that is required is a simple exchange of each of the six 7x2-inch satellite disks in a 42x2-inch configuration in a AIX 2800G4 HT over to 1x6-inch disks (Fig.1), converting the reactor to a 6x6-inch configuration.

Theoretically, as the reactor geometry has not been changed, there is also a need to adjust or modify the process. When the conversion is complete, the process results are impressive. Uniformity levels are achieved that lead to significantly improved yield (see Fig. 2). Looking further ahead, 6-inch wafers might not be the final limit. Some early 200 mm sapphire substrates are already available today, and some initial studies into the MOCVD growth on such wafers have already been carried out.

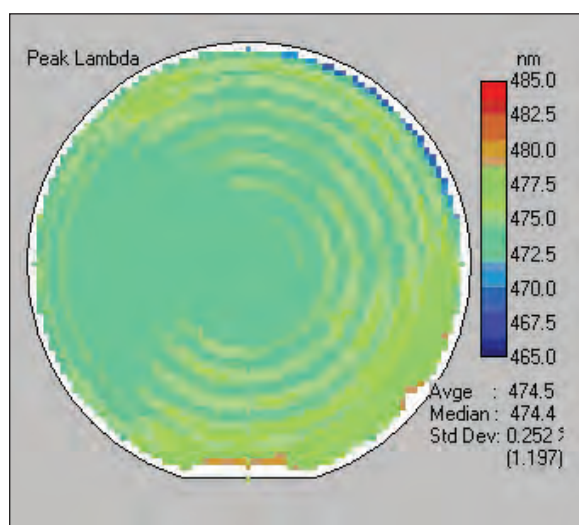


Fig.2: PL uniformity of a GaN/InGaN MQW grown in a 6x6-inch configuration. Standard deviation of wavelength is 1.2 nm

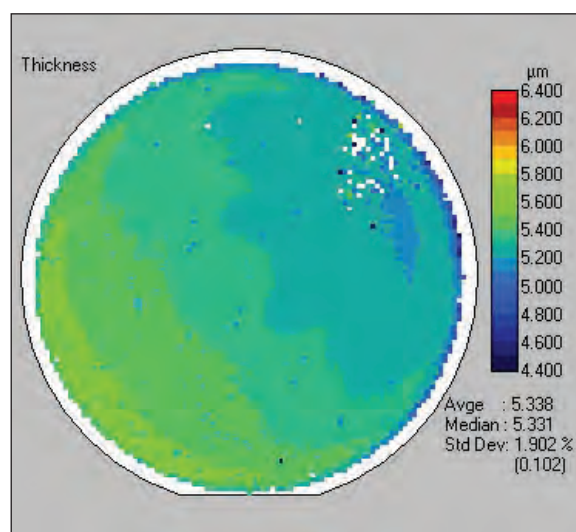


Fig. 3: Thickness uniformity map of a GaN film on 200 mm sapphire substrate. Standard deviation of thickness is 1.9%

Interestingly enough, MOCVD growth platforms for these much larger wafers do already exist. The CRIUS Close Coupled Showerhead Reactor is one of the widely used reactor types for LED manufacturing, and although today it is usually run in a 31x2-inch configuration, the geometry of this reactor can be easily converted into a single 200 mm or even a 300 mm setup. The 200 mm setup was used to perform GaN LED growth experiments. Thickness uniformity of less than 1.9% (std. deviation) was achieved on a 6-inch wafer (Fig 3; 6 mm rim excluded).

Delivering GaN processes on 200 mm substrates hints at another potential route to cost efficient manufacturing - the use of silicon substrates. Silicon is available at a much lower price level compared to sapphire, and is readily available at a commercially attractive price up to 300 mm in diameter. Consequently, GaN-on-silicon processes have been investigated for quite some time.

Although the target applications during the last few years were GaN based electronic devices rather than LEDs, in 2008, a partnership between IMEC (Belgium) and AIXTRON resulted in a successful demonstration of 200 mm GaN/AlGaIn MOCVD growth on (111)-oriented silicon (reported at IWNS 2008).

To achieve this result, a variety of fundamental physical problems had to be overcome. GaN/Si wafers suffer from a significant mechanical strain that is caused by the lattice mismatch between substrate and epilayers, different thermal expansion coefficients and thermal gradients through the wafer.

This usually results in bowing, which is even more pronounced the larger the wafer size. The bowing effect can lead to non-uniform wafer temperatures during the growth process, which would inevitably result in non-uniform film properties.

Not all is lost though as there are ways to manage these issues. Key to this is the use of in-situ monitoring of the layer growth during the growth process, which then allows the adjustment of the layer structure and the process to minimize strain and bow.

The in-situ monitoring tool employed here was the ARGUS mapping system. In this device, a set of photo diodes monitors the light emitted from the wafer surface

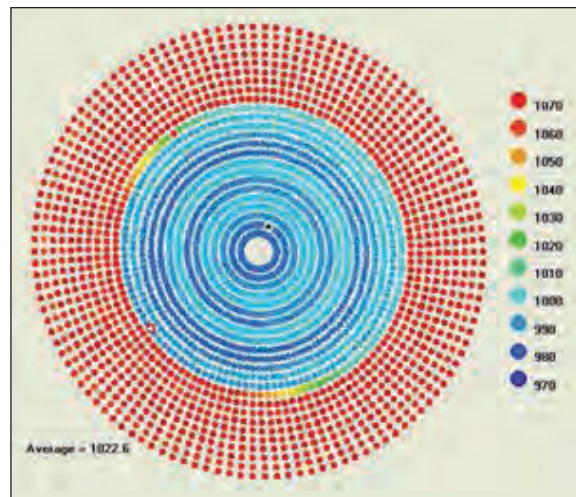


Fig. 4: Temperature profile of a 200 mm GaN/AlGaIn/Si wafer measured by ARGUS. The red dots indicate susceptor area without wafer; the blue dots represent wafer area

along the susceptor radius. As the susceptor rotates, a thermal image of the entire wafer surface (and the susceptor area beyond the wafer) is obtained (Fig. 4). This temperature map is finally used to optimize growth conditions.

The growth results clearly show that GaN/Si processes can be run in a stable and well controlled manner with excellent uniformities (e.g. thickness uniformity of GaN/Si $\sqrt{\sigma} < 0.5\%$). Theoretically, such processes could also be carried out on 300 mm silicon wafers in the same way; the only limitation up to now, is the fact that the required 111-oriented silicon substrates are not available yet.

In summary, switching to 4-inch and 6-inch GaN LED processes is the most immediately realistic opportunity to increase the productivity of HB-LED manufacturing. For MOCVD as the key manufacturing step, the technical risk and the cost related to the conversion to large wafers is very small. The availability of substrates and their cost are likely to be the key parameters that determine the speed of this conversion.

Employing silicon instead of sapphire is an interesting longer-term route to reduce manufacturing cost further, as complex processes on wafers up to 300 mm will become commercially feasible. However, a significant improvement in the efficiencies (lm/W) of LEDs grown on silicon will be required to become competitive with established sapphire based LEDs.

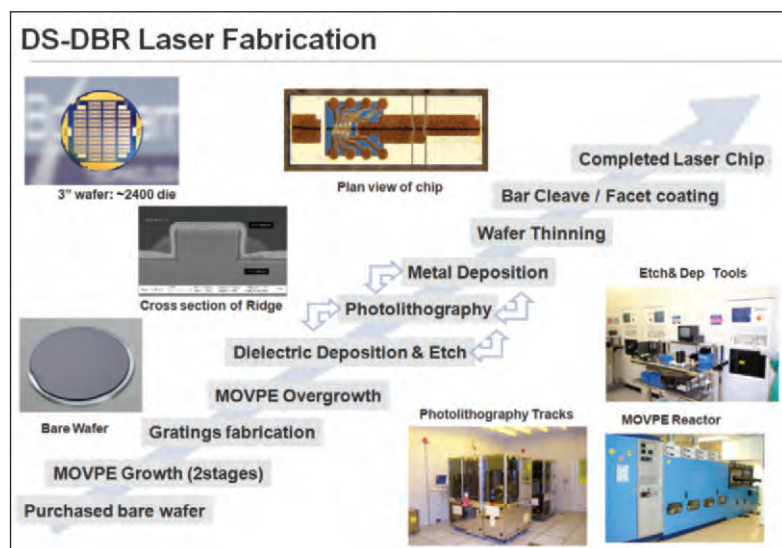
Employing silicon as a substrate instead of sapphire is an interesting longer-term route to reduce manufacturing cost further, as complex processes on wafers up to 300 mm will become commercially feasible

Unlocking the Value of Fab Ownership

The benefits of fab ownership will increasingly outweigh the disadvantages as component manufacturers meet the challenges of lower cost and higher transmission speeds by pushing design and test complexity back to the chip level argues **Oclaro's Andy Carter**.

Fab or Fabless? The question has been asked many times over the last ten years by everyone seeking to make compound semiconductor optoelectronic devices. There is no doubt that the era has passed when the first item on a start-up shopping list was a fabrication facility....but what about companies with well established fabs, such as Oclaro? Are their fabs cash and overhead drains, or are they the key to deliver growth and profitability now that the market is warming up and many component requirements are still differentiated on performance and footprint? The view of the management at Oclaro is that fab ownership offers compelling advantages, and once a certain scale is reached, it is highly differentiating and cost effective. In addition, it acts as a significant barrier to entry for other players.

Fig 1: Fabrication process for the Oclaro DSDBR laser involves three growth stages



Why have a fab?..

Owning a fabrication facility is expensive, and significant volume and scale are needed to allow cost recovery and profitability. Many companies have sought ways of reducing this overhead by outsourcing fabrication, giving quick benefits to the bottom line. However, several aspects of the industry are now changing, and we believe this alters the balance significantly.

There has been and continues to be consolidation, so fewer players are driving higher volumes through their facilities. In addition, many applications are demanding significant levels of photonic integration – not necessarily large scale multi-channel photonic integrated circuits (PICs), but integration of a number of elements, such as lasers, monitor detectors and modulators to drive down footprint and cost whilst delivering best in class performance at the right module level cost point. Component companies seek differentiation in cost, performance and time to market. Ownership of a fab must enable all three aspects to be of full benefit. Time to market benefits can be achieved through utilisation of common and verified building blocks and processes with which devices are built. This is increasingly important, as higher levels of integration are required to meet the functionality demanded.

At Oclaro, we have adopted such an approach to integration. We utilise multiple 'etch and regrowth' processes to fabricate components – three in the case of a tunable laser and five for integrated laser modulators. Such an approach to device fabrication is often targeted for avoidance by outsource advocates, due to complexity and yield issues, whereas our investment in processes and procedures, such as regrowth initiation and surface

cleaning, ensure that yield is maintained even for the most complex processes.

An advantage of such an approach is that no compromise need be built in to the actual design – the best semiconductor structure can still be independently used for a waveguide, laser active region and modulator. We believe this compares very favourably with the alternatives, which use processes such as QWI (Quantum Well Intermixing) or vertically coupled waveguide structures to achieve multi-element functionality. The 'etch and regrowth' methodology gives virtually complete flexibility in design, as well as allowing smooth introduction of improved processes.

Large compound semiconductor fab. costs are typically several million dollars per quarter, so it is useful to ask at what level the fab becomes 'profitable' to the company. A reasonable 'rule of thumb' might be when the fab supports revenue of five to ten times the overhead cost, but as the level of functionality at the chip level is enhanced, the effective 'value' of the chip within the product significantly increases.

For the latest generations of components, such as tunable transmitters, the costs are already favourable, and set to become increasingly so. We are now getting to the point where the incremental cost of the chip fabrication is becoming dominated by materials and direct labour rather than overhead.

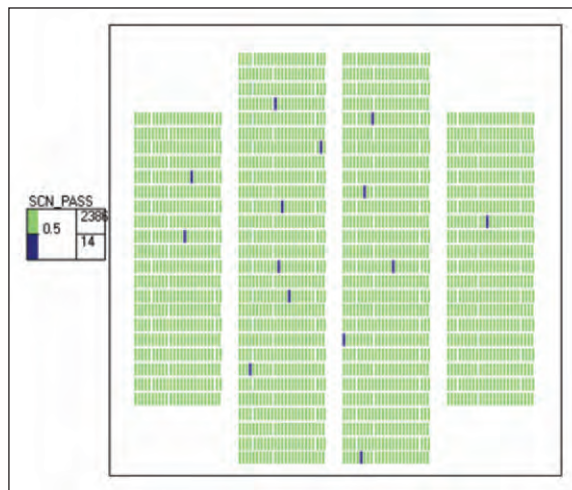
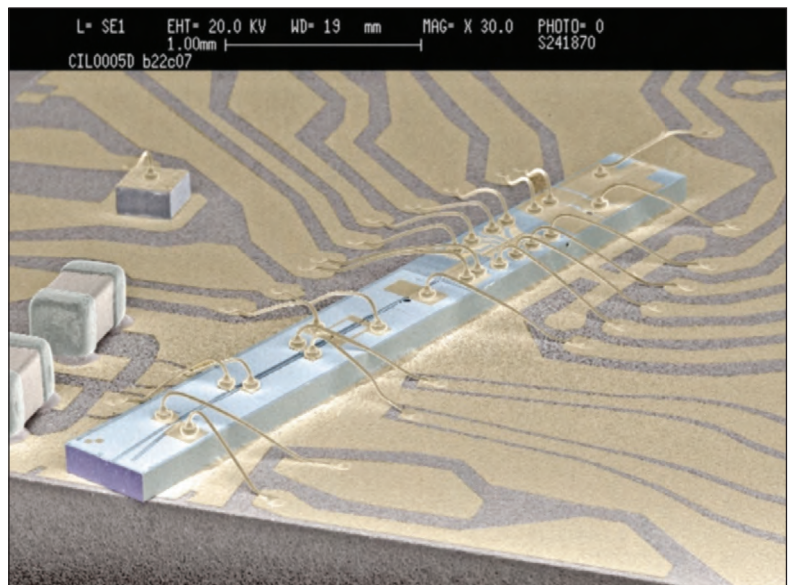
There are perceived advantages to outsourcing in some areas, such as process flexibility, as foundries must support different processes and materials for a wide range of customers. Initial entry costs are low, and capital requirements for the user are minimal. Many of the problems – such as design and IP protection can be managed, provided appropriate controls and procedures are put in place.

The outsource model requires more emphasis on design IP, whereas insourcing enables more leverage from process IP and knowledge. For low volume and start ups, outsourcing is attractive; the barriers come in scaling this to global volume requirements the industry demands.

Oclaro fabs....

Oclaro owns a number of fabrication sites, including facilities for Lithium Niobate, Thin Film filters, Liquid Crystal (as part of the recent Xtellus WSS acquisition) and two major compound semiconductor fabs, at Zurich, Switzerland, and Caswell in the UK.

The two compound semiconductor facilities differentiate in



(Above) Integrated Tunable Laser Mach Zehnder modulator chip for Tunable XFP module testing (Left) On-wafer test map of tuneable lasers

the materials and applications: the Zurich facility is used for the fabrication of high power pump and industrial lasers as well as VCSELs based on GaAs; the Caswell facility focuses mainly on InP based devices as well as providing additional capacity for industrial lasers. Base material growth is by MBE exclusively for pump lasers (Zurich) and by MOCVD (InP and GaAs) at Caswell.

The other Oclaro fabrication facilities are somewhat smaller scale, more specialist and largely independent of the two major fabs, except in aspects of management and best practice sharing. The availability of both InP based and Lithium Niobate (LN) modulator technologies within Oclaro is advantageous and cost effective, with the LN devices appealing as a 'component' play whereas InP is

Bandwidth demand continues to grow exponentially, with steadily reducing revenue per bit . Key attributes of the emerging infrastructure include: packet friendly common infrastructure; converged voice, data & video; zero touch service provision; lower operating costs; node consolidation; scalable service speeds; scalable service level agreements; and increased capacity

very attractive as an integration platform and for PICs. The process complexity of the GaAs based lasers is relatively low compared to that for the InP based devices and circuits, so the article here will focus on the latter, particularly with reference to the more complex integrated devices that are manufactured.

Needs and Differentiators...

Critical to unlocking the value of fab ownership is deciding what the device and circuit demand might be. Our transmission business primarily concentrates on the DWDM space, for long haul and Metro applications.

Bandwidth demand continues to grow exponentially, with steadily reducing revenue per bit. Key attributes of the emerging infrastructure include: packet friendly common infrastructure; converged voice, data & video; zero touch service provision; lower operating costs; node

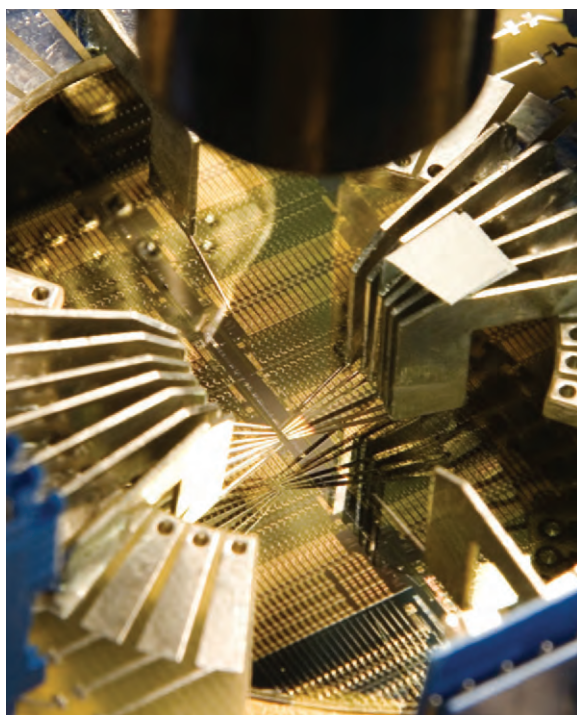
consolidation; scalable service speeds; scalable service level agreements; and increased capacity.

Taking all these together we see a trend to the implementation of an intelligent photonic core, with a reconfigurable optical add-drop multiplexer (ROADM) interconnected mesh topology; full band tunability is critical, with primary capacity per wavelength increasing from 10 to 40 and 100Gbps. More complex modulation formats, including RZ-DQPSK at 40Gbps and coherent PM-QPSK for 100Gbps are increasingly required to allow for upgrades to existing 10Gbps routes using installed fibre plant and to cost reduce new build by transferring dispersion management from the optical domain into the electronic using DSP and coherent detection.

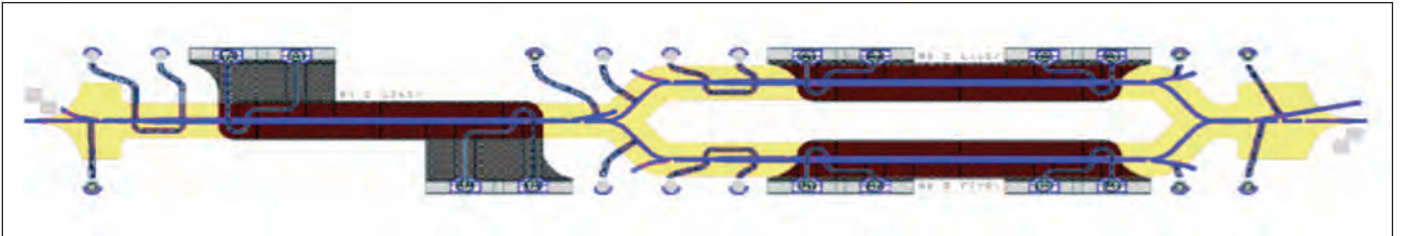
For all these requirements, photonic integration is a key enabling technology for cost and footprint reduction. The challenge is to 'print' the complexity through photonic integration and achieve the scalability through batch processing of wafers. Moving further towards the edges of the network, low cost provisioning of 10G DWDM tunable links in as small a form factor as possible – XFP, SFP+ and pluggable multichannel will be increasingly important. Again, photonic integration is a critical enabler here, backed up by other assembly technologies..

As access and backhaul demands rise, enhanced passive optical network (PON) technologies will be required, which may see demand for low cost tunable lasers rise to commodity levels; we are already studying the implications and network requirements for this. Opening up such applications would require a very low cost tunable device, suitable for deployment in a 'colorless' optical network unit (ONU). Part of such a strategy would demand minimal testing – which is a significant cost driver when devices must be calibrated and guaranteed for frequency stability to Telcordia requirements. Such an application would drive extremely high volume, in the millions per year.

InP-based photonic integration must enable both speed enhancements and cost reduction, whilst retaining full band



Automated on wafer testing of ILMZ chips for Tunable XFP



flexibility through tunability. Examples of components and circuits which we are expanding capacity include 40 Gbit/s integrated modulators, components for coherent (40, 100 Gbit/s) receivers and reduced cost tunability for 10 Gbit/s, based on T-TOSA or T-XFP formats.

The fabs must allow rapid scalability to meet demand, so yields of circuits such as the ILMZ are critical. We are addressing this through process standardisation, control and monitoring. Batch level automation of processes ensures scalability as well as allowing flexibility and capacity to develop next generation technologies.

Looking forward

We believe that we are now entering a critical phase for optoelectronic semiconductor device development – as more functionality and demands are being pulled back to the chip level, the need to control the chip design, development and timescales is becoming increasingly critical. The industry must grow and make sufficient cash to ensure the next generation of technologies – such as 400 or 1000GbE – can be developed and manufactured at suitable cost. This is driving investment now in basic 'building block' technologies and will soon demand further investment in next generation fabrication facilities.

We are starting to ask the questions about how the industry might evolve over the next 5 – 10 years. Will the next generation of photonic fabrication facilities be affordable, even with further industry consolidation? How large will the global requirements for integrated InP optoelectronic circuits become, and how many wafers (3 or 4") would this require?

If it were possible to set up a complete 'foundry' design and fabrication model, would this enable adjacent markets for photonic devices and enable more rapid value growth in the current markets?

To help answer these questions we are working with a number of partners in European (EC) Framework 7 projects such as 'EuroPIC'. Already external organisations such as Technical University of Eindhoven (TU/E) are designing devices and circuits for fabrication in the Oclaro Caswell facility. There is difficulty here – with the key IP strength moving from process to design.

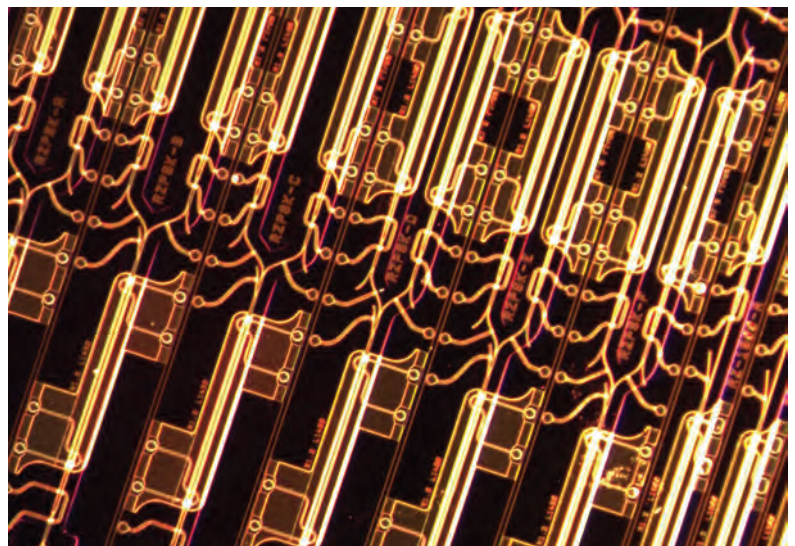
A key enabling factor will be the establishment of qualified device platforms on which designers can create their circuits. In the silicon microelectronics world, no circuit designer would ever question the design of the underlying transistors and resistors – he or she works at a higher level. Standardization of process allows the fab owner to achieve high volumes and establish a virtuous circle of improvement in process capability and production yields.

Furthermore, by establishing qualification at the platform level ('capability' qualification), the designer will be relieved of a major burden in the product development cycle in qualification and reliability proving at the level of individual designs. This way of working is routine in the silicon microelectronics world but in photonics it is new. It will need new ways of working on the part of designers and fabs – and could stimulate new opportunities for fabless design houses and manufacturing companies. It will also require greatly enhanced computer aided design capabilities to support circuit-level optical design.

However this may evolve, we believe that ownership of fabrication facilities and processes right now gives the best possible platform for growth and differentiation in the industry, as well the opportunity to rapidly scale as the insatiable demand for data transmission continues.

Integrated 3 element RZ-DQPSK modulator chip for 40Gbps

Wafer picture of integrated RZ-DQPSK modulators. Each 3 element modulator is 7mm long



IEDM showcases the strengths of III-V transistors

Highlights from IEDM 2009 include the development of novel, normally-off GaN transistors for power electronics and improved gate dielectrics for III-V transistors targeting logic applications. **Richard Stevenson reports.**

The 2009 International Electronic Devices Meeting (IEDM) had a similar flavour to its recent predecessors: developments in silicon CMOS technologies dominated the agenda, but there was also a smaller number of papers detailing important breakthroughs in III-V devices. Several of these focused on GaN-based devices for high-power electronics, and a handful described breakthroughs relating to successors to silicon transistors for logic applications.

Panasonic, NEC and HRL Laboratories all reported advances in normally-off transistors that can be used to perform functions such as switching a DC signal to an AC form, or boosting output voltages. Both of these types of manipulations are needed in circuits built for motor drives and for the linking solar panels to the grid.

Researchers from Panasonic claimed to have made the first single chip, GaN-based inverter IC for motor drives. Their device, which converts a DC source into an AC form, has led to the filing of 141 domestic and 90 overseas patent applications.

The inverter features six of the company's gate injection transistors (GITs) integrated onto a single chip. These transistors are normally-off, which means that they are inherently safer and use a more robust mode of operation than the more common normally-on transistor. The GIT also has a very low switching loss, enabling the construction of an inverter with a conversion loss that is 42 percent less than that of the incumbent technology - a silicon-based insulated gate bipolar transistor.

The epistructure for Panasonic's inverter is grown by MOCVD on silicon substrates, and normally-off operation is realized through a p-type AlGaIn gate above the AlGaIn/GaN heterostructure. The authors from Panasonic claim that the transistor delivers an extremely high drain current and a low on-state resistance, thanks to conductivity modulation resulting from hole injection from the p-type gate. Every transistor in the chip has to be fully isolated from the other five. This is realized with an iron ion doping process that is even remains stable at temperatures well above 1000 degrees C.

Device testing reveals a typical off-state breakdown voltage for the GITs of 700 V, thanks to the thick GaN buffer layer. The threshold voltage and off-state leakage current are stable for over 1000 hours, according to bias-temperature reliability studies.

The engineers at Panasonic have used these transistors to form inverter ICs. Fast recovery diodes are not used in these circuits. Although they have a recovery time of just 50 ns, they are inferior to Panasonic's GITs that recover in just 20 ns.

The 2.5 mm by 2.7 mm inverter built from these transistors employs GITs with a 25 nm gate width. This monolithic chip can deliver an operating efficiency of 93 percent, even at low output conditions of 20W out of a 100W motor driving system, and the researchers claim that even higher efficiencies are possible by cutting the on-resistance in a larger chip.

*The 2009 International Electron Devices Meeting was held between 7-9 December in Baltimore, MD.
Credit: IEEE*



NEC adds neutralization

Like Panasonic, NEC has been developing a new transistor technology. At IEDM it unveiled a GaN power transistor featuring a novel piezo neutralization technology. This addition to the device aids the control and suppression of electrical currents when the power is turned-off, and leads to low-power losses, high-speed switching and high-temperature operation.

The authors of the paper say that conventional HEMTs suffer from a large variation in threshold voltage. This is caused by thickness variations in the AlGa_N layer under the gate that is etched down from 20-30 nm to just a few nm to realize normally-off characteristics.

NEC sidesteps this issue with a five-layer design. This is based on a metal-insulator-semiconductor (MIS) FET with a piezo neutralization layer (see figure 1). The MESFET produces normally-off operation, thanks to the switch from a conventional buffer to one made from AlGa_N.

The NEC transistor benefits from the inclusion of a piezo neutralization layer with an identical composition to the buffer. This causes the polarization charges formed between these layers to cancel out, thereby equipping the FET with high threshold voltage uniformity. Realizing similar levels of uniformity in conventional HEMTs is very tough, due to variations in the thickness of an etched layer – in an Al_{0.15}Ga_{0.85}N HEMT, just a one nanometer difference in thickness produces a 113 mV variation in threshold voltage. NEC's novel transistor also produces a low on-resistance, thanks to the inclusion of an Al_{0.25}Ga_{0.75}N layer. This second electron supply layer has a higher aluminum content than the first one, leading to two-dimensional electron gases in both the channel layer and the piezo neutralization layer. This creates a high sheet carrier concentration of $6 \times 10^{12} \text{ cm}^{-2}$ that gives the MISFET its low on-resistance.

The five-layer structure was grown by MOCVD on 3-inch silicon substrates. Nitrogen ion implantation isolated these devices, and surface passivation was realized by deposition of a SiN film. After a gate footprint was opened in the SiN film, a BCl₃ plasma etch created the gate recess. An Al₂O₃ film provided the dielectric for the MIS gate structure, and a Ni-Au film was employed for the gate electrode in both gate structures. The NEC engineers fabricated Schottky gates across an entire 3-inch wafer, and measured a standard deviation of the threshold voltage of 18 mV using a drain current of 1 mA/mm and a drain voltage of 10V. They say that this variation in threshold voltage is ten times smaller than that for a conventional Al_{0.15}Ga_{0.85}N/GaN HEMT.

Transistors were fabricated with a source-to-gate separation and a gate length of 1 μm, and a gate-to-drain distance of 15 μm. At a threshold voltage of +1.5V the MISFET produced normally-off characteristics, a maximum drain current of 240 mA/mm and an on-resistance of 20

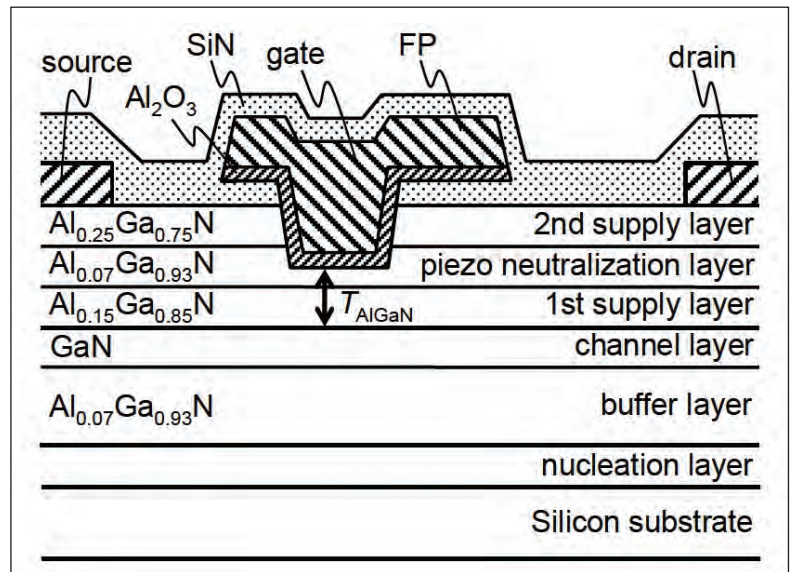
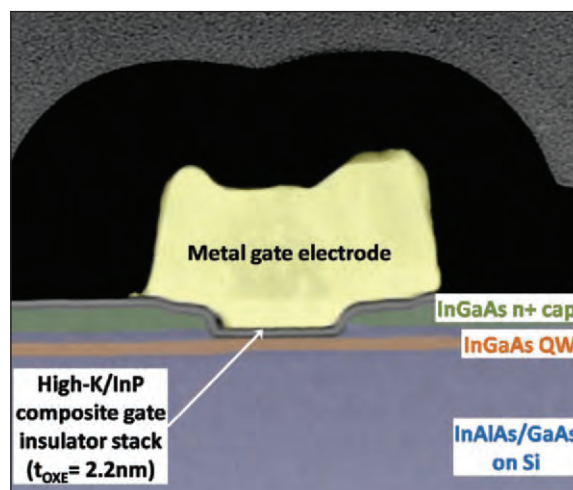


Fig. 1 NEC unveiled a normally-off GaN MISFET that features a piezo neutralization layer. Setting the composition of this layer equal to that of the buffer ensures a high threshold voltage uniformity thanks to complete cancellation of interface charges formed between these layers. Credit: NEC

Ohm-mm. The three-terminal off-state breakdown voltage was more than 1000 V.

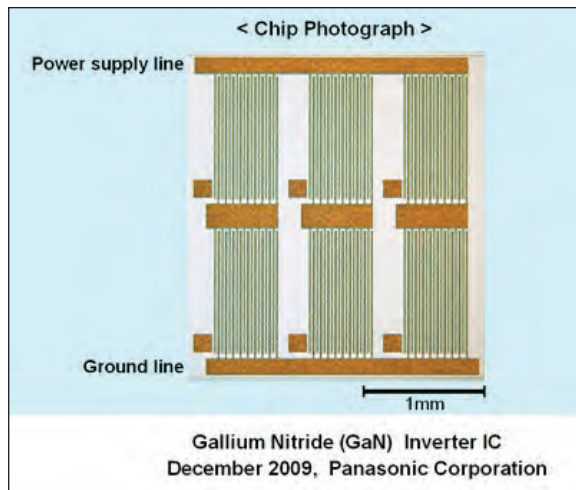
The delegates at IEDM also heard about HRL's development of GaN HEMTs that were fabricated with a fluorine-based process. They have a breakdown voltage in excess of 1100V, and produce a leakage current of less than 10 μA/mm at voltages below 550V.

The engineering team at HRL took two of the die and formed a boost converter, a device for increasing DC output voltage. This operated at a 200 kHz switching frequency and delivered efficiencies of more than 96 percent for voltages up to 200V, and over 96 percent for



Intel has improved its quantum well FET through the introduction of a gate stack based on TaSiOx and InP. IQE carried out the growth of the III-V structure by MBE. Credit: Intel

Panasonic has developed a GaN monolithic inverter IC that features six normally-off gate injection transistors. Credit: Panasonic



voltages up to 360 V. The engineers believe that the efficiency drop at higher voltages is caused by an increase in dynamic resistance and a rise in junction temperature, which could be reduced by improving the heat sink in the GaN package.

Post-CMOS technologies

The handful of papers presented on III-V transistors for logic applications included contributions from SEMATECH, IMEC and Intel. For the last few years IMEC has been working on the development of a germanium channel for p-type conductivity, and an InGaAs channel for n-type conductivity – both types of conductivity are needed to make a suitable successor to CMOS. And at IEDM the Belgium research institute unveiled their latest progress, the development of a common gate stack process involving a sulfur-based treatment and deposition of Al_2O_3 . One of the merits of this approach is that it avoids the need for either interfacial passivation layers or native oxides, such as GeO_2 , between the channel and dielectric.

Fabrication of the MOSFETs begins by taking germanium and $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ substrates, cleaning then, removing their oxides and treating them in ammonium sulfide solution. Atomic layer deposition of 8 nm and 10 nm of Al_2O_3 on germanium and InGaAs substrates follows at 300 degrees C, before these wafers are annealed at 400 degrees C.

The researchers have studied the interface trap density in both structures. They found a relatively high density ($>1 \times 10^{19} / \text{eVcm}^2$) of acceptor-like traps near the conduction band of germanium, but the density was several hundred times less beside the valence band. With InGaAs the opposite was observed: a relatively high density of donor-like traps on the valence band side, and far fewer defects near the conduction band. These results suggest that it is possible to form a p-channel with a high density of free holes, and an n-channel with good electron

conduction and relatively low surface-charge scattering.

Device testing of the germanium and InGaAs MOSFETs revealed drain currents of 600 mA/mm and 200 mA/mm, respectively, at a 2.5V gate bias swing, and maximum transconductances of 340 mS/mm and 95 mS/mm, respectively. On-off ratios for these devices are below 10^4 , partly due to the high off-state leakage current that is believed to stem from the surface leakage paths outside the active area. However, the authors say that this can be addressed through proper device optimization and improvements to the fabrication process.

A US team led by SEMTECH detailed its optimization of a ZrO_2 dielectric at IEDM. This oxide is a promising candidate for making a III-V MOSFET, because it has a very high dielectric constant that is four times that of Al_2O_3 . However, the pairing of ZrO_2 with InGaAs leads to border traps, interface traps, and interface fixed charges. The US researchers have partially addressed all these issues by inserting very thin (L_3) AlO_x layer between these two materials. Adding this interlayer, which is only about a nanometer thick, cuts border traps and fixed charges by a factor of three, and improves MOSFET performance. Drain current increases by 50 percent, and maximum transconductances by 75 percent.

Intel's wells

Over the last few years Intel has been working on an alternative to the III-V MOSFET - the quantum well field effect transistor (QWFET). This type of device can be deposited on a silicon substrate, and it delivers an excellent drive current performance at low voltage, but first-generation devices have suffered from a high leakage current at the Schottky gate.

However, the researchers have now addressed this, and at the 2009 meeting they described the characteristics of a QWFET with a gate stack comprising 4 nm of TaSiO_x and 2 nm of InP. The new gate slashed leakage current by over three orders of magnitude, and led to the fabrication of 75 nm gate length transistors with a maximum transconductance of $1750 \mu\text{S}/\mu\text{m}$, and a drive current of $0.49 \text{ mA}/\mu\text{m}$ at a drain-source voltage of 0.5 V.

Although the gate in this device is just 75 nm wide, the other structures are relatively large, and one of the next goals for Intel is to reduce these dimensions while still retaining the ability to move charges in and out of the quantum wells. The researchers from SEMATECH and IMEC face similar challenges, and the developers of nitride electronics at Panasonic, NEC and HRL still have some way to go before their devices can be commercialized. But all these compound semiconductor devices are making progress, and it is a sure bet that even better results will be presented at the next IEDM, which will be held in San Francisco, CA, from 6-8 December 2010.

Michigan: Auger causes LED droop

Modulation experiments with nitride lasers reveal that Auger is the cause of LED droop

Researchers at the University of Michigan are throwing their weight behind Philips Lumileds' controversial claim that Auger recombination is the cause of LED droop, the decline in device efficiency at higher drive currents.

Pallab Bhattacharya and colleagues have performed modulation measurements on nitride lasers, and extracted a coefficient for Auger recombination - a non-radiative process involving the interaction of an electron, a hole, and a third carrier. The magnitude of this coefficient shows that Auger is the dominant cause of LED droop.

"Prior to our work there has only been one report of the experimental determination of the Auger recombination coefficient in quasi-bulk InGaN layers," explains Bhattacharya. According to him, the approach that he and his co-workers have used is far more direct than the earlier work

- a time-resolved photoluminescence study by Lumileds.

The University of Michigan researchers performed large-signal modulation measurements on a 407 nm laser with four, 3 nm thick quantum wells that were sandwiched between 15 nm GaN barriers. The devices were driven with 120 ns pulses that had a 100 ps rise time, and the emitted light was recorded by an ultra-high-speed GaAs photodetector. Turn-on delays of a few ns were determined for drive currents of 30 mA to 90 mA.

Armed with this information, plus values of the capture cross-section and deep trap density - which were both determined from deep level transient spectroscopy measurements with a UV laser - the researchers performed simulations that yielded a Auger recombination coefficient of $1.5 \times 10^{30} \text{ cm}^6 \text{ s}^{-1}$ at 300K.

They then concluded that Auger recombination is the primary cause of droop by using this coefficient to calculate the internal quantum efficiency in $\text{In}_{0.1}\text{Ga}_{0.9}\text{N}$ quantum wells, and finding that this value agrees "remarkable well" with that measured in quantum well LEDs with an identical active region. Different forms of Auger recombination have been proposed as the cause of droop. Bhattacharya says that his data indicates that the normal Auger process is quite strong, due to the high carrier density in the wells. "However, there is bound to be a defect-assisted process as well."

The researchers are now planning to measure large signal modulation in an InGaN/GaN green laser, and analyze the efficiency droop in green LEDs.

M. Zhang et al. *Appl. Phys. Lett.* **95** 201108 (2009)

Holey laser could aid silicon photonics

European researchers claim to have made the first photonic crystal laser that provides a light source for a silicon waveguide.

Developing lasers for silicon circuits is a hot topic in the III-V research community, because it could lead to low-cost fabrication of ultra-compact optical integrated circuits.

The partnership between the Photonics and Nanostructures Laboratory in Marcoussis, France, and the Belgium research institute IMEC, realized 1.585 μm pulsed emission from an InP-based, two-dimensional photonic crystal heterogeneously integrated to silicon-on-insulator wires.

The photonic crystal lattice, which features line-defect waveguides in a triangular lattice, is designed to cause interference between forwards and backwards waves, leading to propagation of slow light. This is beneficial because it can increase the time that light interacts with a gain medium. Ultimately, this longer interaction time could lead to a cut

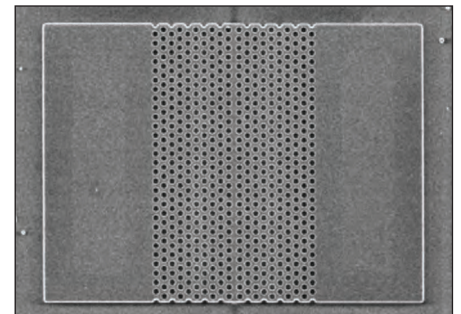
the laser emission threshold.

Pumping the structure with a 1.18 μm laser produced 1585 nm emission in the silicon-on-insulator wire. Thanks to the geometry of the hybrid lasing structure, the researchers could optically pump and collect light through the same wire.

The team is also looking at electrically injecting their lasers.

"It is a very hard task," explains corresponding author Fabrice Raineri from the Photonics and Nanostructures Laboratory. Adding electrical contacts may induce losses and impact the optical properties of the structure, and channeling the current is difficult due to the air holes. "That's why it is important to also discuss optical pumping for applications - it may be more straightforward."

Y. Halioua et al. *Appl. Phys. Lett.* **95** 201119 (2009)



A scanning electron microscopy image reveals the triangular lattice and the line defect in the photonic crystal. Credit: CNRS

GaN offers promise for thermoelectrics

One of the most promising nitride-based thermoelectrics has been built by researchers at the University of California, Santa Barbara.

Researchers at the University of California, Santa Barbara (UCSB), have fabricated a GaN-based thermoelectric that can produce 2.1 μW from a 30 K temperature difference. This is roughly half of the power produced by an InN/AlInN thermoelectric fabricated by Japanese researchers several years ago, but in that case the temperature difference was far higher - 332K.

Temperatures differences across thermoelectrics lead to the generation of a potential difference, and this generates an electrical current.

Today the leading materials for fabricating thermoelectrics are based on Bi_2Te_3 . These materials are scarce and toxic, and devices made from them are limited to operating temperatures of up to 150 degrees C.

In comparison, GaN-based devices are capable of far higher operating temperatures, they are not toxic, and in addition to power generation, they could be used to provide on-chip spot cooling for nitride-based LEDs, lasers and HEMTs.

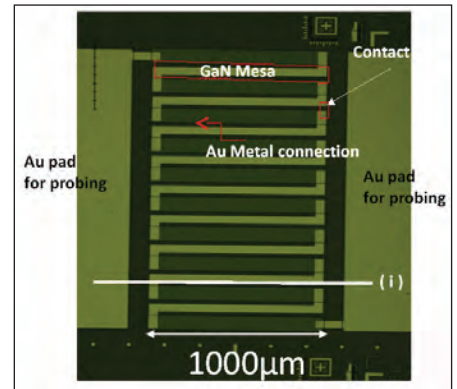
The UCSB team, which includes Hiroaki Ohta, Steven DenBaars and Shuji Nakamura, produced the thermoelectric by first depositing a 3.5 μm thick layer of silicon-doped GaN on sapphire.

Conventional lithography, dry etching with an inductively coupled plasma and the formation of metal contacts led to the creation of a series of devices with 1, 5, 10 and 25 thermoelectric elements.

Applying a 30 K temperature gradient across the 25-element device produced a maximum open circuit voltage of 0.3V and a peak output power of 2.1 μW . High-temperatures tests revealed that the thermoelectric shows no signs of degradation up to 825K, the limit of the testing apparatus.

Ohta says that this work is just a preliminary study. "We will move on to alloys or more complex materials to improve efficiency."

A. Szein et al. *Appl. Phys. Express* **2** 111003 (2009)



UCSB researchers fabricated a series of thermoelectric devices, including a version that contain 10 elements. Credit: UCSB

Microscopy unveils UV LED aging mechanism

An international collaboration has uncovered an aging mechanism in UV LEDs that involves local increases in current, followed by heating and atom migration. This discovery resulted from efforts by researchers at the Royal Institute of Technology, Sweden, to measure the electroluminescence from UV LEDs with a scanning near-field optical microscope (SNOM) that could realize a spatial resolution of 150 nm.

US firm Sensor Electronic Technology provided the 285 nm, flip-chip LEDs, which featured an AlN buffer, an AlN/AlGaIn superlattice, and an active region with five quantum wells.

Optical measurements uncovered well-

distinguished areas that were several microns in diameter and produced emission at longer wavelengths. The density of these spots, which are seen in both aged and fresh devices, is roughly one per 100 μm^2 .

The researchers found that these spots produced relatively high electroluminescence intensity, indicating a local increase in carrier injection. Studies over several days revealed a gradual increase in emission intensity from these spots and a red-shift in emission wavelength.

Possible explanations for this behavior that are based on temperature, strong internal electric fields, and quantum well intermixing were all ruled out. Device behavior is

actually believed to stem from higher currents through the spots, which leads to local heating and atom migration. This decreases the local potential and increases the current once more, creating a cyclical process that continues to fuel itself until LED failure.

Interestingly, these spots are not observed in all types of UV LED. "Currently, we are performing SNOM measurements on UV LEDs emitting at different wavelengths, and, for instance, for a 335 nm emitting device no lower potential spots have been found," said Saulius Marcinkevicius from the Royal Institute of Technology.

A. Pinos et al. *Appl. Phys. Lett.* **95** 181914 (2009)

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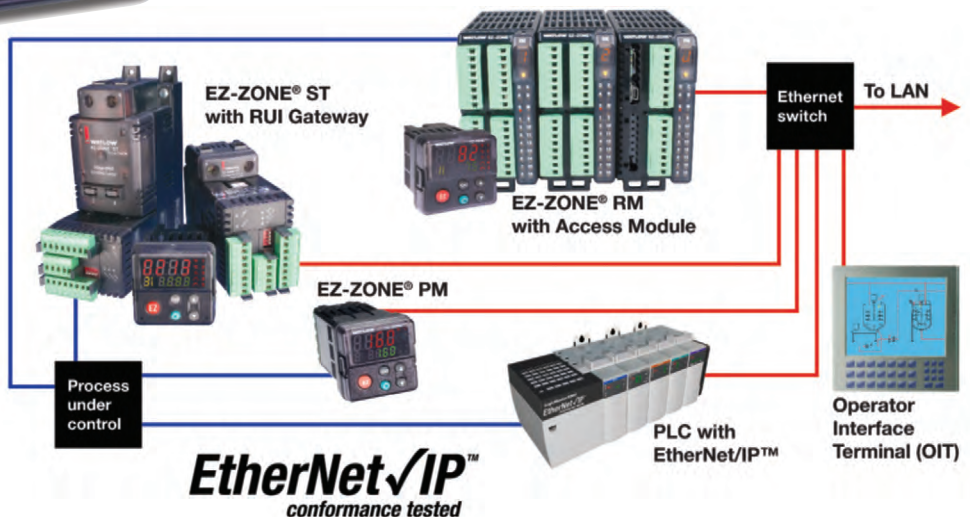


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