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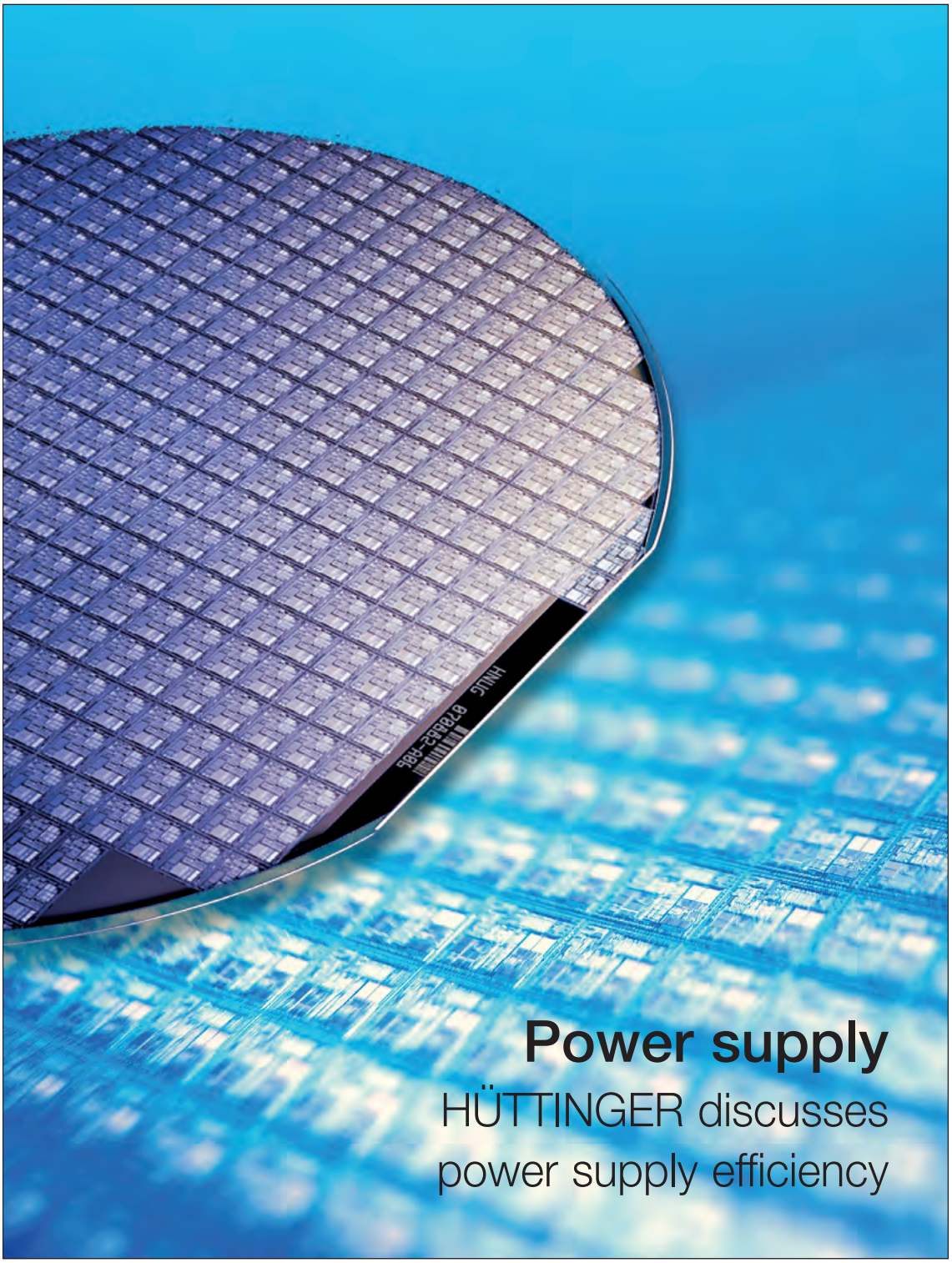

Power supply
HÜTTINGER discusses power supply efficiency

An Angel Business Communications publication

July 2010 Volume 16 Number 5

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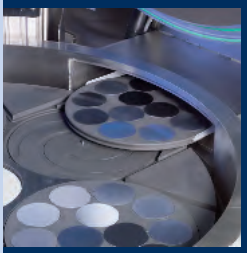

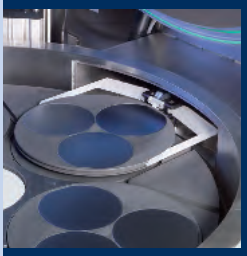

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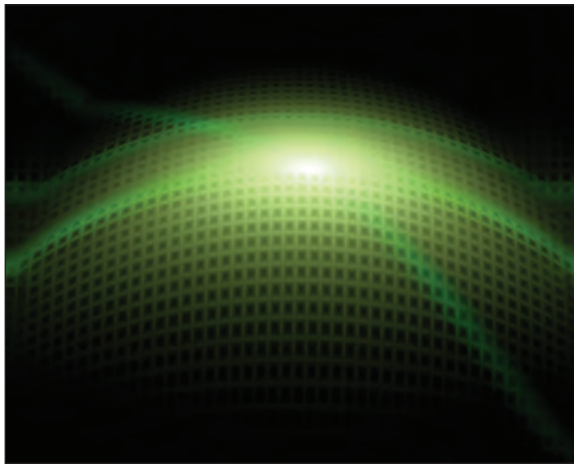
Osram's great green laser

Peruse through the journals and you'll find plenty of papers detailing incremental, but undeniably important breakthroughs. Just occasionally, however, sitting among them you'll also find a gem that makes you sit up and think wow, that really is impressive.

I recently experienced that rare and joyful moment when I spotted Osram's paper announcing a 50 mW, continuous-wave laser emitting at 524 nm.

My shock was two-fold. Firstly, the power output is incredibly high - the only other reports north of 520 nm that I am aware of have been for devices delivering just a handful of milliwatts. And secondly, the German outfit had built its device on the polar plane of gallium nitride, a cut that has been widely touted as inappropriate for long wavelength nitride lasers.



I wrongly assumed that Sumitomo's unveiling of its semi-polar 531 nm laser last summer had answered the question over which plane to grown green lasers on. But Osram's efforts have well and truly muddied these waters.

What is for sure is that the future will settle this debate. Semi-polar lasers are still a relatively immature technology, and how much more performance can be squeezed out of them is not yet clear. But having said that, if you rewind the clock a few years, it seemed that after a decade or more of development, conventional nitride lasers were hitting a wall at 490 nm. With the benefit of hindsight, however, we know that this class of laser could do far better.

Another big question concerns the commercial viability of the various classes of nitride laser. For example, very little has been published on the reliability of semi-polar lasers.

There is also the issue of cost. Conventional gallium nitride substrates are dear, but they are still far cheaper than semi-polar GaN. Substrate prices are not the only issue, however. Yields will play a major role, and today's R&D efforts have only hinted at what is possible in this regard.

What is for sure is that it will be fascinating to witness the commercial development of green lasers. Whether Osram will be the first to triumph is anyone's guess, as Sumitomo, Nichia, and Kaai will also be busting a gut to get their products to market first. It promises to be a great battle.

Richard Stevenson PhD
Consultant Editor

COMPOUND SEMICONDUCTOR CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

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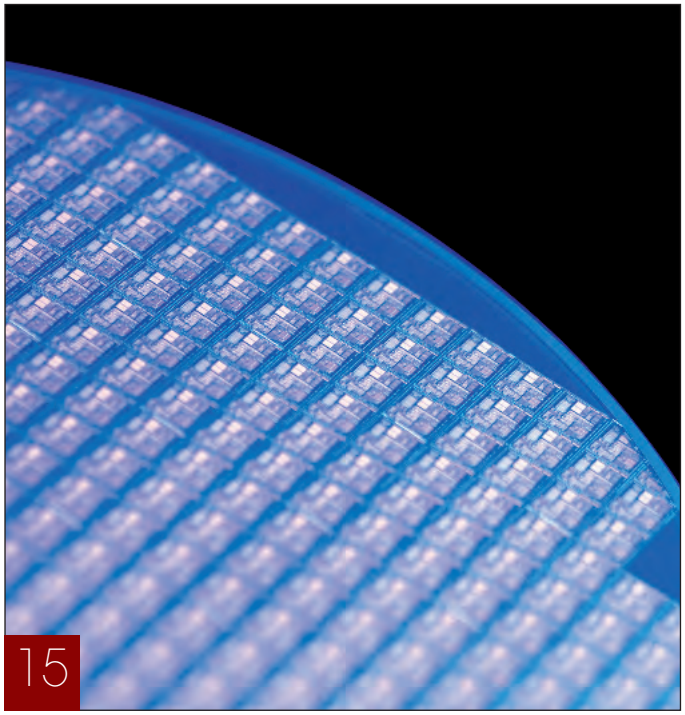
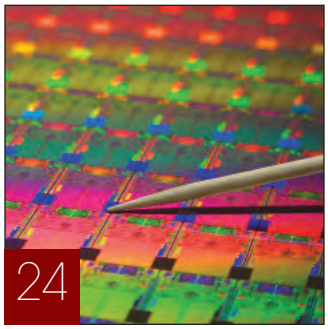
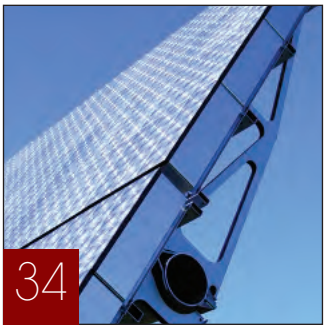


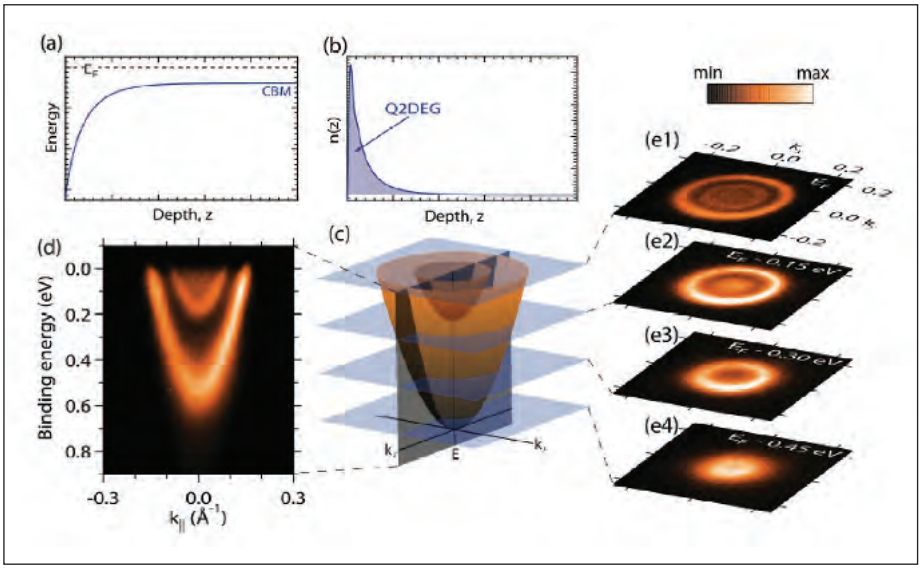




news

Bandgaps: Think they're constant? Think again!

The shrinkage of the fundamental bandgap near the surface of InAs and other compound semiconductors could offer a new route in bandgap engineering. A team of European researchers has found that the semiconductor bandgap is not necessarily constant and varies with surface distance.



The partnership between researchers from the UK, France, Spain and Denmark has looked at the surfaces of some compound semiconductors that can support a quasi two-dimensional electron gas. (Q2DEG) Here, electrons can move freely parallel to the surface but are confined to this region. Traditional semiconductors like silicon and GaAs have a depletion of carriers close to the surface. For a long time, this has been thought of as the norm.

However, new materials are being found which exhibit electron accumulation. For example, Philip King, one of the researchers in this study pointed out that he and others have observed the presence of a Q2DEG zone at the surface of In-rich InGaN and InAlN alloys. In this latest investigation, the localized surfaces of InAs and CdO were investigated for quantum-well states supposedly intrinsic to these materials. Both materials exhibited similar phenomena.

The scientists used the ASTRID synchrotron to obtain Angle-Resolved Photo-Emission Spectroscopy (ARPES) data. This powerful technique directly images the electronic structure of the Q2DEG at the surface, and supplies information regarding the interactions between particles. The InAs(111)B sample was grown by MBE and was silicon-doped to 6x1017cm^3. An amorphous arsenic cap was grown and removed in-situ by annealing at 350^{0}C. The CdO was grown by metal-organic vapor phase epitaxy (MOVPE). The figure below shows the quantum well states at the CdO surface. Similar trends were exhibited InAs.

The researchers were surprised to find that interactions between the particles at the surface caused the bandgap to become smaller close to the surface of the material compared to in the bulk. Phil King commented that it was not the fact that the particle interactions caused a reduction of the bandgap that was unexpected, but the fact that the changes occurred over macroscopic distances within the sample (i.e. the bandgap changes approaching the surface of the materials). These results showed the presence of a complicated interplay between several degrees of freedom within the materials.

He added "The magnitudes of the changes in bandgap are also larger than might be expected considering traditional ICs, which is testament to the greater flexibility and variety of properties that can be achieved in some of these emerging compound semiconductor materials."

Regarding the results, he also explained, "The conventional one-electron picture of 7surface space-charge in semiconductors was different to the electronic structure observed from ARPES, indicating that many-body interactions play an unexpectedly large role in the Q2DEG in these materials."

The relevance of this discovery should serve several purposes. The fact that the bandgap of these semiconductors becomes smaller when approaching the surface is essentially due to interactions between the electrons within the surface electron accumulation layer. Essentially these results could provide a stepping-stone in the advancement of bandgap engineering; the authors suggest even an entirely new route to spatially-inhomogeneous bandgap engineering, eventually leading to tuning the functionality of electronic devices.

Furthermore, as King said, "The surface electronic properties of materials are crucial in any device application, as an electrical contact must always be made to the surface of a material (indeed, in his 2000 Nobel prize lecture, Herbert Kroemer remarked that "the interface is the device")".

"This so-called surface electron accumulation may, for example, make obtaining Schottky (rather than Ohmic) contacts difficult, but could potentially be beneficial for certain device applications such as terahertz generation or chemical sensors."

Traditionally, the way to tune the bandgap of materials is to alloy two or more semiconductors together that have different bandgaps to start with. The findings in this paper show that the bandgap of a single material may be spatially modulated by controlling how strong the interactions are. This could be controlled by changing the doping levels in the material. King says he hopes these results could add an additional tool to band structure engineering.

Further details on this work will be available in the journal 'Physical Review Letters'.

[1] Colakerol, L, et al, Phys. Rev. Lett. 97, 237601 (2006)
[2] King, P.D.C. et al., "Surface Band-Gap Narrowing in Quantized Electron Accumulation Layers", Phys. Rev. Lett. in press"

Expanding Precursor Capacity

Dow Electronic Materials will increase its TrimethylGallium (TMG) manufacturing capability by 60 tons per year to try to meet escalating LED demands. Dow Electronic Materials, a business unit of Dow Advanced Materials has a multi-phase plan to expand its TMG production capacity to meet the surging global demand for the material in the electronics market. The expansion plan includes adding significant TMG capacity in the United States at existing facilities to address short-term demand as quickly as possible.

In addition, Dow Electronic Materials will build a new metalorganic precursor manufacturing plant in Korea, which is expected to begin operating in early 2011, to create capacity for long-term demand. Total additional TMG capacity resulting from the multi-phase plan is expected to be 60 metric tons per year.

"We are excited that we can greatly expand the supply of our high-purity, electronic-grade precursor materials to our customers with this additional manufacturing capacity," said Joe Reiser, global business director, Metalorganic Technologies, for Dow Electronic Materials."

"We are committed to delivering a reliable supply of high-quality materials to our customers and providing them with the service and technical expertise that they expect from a market leader. We will continue to work closely with our customers to meet both near- and long-term needs."

"Demand for TMG today is being driven by explosive growth in LED backlighting of LCD TVs with the potential of future growth of LEDs in the general lighting market," said James Fahey, global general manager, Growth Technologies for Dow Electronic Materials."

"The LED market is growing rapidly, particularly in Korea, Taiwan and other countries in the Asia-Pacific region where there is a large display manufacturing base and semiconductor manufacturers are building and converting capacity to manufacture LEDs."

The new metalorganic precursor plant in Korea will be located in Cheonan, approximately 85 kilometers south of Seoul. Dow Electronic Materials expects to expand the site in the future to manufacture other metalorganic materials in addition to TMG. Dow Electronic Materials currently manufactures TMG and other metalorganic precursors in North Andover, MA, while packaging is done in both North Andover, MA, and Taoyuan, Taiwan.

Ascent Solar Soar with Massive DARPA Contract

DARPA awards Ascent with Multi-Million Dollar Contract through High-Efficiency Low-Cost Portable Photovoltaics (PoP) Program for Copper Indium Gallium (di)Selenide (CIGS) modules. Ascent Solar Technologies will supply its flexible thin-film solar modules produced using CIGS technology to the Defense Advanced Research Projects Agency (DARPA).

Under the Low-Cost Lightweight Portable Photovoltaics (PoP) solicitation, the ASTI-led program, entitled "Flexible High-performance Tandem-junction PV Array", consists of three gated phases, the first of which is 18 months and has an approximate contract value of $3.8M. The entire program is anticipated to continue over the next 54 months. The goal of PoP is to demonstrate low-cost, lightweight photovoltaics (PV) that can stand up to battle conditions and environmental extremes while delivering a power conversion efficiency of 20% or greater by the end of the program.

"We are excited that DARPA selected our team for the PoP project," stated Farhad Moghadam, President and CEO of Ascent Solar. "In order to meet the aggressive goals of performance, capacity, and military toughness, our team has put together a definitive plan that combines our flexible CIGS production experience and enhanced packaging technologies being developed.

RFMD unveils an industry-first for 5GHz band

The integrated 3-stage PA Front End Module (FEM) provides high gain and is claimed to have the best-in-class efficiency over voltage supply levels of 3.0 to 5.0V

RF Micro Devices is marketing the RF5616, a highly integrated 4.9 GHz - 5.8 GHz (ISM band) 3mm x 3mm power amplifier (PA). The RF5616 module is targeted for high-performance mobile PC and embedded applications including access points, gateways, DSL routers, wireless high definition interface (WHDI), and WLAN for wireless video distribution networks.

The RF5616 features a fully matched product design (input/output) and integrated low pass filtering and requires only two external bypass components. RFMD claims that the integrated three-stage PA provides high gain and is an industry-first for 5GHz band front ends. The firm also say it has the best-in-class efficiency and a wide range of voltage supply levels (3.0 to 5.0V), enabling high linear output power of 18dBm to 21dBm.

The RF5616 also features an interstage power detector, reducing sensitivity to voltage supply, temperature extremes and VSWR while improving accuracy of the closed loop power control.

Additionally, a variable linearity mode control enables two modes of operations; a maximum output power and linearity mode, or a more efficient lower output power mode, with a single control pin. Finally, integrated harmonic attenuation eliminates the need for additional filtering, therefore optimizing the efficiency and maximizing output power at the transmit port. A direct-to-battery connection eliminates the need for additional DC circuitry, while integrated input and output matching eliminates the need for additional RF matching. The RF5616 is fully tested and available in an industry-leading 3 mm x 3 mm leadless QFN package with backside ground.

65% Efficient Solar Cells on the Horizon

Nanowire Solar Cell Research has been awarded €1.2million by the Dutch Government with a project targeted to help meet electricity demand in Southern Europe and North Africa. Researchers at the University of Eindhoven (TU) are trying to develop solar cells with an efficiency of over 65% using nanotechnology. In Southern Europe and North Africa these new solar cells could generate a substantial portion of the European demand for electricity. The Dutch government has reserved €1.2 million for the research.

An agency of the Ministry of Economic Affairs, will grant the €1.2 million to researchers Jos Haverkort, Erik Bakkers and Geert Verbong for their research into nanowire solar cells. It is their expectation that, when combined with mirror systems, these solar cells can generate a sizeable portion of the European electricity demand in Southern Europe and North Africa.

Current III/V thin-film solar cells have an efficiency of around 40%, but they are very expensive and can only be applied as solar panels on satellites. By using mirror systems that focus one thousand times they can now also be deployed on earth in a cost-effective manner.

The TU/ researchers expect that in ten years their nano-structured solar cells will attain an efficiency of more than 65%. Scientist, Jos Haverkort said "If the Netherlands wants to timely participate in a commercial exploitation of nanowire solar cells, there is a great urgency to get on board now."

The research is conducted together with Philips MiPlaza. They think that nanotechnology, in combination with the use of concentrated sunlight through mirror systems, has the potential to lead to the world's most efficient solar cell system with a cost price lower than 50 cent per Watt peak. In comparison: for the present generation of solar cells that cost price is €1.50 per Watt peak.

Nanowires make it possible to stack a number of subcells (junctions). In this process each subcell converts one colorof sunlight optimally to electricity. The highest yield reported until now in a nanowire solar cell is 8.4%. Haverkort commented, "We expect that a protective shell around the nanowires is the critical step towards attaining the same efficiency with nanowire solar cells as with thin-film cells." Haverkort thinks that at 5 to 10 junctions he will arrive at an efficiency of 65%.

Furthermore, the researchers expect considerable savings can be made on production costs, because the rapid growth of nanowires on a cheap silicon substrate results in a lower cost of ownership of the growth equipment. Also, the combination of the mirror systems with nanotechnology will imply an acceptable use of the scarce and hence expensive metals such as gallium and indium.

EpiWorks demonstrates 6" CPV capability

EpiWorks Aixtron 2600 G3 reactor used in the first step towards producing low-cost solar cells with the highest conversion efficiency.

EpiWorks, a developer and manufacturer of compound semiconductor epitaxial wafers has announced a major milestone in the development of technology to address the concentrated photovoltaic (CPV) market.

The firm has demonstrated a 6-inch, compound semiconductor PV wafer capability that is the first step in establishing the infrastructure and capability required to produce low-cost solar cells with the highest conversion efficiency. Such devices are desired by the industry.

David Ahmari, EVP of Business Development at EpiWorks commented "We are a manufacturer with an established track record supporting the wireless industry with volume production, but over the past several years we have also established a strong solar cell capability. As we have done with our wireless customers, EpiWorks is excited to push the industry technology roadmap while establishing this critical part of the PV wafer production supply chain."

He continued, "To ensure rapid and successful adoption of this CPV technology, EpiWorks is working closely with key partners, including a US-based semiconductor manufacturer listed on the NASDAQ."

DelSolar shows its Power with Tolerance up to 3%

Latest series include excellent power performance in low lighting conditions and attractive black modules for residential roofs.

DelSolar, a subsidiary of Delta Electronics exhibited its high efficiency solar modules with a positive power tolerance of up to 3% at 'Intersolar 2010'. The solar modules are claimed to feature excellent power performance even in low light intensity conditions.

In addition, DelSolar is marketing a new series of black modules with black-anodized aluminium frames. The dark appearance of the black module model is very aesthetically attractive and may be blended elegantly into a variety of residential roofs.

DelSolar employs highly automated module production lines and inline inspection systems including electroluminescence (EL) to reduce the risk of cell microcracks, improve cell encapsulation, and assure consistent module quality and reliability. The resulting high production quality is supported by DelSolar's 5 year product warranty and performance guarantee of 90% for 10 years and 80% for 25 years respectively.

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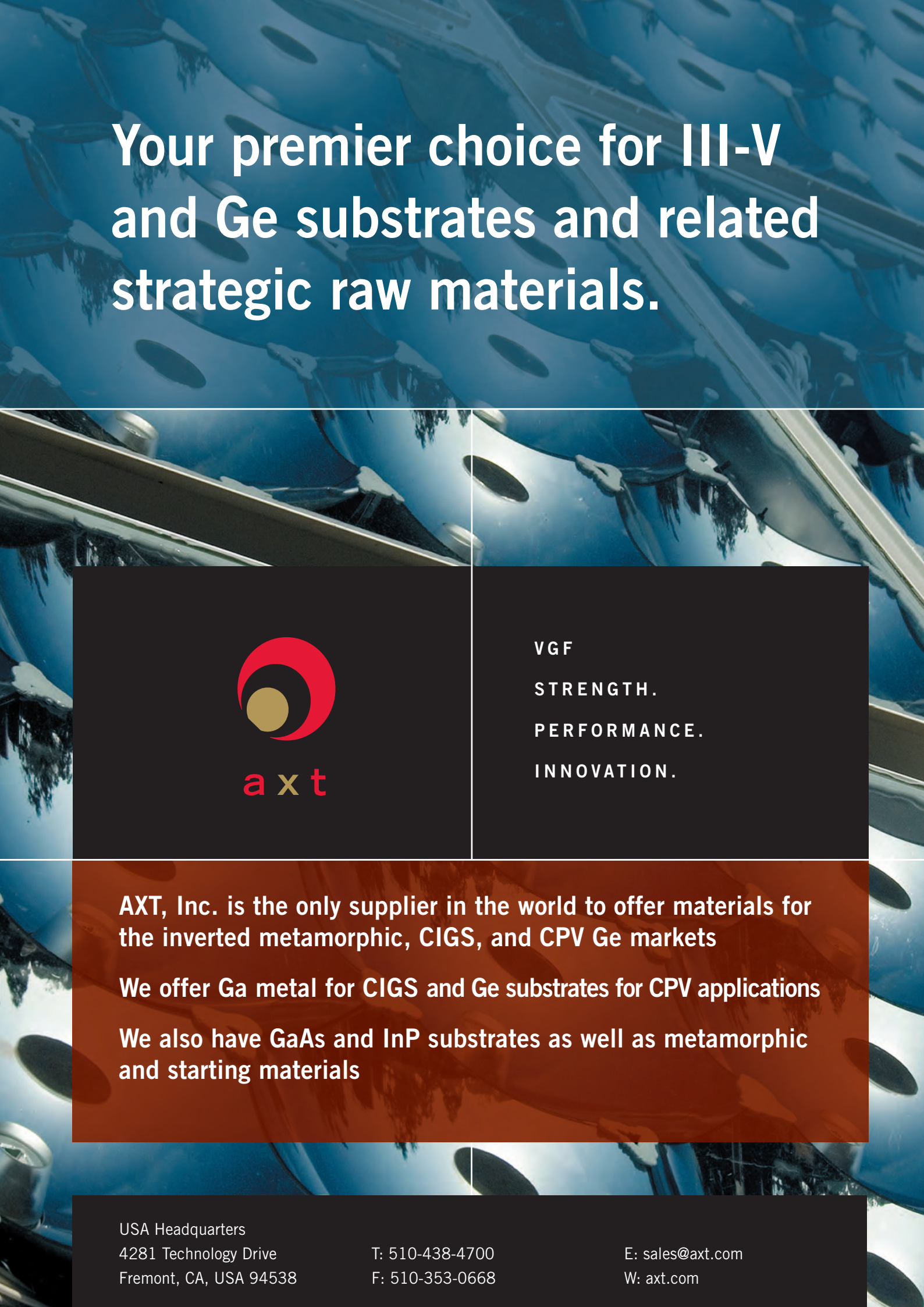

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Stion Expands with TSMC to Create 500 Jobs

The partnership with TSMC will commence a 100 MW expansion of its CIGS thin-film solar panels at Stion's San Jose facility.

Stion, a manufacturer of high-efficiency thin-film Copper Indium Gallium Sulfur-Selenide(CIGS) solar panels has announced a production partnership with TSMC of Taiwan. The firm will commence a 100 MW expansion of its San Jose, California facility following the close of its $70 million Series D financing. Stion had previously raised $44.6 million in equity financing.

Under the agreements, Stion licenses and transfers its thin-film CIGSS technology to TSMC, while TSMC will provide a certain quantity of solar modules to Stion using the technology. TSMC and Stion will also work together to enhance the thin film technology through joint development.

In addition, VentureTech Alliance, a TSMC affiliate, will invest US$50 million to take a 21% stake in Stion.

"TSMC has evaluated a number of thin-film technologies and believes by working with Stion we will gain a robust thin film technology with inherent low cost structure," said YC Chao, TSMC's Senior Director of New Businesses.

Chet Farris, Stion's President and CEO, commented, "Beyond our 100 MW production facility, the strategic partnerships result in a very capital efficient production model as we will gain access to a certain amount of capacity without additional capital commitment from Stion.

He added, "We are pleased to form a win-win relationship with TSMC, a world-class company. The collaboration enables Stion to scale its operations, leverages both companies' strengths to achieve market leadership and to deliver on the promise of efficient, affordable solar energy."

"Working with Stion, TSMC gains a robust thin film technology with inherent low cost structure. With TSMC's R&D capabilities and manufacturing expertise, we believe we can achieve long-term overall leadership in solar PV solutions, and we are happy to be able to contribute to a greener economy," said Rick Tsai, TSMC's President of New Businesses.

"In the crowded field of thin film solar with mostly undifferentiated technology, Stion has distinguished itself with the highest efficiency production ready technology on one square meter, 120 W to 130 W monolithic panels. Stion will show how a PV startup gets to positive cash flow with a $100m dollar equity investment," said Vinod Khosla, Partner at Khosla Ventures, one of the supporting companies.

Stion's panels are specifically designed for use in all major applications, including commercial / government, residential, utility and off-grid. The panels are produced using monolithically integrated circuits and offer a advantages including high efficiency, a convenient form factor (2 ft x 5 ft), improved performance in partial shading, and superb aesthetics according to the manufacturer.

EU rooftop's to provide 40% demand

The European Photovoltaic Industry Association (EPIA) together with Design-Build Solar has organized an event on Building Integrated Photovoltaic (BIPV) systems, at the premises of the Ministry of housing in Madrid, in the framework of the "Solar Decathlon". The event will count more than 170 participants representing mainly architects, installers, representatives from the renewable and construction industries. The speakers, coming from all around Europe, will address the latest technological and market trends within this sector as well as the economic and regulatory frameworks in Spain and within the main European PV markets.

With a total ground floor area over 22,000 km^2, 40% of all building roofs and 15% of all facades in EU 27 are suited for PV applications. This means that over 1,500 GWp of PV could technically be installed in Europe which would generate annually about 1,400TWh, representing 40% of the total electricity demand by 2020.

The integration of photovoltaic energy in buildings provides an enormous development potential for the PV industry as well as for the construction sector.PV applications, apart from contributing to the generation of electricity and improving the passive energy behaviour of buildings, can replace conventional building components and also provide different functions such as, water tightening, weather protection, heat insulation, light modifications, etc.

"Spain has a unique opportunity to develop the BIPV market, which in addition to leveraging the decentralised nature of PV generation, energy generated by the citizen for the citizen, would enable the stimulation of tens of thousands of jobs firmly anchored in the local economy, many of which in the construction industry", said Virgilio Navarro, EPIA's Vice-president and CEO of ATERSA.

Currently in some European countries the BIPV market is driven by specific support schemes, designed in such a way that BIPV systems are rewarded with a higher tariff per kWh generated than for Building Adapted PV (BAPV), where the PV modules are installed on top of the existing building structure and do not provide any additional function. This acknowledges the added effort and extra cost of integrating PV as part of the building envelope. It is in particular the case in France and Italy where BIPV already represents over one third of the annual market. In other countries such as Germany and Spain, where support schemes are not differentiated between both types of systems, BIPV only represents a very marginal share of the market.

RFMD unveils its latest versatile front end module

The highly integrated, single-chip RF3858 supports multiple Tx/Rx applications in the 900 MHz ISM band, including Smart Energy/Advanced Metering Infrastructure (AMI).

RF Micro Devices a global provider of high-performance radio frequency components and compound semiconductor technologies, has announced the availability of the RF3858 front end module (FEM). The RF3858 FEM supports multiple Tx/Rx applications in the 900 MHz ISM band, including Smart Energy/Advanced Metering Infrastructure (AMI).

The highly integrated, single-chip RF3858 addresses the increasing requirements for aggressive size reductions in the RF front end designs for portable equipment.

The RF3858 combines a 1-watt 915 MHz power amplifier capable of 31.5 dBm of output power, with a double-pole double-throw (DPDT) Tx/Rx transfer switch with low insertion loss and high isolation, a low noise amplifier (LNA) with bypass mode, and a Tx harmonic filter.

The RF3858 reduces the number of external components by approximately 80% versus discrete designs, greatly minimizing product footprint, accelerating design-in time and reducing overall assembly costs. The RF3858 is packaged in a small 8.0 mm x 8.0 mm x 1.2 mm over-molded laminate package with backside ground, minimizing next level board space and allowing for simplified integration.

Endwave's Dual-Output VCOs range from to 3.65 to 8.8 GHz

Latest voltage-controlled oscillators (VCOs) range from 3.65 to 4.4GHz and 7.3 to 8.8GHz.

Endwave Corporation, a global provider of high-frequency RF devices and integrated subsystems, has announced the release of its EWV0800YF series of voltage-controlled oscillators (VCOs) with dual outputs with total frequency coverage of 7.3 to 8.8 GHz and 3.65 to 4.4 GHz.

Based on 2 micron InGaP/GaAs heterojunction-bipolar-transistor (HBT) technology, the monolithic-microwave-integrated-circuit (MMIC) oscillators feature on-board divide-by-two prescalers to create a second tuned output range at one-fourth the frequency of the fundamental outputs.

For example, model EWV0801YF tunes with a fundamental-frequency range from 7.3 to 8.3 GHz with typically +13 dBm output power and a divided frequency range of 3.65 to 4.15 GHz with typically +8 dBm output power. The VCO tunes with control voltages of 2 to 13 V and supply current of typically 260 mA.

It achieves phase noise of -116 dBc/Hz offset 100 kHz from the carrier in either band, with subharmonic levels of typically -42 dBc and second-harmonic levels of typically -10 dBc. Pushing is typically 10 MHz/V for a tuning voltage of 5 V while pulling into a 2.0:1 VSWR load is typically 5 MHz peak to peak. The frequency drift with temperature is typically only 750 kHz/°C for a wide operating temperature range of -40 to +85°C.

The higher-frequency model EWV0802YF tunes across a fundamental-frequency range of 7.8 to 8.8 GHz with +13 dBm typical output power and a divided-by-two output-frequency range of 3.90 to 4.4 GHz with +9 dBm typical output power. It matches the excellent phase-noise performance of the lower-frequency model, at -116 dBc/Hz offset 100 kHz from the carrier in either band, with subharmonics of typically -41 dBc and second harmonics of typically -10 dBc. It matches the performance of the EWV0801YF in terms of pushing, pulling, and frequency drift with temperature. Both oscillators are supplied in low-loss 32-lead QFN packages measuring just 5 x 5 mm.

Endwave also produces dual-output VCOs for higher-frequency operation through 15.5 GHz, including models in the EWV0900YF series for frequencies to 9.9 GHz, the EWV1000YF series for frequencies to 10.9 GHz, the EWV1100YF series for frequencies to 11.8 GHz, the EWV1200YF series for frequencies to 12.75 GHz, the EWV1300YF series for frequencies to 13.75 GHz, the EWV1400YF series for frequencies to 14.9 GHz, and the EWV1500YF series for outputs to 15.5 GHz. All include divided-by-two and divide-by-four secondary output ports, and all are housed in the company's enhanced QFN surface-mount packages.

OSRAM: promoter of semiconductor research

The prize, established by Siemens to honour the father of the III-V semiconductors, Heinrich Welker, was first awarded in 1976. OSRAM has sponsored this award for several years.

"For OSRAM as one of the leading manufacturers of optoelectronic components encouraging research in this field is especially important. The Welker Award is given to people who have achieved exceptional progress in the field of opto-semiconductors", said Berit Wessler, in charge of the strategic technology cooperation at OSRAM, as she presented the award to Professor Bhattacharya.

Sylarus to Supply Solar Cell Substrates with 5N Plus

5N Plus has provided financing to Sylarus Technologies ; the firms have entered into a germanium supply and recycling agreement.

5N Plus a manufacturer of high-purity metals and compounds for electronic applications has agreed to subscribe convertible debt of Sylarus Technologies, LLC of Saint George, Utah a major producer of germanium substrates for solar cells.

The financing is designed to help fund Sylarus' expansion plans. Concurrently, 5N Plus and Sylarus have also entered into a long-term supply and recycling agreement under which 5N Plus will provide high-purity germanium feedstock to Sylarus and will recycle various germanium containing residues originating from Sylarus' crystal growing and wafer manufacturing activities.
5N Plus President and CEO, Jacques L'Écuyer said, "We welcome the opportunity to provide financing to Sylarus and are excited about Sylarus' potential for significant growth. Sylarus is one the very few germanium substrate suppliers used for high- efficiency solar cells in both space and terrestrial applications."

This is an area of the solar market that we were not addressing through our existing product offering. Together with the supply and recycling agreement we entered into with Sylarus, this financing further strengthens our germanium related activities and provides a valuable outlet for our subsidiary Firebird's line of products," he added.

"We are equally delighted by this agreement" commented Sylarus President, Scott Mitchell, "as 5N Plus' financing will enable us to more effectively implement our expansion plans. In addition, Sylarus will be provided with a reliable and high-quality germanium feedstock and cost effective recycling options. 5N Plus is a leading provider of material solutions to the solar industry and we expect a positive impact on our business from working with 5N Plus."

GaAs-based detectors extend to the far infrared

A team of French researchers claims that it has fabricated the first GaAs/AlGaAs quantum cascade detector (QCD) capable of operating at very long infrared wavelengths.

Development of this 15 μm detector could provide a stepping stone towards the manufacture of focal plane arrays operating in this spectral range that could be used for meteorology, atmospheric chemistry studies, and Earth observation missions.

Corresponding author Amandine Buffaz from the University of Paris, Diderot-Paris 7, says that the performance of the team's detectors are comparable to those of the incumbent technology, quantum well infrared photodetectors.

However, the cascading detectors have one distinct advantage – very low dark currents that enable long integration times.

The team, which also includes researchers from the Alcatel-Thales 3-5 lab, produced their detectors via MBE growth on a semi-insulating GaAs (001) substrate. The detector's epitaxial layers consist of 30 identical periods of 4 coupled quantum wells that feature AlGaAs barriers with a 232 meV conduction band offset.

Square shaped mesas with 50 μm and 100 μm sides were created with dry-etching techniques, and Au/Ge/Ni ohmic contacts were deposited onto these pixels.

The detector has a responsitivity peak of 14.3 μm, and its detectivity at 25 K and an applied bias of –0.6V is 1 x 1012 Jones.

The detector's performance can be taken to a new level by cutting the tunneling current.

"To reach that aim we will use two theoretical models of electronic transport in QCDs: a 'thermalized subbands' approach that models transport based on diffusion mechanisms; and a resonant tunnelling model."

Comparing the results of each of these calculations should uncover a structure that has carrier transport dominated by diffusion rather than tunneling. Another of the team's goals is to develop detectors operating in other regions of the infrared spectrum.

"The first QCD detecting in the terahertz is under study, and in the immediate future the first thermal imager based on QCD detectors should be fabricated."

A. Buffaz et al. Appl. Phys. Lett 96 172101 (2010)

Exceptional research award goes to Bhattacharya

This year's Welker Award was conferred at the 37th International Symposium on Compound Semiconductors – ISCS – in Takamatsu, Japan. The prize inaugurated in 1976 and sponsored by OSRAM is awarded for exceptional research conducted in the field of compound semiconductors.

This year, the award goes to Pallab K. Bhattacharya, professor at the University of Michigan, for his pioneering work on photonic devices, which are based on III-V compound semiconductors.
With more than 500 publications in the course of his long career Professor Bhattacharya has gained valuable insights in the fields of electronics and optoelectronics.

Outstanding progress was particularly achieved for optoelectronic integrated circuits (OEIC), quantum dot lasers and infrared photodetectors based on his extensive expertise for semiconductors processing technology. Bhattacharya's research accomplishments and his position as one of the most important opinion leaders in the field of III-V compound semiconductors are now acknowledged with the Welker Award.

MOCVD for nanowires

AIXTRON AG has announced a new order for one CRIUS deposition system from the University of Duisburg-Essen. The order was placed in the fourth quarter of 2009 and the system will be delivered in the second quarter of 2010 for the University of Duisburg-Essen Semiconductor & Optoelectronics Center in Duisburg, Germany. The system will be supplied in a 3x2-inch configuration and comes equipped with a ARGUS multichannel pyrometer.

Prof. Dr. rer. nat. Franz-Josef Tegude, Chair of Semiconductor Technology, comments, "We selected the AIXTRON CCS system as part of the University's initiative to acquire a nitride material system for the nitride nanowire NaSoL Project. Overall, we have always been very satisfied with the quality of AIXTRON engineering, processes and service. Of course, we also took into consideration our project partnership. "

The NaSoL Project aims to achieve production of GaN- and (Al,Ga,In)N-based semiconductor nanowires for improved efficiency solar cells and LEDs. The AIXTRON CCS system will provide us with a firm foundation for a smooth and rapid development program for all our partners." NaSoL, which stands for "Halbleiter-Nanodrähte für Solarzellen und Leuchtdioden"*) will result in a new generation of semiconductor nanowires for solar cells and LEDs.

The intention is to replace more costly traditional semiconductor fabrication techniques with MOCVD. Nanowire-based materials have a number of excellent characteristics and offer improved economics. They are not only significantly more efficient both in absorption and in the emission of light, but also promise very low losses in energy transport.

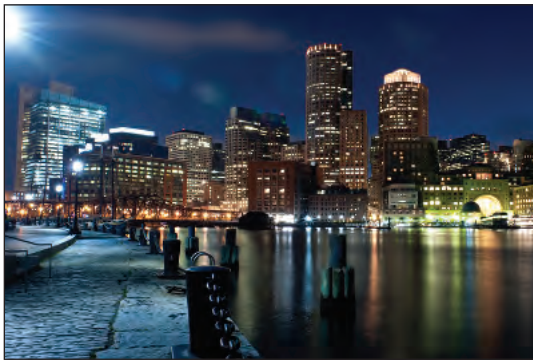
The nanoscale coaxial core-shell heterostructure of these devices has a larger surface area so it absorbs more light and delivers better efficiency. In addition, the new technological process offers device fabrication on lower cost substrates.

Development Centre Opens near Boston

NXP Semiconductors is opening a high performance radio frequency (RF) product creation center (PCC) in Massachusetts. The new facility will focus on the design of RF and Microwave integrated circuits (ICs) used in demanding applications such as defense & aerospace, Industrial, Scientific and Medical (ISM) satellite receivers and broadband communications.

"This new product creation center builds upon NXP's 50-year heritage in RF innovation, further refining, localizing and extending that competence to meet customer demands and create innovative applications," said John Croteau, Senior VP and general manager of the High Performance RF and Lighting business lines at NXP Semiconductors. "Process, packaging and circuit design innovation remain pillars of our strategy, yielding leadership positions in technologies such as SiGe:C, LDMOS and JESD204A."

Ian Gresham, general manager Boston PCC, NXP Semiconductors, pointed out, "The deep pool of experienced and talented RF designers, the active RF customer base and the closeness to Europe make Boston



the ideal location for the new NXP PCC. The PCC team will endeavor to push the limits of our high performance RF & Microwave products overcoming market challenges through innovation."

NXP also has a long history as one of the industry's leading compact model developers, so all technologies are supported by their associated, fully characterized RF models. This in-house process supports the company's global design teams in leading innovation and the development of products and solutions for some of the most pressing RF front-end challenges.

Improving efficiency through power supply

Manufacturers of compound semiconductors look for every opportunity to improve process or yield. HÜTTINGER discusses the energy supply needs for manufacturers and decide that efficiency and robustness are the main requirements for power supplies in semiconductor production.

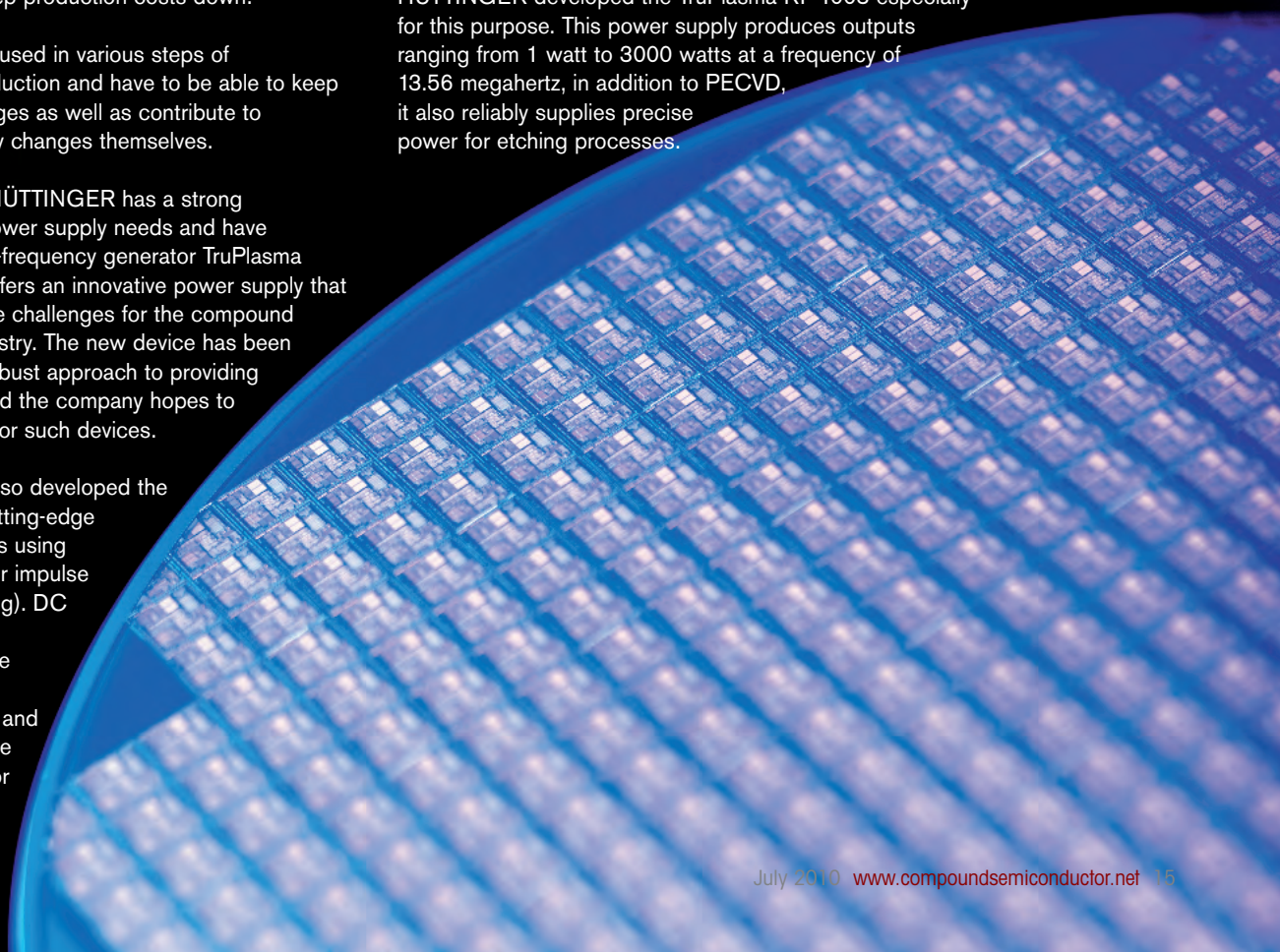
The semiconductor industry is constantly faced with significant change as the industry continues to scale devices and develop new manufacturing techniques. Extreme fluctuations in supply and demand, merciless price wars and short innovation cycles contribute to continual pressure on companies. To remain competitive, companies must be flexible, innovative and constantly find new methods to keep production costs down.

Power supplies are used in various steps of semiconductor production and have to be able to keep pace with any changes as well as contribute to productivity with any changes themselves.

German company HÜTTINGER has a strong understanding of power supply needs and have introduced the high-frequency generator TruPlasma RF1003 they feel offers an innovative power supply that keeps abreast of the challenges for the compound semiconductor industry. The new device has been developed with a robust approach to providing energy efficiency and the company hopes to set new standards for such devices.

HÜTTINGER has also developed the ideal solution for cutting-edge trench-filling process using HIPIMS (high power impulse magnetron sputtering). DC generators from the TruPlasma Highpulse Series 4000 are designed to reliably and accurately supply the necessary energy for these processes.

In fabricating IC circuits, thin layers of materials are applied to a wafer's surface and required structures are constructed. The layering and etching processes often use plasma sources due to high production qualities. To deposit amorphous silicon (a-Si), micro crystalline silicon (μc-Si), SiO^2 and SiNx onto the wafer, PECVD (plasma-enhanced chemical vapor deposition) processes are used. HÜTTINGER developed the TruPlasma RF 1003 especially for this purpose. This power supply produces outputs ranging from 1 watt to 3000 watts at a frequency of 13.56 megahertz, in addition to PECVD, it also reliably supplies precise power for etching processes.



Right: HE_2313 The power supply generating the plasma is a key component of plasma based processes

The TruPlasma RF 1003 has new power combiner technology, called CombineLine, that allows extreme stability for processes.

CombineLine delivers a 50-Ohm output impedance from the power supply, enabling CombineLine to adjust the process optimally at any time. Adjustment networks keep the process constant at an impedance of 50 Ohm. When ideally adjusted, the optimum HF output is introduced into the process.

However, in actual plasma processes, fluctuations always occur that change plasma impedance. The connected matchboxes can react during a limited error adjustment time and re-establish the 50-Ohm state in a matter of seconds. During the error adjustment phases, reflected outputs flow back to the power supply, calling for a quick, precise surge in the power output to hold the energy input steady for the plasma. The reflected output needs to be absorbed into the power supply without damaging it.

This can be done as the combiner technology has a dedicated absorber that can continuously deflect an output of 600 watts. For short-term total reflections of output (short circuit with up to 3 kilowatts of reflected output), the internal components are sufficiently shielded to ensure no damage occurs and that the power supply is operating at the highest plasma stability. CombineLine ensures the defined output is accurately delivered by means of a very broad impedance range.

The results are stable processes for all output ranges. Deposition and etching processes are supplied with precise processing energy required which allows less energy to be used while achieving reproducible results and a higher yield.

An additional benefit of the TruPlasma RF 1003 is an efficiency factor level of more than 80 percent. Due to this efficient energy conversion, the generator is able to reduce energy costs for the user. The source of this high energy conversion level is a special design for internal HF switching phases.

The D converter class employs an optimally adjusted conversion principle produced by interconnecting the high-performance MOSFETs and a low-loss output network. The power supply therefore makes a major contribution to energy efficiency, protecting the environment as well as the customer's bottom line.

With its compact housing in a half 19" design (216 mm x 133 mm x 381 mm), the TruPlasma RF 1003 is ideal for system integration in plasma deposition tools. The CombineLine technology provides a choice of cable length for connecting the matchbox and processing chamber that makes integration unbelievably easy and sets new benchmarks for efficiency.

TruPlasma RF 1003

HIPIMS generators for efficient and high-level trench-filling

Trench-filling with the help of HIPIMS processes is a cutting-edge process in semiconductor manufacturing. As semiconductors become smaller and smaller, the depth-width ratio of the film layers applied to the wafer changes. This change is making it increasingly difficult to fill the trenches. The use of HIPIMS processes makes it much easier to do this.

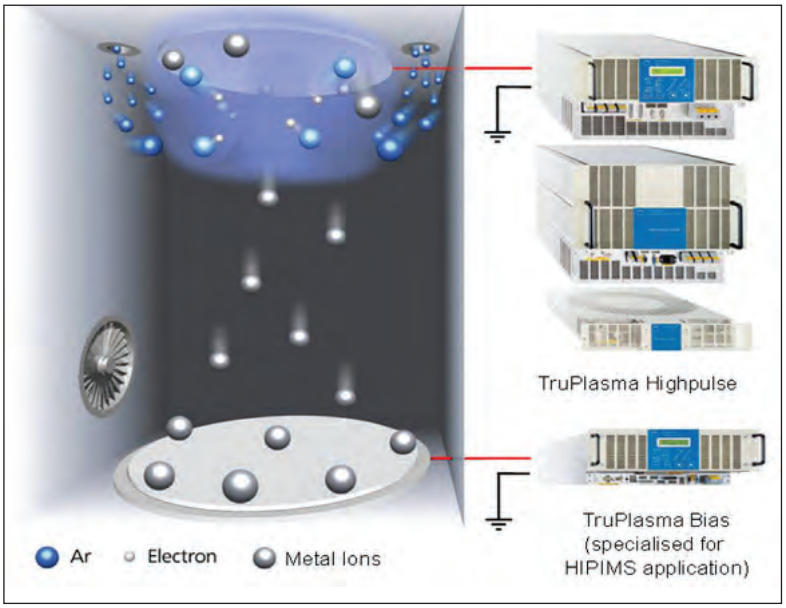
The essential difference between DC and HIPIMS plasmas is the percentage of ions in the sputtered material. While no ionization occurs in DC plasma, HIPIMS plasma has an ionization rate of up to 90 percent – the result of highly energetic pulses in the megawatt range from the HIPIMS power supply. Ionized particles lead to other mechanisms in growing layers. Moreover, an ionized particle stream with a calculated bias voltage travels directly to the substrate. This is how high filling

grades are achieved on uneven substrate surfaces for targeted deposition.

The TruPlasma Highpulse Series 4000 from HÜTTINGER offers the right power supply for both the lab and volume production plants. Pulse outputs from 1 megawatt to 8 megawatts allow for a broad range of scaling. And with little effort, conventional DC cathodes can be run with the HIPIMS power supply, so the new process can be tested and future volume production implemented.

Summary

The use of innovative power supplies offers clear advantages in semiconductor production. Whether for deposition by means of PECVD or for trench-filling through HIPIMS, modern generators provide for stable processes, an increased film quality and fewer defects. They reduce costs considerably and make production processes more efficient, thus contributing to easing price pressures in the semiconductor industry and creating a competitive advantage for companies.



Above: Schematic set up of HIPIMS

Is nanometer-scale III-V CMOS cool enough to rejuvenate Moore's Law?

Scaling silicon ICs involves packing transistors closer and closer together, and this is pushing the power density on the chip towards its limit. Switching to III-V CMOS offers a promising way forward, but can this alternative technology be scaled to a few nanometers, manufactured in really high-volume and made in such a way that it has the look and feel of the silicon incumbent? **Jesús del Alamo from MIT** discusses the issues.

In 1971 the silicon industry entered a new era: production of the first programmable computer processors. The debut chip, the Intel 4004, purred away at 740 kHz and employed 2300 transistors with a line width of 10 μm.

Since then Intel has continually improved performance levels through scaling and technology innovation: its Core i3, Core i5, and dual-core mobile Core i7 processors that were released in the last year or so zip along at gigahertz speeds, and contain billions of transistors with feature sizes of tens of nanometers.

This tremendous improvement in chip performance that has occurred over the last four decades is a largely a result of scaling down the dimensions of the silicon transistor. Continuing in this vein will bring about further progress, but it is getting much harder with every new CMOS generation. That's because with increases in transistor density, power dissipation has reached a practical limit and chips are running very hot. There is now no headroom left unless one is willing to use expensive new packaging and active cooling.

The way forward in this new "power constrained scaling" phase of the silicon industry is to reduce the transistor's operating voltage. With silicon transistors, driving the voltage down while simultaneously enhancing transistor performance has become increasingly difficult, and the operating voltage for CMOS has bottomed at about 1 V for the last few generations of technology. This trend is a serious threat to further progress for the silicon IC. One way to alleviate this looming bottleneck is to switch to a channel with a far higher carrier velocity, which would allow further voltage scaling and better performance.

Several materials could fulfill this role, but by far the most promising are III-V semiconductors: their capabilities at high frequencies are proven; their reliability is also well established; and their deployment in the power amplifiers of mobile phones shows they could be used to manufacture chips in high-volumes in a cost-effective manner. In fact, III-Vs seem the obvious choice, because

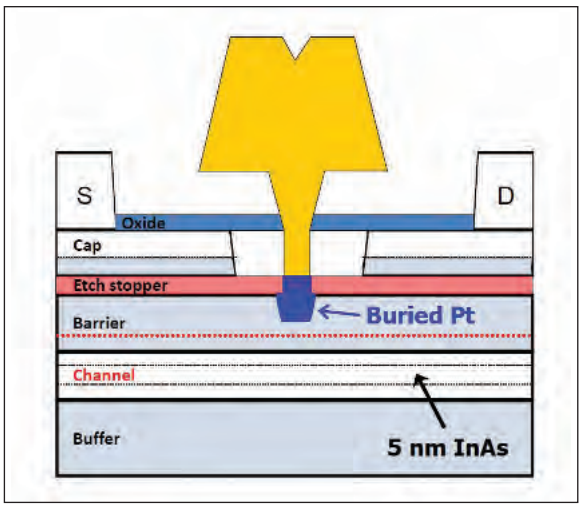


Figure 1. Jesús del Alamo's group at MIT have fabricated HEMTs on an InP substrate that feature a 10 nm-thick channel, which includes a 5 nm-thick, pure InAs core surrounded by an InGaAs cladding. T he barrier is InAlAs, lattice-matched to InP. There is a low resistance InGaAs/InAlAs cap above a thin InP etch-stop layer. The gate is fabricated through a triple-recess process, and its stack includes platinum in its bottom layer, which is driven into the barrier in a thermal step. This leads to an effective reductionin the InAlAs barrier thickness to about 4 nm

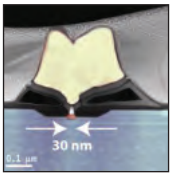


Figure 2. Transmission electron microscopy reveals a gate length for the HEMT of 30 nm

they are the only materials other than silicon with a well-established manufacturing and reliability record.

Room on the roadmap?

The bad news for the III-Vs is that there is a huge barrier for insertion of any new channel material into the CMOS roadmap. At the earliest insertion point that seems plausible today, the gate length will be at most in the 10-15 nm range. This means that the entire transistor will fit in a footprint of less than 100 nm, making it small enough to integrate tens of billions of devices on a single chip. If a disruptive technology such as III-Vs is to stand any chance of success, it will also need to substantially outperform the best scaled silicon option of that day – a performance gain of 30-50 percent seems to be the minimum.

On top of this, a III-V-based approach must also offer the promise of a few scaled generations beyond the insertion node, plus cost-effective manufacturing and unprecedented levels of reliability. Do III-Vs have any chance of success?

One way to answer this question begins by seeing what we can learn from today's devices. An excellent model system is the HEMT, a device with near terahertz capabilities that we have been investigating at MIT for the last few years. Our effort has focused on studying the logic characteristics of InGaAs and InAs HEMTs with gate lengths down to 30 nm. The encouraging news is that these devices exhibit logic characteristics, in terms of current drive and short-channel effects, rivaling state-of-the-art silicon MOSFETs with equivalent gate lengths.

Our transistor portfolio features HEMTs with a channel just 10 nm thick that includes a pure, 5 nm-thick InAs core (see figures 1 and 2). The InAlAs barrier in this structure has an effective thickness of just 4 nm, and the combination of this thin barrier and channel creates a device with excellent short-channel effects that can be scaled to 30 nm gate lengths.Devices with this gate length have excellent output characteristics with very good current drive. HEMTs operating in enhancement mode (V_T=80 mV), an essential requirement for logic applications, have a peak transconductance 1.8 mS/μm at a V_{DS} of just 0.5 V. Measuring performance at this source-drain voltage makes a lot of sense, because if III-V CMOS technology is to succeed, it will have to work at voltages substantially below 1 V.

For logic applications, subthreshold characteristics are more relevant (see Figure 3). Our measurements on 30 nm gate length devices show the drain current dropping sharply below threshold, and the subthreshold swing, which characterizes this drop off, is 73 mV/dec. In addition, the threshold voltage depends little on the value of V_{DS}. This is an important figure of merit in logic applications, called DIBL for drain-induced current lowering, because it insures the reliable operation of the transistors in diverse circuit environments. Our device has a DIBL of 85 mV/V. This value and that for the subthreshold swing are as good as the best silicon MOSFETs of similar gate lengths.

Though less relevant for logic applications, these devices also display remarkable high-frequency characteristics. At a V_{DS} of 0.5 V, they have a current gain cut-off frequency f_t of 601 GHz and a power-gain cut-off frequency f_{max} of 609 GHz. As far as we know, this is the first transistor of any kind, on any material system, that simultaneously exhibits both f_t and f_{max} in excess of 600 GHz. The important implication of these results is that minimizing parasitics and enhancing short-channel effects not only optimizes logic operation - it also yields extraordinary frequency response. This bodes well for the prospects of a future ultra-low power, mixed-signal, terahertz-logic technology based on III-Vs.

One way to make a meaningful assessment of the logic potential of candidate device technologies is to define a figure of merit that integrates performance and short-channel effects. Since key goals in scaling are to maximize the "on" current and minimize the "off" current, a suitable figure of merit is the value of I_{ON} for a fixed I_{OFF} at a fixed operating voltage.

We have determined this figure of merit for our HEMTs, and found that it not only exceeds that for current CMOS technology – it beats that predicted for future generations of the incumbent technology too (see Figure 4). This performance gap is more impressive than it first appears, because silicon MOSFETs have a typical source resistance of 80 Ohm.μm, nearly three times lower than that of our InAs HEMTs. Clearly, there is plenty of headroom for improvements in the performance of our III-V transistors, so long as the extrinsic portion of the device can be properly engineered. One wonders, in fact, how far III-Vs could go?

It takes some work to answer this question. The first step is to extract the electron injection velocity at the *virtual* source, which is the velocity that matters to determine the current in a FET in saturation. We have recently measured this in great detail for different channel compositions, and obtained values in excess of $3x10^7$ cm/s for 30-40 nm gate-length devices operating at V_{DS}=0.5 V (see Figure 5). This set of results shows that increasing the indium-content in the channel increases injection velocity, and that is it possible to reach values that are twice those seen in strained silicon. What's more, this doubling of speed is possible with operating voltages that are less than half of those used in strained silicon CMOS.
Any evaluation of the true potential of III-Vs must also consider potential implications of their low effective mass, such as their small density of states (DOS) and corresponding low quantum capacitance. This could blunt the scaling of the vertical dimensions of the FET and its overall scalability.

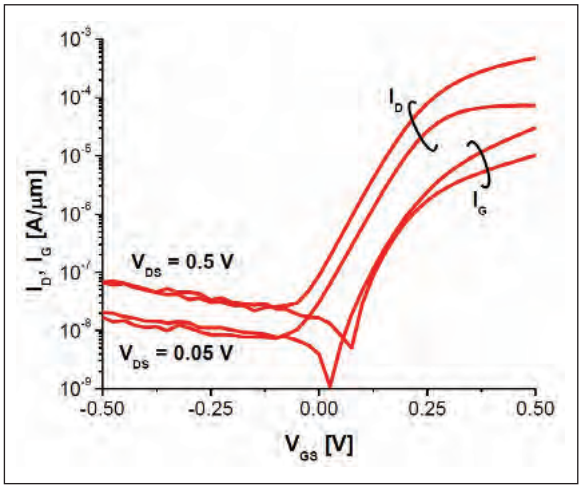


Figure 3. The drain current of InGaAs HEMTs drops off rapidly below threshold.

To address these concerns we have recently carried out a theoretical and experimental study of gate capacitance in advanced InGaAs and InAs HEMTs. Our conclusion: there is a significant increase in the DOS effective mass and the sheet charge density in the InAs channel resulting from the non-parabolicity of its conduction band coupled with channel quantization and biaxial compressive strain. Based on these findings, we believe that it is eminently feasible to produce III-V transistors with 10 nm gate lengths operating at V_{DD}=0.5 V, which have a sheet carrier density in the mid 10^{12} cm^{-2} range.
The upshot of these two recent results – the injection velocity and scaled gate capacitance – indicates that a 10 nm gate-length III-V FET with a thin InAs channel should be capable of reaching a drive current of about 1.5 mA/μm (this will require a source resistance of 80 Ohm.μm). If our predictions are correct, III-V CMOS can deliver a level of performance well above that of the silicon equivalent, even assuming the most optimistic scenario for the incumbent technology.

But is it possible to turn hope into reality by re-engineering our HEMTs, so that they can scale down to these dimensions and realize the desired level of performance? Probably not. Substantial gate leakage current is already present at 30 nm gate lengths (see Figure 3). This is because of the thin InAlAs barrier that separates the gate from the channel. Any further reductions in gate length will demand additional gate barrier thickness scaling yielding intolerable gate leakage currents. So, our HEMTs are already very close to their scaling limit, at least from the logic point of view.
The inevitable conclusion is that a future 10 nm III-V logic FET will require a high dielectric constant ("high K") gate dielectric, something that will only be possible via profound re-engineering of the device.

The development of a reliable, manufacturable gate stack that includes a high-K gate dielectric and yields a high-quality semiconductor interface with a III-V compound semiconductor is as intriguing as any problem in modern semiconductor technology. Like all great challenges, it has been attracting great interest. Recent research from around the world has shown the great promise of ex-situ Atomic Layer Deposition (ALD) and MOCVD for depositing high-K dielectrics on suitably treated InGaAs surfaces. ALD, in particular, has demonstrated its capability to engineer the bonding structure at the III-V surface. This holds the key for Fermi level unpinning and attaining a low density of interface states.

The gate stack is actually one of a handful of very challenging technical problems that must be solved before a III-V CMOS technology can become a reality (Figure 6). Scaling down transistor size is another major concern. Will it be possible to scale III-V transistors to the required dimensions, while preventing excessive short-channel effects and realizing the low levels of parasitic resistance that are required? We can't tell at this point. Straight scaling of the extrinsic region of a modern HEMT to the dimensions required for a 10 nm III-V MOSFET would result in an external resistance two orders of magnitude too high. Addressing this is going to require extensive technology development and simulations. Fortunately, our HEMTs have also served to calibrate modern device simulators, which reproduce their characteristics quite well. These are valuable tools to predict device characteristics in the 10 nm range. If planar devices fail to

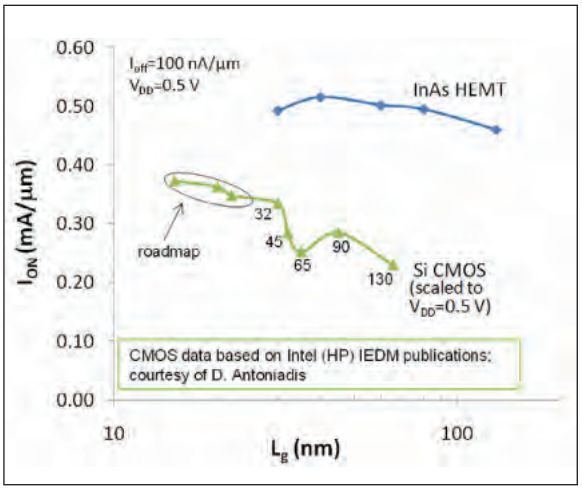


Figure 4. "On" current for an "off" current of 100 nA/μm at V_{DD}=0.5 V as a function of gate length for InAs HEMTs made at MIT. This is a figure of merit that aggregates performance and short-channel effects. For reference, recent scaled silicon CMOS technologies are shown. These data are courtesy of D. Antoniadis (MIT) and are based on detailed analysis of Intel's High Performance CMOS technologies presented at IEDM. Also added are projections from the International Technology Roadmap for Semiconductors

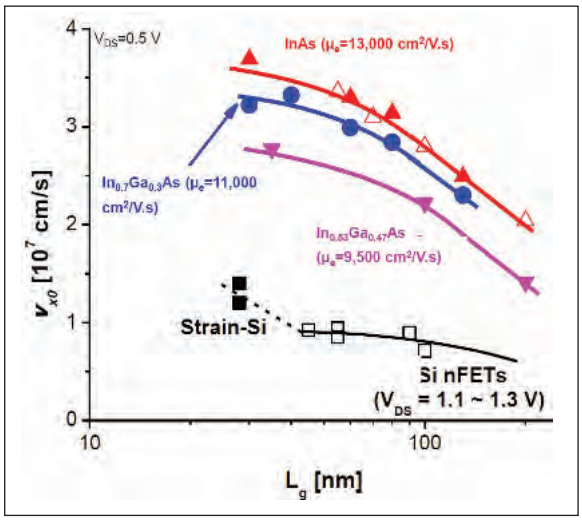


Figure 5. Injection velocity at the virtual source in InGaAs and InAs HEMTs fabricated at MIT as a function of gate length at V_{DD}=0.5 V. For reference, results from bulk and strained silicon CMOS are also included (V_{DD}=1.1-1.3 V). In spite of operating at less than half the voltage, InAs and InGaAs HEMTs significantly outperform silicon MOSFETs

yield the required short-channel effects at the desired lengths scales, we can resort to developing three-dimensional devices. In the silicon domain, FinFETs and nanowire transistors are serious contenders for the 22 nm CMOS node and perhaps beyond. Three-dimensional device demonstrations in III-Vs give hope to this avenue. GaAs FinFETs and InAs nanowire transistors with impressive characteristics have been demonstrated at Purdue, Lund University and other places.

Dealing with the holes

Most III-Vs have very high electron mobilities, making them ideal for n–channel devices. But CMOS needs p-channel transistors too, and the hole mobility for III-Vs is too low - for many arsenides, it is actually lower than it is for silicon. Mobilities in silicon have improved through the addition of strain in the material, with the performance of the p-channel now approaching that of its n-type cousin. It will be interesting to see if the same trick will work for the arsenides.

Other options for the p-channel are also available. Measurements have revealed antimonides mobilities in the 1500 cm^2/V.s range and p-channel transistors have already been fabricated. Germanium transistors are also of interest. Germanium has a high hole mobility that is enhanced through strain. It also has the advantage of being nearly lattice-matched to GaAs. This suggests a possible CMOS platform in which germanium and III-V transistors are integrated side by side.

Last but by no means least on the list of major challenges is the need for a future III-V CMOS technology to closely "look and feel" like the silicon incumbent. Meet this goal and III-V CMOS can then exploit the tremendous economy of scale in the silicon industry. The most likely incorporation of III-Vs in the CMOS road map is via an enhancement to the existing technology through the insertion of a III-V channel - much like the recent additions of high-K/metal gates or strain. Exactly how this plays out will be influenced by what emerges as the best option for the p-channel device, and it is possible that the future will witness two different channel materials sitting side by side, on top of a silicon wafer.

With III-Vs knocking on the door of the CMOS roadmap, it's clear that the present generation of III-V scientists and engineers have an opportunity ahead of them to shape the future of mainstream electronics. Has there ever been a better time to be a III-V semiconductor technologist?

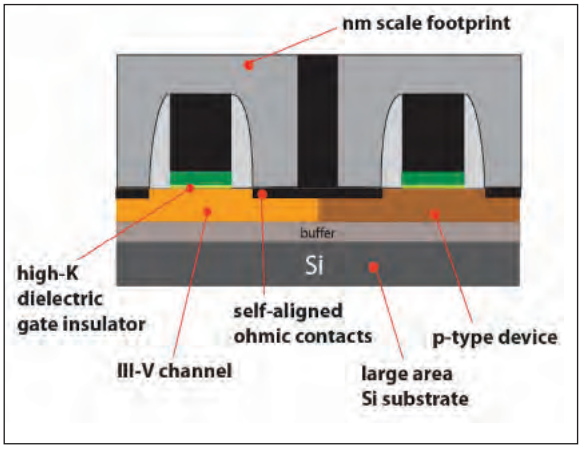


Figure 6. This diagram outlines key challenges to a manufacturable III-V CMOS logic technology

Acknowledgements

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Further reading

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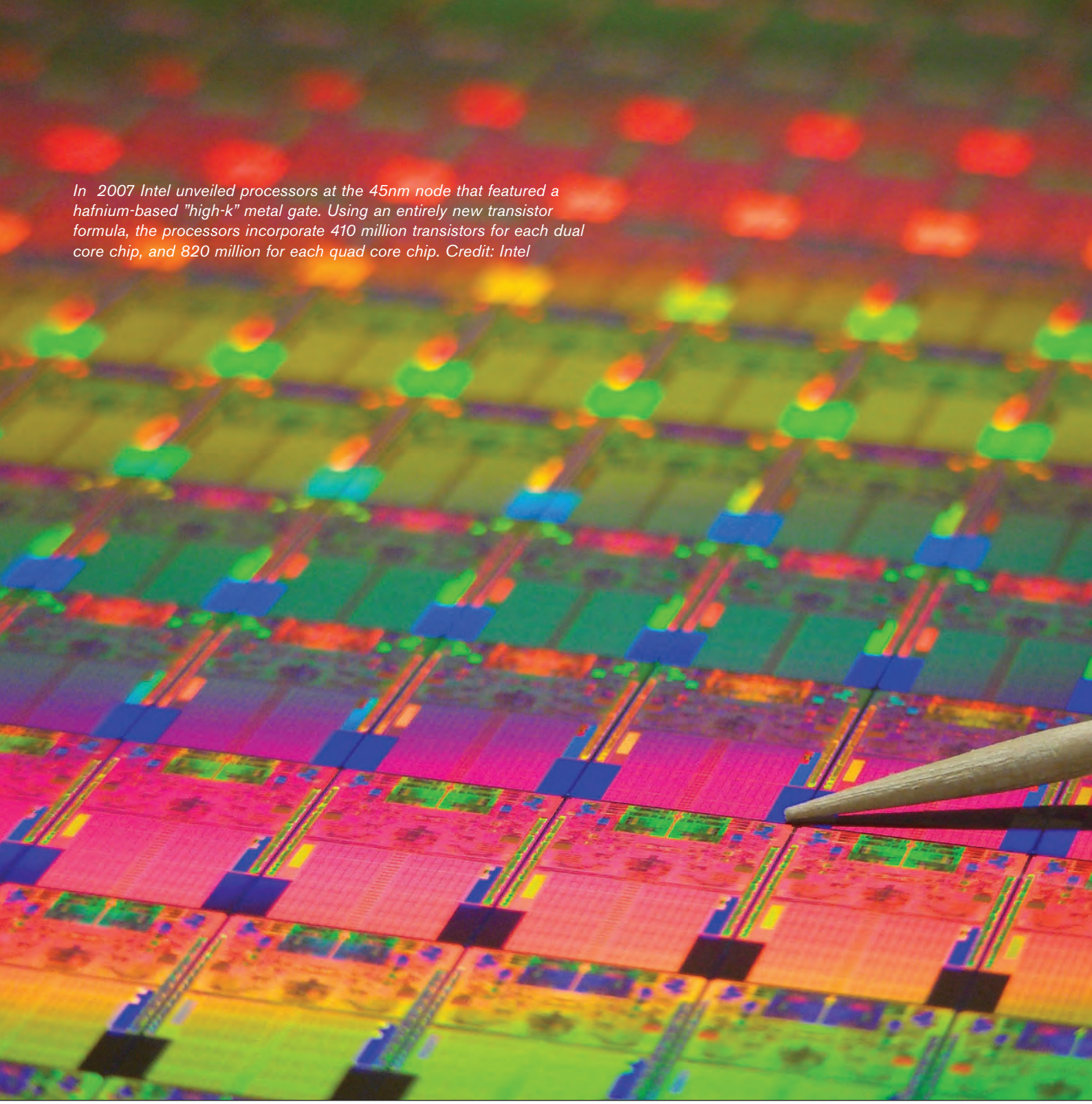
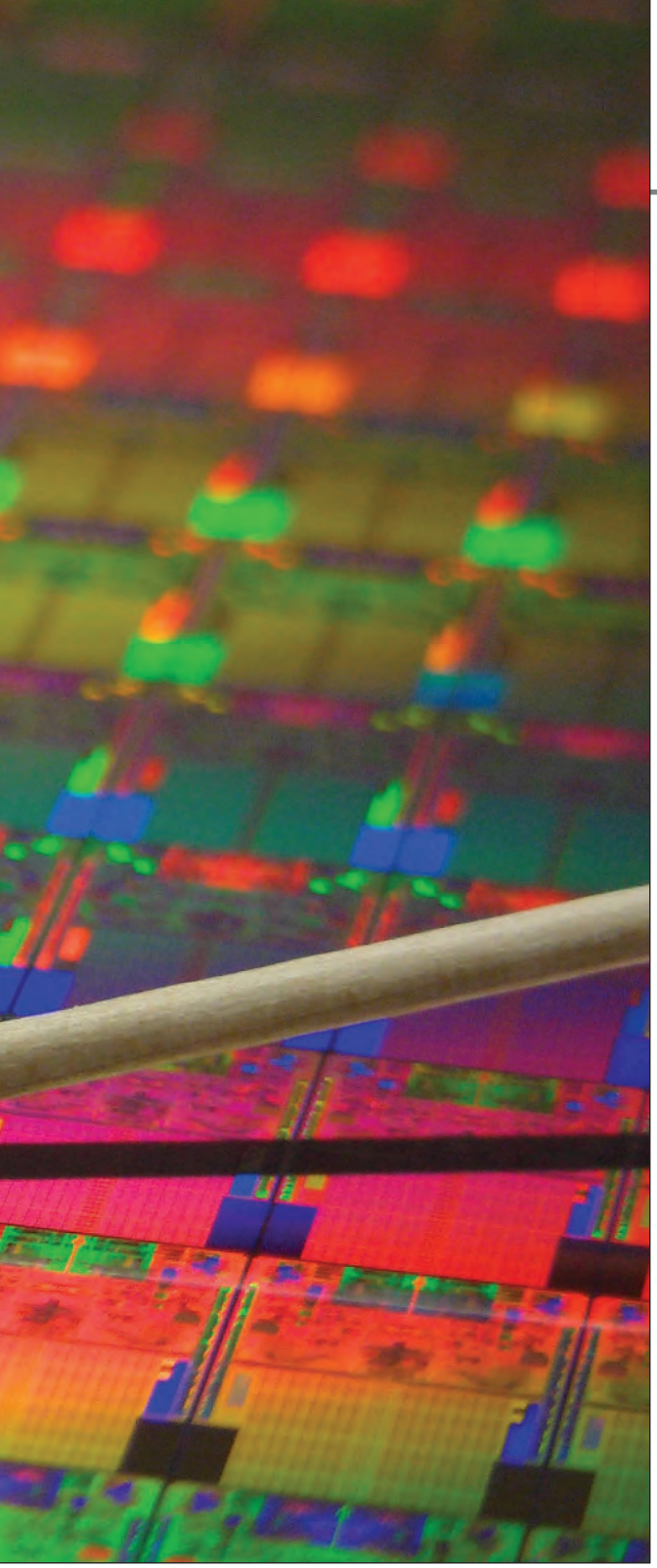


In 2007 Intel unveiled processors at the 45nm node that featured a hafnium-based "high-k" metal gate. Using an entirely new transistor formula, the processors incorporate 410 million transistors for each dual core chip, and 820 million for each quad core chip. Credit: Intel

Uniting III-Vs and germanium for CMOS

Unleashing the high electron and hole mobilities of InGaAs and germanium in an evolutionary CMOS architecture is possible by introducing a common gate stack. This can be formed by a combination of a sulfur-based treatment and deposition of aluminum oxide, and results suggest that this process does not hamper the performance of these novel devices, says **IMEC's Thomas Hoffmann.**



It is nigh on impossible to overstate the progress of CMOS technology since its invention in the 1960s. Most of these tremendous gains have resulted from shrinking the size of the transistors, and for the first four decades no major modifications were needed to the design of the device that exploited the great interface between silicon and silicon dioxide.

But this pairing of silicon and its native oxide could only go so far, and more recently progress has hinged on the introduction of new materials. For example, in 2007 Intel introduced a high-k dielectric based on the far more exotic material, hafnium, into its production process to prevent high leakage currents in its 45 nm node Core 2 Duo process.

Advances like this, along with the introduction of metal gates, provide a massive boost to everyone developing alternative forms of CMOS, such as those who dream about replacing the conventional silicon channel with much higher mobility materials, like germanium and III-V compounds.

Although there is still much to do to make this dream a reality, some progress has been made. In particular, breakthroughs in germanium and InGaAs surface channel MOSFETs have brought the research community far closer to unleashing the potential of these high-mobility channel materials, for high drive current at scaled supply voltage.

Efforts, including those by our team of researchers at the European research center imec, have shown that germanium-based channels are very promising for making high-performance p-FETs. And similar developments, at Intel in particular, have unveiled the great potential of InGaAs channels for the n-FET.

Integrating those two strong contenders under a conventional CMOS process is formidable, and requires overcoming a handful of challenges: growth of selective and defect-free high-mobility materials on a silicon substrate, despite the intrinsic, large-lattice-mismatch; formation of ultra-low resistance contacts to a III/V material; and excellent electrical passivation of the interface between the high-k dielectric and the alternative channel materials.

The latter challenge is particularly tough in the case of CMOS integration, because a common gate stack strategy is necessary in order to passivate the different materials for forming surface-channel devices: germanium (p-FET) and InGaAs (n-FET). We are now working on this problem, and considering a range of architectures for combining a III-V n-MOSFET and a germanium p-MOSFET, such as that shown in Figure 1.

Nearly all well-functioning high-k dielectrics that employ a low-equivalent-oxide-thickness (EOT) material on silicon still start with a thin Si/SiO_2 interfacial layer, and the high-k dielectric is then deposited on top. This route is chosen because the pairing of silicon and its native oxide is a great combination in terms of material quality. A great deal of effort has been applied to mimicking this $silicon/SiO_2$ interface on germanium and III/V materials by introducing an ultra-thin silicon cap that is just a few monolayers thick and can act as a surface passivation layer. Germanium channels have benefited from this approach, and we have

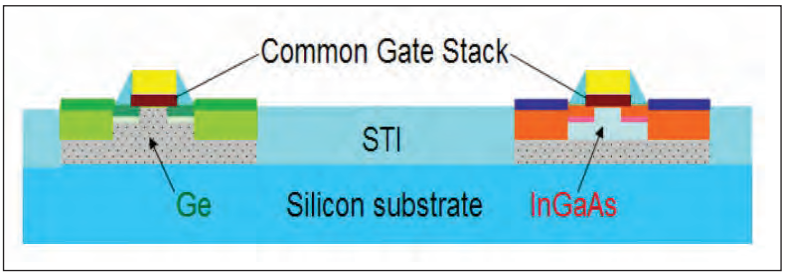


Figure 1: A common gate stack is essential for enabling the high mobilities of germanium and InGaAs to make an impact in future CMOS technology

shown that this can lead to improvements in pMOS devices. (This is not the only route to passivating germanium surfaces, and alternative approaches include thermal deposition of a GeO_2 or GeON interfacial layer, and deposition of some high-k dielectrics).

Turning to the III-V devices operating in inversion mode (the configuration that's suited to digital applications and employed in silicon), the key issue here is to address the near-midgap Fermi level pinning. This results from the high density of states at the high-k/III-V interface, which leads to a less efficient channel potential control from the gate. The implication is that the kind of high-k material used as a gate oxide probably has a secondary impact on the nature and energy distribution of the interface states and, hence, on the Fermi level pinning point. However, the density of interface traps (D_{it}) can be strongly affected by the type of surface preparation used, which could be cleaning or various passivation treatments.

To address the integration of these high-mobility MOSFETs, we have proposed a common gate stack approach for both the germanium p-MOSFET and InGaAs n-MOSFET. This is based on the duality of the oxide-semiconductor interface properties found on the germanium and $In_{0.53}Ga_{0.47}As$ MOS samples. Both of these have undergone a sulfur-based wet-chemical treatment, followed by the growth of an Al_2O_3 common gate dielectric by atomic-layer deposition (ALD) (see figure 2).

After native oxide removal, both of these substrates were treated in ammonium sulfide solution, prior to ALD of Al_2O_3 in a reactor chamber. This is followed by post-deposition anneals at 400 degress C with forming gas. The sulfur treatment process helps to reduce formation of a native oxide, according to our images of the aluminum oxide capped samples (figure 2).

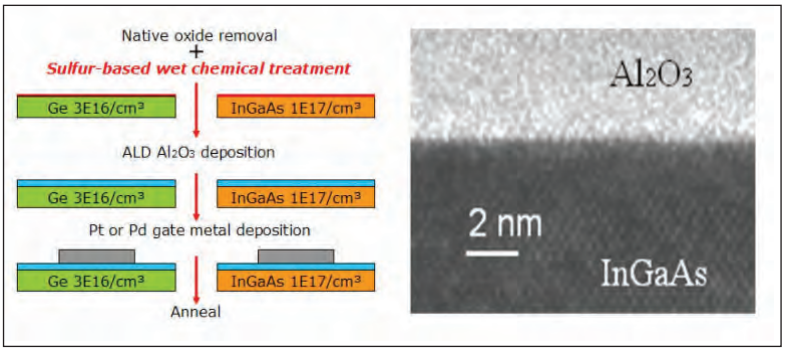


Figure 2. imec has fabricated MOS capacitors with a common gate stack process

To realize high performing devices, it is essential to not only have high channel mobility, but also good "on/off" switching characteristics. Turning the device from its "on" to "off" configuration causes a shift in the channel energy level from a position close to the band edge (conduction band for n-FET, and valence band for p-FET) towards the mid-gap. Efficient swing of the channel potential by the gate bias requires a low level of interface traps in the range of interest (nFET: upper half of the bandgap; pFET: lower half of the bandgap), so it is critical to obtain a sufficiently low level of these traps in those respective regions of device operation.

This is possible, according to our measurements of the density of interface traps in germanium and InGaAs MOS interfaces that have been fabricated using a process capable of producing a common gate stack (see Figure 3).

This data reveals high levels of interface traps in germanium on the conduction band side, and in InGaAs on the valence band side, which can be attributed to acceptor-like and donor-like traps, respectively. A low density of interface traps at the germanium valence band edge suggests less donor-like traps and implies that more

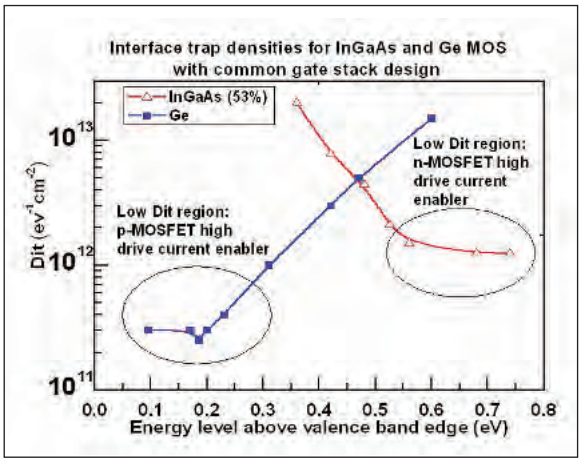


Figure 3: Distributions of the density of interface traps, which are deduced from measured conductance data, show the relatively low number of traps near the valence band of germanium and the conduction band of InGaAs

To realize high performing devices, it is essential to not only have high channel mobility, but also good "on/off" switching characteristics. Turning the device from its "on" to "off" configuration causes a shift in the channel energy level from a position close to the band edge (conduction band for n-FET, and valence band for p-FET) towards the mid-gap. Efficient swing of the channel potential by the gate bias requires a low level of interface traps in the range of interest

free carriers (holes) can be collected in the p-channel. Similarly, the low density of interface traps levels near the InGaAs conduction band edge means less acceptor-like traps and more free electrons for forming the n-channel.

Such features are encouraging. Not only do they make transistor operation possible - they allow the high carrier mobility nature of the germanium p-MOSFET and InGaAs n-MOSFET to be unleashed.

To verify this promise, we have fabricated inversion-type surface-channel MOS transistors with 8 nm of Al_2O_3 on both germanium substrates with n-type doping of 3 x 10^{16} cm^{-3}, and $In_{0.53}Ga_{0.47}As$ substrates with p-type doping of 1 x 10^{17} cm^{-3}. These have been produced with exactly the same oxide stack process that we have already described.

These self-aligned germanium and InGaAs MOSFETs that are built with common gate stack design have produced a very encouraging set of results. These include drain currents of 600 mA/mm and 200 mA/mm at a 2.5 V gate bias swing for InGaAs and germanium MOSFETs respectively. Both transistors have a gate length of 1.5 μm (see Figure 4).

The mobilities in the channels of our common gate stack MOSFETs with 10 μm gates are comparable to the best-reported values anywhere: Hole and electron field-effect mobility values are 400cm^2/V-s and 1300cm^2/V-s, respectively. Producing these results with the common gate stack is a very important breakthrough for the future of alternative CMOS architectures, because it shows that this approach has the potential to draw on the strengths of III-Vs and germanium.

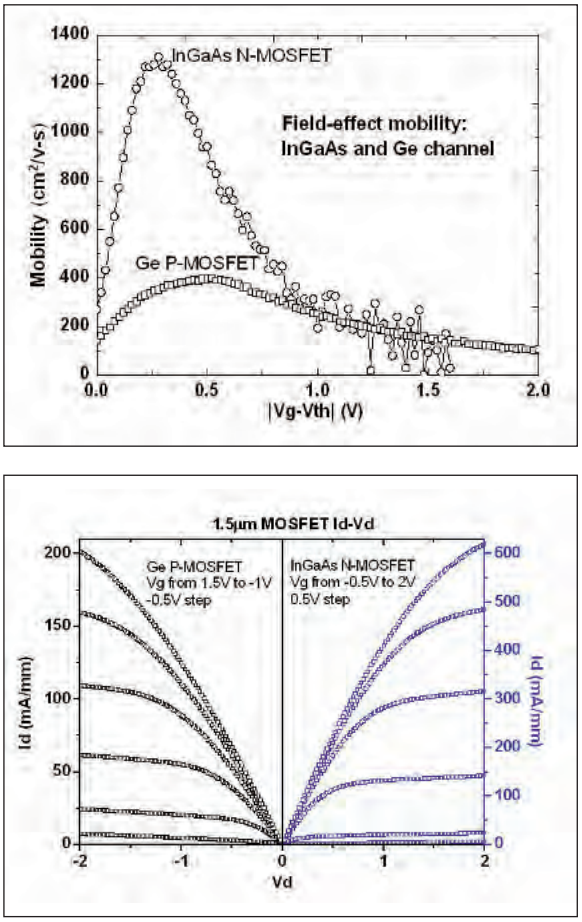


Figure 4: imec's InGaAs and germanium FETs show promising drain currents and mobilities that are comparable to the best results realized anywhere

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Mantech reflects its roots

Increasing GaAs fab throughout, streamlining carrier mobility measurements on pHEMT production wafers and suggesting new ways to improve the performance of this class of transistor featured in this year's CS-Mantech. **Richard Stevenson reports.**

During the middle of the last decade the GaAs-Mantech conference changed its name to CS-Mantech to reflect the expansion of materials used by III-V chipmakers. Since then presentations at this meeting have covered a wider variety of topics, but conference proceedings are still dominated by papers about the manufacture of GaAs transistors. This year was no different, and the delegates that headed to Portland, Oregon, in mid-May, were fed a diet with a large dollop of GaAs. Here we'll look at four of those papers: Skyworks Solutions' account of its fab upgrade to 6-inch; RFMD's non-destructive method for measuring mobilities and sheet charges in pHEMTs; Hitachi Cable's study of pHEMT degradation in BiHEMTs; and the development of a high-frequency HEMT, which was led by researchers at the Indian Institute of Technology–Kharagpur.

Boosting fab throughput

The first of these papers detailed the 4-inch to 6-inch conversion of Skyworks' Newbury Park fab, which processes GaAs HBT and BiFET epiwafers into finished product. Glenn Hafer revealed that these changes led to a 61 percent increase in four-inch equivalent throughput, and a 140 percent hike in die production.

Upgrading the fab was not easy, because conversion had to take place in the existing, fully consumed cleanroom space. In addition, full production output had to be maintained throughout the process, along with no drop in the quality of service provided to every customer.

Implementing the fab upgrade involved the introduction of 27 new tools, plus conversion of another 145 from 4-inch to 6-inch, 8 of which had to be relocated. Switching to the larger wafer size also required development of 51 new 6-inch process recipes to new equipment platforms.

Conversion to the 6-inch fab kicked-off with a high-level, top-down plan that identified the critical phases in the project. A ground-level plan followed, which identified every task needed to complete the fab upgrade. This involved input from every engineer responsible for a particular tool and its process. Once this exercise was complete, it appeared that the entire project could take up to three years; the management wanted it rolled out in just two. So to hit the shorter deadline, the project plan was optimized, with more tasks performed in parallel.

To break this large project down into more manageable

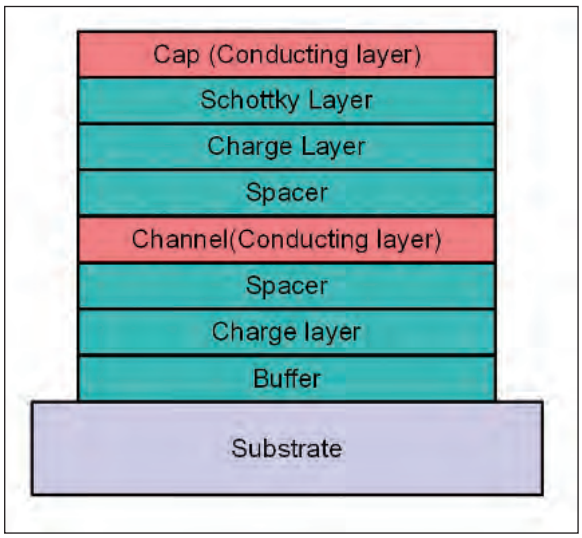


Figure 1. RFMD's pHEMT has two conducting layers: the channel and the cap. It is possible to measure the mobilities in both these layers with a Lakeshore 7612 multi-field Hall system

steps, different staff managed different aspects of the conversion program. By working on smaller projects, those in charge could focus on the finer details.

To keep everyone fully aware of progress, the company held many meetings. Bi-weekly meetings kept senior management informed of progress; various weekly meetings aided internal communication, such as that between factory staff and their managers, or project and program managers; and a daily "9 a.m. 6-inch meeting" helped the company execute efficient production while maintaining project progress. "The number of meetings might seem like overkill, but without them this project wouldn't have been successful," says Hafer.

As the project progressed, tools had to be converted back and forth on many occasions between 4-inch and 6-inch processing. If the technicians were unaware of the latest change, they might have tried to run a process on a tool that was now unsuitable for that task, and wasted good material. To prevent this from happening, a continually updated status for every tool was provided to technicians using a web-based approach.

The day of reckoning arrived when Skyworks tested its first devices produced on its 6-inch line. If failure rates were high, the trouble-shooting needed to remedy this could have taken the company beyond its two-year goal for completing the project. But results were excellent: final test yields for transistors from the first two processes run on the new line were 97.2 percent and 98.0 percent.

Measuring mobilities

Skyworks' biggest rival, RFMD, has also been improving its production process by introducing a Lakeshore multi-field Hall system. This tool allows the company to measure non-destructively, rather than destructively, mobilities in the channel and the cap of a pHEMT plus the channel sheet charge (see Figure 1). Keeping an eye on channel mobility is important, because if it falls too low, this can degrade the transistor's maximum drain current and its drain-source current. However, it is paramount to keep the channel sheet charge close to its target value, because this gives a direct indication of the pinch-off voltage for the FET once the wafers are processed.

The lead author of the paper, Robert Yanka, told *Compound Semiconductor* that carrier mobility in the channel also provides an indication of the condition of the growth system. "When an MBE system is being qualified following a maintenance cycle, mobility can start off low and will rise as the system cleans up. We have specs that let us know when the material is acceptable for delivery to the fab."

Conventional methods for measuring sheet charges and mobilities, such as non-contact sheet resistance approaches and single-field Van der Pauw Hall measurements, are unsuitable for pHEMTs because they fail to distinguish between the high mobility carriers in the channel and the low mobility carriers in the cap. Common ways to determine the sheet charge and carrier mobility in the channel are to either etch away the cap prior to measurement, or to use a specially grown test structure that enables direct measurement of channel properties. Neither approach is ideal. It's not just the added cost that stems from either destructive testing or the growth of additional structures: if the cap is too thin, the depletion layer extends into the channel, and measurements of channel carrier density are underestimated; and if the caps too thick, it contains residual carriers, leading to an overestimate of the channel carrier density.

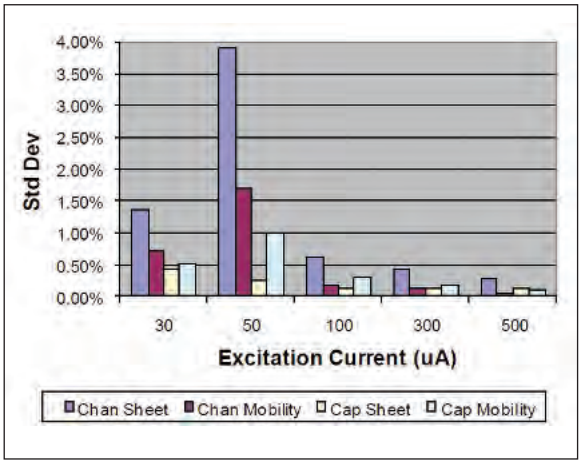


Figure 2. Engineers at RFMD investigated how changes in the excitation current can effect the recorded values of: Channel sheet resistance (Chan Sheet); channel mobility (Chan Mobility); cap sheet resistance (Cap Sheet); and the mobility in the capping layer (Cap Mobility)

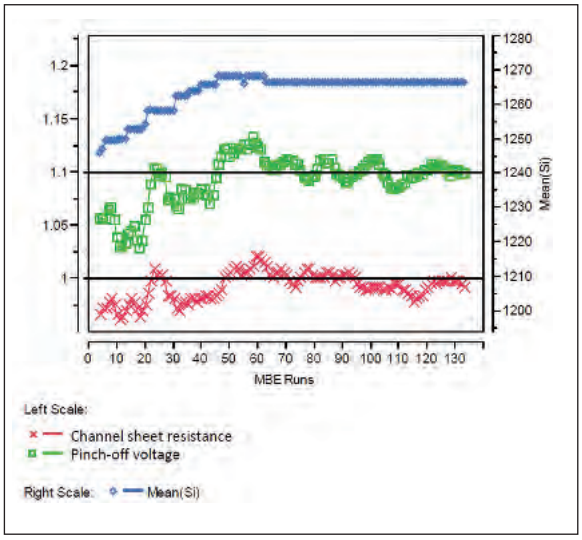


Figure 3. The rapid feedback provided by the Lakeshore 7612 multi-field Hall system makes it an effective tool for process control. Engineers at RFMD used measurements from this instrument to adjust the temperature of the silicon cell, and bring the pinch-off voltage back into the center of the spec. Note the following: the pinch-off voltage and channel sheet resistance values have been normalized; in both cases the data presented is a five-wafer rolling average; and the sign of the pinch-off voltage has been flipped during the normalization process

Multi-field Hall measurements can overcome these issues. The paper presented by Yanka and his co-workers details measurements made on 6-inch wafers produced in a series of runs using magnetic field strengths from 3kG to 15kG and spring-loaded probe pins tinned with indium, which can be "blasted" with a voltage pulse to form an ohmic contact (see Figure 2).

RFMD's engineers use the Lakeshore tool for qualification of MBE reactors following a maintenance cycle. Historical calibrations get the MBE system close to target using multi-field Hall characterization, before a series of three wafers with high, low and nominal doping are then sent for processing to provide the data necessary to finalize the target sheet charge. Growth of product follows, with electrical channel characteristics monitored via Hall measurements on three or four wafers per day.

By monitoring the channel sheet charge density and the pinch-off voltage of processed devices, it is possible to fine-tune the temperature of the silicon effusion cell and produce wafers well within spec (figure 3). Thanks to this feedback, RFMD greatly reduced the number of off-target wafers dispatched for processing.

Optimizing BiHEMT epitaxy

Despite the poor state of the global economy, handset sales are rising again, with the biggest gains in the Smartphone sector. These feature-rich mobile devices incorporate multiple bands and multiple modes, leading to high levels of power consumption and a high chip count. To minimize battery drain and GaAs real estate, some chipmakers have developed processes to unite HBTs with either FETs or pHEMTs. This includes Hitachi Cable, which has been developing a BiHEMT process to unite HBTs and pHEMTs since 2003.

At this year's CS-Mantech, Junichiro Takeda and his co-workers detailed one of the problems that they uncovered when developing the growth process for this product: a reduction in the carrier mobility in the InGaAs channel of their pHEMT from 7000 cm^2/Vs to 5800 cm^2/Vs when this transistor was inserted in their BiHEMT structure (see Figure 4 for details of the device architecture).

To expose the cause of this drop in mobility, engineers used a variety of measurements to compare the pHEMT in the BiHEMT structure with a standalone device. Photoluminescence (PL) measurements produced a peak with the same energy in both structures, indicating that the channel in both pHEMTs had an identical thickness and indium concentration, a conclusion subsequently confirmed by X-ray diffraction measurements.

The PL intensity in the BiHEMT structure was weaker than that from the standalone pHEMT, indicating either an increase in the density of non-radiative recombination centers, or a fall in carrier concentration in this trench. Hall measurements revealed which of these two possible scenarios was to blame: The channel carrier concentration was unchanged, implying that the fall in mobility was probably caused by an increase in defects or impurities in the channel.

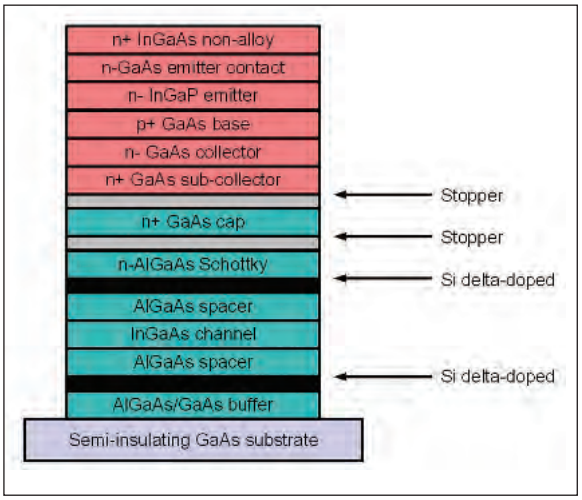


Figure 4. Engineers at Hitachi Cable studied a BiHEMT structure with silicon-doped layers

The engineer's next step was to determine whether pHEMT degradation was caused by HBT overgrowth in particularly, or just the thermal history associated with this growth. To answer this question, pHEMT epiwafers were heated under arsine for between 10 and 90 minutes at the temperature employed for HBT growth. Measurements of carrier mobilities and doping profiles revealed a shocking result: Even though the HBT is grown at a lower temperature than the pHEMT, growth at this temperature can still impact the location of carriers, leading to a broadening of the carrier concentration profile and a reduction in carrier mobility in the channel.

To determine the origin of this carrier broadening, the engineers studied their samples by secondary ion mass spectroscopy (see figure 5). This revealed that indium, phosphor, and aluminum atoms were unaffected by heating. Silicon, however, an element renowned for its low thermal diffusion coefficient, spread out from the δ-doped layers and into the AlGaAs spacer layer and InGaAs channel, where it degraded carrier mobility.

Takeda and his co-workers offered two suggestions for improving δ-doped pHEMTs with a high silicon concentration : increase the spacer layer thickness between the channel and electron supply, which invokes the penalty of a cut in the transistor current; or turn to a uniformly doped electron supply layer.

Complex channels

More and more countries are developing III-V expertise, and this year a partnership between researchers from India Institute of Technology - Kharagpur and National Chiao Tung University, Taiwan, presented a paper on the development of an InAlAs/InGaAs HEMT with a novel composite channel. This transistor could be used to make a W-band power amplifier for radar applications.

The researchers aimed to improve HEMT performance by increasing indium content in the InGaAs channel, which

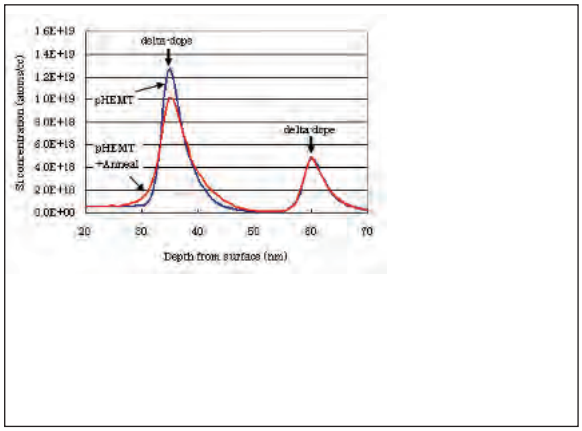


Figure 5. Annealing a pHEMT wafer under arsine at temperatures associated with HBT growth causes diffusion of the silicon dopant

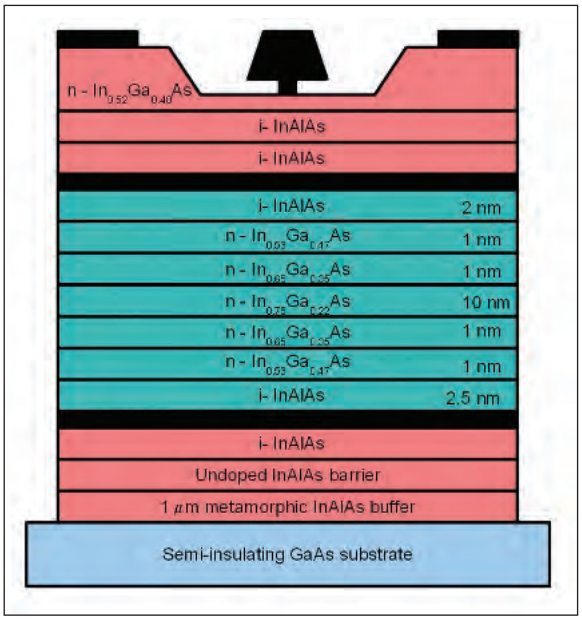


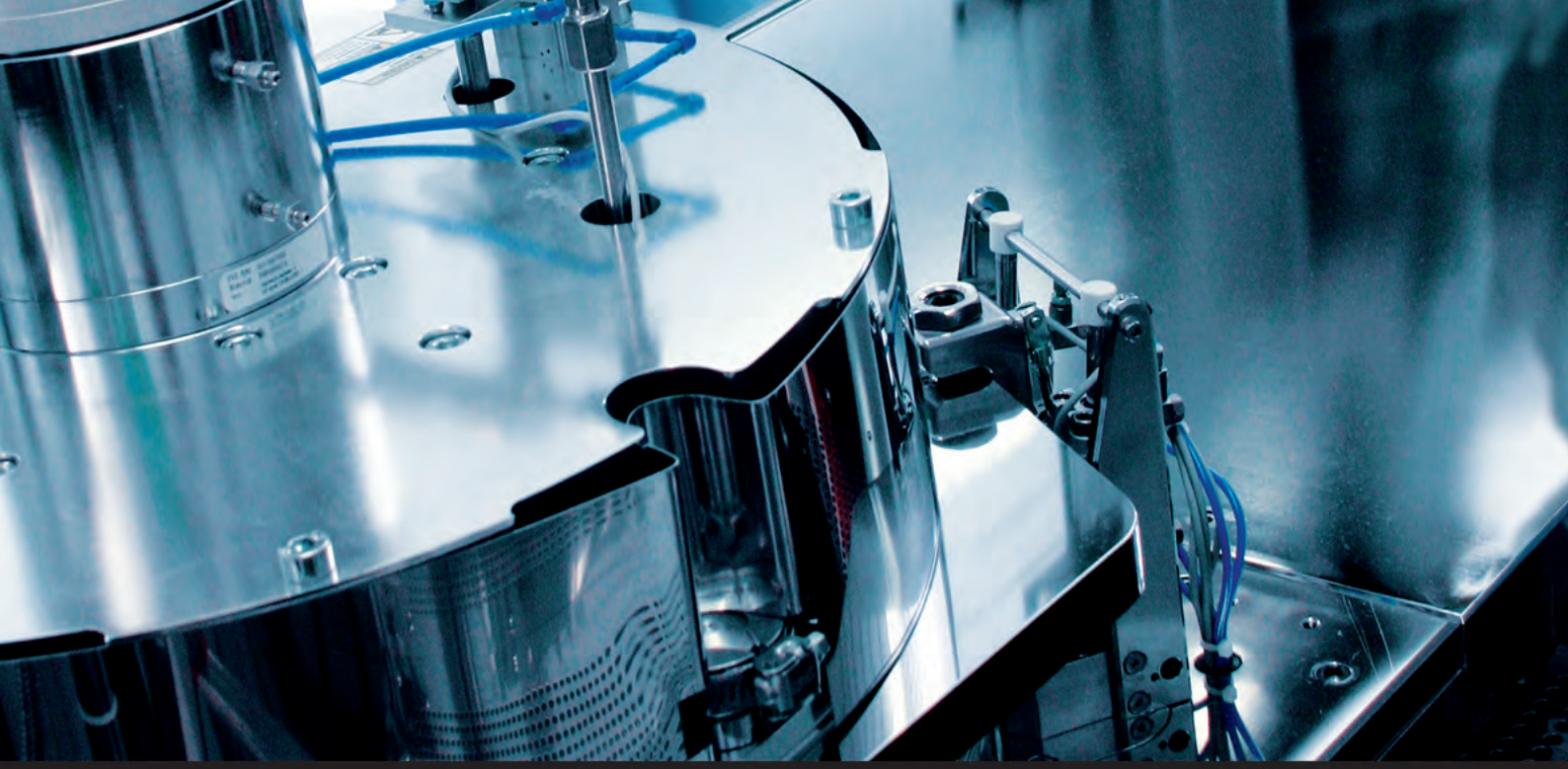
Figure 6. A partnership between researchers India Institute of Technology - Kharagpur and National Chiao Tung University, Taiwan has developed novel pHEMT architectures.

leads to several benefits. It deepens the quantum well, confining more carriers to the channel, it almost eliminates three-dimensional carrier movement, and it enhances mobility via a reduction in the electron's effective mass.

To realize a high-indium-content channel that is free from phase separation, the researchers developed transistors with penta-composite channels that featured graded layers with differing indium content. These structures accommodated lattice mismatch between the layers, and through optimization of indium fraction in the InGaAs layer, δ-doping and spacer thickness, they promise to deliver high currents with good linearity at high frequencies.

The engineers best results were realized with a HEMT featuring an $In_{0.78}Ga_{0.22}As$ channel and a total channel thickness of 14 nm (see Figure 6). This transistor had a drain current of 1029 mA/mm and a transconductance of 648 mS/mm. The device's cut-off frequency and maximum oscillation frequency were 125 GHz and 250 GHz, respectively, values that the team describes as "remarkable", given the gate length of 0.25 mm. This is much larger than that used by today's fastest transistors.

If the team goes down this scaling route and makes progress, then it may well be taking part at next year's CS-Mantech. If this meeting is anything like the last few years, there's bound to be a good number of GaAs related papers presented in Palm Springs, CA, in mid-May 2011.



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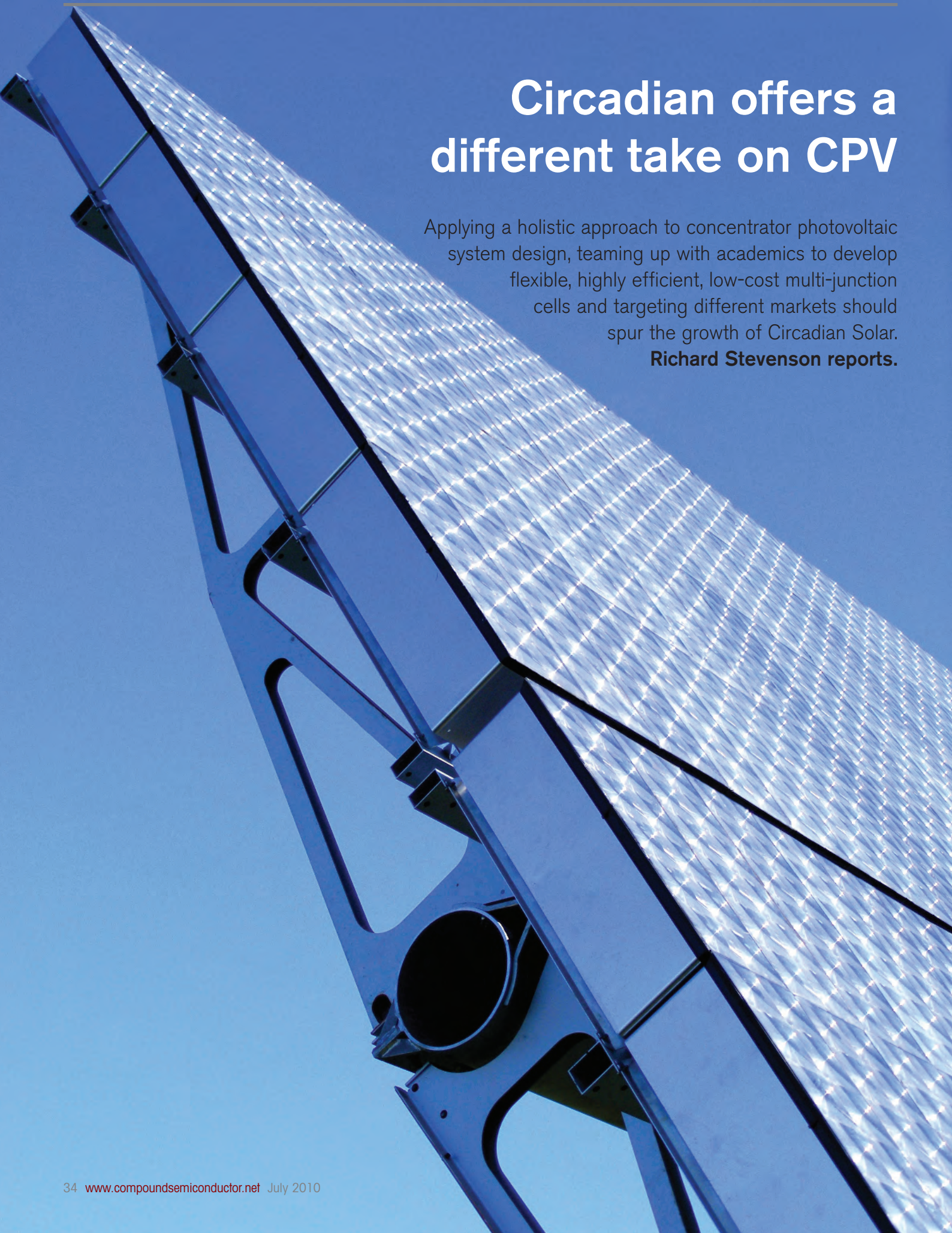

Circadian offers a different take on CPV

Applying a holistic approach to concentrator photovoltaic system design, teaming up with academics to develop flexible, highly efficient, low-cost multi-junction cells and targeting different markets should spur the growth of Circadian Solar. **Richard Stevenson reports.**

Many of the world's hottest regions are so sparsely populated that they are not connected to the electrical grid. Those that live there rely on diesel generators to produce the power that they need for running the local schools, hospitals, mines, water works and so on. But this form of electricity generation is far from ideal: It is expensive; noisy; it leaves a high carbon footprint; and day-in, day-out power generation demands regular fuel deliveries.

Turning to renewable sources can address all of these issues. One option is concentrator solar thermal, which uses the sun's energy to convert water, directly or indirectly, to steam that drives turbines and generates electricity. This obviously works well in these sunny climes, but large volumes of cooling water are required. That's not good, because these locations often have very little rainfall and water is a cherished commodity that needs to be used wisely.

A far better technology for taking advantage of strong, plentiful sunshine is concentrator photovoltaics (CPV). With this approach electricity is generated by tracking the position of the sun across the sky and focusing its rays by a factor of several hundred onto triple-junction solar cells.

One company that is hoping to tap into this potentially lucrative opportunity for CPV over the next few years - and then concurrently start competing for contracts for solar farms when it has cut the cost-per-Watt of its systems through economies of scale - is a little-known UK start-up Circadian Solar.

This University of Warwick spin-off claims that it will be able to manufacture systems delivering world-class performance at very competitive prices, due to its holistic approach to system design. And it aims to eventually get the upper hand over its rivals by exploiting its stake in the development of new processes for multi-junction solar cells that promise to slash production costs through multiple re-use of substrates.

Circadian is led by Jeroen Haberland, former CEO of the thin-film photovoltaic manufacturer Johanna Solar Technology, which was recently acquired by Robert Bosch. When Haberland left this producer of solar cells based on copper, indium, gallium, sulfur and selenium, he wanted to work with a new, emerging photovoltaic technology, and opted for CPV, due to its relative maturity. He joined the team on 1 March 2010; an appointment aimed at taking Circadian on from a university spin-off to a manufacturer of solar systems.

Haberland says that the skill set needed for this transition is different from that needed to build up a spin-off. "That's where I come into the game. Johanna Solar, my last company, was the third high-tech company that I built up." Haberland's strengths include building up companies; setting up structures and processes; securing funding; finding the right location for manufacturing; and bringing products to market.

A holistic approach

According to Haberland, one of Circadian's key advantages over its rivals is its holistic system design that leads to very high efficiencies.

"Overall efficiency depends on a lot of things. But it starts with the alignment of components to have an optimum focus of the sunlight on the cell."

Haberland claims that many CPV system manufacturers buy components "off the shelf", and this makes it far harder to bring the components into optimum optical alignment. "The accuracy of the tracker movement is very important, and it's one of the factors that we have spent a lot of engineering on."

Fluctuations in the strength and direction of the wind can also reap havoc on system performance. To address this, Circadian employs a robust tracker design and a high quality gearbox capable of very accurate tracking – its accuracy is better than 0.4 degrees.

The company's CPV system uses two optical elements for focusing sunlight by a factor of more than 600 onto triple-junction solar cells: a Fresnel lens made from PMMA, which also provides some protection to the cell from the weather; and a second element that is positioned very close to the photovoltaic device. Combining these two makes tight focusing more tolerant to any deviations from perfect optical alignment.

The choice of which type of optical system to use to focus the sun's rays is controversial. Some system makers, such as SolFocus and GreenVolts, are using mirrors rather than lenses. Circadian says that this alternative approach is inferior, because less light hits the cell, a weakness that is compounded if a plate is added on top of the mirror to protect the cell from the elements.

A choice of chips

Triple-junction cells are available from several manufacturers, and Circadian is comparing the performance of many of these in its CPV systems. Haberland knows which manufacturer is giving the best results, but he is not willing to name names. But he will say that there are differences in the performance of the cells produced by different chip manufacturers, which are magnified at the system level.

To begin with, Circadian will be placing orders with at least one of these chipmakers, but in the longer term it is

hoping to switch to a novel form of triple-junction cell. It has a major stake in research being carried out at Radboud University, Nijmegen, The Netherlands into the development of flexible, high-efficiency and lower-cost triple junction cells.

This effort focuses on the removal of triple junction cells from their substrates, which can then be re-used, leading to substantial cost savings. To separate the device from its substrate, a sacrificial AlAs layer is inserted beneath the solar stack and removed after growth by chemical etching. Before this processing step is applied, a 20 μm-thick copper layer is electroplated on top of the epitaxial structure to provide a highly conductive platform for the cells.

The researchers at the University of Radboud are making good progress, and can already produce cells on a 2-inch wafer. One of their next goals is to scale the process to 6-inch production. They might also look at the growth of inverted metamorphic structures, which are suited to this process and promise to enable improvements in cell conversion efficiencies of a few percent (see *Compound Semiconductor* October 2007, p.25).

Staying on track

Circadian has employed conventional triple-junction cells in its prototype tracker systems that feature a 30 m^2 array and are capable of generating about 7 kW. "The system efficiency is much more than 25 percent, which is a very good result," says Haberland.

One of these systems is located on the edge of the University of Warwick Science Park, just a few hundred yards from the company offices. Having this so close by is invaluable for learning about how the tracking system behaves under load. However, it is not possible to gauge how well this CPV system will work in sunny climes. That's because Coventry averages just over 4 hours of sunlight per day and has a mean maximum temperature over a year of less than 14 degrees C. In other words, it is rarely sunny, and even when the sun is out, it doesn't beat down.

So to address the lack of suitable performance data, the company has two further test systems overseas: one in Cyprus; and another at University of Lisbon, Portugal.

"These two test fields in the sun-belt, in combination with the test field here, is good for us in making the next development step," says Haberland.

The aim of the next step is to create the infrastructure for manufacturing, and prepare for the commercial launch of CPV systems. These will be assembled on site, using components manufactured by third parties to specifications set out by Circadian.

Up until recently, nearly all of the biggest deployments of CPV were at testing grounds, but genuine customer orders are just starting to trickle through. "There are signs that things are changing, and that's good for us."

One example of this change is the recent signing of a contract between Concentrix Solar and Chevron Technology Ventures for the deployment of a 1 MW power plant at a Chevron Mining facility in Questa, NM. And another positive sign is the recent completion of a solar power plant of that size built by SolFocus, which is providing clean power to Victor Valley College in Victorville, California.

Over the next year or so Circadian will focus on finding new premises, scaling up its manufacturing, and getting ready for market entry. Once that's done, it should start to win orders in what should be a growing market for CPV.

"What we see – a rough estimate of course, because markets are difficult to forecast – is that in 2020 there will be about 20 GW of CPV installations in total, for both off-grid and on-grid applications," says Haberland.

If Circadian Solar can tap into just a fraction of that business, then it should have a good future ahead of it.

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- Senior research scientist/head of MBE Research Group/ Associate professor at Max Planck Institute for Solid State Research in Stuttgart for 17 years.
- University professor of Materials Science at Darmstadt University of Technology
- Director of Paul Drude Institute for Solid State Electronics in Berlin
- University Professor at Physics Department of Humboldt University Berlin

Visiting research professor at:

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- Tokyo Institute of Technology, Tokyo
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LED droop: do defects play a major role?

Theorists are proposing that density activated defect recombination (DADR) can account for droop, the decline in a nitride LED's external quantum efficiency at high drive currents.

The team from the University of Arizona, AZ, and the Phillips University of Marburg, Germany, reached this conclusion after modeling the recombination efficiency in the active region of light-emitting structures at various current densities. They found that the behavior of their model - which featured monolayer thickness variations, defects and compositional fluctuations - could fit efficiency vs current curves from real nitride devices emitting at 410 nm and 530 nm.

The origin of LED droop is highly controversial, and there have been claims led by engineers at Philips Lumileds and backed up by computational scientists at the University of California, Santa Barbara, that Auger recombination is to blame.

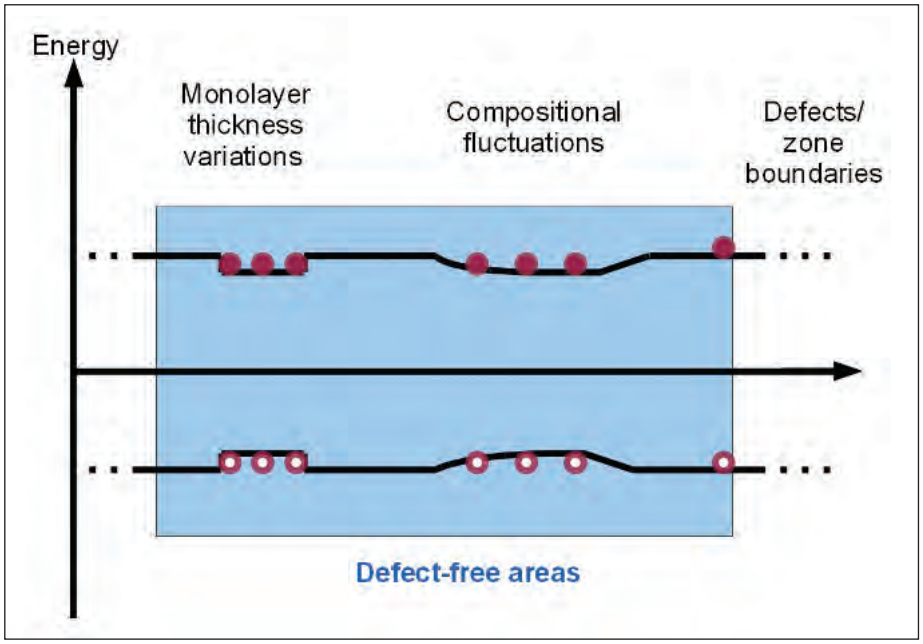
However, state of the art theoretical calculations by this US-German partnership suggest that Auger recombination rates in the nitrides are too small to explain the droop. And interband Auger recombination cannot account for droop either, according to this team, because it would require the energy separation between the higher and lower bulk bands to be very close to the fundamental band gap, which is generally not the case.

The members of the team at the Phillips University of Marburg are also considering whether phonon-assisted Auger recombination could account for droop.

"These calculations are numerically very intensive and the results depend far more critically on details of the used model and material parameters than for the usual direct Auger processes," explains Joerg Hader from the University of Arizona, who is the lead author on the paper.

He says that the initial results suggest that phonon-assisted Auger recombination rates are too low to account for LED droop.

Hader and his co-workers put forward DADR as a possible cause of LED droop after constructing a model where electrons and holes occupy states in local in-plane potential minima at low pump currents. These minima can be caused by fluctuations in either the composition of the well, or its width (see figure).



The researchers from the University of Arizona and the University of Marburg have modeled the radiative recombination in an InGaN active region featuring monolayer thickness variations and compositional fluctuations. As the current increases, carriers leave these potential minima and some end up at non-radiative recombination centers. That accounts for the decline in LED output at higher current densities.

As the current is cranked up, carriers leave these local minima that are relatively free of defects. Some then reach non-radiative recombination centers, which prevent them from playing a role in light generation. This carrier capture explains the decline in light output at higher drive currents.

The team has shown that its DADR model, which assumes Auger recombination can be completely neglected, provides a good fit to experimental internal efficiency data for nitride active regions emitting at 410 nm and 530 nm.

To realize a good fit, the majority of carriers have to be located at energies less than 100 meV from the minimum. This implies fluctuations in the indium composition of 2 to 3 percent, which is entirely feasible.

One of the striking characteristics of LED droop is that it is more pronounced at longer wavelengths. Hader says that this trend is compatible with the researchers' model.

"Longer wavelengths require deeper wells and therefore higher indium content in the wells," explains Hader. "This should lead to stronger disorder, more carrier localization and more defects – the basic ingredients for the DADR model."

One of Hader's next goals is to finish a wide-bandgap version of the simulation software package, SimuLase, which is being developed by the company he spends some time working for, Nonlinear Control Strategies. "It will contain the DADR-model as one of its tools."

He and his co-workers would also like to develop a better understanding of the general tendencies of both DADR and droop, such as their temperature dependence. To do this, the researchers need to develop a hopping-type model.

Hader et al. Appl. Phys. Lett. ***96*** *221106 (2010)*

Osram's powerful green laser questions the benefits of semi-polar growth

Engineers at Osram Opto-Semiconductors have broken the CW output power record for a true green laser with a polar device delivering 50 mW. Their 524 nm green emitter meets the specs for laser pico projectors, which need a 50 mW source emitting between 515 nm and 535 nm to deliver 10 lm of light on a screen.

The German outfit has also fabricated broad-area test lasers, which have been driven in pulsed-mode and emit at 531.7 nm.

These results, which follow on from Osram's report in January of a 516 nm laser emitting 50 mW, question the benefits of fabricating lasers on the semi-polar plane.

Back in summer 2009, when Sumitomo reported a 531 nm pulsed laser and 520 nm CW variant on the $(20\bar{2}1)$ plane, it appeared that by far the best way to reach longer wavelengths was to start with a semi-polar nitride plane that reduced the internal electric fields within the device. Researchers at Osram, however, argue that the key to making a green laser is the growth of a high-quality, indium-rich InGaN active layer.

Understandably, they don't say exactly how they do this. However, they do reveal that they were able to produce longer wavelength lasers by improving epitaxial design and material quality.

Their paper also details the results of calculations that compare the emission wavelength of polar and non-polar quantum wells with indium compositions of 26 to 36 percent and widths of 2.5 nm and 3 nm.

These calculations show that the differences in internal electric field strengths of the two classes of laser mean that a non-polar variant needs an indium content 3-4 percent higher than its polar equivalent if it is to emit at the same wavelength.

Another insight provided by the calculations is the effect of widening the quantum well: Increasing this from 2.5 nm to 3 nm red-shifts emission by more than 10 nm, according to Osram's calculations.

The engineers used MOCVD to produce laser structures featuring AlGaN cladding layers.

A ridge waveguide structure was employed in the 524 nm laser. This has a threshold current of 97 mA and a slope efficiency of 330 mW/A. At an output of 50 mW the wall plug efficiency was 2.3 percent.

Emission at 531.7 nm was realized with the broad area test structures with a laser threshold of 18 kA/cm^2. This was driven with 0.4 μs pulses at a duty cycle of 6 percent.

A. Avramescu *et. al.* Appl. Phys. Express **3** 061003 (2010)

SET makes brighter ultraviolet chips

A US collaboration led by Sensors Electronic Technology (SET) claims to have raised the bar for power output from a single ultraviolet LED chip. The team, which includes researchers from Rensselaer Polytechnic Institute and the US Army Research Laboratory, has produced a 273 nm chip emitting 30 mW, and a 247 nm version delivering 6 mW.

SET's president, Remis Gaska, says that the longer wavelength chip could be used for water sterilization and disinfection. Higher output powers enable an increase in water flow rate, and could lead to a cut in the cost of treatment per liter.

"Although DNA absorption peaks at 265-268 nm, the combination of DNA absorption and wavelength-dependent UV light attenuation in the water shifts the maximum germicidal efficiency to 270-275 nm," says Gaska. His 273 nm chip is in the center of this range.

The shorter wavelength, 247 nm LED is a promising source for water treatment and it could be combined with hydrogen peroxide for chemical decontamination.

The US team realized record output powers from its UV LED chips by reducing built-in strain, improving n-type and p-type doping, and minimizing dislocations and point defects. Thanks to these advancements, the researchers could increase the area of their chips without sacrificing quantum efficiency at low current densities.

Epitaxial structures were produced on sapphire via a combination of MOCVD and migration-enhanced MOCVD, and processed into devices with junction areas of 0.5 mm^2 and 1 mm^2.

LED chips emitting at 273 nm that have a junction area of 1 mm^2 showed an increase in external quantum efficiency as the drive current ramped to several hundred milliamps. At 700 mA, the CW output was limited by the heat dissipation from the junction of the TO-3 package. 247 nm LEDs with a chip area of 0.5 mm^2 produced a peak CW output of 6 mW at 275 mA.

The researchers have also studied the reliability of their LEDs. The output power of a 273 nm , 0.5 mm^2 chip driven at 400 mA (400 μs pulses, 10 percent duty cycle) halved after about 5000 hours of operation. Device degradation was caused by a change in the electrical properties of the p-type layers, which hampered electrical injection, leading to a cut in output power.

M. Shatalov *et al.* Appl. Phys. Express **3** 062101 (2010)

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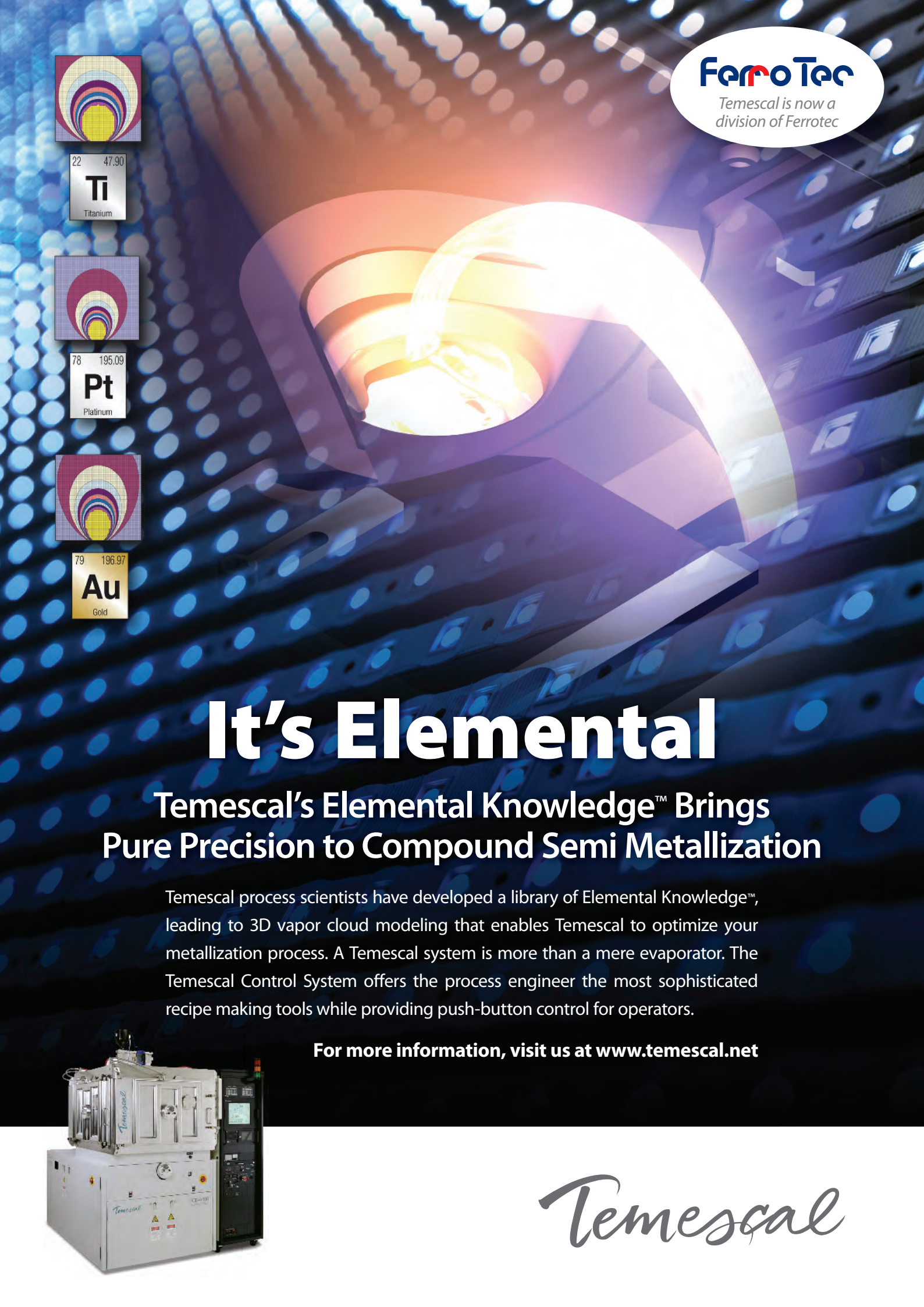

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