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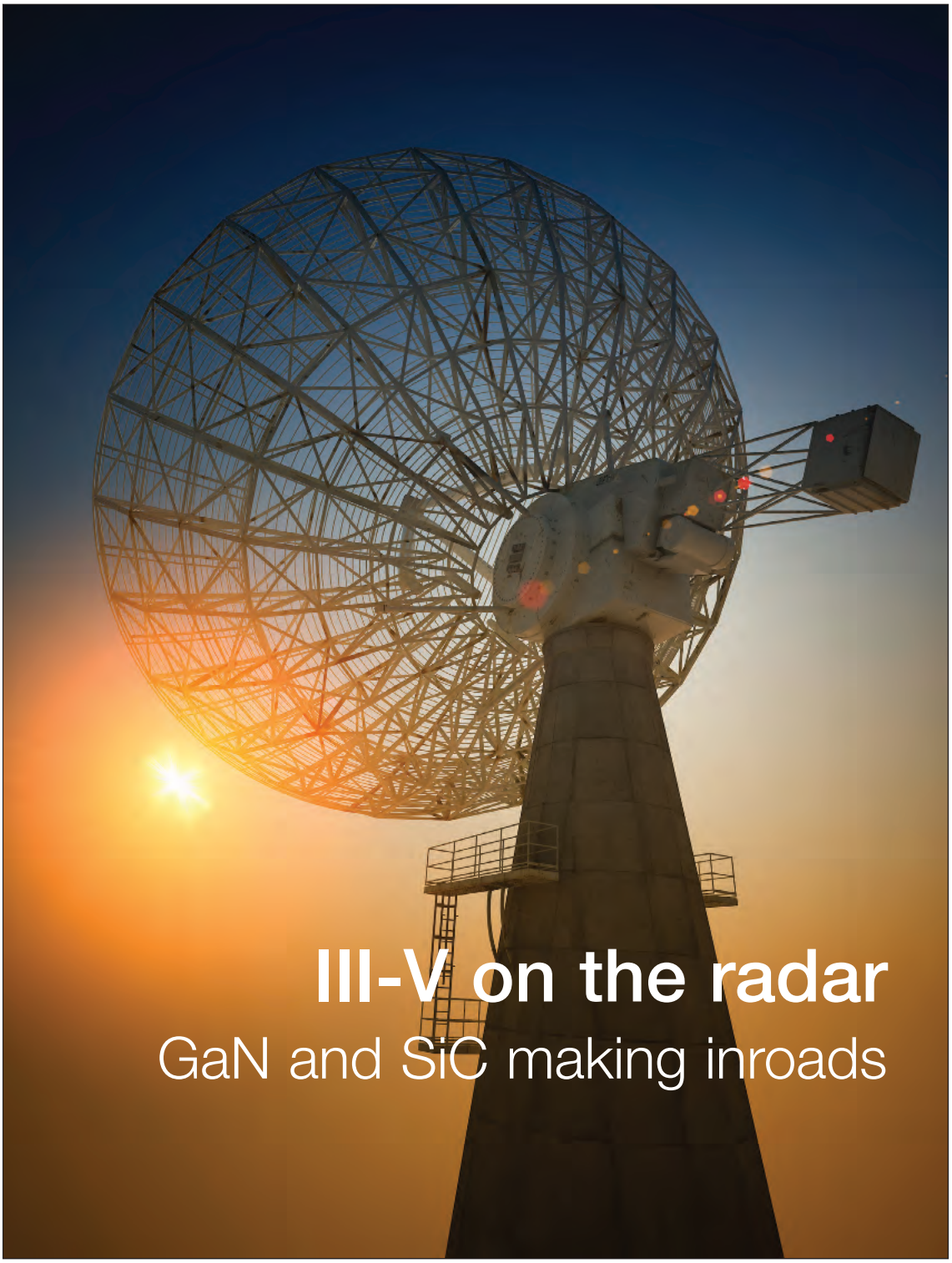

III-V on the radar

GaN and SiC making inroads

An Angel Business Communications publication

August / September 2010 Volume 16 Number 6

ALWAYS ONE STEP AHEAD

HIGHER PRODUCTIVITY // With almost 30 years of experience AIXTRON stands for proven engineering power and dedicated customer support: Our equipment serves a diverse range of customers to manufacture highest LED volumes at lowest cost.

BETTER PERFORMANCE // As the driving force in deposition equipment AIXTRON engineers powerful technology solutions: Our equipment is the best choice available to manufacture the brightest and most efficient LEDs.

SMARTER RESOURCES // AIXTRON's intelligent equipment concept enables optimized use of resources: The results are extremely low consumption of consumables, minimized maintenance requirements and optimized utilization of human resources.

AIXTRON started in 1983 and is today a leading provider of deposition equipment to the semiconductor industry. With our advanced solutions customers worldwide build components for electronic as well as opto-electronic applications. As pacemaker in our line of industry we are keeping always one step ahead.

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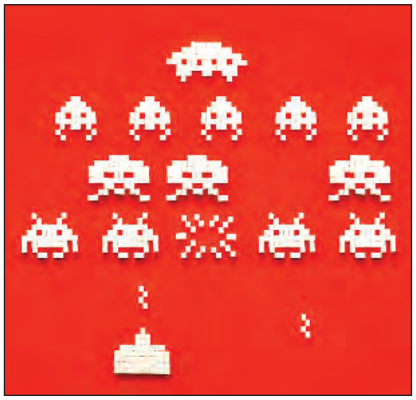
Watch out: silicon chipmakers are invading!

GaN is an undoubtedly a great material. Devices sporting this semiconductor can handle extreme temperatures with aplomb while delivering incredibly high power densities at outstanding efficiencies.

So it's not surprising that several companies have launched electronic devices built with this wonder material over the last few years. Products have been released by firms founded solely to exploit the benefits of GaN, such as Nitronex; experts in GaAs microelectronics, such as TriQuint and RFMD, that have extended their product portfolios to encompass this material; and companies such as Cree, which has broadened GaN coverage into the RF domain. These companies don't have this market all to themselves, however. The virtues of GaN are also attracting the attention of silicon chipmakers that want their cut, including International Rectifier (IR) and Integra Technologies, two companies featured in this issue.



IR, a company with almost 6000 employees and annual sales touching a billion dollars a year, launched its first GaN power devices this February. This firm's tremendous financial clout has enabled it to develop a full production process in-house, including growth of GaN on silicon. Realizing high quality material on this platform is certainly not easy, due to the large differences in lattice constant and thermal expansion of these two materials, and if the process is not optimal strain and cracking result.

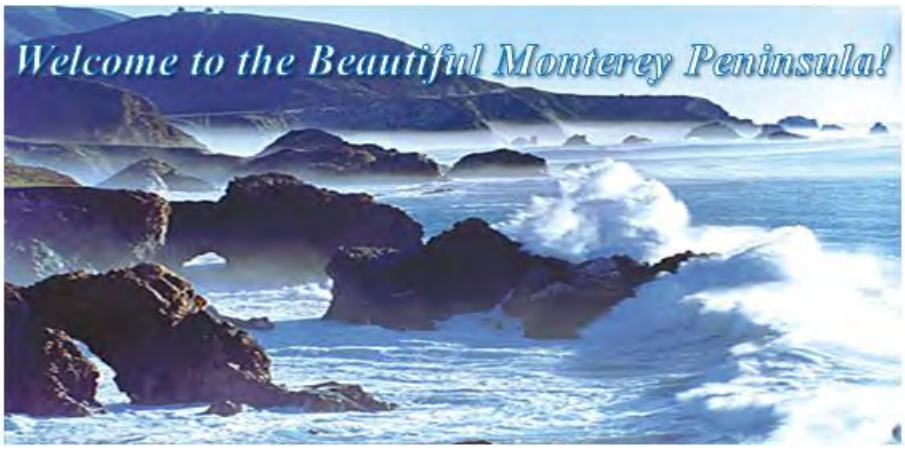
The challenge gets even tougher as the substrates get bigger. But so does the prize: A slash in manufacturing costs, particularly if these wafers can be processed on lines that were once used to churn out silicon chips.

IR has executed on these fronts, honing a 150 mm GaN-on-silicon process that delivers a high yield of rugged devices with incredibly low leakage currents.

The other interloper featured in this issue, Integra, is a much small firm that has chosen a different route for getting its first GaN products to market. This manufacturer of pulsed S-band transistors, which imports 100 mm GaN-on-silicon epiwafers from a Japanese supplier and processes them through its own line, released its first HEMTs at this summer's MTT-S show. Although these chips are off the pace in the key metric of power density, the company claims that it will catch up fast, implementing relatively straightforward changes to its process, such as cutting gate length.

IR and Integra have given many III-V chipmakers a head start in exploiting GaN in RF and power devices, but the gap may not last that long. To watch the race unfold, stay tuned to *Compound Semiconductor*.

Richard Stevenson PhD
Consultant Editor



The 2010 IEEE Compound Semiconductor IC Symposium

We cordially invite you to the 2010 IEEE Compound Semiconductor IC Symposium (CSICS) being held October 3– 6th in beautiful Monterey, California. Over the last 32 years the Symposium has been and continues to be the preeminent international forum in which advances in semiconductor circuit and device technology are presented, debated, and discussed. The scope of the Symposium encompasses devices and circuits in GaAs, SiGe, InP, GaN, and InSb as well as RF/mm-wave and high-speed digital CMOS to provide a truly comprehensive conference. This is the ideal forum for presentation of the latest results in microwave/mm-wave, high-speed digital, analog, mixed mode, and optoelectronic integrated circuits.

The 2010 CSIC Symposium is comprised of a full 3-day technical program, 2 short courses, a primer course, and a technology exhibition. The technical program consists of approximately 60 high quality state-of-the-art technical papers, 4 panel sessions, and an Industry Exhibit. The short courses, which run in parallel on Sunday, October 3, are titled "High Performance Linear Transceiver MMIC Design" and "High-Speed and mm-wave Digital-Rich Transceiver Design" and provide the attendees with a unique chance to learn from ten world-renowned instructors in their respective areas of expertise. The Symposium will also be offering the popular annual introductory level primer course on "Basics of Compound Semiconductor ICs." This year the Symposium will feature approximately 15 invited papers on a wide range of important topics encompassing device engineering to circuit application using advanced compound and other related semiconductor technologies. In addition, the Symposium will continue the tradition of including important "late breaking news" papers.

The technology exhibition will be held on Monday and Tuesday. The exhibition will feature informative and interesting displays with corporate representatives on hand. The list of exhibitors can be found in the CSICS advance program which will be published and distributed in late June.

To complement the Symposium, there are several social events which include the Sunday Evening CSICS Opening Reception, the Monday CSICS Exhibition Opening Reception, the CSICS Tuesday evening theme party, and the CSICS Exhibition Luncheon on Tuesday. Breakfasts and coffee breaks will also be served on Monday, Tuesday, and Wednesday.

The Symposium will be held at the Portola Hotel located in downtown Monterey. Situated 115 miles south of San Francisco and 350 miles north of Los Angeles, Monterey features a stunning waterfront, a lush urban forest, a rich array of historic and cultural resources, museums, gardens, recreational activities and a wide variety of special events scheduled throughout the year. Monterey is the home of the world-class Monterey Bay Aquarium located on the street immortalized in John Steinbeck's novel Cannery Row. Monterey's rich history includes Spanish exploration dating back to 1542, and the establishment of the San Carlos Cathedral by Father Junipero Serra in 1770. It was the site of Alta California's capital under Spain and later Mexico, and the place where California statehood began in 1849.

For registration and further information please visit the CSICS website at http://www.csics.org. Further questions may be addressed to the Symposium Chair: Dave Halchin, Ph:1-336-678-8123 Email: dhalchin@rfmd.com

We hope you can attend,

2010 IEEE CSICS Organizing Committee

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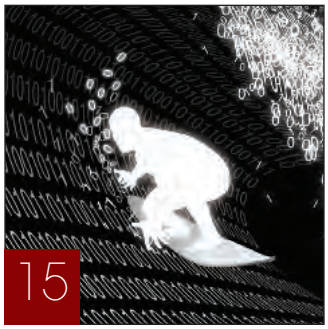
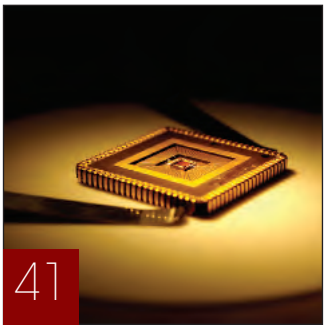
industry & technology





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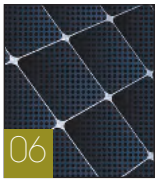
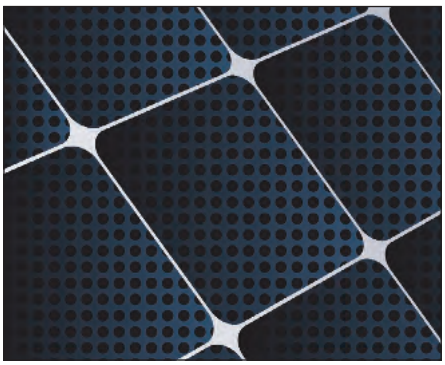


AQT Solar Compact CIGS Plant Could Supply 60MW of Energy

AQT Solar, a developer of CIGS (copper-indium-gallium-diselenide) thin-film solar cells has opened a new fully operational facility in Sunnyvale, California. The facility has already begun production to fill current customer orders of 20 MW, with substantial purchase orders in the pipeline. AQT also released the name of its first customer installation, Sol Pacifico, a large property development, which has ordered 2 MW of energy to power its gated community in Baja Mexico, on the Pacific coast.



AQT's claims its rapid path from inception to production in two years is unprecedented in the solar industry, and illustrates how its technology and business model, dubbed CIGS 2.0, are charting new territory in the market. AQT's new facility, fuelled by a recent $10 million round of funding, currently houses a 15 MW manufacturing line, and can easily scale up to 60 MW of production capacity. The manufacturing line's design allowed for quick on-site deployment and is a result of the company's partnership with Intevac, a leader in high-productivity manufacturing equipment.

The preparation, build-out, line implementation and qualification, and production initiation was completed for the Sunnyvale location in less than eight weeks. The small footprint of each highly-automated machine provides an efficient use of space within the 20,000 square foot facility. As a result, AQT can produce up to 60 MW in an area many times smaller than competitors.

"Starting commercial production so early in our company's lifecycle is a confirmation of our business model, the leverage we receive from world class partners like Intevac and our breakthrough CIGS production process," said Michael Bartholomeusz, CEO of AQT. "We have set aggressive production goals for the remainder of 2010 and beyond and are excited to kick it off in California, the heart of the solar industry."

AQT's first installation, Sol Pacifico, is scheduled to break ground in 2011. The 2 MW project, which will potentially grow to 9 MW, will support a large high-end resort development in Baja Mexico.

Skyworks Maintains Power Amp Share Lead Image suggest

THE Strategy Analytics RF & Wireless Component market research service has explored changes in the handset and cellular device power amplifier (PA) market brought about by the economic slowdown and contraction in cellphone shipments. Its report "Skyworks Maintains Power Amp Share Lead," analyzes the effect changes will have on PA suppliers. The rapid resurgence in handset production pushed the PA market to over $2.4 billion in 2009, driving the two largest suppliers, Skyworks and RFMD. Skyworks held its number one position, led by success in GSM / GPRS / EDGE, while RFMD remained the leading supplier of W-CDMA PAs.

"It is gratifying to see last year's prediction play out as the acquisition of CMOS PA supplier Axiom Micro Devices helped Skyworks maintain share in the recession-resistant low-cost segment of the market," commented Christopher Taylor, Director of the RF and Wireless Components service. "At the same time, demand for ultra low-cost and grey market GPRS handsets expanded rapidly, helping all vendors, but particularly boosting RDA Micro out of obscurity."

Femtocell Revenue to Reach $4 Billion

IN a newly released report by Dell'Oro Group, femtocell market revenues are forecast to reach $4 billion in 2014. Femtocell devices are used to improve mobile network coverage in small areas and connect locally to mobile phones and similar devices.

Dell'Oro Group 'Femtocell 5-Year Forecast Report' offers a complete overview of the Femtocell industry, with regional tables containing manufacturers' revenue, average selling prices, and unit shipments covering the CDMA, WCDMA, and LTE femtocell markets.

"Although we are in the very early stages of commercial femtocells deployments, we expect to see a significant increase in commercial deployments in 2011, and an inflection point in the market in 2012," stated Loren Shalinsky, Senior Analyst at Dell'Oro Group.

"There are 14 commercial deployments around the world, with many more operators in the process of trialing femtocells service. The majority of these trials are expected to turn into commercial deployments in 2012. While only one million units are expected to ship this year, we forecast unit shipments will reach 62 million in 2014, with more than 80 % of those total units being WCDMA femtocells," continued Shalinsky.

New EU Project Focuses on Reducing Power Of Telecom & Data Networks

A EUROPE-WIDE consortium has taken up power consumption of telecommunications and data networks, which are estimated to consume as much as 3% of European electricity. Five partner organisations have come together in the BIANCHO project (BIsmide And Nitride Components for High temperature Operation).

The project will develop materials to allow lasers and other photonic components to become more energy efficient and also more tolerant of high operating temperatures. This power reduction is vital as optical communication systems are becoming the principal way to deliver ever-increasing data-rich broadband services to homes and businesses.

Many photonic components have major intrinsic losses, with around 80% of the electrical power used by a laser chip emitted as heat. The presence of this waste heat necessitates the use of thermo-electric coolers and an air-conditioned environment in order to control the device temperature, cascading the energy requirements by more than an order of magnitude.

The energy losses are mainly due to a process known as Auger recombination, a consequence of the band structure of the semiconductor materials used in making components such as semiconductor lasers and optical amplifiers. Over many years, incremental approaches have sought to reduce the consequent inefficiencies without addressing their fundamental cause. BIANCHO proposes a radical change of approach: to eliminate Auger recombination by manipulating the electronic band structure of the semiconductor materials through the use of novel dilute bismide and dilute nitride alloys of Gallium Arsenide (GaAs) and Indium Phosphide (InP). This will allow the creation of more efficient and temperature tolerant photonic devices which could operate without the power-hungry cooling equipment that today's networks demand. The project brings together five leading European partners with complementary expertise in epitaxy, structural characterization of materials, device physics, band structure modeling, advanced device fabrication, packaging and commercialization.

Coordinated by the Tyndall National Institute (Ireland), the other academic partners are Philipps Universitaet Marburg (Germany) focusing on material growth and characterization; Semiconductor Research Institute (Lithuania) responsible for the design, manufacture and characterization of bismide-based epitaxial structures; the University of Surrey (UK) who contribute unique characterization facilities and modeling expertise. Commercialization of the project results will be led by CIP Technologies (UK) an organization with a long history of applied photonics innovation, particularly in the telecommunications sector.

4 MW Worth of CPV Technology to 'The Solar Zone'

ARIZONA Corporation Commission (ACC) has confirmed that in less than a year, The Solar Zone at the University of Arizona Science & Technology Park (UA Tech Park) has moved from an on-paper concept to a bustling, solar-centric business zone that is advancing solar energy innovation and production.

The Solar Zone is the intended site of four of the 10 new solar power developed through contracts with Tucson Electric Power (TEP) that were endorsed on Tuesday by the ACC. The new projects will combine with two previously announced systems to expand the Solar Zone's generating capacity to nearly 20 MW. Together, the systems will generate enough clean energy to power more than 4,600 Tucson homes annually. The four new tenants join Bell IPC. Site preparation and construction, valued at about $2 million, begins in September 2010.

The new projects will include contributions from Albuquerque based Emcore and Californian company Amonix Solar. Emcore provides compound semiconductor-based components and subsystems for the fiber optics and solar power markets. The firm plans a 2MW Concentrated Photovoltaic (CPV) system in the Solar Zone. Amonix designs and manufactures utility-scale concentrating solar (CPV) systems. The company will build a 2 MW concentrating solar (CPV) system project in the Solar Zone.

The Solar Zone will provide TEP with an opportunity to evaluate different types of systems, including a 5 MW CPV thermal power plant being built by Bell Independent Power Corporation, under a previously approved contract with the utility. TEP also will own and operate a 1.6 MW single axis tracking PV array being developed at the Solar Zone this year by Solon.

"We'll be able to track how these technologies perform side by side, under identical operating conditions, to determine which systems work best for our company and our customers," said Paul Bonavia, Chairman, President and CEO of TEP and parent company, UniSource Energy.

"With five new solar projects locating here establishes The Solar Zone at the UA Tech Park as the largest demonstration site in the nation," said Bruce Wright, UA's Associate VP for University Research Parks.

"We are pleased that our project was selected for the Solar Zone by Tucson Electric Power," said Amy LeGere, Foresight Solar Director of Development. "With 350 days of Tucson sun this is an optimal setting for solar energy generation. We commend the UA Tech Park for its leadership in helping Arizona become a global leader in the renewable energy sector."

Elec-Tech Chooses Veeco As Primary Provider of 130 MOCVD Tools

VEECO INSTRUMENTS has reported that Elec-Tech International has selected its TurboDisc K465i Metal Organic Chemical Vapor Deposition (MOCVD) systems as its "tool of choice" for two new LED factories in Wuhu and Yangzhou, China.

In August Veeco booked the initial systems from a large multi-tool purchase order from Elec-Tech's LED subsidiary, Elec-Tech Optoelectronic Technology (Wuhu). Elec-Tech International is a Shenzhen-listed electronics company that has signed a joint venture cooperative agreement with South Korean firm EpiValley to jointly develop the Chinese LED market.

Tony Wang, Chairman of Elec-Tech commented, "Our Board of Directors has approved our plan to purchase 130 MOCVD tools to ramp production capacity at our two LED factories. Our goal is to

become one of the top three LED companies by output and sales revenue in China within two years, focusing primarily on the general lighting and BLU market, but on other applications as well."

Wang continued, "After a thorough evaluation of the available MOCVD products, we selected Veeco as our preferred and primary supplier for the vast majority of the 130 MOCVD systems we will be installing at our new factories. We believe that Veeco's MOCVD systems have low cost-of-ownership and proven high productivity, and will help us to achieve success in the LED market."

Bill Miller, Executive VP and General Manager of Veeco's MOCVD Operations, commented, "We are extremely pleased that Elec-Tech has chosen Veeco for their production requirements as they build out their aggressive plans in China. We look forward to supporting this important new customer with our best-in-class systems and world-class applications process support."

Crystal IS and Asahi Kasei Sign JV To Manufacture AlN Substrates

CRYSTAL IS, a developer of ultraviolet light emitting diodes (UVC LEDs), and Asahi Kasei Corporation, the parent company of one of Japan's major diversified industrial groups, have signed a joint development agreement.

Under the agreement the two companies will create a manufacturing process for large diameter aluminum nitride (AlN) substrates based on Crystal IS proprietary intellectual property. "After a comprehensive study, we found Crystal IS wafer technology the most advanced and suitable for commercialization"

"Aluminum nitride substrates are a critical component in the fabrication of UVC LEDs for energy efficient water and air sterilization applications," said Steven Berger CEO of Crystal IS. "Building on our intellectual property to develop manufacturable large diameter substrates is an important step towards high-volume production and long term growth."

The development will take place at the Crystal IS facility in Green Island, NY and the program will run in parallel with the company's UVC LED activities.

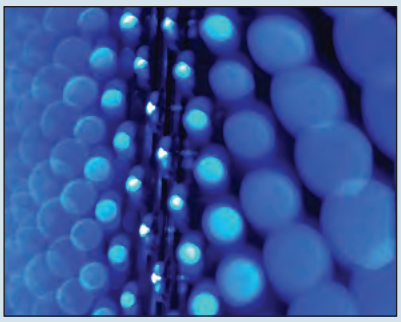
"After a comprehensive study, we found Crystal IS wafer technology the most advanced and suitable for commercialization," said Masafumi Nakao, who heads Asahi Kasei's development of new business in compound semiconductors. "To reinforce our commitment to Crystal IS and the technology, we are happy to make a $2 million investment in the company as we assess the long-term market potential of these substrates for LEDs and a number of other high-power applications."

Crystal IS produces ultraviolet light emitting diodes (UVC LEDs) on Aluminum Nitride (AlN) substrates for the cost-effective production of long lasting, energy efficient, water and air purification devices.

Asahi Kasei is the holding company of the Asahi Kasei Group, one of Japan's largest diversified industrial enterprises. Its electronics business includes Asahi Kasei Microdevices Corporation, claimed to be one of the world's largest compound semiconductor manufacturers.

More light orders for AIXTRON

AIXTRON have announced a substantial multiple order for additional MOCVD tools from Yangzhou Longyao, a LED manufacturing company in Yangzhou, PR China. Yangzhou Longyao is a subsidiary of Rainbow Optoelectronics Material Shanghai Co. Ltd., China, a long time customer of AIXTRON MOCVD equipment.



The order for further CRIUS epitaxial growth reactors was placed at the end of 2009. The systems will be delivered in a 31x2-inch wafer configuration and commissioned at the company's modern facility in the course of the third and fourth quarters of 2010. AIXTRON has been chosen as supplier for Rainbow's large-scale plan to meet the challenges of improved LED performance via the ongoing project entitled 'Deo Light'.

Epistar & Oree Unite To Supply LEDs Worldwide

OREE, a developer of LED planar illumination technology, has secured an investment from Epistar Corporation, Taiwan's largest manufacturer of LED chips. The funding is a demonstration of the relationship between the two companies.

Oree has developed a differentiating technology that brings LED lighting to a new level of efficiency and practicality in terms of energy consumption and cost. Oree's solid-state light source is thin and flat and is ideally-suited for general lighting applications, decorative and architectural lighting, as well as backlighting for LCD panels. Oree is working with customers in Asia and Europe, and expects to begin high-volume production early next year.

As a chip supplier, Epistar Corporation is dedicated to partnering with companies that present novel and promising technologies. Epistar has been manufacturing chips for Oree since 2007, and this continued collaboration will strengthen market penetration in Asia, Europe and the US for both companies.

"Oree has introduced a game-changing LED technology and brought some great talent to the market," said BJ Lee, Chairman of Epistar Corporation.

"By investing in Oree, Epistar has confidence in the significant market potential of our technology," said Eran Fine, founder and CEO of Oree. "This funding will help us meet our high-volume production goals, as well as expand our global reach."

Established in 2006, Oree claims to have pioneered the LED planar light source and is a leading developer of LED planar lighting. Oree's technology addresses the needs of the lighting market, enabling thin and efficient illumination of large areas. Its patented technology allows general lighting and backlight manufacturers to significantly increase system efficiency and dramatically reduces the cost of LED-based systems. Epistar Corporation, headquartered in the Hsin-chu Science-based Industrial Park, focuses on developing, manufacturing and marketing high brightness Light Emitting Diode (LED) products.

Applying its own proprietary Metal Organic Vapor Phase Epitaxy (MOVPE) technology, Epistar has successfully commercialized the full spectrum range of high brightness LEDs with the characteristics of compact size, low power consumption and long operation life.

Cree provides factory light

THE LED lighting revolution achieved another victory with the opening of an industrial plant lit exclusively with LEDs. Located in Etten Leur, The Netherlands, the full-service consumer products packaging plant is owned and operated by Kompak. All interior and exterior lighting fixtures feature Cree XLamp LEDs and were developed and installed by LedNed, a Dutch LED lighting pioneer.

"In building this new packaging facility, Kompak's management wanted to demonstrate its commitment to the highest-quality production systems, while minimizing the plant's environmental impact," said André ten Bloemendal, commercial director, LedNed. "We are particularly proud of the warehouse lighting we developed for this project, Led Lightline, which provides uniform illumination over all horizontal and vertical surfaces, something that is incredibly important given Kompak's nearly 14 meter-high warehouse ceilings." Lightline features motion detection, daylight correction and other custom options to increase light availability in spaces where more light is required. Spanning 3,500 meters, Lightline is fully integrated into the plant's sprinkler system, doubling as emergency lighting should there be a power failure at the plant. Other LedNed products used include LedTube® tube lights in office areas, as well as FlexiLightPanel® LED panels and LedNed consumer bulbs throughout the facility.

According to Steven Nijweide, project manager at Kompak, the use of LED illumination throughout the plant has shown a 20,000-KWh reduction in electricity usage when compared to conventional lighting, translating into a nearly 135,000 kilogram annual carbon offset. In addition to the energy savings, the lighting has been configured to provide automatic, daylight-compensated, and optimal task illumination throughout the office and production areas.

Kompak's facilities are designed for a three-shift operation, making it imperative for the lighting fixtures to work with the building's automation systems. The LED-based luminaires have been easily integrated, creating responsive and functional lighting for employees whenever and wherever they are in the plant.

"Historically, high-bay illumination systems have been difficult to design and implement, given the lumen output required," said Paul Thieken, marketing director, Cree LED Components. "LedNed's Lightline fixtures, featuring Cree's powerful and bright XLamp XR-E and MC-E LEDs, are enabling the Kompak facility to take full advantage of the benefits of LED lighting."

Concentrix Solar Inaugurates First Power Facility in South Africa

PAVING the way for solar power projects in South Africa, Concentrix Solar, a supplier of CPV systems is going to inaugurate its first ever power facility in South Africa at the Aquila Private Game Reserve in Touwsrivier on September 1, 2010. The firm says this is the first major step in developing large-scale solar power projects in South Africa and subsequently the region.

CPV systems are perfectly suited for the use in South Africa with its energy shortage, water scarcity and high temperatures. Concentrix says its systems can be easily and quickly implemented and do not need cooling water or suffer from heat degradation at hot ambient temperatures.

Hansjörg Lerchenmüller, CEO of Concentrix Solar commented, "In addition, this facility will initiate the transfer of know-how and serves to develop local skills in South Africa with immediate effect."

Concentrix is planning to inaugurate a 60 kilowatts (kW) facility at the Aquila Private Game Reserve in Touwsrivier, Western Cape. With this installation, the Aquila Private Game Reserve is able to cover all energy requirements during daylight hours and makes a positive contribution to environmentally friendly tourism as well as improve energy access for the area.

Also, the firm is actively pursuing a project development of a 50 megawatts (MW) utility-scale power plant in the Western Cape. The company has been present in South Africa since 2008 and has the ability to develop large-scale solar projects and deliver turnkey solutions under local conditions utilizing local content.

Concentrix says that with a high amount of direct solar irradiation, South Africa is best suited for the use of its CPV technology, particularly due to its high efficiencies and two-axis tracking. Concentrix Solar is a supplier of concentrator photovoltaic equipment and turnkey power plants for sunny locations. The company was founded in February 2005 as a spin-off from the Fraunhofer Institute for Solar Energy Systems ISE. In December 2009, Concentrix Solar became a division of the Soitec Group.

Bergen University Chooses Plasma-Therm's 790+ for Nano-fabrication Facility

THE University of Bergen's system addition to their facility will assist in the development of free-standing Fresnel zoneplates for neutral helium microscopes.

The 790+ RIE equipment will also support the universities work on biophysics experiments in surface engineering and nano-science experiments to test optical and magnetic properties of nanostructures. "As we move forward with the reach of our experiments, we are constantly searching for reliable, flexible tools that support us in our research and help us push the limits of nano-science. The 790+ system is one of the tools we are using to define the future of nanotechnologies," said Professor Bodil Holst, Nanoscience Programme Leader at the University of Bergen's Department of Physics and Technology.

The 790+ RIE provides a flexible technical solution for etching the variety of structures and materials required for advanced research. Simple operation coupled with manual loading on a large electrode addresses the multiple needs of a university operating environment where different substrate sizes and shapes in addition to ease of use by multiple users is key. "Based on the well proven 790 platform, the newly improved 790+ continues to supply reliable and sophisticated technology for many applications including those at the nanoscale level. The increased area of the 790+ electrode increases uniformity and throughput while maintaining affordability for both university and production settings" said Ed Ostan, executive VP of sales & marketing at Plasma-Therm.

Plasma-Therm, founded in 1974, is a supplier of advanced plasma process equipment that focuses on various specialty markets including photomask, solid state lighting, thin film head and compound semiconductor. Plasma-Therm offers both dry etch & PECVD technologies custom built to meet rapidly changing research needs and the demands of production. The company has sales, service and spares locations throughout North America, Europe and Asia-Pacific.

The University of Bergen, located in Bergen, Norway, is a research university with a high international profile that is committed to academic and research excellence.

The university emphasizes basic research, research-based teaching and the development of academic disciplines. The Faculty of Mathematics and Natural Sciences is one of six faculties at the University of Bergen and has around 2700 students.

The Faculty consists of eight departments, including the Department of Physics and Technology, which provide the foundations for its teaching and research activities.

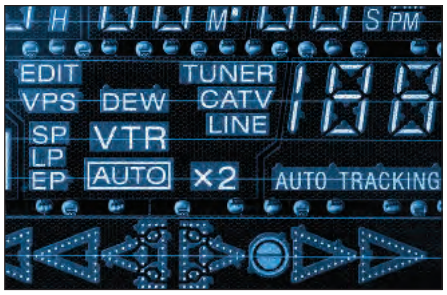
Cree Products To Be Used In ' World's First' All-LED Home

Cree and Habitat for Humanity of Durham have kicked off the construction on the world's first Habitat for Humanity house to be lit with all LED (light-emitting diode) lighting fixtures.

Durham-based LED manufacturer Cree is sponsoring the construction of this home, with Cree employees assisting as volunteers on the project. The home will include Cree's newest LED downlight, the CR6 downlight, as well as other LED products featuring Cree LEDs. The LED lighting in this house is projected to save approximately $250 worth of electricity costs per year over traditional lighting.

The LED lighting in the new Durham home, located at 1015 Moreland Avenue, is part of Cree's previously announced three-year, $1.5 million pledge to provide its high-efficiency LED downlights for all new Habitat homes built in the U.S. The house is expected to be completed by October.

"At Cree, we strive to provide consumers and businesses with cost-saving and energy-efficient LED lighting products to help ease the burden of rising energy costs," said Chuck Swoboda, Cree chairman and CEO. "We're pleased to further our partnership with Habitat for Humanity by supplying LED lights to its U.S. homes and to personally be involved in building this particular home, as it benefits one of our hometown families."

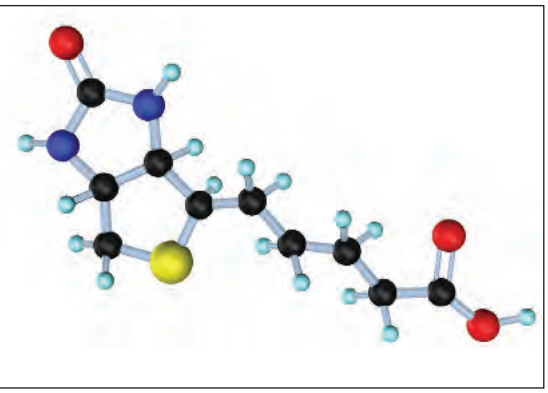


"Habitat for Humanity of Durham recognizes the benefits associated with LED lighting and sees this home as the ideal way to continue our goal of building affordable and sustainable housing for Habitat partner families," said Miguel Rubiera, executive director, Habitat for Humanity of Durham. "We thank Cree for not only providing lighting, but for helping our homeowners save money on their electric bill."

Bruker buy Veeco Metrology Business for $229 Million Cash

VEECO INSTRUMENTS has agreed to sell its Metrology business to Bruker Corporation, a leading provider of high-performance scientific instruments and solutions for molecular and materials research, for $229 million in cash.
The transaction has been approved by the Board of Directors of both companies and is expected to close in the fourth quarter of 2010, pending regulatory review and subject to customary closing conditions.

The sale will transfer Veeco's worldwide Metrology business to Bruker, including Veeco's Atomic Force Microscope (AFM) business in Santa Barbara, CA and its Optical Industrial Metrology (OIM) business in Tucson, AZ, as well as Veeco's associated global AFM/OIM field sales and support organization.



Bruker intends to combine Veeco Metrology with its global Bruker Nano instruments business, which currently sells a broad range of systems and analytical solutions for materials and nanotechnology research. Veeco currently expects cash proceeds from the transaction to be approximately $160 million net of estimated applicable taxes and transaction fees. Additional terms of the transaction were not disclosed. Citigroup Global Markets acted as exclusive financial advisor to Veeco in connection with the transaction.

John R. Peeler, Veeco's CEO, commented: "Following the sale of Metrology, Veeco expects to benefit from greater focus on and investment in our LED & Solar and Data Storage Process Equipment businesses. We believe the sale of Metrology will allow us to accelerate our progress developing new products, gaining share, and aligning with key customers in markets with large growth opportunities, including several "clean tech" markets. The sale is also expected to give us additional financial flexibility to pursue acquisitions and expand customer support for our growing Asia business."

Peeler continued, "Veeco Metrology is a great business that is strong, growing and profitable and has many exciting new products. Even so, it lacks meaningful synergies with our Process Equipment businesses in technology, distribution and customers. We believe it will be a better fit as part of a large and successful instrumentation company, such as Bruker, where the focus will be on continued development of innovative scientific instruments. We have great confidence that the Metrology business will continue to grow and prosper as part of Bruker."

Frank H. Laukien, Bruker's President and CEO added, "We are excited to add Veeco's industry-leading scanning probe microscope (SPM) and optical metrology systems to the Bruker product portfolio of high-performance materials research and nanotechnology instruments. We very much look forward to welcoming the customers, management and employees of the Veeco Metrology business to Bruker after the closing of the transaction."

Veeco will account for the Metrology business segment as a "discontinued operation" effective August 15, 2010. Veeco is therefore updating guidance for third quarter 2010 revenue from continuing operations to be in the range of $255-280 million, with GAAP earnings per share between $1.45 and $1.72 and non-GAAP EPS between $1.13 and $1.33.

Without Metrology, Veeco's updated guidance is that 2010 revenues from continuing operations will be approximately $1 billion, with about 90% from the LED & Solar business segment.

BluGlass and GaN/InGaN RPCVD system

BLUGLASS of Sydney, Australia, which has developed patented GaN-on-glass LED technology, has completed the design, installation and commissioning of its fifth-generation RPCVD system. The latest addition combines the best features of the firm's prototype third- and fourth-generation tools.

Bluglass is a spin off from the III-nitride department of Macquarie University and was established in 2005. The firm has developed a low-temperature process using RPCVD to grow materials including gallium nitride (GaN) and indium gallium nitride (InGaN) on glass substrates. These are primarily used for LED production, with what is reckoned to be significant low-cost potential and inherent scalability.

Also, in May 2009, BluGlass said that it intended to develop high-efficiency group III-nitride solar cells as a supplementary market for its RPCVD technology. Construction of the new tool was enabled as part of the $4.95m grant awarded in June last year under the Commonwealth Government's Climate Ready program for its 'High Efficiency Thin Film Solar Cell Project'.

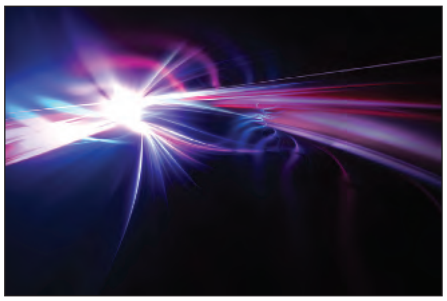
"Not only is this the most advanced and flexible deposition platform that the company has installed to date, but importantly this new-breed RPCVD machine will enable our technology team to deliver optimal process control and, we believe, high-quality single-crystal material," says Chief Technology Officer Ian Mann.

Harvard Files Patent For Highly Directional Terahertz Laser Rays

A COLLABORATIVE TEAM of applied scientists from Harvard University and the University of Leeds have demonstrated a new terahertz (THz) semiconductor laser that emits beams with a much smaller divergence than conventional THz laser sources. The advance, published in the August 8 issue of Nature Materials, opens the door to a wide range of applications in terahertz science and technology. Harvard has filed a broad patent on the invention.

The finding was spearheaded by postdoctoral fellow Nanfang Yu and Federico Capasso, Robert L. Wallace Professor of Applied Physics and Vinton Hayes Senior Research Fellow in Electrical Engineering, both of Harvard's School of Engineering and Applied Sciences (SEAS), and by a team led by Edmund Linfield at the School of Electronic and Electrical Engineering, University of Leeds.

Terahertz rays (T-rays) can penetrate efficiently through paper, clothing, plastic, and many other materials, making them ideal for detecting concealed weapons and biological agents, imaging tumors without harmful side effects, and spotting defects, such as cracks, within materials. THz radiation is also used for high-sensitivity detection of tiny concentrations of interstellar chemicals.



"Unfortunately, present THz semiconductor lasers are not suitable for many of these applications because their beam is widely divergent—similar to how light is emitted from a lamp" says Capasso. "By creating an artificial optical structure on the facet of the laser, we were able to generate highly collimated (i.e., tightly bound) rays from the device. This leads to the efficient collection and high concentration of power without the need for conventional, expensive, and bulky lenses."

Specifically, to get around the conventional limitations, the researchers sculpted an array of sub-wavelength-wide grooves, dubbed a metamaterial, directly on the facet of quantum cascade lasers. The devices emit at a frequency of 3 THz (or a wavelength of one hundred microns), in the invisible part of the spectrum known as the far-infrared.

"Our team was able to reduce the divergence angle of the beam emerging from these semiconductor lasers dramatically, whilst maintaining the high output optical power of identical unpatterned devices," says Linfield.

"This type of laser could be used by customs officials to detect illicit substances and by pharmaceutical manufacturers to check the quality of drugs being produced and stored."

The use of metamaterials, artificial materials engineered to provide properties which may not be readily available in Nature, was critical to the researchers' successful demonstration.

While metamaterials have potential use in novel applications such as cloaking, negative refraction and high resolution imaging, their use in semiconductor devices has been very limited to date.

"In our case, the metamaterial serves a dual function: strongly confining the THz light emerging from the device to the laser facet and collimating the beam," explains Yu. "The ability of metamaterials to confine strongly THz waves to surfaces makes it possible to manipulate them efficiently for applications such as sensing and THz optical circuits."

PV-21 Consortium Set Up To Achieve Competitive PV Solar Energy

The PV21 Renewal project is focussing attention on thin film photovoltaics (PV) which is the fastest growing PV production technology and one which has the opportunity for disruptive R&D over the period of the Renewal programme. With this in mind, the achievements of the thin film platforms, where key materials technologies are demonstrated in PV devices, have been carried forward to the Renewal project.

The work packages cover aspects of innovative PV research from new materials through to fundamentals of thin film PV materials.

The PV21 Consortium will focus effort on the three polycrystalline thin film platforms of silicon, cadmium telluride and the copper indium diselenide (CIS) class of alloys, while encouraging pursuit of the relatively mature wafer silicon technology activity in Loughborough outside the Consortium.

The three basic platforms will be used to test innovative materials and design concepts - for example new absorber materials, transparent conducting oxides (TCOs) or light capture strategies - some of which may also be relevant to the Excitonic

Solar Cells Consortium. The Consortium's structured approach will be enhanced by integration of 'Plus' projects that will inject new ideas and open new pathways towards the ultimate goals of PV21.

The academic partners include nine universities, led by the University of Durham, while the industrial partners includeSemiMetrics, Pilkington Technology and SAFC Hitec.

The Consortium is increasingly aware of the important role played by economic factors in determining the timescale for widespread adoption of thin film PV, and the inclusion of a new package focusing on economic issues will ensure that the planning and management of PV21 will be based on informed choices regarding sustainability, producibility and long term economic viability.

This contextualization of the PV21 research platform will also improve the quality of the Consortium's training program and aid dissemination to a wider industrial and public audience.

The work package is supporting the search for new materials through advanced, high throughput, screening of new materials that will enable a much wider range of materials and alloy compositions to be assessed.

The technological relevance of these new materials will be developed through work packages developing the "platform" processes for high performance solar cells, a techno-economic analysis of cost reduction and consideration of routes to large scale production. The overall objective is to develop thin film solar cells that will lead to higher conversion efficiency at reduced manufacturing cost.

Nanosys & Samsung Alliance accelerate Applications of Nano-Architected Materials

NANOSYS and Samsung Electronics have formed a strategic alliance to accelerate commercial applications of nano-architected materials for the electronics and thin film solar markets.

Nanosys is an advanced materials architect while Samsung is a global provider of telecommunication, and digital products.

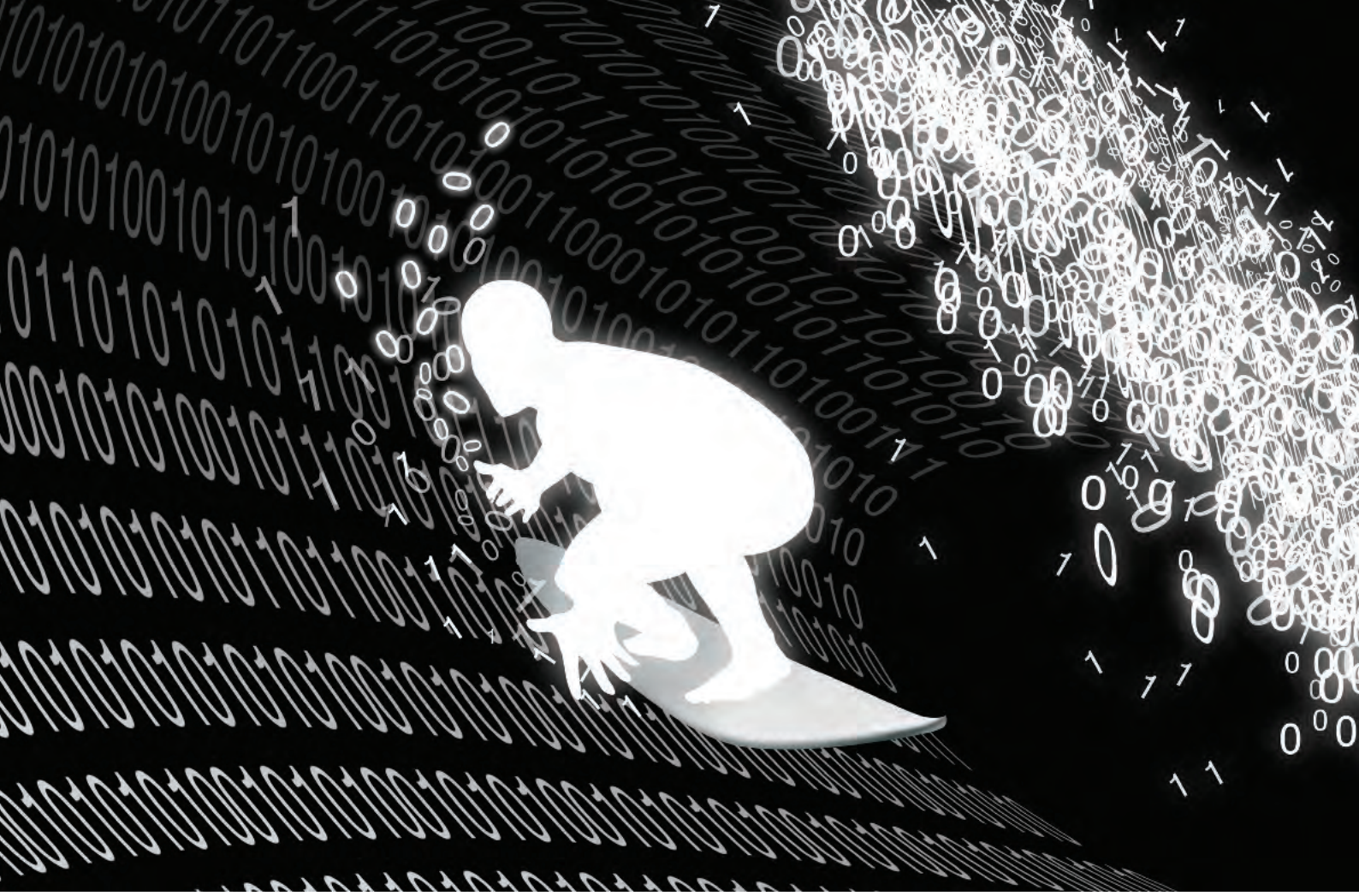
Under the terms of the deal, Samsung will contribute funding and resources to co-develop products using Nanosys technologies, in addition to $15 million equity investment from the affiliated Samsung Venture Investment Corporation.

“We believe that working closely with Nanosys will help us to develop exciting new products for our customers that will address needs in the world’s largest markets across a number of technologies,” said Seungho Ahn, Senior VP of the Intellectual Property Center, Samsung Electronics.

“Samsung is a clear leader in the electronics and solar sectors,” said Jason Hartlove, CEO of Nanosys. “Not only does Samsung bring deep knowledge of solar, memory and display technologies and markets, they bring tremendous experience in scaling up new technologies, which will help us accelerate the development, production and market introduction of devices enabled by our nano-architected materials.”

Samsung’s equity investment will come from Samsung Venture Investment Corporation, with at least an additional $10 million in total from previous venture capital investors including Arch Venture Partners, El Dorado Ventures, Polaris Venture Capital and V enrock.

With this arrangement, Samsung and Nanosys will work together to create a new generation of cost effective, higher-efficiency products in the fields of solar, LED, memory, semiconductor, and display.



GaN HEMTs advance to ultrahigh bandwidths

Tried-and-true strategies for speeding-up InP HEMTs are clarifying the path to extending the bandwidth of their GaN cousins to millimeter-wave frequencies. Significant progress was realized by switching from the familiar pairing of AlGaN and GaN to an AlInN and GaN heterostructure, which combines weaker surface depletion and better vertical scaling with apparently higher carrier velocities, according to **Colombo Bolognesi from ETH-Zürich and Nicolas Grandjean from EPFL.**

A fundamental trade-off between power handling and bandwidth underpins all semiconductor devices: smaller devices are faster, but they handle lower voltages and currents. In short, power roughly scales with the inverse of the frequency squared.

We as device physicists have some flexibility in the face of this trade-off, to the extent that we can play with the composition of the materials to improve breakdown properties. However, there is no free lunch! Typically, materials that can withstand large electric fields show slower moving electrons, precisely because electrons must be tightly held in these materials for them to not breakdown in high electric fields. As someone famous once said, this follows from the "Law of Conservation of Trouble," and it explains why some *Compound Semiconductor* readers get paid the proverbial "Big Bucks" to do what they do!

Within the array of III-V compounds, GaN stands out because it can deliver bandwidths matching or exceeding those of GaAs devices, with at least five times the output power density per unit device width (1-2 W/mm in GaAs to at least 5-10 W/mm in GaN).

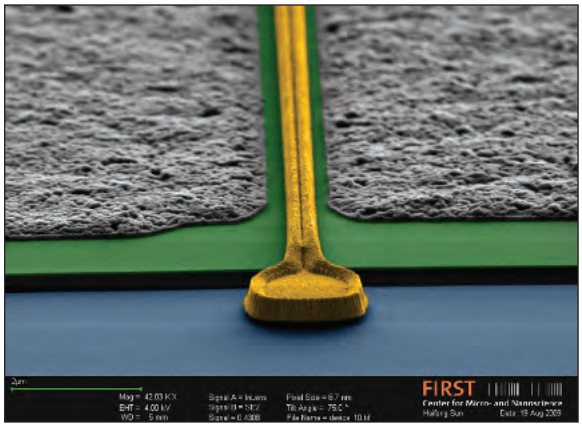


Figure 1. An AlInN/GaN HEMT fabricated at ETH-Zürich from EPFL epitaxial layers

Power at high frequencies is at a premium, and people will buy it, if someone can generate it. There are many angles from which to justify the extension of GaN HEMTs to higher frequencies, and all have to do with the power/frequency trade-off. As a rule of thumb, devices need bandwidths three-to-four times higher than the intended operation frequency, which means that if one wants to generate power at 30 GHz, for say, electronic warfare applications, one needs devices with bandwidths in excess of 100 GHz with a lot of power gain at 30 GHz.

Nitride devices also offer high power-added-efficiencies which are, for example, critical in airborne applications because of the limited aircraft payloads. For instance, a high-resolution radar operating between 27 and 40 GHz must radiate maximum power within a fixed power budget.

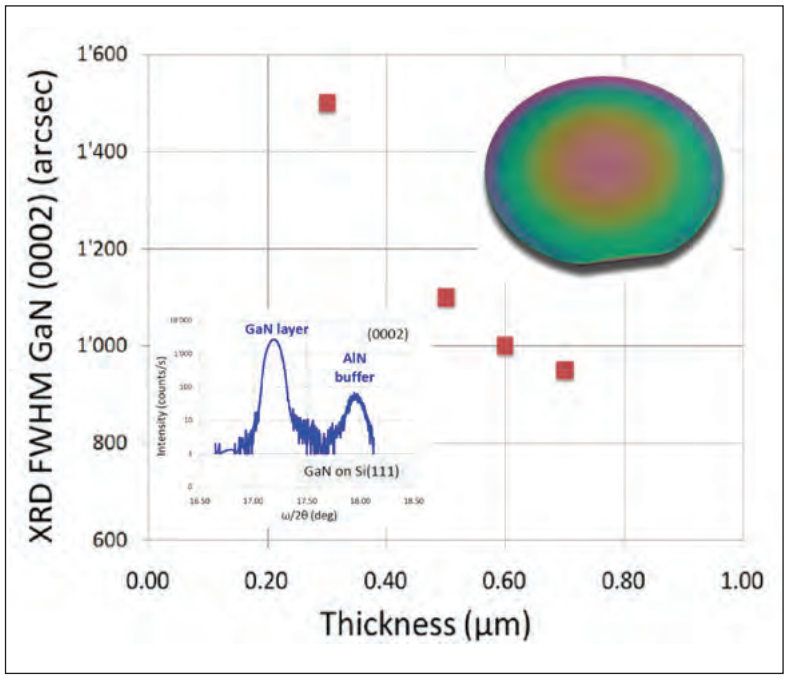


Figure 2. X-ray analysis showing AlInN compositional uniformity for material grown on (111) silicon

The inherent ruggedness associated with widegap semiconductors also potentially renders wideband GaN HEMTs attractive for low-noise, front-end amplifiers. It is possible that these amplifiers could be free of the performance-degrading input protection devices used today to protect sensitive GaAs or InP front ends from damage due to over-voltage.

There is currently also research targeting the development of 500 GHz GaN HEMTs with 10 V breakdown voltages for special digital ICs – whether this is a realistic goal remains an open question, but the work clearly inscribes itself under the umbrella of speed at higher power levels, since nowadays such bandwidths can be only reached with devices showing 3-4V breakdown voltages at best, namely InP DHBTs.

What can GaInAs teach us?

Some inspiration on how to extend GaN HEMTs to mm-wave frequencies can be gained by considering the history of GaInAs channel HEMTs. Since the late 1980s the cutoff frequency record for the GaInAs-based HEMT has steadily climbed from 100 GHz to in excess of 600 GHz. The refinements that have driven this progress offer insights on how to speed-up GaN HEMTs, because ironically, despite the widely different energy gaps and other physico-chemical properties of the materials involved, a number of interesting parallels can be drawn between the two technologies.

The fantastically successful evolution of GaInAs-based HEMTs has on one hand relied on the development of a superior channel layer. Such a channel can confine higher electron densities, and has the added advantage of reducing parasitic delays – channel charging delay, and drain depletion delay – therefore increasing transistor cutoff frequencies. Stronger carrier confinement in the channels results from an increase in the indium content of this layer, an approach that was initially employed in pHEMTs on GaAs before being extended to InP.

The other key to speeding up GaInAs HEMTs has been the location of the gate electrode with respect to the current carrying channel layer. By placing the gate very close to the two-dimensional electron gas (2DEG) channel, it becomes possible to realize deep-sub-micron devices that maintain a good electrostatic control of the channel electrons by the gate electrode, as evidenced by minimized short-channel effects.

In the world of MOSFETs, engineers would characterize such devices as being "well-tempered." By that they mean that the density of channel electrons is well-controlled by the gate electrode, and the channel is effectively shielded from the influence of the drain contact. InP-based materials show weaker surface depletion effects than GaAs, allowing gates to be placed closer to the channel.

Keeping the gate-to-channel distance small compared to the gate length increases device transconductances, and leads to a faster charging and discharging of intrinsic and parasitic capacitances, and ultimately, to faster transistors.

Lattice-matched barriers?

The conventional form of GaN-based HEMT, which involves the pairing of AlGaN and GaN, has undergone more than a decade-and-a-half of frantic development. However, question marks are now hanging over the reliability of this device (see, for example [1, 2]). These are thought to stem from inherent strain in the heterostructure, due to a combination of lattice-mismatch and piezoelectric contributions.

Another concern with this AlGaN/GaN incumbent is surface depletion effects in the 2DEG that arise when the top barrier thickness is thinned much below 15 nm [3]. This can be addressed with AlN thin top barriers that increase channel sheet densities [4], but it is unclear how this impacts the strain-related device degradation. Other research groups have countered surface depletion effects with aluminum-rich AlGaN barriers and various dielectrics, an approach that has yielded impressive cutoff frequencies, with f_T values reaching 190 GHz with 60 nm gate MISFET structures [3, 5].

One promising alternative to the AlGaN/GaN HEMT is a variant based on a heterostructure between AlInN and GaN. This potential successor, which was proposed by Jan Kuzmík from the Technical University of Vienna, can be fabricated with a lattice-matched barrier and thus addresses some of the strain-related reliability concerns associated with conventional lattice-mismatched, AlGaN/GaN heterostructures [6]. Kuzmík has also argued that the pairing of AlInN and GaN should reduce surface depletion effects and potentially unlock the door to the fabrication of GaN HEMTs with excellent channel aspect ratios down to very short gate lengths.

Early experimental efforts suggested that the AlInN/GaN pairing is capable of fulfilling many expectations. The feasibility of ultrathin barrier AlInN/GaN HEMTs has been verified down to 3 nm thick AlInN barriers [7], and such devices have also demonstrated phenomenal stability, even surviving operation at temperatures of 1000 °C [8]. Such high-temperature survival is clearly outside the reach of traditional AlGaN/GaN devices.

To put it simply, it seems that AlInN/GaN heterostructure channels are capable of driving evolutionary improvements reminiscent of those achieved by the transition from GaAs-based pHEMTs to their InP counterparts. And it seems that these benefits can be realized without paying the penalty of more fragile materials, as was the case when moving from GaAs-based HEMTs to high-indium-content GaInAs alloys on InP.

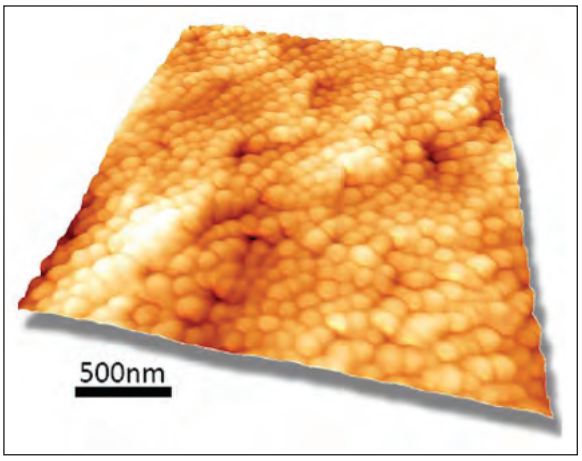


Figure 3. Atomic force microscopy (AFM) measurements indicate that the AlInN barrier is very smooth. The root-mean-square roughness is just 0.5 nm

One key benefit that results from the weaker surface depletion effects in AlInN/GaN HEMTs is a vertical scaling advantage – this is very similar to that seen for AlInAs/GaInAs HEMTs over AlGaAs/GaInAs equivalents [9]. In addition, HEMTs based on AlInN were reported to exhibit higher carrier velocities in the channel, thanks to faster thermalization and decay of hot longitudinal-optic phonons. The upshot of this is higher electron velocities in strong electric fields [10].

Although the analogy to InP pHEMT development is very good, there is one difference between GaN and InP devices. With InP, higher channel velocities stemmed from improved transport properties in GaInAs alloys with a high indium content, which made the devices more fragile, due to the lower temperature stability of high indium content materials.

In comparison, while the AlInN/GaN system does contain some indium, it is the higher aluminum content that is responsible for the ruggedness advantage that AlInN/GaN HEMTs have over their AlGaN/GaN equivalents. The aluminum content in the AlInN alloy that forms the lattice-matched barrier on GaN is 83 percent. This is far higher than the mere 30 percent in strained AlGaN barriers, a fundamental difference that appears to confer a far greater stability of the newer form of HEMT.

By putting some faith into the analogy between AlInN/GaN HEMTs and InP pHEMTs, it is just a small further step to reach the idea that an AlInN/GaN HEMT should yield superior cutoff frequencies compared to its conventional predecessor - just as the case was for InP pHEMTs compared to GaAs pHEMTs.

However, until recently, AlInN/GaN HEMTs have failed to fulfill this promise, conceding a significant bandwidth advantage to their forerunners. But the good news is that thanks to material and process improvements, the ultimate cutoff frequency of AlInN/GaN HEMTs has more than doubled in the last year [11, 12].

Growing AlInN

At first sight it appears quite challenging to grow high-quality AlInN films. There are huge differences in growth conditions of AlN and InN, which have typical growth temperatures of 1100 °C and 500 °C, respectively. In addition, the lattice mismatch between these materials can be as high as 13 percent. However, it is possible to realize a homogeneous ternary through careful optimization of the growth conditions.

At EPFL in Lausanne, Switzerland, AlInN/GaN epilayers are grown in an Aixtron 200/4 RF-S MOCVD system on 2-inch substrates made from *c*-plane sapphire, silicon, and SiC. Growth on sapphire is initiated by a low-temperature GaN nucleation layer, and an AlN buffer is employed for silicon and SiC. In all cases, a 0.5-2 μm-thick, undoped GaN layer follows the buffer. This is grown using conditions to minimize possible parasitic conduction paths, and its net residual doping concentration (N_D-N_A) is typically below 10^{14} cm^{-3}.

All HEMT structures are free from cracks. Dislocation densities in the epilayers are governed by the substrate choice, and range from 7 x 10^8 cm^{-2} for sapphire to 5 x 10^9 cm^{-2} for silicon. Typical X-ray diffraction (XRD) rocking curve linewidths are less than 1000 arcsec for GaN deposited on silicon, below 500 arcsec for GaN grown on sapphire, and under 200 arcsec for GaN epitaxial layers on SiC.

The AlInN/GaN heterostructure features a thin GaN channel, grown under conditions specifically chosen to improve surface morphology so as to form a good interface with the barrier material. An AlN interlayer just a nanometer thick is inserted between the channel and the AlInN barrier to limit the detrimental impact of alloy scattering. When properly done, this delivers a massive improvement in the 2DEG lateral transport properties. Growth of the AlInN layer is typically carried out at 800-850°C, using deposition rates of 0.2-0.6 μm/h. If the temperature is too low, the crystal quality degrades, according to high-resolution x-ray diffraction (XRD). On the other hand, if the temperature is too high, it impairs indium incorporation and prevents formation of near-lattice matched alloys. Treading the fine line between these two unwanted scenarios is crucial to realizing good 2DEG properties, and ultimately is the key to great HEMT performance. Material uniformity of thick, nearly lattice-matched AlInN epilayers grown on GaN-on-sapphire templates can be assessed by energy dispersive X-ray analysis. The indium composition slowly varies across the wafer indicating good homogeneity (see Figure 2). It is typically 17 ± 1 percent for lattice-matching to GaN. The surface of the AlInN barrier is very smooth and has a root-mean-square roughness of just 0.5 nm (see Figure 3).

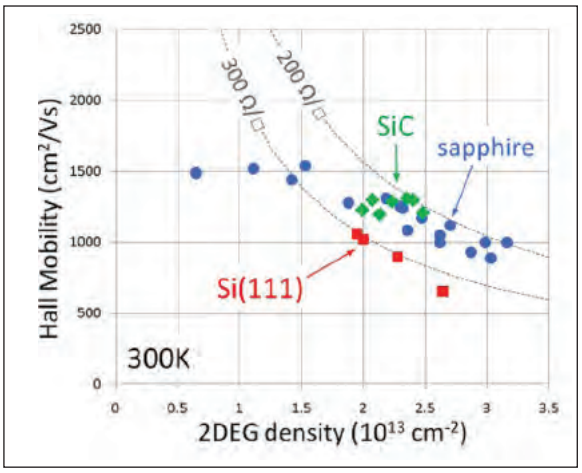


Figure 5. Sapphire and SiC still offer superior platforms to silicon for the growth of AlInN/GaN HEMTs, but silicon is not too far behind

Scanning transmission electron microscopy (STEM) and energy-dispersive X-ray spectroscopy (EDXS) analysis reveals a sharp interface, with no evidence of gallium diffusion into the AlInN barrier (see Figure 4) [13]. If this element, gallium, had significantly contaminated the barrier, it would decrease the 2DEG electron density in the channel. By varying the indium content of the AlInN barrier and its thickness, it is possible to realize 2DEG densities ranging from 0.5-3.5 x 10^{13} cm^{-2}.

Room-temperature mobility in the 2DEG depends on both the sheet carrier density and the type of substrate (see Figure 5). The lowest sheet resistances, typically 200 Ω/□ are obtained on sapphire and SiC. On silicon, the sheet resistance is slightly larger, due to the lower crystalline

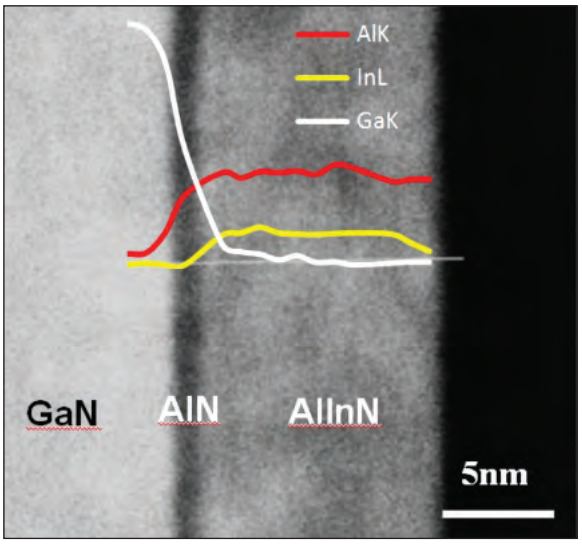


Figure 4. Gallium does not diffuse into the AlInN barrier, according to STEM and EDXF analysis. These are reproduced courtesy of Dr. L. Zhou and Prof. D.J. Smith, Arizona State University

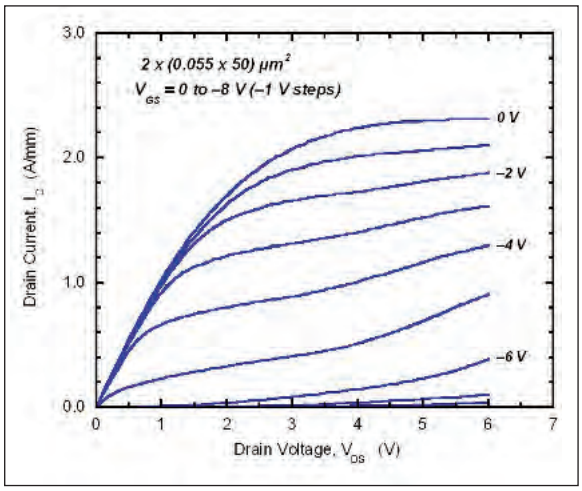


Figure 6. Current-voltage characteristics for an AlInN/GaN HEMT grown on semi-insulating SiC. The gate length of the device is 55 nm

quality of epitaxial layers (as revealed by the XRD linewidths). However, resistance is still only 300 Ω/□. This value indicates that silicon can provide a platform for realizing high-performance millimeter-wave transistors on low-cost substrates. The thermal conductivity of silicon lies between that of sapphire and SiC, and it has the potential to be used as a low-cost platform for GaN/AlInN HEMTs in either systems requiring lower CW power operation, pulsed output (such as radar) and/or in systems requiring many cheap devices (decoys).

Record breaking devices

Our epitaxial HEMT wafers include a structure with a 30 nm AlN nucleation layer, a 1 μm-thick GaN insulating buffer and channel layer, a 1 nm AlN spacer layer, and a 10 nm thick, nearly lattice-matched $Al_{0.86}In_{0.14}N$ barrier. This structure had a channel electron sheet density of 2.4 x 10^{13} cm^{-2}, a mobility of 1,300 cm^2/Vs, and a sheet resistance of 200 Ω/□, according to room-temperature Hall measurements. Incidentally, similar AlInN/GaN HEMT epilayers are commercially available from EPFL start-up NovaGaN.

The layers were processed in the ETH-FIRST Laboratory in Zürich. Mesas were defined in the epiwafers by plasma etching, before ohmic contacts were added by Ti/Al/Au evaporation. Two-step rapid thermal annealing in N_2/H_2 forming gas followed.

Post-process transmission-line measurements revealed contact and sheet resistances of 0.3 Ω/mm and 182 Ω/□. Electron-beam lithography defined Ni/Au T-shaped gates with a 55 nm footprint in the center of the 1 μm source/drain space using high-resolution electron beam resists. A 100 nm-thick, SiN passivation film was then deposited by plasma-assisted CVD and patterned to create the contact pads. Ti/Au was used for the overlay metallization. The 55 nm gate HEMT produces a maximum drain current of 2.3 A/mm at a gate-source voltage (V_{GS}) of 0 V (see Figure 6). Extrinsic transconductance (g_M) peaked at 575 mS/mm when the HEMT was operated at a V_{GS} = -5.3 V and V_{DS} = 4.0 V.

AlInN/GaN devices often show a residual gate leakage current, and this is now a topic of investigation in various groups. Understanding the leakage mechanism, and stemming its flow, will be key to increasing the power-added-efficiency characteristics of these HEMTs, ultimately enabling them to meet the efficiency requirements for certain applications.

The gate leakage origin still is a mystery, but not all researchers involved with AlInN/GaN HEMTs experience excessively high gate leakage currents. Leakage may be primarily associated with epitaxial growth, device processing or even a combination of both. At this time it is known that one can reduce it by inserting insulators between the gate metal and the barrier, but it remains desirable to suppress leakage in a standard HEMT structure to keep the gate as close to the 2DEG as possible. At this point it should be kept in mind that the leakage issue may partly arise due to the thin barriers used – it is then normal to expect a higher leakage than with thicker barriers, just as it is observed in AlGaN/GaN HEMTs!

Transistor microwave performance at the peak f_T bias of V_{DS} = 4 V and V_{GS} = -5.3 V has been measured (see Figure 7), and extrapolation of the short-circuit current gain $|h_{21}|^2$ and of Mason's unilateral gain U with a -20 dB/dec roll-off yields a f_T of 205 GHz and f_{MAX}(U) of 191 GHz. The f_T and f_{MAX} remain high for a broad range

AlInN/GaN devices often show a residual gate leakage current, and this is now a topic of investigation in various groups. Understanding the leakage mechanism, and stemming its flow, will be key to increasing the power-added-efficiency characteristics of these HEMTs, ultimately enabling them to meet the requirements for certain applications

of drain biases, remaining above 160 GHz up to V_{DS} of 8 V. Increasing the drain bias to a V_{DS} of 5 V resulted in a peak f_{MAX}(U) of 200 GHz with an f_T of 188 GHz at a V_{GS} of -5.3 V. A cutoff frequency of 205 GHz is the highest-ever achieved for any GaN-based transistors on any substrate. It is also the first time that AlInN/GaN-based devices have established the record for bandwidth in nitride HEMTs. Although one can expect records to continue to change hands between different types of GaN HEMTs, these results are extremely pleasing considering the rapidity of progress with the new AlInN/GaN heterostructures.

Analysis of the frequency performance, which will be published shortly, reveals that the effective velocity in AlInN/GaN channels is up to 60% higher than in the fastest AlGaN/GaN HEMT channels ever produced. Some theoretical and experimental work has linked higher channel velocities in AlInN/GaN channels to the higher 2DEG concentrations. These are believed to favor the faster dissipation of longitudinal-optical phonons in comparison to the situation in conventional AlGaN/GaN channels. Today, however, it is not possible to fully explain the improved performance observed with AlInN/GaN by this phenomenon. Further studies are necessary. For the sake of comparison, AlInN/AlN/GaN HEMTs were fabricated in a similar manner using epilayers grown on high-resistivity silicon (111) substrates. In this case, the epitaxial structure comprised a 60 nm AlN nucleation layer, 700 nm GaN insulating buffer and channel layer, a 1 nm AlN spacer layer, and an 8 nm-thick, nearly lattice-matched, $Al_{0.86}In_{0.14}N$ barrier. According to room-temperature Hall measurements, the channel electron sheet density was 1.95 x 10^{13} cm^{-2} and its mobility was 1,060 cm^2/Vs. These inferior values compared to the above layers on SiC are a result of a reduction in crystal quality, which was highlighted by broader XRD linewidths. The 2DEG and mobility are 20-25 percent lower than that of the AlInN/GaN HEMT on SiC, and account for the increase in sheet resistance to 300 Ω/□.

Devices with a 80 nm gate length were fabricated on these layers, which show simultaneous cutoff frequencies, f_T of 143 GHz and f_{MAX}(U) of 176 GHz. Although these values are lower than those achieved with the 55 nm

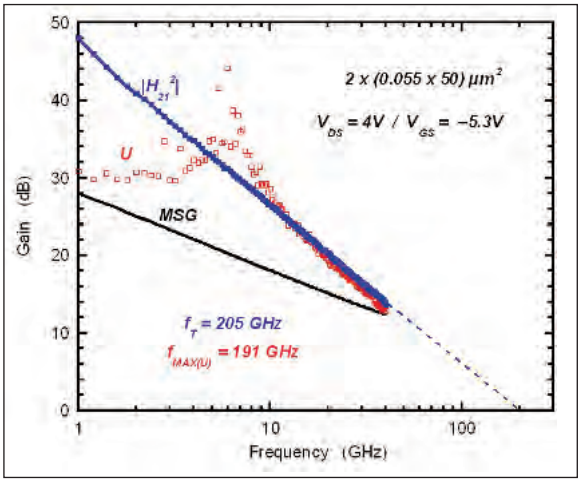


Figure 7. The AlInN/GaN HEMTs fabricated in the EPFL-ETHZ collaboration deliver a record breaking cut-off frequency for any form of GaN HEMT

devices on SiC, they are still the fastest nitride devices ever built on silicon. It is also interesting to note that the f_T's obtained here for the 55 and 80 nm gate HEMTs on SiC and silicon substrates scale almost exactly with the inverse gate length. Clearly, the AlInN/GaN heterostructure has more surprises in store than one could ever anticipate!

AlInN/GaN HEMTs are fast emerging as an interesting alternative to conventional AlGaN/GaN HEMTs which offers much higher maximum current densities and transconductances in a (nearly) lattice-matched barrier system characterized by a superior thermal stability. Although the present article mainly focused on recent EPFL/ETHZ efforts toward extending the devices to higher frequencies, the fundamental properties of the AlInN/GaN system do lend themselves well to the realization of high-power, high-efficiency transistors, as recently reported by workers from Alcatel-Thales with the demonstration of 0.25 μm AlInN/GaN HEMTs with an output power of 10.3 W/mm and a power-added efficiency of 51% at 10 GHz [14]. The combined advantages of AlInN/GaN heterostructures for power HEMTs are extremely attractive and provide ample motivation to find solutions to remaining challenges associated with the material system: one can count on an increasingly important footprint for AlInN/GaN HEMTs in the field of GaN microwave and millimeter-wave electronics for the times to come.

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Integra turbo-charges its S-band transistors with gallium nitride

Since the late 1990s Integra has been manufacturing pulsed, S-band silicon transistors for radar. It has recently expanded its portfolio with GaN versions that are smaller, more efficient, and deliver gain over a far broader bandwidth. **Richard Stevenson** tracks this new venture.

GaN is a great material for producing RF transistors. It can yield devices with high efficiency and excellent gain over a broad bandwidth, characteristics that have encouraged many III-V chip makers within our community to develop high-frequency devices based on this material.

But these companies, which include the likes of Cree, RFMD, TriQuint and Eudyna, will not have this market to themselves. The allure of GaN has also piqued the interest of silicon RF manufacturers, including Integra Technologies, a company with almost 100 staff that makes high-power, pulsed transistors for the aviation industry.

Based in El Segundo, CA, Integra is renowned for its S-band transistors - it claimed that they delivered unparalleled performance when the company was founded in 1997.

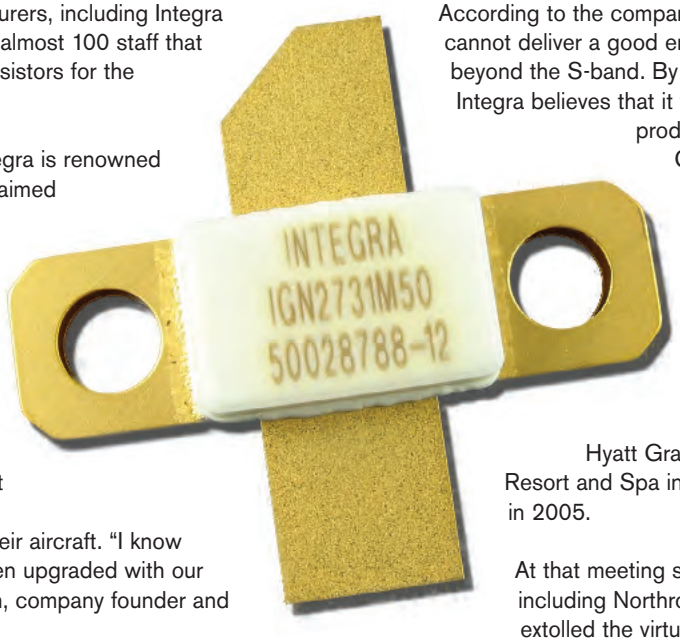
Today Integra is Raytheon's sole supplier of this class of device, which the US defense giant uses to fulfill its a long-term contract to supply radar systems to US airports that help pilots land their aircraft. "I know that London Heathrow has been upgraded with our devices too," says John Titizian, company founder and president.

Silicon's weaknesses

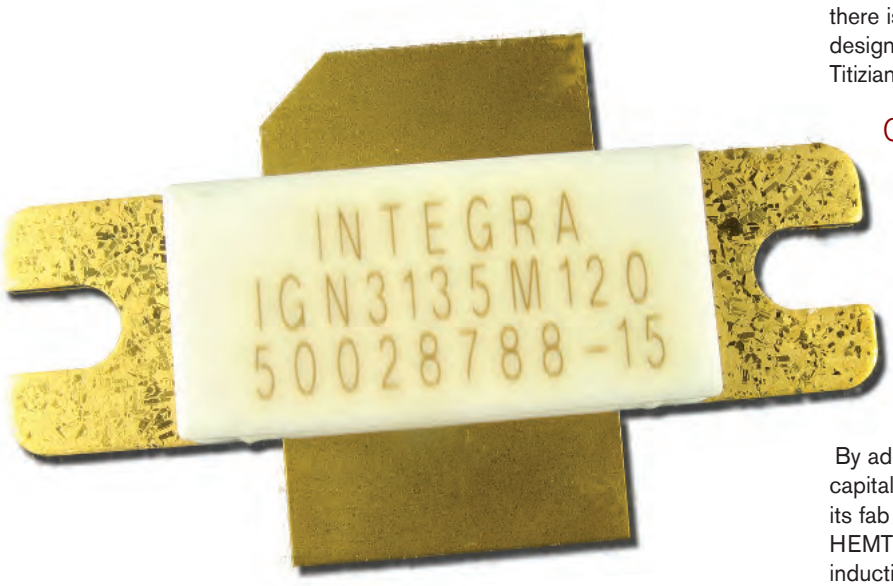
Integra has several reasons for taking its decision to develop GaN transistors for radar applications. Turning to this wider bandgap transistor improves the resolution of radar systems and their target tracking capability. "And instead of having different frequency radars, it is possible to have one radar that covers a lots of bands," enthuses Titizian. He reveals that Integra's decision to diversify into GaN was also motivated by the capability of this material to operate at higher frequencies. According to the company, silicon devices cannot deliver a good enough performance beyond the S-band. By turning to GaN, Integra believes that it will be possible to produce products for the C-, X-, and Ku-bands.

The company's foray into GaN can be traced back to its attendance at a compound semiconductor conference held at Hyatt Grand Champions Resort and Spa in Indian Wells, CA, in 2005.

At that meeting several firms, including Northrop Grumman, extolled the virtues of GaN.



Left: At the IEEE MTT-S International Microwave Symposium in Anaheim, CA, from 23 to 28 May, Integra released a pair of GaN HEMTs. The more powerful of the two S-band products, which is shown here, covers the 2.7-3.1 GHz range



Integra has developed two products operating in the upper S-band (3.1-3.5 GHz). These devices are targeting military radar. The transistor shown here produces 120 W. The other device, which produces over 10 W, is an internally matched part with 50 ohm impedance at the leads

"We were debating whether to go with GaAs or GaN," reminisces Titizian. "After the information we got at that conference we decided that we were going with GaN."

Efforts began in earnest in the latter half of 2008. At that point the company set itself the target of sampling its first GaN products in 2010. It is a goal that has been completely fulfilled following the company's announcement of two GaN HEMT products operating in the S-band at the IEEE MTT-S International Microwave Symposium that was held this May in Anaheim, CA.

Initially Integra's GaN development involved just two senior staff – a process engineer and a designer. Since then the team has expanded to five, with three employees working on the processing of the device and another two focusing on circuit development. This appears to be a remarkably small number of engineers for driving the development of a transistor employing a material entirely new to the company.

Titizian, however, is not surprised by the tremendous progress: " We are semiconductor experts, and we understand semiconductor physics. It's true that GaN presents some different challenges, but we understand the device physics."

When founded, the company's expertise lay in silicon bipolar devices. However, more recently it has expanded its knowledge base, first with the development of silicon LDMOS technology, which is not so far removed from GaN HEMTs. "If we had to go from bipolar to GaN, then that may have been a bigger jump, " says Titizian, who reveals that extensive design iteration was not required for the development of the company's HEMTs. Although there is not as much software available for aiding the design of GaN HEMTs as there is for silicon devices, Titizian says that what exists is adequate.

Outsourcing epiwafer growth

Integra decided against developing in-house, GaN-on-silicon growth expertise. Instead it evaluated material from several epiwafer suppliers. In some cases these wafers were too brittle, or yielded devices with leakage currents that were far too high. However, these problems did not plague the material provided by a Japanese manufacturer, which is now Integra's sole supplier of epiwafers.

By adopting an outsourcing model, Integra slashed its capital expenditure on new equipment needed to provide its fab with the capability to process GaN-on-silicon HEMTs. Its only recent addition is a chorine-based, inductively coupled plasma (ICP) etcher. However, there have also been some adjustments to processing tools on the 6-inch line, so that they are capable of handling 4-inch GaN-on-silicon wafers.

The epiwafers that Integra imports have a silicon (111) foundation, because this orientation is better at accommodating the lattice and thermal mismatches between silicon and GaN than the more widely used (100) cut. Processing this material presents no problem whatsoever for Integra, because the company's bipolar products are also grown on the silicon (111) orientation.

Integra has also been able to draw on its silicon technology for packaging its GaN HEMTs, which share the housing employed for LDMOS devices. Problems associated with parasitics are negated by taking sufficient care with the assembly process.

The pinnacle of all this effort-to-date has been the launch of products at the MTT-S show: a pair of single-ended devices housed in a ceramic flanged package, which deliver either a 25 W or 50 W peak output in the 2.7-3.1 GHz range. Both HEMTs produce at least 12 dB of gain and have a breakdown voltage in excess of 200 V. These performance figures were recorded using 300 μs pulses, a 10 percent duty cycle, and an operating voltage of 50 V.

What's the pecking order?

Although the performance of these devices is impressive for a firm that only started developing GaN products two years ago, these HEMTs are not state-of-the-art commercial products.

"We're getting 3.5 W/mm, and there are devices out there by Cree and Eudyna in the 5 W/mm range," admits Titizian. "We could design devices with higher W/mm, but we're focused on offering a reliable device that will not

To ensure a high reliability for all of its products, Integra employs a gold-metallization process. This element has an incredibly high activation energy, reducing the likelihood that it will undergo electromigration, which could ultimately cause premature ageing of the transistor

drift in performance with time."

One avenue that Integra can explore to improve the performance of its HEMTs is to shorten gate length. The company is going to do just this, and has a target of 0.3 μm in its sights. "I'm absolutely convinced that we'll have comparable devices [to the leading GaN HEMT makers] by next year," claims Titizian.

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Over the next year or so Integra plans to introduce several more GaN products. It has already started adding to its family of GaN S-band products and it is also producing cousins operating at higher frequencies. It has one device operating in the C-band, and over the next few years more devices will be launched in both this band and the X-band.

To protect its product's commercial future, Integra is looking at the intellectual property surrounding GaN transistors, and deciding whether it needs to patent its technology. "There is a lot of public information out there. You can put together a device without infringing on other people's IP," says Titizian.

Performance at a price?

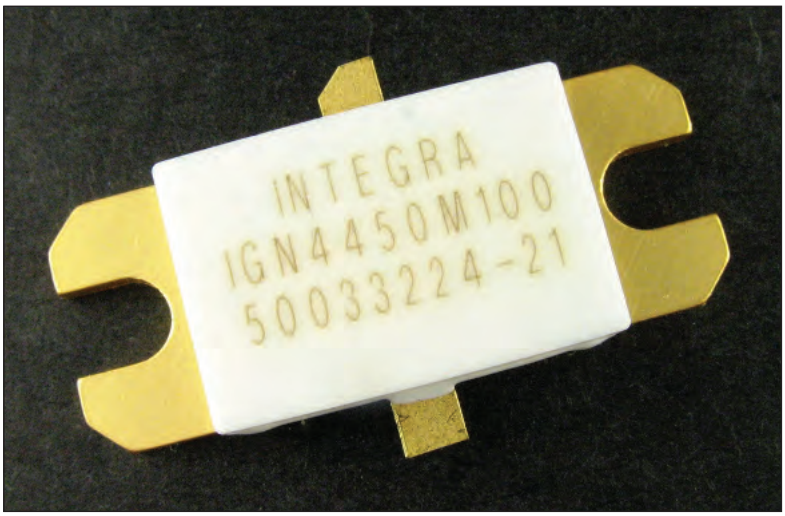
The costs associated with manufacturing Integra's GaN S-band products are significantly higher than those associated with production of silicon transistors operating in a similar part of the microwave spectrum. However, Titizian expects that this cost gap will close as products migrate to larger wafers: "Gallium nitride on 6-inch silicon will probably be available next year, and at some point GaN-on-silicon could be available on much larger wafers, such as 12-inch wafers." This will drive down manufacturing costs, and Titizian believes that there should come a time when GaN is comparable to silicon, in terms of the dollar-per-Watt metric.

Integra is also starting to develop GaN-on-SiC devices, which it says are the only wide bandgap RF technology that the US military is currently willing to deploy. "We are going to offer both technologies to our customers, and we believe that GaN-on-silicon may be cheaper in the long run." Although GaN-on-SiC tends to have the edge in terms of reliability and output power, Titizian says that many applications may be adequately served with the silicon-based equivalent. Titizian reveals that processing GaN-on-SiC wafers does not require any major modifications to the fab. "With the ICP etcher we can do the vias – that is not an issue any more."

Sales of Integra's GaN-based products are expected to grow significantly over the next five years, and account for over half of the company's revenue in 2015. However, that does not mean that Integra will be turning its back on its customers wanting to buy silicon products.

"We are not going to abandon silicon because we've made commitments to our customers," says Titizian. "Most of these systems have a long life cycle that we need to support, and we will support that."

Keeping customers happy has long been acknowledged as one of the keys to a successful business, alongside the launching of new, superior products. Integra is executing on both these fronts, and it looks to be assured of a bright future.



Integra has one HEMT operating in the C-band: the IGN4450M100. This transistor produces more than 100 W of output power at 4.4-5.0 GHz

IR slashes GaN manufacturing costs

GaN power devices are smaller and more efficient than equivalents made from silicon. But significant commercial success will only follow when their manufacturing costs fall, a goal that can be realized by turning to production on 150 mm silicon CMOS processing lines, writes **Michael Briere** on behalf of **International Rectifier.**

There is a downside to the rising standard of living throughout the world: increased energy consumption. This is expected to go up by more than one third over the next twenty years, according to the US Energy Information Association.

But it doesn't have to be like this, because there are many ways to reduce the amount of energy needed to power applications. One opportunity is to introduce electric motors into transportation, to either replace or work in tandem with an internal combustion engine. This can deliver energy savings of 60 percent.

Similarly, it is possible to slash the power consumption of consumer appliances by 50 percent by replacing AC induction motors with inverter-driven, permanent magnet motors. And energy savings can also result from switching to electronic-ballasted forms of lighting and improvements in the delivery of electronic loads, especially for the growing IT infrastructure.

Grasp all these energy saving opportunities and global energy consumption could plummet by a quarter, trimming $2 trillion off of the world's annual electricity bill (assuming that a barrel of oil costs $45). It is a staggering financial saving, which dwarfs the globe's yearly spend on power electronics, $50 billion.

These energy savings can be realized by substantial, optimized and intelligent power electronics for driving various loads. In principle, this form of power electronics is already available, but it could take another decade before prices fall far enough for consumers to buy products incorporating this technology for reducing global energy consumption.

One way to speed this adoption is to increase the performance of modern power electronics, while cutting its cost. Power-converter sub-systems offer the most fertile ground for the uptake of this technology, and improvements have already enabled increasingly dense and efficient working loads.

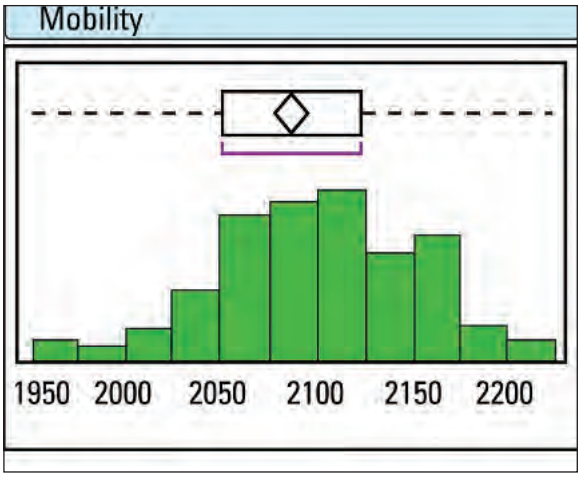


Figure 1: IR's GaN-on-silicon epitaxial process produces HEMTs with a two-dimensional electron gas Hall mobility typically exceeding 2000 cm^2/Vs

Employing these power conversion systems is most attractive when they combine affordability with efficient handling of dense loads. The last 40 years has witnessed significant improvements in these three attributes – density, efficiency and cost – gains that have arguably been dominated by refinements in the power devices that they use. Similarly, manufacture of a radically improved power switch could spur a revolution in power electronic architectures and systems.

At International Rectifier we have been developing a technology capable of delivering this step-change: the GaNpowIR platform. Here GaN-on-silicon epitaxy is combined with device fabrication processing on 150 mm substrates, using a standard, modern, silicon CMOS manufacturing line that has been subjected to little modification to equipment or process discipline.

Displacing the silicon incumbent

Commercial success demands taking market share from the incumbent technology, the silicon power FET. This device has been serving customers for 30 years, and has enabled widespread adoption of switch-mode power supplies. These have surpassed the linear regulator as the dominant power architecture. Alongside the power FET, another mainstay of the power electronics market is the

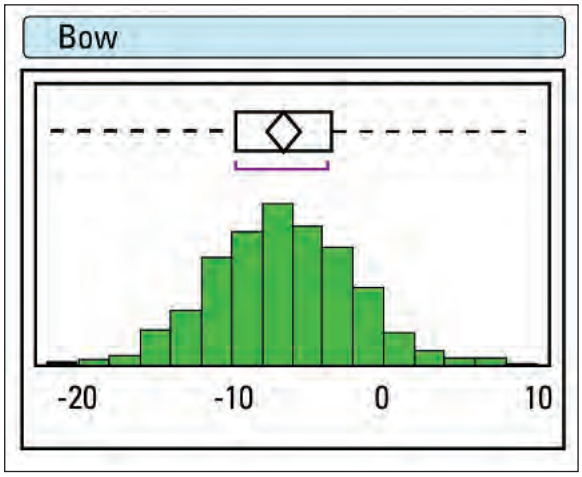


Figure 2: The wafer bow in the 150 mm, GaN-on-silicon epiwafers is well below 60 μm, the upper limit for high-volume processing

silicon-based IGBT, which combines the ease of charge control with the benefits of conductivity modulated drift resistivity. This is often selected for lower frequency conversion systems such as motor drivers.

Significant engineering efforts over the last three decades have driven substantial progress in the performance of both of these devices – figures of merit have improved by an order of magnitude. But wringing out any further gains in performance is going to be tough and costly. It is likely that efforts could yield an economically feasible factor-of-two improvement in the 30 V FET, and a five-fold gain in 600 – 1200 V silicon IGBTs. But any further advances in power device performance for future electronic loads will need new material technologies, such as gallium nitride. Turning to this wide bandgap semiconductor is very attractive because it also enables a 50 to 90 percent reduction in both the size and the weight of conversion subsystems, thanks to a massive cut in cooling system requirements.

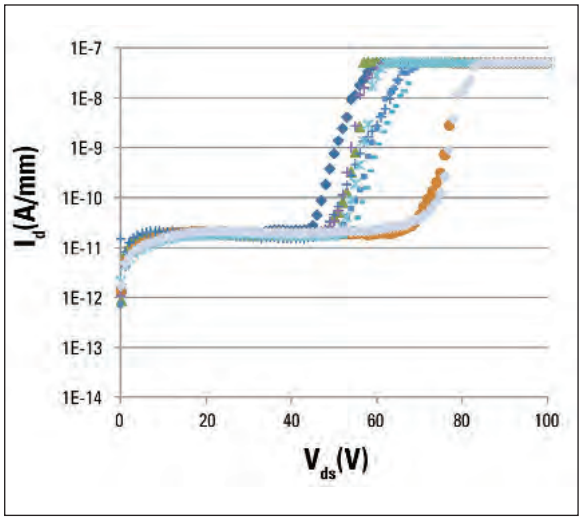


Figure 3: A proprietary insulated gate reduces the reverse-bias drain-leakage current in IR's GaNpowIR devices with a gate length of 0.3 μm. The HEMTs, which have gate-source and gate-drain spacings of 1 μm, exhibit a punchthrough-limited, source-drain breakdown of more than 40 V for a gate voltage of -20V

Although the first GaN HEMT transistor was invented more than 15 years ago by Asif Khan, significant development efforts on practical power devices employing GaN-on-silicon technology are fairly recent. Tremendous progress in this technology is expected over the next 10-20 years, and in just five years figures of merit could improve by an order of magnitude.

Despite all this promise, GaN devices are generally failing to fulfill their commercial potential. That's because they are too expensive to produce, due to the costs associated with substrates, epitaxy, device fabrication, packaging, support electronics and development. The power device marketplace has set a viable, economic-based limit of about $ 3/cm^2 for substrate and epitaxy costs, restricting the choice of substrates to just silicon. Multi-wafer MOCVD tools are essential for providing the required throughput and an acceptable cost-of-ownership, although their current status is quite primitive compared to modern silicon processing equipment.

In addition to realizing low costs for substrates and epitaxial layers, it is imperative to minimize device fabrication costs. To do this, manufacture should employ substrates at least 150 mm in diameter. Selecting such platforms has an additional, significant benefit - widespread availability.

Fabrication of compound semiconductor devices often involves specialized processes such as e-beam and lift-off lithography, and may also include gold metallization steps. Products for military and RF applications can justify the inclusion of these expensive techniques, because the market is willing to accept costs of more than $ 10,000 for finished 100 mm wafers for discrete devices. But these manufacturing costs are incompatible with the far broader power device market.

If power devices based on wide bandgap materials are to displace the incumbents, they must have comparable fabrication costs. Realizing this is only possible by manufacturing devices in volumes comparable to that of silicon devices. In other words, a production throughput of at least 10,000 wafers every week. These volumes must be produced with high yields, using silicon-compatible semiconductor fabrication lines, taking advantage of the current high volume of silicon demand. If these goals are fulfilled, it is possible to tap into today's broad market for power devices that equates to 10 million, 150 mm wafers per year. Success requires significant scalability in device

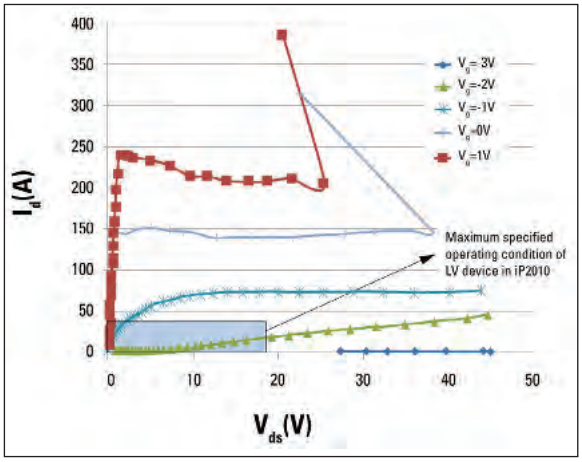


Figure 4: IR's GaN-based power devices intended for 12 V_{in} power conversion applications have a large safe operating area under forward bias.

manufacture, but this is easy to accomplish with existing silicon device fabrication facilities and silicon substrates.

We are adopting all of these measures and using our GaNpowIR platform to manufacture power devices delivering an incredibly high level of performance for their price. By outperforming silicon equivalents in this metric, we are starting to drive market penetration of GaN-on-silicon power devices.

Taking the strain

One of the biggest hurdles to commercialization is the development of cost-effective, high-yield, high-throughput epitaxial processes that are applicable to large diameter silicon wafers. The growth process must address intrinsic mismatches in both the lattice constant and the thermal coefficient of expansion of silicon and GaN. Failure to do this leads to many threading dislocations, plus significant macroscopic film stresses that result in excessive wafer bow and cracking of the film.

Our proprietary film growth process addresses these issues and produces high-quality epitaxial films on 150 mm silicon (111) substrates with a standard thickness of 625 μm. Threading dislocations are significantly reduced, and the dislocation density of 10^9 cm^{-2} in our 2 μm-thick silicon layer predominantly results from edge dislocations. The low density of dislocations, which is comparable to that of GaN films of a similar thickness on SiC, leads to high mobility. Hall mobility measurements indicate that the mobility in the two-dimensional electron gas formed at the interface between the thick GaN buffer layer and the overlying AlGaN barrier layer is often higher than 2000 cm^2/Vs (see figure 1).

High yield manufacturing demands relatively flat wafers for processing lines. The bow of our wafers with 2 μm of epitaxy is less than 20 μm (3 sigma), well below the 60 μm limit for device fabrication (see Figure 2). Many devices can be produced from each wafer, because we can consistently produce truly crack-free material to within 0.5 mm of the wafer edge.

Many GaN devices developed to date suffer from a high leakage current, which stems from the Schottky gates. This leakage - of the order of mA per mm of gate width - is too high for power devices, which typically have an effective gate width of 1 m or so. Such a high leakage causes unacceptable power loss and heating. We have driven leakage currents below 1 μA/mm by employing a proprietary insulated gate construction and very high quality III-N films. This can lead to gate and drain-source leakages of just 10 pA/mm (see Figure 3)

One of the strengths of our devices is their high level of ruggedness in their intended application, initially 12 V to 1 V buck regulators (see Figure 4). The forward-biased, safe operating area for this low voltage power device far exceeds the requirements of the application. These 850 mm gate-width devices have an I_{on}/I_{off} ratio exceeding 10^{10}, which is substantially better than that reported elsewhere for GaN-based devices. I_{on}/I_{off} ratios

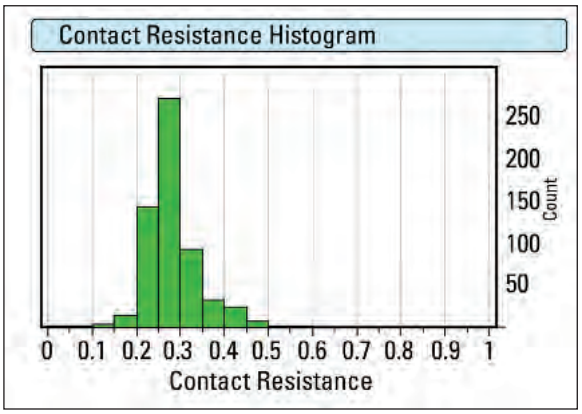


Figure 5: A low contact resistance, which was measured using a standard transmission line technique, ensures high performance for GaN-based power devices operating at relatively low voltages

If power devices based on wide bandgap materials are to displace the incumbents, they must have comparable fabrication costs. Realizing this is only possible by manufacturing devices in high volumes comparable to that of silicon devices, that is production throughput of at least 10,000 wafers every week

of more than 10^8 are routinely achieved for 600 V devices, where I_{off} is measured at 600 V.

A major challenge facing GaN power device manufacturers is the realization of a sufficiently low and controllable source-drain contact resistance. Although this resistance has negligible impact on the overall drain-source resistance of devices operating at 300 V or more, it can play a domineering role in HEMTs operating below 100 V, degrading device performance. In order for these types of devices to be competitive, the contact resistance must consistently be below 0.35 Ω mm. To meet this requirement, we have developed a process compatible with cost-effective, high-volume manufacturing that does not involve gold metallurgy.

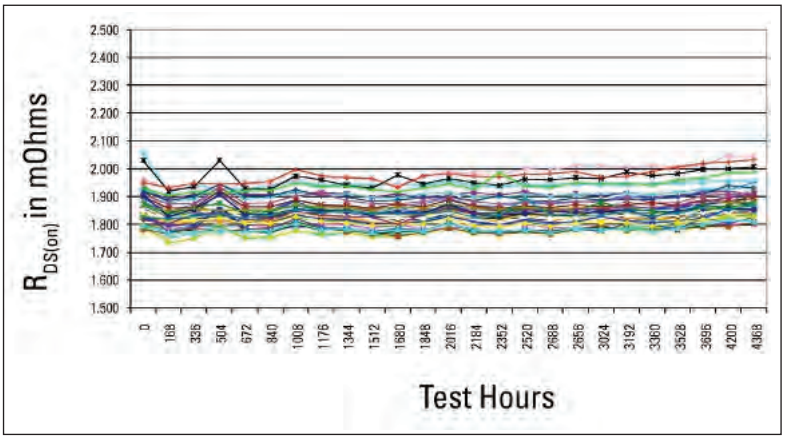


Figure 6: The room-temperature drain-source resistance of IR's power device in its on-state has a high degree of stability over time. Devices with 0.3 μm-long gates with a width of 2.6 m were stressed at 150 °C. Gate and drain-source voltages were −7V and 15 V, respectively

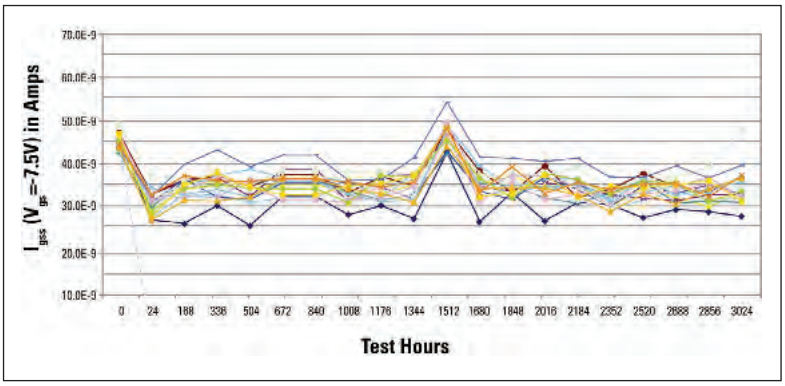


Figure 7: Room temperature gates leakage currents are relatively low and stable, according to tests at -50 V applied to the 8.5 V rated gates. The devices had 0.3 μm-long gates with a width of 2.6 m, and stress was performed at 150°C

Commercially viable, low-voltage GaN devices must also realize effective conduction of the source-drain current from the internal to the external device terminals. We have satisfied this requirement with planarized multi-level metallization, common to silicon ULSI device fabrication. Turning to proprietary, solderable front metallurgy enables production of flip-chip die. This eliminates wire bonding and minimizes other package-related parasitics.

Commercial targets

Profitable manufacturing of large-area power devices requires high yields. In our opinion yields for devices 10 mm^2 in size must exceed 80 percent, a target that we have achieved with our GaNpowIR platform. Such a yield also demonstrates the maturity of our production process.

The other prerequisite to commercialization is the creation of a device with a stable in-circuit performance. The critical figure-of-merit is the drain-source resistance of the device in its "on" state. This shows excellent stability in tests involving accelerated aging (see figure 6). Performance is comparable to that of silicon devices, according to reliability testing over 3 million device-hours.

Other aspects of the device also meet the need for robustness. The gate dielectric shows excellent stability under extreme, accelerated stress conditions (see figure 7); the drain leakage current does not significantly degrade over time; and no physical degradation is observed in the AlGaN barrier layer at the gate edge after several thousand hours of operation. This barrier benefits from the significantly reduced gate-leakage currents resulting from the incorporation of a dielectric at the gate.

This strong set of characteristics gives these devices a great opportunity to help to make cost-effective, significant energy savings in various ways. Customers buying our products manufactured on the GaNpowIR platform can rest assured that they are reliable, stable, and can be produced in high enough volumes to keep pace with demand.

Further reading

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Microsemi ups the power of its SiC transistors

The 2.2 kW static induction transistor developed by **Microsemi** is destined for success. It delivers unprecedented powers and a long lifetime, and it allows UHF radar manufacturers to build systems with far fewer components, say the company's **Mike Mallinger, Bruce Odekirk, Mar Caballero and Francis Chai.**

Designers of defense radar systems are always on the look out for transistors that take power output to a new level. If they adopt such devices into their radar systems, they can increase detection range and improve sensitivity.

At Microsemi, which is headquartered in Irvine, California, we have recently been piquing the interest of these radar system designers with our SiC static induction transistor (SIT) that raises the bar for pulsed output in the UHF band. This device, which we expect to support the next generation of defense radar systems, is in the final stages of qualification and will be in initial production before the year is out. Volume production is slated for early 2011.

The SiC SIT structure is a new technology. So to ensure that the product can be manufactured in high volumes, while always delivering a high-quality performance, we have made significant investment in several areas: wafer supplier qualification; high-power chip design; transistor packaging; transistor pre-matching network optimization; and RF performance characterization and reliability testing. The effort made in each of these areas is detailed below.

We have invested a great deal of time and effort in qualifying multiple wafer vendors. This will allow us to address the high quantity of product required to support volume production of our SiC RF and power switching products. Introducing material analysis procedures has provided confirmation of the quality and the consistency of the epiwafers from each of these suppliers. Routine incoming SiC epiwafer metrology includes cross-polarizer imaging (see Figure 1), AFM surface sampling scans (see Figure 2), and Nomarski microscopy imaging.

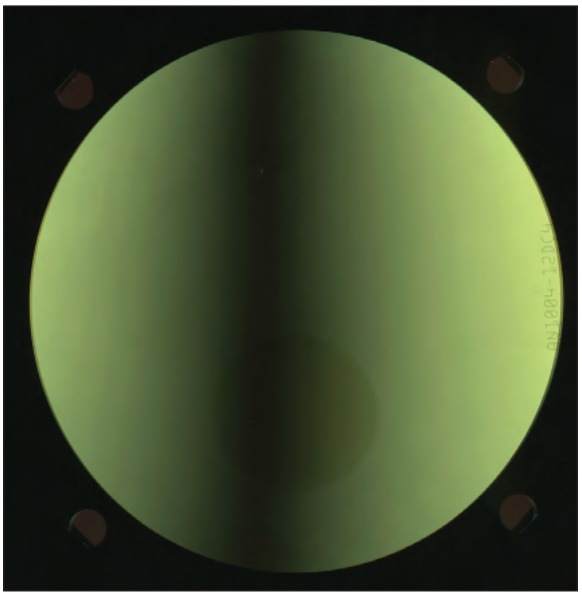


Figure 1. The lack of features in cross-polarized images of the epiwafers sourced by Microsemi indicates the high quality of the material

All these assessments, which can be made on either 3–inch or 4 inch wafers, are recorded via digital data capture. This information can be recalled for reference and analysis. These digital files are frequently compared to both incoming localized laser scattering (LLS) defect maps provided by the epiwafer vendors and final die sort maps.

These types of comparison have proved extremely beneficial: they have enabled us to provide constructive feedback to the epiwafer suppliers; and they have also

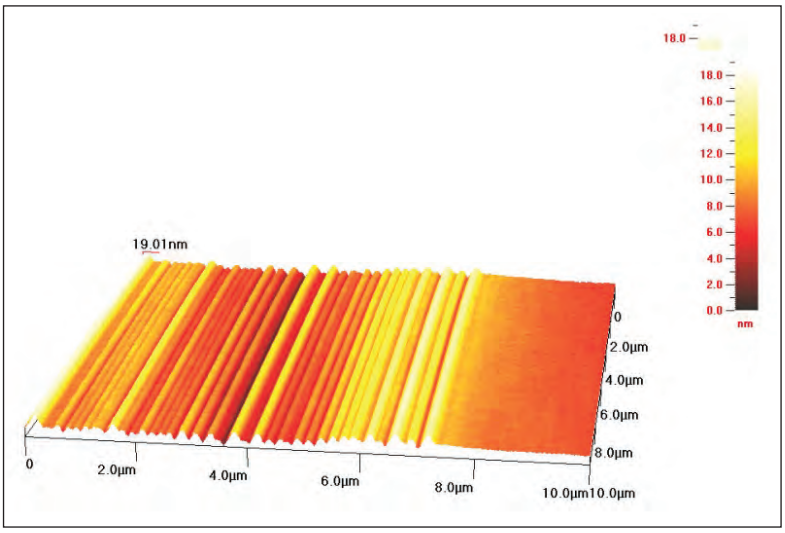


Figure 2. AFM images of Microsemi's SiC epiwafers indicate their low level of surface roughness

guided wafer fab process improvements. Thanks to all this effort we have established sources of material that are prepared to supply our volume production requirements for the next 10 years and beyond.

Within our 4-inch silicon power chip fab in Bend, Oregon, we have created a completely self-contained wafer manufacturing capability. The processes established at this facility include heated implants at up to 1000 °C and implant annealing at up to 1700 °C.

All the tools in this fab that are used for SiC device production are capable of processing both 3-inch and 4-inch SiC. Today all our manufacturing is carried out on the smaller of these sizes, but over the next two years we plan to migrate to the larger format. Our installed 3-inch wafer capacity is capable of supplying all projected radar programs over the next several years. Switching to 4-inch production will more than triple our capacity, and also increase tool redundancy.

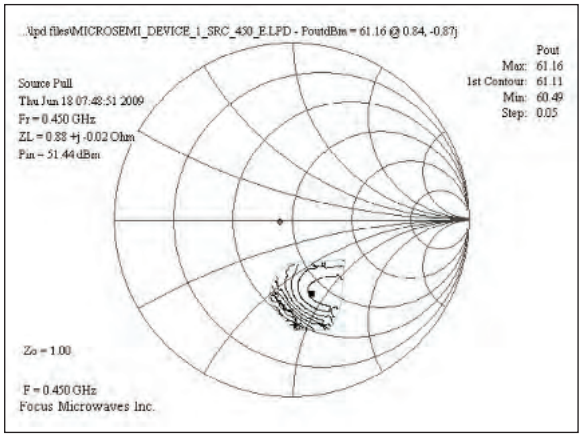
Scaling-up

Our first prototype transistor cell produced only a fraction of the 2kW output power that's possible with our latest product. But this device has been incredibly useful, providing an important building block for the fabrication of our 2.2 kW SIT. It has enabled us to establish our design rules, such as transistor channel width and length. These critical design rules have been subsequently validated by hooking up real devices with probes and extracting their electrical parameters. Devices that we have created adhere to these rules, indicating optimization of the fabrication processes and unit cell RF power performance.

To realize the high output powers demanded by applications such as pulsed radar, we have had to significantly up-scale the transistor cell size. Scaling is not trivial, because increasing chip power density does not necessarily result in amplifier output power scaling. That's because thermal issues can hamper performance, which are related to the extremely high output powers produced by the chip.

However, by optimizing chip geometry we have been able to scale the device without any loss in performance. This has been realized by first performing experiments with design factors such as transistor cell size, chip geometry and chip thickness. Evaluating these results has enabled us to build devices that produce output powers approaching the theoretical transistor periphery-scaling factor.

All the customers that we are targeting with our 2kW transistors demand operational lifetimes in excess of 30 years. To meet this requirement we house our SIT in a hermetically sealed package, use gold-wiring throughout, and employ package plating and a gold-tin seal. History is on our side, because this approach has a proven reliability, having already served successfully in many highly demanding applications. However, due to the substantial increase in overall RF power and power dissipation, a new design is being implemented. This includes qualification of multiple suppliers. Our 2 kW device realizes such a high output power by combining several high-power transistor, multi-cell chips. To ensure the highest levels of repeatability and consistency in RF



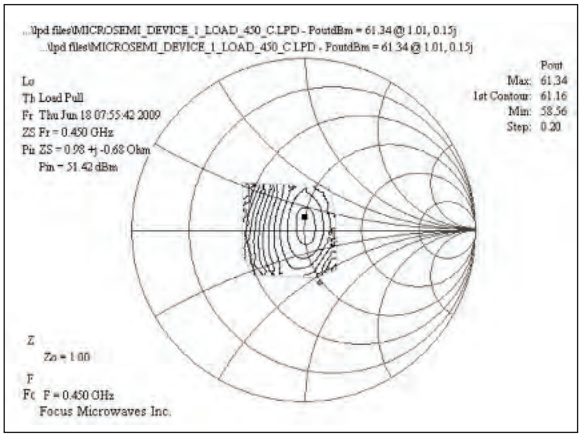
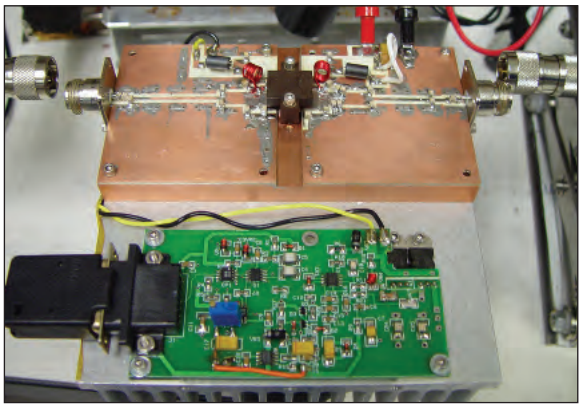


Figure 3. Source pull (left) and load pull (right) analysis offers a quick way to determine the optimum input and output device impedance over the band of interest



A "source pulser" board is used with an RF test fixture to control the DC and RF behavior of the SiC SIT

performance, highly precise automated die-attach and wire-bond machines are used in production.

Driving the SIT

The SIT is designed to operate at full power over 406-450 MHz, a lower spread of frequencies within the UHF band. To do this it should be biased in "class AB, Common Gate" and run with a drain supply at 125 V. The terminal impedances are only a few Ohms, so an external matching network is needed to transform the impedance from the transistor up to 50 Ohms for device characterization and use. Fixture optimization includes a complete "load pull" analysis of the transistor, which can confirm that the matching network is designed for the best overall performance.

One of the benefits of load pull analysis is that it yields valuable information on device performance. It can quickly determine the optimum input and output device impedance over the band of interest, and rapidly deliver a trade-off analysis on critical RF performance parameters. We use these load pull impedance values as a target for the design of the input and output circuit-matching networks.

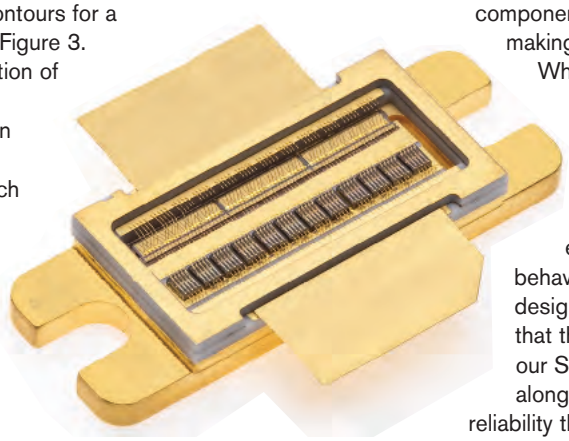
The typical input and output contours for a single frequency are shown in Figure 3. These contours offer an indication of how sensitive the device is to impedance changes. We obtain contours and optimum input/output impedance for each frequency across the band of interest. Our SiC SIT is a depletion mode device. Consequently, application of a gate bias is needed to turn the product 'off' before applying the drain bias. To aid the driving of the SIT, we include a 'source pulser' design with the RF test fixture to control the entire DC and RF functioning of the device. This new circuit technology will hopefully help to speed up our customer's implementation of our products into their power amplifiers.

The primary function of the source pulser is to set an appropriate bias level for the device. The pulser's main component is a high-speed analog switch that toggles between an off-voltage of +15 V and an on-voltage of 3-5 V. The bias switching parameters are synchronized with the RF pulse.

When we start to manufacture our SIT in full production, we will add a bias sequence feature to ensure a proper power-up sequence during RF tests. Future efforts in this area may include the development of highly compact and efficient ASIC versions of the pulser assembly. Our SIT is designed to deliver incredibly high, pulsed powers. To verify that every product is capable of delivering this level of performance through its lifetime we will subject every transistor to a full functional set of tests prior to shipment. Due to the high voltages and currents associated with the driving of the device, the test procedure accommodates the latest operator safety procedures and power handling.

One of the strengths of our SIT is its ability to operate over a wide range of conditions, from very high peak powers at medium pulses to very long pulses at high duty factors. Thanks to its versatility of driving conditions, the SIT can support a wide range of applications. So to help potential customers evaluate what our SIT can do for them we have characterized this transistor for operation at conditions beyond those listed on the standard data sheet. To do this, we have made substantial investments in RF metrology and also developed highly automated test software. The reward of these efforts is the characterization of our products over multiple test conditions with very high levels of accuracy and repeatability. We believe that our SIT will have a massive impact on the design and build of the next generation of radar systems, and also their operational life, which is typically more than 35 years. We expect uptake of our SiC devices to be high. They can slash the number of components that a radar system needs, making it far smaller and cheaper. What's more, the introduction of SiC into radar systems can cut maintenance costs and greatly expand operating life. Making a transition to a new product always involves some effort, because new devices behave differently and require new design rules. But we are convinced that this effort is justifiable, because our SIT offers great performance, alongside the consistency and reliability that designers of radar system are looking for.

Microsemi has a Centrotherm HV 100 high temperature implant anneal system in its power chip fab in Bend, Oregon. This tool is capable of operating at up to 1700°C



Left: Microsemi's SIT, which is shown with the lid off, is shipped in a hermetically sealed package. Gold wiring is used throughout

Inside CIGS Solar Panels

The battles in the solar industry at present are typical of an emerging industry as companies compete for market share as well as touting their technology as the answer to the industry challenges. But what is the true state of solar technology and how does it stand up to some objective observation. **St.J. Dixon-Warren and Tim White of Chipworks** discuss their findings when they looked under the hood of CIGS Solar Panels.

The photovoltaic industry seems at the moment to be in one of those knock-down, drag-out contests typical of the start-up phase of a disruptive technology. Not just the business, but also the variety of technologies themselves – monocrystalline silicon versus polycrystal, bulk materials versus thin film, thin-film silicon versus CdTe (cadmium telluride) versus CIGS (copper-indium-gallium selenide).

At present, crystalline silicon panels account for the vast majority of the market; however, they remain expensive and are unlikely to ever be able to compete with electricity from the grid without subsidies. Thin-film panels have the potential for lower cost production, since the active layers are deposited directly onto molybdenum coated glass.

Vacuum deposition, including co-sputtering and co-evaporation, and non-vacuum based methods are possible, including electroplating. Sputtered films can be either deposited in layers and then alloyed through thermal annealing cycle or co-sputtered using a mixed target.

Chipworks has recently completed a detailed structural analysis of two commercially available CIGS panels, namely the Wurth WSK0020 and the Avancis PowerMax 100 FB. Broadly speaking the panels have a similar structure. They are both made as a sandwich of layers between two glass sheets. The bottom sheet provides a substrate and the top provides protection from the external environment. The optically-active CIGS stack is deposited on the bottom glass substrate. The CIGS stack is comprised of a bottom molybdenum layer, a copper-indium-gallium-selenide (CIGS) layer, and a top aluminum-doped ZnO transparent conductive oxide (TCO) layer.

The bottom molybdenum layer is the cell anode and helps reflect any unabsorbed light back into the active layers. The top aluminum-doped ZnO layer, as well as being the electrically conductive cell cathode, is transparent to allow the sunlight to penetrate into the CIGS layers. Scribe lines are cut into the layers of the CIGS stack to form the individual cells. A layer of transparent polymer material is applied over the CIGS stack followed by the top glass.

Figure 1 is a schematic diagram of two individual cells in a typical CIGS solar panel. It turns out that, in terms of light to electricity conversion efficiency, the optimum width of CIGS cells is around 5 to 10 mm so panels are typically formed using banks of such cells in series. Scribe lines, denoted P1, P2, and P3, are used to create the interconnect structures that form the series connections. Electrical anode and cathode connections are then formed at each end of the series of cells.

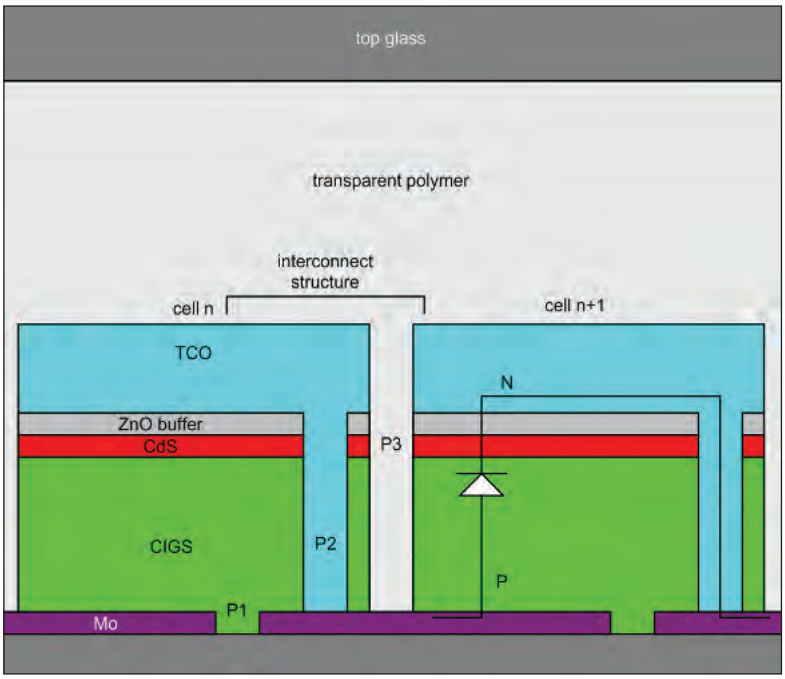


Figure 1 CIGS Solar Panel Structure

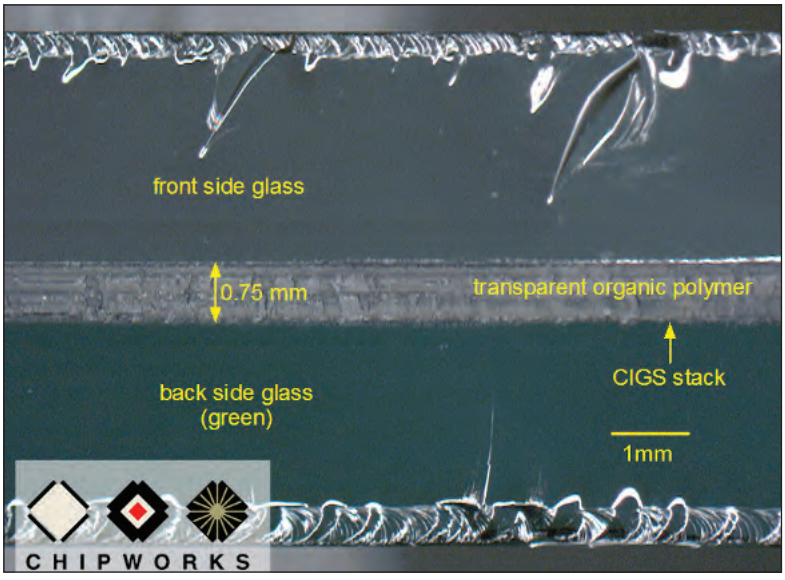
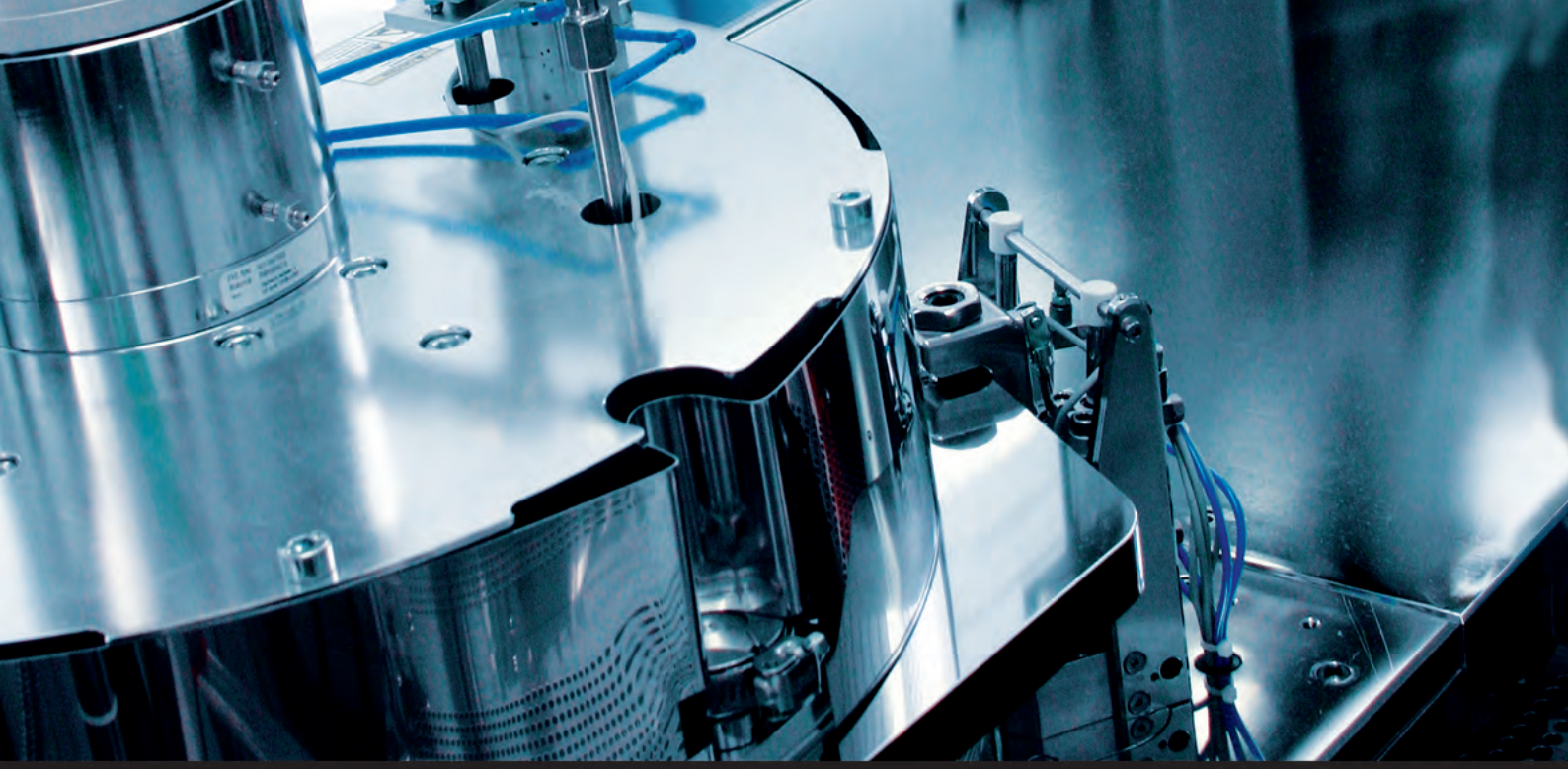


Figure 2 CIGS Solar Panel Cleaved Edge



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While the essential nature of the CIGS cells was the same, Chipworks' analyses of the two competing panels inevitably found differences in the details of their structure, including variation in the layers used for the optically active CIGS stack, the materials used for the transparent polymer layer, and the methods of contacting the active layers

The PN junction apparently forms near the top surface of the CIGS layer as a result of surface segregation of indium rich materials, such as $CuIn_3Se_5$, causing the conductivity type to invert from P-type to N-type, and thus forming a PN junction.

The molybdenum film provides the interconnection and the anode back contact for each cell while the N-type, ZnO:Al TCO is the cathode contact. A layer of CdS and an undoped ZnO buffer layer are often used to reduce lattice mismatch between the CIGS layer and the TCO.

The cleaved edge of one of the CIGS solar panels recently analyzed by Chipworks is shown in Figure 2. The bottom glass is usually (cheap, easily available) soda-lime window glass and appears green in color, due to the presence of sodium. Sodium diffusion into the stack from the glass has been shown to improve cell performance.

Figure 3 shows a cross-sectional view of a P1 scribe line, which provides the electrical isolation between anodes of adjacent cells, as shown schematically in Figure 1. The TCO, CIGS and Mo layers are easily distinguished in the cross-section. The Mo layer was likely laser scribed, which results in a thickening for the layer near the edges.

A detailed SEM cross-section of the CIGS stack is shown in Figure 4. The top surface of the CIGS layers has a very rough morphology, which is partly re-planarized by the TCO. The CdS and ZnO buffer layer were also resolved in the analysis. The compositions were determined by SEM and TEM-based energy dispersive X-ray analysis.

While the essential nature of the CIGS cells was the same, Chipworks' analyses of the two competing panels inevitably found differences in the details of their structure, including variation in the layers used for the optically active CIGS stack, the materials used for the transparent polymer layer, and the methods of contacting the active layers. Such is the stuff of competition; as with the broader photovoltaic market, cost per installed watt will be the final arbiter.

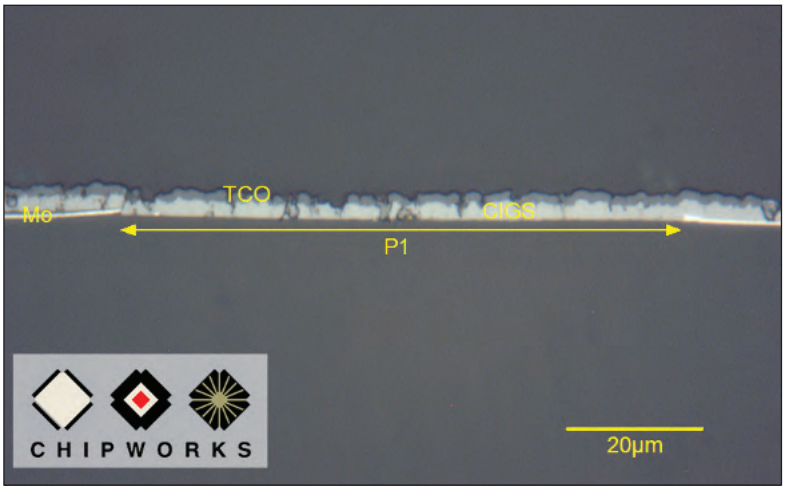

Figure 3. P1 Scribe Lane

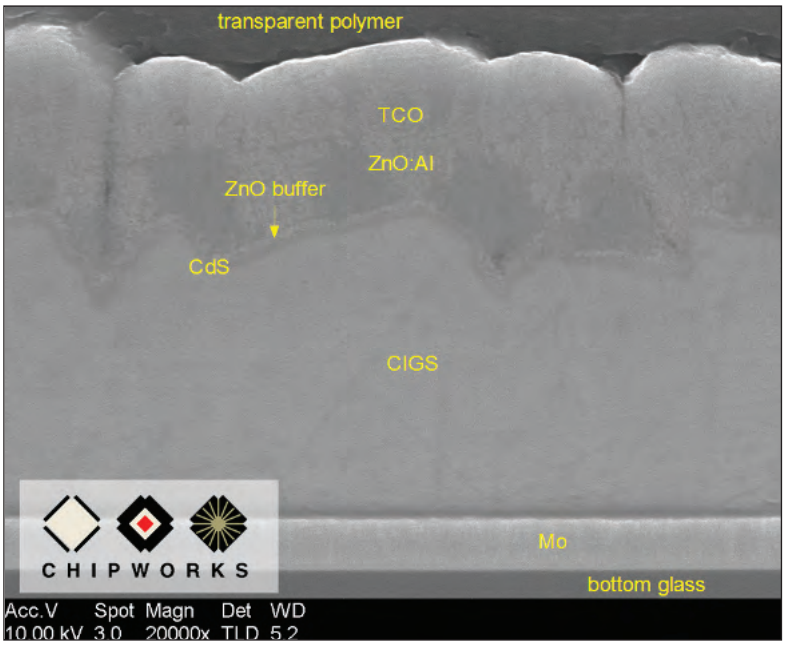

Figure 4. CIGS Stack

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TriQuint ups GaN-on-silicon HEMT efficiency

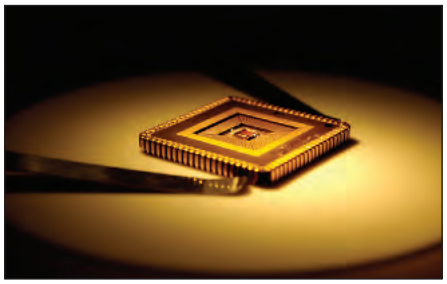
TriQuint claims that it has broken the power added efficiency (PAE) record for GaN-on-silicon HEMTs operating at 10 GHz.

Transistors fabricated in the labs of this US chipmaker have delivered a PAE of 65 percent, a value that is very similar to that produced by the company's commercial, state-of-the-art process on the superior platform of SiC.

Engineers at TriQuint point to improvements in epitaxy and device architecture for closing the PAE gap between GaN HEMTs on silicon and on SiC.

"Epitaxial material was designed to maximize the drain-source current while keeping a low leakage current and a high breakdown voltage," revealed corresponding author Deep Dumka. "Buffer growth was optimized to minimize RF loss."

Dumka told *Compound Semiconductor* that the device fabrication process was similar to



the company's production process for GaN-on-SiC HEMTs. The GaN-on-silicon HEMTs were created by first growing a $GaN/Al_{0.26}Ga_{0.74}N/GaN$ stack on 4-inch silicon (111). Reactive ion etching (RIE) created AlGaN/GaN mesa patterns, and evaporation and rapid thermal annealing formed Ti/Al-based ohmic contacts.

E-beam lithography, a RIE-based low-damage nitride-etch process and evaporation of a Pt/Au metal stack defined 0.25 μm, T-shaped gates that inherently formed a field plate. A second field plate was added on top via optical lithography and Ti/Pt/Au metallization.

This pair of field plates cuts the peak electric field between drain and gate, leading to improved HEMT performance at high voltages.

At an input power of 20.8 dBm, TriQuint's GaN-on-silicon transistor delivered a peak PAE of 65.6 percent, an output power of 33.9 dBm (6.1 W/mm) and a gain of 13.1 dB. This HEMT is also capable of producing 34.5 dBm (7.0W/mm), but this increase in output power comes at the expense of a reduction in PAE to just over 60 percent.

TriQuint's GaN-on-silicon process is being developed with commercial interests in mind. "However, there is no firm date yet for production transfer of this process, since our GaN-on-SiC technology is meeting present demands" says Dumka.

D.C. Dumka *et al.* Electron. Lett. **46** 946 (2010)

UCSB reveals green laser secrets

Engineers at the University of California, Santa Barbara, (UCSB) have shown that AlGaN barriers hold the key to the growth of a high-quality active region for a green semi-polar laser.

The team's investigation focused on devices grown on the $(20\bar{2}1)$ plane of GaN, a cut that Sumitomo employed last summer to win the race for the first green laser.

While Sumitomo has said very little about the architecture of its active region, UCSB, in partnership with substrate supplier Mitsubishi Chemical, is now revealing some important findings about this light-emitting region on semi-polar GaN .

This partnership's recent study involved a comparison of the material quality and device performance of green lasers built with three different types of active region.

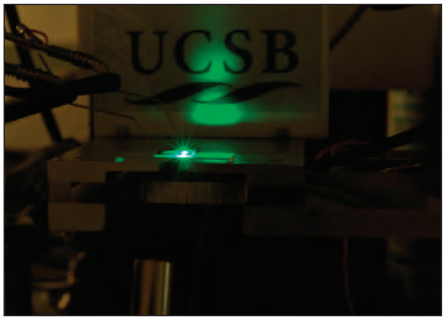
Variants fabricated with 10 nm-thick barriers made from GaN, $Al_{0.05}Ga_{0.95}N$ and $In_{0.03}Ga_{0.97}N$, all produced a spontaneous peak emission wavelength between 520 nm and 540 nm.

All three laser designs featured 4.5 nm-thick InGaN wells, a 1.2 mm-long cavity and high-reflectivity, distributed Bragg reflectors. These mirrors that were formed by sputtering provide reflectivity at the front and rear facets of 97 percent and 99 percent, respectively.

Hioraki Ohta from UCSB admitted that the use of AlGaN causes inferior optical confinement due to its lower refractive index. "However, material quality, and in turn internal quantum efficiency, was much better."

Fluorescence microscopy exposed the superior material quality stemming from the AlGaN barrier. Structures with GaN and InGaN barriers featured many non-luminescent triangles with sides of 100 μm or more, which are presumed to contain many non-radiative recombination centers. These triangles were absent in the structure with AlGaN barriers.

A laser with the AlGaN barrier produced 516.3 nm emission when driven in pulsed mode with a 0.01 percent duty cycle.



Researchers at UCSB have fabricated an 8 mW laser emitting at 516 nm. Credit: UCSB

Threshold current density was 30 kA/cm^2, and the device delivered 8 mW at a drive current of nearly 1A and a 40 V operating voltage.

Ohta says that the team will now focus on further improvement of the active region through optimization of the structure and the growth process.

Y.-D. Lin *et al.* Appl. Phys. Express **3** 082001 (2010)

Novel re-growth sidesteps AlGaAs exposure

Researchers at the University of Sheffield, UK, have developed a technique for making GaAs-based lasers that circumvents re-growth on exposed AlGaAs surfaces. Avoiding re-growth on this ternary is highly desirable, because it is difficult to adequately planarize AlGaAs without degrading the corrugated GaAs grating needed to form single-wavelength, distributed feedback lasers.

The UK team fabricates its quantum well lasers by re-growth of AlGaAs on patterned InGaP. Although this is not the only way to shun re-growth on exposed AlGaAs, it has several major advantages over two rival techniques developed several years ago.

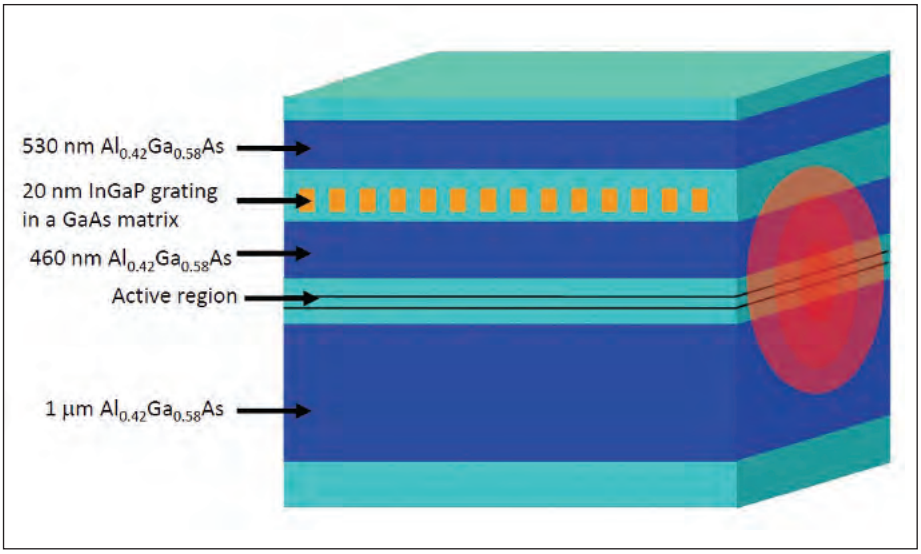
One of these alternatives - which is associated with laterally loss-coupled gratings and aluminum-free structures - involves the formation of a metal or etched grating after the etching of a laser ridge. Low yields result, prohibiting volume manufacturing. InGaP overgrowth on patterned GaAs is the other alternative. But this hampers design freedom, because InGaP is only lattice-matched at one stoichiometry.

The team from Sheffield avoids all these issues by employing an InGaP/GaAs grating layer in conjunction with an AlGaAs cladding. This cladding is spared from exposure to air during patterning, etch and re-growth of the grating, thanks to the combination of selective etching and the insertion of a protective GaAs layer beneath the InGaP. A further benefit of this novel approach is the opportunity to place the grating as far as 450 nm from the active layer, due to the high refractive index contrast between InGaP and GaAs. This should improve reliability and performance, because the re-growth interface can be located within the heavily doped p-material and well away from the active region.

Laser fabrication began with MOCVD growth of device epistructures on (110) n-doped substrates. The planar wafer, which features two InGaAs quantum wells, was patterned with a 148 nm period grating that had been defined in PMMA by e-beam lithography. A combination of inductively-coupled plasma and wet etching removed GaAs and GaInP layers, and after cleaning in dilute hydrofluoric acid, high-quality GaAs and AlGaAs layers were deposited on top of the structure.

Ridge lasers with a 3 μm width and a 1 mm-long cavity produced 7.9 mW at a 62 mA drive current. The corresponding threshold current density was 2 kA/cm^2, and the dominant, 1006 nm mode had a side-mode suppression ratio of 30 dB.

B.J. Stevens *et al.* Electron. Lett. **46** 1076 (2010)



Researchers at Sheffield University, UK, have developed a laser fabrication process involving re-growth of an AlGaAs upper cladding layer on patterned InGaP

Electron blocker boosts brightness in wide-well LEDs

Engineers at Chang Gung University, Taiwan, have almost doubled the external quantum efficiency (EQE) of LEDs featuring relatively wide wells. This gain resulted from switching the electron-blocking layer from a superlattice structure to a 20 nm thick AlGaN layer.

The team's interest in LEDs with wider wells – known as double heterostructure LEDs – was sparked by efforts at Philips Lumileds, which showed that this design can combat droop, the fall in efficiency as drive current is increased. Lumileds claims that Auger recombination – the non-radiative interaction between an electron, a hole and a third carrier – is the main cause of droop. Auger rates can be squashed with a wider well that cuts carrier density in the active region.

The team at Chung Gung University has compared the performance of two LED structures producing peak emission at 420-440 nm. The control sample features an active region with 2 nm-thick GaN barriers and 9.5 nm-thick $In_{0.08}Ga_{0.92}N$ wells, plus a p-type electron blocking structure comprising 20 periods of 2.4 nm-thick $Al_{0.2}Ga_{0.8}N$ and 2.8 nm-thick GaN.

The researchers compared the EQE of this LED to that of a similar device with a 20 nm-thick $Al_{0.25}Ga_{0.75}N$ electron-blocking layer inserted between the active layer and the superlattice.

EQE of the control sample hit 4.6 percent at 100 A/cm^2 and fell to 2.7 percent at 200 A/cm^2. In comparison, the LED with the AlGaN electron-blocking layer produced a peak EQE of 9.5 percent at 65 A/cm^2, falling to 5 percent at 200 A/cm^2.

The researchers postulate that insertion of the AlGaN electron-blocking layer that leads to higher EQE impacts droop via changes in either carrier leakage, hole injection efficiency or polarization mismatch.

M.-J. Lai *et al.* Appl. Phys. Express **3** 072102 (2010)

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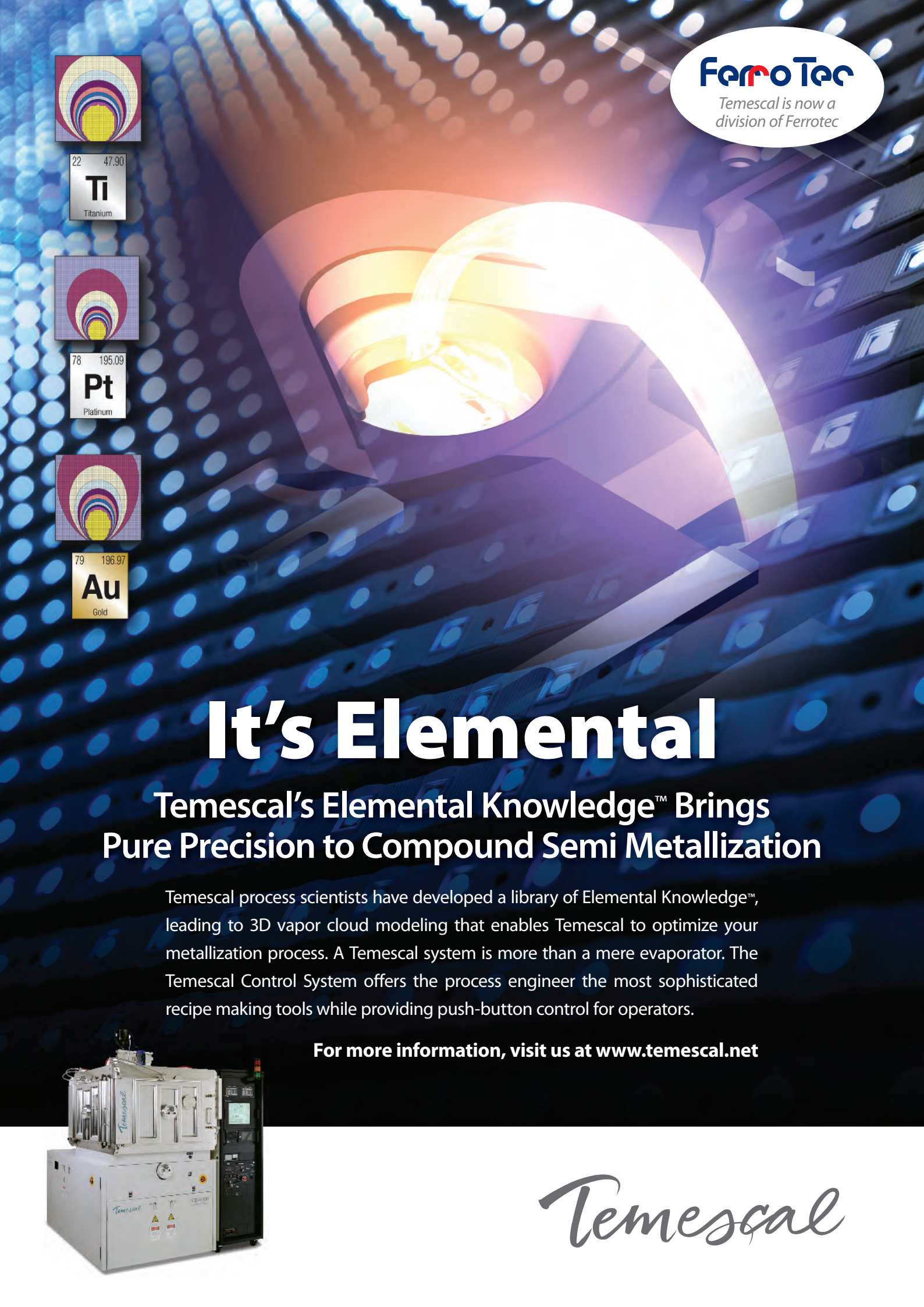

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