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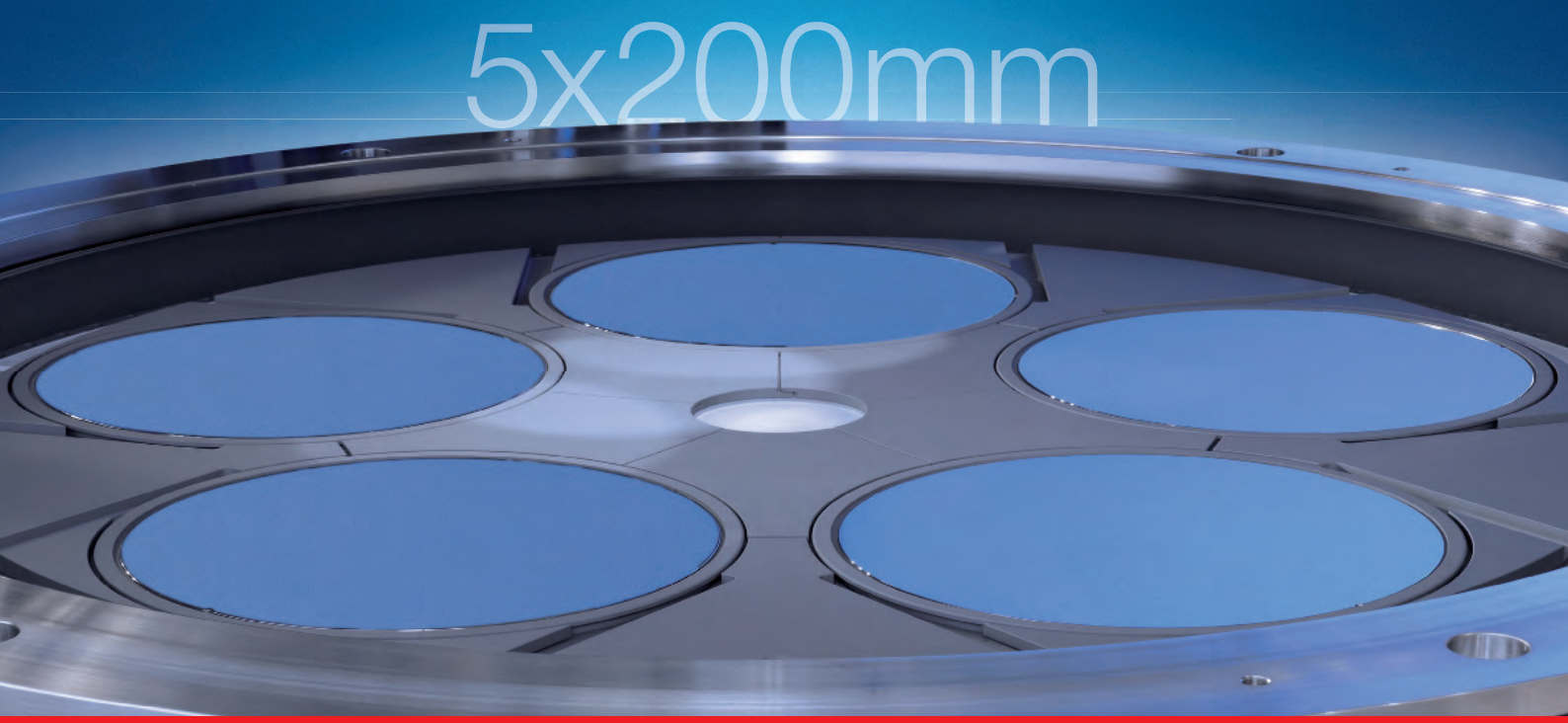
Moore's Law

Turbocharging channels with III-Vs

AIXTRON

200mm GaN-on-Si Batch Reactor



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ALWAYS ONE STEP AHEAD

editorial view

by Dr Richard Stevenson, Editor

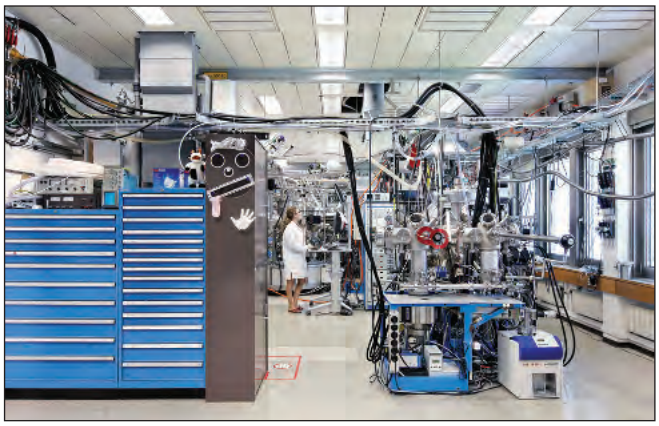
Finding favour with the foundries

IT'S COMMON KNOWLEDGE that silicon CMOS is struggling to keep pace with the rate of progress suggested by Moore's law. Maintaining efficiency gains that have traditionally come from geometrical scaling is getting tough, and it will require the introduction of higher mobility materials into the channel.

When this will happen is not set in stone – a best guess is the 7 nm node – and it is also unclear how silicon foundries will manufacture this new form of IC that will probably sport a pFET based on germanium and *n*-type cousin built from InGaAs.

One way to make such a chip is to turn to a technology known as aspect ratio trapping: trenches are etched in the silicon wafer, before being filled with high-mobility material that forms the channel. This approach addresses the problem of defects formed by lattice matching – imperfections propagate in the direction of a crystal plane before terminating at a trench wall.

It will be interesting to see if foundries go down this trench-filling route by investing in new tools and introducing new deposition processes. After all, they may prefer an alternative way forward – pioneered by IBM – that would ultimately lay many of the new manufacturing challenges at the door of substrate makers. IBM's approach, described in detail in the feature "Turbocharging channel with compounds" (see p30), is to begin with an engineered wafer featuring two very thin high mobility layers: one is a III-V material and the other is an excellent hole



conductor, such as SiGe or germanium. A thin insulating layer separates these two.

Strengths of this technology include an insulator beneath the III-V that cuts leakage currents from source to drain. In addition, because the high mobility materials are present across the entire wafer, circuit designers have more freedom over the placement of their transistors.

So will this wafer-based method catch on? That's hard to say. But it's certainly an interesting option that I'll be keeping my eye on.

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How quickly can LED chipmakers trim the cost-per-lumen and unlock a revolution in solid-state lighting?

Does the future for triple-junction solar cells lie in space or on the ground?

What devices can 'green' optical networks?

Are III-Vs the logical choice for next-generation microprocessors?

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Volume 20 Issue 1 2014

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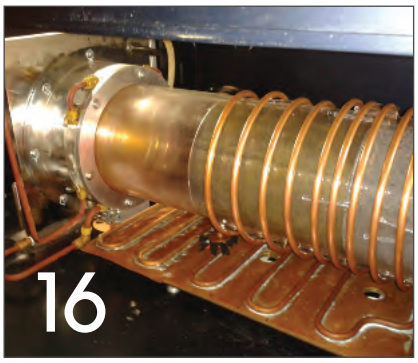
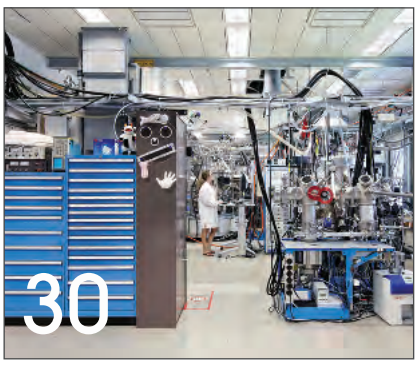
CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

features





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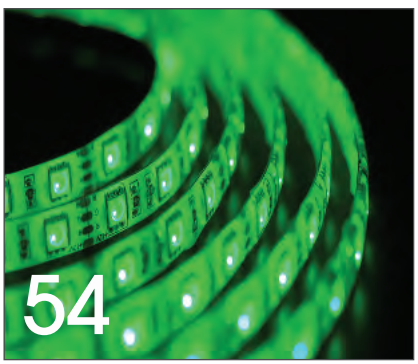
news analysis

research review



Infinera InP PICs to be used in several Telstra networks

INFINERA AND TELSTRA have announced the upgrade of multiple ultra-long haul submarine cable routes, optimising capacity and providing scalability and reliability on key routes of Telstra's network.

The Infinera Intelligent Transport Network will enable Telstra to quickly deploy 10G, 40G and 100G Ethernet and OTN services on: Telstra Endeavour - a 9,124 kilometre submarine cable connecting Sydney and Hawaii; Telstra's Designated Fibre Pair on the Asia America Gateway (AAG) submarine cable connecting Hawaii and California; Reach North Asia Loop (RNAL), which spans 9,000 kilometres to connect Hong Kong, Taiwan, Japan and South Korea Darrin Webb, Chief Operating Officer for Telstra Global, says, "As a trusted network supplier, our job is to ensure we are adapting and creating capacity where it is required. Demand for network services in the Asia Pacific region is growing exponentially and the addition of Infinera's DTN-X platform means we will be well placed to meet the speed and capacity needs of our customers."

"We are continually developing our network to meet customers' requirements and this is just one of the projects we are working on to ensure our network is always growing, improving and providing world class services," adds Webb. David Welch, Infinera CTO, Co-Founder and President, says, "As global businesses turn to cloud-based offerings, we're seeing increasing demand for reliable, global connectivity.

We are delighted to build on our existing relationship with Telstra Global to deploy an Intelligent Transport Network across these major submarine routes.

"With an Infinera Intelligent Network deployed across Endeavour, AAG and RNAL, Telstra can deploy highly reliable, differentiated services to their customers while reducing capital and operating costs through scale, multi-layer convergence and automation. Telstra Global's deployment is a great example of how long-haul super-channels with SD FEC are accelerating the pace of global communities."

The Infinera DTN-X is designed to scale without compromise to enable future upgrades to terabit super-channels and Terabit Ethernet.

The DTN-X converges five Terabits of non-blocking OTN switching into the same platform, resulting in more efficient network utilisation when compared to conventional WDM architectures.

Intelligent software combined with this converged platform automates manual operations to lower operational costs and enable faster service delivery.

Telstra Global provides innovative and flexible global communications services and solutions for organisations looking to maximise the benefits of globalisation, particularly across growth regions such as Asia, whilst driving sustainability and enhancing business agility.

Together with its offshore subsidiaries and international investments, Telstra Global serves companies spanning Asia Pacific, EMEA and the Americas. It operates award-winning networks which are amongst the largest and most diverse in Asia Pacific. It has licences in Asia, Europe and the US and facilitates access to over 1,900 PoPs in 230 countries and territories across the globe.

Anadigics' InGaP technology used in GALAXY Trend 3

ANADIGICS is shipping production volumes of its AWT5001 and AWT5008 ProVantage power amplifiers (PAs) to Samsung Electronics for the new GALAXY Trend 3.

The ProVantage solutions leverage Anadigics' InGaP-Plus technology to space-saving integration and lower overall system cost.

The GALAXY Trend 3, powered by ProVantage PAs, features a 4.3-inch display, dual-core 1.2 GHz processor, and Android 4.2 Jelly Bean operating system.

"We are very pleased to be powering the new GALAXY Trend 3 by Samsung Electronics," says Jerry Miller, senior vice president of Cellular Products at Anadigics. "Our ProVantage solutions deliver outstanding value by providing a best-in-class combination of high power mode efficiency, linearity, and reduced system costs.

With a complete portfolio of industry-leading solutions we continue to help Samsung bring to market a diverse set of mobile devices that target a wide range of segments."

Anadigics ProVantage power amplifiers help extend battery life by offering three selectable bias modes that optimize efficiency for low, medium and high output power levels, as well as a shutdown mode with low leakage current.

These power amplifiers are also designed for use with an external switch mode power supply (SMPS), in applications using average power tracking (APT), to further increase efficiency and reduce current consumption at low and medium operating powers.

Firecomms unveils green transmitter

FIRECOMMS has announced the availability of its 530 nm DC-1 Mb RedLink(R) transmitter for applications requiring extended link lengths over Plastic Optical Fibre (POF).

Operating in the green spectrum at 530nm, the new FT01MHNG transmitter exploits one of the lower attenuation windows of POF. At 0.1 dB/m, the attenuation of the FT01MHNG is considerably lower than that of traditional POF transmitters that operate in the red spectrum with an attenuation of approximately 0.2 dB/m.

These lower attenuation characteristics of the FT01MHNG transmitter make it possible to implement POF links up to 150 m or even 200 m where traditionally link lengths have been limited to 50 m.

Ideally suited for sensing, CANbus/ RS485/RS232 links, gaming, Smart Meter or other industrial command and control applications, the FT01MHNG transmitter opens up new possibilities for the equipment designer to replace more expensive silica-based solutions with POF, remove repeaters which are no longer needed, and implement new designs requiring galvanic or optical isolation where costs or distances have been previously prohibitive.

"Firecomms, a world leader in the research and development of light sources for POF, has pioneered the development of Resonant Cavity LEDs (RCLED) for the past decade," says John Lambkin, Firecomms CTO. "This announcement of a 530 nm based transmitter using extremely rugged InGaN semiconductors is another example of Firecomms' commitment to innovation and investment in our RedLink product line."

Firecomms has now completed a full qualification of these devices verifying

how the wavelength and output power remain remarkably stable over the entire industrial temperature range of -400˚C to +850˚C, and demonstrating their suitability for the most demanding of applications.

Link tests performed using this new transmitter with the Firecomms FR01MHIR receiver have shown transmission distances of up to 200 m depending on actual throughput.

Epistar unveils efficient infrared LED

LOTS OF FORWARD-LOOKING technologies have been well developed and now applied to LED chip production. These include novel transparent conductive thin films, compound mirror structures, and new EPI structure designs for reducing the absorption of light. Recently, Epistar Lab claims to have made an amazing improvement on the infrared products and believes it has set new records in the LED industry.

According to latest data, the infrared product SFPN42 (chip size 1 x 1mm^2) achieved wall plug efficiency of 75 percent with an operating current of 40mA and of greater than 70 percent at 350mA; the power even exceeds 1W and has reached 1027mW with the operating current of 1A. Such an impressed efficiency development has made LED chips more energy saving and eco friendly.

Now the infrared products are mostly adopted in the security monitor, smart touch panel and wireless communication systems. In the future, Epistar wants to use these products in other high potential markets to keep the competitive strength of its customers.

MEI enters Taiwanese market with advanced etch tool order MEI Wet Processing Systems and Services has received an order from a Taiwan based customer for its Advanced Etch Solution.

The tool is based on MEI's Revolution Wet Processing System, a semi-automated rotary wet processing system designed for batch wet processing (etch or solvent) for semiconductor and MEMS (micro-electromechanical systems) applications.

The Advanced Etch wet bench will be used for copper etch and titanium etch wet chemical processing of 200 mm compound semiconductor or MEMS wafers.

"This is a prime example of the Advanced Etch applications market that MEI specialises in supporting," says Ed Jean, MEI's Sales Manager.

"Most wet process equipment suppliers tend to focus on either single wafer processing or generic equipment sales. There is a real need for semiconductor processing solutions that focus on challenging applications solutions, and MEI Wet Processing Systems and Services is meeting these specialised application needs, including proprietary Advanced Etch, Gold Etch, InGaP Etch and patented Metal Liftoff solutions." Founded in 1990 and based in Albany, Oregon, MEI Wet Processing Systems and Services LLC, is a wet processing equipment and service company serving the semiconductor, MEMS, solar, and high technology industries.

MEI's specialties include patented solutions for wet processing applications, automated and semi-automated wet process systems and services, linear and rotary wet benches for the semiconductor and material processing industries, automated chemical delivery systems and control automation software.

Soitec secures €21.3m funding for R&D

THE EUROPEAN COMMISSION has decided that the aid granted by France to the Soitec group to help it conduct the Guépard research and development project complies with the EU rules on state aid. This project is aimed at developing a new concentrated photovoltaic (CPV) technology. The aid addresses a genuine market failure without unduly distorting competition.

Commission Vice-President Joaquín Almunia, who is in charge of competition policy, says, "EU state aid rules encourage innovation and allow public aid to be targeted on projects that contribute to European growth and competitiveness. The Guépard project is a very good example of this: it will develop a high-efficiency photovoltaic cell that will not only contribute to making solar energy more attractive but also provide a credible technological alternative to the European photovoltaic sector, which has recently been destabilised."

At the end of the Guépard project, Soitec will have produced a high-efficiency III-V multi-junction CPV cell.

CPV cells work by concentrating sunlight before transforming it into electrical energy. They are potentially much more efficient than today's silicon or thin film photovoltaic cells at converting solar energy. The Guépard project will be carried out in cooperation with an SME (InPact) and a research institution (CEA-LETI). The lead player, Soitec, will receive €21.3 million in state aid: €5.9 million in subsidies and €15.4 million in reimbursable advances.

The commission examined the compatibility of the aid in relation to its guidelines for state aid for research and development and innovation. After examining the file, the commission concluded that the Guépard project was affected by market failures. In particular, the partner research institution is expected to make the results of its research widely known through academic publications and training. The commission also recognised that investment in new solar technologies could be discouraged in the short and medium term, as the market has recently been destabilised by the dumping of Chinese solar panels. The commission considers that the aid is necessary and sufficient to allow Soitec to carry out the project.

In the absence of state aid, the company's R&D efforts would have been considerably reduced: it would for example have abandoned development of high-efficiency cells, considered to be an excessive risk. This would undoubtedly have affected the development of the CPV sector. Finally, the commission was convinced that the target market (ground-based solar power plants) offers good growth prospects, and that the risk of distorting competition could be removed. Soitec's future market share will be minimal compared to the current market share of leading companies in the sector.

The photovoltaic modules sector has a specific profile; since 2009 the average price of these modules has fallen by two thirds, while at the same time certain Asian companies have seen a sharp increase in their market share.

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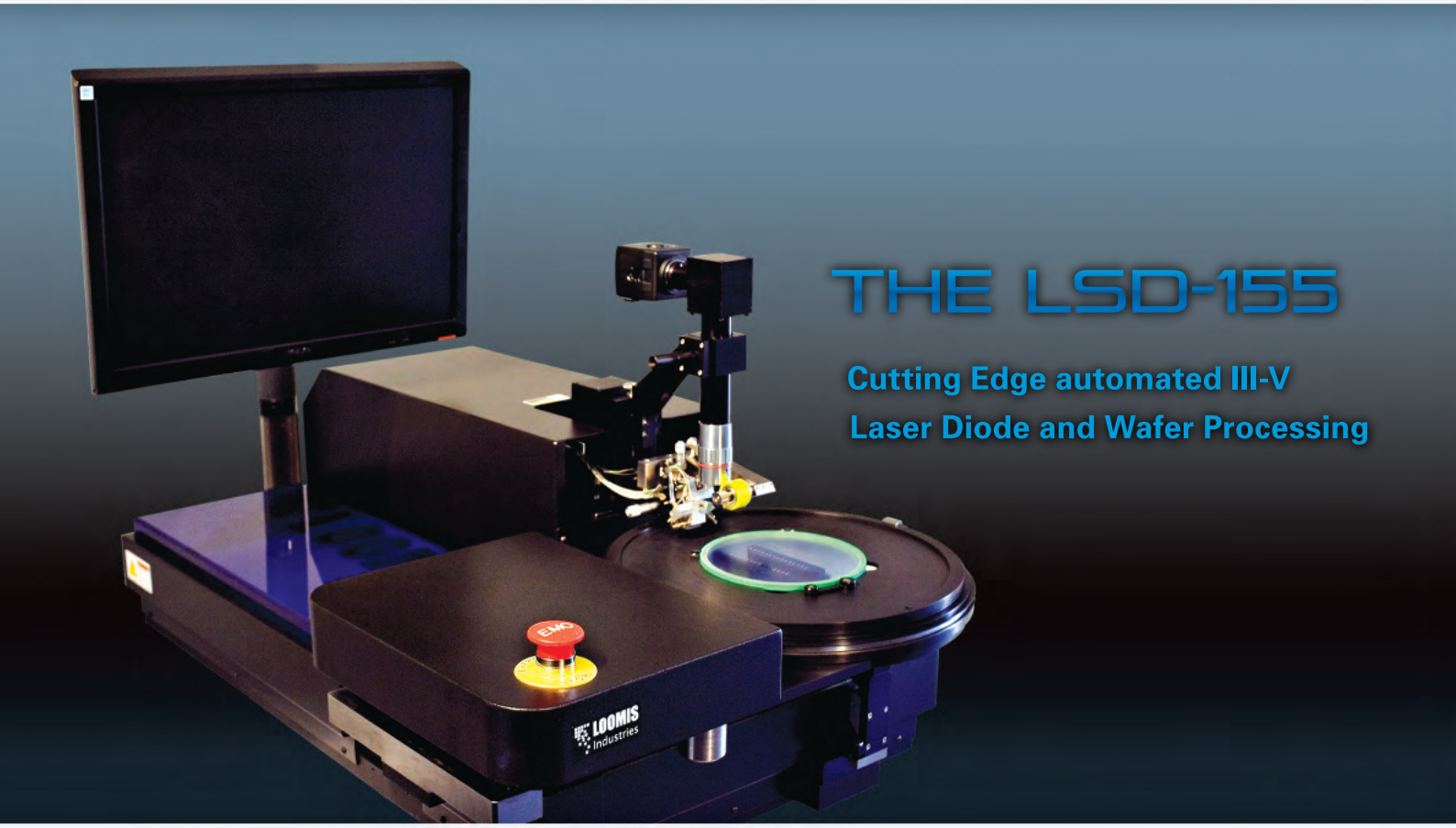

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GaN power defence project reaches conclusion

A GOVERNMENT and industry team led by engineers from the Air Force Research Laboratory's Materials and Manufacturing Directorate (AFRL/RX) have completed a GaN program.

The project focused on assessing, improving, refining, and validating a domestic source of supply for X-Band GaN Monolithic Microwave Integrated Circuits (MMICs). Because GaN semiconductors enable devices and MMICs with improved power, efficiency and bandwidth, MMIC technology offers the highest level of integration and the smallest form factor and they have become the technology of choice for power amplifiers and radars.

MMIC technology typically provides better high-frequency performance by reducing parasitic circuit elements and provides enhanced reproducibility as a result of uniform processing and integration of all circuit elements. GaN products include power amplifiers and supporting MMIC solutions, such as low-noise amplifiers, driver amplifiers and limiters. GaN power amplifier technology significantly enhances the warfighters' capabilitie by increasing radar ranges, sensitivity, and search capabilities when compared to existing radar platforms based on other semiconductor technologies. Additional defence applications for GaN MMICs include communication systems, electronic warfare applications, imaging, and sensor systems.

The Manufacturing and Industrial Technologies Division (AFRL/RXM) Defence Production Act (DPA) Title III team is responsible for conducting this work. Title III is a Department of Defence (DoD)-wide initiative under the Deputy Assistant Secretary of Defence, Manufacturing and Industrial Base Policy (MIBP). The Air Force serves as the Executive Agent for the Title III Program within the Department of Defence and the Title III Program Office is located at Wright-Patterson AFB, Ohio, as a component of AFRL/RXM.Jeffrey Smith, an engineer from RXM, serves as Air Force Executive Agent Program Manager. "The Title III Program is a government-funded venture that aides manufacturers who specialize in materials used for defence applications," Smith says. "Production capabilities that would otherwise be inadequate are transformed to support the material requirements of defence programs in a timely and affordable manner."

Smith notes Title III focuses on materials and components that could be used in a broad spectrum of defence systems. He says, "The direct and indirect benefits to defence programs resulting from Title III initiatives are substantial, and Title III projects create numerous economic and technological benefits for domestic industries and consumers."

DPA Title III engineers worked with Raytheon to execute the program at its Compound Semiconductor Foundry, located within its Integrated Air Defence Centre in Andover, Mass. Raytheon, headquartered in Waltham, Mass., possesses a broad international and domestic customer base, including the U.S. Missile Defence Agency, the U.S. Armed Forces, and the Department of Homeland Security. In addition, its IADC facility is a Department of Defence Category 1A Trusted Foundry (the highest category awarded by the DoD), and is recognized for providing trusted, national security critical components. Their foundry employs 30 researchers and 100 device, circuit and module engineers in addition to numerous production staff operating a 23,000 square foot, Class-100 clean room facility.

This Title III project achieved the primary objective of improving and maturing the production of GaN MMICs by producing a manufacturing process capable of Low Rate Initial Production (LRIP).

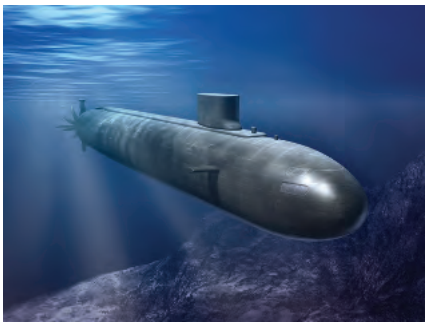
"The project achieved a Manufacturing Readiness Level of 8, meaning the fabrication processes are ready for LRIP for insertion into defence systems," Gene Himes, the AFRL/RXM program manager for the initiative says. "When comparing the final results to the baseline.

Manufacturing Readiness Assessment, Raytheon exceeded all threshold yield key performance parameters resulting in a three times improvement in product yield and a 76 percent cost reduction for its GaN MMICs."

In addition to yield improvements, the team logged more than one million hours of reliability testing over the course of the project. Comprehensive reliability testing helped to eliminate early MMIC failures and exceed the median time to failure key performance parameters by 1,000 times.Raytheon engineers also enhanced their GaN MMIC computer design model, which resulted in first pass design successes, robust models incorporating temperature and process variations, and comprehensive design kits for use in two separate software packages.

"This program exploited the material properties of GaN semiconductors to enable devices and MMICs with higher power, higher efficiency and bandwidth, and superior performance than existing semiconductor technologies," Himes adds.

AJC deploys Infinera technology for submarines



AUSTRALIA JAPAN CABLE (AJC), operator of the AJC cable system between Japan and Australia, has deployed the Infinera DTN-X platform across its submarine network.

The InP based Infinera Intelligent Transport Network, featuring the DTN-X platform with SD FEC super-channels and integrated OTN switching, enables AJC to significantly expand their cable's capacity and rapidly deliver 10, 40 and 100 Gigabit Ethernet services.

Australia Japan Cable offers connectivity and bandwidth, serving their customers, with a 12,700 km submarine fibre optic cable network from diverse landings in Australia, Guam and Japan.

AJC is composed of a consortium of leading service providers including Telstra, AT&T, NTT, Verizon and Softbank.

Infinera provides AJC with the DTN-X platform featuring long haul super-channels with SD-FEC based on one of the industry's most widely deployed Photonic Integrated Circuit and the FlexCoherent Processor, supporting up to 500 Gigabit per second (Gb/s) in a single line card.

The DTN-X platform is also equipped with 1 Tb/s per slot to support higher capacity 1 Tb/s super-channel line cards for future scaling needs.

"To meet the growing bandwidth needs of carrier, enterprise and ISP customers, AJC is significantly increasing the capacity of our network," says Philip Murphy, Head of Engineering at Australia Japan Cable. "We selected an Infinera Intelligent Transport Network because it allowed us to scale capacity while simplifying operations.

"The Infinera Intelligent Transport Network provides AJC a mesh network of 500 Gb/s super-channels with soft decision forward error correction, ensuring the AJC network delivers increased network resiliency while delivering the capacity demanded by their customers," continues Andrew Bond Webster, Vice President Sales at Infinera.

Soraa GaN LED lamps knock out halogen drawbacks

CALIFORNIA based gallium nitride expert Soraa has launched its first line of high colour and white rendering, high light output LED GU10 230V dimmable lamps.

The company says it has released a 10 degree spot version, not available in halogen or from other LED manufacturers, as well as a 25 degree version that has a peak intensity higher than halogen and all other LED GU10 products.

Now customers can buy transformer-free, full visible spectrum Soraa LED GU10 lamps that spectacularly render colours and whites; without beam striations, artefacts or multiple shadows visible in other manufacturer's LED products.

"Soraa's no compromise, full visible spectrum, high colour rendering LED lamps are simply the best on the market today. Our products excel in the key elements that define quality of light: light output, colour rendering, white rendering, and beam definition. The Soraa GU10 lamps provide unmatched light output, perfectly uniform beams, exceptional rendering of colors and whites, full dimmability, long lamp life, dramatically improved energy efficiency, and excellent compatibility," says Jeff Parker, CEO of Soraa. "All these features are made possible through our proprietary GaN-on=GaN LED technology and innovative lamp design."

The company's continuous full visible spectrum Soraa Vivid 2 LED GU10 lamps, with a CRI of 95 and R9 greater than 90, render deep reds and cyans dramatically and accurately and have no artificial spectral "blue-peak". And just like natural light, the violet component of the full visible spectrum makes whites in fabrics and fibres stand out in their intended brightness and tint.

VPEC orders more Aixtron MOCVD reactors

VISUAL PHOTONICS EPITAXY CO. LTD. (VPEC) has ordered two more AIX 2600G3 IC MOCVD systems fully equipped to handle seven 6-inch substrates (7 x 6") in a single run.

VPEC placed the order to expand its microwave epiwafer volume production. The systems have been installed by Aixtron's local Taiwanese office.

Neil Chen, VPEC Vice President, comments, "Our RF microwave device business operation unit will be using the new systems to support our latest capacity expansion designed to meet ever higher demand from customers. We have been using the AIX 2600G3 for more than ten years now with our last multiple systems order having been completed in 2010. This last production capacity addition has put us in the solid commercial position to invest once more in Aixtron's high quality equipment."

VPEC chose the Aixtron systems due to their robustness and extended uptime, along with high throughput. "Aixtron excels at supplying equipment with these features, along with prompt service and process support, all of which are vital for our successful business," Chen concludes.

Aixtron´s Vice President Southeast Asia Christian Geng adds, "Driven by the demand for mobile phones and Wi-Fi, the need for RF power amplifiers based on compound semiconductor heterojunction bipolar transistors (HBTs) continues to rise and microwave device makers are presently adding MOCVD production capacities."

Visual Photonics Epitaxy Co. Ltd., a semiconductor epitaxial wafer pure play foundry, was founded in 1996 and is based in Ping-Jen City, Taiwan. The company provides solutions for wireless communications, optical fibre communications, and solar cell applications.

Plessey order ALSI laser tool

ADVANCED LASER SEPARATION INTERNATIONAL (ALSI) NV has received an order for a laser dicing system from Plessey Semiconductors for its Plymouth, UK based LED manufacturing facility. Keith Strickland, Chief Technology Officer at Plessey says, "An essential process step to achieve our cost and LED performance targets is the singulation of the finished wafer into LED dies.

ALSI demonstrated their experience in dicing and proved in short turnaround time to be able to meet our challenging process, cost and delivery requirements. "ALSI's multi-beam process will be key to the back-end processes to be included in the fabrication line in Plymouth."

IHS: LED lamp retail price falls 11.8%

The December 2013 release of IHS' LED lamp retail price tracker has found the global average LED lamp retail price was $24.5, indicating a fall of 0.4 percent in December over November 2013 and 11.8 percent fall over the same time last year.

IHS says that over the past twelve months the lumens per dollar ratio of LED lamps has increased by 31 percent to 29.9 lumens per dollar. IHS has been tracking the LED lamp retail pricing trends for over two years. Each month IHS analysts sample over 2,500 individual LED lamps sold in retailers across 15 countries globally.

Many players to monopolise chip on board LED market

ACCORDING to Infiniti Research's report, "Global Chip on Board LED Market 2014-2018", the global Chip on Board (COB) LED market will grow at a CAGR of 41 percent over the period 2013 to 2018. One of the key factors contributing to this market growth is the declining ASP of LEDs.

The global Chip on Board LED market has also been witnessing the increasing demand of COB LED in general lighting applications. However, the fluctuating global economic conditions could pose a challenge to the growth of this market.

The key vendors dominating this market space are Citizen Electronics co. Ltd., Cree Inc., Nichia Corp., Osram Opto Semiconductors GmbH, Philips Lumileds Lighting Co., Samsung Electronics Co. Ltd., and Seoul Semiconductor Co. Ltd. Other vendors mentioned in the report are Everlight Electronics Co. Ltd., Lumens Co. Ltd., and LG Innotek Co. Ltd.

Commenting on the report, an analyst from the team says the shift from traditional lighting sources to solid-state lighting technology has resulted in the wider adoption of COB LEDs.

COB LEDs are wide-area light emitters and thus, are increasingly used in highway and street lighting, which require large amounts of light spread across a large area. COB LEDs produce better colour mixing, better lighting effect, and require very low thermal resistance systems, thereby enhancing the total consumer experience. Thus, greater power density, efficient heat dissipation, small space requirement, and high performance makes COB LEDs more suitable than conventional LED packages for various general lighting applications.

3D-Micromac acquires the TLS-Dicing technology of Jenoptik

JENOPTIK is transferring its thermal laser separation (TLS-Dicing) technology as part of a so-called asset deal to 3D-Micromac AG.

As of January 1st, 2014, know-how, patents and results of the development from Jenoptik's Laser & Materials Processing Division have been transferred to 3D-Micromac AG in Chemnitz. Immediate commercialisation of the technology by 3D-Micromac will be possible with the transfer. With the acquisition, the company reinforces its know-how as a system provider for laser systems in the semiconductor industry and advances the expansion of its product portfolio in this area. Jenoptik's Laser & Materials Processing Division will continue in the future to focus on the 3D processing of plastics and metals, for example in the automobile industry.

According to Tino Petsch, CEO of 3D-Micromac AG, TLS-Dicing will enable the company to obtain a technology that will perfectly complement its product portfolio in the semiconductor industry and enable it to expand its market position.

Petsch adds, "In addition to component processing at wafer level we can now also offer innovative solutions for separating of microchips. In the coming months, we will continue to further develop the process in co-operation with the Fraunhofer IISB and implement it in industry-ready machine technology." "Jenoptik's Laser & Materials Processing Division has increasingly focused on its core markets and sharpened its portfolio in recent months," says Dietmar Wagner, general manager of Jenoptik Automatisierungstechnik GmbH, following the contract's signing. 'We are pleased that with 3D-Micromac AG we have found a buyer for TLS-Dicing, which wants to successfully commercialise the technology in the shortest possible time".

TLS-Dicing (thermal laser beam separation) is used in the semiconductor industry's back-end to separate semiconductor wafer in components. A laser heats up the material locally and a cooling medium cools it down immediately afterwards.

The thermally induced mechanical stress leads to a complete cleaving of the wafer. The method is suitable for most brittle materials in the semiconductor industry, including silicon, SiC, germanium and GaAs wafers.

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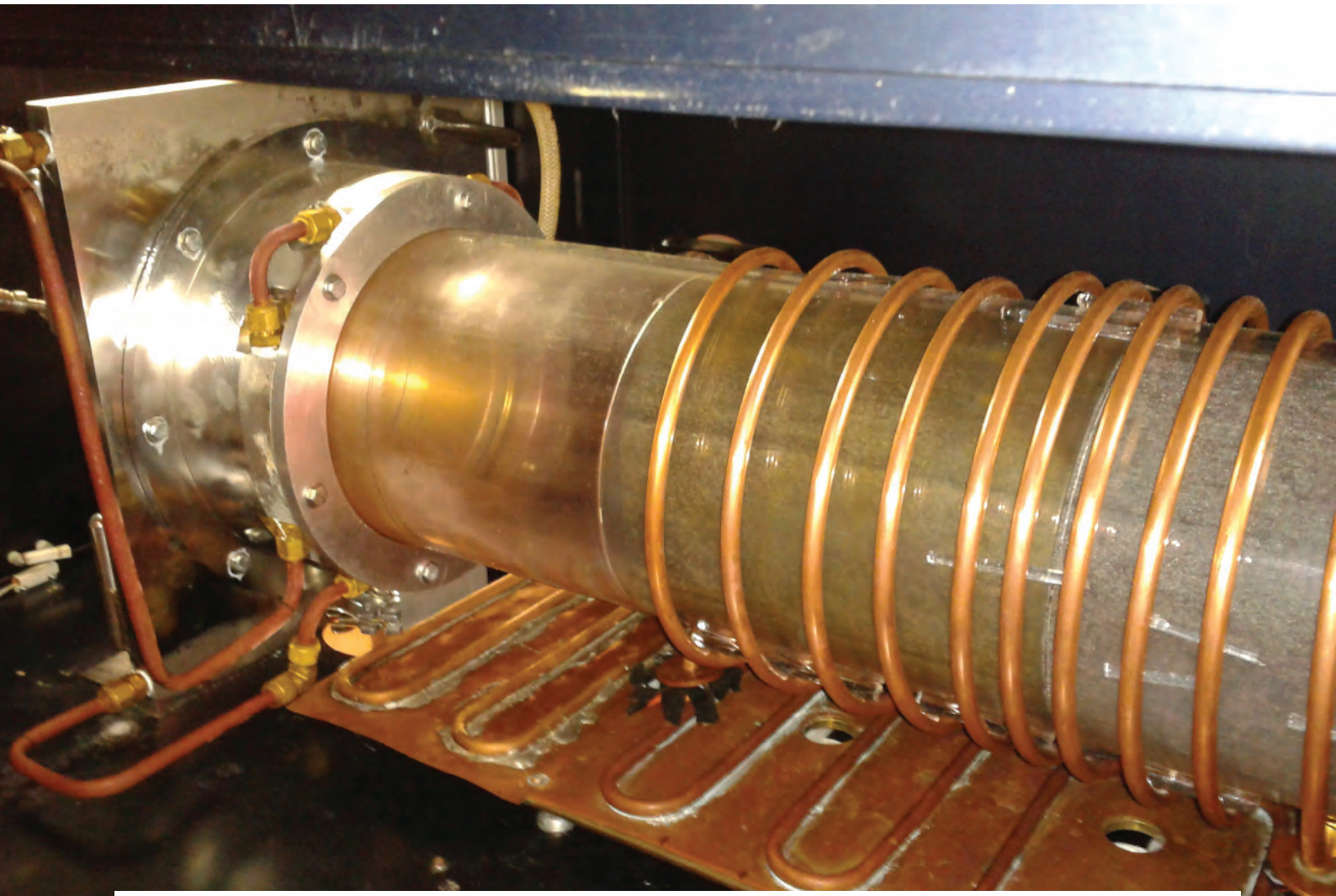


Anvil to serve up cheap SiC switches

With Schottky diodes scheduled for next year and MOSFETs to follow, power semiconductor developer, Anvil Semiconductors, looks set to deliver what industry wants; efficient and cheap SiC devices.

In 2011, UK-based Warwick University launched Anvil Semiconductors to develop cheap but high quality SiC power semiconductor switches. Two years and some £2 million in funds later, the company has just won the National Microelectronics Institute Innovation in power electronics award and will soon deliver its first products.

SiC holds incredible promise as the material for tomorrow's power electronics applications. Devices are faster, more efficient and can withstand much higher voltages and currents than the straight silicon equivalent. SiC Schottky diodes have pretty much replaced silicon *p-n* diodes in switched-mode power supplies for computers, while SiC transistors are making in-roads into hybrid and all-electric vehicle, photovoltaic applications and more. But despite rapid progress, cost is a major stumbling block. Anvil Semiconductors could make a difference. The company has developed a process to produce SiC power switches at a similar cost to silicon by growing layers of SiC on silicon wafers instead of using expensive bulk SiC.

"Our essential cost reduction is substituting a $1000 4H-SiC substrate with a $40 silicon substrate," states Anvil founder and managing director, Peter Ward. "We're [depositing SiC on] 100 mm silicon wafers at the moment but will get up to 200 mm wafers within our pre-production time-scales."

Today, the likes of Infineon and Cree are busy developing SiC devices based on 4H SiC crystalline materials. This polymorph is grown via PVT as a single crystal and then sliced to produce relatively defect-free wafers, up to 6-inches in diameter. However, the growth process is slow and energy-intensive, yielding very pricey substrates.

But a second polymorph could provide an alternative. In theory, layers of 3C-SiC could be grown epitaxially on silicon wafers as this polymorph has a cubic crystal structure just like silicon. But while the resulting wafer could be produced much more cheaply than a 4H-SiC wafer, lattice mismatches and differences in thermal expansion coefficients between the 3C-SiC layers and silicon seed wafer induce in-plane stresses that cause wafer bowing. Device performance plummets and so manufacturers have stuck with the costly 4H-SiC wafers.

However, Ward, and colleagues, have developed a novel, low pressure CVD 3C-SiC growth process, that they claim bypasses these problems. Prior to SiC growth, a mask is placed over the silicon wafer to define structures in the scribe lines of the wafer. The team then deposits a 1.5 μm-thick layer of heavily doped, dislocated material onto the silicon seed wafer. This helps to relieve stresses from lattice mismatches that lead to wafer bowing, and also allows vertical conduction through the interface.

“This layer is doped with dopants from the silicon wafer and nitrogen, allowing us to conduct through the silicon carbide-silicon heterojunction,” says Ward. “So we can conduct from the top to the back of the wafer and have built devices where you cannot see additional resistance at the interface. This makes us very competitive with GaN-on-silicon, which can’t conduct vertically.”

In the same run, monocrystalline SiC is then grown in the die areas between the scribe lines, with polycrystalline SiC forming in the scribe lines. As Ward says: “We are effectively interfering with the epi-process and producing polycrystalline SiC in the scribe lines while growing single crystalline epilayers where we want to build the device.”

Crucially, the resulting mesh of polycrystalline SiC helps to relieve the thermal expansion differential stresses across the wafer that also lead to bowing.

“Instead of trying to fabricate a 100 mm wafer, in terms of stress we are effectively making a 5 mm die,” he adds. “This makes our process very scalable and essentially independent of wafer diameter.”

Indeed, as Ward highlights, his company is only limited to 100 mm wafer sizes at the moment due to the industry’s shortage of higher temperature, large wafer diameter epi-reactors.“Silicon reactors typically run at 1000 °C, but we need a reactor that has been designed to reach 1370 °C and the only ones that exist have been built for [100 mm] 4H SiC wafers,” he explains. “So there aren’t so many of these reactors right now, but we know where they are and who they belong to, and we’ve worked with most of these [organisations].”

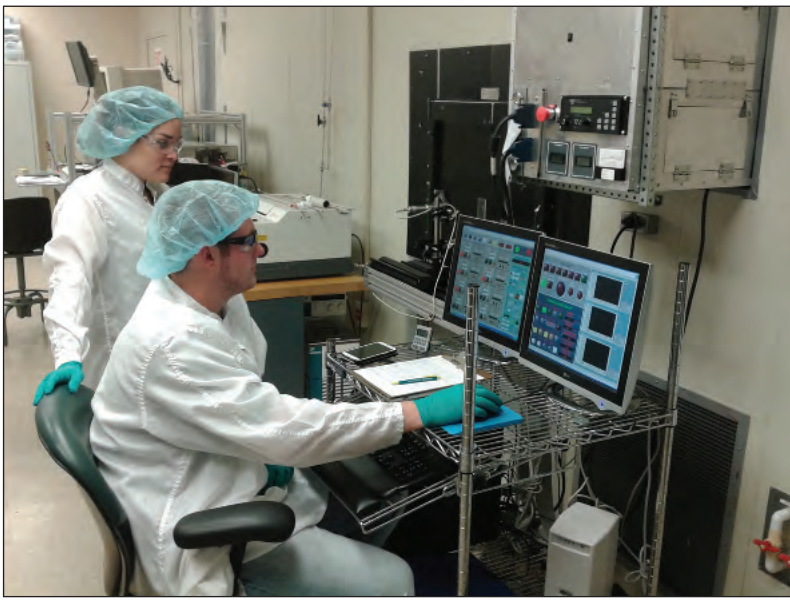
Ward is also adamant the process is scalable to mass production, stating: “ I have spent more decades than I would care to working with silicon, and having spent a lifetime manufacturing silicon devices, I see no reason why this shouldn’t scale.”

> “We hope to stay as a niche product manufacturer but we see a very clear value chain from Schottky diodes to MOSFETs and probably to driver circuits as well.”

In the meantime, the Anvil team is busy building prototypes. A standard Schottky diode, similar to 4H-SiC versions but cheaper, is scheduled for release in 2014. And the company is also running a parallel MOSFET program, which could see prototype devices being released six months after the first Schottky diodes.

Ward won’t talk about performance figures yet, only to say his team is pushing for very low on-resistance devices and is focusing on producing 650 V Schottky diodes and MOSFETs. As he explains, using 3C-SiC on silicon, his team can fabricate a very cost competitive 650 V device.

“Once we prove these 3C-SiC devices are a go-er we will start licensing commodity products,” he adds. “We hope to stay as a niche product manufacturer but we see a very clear value chain from Schottky diodes to MOSFETs and probably to driver circuits as well.”



The Anvil Semiconductor team has been working with researchers at the University of South Florida to hone SiC device development and reactor technology

GaN growth: an extra inch

GaN crystal newcomer, Fairfield Crystal Technology, is ready to take substrates to greater lengths.

WHEN IT COMES TO GROWING high quality, decent-sized GaN crystals, the US government is keen to fund companies that are making it happen.

In the last two years, vertically integrated developer of GaN-on-GaN LEDs, Soraa, has won more than $5 million from DoE agency, Advanced Research Projects Agency-Energy (ARPA-E), to develop large area, low cost GaN substrates. Meanwhile GaN crystal developer, Kyma, recently bagged some $3 million to advance its technology for manufacturing substrates, shortly after releasing commercially available 2-inch GaN substrates.

But now, in the same wave of funding, a third company, Fairfield Crystal Technology, has also attracted $1.5 million to develop a new technique to speed up the growth of GaN single-crystal boules. Perhaps lesser known in the GaN crystal field, the Connecticut-based crystal developer has been manufacturing semiconductor and optical crystal materials since 2004 – key crystals include AlN, ZnS and ZnO – but started looking at GaN two years ago.

“A lot of organisations take one crystal and focus on that but we’ve looked at different crystals which has given us a good understanding of crystal growth with different techniques, using a range of furnaces,” says chief executive, Andy Timmerman. “You know we’ve done a lot on ZnO, have successfully launched AlN, so we see this as the next stepping stone to advance our crystal growth technology and work it into commercialisation.”

Naturally, government backing helps. ARPA-E sees the material as crucial to a new generation of power devices, hence the hefty

weighting in its $27 million SWITCHES program, Strategies for Wide Bandgap, Inexpensive Transistors for Controlling High Efficiency Systems.

And as Timmerman highlights only last month, the Department of Defense opened up solicitations for projects on GaN Technology for GPS L-band space power amplification, as part of its Small Business Innovation Research program. "GaN really has a good fit for our overall research and commercialisation of different products," he adds.

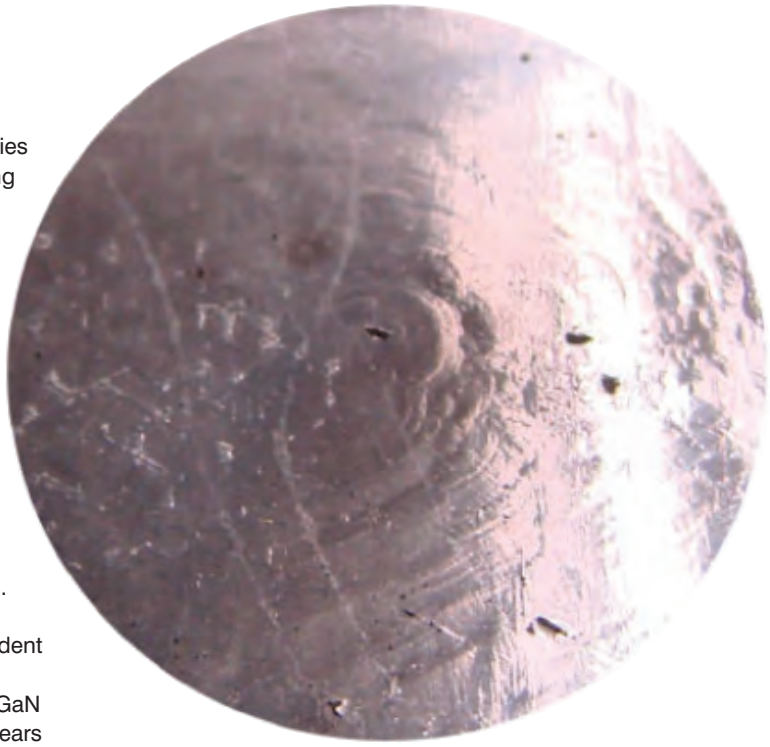
However, Fairfield Crystal is no stranger to US government interest in crystal growth. Preceding 2010, it had won just over $1 million from the National Science Foundation to develop ZnS, CdS, ZnSe and AlN crystals.

Then come 2010, it received $200,000 from the independent government agency to develop a novel approach, and demonstrate and sample 1-inch diameter free-standing GaN wafers for III-Nitride light emitters and detectors. Three years on, NSF funds run into the millions of dollars with the company working on pilot production of 2-inch GaN.

But what exactly is the novel approach? Timmerman remains tight-lipped; when asked if the process is based on either HVPE or ammonothermal methods, he confirms it is not based on the latter.

"It is the current state of the art. We know some folks are using ammonothermal, Kyma has been using a HVPE process, and others are looking at a combination of the two. But ours is different," he says. "It's using a combination of expertise from other crystal growth, be it AlN or ZnO, or even just some of the techniques we've gleaned from growing our optical crystals."

One such technique entails a novel method for growing a ZnO single crystal boule from a ZnO seed within an iridium crucible placed inside an induction-heated physical vapour transport (PVT) furnace system. According to Timmerman, the technique overcomes inadequacies in hydrothermal, CVT and melt growth techniques, but 'is a distinct technology differing from Fairfield's GaN technologies'.



The top surface of a GaN single crystal of about 1-inch in diameter produced at Fairfield Crystal; the company has achieved a dislocation density of 1 X 10^7 cm^{-2}

"However, we have found that having a very very clean source material is a priority [for the GaN process]," he adds. "And we've developed an in-house process with high quality source material.

With this in hand, the team now intends to drive GaN substrate costs down by growing longer boules and slicing more wafers per growth run. And of course, a crucial part of the ARPA-E grant, is to grow 3-inch GaN crystals, within the next three years.

"The time frames are very aggressive, especially since in a number of years other organisations have also been trying," admits Timmerman. "We're cautious but confident we can get there, although we are not dismissive of the challenges."

"The team now intends to drive GaN substrate costs down by growing longer boules and slicing more wafers per growth run. And of course, a crucial part of the ARPA-E grant, is to grow 3-inch GaN crystals, within the next three years"

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LEDs

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Keynote presentation: Young Soo Park
Slashing LED costs with 200 mm silicon substrates

SAMSUNG

William Henry
Applications and opportunities for MicroLED emitters

INFINILED

Pallavi Madakasira
LED light bulbs: When and how will the lighting of tomorrow become the lighting of today

luxresearch

Ulrich Steegmueller
Success factors in the increasingly competitive LED ecosystem

OSRAM
Opto Semiconductors

David Kepniss
Sub part-per-billion analysis of high purity hydrogen - process improvement applications with the HEMS™ analyzer

Power+Energy

Reinhard Benz
Increasing LED performance and reducing production costs to accelerate the growth of LED lighting

evatec
process systems

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Integration of CMOS and III-Vs

Silicon is running out of steam, and the future is widely tipped to be high-mobility channels made from germanium and III-Vs. But how will these materials be introduced in the world's leading silicon foundries?

Keynote presentation: Jean Fompeyrine
Co-integration of III-V and Ge CMOS

IBM

Thorsten Matthias
Direct wafer bonding: Enabling technology for future photonic and electronic integration

EVG

Shinichi Takagi — The University of Tokyo
III-V and germanium FET technologies on Si platform

Aaron Thean
Beyond silicon CMOS: Transforming transistors with heterogeneous material integration

imec

Power Electronics

Silicon has dominated the power electronic market for decades, but wide bandgap semiconductors will soon replace this material. What's the primary role for SiC, and where will GaN feature?

Keynote presentation: Ming Su
Can SiC or GaN power the next-generation hybrid electric vehicle drive systems?

Ford

Keynote presentation: Mike Briere
Pioneering GaN on Si power devices on large diameter substrates

International IOR Rectifier
THE POWER MANAGEMENT LEADER

Philippe Roussel
Vertical integration vs outsourcing in the wide bandgap sector

YOLE Développement

Marcus Behet
SiC and GaN/Si for power electronics – niche forever?

DOW CORNING

Denis Marcon
200mm GaN-on-Si CMOS compatible platform

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Kolja Haberland
Advanced in-situ growth monitoring for GaN based power electronics on silicon

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Knowledge is key

Roman Sappey
Defect inspection and monitoring in SiC and GaN power device processes

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Chris Hodson
Low damage plasma processes for compound semiconductor applications

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Front Ends for Mobile Devices

Handset front-ends are becoming more complex, due to an ever-increasing number of bands used for mobile communication. Will this trend play into the hands of GaAs chipmakers? Or is silicon CMOS technology going to grab market share?

Keynote presentation: Jeremy Hendy
Envelope tracking - transforming the performance of CMOS and GaAs PAs

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Eric Higham
Coming full circle - will Si CMOS burst the GaAs bubble?

STRATEGY ANALYTICS

Thomas Meier
GaAs & Silicon: Co-existence in a wireless world

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Brendan Timmins
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Dirk Schumann
Waterbased stripping innovation for wafer stripping and metal lift-off

bubbles & beyond intelligent fluids

Wolfram Drescher
"Cold split" – A simple thinning and wafering process technique

SILTECTRA

Cris Kroneberger
Non contact magnetic drive assembly for improved reliability and reduced particulates

Temescal

Lasers, PICs and PV

Rocketing levels of internet traffic are putting greater and greater strain on optical networks and data centres. Can this be addressed by advancing the performance of conventional lasers, or does the market need to turn to greater use of PICs?

Keynote presentation: Michael Lebby
Photonic integration in InP: A regrowth-free platform for the fabless manufacturing model

ONECHIP PHOTONICS

Michael Vyvoda
Using proton induced exfoliation to manufacture low-cost, device quality single crystal substrates

GT ADVANCED TECHNOLOGIES

Gregory Fish
III-V heterogeneous photonic and electronic integration on silicon

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Petteri Uusimaa
RGB laser solutions to display and projection application

modulight on your wavelength

Hong Lin
Bulk and free-standing GaN substrate technologies and industry status in the LED, laser diode and power applications

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Rainer Krause - Soitec
Wafer bonded 4-junction GaInP/GaAs//GaInAsP/ GaInAs high performing concentrator solar cells

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Wide Bandgap RF Devices

GaN and SiC have a great set of attributes that make them very promising materials for producing RF devices. But are they now fulfilling their potential and netting substantial sales?

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Overview of GaN reliability improvement activities at the European Space Agency

Chris Horton
Enabling material solutions for GaN in the RF arena

Marc Rocchi
100nm GaN/Si mmW foundry service and MMICs

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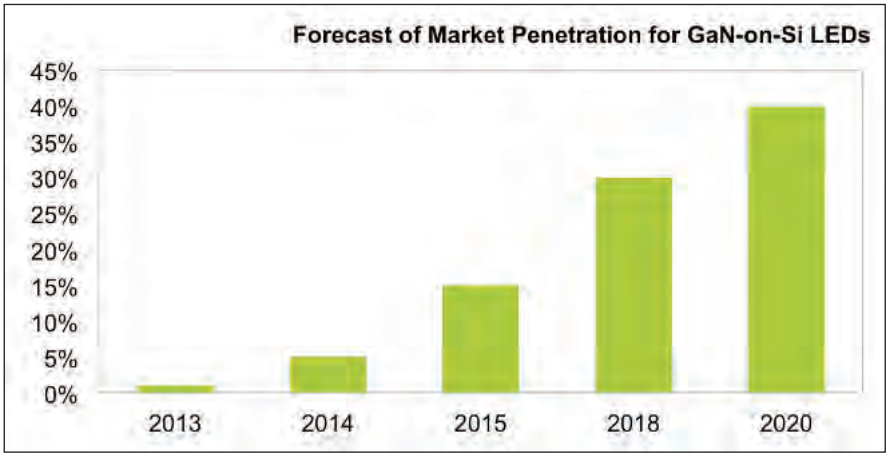
GaN-on-silicon LEDs slated for massive market growth

IHS predicts silicon-based LEDs will nearly rival sapphire-based devices on market share come 2020.

LATE LAST YEAR, analyst business, IHS, forecast GaN-on-silicon LEDs will increase market share from today's 1 percent to an incredible 40 percent by 2020. This monumental 69 percent compound annual growth rate is at odds with other 2013 forecasts, but IHS analyst and author of *GaN LEDs on Silicon – World – 2013*, Dkins Cho, is certain the technology is poised for strong growth. "In 2013, 95 percent of GaN LEDs were manufactured on sapphire wafers with only 1 percent manufactured on silicon," says Cho. "Come 2020, 40 percent will be manufactured on silicon, maybe 3 percent on SiC, with the remainder on sapphire substrates."



Forecasts of Market Penetration for GaN-on-silicon LEDs

According to Cho's forecast, the GaN-on-sapphire LED is still set to retain the largest market share – but only just. However, given GaN-on-silicon's technical challenges, such as the lattice mismatch between GaN layers and the silicon wafer, as well as questionable manufacturing yields, is his forecast of near-market domination realistic?

Cho thinks so. As he points out, a few leading suppliers, most notably in Asia, have recently made good progress performance as well as throughput and yield on 6-inch to 8-inch wafers. Declining to name companies he says: "Looking at the leading GaN-on-silicon LED companies, performance-wise, these manufacturers are producing devices with a similar performance to sapphire-based LEDs. Production yields are more of a problem, but some companies have already overcome this." As Cho highlights, GaN-on-silicon LEDs have been successfully fabricated on 8-inch wafers using legacy CMOS fabrication facilities and equipment with just minor modifications. Indeed, many GaN-on-silicon LED heavyweights already own legacy 8-inch CMOS facilities, and could well be ready to migrate manufacturing to these fabs.

"Samsung and Toshiba already have CMOS semiconductor lines and have produced good devices," he says. "I also expect to see at least one Taiwan-based and two China-based companies enter the market."

The draw to silicon is largely ease of manufacturing and being able to use existing inspection tools. "Silicon has better machining characteristics than sapphire for laser cutting, grinding and polishing," says Cho. "CMOS fabrication on silicon has a long history of production using state-of-the art technologies so there is much greater process knowledge [than sapphire-based LED production]. And the process equipment is well developed and deployed over the entire front-end and back-end process," he adds. "GaN-on-silicon LED production can make use of legacy tools and facilities... to enhance process yields as well as overall yields and through-puts."

Legacy CMOS equipment can also be used for *in-situ* monitoring and inspection, potentially leading to faster improvements in performance than has been achieved with sapphire-based LEDs to date. Still, Cho does not expect the likes of Toshiba and Samsung to convert to CMOS manufacturing immediately. "It is unlikely re-purposing will happen overnight," he says. "Instead we forecast a shift during the coming years."

CMOS rivals

While manufacturers of GaN-on-silicon LEDs will, without a doubt, chip away at the sapphire market share in coming years, other analysts do no concur with IHS's bold predictions. In the Summer of 2013, Lux Research analyst Pallavi Madakasira released her report *Dimming the Hype: GaN-on-silicon Fails to Outshine Sapphire by 2020*. As she asked *Compound Semiconductor* at the time: "Can we really expect an organisation that has invested billions of dollars in its GaN-on-sapphire line to stop running that?" Questioning the performance of GaN-on-silicon LEDs, she also stated: "You have to remember that [GaN-on-silicon LED manufacturers] are catching up on a moving target. GaN-on-sapphire performances will keep improving and costs are going to keep coming down."

And then there's the added complication of Cree. With its continued investment in SiC production and successful transition from 4-inch to 6-inch diameter wafers, can industry really expect the US-based industry heavyweight to lose out to silicon rivals in such a big way?

Still, Cho is standing by his forecasts. Cheap fabrication costs aside, he believes a rising demand for LEDs for medium power lighting as well as applications such as LED-backlit LCD displays will boost GaN-on-silicon LED manufacturing. He also highlights how he has analysed the manufacturing cost and price behaviour of major suppliers across the supply chain as well as interviewed GaN-on-silicon developers and companies not moving to GaN-on-silicon technology.

"The companies making GaN-on-silicon LEDs have sold out production," he says. "Sapphire and silicon carbide market share will continue to go to silicon."

Market analyst Dkins Cho expects at least one Taiwan-based and two China-based companies enter the GaN-on-silicon LED market

Rocky road to real power conversion

The market-ready high voltage GaN-on-silicon power device has been a long time coming. Compound Semiconductor asks Venture-Q's Zel Diel if the industry will deliver soon.

IN 2010, ZEL DIEL, managing director of US-based power electronics analyst business, Venture-Q, started investigating how and when GaN-on-silicon devices for power conversion applications would be commercialised. Within months, he had concluded that by 2016 industry would see high-voltage FETs in low quantities so designers could use them to build demonstration systems. These structures would be deposited on 200 mm silicon wafers to achieve an acceptable cost parity with silicon alternatives.

Nearly four years on and having just unveiled his latest report on commercialization strategies for GaN-on-silicon power devices, Diel's time-frame has shifted. "We're not so far off now. By 2018 system designers will be able to say, yes, I can buy [HEMTs] for $5 or $6 and at a system level cost parity," he says.

Still, the road to true commercialisation is going to be rocky. As Diel asserts, time and time again, market research forecasts, largely relying on vendors' unrealistic product availability timetables, have underestimated the challenges GaN-on-silicon developers face and proven optimistic.

While Efficient Power Conversion (EPC), US, introduced the first commercially available low voltage GaN-on-silicon HEMT nearly four years ago, this company and every other vendor has since struggled to deliver commercially-viable high voltage – 600 V – devices. EPC has repeatedly pushed back delivery of high voltage devices and the only generic 600 V GaN-on-silicon HEMT device publicly introduced by Transphorm has been offered to select partners under non-disclosure agreements.

So why the slow progress? For starters, myriad industry infrastructure constraints exist. "We are dealing with a completely different technology in a system level design

that power system designers have never seen, never had experience with and never been trained with," he says. "We have no reliability systems in industry, only JEDEC, but this is a silicon standard so qualifying for JEDEC doesn't mean a thing; you can't even qualify a part and send it to be integrated into a system as there is no standard on paper."

What's more, both GaN-on-silicon developers and oscilloscope manufacturers have also highlighted the test and measurement challenges posed by high-voltage, high-bandwidth GaN devices. "Tektronix has said it had no oscilloscope fast enough to measure switching in these devices," highlights Diel.

And then there's the technology issues. While the lattice mismatch between the silicon substrate and GaN layers has hampered development, so-called current collapse is proving to be the primary stumbling block stymieing progress.

The phenomenon is an inherent attribute of GaN-on-silicon, as well as GaN-on-SiC HEMT device structures, which manifests as an increase in the device's on-resistance during high voltage operation, degrading performance. Crucially, current collapse, especially in GaN-on-silicon devices, is exacerbated at 400 V operation and higher and is now the the primary focus of research and development efforts in industry and academia.

"Current collapse is the kiss of death and we cannot find a cure," says Diel. "Since 1999 at least 1000 PhD theses have been written on this and still people are struggling with the problem. Vendors are tackling this challenge but no-one has a solution."

So don't these technology challenges twinned with industry infrastructure constraints make a 2018 commercialisation timeline ambitious? Diel thinks not, highlighting recent industry developments that signal real progress.

In October 2013, Powerdec, a developer of GaN-on-silicon HEMTs, demonstrated a 600 V, 10 A HEMT it had produced alongside the University of Sheffield, UK. The device was fabricated using the organisation's proprietary polarisation super-junction process, which Powerdec claims suppresses current collapse.

And then in November 2013, Fujitsu, and University of California Santa Barbara spin-off, Transphorm, signed a deal to integrate the GaN power device businesses of each. The move will boost the market competitiveness of Transphorm's cutting edge GaN technology by capitalising on Fujitsu's manufacturing prowess. In short, industry should see high volume, high performance and cheap GaN devices sooner rather than later.

"Due to long-time research at UCSB and with Cree, Transphorm's technology is very advanced... but moving into manufacturing brings many complex issues," says Diel. "Transphorm has realised this, and this where Fujitsu, a manufacturing powerhouse, comes in."

And we can expect more of the same. Diel predicts we will soon see EPC, in reality the only vendor currently offering GaN-on-silicon HEMTs on the open market, teaming up with a systems manufacturer.

"More and more vendors are now recognising that what they are dealing with is not as simple as research and development presented at conferences," he says.

"I speculate that this Fujitsu-Transphorm deal will be repeated quite frequently as we go forward, and those that don't do this will become laggards."

GaN advances into defence electronics

ABI Research analyst, Lance Wilson, predicts GaN will drive pulsed RF power device market growth. **Compound Semiconductor finds out more.**

WITH THE MARKETS for pulsed RF power semiconductor devices set to top $250 million by 2018, the future for GaN in defence electronics applications looks very healthy.

As Lance Wilson, ABI Research analyst and author of a recent study *Pulsed RF Power Semiconductors* puts it: "Despite everything in the news about defence markets being cut, we are going to see a higher percentage of spending going towards defence electronics."

Wilson has identified what he calls a 'quantum shift' in defence-related procurement away from capital-intensive equipment such as fighter aircraft and towards relatively cheap, electronics-weighty applications such as radar and electronics warfare.

"This does not mean the defence electronics industry gets a free ride – the next three to five years will be tough – but once medium term budget battles are over, I think defence electronics is going to come out as the big winner," he says.

Right now, the pulsed RF power device market is crowded to say the least. Myriad manufacturers from Cree, Freescale, M/A-Com to Microsemi, RFMD, TriQuint, and more, are developing devices based on pure or various blends of silicon, SiC, GaAs and GaN.

Silicon-based devices dominate the sub-1 GHz radar market, both GaN and silicon development is rife for 1-3 GHz markets while in radar applications at 3 GHz and more, market share is all going to GaN. But still, product differentiation isn't easy and consolidation is to be expected.

"Certainly over the next five years we will see consolidation within these frequency divisions," says Wilson. "This isn't based on technical issues but rather on economic and market forces."

The analyst won't name names, but asserts companies with a track record of working with government and defence organisations will have an advantage over new entrants.

"Northrop Grumman and Raytheon, for example, also make their own GaN and use it in radar systems," he adds. "I don't want to say this gives them an advantage but it gives them a manufacturing efficiency that other companies might not have."

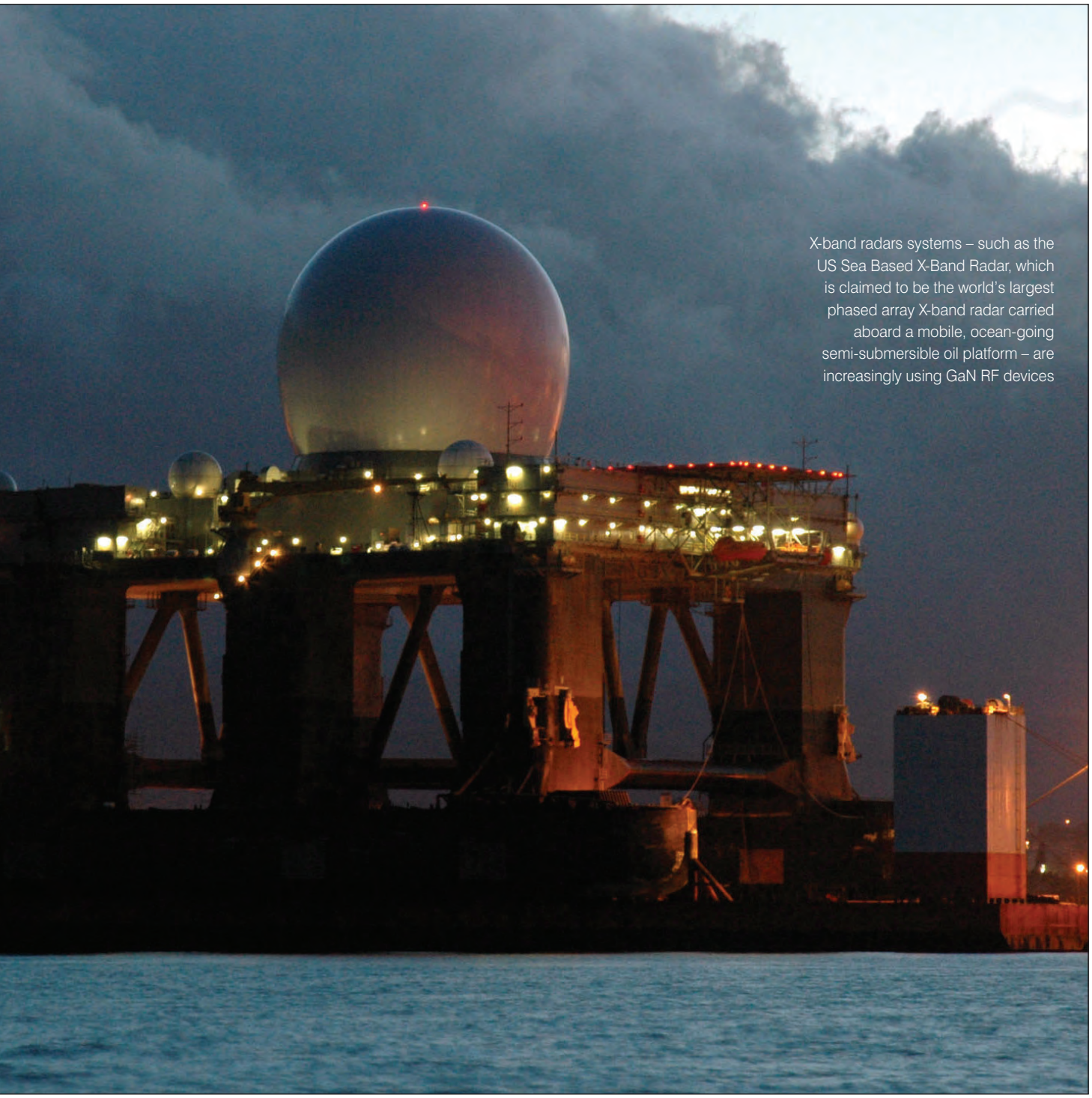
GaN drives growth

Crucially, however, Wilson believes GaN is going to drive most of the market growth between now and 2018. Beyond 4 GHz frequencies, GaN, with its high voltage, high power and high frequency performance, is the only truly viable option.

As Wilson explains, silicon devices can't operate at these frequencies while GaAs cannot produce the peak power levels demanded by most pulsed applications here. As a result, all the above 4 GHz frequency applications that were served by microwave tubes are now open to GaN, and so solid-state device manufacturers are now turning to GaN-on-silicon and GaN-on-SiC devices.

"Most pulsed silicon device suppliers are going into GaN as they recognise a large portion of the business will drift over to the material and they don't want to lose market share," says Wilson. "And for those companies that don't appear to have a GaN program, they do, they all do. Some companies are less vocal than others but all the principle silicon manufacturers have robust GaN development."

Still, this doesn't sound the death knell for manufacturers of vacuum tubes for



X-band radars systems – such as the US Sea Based X-Band Radar, which is claimed to be the world's largest phased array X-band radar carried aboard a mobile, ocean-going semi-submersible oil platform – are increasingly using GaN RF devices

radar applications. As Wilson asserts, these manufacturers 'have not been sitting still and watching their business disappear' and have been developing smaller and smaller micro travelling wave tubes (TWTs) for high power and wideband RF transmission, that are similar in size to solid-state amplifiers.

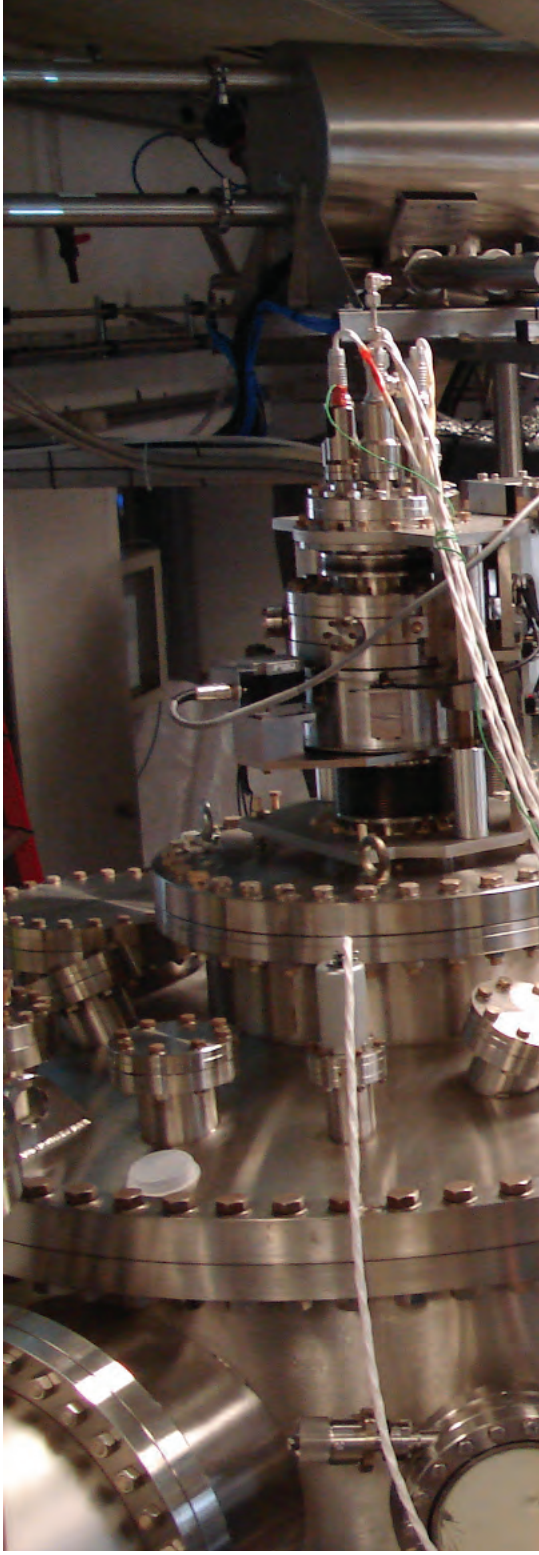
"The wide bandwidths of these TWT amplifiers are very difficult to replicate in solid state, so not all of the tube market will go over to GaN," he says. "And at very higher power – hundreds of kilowatts or megawatts of power – TWTs will never be replaced by solid -state amplifiers."

But when it comes to GaN, does Wilson see a winning technology emerging? Not yet.

While many manufacturers are focusing on GaN-on-SiC devices, US-based Nitronex, for example, is busy churning out GaN-on-silicon RF power devices based on its proprietary SIGANTIC manufacturing process. Here, buffer layers, including an AlN layer, are deposited on the silicon wafer, which in Wilson's words is 'not an easy process'.

"Most people are opting for the epitaxial GaN device on a SiC substrate as there is much better thermal matching," he says. "From a practical standpoint, GaN on silicon substrates are the way things are going, but which one is better from a technology standpoint? The jury is out."

Turbocharging channels with compounds



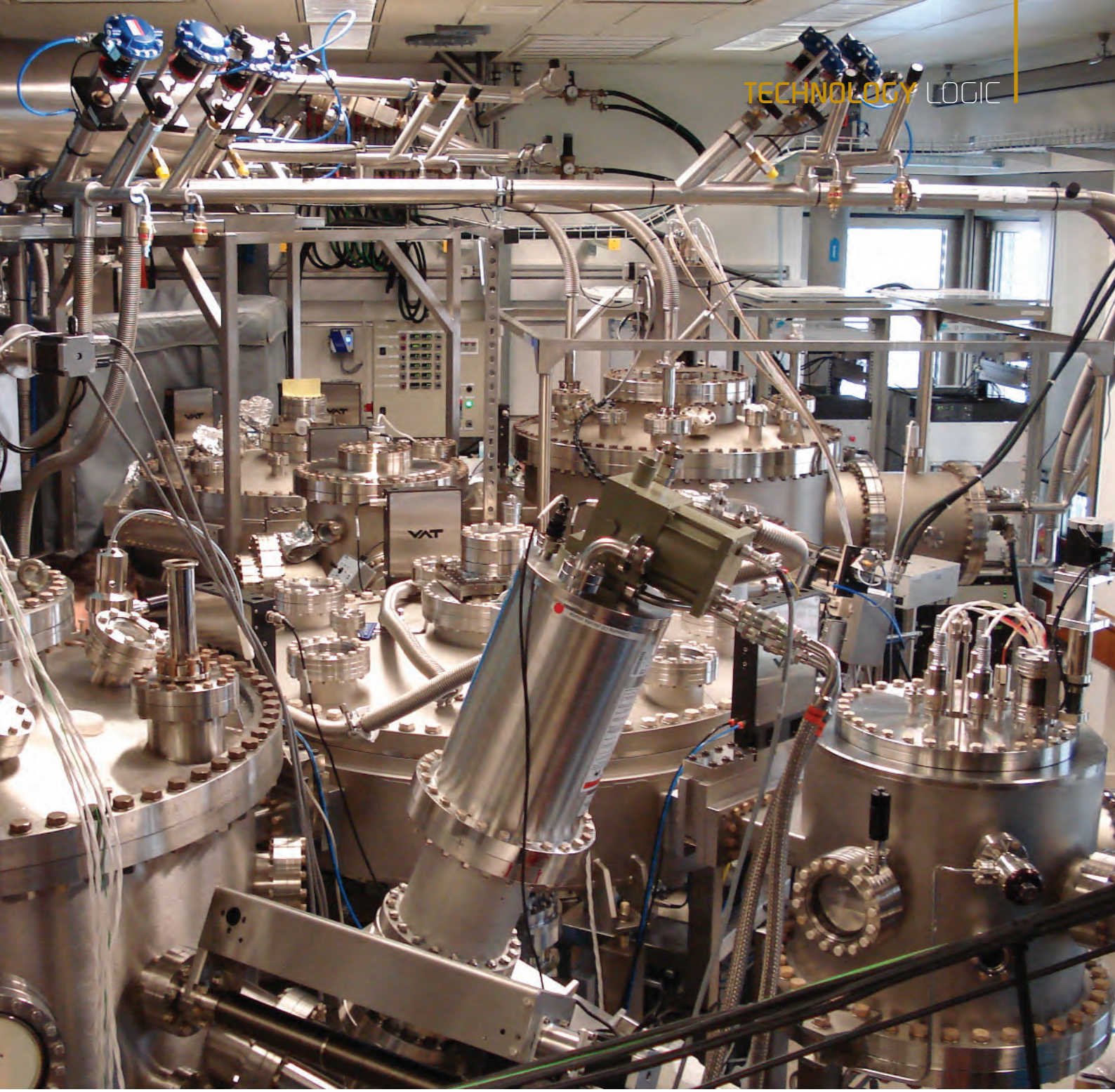
To maintain the improvements in efficiency that traditionally result from shrinking transistor dimensions, foundries will soon have to replace silicon channels with those based on higher mobility semiconductors. This move, a monumental upheaval for the silicon industry, could be easiest to implement by turning to engineered wafers with separate layers for the p-type and n-type transistors, argues Lukas Czornomaz from the Advanced Functional Materials Group at IBM Zurich.

FOUR DECADES of scaling CMOS technology has revolutionized our society. By making transistors ever smaller, faster, cooler, and cheaper, and being able to pack billions of them on the same chip, engineers have enabled the smartphone to become a commodity. This sleek, portable device has fundamentally changed the way we live: Now, wherever we are, we can be participating members of social networks and surfers of the web.

Performance of the smartphone will continue to increase, but it will not be easy to realise further gains in the computational capability of the chips that lie at the heart of these devices. That's because the microelectronic industry is facing some really serious challenges in shrinking dimensions beyond the 14 nm node.

Even getting as far as we have today has not been easy. For the last decade, pure geometrical scaling has failed to deliver the expected benefits in terms of performance and power consumption, and industry has gradually moved to innovation-driven scaling, bringing to market chips based on the likes of strained silicon-on-insulator, high-κ/metal gate technology and tri-gate devices. Now researchers everywhere are foreseeing that in the coming years, silicon – regardless of its form - will probably fail to meet the ultra-low power consumption targets imposed by the exploding demand of 'Mobile-Everywhere' applications.

The main lever for power scaling is the operating voltage of the chips. The target is to trim this from 0.8-0.9 V, which is where it stands today, down to 0.5 V. This cut in operating voltage must go hand-in-hand with a maintaining of the drive-current for the transistors, in order to ensure no reduction in performance. But realising this will not be easy. It will require the charge carriers in the



transistor's channel – either electrons or holes, depending on the particular transistor – to travel far faster from the source to the drain. Today, increases in the charge carrier velocity in silicon often result from the application of very high levels of strain in the material, but the opportunities for further gains are now minimal, especially for *n*-type transistors.

What is possible is that the next revolution in the semiconductor industry will come from the introduction of compound semiconductors as channel materials. Electron and hole mobilities in silicon are just 1400 $cm^2 V^{-1} s^{-1}$ and 450 $cm^2 V^{-1} s^{-1}$, respectively, and far higher values are promised by switching to carefully selected III-V and IV-IV compounds. For example, the electron mobility in InGaAs is in excess of 10,000 $cm^2 V^{-1} s^{-1}$, while hole mobility in SiGe can hit 1900 $cm^2 V^{-1} s^{-1}$. Using these materials to form the *p*-type and *n*-type transistors for CMOS chips would allow the indium and germanium content in the channels to become a new scaling parameter, gradually increasing the carrier velocity for each new technology node and thus improving performance while lowering power consumption.

Researchers will have to answer many questions before it is possible to build hybrid dual-channel CMOS circuits featuring very-large-scale integration (VLSI). They include: How do you get high-mobility channels on a silicon substrate with a good crystalline quality? How do you build nano-scaled devices based on III-Vs and SiGe that are compatible with VLSI? And how do you co-process both types of devices, given the fundamentally different thermal budgets and chemistries that they require?

A team at the IBM Zurich Research Laboratory in Switzerland has been focusing on finding answers to these questions for the last eight years.

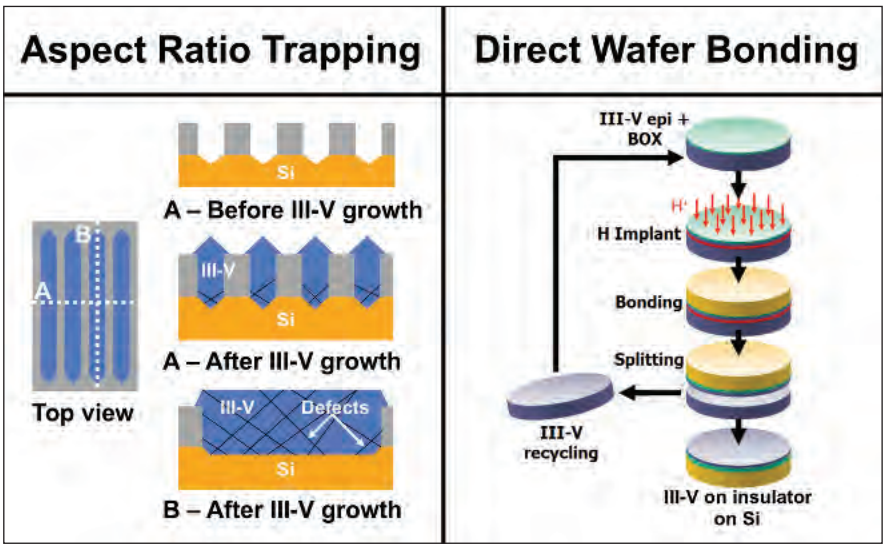


Figure 1. Comparison of the two main routes to integrate III-V on Si substrates: Aspect ratio trapping (on the left) and direct wafer bonding (on the right)

Efforts have now paid dividends: They have developed novel engineered substrates and process technologies for high-volume manufacturing in silicon foundries of VLSI circuits with compound semiconductor materials.

Silicon foundations

Although the microelectronic industry will have to undergo some big changes in the coming years, this will not include a change in substrate. So, to enable III-V and IV-IV compounds to be integrated in CMOS production, these materials will have to be introduced on a silicon substrate.

This is not easy, because integration of different, high-quality crystalline materials demands a matching of crystalline arrangement and lattice constant. While InGaAs, germanium and silicon have a similar crystalline arrangement, their lattice constants are significantly different: Compared to silicon, the average atomic spacing is about 4 percent larger for germanium and 8 percent larger for InGaAs. It is possible to manage the lattice mismatch for SiGe and germanium with some engineering tricks, but this is not possible with InGaAs, because the mismatch between this alloy and silicon is far too high. If attempts are made to grow InGaAs directly on silicon, strain in the ternary is so high that this material relaxes by forming an excessively large number of crystalline defects, which would significantly degrade device performance.

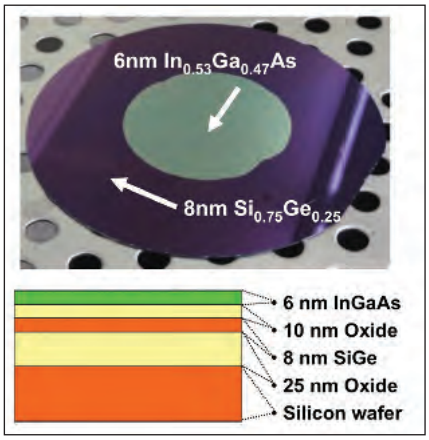


Figure 2. Photograph and associated cross-sectional illustration of a high-mobility dual-channel substrate which comprises a 6 nm thick InGaAs layer on a 8 nm thick SiGe layer on a silicon handling substrate

Today, to overcome this defect-related weakness, industrial researchers are pursuing two approaches. One of the options is known as aspect ratio trapping, while the other – pioneered at IBM – is called direct wafer bonding (see Figure 1 for an overview).

Aspect ratio trapping exploits the defined angles of the crystalline defects. The starting point is to take a silicon substrate and etch out a narrow trench – that is, one with a high aspect ratio, or in other words a groove with a height that is several times greater than its width. When III-Vs are grown directly in this trench, defects form at the interface and propagate along defined angles, before terminating on the trench walls. Thanks to this defect-elimination process, a low defect InGaAs crystal is created at the top of the trench. However, while this argument is applicable across the trench, where there is a high aspect ratio, it fails to hold true along the trench, where defects can propagate to the top channel material. This means that the channel material sitting on top of the trench is located on top of a defective semiconductor, which creates potential leakage paths from source to drain.

Aspect ratio trapping also restricts the availability of InGaAs. As this ternary is only present above the trenches, circuit designers are restricted in their positioning and sizing of the transistors. However, this issue disappears if the trenches can be tied together at a very small pitch, as required for the silicon fins of today.

Despite all these drawbacks associated with aspect ratio trapping, it still attracts a lot of attention, because it is directly compatible with silicon foundries that are now running 300 mm lines and could upgrade to 450 mm. However, foundries may find it much easier to pursue the technology that IBM is developing: direct wafer bonding.

With this approach, thin layers of III-Vs can be transferred onto silicon in the same manner already employed by industry to build silicon-on-insulator (SOI) substrates. Engineers simply grow the InGaAs layer on a donor substrate, before bonding it via an oxide to a target silicon substrate. The thin III-V layer is then released from the donor wafer to yield a III-V-on-insulator structure on silicon. This approach allows the donor wafer to be recycled, thereby maintaining the cost-efficiency of this process.

There are many attractive attributes associated with having a very thin III-V channel on an insulator. This combination is an ideal structure for maintaining good electrostatic control of the gate over the channel at short gate lengths, and it efficiently cuts leakage currents from source to drain. What's more, this combination enables the use of the back-biasing technique, which permits dynamic adjustments of the transistor's operation, so that it can be tuned to be faster or more power-efficient. All these merits reveal why III-V-on-insulator could be the preferred option for low power applications, such as mobile electronics.
The Zurich researchers have used wafer-bonding to create a hybrid, dual-channel

substrate that uses a thin insulator to separate a 6 nm-thick InGaAs film from an 8 nm-thick SiGe layer on a silicon substrate (see Figure 2). This engineered platform has enabled both channel materials to be integrated on the same substrate for the first time, while matching the thickness requirements of the 14 nm technology node. This breakthrough should pave the way towards the production of dual-channel CMOS circuits, where *n*-type transistors could be built on InGaAs and *p*-type transistors on SiGe.

III-V challenges

As readers of this magazine all know, III-V materials have been used for many years for the manufacture of myriad RF/analog chips, LEDs, lasers, solar cells and high-power devices. However, although a lot of know-how has been developed and accumulated over several decades, none of these applications require the fitting of billions of devices onto an area the size of a fingernail – a requirement imposed by CMOS chips. This additional constraint forces engineers and scientists to revolutionize the way III-V devices are fabricated, because gate lengths must be shorter than 20 nm, and, more importantly, contacts have to fit in less than 50 nm.

“As readers of this magazine all know, III-V materials have been used for many years for the manufacture of myriad RF/analog chips, LEDs, lasers, solar cells and high-power devices. However, although a lot of know-how has been developed and accumulated over several decades, none of these applications require the fitting of billions of devices onto an area the size of a fingernail – a requirement imposed by CMOS chips.”

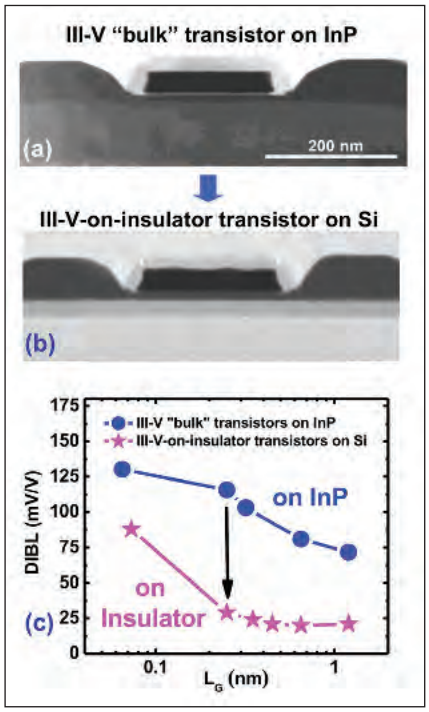


Figure 3. (a) Cross-sectional TEM view of a “bulk” self-aligned InGaAs transistor on InP featuring high-k/metal-gate technology and raised source-drain. (b) Cross-sectional TEM view of an InGaAs transistor fabricated with the same process flow but transferred on a III-V-on-insulator on Si substrate. (c) Comparison of DIBL versus gate length for both types of transistors showing up to a factor of five reduction for devices on insulator

These pre-requisites cannot be met by turning to different lithography levels to define the different elements of the devices, because transistors are way too small. Instead, a so-called self-aligned process has to be developed that enables the construction of all the different building blocks of the device with a single lithography step: the gate definition. By taking this approach, device dimensions and device pitches can be aggressively scaled to meet the requirements of VLSI integration.

In 2012, the Zurich team showed that it is possible to fabricate self-aligned InGaAs transistors. These VLSI-compatible devices feature a gate-first high-κ/metal-gate process with raised source-drain regions, which are just like those employed in industry for the manufacture of the most advanced silicon CMOS technology nodes.

The first ‘bulk’ transistors were fabricated on InP wafers (see Figure 3a), with successful operation down to gate lengths as small as 60 nm. The team then went one better, transferring the fabrication flow to III-V-on-insulator substrates on silicon, which had an InGaAs channel layer just 10 nm-thick (see Figure 3b).

Within the SOI industry, it is well known that this class of engineered substrate offers a large performance boost, thanks to the confinement of the carriers in a very thin channel and better electrostatic integrity. Superior performance translates to a reduction in the drain-induced barrier lowering (DIBL) of the transistors by up to a factor of five (see Figure 3c). DIBL is a key figure-of-merit for the electrostatic performance.

Further accomplishments by IBM Zurich include the construction of InGaAs transistors with a 24 nm gate and a gate-to-gate spacing of just 300 nm (see Figure 4). To date, they represent the smallest, most compact VLSI-compatible InGaAs transistors reported on silicon.

Dual channel developments

In addition to building standalone devices, the advanced dual-channel substrate technology can be used as a base for building small CMOS circuits. One of the benefits of this approach is that both channel materials are stacked on top of each other, so are present everywhere on the wafer. After defining some islands where transistors should be, the InGaAs channel can be removed to expose the SiGe channel where *p*-type devices are to be built (see Figure 5a). Although having both InGaAs and SiGe channels on the same wafer is an

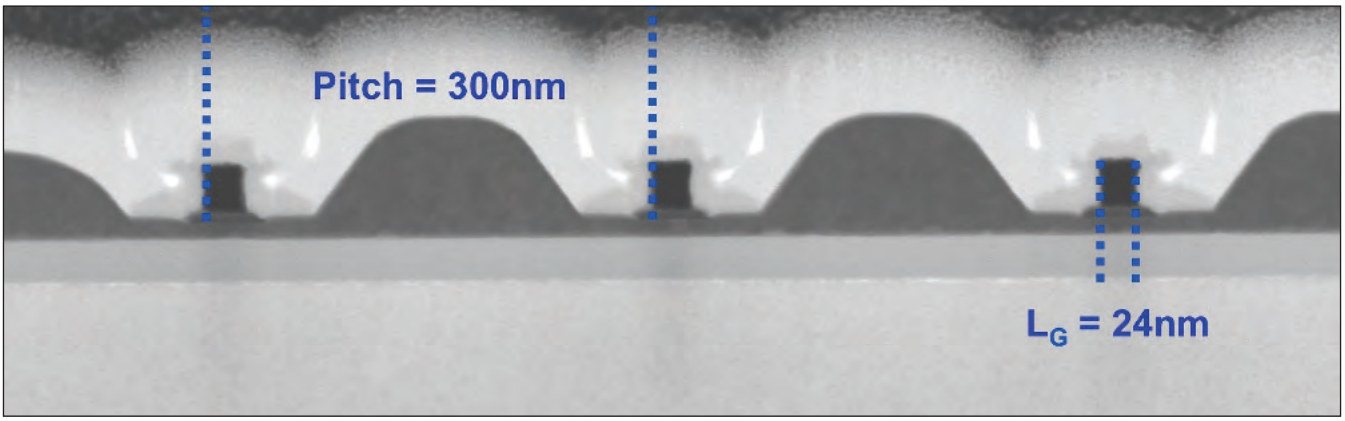


Figure 4 (above). Cross-sectional TEM view of densely packed InGaAs devices on silicon substrates with gate lengths of only 24 nm

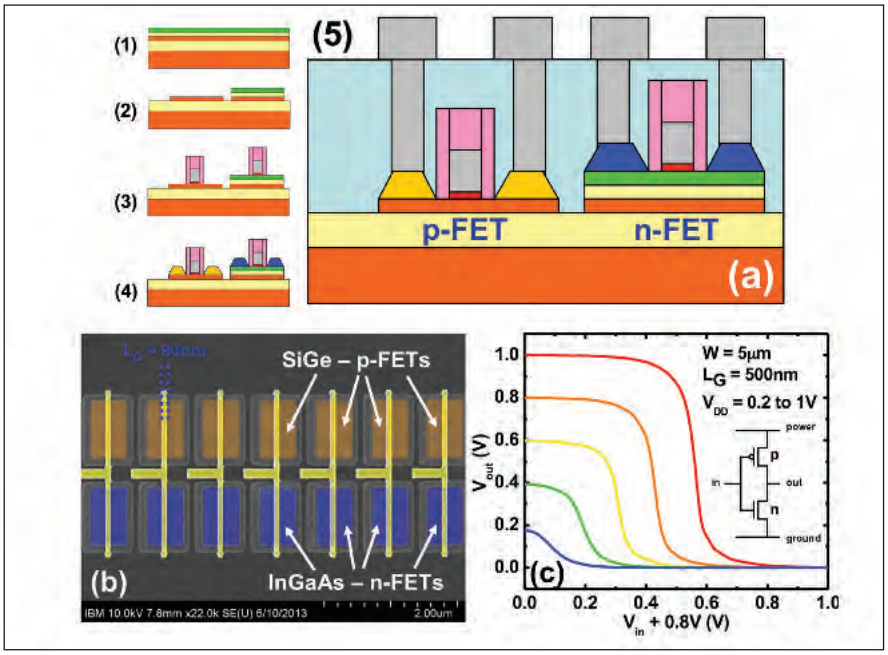


Figure 5. (a) Schematic process flow for the fabrication on hybrid InGaAs/SiGe CMOS circuits based on high-mobility dual-channel substrates. (b) Top-view SEM image on a dense CMOS inverter chain fabricated with 90nm design rules. (c) Hybrid CMOS inverter output characteristic showing a working circuit

enviable starting point, this comes at the penalty of more challenging material processing. InGaAs and SiGe exhibit fundamentally different chemical natures, so processes that work fine with one material can cause etching of the other. To address this, the researchers modified the fabrication flow for building InGaAs transistors on insulator, introducing new chemical cleans, passivation and etch-stop layers.

Thanks to all these developments, the team has have been able to demonstrate the first construction of dense arrays of CMOS inverters built with 90 nm design rules on silicon substrates that feature high-mobility channel materials (see Figure 5b). Inverters are the simplest logic block, and an important step towards the building of more complex CMOS circuits. Thus, by showing an InGaAs/SiGe inverter operating down to 0.2 V (see Figure 5c), the concept of using high mobility materials for CMOS has been validated. What's more, the door has been opened to further developments that could ultimately enable an up-scaling of the technology for high-volume manufacturing.

Clearly, the next steps are to build more complex CMOS circuits such as ring-oscillators and SRAM cells (a very common memory cell featuring six transistors). Armed with these circuits, the team will be able to assess the speed, performance and maturity of this advanced CMOS technology. However, the key test for this hybrid circuit will be to scale its dimensions to that of a state-of-the-art silicon chip and see how it compares. If it performs well, introduction in the foundries will then hinge on whether there are tough manufacturing issues associated with implementing this process. If these new channels materials make an impact, it will open up a new era for the microelectronic industry, where new functions are integrated into chips. It may not be long, for example, until the time comes when multi-core CMOS chips could communicate between cores with light via integrated III-V lasers, while making use of terahertz frequencies. So the promise of hybrid chips is awesome. However, as yet no one knows quite when – or exactly how – this is going to happen.

Further reading

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Addressing the weakness of GaN transistors

Researchers reveal how to slash dynamic resistance, minimise interface traps and identify the origin of current collapse.

BY RICHARD STEVENSON

THERE IS NO DOUBT that the GaN transistor has tremendous promise. Sales of this device, which can act as a switch in the likes power supplies, solar invertors and electric vehicles, are tipped to eclipse $1 billion before the end of this decade, according to market analyst Yole Développement.

However, it is by no means guaranteed that sales will soar to anything like that level. Today, this GaN transistor has several weaknesses that have to be addressed before commercial success can follow. Although the static on-resistance (R_{ON}) of these chips is superior to those of equivalent silicon devices, dynamic resistance is often much higher than that of the incumbents, and this severely compromises the overall performance of these wide bandgap transistors. Meanwhile, a less common but very promising form of the HEMT – that incorporates a metal-insulator-semiconductor (MIS) gate structure and has a lower leakage – has a number of shortcomings. The MIS-HEMT is plagued by threshold-voltage instability and a condition known as current collapse: a temporary increase in R_{ON} after high-voltage off-state biasing that arises from off-state trapping.

Insights into all of these issues and more were provided at the recent International Electron Devices Meeting (IEDM), which was held from 9-11 December in Washington DC. At this gathering, a team from FBH Berlin revealed how the dynamic R_{ON} in a GaN HEMT can be slashed by several orders of magnitude; researchers at The Hong Kong University of Science and Technology reported new insights into interface-induced instability in the threshold voltage of MIS-HEMTs; and a partnership between MIT and Texas Instruments explained why Zener trapping is the origin of current collapse in this class of transistor.

Dynamic improvements

Many have argued that the superiority of the GaN transistor over its silicon rival is captured in a figure of merit for switching efficiency: the product of on-state resistance and gate charge. Compared to commercial silicon devices, many GaN HEMTs made by industry and academia have an R_{ON} that is typically an order of magnitude lower. Unfortunately, such claims of supremacy neglect the difference in the dynamic on-resistance of silicon and GaN devices. "If, for example, you have a 600 volt switching device, and you have an improvement in the static R_{ON} by a factor of ten [by moving from silicon to GaN], but at the same time you will worsen the dynamic switching R_{ON} by a factor of a hundred, there is no use in that," points out Hans-Joachim Würfl from FBH Berlin.

This has led a growing number of GaN developers to take increasing interest in the dynamic resistance of their devices. Resistance tends to have a high value due to temporary charge trapping, which is one consequence of switching. Negative charge trapping often occurs close to the channel, near to the drain-side-edge of the gate. The flow of electrons through the channel is impeded until the trapped charges are emptied, leading to increased conduction loss and compromised system efficiency.

At IEDM, Würfl detailed approaches for realising a dynamic R_{ON} that is comparable to a static R_{ON} in GaN HEMTs designed for switching at 500 V. "That was not imaginable a couple of years ago, when we had a factor of thousand [difference in dynamic and static R_{ON}]."

A study of various HEMT structures uncovered refinements to the device architecture that can slash dynamic R_{ON}. To perform this investigation, engineers fabricated a range of GaN transistors on *n*-type SiC with differing buffer compositions. Normally off devices were fabricated using *p*-GaN gate technology and had a gate length of 1.2 μm, while normally on variants were based on a 0.7 μm Ir/Ti/Au gate technology. All devices were passivated with benzocyclobutene layers, and to prevent spurious vertical leakage and boost yield, source and drain fingers were additionally isolation-implanted at their centre (see Figure 1).

Würfl believes that if the improvements to dynamic R_{ON} are to be worthwhile, they must not come at the expense of a severely compromised breakdown voltage per micron: "The breakdown strength tells you how large you can make the gate-drain distance. Of course, you would like a very small, safe, gate-drain distance, because if this is very small, the static on-state resistance is decreased."

The requirement for a high electric field strength that allows a shorter gate-drain separation rules out doping the buffer with iron and adding an AlGaN buffer: dynamic R_{ON} is reduced with

> At IEDM, Kevin Chen's group from The Hong Kong University of Science and Technology unveiled its deposition process for forming a MIS structure, and also detailed a new approach to characterising the interface traps in MIS-HEMTs. The latter is a tricky task, due to the presence of two interfaces: that between the dielectric and III-N, and that between AlGaN and GaN.

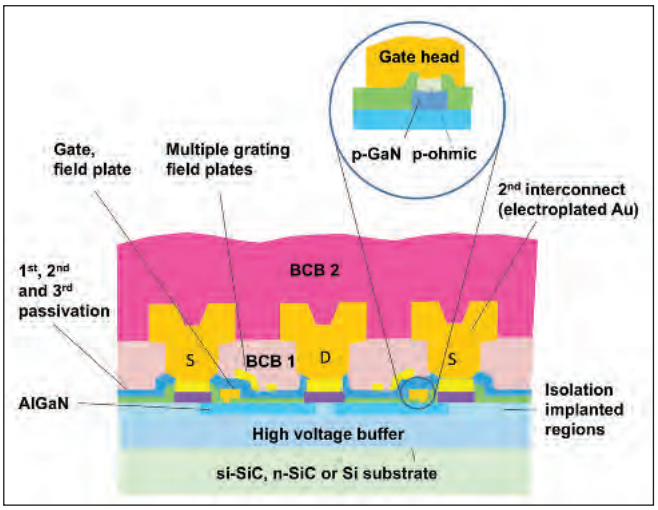


Figure 1. GaN-based high-voltage switching devices developed at FBI. The normally on and normally off devices are fabricated using the same technology, with the exception of the gate module. The inset show details related to the p-type GaN technology, which renders the devices normally off

this approach, but the breakdown strength is just 40 or 50 V/μm, about a third of what is theoretically possible. Simply doping the buffer with carbon is also inappropriate, because although this boosts breakdown strength, it also increases dynamic R_{ON}.

To realise a high field strength and a low R_{ON}, the team from FBH has drawn on both of these approaches. Its best test structure features a graded AlGaN barrier with an average aluminium concentration of 5 percent, which is positioned close to the channel, and a carbon buffer that is doped to 4×10^{18} cm^{-3} and inserted underneath regions that are not prone to large field changes during switching. With this carefully selected combination, HEMTs that switch at 500 V can exhibit a breakdown field strength of 80 V/μm and a produce a dynamic R_{ON} that is just two-and-a-half times that of static R_{ON}.
Time dependency measurements reveal that immediately after switching from the off-state, the dynamic R_{ON} of the HEMT decreases rapidly, before flattening out and getting fairly close to its static value after 100 μs. Decline in dynamic R_{ON} is not exponential, but can be fitted by multiple exponential functions, suggesting that several different trap states are contributing to charging and discharging within the device.

Würfl and his co-workers are now trying to make further improvements to dynamic R_{ON}. This effort forms part of a project involving a large European company, which requires further gains to deliver a competitive product. "Otherwise the difference between [GaN HEMTs and] the very-good-performing silicon is getting smaller and smaller, and there would be a question whether someone would pay the higher price, even if it were for GaN-on-silicon," says Würfl. The team also hopes to increase the breakdown strength of its devices. "I think we could go to 120 V per micrometre," says Würfl, who believes that this is realistic while maintaining the value for dynamic R_{ON} achieved in HEMTs with a breakdown of 80 V/μm.

Interface traps

For high-voltage power switches, the MIS-HEMT is favoured over the more common Schottky-gate HEMT because it is capable of delivering a lower gate leakage current and an enlarged gate swing. However, this more promising class of transistor tends to be plagued by a high density of traps at the interface between the dielectric and the III-N. The dynamic charging and discharging of these traps has been blamed for instability in the transistor's threshold voltage. To address this issue, engineers from The Hong Kong University of Science and Technology have developed a deposition process that yields a high-quality interface. "We believe that we have gotten to the heart of the problem and developed an effective solution," claims team-leader Kevin Chen.

At IEDM, this group unveiled its deposition process for forming a MIS structure, and also detailed a new approach to characterising the interface traps in MIS-HEMTs. The latter is a tricky task, due to the presence of two interfaces: that between the dielectric and III-N, and that between AlGaN and GaN.

Chen's team form a high-quality MIS structure by employing an *in-situ*, low-damage remote plasma treatment to remove the native oxide and add a nitridation inter-layer. After this, they deposit a gate dielectric. Components of the plasma, NH_3-Ar-N_2, perform different roles: NH_3-Ar removes the native oxide, while the N_2 enables deposition of the nitridation inter-layer. On top of this, engineers deposit, *in-situ*, a 25 nm-thick layer of Al_2O_3, before the entire structure is annealed at 500 °C under oxygen.

Interface traps in the MIS-HEMTs were uncovered by analysing the frequency- and temperature-dependent onset of the second slope in the current-voltage characteristics. Using frequencies varying from 400 Hz to 10 MHz and temperatures from ambient to 200 °C, engineers determined an interface trap density of $10^{12} - 10^{13}$ cm^{-2} eV^{-1}.

Monolithic circuits

In a separate paper presented at IEDM, Chen and his co-workers claimed the first demonstration of a form of GaN-based high-voltage start-up circuit – one with low standby-power consumption and designed for off-line switch-mode power supplies. This mode of power supply is used in personal computers, battery charges, central power distribution systems, consumer electronics and LED lighting.

To form their monolithic circuit, the engineers used E-mode and D-mode HEMTs, rather than the more conventional Schottky-gate HEMTs (see Figure 2). According to Chen, two of the strengths of the E-mode MIS-HEMT over its conventional cousin

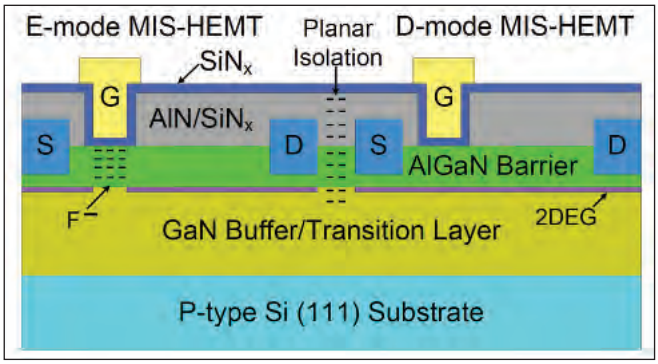


Figure 2. Engineers at The Hong Kong University of Science and Technology have produced monolithic integrated circuits with E-mode and D-mode MIS-HEMTs

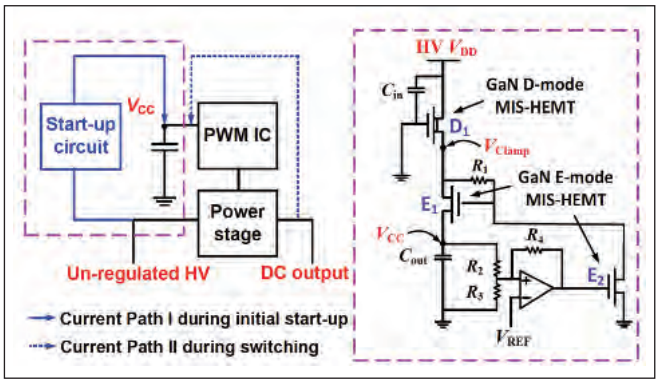


Figure 3. The switch mode power supply produced by the team at The Hong Kong University of Science and Technology contains three GaN MIS-HEMTs

are: a larger positive threshold voltage that enables enhanced electromagnetic interference immunity; and a larger gate swing, which increases the compatibility with existing silicon-based gate driver ICs. The D-mode MIS-HEMT also has its merits, being more suitable than a conventional equivalent for the large negative threshold voltage – typically -5 V or more – needed in the start-up circuit.

The epitaxial structure used for making the 600 V MIS-HEMTs for the IC was deposited on silicon and contained a 21 nm-thick GaN/$Al_{0.25}Ga_{0.75}N$/AlN barrier layer and a 3.8 μm-thick GaN buffer. Device fabrication involved electron-beam evaporation of Ti/Al/Ni/Au source and drain contacts, deposition of an AlN/SiN passivation layer and planar isolation of active regions by fluorine ion implantation. After opening the gate window, ions were applied to the gate region of E-mode devices. This was followed by the NH_3-Ar-N_2 plasma treatment process previously decsribed, deposition of a 17 nm-thick film as the gate insulator, and the addition of a Ni/Au gate electrode.

Chen says that one of the highlights of the team's device technology is its passivation process, which leads to effective suppression of current collapse and a very small dynamic on-resistance. E-mode MIS-HEMTs have a high threshold voltage of 3.6 V and a large gate swing of 14 V, thanks to integration of fluorine implantation, surface nitridation and the gate dielectric processes. Supplied with an input of 200 V, the power supply circuit (see Figure 3) has a start-up current of 1.07 mA, a start-up time of 65 ms (with a 10 μF output capacitor), and a stand-by power that is calculated to be 2.1 mW. "The performance is comparable to a silicon-based circuit in terms of the start-up current and standby power consumption," says Chen.

According to him, the ultimate goal for his team is to build a circuit with GaN for a highly efficient, compact, off-line switch-mode power supply. "The hysteresis comparator in the start-up circuit can be achieved using GaN E/D-mode HEMTs or MIS-HEMTs, which has not been done in this work yet." If the circuit is to demonstrate commercial viability, it must also pass reliability tests involving operation under extreme conditions for lengthy periods.

Zener trapping

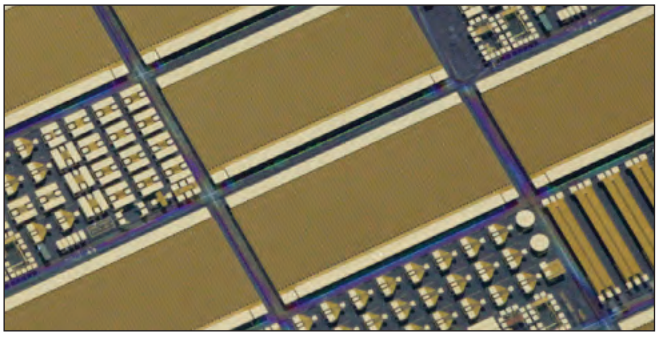
The weakness referred to as current collapse, the temporary increase in a GaN transistor's R_{ON} after high-voltage off-state biasing, is known to result from excessive trapping. Its precise origin, however, has been something of a mystery – but it is starting to unravel, with a team from MIT and Texas Instruments claiming at IEDM that current collapse stems from high-field, tunnelling-induced electron trapping. These researchers studied this phenomenon in AlGaN/GaN MIS-HEMTs with a breakdown voltage greater than 600 V. Devices were fabricated from a 6-inch III-N-on-silicon epiwafer supplied by a commercial vendor.

Step-stress measurements were made on these transistors by increasing the drain-source voltage by 20 V every 10 s. Linear drain current, which is inversely proportional to R_{ON}, degraded by about 10 percent as the voltage approached 200 V, before abruptly dropping to 10 percent of its initial value. Further degradation occurred as the voltage was cranked higher, with the linear drain current becoming negligible and R_{ON} increasing by around 10 orders of magnitude. However, this damage is fully recoverable – initial device characteristics recovered with strong UV illumination or moderate thermal treatment, such as heating for 3 hours at 100 °C.

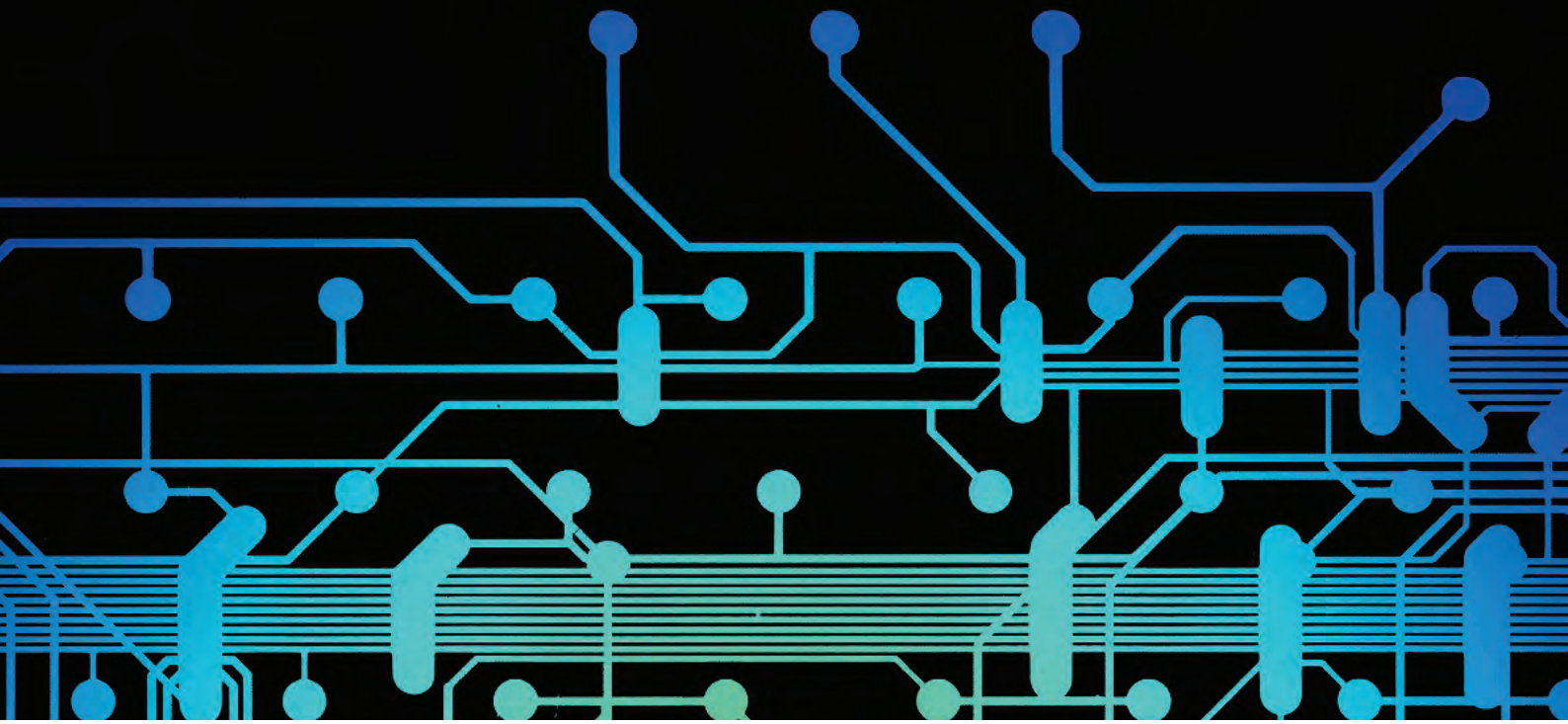
To increase the operating voltage of GaN MIS-HEMTs, many developers have turned to multiple gates that may also prevent current collapse – although their effectiveness to address the later issue is unclear. To try and resolve this, the US team investigated the influence of device geometry. They found that the lengths of the three field plates used in the transistor do not impact trapping characteristics.

A study of the dynamics of trapping followed, involving plotting of trapping time as a function of the reciprocal of the peak electric field, which occurs inside the AlGaN barrier and under the edge of the third field plate. The shape of this graph strongly suggests that the origin of current collapse is a valence-band-to-trap tunnelling process, which the team refer to as Zener trapping. Substitutional carbon on nitrogen sites is suggested to be a primary culprit. Team-member Donghyun Jin says that if carbon is to blame, it should be minimised in the GaN channel and AlGaN barrier to reduce Zener tunnelling. "However, its concentration in the buffer should be retained high enough to achieve high resistivity and a high level of breakdown voltage."

So, a delicate balancing act is recommended, just as it is to realise the combination of a high breakdown voltage and low on-resistance in conventional HEMTs. Optimising these trade-offs will take time, but progress may well be reported at papers given at the next IEDM, which takes place in December in San Francisco.

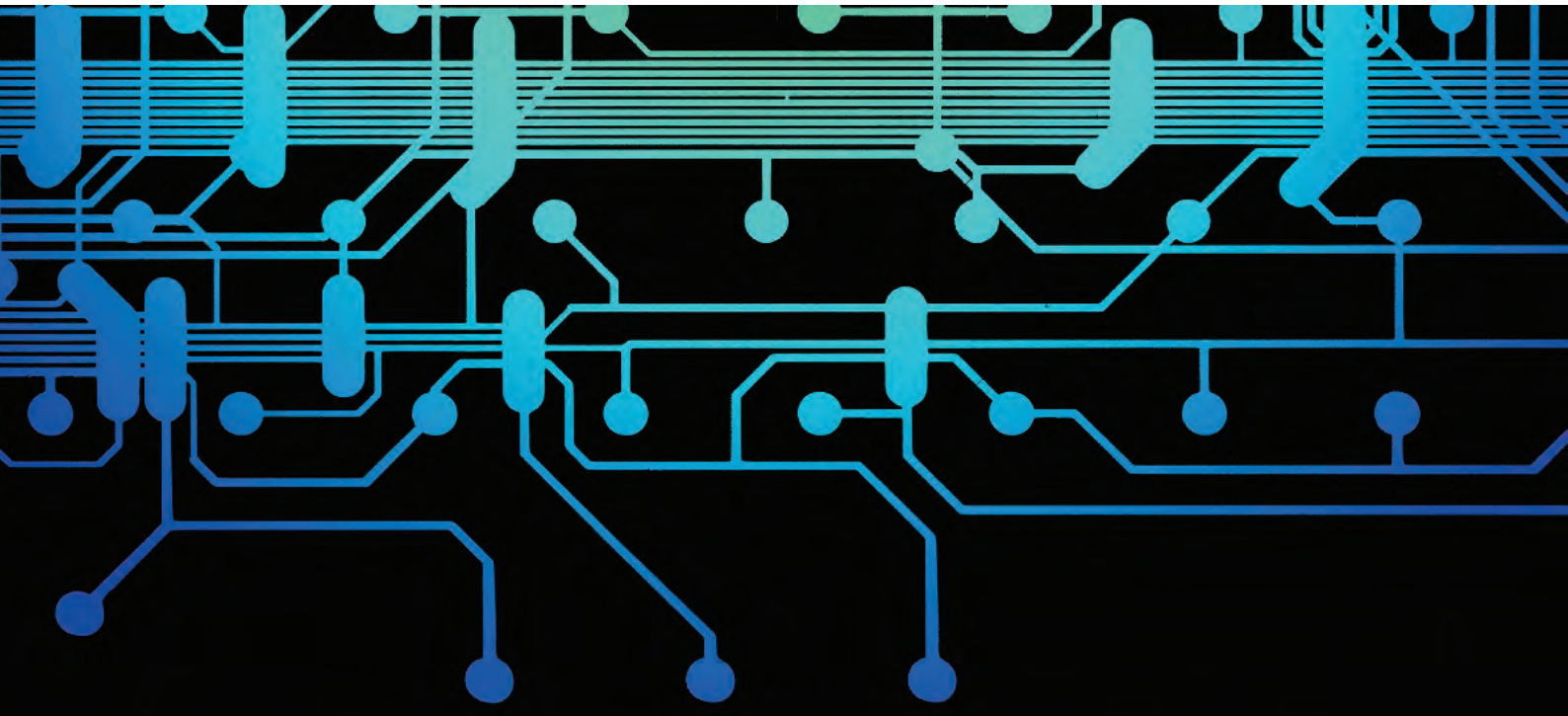


Devices made by FBI on SiC substrates



Bringing the inverter onto the chip

Monolithic integration of LEDs and transistors is helping to usher in a new era for solid-state luminaires, where the emitter and its control electronics are united on single chip. By Zhongda Li and co-workers from The Smart Lighting Engineering Research Centre at Rensselaer Polytechnic Institute.



THE DRIVING CONDITIONS for the LED could hardly be more different from the output from the mains. While the LED needs just a few volts of direct current, mains delivers an alternating current at voltages ranging from 110 V to 250 V, depending on the country.

To address this difference, solid-state light bulbs contain an AC-to-DC power converter to modify the supply from the mains into a form that can drive the LEDs. The electronic driver actually carries out several roles, including maintaining a stable light output when the temperature of the LED chips change, and providing functions such as dimming and colour tuning.

Today, the electronic driver circuits for LED bulbs are assembled from various discrete components, such as power transistors, capacitors and logic controller ICs. These are connected together on a printed-circuit board (PCB), which is usually bulky – it can take up as much space as the LEDs.

The perfect solution for the future of solid-state lighting is to monolithically integrate the LEDs, power transistors and controller ICs on a single chip. Since the LEDs in the bulb are based on GaN, all the devices must be built with this wide bandgap material.

Taking this approach will eliminate the parasitic inductance, capacitance and resistance between the driver board and the LED chips, and thereby allow the lighting system to operate at far higher switching speeds. In turn, this could boost efficiency and enable a trimming of the size of the passive components, as smaller inductors and capacitors can be used at higher frequencies. The upshot of all of this would be more frugal driver circuits with a smaller form factor than the current PCB solution.

Thanks to recent breakthroughs in GaN power device technologies, the building blocks are in place to form the electronic driver circuits with this material system. Power switching transistors, which are the key components in LED driver circuits, have already been made in GaN, and they show outstanding performance: Compared to conventional silicon transistors, they have a higher breakdown voltage, lower specific on-resistance and a higher operating frequency. In addition to these material property advantages over silicon, GaN can be made into HEMTs that exploit two-dimensional quantum confinement at the heterojunction to boost electron conduction. And on top of that, by combining a GaN HEMT structure with the metal-oxide-semiconductor (MOS) gate, it is possible to create a hybrid device structure called a MOS-channel HEMT. This has a positive threshold voltage, an extremely low gate leakage current, and is easy to drive.

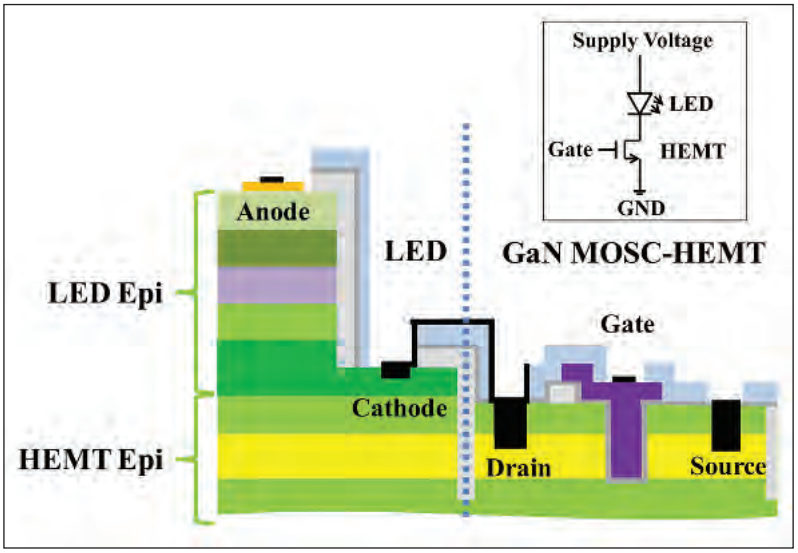


Figure 1. Monolithic integration of LEDs, power transistors and logic ICs in GaN

At the Smart Lighting Engineering Research Centre at Rensselaer Polytechnic Institute we have drawn on all these device technologies to demonstrate the world's first monolithic integration of GaN LEDs and MOS-channel HEMTs (see Figure 1). This accomplishment – which involved using a unified process to fabricate both classes of device on single GaN-on-sapphire wafer (see Figure 2) – is an important stepping-stone to making an LED bulb from an emitter and electronic control circuit on a single chip.

We commenced fabrication with MOCVD growth of a GaN LED structure on a commercial HEMT epiwafer, which was formed on a sapphire substrate. LED growth involved deposition of a 0.5 μm-thick *n*-type GaN film, followed by a

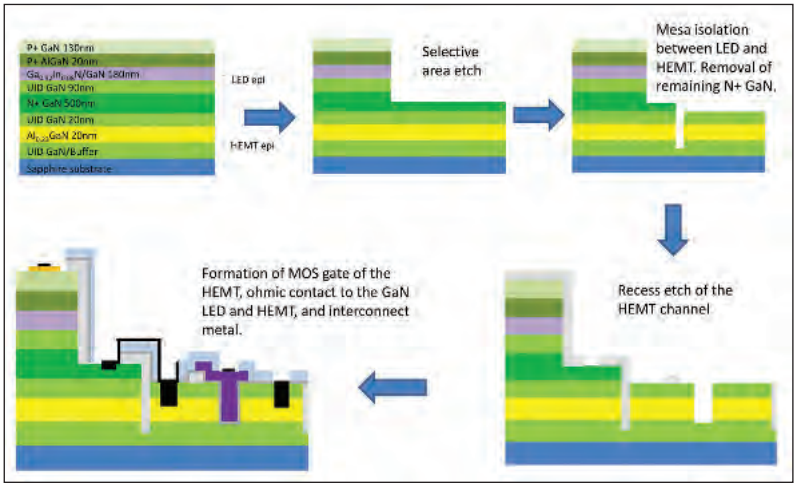


Figure 2. Process flow of the GaN LED and MOS-channel HEMT integration using selective epi removal

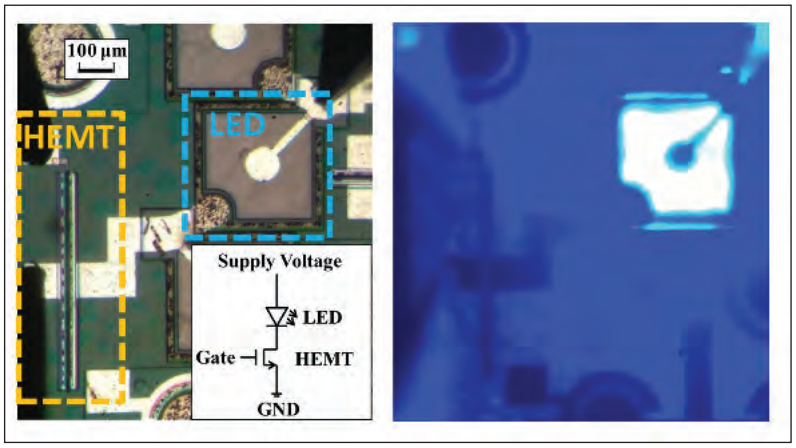


Figure 3. Optical images of the integrated GaN LED/HEMT pair in off-state (left), and with the LED lighted up (right). Inset in (a): the schematic view of the circuit configuration

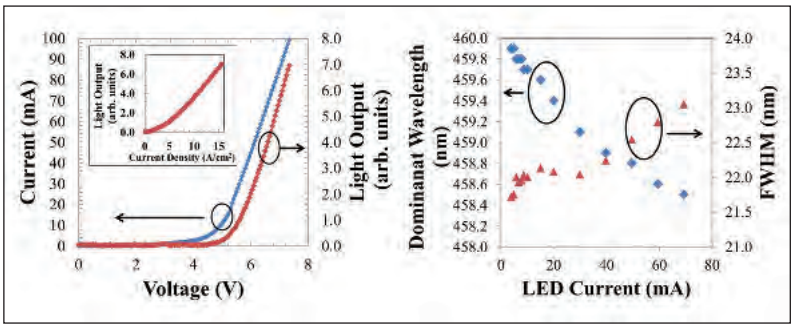


Figure 4. Characteristics of the integrated GaN LED

multiple quantum well structure and finally *p*-type GaN layers.

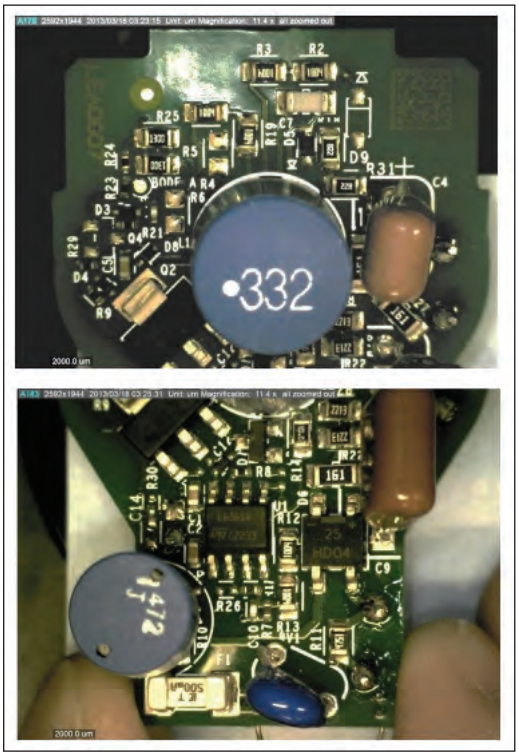
Formation of our circuit began with a chlorine-based, inductively couple plasma reaction-ion etch of selected regions of the LED structure to expose the *n*-doped GaN. Further etching defined trenches between GaN LED and HEMT, isolating these devices. After that, we removed the remaining *n*-type GaN that was on top of the HEMT, located where the MOS-channel HEMT would be fabricated. Following this, electron beam lithography patterned submicron recess channels of the MOS-channel HEMTs. These are etched, with a subsequent wet chemical process removing any damaged that occurred.

After cleaning this structure, we deposited SiO_2 as a gate dielectric, followed by polysilicon as the gate electrodes. The ohmic contacts of the MOS-channel HEMTs and the cathode contact of the LEDs were formed at the same time. After this, the anode contacts of the GaN LED were added. Finally, the cathode of the LED was connected to the drain of the MOS-channel HEMT.

The blue-emitting LED that resulted has a dominant wavelength of 459 nm, a full-width half-maximum as narrow as 22 nm and produces a relatively linear increase in light output with current (see Figures 3 and 4). These characteristics show that it is feasible to integrate a GaN LED with a GaN MOS-channel HEMT process. Current-voltage characteristics for the integrated LED and HEMT are consistent with the expected behaviour for a transistor and diode connected in series: Current is limited by the LED before it turns on, and afterwards it is restricted by the transistor's saturation current. The intensity of the LED light is fully modulated by the gate voltage of the MOS-HEMT with good linearity (see Figure 5). High temperature operation of the integrated GaN LED/transistor pair has been demonstrated up to 225 °C.

Our monolithic integration demonstrates the process compatibility of GaN LEDs and GaN transistors, and in particular an approach to unifying a GaN transistor with a MOS gate. This is a noteworthy achievement, because the MOS gate process usually requires a higher thermal budget than the Schottky gate process used in the GaN HEMT.

The MOS gate is not just an essential element in a power transistor – it also holds the key to the future of the GaN CMOS IC platform. Integrating a GaN LED and transistor is the first step towards the creation of the light-emitting power ICs (LEPICs) platform, where a single chip contains LEDs, power transistors and logic ICs. Constructing LEPICs could revolutionise solid-



Driver circuit board of a commercial LED light bulb (Courtesy to Casey Goodwin, Smart Lighting ERC, RPI)

state lighting, because such a platform could play an important role in LED control technologies and add functionalities required for emerging lighting applications. One example of this is visible light communication (VLC), also known as Li-Fi, where the visible spectrum is used for free-space optical communication.

This technology is ideal for localized high-volume data transmission in the office and the home. The frequency of visible light is in the range of hundreds of terahertz, so VLC has the potential for a much higher data capacity than that possible with a conventional wireless RF network. Flickering of the light source will not be an issue, because the on and off modulations that provide data transmission will occur at far higher speeds than the human eye can perceive. Meanwhile, the small form factors of the LEPICs also make them suitable for distributed lighting, with each light source serving as an independent data channel. Living in such a world, LED bulbs will not only be at the forefront of lighting – they'll also be a big player in wireless technology.

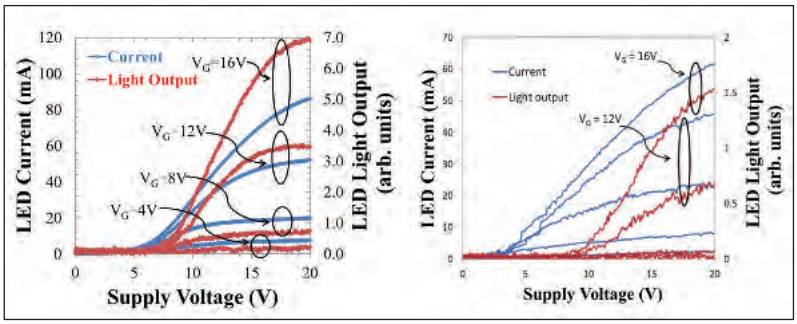
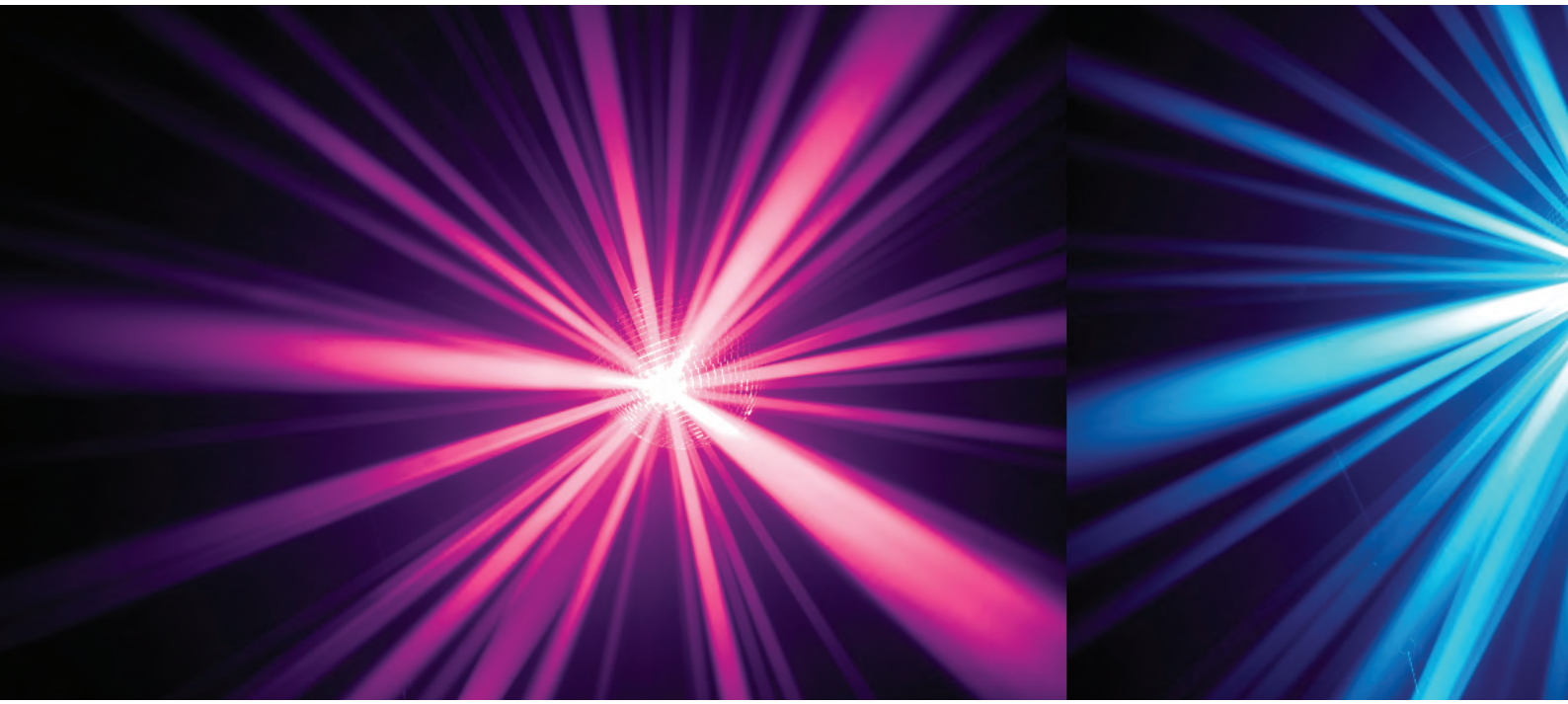


Figure 5. LED current and light output intensity as a function of the supply voltage and the gate voltage of the GaN MOS-channel HEMT at room temperature (left) and at 225 °C (right)

Further reading:

R. Karlicek, "Smart lighting – beyond simple illumination," in IEEE Photonics Soc. Summer Topical Meeting Series, Seattle, WA, 2012, pp. 147-148.
T. P. Chow and Z. Li, "Recent advances in high-voltage GaN MOS-gated transistors for power electronics applications," in GaN and ZnO-based Materials and Devices. Berlin, Germany: Springer, 2012, pp. 239-250.
Z. Li *et. al.* Appl. Phys. Lett. **102** 192107 (2013)



The evolving GaN VCSEL

Building a GaN VCSEL is far harder than making one from GaAs, but progress is being made through the introduction of different types of mirrors, alternative current injection schemes and new crystal orientations.

BY DANIEL FEEZELL FROM THE UNIVERSITY OF NEW MEXICO.

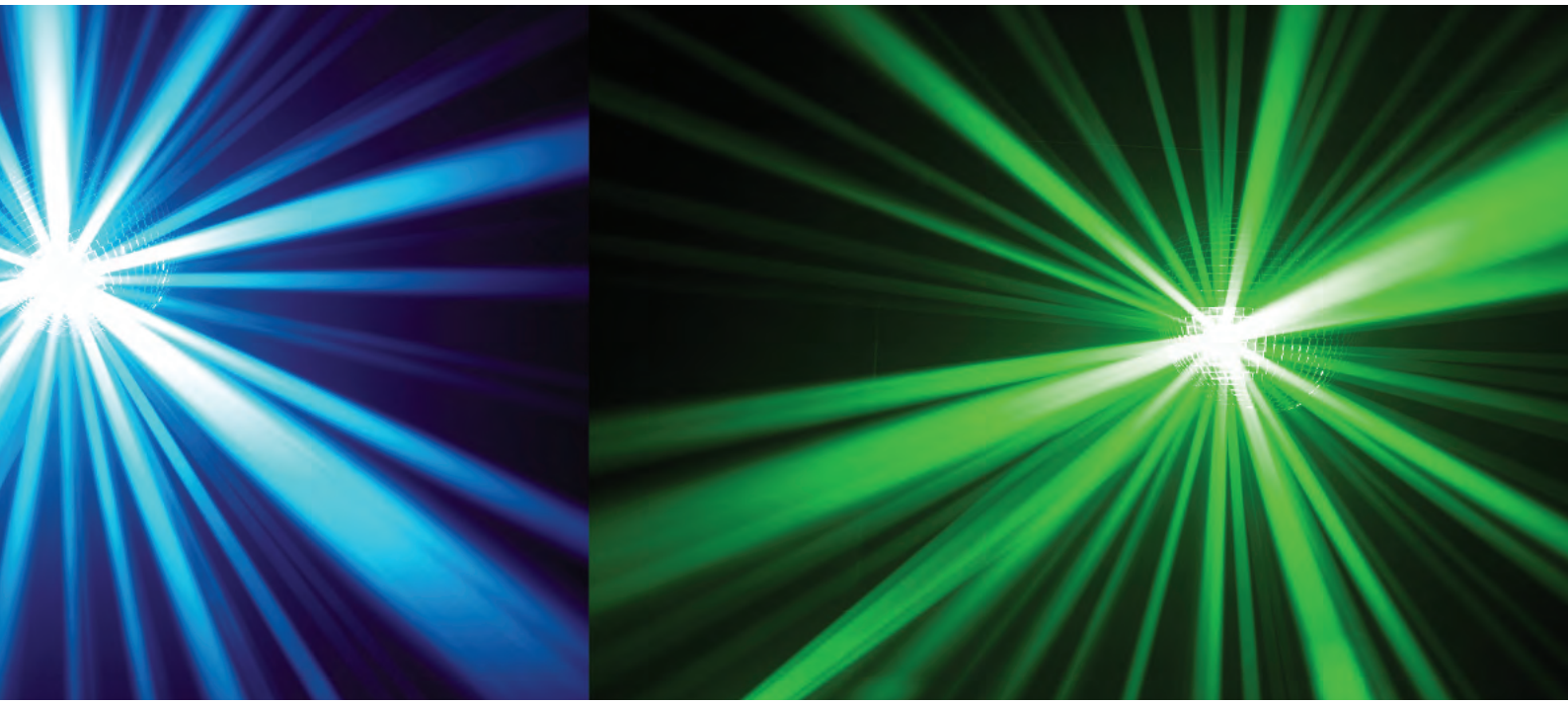
THE VERTICAL-CAVITY SURFACE-EMITTING LASER (VCSEL) has several advantages over its edge-emitting cousin. Superiorities include a lower threshold current, direct modulation at high speeds, a circularly symmetric output beam, wafer-level testing and the option to form densely packed, two-dimensional arrays. Thanks to the geometry of this class of laser, monolithic processing of large batches of devices is possible, and there is no need for cleaving, facet coating and bar handling. Consequently, the VCSEL can combine relatively low manufacturing costs with great performance.

Origins of the device can be traced back to 1977, when Kenichi Iga from Tokyo Institute of Technology first proposed this class of laser. Commercialisation followed in the 1990s, and the VCSEL is now serving a wide range of applications, including fibre optic communication networks, optical interconnects, data storage, sensing and laser printing.

As the VCSEL has evolved, researchers have expanded the range of material systems that can be used to produce this device, cut threshold currents to sub-milliamp levels and increased output powers. They are now in excess of 7 mW for single-lateral-mode devices and beyond watt-level for multi-lateral-mode devices. Error-free serial data rates have also increased significantly, with recent demonstrations exceeding 50 Gbit/s.

These impressive figures suggest that the VCSEL has no weaknesses. But that's not true. Although this chip delivers very high levels of performance when emitting at the standard wavelengths of 850 nm and 980 nm, it has been very challenging to stretch emission to 1310 nm or 1550 nm, the wavelengths used for long-haul data transmission in optical fibre. Shifting the output to shorter wavelengths has also been tricky, and this has prevented the VCSEL from being used in high-resolution printing, high-density optical data storage, head-up displays, backlighting and chemical/biological sensing (see Figure 1).

Here, we will look at the challenges of fabricating VCSELs that are based on the III-N materials system and span 400 nm to 550 nm. Some impediments to forming this device are very similar to those for



making long-wavelength VCSELs with InP-based materials: a lack of a lattice-matched material system for forming high reflectivity mirrors; the difficulty of realising efficient current spreading layers; and the challenge of producing robust confinement, for both the current and the optical mode. However, the nitrides also presents some additional, substantial complications.

VCSEL challenges

To understand why it is so difficult to make a GaN-based VCSEL, one must first understand how this device operates. It is formed by sandwiching a thin active region between parallel mirrors, and it features a cavity length of a few microns – that's hundreds of times shorter than that of an edge emitter.

The short cavity length enables high-speed direct modulation, thanks to the small photon volume. However, the gain per round-trip pass through the cavity is far less than that for an edge-emitter. To compensate, cavity loss must be very small, and thus the reflectivity of the mirror, which is a distributed Bragg reflector (DBR), must be very high – it has to be of the order of 99 percent.

With a GaAs-based VCSEL, it is relatively easy to form such a high reflectivity. Engineers just have to form a stack of lattice-matched, quarter-wavelength thick alternating layers of GaAs and AlGaAs, which can both be doped, thereby enabling electrical injection into the cavity. Replicating this approach with the III-Ns has proved impossible, so far, because there are no straightforward methods to form lattice-matched, highly reflective conducting mirrors. This had led several groups to introduce new types of device structures, which either combine an epitaxial DBR with a dielectric one, or employ dielectrics for both mirrors (see Figure 2).

Another consequence of the VCSEL's short cavity length is the complex standing-wave profile of the electric field intensity. To optimise laser performance, it is essential to position the active region at the peak of this standing wave, while aligning lossy layers, such as heavily doped layers, at a standing wave null. Very precise control of the cavity length is needed to realise this. This is readily achievable in all-epitaxial structures, but more challenging in devices that feature double dielectric DBRs and are formed with substrate lift-off or thinning.

A lack of conductivity in the mirrors used in a GaN VCSEL makes it harder to deliver uniform current injection into the active region, and ultimately to realise high modal gain. Carriers are introduced into the active region with sophisticated current injection schemes, such as single or double intra-cavity contacts. With these approaches, a highly conductive layer spreads the current laterally, prior to injection into the active region.

III-nitrides are unsuitable for current-spreading, due to their very low conductivity. Better is the semi-transparent material indium tin oxide (ITO), but even its conductivity is insufficient to prevent current spreading issues for device apertures greater than 10 μm in diameter. ITO also has significant optical loss in the visible, making the placement of this layer critical to device performance.

A further challenge for the GaN-based VCSEL is current confinement. It is tricky to do this with selective oxidation, a process that is repeatable and reliable for manufacturing GaAs VCSELs. So researchers have turned to current confinement schemes that include patterning apertures in SiO_2 or Si_3N_4 and selective-area surface passivation via reactive ion etching of *p*-GaN.

Challenges unique to GaN

On top of the challenges just highlighted, III-nitrides have their own materials issues. Devices grown on the most common GaN plane, the *c*-plane, are hampered by polarization-related electric fields within the active region that impair material gain and increase threshold currents. Device progress is also held back by the high-cost and limited availability of high-quality native substrates, which are needed to realise epilayers with acceptable defect densities. But even if this native foundation is used, high-quality epilayer growth is tricky, due to the lack of lattice

Figure 1: Applications for GaN-based VCSELs include high-density optical data storage, displays, high-resolution printing, and chemical/biological sensing

and thermal matching between most III-Ns (there is an exception: GaN and one composition of AlInN). This places restrictions on epitaxy, and tends to lead to material that is plagued with cracks or extended defects. These imperfections cut mirror reflectivity, increase scattering loss and result in current leakage paths.

Finally, the internal quantum efficiency of an InGaN emitter diminishes at higher drive currents and longer wavelengths – well-known issues that are referred to as droop and the green gap, respectively. Droop is a non-radiative process, so it ideally clamps in diode lasers above threshold, but it still increases the threshold current. Meanwhile, the green gap makes it very difficult to fabricate VCSELs emitting at 500 nm and beyond.

First breakthrough

In April 2008, more than a decade after Shuji Nakamura reported the first electrically injected, GaN-based edge emitting laser, researchers at the National Chiao Tung University (NCTU) in Taiwan announced the first electrically injected GaN-based VCSEL. This 462.8 nm laser featured a 10 μm-diameter aperture, produced a continuous output at 77K, exhibited a clear transition from spontaneous to stimulated emission, and had a threshold current and threshold current density of 1.4 mA and 1.8 kA cm^{-2}. The authors did not report the output power of this chip, but revealed a divergence angle of about 11.7°, a polarization ratio of 80 percent, and a non-uniform emission profile across the aperture above threshold, with several apparent bright spots.

Development of the bottom epitaxial DBR, which showed a reflectivity of 99.4 percent and was crack free, played a crucial role in the first demonstration of an electrically injected, GaN-based VCSEL. On this mirror – a 29 period epitaxial AlN/GaN bottom DBR – the researchers formed a ten-period $In_{0.2}Ga_{0.8}N$ (2.5 nm)/GaN (7.5 nm) quantum well/barrier stack and an eight period dielectric Ta_2O_5/SiO_2 top DBR. Inserting five-and-a-half pairs of AlN/GaN superlattices with an optical length totalling $\lambda/2$ cut biaxial strain in the DBR. Carriers entered the active region via a lateral double-intra-cavity current injection scheme employing a SiN_x current aperture. ITO with a thickness of 240 nm, equating to λ, covered this and improved current spreading.

Limitations of this design were probably: the relatively thick ITO layer, which introduced significant optical loss to the cavity; current crowding in the intra-cavity contact; and poor thermal conductivity of the sapphire substrate. It is also possible that the absence of an electron-blocking layer impaired carrier confinement.

Efforts by NCTU were followed by a flurry of results showing device improvements (see Figure 3 for details). In 2008 Nichia Corporation reported the first electrically injected lasing at room temperature, using a device based on a flip-chip geometry. By employing a vertical contact configuration and mounting a chip that features double-dielectric DBRs on a highly thermally conductive silicon substrate, the researchers addressed three issues: current crowding, low thermal conductivity of sapphire, and the challenges associated with III-nitride DBR growth. Thanks to these refinements, the VCSEL did not suffer from a hike in operating voltage that can occur with severe current crowding and lead to greater heat generation. Optical losses were minimal in the device, thanks to the high reflectivity of the DBR.

To form this chip, the researchers began by forming an epiwafer on *c*-plane sapphire with an active region comprising a two-period stack of interleaving 9 nm-thick quantum wells and 13 nm-thick barriers. Current injection occurred through an 8 μm diameter, SiO_2 aperture covered with 50 nm of ITO, plus metal electrodes that formed the *p*-side contact. Measurements revealed that the ITO had an optical loss of 0.5 percent near the lasing wavelength, so to minimize this, the team added an Nb_2O_5 layer with a thickness of $\lambda/8$. This positioned the centre of the ITO at a standing-wave null.

Final fabrication steps included deposition of an 11.5 period SiO_2/Nb_2O_5 bottom DBR over a portion of the current injection area, the addition of a bonding metal to the top of the planarized structure, and flip-chip bonding to a silicon substrate, followed by sapphire removal via laser lift-off. Chemical-mechanical polishing thinned the *n*-side of the bonded epitaxial layers to 1.1 μm, before the team added an *n*-contact and a seven period SiO_2/Nb_2O_5 top DBR.

The 414.4 nm VCSEL that resulted was capable of delivering continuous-wave emission at room temperature, had a threshold current of 7.0 mA and threshold current density of 13.9 kA cm^{-2}, and produced a peak output of 0.14 mW. Threshold voltage for the device was a relatively low 4.1 V – about half that of the VCSEL from NCTU – due, most likely, to vertical current injection.

Although the emission from this laser was linearly polarized, its orientation with respect to the crystal axes was unclear and probably random. That's not surprising, given the cylindrical symmetry of the VCSEL cavity and relatively isotropic gain in the quantum well plane. Developers of this device also noted non-uniformity in the lasing spot across the current aperture. This might be due to inhomogeneities in cavity length, surface morphology, or active region quality.

By turning to dielectrics for both the mirrors, the researchers circumvented challenges associated with the growth of high-reflectivity, crack-free DBRs, and they also benefited from superior heat dissipation and current injection. But they paid a penalty for all of this: greater process complexity. Fabrication of a double-dielectric VCSEL involves bonding, laser lift-off and well-controlled thinning. Cavity-length control is also tough, because it is difficult to polish a large-area substrate in a uniform manner to a sub-micron thickness.

Better foundations

Following in the footsteps of developers of GaN-based edge-emitting lasers, Nichia's researchers switched to free-standing GaN substrates. That move increased the room temperature, continuous-wave output power of their VCSELs by almost a factor of five to 0.62 mW. Improvement stemmed from slashing the defect density in the epitaxial layers by three orders of magnitude to several million per square centimetre.

The team attributed the higher output power of its VCSEL – which employed the same fabrication and device structure as its predecessor, with the exception of the substrate removal process – to a more uniform and complete filling of

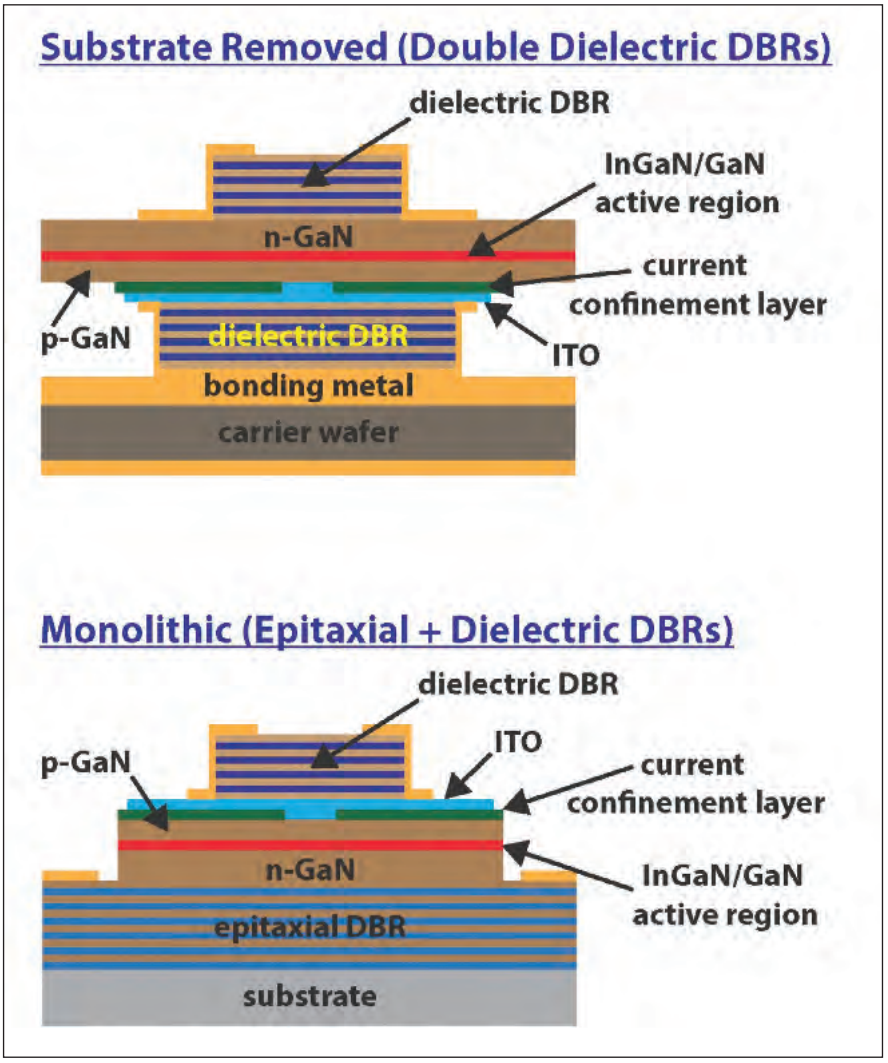


Figure 2: GaN VCSEL structures that have been demonstrated. The top structure requires wafer bonding and removal of the substrate from the cavity using thinning or etching. The bottom structure utilizes a lattice-matched epitaxial bottom DBR and a dielectric top DBR

the lasing aperture. Longitudinal mode spacing indicates a 4 μm cavity length, which is sufficient to support a number of longitudinal modes. Multiple modes might account for the higher threshold currents in these devices.

Switching from sapphire to a native substrate increased operating lifetime significantly. However, even with this superior foundation, the threshold current still increased after only 10 minutes of operation. Meanwhile, variations in cavity length are higher than those for the VCSEL formed on sapphire, because lapping and polishing is required to remove native GaN.

Researchers at Nichia and NCTU have continued to refine their GaN VCSELs over the last few years, and other groups have also contributed to the development of this device. Advances at NCTU led to the report of room-temperature, continuous-wave lasing in summer 2010, using a hybrid DBR design on a sapphire substrate. Improvements in performance resulted from: a trimming of ITO thickness to 30 nm to reduce optical loss; the addition of an AlGaN electron-blocking layer to quash carrier overflow; and an improved *p*-side contact, thanks to the introduction of a 2-nm-thick p^+-InGaN layer between *p*-GaN and ITO.

Using a similar fabrication process, device geometry and epitaxial bottom DBR as before, but moving to a ten-period InGaN (2.5 nm)/GaN (12.5 nm) quantum well/barrier stack and increasing the pairs of Ta_2O_5 and SiO_2 layers from eight to ten, helped improve device performance. Emitting at 410 nm, the second-generation VCSEL had a reduced threshold voltage of 6 V and

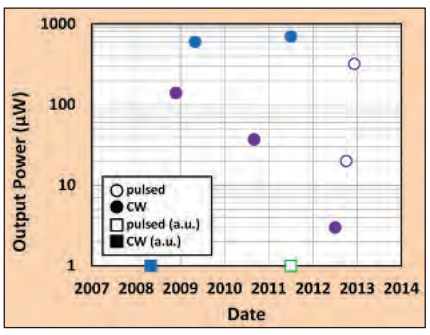


Figure 3: Electrically injected GaN-based VCSEL output power vs. time. Closed circles are CW, open circles are pulsed, and squares represent output powers originally reported in arbitrary units (a.u.). Data points are color-coded to the emission wavelength

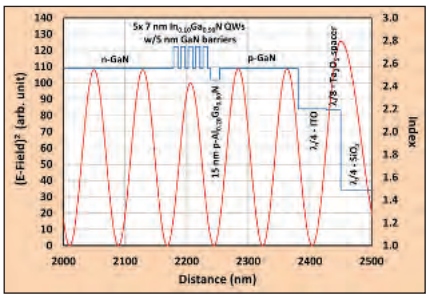


Figure 4: Standing-wave profile in the cavity region of a typical GaN-based VCSEL, illustrating the alignment of the gain region with a standing wave peak and the lossy ITO with a standing wave null

produced an output power of 37 μW. Threshold current and threshold current density were 9.7 mA and 12.4 kA cm^{-2}, and the polarization ratio at this shorter wavelength was only 55 percent.

Researchers at Nichia have also made recent advances, using their fabrication process for violet VCSELs to make blue and green cousins. The blue emitter produced a continuous-wave output of 0.7 mW, while the green equivalent delivered a pulsed output (power not revealed). According to this team, the homogeneity of the lasing spot within the injection aperture is critical to obtaining higher performance. This underscores the importance of effective, lateral-current-spreading layers.

Further contributions to VCSEL development have come from Panasonic Corporation, which has produced violet VCSELs capable of continuous-wave operation using a fabrication process similar to that developed by Nichia. This team, which is currently developing GaN-based VCSEL arrays, has turned to relatively long cavity lengths of typically 6 μm to permit multiple longitudinal modes within the gain spectrum. Merits of this approach include reduced thermal sensitivity and increased uniformity of the elements in the arrays.

Non-polar structures

Another option for improving VCSEL performance is to turn to non-polar structures, which increase optical gain and lower threshold current density through the elimination of the quantum confined Stark effect (QCSE). A team from the University of California, Santa Barbara, which included myself, pursued this approach. We were the first to demonstrate a GaN-based VCSEL on a nonpolar (*m*-plane) substrate.

By switching to non-polar or semi-polar quantum wells, in addition to avoiding or reducing the QCSE, we can ensure that the polarization direction of the lasing mode is always aligned along a given crystal direction. This is not the case for conventional VCSELs, which typically exhibit a random polarization direction.

We formed our VCSEL on a free-standing, *m*-plane GaN substrate. Fabrication involved a band-gap-selective, photo-electrochemical (PEC) undercut etching of an intra-cavity embedded sacrificial layer of InGaN. This enabled bonding and removal of the epitaxial layers from the substrate. Thanks to this approach, we could realise precise cavity length control while employing top and bottom dielectric DBRs and recycling expensive, free-standing GaN substrates. To improve current spreading, we used a λ/4-layer of ITO that was positioned at a standing-wave null of the cavity to minimise optical loss (see Figure 4).

Violet VCSELs produced in this manner emitted 19 μW and had a threshold current of 70 mA. This high threshold may be due to ITO absorption loss or cracking during the bonding process. Polarization of the lasing mode was observed to be along the *a*-direction for all devices tested.

The polarization ratio for these devices is close to one (see Figure 5 for an illustration of polarization alignment). Thanks to polarization locking in these non-polar VCSELs, they could someday be used to fabricate large arrays of devices with the same polarization direction. Such emitters may find use in various applications.

Alternative mirrors

Further progress of the electrically injected, GaN-based VCSEL was reported in 2012 by a team from EPFL. They formed monolithic devices using highly reflective, defect-free $Al_{0.18}In_{0.82}N$ DBRs that are lattice matched to GaN. A free-standing *c*-plane GaN substrate provided the foundation for this emitter, which featured a bottom epitaxial DBR and a top dielectric DBR. Such a structure avoids the tricky fabrication steps of the other approaches, which require the removal of the cavity from the substrate or substrate thinning. The price to pay for this is a more challenging epitaxial structure. However, with well-developed epitaxial DBR technology, this

monolithic structure presents a viable path toward high-volume manufacture of GaN-based VCSELs.

The EPFL team has also pioneered a simple method for forming a current aperture – passivating portions of the *p*-GaN with reactive-ion-etching, plasma treatment. With ITO acting as the current spreading layer, uniform light emission is possible throughout the aperture. Devices lased at 420 nm, produced a pulsed output of more than 300 μW and had a 70 mA threshold current. Researchers blamed the high threshold current on ITO absorption loss and insufficient reflectivity in the top DBR. Options for cutting current are to trim the thickness of the ITO and tune its position.

Which way forward?

Over the last few years, progress of the GaN VCSEL has been significant, but key challenges must be overcome before this device can enjoy commercial success. Researchers must pursue either new DBR technologies, or develop methods to generate stand-alone cavities that have well-controlled lengths and can be attached to dielectric DBRs. If air-gap bottom DBRs could be created by selective removal of every other λ/4-layer using band-gap-selective PEC etching, only several periods would be needed to produce extremely high reflectivities. However, fabrication of such structures is very tough. So it may be that further optimisation of the AlInN DBR scheme developed at EPFL leads to the first manufacturable GaN-based VCSEL.

What is clear is that if approaches involving substrate removal via backside wafer thinning are to become commercially viable, they will require more precise control of cavity length. This might be possible with a combination of thinning and band-gap-selective PEC etching, which could planarize the cavity with an embedded stop-etch layer placed at the desired cavity thickness. Full substrate removal using PEC etching also presents challenges. However, this approach does provide cavity length control and it enables the recycling of expensive, free-standing GaN substrates.

Another area requiring improvement is that of the current spreading layers. Addressing this is essential for the realisation of larger-area devices that will deliver higher output powers. The ITO technology that is widely used today has been pushed to its performance limits, so further progress will hinge on the introduction of novel injection schemes and materials. This could involve the introduction of reliable, low-resistance tunnel junctions in GaN. Armed with this refinement, engineers would not have to concern themselves with the current spreading issue, because *p*-GaN could be replaced with higher conductivity *n*-GaN. Alternatively, developers of GaN VCSELs could increase current spreading by employing novel, two-dimensional materials with high transparency and high lateral conductivity.

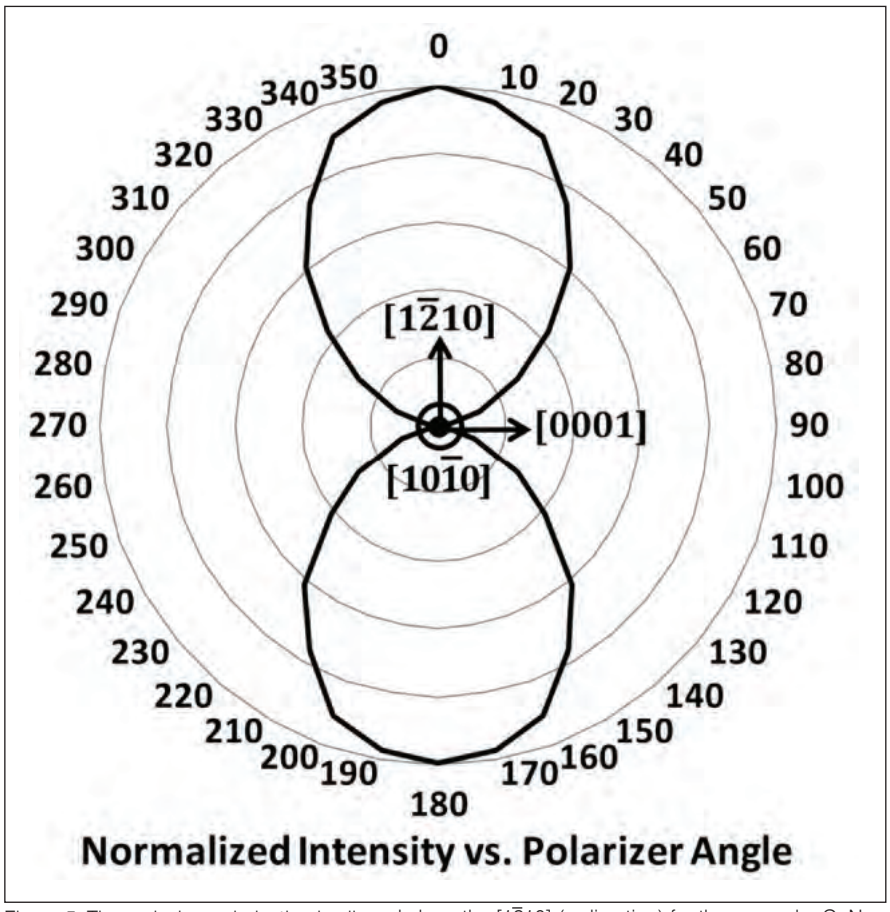


Figure 5. The emission polarization is aligned along the [1$\bar{2}$10] (a-direction) for the non-polar GaN-based VCSEL. Polarization ratio is close to one

Lastly, efforts must be directed at a systematic examination of the non-polar and semi-polar orientations, to uncover their potential for increasing optical gain and reducing threshold current. Increasing the per-pass-gain would permit DBRs with lower reflectivity, relaxing the design space. Success of green edge-emitters built on semi-polar planes motivates exploration of this orientation for green VCSELs. Non-polar and semi-polar orientations might also enable high-power VCSEL arrays with uniformly polarized emission characteristics.

Further reading

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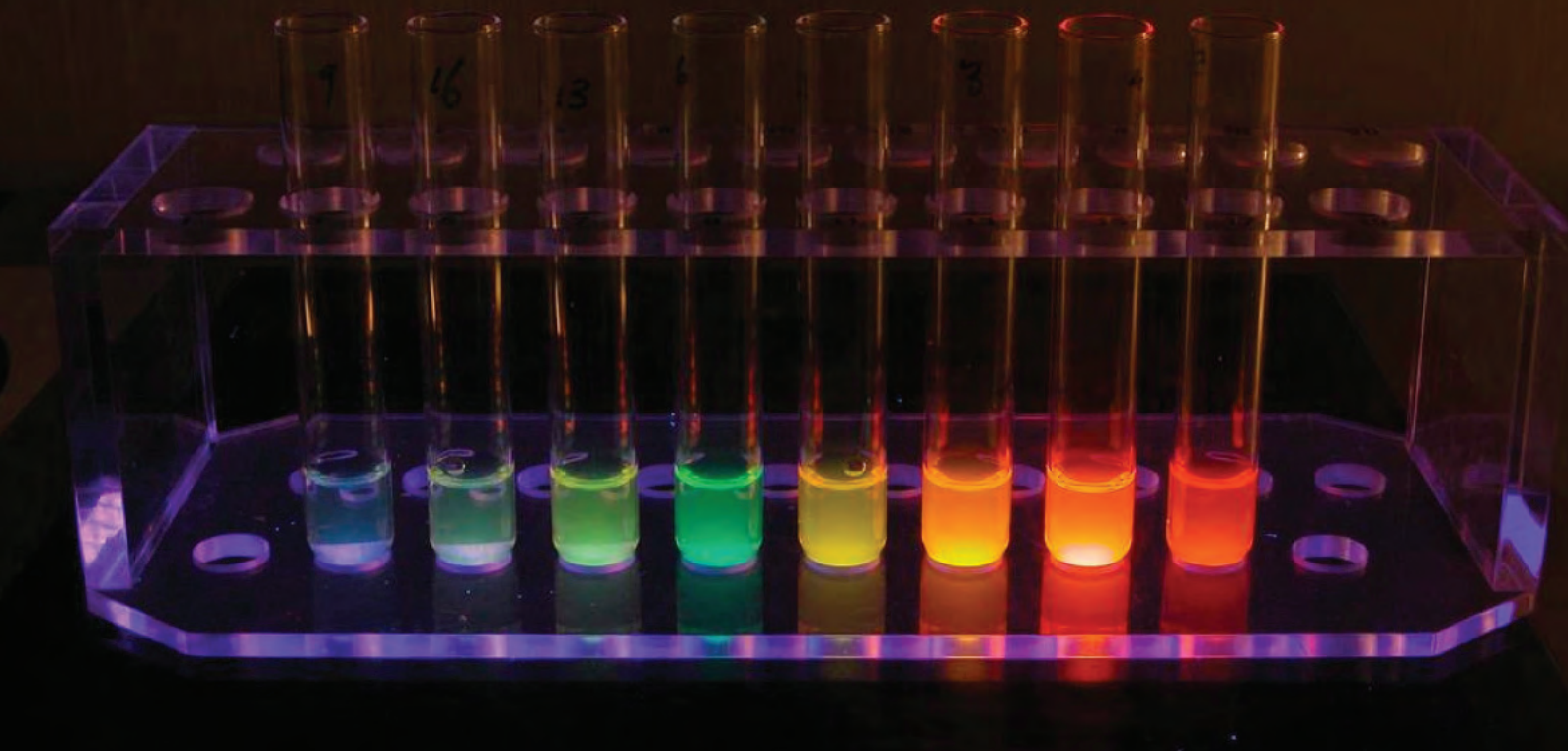
Increasing ultraviolet efficiency with nano-patterned sapphire

Switching from conventional patterning of sapphire to a nano-scale variant trims epitaxial growth times and materials costs while boosting extraction efficiency.

By JIANCHANG YAN, PENG DONG, AND JUNXI WANG from the INSTITUTE OF SEMICONDUCTORS AT THE CHINESE ACADEMY OF SCIENCES.



DEEP ULTRAVIOLET (DUV) sources can serve many applications, including air and water purification, disinfection, bioagent detection (see image above), curing and non-line-of-sight communication. Traditionally, the mercury lamp has served this spectral range, but it is bulky, fragile and unsuitable for providing a modulated light source.

All of these weaknesses can be addressed with a DUV LED. Following several years of research into this class of solid-state emitter, chips now span 365 nm to 210 nm, with some devices producing milliwatt levels of light output while operating for thousands of hours. It is a level of performance that is adequate for some applications, but far higher levels of performance will drive significant market penetration for the DUV LED. Today it is held back by a modest internal quantum efficiency and a low light extraction efficiency, which combine to limit this chip's external quantum efficiency and output power.

The low internal quantum efficiency stems from the high density of crystal defects – they are typically of the order of 10^{10}-10^{11} cm^{-2}. DUV LEDs are riddled with these defects because there is a large lattice mismatch and a significant thermal expansion mismatch between the sapphire substrate and the AlN and AlGaN epilayers that form the LED (see Figure 1). Meanwhile, light extraction is poor, due to the combination of low internal total reflection at the epi-layers' flat interfaces and absorption of the emission from the active region by the top *p*-GaN.

One option for increasing light extraction in these devices is to follow a widely adopted approach for boosting the brightness of blue LEDs. Forming these blue-emitting chips on micro-cone-shaped, patterned-sapphire has not only increased light extraction, but also enhanced crystal quality, leading to a substantial hike in luminous efficiency. However, care must be taken when attempting to replicate this type of approach with DUV LEDs, because AlN does not completely coalesce to form a smooth surface on conventional, micrometre-scale patterned sapphire. Why? Because the aluminium species have a low surface mobility.

Some research groups have suppressed crystal defects, both in AlN and in the upper epilayers, by turning to epitaxial lateral overgrowth techniques on either micro-striped patterned sapphire, or on templates formed by the growth of AlN on a flat sapphire substrate. AlN can then coalesce on unetched flat regions, leading to enhanced light output and external quantum efficiency for the DUV LEDs. However, this approach is not without its penalties. Due to the large space between the micro-patterns, coalescence thicknesses for AlN can be up to 10 μm, and this leads to far greater epitaxial time and cost.

From micro to nano

To trim the coalescence thickness while maintaining a high output power for the DUV LED, our team at the Institute of Semiconductors at the Chinese Academy of Sciences has developed novel nano-patterned sapphire substrates. They form the foundation for nanoscale epitaxial layer overgrowth of an AlN template layer for DUV LEDs (see Figure 1).

Turning to these nano-patterned substrates slashes the coalescence thickness of the AlN film to just 3 μm. This is not at the expense of material quality – according to high-resolution X-ray diffraction and cross-sectional transmission electron microscope analysis of AlN and upper epilayers – and it enables the fabrication of LEDs with an impressive level of performance. Driven at 20 mA, a 282 nm LED formed on this foundation produces nearly twice the output power of an equivalent device formed on a conventional AlN-on-sapphire template.

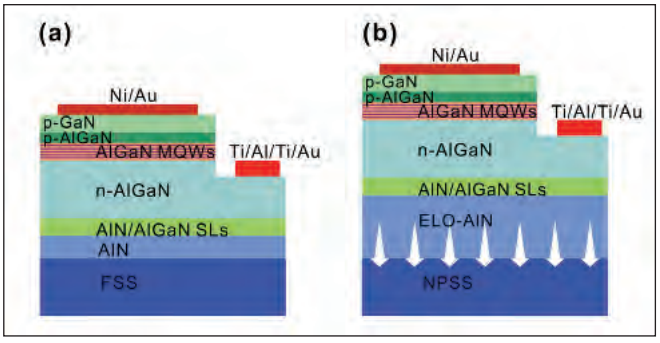
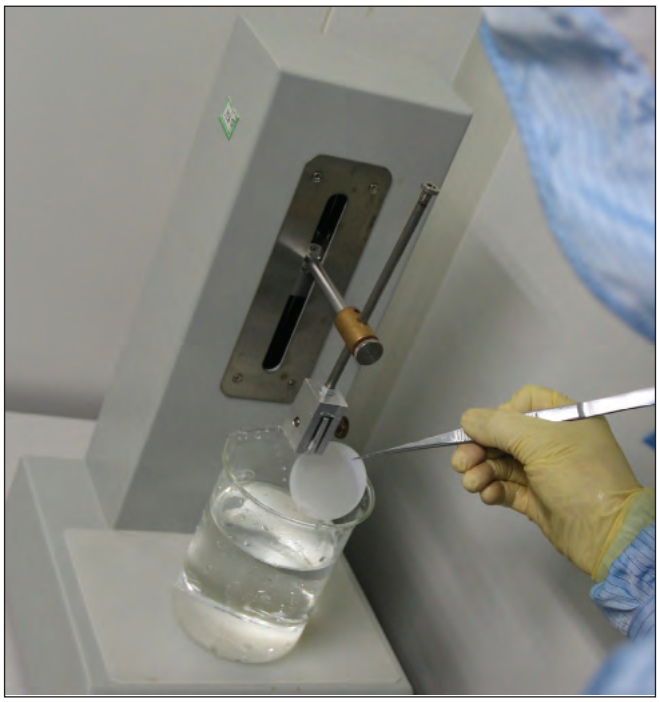


Figure 1. The device structure of the DUV LED on flat sapphire substrate with a 1-μm-thick AlN template layer (a) delivers an inferior performance compared to that built on a nano-patterned sapphire substrate with a 4-μm-thick AlN template layer (b)



Forming nano-patterned sapphire involves dip-coating and cleaning processes

We formed our patterned sapphire with a nanosphere lithography technique that involves wet-etching (see Figure 2). We begin by depositing a 200-nm-thick SiO_2 film onto 2-inch (0001) sapphire by plasma-enhanced CVD. A positive photoresist is then spin-coated on this oxide, before a highly ordered self-assembled monolayer of polystyrene nanospheres is added via dip-coating. The wafer is then exposed to UV light using conventional photolithography, before the nanospheres are removed with deionised water and the photoresist developed to form nano-sized holes. Subsequent inductively coupled plasma etching transfers this pattern to the SiO_2 film, before the sapphire substrate is etched for 10 minutes in a mixture of H_2SO_4 and H_3PO_4 solution and the SiO_2 mask removed by HF.

This process creates a sapphire substrate that is patterned with concave triangular cones, which have dimensions defined by the anisotropic etching of the sapphire crystal (see Figure 3 for scanning electron microscopy images of pattern sapphire with periods of 900 nm and 600 nm).

Growth of our epistructure is undertaken with our homebuilt low-pressure MOCVD tool. It is fitted with trimethylaluminum, trimethylgallium and ammonia for providing aluminium, gallium and nitrogen sources, respectively.

Starting with nano-patterned sapphire with a 900 nm period, we deposit a 25-nm low-temperature AlN buffer layer at 550 °C, before ramping the temperature to 1200 °C to grow a 4-μm AlN template. Growth of this layer occurs under continuous flow, with a relatively low V/III ratio of below 1000 and a low chamber pressure of 50 torr.

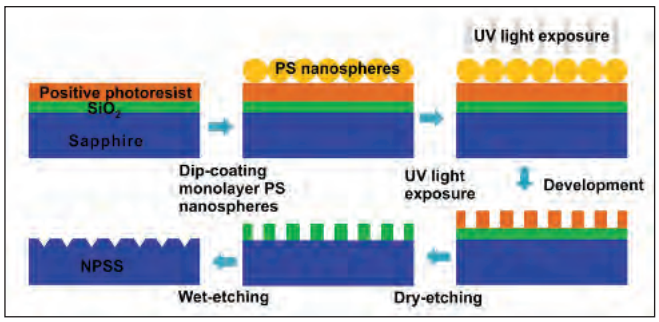


Figure 2. The process flow for fabricating the nano-patterned sapphire

We have scrutinised the quality of this AlN film with a variety of techniques. Cross-sectional scanning electron microscopy reveals that the AlN completely coalesced after 3-μm of growth, thanks to the nano-scale substrate patterns and the AlN lateral growth. Meanwhile, atomic force microscopy shows that the AlN is smooth – it has a root-mean-square roughness of 0.15 nm. The crystal quality of this 4 μm-thick AlN film is better than that produced on conventional sapphire, according to X-ray rocking curves that provide figures for full-width at half maximum of 86.4 arcsec and 320.4 arcsec for the (002) and (102) directions, respectively. Patterning sapphire also cuts defects, with threading dislocations reduced due to bending that results from lateral overgrowth.

On the 4-μm-thick AlN template formed on our nano-patterned sapphire we deposited: a 20-pair AlN/AlGaN superlattice; a 3.5-μm-thick, silicon-doped *n*-$Al_{0.55}Ga_{0.45}N$ layer; five 3-nm-thick, un-doped $Al_{0.4}Ga_{0.6}N$ quantum wells sandwiched by 12-nm-thick, silicon-doped $Al_{0.5}Ga_{0.5}N$ barriers; a magnesium-doped $Al_{0.65}Ga_{0.35}N$ electron-blocking layer; a 50-nm-thick, *p*-AlGaN cladding layer; and a 150-nm-thick, highly doped *p*-GaN contact layer. For comparison, we also formed an identical structure on conventional sapphire, using a 1 μm-thick AlN template.

Better, brighter material

Superior material quality in the structure formed on nano-patterned sapphire is revealed with transmission electron microscopy (see Figure 4). Dislocation density in the *n*-AlGaN layer formed on patterned sapphire is 1.6×10^9 cm^{-2}, compared to 3.4×10^9 cm^{-2} for the same epilayer on conventional sapphire. Cutting the dislocation density increases the internal quantum efficiency from 28 percent to 45 percent, according to temperature-dependent photoluminescence measurements on 'top-GaN-less' multiple quantum well structures.

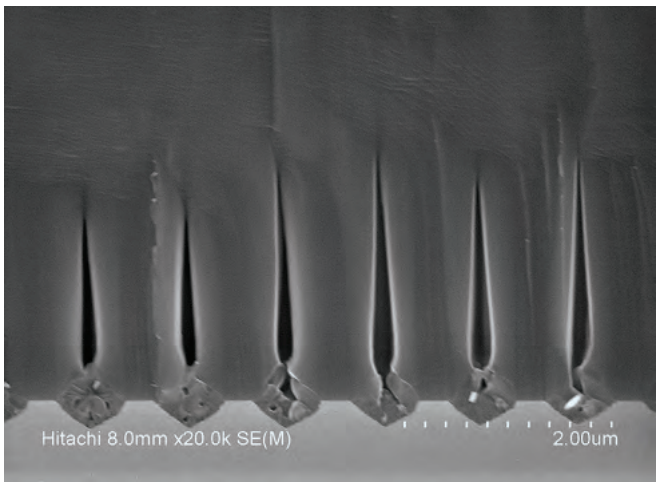


Figure 4. Cross-sectional scanning electron microscopy reveals the high quality of the AlN grown on nano-patterned sapphire

Epiwafers were used to form 380 μm by 380 μm devices. Contact photolithography and inductively coupled plasma etching defined the *p-n* junction mesa, prior to the deposition of a Ti/Al/Ti/Au (20 nm /120 nm/20 nm/100 nm) metal stack onto the *n*-AlGaN using an electron-beam evaporator.

This was annealed in nitrogen gas at 850 °C. The ohmic contact for *p*-GaN employed a Ni/Au (5 nm/10 nm) metal stack, annealed at 550 °C in air. Chips were then flip-chip bonded with gold bumps to silicon sub-mounts, which were attached to metal-core printed circuit boards with sliver paste for device testing. This improved heat dissipation from the DUV LED.

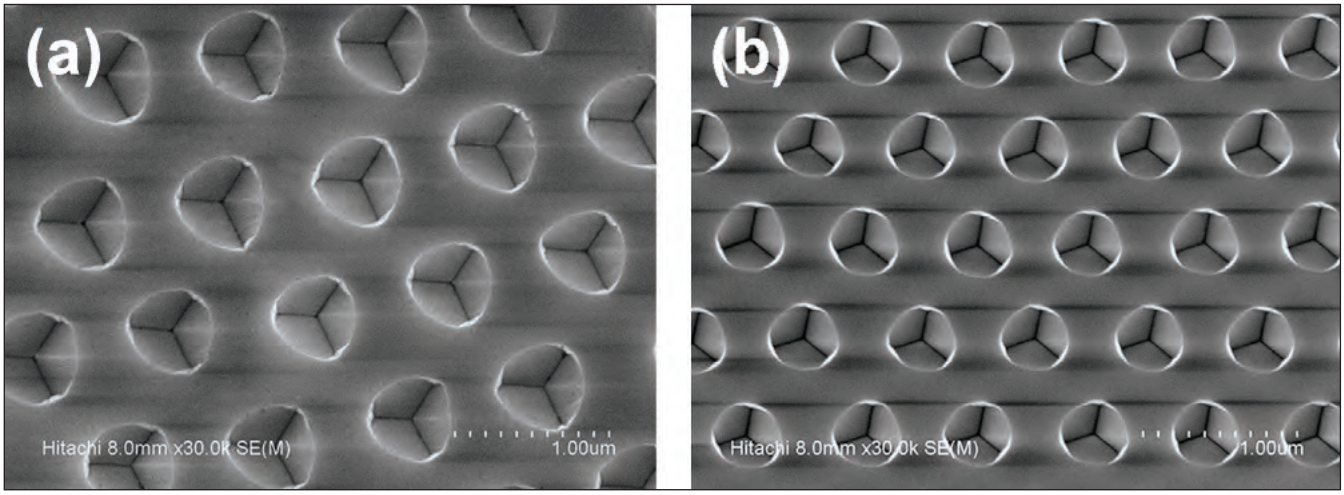


Figure 3. Scanning electron microscopy images of the fabricated nano-patterned sapphire with periods of 900 nm (a) and 600 nm (b)

> The DUV LED's efficiency and output power can be increased with a combination of superior heat dissipation, optimisation of the dimensions of the nano-patterned sapphire, and improvements to the growth processes used to deposit AlN onto the substrate.

Our devices built on patterned sapphire emit a peak wavelength of 282 nm and, when operated at 20 mA, produce an output power and external quantum efficiency of 3.03 mW and 3.45 percent, respectively. Output saturates at 60 mA, hitting 6.56 mW. In comparison, the equivalent LED formed on conventional sapphire is limited to 2.53 mW at 50 mA, primarily due to inferior heat dissipation.

Driven at 20 mA, our DUV LED grown on the novel platform delivers an external quantum efficiency that is 98 percent higher than that of the control sample (see Figures 5 and 6). Since external quantum efficiency is a product of internal quantum efficiency, light extraction efficiency and carrier injection efficiency – and the measurements for 'top-GaN-less' multiple quantum wells show a 60 percent gain in internal quantum efficiency with the patterned sapphire – it is highly likely that the patterning has boosted extraction efficiency. This is to be expected, because light scattering at the interface between AlN and nano-patterned sapphire should decrease total internal reflection and absorption in the *p*-GaN layer, while increasing the photon's opportunity for escaping from the sapphire backside.

We will now try to build even more impressive devices. The DUV LED's efficiency and output power can be increased with a combination of superior heat dissipation, optimisation of the dimensions of the nano-patterned sapphire, and improvements to the growth processes used to deposit AlN onto the substrate. In addition, we will investigate the impact of nano-patterning on the reliability of our devices.

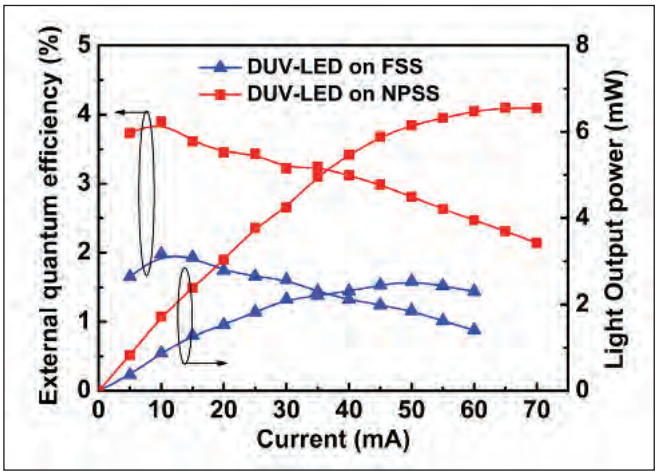


Figure 6. Nano-patterning increases the output power and the efficiency of DUV LEDs

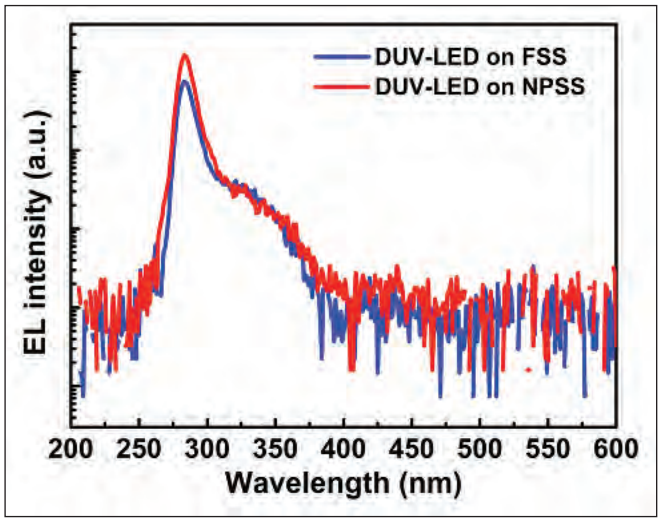
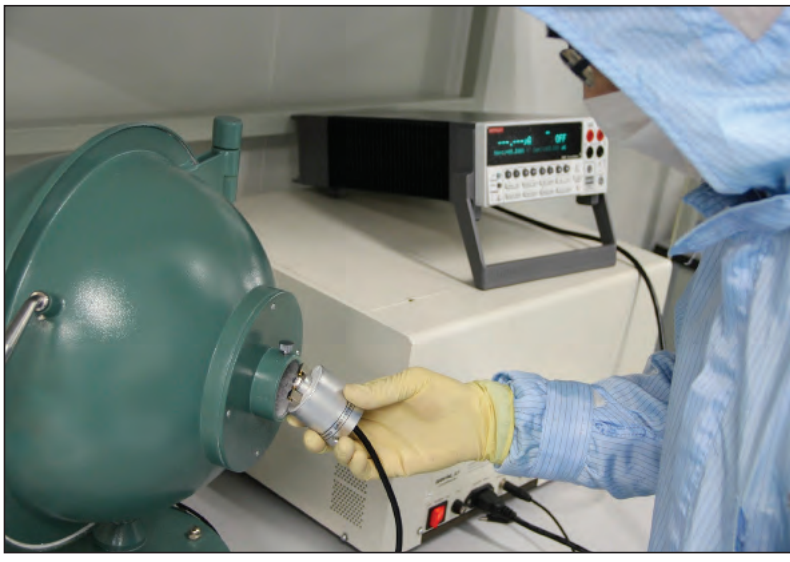


Figure. 5 The patterning of sapphire leads to an increase in electroluminescence intensity



Measuring ultraviolet LED output

Going Green
with cubic GaN

Conventional green LEDs are plagued by strong internal electric fields, which impair recombination and make it difficult to address droop. The solution is switch to growth on the cubic phase of GaN, which is free from internal fields and has a smaller bandgap, making it easier to reach longer wavelengths.

By MARK DURNIAK and CHRISTIAN WETZEL
from RENSSELAER POLYTECHNIC INSTITUTE

THE SOLID-STATE LIGHTING REVOLUTION is now upon us. Businesses and homeowners are trimming their electricity bills, and by 2030 an ever-increasing uptake of LED bulbs could lead to savings as high as $30 billion, according to the US Department of Energy.

Most consumers that are currently investing in solid-state lighting are buying bulbs that employ a highly efficient blue LED to excite a phosphor, which then re-emits photons of lower energy, usually in the yellow spectral region. Colour mixing of blue and yellow creates a white-emitting luminaire.

This approach has the merit of simplicity, but it is not ideal. One weakness is the inherent conversion efficiency ceiling, stemming from the Stokes loss in the down-conversion of high-energy blue photons to lower energy yellow photons. In addition, the colour temperature or 'warmness' of the white light is fixed, governed by the mix of phosphors.

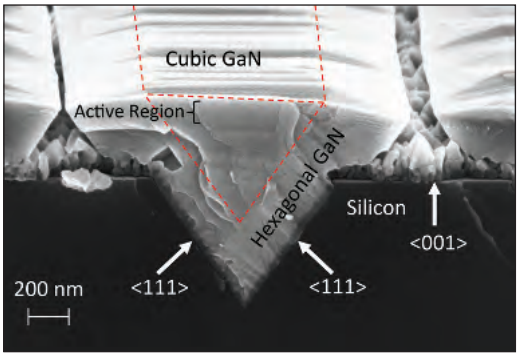


Figure 1. Growth of hexagonal GaN in 'V-shaped' trenches leads to the formation of cubic GaN

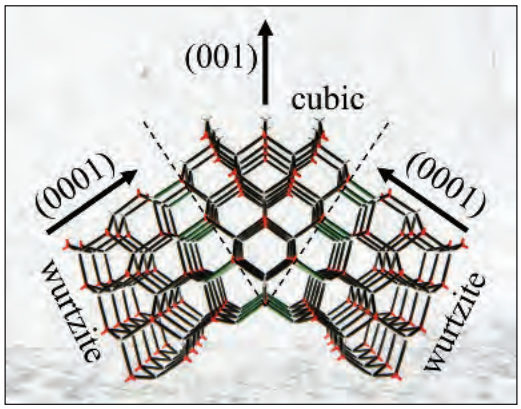


Figure 2. Model of the cubic/hexagonal GaN interface

These limitations can be lifted with luminaires based on the colour mixing of several LEDs, such as those emitting in the red, green and blue. With this approach, which can involve three or more LEDs, it is possible to construct a high-quality, colour-tuneable light source. The Philips HUE bulb is an example of this, which allows users to pick the colour they want by running an app on their smart phone.

Another advantage of the colour mixing approach is that it can achieve higher theoretical efficiencies than phosphor conversion. The efficacy of this form of lighting is then governed by the efficiencies of the LEDs.

Blue and red LEDs excel in this regard, but the same cannot be said for their green-emitting cousins. At modest currents, such as 20 mA, their efficiency is significantly inferior. And when the current is cranked up, they are more prone to droop, so their efficiency plummets faster.

These weaknesses have several origins, all associated with flaws in material characteristics. To produce a green LED, engineers use a similar growth process to that employed for making a blue emitter, but increase the indium content in the InGaN quantum well. Unfortunately, this increases the crystalline strain in the well, leading to the generation of crystalline defects that peg back the efficiency of the green LED.

This device is fabricated from the hexagonal, or wurtzite, phase of the wide bandgap material, which features strong internal fields. These fields cause a shift in wavelength as the current is increased, due to a phenomenon known as the quantum confined Stark effect. This is particularly severe in green LEDs.

As well as the shift in emission wavelength, there is a pulling apart of electrons and holes, which pile up on opposite ends of the well. This impairs the radiative recombination efficiency. Turning to narrower wells can bring the charge carriers closer together, but may have very damaging side affects associated with the increase in carrier density. Auger recombination is known to increase with the cube of carrier density, and if, as many believe, this is the primary cause of droop, turning to thinner wells will fail to improve the performance of a green-emitting LED at meaningful current densities.

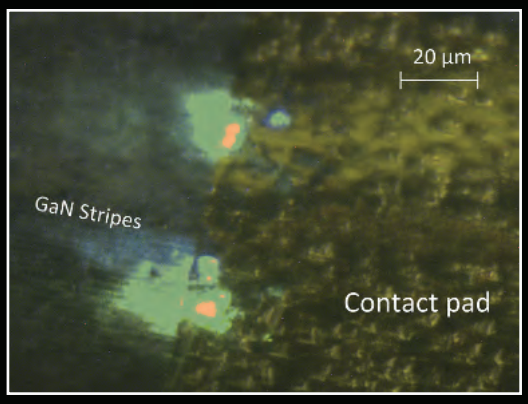


Figure 3. LEDs formed in the stripes of a silicon wafer produce green emission

So, as you can see, the green gap is a very tricky problem. Researchers are trying to solve it, however, with some taking radical steps that will allow a lowering of the carrier concentrations in the quantum wells. Since it is difficult to see how one could do this with polar material, groups are trying different approaches, such as growing devices on non-polar faces of hexagonal GaN. And at the NSF-funded Smart Lighting Engineering Research Center at Rensselaer Polytechnic Institute we are taking a similar, but distinct tack, by turning to the cubic phase of GaN.

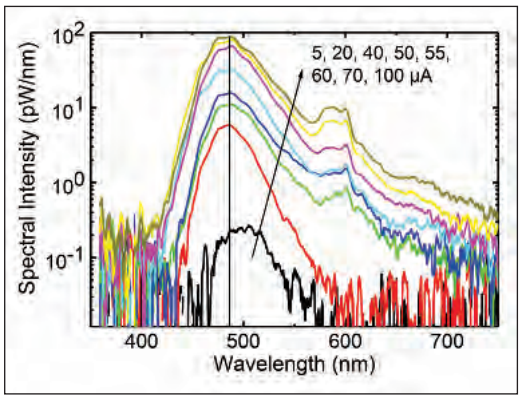


Figure 4. Unlike a conventional green LED, cranking up the current does not lead to a shift in emission wavelength

Attributes of cubic GaN

One of the great strengths of the cubic phase of GaN is that it has no internal electric fields in the typical growth direction, and thus no quantum confined Stark effect. The benefits of this are twofold: bands no longer move with increasing current, so the emission wavelength is fixed; and the overlap of electrons and holes in the quantum wells increases, so these carriers are more likely to recombine radiatively. Removal of the electric fields also opens up the possibility to turn to wider quantum wells that enable efficient radiative recombination while lowering Auger recombination rates.

Another great virtue of cubic GaN is its bandgap: At 3.2 eV, it is 0.2 eV lower than that of the hexagonal phase. This difference means that cubic GaN has almost a 30 nm head start prior to growth for making long-wavelength emitters, which is a great benefit when aiming for green LEDs.

What's more, cubic GaN theoretically has better transport properties than the hexagonal variant due to higher crystal symmetry. Holes are a necessary player in producing light from LEDs, but *p*-type hexagonal GaN is notorious for its low concentration of holes and their poor mobility. Since holes do not move around as freely as electrons, most of the emission from an LED comes from the last quantum well – the one closest to the *p*-side. Better hole mobility would increase its population in many quantum wells, culminating in more light from the device. At low hole concentrations, hole mobility in cubic GaN has been reported at 350 $cm^2 V^{-1} s^{-1}$ compared to less than 200 $cm^2 V^{-1} s^{-1}$ in hexagonal GaN.

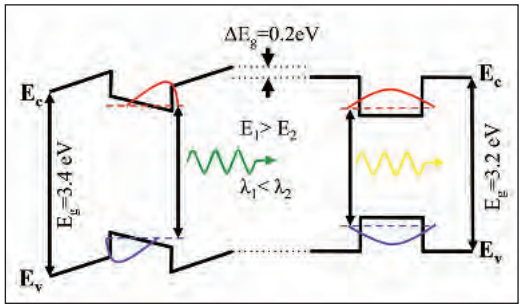


Figure 5. In a hexagonal InGaN quantum well (left), electron and hole wave-functions are spatially separated due to internal polarization fields. In a cubic InGaN quantum well of the same Indium composition (right), carriers overlap and the emitted photon is of longer wavelength

Increasing dimensions

We are not the pioneers of cubic GaN, and our contribution to this field is to increase the size of this material. We are following in the footsteps of the likes of the groups of Donat As at the University of Paderborn, and Tom Foxon and Sergei Novikov at the University of Nottingham – teams that produced cubic GaN layers and devices, starting mainly with 3C-SiC and GaAs cubic substrates.

The MBE growth technique that both of these groups have used is highly versatile, but limited to growth rates of the order of 100 nm/hr. This means that the deposition of an LED structure can take 10 hours or more, an impractically long time for LED manufacture, which is better served by MOCVD. Groups led by Heber Vilchis from Cinvestav and Shigefusa Chichibu from the University of Tsukuba have shown that this deposition technology can form cubic GaN on GaAs and 3C-SiC, respectively, but crystal size is small and phase purity poor. We are now addressing these shortcomings with an approach that offers production scalability, and begins with the most common form of silicon. By using this form, silicon (001), we have the potential to reach wafer sizes of 300 mm.

To address the well-known mismatch problem, we do not directly deposit a film of cubic GaN on a flat silicon wafer, but instead initiate growth in narrow stripes, which can eventually coalesce (see Figure 1). By employing a micro-patterned substrate, we can 'trick' GaN into forming the cubic phase in micro-stripes created from two separate hexagonal crystals.

One of the biggest challenges that we face is that the cubic phase of GaN is metastable – from a thermodynamic perspective, it would rather be hexagonal. However, the energy difference between the two phases is only 10 meV/atom, and if this wide bandgap material forms the cubic phase, it will probably stay that way. The challenge is to get the atoms into the cubic configuration for long enough to repeat the pattern. The difference between these polytypes is merely one of stacking: in the hexagon phase the layers alternate ABABAB, whereas in the cubic phase, every third layer is the same, so the pattern is ABCABC.

Our starting point is a micro-patterned silicon (001) substrate, which is prepared by our collaborator, the group of Steven Brueck at the University of New Mexico. This team uses interference pattern lithography to define long stripes parallel to the (110) direction. These stripes are then etched into the silicon to produce an array of V-shaped grooves with (111)-type sidewalls running the length of the substrate. The grooves have an 800 nm opening and are spaced at a 4 μm pitch.

There is a lattice mismatch of about 20 percent between hexagonal GaN and silicon (111). So, if thick layers are required, complicated strain management structures are needed to prevent cracking. However, our application only requires a thin layer, so we avoid such complexities.

To prevent alloying of silicon and gallium, we begin by growing an AlN/AlGaN buffer layer. This is followed by deposition of hexagonal GaN: Two (0001) planes of hexagonal GaN grow from the (111) sidewalls of the grooves towards one another (see Figure 2). It is this growth that is the key to our approach, because, atomically, the (0001) plane of hexagonal GaN looks exactly like that of the (111) face of cubic GaN. The two (0001) planes are offset by the natural angle between (111) faces, due to the geometry of the substrate. So, when the next adatom wanders down into the groove, it doesn't see two hexagonal GaN crystals growing out at one another – it sees the cubic phase, and settles in a cubic lattice position.

Following this nucleation of the cubic phase, growth proceeds rapidly upward, filling the groove in the new (001) direction. The result is a long, 2-3 μm wide triangular prism of single-crystal cubic GaN that is nestled in the stripe. It features a hexagonal GaN cladding on two of its sides.

With the cubic phase present, it is now possible to grow LED structures, just as one would for the hexagonal case. Forming a high-quality green LED is much easier with this phase of GaN, however, because: less indium in needed in the wells, thanks to the smaller bandgap of cubic GaN; and there is less strain in the active region, because the InGaN layer is only grown in long, thin stripes. A more relaxed layer is beneficial, because it is less likely to form dislocations and more likely to incorporate more indium.

Scrutinising our sample with electron-backscatter diffraction confirms the presence of cubic GaN in the centre of the stripe, and hexagonal material at the edges. Meanwhile, cathodoluminescence reveals that our cubic material has a band-gap of 3.23 eV. According to cross-sectional transmission electron microscopy, the cubic regions are virtually free of line defects and without wurtzite inclusions. This is a breakthrough, because other groups have reported wurtzite inclusions within their cubic GaN. These imperfections may have a detrimental effect if present in the active region of an LED.

We have fabricated a fully functioning, green-emitting cubic GaN LED on our engineered substrate (see Figure 3). It's electroluminescence spectra are stable, even when the driving current is changed by an order of magnitude (see Figures 4 and 5). In comparison, subjecting a similar hexagonal GaN LED to changes of drive current of this order can induce a blue-shift in emission wavelength of up to 20 nm. We have also carried out preliminary electrical measurements with nano-probes, finding good electrical performance for *p*-doped cubic GaN (see Figure 6).

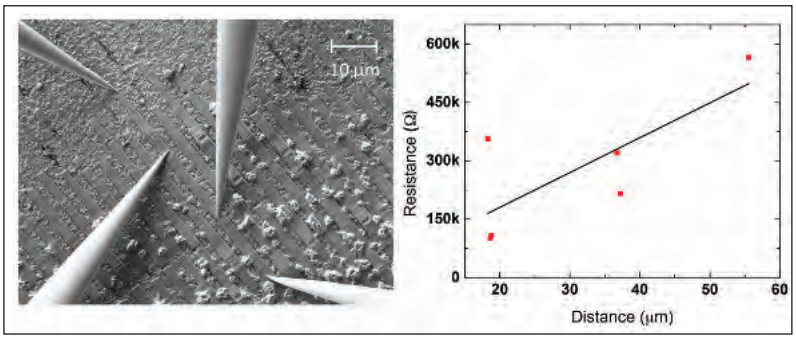


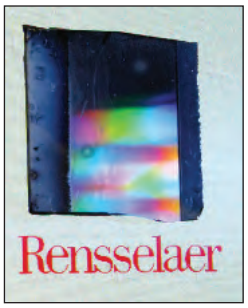
Figure 6. Nano four-point-probe and transmission line experiments indicate that resistivity is about 0.28 Ωcm

Our proof-of-concept devices built of cubic GaN are promising, wavelength-stable green LEDs with good electrical properties. But there is more work to do. First, we want to propel the LED to longer wavelengths: Why should we stop at green, when we could reach yellow and even red?

In addition to reaching deeper into the colour spectrum, we will continue our study of the widely unexplored electrical properties of the cubic phase. We also plan to fabricate higher-performance cubic LEDs by removing the silicon substrate, so light extraction is increased through the underside of the stripes. A longer-term goal of ours is to expand and coalesce the separate cubic GaN stripes into a single, large epitaxial film. Ultimately, this technology has the potential to be scaled up to larger silicon wafers. Handling and processing equipment is already in place for this, thanks to the silicon IC industry.

If we could bring this technology to 300 mm or larger wafers, this could drastically increase the number of LEDs that could be formed from a single growth run. What's more, these cubic GaN templates don't just have to be the ideal platform for making green LEDs – they could be a great foundation for blue and red emitters too. If they could arm the makers of colour-tuneable lighting systems with efficient LEDs spanning the entire visible spectrum, it would enable them to offer products that set a new benchmark for performance.

This work was supported primarily by the Engineering Research Centers Program of the National Science Foundation under NSF Cooperative Agreement No. EEC-0812056. This work was also supported by New York State under NYSTAR contract C090145. Any opinions, findings and conclusions or recommendations expressed in this material are those of the author(s) and do not necessarily reflect those of the National Science Foundation or New York State.



Cubic GaN grown on micro-patterned silcion (001). Direct GaN on silicon technology could lead to fully integrated LED displays

Further Reading

J. M. Stark, et al. Appl. Phys. Lett. **103** 232107 (2013)

Accelerating SiC growth and throughput

Novel reactor enables rapid growth of high-quality 150 mm SiC epiwafers

A JAPANESE TEAM claims to have set a new benchmark for high throughput of high-quality epiwafers by developing a novel 150 mm SiC reactor.

The high-performance tool, which features high-speed wafer rotation and is capable of growth rates of 40-50 μm/hour, was developed through collaboration between five institutions: the Central Research Institute of Electric Power Industry (CRIEPI), Denso, NuFlare Technology, Toyota Motor Corporation and Toyota Central R&D Labs. In addition to the high growth rate – conventional reactors are limited to 30 μm/hour or less, according to reports from academia – strengths of the Japanese reactor include its capability to produce epiwafers that combine a low defect density with excellent thickness and doping uniformity.

Team-member Hiroaki Fujibayashi, who is affiliated to CRIEPI and Denso, believes that in order for a successful SiC device market to develop, there must to be a low-cost, 150 mm growth technology. And it must deliver a high-throughput of wafers with a low defect density and high uniformity.

"Therefore, I consider that the high quality and high throughput of a 6-inch SiC epitaxial growth process, such as that of our technology, can contribute to growth of the SiC power device market."

The engineering team refer to their single-wafer tool as a 'dual reactor system'. Thanks to its design, a throughput of 4 wafers/hour is possible, assuming a growth time per wafer of 15 minutes. Although a multi-wafer reactor has the potential for even higher throughput, there are several good reasons for preferring a single-wafer tool, according to Fujibayashi. He argues that single-wafer reactors are smaller, and this leads to a shorter heating-cooling time and reduced maintenance costs.

What's more, he points out that the development of reactors accommodating even larger wafers is much easier with a single-wafer platform. With this type of tool, moving from a 150 mm wafer to a 200 mm wafer requires an increase in holder diameter of 50 mm; but with a multi-wafer reactor, the holder diameter would have to increase by 100 mm for an identical increase in wafer size.

High-speed wafer rotation is common for the epitaxy of silicon and III-Vs, where it provides high growth rates and enhanced uniformity. But, up until now, it has not been applied to SiC, due to the far higher growth temperatures – they are typically 1600 °C.

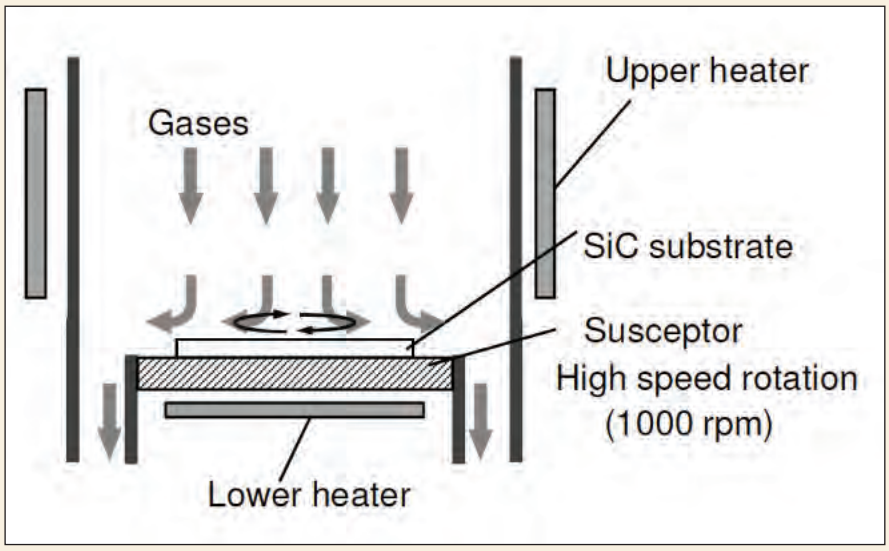
The team has determined the roles of rotation speed and pressure on growth rates. It has carried out a series of experiments involving deposition of SiC on 4H SiC substrates with a 4° off-cut silicon face. Rotating at 50 revolutions-per-minute (rpm), changes in pressure had little impact on growth rate. But when rotation was cranked up to 1000 rpm, changes in pressure from just below 100 mbar to almost 1000 mbar more than double growth rates to around 50 μm/hour.

At higher pressures, improvements in thickness uniformity with increasing rotation speed are magnified: At 500 mbar, uniformity can be around 0.25 percent at 1000 rpm, compared to 1.5 percent at 50 rpm, when uniformity is defined in terms of the standard deviation divided by the mean.

Really high pressures are not recommended, however. Simulations suggest that at 800 mbar a swirl of gas near the edge of the chamber can be generated, which could lead to particles that contaminate the wafer.

Employing a system pressure of 267 mbar and a rotation speed of 1000 rpm, engineers deposited a 9.3 μm film of 4H SiC on a 3-inch wafer at a growth rate of 37 μm/hour. Total morphological defects in this epiwafer were just 0.2 cm^{-2}, while the root-mean-square roughness of the film was just 0.18 nm.

Turning to a 150 mm substrate and depositing a slightly thicker film at an identical pressure produced thickness and doping uniformities of 2.8 percent and 5.2 percent (uniformities are defined in terms of the standard deviation divided by the mean, and calculated using a 6 mm edge exclusion).



Although the SiC reactor is similar to those used for silicon epitaxy, the hot zone features a higher number of heaters: As well as the two-zone lower heater, there are additional upper heaters. Resistance heaters are used throughout, and precise control of the radial temperature uniformity across the entire wafer is possible with a lower heater system featuring inside and outside heaters.

H. Fujibayashi *et. al.*
Appl. Phys. Express **7** 015502 (2014)

CSindustry awards2014

The 2014 CS Industry Awards recognise success and development along the entire value chain of the compound semiconductor industry The nomination process has now closed and the shortlist has been decided. The following companies are all worthy winners but only one can lift the trophy. Who wins, you decide. Please use your vote and make your nomination count. Reward and recognise the companies who are driving the industry to new heights.

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  PVDNC AlN Templates
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- **Infineon AG**
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R & D Award
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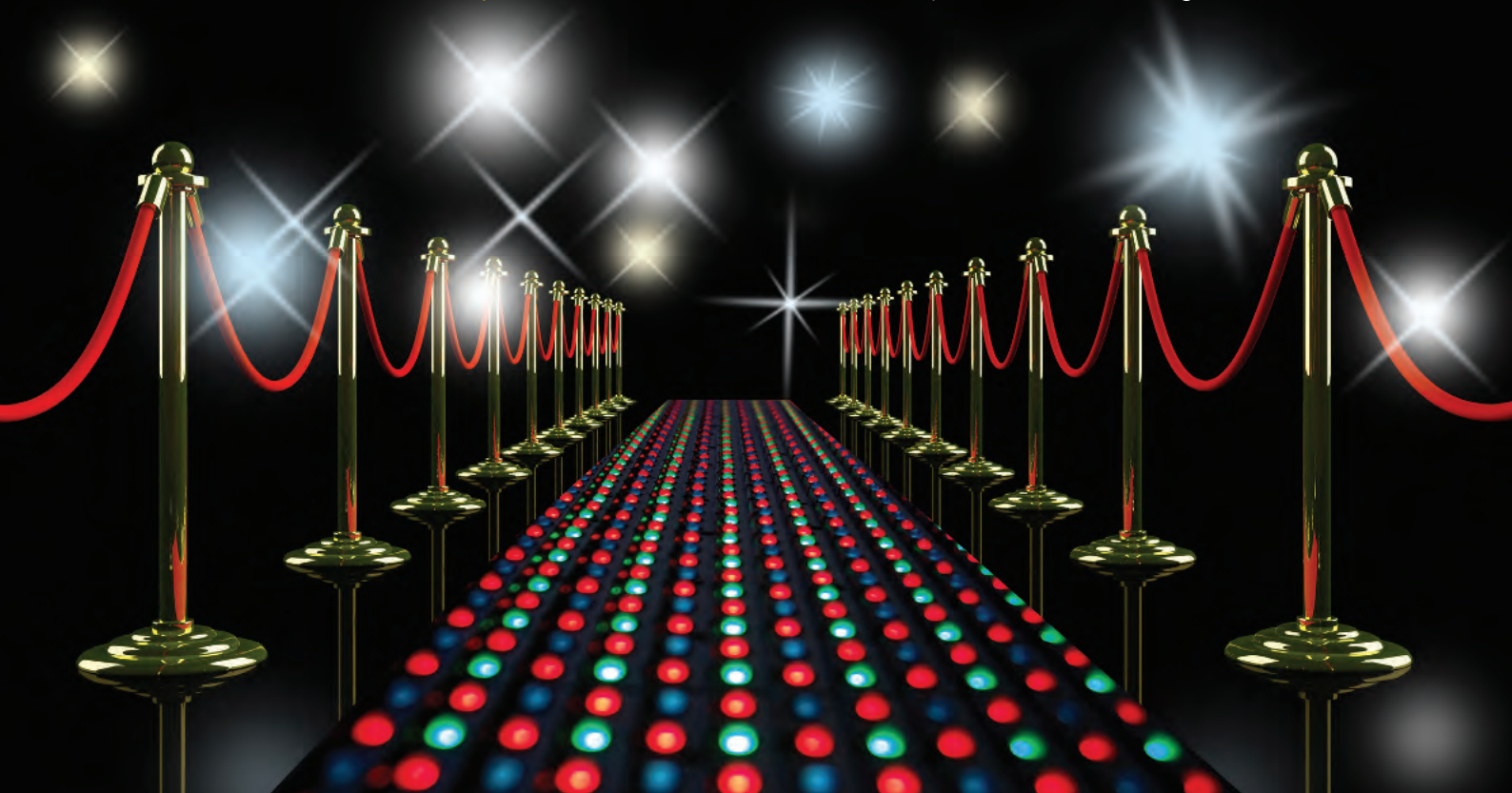
  4 Junction Cell

For further information please contact: Jackie Cannon at jackie.cannon@angelbc.com



Debut for double-quantum-well tunnel FET

Novel tunnel FET targets low power and radio frequency applications

ENGINEERS FROM MIT are claiming to have fabricated the first tunnel FET with a double quantum well InGaAs/GaAsSb structure.

Additional accomplishments for this team, which work at the Microsystems Technology Laboratory, are a first demonstration of area-dependent drive current for this class of device and the realisation of backward-diode operation characteristics (backward diodes deliver their highest current when reverse biased, due to tunnelling of carriers).

This team's novel FET is a promising device for two types of application: It has the potential to deliver a very low sub-threshold swing – a measure of the change in voltage needed to increase the drive current by an order of magnitude – making it attractive for low power applications; and as a backward diode, it could find deployment in radio frequency applications for mixing and detection.

One of the team's motivations for developing its double quantum well TFET has been to expand the drive current range capable of delivering a low sub-threshold swing. Previous forms of TFET have demonstrated a sub-60 mV/decade sub-threshold swing, but only at low drive currents.

In 2011, Sapan Agarwal and Eli Yablonovitch from the University of California, Berkley, unveiled the results of theoretical investigations, which suggested that density-of-state switching is capable of realising a steep sub-threshold swing over a wide range of drive currents. In order to produce this form of switching, the TFET must feature two quantum wells overlapping in the confinement direction.

The MIT device exhibits this trait, with wells formed by an 18-nm thick *p*-type $GaAs_{0.5}Sb_{0.5}$ layer doped with beryllium to a concentration of 10^{19} cm^{-3}, and a 15 nm-thick *n*-type $In_{0.53}Ga_{0.47}As$ layer doped with silicon to a concentration of 10^{17} cm^{-3}. These epilayers were deposited onto a semi-insulating InP substrate by MBE (see Figure).

Device fabrication involved: patterning with e-beam lithography; the addition of a HfO_2 gate dielectric, which is 5.3 nm-thick, by atomic layer deposition; and removal of GaAsSb to suspend an InGaAs air bridge via a highly selective wet etch. Depositing a layer of Al_2O_3 passivated the device.

Measurements by the team show that the current delivered by their TFET is proportional to its gate area. Four devices were used to determine this, with gate areas ranging from just above 10 μm^2 to almost 90 μm^2.

A weakness of the device is its high sub-threshold swing: its minimum value is 140 mV/decade, and it has an effective value of 220 mV/decade over 20 nA to 2 μA.

The engineers from MIT believe that one of the causes of the high sub-threshold swing is the high off-current. This may originate from leakage through the 30 nm-thick InP buffer layer, and could be addressed by undercutting the InP layer under the drain current.

Another reason for the high sub-threshold swing is the high density of interface traps, which are located in the InGaAs conduction band at the HfO_2/InGaAs interface.

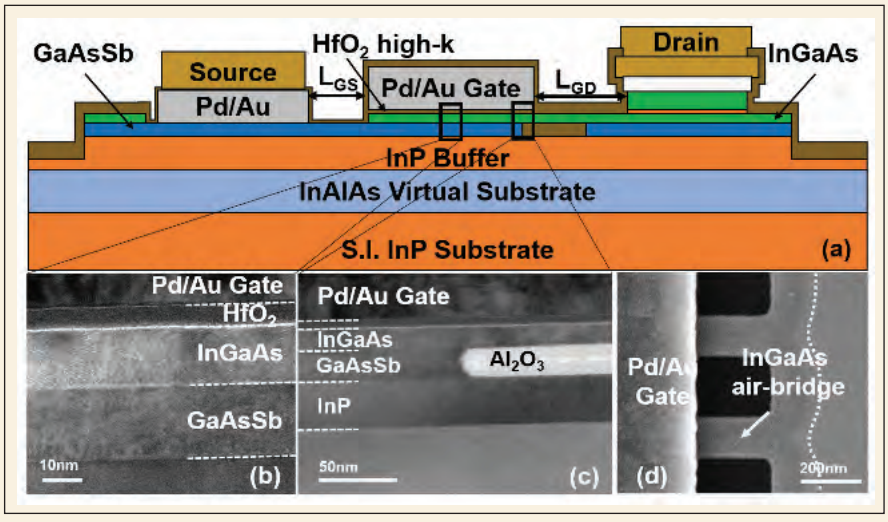
According to capaitance-volatge measurements, the minimum value for the denisty of interface traps is 2 x 10^{12} cm^{-2} eV^{-1}.

"The density of interface traps is mainly due to the dangling bonds on the InGaAs surface, prior to dielectric deposition," explains Tao Yu from MIT, who believes that these traps might be minimised with a passivation step involving chemical methods or plasma treatment.

Measurements of the gated-diode nature of the TFET reveal that it exhibits tuneable backward diode behaviour. The gate bias can be adjusted to optimise minimum noise or high sensitivity.

"We have not yet done a deeper study on the actual RF performance of the device, but according to previous studies on backward diodes, the RF application of the device should be promising after calibration and optimisation," says Yu.

Other plans for the team are to suppress the interface trap density, cut leakage and improve sub-threshold swing through optimisation of the gate dielectric and device architecture.



Engineers from MIT have fabricated a double quantum well FET (a). Cross-sectional tunnelling electron microscopy provides images of the tunnelling junction and gate stack in the gated region (b), and the edge of the InGaAs air bridge (c). A top view of the air-bridge, after suspension, is provided by a scanning tunnelling microscope (d).

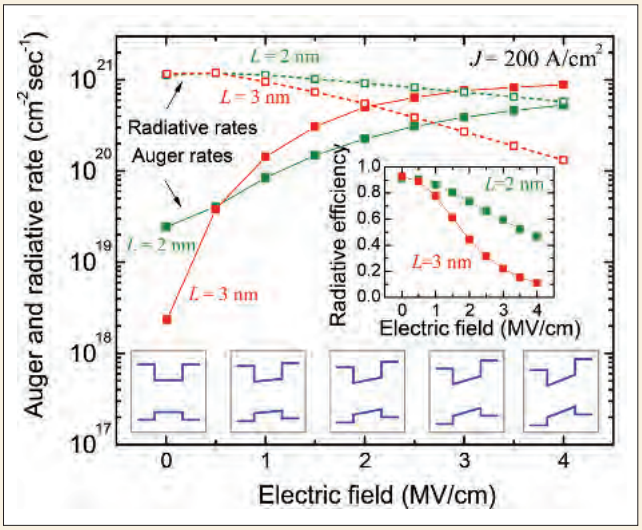
T. Yu *et. al.*
IEEE Electron Dev. Lett. **34** 1503 (2013)

Combatting droop in ultraviolet LEDs

Gradual variation in quantum well composition promises to slash Auger rates in AlN/GaN LEDs

ULTRAVIOLET LEDs, like their visible cousins, suffer from droop, a decline in efficiency with increasing current density. But it should be possible to combat this unwanted phenomena in conventional, polar LEDs by turning to active regions with a gradual variation in quantum well composition. This modification compensates for the effect of the electric field acting on the holes.

This opportunity for improvement is one outcome of a theoretical study by an international partnership that has revealed how the polarization field in an AlN/GaN LED magnifies Auger recombination, and also edges up radiative recombination.



Eight-band calculations reveal the dependence of Auger and radiative recombination on the electric field strength in quantum wells of differing thickness. The inset details the plummeting internal quantum efficiency with increasing field strength.

"We present an intuitive explanation of why such an enhancement should occur, and we support it with calculations," says Roman Vaxenburg from Technion, who has carried out this work as part of a team that includes university colleague Efrat Lifshitz, Anna Rodina from Ioffe Physical-Technical Institute and Alexander Efros from the Naval Research Laboratory.

The multi-national team has also considered non-polar LEDs: Their latest calculations indicate that Auger-induced droop should be present in InGaN/GaN LEDs, but not in their GaN/AlN cousins. "These two materials have different energy gaps, which strongly affects the efficiency of the Auger process in the non-polar case," explains Vaxenburg.

He and his co-workers argue that in all forms of LED, the probability of non-radiative Auger recombination – a process involving the excitation of charge carriers to continuum states – is governed by the overlap between the wavefunction of the localised initial state and that of delocalised carriers.

Due to strong polarization fields in the quantum well, polar LEDs feature sharp corner-like features and a tilted shape of the confining potential. This creates high Fourier components in the localised carrier wavefunctions that match the momentum of the excited carrier, leading to high rates of Auger recombination.

According to Vaxenburg, the team's calculations are rather difficult to do: "All the steps, from the theory construction to the actual coding, are very involved. Fortunately, we ended up with a very efficient code, which allowed us to collect all the data within a few weeks, running several powerful computers."

Even such complex calculations can fail to accurately describe every aspect of the LED. The team's current eight-band model ignores contributions from higher energy bands and neglects screening effects created by free carriers, which could modify the electric fields in the structure.

"However, the general effect of the Auger enhancement by the electric field should persist, because the sharp features in the potential profile will be there in any case," argues Vaxenburg.

Calculations considered quantum well widths of 2 nm, 2.5 nm and 3 nm, electric fields from 0 to 4 MV cm^{-1} and an injection current of 200 A cm^{-2}. Radiative rates in all wells decrease at higher fields, due to decreasing electron-hole overlap.

This impact is greatest in the widest wells, where carrier separation is more pronounced (see Figure). Meanwhile, the Auger rate increases by one-to-three orders of magnitude with increasing field strength.

One upshot of the changes in Auger rate and radiative rate is a strong reduction in internal quantum efficiency with increasing electric field. Note that when this field is zero, however – which is the case for a non-polar AlN/GaN LED – the radiative rate is far higher than the Auger rate.

The latter finding suggests that in polar AlN/GaN LEDs, the Auger rate, which is governed by a hole-hole-electron process, could be suppressed by restoring a rectangular confining potential for the holes. This is possible by gradually varying the quantum well layer composition to create a gradual increase in bulk energy gap.

Goals for the team include an extension of the calculation beyond the standard eight-band model. "We will add a more realistic self-consistent profile, which will depend on the carrier concentration and will reflect the screening effects," explains Vaxenburg.

R. Vaxenburg *et. al.*
Appl. Phys. Lett. **103** 221111 (2013)

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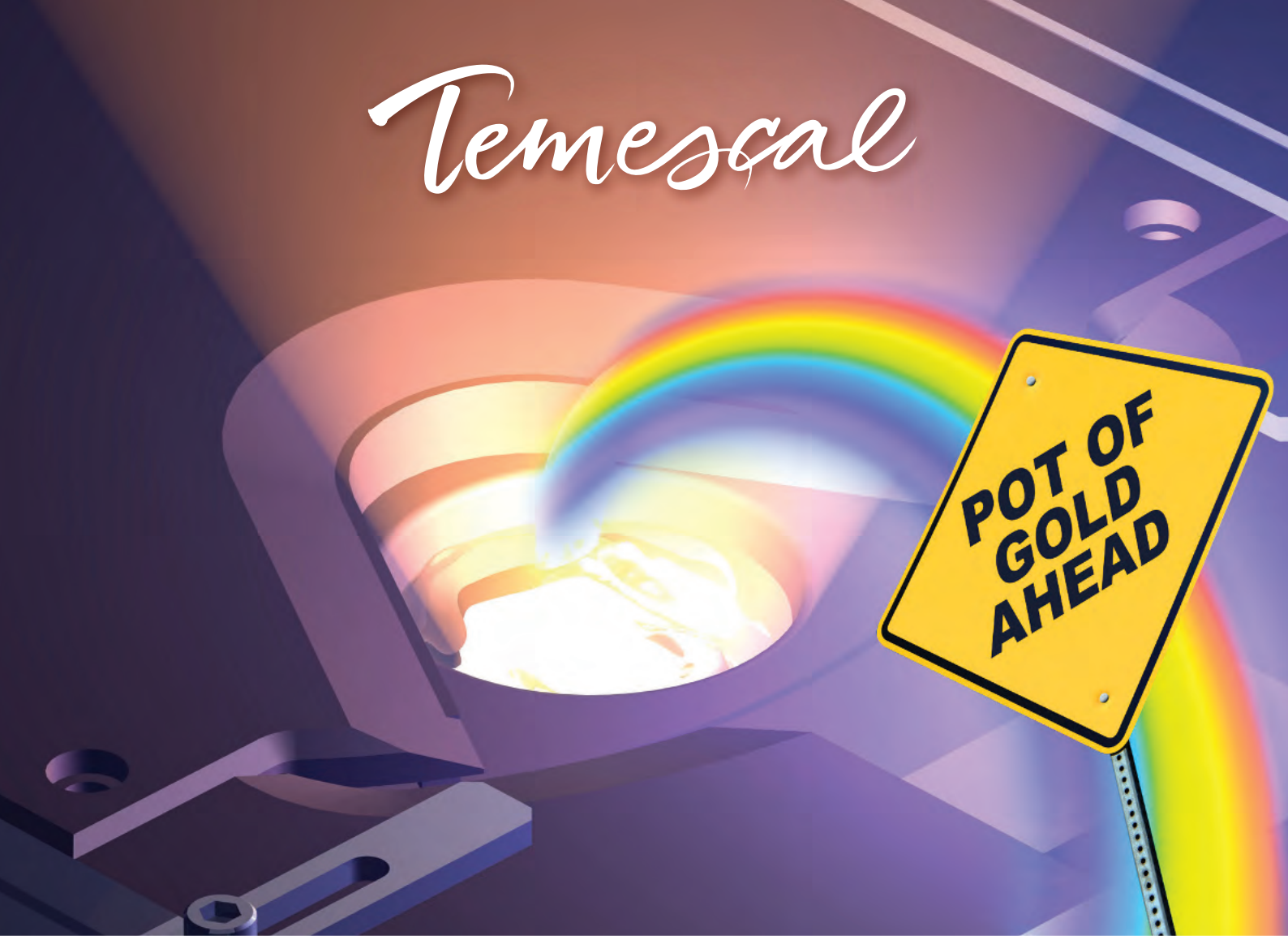

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At Temescal, we're dedicated to mapping and better understanding the dynamics of the flux cloud. Through extensive testing and research, we have collected hundreds of vapor cloud maps and used these maps to advance and automate the process of lift-off uniformity mask design.We can help you find the pot of gold in your metallization process.

To find out more, visit **www.temescal.net/auratus-gold** or call **1-800-552-1215**.

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