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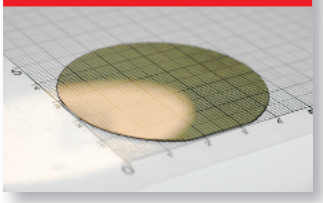
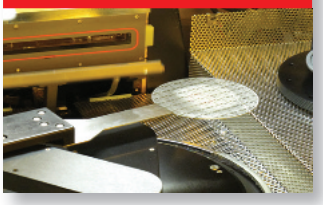
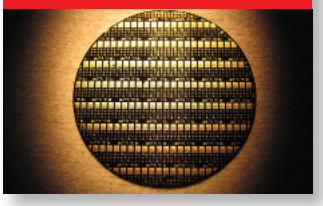
Great GaN yields better devices



Capacity hike for GaN transistors



Cooling HEMTs with diamond



Turbo-charging the VCSEL

Bigger wafers for GaN-on-silicon

Translucent

Perfecting GaN-on-silicon

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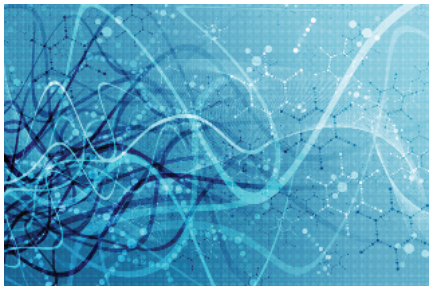
ALWAYS ONE STEP AHEAD

editorial view

by Dr Richard Stevenson, Editor

A really radical device

AT THE HEART OF EVERY ISSUE OF this magazine lie a collection of features detailing breakthroughs at the chip level. All these articles describe some aspect of novelty, which is more radical in some cases than others.



Breakthroughs that are important, but not revolutionary, would include improvements to existing device architectures. This might be the insertion of a superior photonic structure into an LED that leads to an increase in extraction efficiency, a new gate stack that cuts the density of interface traps in a III-V MOSFET, or a different style of field plate that trims the leakage current in a GaN HEMT.

More radical is the creation of a new device. It might be formed by building an entirely new structure, or it might result from merging two devices into something that exceeds the sum of the parts.

In this issue, we have a contribution in this latter vein from John Dallesasse and Kanuo Chen from the University of Illinois at Urbana-Champaign. This duo has combined a quantum cascade laser (QCL) and a transistor to create a novel source that can produce emission from the mid infrared through to terahertz frequencies.

Their three-terminal hybrid improves on the capability of the QCL, a promising device for gas sensing. With the QCL, changing the operating voltage shifts the emission wavelength, making it possible to conduct a frequency sweep through the absorption peak of gas molecules. However, when the operating voltage of the transistor is changed, it alters the injection of carriers into the active region, and thus the output power of the laser.

Turning to the transistor-injected QCL eliminates this variation in output power, because it is then possible to independently control the injected current and the voltage across the active region. What's more, by dithering the base-collector bias voltage at a fixed emitter-base bias, the laser's frequency can be modulated, aiding the detection of chemical species.

But will this device be used for gas sensing on a grand scale, or will it be confined to academia? Well, signs are good for commercialisation. Its design is similar to a HBT – the main differences are the addition of optical confinement layers on the top and bottom of the device and the inclusion of a cascade region. This means that it should be possible to make the device in a GaAs IC foundry. So maybe, just maybe, this device will be more than just radical – it will be commonplace too.

Editor Richard Stevenson richardstevenson@angelbc.com +44 (0)1291 629640

Contributing Editor Rebecca Pool editorial@rebeccapool.com
News Editor Christine Evans-Pughe chrise-p@dircon.co.uk
Director of SEMI Publishing Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205

Senior Sales Executive Robin Halder robin.halder@angelbc.com +44 (0)2476 718109

Sales Manager Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215

USA Rep: Brun Media: Tom Brun E: tbrun@brunmedia.com Tel: +001 724 539-2404
Brun Media: Janice Jenkins E: jjenkins@brunmedia.com Tel: +001 724-929-3550

Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200

Design & Production Manager Mitchell Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214

Circulation Director Jan Smoothy jan.smoothy@angelbc.com +44 (0)1923 690200

Chief Operating Officer Stephen Whitehurst stephen.whitehurst@angelbc.com +44 (0)2476 718970

Directors Bill Dunlop Uprichard – CEO, Stephen Whitehurst – COO, Jan Smoothy – CFO, Jackie Cannon, Scott Adams, Sharon Cowley, Sukhi Bhadal, Jason Holloway.

Published by Angel Business Communications Ltd,
Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK.
T: +44 (0)1923 690200
F: +44 (0)1923 690201
E: ask@angelbc.com

Angel Business Communications Ltd
Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK.
T: +44 (0)2476 718 970
F: +44 (0)2476 718 971
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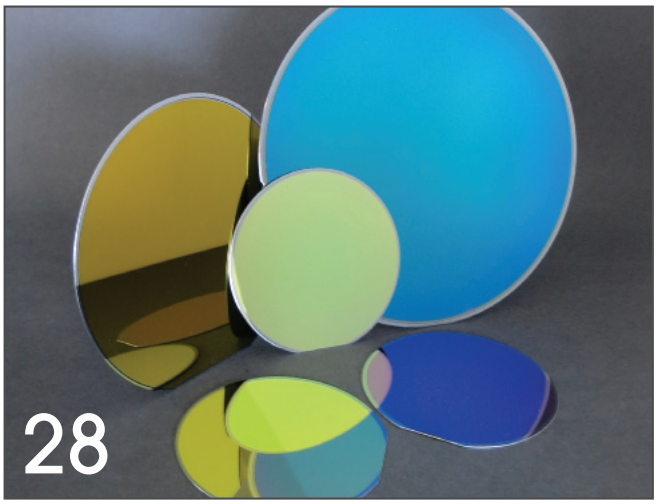

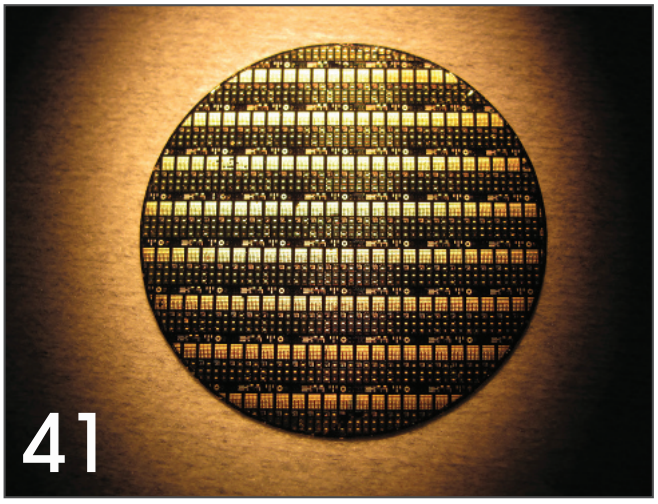

Global LED market to reach $42.7 billion by 2020

ACCORDING to a new market research report *Global Light Emitting Diode (LED) Market (Technology, Application and Geography), 2013 – 2020* by Allied Market Research, the LED (chips and components) market is forecast to reach $42.7 billion by 2020, registering a CAGR of 13.5 percent from 2014 to 2020.

Asia Pacific leads the LED technology market with approximately three quarters of the global electronics manufacturing industries. North America, due to its high-tech forensic and medical applications leads the market for UV LEDs. It is anticipated that LED lights will command about 20 percent share of the global lighting market by 2020. This will be equivalent to two thirds of the revenue for LED. However, the demand for basic LED in backlighting applications would decline as OLED broadens its horizon of applications and would eventually supersede basic LED mobile displays.

UV LEDs are mainly used in medical treatments and forensic tests. According to the report, further development of the market is expected as companies rigorously work out acquisitions to expand their product portfolio and applications. In January 2013, Noblelight acquired Fusion UV, manufacturer of UV LED technology. Developed regions, though, are early adopters of the UV LED technology; the healthcare sector in developing regions such as Asia Pacific is also contributing to the growth of the technology. The growing medical tourism and lower cost of treatments will strengthen the adoption of UV LED technology in developing regions.

Governments across the globe are implementing LED lighting in most of the public settings to save energy. The US government has already started replacing the conventional street lights with LEDs, which it is anticipated to complete by the end of 2014. Such developments will be instrumental in the growth of the LED market. "The growth in revenue will be slower than the rise in unit sales of LEDs due to the constantly declining price of LEDs; however, the overall market would grow at a constant pace due to growing demand for LEDs and expanding applications" states

AMR analyst Ranjan Singh. "Continuous development in the technology suggests huge underlying potential for OLEDs during the forecast period," adds the analyst citing the recent rollouts of OLED mobile handsets by Samsung and Nokia. High brightness (HB) LEDs hold nearly 60 percent of the market share as it can provide much brighter light with lower voltages as compared to other market alternatives. The rapid growth in 4K TV segment suggests that HB LED will continue to hold the key to the growth of LED technology market. Major companies such as Samsung SDI and RIT Display are investing substantially on the development of advanced OLED display technologies.

Rising application of LED in general lighting has compelled manufacturers to concentrate on new LED lighting products and expand their production. OSRAM opened its LED assembly plant in Wuxi, China, to expand its fully loaded LED capacities and also to strengthen its market position in the global LED market. The company has chosen the plant location in China to capture the highly potential Asian market.

Notable players in this space include and profiled in report are American Bright Optoelectronics, Cree, International Light Technologies, Ledtronics, Philips Lumileds Lighting Company, Samsung Electronics, Seoul Semiconductor, OSRAM Licht AG, Nichia, LG Innotek, GE Lighting Solutions and Toyoda Gosei.

Nichia, Samsung, and Osram held nearly 35 percent share in the global LED market revenue in 2013. Allied Market Research (AMR) is the market research and business-consulting wing of Allied Analytics LLP based in Portland, Oregon, USA.

RFMD and TriQuint renamed Qorvo

RF MICRO DEVICES and TriQuint Semiconductor have revealed that their combined companies will be renamed Qorvo.

Pronounced kor-vo, the new name is said to convey the combined company's ability to deliver the core technologies and innovation that will enable customers to launch their next-generation designs even faster. "We believe that our new name reflects our company's commitment to keep customers at the centre of all that we do," said Bob Bruggeworth, RFMD president and CEO, who will serve as Qorvo's CEO following closing of the merger. "As a new leader in RF solutions, Qorvo will offer the agility, innovation and precision customers need for success in mobile, infrastructure, and defense markets."

"Our companies have been RF industry pioneers developing many of the core technologies our world now relies on," said TriQuint CEO Ralph Quinsey, who will serve as non-executive Chairman of Qorvo following closing of the merger. "Qorvo is building from our foundation of true innovation to solve our customers' most difficult challenges. We do this so that their customers, whether mobile consumers or troops on the move, will be able to connect with loved ones, protect our security, or voyage to new lands."

Shareholders of both TriQuint and RFMD voted to approve the merger on September 5th, 2014, and the transaction is expected to close in the second half of 2014, following other required regulatory approvals and satisfaction of customary closing conditions. Qorvo is expected to be traded on the NASDAQ Global Stock Market under the ticker symbol 'QRVO' after the merger.

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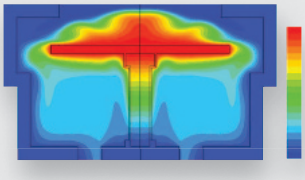

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Emcore announces sale of space PV activities

EMCORE, a provider of compound semiconductor-based components, subsystems, and systems for the fibre optics and space solar power industries, has announced that it has entered into a definitive agreement with an affiliate of private equity firm Veritas Capital.

Under this agreement, the affiliate of Veritas has agreed to purchase Emcore's space photovoltaics business for $150 million in cash. The transaction is subject to approval by Emcore's shareholders and other customary closing conditions and is currently expected to close in December 2014 or January 2015.

Emcore's Space Photovoltaics business was founded in 1998 and is based in Albuquerque, New Mexico. The business provides products for space power applications including high-efficiency multi-junction solar cells, coverglass interconnected cells and complete satellite solar panels, along with terrestrial applications, including high-efficiency multi-junction solar cells for concentrating photovoltaic power systems.

"Veritas Capital is excited to be associated with Emcore's space photovoltaics business. The management and employees at Emcore have an established history of providing leading technology and reliable products to the worldwide satellite industry.

We look forward to continuing this excellent track record under our ownership and to working with the Space Photovoltaics team to expand the business," said Benjamin Polk, Partner of Veritas Capital.

"Veritas' proven track record of fostering growth in high-technology and defense industry companies makes it an excellent fit for Emcore's Space Photovoltaics business. Emcore's board ofdDirectors and management team believe this transaction will benefit our satellite customers while providing considerable value to our shareholders," said Hong Hou, president and CEO of Emcore Corporation.

US scientists grow GaAs films on low cost substrates

III-V SEMICONDUCTORS such as GaAs make highly efficient solar cells but the GaAs or Ge substrates used for their epitaxial growth account for more than half of the cost, giving limited use in terrestrial photovoltaic applications.

While efforts have been made to grow high quality single-crystalline GaAs and III-V materials on low-cost substrates such as metal foils, they have not been very successful. Either the cost-reduction has been insufficient for making solar cells for terrestrial use or the opto-electronic properties have become degraded so the power conversion efficiency is low.

Now a research team from the University of Houston, South Dakota School of Mines and Technology, and NASA Johnson Space Center, has reported the heteroepitaxial growth of high mobility, single-crystalline-like *n* and *p-type* doped GaAs thin films on inexpensive, flexible metal foils using an MOCVD process. The GaAs films exhibited hole and electron mobilities as high as 66 and 300 cm^2/V-s, respectively. The epitaxy enabling substrate for GaAs growth was single-crystalline-like Ge thin film on biaxially textured templates made by ion beam assisted deposition on metal foil.

According to the team, the GaAs films on metal foils showed single-crystalline-like nature, strong biaxial texture, low grain misorientation (less than 2^o) and strong photoluminescence at room temperature. Precise control of doping and carrier concentration was achieved, resulting in GaAs films with high carrier mobility and electrical conductivity.

The researchers believe the work can pave the path for roll-to-roll manufacturing of flexible III-V solar cells for the mainstream photovoltaics market.

'High mobility single-crystalline-like GaAs thin films on inexpensive flexible metal substrates by metal-organic chemical vapor deposition' by P. Dutta et al, appeared in Appl. Phys. Lett. **105** 092104.

Riber introduces compact new 3inch research MBE system

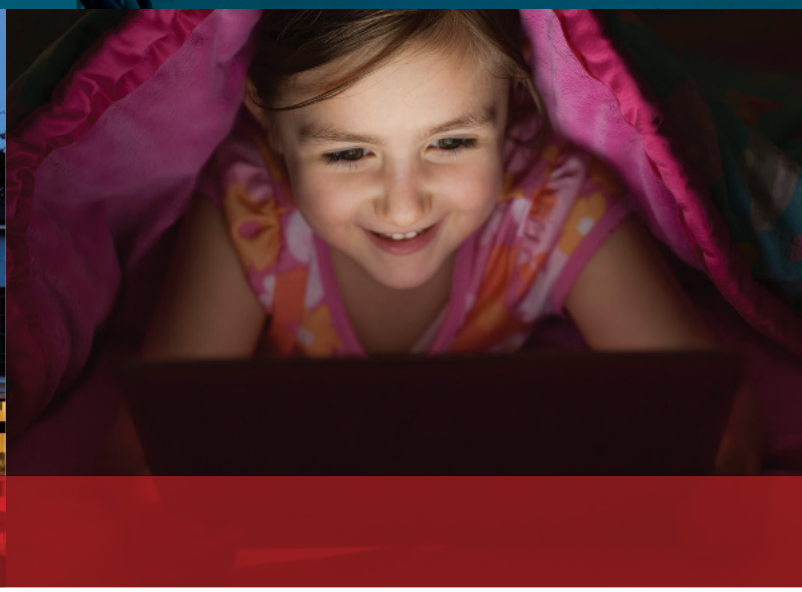
RIBER has launched a new 3inch substrate MBE research system, the Compact 21 Discover, which it presented at the 18th International Conference on Molecular Beam Epitaxy, held in Flagstaff, USA.

The new model is claimed to revolutionise research MBE by presenting the reactor on an open frame, enabling 360 degree access to the machine's components and incorporating the transfer rod, traditionally a fragile, long part of the system, into the electronics cabinet.

The company describes it as the most compact and ergonomic 3inch MBE system on the market.

Based on the recent Compact 21DZ, the Discover is also the only 3 inch MBE system on the market to combine 12 symmetric cell ports with a 10 inch central port, offering flexible performance.

Lower Cost LEDs



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Learn how Veeco's TurboDisc EPIK700 GaN MOCVD system can improve your LED manufacturing process today.

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Veeco's New TurboDisc EPIK700 GaN MOCVD System

Dow Corning sets new standard for 150 mm SiC wafer crystal quality

DOW CORNING, the supplier of silicon and wide-bandgap semiconductor technology, has announced that it now offers 150mm diameter SiC wafers under its Prime Grade portfolio.

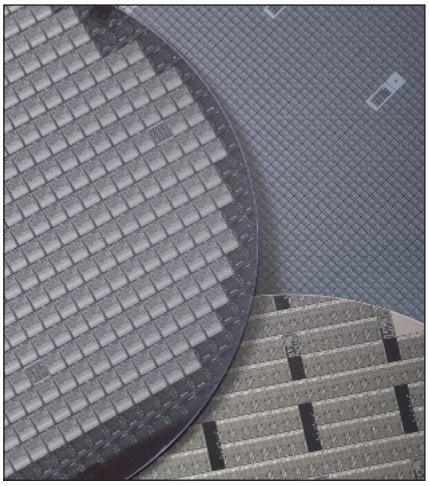
Recently launched to set new standards for 100 mm SiC wafer quality, the portfolio also offers three tiers of manufacturing quality 150mm SiC substrates: Prime Standard, Prime Select and Prime Ultra. Each tier offers increasingly stringent tolerances on critical defect types that adversely impact device performance, such as micropipe density (MPD), threading screw dislocations (TSD) and basal plane dislocations (BPD).

"SiC wide-bandgap power semiconductors have rapidly evolved from a cutting-edge niche into an established technology sector that is increasingly focused on the manufacturing economies afforded by SiC crystal quality, wafer size and other critical factors," said Tang Yong Ang, vice president, Compound Semiconductor Solutions, Dow Corning.

"Dow Corning's decision to expand its Prime Grade portfolio to include 150mm diameter SiC wafers aims to meet this very competitive demand.

As we rapidly scale production of these high-quality wafers, our customers will be able to more confidently pinpoint the SiC substrate that optimizes the performance and cost of their next-generation device design while leveraging the improved economies of scale offered by larger wafer diameters."

While many SiC wafer manufacturers promise low micropipe densities for their 150mm substrates, Dow Corning is



among the first to specify low tolerances of other defect types, such as TSD and BPD. Such defects reduce device yields, and inhibit the cost efficient manufacture of large-area, next-generation power electronic devices with higher current ratings.

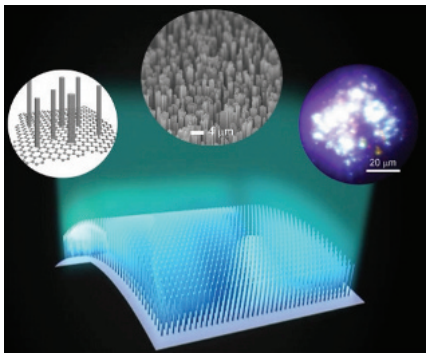
Bendy LEDs and solar cells are one step closer

FLEXIBLE ELECTRONICS and optoelectronics devices are usually made with organic materials. But inorganic compound semiconductors such as GaN would offer better optical, electrical and mechanical properties if it were possible to grow them on flexible substrates.

In a new open access journal APL Materials, a team of Seoul National University (SNU) researchers led by Gyu-Chul Yi describes their work growing GaN micro-rods on graphene to create transferrable LEDs and enable the fabrication of bendable and stretchable devices. The picture below shows the process.

"GaN microstructures and nanostructures are garnering attention within the research community as light-emitting devices because of their variable-colour light emission and high-density integration properties," explained Yi.

"When combined with graphene substrates, these microstructures also show excellent tolerance for mechanical



deformation." Ultrathin graphene films consist of weakly bonded layers of hexagonally arranged carbon atoms held together by strong covalent bonds. This means graphene can provide the desired flexibility with mechanical strength. Also it's also chemically and physically stable at temperatures in excess of 1,000 ^{o}C.

To create the actual GaN microstructure LEDs on the graphene substrates, the team uses a catalyst-free MOCVD process they developed back in 2002. "Among the technique's key criteria, it's necessary to maintain high crystallinity, control over doping, formation of heterostructures and quantum structures, and vertically aligned growth onto underlying substrates," Yi says.

When the team put the bendability and reliability of GaN micro-rod LEDs fabricated on graphene to the test, they found that "the resulting flexible LEDs showed intense electroluminescence and were reliable - there was no significant degradation in optical performance after 1,000 bending cycles," noted Kunook Chung, the article's lead author and a graduate student in SNU's Physics Department.

"By taking advantage of larger-sized graphene films, hybrid heterostructures can be used to fabricate various electronics and optoelectronics devices such as flexible and wearable LED displays for commercial use," said Yi.

The article, 'Growth and characterizations of GaN micro-rods on graphene films for flexible light-emitting diodes' by Kunook Chung et al appeared today in the journal APL Materials.

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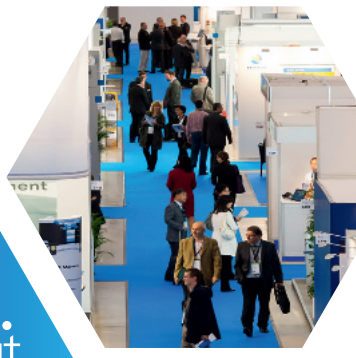

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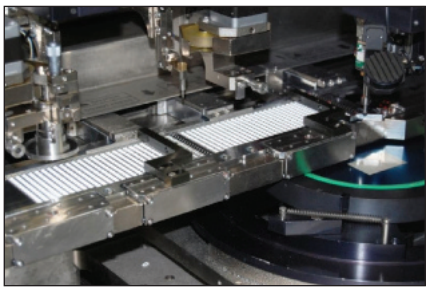
Plessey adds in-house LED assembly line to UK facility



PLESSEY has added an LED assembly line to its expanding Plymouth UK facility. The company says the assembly line will enable it to focus on its high brightness LED growth plans based around its solid-state lighting and sensing business, taking new products from concept to production in less time whilst also functioning as an innovation centre for next generation LED packages.

The Plessey bespoke assembly line uses a laser saw process and finishes with an automatic test for industry standard PLCC (Plastic, Leadless Chip Carrier) packages.

The line includes die attach, wire bonding, phosphor mixing, encapsulation and singulation, in addition to all the other industry-standard, supporting equipment and processes. Designed specifically around speed and flexibility, the line will provide customers with engineering samples for evaluation and pilot builds ahead of full production.

Mike Snaith, Plessey's operations director said: "The industrialisation of GaN-on-Silicon LED technology does not end at producing wafers - it also requires as much attention to the back-end processing to ensure that all the benefits we make at wafer level are fully realised in the final product. This is the best way to provide customers with the LED products they need."

Plessey's Plymouth facility is already demonstrating returns for this transition, enabling it to build working samples of complete in-house filament prototypes for the new market of LED filament replacement bulbs. The filament prototypes use a dedicated die and assembly, all of which is designed and manufactured within the facility.

Keith Strickland, Plessey's CTO, added: "The fact that we are recruiting recognised industry shapers from the world of solid-state lighting is a tangible endorsement that the Plessey value proposition is both exciting and credible." The facility brings additional benefit with wafer sawing and going forward, new LED packaging standards will be established to match the benefits made at wafer level. Plessey's assembly line investment is the start of this cycle of innovation where a revision of the value chain for LEDs and solid-state lighting is taking place.

Plessey's MaGIC (Manufactured on GaN-on-Si I/C) High Brightness LED (HBLED) technology has won awards for its innovation and ability to cut the cost of LED lighting by using standard silicon manufacturing techniques.

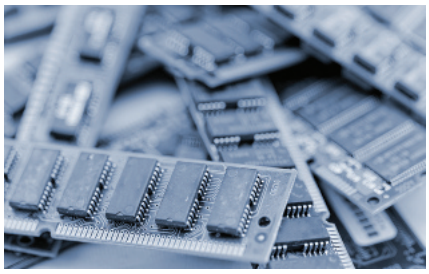
Plessey's range of products for lighting applications will be on show at LuxLive, ExCel London, 19-20 November.

GaN to drive pulsed RF power chip market

MARKETS FOR PULSED RF power devices up to 18GHz are expected to show continued growth over the next five years despite the current economic turmoil and cuts in defense spending. While their association with consumer spending fuels the volatility of many global electronics markets, pulsed RF power devices are supported by quite different priorities. According to market analyst ABI Research, the pulsed RF power semiconductor device market will exceed $300 million by 2019, with GaN driving growth.

"Many RF power semiconductor manufacturers are on a quest to find markets unrelated to mobile wireless infrastructure," notes ABI Research Director Lance Wilson. "Device prices in wireless infrastructure are falling, and the total available market is flattening out."

Some markets that use pulsed RF power devices, such as transportation safety and military, are experiencing solid growth even in the midst of today's economic downturn. These devices are used in radars for military, weather and marine applications, and in the current worldwide upgrade of the air traffic control system. There is also a market segment devoted to the avionics transponder and air navigation market, which is also lifted by the overall air traffic control upgrade.



Intrinsically less "optional" than many consumer markets, these segments are therefore less sensitive to economic upheavals than consumer-driven markets, although they are not totally immune to the macro economy. Understanding this, many semiconductor manufacturers are attempting to enter this market space; however, some factors may complicate their efforts. Pulsed RF power device markets are becoming very competitive technologically: GaN and SiC devices are vying for market share along with the more established Si and GaAs based technologies.

However, the market may not be able to support all the new entrants. "Undoubtedly some consolidation will continue to occur. While not guaranteed success, those companies that have a track record working with government agencies and defense contractors are going to have an advantage over those that are new entrants," adds Wilson.

In the article "The maturing MOSFET" in the August&September 2014 edition of *Compound Semiconductor* the name of John Palmour, Cree's chief technology officer, was spelt incorrectly. We apologise for this error.

IQE, Win and NTU to create compound semiconductor centre in Singapore

IQE has entered into a Memorandum Of Understanding (MOU) with Win Semiconductors and Nanyang Technological University (NTU) to participate in the formation of a centre of excellence for the development of compound semiconductor technology in Singapore.

The MOU anticipates the creation of a new entity called the Compound Semiconductor Development Centre (CSDC), which will be jointly owned by IQE, WIN, NTU, local management and key academics. The centre is expected to start operations next quarter.

The three partners believe that compound semiconductor technology will play a significant role in the future of the overall semiconductor industry, and that this initiative will provide a focal point for effective collaboration between industry and academia in developing next generation technologies.

It recognises the significant investment that is already been made globally into the many emerging markets for compound semiconductors, and its purpose is to accelerate the development of the technology in Singapore, and provide an effective incubator for bringing new innovations to market.

The Economic Development Board of

Singapore has played an important role in pulling this initiative together, which provides a good fit with other compound semiconductor development activities being undertaken in Singapore such as the SMART-LEES initiative. These initiatives are creating next generation IP in Singapore which will support continued economic growth and prosperity in Singapore.

This project forms part of IQE's global reorganisation plan. As part of its contribution to this joint venture, IQE will be providing facilities, equipment and IP on favourable terms to the CSDC. As a consequence, IQE is creating provisions of £4.2m for asset impairment comprising the transfer of tools to the CSDC and £7.7m for the lease of existing buildings and facilities.

Drew Nelson, chief executive of IQE, said: "IQE is proud to be a founding partner of the CSDC. It represents a very innovative approach to making the most of the skills and talent that exist in Singapore. We believe that this will provide an effective route to overcoming the barriers that prevent new ideas and innovations being successfully brought to market and advancing and commercialising new compound semiconductor technologies. This initiative is a strong fit with IQE's strategy for technology leadership."

Yoon Soon Fatt, NTU said: "We have built an exciting compound semiconductor capability within NTU. The CSDC provides a meaningful collaboration for us with two key industrials within the compound semiconductor industry. We are very pleased to be partnering with IQE and WIN. We look forward to the opportunities that this presents"

Terence Gan, director of electronics at the Singapore Economic Development Board said: "Singapore is committed to develop the compound semiconductor industry and welcomes the creation of CSDC. Compound semiconductors make energy efficient LED lighting and fibre optic communications possible, and will enable the creation of ultra-fast and ultra-energy efficient semiconductor integrated circuits. CSDC is an important partner to grow our pipeline of compound semiconductor R&D talent."

Sofradir announces megapixel IR detector for space programs

SOFRADIR, the French developer of advanced IR detectors, has launched the Next Generation Panchromatic detector (NGP), a 1024 x 1024 visible to short wavelength infrared (SWIR) Focal Plane Assembly.

According to the company, NGP is the first European-made space-oriented megapixel array that space agencies can consider for deep space science (planets and asteroids studies), Earth observation and Earth monitoring (meteorology, global warming studies, agriculture surveillance,...) applications. Sofradir developed the large format NGP, which is based on mercury cadmium telluride (HgCdTe) technology, as part of an R&D contract with the European Space Agency (ESA). NGP's 1k x 1k format is four times larger than existing Sofradir SATURN starring array IR product currently deployed on observation satellites or spacecraft. The NGP detector has already been selected this year for the SENTINEL-5 mission planned for launch by 2021 on-board METOP-SG satellite in order to monitor the Earth atmosphere from a polar orbit.

"Sofradir is extremely proud to make the large format NGP 1024x1024 visible to SWIR detector available to our customers focusing on space applications," said Philippe Chorier, space department manager at Sofradir. NGP 1k2 attests to Sofradir's increasing technological leadership in producing reliable and high performance IR products for space applications. The product's ready-to-deploy feature responds to demands to shorten space mission delivery times or to minimize the risks in delays. Based on its added performance and time saving benefits, we anticipate a lot of interest in NGP 1k2 in future space missions".

Infrared detectors from Sofradir are currently on-board Helios II (Earth observation) and Spirale (early warning system) military satellites, as well as the Venus Express scientific probe (SPICAV / SOIR instrument - Spectrometry for Investigation of Characteristics of the Atmosphere of Venus / Solar Occultation IR-).

Its IR products were also to be deployed in space instruments on Sentinel 2, part of the European GMES (Global Monitoring for Environment and Security) space initiative, on the TROPOMI/Sentinel 5 Precursor (part of the GMES), the hyperspectral Earth observation systems PRISMA (Italy) and HYSUI (Japan), as well as on scientific instruments such as Phobos Grunt and Nomad (ExoMars Trace Gas Orbiter). Other programs in progress include: MUSIS/CSO (successor of HELIOS II), MTG (Meteosat Third Generation, ESA), and SGLI (Second generation GLobal Imager) instrument onboard GCOM-C (Global Change Observing Mission -Climate), HAYABUSA2 (asteroid study) or CHANDRAYAAN-2 (lunar surface mapping).

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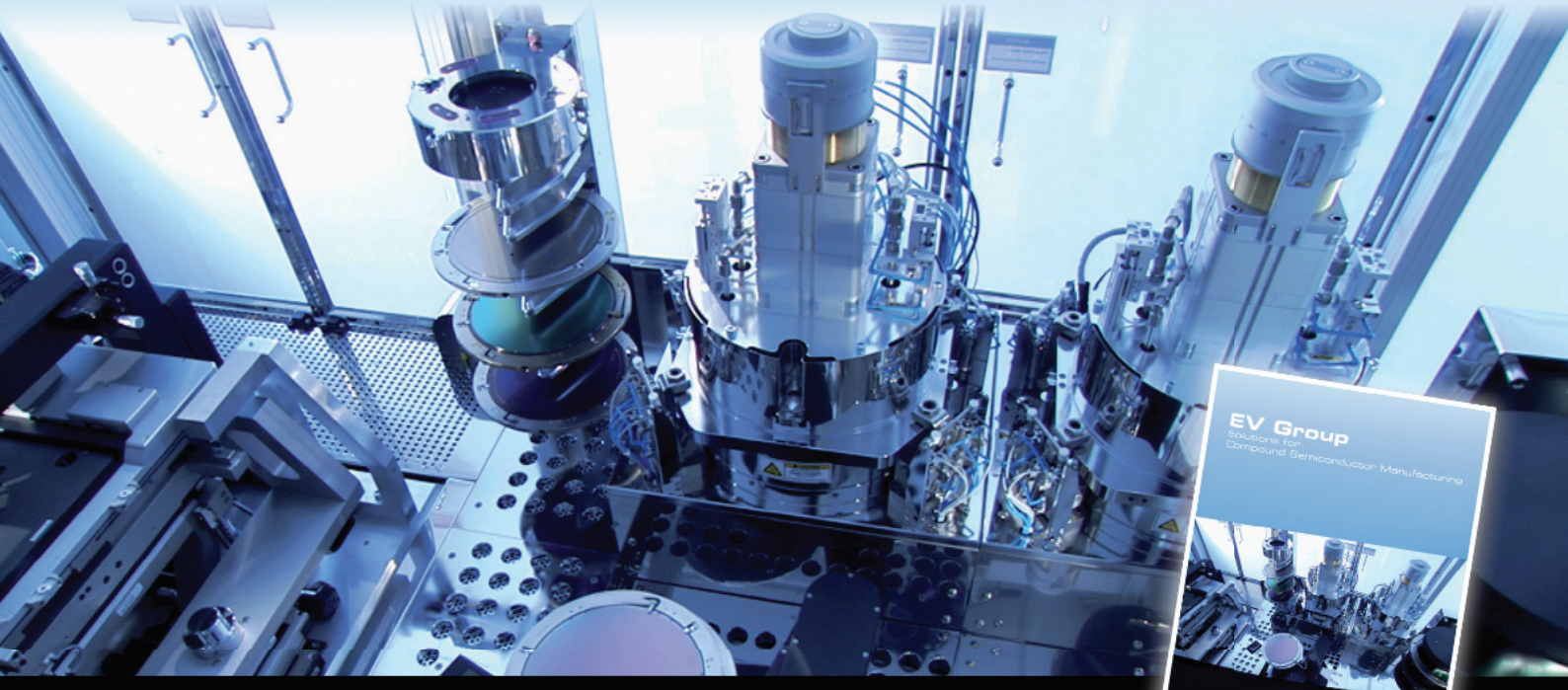

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Merck KGaA to acquire Sigma-Aldrich

MERCK KGaA and Sigma-Aldrich have entered into a definitive agreement under which Merck KGaA, Darmstadt, Germany, will acquire Sigma-Aldrich for $17.0 billion (€13.1 billion), establishing one of the leading players in the $130 billion global life science industry.

Merck KGaA, Darmstadt, Germany, will acquire all of the outstanding shares of Sigma-Aldrich for $140 per share in cash. The agreed price represents a 37 percent premium to the latest closing price of $102.37 on September 19, 2014, and a 36 percent premium to the one-month average closing price. The transaction is expected to be immediately accretive to Merck KGaA,

"This transaction marks a milestone on our transformation journey aimed at turning our three businesses into sustainable growth platforms", said Karl-Ludwig Kley, Chairman of Merck KGaA, Darmstadt, Germany's Executive Board. "For our life science business it's even more than that: it's a quantum leap.

"In one of the world's key industries two companies that fit perfectly together have found each other to present a much broader product offering to our global customers in research, pharma and biopharma manufacturing and diagnostic and testing labs. As such, the

combination of Merck KGaA, Darmstadt, Germany, and Sigma-Aldrich will secure stable growth and profitability in an industry that is driven by trends such as the globalization of research and manufacturing."

He added: "What's more, the combination gives us the possibility to invest even more in innovation going forward. We are delighted to make this compelling proposition to Sigma-Aldrich's shareholders, who will obtain full and certain cash value for their shares."

Rakesh Sachdev, president and CEO of Sigma-Aldrich, said, "We are excited to join forces with Merck KGaA, Darmstadt, Germany, a distinguished industry leader. This transaction is a clear validation of our success in transforming Sigma-Aldrich into a customer-focused and solutions-oriented global organization. This is a testament to the strength of the Sigma-Aldrich brand and the accomplishments of our 9,000 employees worldwide.

"We believe this is a very positive outcome for our shareholders, who will receive a significant premium, and our employees, who will benefit from enhanced opportunities as part of a larger, more global organisation."

In the Laboratory & Academia business, together EMD Millipore and Sigma-Aldrich will offer their customers a complementary range of products across laboratory chemicals, biologics and reagents. In pharma and biopharma production, Sigma- Aldrich will complement EMD Millipore's existing products and capabilities with additions along the entire value chain of drug production and validation.

Shaped over almost 350 years by a family of owners, Merck believes that the combination will afford new opportunities to employees at both companies. It plans to maintain a significant presence in St. Louis, and in Billerica, following completion of the transaction, as well as in important EMD Millipore sites such as Darmstadt and Molsheim, France.

Veeco's ion beam technology reaches milestone

VEECO INSTRUMENTS has announced that its new OdysseyIon Beam Deposition(IBD) Upgrade for the NEXUS IBD-LDDSystem has repeatedly produced photomask blanks with zero deposition defects larger than 70 nm. This represents a significant milestone toward the manufacture of semiconductor devices with advanced extreme ultraviolet (EUV) lithography, according to the company.

EUV mask blank defects are, as a practical matter, impossible to repair and can render a semiconductor device useless. Because of this, mask blank defects have been a key obstacle toward high volume manufacturing.

"EUV lithography brings chipmakers the ability to manufacture higher performing devices at lower cost compared to manufacturing methods which rely on multiple patterning steps," said Ron Kool, senior VP of EUV product and service marketing at ASML, the Netherlands-based lithography systems company. "As ASML is making steady progress preparing the scanner and light source for industrial high volume manufacturing, the readiness of the EUV industry, including mask blanks, is critically important to our customers. Veeco's dedication to the Odyssey upgrade program, done in coordination with customers, consortia, and other industry stakeholders, is a model for EUV infrastructure advancements."

Veeco IBD technology leads the industry in high film quality, featuring extremely low particulate deposition and precise control of optical properties for single or multi-layer processes. These technology features are required for defect-free, high volume EUV manufacturing. Currently, all of the leading EUV mask blank manufacturers use the Veeco NEXUS IBD-LDD system.

"Veeco is committed to working with our customers and industry partners to advance the EUV roadmap and increase the output of defect-free mask blanks," said Jim Northup, Senior Vice President and General Manager of Veeco Advanced Deposition & Etch. "We have made significant investments in the Odyssey upgrade and consolidated our optical coating and ion beam resources in a single R&D site to ensure ongoing development of our industry-leading IBD technology."

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Electric vehicles:

SiC and beyond

As recent forecasts from Lux Research predict SiC devices will crack auto-markets by 2020, have GaN-on-silicon alternatives stalled? Rebecca Pool investigates

WITH THE MARKET FOR DISCRETE POWER electronics components set to reach some $15 billion by 2020, manufacturers are racing to deliver SiC and GaN-on-silicon devices with higher current densities and better thermal management than the silicon incumbent. Industrial, electronics and renewables generation applications all demand these smaller, more efficient wide bandgap devices, but right now, by far the most promising market for power electronics makers is electric vehicles.

As Lux Research analyst, Pallavi Madakasira, highlights, efficient power electronics is crucial to reducing battery sizes in electric vehicles, which has massive knock-on benefits for the rest of the automotive system including wiring, packaging and weight.

"Once you start achieving the efficiency savings, you can get away with having a smaller lithium ion battery, and then you only require, for example, a smaller heat sink, so you cut costs and save space and weight," she says. "[Efficiency savings] have a cascading effect across the entire system that really do add up."

In her latest research, Madakasira forecasts SiC device manufacturers, such as Infineon, Cree and ST Microelectronics, will cash in on the auto-market's growing performance needs before GaN contemporaries, with SiC diodes displacing silicon devices as early as 2020. "Silicon carbide has a significant lead in the industry primarily due to the sheer number of developers that have invested in the technology," she says. "Big volume manufacturers, such as Infineon and ST churn out several hundreds of thousands if not millions of diodes."

In contrast, Madakasira reckons only around two GaN-on-silicon manufacturers are offering products at lower voltage applications. And as she adds: "We know that the GaN developers are not planning to target the automotive industry anytime in the near future, at least not in the next three to five years."

Instead, these GaN players are already making in-roads to renewable generation and grid storage markets. "Certification [in automotive markets] takes time and GaN players cannot generate revenue overnight here," says Madakasira, "We will see the first GaN solar inverter from Transphorm hitting the market come 2015. The technology must make its mark and establish credibility here before transitioning to what might seem like a more daunting automotive market."

In the meantime, SiC devices looks set to reach plug-in hybrid electric vehicles first, where power savings equate to greater reductions in overall vehicle cost. As Madakasira points out, electric vehicles such as the Nissan Leaf probably won't contain a SiC device, as the battery is already small and a more exotic diode or transistor is simply too expensive for this low-end model.

"The cost savings must offset the pricier SiC device," she explains. "This cannot happen in the Nissan but we do expect plug-in vehicles to be the sweet-spot

The Mitsubishi Concept GC-PHEV; PHEV's are expected to be the sweet-spot for SiC devices.

for these types of solutions." But it is only a matter of time before GaN-on-silicon devices reach electric automotive markets. Madakasira reckons the technology will probably catch up within the decade, with products being released come 2023, once devices have been tried and tested in other applications.

"It's a common misconception that SiC is the only technology that is ideal for automotives. Yes, SiC can operate at the high temperatures but not every function within the vehicle requires [this]; so for GaN, it's a question of when, not if," she says. "Then we also expect to see hybrid systems, either a combination of silicon, SiC and GaN, or simply a combination of GaN and SiC."

Cost shouldn't pose a major issue for later GaN-on-silicon entrants. While the cost of growing complex buffer layers on silicon substrates negates some of the obvious cost benefits using these large diameter wafers, devices will still be cheaper than SiC products. "GaN-on-silicon device prices will never be as cheap as [pure] silicon alternatives but they will likely be cheaper than SiC devices where substrate costs have always been high," explains Madakasira.

And the analyst reckons future prospects may still exist for GaN-on-SiC devices, at the high voltage applications currently reserved for SiC devices. "It's a given that SiC can do really well at high voltages [900 V and beyond], but can GaN-on-SiC do that too?" she asks.

"Companies claim to have the know-how, still there is not any business commercialising these products right now, so it remains to be seen."

BluGlass rises to MOCVD challenge

From LEDs to power electronics, BluGlass's low temperature plasma-based CVD process is set to ease GaN-on-silicon fabrication and offer a cool alternative to MOCVD. Rebecca Pool reports

FOLLOWING LAST YEAR'S hefty injection of Aus$3 million (£1.67 million) in federal funds to demonstrate high efficiency, cheap GaN LEDs, Australia-based semiconductor process developer, BluGlass, is now revealing results.

In July, this year, the company claimed its best ever light output from a *p*-GaN layer, grown via its low temperature remote plasma CVD process (RPCVD), onto a MOCVD partial LED structure. And in early August, the company unveiled a scaled-up version of its RPCVD system that's set to accelerate the development of brighter LEDs.

The company has spent nearly a decade developing its low temperature process to grow GaN, and more recently, *p*-GaN layers on MOCVD structures. To achieve low temperature growth, the company replaces the ammonia source of an existing MOCVD system with nitrogen gas, passed through an electrical coil to

generate a plasma. Directly supplying nitrogen via a plasma allows the company to deposit layers at relatively low temperatures. Actual figures remain elusive, but BluGlass's aim is to match the temperatures used to grow MOCVD multi-quantum wells.

While the company has worked with Emcore/Veeco systems in the past, this time round it has retrofitted a larger Thomas Swan/ Aixtron system. As Bluglass chief technology officer, Ian Mann, says: "We haven't been trying to build our own system from the ground-up but, more simply, have been retrofitting the most common systems out there."

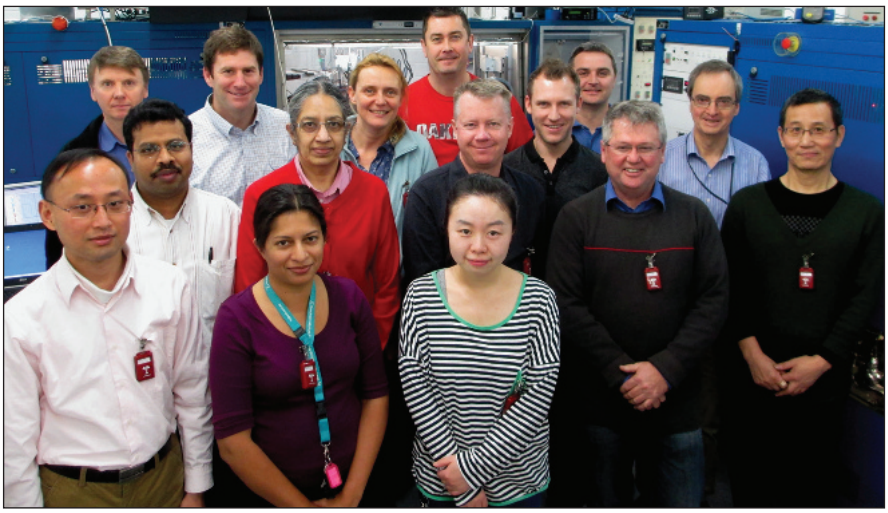
"This latest reactor is well known, is economical to run, and will be capable of generating a single 8 inch wafer," he adds.

To date, BluGlass has been primarily working with two inch sapphire and silicon substrates, but Mann and colleagues hope the new system will help to prove RPCVD at larger wafer sizes. "The reality is, for silicon, 2-inch substrates aren't relevant in the market and most people are going to silicon at larger scales," he says. "Thanks to our lower temperatures, we aim to have better control over cracking and bow in these larger wafers and we've had considerable interest in how this system is going to perform at these wafer sizes."

Mann also hopes the latest retrofit system will tackle the crucial issue of scaling. As he highlights, he and colleagues are always asked whether or not their plasma-based CVD development-sized systems can reliably scale to production processes.

"This system is our answer to that question," he says. "We aim to convince customers that we have taken what we've been doing on the smaller system and repeated this here, while at the same time improving performance."

And as Mann asserts, that the latest Aixtron system isn't a world away from the full-scale systems populating today's production floors." The technology isn't dramatically different; the main difference is that production systems today are larger" he says. "So we feel quite comfortable that our latest system isn't far away from the final platform we are trying to develop."



With the second larger system installed, the BluGlass team is ready to scale up its RPCVD process for LED and power electronics markets [BluGlass].

Research to date has been primarily focused on depositing the RPCVD *p*-GaN layer onto the MOCVD-grown multi-quantum well layers. As Mann explains, the growth initiation of this layer and subsequent growth had proven a real challenge, so he and colleagues developed their existing reactor to operate with a higher density nitrogen plasma.

"This enhanced plasma system has formed a core part of our intellectual property and has proven critical to good growth," he says. "The way the MOCVD ends becomes the beginning of RPCVD growth, so we've made some subtle but simple changes to the final MOCVD [processes], which has helped ultimate device performance."

And with the growth of RPCVD layers on MOCVD templates in place, researchers are keen to use RPCVD to grow full structures, in much the same way as MOCVD is used to grow entire structures. This second larger system can only help.

"We've been very interested in trying to grow multi-quantum wells and *p*-GaN layers together in the same chamber," says Mann. "We've been very active on our *p*-GaN research, but with the larger system up and running, we can afford to push our research programmes in different directions, and this is something we are keen to put to the test."

Sapphire and silicon

But it's not all about silicon. As Mann emphasises, BluGlass's technology is intended to be 'substrate-agnostic' and right now, the bulk of the LED market is still fabricating structures on sapphire.

Indeed manufacturers have been keen to find out exactly what the company's low temperature RPCVD process can do for multi-quantum well growth.

"With the low temperatures, you can incorporate more indium into the multi-quantum wells, which lets you fabricate LEDs emitting at longer green and yellow wavelengths," he says. "Developing quantum well technology has always been on the cards, and is funded by company's federal Grant. Our second system provides more opportunity to explore such avenues."

Crucially, BluGlass also intends to take its low temperature growth process to power electronics markets. As Mann highlights, almost all HEMT structures are grown on silicon, so manufacturers are grappling with many of the same issues as LED players, a fact he and colleagues hope to exploit.

"There is still this cracking and bowing of large wafers, due to lattice and thermal mismatches between silicon and GaN," he says. "So a low temperature GaN on silicon platform could help power electronics manufacturers as well as LED [suppliers]."

And of course BluGlass's latest system – with its 8 inch wafer capacity – opens more doors to these markets. "Both GaN-on-silicon markets are looking towards larger substrates, LED [players] are looking at eight inch sizes and power electronics developers are looking at six inch substrates," says Mann. "These people are expected to move to eight inches in the future."

Infineon and International Rectifier: WHAT NEXT?

What does Infineon's latest acquisition mean for industry? Rebecca Pool talks to the company to find out its plans

AS THE NEWS SINKS IN that Infineon is to buy International Rectifier, many in the industry are wondering what next?

In its biggest acquisition yet, Germany's largest chipmaker stumped up $3 billion in cash for IR, bolstering its international presence in the US and Asia, and gaining one of the largest manufacturers of power management chips in the world.

The move complement's Infineon's range of high voltage MOSFETs – the biggest chunk of IR revenue came from its low voltage MOSFETs – and also delivers low power IGBTs to its 1000 W to 2000 W range of the same devices. And while Infineon is still reaping the rewards of buying digital power management IC maker Primarion in 2008, IR provides power devices for new markets including notebooks and game consoles.

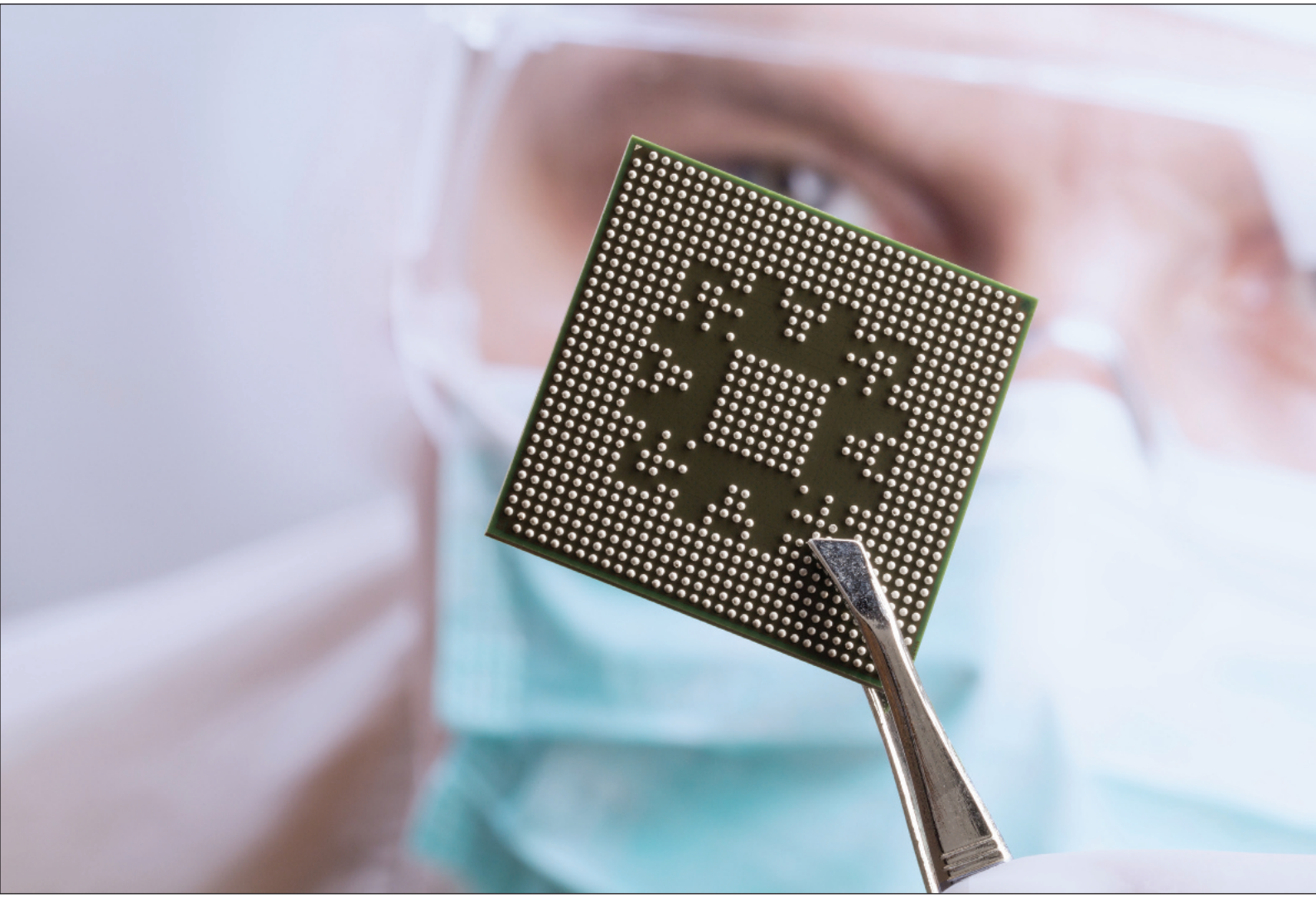
Still, the best may be yet to come. Infineon has been manufacturing SiC diodes since 2001, and introduced its first SiC transistor – the 'CoolSiC 1200 V JFET – last year, which combined with MOSFET and driver IC gives a direct drive device for solar, UPS and industrial drives applications.

But while this has meant the business has had high voltage markets stitched up, the lower voltage end of the market has presented a problem. Not any more; enter IR with its GaN-on-silicon HEMTs for applications of 600 V and less.

"We started GaN research and development, but we haven't had a product on the market yet," says Tillmann Geneuss, manager of communications at Infineon. "It's no secret that, for GaN, companies such as International Rectifier and Transphorm are leading the competition."

Clearly, acquiring IR changes this. As Geneuss points out: "GaN has been a huge effort for IR, and it has generated a lot of intellectual property on the GaN-on-silicon epitaxy process."

And crucially the company has myriad very solid epitaxy-related patents for



depositing the buffer and GaN layers onto the silicon substrate. "There is sapphire, SiC and even bulk GaN, but silicon is the cheapest carrier solution," says Geneuss. "And that's why we think this has been a very valuable effort, because when it comes to the long-term and mass production, you have to look for the most cost-effective way to implement this."

Still Infineon isn't expecting instant gratification from IR's precious GaN-on-silicon technology. According to Geneuss, the market is in its infancy and GaN revenues have been very small for IR and other players such as Transphorm.

"We already are seeing first revenues but expect it will take five years or more before we see really significant revenues," he says.

In the interim the company is firmly focusing on developing 'the best solution' that will include IR's GaN-on-silicon devices and Infineon's SiC products. "Customers require solutions, not individual products, and these new materials will not survive as standalone products," he says. "So we want to include the new technology with, say, our best IGBT, MOSFET or diode, in the best package to offer the best solution in terms of cost-performance-ratio and power density."

So where does Infineon's plans leave other GaN-on-silicon companies? Japan multinational, Panasonic, holds a hefty chunk of the market's GaN-on-silicon IP and is sampling 600 V GaN-on-silicon transistors. But what about the key, but much smaller players, such as Canada-based GaN Systems, EpiGaN, Belgium, Japan-based Transphorm and US-based EPC?

Media reports are already hinting at more acquisitions to come. And as senior analyst from Yole Développement, Philippe Roussel, told *Compound Semiconductor:* "We anticipate more consolidations in the GaN area over the next two years and have several indications to who might be the next ones, but cannot disclose."

And if the GaN-on-silicon market develops slowly, the industry's start-ups could falter. Just less than two years ago, US-based SiC device manufacturer, SemiSouth, closed down. Despite investment from Silicon Valley manufacturer of devices for high voltage power conversion systems, Power Integrations, the up and coming business clearly couldn't generate cash flow in a rising market. Could the same happen to pure GaN players?

As Geneuss concludes: "Introducing components on these emerging wide band-gap materials is a marathon, not a sprint."

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SOLID-STATE LIGHTING

Soaring sales of LED bulbs are creating a great opportunity for chipmakers. But what do companies need to do to stand out from the crowd and win substantial orders while maintaining healthy margins?

KEYNOTE	Opportunities for laser diodes in solid-state lighting **Jon Wierer - SSLS Scientist - Sandia National Laboratories**	Sandia National Laboratories
ANALYST	How will the solid-state lighting evolution unfold, and what will it mean for the LED chipmakers? **Stewart Shinkwin - Market Analyst, LEDs and Lighting - IHS Technology**	IHS
SPEAKER	Commercialisation of GaN on Silicon for LEDs **Keith Strickland - Innovations & Technology Director - Plessey Semiconductors**	plessey
SPEAKER	Increasing LED output with advanced plasma processing **Mark Dineen - Product Manager - Oxford Instruments**	OXFORD INSTRUMENTS The Business of Science®
SPEAKER	Lowering LED epitaxial wafer cost through AlN transition layers using plasma vapor deposition **Scott Kroegar – Vice President, Product Commercialization - Deposition & SiC - GT Advanced Technologies**	GT ADVANCED TECHNOLOGIES

III-V CMOS

By the end of this decade, it is said that silicon CMOS will have run out of steam. But what role will III-Vs have to play in the microprocessors of the future?

KEYNOTE	Heterogeneous integration of III-V's and CMOS **Daniel Green - Program Manager - DARPA**	DARPA
ANALYST	When will III-Vs make an impact in the silicon foundries? And will it last for long? **Mike Corbett - Managing Partner - Linx Consulting**	LINX Consulting
SPEAKER	III-V FETs for future logic applications **Jesus A del Alamo - Director of the Microsystems Technology Laboratories - MIT**	
SPEAKER	Opportunities and challenges of III-Vs in Si-based nanoelectronics industry **Matthias Passlack - Deputy Director - Taiwan Semiconductor Manufacturing Company (TSMC)**	tsmc
SPEAKER	Advanced in-situ metrology for III-V on silicon technology **Kolja Haberland - Chief Technology Officer - LayTec**	LAYTEC Knowledge is key
SPEAKER	Optimization of III-V R&D and manufacturing using advanced analytical methods **Temel Buyuklimani - Senior Director - Quadrupole SIMS Services - Evans Analytical Group**	EAG Evans Analytical Group

POWER ELECTRONICS

From a performance perspective, GaN and SiC are superior to silicon But high prices are holding them back from displacing the incumbent. How can this be addressed?

KEYNOTE	Ditching the package to drive down GaN transistor costs **Alex Lidow - CEO and Co-founder - Efficient Power Conversion (EPC)**	EPC
ANALYST	When can WBG power electronics truly take off? Remaining technical and economic barriers to overcome **Philippe Roussel - Business Unit Manager - Yole Développement**	YOLE Développement
SPEAKER	SiC technology in power electronics – a step change in value **Markus Behet - Global Market Segment Manager - Dow Corning Corporation**	DOW CORNING
SPEAKER	High performance GaN-on-Si power epiwafers employing rare earth oxide buffer layers **David Williams - VP of Business Development - Translucent**	Translucent
SPEAKER	Presentation TBC **Chris Horton - Director, Global Sales & Marketing - Cree Materials Business**	CREE
SPEAKER	Presentation TBC **TBC - KLA-Tencor**	KLA-Tencor
SPEAKER	Developments in PVD technology for power electronics enabling roadmaps in compound semiconductor devices **Reinhard Benz - VP Sales and Marketing - Evatec**	evatec

FRONT-END MOBILES

What's the biggest threat to revenues for GaAs power amplifiers? Is it the emergence of multi-band, multi-mode PAs built with this material, or the emergence of CMOS solutions?

KEYNOTE	The path to intelligent integration **Jim Cable - CEO, President and Chairman - Peregrine Semiconductor**	Peregrine Semiconductor
ANALYST	Multi-mode, multi-band PAs: friend or foe to the compound semiconductor industry? **Eric Higham - Director - Advanced Semiconductor Applications - Strategy Analytics**	STRATEGY ANALYTICS
SPEAKER	Improving system level integration and overall efficiency **Peter Gammel - Corporate CTO - Skyworks Inc.**	SKYWORKS
SPEAKER	LTE is driving complexity in smartphone design **Sean Riley - Vice President of Mobile Products - TriQuint**	TriQuint Reach Further • Reach Faster

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OPTOELECTRONICS

Does the growth of the datacom market signal a long-awaited return to better times for the makers of optical components? Is the CPV industry finally starting to gain a foothold in the solar industry?

KEYNOTE	Presentation TBC **TBC - SOITEC**	Soitec
ANALYST	Where the CPV industry is heading, and what it needs to do to increase its market share? **Karl Melkonyan - Analyst - Solar Research - IHS Technology**	IHS
SPEAKER	Mid infrared light emitting diodes enable portable, battery powered gas sensing **Des Gibson - CEO - Gas Sensing Solution**	GSS
SPEAKER	Presentation TBC **The' Linh Nguyen, Senior Manager IC Development- Finisar**	Finisar

RF-ELECTRONICS

The potential of GaN in the RF arena has never been in doubt. But does it now satisfy all the requirements for deployment in the most taxing situations?

KEYNOTE	GaN for radar applications **Takahisa Kawai - General Manager - SEDI (Sumitomo Electric Device Innovations, Inc.)**	SUMITOMO ELECTRIC DEVICE INNOVATIONS
ANALYST	The Future for GaN, SiC, InP and GaAs in defense/military applications **Asif Anwar - Director - Strategy Analytics**	STRATEGY ANALYTICS
SPEAKER	Presentation TBC **Walter Wohlmuth, Associate VP Technology- WIN Semiconductors Corp.**	win SEMICONDUCTORS

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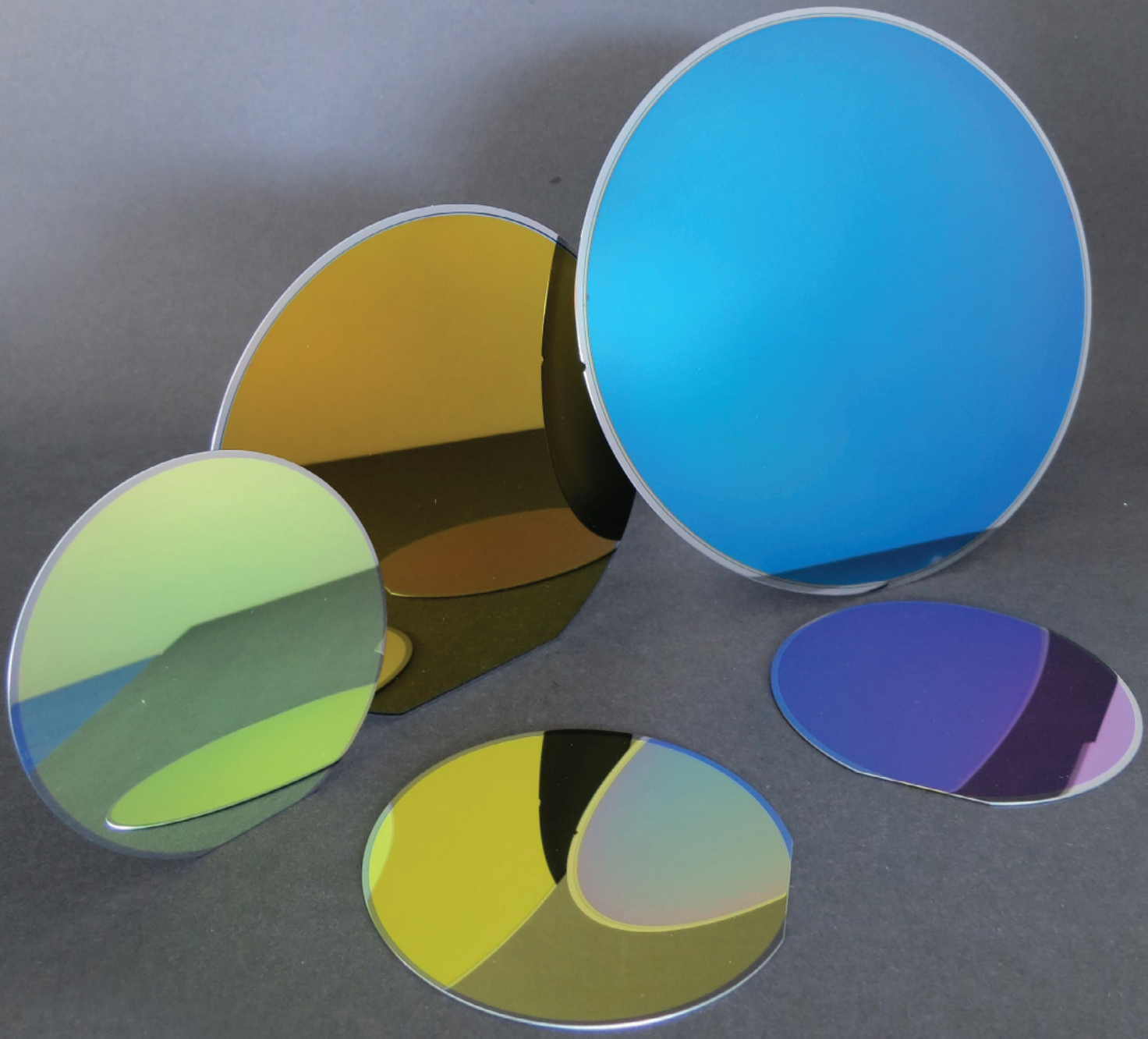

Perfecting GaN-on-silicon

power electronics

Inserting rare earth oxides increases material quality, trims wafer bow and boosts transistor performance

BY DAVID WILLIAMS, ANDREW CLARK, F. ERDEM ARKUN AND RYTIS DARGIS FROM TRANSLUCENT

WITH ELECTRICITY NOW accounting for a staggering 43 percent of primary energy consumption, according to the International Energy Agency, the benefits of efficient energy conversion – from both an environmental and an economic perspective – are bigger than ever. And this pay-off is only going to grow as more electrical systems are manufactured for deployment in electric vehicles, computer power supplies, solar cell inverters and power converters for LED lighting.

One area where the use of electrical systems will grow fastest is in electrical vehicles. Speaking on behalf of Ford at CS International 2014, Power Semiconductor Research Engineer Ming Su revealed that 25 percent of the company's vehicles are expected to be electrified by 2020. Making the electrical conversion in these vehicles as efficient as possible will be high on the priority list of engineers based in the US, because this will help automobiles to satisfy a government mandate for 2025 that demands a fuel efficiency of at least 54.5 miles per gallon.

Thanks to its low cost, widespread availability and familiarity, silicon has been the semiconductor of choice for many years in electrical systems, where it is used to perform various roles, including voltage conversion. However, judged purely in terms of performance, this incumbent is inferior to wide bandgap semiconductors, such as SiC and GaN. Switch from silicon to GaN and it is possible to construct devices that combine a low on-resistance with a low parasitic capacitance, culminating in low power losses when the device is on and when it is switching between states.

These great attributes, which stem from the use of a high-mobility two-dimensional electron gas at the interface between the GaN and AlGaN layers of a HEMT, make this class of transistor a promising device for incorporation into switched-mode power supplies serving many of the applications outlined above. According to the GaN power semiconductor manufacturer EPC of El Segundo, CA, 600 V devices account for a quarter of the overall power transistor market, with devices rated at 200 V or below pulling in three-quarters. Since GaN HEMTs are capable of covering all these voltages, there is good reason to believe that this wide bandgap semiconductor can be adopted in a broad range of power conversion applications.

Foundations for GaN

Ideally, manufacture of GaN HEMTs would involve growth on a native substrate. However, GaN substrates are prohibitively expensive and limited in size and availability, so different foundations must be used. The most common alternative, silicon, enables the fabrication of GaN HEMTs that are competitively priced compared to the incumbent. However, the penalty to pay for growth on silicon is that the production of these devices is far from easy. Engineers don't just have to contend with bow of the epiwafers, caused by differences in lattice constants and thermal expansion coefficients – there are also challenges related to unwanted chemical reactions at the silicon surface.

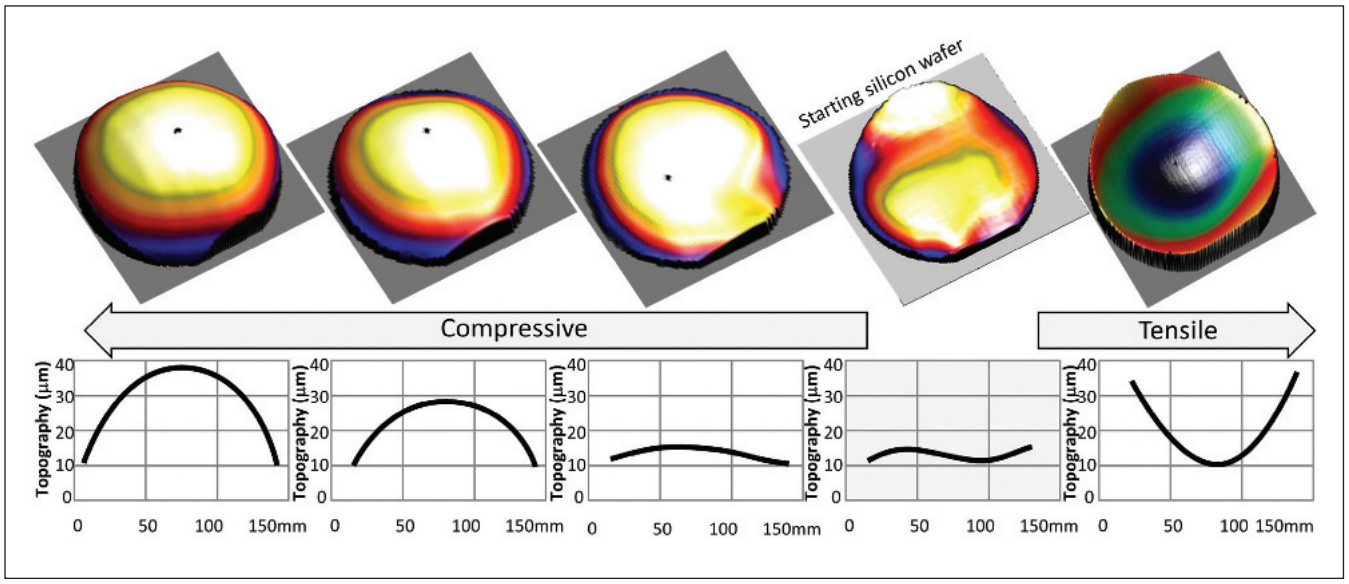

Figure 1. It is possible to control the bow using REO layers. The plot second from the right is a silicon wafer prior to any depositions. Bow measurements are taken using an FRT MicroProf 3D optical profilometer

One unwanted reaction is that of silicon with ammonia to create SiN. This resulting nitride can grow in an amorphous manner, destroying the crystal registration and with it the quality of the overlying GaN. Turning to a gallium wetting-layer is not a viable solution, because silicon is soluble in liquid gallium, so defects arise from the meltback of gallium. This doesn't occur with aluminium, the only alternative wetting material, but in this case the growth conditions have to be carefully controlled to minimise eutectic-driven diffusion of silicon into the upper GaN layers. And if there are any imperfections in the quality of AlN, such as pinholes, GaN can make contact with silicon, leading to meltback defects or silicon diffusion into GaN.

To avoid all of these issues, our team at Translucent of Palo Alto, CA, has pioneered the development of an engineered buffer that aids the transition between silicon and GaN, and returns full design freedom to MOCVD process engineers. Our buffer is an insulating, single-crystal rare-earth-oxide (REO), with a composition carefully chosen to be lattice-matched to the silicon on its lower surface. Meanwhile, an upper surface is engineered so that defect growth is quite dissimilar to that associated with GaN on silicon – and more like that of GaN on sapphire – thanks to the GaN lattice being more closely matched to its foundation.

Benefits of the REO are not limited to lattice matching: this layer is also chemically inert, so it provides a physical barrier to silicon diffusion. Consequently, it is not possible for gallium to come into contact with silicon. What's more, epistructures grown with our engineered substrates can maintain a high degree of lattice registration, because the REO is lattice-matched to the silicon substrate. Note that the top interface between GaN and the REO is chosen to have a small mismatch, because this softens the interface and provides a degree of compliance.

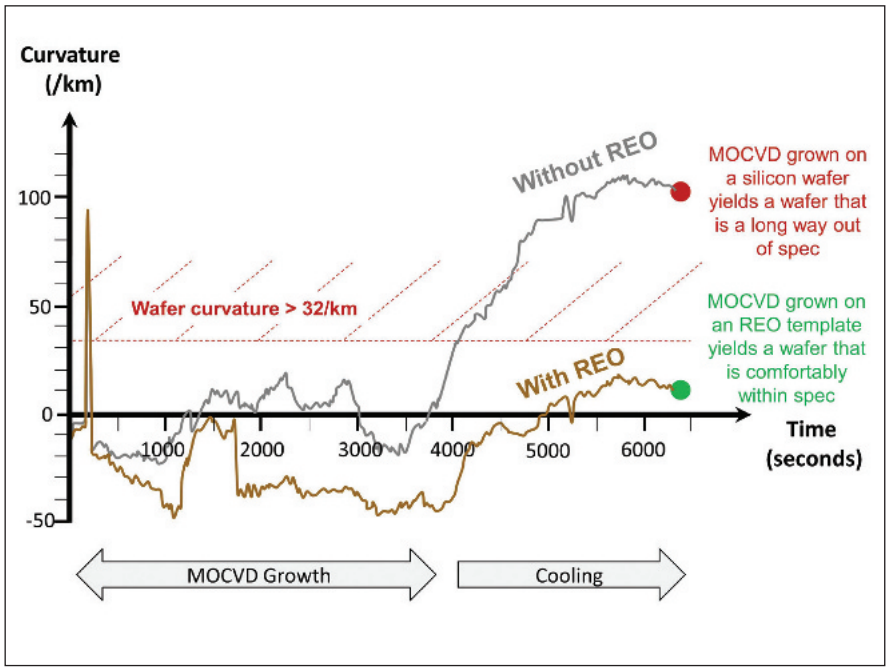

Figure 2. MOCVD bow during growth. This trace shows the curvature of two wafers on the same platen in a run. One was a bare silicon wafer and the other an REO template. In-situ monitoring of the entire process is via a LayTec EpiTT system that records the true wafer temperature, curvature, and reflectivity signals at 450 nm and 633 nm. These tools monitor the evolution of the GaN surface and the quality of the bulk GaN growth throughout the growth process. The start of the MOCVD run is at time = 0, and growth occurs up to 3800 s at which point the wafer begins to cool and tensile bowing starts. When unloaded after 6400 s, the two-dimensional electron gas on the silicon wafer has a curvature of 106/km, where as that grown on the REO template has a curvature of only 11/km. A curvature of 106/km corresponds to a bow of 133 μm, which is out of spec, where as a curvature of 11/km corresponds to a bow of only 14 μm, which is comfortably within spec for this sized wafer.

Benefits of the oxide

Turning to an REO offers a new route to the production of epiwafers with a very low bow, which is a pre-requisite for processing in silicon lines. We can manage bow by pre-straining the wafer. Prior to MOCVD deposition of GaN, we make the wafer dome shaped. Without this, the MOCVD process would naturally result in wafers that are bowl-shaped – but thanks to the pre-straining, we are left with epiwafers that are very flat (see Figure 1, which shows a selection of wafers that have been measured, post REO growth, using a three-dimensional optical profilometer).

By adopting this approach, GaN epiwafers with an REO layer can be flat enough to be compatible with steppers used in microlithography. The requirements originate from the depth of field of the optical system in the stepper, and are defined in terms of maximum bow by SEMI. Wafers with a diameter of 100 mm, must have a bow below 40 μm, while those that are 150 mm and 200 mm across must have bows of less than 60 μm and 65 μm, respectively.

Improvements in device performance also result from inclusion of an REO. This oxide is an insulator, so it increases the transistor's breakdown voltage. In addition, a common failure mechanism is addressed: devices often breakdown due to silicon diffusion, but this can't happen when an REO is involved, because this oxide provides an impenetrable barrier to silicon atoms.

To mitigate this diffusion process when producing conventional devices, thicker GaN layers are required. This adds to production costs, and must be weighed against the expense associated with deposition of a REO layer. Note that the insulating nature of this oxide means

that it also reduces the thickness of GaN required to hit a particular blocking voltage. We anticipate that by preventing diffusion and aiding device robustness to high voltages, we may be able to trim the GaN thickness by at least 25 percent and also potentially remove all of the interlayers. These actions could result in a significant cost saving associated with device production.

A further benefit of our technology is that it is considerably different from other techniques for forming GaN-on-silicon, giving it an enviable position in terms of intellectual property. IP ownership is increasingly viewed as an important asset as the industry matures: Indeed the French market analyst, Yole Développement, recently produced a market report dedicated exclusively to GaN-on-silicon IP, underlining the importance of proper IP protection.

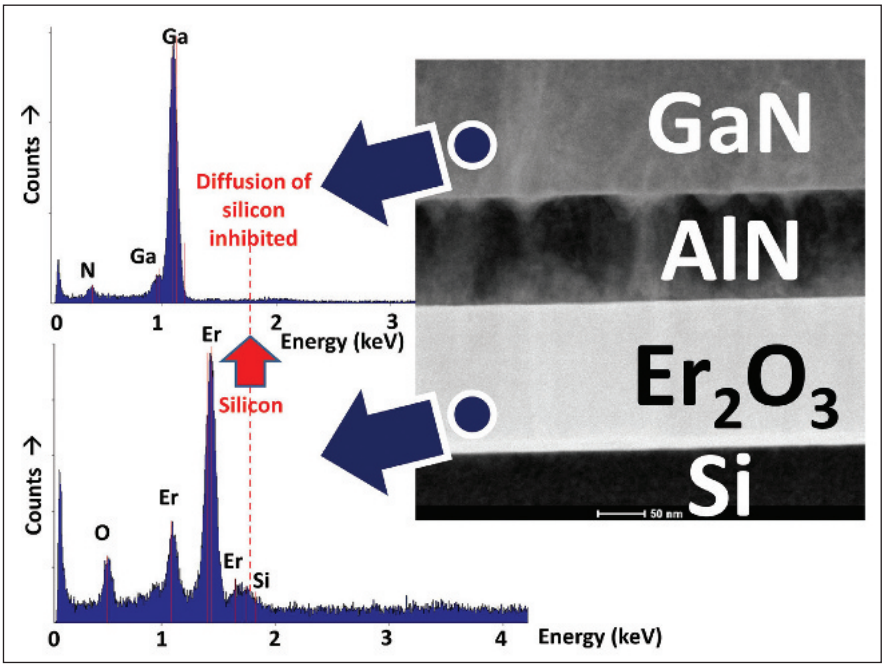

Figure 3. Transmission electron micrograph and composition analysis demonstrates that a rare-earth oxide layer can provide an impenetrable barrier to silicon diffusion.

Promising results

Experimental results on epiwafers and HEMTs back up our claims of the virtues of our REO-based technology for GaN-on-silicon transistors. These efforts included a side-by-side comparison of a 100 mm silicon wafer, and our engineered, REO-based template that had been pre-strained to offset the stresses from MOCVD deposition. These wafers were placed in adjacent pockets in an MOCVD run conducted using a standard sapphire process for the production of 2 DEG HEMT structure. After growth, the epiwafer with the oxide interlayer had less than one-quarter of the curvature of the structure grown on bare silicon, and with a bow of just 14 μm, the epiwafer with the REO layer was comfortably within spec for processing in a silicon line (see Figure 2). In contrast, the GaN-on-silicon wafer was significantly out-of-spec.

By turning to AlN interlayers, it is possible to reduce the bow and manage defect propagation in GaN-on-silicon HEMTs. These AlN layers can also be used within our structures, but we plan to work to reduce and even eliminate them, because we expect the REO to take over much of this functionality (figure 2 shows how an REO layer can be used to bring a process that is out-of spec, to being comfortably within spec, in terms of wafer bow).

Impenetrability of the REO layer to silicon diffusion is proven with a combination of transmission electron microscopy and energy dispersive X-ray analysis of a structure with layers of GaN, AlN, and ErO on top of silicon (see Figure 3). According to the X-ray analysis, there is no trace of silicon in the GaN layer. In addition, no oxygen or erbium is found in the GaN, indicating that the REO does not act as a source of contamination.

High crystal quality of the HEMT structures formed on our engineered templates is revealed in X-ray diffraction plots, which feature relatively sharp AlGaN fringes. The widths of the X-ray peaks can determine dislocation densities in the epitaxial structure, according to the work of Detlef Hommel and co-workers from the University of Bremen.

Values of 600 arc seconds for the (002) reflection and 1400 arc seconds for the (102) reflection suggest that the dislocation density in the GaN layer is 2 x 10^{10} cm^{-2}. In our view, this value is perfectly respectable, and provides further validation that our template provides a good foundation for the subsequent MOCVD growth of GaN.

Another great attribute of our REO layer is that it leads to a growth mechanism that is the same as that for GaN deposited on sapphire, which is the most common substrate for GaN growth, but one that is unsuitable for electrical devices, due to its insulating properties.

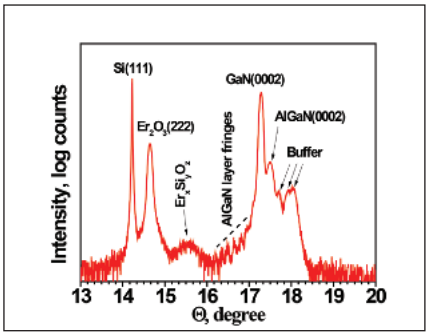

Figure 4. X-ray diffraction uncovers the components of an REO template and GaN 2DEG HEMT structure

Mapping of the surface of GaN grown on REO by atomic force microscopy reveals the presence of parallel atomic steps, indicating that two-dimensional step-flow growth occurs – just like it would on sapphire (see Figure 5).

The quality of the underlying undoped GaN was independently evaluated via Hall measurements – an *n*-doped GaN calibration layer doped to $1.1x10^{18}/cm^3$ had a measured mobility of 250 $m^2 V^{-1}s^{-1}$.

Device results

Using a modified GaN-on-sapphire MOCVD process, HEMT device layers were grown on Er_2O_3-on-silicon (111) templates. An AlN buffer layer was grown on the Er_2O_3, followed by a thick GaN layer, a 3 nm AlN interlayer, an 30 nm-thick barrier layer of $Al_{0.25}Ga_{0.75}N$ and a 1 nm GaN capping layer. Throughout the MOCVD run, laser reflectometry and emissivity corrected pyrometry monitored the growth of the nitride layers.

The finished wafers were processed using a standard interdigitated source and drain design (with no field plates) and employed all of the standard processing steps such as BCl_3/Cl_2 reactive ion-etching and deposition of gold-free contacts that are common to today's GaN-on-silicon FETs.

Typical results for the completed generic device are given in Figure 6. The results confirmed that this new approach for making III-N power FETs on silicon using an REO buffer is a viable alternative to other methods commonly used to deposit GaN on silicon. We demonstrated that, using standard MOCVD processes, devices with perfectly reasonable performance can be made.

Indeed, these devices have a performance that is equivalent to those shown by similar devices not grown on-top of the REO. Additionally, we have demonstrated complete MOCVD design freedom over the available MOCVD processes that can be used because of the chemical and physical properties of the REO layer.

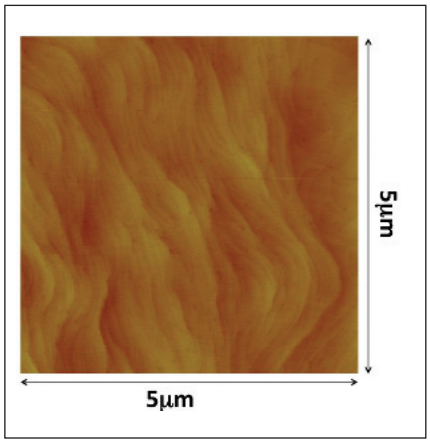

Figure 5. Atomic force microscopy reveals the characteristic step-flow morphology. The z-range is 4.2 nm and the RMS 0.51 nm (MOCVD courtesy of www.bluglass.com.au)

What's next?

We can produce REO templates with diameters of 150 mm and 100 mm, and we are presently ramping-up our 200 mm REO production in our facility. Allied to these efforts, we are engaging with customers and promoting REO templates as a genuine alternative to the step-graded and superlattice approaches that are more commonly employed today.

During these conversations, we are pointing out that our REO material can take on the role of a gate dielectric on top of an MOCVD structure, thanks to its high dielectric constant of 12 to 15.

Our REO-based templates are not limited to serving the power electronics markets – they are attractive options for the production of LEDs and RF devices. One way that these REOs can aid LEDs grown on silicon is by introducing a mirror beneath the active region that stops light from being absorbed by the substrate.

This insertion of a distributed Bragg reflector, however, is not the only role that an REO can play – it can also allow the introduction of the more common orientation of silicon, silicon (100), into the LED industry. Deposition on this orientation of silicon is potentially very useful, because it enables the growth of non-polar and semi-polar GaN, which can lead to higher efficiencies at longer wavelengths, thanks to either the reduction or elimination of energy-sapping internal electric fields.

This opportunity for REO-based templates, alongside their tremendous promise in power electronics, shows that there are multiple benefits to inserting an oxide layer between silicon and GaN. We hope that many will look to pursue this route, and allow us to play a significant role in helping this industry to make better compound semiconductor devices.

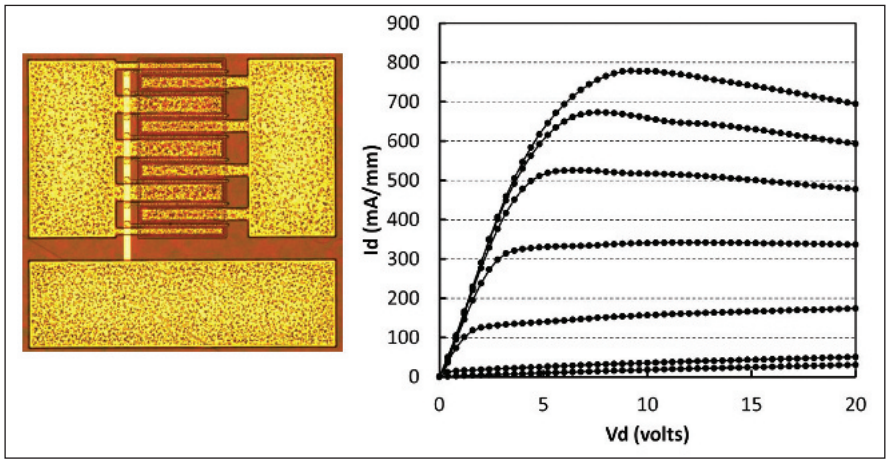

Figure 6. A photomicrograph of a typical device layout is shown for processed GaN-on-REO-on-Si FET that yields the following results: A drain current of 800 mA/mm, a channel mobility of 920 $cm^2 V^{-1}s^{-1}$, a channel sheet carrier concentration of 1.36×10^{13} $/cm^2$ and sheet resistivity = 496 Ω/sq. (Device processing: Rick Brown, www.CayugaMicroDevices.com)

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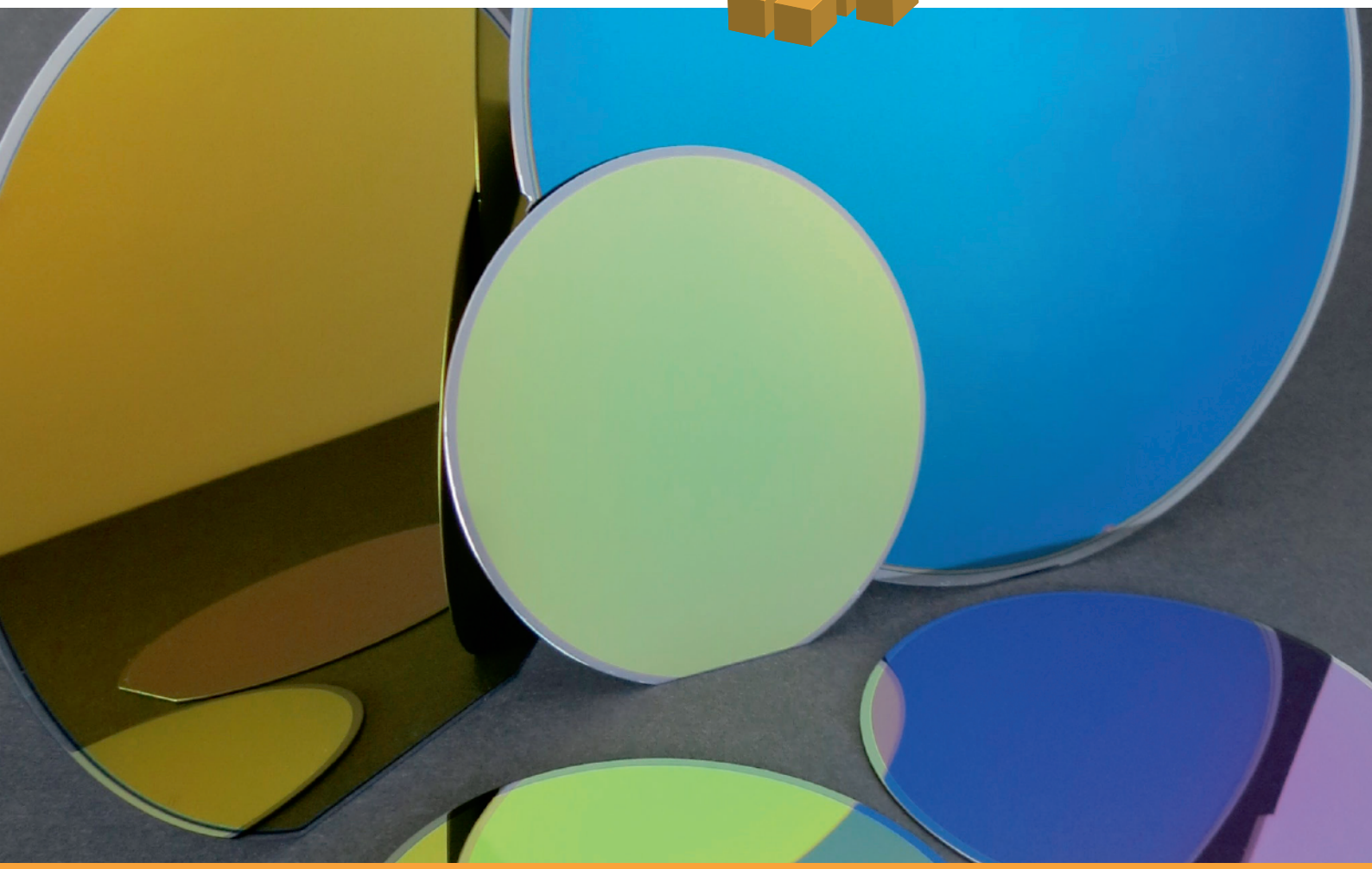

III-N MOCVD HEMT
Rare Earth Oxide (REO)
Silicon

GaN-on-Si Epiwafers

Translucent's revolutionary GaN-on-Si technology employs a patented Rare Earth Oxide (REO) layer that electrically isolates the device layers from the substrate and also provides a physical barrier to stop silicon diffusion.

- Insulating REO buffer isolates GaN from silicon
- REO enables superior high voltage device performance at a competitive price

Germanium
Silicon

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BY DIETER BIMBERG FROM THE TECHNICAL UNIVERSITY OF BERLIN, ANDERS LARSSON FROM CHALMERS UNIVERSITY AND ANDREW JOEL FROM IQE

WHEN YOU HEAR THE PHRASE 'heavy industry' your mind might conjure up images of colossal steel-making plants, vast, busy dockyards, or endless rows of gritty smokestacks belching unpleasant and toxic gases aloft. But in the twenty-first century, you might equally well think of massive environmentally controlled data centres lying just a stone's throw from cold-water lakes or other natural chilled water sources, and surrounded by high-latitude evergreen forests. Due to the tremendous amount of energy these data centres now consume, such places of extreme data storage, transfer, and manipulation are our modern-day factories supporting the world's infrastructure, daily operations, and thirst for information and instant communications.

To aid their running, datacentres are being located alongside power stations. And to trim the electricity bills, more of them are cropping up in regions with access to low-cost natural and renewable power, such as Iceland, a country blessed with a rich source of geothermal energy, and Sweden, a country renowned for both natural beauty and cold water Baltic bays ideal for datacentre cooling and low-cost power sourcing.
Throughout this decade and into the next, datacentres will increase in number to try and satisfy the seemingly insatiable demand for data everywhere, ubiquitous connectivity, and unlimited and seamless human and machine interfaces, all believed at near zero cost. This vision is driven by trends towards cloud computing, big data, and the Internet-of-Things.

To try and prevent the energy that datacentres consume from getting out of hand, there is a need to develop more reliable, higher-speed data-transmission links that consume less energy. The traditional medium for supporting data transfer is a length of copper wire in the form of a 'twisted pair' connector, but this has already been replaced in many datacentres with short-reach, laser-diode-based optical links and interconnects, which combine a higher data capacity with greater bandwidth density, higher transmission efficiency, a more robust operating temperature range, longer reach, and lower costs.

These optical links are being continuously refined, leading to faster and faster aggregated transmission speeds, i.e. increased bandwidths (see Figure 1).

A key ingredient in these optical links is the light source. Previously the most common form of this device for longer distances was an edge-emitting laser diode, which employs cleaved crystal facets as reflectors to form the laser cavity, forcing coherent light to be emitted from the edge of the device.

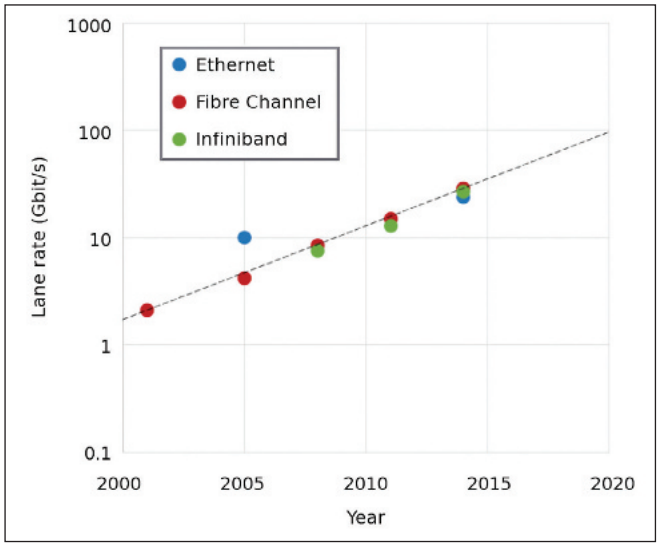


Figure 1. Lane rates are increasing to help to try and meet the insatiable demand for more data, and they could eclipse to 100 Gbit/s by the end of the decade.

One downside of this architecture is that it must involve the fabrication of discrete devices, with manufacturing and testing only performed on fully processed edge-emitting devices. An additional weakness is that the output from these devices shows an elliptical beam profile, which is tricky and expensive to collimate and to focus into the end of an optical fibre.

Due to these limitations, the vertical-cavity-surface-emitting laser (VCSEL) is a far more attractive class of laser diode for deployment in short-reach optical interconnects for datacentres, server farms, and supercomputers. This class of laser contains an active layer confined by two distributed Bragg reflectors (DBRs), which are formed via the growth of multiple thin epitaxial layers on a semiconductor substrate. With this device geometry, light exits the chip through either the upper or lower DBR reflector, thus in a direction that is vertical (perpendicular) to the surface of the VCSEL (see Figure 2 for top-emitting VCSEL). Thanks to surface emission, the VCSEL can be tested on wafer, which delivers an enormous cut in manufacturing cost and lends itself to the fabrication of laser arrays comprising multiple emitters on a single chip. By using direct butt-coupling, adding a lens to the emitting surface of the VCSEL, or by using a fibre with a built-in lens tip, it is possible to couple the emitted light into a standard multiple-mode optical fibre. In high optical output power or illumination applications, arrays of VCSELs may be used in concert with a microlens array to collimate the emitted light.

The speeds (data bit rates) of commercially available optical fibre links are held back by the light source, and presently show maximum bit rates of between 10 Gbit/s and 28 Gbit/s. The maximum operating bit rate of a VCSEL depends on several intrinsic device parameters including the damping of the modulation response, thermal effects, and aspects of device design that determine parasitic resistance and capacitance.

Turbo-charging the VCSEL

To spur the VCSEL to higher speeds, our team of researchers at the Technical University of Berlin (TU Berlin), Germany, at Chalmers University of Technology, Sweden, and at the UK-based epitaxial-wafer manufacturer IQE plc, has developed new device architectures that can increase data transmission speeds. This work first evolved as part of a European Commission-funded programme called VISIT – Vertically Integrated Systems for Information Transfer, during the years 2008-2011 .

We have made essential refinements to the VCSEL design (Figure 3), including replacement of the GaAs-based active layer with a strained InGaAs/AlGaAs quantum well structure to provide higher differential gain, and the introduction of separate confinement heterostructures to speed up the transport of carriers and ensure low gain compression. In addition, we trimmed the cavity length to boost optical confinement; cut the number of mirror pairs in the top distributed Bragg reflector, in order to cut reflectivity and ultimately shorten the photon lifetime; and introduced more advanced interface grading and modulation doping schemes in the DBR mirrors,

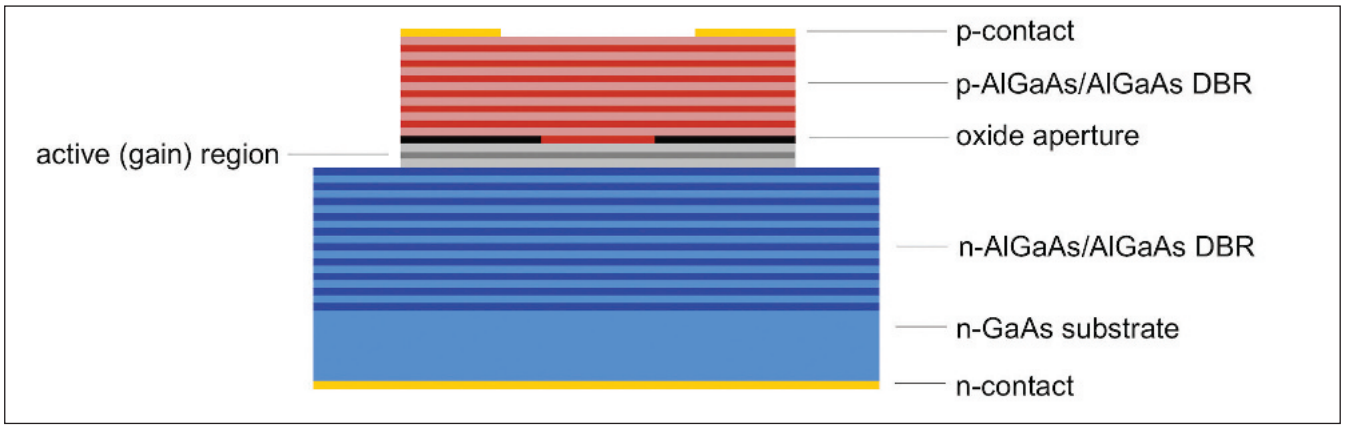


Figure 2. A typical GaAs-based VCSEL structure features an active region sandwiched between two multilayer mirrors (DBRs). Carriers are injected through the contacts on the top and bottom of the structure, with light emitting through the top. The beam profile is governed by the width of the oxide aperture.

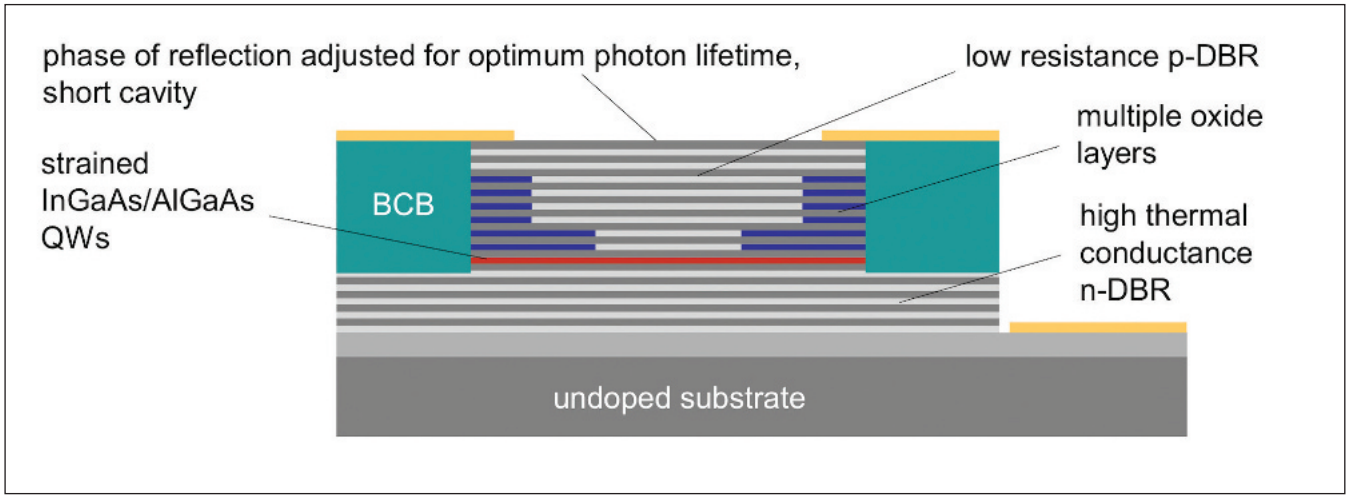


Figure 3. Refinements of the VCSEL design have propelled speeds to 50 Gbit/s and beyond.

to lower resistance and optical losses. Completing this list of enhancements was the inclusion of multiple oxide layers, the introduction of an undoped substrate to lower capacitance, and the use of an AlAs binary compound in the bottom mirror to reduce the thermal impedance.

These changes to the VCSEL structures have impacted the epitaxial deposition process. Growth of the new device structures demands exceptionally tight control over compositional uniformity, maintenance of strain, and highly accurate placement of layers for forming an oxide aperture for current and optical confinement.

Changes to the VCSEL designs have wrought improvements in performance. For VCSELs emitting at 850 nm the modifications to the active region and the cavity have delivered a doubling of differential gain, a 30 percent cut in threshold carrier density, and a 20 percent increase in the optical confinement factor. Carrier transport has also improved, while the diffusion capacitance has decreased, as demonstrated by Chalmers.

A better DBR has resulted from the new design. Differential resistance has fallen by 25 percent in the top mirror, while free carrier absorption has showed little, if any, increase. Meanwhile, in the bottom mirror the switch to the pairing of AlAs and $Al_{0.12}Ga_{0.88}As$ has delivered a 40 percent hike in thermal conductivity. Parasitic capacitance has decreased between 30 and 40 percent via the addition of extra oxide layers.

Due to all of these changes, VCSEL speeds have been catapulted to beyond 50 Gbit/s (see Figure 4; from Electronics Letters, August 2013) and to such an extent that the optical interconnect speed is largely limited by the speed of the drive electronics and the optical receiver. Recent work at IBM (Yorktown Heights, NY), using Chalmer's 850 nm VCSELs and drive and receiver electronics developed at IBM, has enabled optical interconnects operating at a channel rate of 64 Gbit/s (Optical Fiber Communication Conference, 2014, paper Th3C.2), which is a world record for VCSEL-based interconnects. IBM has also demonstrated transmission at 51.56 Gbit/s (the InfiniBand HDR data rate) with the VCSEL-based transmitter held at a high temperature of 90°C.

Measurements of bit-error-rate and eye diagrams for 850 nm VCSEL-based optical interconnects at bit rates from 50 Gbit/s to 57 Gbit/s are shown in Fig. 5. The bit-error-ratio is a measure of the probability that a data bit is erroneously detected, with 10^{-12} typically considered 'error-free' for short-reach optical fibre interconnects. An eye diagram is constructed by overlaying sweeps of different segments of the digital data stream, thus creating an 'eye' displaying the on and off-levels and the transitions between these.

Boosting efficiency

Fast speeds are highly commendable, but they are not the only metric that matters: the energy dissipation per bit is probably still more critical, for it is this that has the larger influence on the power drawn by the datacentres. This is exactly the focus

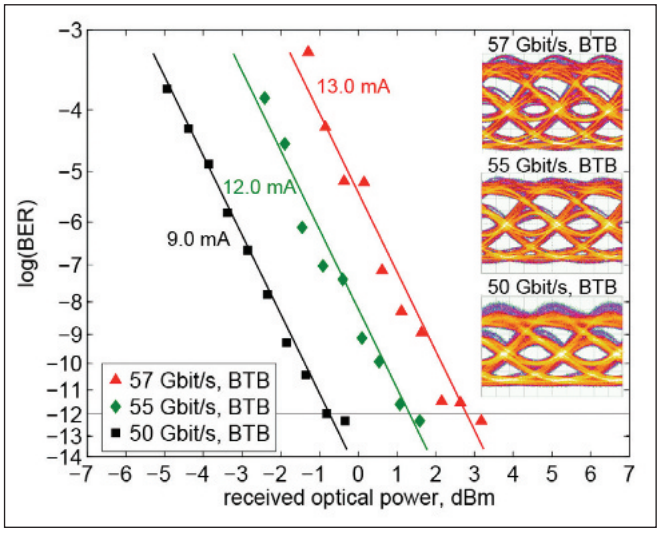


Figure 4. Data transmission over a VCSEL-based optical interconnect at 50, 55 and 57 Gbit/s.

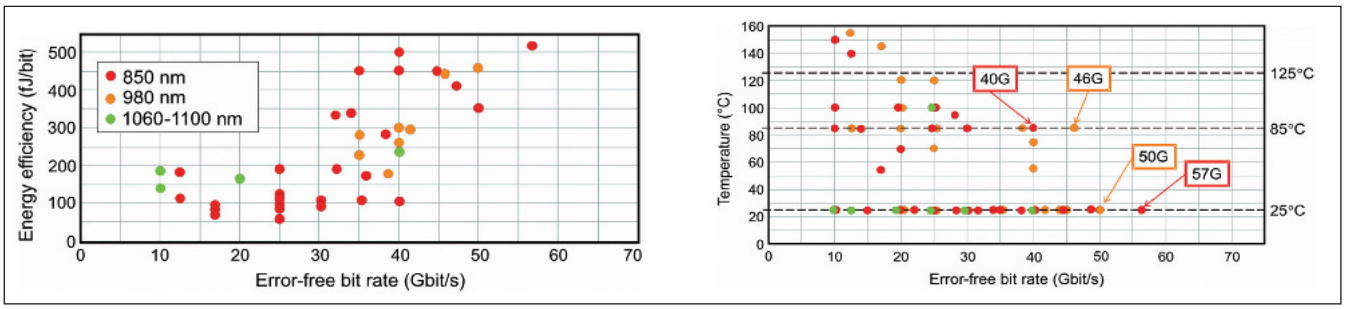


Figure 5. Energy efficiency (a) in units of femtojoules per bit and temperature (b) both versus error-free bit rate of state-of-the-art infrared VCSELs.

of the work at TU Berlin, wherein the VCSELs have broken every conceivable VCSEL energy efficiency record during the past several years at both 850 nm and at 980 nm (see Figure 5). By making independently similar changes to the epitaxial structure, including those previously listed, and by adding additional current spreading layers and proprietary changes to the quantum wells and distributed Bragg reflector (DBR) mirrors to increase the differential gain and the heat dissipation, the energy dissipation was decisively lowered in 2013 beyond the level requested by the ITRS road map for 2015.

We have strived to excel in this area, and earlier this year during the Photonics West 2014 conference (held during 1-6 February 2014, in San Francisco, CA) TU Berlin announced in partnership with IQE plc that error-free operation at speeds of up to 40 Gbit/s had been accomplished, with a record low energy dissipation (below 108 fJ/bit). This dissipated energy per bit at 40 Gbit/s is at least four times less than any other published result for VCSELs. For this work TU Berlin received the SPIE 2014 Green Photonics Award in Communications, after having previously already received this award in 2012.

In more recent work the 980 nm VCSELs that enabled this record also demonstrated extreme temperature stability during high-speed operation at 46 Gbit/s and temperatures of up to 85°C. These superb results were presented by the TU Berlin group at the IEEE ISLC in Palma de Mallorca, Spain during 6-11 September 2014.

The energy dissipation per bit is not fixed for a VCSEL, but depends on the transmission speed, the operating conditions, the intrinsic VCSEL materials and thus on the epitaxial design, and the other components along with the VCSELs that form a complete optical interconnect, such as the VCSEL driver electronics, the photoreceiver, and the modulation scheme. As demonstrated in 2013 when providing error-free operation at 25 Gbit/s, TU Berlin VCSELs have demonstrated that they can deliver a record-low dissipated energy of 56 fJ/bit. This remains to date the lowest reported value of dissipated energy at error-free operation for any semiconductor laser diode at any wavelength or bit rate, and it was achieved at a current density of just ~10 kA cm^{-2}. This result demonstrates the suitability of these devices for application in reliable, sustainable commercial 'green' optical interconnects.

Emerging new markets

Development of epitaxial processes to produce these highly complex structures, alongside refinements to the VCSEL architecture, will not just led to faster and more efficient lasers for datacentres – it will also help to drive the deployment of this class of laser in a wide range of new and emerging industrial, commercial, and consumer applications. Penetration into these new markets will be aided by establishing a European production capability that brings VCSEL manufacturing to a level comparable to LED and CMOS manufacturing. Such efforts are underway, with IQE plc taking part in a €€ 23 million programme announced this May, entitled VCSEL Pilot Line for IR Illumination, Datacom, and Power Applications (VIDaP).

Partners in this European project, which is funded by the European Commission, include Philips, STMicroelectronics, Sick and Sidel. Together, these firms will bring together existing high-volume production facilities at IQE with key end users to create a consortium delivering an end-to-end production supply chain. This should significantly reduce the cost-per-function for the VCSEL, by reducing GaAs processing costs whilst increasing device performance.

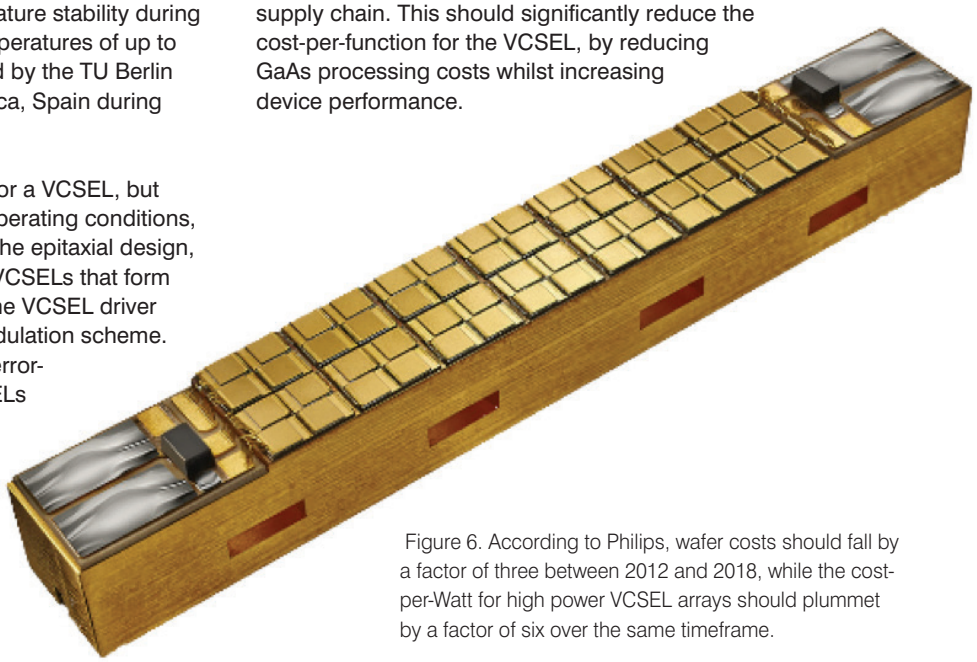
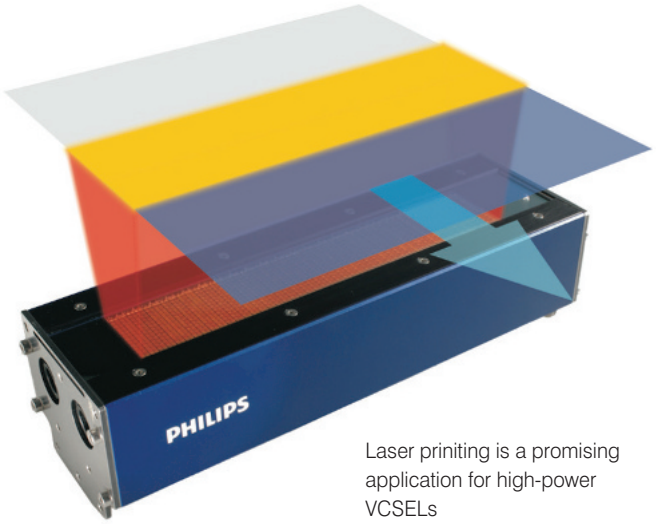


Figure 6. According to Philips, wafer costs should fall by a factor of three between 2012 and 2018, while the cost-per-Watt for high power VCSEL arrays should plummet by a factor of six over the same timeframe.

One emerging application that could swell VCSEL sales is gesture recognition – this could be used for gaming and non-contact navigation. This class of laser could also be used in depth imaging for 3D vision, using 'time-of-flight' technology. In addition to these consumer applications, VCSEL deployment is set to rise in industry as chip volumes increase and devices offer greater performance at lower cost (see Figure 6). This surface-emitting laser may be used for highly efficient, digital thermal processing. Examples of this are high efficiency production-line heating, paint curing and ink finishing in commercial printing.

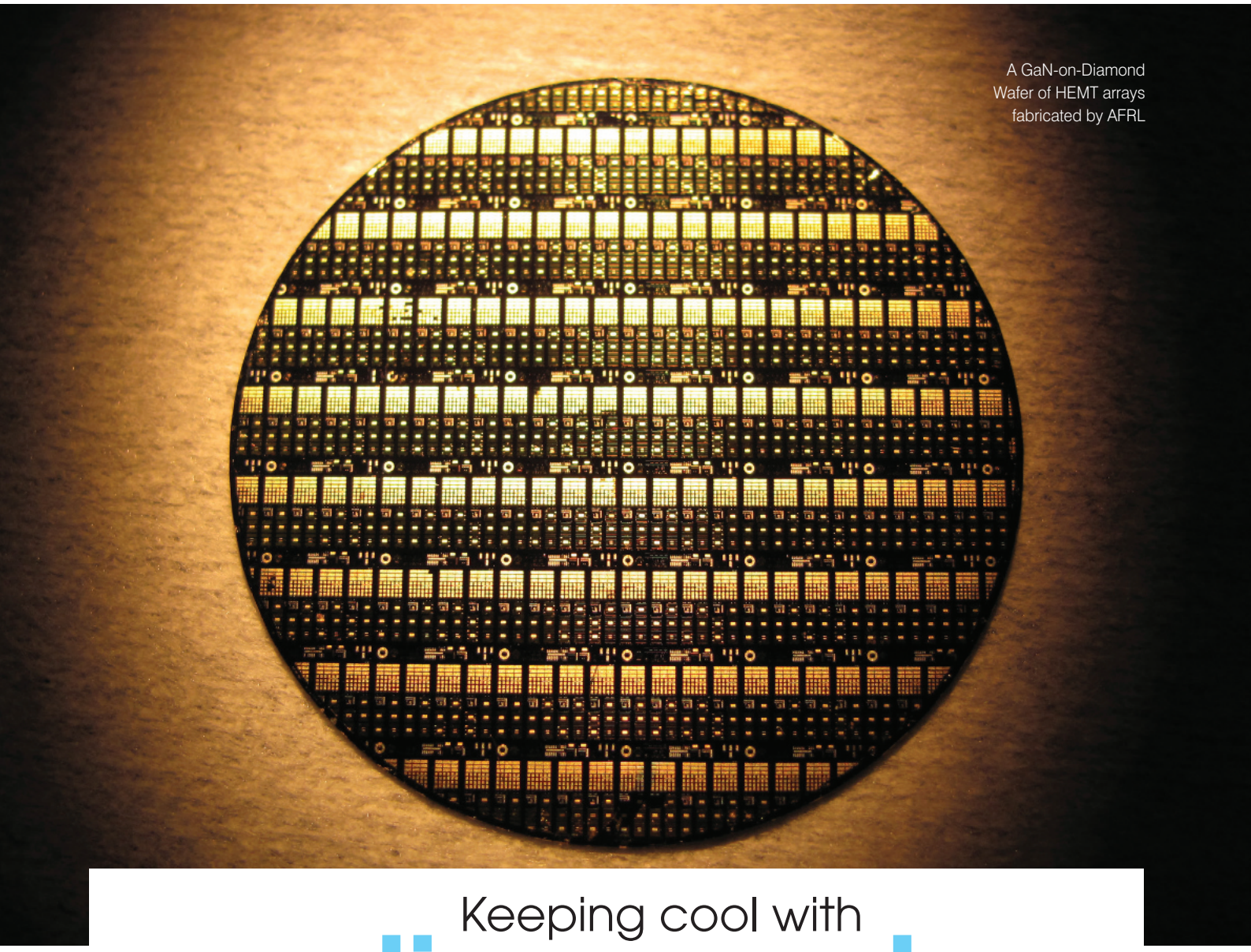
On top of this, it is possible for VCSELs to find deployment in illumination for IR cameras for security, safety and night vision; ultra-high density magnetic storage using heat-assisted magnetic recording, and cosmetics and healthcare devices. There are clearly many opportunities for the VCSEL, and shipments will rise as deployments increase in data centres, and then extend to other applications. Initially, it will be the speed and efficiency of this class of laser that will drive its uptake, but there will then come a time when it is power density at low cost that is responsible for the mass adoption of the VCSEL across multiple end markets.

Advances in the manufacturing process will have to underpin this growth of VCSEL volumes. The groundwork is already being laid, as production moves to larger wafers, using processes that are similar to those employed in the LED and silicon CMOS industries. It is only a matter of time, therefore, before the VCSEL becomes a mainstream product serving myriad applications.



Laser priniting is a promising application for high-power VCSELs

The authors wish to express their gratitude to James Lott from the Technical University of Berlin for his contribution to the work and this article.



A GaN-on-Diamond Wafer of HEMT arrays fabricated by AFRL

Keeping cool with diamond

By sucking heat from GaN HEMTs better than other substrates, diamond enables transistors to operate at higher ambient temperatures and have reduced finger spacing

BY FELIX EJECKAM FROM ELEMENT SIX TECHNOLOGIES

THANKS TO A TREMENDOUS SET OF INTRINSIC CHARACTERISTICS, GaN-based RF transistors are setting a new benchmark for solid-state device performance. But that does not mean that they are fulfilling their true potential, because the heating in channel degrades device lifetime when the RF chip operates near its peak power output.

To address this weakness, our team (initially Group4 Labs, acquired by Element Six in 2013) began in 2003 to develop a higher thermal conductivity substrate that more effectively extracts heat out of a transistor based device: directly deposited CVD diamond.

This development will allow GaN-on-diamond devices to replace the more common GaN-on-SiC devices and traveling wave tubes in defence radar and electronic warfare systems. What's more, commercial systems such as cellular base stations, weather and communications satellites and power devices may be able to deliver greater energy efficiency, while being lighter and

PHYSICAL PROPERTIES OF VARIOUS BULK MATERIALS

	Si	GaAa	SiC	GaN	SAPPHIRE	CVD DIAMOND
THERMAL CONDUCTIVITY (@300K) (W/m-K)	135-150	35-50	390-450	150-250	35	1000, 1500, 2000
ELECTRICAL RESISTIVITY @ 300K (Ω-cm)	~ $2.3x10^5$	~ 10^4 - 10^8	~ 10^4-10^6	~ 10^6	~ 10^{17}	~ 10^{13}-10^{16}
YOUNG'S MODULUS (110) @ RT (GPa)	130	~ 83	~ 390-700	~ 180-200	~ 250-400	~ 1,100
DIAMETER AVAILABILITY TODAY	12"	6"	6"	1.2"	2"-4"	6"

Table 1. Electrical and thermal properties of various commercially available substrates commonly used in RF electronics or that may be used to host GaN.

smaller, due to the introduction of directly deposited diamond substrates.

One reason that the authors advocate a move to diamond is because it is the best commercial heat-spreading material in the world. It can have a room temperature thermal conductivity of more than 1500 W m^{-1} K^{-1}, and can be four-to-five times that of the next best semiconductor substrate, SiC (see table 1 for details of key physical properties of various compound semiconductors). Diamond can be deposited to within hundreds of nanometres of the GaN channel, where it can efficiently extract heat out of the transistor-based device.

Simulations, modelling, and experiments all illustrate the promise of GaN-on-diamond. Researchers from various groups, including those assembled by the Defense Advanced Research Projects Agency (DARPA), have determined that such transistor-based devices can operate at reduced channel temperatures and are capable of delivering about three times the areal power density of state-of-the-art GaN-on-SiC RF power amplifiers.

Diamond development

The first thought of turning to diamond substrates is now more than a decade old, since which there have been several key breakthroughs. They include showing that high-quality diamond substrates can be deposited on 3-inch and 4-inch GaN wafers; demonstrating that it is possible to construct RF power amplifiers incorporating our diamond technology and undertaking numerous mechanical/materials, electrical, thermal, and reliability measurements that clearly indicate the superiority of GaN-on-diamond over GaN-on-SiC in RF electronics. Unusual for a new semiconductor technology, the authors' wafer formation process has undergone very few changes during its development (see Figure 1 for a pictorial overview of the progress). However, during that time there has been an exhaustive refinement with optimization of virtually every aspect of GaN-on-diamond wafer technology. These efforts include introducing larger wafers, improving coverage yield of GaN-on-diamond, optimising the thickness of interfacial material between the GaN and diamond, reducing the wafer bow and warp and refining methods for depositing/removing protection layers on top of the GaN epitaxy.

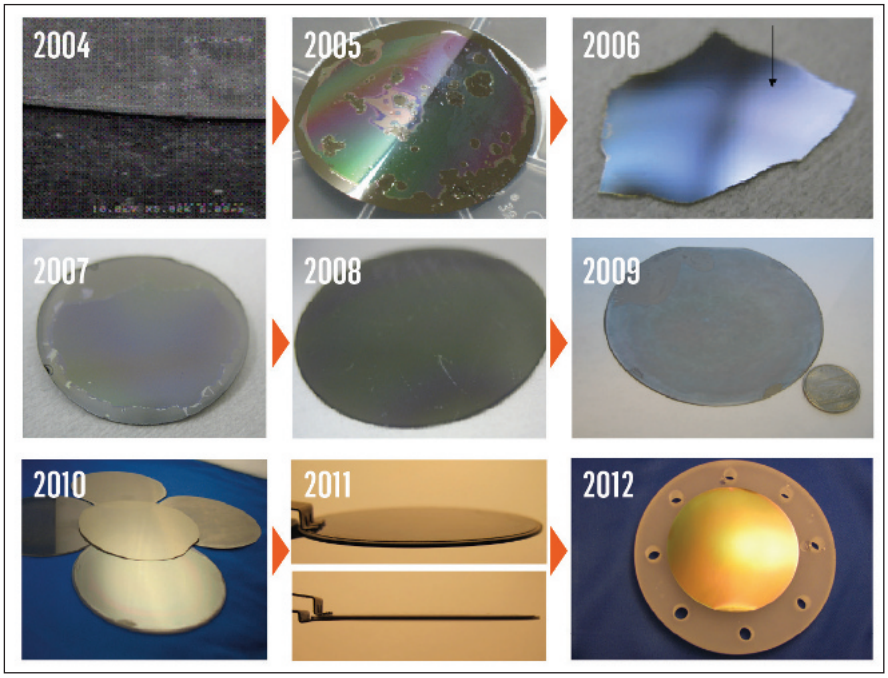


Figure 1. Development of GaN-on-diamond wafers includes the first carrier mounted 3-inch GaN-on-diamond wafer in 2011 and the first 4-inch free-standing GaN-on-diamond wafer in 2012.

GaN-on-diamond wafers (see Figure 2) are formed by first depositing the AlGaN/GaN HEMT structure by MOCVD on high resistivity silicon. The epitaxial stack includes a 1.2 μm-thick proprietary transition layer, an 800 nm-thick undoped GaN buffer layer, a 17 nm-thick $Al_{0.26}Ga_{0.74}N$ Schottky barrier and a 2 nm-thick GaN cap layer.

This epitaxial structure – GaN buffer, AlGaN barrier and GaN cap – is coated on the bottom of the GaN buffer with a dielectric and then a 100 μm-thick CVD diamond layer. This pair of additional layers is added by first removing the host silicon (111) substrate and transition layers beneath the AlGaN/GaN epitaxy, before depositing a 35 nm-thick proprietary dielectric onto the exposed AlGaN/GaN, and finally growing a 100 μm-thick CVD diamond substrate onto the dielectric adhering to the epitaxial AlGaN/GaN films.

The real test for GaN-on-diamond is whether it delivers improvement to transistor performance. This is the focus of the remainder of this article, which details two studies: The first is of a comparison of GaN-on-diamond and GaN-on-silicon HEMTs – note

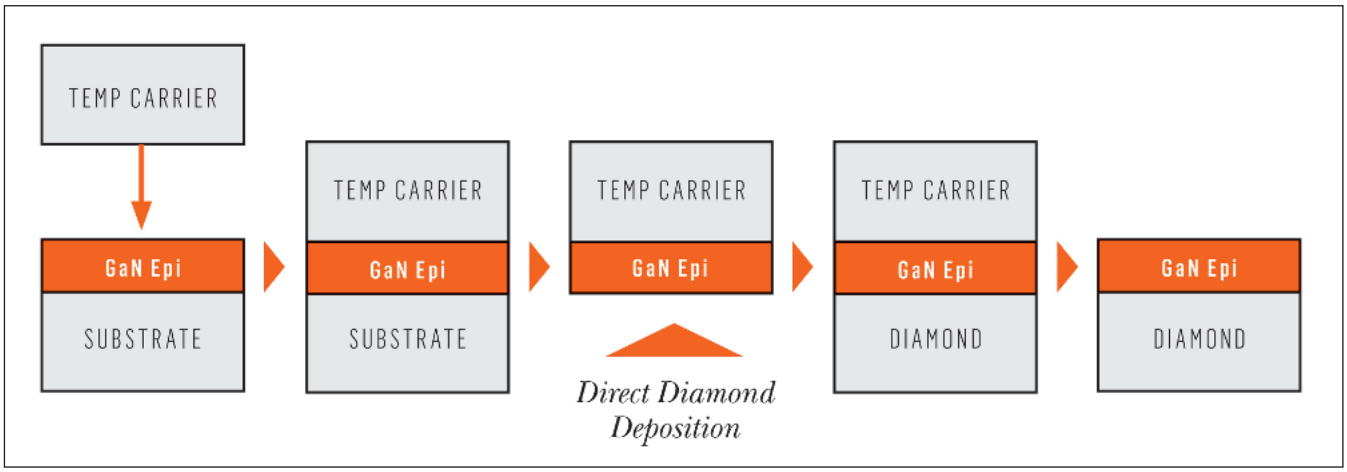


Figure 2. GaN-on-diamond structures are formed by: bonding the GaN face to a temporary carrier; etching away the substrate and transition layers; depositing a 35 nm-thick dielectric and then a diamond layer on the backside of GaN; and removing the temporary carrier.

that the GaN-on-diamond originally comes from a silicon substrate; and the second compares device performance to the GaN-on-SiC HEMT, which is the industry's prevailing GaN technology.

Recently, engineers at the US Air Force Research Laboratory (AFRL) have independently investigated whether the team's GaN epi-flip and diamond deposition process is detrimental to GaN epitaxy, and whether it can lead to any deterioration in device performance. Their examination involved the analysis of thousands of GaN-on-diamond and GaN-on-silicon HEMTs. To make the comparison as fair as possible, the GaN-on-silicon was grown at the same time as the GaN that was to be transferred to diamond. Dimensions of the HEMTs (identical on both silicon and diamond substrates) included a gate width of 300 mm (2 x 150 mm), a gate length of 0.15 mm and source-drain distance of 4.5 mm.

Epiwafers, plus devices formed from them, were scrutinised with a wide range of measurements. Entire wafers were mapped for sheet resistivity, carrier mobility, carrier density, contact resistance, sheet resistance and buffer isolation current, while measurements on passivated devices assessed values for transconductance, maximum DC drain current, saturated DC drain-source current, threshold voltage, gate leakage and knee voltage. On top of this, engineers obtained passivated RF data for the devices, including values for breakdown voltage, f_{max} (MAG), f_t, current-voltage and transfer curves. Aside from one exception – surface gate leakage – no statistically significant differences were uncovered between DC and RF measurements for GaN-on-silicon and GaN-on-diamond (see table 2 for a summary of the results).

RF performance of both types of device was then assessed with continuous-wave Maury load pull measurements at X-band (10 GHz) frequencies and various drain voltages. Select devices were matched for best power-added efficiency and biased at a quiescent drain current of 30 mA, corresponding to 100 mA/mm, in a class AB configuration. Measurements on wafers held at 25 °C on a vacuum chuck using drain voltages between 15 V and 25 V revealed that switching the foundation from silicon to diamond boosted output power by typically 1-1.5dBm and increased power-added efficiency by 7 percentage points (see Figure 3).

Engineers at AFRL also compared the current droop in both types of HEMTs. This study revealed that GaN-on-silicon HEMTs are more sensitive to pulse lengths than GaN-on-diamond HEMTs (see Figure 4), due to increased self-heating.

A combination of infrared thermography and micro-Raman techniques unveiled the thermal performance of the GaN-on-diamond and GaN-on-silicon HEMTs. Due to a 'spot-size' larger than that of the entire transistor, infrared measurements were only qualitative. These measurements made on-wafer, un-attached to a stage, involved devices operating at a drain-voltage of 25 V and drain current of 130 mA. Values for thermal resistance – the difference between the observed region's hottest temperature and that at the base of the substrate, divided by the product of the drain voltage and current – were just 7.44 K W^{-1} mm^{-1} for GaN-on-diamond HEMTs, compared with 16.6 K W^{-1} mm^{-1} and 11.5 K W^{-1} mm^{-1} for those with silicon

	GaN-ON-DIAMOND	GaN-ON-SILICON
Rc (Ω-mm)	0.36 (0.11)	0.49 (0.09)
Rsh (Ω/sq)	441 (39.4)	429 (17.8)
IISO@50V (uA)	89 (103)	226 (186)
GmPeak (mS/mm)	238 (18.6)	214 (5.3)
Vth (V)	-3.58 (0.04)	-3.81 (0.05)
Imax (mA/mm)	813 (56.3)	697 (39.6)
Idss (mA/mm)	707 (58.6)	617 (57.3)
Igl (uA/mm)	-5.66 (5.49)	-0.56 (0.84)
Vbk (V)	25.75 (10.64)	27.94 (5.02)
GLag@5V (%)	7.9 (NA)	7.1 (NA)
Dlag@5V (%)	10.0 (NA)	10.6 (NA)

Table 2. A summary of average (and standard deviation) DC and RF measurements made by AFRL on identically designed GaN-on-diamond and GaN-on-silicon HEMTs.

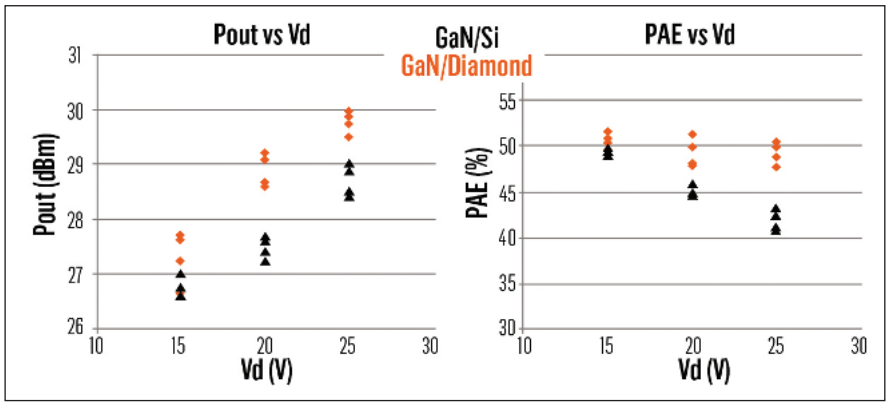


Figure 3. X-band load-pull measurements taken from GaN-on-diamond and GaN-on-silicon HEMTs across multiple levels of power dissipation.

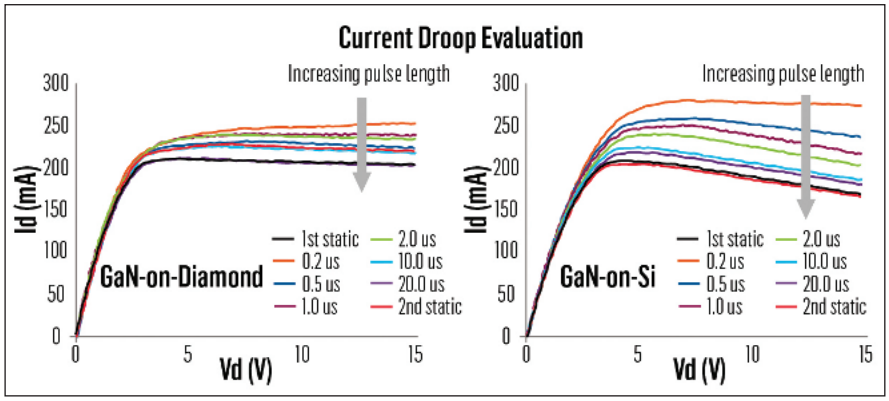


Figure 4. Current droop measured from GaN-on-diamond (left chart) and GaN-on-silicon HEMTs (right chart) across various duty-cycles.

devices, with a gate-to-gate spacing of 10 mm and 40 mm for GaN-on-diamond and 30 mm and 40 mm for GaN-on-SiC (see Figure 7). Gate temperatures were measured in all these devices, which had a common packaging configuration and operated at multiple power dissipation levels.

Simulations suggest that for a similar peak channel temperature, GaN-on-diamond HEMTs can employ one-third of the gate-to-gate spacing of GaN-on-SiC equivalents, thanks to a 40 percent reduction in channel-to-substrate thermal resistance.

To verify this, engineers probed thermal characteristics with micro-Raman thermography and gate thermometry (see Figure 8). Both of these techniques are not capable of measuring the true peak temperature that occurs in the HEMT, so peak temperatures are simulated – these represent the hottest nodal temperature in the HEMT finite element model. Confidence in the peak-temperature calculations derives from a good agreement between the model, the gate thermometry and the micro-Raman measurements. HEMT temperatures determined via measurement of gate forward bias voltage, which is calibrated

and SiC foundations, respectively. Quantitative measurements of thermal resistance are possible with micro-Raman thermal analysis, which has a spot volume of about 1 mm^3 from the GaN surface into the buffer.

Temperatures measured between the gate and drain (nearer the former) as well as near the edge of the diamond substrate, led to values for thermal resistance of about 8.0 K W^{-1} mm^{-1} for the GaN-on-diamond HEMT (see Figure 6). In comparison, GaN-on-silicon equivalents exhibited thermal resistance of about 21 K W^{-1} mm^{-1}.

Comparisons with SiC

For high-power GaN RF applications, the industry's leading substrate is SiC. So, it is the performance of HEMTs built on this platform that set the benchmark against which GaN-on diamond devices should be judged. Engineers at Raytheon have compared these two classes of device, using 10 x 125 mm HEMTs formed with the company's microwave GaN process. This study involved forming a portfolio of

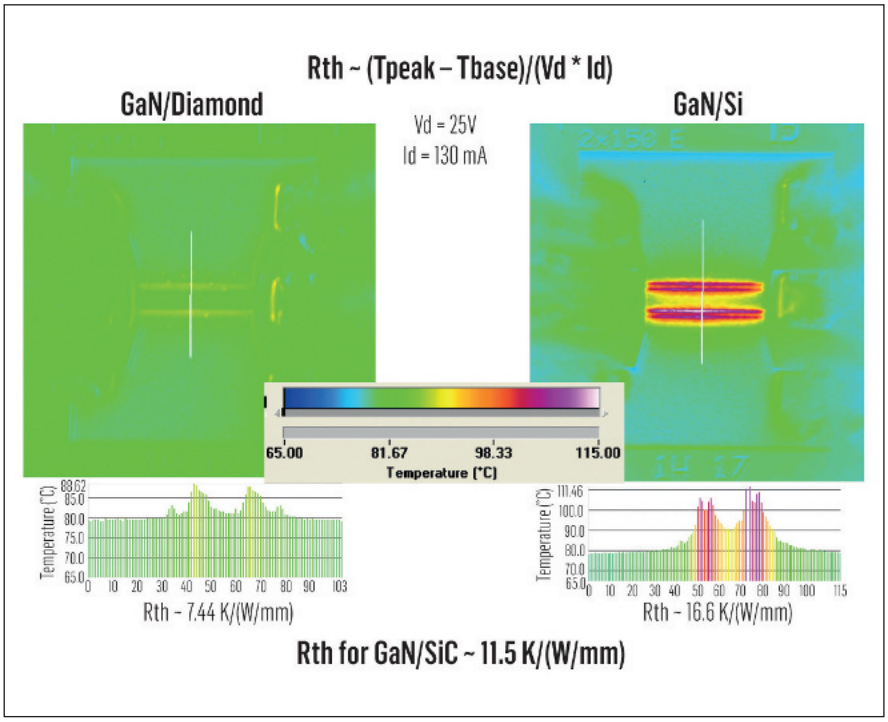


Figure 5. An infrared image of GaN-on-diamond and GaN-on-silicon HEMTs under bias. The temperature difference between the device's gate and the base of the substrate was used in the calculations.

to temperature, are in good agreement with simulations. They show that at a dissipated power of 4.2 W/mm, the peak junction temperature of the 10 mm gate-to-gate GaN-on-diamond HEMT is just 6.3 °C (6 percent) higher than the 30 mm gate-to-gate GaN-on-SiC device. And for 40 mm gate-to-gate spacings at 4.2 W/mm dissipated power, the GaN-on-diamond device has a junction temperature 8.5°C lower than the GaN-on-SiC equivalent. These efforts also reveal that switching from SiC to diamond delivers a spike in areal dissipation density from 140 W/mm^2 to 420 W/mm^2.

These results are for an early generation of GaN-on-diamond structures. Measurements on more recent material show that thermal performance has improved, which should result in even more impressive devices.

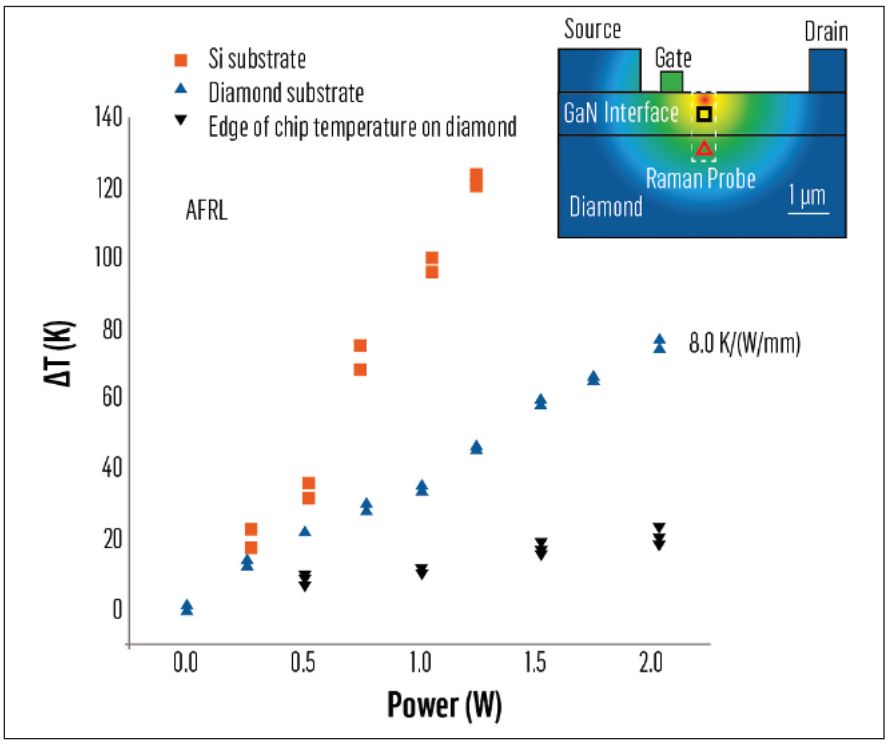


Figure 6. Temperature change measured for GaN-on-diamond and GaN-on-silicon HEMTs using a micro-Raman technique.

Is GaN-on-diamond reliable?

The introduction of any new substrate will always bring concerns over reliability. With diamond, scepticism can stem from its significant differences, compared to GaN, in its thermal expansion coefficient, crystal structure, surface properties and internal stress. To put these concerns to bed, the authors have subjected GaN-on-diamond HEMTs to channel temperatures of up to 350°C using a constant source-drain voltage of 24 V.

A series of endurance tests involved monitoring the source-drain currents and gate leakage currents of batches of devices operated for thousands of hours at elevated channel temperatures. Currents for the GaN-on-diamond HEMTs deviated by less than 25 percent of their starting values after: 4,000 hours at 350°C, 9,000 hours at 290°C and 17,000 hours at 210°C. In contrast, all the control GaN-on-silicon devices, which share the same GaN epitaxy and device structure as their GaN-on-diamond cousins, catastrophically failed within a few hundred hours of the start of the tests.

Apparently, removal of the highly defective transition layers between GaN and silicon, prior to diamond deposition, contributed to the improvements resulting from the introduction of GaN-on-diamond. However, to confirm that this is the case, more research is warranted to better understand these results. Trimming the thermal resistance by 40 percent by switching from GaN-on-SiC to GaN-on-diamond should have two major benefits on the design of radar, electronic warfare, defence radio, communications and weather satellites, cellular base stations, and naval avionics systems: it should cut cooling complexity and cost, and it should deliver a three-fold increase in the areal power density of the GaN transistor.

Reductions in cooling complexity and cost are possible when thermal resistance falls, because less stringent demands are placed on the coolant temperature. This can open the door to simpler, cheaper thermal management

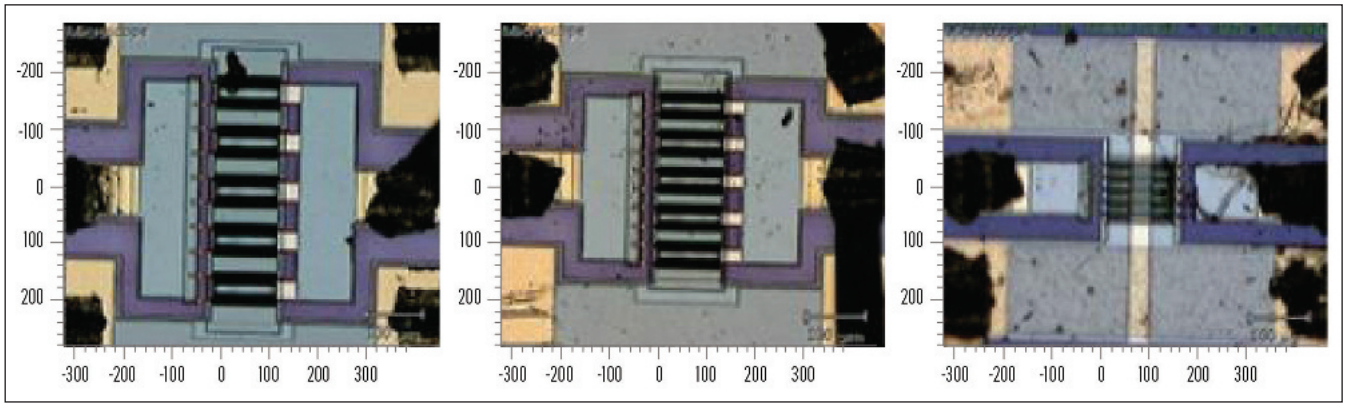


Figure 7. GaN HEMTs characterized by micro-Raman and gate thermometry techniques. From left: GaN-on-SiC 40 micron gate-to-gate spacing, GaN-on-SiC 30 micron gate-to-gate spacing, and GaN-on-diamond 10 micron gate-to-gate spacing.

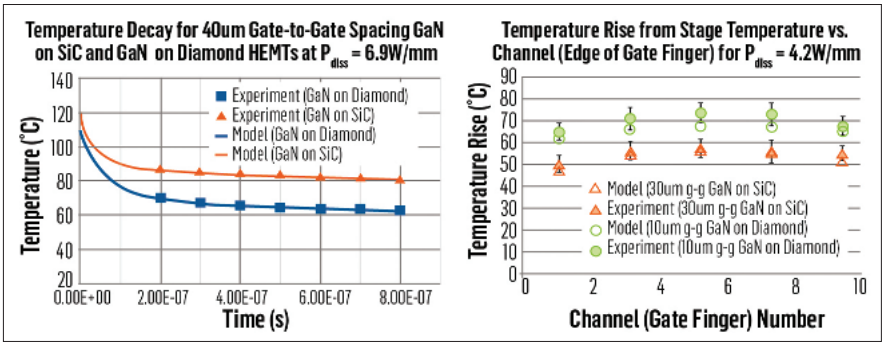


Figure 8. A comparison of simulations and experimental values for the temperatures for GaN-on-SiC and GaN-on-diamond HEMTs. Experiments involved gate thermometry (left) and micro-Raman (right) techniques. On the left, GaN-on-diamond and GaN-on-SiC HEMTs are compared with equivalent gate-to-gate spacing and dissipation (6.9 W/mm). On the right, the GaN-on-diamond HEMT has a threefold reduction in gate-to-gate spacing relative to the GaN-on-SiC HEMT.

systems; and it can also enable higher coolant (or device operating) temperatures, because the temperature rise from the coolant to the gate is lower. The higher areal power densities that are possible with the reduced thermal resistance of GaN-on-diamond derive from a shrinking of gate finger separation by a factor of three, leading to smaller, cheaper GaN-on-diamond devices.

For the manufacturers of power amplifier chips, processing three times fewer GaN-on-diamond wafers than GaN-on-SiC variants, while maintaining the same total RF output power, leads to significant reductions in fab costs – assuming that commercial GaN-on-diamond wafers are competitively priced to GaN-on-SiC wafers. And if the GaN-on-diamond wafer price is low enough, then vendors' power amplifier savings can be passed on to the system maker, reducing the power amplifier price per watt.

This is an attractive scenario, showcasing the opportunity for GaN-on-diamond technology to deliver revolutionary advantages for system performance and cost, which can make it the ideal choice for next-generation HEMTs.

Many people have contributed to the work described in this article: Daniel Francis, Firooz Faili, Frank Lowe, Tim Mollart, Joe Dodson, Daniel Twitchen and Bruce Bolliger from Element Six Technologies; Dubravko Babic from the University of Zagreb; Quentin Diduck from Avogy; Chandra Khandavalli from iMata Technologies; Matthew Tyhach, David Altman and Steve Bernstein from Raytheon Company and Samuel Graham from Georgia Institute of Technology.

The views expressed are those of the author and do not reflect the official policy or position of the Department of Defense or the US Government.

Contributions to GaN-on-diamond development

Key milestones in GaN-on-dimaond development:

- In 2005, DARPA's award to Group4 Labs, Inc. of the first seed contract to demonstrate a 10 mm x 10 mm piece of GaN-on-diamond wafer. DARPA would provide instrumental funding later on – via the Near Junction Thermal Transport effort under DARPA's Thermal Management programme to characterize the thermal benefits of the new technology. P1 Diamond and Crystallume Corporation grew the first wafers for the team in 2004 and 2005, respectively.
- In 2006, the first-ever operational transistor on a GaN-on-diamond wafer. The transistors were made by Wright Patterson Air Force Research Labs.
- The US Missile Defense Agency awarding the first of many SBIR programs. TriQuint Semiconductor and Raytheon Company were the first commercial entities to demonstrate operational GaN-on-diamond transistors. The US Navy SBIR program was the first to fund a reliability-related programme with the team in 2009.
- In 2009, Element Six SA – the largest synthetic diamond maker in the world – becoming an instrumental backer of GaN-on-diamond. Element Six subsequently enabled scale-up of the technology after acquiring Group4 Labs in 2013.

Reference

M. Tyhach *et. al.* "Analysis and Characterization of Thermal Transport in GaN HEMTs on SiC and Diamond Substrates", accepted to GOMACT 2014.

D.C. Dumka *et. al.* "Electrical and Thermal Performance of AlGaN/GaN HEMTs on Diamond Substrate for RF Applications" in 35th IEEE Compound Semiconductor IC Symposium (CSIC) Oct 13-16 2013, Monterey, CA, Section F.4.

G.D. Via *et. al.* "Wafer-Scale GaN HEMT Performance Enhancement by Diamond Substrate Integration" in 10th International Conference on Nitride Semiconductors, ICNS-10, August 25-30, 2013, Washington DC, USA.

F. Ejeckam *et. al.* "3,000+ Hours Continuous Operation of GaN-on-Diamond HEMTs at 350C Channel Temperature", Accepted for publication to Semi Therm Conference Mar 9-13, 2014, San Jose, CA.

F. Ejeckam *et. al.* "GaN-on-Diamond Wafers: A Progress Report", Accepted for publication at GOMACTech-14, as Paper No. 23.14, April 3, 2014, Charleston, SC.

J. Pomeroy *et. al.* "Achieving the Best Thermal Performance for GaN-on-Diamond" in 35th IEEE Compound Semiconductor IC Symposium (CSICS) Oct 13-16 2013, Monterey, CA, Section H.4.

Slashing GaN costs with SILICON

Production costs for GaN-based devices will plummet when epilayers are formed on 200 mm silicon

BY DENIS MARCON AND YOGA SARIPALLI FROM IMEC

DEVICES BASED ON GaN can serve a vast number of applications. Transistors constructed from this wide bandgap semiconductor can increase the efficiency of power supplies, solar invertors, and base station transmitters; LEDs made from GaN are already backlight billions of screens and illuminate numerous homes and offices; and sensors fabricated from this material can detect gases such as nitrogen dioxide, a source of air pollution. With all these GaN devices, if the cost of their manufacture falls, their deployment will rise.

One way to drive down costs is to switch the growth of the GaN-based epitaxial structures to a cheaper foundation – the best in this regard being silicon with a diameter of 200 mm. Epiwafers formed in this manner can be processed at very low costs, by shipping material to under-utilized, fully depreciated 8-inch silicon fabs.

Producing GaN devices in this manner is appealing, but challenging. It is far from easy to obtain wafers that have a small, controlled bow, are free of cracking or surface pits, and are made up of layers with a low density of defects. That's partly because the thermal expansion mismatch between silicon and GaN can cause the build-up of excessive tensile stress, which is alleviated by film cracking; and it is partly because the lattice mismatch during growth, plus the thermal mismatch during cool down from higher temperatures, can give rise to a high density of defects.

These lattice and thermal mismatches can also cause the wafer to bow, and if exceeds just 50 μm for a 200 mm wafer, this can prevent it from being processed in a silicon line. Note that wafer bow tends to increase with increasing wafer size, making up-scaling difficult.

At imec, an internationally renowned microelectronics research centre based in Leuven, Belgium, we are addressing these challenges. We are developing an epitaxial process for the growth of GaN on 200 mm silicon, while many vendors active in this area are focusing on the smaller 150 mm platform. Our expertise in GaN is considerable, as we have spent more than a decade developing GaN devices: depletion-mode and enhancement-mode power transistors, power diodes, and other types of devices, such as air sensors and LEDs (see Figure 1). We share the technology that we have developed with today's and tomorrow's partners, so that they can use this to design and produce their first devices in-house or at imec.

By carefully optimising each of the layers in our GaN-on-silicon structures, including the key buffer layer, we have been able to form epiwafers with a low defect density and smooth surface. According to atomic force microscopy measurements on areas of 5 µm by 5 µm, the surface has a root-mean-square roughness of just 0.4 nm.

From a manufacturing perspective, producing a few good-quality 200 mm GaN-on-silicon wafers is promising, but this will not amount to much unless it is followed up with a demonstration of long-term reproducibility. We have done just that, using various measurements to determine the quality and reproducibility of our buffer layer in structures grown on a MaxBright Veeco reactor. Crystal quality of the buffer layer shows small variation from wafer to wafer, according to X-ray diffraction measurements with a Jordan Valley QC3 tool (see Figure 2a). What's more, the average of the full-width-at-half-maximum (FWHM) for the AlGaN buffer is among the best reported in literature,

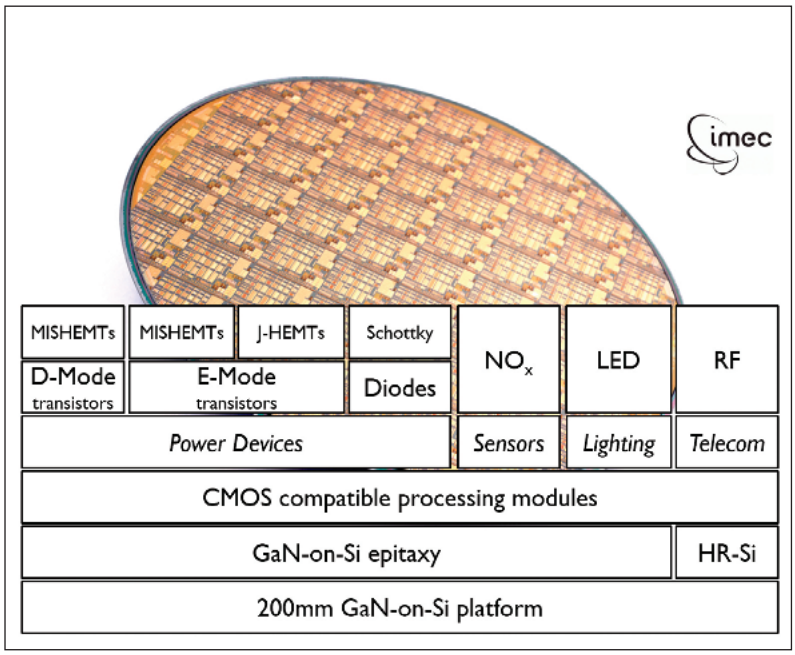


Figure 1. imec's 200 mm GaN-on-silicon platform, which can be used to manufacture a wide variety of devices.

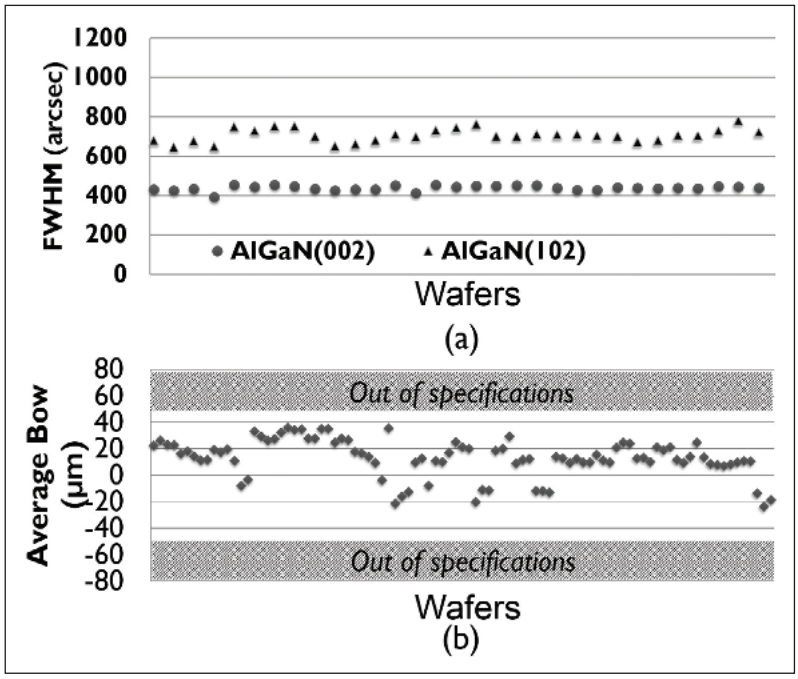


Figure 2. The 200 mm GaN-on-silicon wafers produced at imec have a buffer with excellent material quality, according to X-ray diffraction measurements (a), and a very low level of wafer bow (b). Bow must be below 50 μm bow for processing in a silicon line.

which includes smaller wafer sizes. In addition to the high crystal quality of the buffer, it is sufficiently flat to allow our epiwafers to be run through a silicon line. Measurements on 90 wafers show that all of them are suitable for processing (see Figure 2 b).

Another essential characteristic for all GaN-on-silicon epiwafers, if dedicated to power switching devices, is a low leakage current at high voltages. We determine whether our wafers meet this criterion by applying a voltage between two isolated metal pads. At 1100 V – the limit of our system – leakage measured over 20 structures across the wafer is uniform, and well below a typical spec of 1 μA/mm.

Silicon foundry suitability

Flat wafers are not the only consideration when processing GaN-on-silicon wafers in silicon lines. Engineers working in these fabs are very concerned over the use of gallium, which can contaminate the lines, because this element is a *p*-type dopant in silicon.

At imec, we have faced this issue, with the device processing team that is keen to to push GaN in the line working together with the contamination team. Together, we have found ways to prevent gallium contamination, which opens the door to putting GaN-on-silicon wafers through the lines after standard silicon lots.

A second challenge that we have faced in introducing our GaN technology in a CMOS line is associated with the contacts: they must be as good as those that include gold, but are free from this element. We have succeeded in this endeavour, producing gold-free ohmic modules with very little variation in contact resistance and a high level of reproducibility from wafer to wafer (see Figure 3). These contacts are reliable under high current density and high temperature conditions, and with an annealing temperature for the module below 600°C, they offer flexibility in process integration.

Following optimisation of the general processing modules, such as ohmic contacts and passivation, device engineers working with us, in synergy with processing engineers, can optimise their device technology. Support for this effort comes from intense TCAD and modelling activity.

Our 200 mm GaN-on-silicon platform can be used to form a range of power switching devices: depletion mode (D-mode) MISHEMTs; enhancement mode (E-mode) MISHEMTs and J-HEMTs; and power Schottky diodes, which are standalone devices that are compatible

with transistor processing, so allow a high level of integration. The D-mode transistors that are normally on are well established, with 600 V-rated devices exhibiting an on-resistance of just 0.8 mΩ cm^2. However, most research efforts are now focused on the realisation of highly performing E-mode devices, because they are easier to use in circuits – they do not have to be paired with a silicon transistor to form the preferred, normally-off mode of operation. It is the E-mode form of the device, which is normally off, that will lead to a ramp in sales of GaN transistors.

Two-pronged approach

One of the common approaches to making an E-mode device is to recess the AlGaN barrier and then deposit a gate dielectric. An alternative, popular process involves growing a *p*-type layer on top of the AlGaN, and then etching the *p*-type layer in the active region only. Both approaches, which form MISHEMTs and J-HEMTs respectively, have their pros and cons. This is why our partners – whose names cannot disclosed for reasons of confidentiality – are pursuing both options to de-risk their future investment on processing development.

MISHEMTs that we have produced exhibit a uniform threshold voltage of around +1.2 V, and a low leakage current that is in the pico-amp range at a gate voltage of 0 V (see Figure 4 a). Under forward gate bias with a 10 V gate voltage, current is below 1 nA/mm, and the breakdown voltage exceeds 15 V (see Figure 4 b).

At a gate voltage of 0 V, the breakdown voltage exceeds 600 V, demonstrating the true E-mode nature of these devices. They deliver state-of-the-art performance for an E-mode transistor, with an on-resistance of 1.5 mΩ cm^2, which is far superior to that of a standard silicon equivalent. We are now trying to take these 600 V devices to a higher level of maturity, and to increase the threshold voltage beyond 2 V, while trimming the on-resistance to below 1 mΩ cm^2.

We have also used our 200 mm GaN-on-silicon platform for the development of power rectifiers. The biggest challenge with this class of device is to combine a low turn-on voltage with a low leakage current. We have succeeded in this regard by pioneering an innovative, proprietary device architecture named the gate-edge terminated (GET) diode. This class of diode has a turn-voltage that is below 1 V, and a leakage current less than 1 μA/mm at high reverse voltage (see Figure 5).

An additional strength of these devices is their incredibly short reverse recovery time, which

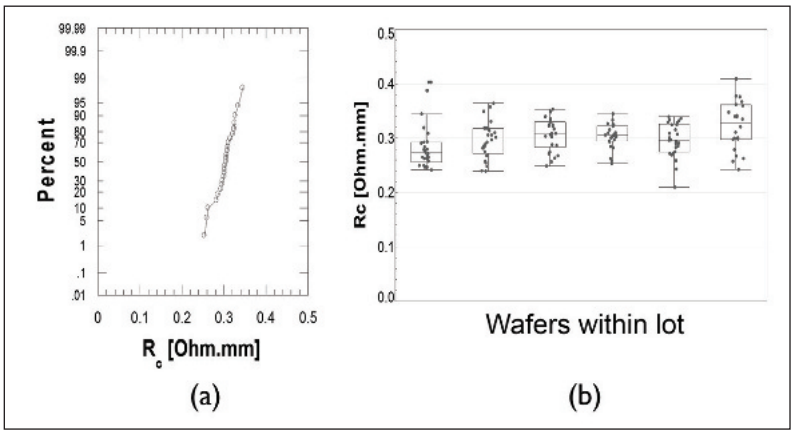


Figure 3. Gold cannot be employed as a contact metal in silicon lines, so imec's engineers have developed a gold-free alternative that has a low contact resistance and a high level of reproducibility (a). There is a small degree of variation in contact resistance between within six wafers within one lot (b).

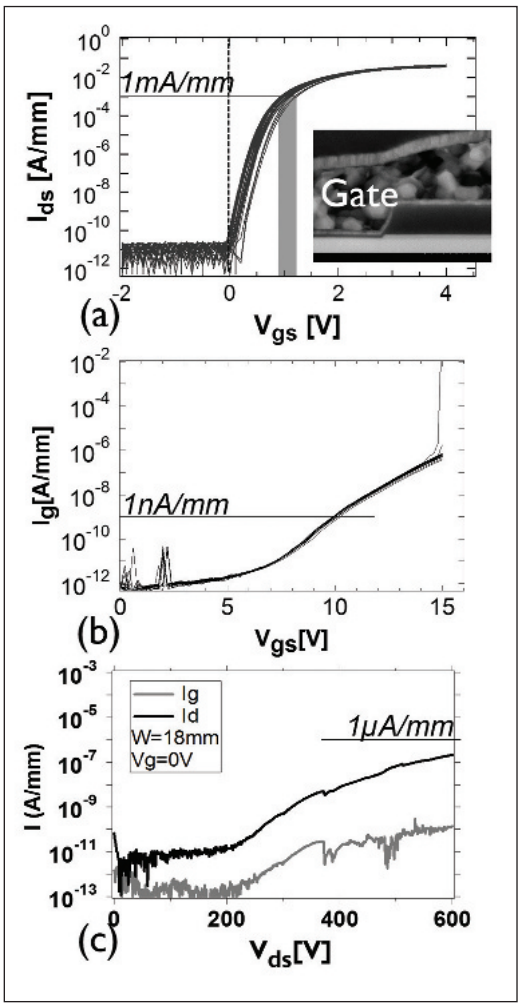


Figure 4. E-mode MISHEMTs produced at imec combine a uniform threshold voltage of typically 1.2 V (a) with a low leakage current (b) and a breakdown voltage in excess of 600 V (c).

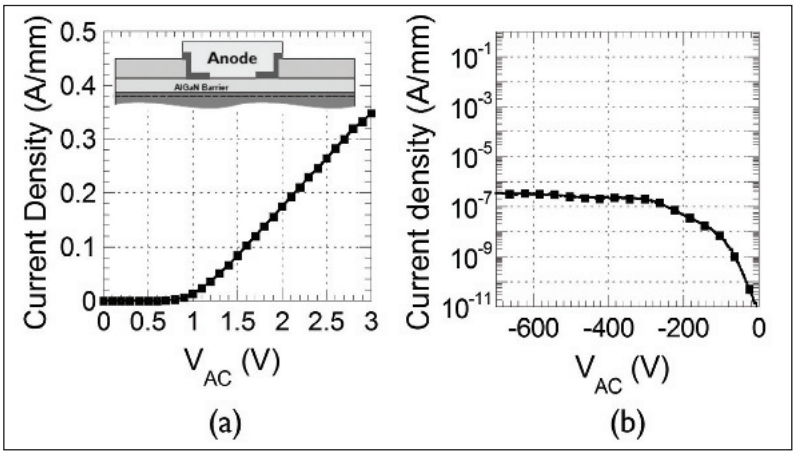


Figure 5. The low turn on voltage (a) and low leakage current of imec's novel, proprietary gate-edge terminated diodes make them ideal for use in electrical systems delivering highly efficient switching.

results from them being majority-carrier Schottky diodes. Short recovery times slash switching losses, enabling these devices to increase the efficiency in electrical systems, such as solar inverters. We expect that once these devices appear on the market, they will replace silicon and SiC diodes, because they offer a better performance than the former, and are inherently cheaper than the latter.

Detecting gases

Our 200 mm GaN-on-silicon platform is not restricted to the production of power devices: it is also capable of producing NO_x sensors and LEDs, while RF devices offer an opportunity for future collaboration. It is astonishing how the same GaN material and platform can be used for so many different applications!

Detecting levels of NO_2 is very important, because emissions of this gas can jeopardize human health and cause ecosystem damage. Consequently, there is a great demand for ultra-compact, portable and even wearable low-cost continuous NO_2 monitoring devices. Sensors on the market today do not satisfy all these requirements. They are either too costly, too bulky, or fail to provide the NO_2 sensitivity or reversibility required for continuous air quality monitoring, where detection at concentrations of less than 50 parts-per-billion is needed.

It is possible to meet all these requirements with our GaN-based technology that can yield devices with a reaction time below 2 seconds and a detection limit below 1 ppb for NO_2 (see Figure 6). With these devices, the level of NO_2 concentration is revealed by variations in the resistance of the two-dimensional electron gas in the channel. These devices are showing much promise, having already been used to monitor NO_2 inside underground parking garages, where they have produced very good results.

It is clear that GaN devices are accounting for an ever-larger proportion of the semiconductor market. The 200 mm GaN-on-silicon platform that we have developed with our partners will help to accelerate the increasing deployment of this wide bandgap semiconductor, which can be used to make many different devices. Some companies might find it a formidable challenge to make the transition to manufacturing GaN devices, but this should not be too daunting, as we can help them to gain easy access to this technology, accelerate their internal GaN development and provide them with access to next-generation GaN-based epitaxy and device technologies currently under development.

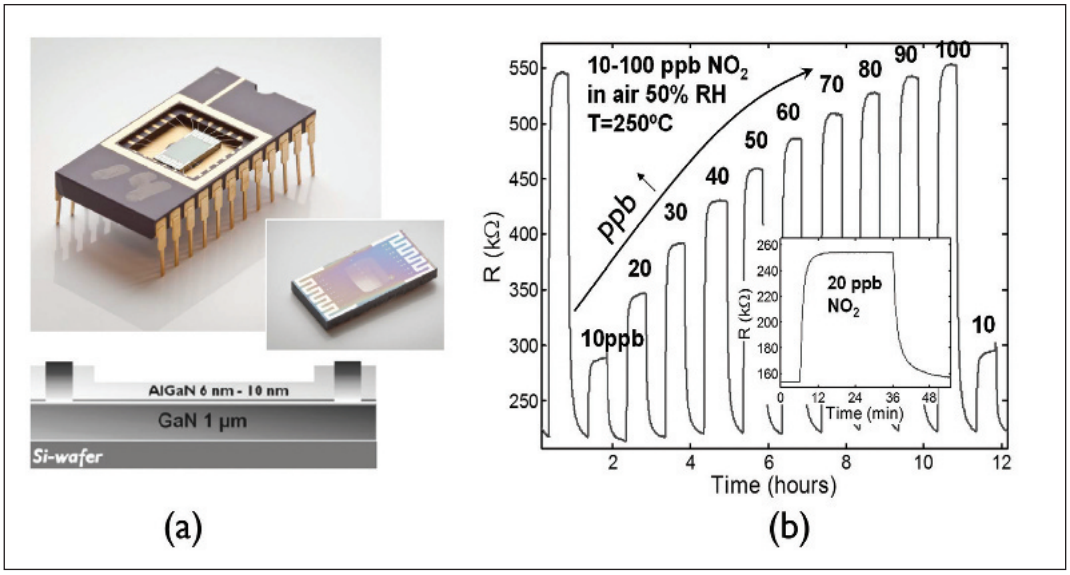


Figure 6. imec's GaN-on-silicon platform can be used to make NO_2 sensors (a). Detection of this pollutant oxide is possible downto levels of 10 parts per billion (ppb) and below, with the sensor delivering a quick response to changes in concentration that lead to changes in the resistance of a two-dimensional electron gas.

Increasing the availability of GaN HEMTs

A robust, reliable foundry process will spur a proliferation of GaN applications

BY WALTER WOHLMUTH, WEI-CHOU WANG, I-TE CHO AND WEN-KAI WANG FROM WIN SEMICONDUCTORS

THE TREMENDOUS AMOUNT OF MONEY poured into the development of GaN RF and power devices is enabling new markets and driving an upheaval in existing ones. Thanks in part to governments around the world funding a variety of projects – including US initiatives such as DARPA's Wide Bandgap Semiconductors for RF and AFRL's title III GaN-on-SiC programme, plus the European effort KORRIGAN and the Japanese project NEDO – this technology has matured significantly.

GaN technology is now at a comparable maturity level to the GaAs technologies of the late 1990s, prior to the explosive growth in that industry. This was driven by commercial opportunities requiring higher data transmission and better efficiency.

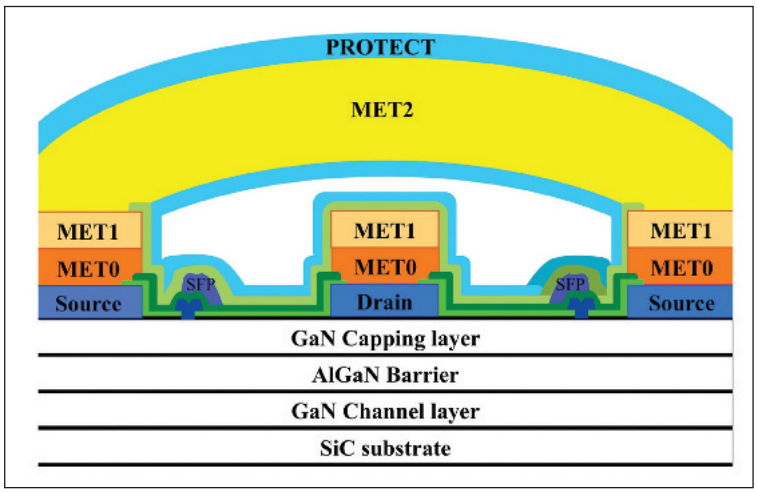


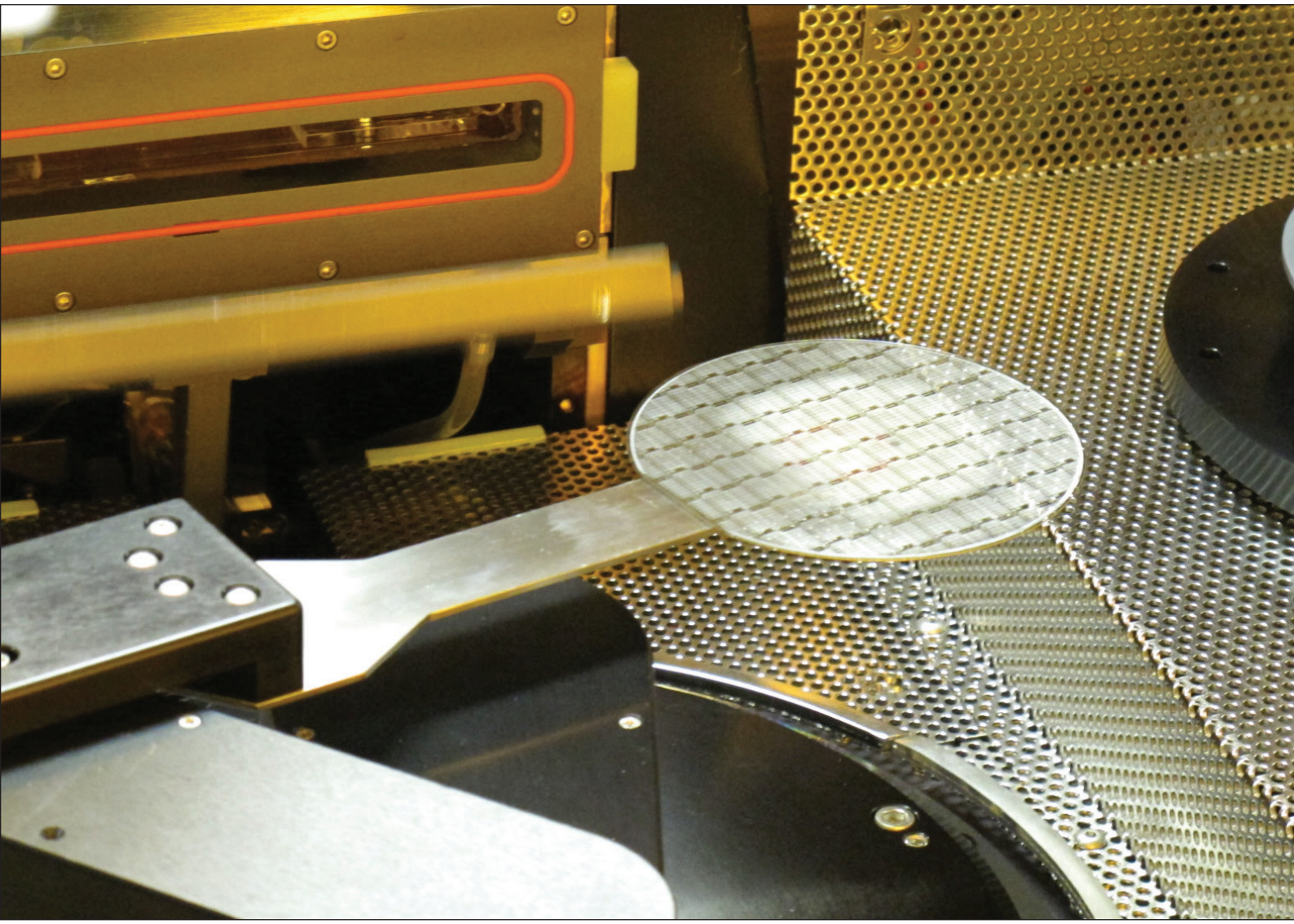
Figure 1. WIN has a GaN process involving damascene T-gates with overlying source-coupled field plates to control the electric field distribution. A thick 4 μm air-bridge enhances current handling capabilities and provides high-Q inductors.

The commercial opportunities for GaN include wireless communication. The traditional transistor deployed in base stations is silicon LDMOS, but migration to 4G LTE and HSPA networks sporting higher bandwidths has triggered a move to GaN HEMTs combining higher efficiency, higher bandwidth and reduced cooling requirements with a comparable price at the system level. This trend is set to continue, as base station products formed with GaN deliver the requirements for 4G communications while offering excellent reliability.

Other opportunities for GaN in the RF arena include a class of satellite communication known as VSAT, which is moving towards a more complicated, data-intense transmission technology referred to as the 4096 QAM format.

There are also changes in cable TV transmission technologies that are playing into the hands of GaN, as operators move to OFDM transmission on both up and downstream paths, due to the implementation of DOCSIS3.1 specifications that have a higher bandwidth in order to serve video-on-demand and HDTV.

And it is not just silicon LDMOS that is under threat from GaN – this material could also displace archaic, staid technologies such as travelling-wave tubes and magnetrons used for microwave heating and phased array radar. In today's microwave ovens, heating is extremely inefficient, imprecise, and bulky, and introducing GaN could address all these weaknesses. Meanwhile, a switch to GaN in radar system architecture could trim weight and cooling



Automation on WIN's GaN-on-SiC wafer processing line

needs, benefits that are highly welcome in the field of avionics. What's more, GaN devices could replace travelling wave tubes for phase shifters.

GaN will also start to displace GaAs in some applications. Low-noise amplifiers based on GaN are more rugged than their GaAs counterparts, so circulators or isolators can be removed from the antenna path. Meanwhile, for power amplification, GaN delivers more power per unit area.

Why WIN?

To address all of these markets, WIN Semiconductors is offering a comprehensive portfolio of GaN technologies from sub-GHz to 40 GHz, including power amplifiers, low-noise amplifiers, RF switches and passive components. Our flexible and open foundry approach enables these technologies to be optimized to meet customer needs. In addition, they can be paired with our extensive GaAs technology, allowing customers to enjoy the best of both worlds.

Another advantage that we have is that we can apply lessons to GaN manufacturing that we learnt from increasing our GaAs manufacturing volume, which is upwards of 24,000 150-mm wafers per month. This provides us with a competitive edge for cycle time, customer service and support, breadth of technologies, and competitive prices due to economies of scale.

If GaN devices are to become a mainstream, mass production technology, long-term demand for them will only exist if they can be manufactured in a manner that yields stable, reliable and repeatable products. Significant progress has been made by material suppliers, leading to better-quality semi-insulating SiC substrates with fewer defects and greater consistency.

This has been backed up by advances by suppliers of epitaxial growth services, with improved material quality enabling a stable supply chain. Thanks to these breakthroughs, optimising device processing is quicker than ever, because experiments produce far fewer ambiguous results, so learning is now very fast.

In comparison, GaN-on-silicon technology is not as mature. High defect densities impact material quality and repeatability, and there are also issues associated with excessive wafer warpage and losses associated

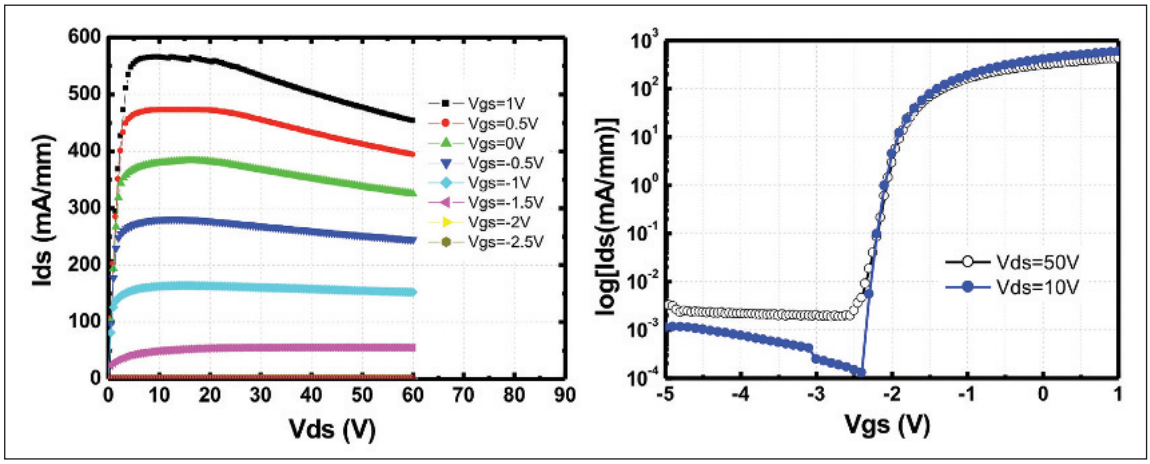


Figure 2. DC performance on the 0.50 μm GaN-on-SiC process. The I_{ds}-V_{ds} curve records operation to 60 V for the nominal 160 V breakdown voltage process. The plot reveals good sub-threshold characteristics and high I_{on}/I_{off} ratio for a compound semiconductor technology

with large edge exclusion zones. All of these are induced in part by the large lattice mismatch between GaN and silicon.

As well as these material issues, there are drawbacks in device design with GaN-on-silicon. Most high performance GaN RF power amplifiers require low resistance and low inductance source vias. Backside via formation can be challenging once the silicon substrate is thinned due to excessive warpage. The thermal conductivity of silicon is inferior to that of SiC resulting in electro-thermal performance issues for GaN-on-silicon devices that limit the power density of the transistors.

Power switching devices are less affected by this, because they generate far less heat under normal operating conditions than their RF counterparts. What's more, power devices don't tend to include backside source vias, simplifying backside wafer processing and reducing cost. Consequently, GaN-on-silicon technology is predominantly used in the power switch market, where it gives little away in performance to GaN-on-SiC, but is cheaper. In contrast, in the RF market there is a premium placed on performance and reliability, so GaN-on-SiC reigns supreme. Note, however, that there are niche opportunities for GaN-on-SiC for power switches, with the greatest chance of success in applications requiring blocking voltages in excess of 600 V.

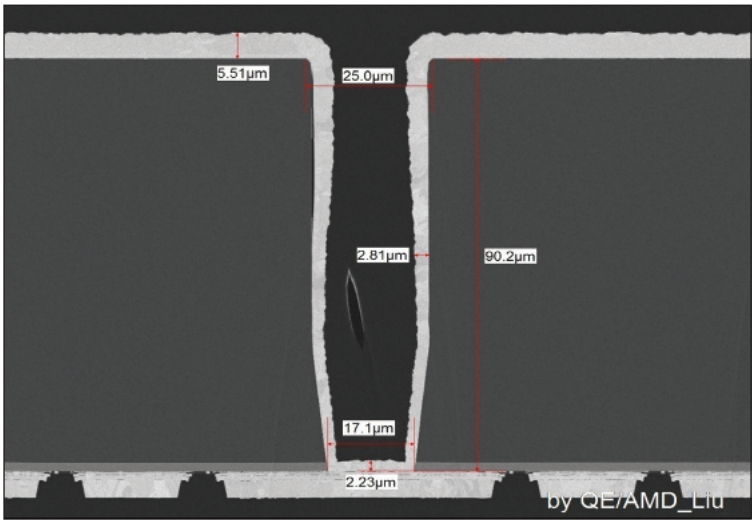


Figure 3. Scanning electron microscopy cross-section of a transistor with an integrated source backside for low-source inductance and resistance connections. A 30 μm x 60 μm oval substrate via connects backside metallization to the front-side source of the transistors. The T-gate is visible adjacent to the source pads on the bottom of the figure. Note that the divot inside the substrate via is potting material used to prepare the sample before SEM imaging

Device manufacture

We sub-divide the engineering of our transistor into five main areas: epitaxial design on SiC substrates, dielectric engineering, metallurgical engineering, electro-thermal design, and interface engineering. Many groups around the world have investigated these topics in detail, leading to a vast body of published literature on every one of these subjects. Insights are offered in the form of patents and papers, and we undertook a painstaking analysis to manoeuvre around existing IP.

High-voltage handling and high output power of the transistors is possible through the use of a damascene T-gate and an overlying source-coupled field plate. Minimal charge trapping and dispersive effects result from interface and dielectric engineering, enabling good, stable and repeatable device performance.

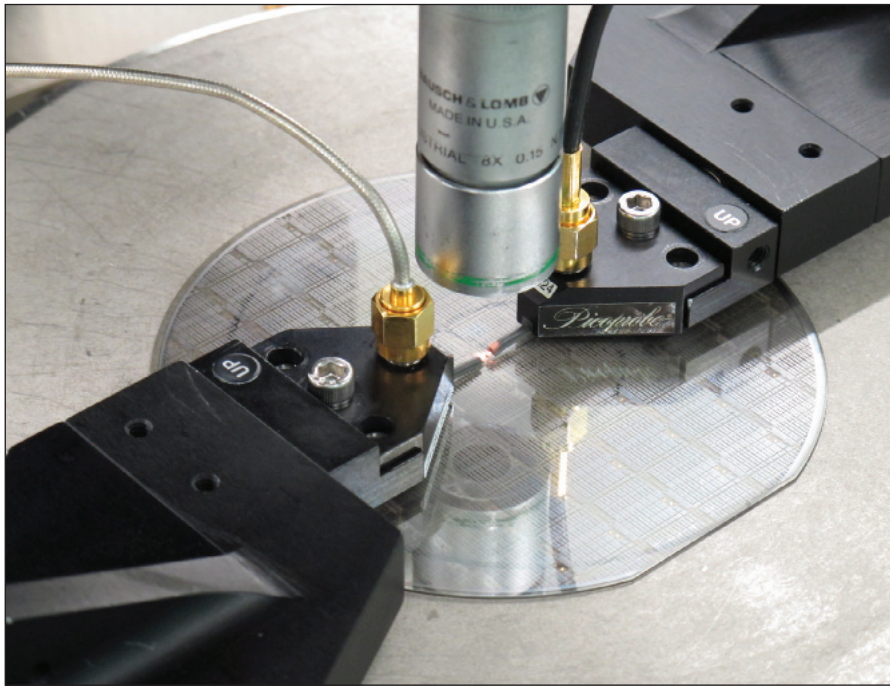
We offer a portfolio of transistor technologies, with different gate lengths and breakdown voltages. Devices formed with our 0.15 μm and 0.25 μm processes are engineered to operate at 28 V, and have a minimum breakdown voltage of 70 V. Meanwhile, the GaN HEMTs fabricated with our 0.50 μm process are designed to operate at 50 V and have a minimum breakdown of 130 V (see Figure 2).

In our case, the interconnect and passive component architecture for the GaN MMIC processes has been leveraged from our GaAs MMIC technology, but modified primarily for higher operating voltages. Circuits are constructed with high-performance, edge-lifted ELC MIM capacitors, thin film resistors, and high-Q inductors that are commonly deployed in our GaAs technology. This creates a GaN technology that features a robust MMIC process with a 4 μm-thick air-bridge metal and 1 μm-thick global interconnect metals.

We were able to draw on our expertise as the world's largest manufacturer of GaAs devices to re-engineer the back-side processing of GaN-on-SiC HEMTs, rather than following the approaches our competitors. Our efforts led to the development of a highly manufacturable process technology that includes: high-speed etching through SiC and then GaN-based materials; improved wafer mounting media involving specialized bonding wax and substrates; handling of by-product formation during high-speed etching and subsequent, repeatable removal of by-products; and back-side seed layer optimisation for good adhesion and conformal coverage in 100 μm deep vias with a width of less than 30 μm (see Figure 3 for a 30 μm x 60 μm oval substrate via that connects back-side metallization to the front-side source of the transistors).

Additional aspects of our processing technology include improvements in regards to demounting of a highly stressed thinned wafer; high-speed sawing with minimal chipping of an extremely hard SiC material system; optimisation of tape materials to provide environmentally-friendly, green material usage; and care to control interactions between all of these many processes.

Using this approach, we produce devices that deliver high-efficiency RF performance. By reducing source inductance and resistance, our HEMTs provide stable linear gain at low input power and have good 3dB/decade compression. When delivering a 3 GHz, continuous-wave input signal at a 50 V bias, the output power exceeds 5.5 W/mm, power-added efficiency is greater than 60 percent, and linear gain is almost 19 dB higher than that produced with silicon LDMOS technology (see Figure 4).



On-wafer measurements on WINs GaN-on-SiC wafers

Reliability of our devices has been proven through extensive reliability testing that complies with many JEDEC specifications. By working in collaboration with researchers at the University of Bristol, Centre for Device Thermography and Reliability, we have accurately determined the junction temperatures for the devices during reliability testing and under normal operating conditions. One of the JEDEC specifications is associated with a DC high-operating-lifetime-test that forms a basis for evaluating the mean-time to failure (MTTF). Testing involved four sets of samples from the 0.25 μm GaN-on-SiC process, with devices driven until they failed at temperatures ranging from 331 °C to 369 °C. Curve fitting revealed an MTTF of 1

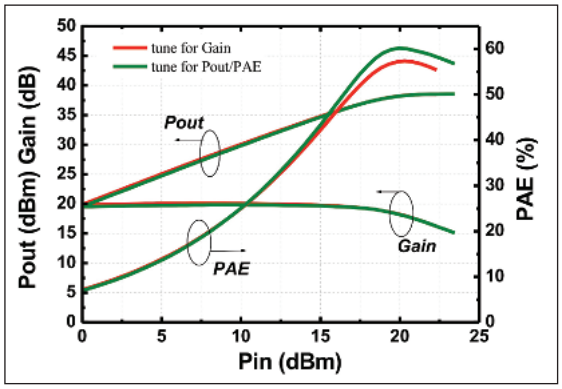
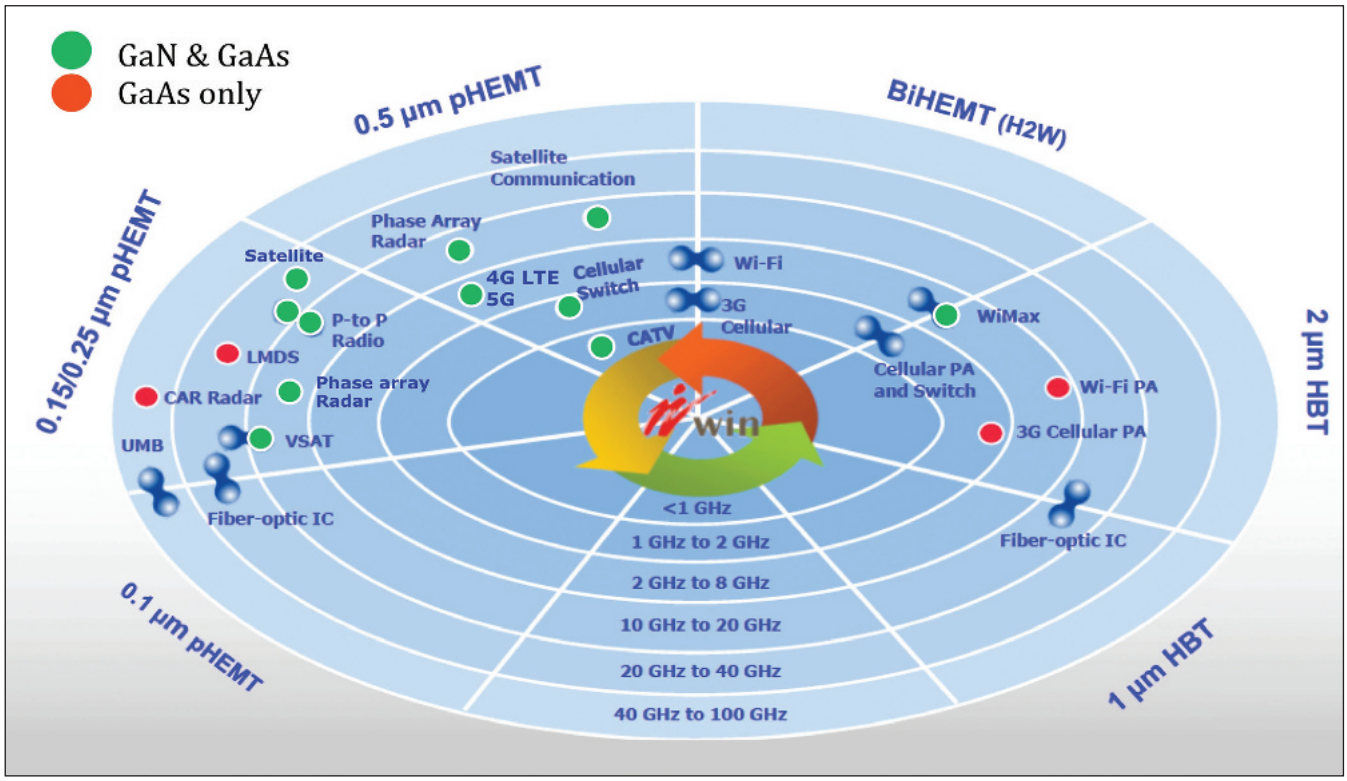


Figure 4. RF performance on the 0.50 μm GaN-on-SiC process at 3GHz with I_{dq}= 10mA/mm and V_{ds}=50V for a 1.25 mm device achieving more than 5.5 W/mm under continuous-wave conditions



Many different applications are enabled by WIN Semiconductor Foundry Services

million hours and an activation energy of 2.1 eV for a peak channel temperature of 238 °C. These findings are in line with recent reports in literature (see Figure 5).

On its own, an excellent process for producing GaN HEMTs is of little value to designers – it needs to be backed up with a comprehensive process design kit providing accurate modelling and supporting data. We have met this need and offer a proprietary, scalable model that can simultaneously predict GaN HEMT performance under DC and pulse operating conditions, and provide a good prediction of large-signal characteristics (see Figure 6).

This model, which is supported in both Agilent ADS and AWR Microwave Office software platforms, also includes comprehensive passive modelling. This exploits our expertise in passive components, with the model modified for differences in substrate and epitaxial materials. Engineers that are armed with this toolkit and use our GaN fabrication services are well placed to tap into the many, growing opportunities for this wide bandgap transistor. During the next decade, it is sure to become the incumbent technology in many parts of the RF domain.

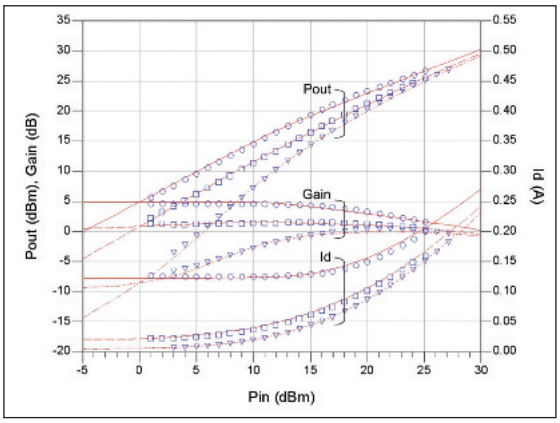


Figure 6. Model verification for one-tone characteristics at 10 GHz measured with 50 Ω termination for a 1.25 mm, 10 x 125 µm device. Good fit obtained for various quiescent I_{dq} conditions. Note that symbols and lines represent measured and simulated data, respectively.

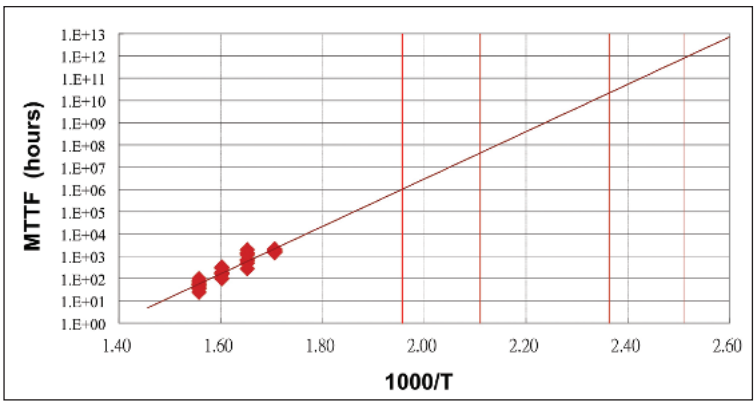


Figure 5. Mean-time-to-failure (MTTF) performance for the 0.25 µm GaN-on-SiC process. Activation energy is 2.1 eV and MTTF is 1 million hours at a peak junction temperature of 238 °C.

The authors would like to thank all the members within WIN Semiconductors who supported the GaN technology development, including the characterization, modelling, reliability, manufacturing, logistics, industrial engineering, customer engineering, sales and marketing, and quality control teams.

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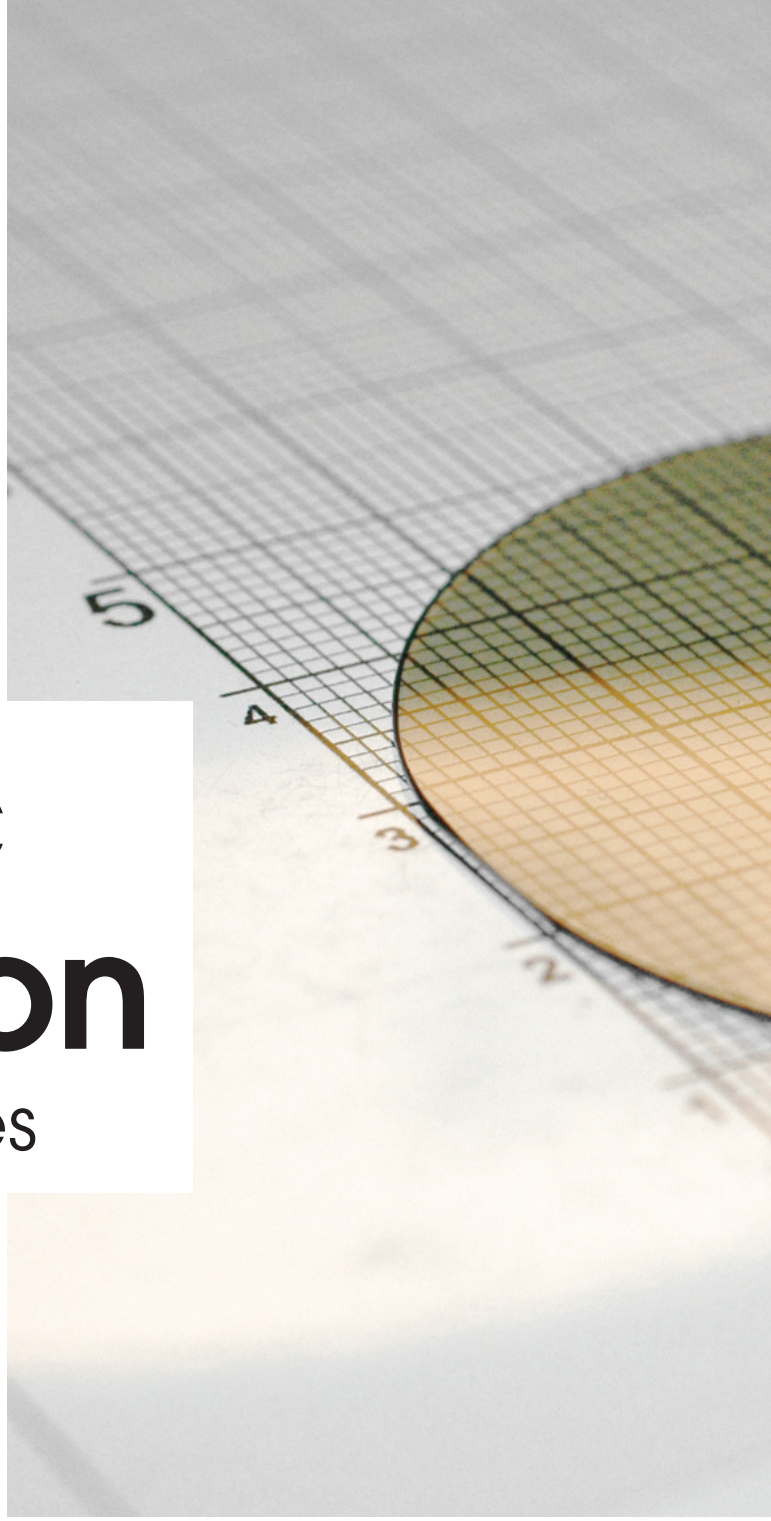


Fantastic foundation

yields great devices

GaN substrates formed from ammonothermal growth underpin the fabrication of devices delivering outstanding levels of performance

BY PIOTR WILINSKI FROM AMMONO

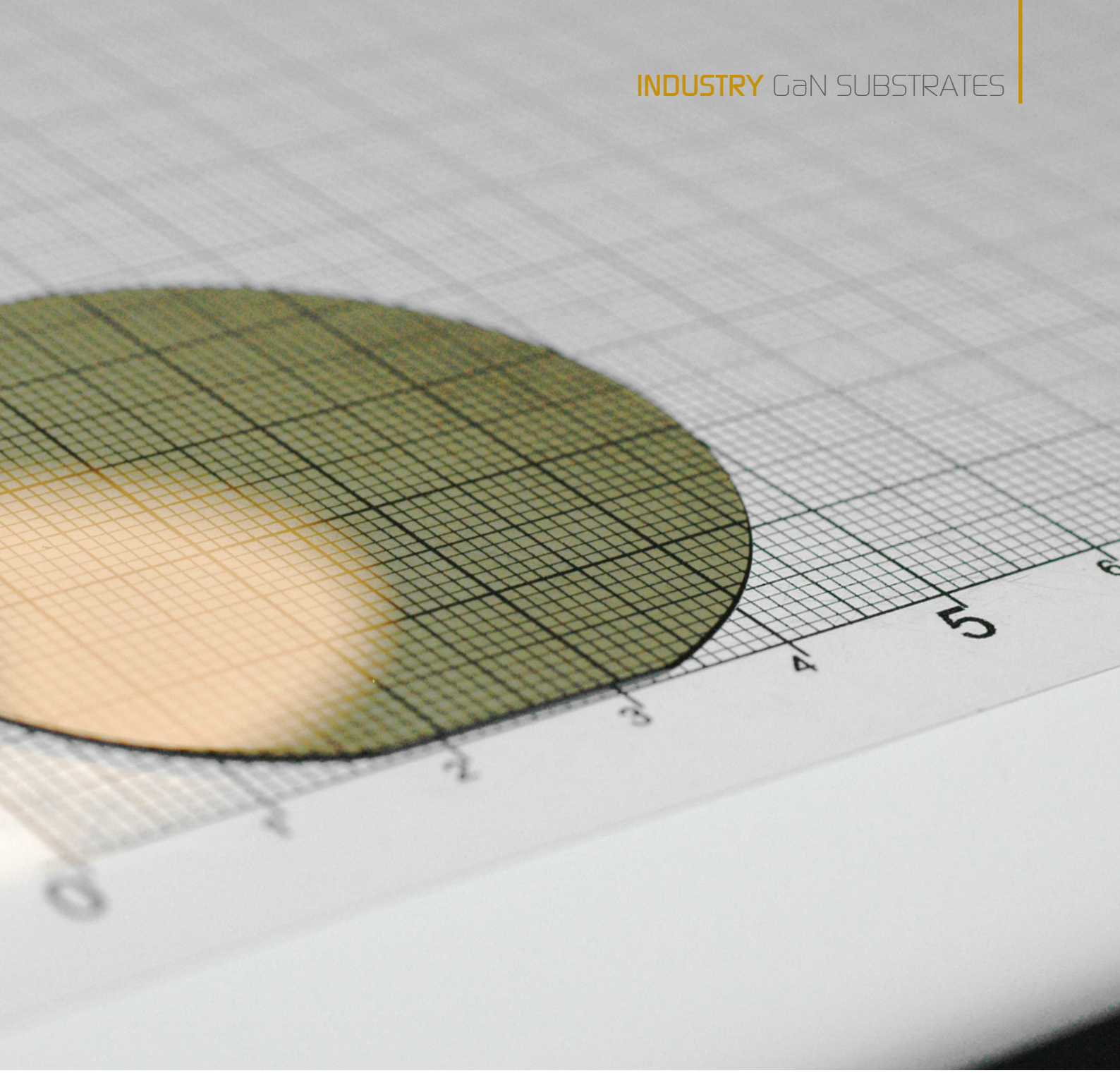
IF YOU WANT to make a great GaN device, you must start off with a native substrate. By doing this and thus employing homoepitaxial growth, issues associated with differences in thermal and lattice mismatch are eliminated, so the epiwafers are flat and material quality high.

A native substrate is actually the only option for growing ultraviolet, blue and green lasers – all alternative foundations lead to material quality that is insufficient for the manufacture of commercial products. Due to this monopoly, it is not that surprising that for the makers of GaN substrates, shipments to laser diode manufacturers account for a high proportion of sales. Lasers formed on these substrates feature in the read and write heads Blu-ray players and recorders, and shipments of edge-emitting chips should increase as they are deployed in optical laser displays, laser TVs, movie projectors and pico-projectors, printers, and lithography systems.

In comparison to the laser, the LED is a less demanding device, capable of delivering good performance with material of lesser quality, formed via GaN growth on a foreign substrate. However, for really high levels of performance at very high currents densities, a GaN substrate is invaluable. Soraa, Panasonic and Seoul Semiconductor use this foundation to make LEDs, and are causing something of a stir with devices delivering very high output power densities, while suffering from relatively little droop – the decline in device efficiency with increasing current. GaN substrates are also valued in the electronic domain. Armed with this foundation, engineers can turn to vertical device architectures and produce smaller chips with higher breakdown voltages, higher power densities and higher signal frequencies.

Variations in quality

It would be easy – but wrong – to think that all GaN substrates would yield the same results. While differences between the



performances of devices made on different types of substrate may be bigger than the variations between those made on GaN, the quality of the native substrate does still have a big impact on the attributes of the resulting chip.

The majority of GaN substrates sold today are formed by depositing a thick layer of this material by HVPE to form a GaN crystal, and then slicing this up. Manufacture by this approach, which is employed by the likes of Sumitomo, Hitachi and Mitsubishi, produces a substrate that is not perfectly flat, because at some point GaN growth had to be initiated on a non-native substrate. What's more, the defect density in these substrates is far higher than that found in InP and GaAs substrates – it is typically in the region of 10^6 cm^{-2}.

GaN substrates with a far higher material quality are possible with the ammonothermal growth technique that we pioneer at Ammono of Warsaw, Poland. Our approach involves the growth of Ammono-GaN crystals in an autoclave containing GaN seeds, ammonia, and alkali metal amide mineralizers. Heating this concoction to around 550 °C, while maintaining it at pressures of typically 5000 atmospheres, leads to the growth of GaN crystals with a dislocation density that can be as low as 10^3 cm^{-2}. They can be sliced into crystals that are exceptionally flat.

We are currently scaling up our production of GaN crystals to serve our customers, which number more than a hundred. By building bigger autoclaves, we can grow bigger crystals and increase the size of our substrates from 2-inch – our standard offering today – to 4-inch. The industry will eventually move to even larger substrates, and there is no fundamental reason why we cannot move accordingly, by producing 6-inch and then 8-inch material.

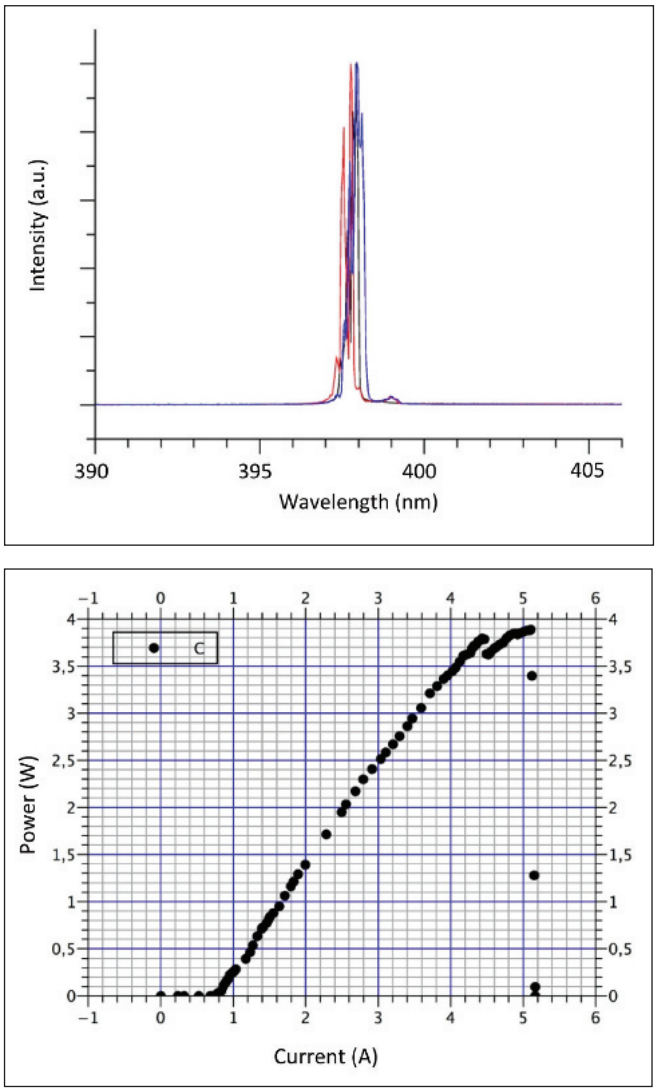


Figure 1. UV Laser Matrix emission spectrum (a) and the dependence between the optical power and current (b)(courtesy of TopGaN).

Scrutinizing our material with various common semiconductor characterisation techniques, such as X-ray diffraction, microscopy and optical methods has already proven that this form of GaN is superior to its HVPE-grown cousin (see *Bulk GaN: Ammonothermal trumps HVPE* from *Compound Semiconductor* March 2010, p.12). Also, intrinsically, for bigger wafers sizes the production cost for an Ammono-GaN wafer is lower than for HVPE GaN. To what extent this leads to superior device performance is still to be fully established, but we are making efforts to determine this by teaming up with various partners, together producing and evaluating devices built on our substrates.

In the majority cases, results obtained by these partners are confidential and covered by non-disclosure agreements. But there are some instances where we can reveal findings, because participants in the project have received external funding and there is an obligation to report results in the public domain.

Better lasers

One such effort has focused on the fabrication and testing of laser diodes. This has showcased the virtues of working with GaN substrates formed from ammonothermal crystal growth.

When nitride lasers can deliver an output of a Watt or more, they can be used in laser displays delivering exceptional brightness and colour resolution. What's more, these sources can be used to construct high-power laser arrays that form the heart of efficient white-light sources involving the pumping of a phosphor. This technology is being pursued by BMW for use in car headlights.

Working in partnership with TopGaN Lasers and the Institute of High Pressure Physics in Warsaw, Poland, powerful arrays of InGaN laser diodes have been fabricated. By forming several stripe emitters on a single chip, the power density per emitter is reduced. This avoids catastrophic optical damage that leads to facet melting – which can occur above a threshold current density of around 50 MW/cm^2 – and ultimately creates devices with long lifetimes.

Violet-emitting chips formed in this manner with three and 16 emitters have delivered a maximum output power of 2.5 W and 4 W, respectively (see Figure 1). These laser, which deliver a performance that is 'top of the class', typically operate at 408 nm - 412 nm. Threshold current for three-stripe emitter is 1.2 A, corresponding to a current density of 5 kA/cm^2, and threshold voltage is 6.5 V. Meanwhile, slope efficiency is 0.76 A/W, and for a 10 μm stripe-width device the line-width is very narrow – it is just 0.25 nm. Another impressive attribute of these chips is that their light-current characteristics for individual stripes are fairly similar, with emission comparable within an experimental error of ±0.4 nm. This means that the emission wavelength is very uniform within one chip.

As explained previously, this multi-emitter chip design avoids catastrophic optical damage at the facet, leading to a long lifetime. For our 16-emitter device, which delivers an output of 4 W at a 6A drive current, the operating current density is just 18 kA/cm^2. This enables a reasonable lifetime that exceeds 6000 hours.

We attribute the world-class performance of these lasers to the exceptional quality of the Ammono-GaN substrates. If the defect density in a laser is high, or non-uniform, it is well established that this impairs performance, shortens lifetime, drags down efficiency and hampers reliability. These issues do not exist in our partner's lasers – one of the great strengths of our substrates is their very low, homogeneous dislocation density that is replicated in the epitaxial structure.

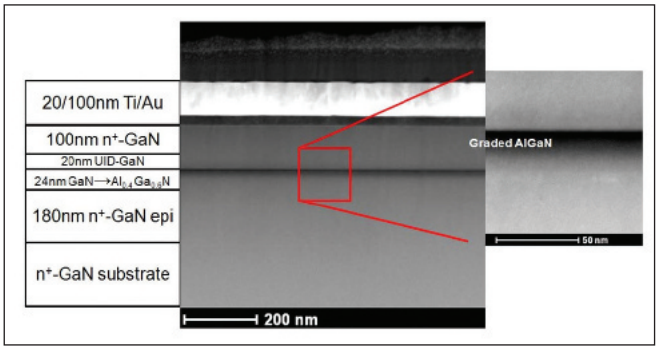
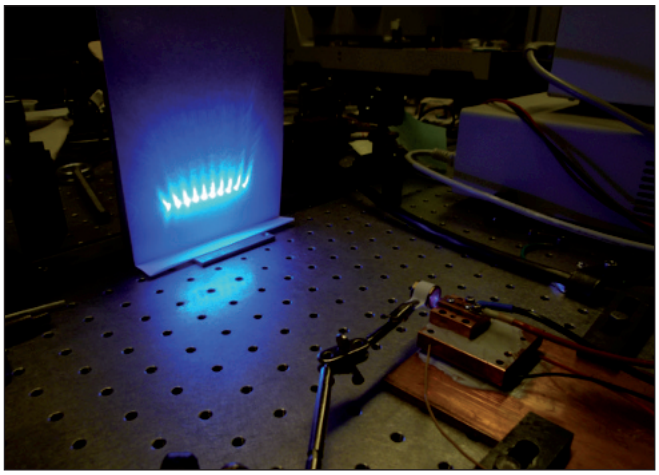


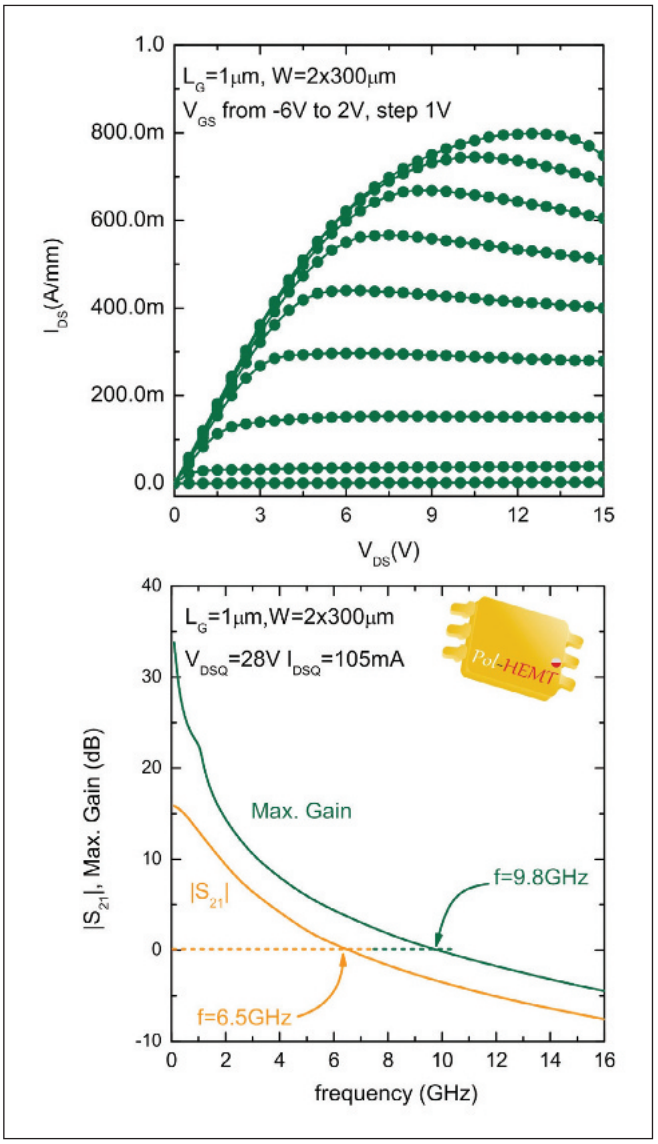
Figure 2. Epistructure of the GaN Schottky barrier diode and a corresponding scanning tunneling electron microscopy image. The growth interface between bulk substrate and epitaxial layer is invisible. (Courtesy of University Notre Dame)



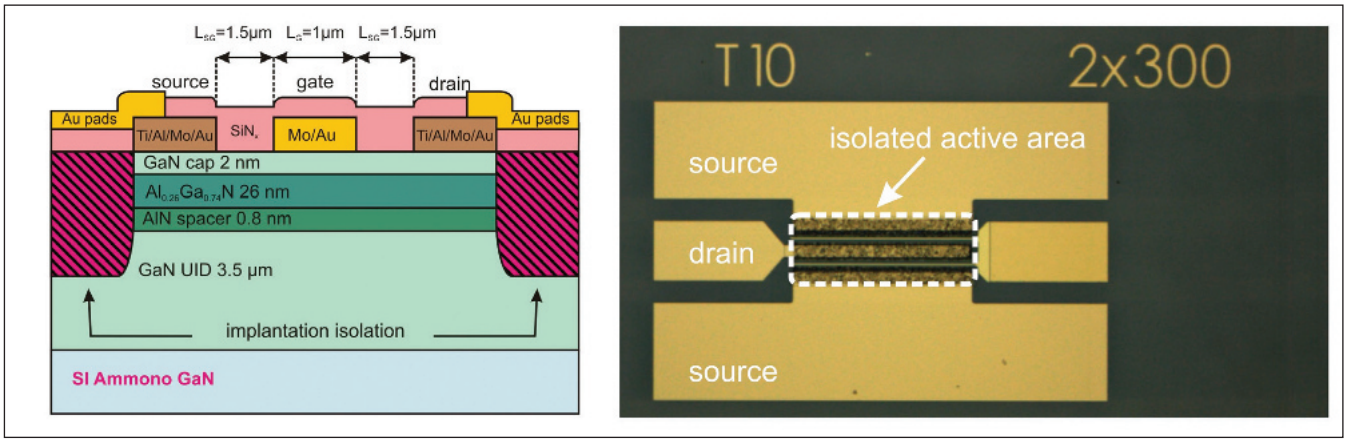
TopGaN has produced lasers with Ammono's GaN substrates that deliver state-of-the-art output powers.

A further virtue of our substrates is their high level of conductivity, which stems from an electron concentration of the order of 10^{19} cm^{-3}. This high concentration produces a lowering of the refractive index in the GaN substrate, enabling a so-called plasmonic effect. This is highly beneficial, because a higher output power results from a lower level of laser mode penetration into the substrate, and enhanced wave-guiding and light confinement within the laser chip. Consequently, it is possible to trim the AlGaN cladding layers while maintaining high-performance. In turn, this leads to a simpler laser diode structure that is: less bowed, thanks to smaller stress generated by lattice mismatch between the AlGaN cladding and the InGaN/GaN quantum wells; and has a lower defect density than conventional devices, which have thicker AlGaN claddings.

Trimming the AlGaN cladding thickness has proven to be highly beneficial for the fabrication of Ammono-GaN 460 nm, blue laser diodes grown by plasma-assisted MBE. This growth technology is ideal for growing quantum structures, because it can realise very sharp interfaces and provide very good control of epitaxy parameters at relatively low temperatures in a non-hydrogen environment. By reducing the thickness of the AlGaN cladding, lifetime of the laser can top 2000 hours. This Ammono-GaN based device, which delivered a maximum output power of 80 mW, delivers outstanding performance for an MBE-grown blue laser diode.



DC and RF characteristic of the Ammono-GaN HEMT(courtesy Institute of Electron Technology, Poland)



Ammono-GaN HEMT cross-section (left) and view from the top (right) (courtesy Institute of Electron Technology, Poland)

Different planes

To produce green-emitting devices based on the nitrides, engineers have to increase the indium content in the quantum well. In conventional structures grown on the *c*-plane of GaN, this leads to high internal electric fields that pull apart the electrons and holes and hamper light emission.

These unwanted electric fields can be reduced, and even eliminated, by growing devices on different planes of GaN, known as semi-polar and non-polar planes. Ammono-GaN substrates with these orientations are available commercially from us.

Our partners have started to investigate the potential of devices grown on this classes of substrate, fabricating LEDs and laser diodes on the semi-polar ($20\bar{2}1$) plane. Using plasma-assisted MBE, LEDs were formed on this substrate and also on the (0001) plane. Peak emission wavelength varied considerably between the two forms of device, with emission at 387 nm for the semi-polar LED and 462 nm for the non-polar, due to considerably lower indium incorporation for growth on the semi-polar plane.

Characterisation of the semi-polar epitaxial LED structure reveals a smooth surface morphology with atomic steps, according to atomic force microscopy, and high photoluminescence intensity. Inspection of the material with a transmission electron microscope indicates that the interfaces are abrupt and there is good structural quality. Ultraviolet laser diodes emitting at 388 nm have also been formed on ammonothermal ($20\bar{2}1$) substrates. Devices with a ridge waveguide along [$\bar{1}2\bar{1}0$] direction exhibited a threshold current density and voltage of 13.2 kA/cm^2 and 10.8 V. These values are quite high, but should be reduced by processing the ridge along the [$10\bar{1}4$] direction, because this should lead to higher material gain, thanks to in-plane anisotropy.

Electronic devices

Native substrates should also aid GaN power devices. Currently, these are manufactured on either silicon or SiC, but if GaN were used, this would allow a switch from a lateral to a vertical device architecture. With lateral devices, there are many problems associated with lateral current flow near the buffer layers and overlying dielectric layers, including current-collapse, high dynamic on-resistance and an inability to support avalanche breakdown. Further downsides arise from stress in the buffer layers that cause wafers to bow, limit epilayer thickness and ultimately place a ceiling on the maximum blocking voltage, which is typically no more than 1.2 kV.

Turning to a native substrate allows GaN power devices to be constructed with a vertical architecture. Current can then flow through the epitaxial layers, leading to devices that are immune from current collapse and dynamic on-resistance.

In such devices, which exhibit true avalanche breakdown, charge trapping effects and barriers to heat removal are absent, and it is possible to grow very thick layers of GaN that produce very high blocking voltages.

Our partners have started to investigate the potential of such devices grown on native substrates, evaluating the performance of GaN Schottky barrier diodes and HEMTs. At the IWN conference held this year, we co-authored a paper detailing a 6 GHz RF power transistor formed on Ammono-GaN, following our collaboration with the Institute of Electron Technology from Warsaw. In HEMTs and GaN Schottky barrier diodes, the low defect density in the ammonothermal substrate is retained in the epilayers, which have an atomically smooth surface and flat interfaces.

Comparisons between devices built on different forms of GaN substrate are still to be carried out. However, some very impressive results were realized with devices formed on Ammono-GaN (see Figure 2). Schottky diodes produced at University of Notre Dame produce a leakage current density of the order of 10^{-11}A cm^{-2}, according to publications by this team.

The electric field at breakdown voltage in these devices is 3.3 MV/cm, so close to the theoretically predicted critical field of 3.5-3.8 MV/cm. The HEMTs on Ammono-GaN have a two-dimensional electron gas density of 8 x 10^{12} cm^{-2} with a mobility of 1600 cm^2 V^{-1} s^{-1} at 300 K and 8000 cm^2 V^{-1} s^{-1} at 77 K.

These results, plus those of the LEDs and lasers, highlight the promise of Ammono-GaN, and indicate that better substrates lead to better device results. Availability of this material will steadily increase, and in time there should be more devices based on homoepitaxial GaN on the market delivering top of the class levels of performance.

Programs with Ammono participation

In 2013, Ammono started to work with the European Space Agency. This partnership began because GaN is now viewed as a key strategic material for the development of space electronics.

Devices made from this material are perfect for space applications: they have a high resistivity to ionizing radiation, a low energy loss, and when they are grown on Ammono-GaN they can deliver a higher electrical efficiency than when they are formed on other materials. Today, Ammono develops wafers optimized for the development of RF electronics for space communications. The exceptional quality of the substrate leads to devices with a longer lifetime, which is highly valued, due to the very high costs associated with getting every kilogram into space.

Another program launched in 2013 is the Strategies for Wide-Bandgap, Inexpensive Transistors for Controlling High-Efficiency Systems (SWITCHES) initiative run by the US Advanced Research Projects Agency-Energy. This $27 million programme aims to stimulate the development of power electronics on GaN and related materials. Ammono is involved in two projects within the programme. They have the goals of conceiving transistors and Schottky barrier diodes that will allow more efficient energy transmission.

Last but not least, one of the share-holders of Ammono is Nichia – the world leader in optoelectronics. The access to top of the class substrates allows them to keep at the forefront of optoelectronic innovation.

CSindustry awards2015

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Accessing the mid-infrared and beyond

Merging the quantum cascade laser and transistor promises new applications involving mid-infrared wavelengths through to terahertz frequencies

BY JOHN DALLESASSE AND KANUO CHEN FROM THE UNIVERSITY OF ILLINOIS AT URBANA-CHAMPAIGN

IT IS FAR FROM EASY to create a coherent source of emission between mid-infrared wavelengths and terahertz frequencies. But if success is possible, great rewards may follow – if these new devices could be commercially viable, they could serve new applications and open the door to new markets.

Many of the opportunities for frequency-tuneable sources in the mid-infrared and beyond are associated with identification of chemical species. Numerous substances have distinct molecular resonances in this spectral range, so frequency-tuneable sources could be used for chemical process monitoring, automotive applications, biomedical imaging and histopathology, chemical and explosive detection, greenhouse gas monitoring, ground and waste water monitoring, homeland security, and a host of other applications that rely on detecting the presence and quantity of a given chemical.

A frequency-tuneable source can be used to detect chemical species by sweeping its frequency so that it excites a molecular vibration. Hitting a frequency that causes molecules to resonate leads to the absorption of light, and this can be picked up by the dip in the response of a detector. To detect with the best signal-to-noise ratios, high-intensity, spectrally narrow, tuneable source are required.

Such sources are also preferred for imaging, with power changes in a detector array enabling spatial localization of compounds in various samples, including biological specimens. When imaging techniques with mid-infrared lasers identify cancerous cells, this approach can realise greater speed, accuracy, and resolution than conventional methods.

Another application for optical sources emitting from the mid-infrared to terahertz frequencies is point-to-point communication links. To serve

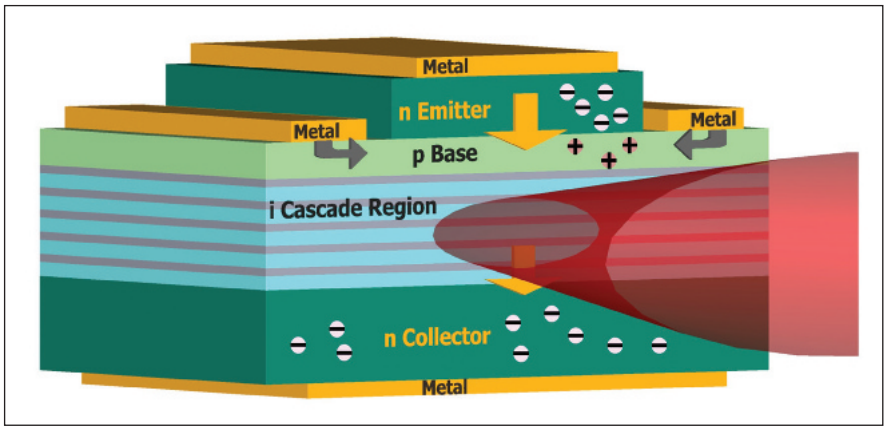


Figure 1. The transistor-injected quantum cascade laser is a three-terminal device that is designed to obtain coherent radiation from mid-infrared wavelengths through terahertz frequencies. This device utilizes the transistor effect and minority carrier injection to enhance the performance of the quantum cascade laser. Gold arrows show the electron flow through the structure, which is controlled by the grey hole flow into the p-type base.

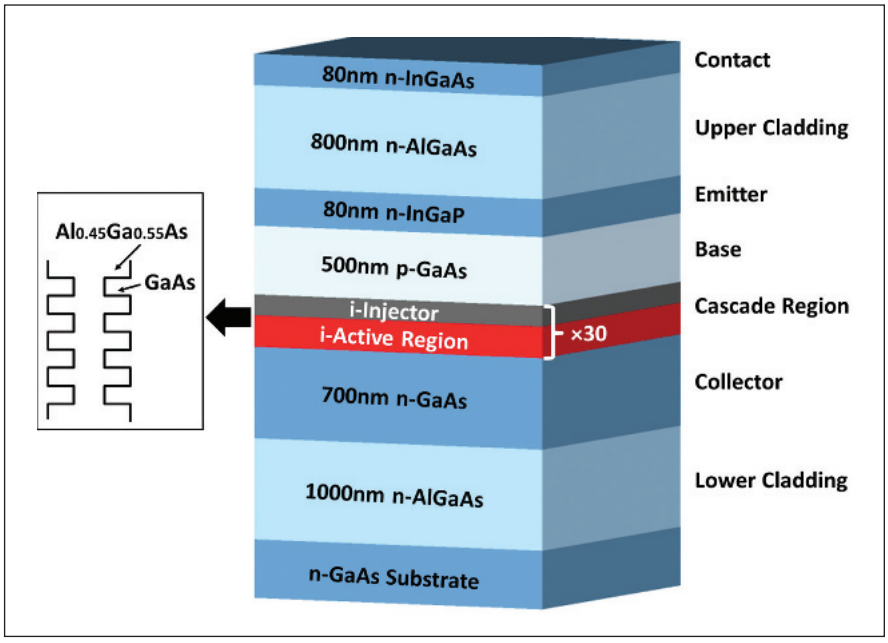


Figure 2. An example of a typical epitaxial structure for the TI-QCL. The collector contains low-refractive-index layers for optical-mode confinement. Within the base-collector junction is the quantum cascade gain region. Above the quantum transition region is a p-type, lightly doped base. Graded doping that increases near the emitter-base junction minimises free carrier absorption. The emitter itself is formed from InGaP to ensure a high emitter injection efficiency, and within the overall emitter structure are low refractive index layers to provide optical mode confinement. The entire structure is capped with a heavily doped n-type contact layer.

this, sources must be independently modulated in amplitude and frequency at high data rates.

For all the applications outlined above, the ideal source is compact and highly efficient, so that a battery can power it. Operation at typical ambient temperatures, without the need for cooling is also essential for widespread uptake in portable handheld systems, or in systems that are field deployed for environmental monitoring.

QCLs: Pros and cons

A great breakthrough that has paved the way to the realisation of practical sources in the mid-infrared and beyond came in 1994, with the development of the first quantum cascade laser (QCL). This two-terminal unipolar n^+-i-n device can generate photons with desired wavelengths if layer thicknesses are carefully engineered, and the applied voltage adjusted. Changing the voltage modifies the separation between the energy states, so it determines the emission wavelength and influences the rate at which these transitions occur, because the electron wavefunction in the cascade region is field dependent.

Thanks to the wavelength of the QCL being only loosely constrained by material parameters – and governed by the engineering of the layer thicknesses for a specific bias voltage – this class of laser has demonstrated emission over a very broad wavelength range.

Tuning emission through adjustments in voltage is an attractive feature of the QCL, but it comes at a price: changes in voltage also influence the lifetime of the photons. This means that when there are adjustments to the electric field across the cascade region, this changes both the shape of the electron wavefunction and the state energy, and because the QCL is two-terminal device, changes in output power follow. So in short, adjusting the applied voltage changes both the emission wavelength and the output power. Clearly this is undesirable, because in many applications it is preferable to fix the output power while adjusting the wavelength.

It is possible to see how to improve the QCL by examining the operation of the bipolar junction transistor (BJT). When formed as a *n*-*p*-*n* structure, the electrons in this class of device are injected from a forward biased *n*-p emitter-base junction into the base, before they diffuse across to the collector and are swept away by the field in the reverse-biased *p*-*n* base-collector junction. This chain of events occurs as the carriers take a random walk from the quasi-neutral base into the collector junction field region. The 'magic' of the BJT stems from the use of a small hole current into the base contact, which controls a large electron current sourced by the emitter and captured by the collector.

Our team at the University of Illinois at Urbana-Champaign has combined the attributes of the BJT with those of the QCL to form an innovative device that provides independent control of field across, and current through, the quantum transition region. With this novel, hybrid design, which we refer to as the transistor-injected (TI) QCL, the electric field controls wavelength while the current controls the laser power.

The TI-QCL is similar in design to the HBT (see Figure 1). Key differences are the addition of layers on the top and bottom of the device to provide optical confinement, the inclusion of the cascade region, and some variations in layer thicknesses and doping levels.

It is possible to fabricate our novel laser on a range of substrates. It can be grown on an *n*-type conductive substrate, with the collector contact made to the back of the wafer (see Figure 2, which shows a simplified epitaxial layer structure); and it can be formed on an insulating substrate, with all contacts made to the top surface. What's more, thanks to the similarity of the TI-QCL and the HBT, in terms of design and processing steps, it should be possible to produce this device in a commercial GaAs IC foundry.

The introduction of a third terminal offers plenty of freedom, in terms of device operation (see Figure 3 for a band structure diagram). Frequency modulation at fixed output power is possible by dithering the base-collector bias voltage while using a fixed emitter-base bias – adjustments to the voltage alter the slope of the bands, and thus the transition energy.

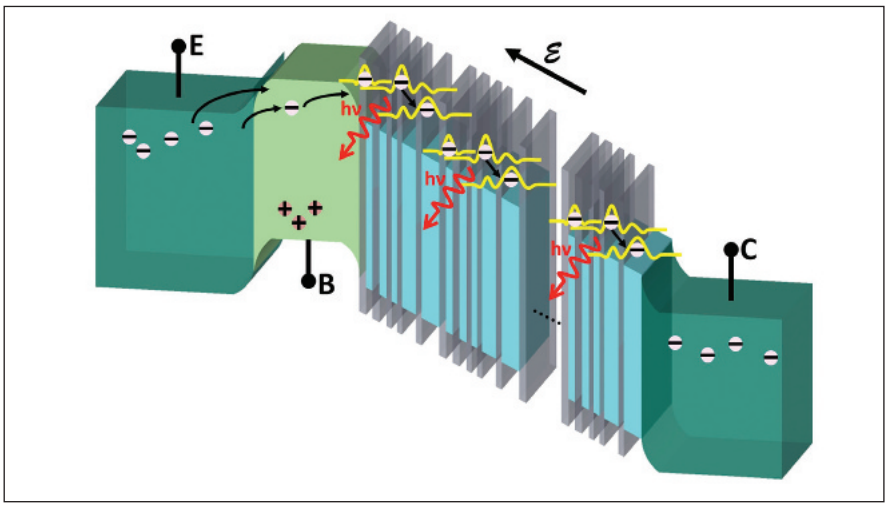


Figure 3. The band structure of the TI-QCL showing the emitter (E), base (B), and collector (C) contacts. In this n-p-n device, electrons are injected into the p-type base by the forward biased emitter-base junction and then diffuse across the base, before they are swept away by the field region in the reverse-biased base-collector junction. Within the field region of the base-collector junction, electrons travel through a staircase potential in discrete steps, emitting sub bandgap photons at a wavelength established by the design of the quantum wells and barriers as well as the applied electric field "ε" set by the base-collector bias.

Varying frequency while maintaining a constant output power is extremely useful for identifying chemical species. By sweeping frequency back and forth across a molecular absorption line at a fixed output power, enhanced signal-to-noise performance is possible, enabling superior detection of low concentrations.

Communications applications may also be targeted with our TI-QCL, because frequency modulation has the potential to be very fast, as it is based upon the electric field change in the structure. Amplitude modulation is also possible, due to modulation of the emitter-base bias. In this case, modulation rates are limited by transit times across the base and through the quantum transition region, so are slower than those resulting from frequency modulation. In addition, frequency and amplitude can be modulated independently, by adopting a common base configuration that provides separate control of the emitter-base and base-collector junctions.

A further benefit of our TI-QCL is its low internal loss, which stems from the *n*-*p*-*n* structure and the fundamentally different method of current injection. Losses due to free carrier absorption are minimal, thanks to the absence of doping from the cascade region and much lighter doping levels near the cascade region. Further improvements to internal loss result from the creation of a depletion region around the QCL structure in the regions of high optical field intensity where absorption is greatest.

Due to these refinements, there is the promise of a lower laser threshold current, an increased differential quantum efficiency and a hike in wall plug efficiencies. An increase in the latter is highly valued, because this is critical for portability and energy-sensitive applications.

Modelling the device

Device modelling is not trivial. To design a TI-QCL that works as intended requires modelling of the electron wavefunctions and energy levels under various electric fields, as well as modelling of optical modes and simplified modelling of the electrical transport characteristics.

Modelling of the electron wavefunctions and energy levels offers insights into laser properties, such as the gain characteristic.

Such calculations can reveal the voltage swing needed to produce a desired change in output frequency. Meanwhile, waveguide modelling allows engineering of the optical mode and an estimation of internal loss based upon free-carrier absorption. It is important to carry out this modelling for both the engineering of the epitaxial layer stack, and for determining the widths of the emitter and base mesa, which control lateral mode confinement. The last aspect of modelling, that of the electrical transport characteristics, is performed to enable a prediction of the current-voltage characteristic of the device.

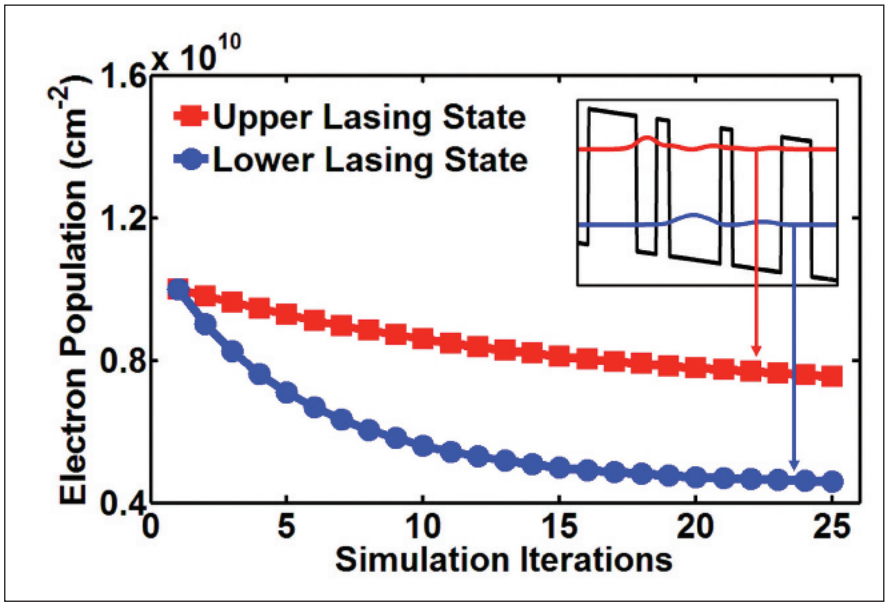


Figure 4. Modelling results reveal the electron sheet density in the two most important states for lasing action – the upper and lower lasing states. The simulation shows convergence toward an electron population that is higher in the upper lasing state than the lower lasing state – a necessary condition for laser operation.

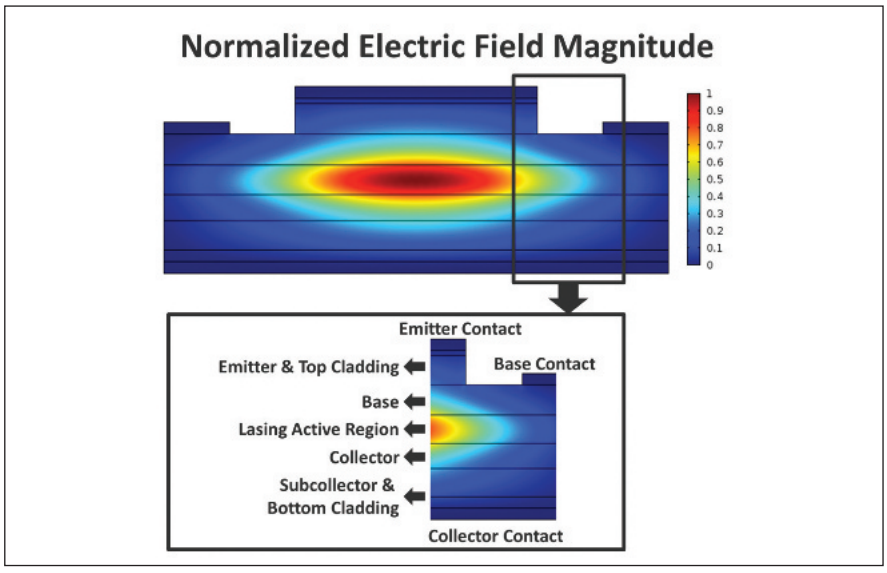


Figure 5. Two-dimensional optical waveguide modelling of the TI-QCL showing mode confinement provided by the upper and lower cladding layers, as well as the emitter ridge. The confinement factor and the layer doping levels are used to provide an estimate of the optical losses due to free carrier absorption.

So far we have only published results from device modelling, due to an initial focus on design and concept validation. To prove that our device is capable of fulfilling its promise, is must be capable of generating stimulated emission, which requires a population inversion – the presence of more carriers in the excited state than the ground state.

Calculations of electron wavefunctions have enabled us to determine state transition rates, and from this state population densities. The good news is that the population densities for the two most important states for lasing action converge to values that will allow a population inversion (see Figure 4). We have also undertaken waveguide modelling for our laser design, determining the expected mode profile (see Figure 5). Further data showing device operation is being prepared and will be soon be published.

The great potential of our device, and the encouraging preliminary results from our modelling efforts, are providing motivation for us to continue to pursue the development of a TI-QCL. Supported by funding from National Science Foundation, we will focus on device design refinement, fabrication, and characterization, with the primary goal of achieving a performance suitable for portable systems. This system-enabling work will focus on design iterations to improve device performance, demonstrate operating wavelengths that extend through terahertz frequencies, show extended tuning range, and expand the ability to modulate at high speeds.

Beyond this initial device-level work, we will explore, in collaboration with partners, the use of our novel QCL in specific applications such as chemical sensing and biomedical imaging. We look forward to a future where these devices are broadly deployed to help maintain air and drinking water quality, ensure process efficiency in chemical and semiconductor manufacturing, and help provide early detection of illnesses such as cancer.

Laser-lift off for ultraviolet LEDs

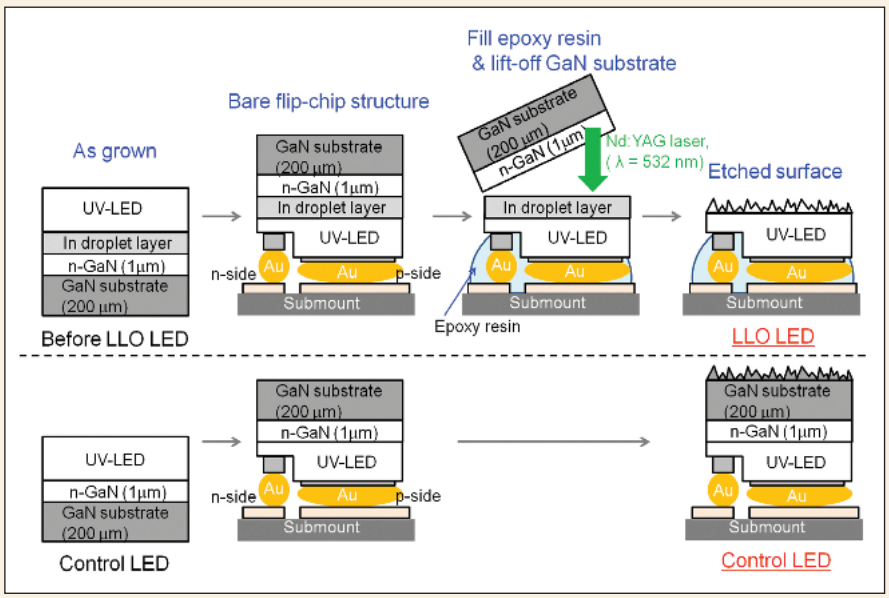
A superlattice built by pairing InGaN with GaN allows laser-lift off of an ultraviolet LED from its light-absorbing, native substrate

THANKS TO A NOVEL laser-lift off technique, a team from Meijo University in Japan has fabricated an ultraviolet LED that combines high-crystal quality with low levels of substrate absorption.
To produce this device, the researchers began by forming a 380 nm LED on a native GaN substrate. By subsequently removing this foundation, which absorbs emission, output increased by 70 percent.
GaN is not the conventional substrate for ultraviolet LEDs emitting around 380 nm. Sapphire is far more common, because a well-established technique exists for separating this foundation from the device layers.

This widely used approach begins by directing the emission from a high-energy pulsed ultraviolet laser, such as a 248 nm KrF pulsed excimer laser, through the substrate's backside. Strong light absorption occurs in the GaN next to the sapphire, with the wide bandgap material decomposing to induce the formation of gallium droplets. It is then easy to remove the device from its substrate. Note that any roughening of the GaN that occurs during this step may be beneficial, because it increases light extraction from the chip.

Sapphire substrates are not ideal for making ultraviolet LEDs, because they are not perfectly lattice-matched to GaN, so there is a high level of defects in the epilayer, impairing the internal quantum efficiency. Switching to a native substrate improves efficiency, but laser lift-off is harder, because the absorption properties of the substrate are essentially the same as the initial GaN device layers.

To overcome this lack of contrast in absorption, the team from Meijo University inserted an InGaN-GaN superlattice underneath the device structure. During growth of subsequent layers at 1040 °C, this composite decomposes to form a layer of indium droplets, which absorb visible and infrared radiation due to surface plasmon resonance. The researchers exploited this resonance, directing the emission from a 532 nm laser at the epiwafer, with



Substrate removal is possible by using a superlattice with eight pairs of $Ga_{0.85}In_{0.15}N$ and GaN. This composite converts to a layer with indium droplets after the growth of additional material at 1040 °C. Light extraction is increased by etching the surface with hot potassium hydroxide.

absorption of light in the indium droplet layer leading to separation of the device from the substrate (see Figure 1). This approach is very promising, because it could allow re-use of GaN substrates in ultraviolet LED fabrication, trimming production costs associated with this technique.

Ultraviolet LEDs were formed by taking a native substrate with a threading dislocation density of less than 10^6 cm^{-2}, and depositing on this a: 1 μm-thick layer of *n*-type GaN; a superlattice with eight pairs of $Ga_{0.85}In_{0.15}N$ and GaN; another 1 μm-thick layer of *n*-type GaN; a 2 μm-thick, n-type layer of $Al_{0.03}Ga_{0.97}N$; a ten-period superlattice with 2 nm-thick alternating layers of $Ga_{0.97}In_{0.03}N$ and GaN; a multi-quantum well with 6 nm-thick layers of $Ga_{0.95}In_{0.05}N$ and 15 nm layers of GaN; a *p*-type, 20 nm-thick electron-blocking layer made from $Al_{0.13}Ga_{0.87}N$; and a 120 nm-thick, *p*-type GaN contact layer. The team also produced a control, which differed due to removal of the first superlattice and a 1 μm-thick layer of *n*-type GaN. Flip-chip LEDs were formed from these epiwafers. Devices had dimensions of 500 μm by 600 μm and were mounted on sub-mounts with gold bumps. Gaps between the chip and the sub-mount were filled with an epoxy resin. Cathodoluminescense revealed that inserting the superlattice beneath the device increased threading dislocation density from 3 x 10^6 cm^{-2} to 5 x 10^7 cm^{-2}.
"We believe that the epilayer can be of lower defect density after optimization of the indium droplet layer," claims Daisuke Iida from Meijo University.

Measurements of light output revealed that once the LED had been separated from a 200 μm-thick GaN substrate, it had a 70 percent higher output at a 50 mA.
"We didn't optimize the growth condition and structure for our LEDs," admits Iida, which explains why they produced a inferior performance to devices emitting at similar wavelengths made by other groups.
One of the aims for the team is to now see how many times it is possible to re-use the GaN substrate during ultra-violet LED fabrication.

D. Iida *et. al.* App. Phys. Lett. **105** 072101 (2014)

Dislocation-free GaAs on silicon offers a route for scaling CMOS

Etching silicon to create a trench with silicon {111} planes enables the growth of dislocation-free GaAs

MAINTAINING THE MARCH of Moore's Law throughout this decade and beyond will require a switch from silicon channels to those sporting higher mobilities. Making this modification will allow devices to maintain their speed while working at a lower operating voltage, and will ultimately enable a scaling of power consumption per transistor.

III-Vs are very promising candidates for realising higher electron mobilities, but forming them on silicon substrates – the only platform suitable for microprocessor manufacturing – is very tricky, due to lattice mismatches and differences in polarity between the two types of material. However, success is possible, according engineers from imec. This team has developed a reproducible process for forming dislocation-free, 40 nm-wide GaAs trenches with good uniformity across 300 mm silicon substrates.

According to corresponding author Weiming Guo from imec, although the academic literature contains reports of III-V material with small dimensions integrated on silicon, it is rare to find a description of a procedure suitable for industrial mass production. "Our work reveals an interesting way towards this goal."

Using GaAs, rather than InP, as a foundation for transistors may raise a few eyebrows, as the standard structure for a III-V FET is an InGaAs channel on an InP buffer. However, it is challenging to grow InP and related materials when dimensions are small, argues Guo. "Secondly, even if defect-free InP/InGaAs could be grown for a FinFET structure, intrinsic carbon doping during MOCVD growth of InP will make it *n*-type, and this causes a high leakage current in the transistor."

Turning to GaAs allows greater control of carbon doping. "Although carbon could not be completely avoided, because it is an intrinsic *p*-type dopant for GaAs, leakage due to this mechanism can be neglected," explains Guo.

Dislocation-free growth of GaAs is possible via deposition on the {111} planes of silicon

The team began with 300 mm on-axis (001) substrates, employing a standard shallow trench isolation scheme to create regions of silicon aligned along the <110> direction with a 40 nm width and a length of 10 μm. Etching these wafers in 5 percent tertramethylammonium hydroxide at 80 °C removed the silicon. Different etch rates on different crystal planes led to V-shaped groves at the bottom of the trench formed from intersecting silicon {111} facets.

Growing on these facets is highly beneficial on three counts: Nucleation of GaAs is easier on silicon (111) than silicon (100); the glide plane of lattice mismatch dislocation is parallel to the two V-shaped interfaces between GaAs and silicon; and with this geometry, dislocations are trapped at sidewalls, rather than propagating to the surface.

Before GaAs is deposited into the trenches, silicon wafers are cleaned with a method developed by Advanced Materials that removes the thin oxide layer formed when the silicon surface is exposed to air.

After this cleaning step the wafer is loaded into an Applied Materials MOCVD reactor, and using trimethylgallium and tertiarybutylarsine precursors, a GaAs buffer layer is grown at 400 °C, before the temperature is ramped to 580 °C and the trench filled with this alloy.

According to a variety of characterization techniques, the quality of the GaAs in the trench is very high. Scanning electron microscopy images reveal that the overgrown GaAs has clear facets and a smooth surface, indicating high-quality GaAs. Meanwhile, X-ray diffraction shows that the GaAs is fully relaxed and of good crystal quality – and transmission electron microscopy reveals an absence of boundaries between grains and phase domains.

The engineers have also scrutinized the trenches with scanning spreading resistance microscopy. The resistance of the GaAs in the trench is about two orders of magnitude higher than that of the substrate, which has a *p*-type carrier concentration of 10^{14} cm^{-2}. So, in other words, there is a very low concentration of electrically active silicon in GaAs, implying that if transistors were formed, current leakage through to the substrate would be minimal.

Attempts are now underway to reduce the width of the channel so that it is suitable for producing transistors at the 10 nm node.

"Success of selective III-V growth not only depends on growth parameters, but also on the quality of pre-growth patterning, thus you can imagine that it will need quite some work to obtain high quality material," says Guo.

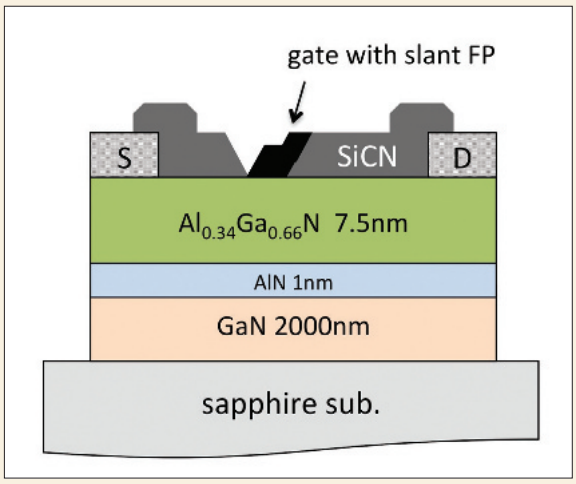
W. Guo *et. al.* Appl. Phys. Lett. **105** 062101 (2014)

Slanted field plates spawn superior HEMTs

Higher breakdown voltage and improved RF characteristics result from the introduction of slanted field plates

CALCULATIONS BY SEVERAL GROUPS have shown that switching from a conventional field plate to slanted variant (see figure) trims the peak electric field in a GaN HEMT, leading to improved device performance. Putting this theory into practice has not been easy, but a US-Japan team has just succeeded in this endeavor, with results validating the superiority of the slanted field plate.

What's more, this recent work shows that this form of field plate delivers better device performance than the common alternative, the multiple-field plate, which also cuts maximum electric field in GaN HEMTs.



HEMTs with a slanted field plates deliver a 66 percent increase in breakdown voltage compared with those employing a double field plate.

Team member Tetsuya Suemitsu from Tohoku University, Japan, argues that the weaknesses of the multi-field approach are not limited to inferior device performance – their fabrication requires two or more additional masks, depending on the number of the field plates employed. "This could be a penalty on cost, yield, and the turnaround time of the fabrication process."

In comparison, the approach adopted by Suemitsu, plus colleagues in his department and at engineers at MIT, is simple. It is also versatile, because it can be applied to conventional field plates, thereby allowing a systematic study of breakdown voltage with different plate geometries.

The approach of the US-Japan team involves the adoption of field plates as part of the gate metallisation process. The key to producing the slanted field plate is to control the mass flow ratio of carrier gases during plasma-enhanced CVD of the dielectric film. "This can be done by programing a recipe of the PECVD system," says Suemitsu.

Demonstration of the superiority of the slanted field plate begins with the growth of an AlGaN/GaN heterostructure on sapphire. This substrate is not as common a foundation as SiC and silicon for the production of GaN HEMTs. However, the team selected it because they view the AlGaN/GaN heterostructure on a sapphire substrate as the most conservative material system.

"In future study, we will use [SiC and silicon] substrates and more advanced heterostructures, such as an InAlN barrier, to show the impact of the slanted field plate on the state-of-the-art devices," says Suemitsu. "We believe that our slanted field plate process is applicable to any substrate and heterostructure."

Aside from the addition of the slanted field plate, GaN HEMTs were fabricated with standard processes. Ti/Au-based ohmic electrodes were formed by electron-beam evaporation and lift-off, before chlorine-based inductively-coupled plasma etching provided device isolation and ohmic annealing was undertaken.

Engineers used SiCN as the passivation film, depositing a 200 nm-thick layer while varying the ratio of the two carrier gases, hydrogen to ammonia. After defining gate patterns, etching vertically with hexafluoroethane and horizontally with sulphur hexafluoride yielded a slanted profile for the dielectric.

Adding gates of nickel and gold via evaporation, first with the sample pointing normal to the source and subsequently tilted, created slanted field plates with metal deposited only at the drain side of the sidewall.

Finally, reactive-ion etching exposed contact holes for ohmic electrodes, before Ti/Pt/Au probing pads were added by electron-beam evaporation and lift-off.

The team also formed a device without a field plate, plus those with two or three field plates, and compared the performance of all these transistors. The absence of a field plate led to a hard breakdown voltage of 83 V, while the addition of a slanted plate led to no hard breakdown up to voltages of 160 V. By defining an off-state breakdown voltage as the drain voltage at a drain current of 1 mA/mm, the slanted field plate design was shown to deliver a 66 percent increase in breakdown voltage compared with a double-field plate, and roughly a 30 percent increase compared with a triple-field plate.

RF performance also improved with the slanted field-plate: The maximum frequency for current gain was 28.8 GHz with this transistor architecture, compared with 12 GHz and 24.7 GHz for devices with two and three field plates, respectively.

Plans for the future include employing two-dimensional device simulation to optimise the design of the slanted field plate.

"We will also introduce advanced material systems such as InAlN/GaN heterostructures on SiC substrates, to push up the limit of the product of the cutoff frequency and breakdown voltage," says Suemitsu.

T. Suemitsu et. al.
Appl. Phys. Express **7** 096501 (2014)

Graphene unites silicon and GaAs

Ultra smooth GaAs films results from using graphene buffers on silicon substrates

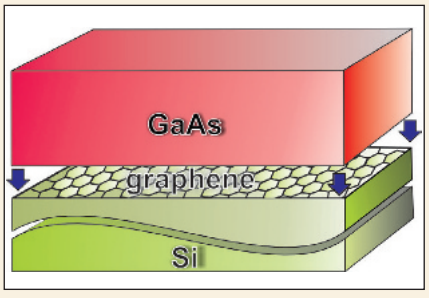
UC LOS ANGELES (UCLA) researchers, in collaboration with colleagues at UC Irvine and UC Riverside, have come up with a new way of depositing smooth GaAs films on silicon substrates using graphene buffer layers in between.

According to the researchers, the compatibility of their growth technique with current silicon planar CMOS technology presents an important step towards integrating electronics and photonics on the same chip. Applications such as photonic networks on chip, optical transceivers, free-space laser communications, and microwave photonics could benefit.

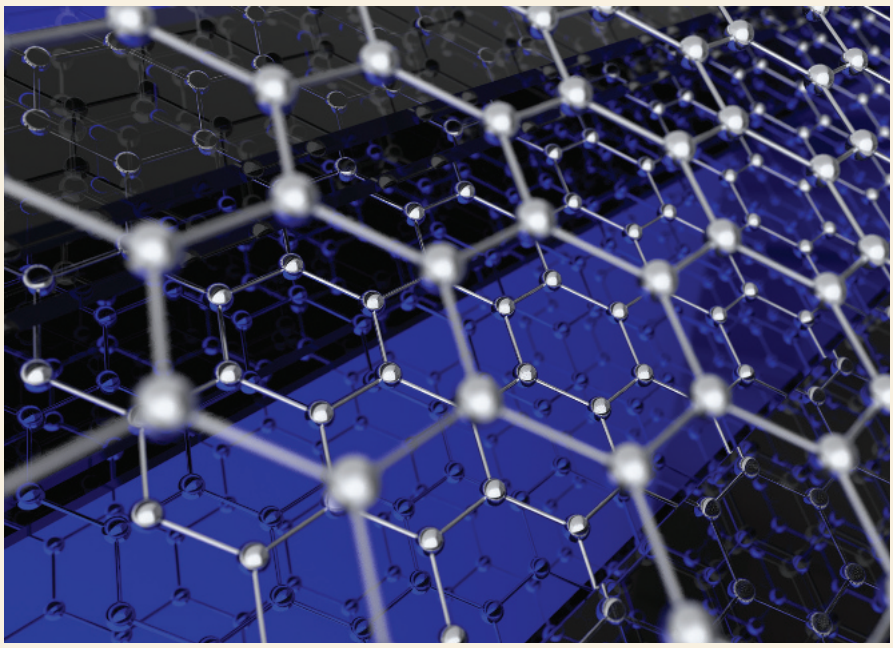
Led by Kang L Wang, the Raytheon Professor of Electrical Engineering at UCLA and the study's principal investigator, the group showed that ultra-smooth and epitaxial GaAs thin films can be deposited successfully on a growth-assisting graphene layer, which functions as a lattice-mismatch/thermal-expansion-coefficient-relieving layer.

The approach involves depositing hetero-layered GaAs by MBE on graphene-on-silicon under a constant arsenic flux at growth temperatures ranging from 350 °C to 600 °C.

The low energy of the graphene surface and the GaAs/graphene interface is overcome through an optimised growth technique, which includes initiating the growth with a gallium prelayer at room temperature. This increases the wettability of the graphene surface, facilitating the nucleation process.



A graphene interlayer enables the growth of high-quality, very thin films of GaAs on silicon substrates



In addition to the effect of the gallium prelayer, the growth rate was observed to have a significant effect on the surface morphology of GaAs. It turns out that a lower growth rate of GaAs yields a smoother surface. In this way, the researchers obtained an atomically smooth low-temperature GaAs nucleation layer.

A few experimental investigations have already been reported on the growth of GaAs nanowires on silicon using graphene. Nanowire on graphene, according to the researchers, is technologically easier to realise than smooth GaAs on graphene. Nevertheless, successful operation of nanowire-based devices is impeded by carrier loss mechanisms, surface-state induced band bending, Fermi level pinning, poor ohmic contacts, and uncontrolled incorporation of *n*- and *p*-type dopants.

These issues result in poor optoelectronic performance. In effect, nanowire-based devices have still has not turned out to be an alternative to their counterpart, smooth thin-film based devices.

The results by the West-coast researchers suggest the UCLA technique can be applied to other light-emitting III-V semiconductors such as InP and GaSb on silicon.

The team has overcome several material-related challenges in this work. Most significantly, while conventional direct heteroepitaxial deposition of GaAs on silicon requires the growth of 1 μm-thick GaAs to realise a certain material quality, the UCLA-led group's growth technique demonstrated that the same quality can be obtained by depositing only 25 nm of GaAs on top of silicon.

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