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Better models for efficient solar cells

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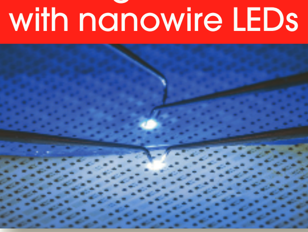
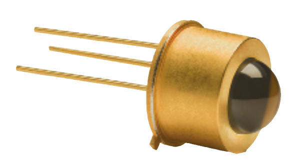
Seeking success with nanowire LEDs



Slashing the costs of GaN MMICs

Ultraviolet LEDs for analysing DNA



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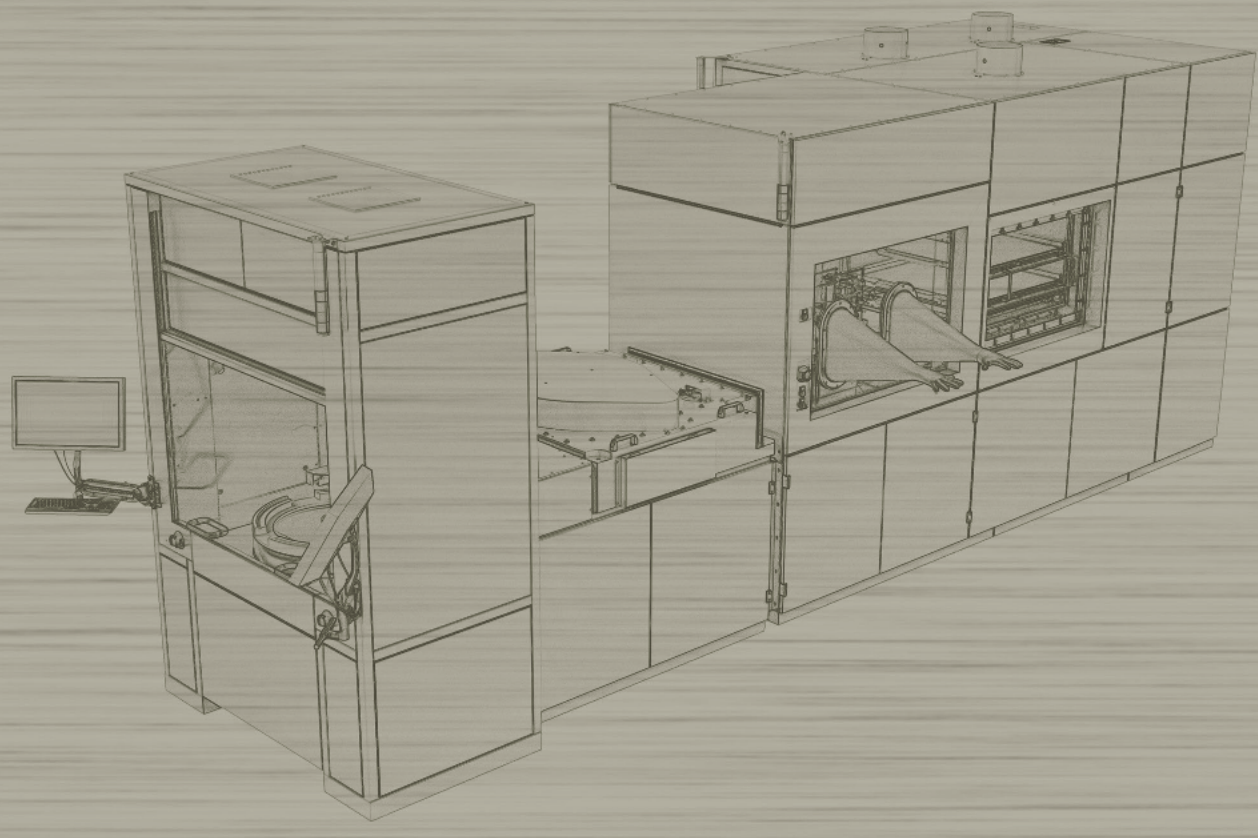

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Our technology. Your future.

editorial view

by Dr Richard Stevenson, Editor

The ultimate reward?

FOR THOSE OF US THAT LOVE OUR WORK, successes deliver tremendous rewards. After devoting years to cracking a tough and important problem, our triumph allows us to feel that all that time spent toiling away was more than worthwhile.

That warm glow of hard-won success will be well known to the pioneers of the blue LED. More than twenty years have passed since they got their devices to either emit light, or deliver a step-change in efficiency, but I suspect that they have no trouble in recollecting the buzz of excitement they had on those glorious days of yesteryear.

This autumn, three of the founding fathers of the blue LED – Isamu Akasaki, Hiroshi Amano and Shuji Nakamura – have been given an additional reason to feel proud of their successes. These three researchers have netted one of the greatest academic prizes of them all, the Nobel Prize for Physics (it was awarded 'for the invention of efficient blue light-emitting diodes which has enabled bright and energy-saving white light sources').

While I'm sure that these Nobel Laureates will welcome both the kudos and the share of the prize-money, I bet that they might derive even greater satisfaction from seeing the fruits of their labour all around them. As these trailblazers of the GaN LED go about their daily lives, they must get a great kick of satisfaction from seeing millions of us investing in solid-state lightbulbs and staring at LED-backlit screens.

Thanks in part to their efforts, the LED has evolved from a lab-based chip to a ubiquitous device. However, there is still much more work to do, given that solid-state lighting for all of humanity is still a distant dream. There may not be a Nobel Prize for doing this, but delivering reliable, affordable lighting to the third world is an achievement that should make any of us proud.

Going after this is a long-term goal for the French start-up Aledia, who describes their approach to LED manufacture in the feature *What is the best business model for nanowire LEDs?* on p.45 of this issue. Take a look and judge for yourself whether this is where the future of the LED lies.

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Compound Semiconductor is published eight times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £105.00/€158 pa (UK & Europe), £138.00 pa (air mail), $198 pa (USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher. Every effort has been made to obtain copyright permission for the material contained in this publication. Angel Business Communications Ltd will be happy to acknowledge any copyright oversights in a subsequent issue of the publication. Angel Business Communications Ltd © Copyright 2014. All rights reserved. Contents may not be reproduced in whole or part without the written consent of the publishers. The paper used within this magazine is produced by chain of custody certified manufacturers, guaranteeing sustainable sourcing.US mailing information: Compound Semiconductor, ISSN 1096-598X, is published 8 times a year, Jan/Feb, March, April/May, June, July, August/September, October, November/ December by Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Rd, Coventry CV5 6SP. UK. The 2014 US annual subscription price is $198. Airfreight and mailing in the USA by agent named Air Business Ltd, c/o Worldnet Shipping Inc., 156-15, 146th Avenue, 2nd Floor, Jamaica, NY 11434, USA. Periodicals postage paid at Jamaica NY 11431. US Postmaster: Send address changes to Compound Semiconductor, Air Business Ltd, c/o Worldnet Shipping Inc., 156-15, 146th Avenue, 2nd Floor, Jamaica, NY 11434, USA. Printed by: Pensord Press. ISSN 1096-598X (Print) ISSN 2042-7328 (Online) © Copyright 2014.

contents

CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY Volume 20 Issue 8 2014

features

41 III-Nitrides: Advances and controversy

Breakthroughs in power electronics, advances in ultraviolet emitters and new arguments associated with the debate on droop featured at the latest international nitrides meeting

45 What's the best business model for nanowire LEDs?

Should developers of nanowire LEDs seek success with devices sporting diminished droop? Or should they try undercutting the cost of incumbent chips?

50 Larger wafers slash GaN MMIC costs

High-quality wafers processed on a 150 mm GaAs fabrication line promise low GaN MMIC production costs

56 AlN substrates performance improvements in ultra-violet LEDs

Single-crystal, high-quality AlN substrates underpin the production of bright, reliable ultraviolet LEDs delivering superior wavelength stability

62 Improving modeling of high-efficiency solar cells

Analytical models accounting for reflections and photon recycling provide accurate predictions of device results

68 Trimming grid losses with SiC

Equipping the grid with SiC-based solid-state transformers will lead to more efficient delivery of better-regulated power

news

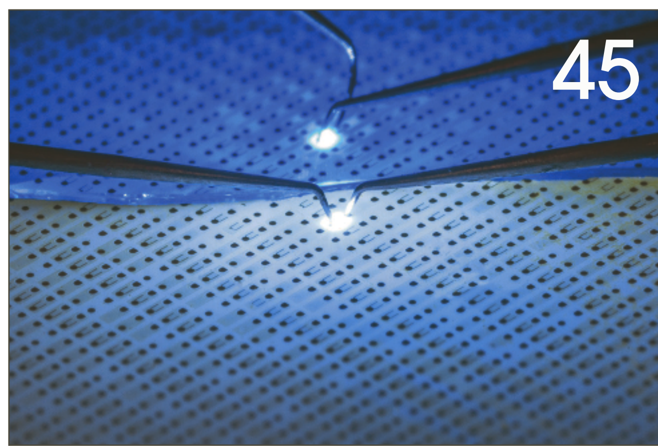
06 LED inventors win Nobel Prize
07 Samsung to scale back LED lighting
08 Nidec develop magnet-less motor drive with SiC inverter
09 Researchers develop new technique for analysing GaN
10 Veeco system speed transition from R&D to production
12 Record-breaking DARPA InP amplifier runs at 1012GHz
13 Plessey demonstrates large GaN-on-silicon LED capability
14 SiC and GaN to gain 13 percent of a $23B market
15 Rubicon reports decline in Q3 revenue

news analysis

20 Growing the terahertz transistor
22 All eyes on GaAs
24 Hybrid hope
26 Big Blue ambition
28 RFMD-TriQuint finish on a quarterly high
30 Reactor start-up to exploit research markets

research review

75 GaN: Building better transistors
76 Wafer bonding offers a route to high efficiency solar cells
77 Green lasers thrive with interfacial misfit dislocations



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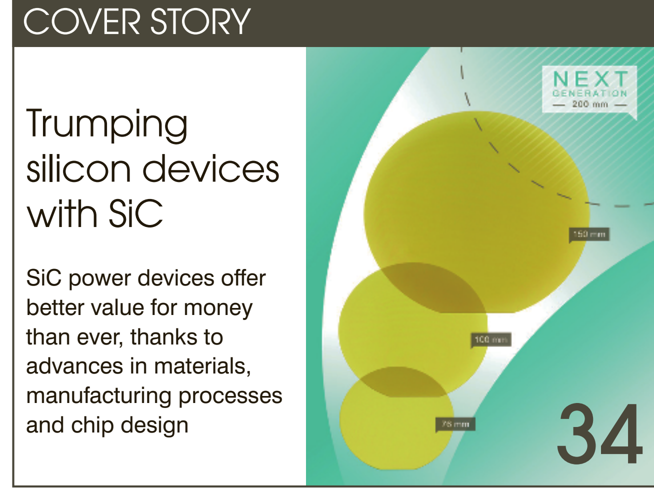


Trumping silicon devices with SiC

SiC power devices offer better value for money than ever, thanks to advances in materials, manufacturing processes and chip design

LED inventors win Nobel Prize

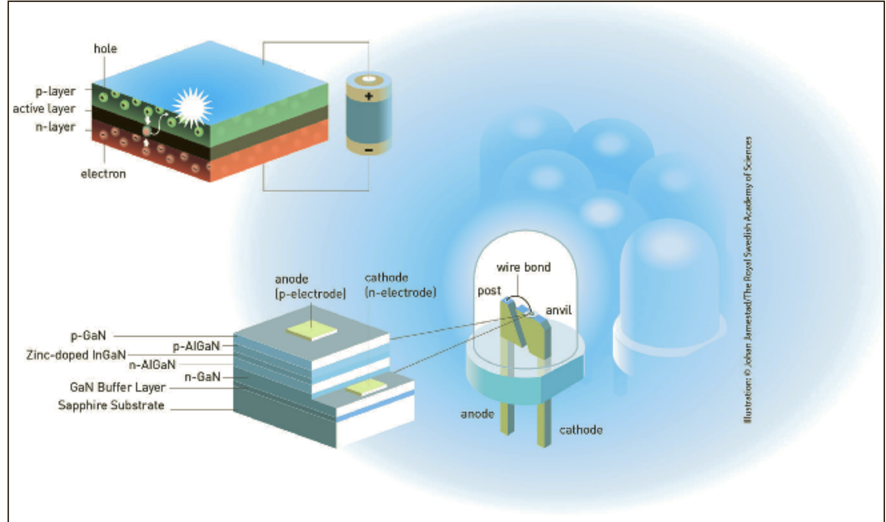
ISAMU AKASAKI, Hiroshi Amano and Shuji Nakamura have been awarded the 2014 Nobel Prize for Physics for their invention of the blue LED. Akasaki and Amano carried out their pioneering work together at Nagoya University while Nakamura was employed at Nichia Chemicals, a small company located in Tokushima on the island of Shikoku.

GaN was the material of choice for all these three researchers. Early on, the material was considered appropriate for producing blue light, but practical difficulties had proved enormous. No one was able to grow GaN crystals of high enough quality, since it was seen as a hopeless endeavour to try to produce a fitting surface to grow the GaN crystal on. Moreover, it was virtually impossible to create *p*-type layers in this material. Nonetheless, Akasaki was convinced by previous experience that the choice of material was correct, and continued working with Amano, who was a PhD-student at Nagoya University. Nakamura also chose GaN before the alternative, zinc selenide, which others considered to be a more promising material.

In 1986, Akasaki and Amano were the first to succeed in creating a high-quality GaN crystal by placing a layer of AlN on a sapphire substrate and then growing the high quality GaN on top of it. A few years later, at the end of the 1980s, they made a breakthrough in creating a *p*-type layer. By coincidence Akasaki and Amano discovered that their material was glowing more intensely when it was studied in a scanning electron microscope. This suggested that the electronic beam from the microscope was making the *p*-type layer more efficient. In 1992 they were able to present their first diode emitting a bright blue light.

Nakamura began developing his blue LED in 1988. Two years later, he too, succeeded in creating high-quality GaN. He found his own way of creating the crystal by first growing a thin layer of GaN at low temperature, and growing subsequent layers at a higher temperature. Nakamura could also explain why Akasaki and Amano had succeeded with their *p*-type layer: the electron beam removed the hydrogen that was preventing the *p*-type layer to form. For his part, Nakamura replaced the electron beam with a simpler and cheaper method: by heating the material he managed to create a functional *p*-type layer in 1992. Hence, Nakamura's solutions were different from those of Akasaki and Amano.

During the 1990s, both research groups succeeded in further improving their blue LEDs, making them more efficient. They created different GaN alloys using aluminium or indium, and the LED's structure became increasingly complex. Akasaki, together with Amano, as well as Nakamura, also invented a blue laser. Since blue light has a very short wavelength, it can be used store four times more information than with infrared light associated with a CD. This increase in storage capacity quickly led to the development of Blu-ray discs with longer playback times, as well as better laser printers.



Military growth for GaAs chips

BETTER THAN commercial market, growing momentum behind the use of solid-state technologies in radar, electronic warfare, communications and other systems will drive increased demand for GaAs devices through 2018.

According to the Strategy Analytics Advanced Defense Systems (ADS) service report, 'GaAs Industry Outlook 2013-2018' predicts that GaAs device demand from the defense sector will grow at almost three times the growth rate for the commercial GaAs device market. The military GaAs device market will grow at a CAGR (compound annual growth rate) of nearly 13 percent, exceeding over half a billion dollars by 2018. While GaAs devices are used in Electronic Warfare (EW) and smart munitions applications, the communications and radar applications will drive the bulk of demand. The largest usage of GaAs devices will continue to come from radar applications which will account for over 60 percent of the merchant GaAs military market revenue.

"Changing battlefield philosophies including a shift toward more asymmetric conflicts will place a premium on electronic capabilities," noted Asif Anwar, Director of the ADS service. "GaAs devices have traditionally played an important role in defense applications and future system requirements are driving increasing demand for solid-state solutions which will propel demand for GaAs devices as well as other compound semiconductor technologies."

"GaAs will also continue to be an enabling technology for commercial markets with increasingly sophisticated smartphones ramping up GaAs device content as well as growth in non-cellular markets," commented Eric Higham, North American Director for ADS. However, there will be serious challenges in the future as increasing competition from technologies like silicon and GaN.

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Samsung to scale back LED lighting

SAMSUNG ELECTRONICS will cease its LED lighting business outside of South Korea, scaling back what was identified as a key growth business four years ago, according to a news report by Reuters. LED, rechargeable cells for hybrid electric cars, solar cells, medical devices and biopharmaceuticals were five areas singled out by the Samsung Group in 2010 as new growth drivers. At the time, the group forecast the businesses would generate £29.5 billion in annual revenues by 2020 for its affiliates including Samsung Electronics.

But, says the Reuters report, Samsung Electronics has struggled to gain traction in the LED lighting market, failing to loosen the grip of established rivals such as Philips and Osram in advanced markets while facing mounting margin pressures from Chinese competitors in emerging markets. Samsung Electronics will remain active in the LED industry through the LED component business, focusing on areas such as backlighting for displays of consumer products like televisions. "In recent weeks, news had been circulating that Samsung was planning to announce it would leave the LED lighting business altogether," said Stewart Shinkwin, market analyst for lighting & LEDs at IHS Inc in a recent research note. "While the new development stopped short of a complete divestment with Samsung continuing to keep its LED luminaire business, the news is proof that increasing competition from lower-priced Chinese competitors is making the overall LED market less profitable for most manufacturers, ".

According to Shinkwin, the LED luminaire (fixture) market has not seen the same price competition that has plagued the LED lamp market. LED luminaire manufacturers have managed to maintain higher margins as products are more differentiated. "For all its heft, however, Samsung has not also been able to benefit from its vertically integrated

supply chain, in which the company provides components for its own internal divisions to market to external markets." A few years ago, the low-priced products from the Chinese were generally of inferior quality in terms of lifetime, efficiency and colour rendering, says Shinkwin. But the LED lamps from China today are comparable in performance while remaining significantly cheaper, forcing many high-end LED lamp manufacturers to drop prices significantly and to accept lower margins. The margins, in turn, have now become unsustainable for a number of suppliers.

Osram achieves record figures with green LEDs

THE Hi-Q-LED project funded by Germany's Federal Ministry of Education and Research (BMBF) has made pioneering advances with green LEDs, diminishing what is known as the 'green gap' phenomenon - the significant drop in efficacy in the green spectral range. The result is a green-emitting InGaN LED which achieves 147 lumens per watt at a wavelength of 530 nm and a spectral width of 35nm. In addition, another green LED developed by combining a blue chip with a phosphor converter, has achieved a record-breaking efficacy exceeding 200 lm/W.

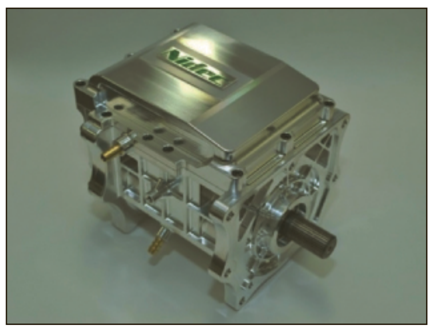
As part of the LED Lead Market Initiative funded by the BMBF, the working group for Efficient LED Solutions with High Colour Rendering Indices in the 'Hi-Q-LED' project headed by Osram Opto Semiconductors has developed two ground breaking green LED prototypes. Green all-InGaN LEDs close the 'green gap' Conventional LEDs show a significant efficacy drop at wavelengths above 500 nm - a phenomenon known as the 'green gap'. Research activities in the framework of the project have enabled the development of a narrowband green

LED with a record efficacy of 147 lm/W for a chip size of 1 mm^2 and a driving current of 350mA (current density: 45 A/cm^2).

The LED has a central wavelength of 530nm and a forward voltage of 2.93 V at this current density. A reduction of the carrier density in the light-emitting layers and a significantly improved material quality were the key factors behind this breakthrough. Thanks to a significantly reduced dependency of the efficacy on the operating current compared to conventional green LEDs, the LED prototype shows significantly improved performance at higher current densities and achieves as much as 338 lumen at 125 A/cm^2. "InGaN-based LEDs, in which the light output is generated by an InGaN semiconductor exclusively, offer a much more narrowband emission with a spectral width of approximately 35nm compared to green LEDs that are based on phosphor conversion. This breakthrough is an enabling technology for highly efficient projection systems requiring a high color rendering index", said Andreas Löffler, project manager at Osram Opto Semiconductors. A high colour rendering index or an increased colour gamut means a more vivid, higher-quality image.

The second approach of the project, which was to create a new, even more efficient green LED, comes into play in cases where the spectral bandwidth of the LED is not critical. Record-breaking figures demonstrated were 209 lm/W (210 lm) with a chip size of 1mm^2, a central wavelength of 540 nm, a forward voltage of 2.88 V and a driving current of 350 mA (current density: 45 A/cm^2). For a current density of 125 A/cm^2, it proved possible to increase the light output to above 500 lm. Despite this high current density, the efficacy of these devices amounts to 160 lm/W. The efficacy peaks at 1.5 A/cm^2 with a maximum of 274 lm/W.

Nidec develops first magnet-less motor drive with a SiC-based inverter



NIDEC CORPORATION has announced that its Research and Development Centre in Kyoto, Japan, has made the world's first concept model of a drive system using a magnet-less motor with a SiC based inverter.

The Nidec Research and Development Centre's lightweight motor drive system, takes up 32 percent less volume and is 69 percent lighter than a conventional motor drive system, including motor and inverter. It is expected that the characteristics of lower power losses will contribute to reducing power consumption. The SiC power semiconductors used in the 44kW motor drive, liquid cooled concept model were developed through Nidec's participation in the Kyoto super-cluster program of the Japan Science and Technology Agency. This was supported by a number of universities working with corporations and public research organisations.

A core institution of the Kyoto super-cluster program is the Advanced Scientific Technology & Management Research Institute of Kyoto. The Nidec R&D Centre has made open innovation by joint collaboration with Rohm; with Nichicon; and with Kyoto, Osaka and Ritsumeikan Universities. It has also worked with Yokohama National University in the technology of thermal analysis for motor drive systems, including circuit simulation of the SiC based inverter. An integrated motor-drive system (in which the inverter is built inside the motor housing) will be developed in 2015.

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Connecting, informing and inspiring the compound semiconductor industry

Taiyo Nippon Sanso to install GaN MOCVD system at Epistar Corporation

TAIYO NIPPON SANSO (TNSC) will install its mass-production GaN MOCVD system UR25K (6 inch X 7 wafers) into Epistar for development of light emitting diodes grown on 6 inch sapphire substrates. TNSC have announced that with the two companies' foresight into the 6 inch LED market, TNSC will be working with Epistar to improve the hardware aspect of the equipment. TNSC announces that the two companies in the LED and MOCVD manufacturing industry, Epistar and TNSC respectively, hope to accomplish the goal of improving and developing 6 inch LED and mass-production MOCVD.

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German researchers develop new technique for analysing GaN properties

THE FRAUNHOFER INSTITUTE FOR LASER TECHNOLOGY ILT working closely with RWTH Aachen University's Institute of Physics (IA) has developed an analysis technology that, for the first time, allows the structural and electronic properties of GaN and GaN composites to be studied optically on the nanometer level.

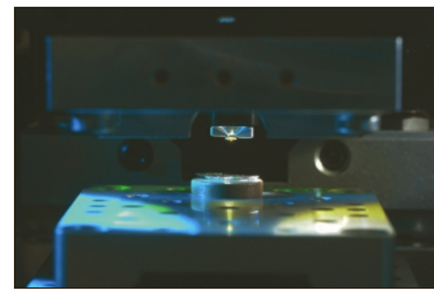
The resolution of conventional optical microscopes reaches its physical limits when confronted with objects on the nanometer scale. Because of the light source employed, structures in the nanometer range cannot be brought into focus. Near-field microscopy circumvents this limitation and penetrates the nanometer domain to provide an optical view. But this places extremely high demands on the light source used.

With fellow researchers from the Chair for Experimental Physics at RWTH Aachen University, scientists from Fraunhofer ILT have spent the past few years developing an innovative, broadband tunable laser system that is geared toward the particular requirements of semiconductor analysis at the nanometer level.

Wavelength can be adjusted to the material under inspection, which enables the new system to investigate a wide range of materials. In contrast to the solutions available on the market to date and those employed in research and development, the new system from Aachen provides the means for much faster spectroscopic analyses. It has also opened up access to material systems that were beyond the capacities of previous systems. This includes GaN and GaN composites.

Using the new analysis system, last year the researchers in Aachen were able to obtain an optical 2D image showing tensions in the crystal structure of undoped GaN wafers for the very first time. Computer simulations helped quantify the exact extent of the tension.

Recently the technique was also applied to a variety of doped GaN layers within complex structures. It's the first time an optical technique has been available to study the structural and electronic properties of GaN and GaN composites on the nanometer scale. (Pictured above is a near field microscope with a fragment of GaN wafer.)



Near-field microscopy offers cost and quality benefits over standard analysis techniques. The structural properties of thin GaN layers are currently studied using transmission electron microscopy; however, the costs incurred are extremely high, due in part to the laborious sample preparation process. Near-field analysis can usually be conducted without any preparation.

Another benefit concerns secondary ion mass spectrometry, which is used to study the electronic properties. Although this technique can be used to determine electronic properties along an axis at the nanometer level, it isn't yet possible to laterally ascertain the concentration of doping atoms at a comparable resolution. The technique also damages the samples.

In contrast, near-field microscopy offers nanometer-scale resolution in all dimensions. It is a completely non-destructive technique and can be implemented under normal conditions.

EPC Introduces 80 V monolithic GaN half bridge efficiency approaching 98 percent for power system designers

EFFICIENT POWER CONVERSION (EPC) has announced the EPC2105, 80 V enhancement-mode monolithic GaN transistor half bridge. By integrating two eGaN power FETs into a single device, interconnect inductances and the interstitial space needed on the PCB are eliminated, claims the company.

This increases both efficiency (especially at higher frequencies) and power density, while reducing assembly costs to the end user's power conversion system. The EPC2105 is ideal for high frequency DC-DC conversion and enables efficient single stage conversion from 48 V directly to 1V system loads.

The device offers power systems designers a solution that increases efficiency and power density for complete buck converter systems approaching 98 percent at 10A when switching at 300kHz and converting from 48V to 12V, and 84 percent at 14A when switching at 300 kHz and converting from 48 V to 1.0 V. Each device within the EPC2105 half-bridge component has a voltage rating of 80 V. The upper FET has a typical RDS(on) of 10mΩ, and the lower FET has a typical RDS(on) of 2.3 mΩ. The high-side FET is approximately one-fourth the size of the low-side device to optimize efficient DC-DC conversion in buck converters with a high VIN/VOUT ratio.

The EPC2105 comes in a chip-scale package for improved switching speed and thermal performance, and is only 6.05 mm x 2.3 mm for increased power density. The 2in x 1.5in EPC9041 development board is also available, containing one EPC2105 integrated half-bridge component using the Texas Instruments LM5113 gate driver, supply and bypass capacitors.

The board has been laid out for optimal switching performance and there are various probe points to facilitate simple waveform measurement and efficiency calculation.

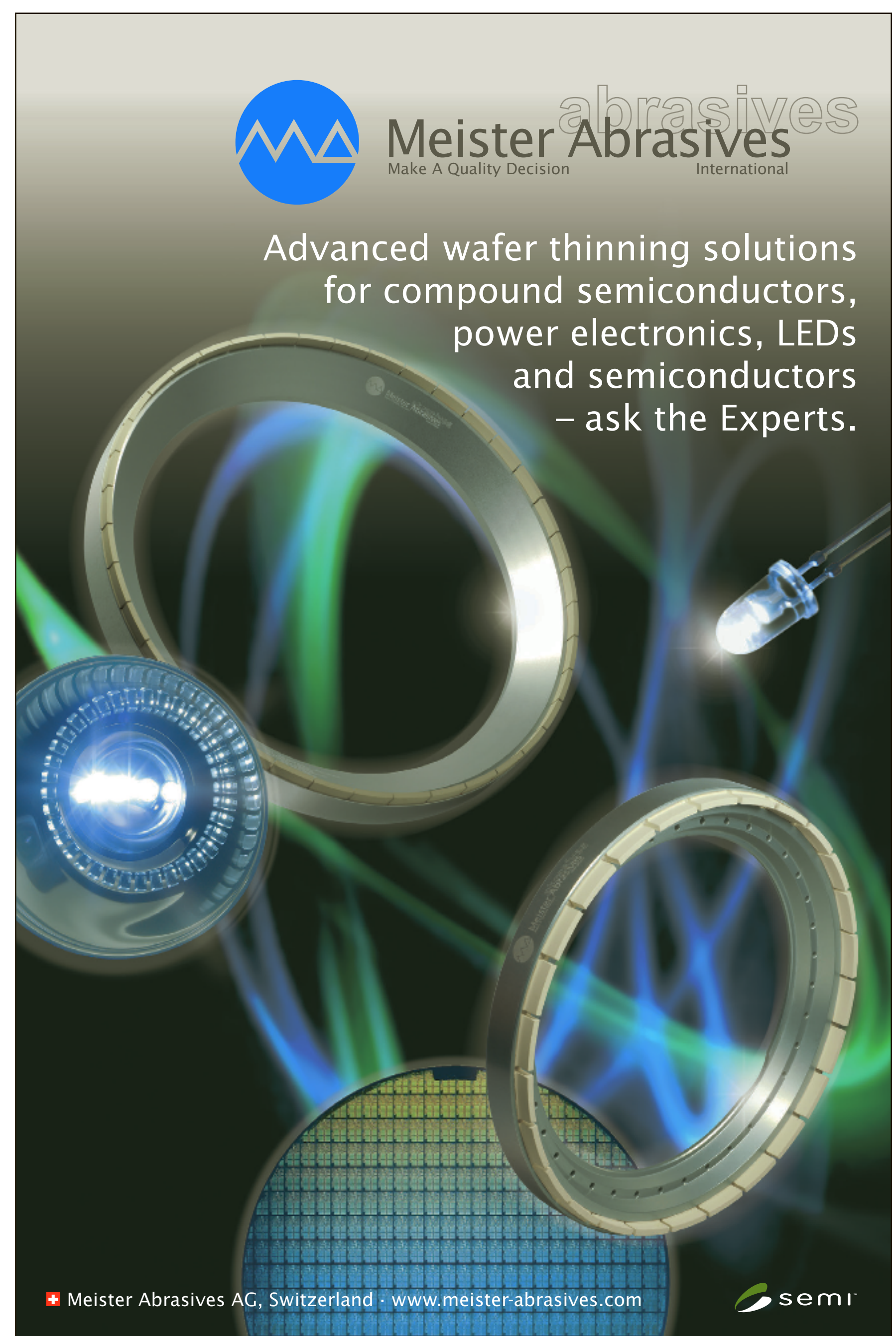
Veeco system designed to speed transition from R&D to production

VEECO INSTRUMENTS has introduced the Propel GaN MOCVD system, which incorporates single-wafer reactor technology to aid film uniformity, yield and device performance.

This new 200mm MOCVD system and technology enables the development of highly-efficient GaN-based power electronic devices that will accelerate the industry's transition from R&D to high volume production, says the company. Veeco's new Propel Power GaN MOCVD system is designed specifically for the power electronics industry.

Featuring a single-wafer 200mm reactor platform, capable of processing six and eight-inch wafers, the Propel Power GaN MOCVD system deposits high-quality GaN films that result in the production of highly-efficient power electronic devices. The single-wafer reactor is based on Veeco's leading TurboDisc design with technology including the new IsoFlange and SymmHeat technologies that provide homogeneous laminar flow and uniform temperature profile across the entire wafer.

Customers can transfer processes from Veeco K465i and MaxBright systems to the Propel Power GaN MOCVD platform.



"Leading power electronics manufacturers are currently progressing from R&D to pilot production, developing and qualifying novel device structures with a focus on improved reliability, yield and cost," said William J. Miller, executive vice president, Veeco.

"With its superior design, technology and performance, Propel is a platform that will provide exciting future growth opportunities for our customers and for Veeco."

The Propel MOCVD system is based on Veeco's MOCVD TurboDisc technology and features long campaign runs and low particle defects. In addition, the proprietary SymmHeat technology drives uniform thermal control for good thickness and compositional uniformity. Providing a seamless wafer size transition, the system deposits high quality GaN epitaxial layers on silicon wafers that are six and eight inches in diameter.

"Beta testing by power electronics industry leaders has shown that the Propel system is ideally suited for fast cycles of learning with excellent particle performance," said Jim Jenson, senior vice president and general manager of Veeco MOCVD.

"This validation is great news for customers as they work to develop innovative processes and technologies for their product roadmaps. As we've demonstrated in the LED industry, Veeco's goal is to help power electronics customers also improve device efficiency, reduce manufacturing costs, and ultimately move into high-volume manufacturing."

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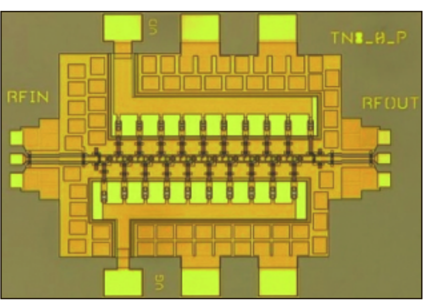
Record-breaking DARPA InP amplifier runs at 1012GHz

TERAHERTZ ELECTRONICS PROGRAM could pave way for new sub-millimeter wave applications DARPA's Terahertz Electronics program has created the fastest solid-state amplifier IC ever measured. The ten-stage common-source amplifier made from InP operates at a speed of one terahertz (1012 GHz) – 150 billion cycles faster than the existing world record of 850GHz set in 2012.



"Terahertz circuits promise to open up new areas of research and unforeseen applications in the sub-millimeter-wave spectrum, in addition to bringing unprecedented performance to circuits operating at more conventional frequencies," said Dev Palmer, DARPA program manager.

"This breakthrough could lead to revolutionary technologies such as high-resolution security imaging systems, improved collision-avoidance radar, communications networks with many times the capacity of current systems and spectrometers that could detect potentially dangerous chemicals and explosives with much greater sensitivity." Developed by Northrop Grumman Corporation, the InP Terahertz Monolithic Integrated Circuit (TMIC) exhibits a measured power gain of 9dB at 1.0 terahertz and 10dB at 1.03 terahertz. "Gains of six decibels or more start to move this research from the laboratory bench to practical applications-nine decibels of gain is unheard of at terahertz frequencies" said Palmer.

"This opens up new possibilities for building terahertz radio circuits." Current electronics using solid-state technologies have largely been unable to access the sub-millimeter band of the electromagnetic spectrum due to insufficient transistor performance. To address the 'terahertz gap' engineers have traditionally used frequency conversion-converting alternating current at one frequency to alternating current at another frequency-to multiply circuit operating frequencies up from millimeter-wave frequencies. This approach, however, restricts the output power of electrical devices and adversely affects signal-to-noise ratio. Frequency conversion also increases device size, weight and power supply requirements.

DARPA has made a series of strategic investments in terahertz electronics through its HiFIVE, SWIFT and TFAST programs. The objective of the Terahertz (THz) Electronics program is to develop device and integration technologies necessary to realize compact, high-performance electronic circuits that operate at center frequencies exceeding 1.0 THz.

Skyworks reports record Q4 results

SKYWORKS SOLUTIONS, the maker of analogue semiconductors, has reported its fourth fiscal quarter and year-end results for the period ending October 3, 2014. Revenue was $718.2 million, up 51 percent year-over-year and 22 percent sequentially, consistent with the updated outlook provided on October 14, 2014 and exceeding the company's original guidance midpoint of $680 million.

On a non-GAAP basis, operating income for the Q4 of 2014 was $235.7 million, up 81 percent from $130.3 million in the Q4 of 2013. Non-GAAP diluted earnings per share for the fourth fiscal quarter of 2014 was $1.12, including a $0.03 fiscal year-end tax benefit, compared to $0.64 for the prior year Q4.

On a GAAP basis, operating income for the fourth fiscal quarter of 2014 was $198.1 million and diluted earnings per share was $0.90. For fiscal year 2014, revenue was $2.3 billion, up 28 percent from fiscal 2013, while non-GAAP diluted earnings per share was $3.24, up 47 percent year-over-year. GAAP diluted earnings per share for fiscal 2014 was $2.38. "Skyworks is aggressively executing on our strategy to deliver sustainable, above market growth with diversified analogue semiconductor returns," said David J. Aldrich, chairman and chief executive officer of Skyworks.

Our advanced solutions are at the heart of mobile connectivity and the Internet of Things, and are empowering exciting new applications spanning mobile payments, to streaming music services, to on-demand media. Given our accelerating design win momentum and deep product pipeline, we have never been better positioned to grow demonstrably faster than our addressable markets and in turn, to deliver best-in-class financial returns.

"Fiscal 2014 was a record year for Skyworks as we exceeded key metrics in each and every quarter and crossed the $2 billion revenue threshold," said Donald W. Palette, vice president and chief financial officer of Skyworks.

Based on broad customer demand and crisp operational execution, we are now scaling to more than a $3 billion revenue run-rate with annualized non-GAAP earnings per share approaching $5.00. Specifically, for the first fiscal quarter of 2015, we anticipate revenue to be up 52 percent year-over-year to $770 million with further margin expansion yielding $1.18 of non-GAAP diluted earnings per share.

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Plessey demonstrates large GaN-on-silicon LED capability

PLESSEY have announced its capability to make large, high-performance, high-volume GaN-on-Si LED die. It has produced a 20 square mm die design that will generate up to 5W of blue light over a 400-480nm wavelength range, as a technology demonstrator.

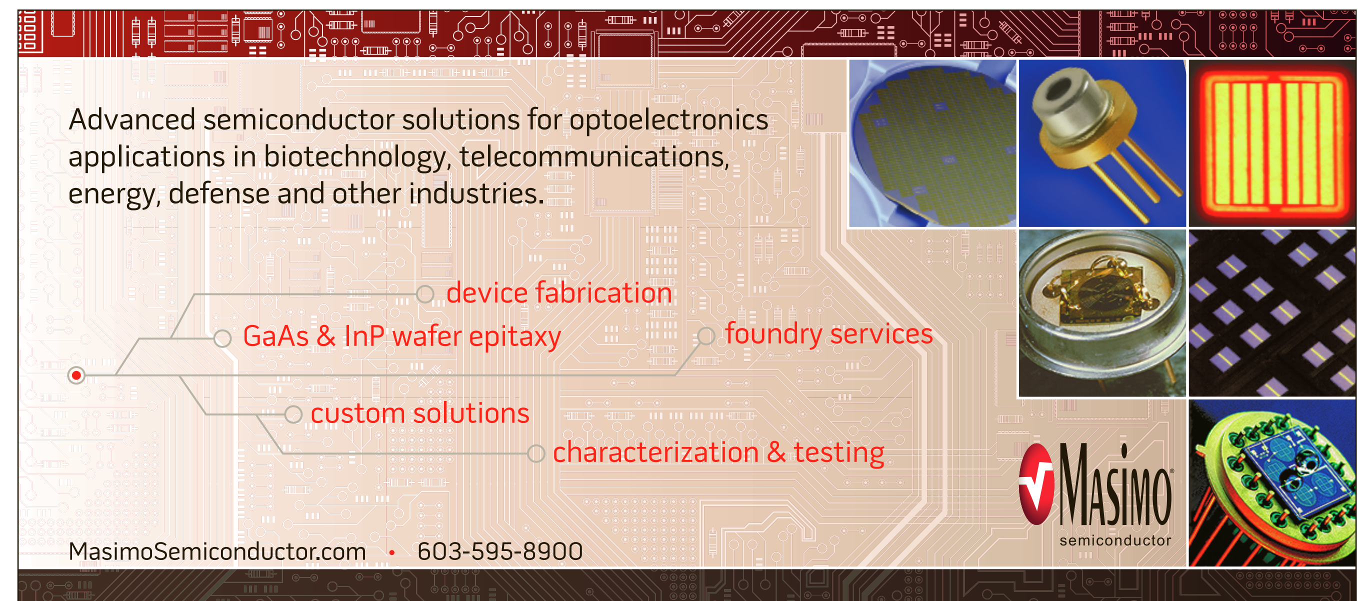
According to Plessey, this large die benefits from three features of the Plessey process; low thermal resistance of silicon; a single-surface, emitter die design; and 6-inch wafer processing. Large area LED die help customers in many ways, particularly for Chip-on-Board (CoB) products in providing a much simpler, more uniform light emitter whilst reducing die attach and wire bond overheads. The low thermal resistance of the silicon substrate makes for easier thermal management and enhanced reliability resulting from lower temperature operation. The die uses Plessey's vertical design structure that has a cathode top and anode bottom contacts, which is ideal for scaling the effectiveness in applying large die. And, with 6-inch wafer processing coupled with best-in-class across wafer uniformity, Plessey makes such large die a real commercial proposition.

David Owen, Plessey's marketing director, explains: "It is clear that the next wave of general lighting products will see LEDs applied in ways that truly exploit the benefits obtained through Plessey's leading GaN-on-Si technology. This announcement marks the start of a phase where we engage with our key partner customers in defining the commercial realisation of lighting products based on Plessey's large GaN-on-Silicon LED die."

Silvaco joins Japanese gallium oxide project

SILVACO JAPAN has joined Japan's Strategic Innovation Promotion (SIP) program project 'Research and Development on Fundamental Technologies of Gallium Oxide Power Devices'. Promoted by New Energy and Industrial Technology Development Organisation (NEDO), the project also includes the National Institute of Information and Communication Technology, Tamura Corporation, Tokyo University of Agriculture and Technology and New Japan Radio. Transistors and diodes with Ga_2O_3 - a new semiconductor material with wide band gap - are expected to have higher breakdown voltage, higher output and lower dissipation compared to traditional compound semiconductor devices. Moreover, it is theoretically possible with ß-Ga_2O_3 to create large diameter single crystalline substrates by melt growth method, at low energy and for a low cost, enabling production of bulk single crystal. These characteristics will have significant advantages for industrial applications.

The National Institute of Information and Communication Technology, Tamura and KOHA have already successfully developed the world's first MOSFET using Ga_2O_3. The SIP project's aim is to establish the fundamental technologies for Ga_2O_3 power devices by fiscal year 2018. "Silvaco has many years of experience in the development, sales and technical support of semiconductor process and device simulators," commented Iliya Pesic, President of Silvaco Japan. "Silvaco has key advantages in simulation technology for silicon and compound semiconductor power devices. Silvaco's leading edge technologies with proven performance in wide band gap semiconductors will enable it to make a significant contribution to the project."



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SiC and GaN to gain 13 percent of a $23B market

POWER ELECTRONICS will grow to a market worth $23 billion for discrete components in 2024, up 77 percent from $13 billion today according to Lux Research.

Silicon-based devices will remain the main technology of choice with an 87 percent share, but new SiC and GaN technologies will be the fastest-growing – at 30 percent and 32 percent annual rates respectively. Together, they will gain a combined 13 percent share in 2024.

"As power demands in applications from consumer electronics to the power grid get more demanding, silicon is running up against physical limits, offering opportunities for both SiC and GaN," said Pallavi Madakasira, Lux Research Analyst and the lead author of the report titled, 'Sizing-up the $23 Billion Discrete Power Electronics Market in 2024. GaN is a direct threat to silicon, as it can replace silicon in many applications, while SiC transistors can actually create additional new opportunities for silicon in high-voltage applications that will use SiC and silicon components together," she added. Lux Research evaluated the $23 billion market for discrete power electronics, assessing market drivers and diverse technologies. Among its findings are that consumer electronics and IT will account for 48 percent of the market in 2024, or about $11 billion.

Consumer electronics make up most of this segment, expanding from $7 billion in 2014 to $10 billion in 2024, driven by growth of low power tablet computers as well as ongoing popularity of mobile phones. The transportation market, worth nearly $1.2 billion in 2024, will be the big driver for both SiC and GaN. Transportation uses will account for 65 percent of the total market for SiC and 41 percent of the total market for GaN.

Notwithstanding their high growth rates, SiC and GaN remains a small total share of the market. For SiC, high costs will make SiC transistors less viable in many applications, while GaN's adoption will be held back by delayed product roll-outs and capacity expansions.

GaN-on-silicon LEDs offer better than 50 percent light output efficiency

PLESSEY has announced that its MAGIC GaN-on-silicon technology has successfully achieved light output of 120 Lumens per Watt with greater than 50 percent light output efficiency.

Plessey's first engineering samples in the 5630 PLCC2 package are now shipping with other package variants available on demand. Blue die with a wavelength of 455nm are also available and being shipped to lead customers.Keith Strickland, Plessey CTO, said: "Having developed and put into production the first of our MAGIC LEDs in 2013, the next step was to demonstrate that the GaN on silicon technology could deliver output performance levels comparable with other LED technologies.

"Whilst 120 Lumens per Watt for an LED may be considered 'acceptable' to industry, we must remember that we have doubled our LED light output in the past six months. I see no reason why we cannot reach state of the art in LED die output performance within the next six months. This current process technology will become the base for our Application Specific LEDs, the ASLED that bridges the gap between the LED component suppliers and the solid state lighting fixture designers and OEMs."

Mike Snaith, Plessey Operations Director, commented: "Achieving greater than 50 percent light output efficiency is a superb achievement for the team here in Plymouth. The combination of expertise and a sustained period of light output performance improvement in the core LED material is due to our holistic approach to LED development - our in-house experts in epitaxy growth, process development and die design all working together"

Rubicon reports decline in Q3 revenue

RUBICON TECHNOLOGY has announced third quarter revenue of $8.0 million, at the low end of its previous guidance range. Revenue declined by $6.5 million sequentially, of which $5.5 million was attributable to lower two-inch core sales in the period.

With the LED market migrating from two-inch to four-inch substrates, much of the remaining two-inch demand comes from the mobile device market. William Weissman, Rubicon's Interim CEO and CFO commented: "While usage of two-inch material for the mobile device market continued to grow in the third quarter, that demand was largely satisfied by the considerable inventory of two-inch material in the supply chain. In addition, there has obviously been capacity added in the marketplace this year to serve the mobile device market.

"As a result, there were limited opportunities to sell two-inch material in the quarter. However, we are seeing a meaningful increase in two-inch orders in the fourth quarter."

The company reported continued progress with the introduction of its patterned sapphire substrate (PSS) product. Mr. Weissman said: "While the progress in PSS is not yet meaningfully reflected in our revenue, we are now qualifying with nearly all of the world's top-tier LED chip manufacturers. The size of the orders from certain customers will begin to increase over the next six months as we progress from initial qualification toward full qualification with those customers. We expect production orders by mid next year and, based on the progress we are making, we believe that our PSS capacity should be fully utilised by the end of next year."

GAAP loss per share in the third quarter was $0.53 and included certain non-cash charges, the majority of which were associated with changes made to the company's polishing platform in order to reduce product costs. Excluding these non-cash charges, non-GAAP loss per share was $0.36 in the third quarter, as compared with the company's guidance of a per share loss of between $0.39 and $0.44, due to a combination of reduced product costs and product mix.

Commenting on the outlook for the fourth quarter of 2014, Mr. Weissman said: "We expect continued progress in growing the wafer business, particularly with PSS wafers. We are seeing improvement in the two-inch market, however, pricing remains very challenging.

Although the pricing environment improved in the first half of the year, the excess supply of two-inch in the third quarter drove pricing for two-inch core 30 percent lower than the previous quarter.

Plessey show large GaN-on-Si die

PLESSEY presented the results of its partnership with Litecool, a Sheffield-based thermal solutions provider, to visitors during LuxLive in November. Plessey showcased its large area LED die assembled in the Litecool MicroSpot product. Litecool develops and manufactures heat management solutions for LED lighting products. Its LED module allows the LED diodes to be mounted directly on to the heat spreader without anything underneath to obstruct the escaping heat. This offers lighting product designers an LED module that stays cooler allowing the use of smaller, lower cost heat sinks, according to the company.

The Plessey large area LED die is a 4.5 x 4.5mm design that will generate up to 5W of blue light over a 400-480nm wavelength range based on its GaN-on-Silicon MaGIC LED technology. Litecool has packaged the Plessey's single source LED emitter into its 10W MicroSpot package with the thermal resistance (junction to heat sink) of just 0.7C/W, producing a beam angle of 18 degrees and a luminance size of 42mm.

Litecool's CEO, James Reeves, said: "We have used our latest generation of technology to ensure ground breaking thermal resistance for this unique package. This powerful single source emitter works exceptionally well with secondary optics and with our technology keeping it cool. I can see this being a hit in the spotlight market where high lumen density is essential."

David Owen, Plessey's marketing director said: "Plessey's technology has already shown how we can overcome what up to now has been a significant cost barrier in large-scale LED illumination. The use of Litecool's LED module technology enables us to maintain the lumen density not just at source but at luminaire level - a 10W spotlight that is just 42mm in diameter."

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Connecting, informing and inspiring the compound semiconductor industry

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A selection of the 35+ presentations over two days covering six themes

SOLID-STATE LIGHTING

Soaring sales of LED bulbs are creating a great opportunity for chipmakers. But what do companies need to do to stand out from the crowd and win substantial orders while maintaining healthy margins?

KEYNOTE	Opportunities for laser diodes in solid-state lighting **Jon Wierer - SSLS Scientist - Sandia National Laboratories**	Sandia National Laboratories
ANALYST	How will the solid-state lighting evolution unfold, and what will it mean for the LED chipmakers? **Stewart Shinkwin - Market Analyst, LEDs and Lighting - IHS Technology**	IHS
SPEAKER	Commercialisation of GaN on Silicon for LEDs **Keith Strickland - Innovations & Technology Director - Plessey Semiconductors**	plessey
SPEAKER	Increasing LED output with advanced plasma processing **Mark Dineen - Product Manager - Oxford Instruments**	OXFORD INSTRUMENTS The Business of Science
SPEAKER	Lowering LED epitaxial wafer cost through AlN transition layers using PVD **Scott Kroegar - Vice President, Product Commercialization - Deposition & SiC - GT Advanced Technologies**	GT ADVANCED TECHNOLOGIES
SPEAKER	Yield optimization of compound semiconductor processes through an effective metrology strategy **Torsten Stoll - Product and Marketing Manager - Nanometrics**	nanometrics
SPEAKER	Plasma dicing for III/V and thin wafers **Reinhard Windermuth - Sales Manager - Panasonic Factory Solutions**	Panasonic Factory Solutions Europe

OPTOELECTRONICS

Does the growth of the datacom market signal a long-awaited return to better times for the makers of optical components? Is the CPV industry finally starting to gain a foothold in the solar industry?

KEYNOTE	Presentation TBC **Speaker TBC - Soitec**	Soitec
ANALYST	Where the CPV industry is heading, and what it needs to do to increase its market share? **Karl Melkonyan - Analyst - Solar Research - IHS Technology**	IHS
SPEAKER	Mid infrared light emitting diodes enable portable, battery powered gas sensing **Des Gibson - CEO - Gas Sensing Solutions**	GSS
SPEAKER	IC design for very high-speed optical communications – A holistic approach **The' Linh Nguyen - Senior Manager IC Development- Finisar**	Finisar
SPEAKER	UV LED - We are just scratching the surface of the technology's true potential **Pars Mukish - LED & Sapphire Activities Leader - Yole Développement**	YOLE Développement
SPEAKER	Unlocking opportunities for compound semiconductors with micro assembly **Chris Bower - Chief Technology Officer - X-Celeprint**	XCeleprint

RF-ELECTRONICS

The potential of GaN in the RF arena has never been in doubt. But does it now satisfy all the requirements for deployment in the most taxing situations?

Role	Presentation
KEYNOTE	GaN for radar applications **Takahisa Kawai - General Manager - Sumitomo Electric Device Innovations, Inc. (SEDI)**
ANALYST	The future for GaN, SiC, InP and GaAs in defense/military applications **Asif Anwar - Director - Strategy Analytics**
SPEAKER	GaN for commercial RF applications enabled by the pure-play foundry model **Walter Wohlmuth - Associate VP Technology - WIN Semiconductors Corporation**
SPEAKER	Presentation TBC **Chris Horton - Director, Global Sales & Marketing - Cree Inc.**
SPEAKER	Presentation TBC **Marianne Germain- Chief Executive Officer - Epigan**

III-V CMOS

By the end of this decade, it is said that silicon CMOS will have run out of steam. But what role will III-Vs have to play in the microprocessors of the future?

Role	Presentation
KEYNOTE	Heterogeneous integration of III-V's and CMOS **Daniel Green - Program Manager - Defence Advanced Research Projects Agency (DARPA)**
ANALYST	When will III-Vs make an impact in the silicon foundries? And will it last for long? **Mike Corbett - Managing Partner - Linx Consulting**
SPEAKER	III-V FETs for future logic applications **Jesus A del Alamo - Director of the Microsystems Technology Laboratories - MIT**
SPEAKER	Opportunities and challenges of III-Vs in Si-based nanoelectronics industry **Matthias Passlack - Deputy Director - Taiwan Semiconductor Manufacturing Company (TSMC)**
SPEAKER	Advanced in-situ metrology for III-V on silicon technology **Kolja Haberland - Chief Technology Officer - LayTec AG**
SPEAKER	Eliminating material boarders for heterogeneous integration through new wafer bonding processes **Thomas Uhrmann - Head of Business Development - EV Group (EVG)**

FRONT-END MOBILES

What's the biggest threat to revenues for GaAs power amplifiers? Is it the emergence of multi-band, multi-mode PAs built with this material, or the emergence of CMOS solutions?

Role	Presentation
KEYNOTE	The path to intelligent integration **Jim Cable - CEO, President and Chairman - Peregrine Semiconductor**
ANALYST	Multi-mode, multi-band PAs: friend or foe to the compound semiconductor industry? **Eric Higham - Director - Advanced Semiconductor Applications - Strategy Analytics**
SPEAKER	Improving system level integration and overall efficiency **Peter Gammel - Corporate CTO - Skyworks Inc.**
SPEAKER	LTE is driving complexity in smartphone design **Sean Riley - Vice President of Mobile Products - TriQuint Semiconductor**

Connecting, informing and inspiring the compound semiconductor industry

POWER ELECTRONICS

From a performance perspective, GaN and SiC are superior to silicon, but high prices are holding them back from displacing the incumbent. How can this be addressed?

KEYNOTE
Ditching the package to drive down GaN transistor costs
Alex Lidow - CEO and Co-founder - Efficient Power Conversion Corporation (EPC)

ANALYST
When can WBG power electronics truly take off?
Pierric Gueguan- Senior Power Electronics Market Analyst - Yole Développement

SPEAKER
SiC technology in power electronics – a step change in value
Markus Behet - Global Market Segment Manager - Dow Corning Corporation

SPEAKER
High performance GaN-on-Si power epiwafers employing rare earth oxide buffer layers
Andrew Clark - VP Engineering - Translucent Inc.

SPEAKER
Presentation TBC
Brian Crawford - Director of Business Development - KLA-Tencor

SPEAKER
Driving down costs for next-generation PVD processes
Reinhard Benz - VP Sales and Marketing - Evatec

SPEAKER
Gallium nitride epitaxy on large area silicon substrates for power applications
Yoga Saripalli- Principle Engineer - GaN Epitaxy Group - imec

SPEAKER
Optimization of III-V R&D and manufacturing using advanced analytical methods
Temel Buyuklimani - Senior Director - Quadrupole SIMS Services - Evans Analytical Group (EAG)

SPEAKER
Accelerating the transition from R&D to production for GaN power electronics using MOCVD technology
Sudhakar Raman - Vice President, Marketing - Veeco Instruments

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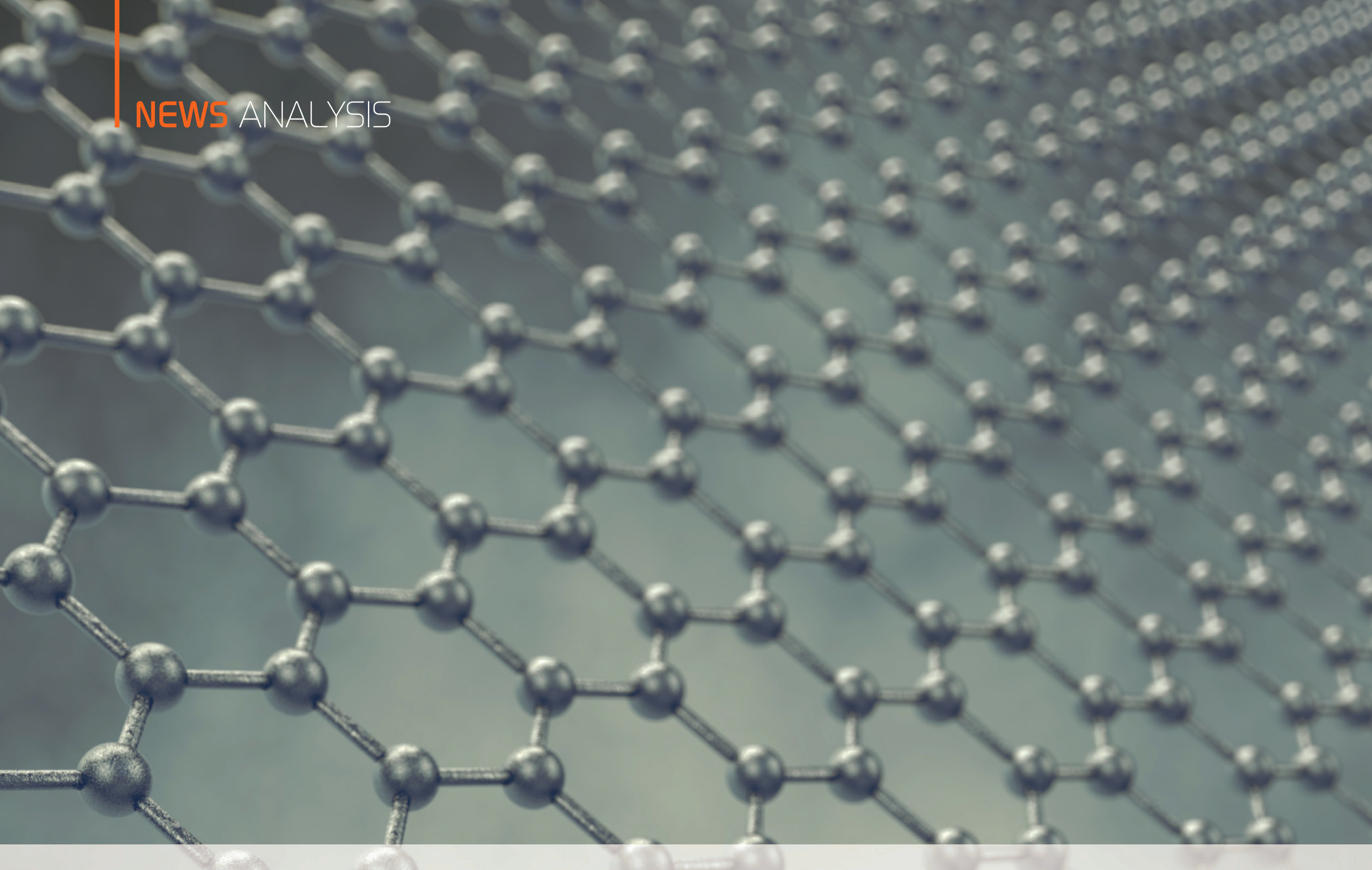

Growing the terahertz transistor

Breakthrough GaN-on-graphene growth brings Naval Research Laboratories' researchers close to hot electron transistors. Rebecca Pool reports

CLAIMING A WORLD FIRST, researchers from the US-based Naval Research Laboratories have successfully grown a high-quality GaN film on graphene, a critical step to developing so-called hot electron transistors for terahertz frequency applications.

Using MOCVD, GaN films were grown on functionalised epitaxial graphene, over an AlN nucleation layer, yielding a crystalline quality on par with GaN grown on sapphire. What's more, lead researcher, Charles Eddy from NRL's Electronics Science and Technology division, says that his team can use the same process to grow structures across a 4-inch wafer, setting the scene for cost-effective device manufacture.

Hot electron transistors (HETs) hold great promise for high-frequency, high-speed current switching applications as, during operation, the electrons tunnel ballistically through base and collector structures. However, today's state-of-the-art HETs include a metal or heavily doped semiconductor base layer that impedes electron movement, limiting device performance.

With this in mind, researchers worldwide are turning to graphene as an alternative base layer material. Electrons fly through this so-called wonder material, enabling cut-off frequencies in excess of 1 THz, and pleasingly, researchers have mastered methods to grow a single layer of graphene – epitaxial graphene – on SiC substrates.

But while graphene solves a lot of problems, it also raises new issues. As Eddy puts it: "Graphene, and any other 2D material, has very good in-plane bonds, but not very good out-of-plane bonds. There aren't actually any atomic bonds to connect to if you want to try and grow a material, such as GaN, directly onto a graphene surface."

Indeed, deposit GaN directly onto a graphene surface and individual crystallites form instead of a continuous film. And while researchers have modified the surface to circumvent this problem – treatments include plasma-spraying the surface and adding nanostructures – the resulting graphene-GaN interface can inhibit final device performance.

However, a surface modification process, originally pioneered by Eddy's team to integrate high-κ gate dielectrics with graphene, looks set to solve the problem. So-called fluorine functionalisation involves dosing the graphene surface with xenon difluoride to create semi-ionic carbon-fluorine bonds that provide nucleation sites for III-nitride deposition.

With the nucleation sites in place, Eddy and colleagues then deposit a buffer AlN film onto the functionalised graphene, prior to GaN growth. Aluminium atoms have a higher sticking coefficient than gallium atoms, and in Eddy's words: "Gallium just isn't as easy to stick as aluminium."

But the surface modification success comes with a hitch. The semi-ionic fluorine bonds can attach to the graphene surface while preserving its structure, but these bonds cannot withstand the high temperatures of conventional MOCVD.

"Ionic bonds would break the bonding in graphene and kill its electronic properties," says Eddy. "However, the [semi-ionic] bonds are very temperature sensitive, so to grow III-nitrides on graphene we really need a low temperature epitaxial growth process."

And as it happens, the NRL researchers have been developing a low temperature process, based on atomic layer epitaxy. Closely related to MOCVD, the process relies on a metal-organic precursor and nitrogen for epitaxial growth.

"Rather than using ammonia that is cracked at the high temperatures of MOCVD to create the nitrogen reactivity you need, we use a nitrogen plasma to provide the reactive nitrogen," says Eddy. "This reacts with the metal-organic precursor at the graphene surface, so all the reactions happen on the surface at a much lower growth temperature." And so III-nitride growth takes place at only 280 °C, about half the temperature of conventional MOCVD.

With both graphene functionalisation and low temperature epitaxy in hand, Eddy and his team have grown HET structures on 16 mm^2 functionalised epitaxial graphene sheet. "The 16 mm^2 sheet was used just for economics but the growth process is readily scalable," asserts Eddy. "We could grow the structure over a 4-inch wafer right now."

The researcher also believes initial devices could be just a year away. X-ray diffraction analysis indicates the crystalline quality of the layers is comparable to growth on sapphire, and Eddy reckons his team can do better.

"The lattice mismatch between graphene and AlN is 4.5 percent, which is significantly smaller than the 13 percent between AlN and sapphire," he says. "Given this, we should be ultimately getting better crystalline quality."

So now the team is exploring the underlying physics to boost material quality further. "We want to understand the mechanisms with better clarity," says Eddy. "Our work shows it is possible to grow [hot electron transistor] structures using this process, so the question is can we now control it enough to improve materials quality and make better performing devices?"

Terahertz designs: the NRL research team is pioneering GaN-on-graphene growth in a bid to fabricate hot electron transistors.

All eyes on GaAs

GaAs demand from military sectors is poised for growth, but will the industry favourite fend off competition from up and coming GaN alternatives?

Rebecca Pool investigates

WITH GLOBAL SPENDING on defence set to increase by 2.25 percent year-on-year to more than $2.1 trillion by 2023, the market for GaAs chips looks very solid. In his recent report, *GaAs Industry Outlook 2013-2018*, Strategy Analytics analyst, Asif Anwar, predicts GaAs device demand for defence sectors will grow at almost triple the rate of commercial GaAs markets, with one of the biggest pushes coming from communications applications.

"The growth rate is higher than commercial sectors as you are starting from a relatively low level," says Anwar.

"But certainly in communications applications, military markets have been catching up with a commercial sector that already has LTE-based, data-centric and IP-based communications."

As Anwar highlights, users of today's wireless devices demand Internet access, video-streaming, cameras and more. And, of course, these technologies demand linear and highly efficient compound semiconductors.

"GaAs semiconductors are the incumbent and state-of-the-art technology in cellular handsets that typically employ more than one GaAs-based power amplifier to enable operation across a spate of different frequency bands," he says. "But now we will see this GaAs-based technology being used more and more in the handheld terminals used by your war-fighters on the ground."

The second critical application for GaAs devices is, of course, radar. This sector currently accounts for more than 60 percent of GaAs military market revenue and will remain a hefty income earner for the technology, for some time yet.

According to Anwar, GaAs transmit/receive (T/R) modules, now standard in the active electronically scanned array radars of fighter aircraft, are rapidly transferring to different platforms. Manufacturers of naval- and land-based radar systems, for example, are turning to such solid state technology to extend capabilities of future systems.
"You may not get the same kind of volume in a naval radar system as you do in a fast-jet platform, but a naval radar can be much larger and require as many as 20,000 transmit-receive modules," says Anwar.

And as the analyst adds: "We're also seeing a replacement of traditional RF

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technology in systems that use a passive electronically scanned array fed by a transmitter, with a solid state-based transmitter displacing travelling wave tube-based technology."

Make way for GaN

But what about GaN? From radars to tactical jammer systems, the defence industry has spent more than a decade developing GaN for military applications. Thanks to its high power density and efficiency, the technology has clear benefits in high performance systems, with the likes of Raytheon, TriQuint, Northrop Grumman and Cree proving its manufacturability through US Department of Defence programs.

"New radar systems are looking towards GaN as being the go-to technology," says Anwar. "Raytheon, for example, is looking to GaN for the Patriot radar while Airbus Defence & Security introduced the GaN-based TRS-4D naval radar."

But as Anwar highlights, manufacturers of GaAs-based systems don't need to worry yet. In the same way that TWT-based technologies currently underpin many radar systems and will be in operation for the next decade or more, GaAs-based technologies are not going to disappear overnight.

For starters, current military platforms, be they fighter jets or naval vessels, have very long lifetimes. Mid-life upgrades are likely to see GaN-based radar systems replacing GaAs technologies, but this scenario could be at least a decade away. And right now, even the latest platforms are emerging with GaAs T/R modules.

For example, according to Anwar, SAAB Gripen's latest fighter jet, the NG (next generation), is set to come into service come 2018 using a GaAs active electronically scanned array antenna. Similarly, planned upgrades to the Eurofighter Typhoon combat jet radar will also be underpinned by GaAs technology.

"My understanding is the Eurofighter radar is a modular design, so when the craft comes for a mid-life platform upgrade, its GaAs radar could eventually be replaced with the latest GaN-based T/R modeules."

"Yes, GaAs technologies will see a squeeze," argues Anwar, "but developments take time in the military world and we will not see the GaAs market crashing overnight."

The Institute of Compound Semiconductors could be up and running by late 2016.

Hybrid hope

Backed by IQE, the UK-based Institute of Compound Semiconductors is set to boost III-V on silicon fabrication across Europe. Rebecca Pool investigates

IN EARLY OCTOBER THIS YEAR, the Vice-Chancellor of UK-based Cardiff University, Colin Riordan, unveiled bold plans to build a multi-million pound *Institute of Compound Semiconductors*, that could change the face of materials and device fabrication in the UK.

The new, Wales-based manufacturing facility will focus on fabricating compound semiconductors-on-silicon materials and devices, and could be up and running by late 2016.

IQE is a major partner and as Phil Buckle, Head of Condensed Matter and Physics at Cardiff, and a key player in the new Institute, puts it: "Drew Nelson, the chief executive of IQE, is very passionate about this, as is our vice chancellor."

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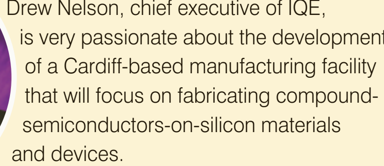


Drew Nelson, chief executive of IQE, is very passionate about the development of a Cardiff-based manufacturing facility that will focus on fabricating compound-semiconductors-on-silicon materials and devices.

grander plan to convert a disused industrial space in Cardiff into a cutting-edge tech campus. This would include ICS, a social science park, an innovation centre for start-ups, and a research facility to promote commercialisation. But crucially for the semiconductor industry, ICS, would provide manufacturing scale facilities to support an indigenous industry across Europe.

"Right now, if IQE grows an 8-inch GaN-on-silicon wafer, they then have to say to customers, 'if you want to process this, then you've got to go to, say, Singapore'," explains Buckle.

"This is a real problem for the UK and Europe, so the idea here is that our large-scale facilities will cope with this and really pull through our materials into manufacturing markets."

The facility will include the main fabrication line for 8-inch compound semiconductors-on-silicon. According to Buckle, all III-V materials, including GaN, InGaN, InP, and antimonides, are likely to be included with device fabrication ranging from exotic electron spin quantum devices to semiconductor lasers, FETs, and photonic structures.

"For a number of years 8-inch [wafer lines] have been the workhorse of silicon foundries and what the compound semiconductor industry now needs is a comparable 'silicon mentality' facility," says Buckle.

"Having this facility will also enable high quality research within a highly controlled fabrication plant, bringing reproducible and efficient research based devices through to manufacturing ready technology."

And critically, a small-area fabrication line devoted to making research manufacturable and operated by the same engineers as the key fabrication line, is to also be included. As Buckle points out: "Very often a big barrier for companies is they have to significantly re-engineer research to make it manufacturable. But if the researchers can say, 'with a minimal amount of engineering this can be translated to a large area line', then we have a business."

Off the ground

So the next step is to secure all funds. The University's vice chancellor has promised ICS a significant cut of his £300 million innovation budget. Meanwhile, Buckle and colleagues are also busy levering funds from the Welsh Assembly as well as the European Commission's research and innovation pot, Horizon 2020.

And while IQE's input is public knowledge, several other yet-to-be-named companies will also be joining ICS. "We've moved away from the days of large corporations having research laboratories," highlights Buckle. "And certainly in the compound semiconductor industry, no single company is large enough to sustain pure research without collaboration or the use of shared facilities."

Buckle is certain that equipment suppliers will also join the new venture; ICS looks set to be a unique facility where the likes of Oxford Instruments may wish to second engineers and trial equipment within a process line.

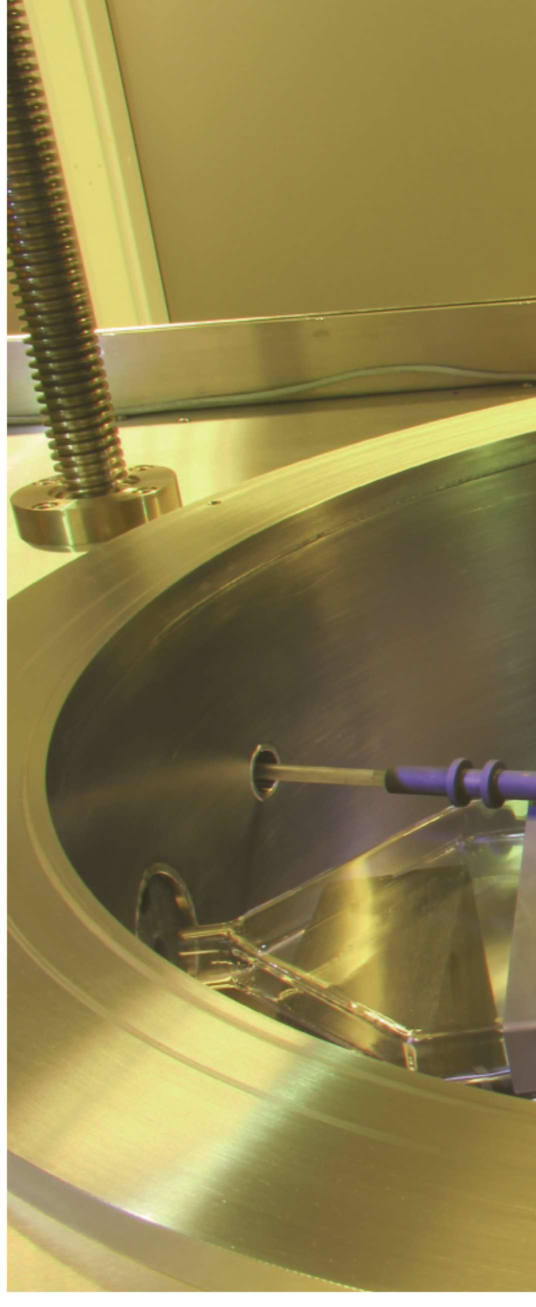
In the meantime, the researcher expects building work to start within six months, with a fab coming online, at earliest, in two years. And even grander plans are in place, further into the future.

"The long-term goal is for this to stimulate the fifth semiconductor cluster in Europe," he says. "Eindhoven, Dresden, Grenoble and Leuven [imec] are primarily silicon-based but this would be the first cluster based on compound semiconductors."

Reactor

start-up to exploit research markets

About to fulfill its first order, Sweden start-up, Epiluvac, is ready to deliver CVD reactors to wideband gap materials developers worldwide. Rebecca Pool reports



EARLIER THIS AUTUMN, Sweden-based Epiluvac revealed it is to start providing silicon carbide CVD epitaxy reactors – in different configurations – to research communities around the world. While SiC Schottky diodes have long been used in power factor correction, the power semiconductors are making in-roads into solar, rail traction, UPS and automotive markets.

France-based analyst business, Yole Développement, recently reported that the SiC chip market almost reached $100 million in 2013, thanks to well-established markets. And as the likes of Infineon, Cree, Rohm, ST Microelectronics and more race to develop smaller, cheaper and more efficient diodes and transistors for these as well as growing markets, good quality materials are more important than ever.

Hot wall CVD reactors, pioneered in Sweden, at Link ping University, are critical to the development of wide bandgap semiconductor manufacture, taking pride of place in many a research laboratory since the mid-1990s. And as Bo Hammarlund, managing director of Epiluvac, highlights, demand is rising.

"Today the business for silicon carbide mainly comes from diodes for UPSs and inverters," he says. "But we now see a driving force to improve SiC transistors, reduce costs and build powerful, reliable modules."

"I also see convincing arguments that SiC switching transistors will be adopted in the power train for the next generation of hybrid electric vehicle, battery- and fuel cell-electric vehicles, and all-electric vehicles," he adds.

So with this in mind, Hammarlund is determined to capture custom from researchers and developers of SiC materials, whom he believes his company is best placed to serve. As he highlights, Epiluvac is next to Lund University within Sweden's Kista research region, home to numerous SiC-related start-ups. Companies include key SiC epitaxy player, Ascatron, SiC bi-polar transistor developer, TranSiC – acquired by industry heavyweight, Fairchild, in 2011 – as well as epitaxial graphene-on-silicon-carbide supplier, GraphenSiC, advanced silicon epitaxy service provider, Nocilis Materials, and more.

Hammarlund himself has been instrumental in setting up some of these companies. As he puts it: "We will find good and interesting business in developing cutting-edge CVD reactors to research and development, and small-scale production."

And while CVD equipment heavyweight, Aixtron, also delivers hot-wall CVD tools, primarily to larger businesses, researchers and start-ups will remain Epiluvac's target market. "We're not competing with Aixtron, they are a company of 800, we are a company of eight," says Hammarlund. "Researchers really demand high quality materials that in my opinion large-scale reactors cannot provide at the moment. They also don't have the flexibility [of smaller systems] and are very expensive to run."

So what exactly is Epiluvac providing? The company has developed both single- and dual-wafer hot wall reactors, for 6-inch wafer diameters.

According to Hammarlund, his company's new reactor includes several new features such as separated gas lines to the SiC substrate, so the gases mix just above the substrate. As the managing director points out, this

prevents nucleation of the material in the gas phase before the gases have reached the substrate.

"We also have a new design of reaction cell, which saves consumables. This, for example, keeps silicon carbide deposits on graphite [components] to a minimum, extending the active period before the user has to exchange these expensive [parts]," he adds. "And heating is resistive rather than RF-generated."

With its new technology in tow, Epiluvac plans to deliver a single-wafer 6-inch reactor – custom designed for experimental SiC research – to its first customer before this issue of *Compound Semiconductor* goes to press. But it's not all about SiC. While the company has focused on SiC first, it is also looking at GaN markets, and intends to start designing reactors for GaN materials by the end of the year.

"The demand for GaN semiconductors will grow due to fifth-generation mobile telecoms base stations, which will be [reaching markets] around 2018," says Hammarlund. "So right now there is a big effort to get European industry ready to produce GaN power transistors for 10 GHz basestations."

As Hammarlund highlights, his company's reactors are modular and consist of a basic platform that can be adapted for different materials. And beyond SiC and GaN, the company has also set its sights on AlN, SiGe and graphene.

"We [will] be able to pick up new demands at an early stage not only for SiC, but also GaN, AlN and graphene," he says. "It is also our ambition to stay in close contact with our customers to customise tools for their specific needs. We have a lot of experience in doing this."

"We now see a driving force to improve SiC transistors, reduce costs and build powerful, reliable modules."

Bo Hammarlund

Big Blue ambition

IBM researchers have grown GaN films on graphene to produce blue LEDs; wafer-scale manufacturing is next. Rebecca Pool reports

EARLIER THIS YEAR, IBM researcher Jeehwan Kim and colleagues unveiled a blue LED comprising GaN layers on epitaxial graphene. The GaN films had a low defect density and surface roughness on par with layers grown on conventional SiC and sapphire substrates while the performance of the LED matched that of a conventional GaN-on-sapphire device.

Kim's latest results form part of an IBM drive to produce wafer-scale, single-crystalline sheets of graphene that can then be used as cheap, reusable substrates on which to grow single-crystalline III-nitride layers, and manufacture cheap GaN-based devices.

The plan is to lift off the semiconductor layers from a wafer-scale graphene substrate, and then transfer these layers to an arbitrary substrate. The remaining graphene substrate will be repeatedly re-used for further III-nitride film growth, giving way to extremely cheap GaN device manufacture. Kim and colleagues are getting close.

Materials growth

The main barrier to growing single crystalline films on graphene is the material's lack of so-called dangling bonds. As Kim explains: "The material has no broken bonds on its surface, there are no attraction forces and so it is very difficult to nucleate materials on top of graphene."

To overcome this, Kim and colleagues first grew graphene onto a SiC wafer containing nanometre-scale steps to act as nucleation sites for subsequent GaN epitaxy. For many researchers in the field, a next step has been to deposit an AlN buffer layer to a SiC substrate, followed by GaN growth. But Kim wanted to pursue a different route.

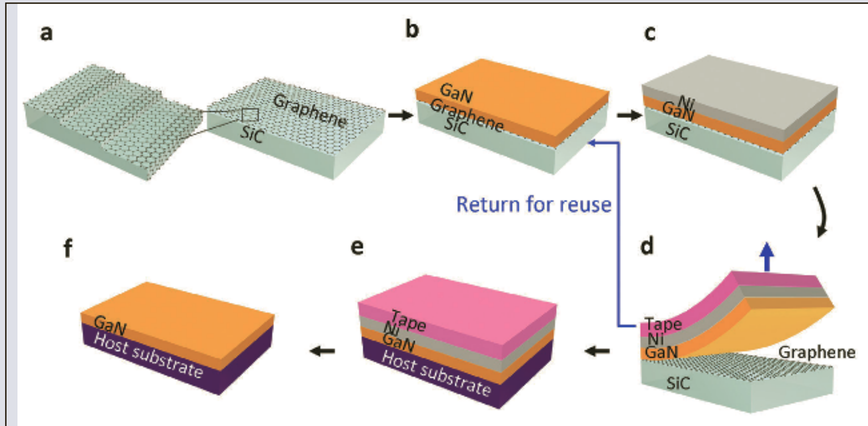
"If we used an AlN buffer layer on the graphene, growth would be easier but I didn't use it on purpose," he says. "To fabricate a vertical functional device, it is desirable to deposit layers onto a highly conductive layer, and AlN is not so ideal in this case."

Instead, Kim, and colleagues turned to van der Waals epitaxy. This alternative epitaxy mechanism circumvents the lattice matching requirements of conventional epitaxial growth as the substrate and overlying epitaxial layer only form weak van der Waals bonds, rather than the covalent bonds of conventional epitaxy.

And so, using carefully controlled growth kinetics in a MOCVD reactor, Kim and colleagues grew single-crystalline, 1 cm^2, GaN films onto the epitaxial graphene. As Kim highlights: "The GaN crystalline quality was comparable to that typically obtained with conventional AlN-buffer-assisted GaN epitaxy on SiC or sapphire substrates.This is totally different from conventional epitaxy growth, and you can substantially reduce dislocation-related defects in principle."

The next step was to release the GaN film and demonstrate exactly how re-usable the graphene-on-SiC substrate could be. To this end, the researchers deposited a layer of nickel onto the GaN film, to create enough strain within the semiconductor film to overcome the relatively weak GaN-graphene bonds. A thermal release tape was then added, with the GaN film being completely removed and transferred to a second substrate.

Microscopy and spectroscopy analyses revealed the process to be a success. Uniform coverage of graphene was observed across the released interface,



Schematic for growing and transferring single-crystalline thin films onto and from epitaxial graphene. [IBM]

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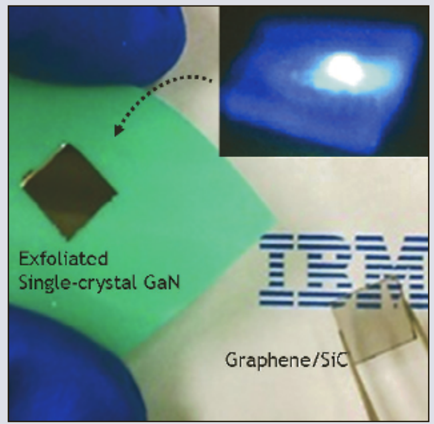


IBM researchers have grown single-crystalline films of GaN on epitaxial graphene. [IBM]

without any trace of graphene residue on the GaN film.

Crucially, Kim and colleagues went on to grow an LED stack on a recycled graphene-SiC substrate that had been previously used three times. Light emission peaked at a wavelength typical for III-nitride LEDs.

Kim is confident that this process will now scale as necessary. “I have demonstrated the [growth/transfer] process four times, but conceptually believe this could be repeated infinitely,” he says.

Similarly, wafer-scale demonstration shouldn’t pose a problem. “Right now our substrate size is 1cm by 1cm, limited by the size of our lab-scale MOCVD reactor,” he adds. “But in principle, wafer-scale GaN release is possible. The graphene substrate is single crystalline, so if you perform the process at a manufacturing scale, it is going to work.”

So where next for the IBM researchers? Working closely with chief collaborator, Can Bayram, Kim and colleagues have transferred GaN layers onto flexible plastic substrates and silicon wafers, a crucial step to low-cost wafer-scale fabrication of GaN devices. Kim is currently focused on fabricating more LED structures but has additional plans.

“I developed this technique to get an idea of how to grow any type of single crystalline material on graphene,” he says. “I have demonstrated GaN and am now going to try other materials on graphene.”

RFMD - TriQuint

finish on a quarterly high

Amid financial success, RFMD and TriQuint executives eye post-merger prospects. Rebecca Pool reports

WITH RFMD AND TRIQUINT reporting very healthy quarterly results, shares for each company jumped between five and ten percent towards the end of October. TriQuint beat analysts' expectations with its latest round of revenue rising by almost 9 percent to $272 million, while RFMD reported a quarterly record as revenue soared by 15 percent sequentially.

In his second quarter 2015 earnings call, RFMD chief executive officer, Robert Bruggeworth, repeatedly emphasised how company revenues are being driven by 'an exploding demand for mobile data'. "Across the mobile data landscape, consumers are demanding more bandwidth to support data-hungry applications," he highlighted. "RFMD solutions are a key enabling technology... and [the company] is supplying the industry's leaders the products they need to differentiate their devices."

And Ralph Quinsey, TriQuint chief executive, agreed, attributing improving finances to buoyant communications and defence markets demanding GaAs and GaN devices, and filters. "BAW [filters]... generate hundreds of millions of dollars in revenue that had modest roots in the defence market," he said. "GaN-based products... are following a similar path with new opportunities openings in base station power and other commercial applications that require higher power, higher efficiency and greater bandwidth."

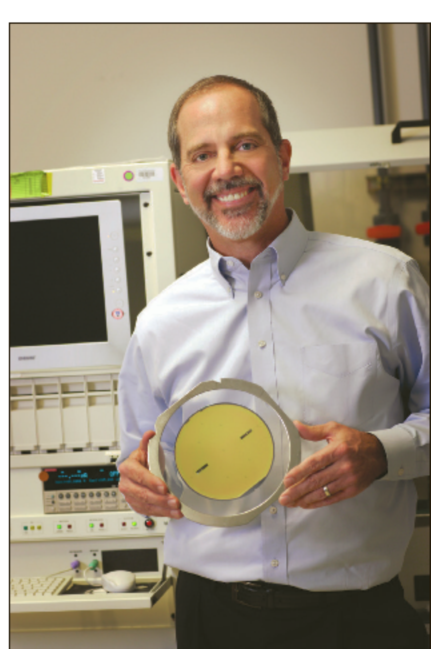
Merger moves

However, change is afoot, and come the next finance quarter, industry players are likely to be listening to the results of Qorvo, the new company to emerge from the pending RFMD-TriQuint merger, scheduled to complete by the end of this year. Dubbed 'a merger of equals', executives from both sides are, predictably, upbeat about future company prospects.

Throughout their earnings calls, neither chief executive would be drawn on specific future products; in Bruggeworth's words: "We have not realised any synergies between the TriQuint and RFMD merger yet". But each highlighted overwhelming shareholder support for what will be a formidable presence in the RF chip industry. Without a doubt, handset markets represent a massive opportunity for the new company. As Bruggeworth highlighted: "We will have the various technologies that we believe are needed in the RF front end for the handset in particular."

"There's opportunity for us to gain some [market] share as we come together and get our product and technology roadmaps aligned," he added. But base station power markets are also significant. According to Quinsey, third quarter revenues in this market hit a hefty $25.6 million, up more than 53 percent compared to the same time last year. "We continue to experience strong demand related to the worldwide 4G LTE build out," he said. "Over the last 18 months, demand for our base station products has ramped to just north of $100 million a year. We expect to maintain this level... well into 2016."

"We continue to experience strong demand related to the worldwide 4G LTE build out," said TriQuint CEO Quinsey. "Over the last 18 months, demand for our base station products has ramped to just north of $100 million a year. We expect to maintain this level... well into 2016."



Ralph Quinsey, TriQuint chief executive, describes base station power markets as 'significant'. Third quarter revenues in this sector hit a $25.6 million, up more than 50 percent compared to the same time last year.

And as wireless infrastructure markets evolve, China, followed by India, look set to offer some golden opportunities. Executives from RFMD and TriQuint were keen to point out how China's LTE infrastructure market remains steady while the same again in India is showing signs of growth.

"[Compared to India] I've seen more activity on the China LTE buildouts," highlighted Norman Hilgendorf, RFMD president of multi-market product groups. "But everybody is expecting that India will be hot on the heels of China in building out LTE infrastructure as there's a large subscriber base that going to want the benefits of 4G."

Quinsey concurred, stating: "For India and China, we have seen a good solid buildout throughout the year... [that will be] sustained for quite a long time." But also for the present TriQuint chief executive, defence markets remains as crucial as ever. His company has continued to launch GaN product after GaN product, reaping the ensuing defence revenues.

"We remain in the early innings of a defence industry upgrade cycle with the ramp of the joint strike fighter and the retrofit of US and international fleets to phase [in] radar and advanced electronics," he said. "I expect Qorvo will benefit from this legacy technology development."

Q&A Roy Qiu

Global Market Sector Head Solar & LED, Linde Electronics

Q How would you describe the current state of the LED industry?

A The global LED industry has grown very fast since 2010. The quantity of MOCVD tools installed worldwide by Q1'14 has exceeded 2,700 sets; this number was less than 1,000 in 2009.

Display backlighting and general lighting are the two biggest application markets for LED. With the saturation in display backlighting, especially for TV, where LED penetration will reach 98% in 2014, the future growth of the LED market will, to a large extent, depend on further development in general lighting. LED lighting is still at an early stage of adoption. It accounts for a small but increasing share of the total lighting market. Rising electricity prices, mounting concerns about climate change, and the desire for energy independence are driving the global lighting market to shift toward energy-efficient light sources: LED-based lighting products.

It is estimated that the global lighting market generates an annual revenue of nearly $100 billion; LED products accounted for 18 percent of lighting revenues in 2013. We believe that LED's share will keep increasing in the years to come. The industry's future is bright, but it is experiencing painful overcapacity. Current LED capacity installed in the world is enough to meet the global demand by 2018, so market consolidation is unavoidable and harsh.

Only providers that have good channels to the end market with continuous innovation in high-performance, cost-competitive products will eventually survive and enjoy a profit. Half of LED makers may disappear in the next five years in the shakeout as the market matures.

Increased adoption driven by continuous cost reduction and improved consumer awareness represents an enormous energy savings opportunity for the world and an enormous market opportunity for LED lighting manufacturers and component and materials providers.

Q Are LED chipmakers concerned about quality of gases supplied in the industry? Or is price their primary concern?

A Yes, LED chipmakers are very sensitive to material purity because unexpected impurities lead to declined device performance and/or early failure. For example, ammonia (NH_3) gas used to react with Trimethylgallium (TMGa) to form Gallium Nitride (GaN) layers in LED chip making. The LED industry demands highest product purity (7N, i.e. 99.99999%) with lowest impurity - especially of moisture (some customers require that moisture level be below 50 ppb).

Q Are you developing new sources, or new technologies to deliver them?

A Linde has developed and delivered the best-in-class ultra-high purity ammonia supply solution. This meets the critical demand of global top LED customers to achieve the highest ammonia purity at a stable high flow rate (3000 slpm), but with lowest moisture impurity (<20 ppb). At the same time, Linde's small scale SMR (steam methane reformer) hydrogen (H_2) plants make a switch from trailer supply to onsite generation economically viable for small fabs (approximately 50% of the size of conventional hydrogen plants).

Customers get benefits of simplified supply chain and lower unit costs without the need to use electrolysers.

Q How does Linde set itself apart from the competition?

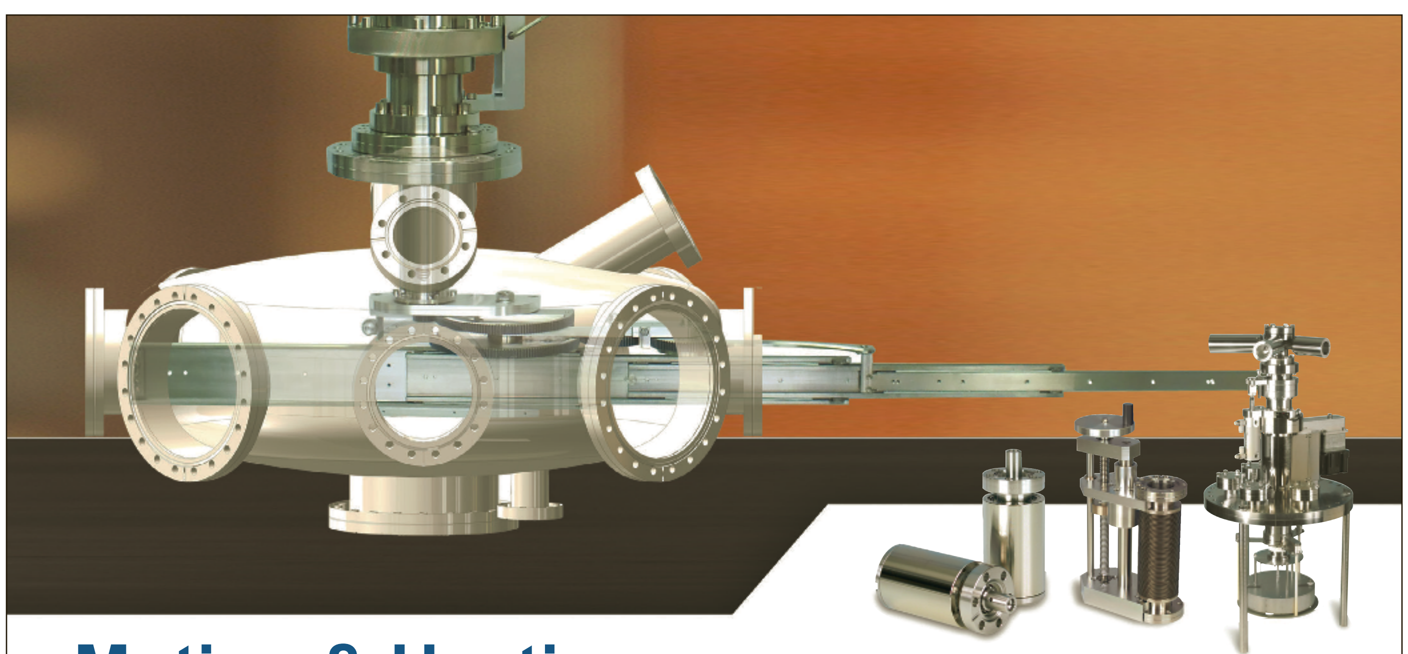
A Linde provides turnkey solutions with a full product portfolio - gas, engineering, and service - reducing, for customers, complexity and interfaces with multiple suppliers. Linde also has local production facilities of ultra-high purity ammonia in China, Taiwan, and Korea, where around 80% of global LED production capacity has been built. Linde is leading in technology - our NH_3 supply system with stable high flow and low moisture is the best in the market. We also have an on-site NH_3 purification solution available for demand of over 1000 tonnes per annum.

Q Do you believe that competition for sales is fiercer than ever, given the launch of materials suppliers in China and USA entering the market?

A There are a few local producers and suppliers of ammonia in China and Taiwan. LED customers choose Linde because of superior technology for gas purification and delivery, security of supply running three high-purity ammonia plants in Taiwan, Korea, and China, turnkey capabilities including gas supply, hardware installations, and operation and maintenance from a single supplier.

Q What are your biggest selling products into this industry? Why?

A The top three products that Linde sells to the LED industry are ultra-high purity ammonia and H_2 and N_2 gases. These are the major gas molecules in the process of epitaxy wafers, which is the most important process among all the LED chip processes. Linde is a global lsupplier of ultra-high purity ammonia purification with a lot of H_2 and N_2 resources near leading LED manufacturers in Asia and Europe.



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Trumping silicon devices with SiC

SiC power devices offer better value for money than ever, thanks to advances in materials, manufacturing processes and chip design

BY MARKUS BEHET FROM DOW CORNING

FOR POWER ELECTRONIC applications requiring devices that can handle 600 V or more, chips that deliver the best performance are made from a stack of homoepitaxial layers of SiC that are deposited on a native substrate. Armed with this combination, devices can operate reliably and efficiently at extreme temperatures, deliver high power densities and ultimately enable significant reductions in power losses at the system level. These capabilities are not associated with the incumbent power electronic material, silicon, which highlights the tremendous potential of SiC devices.

Just how big are SiC's performance advantages over silicon? Well, for example, the junction temperature for silicon is limited to 150°C, while SiC equivalents can operate at extreme temperatures that are hundreds of degrees higher than this. This is due to the inherent low intrinsic carrier density of wide bandgap semiconductors like SiC. What's more, the electric breakdown field for SiC is ten times that of silicon, enabling thinner devices to block far higher voltages; and this wide bandgap material has a higher saturated electron drift velocity, leading to significantly faster switching speeds. SiC also offers comparatively low on-resistance due to its ability to allow higher doped and thinner drift regions for the same breakdown voltage ratings. Together, these collective properties make it clear that SiC has the potential to unleash a radically advanced generation of power electronic devices in systems that are more compact, integrated and energy efficient than what silicon makes possible.

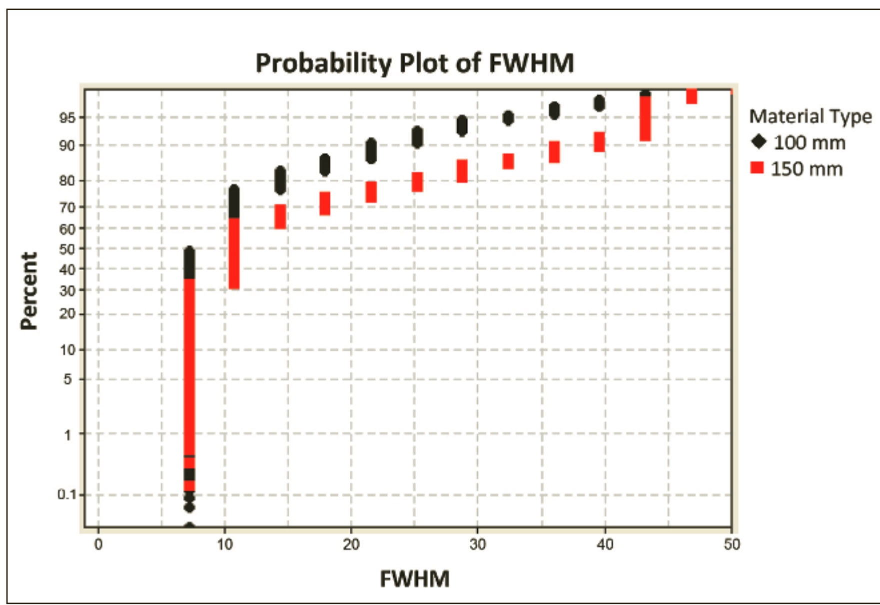

Figure 1. Low full width half maximum (i.e. higher resolution) X-ray diffraction measurement of 150 mm diameter SiC wafers show that they can now deliver crystal quality similar to 100 mm wafers.

Fulfilling this dream is not easy, however. Widespread industrial adoption of SiC is yet to take place, primarily because there are concerns that the cost of SiC is prohibitively high compared to that of silicon. SiC is certainly more expensive than silicon, but determining how much more – and whether it still offers value for money – is not that easy, because it is more complicated than just considering the cost of the wafers. A rigorous evaluation must include factors such as: the level of defect densities in SiC

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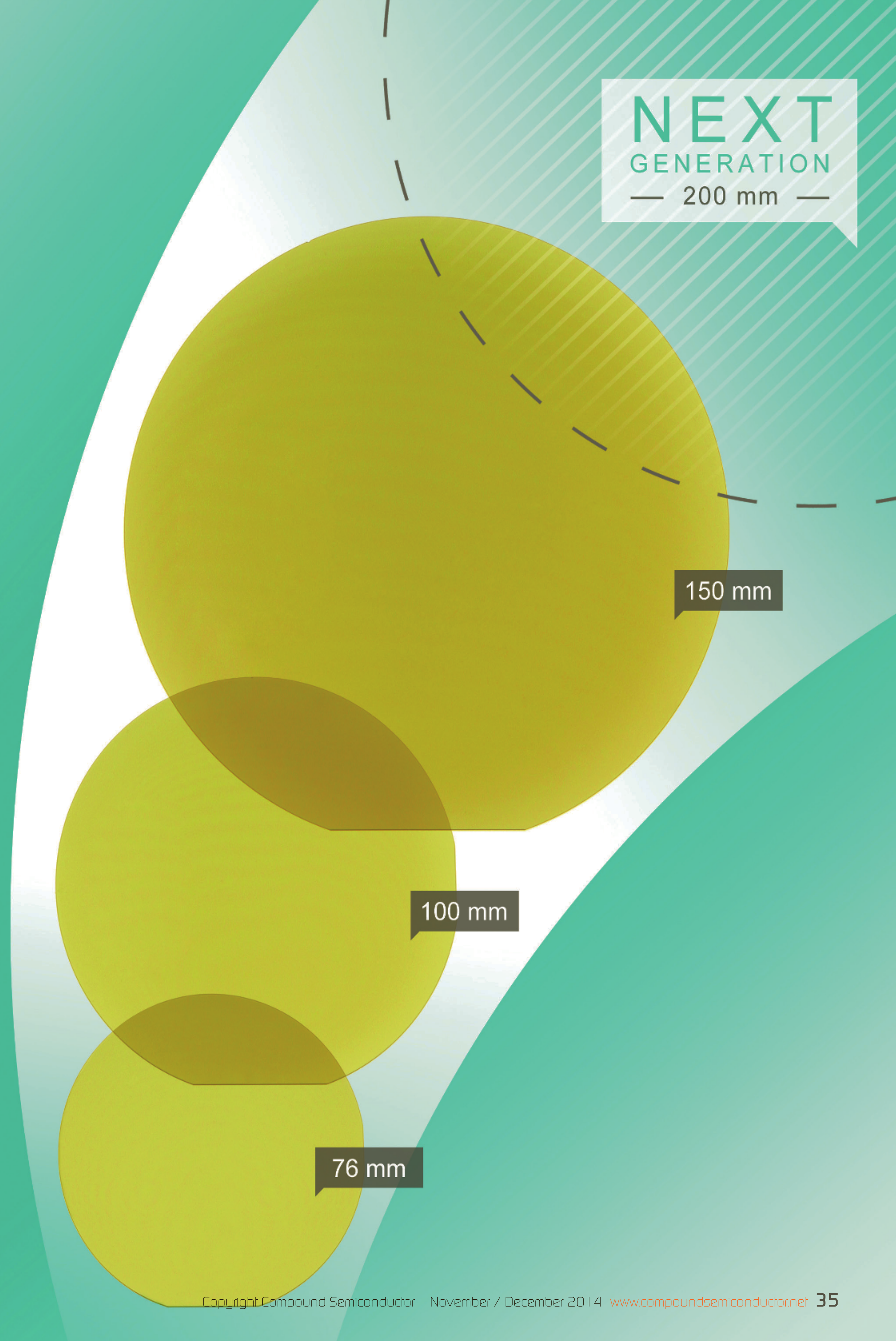
NEXT
GENERATION
— 200 mm —
150 mm
100 mm
76 mm

substrates; the material's complex but improving manufacturing economies of scale; and the impact of SiC's physical idiosyncrasies on module design, such as its positive temperature coefficient of the forward-bias on-state resistance, which prevents thermal runaway of paralleled devices.

What is clear is that SiC devices are getting more competitive, thanks in part to improvements in wafer quality and epitaxy processes, the introduction of larger substrates, and innovations in chip design. Together, these advances have increased the value of this technology closer to – and in some cases beyond – that of silicon in power electronic applications demanding high power densities, small form factors and reduced losses.

Boosting yield

When it comes to substrate sizes, SiC is no match for silicon. Substrates today for SiC are typically 100 mm and will obviously yield fewer devices than 200 mm and 300 mm silicon wafers. However, 150 mm SiC substrates are starting to emerge, and improvements in SiC crystal quality and power device performance are allowing a closing of the gap in device yield per wafer.

Fabs that switch from 100 mm to 150 mm SiC can more than double the number of devices per wafer. But shifting to the larger diameter substrates offers other benefits as well. For example, this migration eliminates special handling costs by allowing the use of conventional 150 mm silicon fabrication equipment – with a few exceptions like SiC-specific implantation and annealing tools. Additionally, the bang-per-buck of the SiC chip benefits from a trimming of material cost associated with metal deposition.

Yet, even if production volumes are reasonably high, 150 mm diameter SiC wafers are still a comparatively expensive platform for device development – especially if the quality is poor. So, to take full advantage of this larger format, it is essential that SiC epiwafers support high production yields by maintaining or reducing the defect densities already achieved in 100 mm SiC substrates today. The starting point, the SiC substrate, has improved significantly over the years. According to high resolution X-ray diffraction and synchrotron white beam X-ray topography, today's 4H-SiC substrates exhibit a high degree of crystalline perfection.

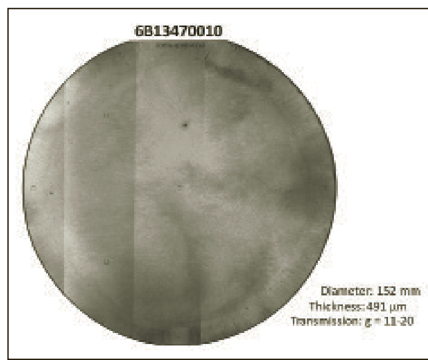

Fig. 2 Basal plane dislocation values determined using a synchrotron white beam X-ray topography transmission scan of a 150 mm SiC wafer with an (11$\bar{2}$0) g-reflection.

> "Growth of films with n- and p-type dopants is possible, with thicknesses ranging from a few microns to more than 100 µm. The latter is needed to produce high-voltage devices capable of handling in excess of 10 kV."

Scrutinizing the wafers with synchrotron white-beam X-ray topography allows the monitoring of individual defect levels on wafers that have been grown with the current physical vapour transport process. In SiC substrates, the four most prominent types of defect are: micropipes, threading screw dislocations, threading edge dislocations and basal plane dislocations. While significant progress has been made in decreasing the density of micropipes to well below 1/cm^2, the other three classes of defect still attract attention, since they can potentially degrade the performance of certain types of SiC-based devices. Several studies have focused on basal plane dislocations, because they can cause a cascade of expanding stacking faults in the active device region under high injection conditions. Bipolar devices such as *p-i-n* diodes, bipolar junction transistors and thyristors suffer as a result, impaired by an undesired forward voltage drift, generally referred to as 'bipolar degradation'.

At Dow Corning, a supplier of SiC substrates and epiwafer services, we are making tremendous efforts to offer our customers a great foundation for device fabrication. We have maintained excellent crystal quality as we transitioned our crystal growth technology from crystals suitable for 100 mm substrates to those that can yield 150 mm variants. Large areas of our 100 mm wafers currently show basal plane dislocation densities as low as 10/cm^2, and threading screw dislocation densities as low as 100/cm^2. Our 150 mm wafers are already approaching these very competitive and industry-leading values.

To take advantage of the entire 150 mm wafer surface, it is crucial to refine the characteristics of the epitaxial film and the device fabrication process. The starting point for optimising the epitaxy, and subsequently the device, has to be access to a substrate with a high degree of crystal perfection. Our substrates fulfil this requirement, being sufficiently well polished to minimize sub-surface damage and cleaned to allow unhindered step-flow growth during the epitaxy process.

Our efforts also include advances in epiwafer manufacturing. The introduction of multi-wafer chemical vapour deposition tools is simplifying the integration of 150 mm SiC wafers and helping to ensure continuity in epitaxial defect reduction between films formed on 100 mm and 150 mm substrates. Growth

of films with *n*- and *p*-type dopants is possible, with thicknesses ranging from a few microns to more than 100 µm. The latter is needed to produce high-voltage devices capable of handling in excess of 10 kV.

We have drawn up epitaxy roadmaps for 150 mm SiC wafers that aim to deliver deviations from the target value that are less than 10 percent for doping, and below 5 percent for thickness. These goals should be met while maintaining excellent uniformity over the entire wafer. By fulfilling these criteria, we will help our customers to realise high yields on 150 mm SiC substrates, and support their efforts to design and develop a range of SiC devices.

Today, our high-quality 100 mm-diameter SiC epitaxial wafers are supporting high-yield, mass production of diodes and transistors. These devices are mostly built to handle 600 V or 1200 V, and are used in a wide variety of power electronic applications, including photovoltaic inverters, power supplies for data and telecom servers, and various power-factor correction, switched-mode power supplies. Managers of the fabs that are churning out these chips are planning to transfer their device production from 100 mm to 150 mm wafers in the next two years. This should reduce manufacturing costs by leveraging economies of scale.

Cost and performance

If defect densities continue to fall in 150 mm epiwafers, this will help to drive their uptake and cut chip costs. A key figure of merit is the performance they deliver per dollar, and evaluations of this must consider the chip architecture, which benefits from the great set of intrinsic characteristics associated with SiC: Devices can handle higher currents at higher temperatures, while sporting smaller die size. Thanks to this miniaturisation, there is the promise of offsetting the higher wafer costs of SiC (see figure 3 for an analysis of total manufacturing costs for similar specified silicon and SiC devices).

Today, SiC epiwafers may well be more than twenty times as expensive as silicon equivalents, and our model suggests that in order to realise cost parity, the number of SiC devices extracted from the wafer must more than double. That is not a tall order, though, given that the intrinsically superior properties of SiC already enable engineers to turn to designs with a reduction in die area by a factor of two or more.

Using these chips can lead to benefits at the module and system level, by unlocking the door to a new generation of smaller, more-energy-efficient, power-electronic modules.

Commercialisation of SiC devices can be traced back to 2001, when Infineon introduced the first commercial SiC Schottky barrier diode. Now, more than a decade on, SiC diodes are manufactured by multiple firms, and they deliver a level of performance that dwarfs their predecessors. Commercial SiC power switches, however, are fairly new. They made their debut in 2011, and now they are available in forms such as the MOSFET and JFET, in discrete and module formats.

The silicon industry is not wresting on its laurels and accepting a loss of market share to SiC transistors. Instead, it has introduced and upgraded silicon power transistors, such as IGBTs. These transistors have continuously lowered on-resistance by using high injection and conductivity modulation.

However, there is a price to pay for that cut in resistance: IGBT switching losses increase and switching frequencies decrease. Its brother – the silicon MOSFET – surpasses the unipolar on-resistance limit at a certain breakdown voltage with the use of superjunction technology, but these devices are so far only available up to 900 V.

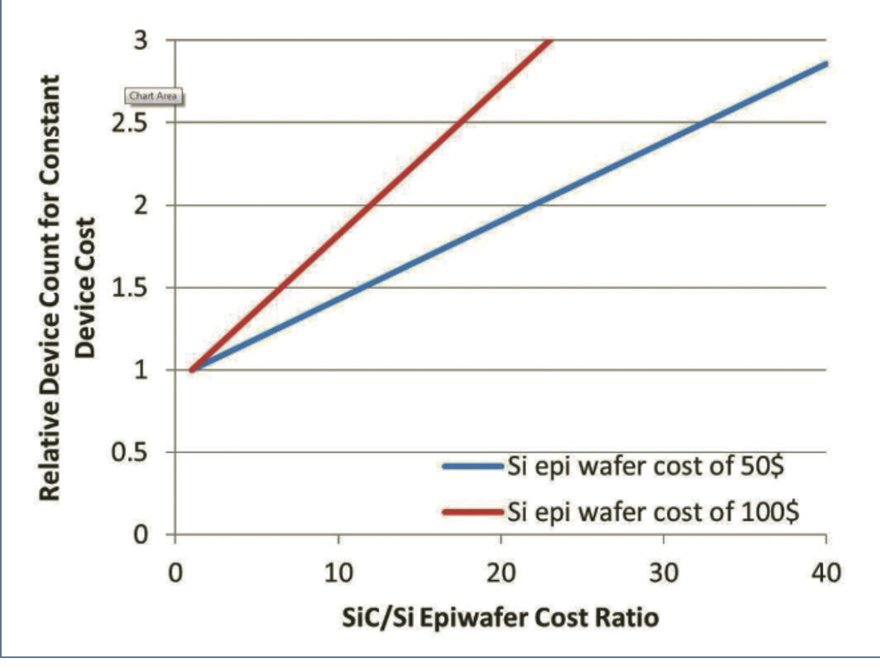

Figure 3. The total manufacturing costs for a fixed wafer diameter include the cost of the epiwafer (Wafer$) plus manufacturing, testing and packaging process (Fab$). Good economics dictate that manufacturing costs should remain fairly constant relative to the number of dies per wafer. Hence, it can be assumed that while Wafer$ may increase with diameter, Fab$ costs generally do not change significantly, so increasing die count is the only way to offset any increase in wafer costs as illustrated by the equation: (Wafer1$ + Fab$)/(Device Count1) = (Wafer2$ + Fab$)/(Device Count2) = Constant. Using this equation, it is possible to calculate the manufacturing throughput required to make 150 mm SiC wafers a more competitive technology than silicon. The graphs above consider the case where Fab$=$1,000 and silicon wafer costs=50$ or $100. These examples are close to that for a power transistor, and illustrate the typical decline in new wafer price as use volume increases.

> "With substrate costs falling and defect densities in constant decline, the call for SiC power electronic devices is getting louder and louder. While discussion in this article has focused on the migration to 150 mm substrates and epiwafers, this is not the end but a stepping-stone to 200 mm SiC"

SiC devices don't suffer from these compromises. Drift-layer resistance is much lower than that for silicon devices, making it possible to realise a low on-resistance. Consequently, adoption of SiC MOSFETs is climbing as they also allow designers to increase switching frequencies and reduce passive components at the system level. Taking advantage of this – and also the high operating temperature and low conduction and switching losses at high switching speeds of today's commercial SiC transistors – enables reductions in cooling requirements and heat sink sizes. The upshot is power electronic designs with significantly smaller form factors, and lower overall system costs.

Tapping into these benefits has required a great deal of effort in developing a reliable, robust MOSFET. This transistor has been dogged by device processing and material quality issues that have been addressed via improvements to the oxide formation process; reductions in surface roughness; and increases in the gate oxide stability. These advances, allied with improvements in epitaxial processes, have led to the production of MOSFETs featuring an intrinsic body diode and exhibiting very little reverse recovery charge. Cheaper, smaller modules are the result.

At the system level, the case for replacing silicon chips with those based on SiC is even stronger than it is at the module level. In the automotive industry, makers of hybrid vehicles are considering turning to SiC to boost fuel efficiency by 10 percent and slash the size of power control units by 80 percent. Meanwhile, in the data and telecommunications industries, SiC diodes are needed to realise current and future efficiency standards for power-factor-correction power supplies. Yet another sector where SiC can play a role is in electric motor systems, where the introduction of more stringent efficiency standards should drive up deployment of high-performance electronics based on either SiC, or a combination of this and silicon in variable speed drives.

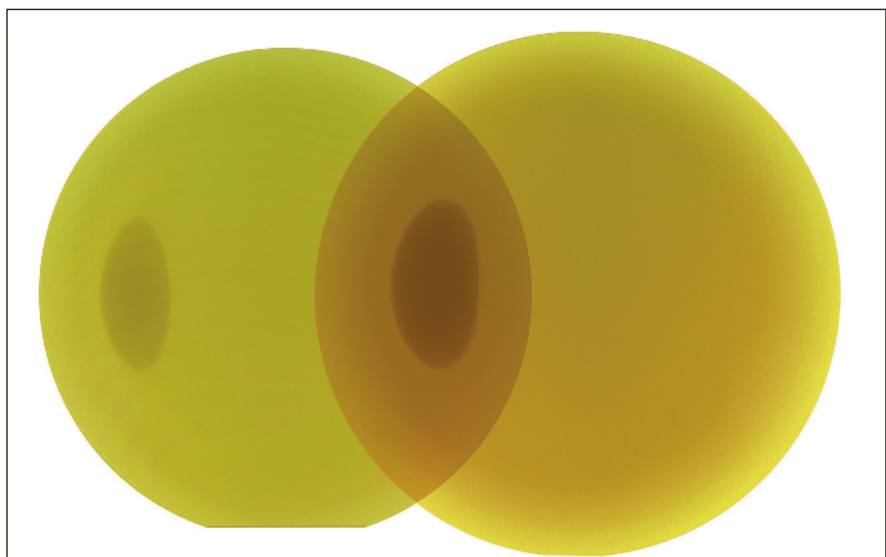

Figure 4. Initial results from a 200 mm diameter expansion project at Dow Corning; a commercial 150 mm SiC wafer is shown on the left hand side.

The road ahead

With substrate costs falling and defect densities in constant decline, the call for SiC power electronic devices is getting louder and louder. While discussion in this article has focused on the migration to 150 mm substrates and epiwafers, this is not the end but a stepping-stone to 200 mm SiC, which will be in demand as market adoption surges and chipmakers continue in their quest to realise superior economies of scale.

Efforts to trim costs are not restricted to chipmakers, as all seriously competitive SiC suppliers are establishing short- and long-term goals for driving internal manufacturing costs down through cost roadmaps. As a leading supplier, we are even establishing product-grading schemes for 100 mm and 150 mm SiC prime grade wafers. Thanks to this scheme, device designers can select the type of SiC material that is best at balancing their expense and design goals.

We believe that over the next 18 months, the supply chain for 150 mm SiC materials and devices made from this will rapidly expand, and adoption of SiC power electronics in various sectors will rise, due to competitive incentives and pressure to improve efficiencies. Given all this, now is the time for makers of photovoltaic inverters, hybrid electric vehicles, power suppliers and power drives for electric motors to consider what the adoption of SiC power electronics can do for them.

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III-Nitrides:

Advances and controversy

Breakthroughs in power electronics, advances in ultraviolet emitters and new arguments associated with the debate on droop featured at the latest international nitrides meeting

DUNCAN ALLSOPP FROM THE UNIVERSITY OF BATH REPORTS

THERE'S NO LET UP in the pace of development of III-Nitride technology, judging from the research reported at the recent International Workshop on Nitride semiconductors (IWN-2014). And for those that gathered in Wroclaw, Poland, a vibrant and welcoming venue for this year's Workshop, there was the opportunity to revel in an ideal environment for reporting exciting advances in GaN power electronics and solid-state lighting.

While the application of III-Nitrides to solid-state lighting will have caught the eye of many round the world, often quite literally, it is quite possible that an even greater impact on humanity will be the deployment of this wide bandgap material in power electronics. When this will happen is hard to say, but it could occur sooner than we think, thanks to advances reported at the recent IWN meeting. At this gathering Daisuke Ueda of Kyoto University of Technology detailed his team's advances in the monolithic integration of GaN gate-injection transistors. These devices could underpin the next generation of efficient consumer products, like air conditioning units, with the chances of commercial success aided by Ueda's collaboration with Panasonic Corporation.

This was not the only advance in GaN electronics to catch the eye. Alexandros Georgakias of the Foundation for Research and Technology-Hellas (FORTH), Greece, reported plasma-assisted MBE growth of GaN on substrates made from polycrystalline diamond. After crystalline diamond, this substrate has the highest thermal conductivity of materials known to mankind, making it an ideal heat-extracting substrate that could enable even more efficient GaN power transistors. Georgakias's talk also outlined the fabrication of a GaN/AlGaN HEMT on this heat-spreading platform. The breakthrough in this work is the absence of a crystallographic relationship between III-Nitrides and the polycrystalline substrate.

Another driver for deployment of GaN power electronics is the need for high-efficiency, high-speed power converters for wind turbines and photovoltaic systems. Srabanti Chowdhury of Arizona State University in the US pointed this out in her presentation, where she championed vertical geometry GaN switches that are grown on bulk GaN substrates. This transistor architecture boosts the breakdown electric field to a value that is more than twice that realised in lateral HEMTs.

Scrutinising reliability

As GaN matures, there has been increasing effort devoted to factors that either limit the performance and reliability of devices, or impair the yield of processes used in their manufacture. Like forensic science, this is painstaking and at times frustrating detective work, where the outcome is often a 'smoking gun', rather than a clean, categorical relationship between cause and effect.

On the last day of the conference Claude Weisbuch, a professor at both the Department of Materials at the University of California, Santa Barbara and CNRS-École Polytechnique in France, made a case for Auger recombination as the cause of droop in nitride-based LEDs.

Several talks in this area were given at IWN-2014, including invited papers from the University of Padova group and from Martin Kuball of Bristol University, UK. Both presentations reviewed how impurities and dislocations in the buffer layer below the channel of a GaN-based HEMT can impact this transistor's transient and high-voltage performance. In these devices, carbon and iron impurities appear to be a double-edged sword, delivering the benefit of inhibiting parasitic electrical current flow, but paying the price of contributing

While attending IWN, many delegates catch up with colleagues and discuss advances in III-Nitrides. Here Bernard Gill (left) from Montpellier 2 University, France, is in conversation with Bruno Daudin (centre) from CEA-Grenoble, France, and Yasushi Nanishi (right) from Ritsumeikan University, Japan.

to unwanted transient effects in GaN based HEMTs. Such a situation is by no means uncommon for semiconductor technologies, as solving one problem often introduces another, leaving the engineer or researcher to evaluate the best compromise for the device application.

Reliability is also a big issue for LED manufacturers, with dislocations fingered as the origin of many ills. Eliminating them is a major driver behind the worldwide research effort at developing nano-LED arrays and nanowire lasers – forming these involves the growth of dislocation-free GaN nanowires by either MBE or MOCVD.

Many presentations at the meeting detailed advances in this area, including three invited talks: a plenary presentation by Pallab Bhattacharya from the University of Michigan, who reviewed his group's pioneering work on light emitters formed from III-Nitride nanowires and quantum dots; a paper by Miguel Sanchez-Garcia, Universidad Politécnica de Madrid, on impressive developments in the growth of nanowire light emitters by MBE; and a presentation by Nathan Gardner, who reviewed the progress of Glo AB towards commercial exploitation of InGaN/GaN core-shell array LEDs. Gardner's paper described core-shell devices with peak emission wavelengths ranging from 415 nm to 605 nm, peak external quantum efficiencies exceeding 35 percent, and electrical efficiencies at low currents that can be as high as 95 percent.

Fundamental studies of the growth and properties of III-Nitride nanowire structures were also discussed in Wroclaw. Shunsuke Ishizawa from the Kishino group at Sophia University, Japan, claimed that a photonic band structure had been observed in regular arrays of GaN/InGaN nanowire LEDs. This confirms a result recently reported in the literature, and one that, as Ishizawa demonstrated, has the potential to enable flexible shaping of the light beam emitted from nanoLED array devices.

Meanwhile, a French-Swiss collaboration between CEA-CNRS, Grenoble, the Ecole Polytechnique Fédérale de Lausanne and the University of Rouen, produced a GaN/AlInN core-shell structure that efficiently emitted ultraviolet light.

This paper was one of several reports at IWN describing advances in UV LED and laser technology. Progress in this field includes improvements to AlGaN crystal quality on sapphire and in LED structures. These advances have propelled external quantum efficiencies to over 3 percent for UV-C (280 nm – 100 nm) and over 6 percent for UV-B LEDs (280 nm – 100 nm), according to Cyril Pernot of Nikkiso Giken Company, Nagoya, Japan.

Challenges to realising efficient, electrically pumped UV-lasers emitting below 280 nm were outlined by Tim Wernicke of the Technical University of Berlin, while Thomas Wunderer from PARC, a Xerox company, reviewed strategies for making compact UV laser sources.

Another area of UV optoelectronics, solar blind avalanche photodiodes, was the subject of a couple of talks, including one by Russell Dupuis' group at the Georgia Institute of technology. Dupuis reported an avalanche gain of greater than 7000 at a reverse bias of 102.5 V in devices fabricated from MOCVD-grown GaN on free-standing native substrates.

Better foundations

Given the location of this international workshop, it would remiss not to report on the progress announced on free-standing GaN substrates. Two entire sessions of oral presentations were devoted to the growth of III-Nitride substrates and related issues. On top of this there were a series of excellent posters on these topics, plus a wide range of papers on optical and electronic devices fabricated on such substrates.

Close to the main entrance of Centennial Hall's is the 'Pergola' - a colossal, semi-circular, ivy-covered colonnade winding around one of the city's most magnificent and popular attractions - the multimedia fountain. Unveiled in 2009, 20 years after the first free elections in post-war Poland, Wrocław's fountain projects water up to 40 m high through an array of 300 different nozzles, which can rotate, gyrate, pulse and even create a giant screen of water. Animated projections can be displayed on this screen while music orchestrates the show through the park's speakers.

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It is well known that GaN crystals of exceptional quality can be formed via the ammonothermal method. This approach is being pursued by Ammono S.A. of Poland, Soraa of California, and Mitsubishi Chemical Corporation of Japan, and at IWN 14 all three companies reported the production of GaN crystals with excellent structural quality – high resolution X-ray diffraction curves exhibit very sharp peaks, and the material has a very low dislocation density of less than 10^4 cm^{-2}. It is these low dislocation densities that are exciting the interest of commercial chipmakers seeking an edge on the performance of the top range LEDs and transistors.

One downside of the ammonothermal method is its slow growth rate. To try and replicate the quality of these crystals while speeding up the process, Michal Bockowski and colleagues at the Institute of High Pressure Physics in Warsaw, Poland, are investigating the use of ammonothermal substrates as very effective seed crystals for the production of substrates grown by HVPE. This form of epitaxy can lead to high growth rates without recourse to the combination of high pressure and high temperature.

The Workshop also provided a stage for reporting the demonstration of a III-Nitride quantum cascade laser emitting at 5.4 THz. Speaking about this effort, Eva Monroy of the Université Grenoble-Alpes, France, reviewed the latest results on intersubband transitions in nitrides. Of particular note was the enhancement of nonlinear phenomena at 1.55 μm, obtained when GaN/AlN quantum wells were replaced with quantum dots. This result could have commercial implications, because it will be of interest to those developing optical switches and electro-optic modulators for optical fibre telecommunications networks.

As well as attending the stimulating sessions of oral presentations outlined above, delegates benefited from two lively, packed poster sessions. If anything the poster sessions were overwhelming both in the number and quality of the posters, making it impossible to view everything of interest. Maybe this is something that the organisers of IWN-2016, to be held in Florida, should bear in mind in their planning.

The International Workshop on Nitride Semiconductors was held in Wrocław Congress Centre, which forms part of Centennial Hall complex.

Debating droop

Finally, these days, what international gathering of researchers in III-Nitride science and technology can pass without a little contention over the origin of efficiency droop in LEDs? IWN-2014 did not disappoint in this respect, with the very first session on III-Nitride Optical Devices accommodating two invited talks offering differing views on the origin of this malady.

First up was an invited paper by Bastian Galler from Osram, Germany. He described a model that shows that an Auger process involving two electrons and one hole (eeh) is far stronger than that based on a one-electron-and-two-holes (ehh) Auger process. In a later paper Galler's colleague, Anna Nirschl, reported the impact of this work on droop. She described an experiment that is thought to visualise photoluminescence arising from hot charge carriers occupying a quantum well of wider band gap than the photon energy used to excite to luminescence in narrower-band-gap quantum wells. From this experiment the authors were able to attribute this high-energy emission to Auger processes.

Next up was Francesco Bertazzi of the Politecnico di Milan, Italy. He described new calculations of the Auger coefficients in the eeh and ehh processes. His group also considered the theory of hot electron transport in the structure used by the team from the University of California, Santa Barbara, and CNRS-Ecole Polytechnique in France, in their renowned experiment that enabled the detection of electron emission from an InGaN/GaN LED. Bertazzi concluded that the hot electron emission detected by the UCSB and CNRS-Ecole Polytechnique team does not derive from Auger recombination. Countering this on the last day of the Workshop Claude Weisbuch, in a tour-de-force plenary talk, eloquently defended the interpretation of the UCSB-CNRS experiment as Auger recombination being the cause of efficiency droop in LEDs.

This is an area where understanding is undergoing rapid development, so it is not that surprising that disagreement is rife. It is also worth noting that the cause of hot electron effects can be difficult to isolate, especially in complex heterostructures where very high electric fields exist, as is the case in GaN LEDs, making the quest for the origin of efficiency droop a particular challenge.

When asked, Anna Nirschl stated that the Osram Auger visualisation experiment could only account for a fraction of the leakage current observed in many LEDs under high drive currents. For Auger-sceptics and uncommitted observers alike this admission, combined with the theoretical work of the Politecnico di Milan group, means that we can expect further entertainment from a debate that seems to generate more heat than light, much as Auger recombination does.

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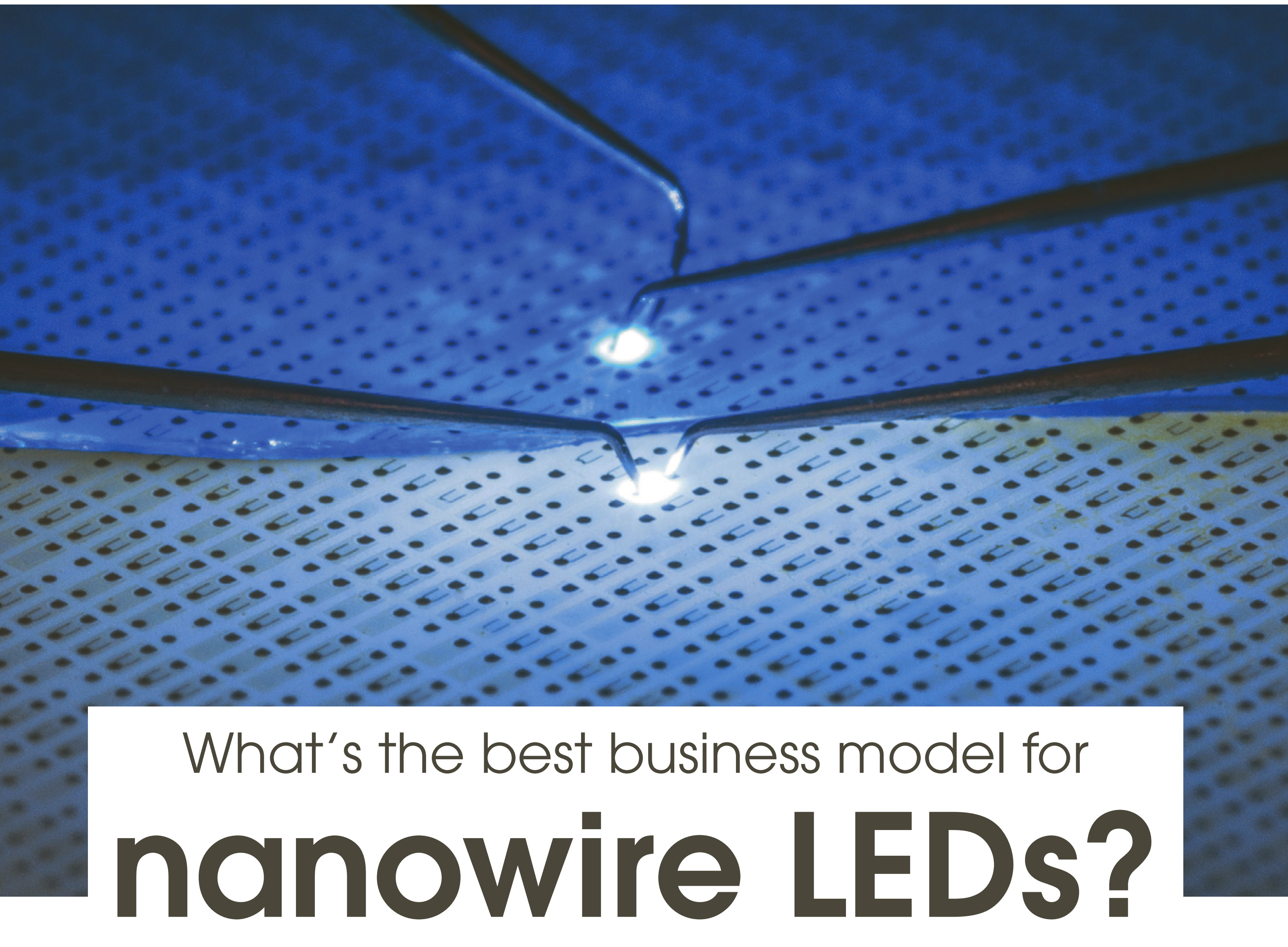


What's the best business model for nanowire LEDs?

Should developers of nanowire LEDs seek success with devices sporting diminished droop? Or should they try undercutting the cost of incumbent chips?

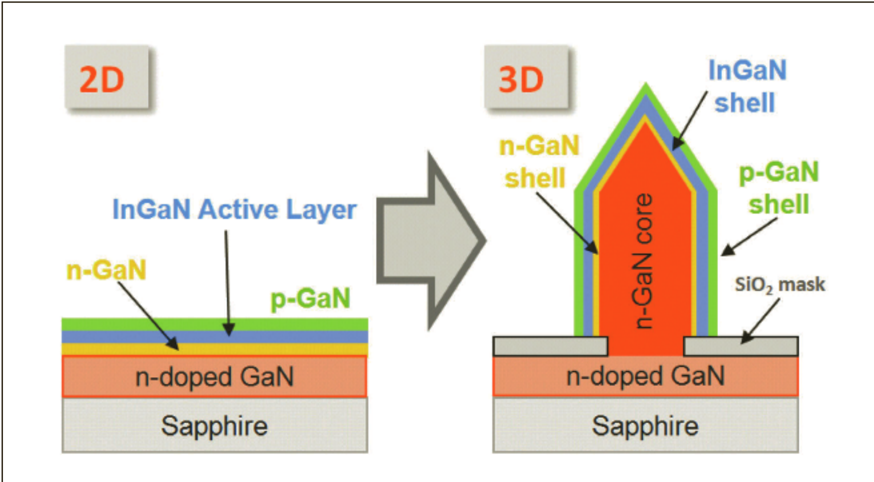
RICHARD STEVENSON INVESTIGATES

THERE ARE TWO well-trodden paths for winning market share: Make your product better than what is out there, or make it cheaper.

Both options are on the table for developers of nanowire LEDs, which are devices that are based on the growth of long, cylindrical structures from out of the plane of a substrate. The novel architecture of this device could aid the growth of indium-rich, high-quality active regions, making it easier to fabricate green-emitting LEDs; and the design can allow a trimming of the current density through the structure, leading to a reduction in droop, which is the decline in efficiency as the current through the chip is cranked up. Alternatively, nanowire LEDs could lead to plummeting production costs, if the design can slash the amount of epitaxial material required to make a device.

Today, nanowire LEDs are in their infancy, so it is not yet clear whether they can displace the traditional planar LED through superior performance, lower cost, or a combination of the two. Evaluating the potential for superior performance forms part of the activities of European projects involving one of the world's leading chipmakers, Osram, while French start-up Aledia is pursuing the opportunity for driving down device costs.

CEO of Aledia, Giorgio Anania, is convinced that by slashing chip costs, his brand of nanowire LED can compete with its conventional cousin in all markets, and can ultimately play a massive role



Nanowire LEDs and their variants have a markedly different architecture from conventional, planar devices. Osram is core-shell microrod LEDs, which are larger than their nanowire cousins, and open up the opportunity to pack phosphor between the light emitting structures.

in what will become the biggest market of all for this device, solid-state lighting. "There are seven billion people, most of them need [LED lighting to be] cheaper – they can't pay $20 a light bulb."

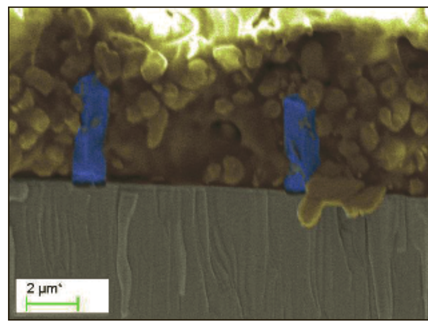
To drive down costs – it is claimed that Aledia's LEDs have the potential to be produced for just a quarter of that of incumbents – the company is pursuing a radically different design. But to understand why it is revolutionary, one must first understand what the more common approach is.

"What everyone except us has done is to start from a good crystal substrate, mask it and open holes," explains Aledia. Nanowire LEDs are then constructed by growing up from the holes a cylindrical structure that is subsequently wrapped in a series of epitaxial layers. "The trouble there is that you've got this buffer, typically a GaN buffer. You now have the whole cost of the two-dimensional LED."

The radical route of Aledia is to dispense with the buffer. This approach is clearly more risky, but if it comes off, the company not only saves money by eliminating the buffer, but also benefits from far greater freedom over the choice of the substrate. Large area silicon is currently the preferred choice, due to its low cost and the availability of sophisticated, highly capable processing equipment for this type of wafer.

Merits of the silicon foundation extend beyond low cost manufacturing. Constructing LEDs on this foundation will also help to usher in an era of smart lighting, which could be underpinned with chips featuring three-dimensional stacking technologies.

"This is a well-known technology for the semiconductor world, but one which you can only do if you are on large-area silicon, because that is where the machines and technologies are developed," explains Anania. "We happen to be the only company on the planet in that position today."



An example of nanowires fabricated by Osram and its partners: Side-view of microrods (blue) on a GaN template (grey) embedded in a micrograin phosphor and silicone matrix (yellow).

Aledia's foundations

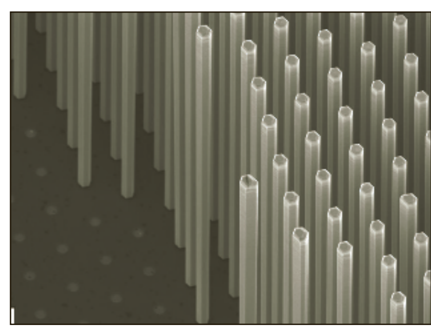
Aledia's nanowire LEDs originated in the labs of scientists at the research institute CEA-Leti. Two of the founders – COO Xavier Hugon and CTO Philippe Gilet – came from there, with Anania coming on board when the pair tried to raise investment to form a company to commercialise the device.

"They were going to be going out looking for money, but if you haven't done that before, you are lucky if you get one million," recollects Anania. The venture capitalists that were interested in backing a nanowire start-up wanted Anania to run the company, due to his success at Bookham, and he had to decide whether after leading a company of several thousand employees, he wanted to turn his hand to this. He weighed up the pros and cons, and decided to take on the challenge, reasoning: "It is high risk, it is a big technical bet, but if it works it is huge."

Since its founding in 2011, Aledia has come a long way. "When I look back at where the technology was when we did the spin out, I'm shocked that we were so foolhardy," admits Anania. "I look at the pictures now. They were wires, but you wouldn't think they were wires – they looked like bits of stones on a dirty floor."

Progress has been underpinned by €12 million of funding, which has enabled an increase in the workforce – there are now around 50 people working for the company, including some who are contracted from CEA-Leti. With development of nanowire LEDs accelerating and performance improving, 58 patents have been filed to detail and protect the innovation.

The advances that have been made have not been easy to come by, partly because worldwide efforts on this class of LED are few and far between, so it is not possible to derive much benefit from the breakthroughs of others. What's more, the growth and characterisation of nanowires is far more challenging than that of their planar cousins. "In 3D it's horrendously difficult. So many things cannot be measured – they need to be measured indirectly," explains Anania.



Angled scanning electron image of microrods produced by Osram and its partners. The microrods have a height of 40 μm at a diameter of ~900 nm and feature side facets that form a surface 15 times larger than that of the substrate they are standing on.

A sense of scale

Development of the company's products takes place on 8-inch wafers. This is significantly more costly than using far smaller wafers, but the key benefit is that it removes the need to scale up the process for production. "I don't believe the guys who say that they are on 2-inch, and when they get it to work, they'll move it up to 8-inch," remarks Anania, arguing that processes always need to be changed when introducing larger wafers.

After the company has fully mastered its growth of nanowire LEDs, it will carry out this manufacturing step in-house. Wafers will then be shipped to foundries for processing, before the chips are sent on to high-volume packaging houses. "These are not partners, these are sub-contractors," asserts Anania, adding that the final products will be LEDs and modules.

Anania is rather reluctant to discuss the possible performance of Aledia's first generation products, which might be shipped in small quantities for customer evaluation in 2015. However, he is convinced that the performance of his company's devices will steadily close the gap with their conventional cousins, rather than forever playing catch-up.

The basis for this argument is that the incumbents have hit a plateau. "The leaders have made the hero samples at 200 lumens per watt, but there is no encore possible," says Anania, pointing out that although many of the Chinese LED chipmakers are well off the pace today, they will catch up to create a commodity market. Price is then the major differentiator, playing into the hands of Aledia.

It is not clear what sector of the LED market will generate the first significant revenues for the French start-up. Anania sees opportunities in outdoor displays, where the brightness of nanowire LEDs will be a major asset, and he thinks they could also have a role to play in the automotive industry. Another opportunity is in screens, which are currently dominated by LED-backlit liquid-crystal displays. Here, Anania predicts that nanotechnology will take over, because this is inherently superior for forming pixels: "Each LED is an emitter, and you've got no edge effects."

The ultimate application is solid-state lighting. Anania believes that the company will ultimately crack this market, because the efficacy of its nanowire LEDs can climb to hundreds of lumens per Watt. Thanks to growth of material on the *m*-plane, these devices are not plagued by the internal electric fields that hamper the output of their conventional cousins, so they should be able to outperform them.

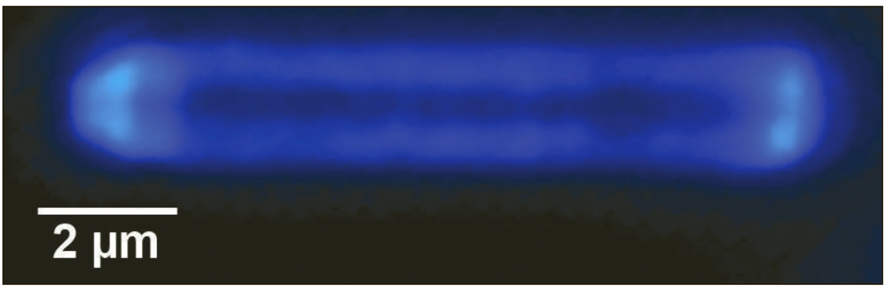
Different planes

In part of the project SMASH – smart nanostructured semiconductors for energy-saving light solutions – scientists evaluated the merits of nanowire LEDs in more detail. Martin Strassburg, a partner in the project who works for Osram Opto Semiconductors, told *Compound Semiconductor* that the internal quantum efficiency for nanowires is typically 65 percent, compared to 85 percent for conventional *c*-plane LEDs.

This shortfall is a major impediment to a high output power: The lack of an internal electric field within the device means that there is a relatively small difference in wavelength between absorption and emission, allowing reabsorption to contribute to losses from the active region. In order to form devices with a high external quantum efficiency, internal quantum efficiency must reach the realms of 80 percent.

One advantage of the 'core-shell' nanowire LED, according to Strassburg, is that it can suffer from far less droop than its conventional cousins: "Due to the increase in active area, we can reduce the effective current density by a factor of ten. You are then able to operate the blue LED at its maximum internal quantum efficiency." With green

An array of core-shell microrods emitting blue light under resonant excitation with an ultraviolet light source. The bright spot in the centre is an artifact due to blooming effects.



Single core-shell microrod lying on its side and emitting blue light under resonant excitation with an ultraviolet light source. Because of wave-guiding effects, the ends appear brighter than the side facets.

LEDs, droop is more pronounced, so this type of nanowire can only operate nearer its maximum, but this still leads to a substantial increase in light output at reasonable drive currents.

Those working in the SMASH project hoped that nanowires could trim defect densities in LEDs, thanks to strain relief. Although this happened in some areas of the device, next to them were regions with higher defect densities. "We ended up more or less abandoning this part of development, because the grain sizes were much smaller than the chip size would be. But it was good to know that this was a dead end, and should not be pursued further," reflects Strassburg.

Researchers in the SMASH project also explored the development of quantum disc nanowire LEDs, which have the layers of the structure separated vertically along the protruding wire. Such a structure could, in theory, be formed by growing a conventional LED and then etching away material from the top to form wires. Obviously, however, it is better to employ a 'bottom-up' approach: This cuts material costs and can lead to longer-wavelength devices, because more indium can be incorporated into the active region without impairing crystal quality.

Encouragingly, the internal quantum efficiency of MBE-grown, green-emitting nanowires sporting this disc architecture exceeds that of their planar cousins. However, these results cannot be replicated when this class of nanowire is grown by MOCVD, the preferred technology for high-volume LED manufacture. Due to this issue, Osram is not currently pursuing this disc-in-a-nanowire architecture.

One area where Osram is active is in the development of LEDs that share some hallmarks of the nanowire devices, but are a bit bigger. Referred to as microrod LEDs, these structures are 10-20 μm high, have a diameter of around 1 μm, and are spaced apart by between 2 μm and 5 μm.

With this geometry, it is possible to pack a phosphor between the LEDs. "The phosphor has a grain size of about ten to thirty microns, but if you put it in a mill and reduce the diameter, you can have it so small that you can fit it in between the space of the nanorods."

Placing the phosphor up against the microrods leads to a hike in performance, according to Strassburg, who explains that *m*-plane emission is easily extracted to the side facets, where it cannot be re-absorbed, but goes directly into the phosphor. Here the light is converted and cannot be reabsorbed by the microrods, thus trimming the losses associated with the LED. What's more, thanks to being closer to the chip, the phosphor temperature is probably about 20 °C lower than if it were remote, enabling the LED to operate at a higher efficiency for more hours.

Although these microrod LEDs may feature a completely different active area morphology, incorporated in a package, they would look just like today's products. "That's why these nanowires, in combination with a phosphors, are a mid-term replacement – unless there is some fundamental limitation of the internal quantum efficiency."

Osram is looking at this, partly through a project entitled GECCO that involves partners from Germany, Spain, Poland and the UK. As they make progress, and Aledia refines its nanowire LEDs for commercial launch, it will be interesting to see if reports of nanowire LED development appear from other leading chipmakers – and further ahead, what emerges as the best business model for the nanowire LED.

- *Compound Semiconductor* contacted LED nanowire developer Glo during the preparation of this article. Glo declined the opportunity to be interviewed.

Anania's view on GaN-on-silicon LEDs

Recently, GaN LEDs grown on large silicon substrates have hit the headlines as a route for cutting chips costs. Anania, however, does not expect this form of LED to take the industry by storm: "Two or three years ago, there was the belief that you could really lower the costs by doing that. I think that's gone away."

Anania argues that while the likes of Osram have developed the technology, they are not using it for high-volume chip production because the savings aren't big enough. "The performance is less good, the yield is less good, the MOCVD time is doubled and the amount of GaN you need is twice as much." According to Anania, the cost saving is only about 25 percent when switching to a silicon platform, so whether this is worthwhile depends on the existing infrastructure of the company: "If you happen to be Samsung and you have empty 8-inch fabs, then it makes sense, because it's not going to cost you anything to do it. If you are Osram and you don't have any 8-inch fabs, you've got 6-inch sapphire and it's pretty good stuff, the cost-delta isn't all that big."

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Larger wafers
slash GaN MMIC costs

High-quality wafers processed on a 150 mm GaAs fabrication line promise lower GaN MMIC production costs

BY PHILLIP SMITH, PC CHAO AND RICH ISAAK FROM BAE SYSTEMS AND IVAN ELIASHEVICH FROM IQE

RF AND MICROWAVE POWER amplification is undergoing a revolution, thanks to the development of the GaN HEMT. By switching from the previous incumbent material, GaAs, to the wide bandgap alternative, GaN, it is possible to achieve the same electron mobility and high frequency response as GaAs with an order of magnitude hike in RF power density, which stems from a five-fold increase in breakdown voltage and a doubling of drain current. Consequently, when GaN HEMTs are constructed with today's industry-standard processes and sport gate lengths ranging from 0.15 μm to 0.5 μm, they can deliver wide bandwidth, high power and high efficiency at frequencies ranging from 0.1 GHz to 100 GHz.

To exploit these demonstrated performance advantages in commercial and military systems, many groups from around the world have turned their attention to improving the affordability of this GaN transistor technology. To drive down costs, they are scrutinizing several factors: the price of materials, which includes starting wafers, metals and chemicals; labour; process yield; and process uniformity.

Properly evaluating the cost of new technologies is not trivial, and it is possible to compare the affordability of GaN MMICs in different ways. Judged in terms of a key metric – dollars per watt of RF output power – GaN HEMTs produced on 100 mm SiC substrates already undercut their GaAs cousins formed on 100 mm and 150 mm wafers. However, superiority on that front is often outweighed by the comparatively higher price of individual GaN chips, and this higher outlay is still seen by many as an impediment to far greater deployment of this class of device.

One approach to increasing sales of GaN MMICs is to take the well-trodden path for trimming production costs employed within the semiconductor industry. This involves introducing larger wafers, exploiting the economies of scale afforded by batch processing. In the high-volume silicon fabs, ICs are now produced on 300 mm wafers, and migration to a 450 mm platform is under consideration. Similarly, GaN-on-SiC migrated from 50 mm wafers to 75 mm and 100 mm variants over the past decade, with material suppliers II-VI and IQE having recently gone even further – in 2013, IQE unveiled 150 mm GaN-on-SiC epiwafers based on advances in SiC substrates and epitaxial growth.

Yield must not be compromised, however, if the introduction of larger wafers is to lead to substantial cost saving – and history attests that accomplishing this feat can be quite challenging. In the 1980s, when MESFET makers transitioned to larger wafers, there was initially a drastic falloff in yield. Primary reasons for this were a lack of control and non-uniformity in gate recess depth that resulted from a process based on time-of-flight wet etching (later, this weakness was mitigated by the introduction of spray etchers).

Parameter	100mm	150mm
Usable Wafer Area	1	2.4
Chip Sites per Wafer	1	2.4
Epi Wafer Cost	1	1.2
Process Cost (labour, chemicals etc.)	1	1.2
Total Cost per Processed Wafer	1	1.2
Fab Cost per Good Chip	1	0.50

Table 1. Relative cost of 150 mm versus 100 mm GaN-on-SiC processes, normalized to 100 mm. Usable wafer area subtracts a 5 mm unusable epi/process ring along the outer edge of each wafer, and cost per good chip assumes yield is maintained at the same level as wafer size is increased.

Note, however, that migration to larger wafers does not necessarily have to cause yield to nosedive. In the 1990s, MMIC foundries were able to cleverly combat yield loss when scaling pHEMTs by adding etch-stop layers to the epitaxial structure and employing selective recess etching. With these process refinements, engineers realised excellent gate recess etch uniformity, limited primarily by starting wafer uniformity.

Our team at BAE Systems has enjoyed a similar experience as we have scaled our GaN-on-SiC HEMT process to make it suitable for 150 mm wafers. One of the merits of many GaN-on-SiC HEMT processes, including our own, is that they require no gate recessing. Consequently, device and circuit uniformity is highly dependent on epilayer uniformity – and if the starting wafer is uniform, GaN devices, if fabricated carefully, can be nearly as uniform.

We have calculated that per-chip fabrication costs can plummet by 50 percent when the GaN-on-SiC process is migrated from 100 mm to 150 mm wafers (see table 1). Note that this analysis does not include the additional cost of back-end steps, such as on-wafer test, wafer dicing and chip inspection. These post-processing steps become somewhat more efficient with larger wafers, but the gain is not nearly as high as the two-fold improvement associated with fabrication. This is a drag on the overall reduction in chip cost, which in practice is typically 40 percent.

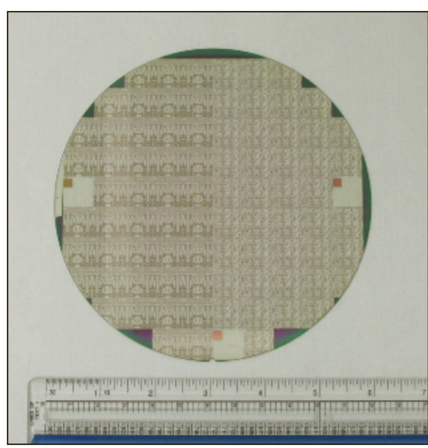

Figure 1. A fully processed 150 mm GaN HEMT MMIC wafer.

In our case, the benefits of switching GaN-on-SiC MMIC production to a 150 mm line are more than just a trimming of chip fabrication costs due to scaling. Visual and line yields are also higher, thanks to increased automation, and fewer wafers are required to meet customer delivery quantities, lowering cost associated with wafer qualification. What's more, because we have been running 150 mm GaAs processes (MESFET and PHEMT) in our facility for more than a decade, we are able to draw on a great deal of relevant expertise. This has helped us to demonstrate the industry's first 0.2 μm GaN MMIC process on 150 mm SiC substrates (see Figure 1).

Other firms are moving in a similar direction, with plans to release processes on wafers of this size – for example, RFMD announced that in 2014 it will release a process with a 0.5 μm gate length that is targeted at low frequency commercial applications. In comparison, the gate length for our processes is just 0.2 μm, so our MMICs are widely applicable for defence applications at frequencies up to around 50 GHz.

Choosing the right material

Production of all of today's GaN RF devices and MMICs is undertaken on one of two competing material systems – GaN is deposited on substrates made from either silicon or SiC. When grown on the former, there is a potential cost advantage, in part due to the ability to scale to larger wafers, such as those with 200 mm diameters. However, this advantage has to be weighed against the inferior thermal conductivity and electrical resistivity of the silicon substrate, which compromises both the high frequency and power performance of devices and circuits fabricated on this foundation.

For high-reliability military applications, this compromise is generally unacceptable, making GaN-on-SiC the preferred technology. Devices made with this combination of wide bandgap materials feature an intrinsically higher thermal conductivity for the substrate that results in lower channel temperature, which improves both the performance and long-term reliability of GaN power amplifiers produced in the process.

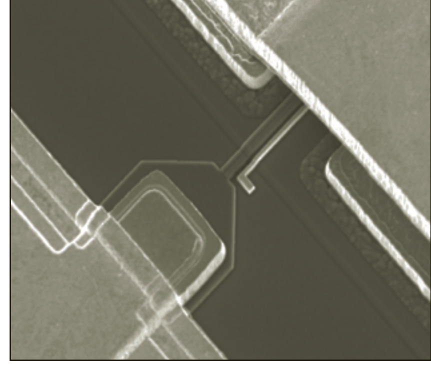

Figure 2. 0.2 μm gate-length field-plate GaN HEMT device.

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The epiwafers that we process on our 150 mm line feature an AlGaN/GaN structure with a thin GaN cap and an iron-doped GaN buffer. This particular heterostructure provides a high sheet-charge density for high full-channel current and output power while maintaining good reliability.

Our starting material is provided by epiwafer manufacturer IQE. Growth of the nitride epilayers takes place on the 4H polytype of SiC that is loaded into a state-of-the-art multi-wafer production MOCVD reactor, which is capable of delivering improved uniformity over larger wafer areas. Wafers exhibit a low density of defects, with the majority being substrate-related micropipes and polytypes. Sheet resistance uniformity is 1.2 percent, which is slightly better than that for theheterostructures grown on 100 mm predecessors; and compositional uniformity is excellent, with variations in aluminium content of below 1 percent.

Figure 3. Scanning electron microscopy image of fully plated-through 60 µm square vias.

One of the challenges associated with hetero-epitaxial growth is the warping and bowing of epiwafers, which stems from differences in lattice constant and thermal expansion coefficient between the epitaxial layers and the substrate. In the worst cases, epiwafers can even crack. However, even deviating from being perfectly flat by a fraction of a millimetre can render wafers unsuitable for processing.

Our 150 mm GaN-on-SiC epiwafers are formed on substrates that are 500 µm thick. This is similar to the thickness of the substrates used for the 100 mm GaN-on-SiC process, and the reduction in thickness-to-diameter ratio associated with scaling has meant that it was initially a challenge to realise an acceptable warp.

> "Comparisons of output power and power-added efficiency at 4 GHz for wideband GaN MMIC power amplifiers formed on 150 mm and 100 mm wafers are favourable, with the larger format leading to marginally better performance and a tighter distribution."

To address this, engineers at IQE performed a series of experiments, and used their findings to refine their processes so that bow and warp for the 150 mm epiwafers could be reduced from in excess of 100 µm to typically 40 µm. This level of warp is suitable for high-yield wafer processing.

Processing and performance

Automated cassette-to-cassette equipment is employed in our 150 mm line, leading to reduced manual wafer handling and increased yield. With this tool-set, our development of a process for 0.2 µm GaN-on-SiC MMIC fabrication has been quite straightforward – the bulk of the effort went into optimizing the existing 100 mm GaN mesa, ohmic, nitride deposition and via-hole formation processes using 150 mm tools to achieve good uniformity and yield on the wafers (see Figure 2 for a scanning electron microscopy image of a representative GaN HEMT device, where the 0.2 µm gates and field plates are patterned using electron beam lithography).

We have also developed a 150 mm backside process. Although some of the process steps and tools required for this – such as the SiC grinding machine – have taken time to establish, we have not noted any backside process-related issues. Thickness uniformities of less than 5 percent are possible across wafers with a final thickness of 100 µm (see Figure 3 for an example of fully plated-through via holes produced as part of this backside process).

To test the capability of devices produced on 150 mm wafers, we subjected these transistors to a series of DC and RF tests, comparing their performance to those fabricated on the 100 mm line. Results are favourable, with HEMTs produced on 150 mm wafers exhibiting a two-terminal gate-to-drain breakdown in excess of 90 V, which is comparable to equivalents fabricated from 100 mm wafers. At a drain-source voltage of 10 V, transistors formed on 150 mm wafers have an average normalized maximum drain current of 1,124 mA/mm, a peak transconductance of 372 mS/mm and pinch-off voltage of -3.1 V.

Compared to devices formed on 100 mm wafers, drain current and transconductance are superior by about 5 percent, and pinch-off voltages are very similar (see table 2). The specification yield for these three DC parameters is 100 percent, as measured on 30 sites across the

Parameter	100mm Value	150mm Value
I_{max} (mA/mm)	1075 ± 10%	1124 ± 5%
g_m (mS/mm)	355 ± 10%	372 ± 5%
V_{po} (V)	-3.3 ± 5%	-3.1 ± 5%

Table 2. Comparison of key DC parameter values and uniformity, 150 mm versus 100 mm at V_{ds} of 10 V.

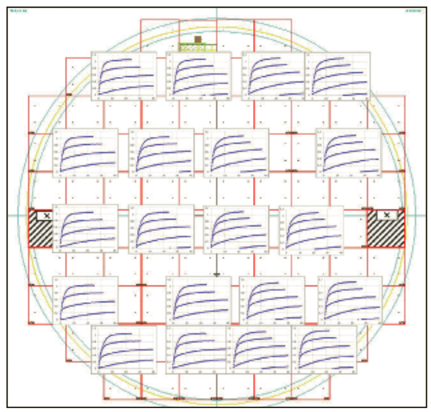

Figure 4. Mapping of 0.2 μm GaN HEMT pulsed current-voltage characteristics across a 150 mm wafer, pulsed at Vg = -5V, V_{ds} = 30 V. Excellent pulsed current uniformity and device yield are observed.

Development of affordable GaN MMICs will enable the fielding of advanced electronic warfare systems on aircraft such as the F15. Credit: US Air Force

150 mm wafer. Somewhat unexpectedly, switching fabrication from 100 mm to 150 mm wafers actually led to improved uniformity for some DC characteristics, such as maximum drain current and transconductance. We attribute this to the enhanced starting wafer uniformity and quality, plus the improved process control of the 150 mm fabrication line.

Results of pulsed current-voltage characteristics are also encouraging, with devices formed on 150 mm wafers giving similar levels of performance to those made from 100 mm material. Pulsed current uniformity and device yield are excellent, according to GaN HEMT pulsed current-voltage characteristics across a full 150 mm GaN-on-SiC wafer (see Figure 4).

Comparisons of output power and power-added efficiency at 4 GHz for wideband GaN MMIC power amplifiers formed on 150 mm and 100 mm wafers are also favourable (see Figure 5), with the larger format leading to marginally better performance and a tighter distribution. RF spec yield is also better, rising from 70 percent to 76 percent, according to full on-wafer RF testing.

Lastly, MMIC final-visual-yield has increased with the migration to larger wafers, rising from 85 percent to 95 percent. We expect this improvement stems from the reduction in manual wafer handling resulting from the use of automated 150 mm equipment, and we note that it is consistent with improvements we saw after transitioning our 75 mm GaAs MESFET and PHEMT processes to 150 mm wafers.

The improvements in visual yield, along with the higher proportion of devices meeting RF criteria, has culminated in overall chip yield per wafer rising from 59.5 percent to 72.2 percent for the MMIC example shown. This exceeds the assumption made for Table 1 that 100 mm yield would be simply maintained at the same level on 150 mm wafers, and makes an even more compelling argument for the improvement in affordability wrought from scaling. This will help to cut the cost of GaN MMICs, and should spur their uptake in various defence applications at many important frequency bands that the 0.2 µm gate length GaN process targets.

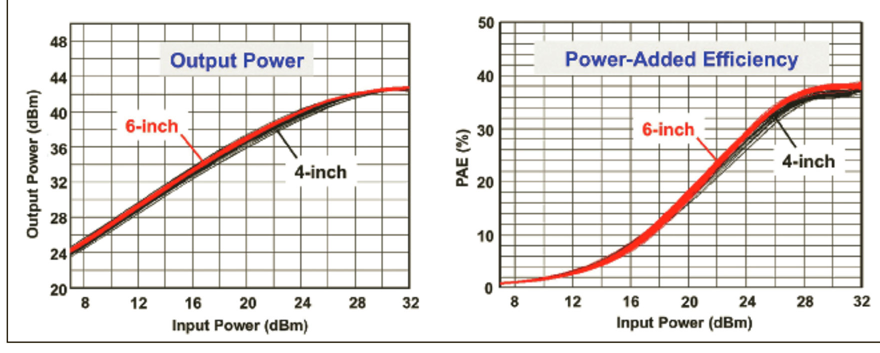

Figure 5. RF performance (Pout and power-added efficiency) comparison for a wideband (0.5-5 GHz) MMIC power amplifier fabricated on 100 mm and 150 mm wafers. Comparable performance (slight improvement in PAE), somewhat tighter distributions and higher RF spec yield have been observed for early 150 mm wafers. Data shown was taken at 4 GHz with 28 V V_{ds}.

Further reading

R. Isaak et al, "The First 0.2 µm 6-Inch GaN-on-SiC MMIC Process," CS ManTech Conf., May 2014, pp. 229-231.

L. Gunter et al., "The First 0.1 µm 6" GaAs PHEMT MMIC Process," CS ManTech Conf., April 2006, pp. 23-26.

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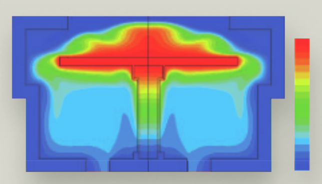

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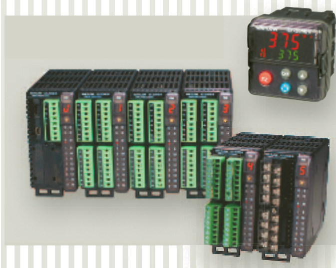

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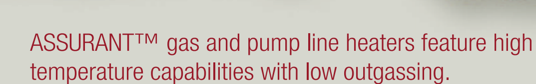

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AlN substrates propel performance improvements in **ultraviolet** LEDs

Single-crystal, high-quality AlN substrates underpin the production of bright, reliable ultraviolet LEDs delivering superior wavelength stability

BY LEO SCHOWALTER of CRYSTAL IS

TO ANALYSE AND MANIPULATE DNA, scientists begin by determining the purity of this life-determining molecule. Purity and concentration levels are exposed by measuring the absorption associated with DNA and protein, which have peaks in the ultraviolet region of the electromagnetic spectrum at wavelengths of 260 nm and 280 nm, respectively. Armed with this information, it is then possible to uncover genetic disorders, create DNA fingerprints of individuals, and make genetically engineered organisms that enable the manufacture of products such as insulin, antibiotics, and hormones.

Absorption measurements of DNA and proteins are often carried out using mercury, deuterium and xenon flash lamps, which can also serve many other established markets, such as those involving the disinfection of water and air and the curing of resins. However, that does not imply that these lamps, which emit in the UVC range that spans 280 nm to 100 nm, are great sources of ultraviolet radiation: They are fragile, bulky, lack portability, and are not particularly efficient.

A very attractive alternative to these ultraviolet lamps is the LED that emits in the UVC range. This solid-

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state light source can be an efficient, cost effective, and more environmentally friendly replacement that is wavelength specific. What's more, it promises high optical output, long lifetime, low power consumption and low maintenance costs.

UVC LEDs are already available today, having been introduced to the marketplace several years ago. Unfortunately, initial products failed to live up to their billing, delivering a low output power and suffering from a lack of reliability. These weaknesses have impeded the uptake of this technology.

Today, this situation has changed, with far better devices available. Improvement in the marketplace has been driven by our efforts at Crystal IS of Green Island, NY, where we manufacture a portfolio of high-performance UVC LEDs. These products owe their superiority to their foundation – high quality, single-crystal AlN. Depositing epilayers on this substrate, rather than the more conventional sapphire, allows the growth of pseudomorphic $Al_xGa_{1-x}N$ layers with very low defect densities. The devices that result, which premiered earlier this year under the brand name Optan, are made with processes employed for

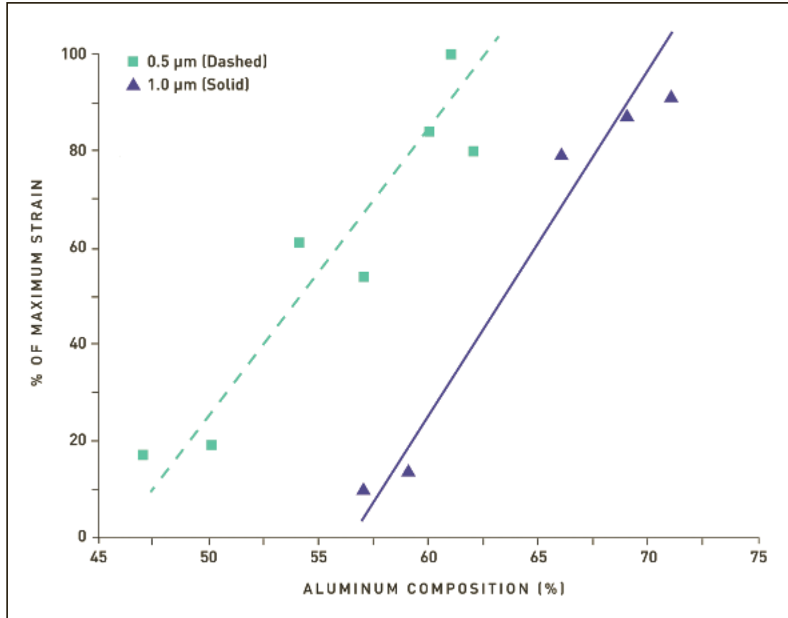

Figure 1. The percentage of maximum (psuedomorphic) strain as a function of aluminium composition for layers with different thicknesses. Dashed and solid lines are provided as guides to the eye for each thickness.

manufacture of visible LEDs. They offer industry-leading light output, superior lifetime and reliability, and excellent spectral quality.

Building on AlN

Ultraviolet LEDs and their visible cousins have several things in common – they are both formed by depositing, via MOCVD, a stack of epilayers from the AlN/GaN/InN materials system. However, they differ in material composition. For devices emitting in the visible or near ultraviolet and serving the multi-billion dollar lighting industry, aluminium content is low, and the LED is rich in gallium with indium. To reach the far shorter wavelengths of the ultraviolet UVC range, far more aluminium is required, along with proportional decreases in gallium.

Visible and ultraviolet LEDs are often formed on sapphire. This foundation meets the temperature and chemical compatibility requirements for hetero-epitaxial growth of III-nitride semiconductors, but film deposition is hindered by large lattice and thermal expansion mismatch. This gives rise to a high density of defects, which is a far more significant problem in UVC LEDs than those emitting in the visible, because as the emission wavelength gets shorter, the defects have a bigger impact on internal quantum efficiency.

It is possible to reduce the density of defects in GaN-on-sapphire UVC LEDs by employing novel epitaxial growth techniques. However, a far bigger gain is made by turning to pseudomorphic growth of high-aluminium-content AlGaN layers on AlN substrates. To realise this, we have developed a technology to grow large diameter boules of high quality AlN; and developed techniques to obtain high quality, pseudomorphic growth of AlGaN on this single-crystal foundation.

Here we will focus on describing our efforts at addressing the latter challenge – the pseudomorphic growth of AlGaN on AlN (note that the growing of high-quality boules of AlN by our team is described in many papers, such as *Structural and Surface Characterization of Large Diameter, Crystalline AlN Substrates for Device Fabrication* (published in *Journal of Crystal Growth* **310** 887 (2008))).

Development of our AlGaN-on-AlN growth process began with a project to determine the pseudomorphic limit for these substrates. We carried out various growth experiments, using different compositions and thickness for *n*-type $Al_xGa_{1-x}N$ layers. This led to the deposition of a range of layers – from almost completely relaxed to completely strained (Figure 1).

This series of experiments determined that if the aluminium content is around 60 percent, layers can be grown fully pseudomorphic up to a thickness of 0.5 mm; and if the aluminium content is as high as 70 percent, layers with a thickness of 1 mm can be formed that are pseudomorphic. The great strength of pseudomorphic growth is that it does not lead to the generation of misfit dislocations, so no new threading dislocations are

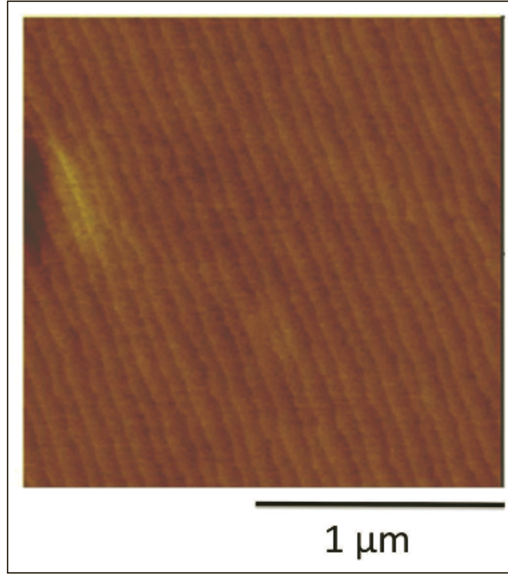

Figure 2. Step-flow growth is revealed by atomic force microscopy images of pseudomorphic $Al_{0.7}Ga_{0.3}N$. The root-mean-square roughness is just 0.1 nm, and the height range of the image is 1.7 nm.

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generated. Consequently, it is possible to grow thick layers with a density of threading dislocations comparable to that found in the starting substrate. Armed with the information uncovered in this study of AlGaN films, we can ensure that very few dislocations are generated during hetero-epitaxy.

To realise high-quality epistructures, we have produced *n*-type $Al_xGa_{1-x}N$ with a smooth surface, in order to create sharp interfaces in the *p–n* junction and thin active region. Through experimentation with roughening surfaces and optimisation of the proportion of aluminium in $Al_xGa_{1-x}N$ layers, we found that $Al_{0.7}Ga_{0.3}N$ layers can be deposited with very smooth surfaces (see Figure 2). According to atomic force microscopy, these layers typically have a step flow growth pattern with atomically smooth surfaces over areas of 2 x 2 μm^2.

One of the biggest challenges in incorporating $Al_{0.7}Ga_{0.3}N$ into our LEDs is that it can be plagued with a low conductivity. As aluminium concentration increases, conductivity tends to fall, due primarily to the reduced mobility and deeper level for the donors in the conduction band. However, by optimizing doping levels and growth conditions, it is possible to increase conductivity to a level suitable for incorporation in LED structures.

We have produced LEDs containing a high aluminium-content electron-blocking layer, a *p*-type $Al_xGa_{1-x}N$ hole injection layer and a *p*-type GaN contact layer. Thanks to a low surface roughness, as verified by atomic force microscopy (see Figure 3), allied to a low defect density, these devices deliver a very high level of performance.

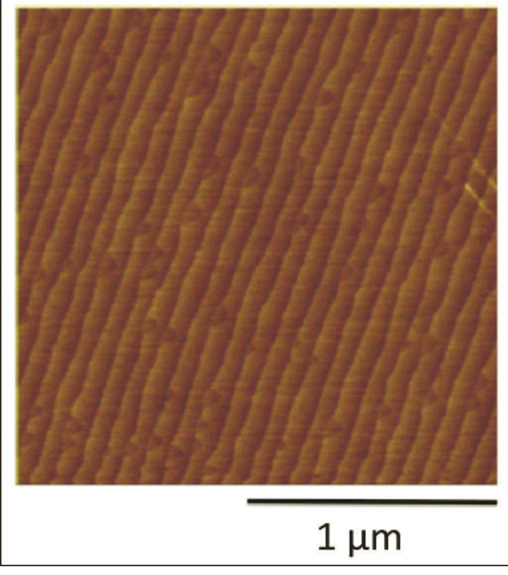
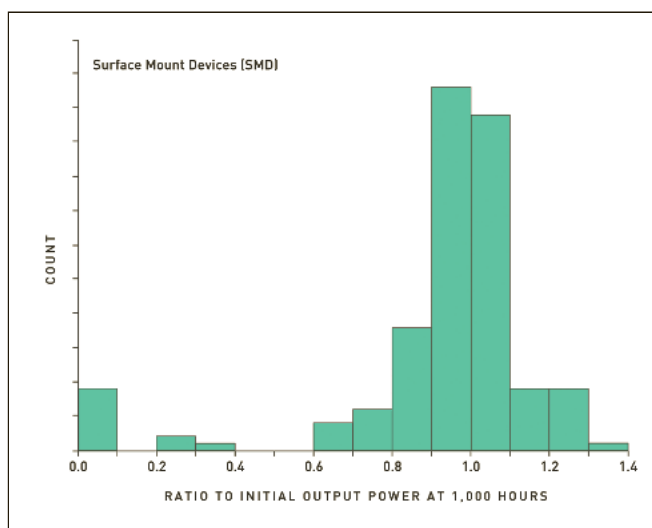


Figure 3. Step-flow growth during the deposition of the UVC LED structures is revealed by atomic force microscopy. The root-mean-square roughness is just 0.2 nm, and the height range of the image is 1.6 nm.

This is only possible when a device has a low density of defects, because these imperfections give rise to non-radiative recombination, with injected carriers generating heat rather than ultraviolet emission.

Driving down defects and realising high internal quantum efficiency is not a guarantee of great performance – to do that, photons must also be extracted from the chip with high efficiency. This is non-trivial, because nitride semiconductors have a relatively large index of refraction, which results in a relatively narrow escape cone for photon extraction. If photons approach the semiconductor-air interface at an angle greater than the escape cone they undergo total internal



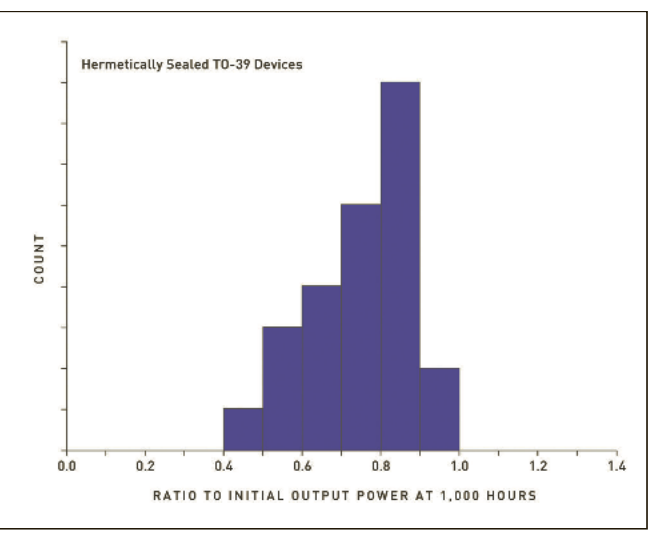
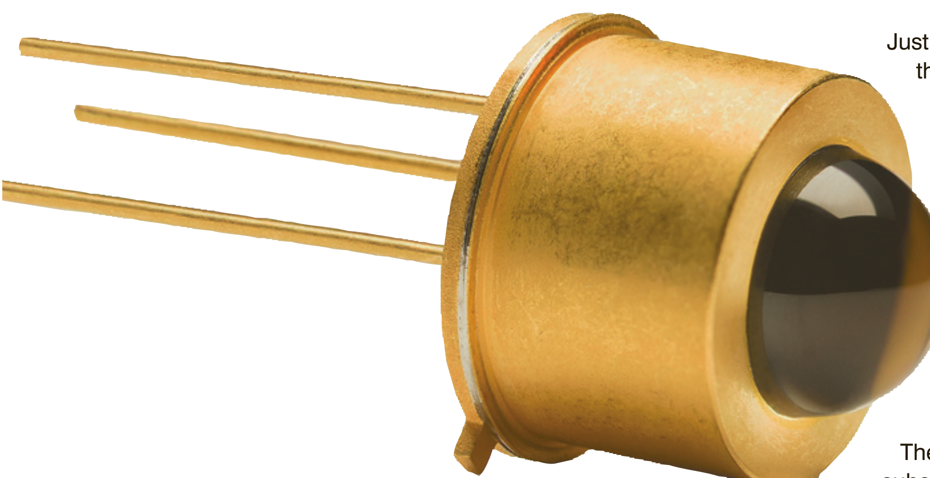


Figure 4. Housing UVC LEDs in a hermetically sealed TO-39 package, as the devices in the right figure, prevents the failure of devices after 1000 hours of continuous-wave operation at a drive current of 100 mA



reflection, and it is likely that they will be absorbed before multiple reflections bring them to within the escape cone.

To minimise the proportion of photons trapped and lost within the ultraviolet LED, we employ a variety of extraction techniques. They have been adapted from standard techniques used to increase the output of visible LEDs, with processes tailored for the materials used in ultraviolet emitters.

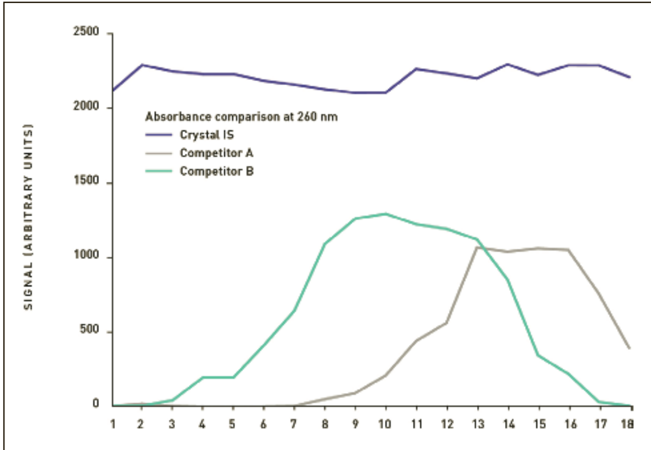
Better, brighter devices

Devices that result combine high brightness with a high level of reliability. Optical measurements on 170 LEDs in a lead frame package, run at 100 mA for 1,000 hours in continuous wave (CW) operation, reveal that the median LED emits just over 97 percent of its initial output (see Figure 4).

Just 21 devices, equating to 12.4 percent of the sample size, emit less than 40 percent of their initial output after 1000 hours. Many of them deliver no light by the end of the test, due to a malfunction of the contact metallization or packaging. Analysing the failed devices reveals corrosion and metal migration, often exacerbated by environmental conditions. Encouragingly, a sample of 40 devices in a hermetically sealed TO-39 package exhibited no failures of this nature.

These results show that single-crystal, AlN substrates can lead to brighter, more reliable devices. But that's not all: This superior foundation also leads to LEDs that deliver a more consistent emission wavelength and emission peak fidelity, without sacrificing efficiency gains. This means that they are better suited to satisfying the needs of those looking to determine the purity and concentration of samples, such as DNA. The increased light output stability – which ensures consistent and repeatable measurements – can be seen in tests that compare our LEDs to those of UVC LEDs produced by other chipmakers (see Figure 5). These investigations highlight the stability of our LEDs with a peak wavelength of 260 nm and 280 nm.

Our efforts at developing AlN substrates will continue, and in turn this should lead to further gains in the performance of UVC LEDs. Brighter, more reliable devices will follow, and the number of applications that can be addressed by the ultraviolet LEDs will continue to rise.



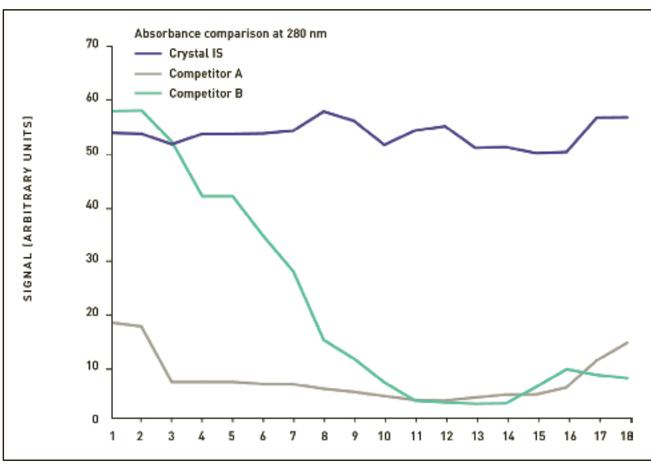


Figure 5. Thanks to a high-quality, single-crystal AlN substrate, the wavelength stability of UVC LEDs manufactured at Crystal IS is superior to that of rival devices.

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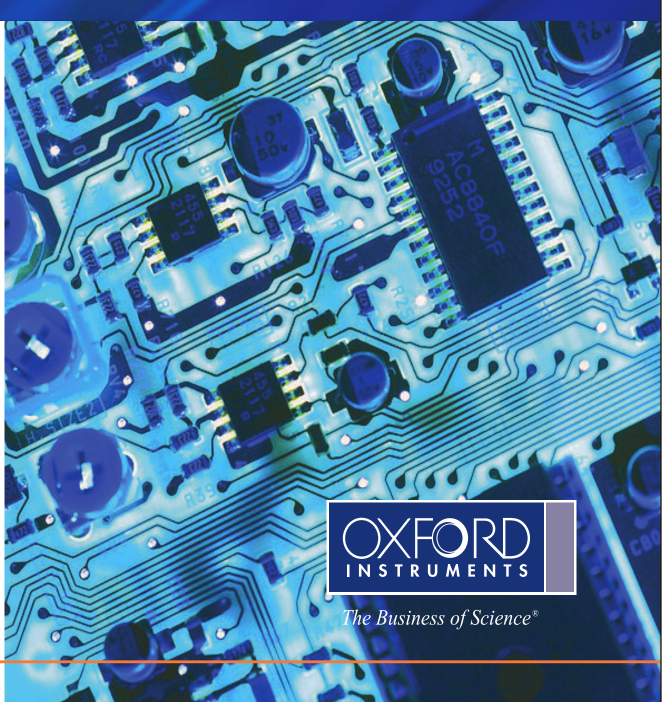

Improving modeling of high-efficiency solar cells

Analytical models accounting for reflections and photon recycling provide accurate predictions of device results.

BY MATTHEW LUMB from the GEORGE WASHINGTON UNIVERSITY and THE US NAVAL RESEARCH LABORATORY, ROBERT WALTERS from the US NAVAL RESEARCH LABORATORY and MYLES STEINER and JOHN GEISZ from THE NATIONAL RENEWABLE ENERGY LABORATORY.

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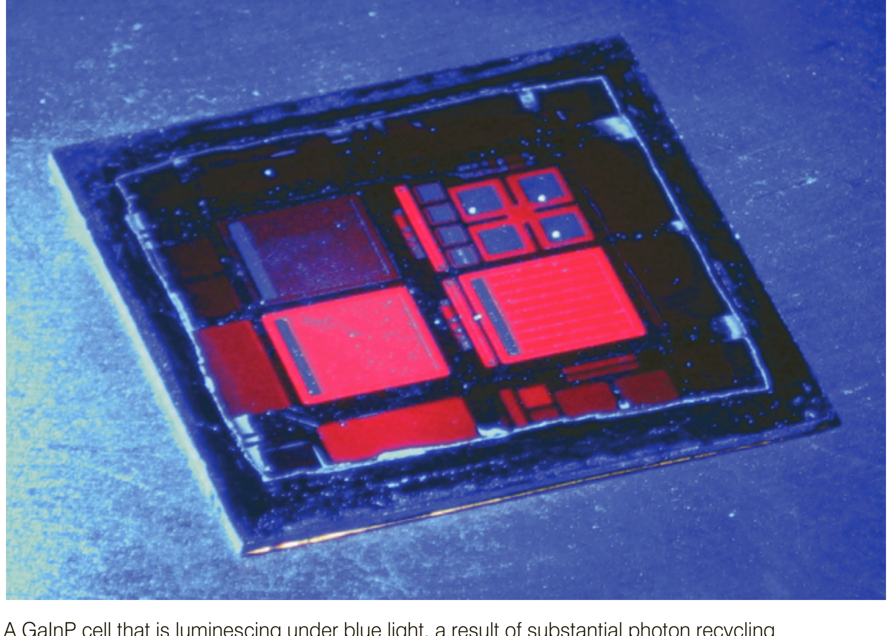
MANY RESEARCHERS IN THE SOLAR SECTOR are pursuing the same goal – to come up with a technology that increases photovoltaic efficiency. It's a worthwhile aim, because if a cell can extract more electrical energy from the sun's rays, solar power may become more affordable, leading to increased sales and better economies of scale.

Several approaches are available for developing higher efficiency cells. One option is to design and evaluate a new architecture in the lab, and an alternative approach is to model new device designs to see if they are superior. In practice, a mix of both these approaches tends to work best, with measurements on real devices verifying the capability of a new cell design that produces promising results in modeling efforts.



A GaInP cell that is luminescing under blue light, a result of substantial photon recycling enhancement due to the back reflector.

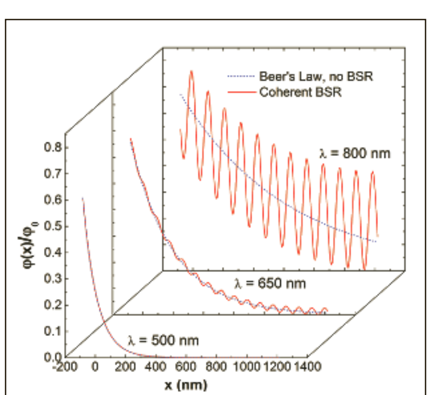
Whatever materials are used to build a conventional solar cell, ultimately efficiency is limited by a fundamental process: radiative recombination. It follows from the reciprocity of absorption and emission processes that if all other loss mechanisms are entirely suppressed, the resulting, perfect solar cell would also, in fact, be a perfect LED.

This relationship between a faultless LED and a solar cell has been known for many, many years, and in the 1950s it was employed by Nobel-prize-winning physicist William Shockley and co-worker Hans-Joachim Queisser to derive the efficiency limit for a solar cell. This model, which accounts only for band-to-band radiative recombination of electron-hole pairs, assumes that all other processes are ideal. It is widely used by researchers in the photovoltaics community today, and one of its strengths is that it is able to express the potential of competing technologies in the simplest terms. However, real world solar cells are seldom close to ideal. Efficiency is impaired by optical losses, non-radiative recombination and electrical losses, which usually combine to make the Shockley-Queisser limit a gross overestimation.

Models that can provide a more realistic value for efficiency are highly desired, because they can aid efforts to improve solar cells. This need is particularly acute for III-V cells, which come closer than many other material systems to reaching their fundamental limit, thanks to advances in epitaxy, processing and optical management. In space, these cells are united with those made from germanium to power satellites, and in sunny climes these cells lie at the heart of power generation systems featuring mirrors or lenses that focus the sun's radiation by factors of several hundred or more.

In the 1970s, Harold Hovel and Jerry Woodall introduced a more sophisticated model that is better at capturing the performance of single-junction cells. This pair of researchers, who were working at IBM Research Laboratory in Yorktown Heights, New York, developed an analytical drift-diffusion model that contains all the real world losses (see "The Hovel and Woodall model" for details).

However, this approach is far from perfect, because it fails to account for the contribution to energy generation that occurs in cells employing a high reflectivity back mirror, which increases absorption within the cell and enhances photon recycling. A more complete model would include coherent and incoherent optical effects, such as contributions from back surface reflectors, which increase the probability of photon absorption; and it



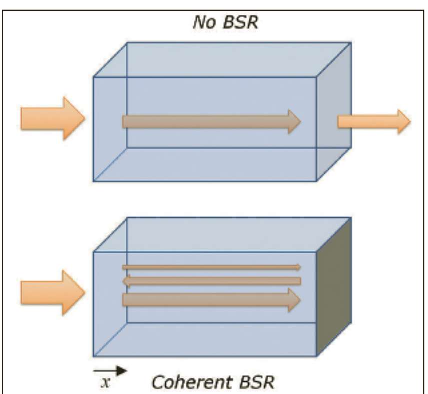


Figure 1. A generation function accounts for optical effects in a cell. A modified form of this function is used when a gold mirror is added to the cell's backside to create a coherent back-surface reflector (BSR).

would account for photon recycling, a process where photons spontaneously emitted by the material through radiative recombination are reabsorbed by it.

Previously, numerical methods have been employed to construct a fully numerical drift-diffusion model that accounts for all these effects. Including them all is essential for accurate modeling of today's best devices, which are coming very close to the fundamental efficiency limit.

Strengths of these numerical models include their flexibility and precision. But these merits have to be weighed against several downsides, which can be addressed by turning to an analytical model that includes the additional optical effects – which is an approach that has been pioneered by our team from the US Naval Research Laboratory, George Washington University and the National Renewable Energy Laboratory (NREL).

One of the virtues of our analytical model is that it avoids the need for advanced numerical techniques for solving boundary value problems on a mesh grid, resulting in a model that is easy to develop. What's more, the analytical model provides an excellent intuitive understanding of the inner workings of a solar cell, due to separate treatment of different regions within the device. All this is possible while delivering comparable accuracy to the numerical model, so long as we can meet the assumptions upon which the model is based.

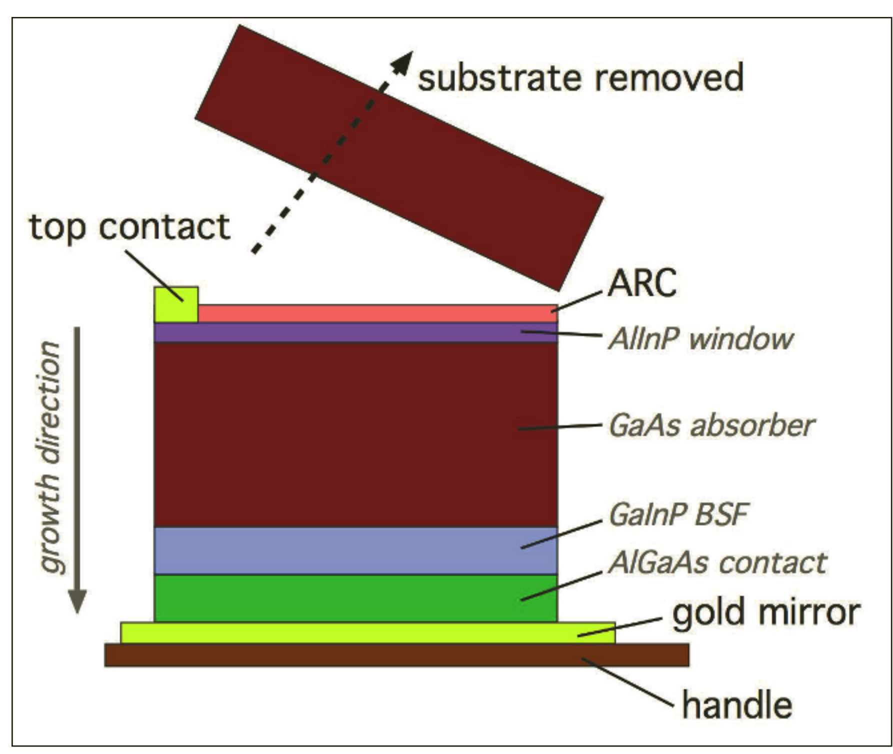


Figure 3. An inverted growth process enables a mirror to be positioned directly beneath the cell, enhancing light absorption. Another benefit of this approach is that it allows re-use of the substrate.

To date, our work has been restricted to the modeling of single-junction devices. However, it should be possible to extend this effort to multi-junction variants. This will require modification of the model to include luminescent coupling, which occurs when the emission from the top cell generates photons in the cell beneath.

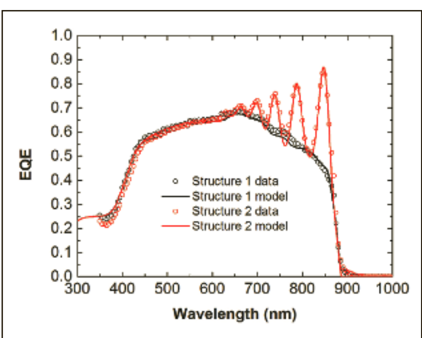


Figure 2: Modeled and experimental values of the external quantum efficiency of two GaAs solar cells of the same 1 μm thickness: structure 1 has no back reflector, whereas structure 2 has a high reflectivity gold back reflector. Note that the external quantum efficiency is a measure of the spectrally resolved probability of an incident photon being captured and converted into an electron in an external circuit.

Handling multiple reflections…

To account for the multiple reflections inside the cell when a back mirror is present, we have added a generation function to the drift-diffusion model. It is possible to determine a compact analytical expression for this function at every point in the solar cell by summing the fields of the multiple reflected beams in the absorbing region. This expression can then be incorporated into the drift-diffusion calculations, and solved in an analogous way to the original Hovel and Woodall model. Note that this approach can be applied to both coherent and incoherent reflections from the back surface reflector.

We can illustrate this approach by considering the simple case of a GaAs absorber with a coherent gold back reflector (see Figure 1). At short wavelengths GaAs is strongly absorbing, so the generation function resembles that of Beer's law – this states that as light passes through a substance, its intensity decreases exponentially. For wavelengths near the bandgap of GaAs, this law is not valid, and the generation function deviates significantly as GaAs becomes semi-transparent. In this wavelength region, the solar cell acts like a Fabry-Perot cavity, with the forward and reverse propagating fields interfering to produce an overall enhancement in the photon density absorbed by the GaAs. This leads to an increase in photocurrent.

Adding a gold mirror to the thin GaAs homojunction solar cell leads to a significant increase in its external quantum efficiency (see Figure 2, which shows that modeling can replicate experimental measurements by capturing coherent optical effects arising due to the back surface reflector). However, these demonstration devices were fabricated without a front side anti-reflection coating, leading to losses of

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approximately 30 percent at the front surface. Therefore, the mirrored cell in this example has not reached the realms of ultra-high efficiency.

Production of these cells begins with MOCVD growth of the epitaxial layers on a GaAs substrate. During post-growth processing, if an external back metal contact is deposited on the rear side of the substrate, the thick absorbing substrate will act as a photon sink to any internally emitted radiation (this is the case for structure 1 in Figure 2).

It is possible to insert a highly reflective back contact by removing the substrate and depositing the mirror directly on the rear side of the epitaxial layers. An innovative way to do this, pioneered at NREL in 2007, begins with the growth of the solar cell in an inverted configuration, with the front layers grown first and the back layers grown last. Layers are then re-orientated during post-growth processing to create a structure where the rear surface of the actual solar cell is immediately accessible. A highly reflective metal or dielectric-metal mirror can then be deposited on the growth surface (this is the case for structure 2 in Figure 2, and the device that results from this approach is shown in Figure 3).

Fabrication of this type of cell is completed by bonding the epistructure to a handle wafer, such as silicon or a flexible plastic, and then removing the native substrate – wet chemical etching is one way to do this, though other techniques have been developed that allow the substrate to be preserved and reused. Epilayers are then processed into individual solar cell devices with front contacts.

> “When a cell is generating power, there are actually a great number of recombination events happening simultaneously, with photons emitted in all directions inside the absorber. Ideally, most of those photons are recycled into new electron-hole pairs. Progress towards this goal is possible with a back surface reflector, which suppresses photon escape through the rear surface of the cell and thus improves the external radiative efficiency”

… and photon recyling

In addition to multiple reflections, the other significant improvement of our analytical model over that developed by Hovel and Woodall is the inclusion of photon recycling. In a perfect cell, all of the solar radiation that impinges on the front surface will be absorbed. Then, in order to generate power from the device, some radiative recombination must occur. This is an inescapable loss, but in an ideal cell all the non-radiative processes are negligible, and all of photons generated by radiative recombination can only escape the device through its front surface.

When a cell is generating power, there are actually a great number of recombination events happening simultaneously, with photons emitted in all directions inside the absorber. Ideally, most of those photons are recycled into new electron-hole pairs (see Figure 4).

Progress towards this goal is possible with a back surface reflector, which suppresses photon escape through the rear surface of the cell and thus improves the external radiative efficiency.
One of the consequences of photon

The Hovel and Woodall model

IN THE 1970s, Hovel and Woodall made an important scientific contribution to solar cell efficiency modeling with the introduction of an analytical drift-diffusion model for single-junction solar cells.

This model capitalizes on the fact that simple *p-n* homojunction solar cells typically operate in the low-injection regime and have carrier populations well-described by Boltzmann statistics. Under these approximations, the diffusion problem for minority carriers in the quasi-neutral absorber regions can be solved analytically. Optical generation in the cell is described by Beer’s law, which is a good approximation for an optically thick homojunction. By coupling this model with accurate values in the literature for optical constants, semiconductor band parameters, minority carrier transport properties, non-radiative lifetimes and interface recombination rates, it is possible to make remarkably accurate predictions of solar cell performance.

However, the model fails to capture two significant effects related to photon management, both of which are crucial in devices approaching the fundamental limit: coherent and incoherent optical effects, such as back surface reflectors to improve the probability of photon absorption; and photon recycling, where the photons spontaneously emitted by the material through radiative recombination are reabsorbed by the material.

recycling is a cut in the net rate of radiative recombination. This can also be stated in another way – as photon-recycling increases, the radiative lifetime of minority carriers increases until the external radiative efficiency limit is reached. However, if photon recycling is to deliver a performance improvement, it is paramount that the *internal radiative efficiency* of the material – that is, the fraction of recombination events that are radiative – approaches unity. When this happens, the net lifetime of minority carriers increases due to photon recycling, which leads to an increase in their diffusion length.

In III-Vs cell made today, material quality is exceptionally high, enabling cells to operate at very high internal efficiencies. In these devices, the voltage produced by a solar cell provides an excellent indicator of photon recycling, which impacts the recombination rate and therefore the dark current.

Our efforts at capturing photon recycling in our model (see "Including photon recycling in an analytical model") have helped us to appreciate the importance of maximizing the external radiative efficiency of solar cells. Motivated by this, members of our team at NREL have developed an important modification to conventional homojunction solar cells: the thick emitter concept.

The traditional architecture for a high efficiency III-V cell includes a thin, highly doped *n*-type (emitter) layer atop a thick, lower doped *p*-type (base) layer. Short wavelength light, with a short penetration depth, is predominantly absorbed in the emitter layer and longer wavelength light in the base layer. In contrast, our new design features a thick, moderately doped *n*-type emitter layer atop a thin *p*-type base layer, giving rise to a high external radiative efficiency.

There are several reasons why a thickening of the emitter boosts performance. First, so long as the diffusion length of minority carriers significantly exceeds the thickness of the quasi-neutral regions (which is required for efficient minority carrier extraction in solar cells), a structure with a thick, low doped *n*-type layer can achieve a lower diffusion current than an analogous structure containing a thick, low doped *p*-type layer due to the lower diffusivity of minority holes to minority electrons.

Another reason why our novel architecture increases efficiency is that almost all the photocurrent in the thick emitter structure is produced from the emitter, so device performance is very sensitive to the minority carrier lifetime in this layer. It is possible to optimize the emitter doping concentration to ensure high quality material with a close-to-unity internal efficiency, and a long enough diffusion length to provide efficient minority carrier collection.

When the thick emitter is included in a structure with efficient photon recycling – such as a device with very high internal efficiency and a high-reflectivity, back-surface reflector – this can lead to significant voltage enhancements. In contrast, in a conventional, thin-emitter structure, the dark current and photocurrent contributions of the solar cell are distributed more evenly among the emitter, depletion and base regions of the solar cell, making it more difficult to design a device with both high performance and high sensitivity to photon recycling effects.

Our modeling and experimental efforts have determined the significant increase in voltage output that results from the inclusion of a gold back mirror on our thick emitter GaAs cells (see Figure 5). This device delivers a conversion efficiency of 27.8 percent, within 3 percent (relative) of the current world record for a single-junction solar cell. The performance of this device approaches the fundamental, thermodynamic limit for an ideal GaAs cell.

We have used a variety of models to predict the performance of this thick-emitter, single-junction cell. Calculations based on the model by Hovel and Woodall underestimate performance, due to a failure to capture the optical enhancement that arises due to the multiple reflections from the back surface reflector, and the suppression of radiative recombination due to photon recycling. Slight improvement results from the inclusion of a more realistic generation function that incorporates multiple reflections from the back mirror and the concomitant increase in the short-circuit current density. However, this model still assumes bulk lifetime values with

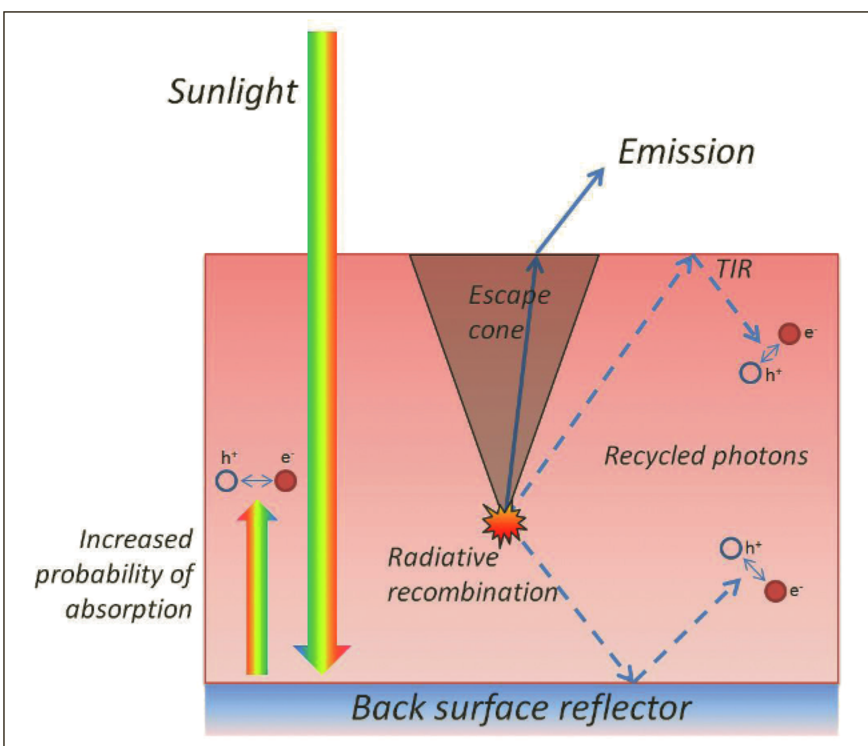
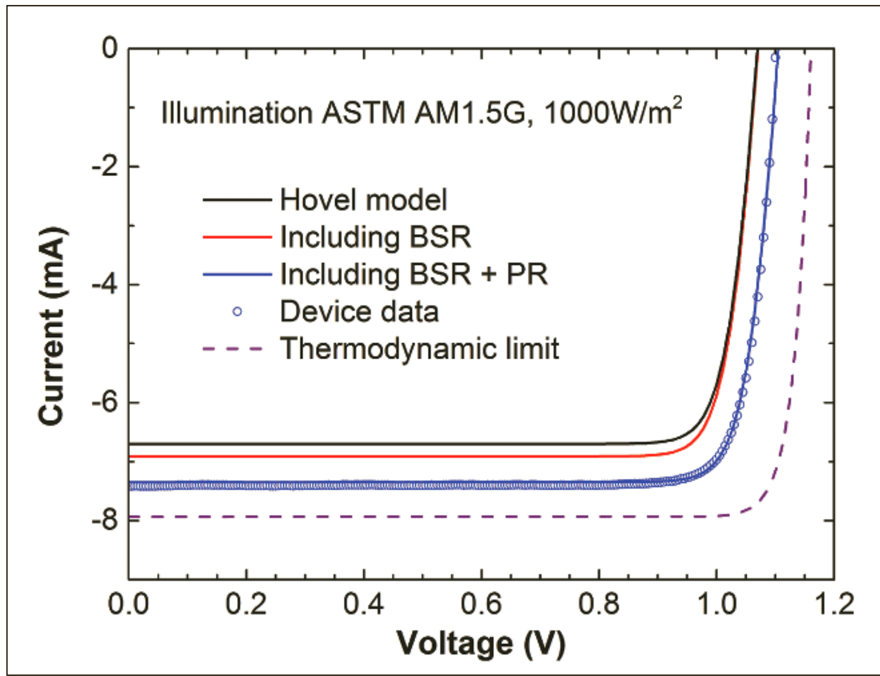


Figure 4. If photon recycling is ideal, the only photons that are able to escape the absorber pass through the front surface; all other photons are recycled to generate new electron-hole pairs. The inclusion of a back surface reflector improves the probability that incident sunlight is absorbed within the device.



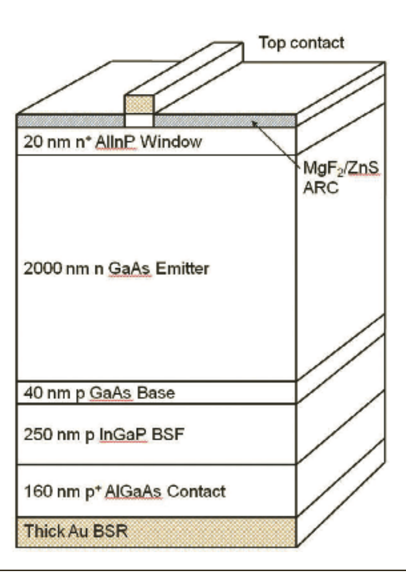


Figure 5. A variety of models have been used to try and capture the performance of the thick-emitter, single-junction cell that incorporates a reflecting gold mirror at the bottom of the device. The model by Hovel and Woodall fails to accurately reproduce the experimental data. Incorporating multiple reflections from the gold mirror, which is also known as a back surface reflector (BSR) improves the calculation, but both BSR and photon-recycling contributions are required to replicate the experimental results.

no photon recycling, giving a diffusion length of 4.3 µm for minority holes in the emitter.

When photon recycling it taken into account, the diffusion length increases to 17.1 µm and the minority carrier lifetime increases. Our model can then capture the increase in photocurrent extraction efficiency and reduction in dark current. Both these improvements impact the light-current-voltage curves, where it is possible to note increases in short-circuit current density and open-circuit voltage. This voltage exceeds that predicted by the Hovel and Woodall model and highlights the need for modeling that includes photon management strategies, which allow solar cells to get even closer to their fundamental performance limit.

The authors would like to thank Dr. I. Vurgaftman, Dr. A. Hanbicki of the Naval Research Laboratory, J. Adams, V. Elarde, G. Hillier and the R&D team of Microlink Devices Inc., and D. Friedman, I. García and S. Kurtz of NREL for helpful discussions relating to this work. Research at NREL was supported by the U.S. Department of Energy under Contract No. DE-AC36-08GO28308 and funded in part by the Foundational Program to Advance Cell Efficiency.

Accounting for photon recycling in an analytical model

BY MAKING A FEW simplifying assumptions it is possible to capture the physics of photon recycling with an analytical model. The key principle that we need to consider is the reciprocity relation linking the absorbed and emitted radiation.

Under voltage bias, we assume that the quasi-Fermi level separation in the device is equal to the applied bias at all points within it – this is a very good approximation for a typical homojunction solar cell under low-injection conditions. Under this assumption, the rate of radiative recombination is uniform throughout the cell; and the photon current escaping the solar cell, which is related to the internal photon current, is determined from the generalized Planck equation and the absorbance of the structure. The absorbance is the total probability of a photon incident on the cell from outside being absorbed, which is straightforward to compute for a multilayered medium.

The fraction of the total photon current in the absorber unable to escape the solar cell is known as the photon recycling factor [see, for example, Asbeck, J. Appl. Phys. **48** 820 (1977)], which determines the average reduction in the net radiative recombination rate for the electron-hole pairs in the cell. This number is a function of the particular geometry of the cell and, in conjunction with the lifetimes of competing non-radiative processes, enables calculation of the overall minority carrier lifetimes in the absorber layers of the cell.

The final simplifying assumption that we make is to assume that the net recombination rate at a given bias in the dark is equivalent to that in the light. This is the often used principle of superposition in solar cells.

Trimming grid losses with SiC

Equipping the grid with SiC-based solid-state transformers will lead to more efficient delivery of better-regulated power

BY DANIEL FERNÁNDEZ HEVIA FROM INAEL ELECTRICAL SYSTEMS AND JOSÉ MILLÁN FROM IMB- CNM-CSIC

WHEREVER YOU LIVE, you will tap into an electrical grid that is far from perfect. Its weaknesses– which have been known for a long time but are yet to be addressed – include differences between the energy that is available and that supplied; a voltage profile that is far from constant; and a substantial reliance on relatively dirty, low-efficiency power plants for satisfying energy demand at peak periods.

Governments around the globe are aware of these shortcomings. For example, to try and improve the electrical infrastructure within Europe, the European Commission has introduced a directive to substantially improve the efficiency of conventional transformers in all European countries.

Success is expected to result from the replacement of a passive element, the conventional transformer, with an active element that interacts with the grid. The active element will be based on power electronics, which can sit right at the heart of the electric energy cycle, transforming voltages from one form to another and addressing many of the weaknesses outlined above.

Conventional power electronics features circuits made with silicon components. However, that is not ideal, because diodes and transistors made from this material are limited in terms of blocking capability, operating temperature and switching frequency.

A better material in all these regards is SiC – and that's why our multi-disciplinary team has adopted it to develop a whole new generation of cost-efficient, commercially viable high-voltage devices that are specifically intended for deployment in power generation, transmission and distribution. Working together in a project entitled SPEED - Silicon Carbide Power Electronics technology for Energy-efficient Devices – our 17 partners from nine countries are backed by 20 million of funding from the European Union, and are aiming to construct an efficient converter for wind turbines and a new SiC-based solid state transformer for the distribution grid (typically a 24 kV/400 V, 400 kW unit). As a collateral benefit, there are a large number of other fields that will benefit from the technologies to be developed: defense, aerospace, and transportation are the most obvious candidates.

SiC components and monolithically integrated circuits would offer a whole new range of possibilities in many applications. From a cost perspective, reductions would mainly arise from a substantial trimming of the size and weight of ancillary components, such as coils and cooling systems. Deployed in aircraft, SiC power electronics would minimise active column, double power densities and increase system stability. On military vessels, the introduction of this wide bandgap semiconductor could slash the weight of the radar power system by 75 percent, equating to trimming 80 tonnes, thanks to the use of high frequency utility transformers. For wind generation, SiC promises $18 billion per year of fuel cost saving, and this class of device could also improve the efficiency that energy from solar panels is converted into that suitable for the grid. In jeeps, turning to SiC can minimise active cooling, and in electric and hybrid electric vehicles, it can double the inverter power density.

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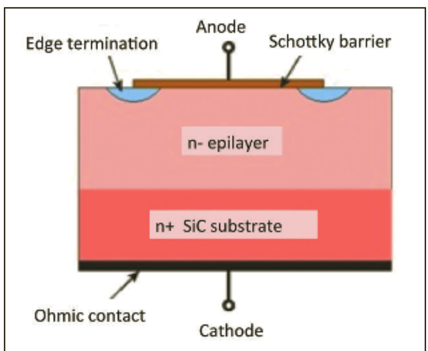
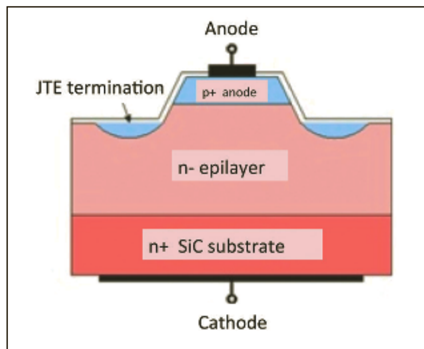




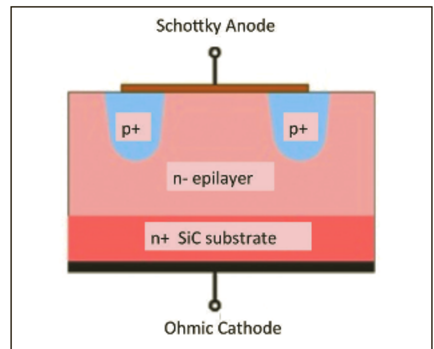


Figure 1. Cross-section of 4H-SiC 3.3 kV Schottky, JBS and PiN diodes

Why not GaN?

Another recent candidate for this new generation of semiconductors is GaN. Many of the strengths of SiC, such as its high-voltage blocking capability, high-temperature operation and high switching frequencies, are also found in this other wide bandgap material. But thick epilayers, such as those greater than 10 μm, are currently very difficult to produce, limiting the voltage withstand capability of the device; note, for example, that a 10 kV SiC MOSFET has an epilayer of 100 μm or even more. To scale this device voltage, it is critical to be able to grow thick, high-quality SiC that is free from imperfections such also micropipes or basal plane defects.

High-quality epilayers are possible in SiC, but not so easy in GaN, a material with a bright future in 600 V devices to be used in electric vehicles and hybrid electric vehicles, both in the inverters and chargers. Meanwhile, SiC seems to be far better positioned to win the battle of the higher voltages, starting in the range 1700-3300 V for inverters in wind turbines or solar panel, and going all the way up to 10 kV+ devices to be deployed in the smart electricity transmission and distribution grid.

Besides the high-voltage withstand properties, we have selected SiC for our efforts due to the far greater commercial availability of native substrates and the maturity of the technological processes associated with this material. SiC diodes have now been on the market for more than a decade, being joined more recently with a variety of transistors, such as JFETs and MOSFETs. Advances in device yield and the performance of SiC devices have been underpinned by improvements to the substrate. Now on the market are SiC substrates with a diameter of 100 mm, and 150 mm equivalents will soon follow. The quality of these foundations for SiC growth are getting better and better, with the density of micro pipes – a type of defect that can kill devices – plummeting to just 0.75 cm^{-2} for a 75 mm wafer. However, that's not to say that more cannot be done: Basal plane dislocations are still under investigation for causing poor reliability in bipolar devices.

It is worth noting, however, that even when SiC substrates have imperfections, it is still possible to produce some very impressive devices. Several research teams from around the world have demonstrated diodes with very high blocking voltages, such as 19 kV, due to a sufficiently long minority carrier lifetime in thick epilayers that allow conductivity modulation. Several members of our team are active in this area and will try to develop cost-efficient, highly reliable processes for producing high-quality, thick epilayers that are suitable for high-voltage devices.

Building better diodes…

The building blocks for power electronics are diodes, which control the flow of current, and transistors, which can turn it on and off. Since both devices are being manufactured today, it would be foolish of us not to evaluate what is already commercially available before building own devices.

For diodes, sales are tipped to rise, as they first replace silicon bipolar rectifiers covering the 600-6500 V range, and then power switches operating above 1.2 kV.

The most established form of this diode is the Schottky barrier diode, which has been commercially available since 2001 and is renowned for its extremely high switching speed and low on-state losses. Since it launch, the range of current ratings and blocking voltages has increased, and it is now possible to purchase SiC devices that operate up to 1.7 kV, or are capable of handling 20 A and blocking 600 V. This expanded portfolio of devices will allow their deployment to diversify from the likes of power factor correction and high-voltage secondary side rectification to incorporation in medium power motor drive modules.

Even higher voltages are expected for the SiC Schottky barrier diode, which should be capable of blocking voltages up to 3.5 kV. In fact, there are already reports of large-area 3.3 kV Schottky barrier diodes capable of operating at high temperatures and delivering forward currents of 10-20 A.

Although it is possible to produce a similar blocking voltage with silicon, the drift layer thickness must be ten times higher, and device performance is impaired by a reverse recovery charge that is not present in the SiC diode. These attributes of the SiC Schottky barrier diode ensure that it is a great choice for a freewheeling diode that is partnered with a silicon IGBT.

If higher blocking voltages and lower leakage currents are needed, the SiC *p-i-n* diode should be chosen in preference to the Schottky barrier diode. Development of this class of device has led to reports of SiC *p-i-n* diodes that combine a forward voltage of 3.2 V at 180 A (100 A/cm^2) with a blocking voltage of 4.5 kV and a reverse leakage current of 1 μA.

The weakness of the SiC PiN diode is its reverse recovery charging during switching. To address this, some researchers are developing junction barrier Schottky diodes, which combines Schottky-like on-state and switching characteristics and *p-i-n*-like off-state characteristics. However, these devices are not commercially available, due to reliability problems associated with charge recombination at planar defects.

All three types of device have a far higher thermal conductivity than those made from silicon and GaAs, and this allows them to operate at higher current density ratings and to slash the size of the cooling systems. One of the primary goals of our project is to quantify in detail the system-wide economic advantages of using SiC components. Preliminary calculations show that even when the components are substantially more expensive than silicon equivalents, the overall cost-reduction in a system can exceed 50 percent, thanks to reductions in the bills for the cooling systems and the passive components, such as coils and capacitors. All three types of diodes are shown in Figure 1.

… and switches

For switching at voltages exceeding 600 V, SiC transistors have two strong silicon competitors: the IGBT; and the power MOSFET, which includes the CoolMOS family and other advanced trench devices. However, when blocking voltages reach the range of 1.2 kV to 1.8 kV, the silicon MOSFET is not a realistic option, while the silicon IGBT suffers from high dynamic losses at fast switching speeds. In comparison, SiC switches produce great performance at high voltages and high temperatures, while handling very fast switching speeds. In addition, there is increasing demand for SiC high-voltage controlled switches, opening up new opportunities to increase the sales of these transistors.

One promising class of SiC transistor is the JFET, which combines an ultra-low specific on-resistance with a capability to operate at high temperatures and high frequencies (see Figure 2). One of the partners in our project, Infineon, has developed a 1.5 kV, 0.5 W on-resistance hybrid switch by pairing, in a cascode configuration, a 1.5 kV vertical SiC normally-on JFET and a 60 V silicon MOSFET. One downside of incorporating silicon is that it prevents high-temperature operation, so new SiC JFETs were developed by the now defunct SemiSouth. These are normally-off, due to the high built-in voltage of SiC *p-n* junctions, but they are compromised by high resistive channels and low threshold voltages.

An alternative to the JFET is the MOSFET. For many years this was held back by a very low inversion channel mobility, which prevented production of low-resistance MOSFETs that could prove the capability of SiC transistors in power electronics. Recently, however, two techniques have emerged that can increase the quality of the MOS interface: post-oxidation annealing in a nitrogen environment and formation of the MOS channel on alternative crystal faces. These approaches have trimmed interface trap density in the MOS channel and improved surface morphology, leading to carrier mobilities on fabricated lateral MOSFETs of 50 cm^2/Vs and 73 cm^2/Vs for thermally grown and low-pressure CVD gate oxides, respectively.

One of the goals of our project is to push this transistor technology to its limit, with effort directed in particular at improving wafer quality. We aim to pave the way for cost-efficient SiC MOSFETs to be used in prototype solid-state transformers.

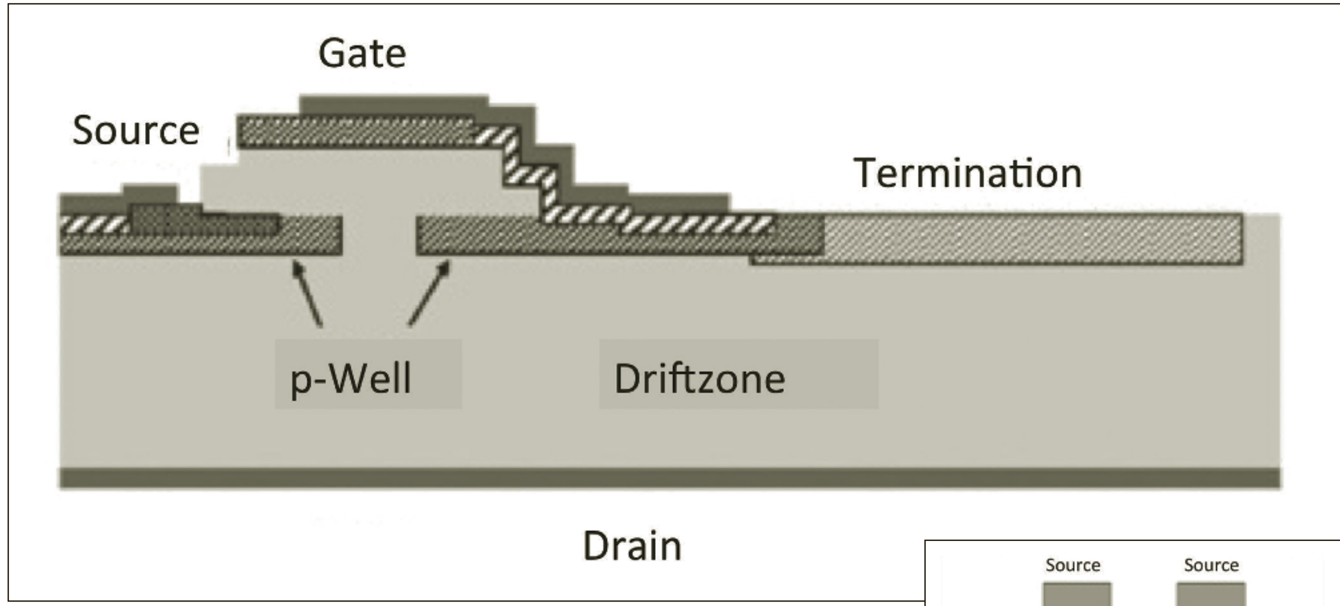
We are also aware that back-end processes, such as passivation schemes, are of crucial importance, because they can affect the efficiency of the edge termination. Developing packages capable of withstanding high temperatures is also very important, because this will allow SiC devices to fulfil their potential for high-temperature operation. All of these goals are being pursued, and results will be reported as the project progresses.

Deployment in the grid

After we have developed a range of devices operating at voltages both above and below 3.3 kV, we will use them to construct power conversion cells – these will make up the basic building blocks of a solid-state transformer for power transmission. Input and output ports of these conversion cells, which have a target power of 10 kW, will be connected in series and/or parallel in order to accomplish the solid-state transformer voltage requirements. The final arrangement will be governed by the availability of the devices that we make.

These cells will be used to perform AC-DC, DC-DC (with galvanic isolation) and DC-AC conversion. This means that our SiC devices will be used to construct two different types of bidirectional cell, which either provide AC-DC or DC-DC conversion. By building a variety of these

Infineon has been a pioneer of the SiC Schottky barrier diode. In June 2014 it launched its fifth generation of thinQ! SiC Schottky diodes. They are claimed to feature ultra-low forward voltage even at operating temperatures, more than 100 percent improved surge current capability and excellent thermal behaviour.



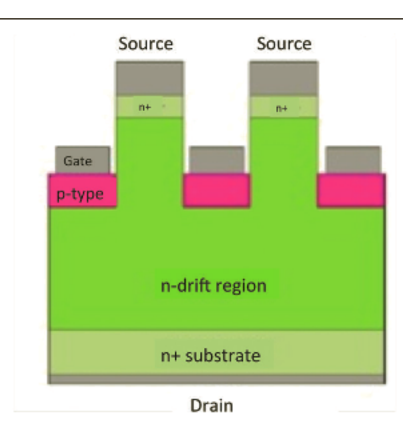


Figure 2. Cross-sections of normally-on (a) and normally-off (b) JFETs from Infineon and SemiSouth, respectively

cells with different SiC devices, we will be able to the select optimal bidirectional AC-DC and DC-DC power cells for the final solid-state transformer demonstrator.

Our prototype transformer will outperform the incumbent, which is a relatively cheap and reliable device that suffers several weaknesses, including: low power density (for the power delivered, the transformer is bulky and heavy), large losses at light load, sensitivity to harmonics, offset and imbalances, and no effective overload protection. Turning to a solid-state transformer will slash the size and weight of the transformer core, increase control over the transformation process and provide some energy storage. Thanks to capabilities like this, the transformer can incorporate additional functionality, such as harmonics, reactive power and imbalances compensation. With a conventional transformer, this would only be possible with a separate power converter.

One of the most important features of the solid-state transformer is that it can provide automatic, continuous on-load voltage regulation, contributing to a smoothing effect for the voltage profile through the grid. This form of on-load voltage regulation will help the power grid to be more flexible, due to distributed generation.When distribution networks are added, energy flow is no longer one-directional, because the distributed pieces of generation impose bi-directional energy flow.

Additional benefits associated with the introduction of solid-state transformers include a provision for reactive power compensation; on-demand definition of the wave shape, including harmonic compensation; and environmental benefits. Conventional transformers may be immersed in oil, or they can suffer the penalty of inferior efficiency conversion when they are dry, while solid-state transformers can combine high levels of efficiency with an absence of oil.

Construction of oil-free, high-efficiency, solid-state transformers could play a key role in fulfilling the European ECODESIGN Regulation, which calls for substantial cuts in grid losses. This mandate will require a substantial hike in the efficiency of conventional transformers in all European countries. Armed with the solid-state technology developed in our project, it should be possible to cut grid-level losses far beyond the expectations outlined in the in the ECODESIGN regulations. Our view is that grid-level losses can be minimised in a network equipped with solid-state transformers, due to an optimized voltage profile, instantaneous matching of offer and demand, and optimized energy management.This approach will pay greater dividends than that stemming from the sole reduction of individual losses in an individual piece of equipment.

Note that when judgements are made on the merits of classical and solid-state transformers, they should not be performed on the basis of cost and robustness of standalone pieces of equipment. Instead, evaluations must consider the overall performance that is provided – that is, they must take into account the additional power converters and storage elements that should be added to the classical power transformer to achieve equivalent solid-state technology performances. If these calculations are undertaken, deployment of solid-state transformers will increase in power transmission systems.

Our project will investigate a variety of options for how solid-state technology could impact the grid, and consider the impact of replacing silicon devices with those made from SiC, and inserting SiC devices in existing silicon-based circuits (see box “Goals of SPEED”).

When our transformers set a new benchmark for performance, it may trigger a need for a new approach to standardization. It is possible that the tests and performance indicators

The goals of SPEED

The EU-funded project SPEED aims to improve the performance of solid-state transformers (SST). Efforts will be directed at both existing topologies involving replacing silicon by SiC power devices and new topologies. There will be a special focus on three areas:

1. The study of new SST topologies, including those derived from the modular multilevel converter (MMC). Modifying a classical MMC to include a medium frequency transformer at the cell level is expected to provide benefits in terms of modularity, controllability and reliability. Moreover, a MMC provides a power transmission port, opening the possibility to implement a multiport converter. Due to the modular nature of a MMC, high voltage is not a major requirement, so 1.7 kV SiC power devices are adequate in principle. The main advantages of SiC devices are their switching and thermal properties. Added functionalities are under study for the topologies being developed. These include:

- Fault tolerance: self-healing, redundancy.
- Safety and overvoltage/overcurrent protection
- Statcom like functionalities: Harmonics, unbalance and reactive power compensation

2. Use of SiC devices in existing silicon-based SST topologies:

- Impact of new SiC power devices on the SST efficiency. Due to its superior switching characteristics, a considerable reduction of switching losses is expected with SiC devices in comparison with those in SST based on conventional silicon devices.
- Design of the drivers. Many of the new SiC devices recently developed cannot be considered as a direct drop-in replacement of current silicon devices in existing applications due to the different levels of voltage and current to switch-on and off. Therefore, specific drivers and controllers must be designed for these new devices.
- Switching frequency and dynamic response: increases in switching frequency to enable a reduction of the passive elements needed, as well as an improvement of the dynamic controls response (higher bandwidth). This can be of great importance; for example, it can enhance the SST capability to provide harmonic compensation.
- Impact of new SiC power devices on the SST voltage and current ratings. SiC might be of special interest to reduce the number of levels in diode-clamped multi-level topologies, due to their higher breakdown voltage. It is important to note that reducing the number of levels eases the construction and control of the power converter, but it may have a negative impact on the wave shapes and the passives required for filtering.

3. Optimisation of the medium frequency electromagnetic transformer (materials and design) used in the SST. The frequency operation range of the electromagnetic transformers needed for providing galvanic isolation to the overall converter will be higher than in the case of a conventional SST based on silicon devices. Therefore, materials such as ferrites and amorphous alloy core transformers should be considered for this application.

normally used for the three-phase power converters already present in the grid, such as inverters in solar farms and wind turbines, might be inadequate for the solid-state transformers. A similar situation may arise for power converters, and in both cases if new standards are introduced, they must reflect that transformers are ubiquitous elements, with a huge impact on overall grid reliability, so high levels of reliability are paramount. We hope to develop these new standards for solid-state transformers within our project, which promises to lay the foundations for an era of far more efficient electrical grids.

Project SPEED is funded by the European Commission through Grant Agreement number 604057. Partners in the project are INAEL Electrical Systems, ABB Schweiz AG, CSIC – CNM, ENEL Distribuzione S.P.A., University of Bremen, University of Ovideo, Norstel AB, Ascatron AB, The University of Nottingham, Infineon Technologies (Germany, Austria), Technical University of München, Fraunhofer, Czech Technical University in Prague, University of Hanover, Annealsys SAS, Ingeteam Power Technology SA.

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GaN: Building better transistors

Low-temperature interlayers and double heterostructures lead to the formation of transistors with low defect densities and high breakdown voltages

TWO TOP TRICKS for building a better GaN transistor on a silicon substrate are to trim strain via the insertion an AlGaN interlayer into the buffer, and to increase electron confinement by introducing a double heterostructure.

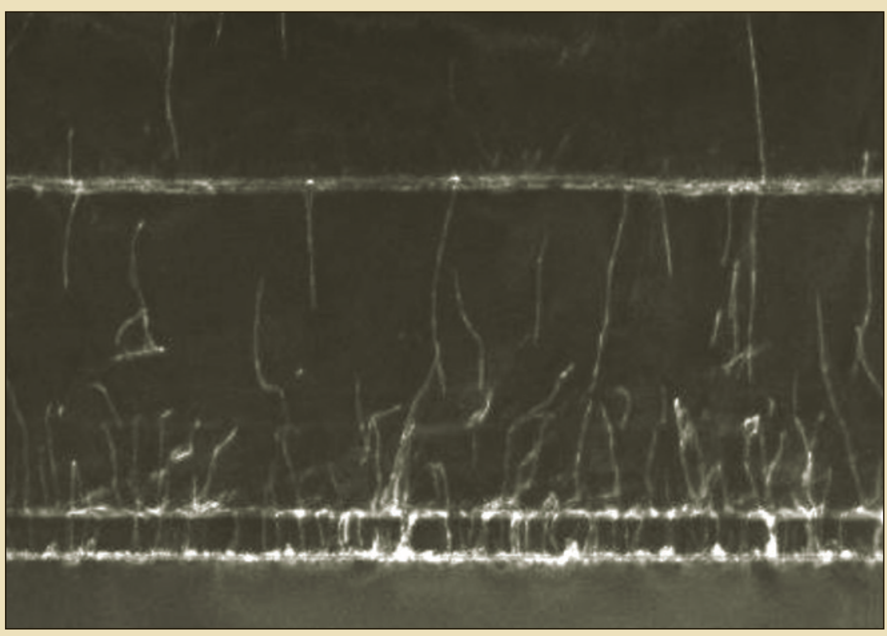
While many research groups turn to one of these two, a team from National Chiao Tung University in Taiwan is claiming to have gone one better by combining them.

"To the best of our knowledge, this is the first study demonstrating the low-temperature AlGaN interlayer in an AlGaN/GaN/AlGaN double heterostructure on a silicon substrate," says Yu-Lin Hsiao, lead-author of the paper detailing this work.

Thanks to insertion of a low-temperature interlayer, the device suffers from less stress, has fewer dislocations and a higher breakdown voltage. Performance is also enhanced by the introduction of the double heterostructure: This increases electron confinement in the GaN channel, which helps to cut the leakage current in the back barrier.

To demonstrate the superiority of their two-pronged approach, the researchers evaluated the performance of devices based on three different structures: one contained a double heterostructure and a low-temperature interlayer, while the two controls featured either a low-temperature interlayer and a single heterostructure, or a double heterostructure without the low temperature interlayer.

All three structures were deposited on 150 mm silicon substrates featuring an 800 nm-thick transition layer – it consisted of one AlN layer and three AlGaN layers. "We think that it is a common transition layer structure, but different groups may have different transition layer thickness," explains Hsiao. The interlayer inserted by the Taiwanese team was a 21 nm-thick film of $Al_{0.5}Ga_{0.5}N$, sandwiched between two 1 µm-thick layers of $Al_{0.1}Ga_{0.9}N$.



Cross-sectional transmission electron microscopy images reveal that the density of screw dislocations is significantly reduced after the insertion of a low-temperature AlGaN interlayer. Slashing the density of these screw dislocations is highly beneficial, because this class of defect is believed to be the primary cause of the decrease in breakdown voltage in GaN-on-silicon transistors.

"For this kind of structure, it is important to optimize the low-temperature-AlGaN interlayer under different growth temperatures and different growth duration," says Hsiao. Optimising the interlayer leads to a cut in dislocation density in the $Al_{0.1}Ga_{0.9}N$ back barrier.

"Another important thing [to determine] is when is the best time to insert the low-temperature AlGaN. We have to find out the critical thickness during the first $Al_{0.1}Ga_{0.9}N$ back-barrier layer growth," explains Hsiao. Efforts at determining this are aided by *in-situ* curvature measurements, which are provided by a Laytec EpiCurve TT system installed in the team's Thomas Swan MOCVD system.

Completion of the growth of the double heterostructure transistor involved deposition of a 90 nm-thick channel and a 30 nm-thick $Al_{0.2}Ga_{0.8}N$ top barrier. For the single heterostructure control, devices were formed from the pairing of GaN and $Al_{0.2}Ga_{0.8}N$.

To compare the breakdown voltage of all three structures, isolated regions were defined by dry etching, before multilayer metals were deposited with an electron-beam evaporator, and structures were then subjected to rapid thermal annealing under nitrogen gas for 60 seconds at 800 °C. Devices that resulted had a 100 µm gate width, a 1 µm gate length, a gate-to-drain spacing of 4.5 µm and a gate-to-source spacing of 1.5 µm.

Breakdown voltages for both conventional structures were below 400 V, compared to more than 600 V for the device that combined a double heterostructure with a low-temperature interlayer.

The team now plans to insert two or more low-temperature interlayers in the thick $Al_{0.1}Ga_{0.9}N$ back barrier to further increase breakdown voltage.

Y. -L. Hsiao *et. al.*
Appl. Phys. Express **7** 115501 (2014)

Wafer bonding offers a route to higher efficiency solar cells

Cells with many junctions can be formed via room-temperature wafer bonding

A PARTNERSHIP between researchers from Sony Corporation and the Chinese Academy of Sciences has developed a process for bonding together InP and GaAs solar cell wafers.

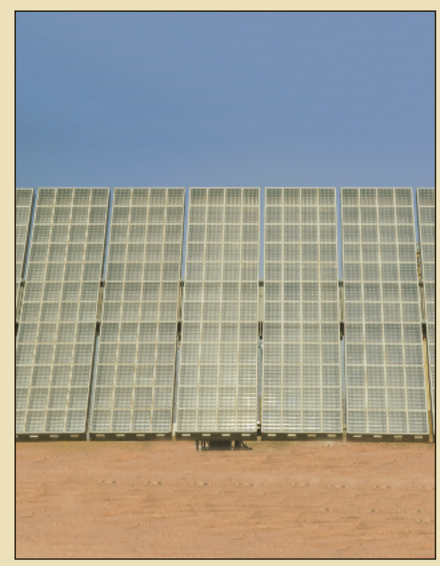
This approach could drive up solar cell conversion efficiency, enabling a trimming of the generation costs for concentrating photovoltaic systems and making this technology a more competitive form of renewable energy.

The wafer-bonding approach developed by the team will unlock the door to an increase in the number of junctions – the key to boosting solar cell efficiency. Today's highly efficient cells often use three junctions to absorb the sun's radiation that stretches from 390 nm to 1700 nm, but, according to the researchers, to progress to more than four junctions requires high-quality wafer bonding of InP and GaAs wafers.

"The accomplishment of our work is to attain the lowest bond resistance between different compounds wafers," says Sony's Shiro Uchida, who is the corresponding author of the paper detailing this work.

Extremely low bond resistances are essential, because cells installed in concentrating photovoltaic systems are bombarded by the sun's radiation that has been focused by a factor of several hundred or more, causing current densities within the device to hit values of up to 10 A cm^{-2}.

Uchida and his co-workers unite wafers with a room-temperature, argon-ion based approach that is superior to both fast-atom-beam-activated wafer bonding and fusion bonding. This pair of more common approaches are capable of realising strong bonds, but the bond interface resistance is too high, even after is has been quashed through either long annealing times, which can be between 30 minutes and three hours, or elevated temperatures of up to 700 °C. With a bond interface resistance of typically 0.01 Ω cm^{-2} or more, peak current in the cell is limited – and if high temperatures are involved, the hybrid cell can be plagued with defects, cracks and voids.



Increasing the number of junctions via a wafer-binding step promises to increase the competitiveness of concentrating photovoltaic systems.

A far lower interface resistance of just 2.5×10^{-5} Ω cm^{-2} is possible with the team's room-temperature bonding technique. Tadatomo Suga's group from Tokyo University invented this approach, which involves argon ions.

Uchida and his co-workers discovered how to realise such a low interface resistance after bonding a variety of commercial substrates together. A series of experiments were conducted using a Mitsubishi Heavy Industries room-temperature wafer-bonding tool, which incorporates an argon-ion gun in a vacuum chamber that can reach a pressure of less than 10^{-5} Pa.

After wafers were exposed to low-energy argon ions to activate their surfaces and create dangling bonds, they were pressed together in this chamber with a force of 5000 N. Adding a stack of metals formed ohmic contacts, before the wafers were diced into 3 mm x 3 mm chips and subjected to current-voltage measurements. Bonding a 450 μm-thick, GaAs substrate, which was silicon-doped to 3×10^{18} cm^{-3}, to a 600 μm-thick, GaAs substrate doped with sulphur to a concentration of 3×10^{18} cm^{-3}, created a structure with a high interface resistance. It exhibited diode-like characteristics, which might stem from a bonded interface with a high potential barrier for electron transport.

Following this result, the team tried to drive down the interface resistance by coating the wafers with a very thin layer of titanium, which is effective in reducing the Schottky barrier. The researchers deposited either a 2 nm-thick or a 2.8 nm-thick film of titanium on a 450 μm-thick, GaAs substrate that was zinc-doped to 1×10^{19} cm^{-3}; and they deposited a titanium layer of identical thickness on *n*-type InP.

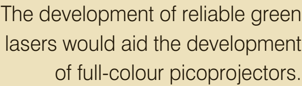
Electrical measurements revealed that when the wafers with a 2 nm-thick layer of titanium were bonded together, the bond interface resistance was 1.4×10^{-4} Ω cm^{-2}, rising to 2.1×10^{-4} Ω cm^{-2} when the thickness of the titanium layer on each wafer was 2.8 nm.

Even lower bond-interface-resistances were possible by attaching the heavily *p*-doped GaAs substrates directly to *n*-type InP. Following optimisation of the bonding conditions, the researchers recorded a value of just 2.5×10^{-5} Ω cm^{-2}. This low resistance is thought to result from a band structure that allows for the presence of both a tunnel current and a trap-assisted current.

S. Uchida *et. al*.
Appl. Phys. Express **7** 112301 (2014)

Green lasers may thrive with interfacial misfit dislocations

Anchoring misfit dislocations at interfaces allows green laser designers to turn to relaxed InGaN waveguides



The development of reliable green lasers would aid the development of full-colour picoprojectors.

RESEARCHERS from Corning have raised a few eyebrows within the nitride community by revealing that it is possible to drive laser diodes in continuous-wave operation for hundreds of hours even when they contain interfacial misfit dislocations.

Team member Dmitry Sizov says that they have prevented this imperfection from severely hampering laser performance by turning to a semi-polar III-N materials system and employing a design that maintains misfit dislocations at a sufficient distance from the active region.

"In the past there was no evidence that a semiconductor laser can reliably operate with a high density of misfit dislocations just 100 nanometres away from the quantum wells," says Sivoz.

Removing the need to banish misfit dislocations from the laser structure opens the door to the introduction of new designs, such as those with a higher indium concentration in the waveguide core and more aluminium in the AlInGaN cladding. "Both would be helpful to strengthen optical confinement in the waveguide, leading to an increase of modal optical gain and a reduction of optical loss in the claddings," explains Sizov, who points out that these refinements should lead to an increase in laser efficiency.

According to him, a further benefit of allowing misfit dislocations into the structure is the reduction of compressive strain in the quantum wells via the growth of the active region on a relaxed InGaN waveguide. "Therefore, higher indium incorporation should be possible, to further increase lasing wavelength." It is hoped that the introduction of a relaxed InGaN waveguide will lead to new records for green laser performance.

However, to see if this is possible, there must first be optimisation of the fabrication processes, crystal growth and some other design features. This is on-going, but not easy, according to Sizov. The efforts of the team from Corning have built on the successes of scientists at the University of California, Santa Barbara. That team formed LEDs on relaxed InGaN templates and fabricated lasers with an active region sandwiched between relaxed InGaN waveguide layers.

Sizov and his co-workers have gone one step further, constructing continuous-wave lasers with this type of design. These emitters have been formed via MOCVD growth of a laser structure on a free-standing $(20\bar{2}1)$ substrate.

After deposition of a GaN buffer layer, the researchers added an *n*-type AlInGaN cladding layer that was lattice-matched in the *c*-direction, but slightly lattice mismatched in the *a*-direction. An *n*-type $In_{0.05}Ga_{0.95}N$ layer was grown on top, with a thickness exceeding the value for relaxation along the *c*-direction. This led to the formation of a misfit dislocation array at the interface between the cladding and bottom waveguide.

Addition of a hole-blocking layer prevented hole overflow into the cladding-bottom waveguide interface, before an active region with two quantum wells was deposited, followed by a *p*-type $In_{0.05}Ga_{0.95}N$ waveguide. The latter had the same lattice constant as the bottom waveguide, preventing relaxation in this layer. Finally, a *p*-type AlInGaN cladding layer with the same composition as its *n*-type cousin was deposited onto the epitaxial stack. With a thickness exceeding 600 nm, it relaxed via the formation of another misfit dislocation array between the top waveguide and the top cladding. The epiwafers formed from this growth were used to fabricate lasers with a standard ridge waveguide geometry. Optical loss measurements on these devices revealed that *p*-type activation increased the internal waveguide loss from close to zero to 10 cm^{-1}. The conclusion: Misfit dislocations did not contribute to internal loss, which was dominated by acceptor-bound hole absorption that occurs after *p*-type activation.

The team studied the reliability of its 503 nm lasers, driving them at 150 mA, a current that produced an output of 3-4 mW. They were found to have a lifetime of 400 hours, which is well short of the 10,000 hours to 30,000 hours required for commercial deployment. "But we see no evidence that the degradation is due to misfit dislocations, and we hope that improvement of fabrication would greatly increase device lifetime," says Sivoz.

He and his co-workers have scrutinising degraded and non-degraded structures by photoluminescence and transmission electron microscopy, finding that reliability is compromised by point defects that might be due to nitrogen vacancies.

The next steps for the team are not clear, because the group has been recently acquired by ThorLabs.

D. Sizov et. al.
Appl. Phys. Express **7** 112710 (2014)

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