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Volume 21 Issue 1 2015

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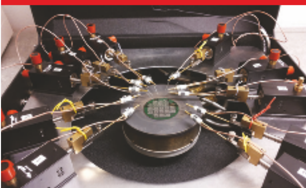
Routes to slashing the cost of CPV

Etching sapphire enhances LEDs

3C SiC promises cheaper MOSFETs

Handling heat with SiC circuits



IEDM: what future for the III-V FET?

EV Group

Heterogeneous integration

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editorialview

by Dr Richard Stevenson, Editor

Silicon CMOS: Will III-Vs have a role to play?

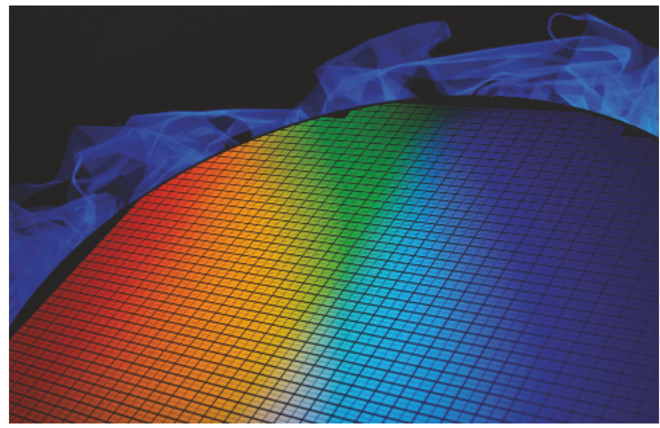
WHEN AN ESTABLISHED, important technology runs out of steam, a quest begins for a modification that will inject a new lease of life. Potential refinements can initially generate a great deal of excitement, before greater scrutiny follows that exposes weaknesses associated with the successor.

This scenario is playing out today in the world of silicon CMOS. Mobility in the silicon channel could hold back the performance of next-generation ICs, with the combination of InGaAs nFETs and germanium pFETs touted as a promising way forward.

Within this magazine, we have highlighted many successes that will help to unlock the door to the production of nanoscale InGaAs FETs on silicon substrates. These triumphs include the realisation of high-quality III-V material on a silicon substrate, through approaches such as that pioneered by imec: Researchers at this insititute have learnt how to grow compound semiconductors in tiny V-shaped silicon trenches.

What has been lacking so far from the experimentalist camp is the fabrication of transistors that are small enough to make an impact at around the 10 nm node. Gate lengths of existing InGaAs FETs tend to be 20 nm or more, and it is not clear whether the performance advantages over silicon will be maintained with scaling.

Theorists have looked into this, with a team from Samsung Semiconductor suggesting that for a fine width of 6 nm, a switch to an InGaAs *n*-type finFET will fail to produce a hike in performance. These calculations, which were presented at the International Electron Devices Meeting (see page 66 for a report



of III-V MOSFET developments presented there), indicate that strained germanium offers a better way forward, so long as devices can be formed with a low contact resistance.

Meanwhile, calculations from a team from the University of Udine present a different picture, suggesting that for a device with a 11.7 nm gate – transistors with that dimension are expected to make their foundry debut in 2020 – a switch from silicon to InGaAs delivers a 30 percent gain in on-current.

Based on these papers, there is clearly some uncertainty over the role that InGaAs FETs could play in the future of CMOS. What is clear is that introducing these devices into foundries will not be easy, so unless the increase in performance is substantial, it is possible that a switch to III-V transistors will never happen.

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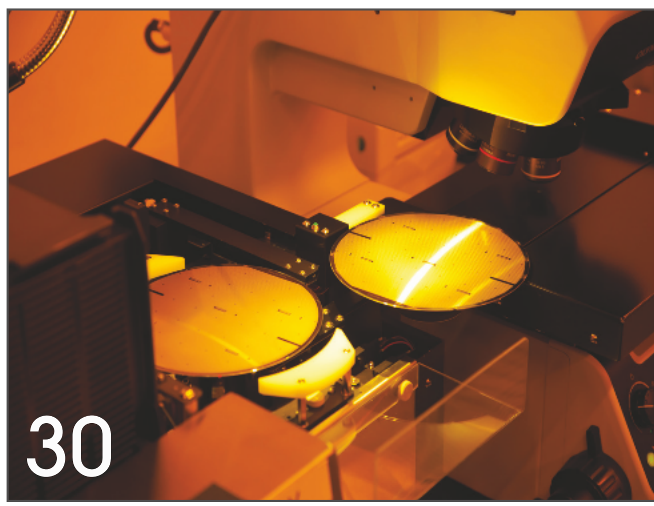
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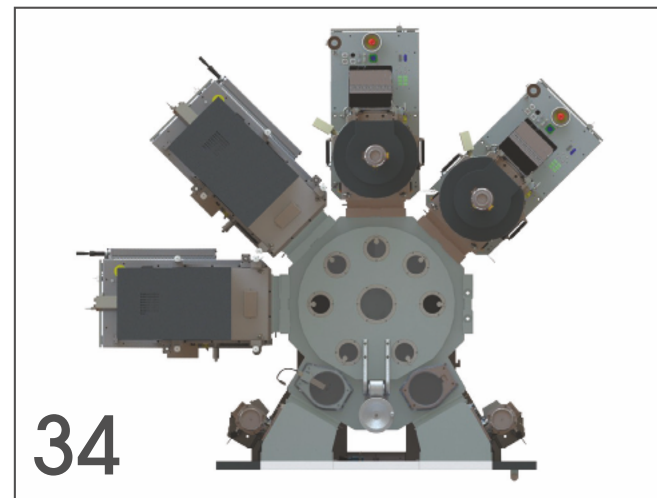
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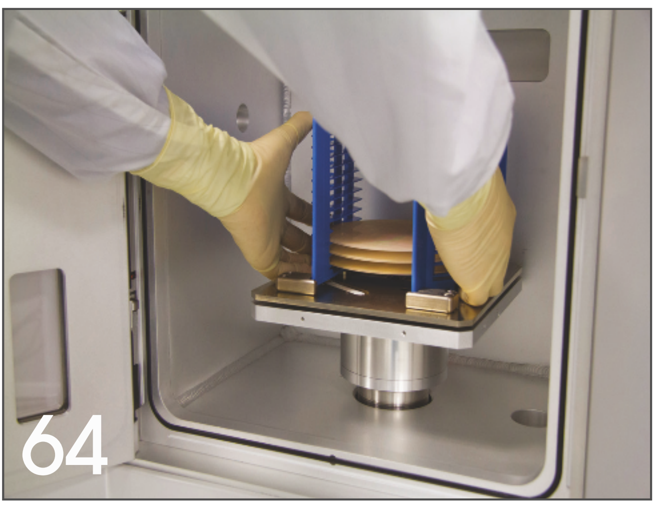
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International team constructs first group IV semiconductor laser

SCIENTISTS from Forschungszentrum Jülich and the Paul Scherrer Institute in Switzerland in cooperation with international partners have made the first GeSn semiconductor laser, which is also the first made solely of group IV elements.

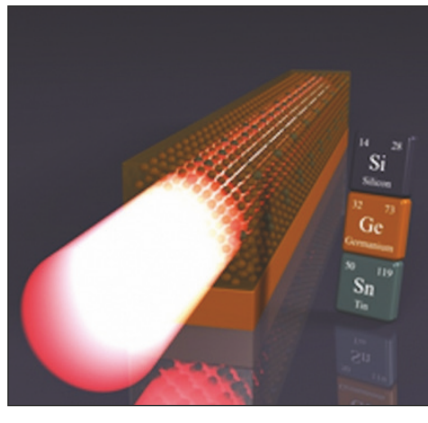
The GeSn laser can be applied directly onto a silicon chip, creating a new basis for transmitting data on computer chips via light: this transfer is faster than is possible with copper wires and requires only a fraction of the energy. The results were published in the journal Nature Photonics.

"Signal transmission via copper wires limits the development of larger and faster computers due to the thermal load and the limited bandwidth of copper wires. The clock signal alone synchronising the circuits uses up to 30 percent of the energy - energy which can be saved through optical transmission," explains Detlev Grützmacher, director at Jülich's Peter Grünberg Institute.

Typical semiconductor lasers consist of elements from groups III or V and their crystal properties are such that they cannot be directly integrated onto silicon. In contrast, group IV semiconductors - to which both silicon and germanium belong - can be integrated into the manufacturing process without any major difficulties, according to the researchers.

However, neither element is very efficient as a light source. They are classed among the indirect semiconductors. In contrast to direct semiconductors, they emit mostly heat and only a little light when excited. That is why research groups all over the globe are intensively pursuing the objective of manipulating the material properties of germanium so that it would be able to amplify optical signals and thus make it a usable laser source.

The scientists at Jülich's Peter Grünberg Institute have now for the first time succeeded in creating a 'real' direct group IV semiconductor laser by combining germanium and tin. "The high tin content is decisive for the optical



properties. For the first time, we were able to introduce more than 10 percent tin into the crystal lattice without it losing its optical quality," reports PhD student Stephan Wirths.

"The functioning of the laser is so far limited to low temperatures of up to -183˚C, however. This is mainly due to the fact that we worked with a test system that was not further optimised," adds Dan Buca. In cooperation with his colleagues fromSiegfried Mantl's group at PGI-9, Stephan Wirths applied the laser directly onto a silicon wafer whose properties were subsequently measured at the Paul Scherrer Institute in Switzerland.

PhD student Richard Geiger fabricated the laser structures there. "That way, we were able to demonstrate that the GeSn compound can amplify optical signals, as well as generate laser light," reports Hans Sigg from the Laboratory for Micro and Nanotechnology.

The laser was excited optically for the demonstration. Currently, the scientists in Dan Buca's group at Jülich are working on linking optics and electronics even more closely. The next big step forward will be generating laser light with electricity instead, and without the need for cooling if possible. The aim is to create an electrically pumped laser that functions at room temperature.

GaN Power conversion market to hit $1.1 Billion in 2024

ACCORDING TO A REPORT by Lux Research, the market for GaN discrete components in 2024 will reach $1.1Billion market. However, the substrate that the GaN device is built on - silicon, SiC, or GaN - makes a big difference in the cost and performance of the device. GaN-on-Si will dominate the GaN market for at least the next decade, growing to $1 billion in 2024, a 90 percent share, says the report.

"Of the three GaN flavours, GaN-on-Si will be the cheapest, pushing adoption of GaN-on-SiC or GaN-on-GaN out into the future," said Pallavi Madakasira, Lux Research Analyst and the lead author of the report titled, 'Breaking Down the Gallium Nitride Power Electronics Market'. Even though both GaN-on-SiC and GaN-on-GaN offer performance improvements over silicon, high prices for SiC and GaN substrates will limit adoption," she added. Lux Research analysts evaluated the overall GaN market, besides evaluating the growth prospects of the three GaN flavours. Among their findings are that transportation and renewables/grid are key markets. GaN-on-Si will be the runaway leaders in the renewables and grid markets, as well as transportation, attaining markets of about $350 million and $380 million, respectively, in 2024. Next in adoption will be IT and electronics.

GaN-on-SiC will grow the fastest. GaN-on-SiC will grow at a 46 percent CAGR from 2017 to 2024, reaching $140 million. Driven by the SiC substrates' ability to function efficiently at high temperatures, it will gain the most adoption in transportation. GaN-on-GaN is a non-starter for now.

The lack of cheaper GaN substrates and a relative lack of developers mean GaN-on-GaN will have little commercial role in the next decade. More R&D is needed on cost-saving innovations like hybrid manufacturing processes.

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Epistar to buy TSMC's LED subsidiary

EPISTAR and TSMC have approved the sale of TSMC Solid State Lighting to Epistar for $25.85 million.

After the transaction, Epistar will own 94 percent of the company, and TSMC will exit the LED business. The company will be operated by Epistar and TSMC SSL's current team. TSMC SSL has recently developed high-efficiency LED lighting products using an innovative Phosphor-on-Die (PoD) chip-scale packaging technology. However, the company has struggled to reach profitability due to oversupply following the massive expansion of the LED industry in the past few years.

As a late entrant, TSMC SSL has also faced difficulties overcoming patent obstacles and establishing sales channels. Epistar is the world's largest manufacturer of LED epitaxial wafers and dies, with patents recognised by the major industry players, cross-licensing with Philips and Toyoda Gosei, and a wide network of sales channels covering customers across the globe.

Speaking on his hopes for collaboration, TSMC SSL chairman Steven Tso said: "I believe that we can reach a win-win scenario with TSMC SSL led by Epistar and SSL's present team. Epistar's operations can take off with redoubled strength, the development of the LED industry will accelerate, and consequently TSMC SSL's shareholders and employees will benefit as well."

LED lighting demand is expected to increase significantly between 2014 and 2017, with a rapid increase in penetration rate. Epistar successfully acquired Formosa Epitaxy at the end of 2014 with the goal of obtaining the capacity and talent needed to drive growth.

Aixtron to continue restructuring

AIXTRON, the German maker of semiconductor deposition systems, has announced that as part of its continuing reorganisation, it plans to reduce around 60 of 800 jobs across the group.

Additionally, it will be continuing with other cost-cutting measures, and pursuing new market opportunities, for example with its new AIX R6 next generation MOCVD tool for LED manufacturing and in future business fields such as power and logic semiconductors as well as OLED.

"Letting employees go is never easy. As management, however, we have a responsibility for the whole company. Having reduced the executive board to two members in the middle of last year already should be viewed in the same light", said Martin Goetzeler, CEO.

"Customer needs are evolving. The focus is increasingly on process and user-oriented solutions while we are executing our productivity programs in all areas of the company", commented Bernd Schulte, chief operating officer.

Aixtron will present its figures for the 2014 financial year and provide an outlook for the current year on February 24, 2015.

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International Rectifier now part of Infineon

INFINEON TECHNOLOGIES AG has announced the closing of the acquisition of International Rectifier. The El Segundo based company has become part of Infineon following the approval of all necessary regulatory authorities and International Rectifier's shareholders.

"The acquisition of International Rectifier is an important step for Infineon to foster our position as a global market leader in power semiconductors. We are sure that International Rectifier and its employees will make a great contribution to a joint successful future. Together both companies make a powerful combination", says Reinhard Ploss, CEO of Infineon. "We offer our customers an unparalleled product portfolio.

Infineon's board (L - R): Arunjai Mittal, Reinhard Ploss, and Dominik Asam

Our profound understanding of their needs enables us to provide the best possible and competitive solutions. The acquisition helps us to accelerate our strategic approach 'from product thinking to system understanding'."

The combined company is led by Reinhard Ploss, CEO, Arunjai Mittal, Member of the Management Board Regions, Sales, Marketing, Strategy Development and M&A, and Dominik Asam, CFO. President of International Rectifier and of Infineon North America is Robert LeFort.

International Rectifier is complementary to Infineon: the combined company gains greater scope in product portfolio and regions, especially with small and medium enterprise customers in the US and Asia. The merger taps additional system know-how in power management. It expands the expertise in power semiconductors, also combining leading knowledge in compound semiconductors, namely GaN.

Furthermore, the acquisition will drive greater economies of scale in production, strengthening the competitiveness of the combined company.

The acquisition is expected to be accretive to pro-forma earnings per share (EPS) already in the current fiscal year. Synergies are expected to further drive significant accretion, building on International Rectifier's existing successful operational restructuring.

At the latest within fiscal year 2017, International Rectifier's margin contribution is expected to be at least in line with Infineon's target of 15 percent Segment Result margin over the cycle.

On August 20, 2014, Infineon had announced that it was to acquire International Rectifier in a deal worth approximately $3 billion.

The Board of Directors of International Rectifier and Infineon's Supervisory Board unanimously supported the offer of Infineon to pay USD 40 per outstanding share. Subsequently, all regulatory authorities had approved the acquisition - as did the shareholders of International Rectifier with a majority of 99.5 percent of all votes cast.

SAMCO offer customer demos on new GaN-on Si MOCVD system

SAMCO, the Japanese semiconductor process equipment company, has announced MOCVD demonstration capability on a new GaN-on-Si system, the GaN-550, from Valence Process Equipment Inc (VPE) of Branchburg NJ, USA.

SAMCO sells and distributes the GaN-550, which is equipped with a 550 mm in diameter carrier for mass production of GaN power devices. The demo system will be available for customer demonstrations at SAMCO's R&D facility in early 2015. SAMCO is expanding its wide range of dry etching and plasma-enhanced chemical vapor deposition (PECVD) systems for wide-bandgap semiconductor applications such as LEDs, laser diodes and RF devices. One of SAMCO's strengths is the process of nitride semiconductors, which play important role in green electronics.

VPE is a start-up company, providing MOCVD systems for GaN-based LEDs. VPE's GaN-500 MOCVD system employs a unique reaction chamber design and is highly-efficient at reducing gas consumption by up to 40 percent compared with other MOCVD systems. SAMCO has installed a new GaN-550 MOCVD system, which was developed from GaN-500, and has low process gases consumption, high-speed gas switching, and superior temperature control.

The specially designed gas injector requires fewer reactor cleanings, which increases system availability and uptime.

The GaN-550 system can grow more than 5μm/hour GaN at the uniformity of less than 1 percent. While the carrier size of GaN-500 is 500 mm in diameter, the carrier size of GaN-550 is 550 mm in diameter for higher throughput, up to 2 inch x 72, 4 inch x 20, 6 inch x 7 or 8 inch x 4 per batch.

IQE: Financial end of year as expected

IQE PLC, a supplier of advanced wafer products and services, has provided an unaudited trading update for the year ended 31 December 2014.

The group's revenue for the year is expected to be approximately £112m, with second half revenues of around £60 million. Other headline trading figures are also expected to match expectations. EBITDA is projected to be up by around 8 percent year on year at approximately £27m, following a second half EBITDA of approximately £16 million. Adjusted, fully diluted EPS for the year is expected to be up around 20 percent at approximately 2.4p.

The company also says that net debt at 31 December 2014 will be around £31 million, down from £34.4 million a year earlier. This progress has been made after approximately £5 million of cash restructuring costs (now complete) and after approximately £8 million of contingent deferred consideration (payments of which will end in 2016).

The company says that the wireless business is enjoying an improved outlook, the photonics business continuing to show strong double digit growth, and the group's new technologies, including the development of the GaN, progressing well.

Drew Nelson, CEO and president of IQE plc, said: "We are excited by the market developments that are leading to the increasing deployment of compound semiconductor solutions across a range of applications, and that consequently offer potential for IQE to deliver continued steady growth as a result of the Group's unique position in the compound semiconductor materials marketplace.

He added: "We are confident about the progress that we expect to make during 2015. I look forward to updating shareholders on the how we are performing when we announce our final results in March."

The compound semiconductor materials that IQE makes are used in a diverse range of end markets including wireless communications, a broad range of consumer and industrial applications using advanced photonic lasers and sensors, high resolution infrared systems, advanced solar power (CPV), high efficiency LED lighting, and efficient power switching.

IQE is working with silicon chip companies and on a number of major government-funded programmes to develop next generation technology which will combine the scale and maturity of the silicon industry with the advanced properties of compound semiconductors.

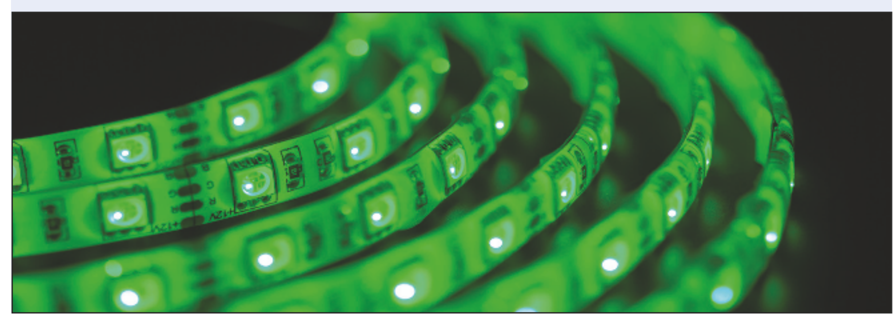
Historically, approximately 80 percent of IQE's sales have been into the wireless communications market.

This market continues to enjoy significant and sustainable long term growth, driven by the proliferation of increasingly complex wireless communication devices and systems such as LTE/4G, dual band WiFi, and GPS location devices, which require increasingly complex compound semiconductor solutions.

Soraa completes line of LED lamps

SORAA has extended its line of PAR and AR111 lamps to offer a full range of halogen replacement lamps from 50W to 120W halogen equivalent. The newly launched 12.5W line features a lower wattage addition to its award-winning, full visible spectrum PAR30 and AR111 LED lamps, while maintaining the high Centre Beam Candle Power (CBCP) characteristic of Soraa's lamps. Featuring Soraa's third generation GaN on GaN LED, the company's new 12.5W PAR30 lamps are for 75W to 120W equivalent lighting applications in retail, hospitality and museum environments; while the 12.5W AR111 lamps offer an efficient choice for retail applications.

"The market is awash in low performance, poor light quality PAR30 and AR111 LED lamps, so when we introduced our full visible spectrum large LED lamp portfolio earlier this year, the reception was outstanding. And I'm pleased to announce that today, we made those lamps better," explained George Stringer, senior VP Americas sales and marketing at Soraa.



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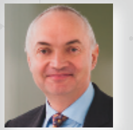

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Luc Van den hove, President & CEO, **imec**

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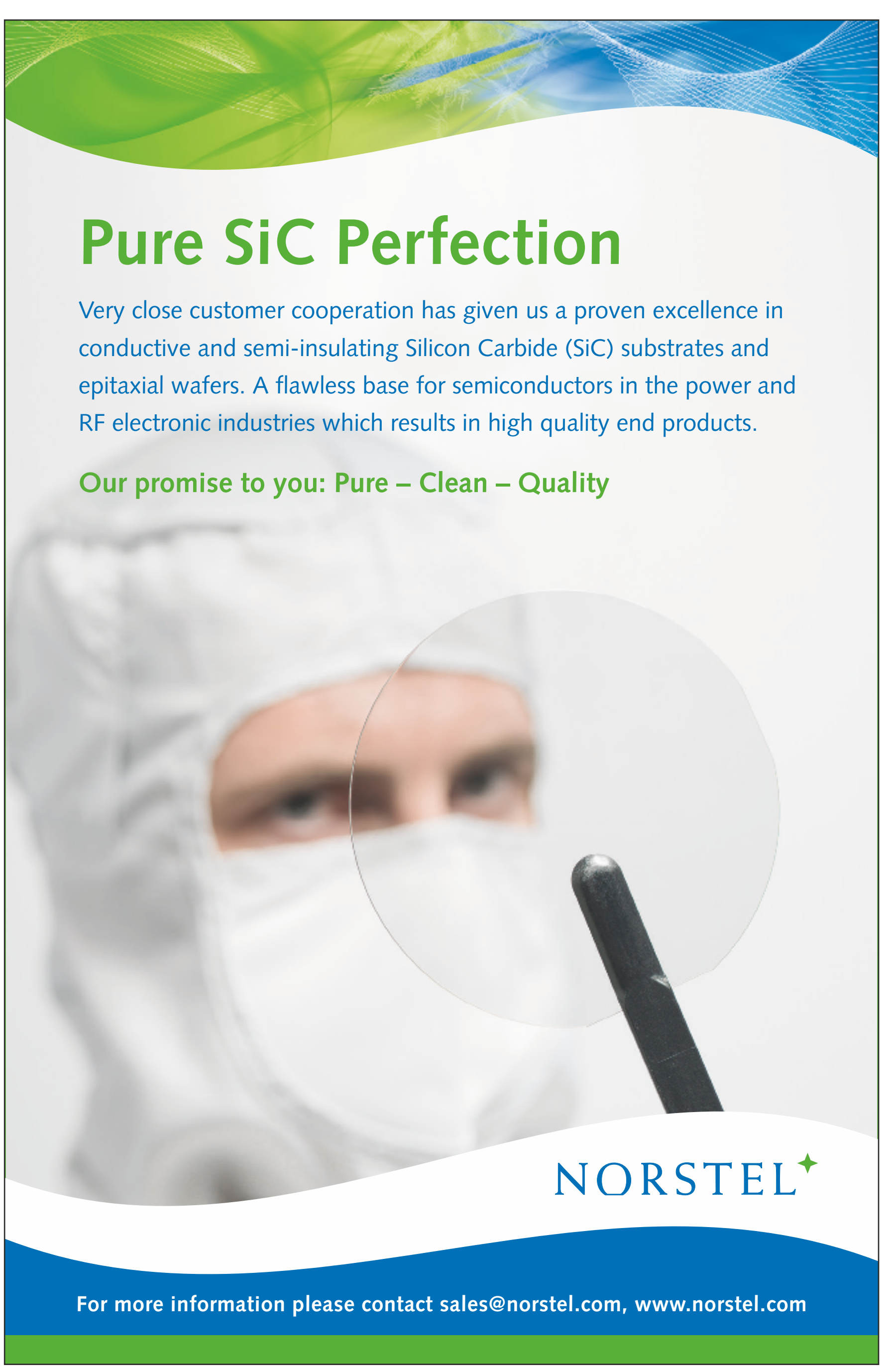
Sanan orders 50 GaN MOCVD reactors

VEECO INSTRUMENTS has won an order from Sanan Optoelectronics, the largest LED manufacturer in China, for 50 TurboDisc EPIK700 GaN MOCVD reactors for the production of LEDs.

"Sanan chose the EPIK700 due to its industry leading cost of ownership model and excellent footprint efficiency," said Zhiqiang Lin, Vice Chairman and CEO of Sanan. "Our beta testing of EPIK700 proved its production-worthiness, and we are confident in its capabilities and value to our Xiamen business expansion plans. Veeco has been a great partner for Sanan as we have solidified our position as the top LED manufacturer in China and increased our business outside of China as well."

Based on Veeco's TurboDisc technology, the EPIK700 MOCVD system should enable customers to achieve a cost per wafer savings of up to 20 percent compared to previous generation MOCVD systems through improved wafer uniformity, reduced operating expenses and increased productivity. "This large order from Sanan, the largest single purchase order Veeco has received since 2009, speaks volumes about the EPIK700's production readiness and the recovery in the MOCVD market," said John Peeler, Veeco's Chairman and CEO.

"We are in a great position to continue to serve our LED customers with the best MOCVD technology and customer support, and remain the industry leader."

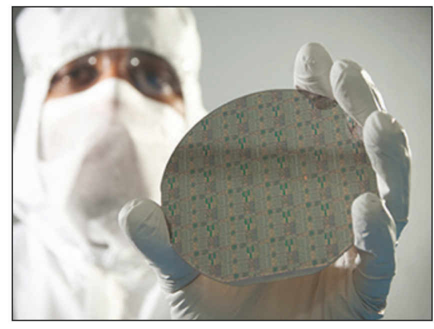


Raytheon GaN chips approved for space

RAYTHEON has successfully validated its GaN Monolithic Microwave Integrated Circuit (MMIC) technology for use in space-bound equipment.

Raytheon GaN MMICs, fabricated at its Andover, Massachusetts foundry, demonstrated the radiation hardness required for space through Single Event Burn-out (SEB) and Total Ionising Dose (TID) testing.

The results showed the devices are not susceptible to catastrophic failure caused by heavy ions. Further testing showed no loss of performance at exposure levels up to 1Mrad, significantly more than is needed for typical space applications.



"Raytheon's GaN technology is mature, robust, and already integrated into a number of defense systems for land, sea and air," said Paul Ferraro, Raytheon's vice president of Integrated Defense Systems' Advanced Technologies Programs. "Now that our GaN is validated for space, Raytheon customers can use this game-changing technology in a wide variety of space-based applications."

Cree launches extreme high power LEDs

CREE has announced the commercial availability of XLamp Extreme High Power (XHP) LEDs, a new class of LEDs that enable a system cost reduction of up to 40 percent for lighting applications.

The first LEDs powered by Cree's SC5 Technology Platform, XLamp XHP50 and XHP70 LEDs provide twice the lumen output and improved reliability compared to previous LEDs of the same size. The technology of the new XHP LEDs will help drive the next major innovations in lighting system design.

"Cree's new technology is game-changing compared to the incremental advances of other LED suppliers. The breakthrough performance of XHP LEDs enables both new design possibilities and dramatically lower system costs for LED lighting," said Nate Heiking, advanced lighting Product Manager, Kenall Lighting. "We're excited that Cree's new class of Extreme High Power LEDs will accelerate customer adoption of LED lighting."

XHP LEDs allow lighting manufacturers to reduce the size and cost of their lighting system design by using fewer, more reliable LEDs to achieve the same brightness. XHP LEDs enable new lighting designs that require fewer optics, a smaller printed circuit board, a smaller housing and less handling. XHP LEDs also achieve longer lifetimes even at higher operating temperatures and currents than previous LED technology, allowing lighting manufacturers to reduce heat sink size and cost without impacting the rated lifetime.

In addition, XHP LEDs enable other cost reductions at the system level not possible with other LED solutions. For example, in roadway and outdoor area lighting, on top of the luminaire cost savings, XHP LEDs can produce a radically smaller and lighter luminaire that requires a less expensive pole. Similar dramatic cost savings over existing solutions may be achieved in a wide variety of lighting applications, including track, stadium and high bay.

"Cree's new Extreme High Power LEDs demonstrate our belief that high-

power LEDs are what will drive the industry towards the next generation of lighting system designs," said Dave Emerson, Vice President and general manager for Cree LEDs. "Leveraging our groundbreaking SC5 Technology Platform, Cree's new XHP LEDs deliver not only exceptional performance, but also enable up to 40 percent system level cost reductions."

As the first LEDs to incorporate the SC5 Technology Platform, the new XHP LEDs are said to introduce significant advancements in light output, colour consistency and design flexibility.

XLamp XHP50 and XHP70 LEDs shatter the industry's perceived limit of LED lumen density by delivering up to 2546 lumens at 19 watts from a 5.0 x 5.0 mm package and up to 4022 lumens at 32 watts from a 7.0 x 7.0 mm package, respectively.

Through improvements in the light conversion process, Cree has reduced LED-to-LED color variations and, among other options, offers XHP LEDs in 2-step and 3-step EasyWhite bins for 3500K through 2700K in 80 and 90 CRI. The XHP LEDs introduce a new, innovative package that allows manufacturers to choose either 6 V or 12 V configurations from the same LED through the solder pad design on the circuit board.

Samples of both XLamp XHP50 and XHP70 are available now, and production quantities are available with standard lead times.

Emcore closes sale of tunable lasers and transceivers to NeoPhotonics

EMCORE, a provider of compound semiconductor-based components, subsystems, and systems, has completed the previously announced sale of its tunable laser and transceiver product lines for $17.5 million to NeoPhotonics.

With the closing of the transaction, Emcore received $1.5 million in cash and a promissory note from NeoPhotonics in the principal amount of $16 million.

The promissory note will mature two years from the closing date of the transaction, subject to repayments under certain circumstances, and is secured by certain of the assets sold to NeoPhotonics in the transaction. The purchase price is subject to certain post-closing adjustments for inventory, net accounts receivable and pre-closing revenue levels, which will increase or decrease the principal amount of the promissory note as applicable.

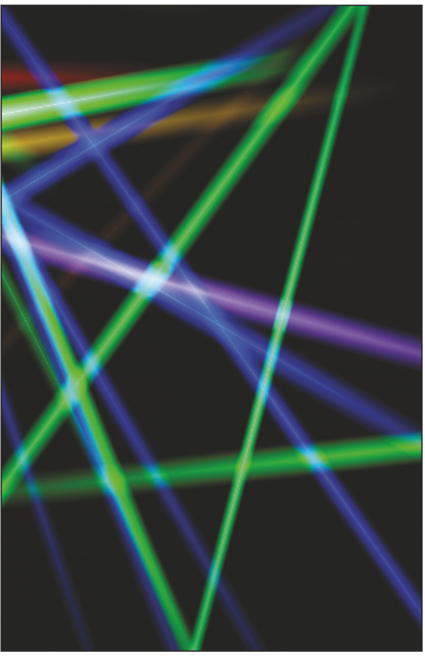
NeoPhotonics, based in San Jose, California, is a designer and manufacturer of photonic integrated circuit, or PIC, based optoelectronic modules and subsystems for bandwidth-intensive, high-speed communications networks. The sale includes Emcore's External Cavity Laser (ECL)-based Integrable Tunable Laser Assembly (ITLA), micro-ITLA, Tunable XFP transceiver and Integrated Coherent Transmitter (ICT) products for 10, 40, 100 and 400 Gbps telecoms networks.

Emcore retains its broadband fibre optics products including CATV transmitters and modules, Fibre-to-the-Premise transceivers, InP-based lasers, photodiodes and modulators, RF over fibre satellite communications products, video transport equipment, and microwave and speciality photonics products.

NSF awards half million dollars to develop arrays of blue and green VCSELS

THE US NATIONAL SCIENCE FOUNDATION (NSF) has awarded a $500,000 Faculty Early Career Development award to Daniel Feezell at the University of New Mexico to study VCELS. The 'Short-Wavelength Vertical-Cavity Surface-Emitting Laser Arrays Using Nonpolar and Semipolar GaN' project begins in March and continues through February 2020.

The goal is to develop arrays of blue and green VCSELs with stable polarisation of the light emission by using novel orientations of the GaN. Applications of this technology, according to Feezzell, could include improved high-density optical data storage and high-resolution printing, improved mobile displays and projectors, and advancements in chemical/biological sensing and atomic clocks.



One example of a possible practical application would be the addition of projection capabilities on smartphones. Feezell said such a projector could be included on the back of the phone, right next to the camera.

"This would allow your phone to become a display projector, so you could view movies, pictures, or PowerPoint slides on the wall or on a screen instead of directly on your phone," Feezell said. "You could basically have a projector in your pocket."

He said the vertical geometry of VCSELs has several advantages over conventional edge-emitting lasers, including high beam quality, small form factor, the ability to form densely-packed arrays, and lower power consumption. Feezell's work will focus on adding stable polarisation and increasing the output power using arrays.

Feezell said he will also be researching how to create a green VCSEL, which has not yet been developed. Red and blue VCSELs have been developed, and adding a green VCSEL would complete the RGB (red, green, blue) spectrum, allowing for the creation of white light, which makes possible technologies such as display screens or LED light bulbs for room lighting and other uses.

Much of the work on the project will be done at UNM's Center for High-Technology Materials, and some will be done in collaboration with the Center for Integrated Nanotechnologies at Sandia National Laboratories.

Feezell said he believes that GaN-based VCSELs hold untapped potential. "I love this particular topic of GaN-based VCSELs," he said. "It's still an immature field and many of the applications are still not developed or known."

The NSF CAREER program is geared toward helping early-career faculty get strong starts on their academic careers.

The award is NSF's most prestigious award in support of junior faculty who exemplify the role of teacher-scholars through outstanding research, excellent education, and the integration of education and research within the community. Such activities should build a firm foundation for a lifetime of leadership in integrating education and research.

VLC Photonics expand optical integration services

AS PART of its optical integration services, VLC Photonics is offering a new Multi-Project Wafer (MPW) Standard Design service for custom photonic integrated circuits (PIC) with fixed service costs for each manufacturer and cell size. The MPW shuttle runs are available on different generic technology manufacturing platforms such as Silicon-on-Insulator, PLC, TriPleX and InP.

"After several years in market, by serving customers and performing our own R&D using all the MPW manufacturers around the globe, we are ready to offer a frozen price, independent of the chip functionality", Pascual Muñoz, VLC Founder explained. "This is the equivalent to generic manufacturing, where costs are fixed by chip area independently of its content and end functionality, but at a design level" he added.

"The wide range of integration technologies and fabrication platforms makes selecting the best manufacturing approach for each application and device quite difficult for our customers," adds Iñigo Artundo, CEO of the company. "We learned our customers value an easy and straight-forward solution that allows to directly choose the most suited way to prototype their PICs". Artundo assures that any company with some basic experience on photonic integration will be able to navigate all the MPW design and manufacturing options currently offered by VLC Photonics.

"Customers will also be able to get approximate costs and manufacturing times to configure their own projects immediately. Furthermore, they will directly interface our engineers one click after, to clear out any hurdles they may find when facing any integration project".

Allos Semiconductors to offer Azzurro patents and technology

ALLOS SEMICONDUCTORS GMBH, formed in mid-2014 in Dresden, to focus on GaN-on-Si technologies and markets, has acquired the exclusive ownership of the technology, know-how, and IP of former Azzurro Semiconductors.

Azzurro, a spin-off from the University of Magdeburg in Germany, specialising in GaN-on-silicon epi-wafers and products, filed for bankruptcy earlier this year.

The driving force behind Allos Semiconductors' foundation in June was the growing demand for technology to grow GaN on silicon substrates. An increasing number of LED and power semiconductor companies want to master the technology to grow 150 and 200mm GaN-on-Si wafers successfully themselves to supply cost-effective high-quality GaN devices processed in standard silicon fabs.

According to Allos, there are tremendous technological challenges to make GaN-on-Si happen.

For Allos' customers, it says, the opportunity is to reduce not only cost and time-to-market but also the development risk by building their effort on Allos' proven GaN-on-Si platform and know-how. Now with the acquisition of Azzurro's IP, in addition to its existing offering, Allos will make the proven Azzurro technology platform available through technology transfer, licencing and customised development work.

Allos says that this will complement its service offering advice on business and technology strategies and supporting setting up GaN-on-Si operations all the way from establishing an epitaxial wafer fab to market entry.

EPC introduces 60V and 80V monolithic GaN half bridges

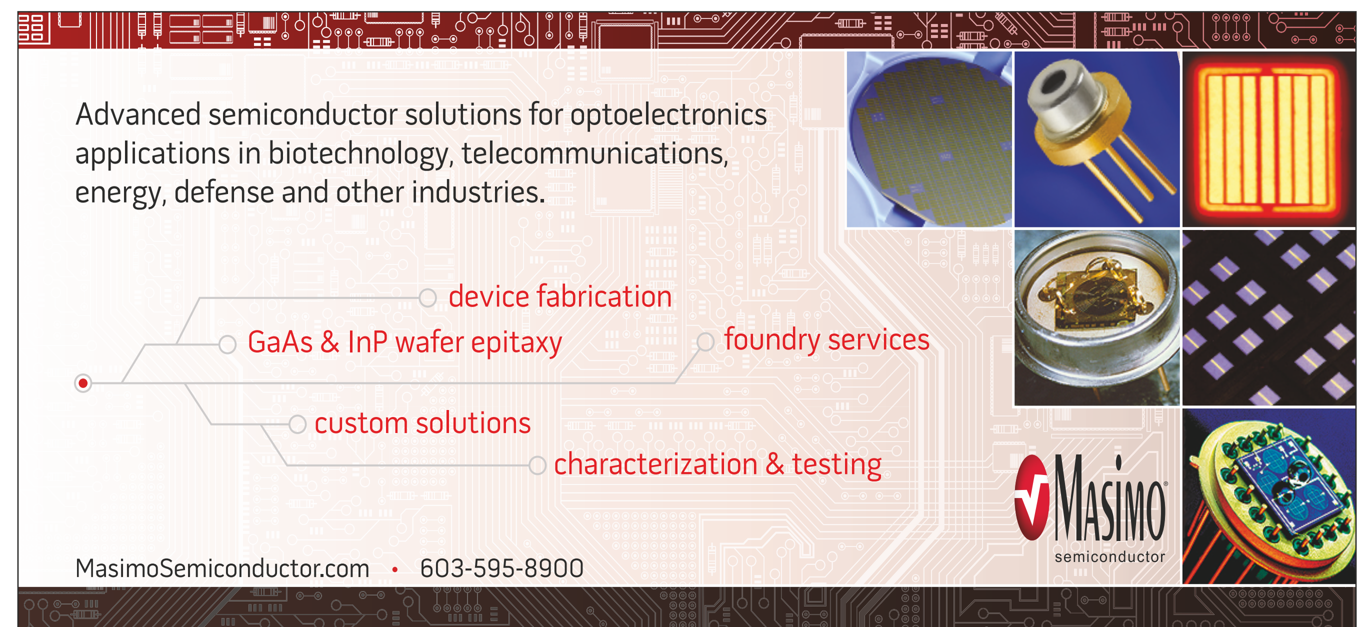
EPC has announced the EPC2102, 60V and the EPC2103, 80V enhancement-mode monolithic GaN transistor half bridges.

For applications requiring a symmetric device ratio, the devices provide monolithic half-bridge eGaN ICs with two equal-sized die. By integrating two eGaN power FETs into a single device, interconnect inductances and the interstitial space needed on the PCB are eliminated. This increases both efficiency (especially at higher frequencies) and power density, while reducing assembly costs, says EPC.

Using an EPC2103 in a typical buck converter, system efficiency is greater than 97 percent at 20 A, when switching at 500 kHz and converting from 48V to 12V.

The second device, the EPC2102 60 V half bridge, achieves 98 percent system efficiency at 18 A, when switching at 500 kHz and converting from 42 V to 14 V. In addition to the single-chip half bridges, two development boards are being announced. The EPC9038 and the EPC9039 boards contain one EPC2102 or EPC2103 integrated half-bridge component, respectively, along with a Texas Instruments LM5113 gate driver and all necessary supply and bypass capacitors.

The board has been laid out for optimal switching performance and there are various probe points to facilitate simple waveform measurement and efficiency calculation.



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SOLID-STATE LIGHTING

Soaring sales of LED bulbs are creating a great opportunity for chipmakers. But what do companies need to do to stand out from the crowd and win substantial orders while maintaining healthy margins?

Opportunities for laser diodes in solid-state lighting
Jon Wierer - SSLS Scientist - Sandia National Laboratories

ANALYST

How will the solid-state lighting evolution unfold, and what will it mean for the LED chipmakers?
Will Rhodes - Research Manager - IHS Technology

SPEAKER

Commercialisation of GaN-on-silicon for LEDs
Keith Strickland - Innovations & Technology Director - Plessey Semiconductors

SPEAKER

Increasing LED output with advanced plasma processing
Mark Dineen - Product Manager - Oxford Instruments Plc

SPEAKER

Yield optimisation of compound semiconductor processes through an effective metrology strategy
Torsten Stoll - Product & Marketing Manager - Nanometrics Inc.
nanometrics

SPEAKER

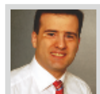
Plasma dicing for III/V and thin wafers
Reinhard Windemuth - Sales Director ME Europe - Panasonic Factory Solutions

OPTOELECTRONICS

Does the growth of the datacom market signal a long-awaited return to better times for the makers of optical components? Is CPV technology finally starting to gain a foothold in the solar industry?

KEYNOTE

Highest CPV cell and module efficiencies and CPV power plants
Rainer Krause - Director Smart Cell Development - Soitec

ANALYST

Where is the CPV industry heading, and what needs to happen to increase its market share?
Karl Melkonyan - Analyst Solar Research - IHS Technology

SPEAKER

Mid infrared LEDs enable portable, battery powered gas sensing
Des Gibson - CEO - Gas Sensing Solutions Ltd

SPEAKER

IC design for very high-speed optical communications – a holistic approach
The' Linh Nguyen - Senior Manager IC Development- Finisar Corporation

SPEAKER

UV LED - We are just scratching the surface of the technology's true potential
Pars Mukish - LED & Sapphire Activities Leader - Yole Développement

SPEAKER

Unlocking opportunities for compound semiconductors with micro assembly
Chris Bower - CTO - X-Celeprint Ltd

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III-V CMOS

By the end of this decade, it is said that silicon CMOS will have run out of steam. But what role will III-Vs have to play in the microprocessors of the future?

Heterogeneous integration of III-Vs and CMOS
Daniel Green - Program Manager - Defence Advanced Research Projects Agency

ANALYST

When will III-Vs make an impact in the silicon foundries? And will it last for long?
Mike Corbett - Managing Partner - Linx Consulting

LINX-Consulting

SPEAKER

III-V FETs for future logic applications
Jesús A. del Alamo - Director of the Microsystems Technology Laboratories - MIT

SPEAKER

Opportunities and challenges of III-Vs in Si-based nanoelectronics industry
Matthias Passlack - R&D Deputy Director Europe - Taiwan Semiconductor Manufacturing Company

SPEAKER

Advanced in-situ metrology for III-V on silicon technology
Kolja Haberland - CTO - LayTec AG

SPEAKER

Eliminating material borders for heterogeneous integration through new wafer bonding processes
Thomas Uhrmann - Head of Business Development - EV Group

FRONT-END MOBILES

What's the biggest threat to revenues for GaAs power amplifiers? Is it the emergence of multi-band, multi-mode PAs built with this material, or the emergence of CMOS solutions?

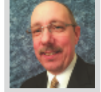
KEYNOTE

The path to intelligent integration
Jim Cable - CEO, President and Chairman - Peregrine Semiconductor Corporation

ANALYST

Multi-mode, multi-band PAs: friend or foe to the compound semiconductor industry?
Eric Higham - Director - Advanced Semiconductor Applications - Strategy Analytics

SPEAKER



Improving system level integration and overall efficiency
Ed Anthony - VP Engineering - Skyworks Inc.

SPEAKER

LTE is driving complexity in smartphone design
Sean Riley - VP of Mobile Products - Qorvo

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POWER ELECTRONICS

From a performance perspective, GaN and SiC are superior to silicon, but high prices are holding the materials back from displacing the incumbent silicon. How can this be addressed?

KEYNOTE

Ditching the package to drive down GaN transistor costs
Alex Lidow - CEO and Co-Founder - Efficient Power Conversion Corporation

ANALYST

When can WBG power electronics truly take off?
Pierric Gueguan- Senior Power Electronics Market Analyst - Yole Développement

SPEAKER

SiC technology in Power Electronics – A step change in value
Tang Yong Ang - VP Compound Semiconductors - Dow Corning Corporation

SPEAKER

High performance GaN-on-Si power epiwafers employing rare earth oxide buffer layers
Andrew Clark - VP Engineering - Translucent Inc.

SPEAKER

Automated defect monitoring strategy for surface and photoluminescence yield impacting defects
Brian Crawford - Director of Business Development - KLA-Tencor

SPEAKER

Driving down costs for next-generation PVD processes
Reinhard Benz - VP Sales and Marketing - Evatec Ltd

SPEAKER

Gallium nitride epitaxy on large area silicon substrates for power applications
Yoga Saripalli- Principle Engineer - GaN Epitaxy Group - imec

SPEAKER

Optimisation of III-V R&D and manufacturing using advanced analytical methods
Temel Buyuklimani - Senior Director, Quadrupole SIMS Services - Evans Analytical Group

SPEAKER

Accelerating GaN power electronics devices using MOCVD technology
Sudhakar Raman - VP Marketing - Veeco Instruments

SPEAKER

Measurement solutions for high power WBG semiconductor materials and devices. How to optimise and minimise power conversion switching loss
Stewart Wilson - European Business Manager - Keysight Technologies

SPEAKER

Cutting conversion losses with cost-efficient GaN-on-silicon
Marianne Germain- CEO - EPiGaN nv

RF-ELECTRONICS

The potential of GaN in the RF arena has never been in doubt. But does it now satisfy all the requirements for deployment in the most taxing situations?

KEYNOTE

GaN for radar applications
Takahisa Kawai - General Manager - Sumitomo Electric Device Innovations, Inc.

SUMITOMO ELECTRIC DEVICE INNOVATIONS

ANALYST

The future for GaN, SiC, InP and GaAs in defence/military applications
Asif Anwar - Director - Strategy Analytics

STRATEGYANALYTICS

SPEAKER

GaN for commercial RF applications enabled by the pure-play foundry model
Walter Wohlmuth - Associate VP Technology - WIN Semiconductors Corporation

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Anvil sizes up LED markets

Can SiC power electronics player, Anvil Semiconductor, deliver high performance green LEDs at CMOS prices? Rebecca Pool finds out more.

WHILE ANVIL SEMICONDUCTORS has carved a name for itself developing SiC power semiconductor switches based on its novel, low pressure CVD growth process, the UK-based Warwick University spin-off is now eyeing LED markets. Joining forces with the Cambridge Centre for GaN at the University of Cambridge, the organisation has grown cubic GaN on cubic SiC-on-silicon, or 3C-SiC-on-silicon, wafers via MOCVD. Sample LEDs are next.

"We've been talking about growing cubic GaN on cubic SiC for around a year, as this potentially opens up the LED market for our 3C-SiC on silicon material," explains Jill Shaw, chief executive at Anvil Semiconductors.

"Growing cubic GaN is very difficult and nobody has successfully done it using a commercialisable process before, partly because they haven't grown it on the (100) face of a reasonably lattice matched substrate such as cubic SiC," she adds.

As Shaw highlights, the company's intellectual property lies in growing cubic SiC-on-silicon for power device applications. Prior to SiC growth, a mask is placed over the silicon wafer to define structures in the scribe lines of the wafer.

Anvil researchers then deposit a 1.5 μm-thick layer of heavily doped, dislocated material onto this silicon seed wafer to relieve stresses from lattice mismatches during SiC growth.

An Anvil wafer: researchers have grown cubic GaN layers on the cubic SiC-on-silicon wafers

Monocrystalline 3C-SiC is then grown in the die area between the scribe lines – where future devices will be fabricated – with polycrystalline SiC forming in the lines to soak up the thermal expansion differential stresses across the entire wafer.

Having fabricated 650 V Schottky diodes, MOSFETs and more, the process clearly works for power semiconductors, but can it stretch to LEDs?

While researchers worldwide have already grown conventional hexagonal GaN on sapphire, SiC, bulk GaN and silicon wafers, via MOCVD, cubic GaN is a different matter. Compared to hexagonal GaN, the cubic polymorph has no internal electric fields, a narrower bandgap and faster transport properties, paving the way to better performing green LEDs. However, the cubic phase of GaN is metastable, so from a thermodynamic perspective, the crystal structure of the semiconductor tends to revert to the lower energy hexagonal polymorph.

But, by modifying MOCVD parameters such as gas flow and temperature, the Cambridge Centre for GaN team managed to grow cubic GaN on quadrants from Anvil's 100 mm diameter 3C-SiC-on-silicon wafer.

"The Cambridge researchers actually said they didn't think the cubic GaN phase would be stable and growth would be difficult," says Shaw. "But by carefully selecting MOCVD parameters they successfully grew single phase cubic GaN straightforwardly and at a similar growth rate to hexagonal GaN."

With success in hand, the researchers are also growing multi-quantum well structures onto the material, the next step to proving the material can be used to make LEDs.

Indeed, as Shaw puts it: "So far all we have done is demonstrate that you can produce cubic GaN on cubic SiC; we've still got to be able to develop LEDs."

But having applied for a government-funded Innovate UK award – designed for developing innovative engineering ideas – Shaw and colleagues are hopeful a demonstration LED could be developed within a six month programme.

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In the meantime, cost remains an obvious issue. Talk to LED industry players, and the jury is out on whether or not GaN-on-silicon LEDs actually make financial sense.

Proponents point to how fully depreciated CMOS equipment can be used to cheaply grow decent-performing LED structures on large silicon wafers. Meanwhile, others question the cost-savings as sapphire wafers get bigger and the performances of GaN-on-sapphire LEDs improve.

But for Shaw, Anvil's route to LEDs could offer a key advantage. "With our process, you have the advantage of fabricating LEDs on a large silicon wafer but potentially you also get efficiency improvements from using cubic GaN," she says. "So we're effectively bringing the performance benefits of LEDs made in cubic GaN grown on SiC down to silicon prices."

The business case is compelling, and as Anvil awaits government funding to proceed, Shaw is eyeing potential industry partners to help commercialise the technology."We intend to act as a fabless supplier of 3C-SiC-on-silicon wafers in the LED market," she says. "So partners could range from larger LED manufacturers that want to develop LEDs on cubic GaN on 3C-SiC-on-silicon wafers to substrate suppliers. There is a wide range of opportunities as far as we're concerned."

Terahertz triumph

As Northrop Grumman and DARPA smash electronics speed records, project leaders reveal this is only the beginning. Rebecca Pool reports.

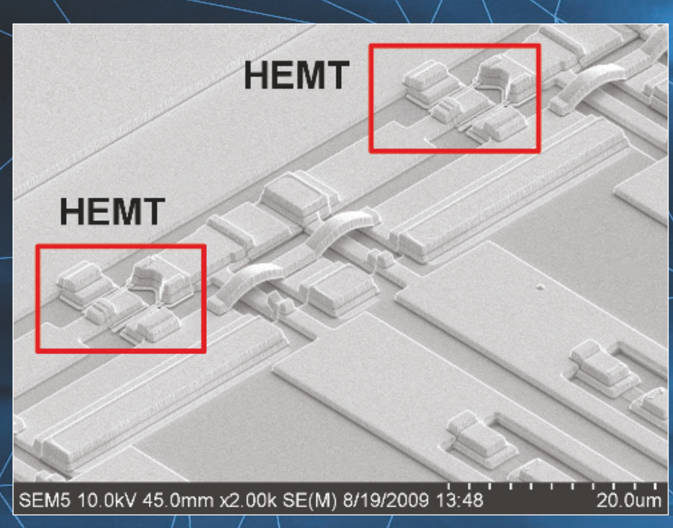
In late 2014, Northrop Grumman and DARPA set a world record with a breathtakingly fast terahertz integrated circuit amplifier, opening the door to extra-sensitive spectrometers, incredibly high resolution imaging and high capacity data networks.

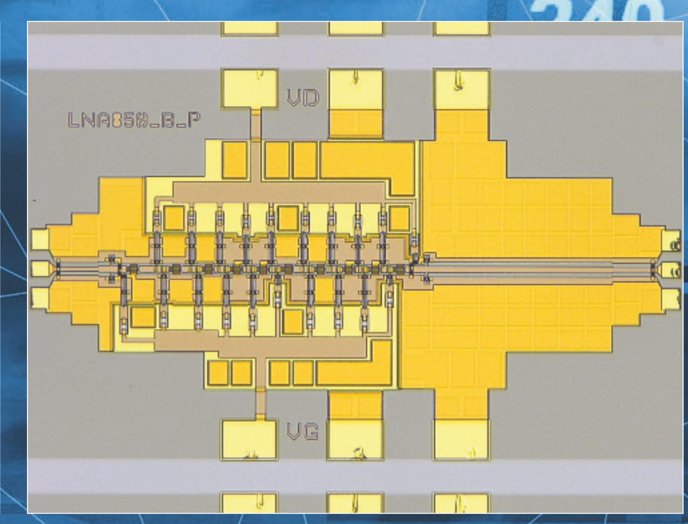
The amplifier uses ten, 25 nm InP HEMTs in series to produce an overall gain of 10 dB at 1 THz, and 9 dB at 1.03 THz. These power gain figures massively outstrip those in state-of-the-art ICs, and according to the Northrop Grumman-DARPA team, this is only the beginning.

"The team has made an amazing breakthrough by demonstrating an amplifier at 1 THz," says Dev Palmer, program manager of DARPA's THz Electronics program. "The theoretical maximum operating frequency of this technology is somewhere between 2 and 3 THz, so there's plenty of room at the top."

Terahertz is the slice of the electromagnetic spectrum that lies between infrared light and radio waves, from 300 GHz to 3 THz. Called the sub-millimetre wave frequency band, the wavelengths here are shorter than 1mm and able to penetrate many materials without using ionising radiation.

The chief aim of the Terahertz Electronics programme has been to fabricate all the components, from the subcomponents of an exciter to the parts for a receiver, needed to make a terahertz radio. To date, Northrup





DARPA's terahertz monolithic integrated circuit is the first solid-state amplifier demonstrating gain above 1 THz (1012 GHz).

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Grumman, has achieved just this at 700 GHz and 850 GHz and is set to repeat history at a terahertz.

"A decade ago, there was no consensus in the scientific community whether an integrated circuit operating at one terahertz was technologically possible," says Bill Deal, program manager of Terahertz Electronics at Northrop Grumman "But, as an interdisciplinary team of scientists and engineers, [we have] worked together in scaling all facets of MMIC technology to enable this result."

The next crucial step is to increase the gain of the amplifier IC from 10 dB to more than 15 dB. As Deal explains: "We want to increase the gain to a level where it makes sense to package the component, and then it becomes a very easy-to-use laboratory component."

"To do this we need to get our gain above 15 dB, and we hope to achieve this in a matter of months," he adds.

And of course, scaling the electronics to boost gain and speed is as important as ever. Using MBE, Deal and colleagues grow the InP-based transistor's epitaxial layers, then using electron beam lithography to fabricate a T-gate to form the transistor. Scaling the gate length is really critical," says Deal. "It reduces the capacitances and increases the maximum frequency of oscillation of the transistor, allowing the device to have gain at higher frequencies."

And while the gate length of a III-V device to 25 nm is small – today's standard CMOS processes have only just hit 14 nm – future gate sizes could shrink further yet.

"We do have some experiments aimed at shrinking the gate to as low as 20 nm," says Deal. "But a lot of this is very experimental and and other parts of the device have to be scaled at the same time to improve performance."

DARPA's Palmer has no qualms about the project's success, highlighting: "Northrop Grumman has demonstrated all components at 700 and 850 GHz, so I think it's well within their capability to build the same at 1 THz."

In the meantime, the team is also working on fabrication. In Deal's words, 'it's a very sophisticated process', but the researchers have fabricated the amplifier IC across several runs, each comprising batches of typically six wafers. Statistical analyses are underway as transistor performances are monitored and improved.

Deal reckons the early adopters of the technology will be other researchers. "I actually see scientists using it first for applications such as atmospheric sensing and radio astronomy," he says. "These researchers are pushing the limits on the types of measurements they can do."

The project has also received interest from businesses looking to establish large bandwidth, short range data connections between data farms using radio links instead of fibre optics cable.However, the key applications are high resolution radar imaging and spectroscopy. "For high resolution imaging, image resolution increases as wavelength shrinks," explains Palmer. "And we have many molecules, including industrial chemicals, with distinct signatures in this frequency band for rotational spectroscopy."

And the breakthrough also brings good news for high data rate communications. "Even very small fractional bandwidths at terahertz frequencies are many gigahertz wide," adds Palmer. "So you can get high data rates without resorting to complex modulation schemes."

GaN substrates

fresh from China

A China-based manufacturer of GaN materials is ready to rival western players; Rebecca Pool talks to Wang Jianfeng of Nanowin to find out more.

IN LATE OCTOBER, China-based semiconductor business, Nanowin, revealed plans to mass-produce high quality 2-inch GaN substrates with industry-low dislocation densities.

Targeting blue and green laser diode markets, the company claims to have demonstrated high-performance devices and is now intent on becoming a world-leading nitride semiconductor material provider.

As Nanowin chief technology officer, Wang Jianfeng, points out, HVPE-grown GaN substrates, with a thickness of less than 1 mm, typically have a dislocation density of around 1×10^5 cm^{-2}. However, the dislocation density of his company's substrates comes in at a much lower 1×10^4 cm^{-2}.

The key to the company's impressive results lies in clever nanostructure etching at the initial GaN film surface and carefully controlled growth conditions. Using electrodeless photoelectrochemical etching, Jianfeng and colleagues etch arrays of nanopyramids into GaN films, grown on sapphire substrates, to relieve compressive stress within the film.

"We do some interface engineering at the GaN surface, fabricating nanostructures and then optimising initial growth conditions to reduce the dislocation density," explains Jianfeng. "From the high quality GaN nanostructure layer, we then grow a very high quality GaN nanolayer."

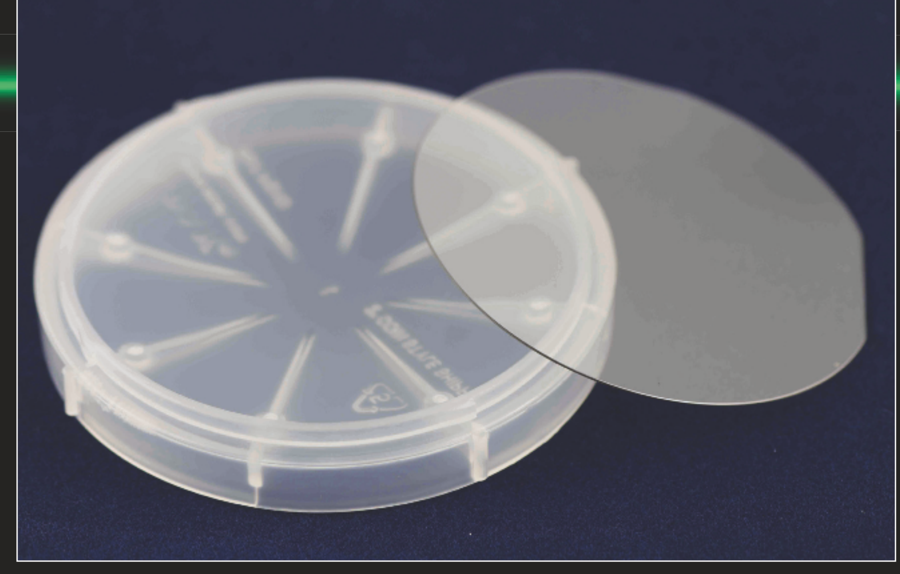
The GaN substrate is grown via HVPE on a 'home-made' system that, according to Jianfeng, incorporates an *in-situ* optical monitoring system. During GaN growth, Jianfeng and colleagues can closely monitor myriad characteristics including wafer curvature, refraction and reflections, adjusting parameters accordingly to ensure uniform growth.

Clearly fabrication requires skilled intervention, but the company claims to currently be churning out around 200 substrates a month and according to Jianfeng, can produce up to 700 substrates a month.

"Our yield is around 75 percent," adds Jianfeng. "And in three years time we will be manufacturing more than 1000 pieces a month with a dislocation density of only 1×10^4 cm^{-2}. These substrates will be for laser diode manufacturers."

Indeed, working with the Suzhou Institute of Nanotech and Nanobionics, Nanowin has already manufactured blue laser diodes with low threshold current density, low operation voltage and long lifetimes as well as green laser diode structures with, as Nanowin puts it 'excellent luminescence homogeneity'.

And the company also claims to have fabricated LEDs, based on its GaN



China-based Nanowin is ramping up manufacture of its two inch GaN substrates

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wafers, with injection current densities larger than those reported by US-based Soraa and more than 30 times greater than typical GaN-on-sapphire LEDs.

Nanowin has yet to secure any firm contracts with laser diode manufacturers, although as Jianfeng is keen to point out: "We are keeping close contacts with Osram, Nichia, Sony, Panasonic, Soraa for example, as well as new start-up companies in China."

And without a doubt, the company's wafer costs have appeal. Today's two inch GaN wafer, with a dislocation density of between 1 x 10^6 cm^{-2} and 1 x 10^7 cm^{-2} would set you back some US$1500 while the cost of a wafer with a lower dislocation density of around 1 x 10^5 cm^{-2} rises to around US$3000.

But as Jianfeng highlights, a Nanowin wafer will cost between US$1500 to US$1800, and as he adds: "I think the cost will rapidly reduce with volume production."

Contracts and costs aside, if the company is to makes waves in the worldwide GaN wafer marketplace and rival the likes of Hitachi Cable, Mitsubishi Electric, Sumitomo, Kyma and many, many, more, it will need a water-tight intellectual property portfolio. Jianfeng isn't fazed.

"We already have forty patents in China," he says. "And right now we have several patents pending in the US, Europe and Japan."

M/A-COM

the future and beyond

Late last year, M/A-COM added BinOptics to its ever-growing line of industry acquisitions. Where next for the high performance semiconductor supplier?

Given its recent BinOptics deal, no matter how you look at it, M/A-COM has set itself up for the future. This, the latest in a steady stream of acquisitions, secures the company a rock solid foothold in a network market, slated for growth, growth and more growth.

Globally, Cisco has predicted that mobile data traffic will grow 11-fold from 2013 to 2018, representing an annual compound growth rate of 61 percent. More data traffic will drive demand for data storage and networks across the board, an opportunity that M/A-COM is set to capitalise on.

"M/A-COM has been a provider of high performance analogue, RF, microwave, millimetre-wave solutions and now we have added photonics as well," says Vivek Rajgarhia, director of strategy. "Our strategy has been to create a portfolio of different semiconductor technologies – CMOS, GaN, SiGe, InP, GaAs and now silicon photonics – so we can pick and choose the right technology for the right application, market and performance parameter."

The first key addition came in 2010, when the then predominantly GaAs semiconductor developer, M/A-COM, acquired high-frequency point-to-point GaAs chipset maker, Mimix Broadband, to bolster its high performance semiconductor offering. Then, in 2011, the company bought Optomai, adding GaAs and InP-based ICs and modules for 40G and 100G fibre optic networks to its CATV/broadcast and point-to-point/infrastructure businesses.

Following this entry point into the 100G optical space, the company snapped up Mindspeed in 2013, adding more weight to its 100G optical networking products and gaining a firm foothold in SiGe markets. GaN RF semiconductor developer, Nitronex, followed in early 2014, extending M/A-COM's product reach from pulsed avionics to continuous wave applications. And then silicon photonics design company, Photonics Controls, and microelectronics prototyping business, IKE Micro, were scooped up soon afterwards.

The latest acquisition of BinOptics positions M/A-COM strongly as a merchant supplier of InP-based laser diodes in optical communications markets. But, crucially, as Rajgarhia highlights: "This is a transformative acquisition, moving us from purely optoelectronics and into photonics."

With BinOptics, M-A/COM can now flood data centre, mobile backhaul, silicon photonics and access network markets with InP lasers. And factoring in all acquisitions, the company has the key the building blocks to provide 100G and 400G transceivers for high speed datacomms.

"We have been, for example, supplying TIAs, CDRs and modulators, but with BinOptics, we now have the laser chip as well," highlights Rajgarhia. "Photonics Controls provides us with silicon photonics so now we have both transmit and receive functions, and all the key building blocks to enable a 100G transceiver."

"We have essentially consolidated all the high speed semiconductor content in 100G and 400G transceivers and are well positioned from the data centre to the longhaul optical segments," he adds.

Business as usual

So what now for BinOptics? Rajgarhia confirms that for the company, it is business as usual. "Their photonics products are completely complementary to our capability and we are expanding capacity."

Indeed, in M-A/COM's recent earnings call, chief executive John Croteau highlighted capacity constraints in data access markets. Given this, he said the company intends to double BinOptics's capacity in six months, quadruple output in a year, and as he added: "[There] is exponential growth potential, and ... revenues could scale accordingly."

Rajgarhia also expects significant demand from silicon photonics markets. "Silicon photonics is the

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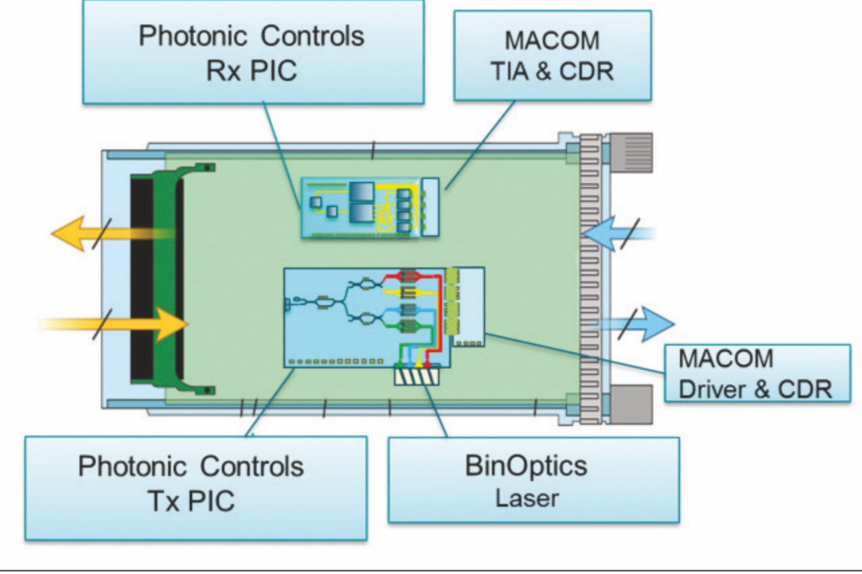
M/A-COM intends to cash in on data centre growth and more.

upcoming field especially in data centres, and we are designing silicon photonics chipsets for 100G and beyond applications."

However, the strategy director doesn't expect the technology to become mainstream in 100G equipment modules for at least two years. "For data centre markets overall we could use silicon photonics, InP or directly modulated lasers," he adds. "And while data centres are definitely a big growth segment, metro and longhaul markets will also see significant growth."



100G transceiver: With its acquisitions, M-A/COM now offers a one-stop shop for all the key components for their customers to build next generation transceivers.

But BinOptics doesn't just boost M-A/COMs photonics offering, it also provides the company with a well established customer base across Asia Pacific. Industry reports claim nearly all of BinOptics's revenue comes from this region, and without a doubt, M-A/COM will, again, capitalise on this fact.

"BinOptics is strong in Asia and we can expect to expand here, as well as into Europe and North America," says Rajgarhia, who will not be drawn on any future acquisitions for M-A/COM:

"We do not want to get into the same space as the Broadcoms. We are in the high perfomance, not the commoditised space, and in plain words I describe our strategy; 'if the product is difficult to make and difficult to sell, then that's the business we are in."

VCSEL visions

As VCSEL manufacturers prepare for industry growth, Anadigics intends to be the first to capture market share. Rebecca Pool reports.

WITH THE VCSEL market poised for rapid growth, semiconductor manufacturers worldwide are ready for action. In March 2014, a pan-European consortium including IQE, Philips and ST Microelectronics unveiled bold plans to get VCSEL fabrication ready for volume production in just three years.

Eight months on, Anadigics has joined the VCSEL race offering VCSEL foundry services and having developed the industry's first 6-inch VCSEL wafer fabrication process. But with production volumes slated for next year, the US-based developer of GaAs semiconductors looks set to lead the pack.

"We have adapted the six inch facility that we've used for our RF processes," says David Cheskis, director of optical products at Anadigics. "We've produced a lot of VCSEL wafers here, customers are sampling products based on these and we believe we will transition to production volumes in the second half of 2015."

As Cheskis points out, the 6-inch VCSEL line is not a world away from the company's 6-inch analogue GaAs wafer fab that opened fifteen years ago.

"We work off the same baseline processes with etch tools, position tools and metallisations, and many of the processes have been ported over or adapted from our RF process," he explains. "But we have also needed to implement several different processes that are unique to the VCSEL flow."

"For example, an oxidation furnace has been acquired that was not part of the RF process, and we've developed other rather unique proprietary steps that enable us to fabricate the VCSEL on a six inch [line] using the same basic tool set," he adds.

In addition, Cheskis's team has devised a metal contact process, adapted from that used for RF products and also developed unique 6-inch VCSEL on-wafer test capabilities.

The Anadigics director is certain manufacturing VCSELs on 6-inch wafers is going to be crucial to the technology's success. For starters, fabricating VCSELs on the larger GaAs wafers will bring far greater economies of scale than those manufactured within today's three and four inch fabs; cost per square millimetre is lower with more die made per wafer.

And while VCSELs are generally fabricated in a way that may resemble

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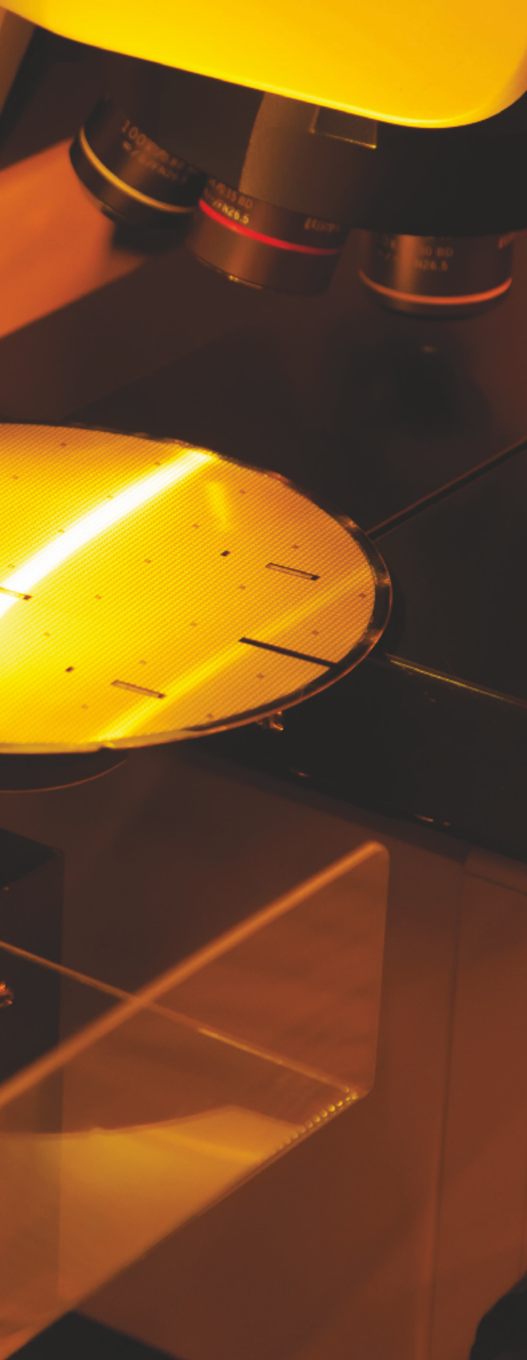

Left: VCSEL ambition: six inch wafers at Anadigics' manufacturing facility in New Jersey, US.

LED or CMOS processing, manufacturing is still relatively slow, and at best, takes place on 4-inch wafers where process control can be limited and some production steps are still manual.

As the Anadigics director puts it: "The fabs that people use to make three and four inch wafers are very much like laboratories, but our state-of-the-art GaAs facility runs 24 hours a day, seven days a week with the latest operating systems and tools."

"One thing we've learned along the way is that it's really hard to make this transition from three and four inch to six inch," he adds "But we have a lot of experience with this transition, and we've been very aggressive in implementing a VCSEL process on our six-inch GaAs facility."

What's more, Cheskis is also convinced that his company already achieves better process control in its 6-inch facility compared to a 3- or 4-inch fab.

"The same tools as the six inch toolset are used in eight and twelve inch facilities, so we've got a lot of advanced techniques that we can use to control the processes across the wafer," he says. "We've seen very good yields across the wafer for our process and we're getting these again and again."

And while Cheskis won't be drawn on actual yield or device performance figures, he adds: "Just about any VCSEL that can be made on GaAs is something that we have done here."

The right applications

So which mainstream application will VCSELs find first? Faster datacoms, gesture recognition in smartphones and heat sources in industrial processes are just a few of several up and coming applications that will demand the GaAs VCSEL.

Cheskis believes myriad opportunities are out there with VCSEL manufacturers already busy fulfilling orders for optical communications. He also reckons that if VCSELs fabricated on 6-inch wafers can hit a similar cost structure to LEDs, then a VCSEL's better performance will drive significant volumes for the technology in, for example, mobile applications.

However, he is also closely watching gesture recognition in mobile phones and reckons this high volume market will really fuel the move from 3- and 4-inch to 6-inch wafers for VCSELs.

"There are many millions of devices for a mobile application that will consume a lot of wafer realty, and I don't think there is enough capacity in the world with existing VCSEL manufacturers [to fulfil demand for mobile applications]," he says. "But because of the time and investment we've made so far, we're ahead of the game and this is an opportunity for us to capitalise on our core competencies in six inch manufacturing."

"We think VCSELs are going to be big and we're very excited about it," he adds.

Right: A technician tests six inch VCSELs at the Anadigics test facility in New Jersey.

Q&A

Tang Yong Aug

Vice President, Compound Semiconductors, Dow Corning

Q SiC devices have many great attributes, such as high efficiencies, high operating temperatures and the ability to handle high current densities. Why is it, then, that the penetration into a silicon-dominated market is not that fast?

A The SiC market has steadily grown over the years, but the biggest impediments to this growth are price and reliability. Only lately has the market started to get into MOSFETs, which are the transistors. I believe that this is the next phase of the growth of SiC: More people will get diodes and transistors in their modules, and you will see the price eroding to a price that is more competitive compared to a silicon counterpart.

Q One of the world's leading SiC substrates makers, Cree, is vertically integrated, and ships SiC devices and modules. Do you think that gives Cree an edge in today's industry?

A I believe that it gives them a big edge. That's not only in economies of scale – I also believe that they have the advantage of device knowledge, to validate the competitiveness as well as the differentiation of silicon carbide, which substrates makers like ourselves and a few of our other competitors may not have.

That is also one of the key reasons why Dow Corning, even though it has done fantastically in 2014, believes that the path going forward for SiC will be through partnership.

Q Dow Corning is looking for a partner to work with. Can you explain this vision, and why a partner is more than just a valued customer?

A The way we look at partnerships is firstly to increase the adoption of SiC in the market. We are definitely not looking for partners who are just start-up companies and who do not have the financial capability. We are looking for partners either to help us be more competitive and complement our skills and competencies in SiC; or we are looking at partnerships in the downstream supply chain who enhance the value of SiC at the product level.

Q SiC substrates have come a long way, and are no longer riddled with device-killing micro-pipe defects. So why would a device maker consider partnering with you, rather than just buying substrates off the shelf and producing devices in secret?

A I believe that a device maker or product maker who wants differentiation as well as more assurance of their supply chain would want more integration in order to ensure that they are well-positioned to supply a growing market for SiC devices.

Q So are you suggesting that there are concerns over SiC substrate shortages in the industry?

Yes, there are two concerns. One concern is in the 6-inch supply. As the market migrates from 4-inch to 6-inch supply to get cost and price competitiveness, I believe that there will be the need for more 6-inch supply in the market.

The second reason for vertical integration through a partnership is that the current supply from SiC vendors is not an ideal situation. We have in Cree a very big supplier of SiC, and the rest of the suppliers, including Dow Corning, are not as big. And because they are not as big, there are no economies of scale. People who want to really increase the adoption of SiC at the product level want some form of assurance of the supply chain.

Q Have you started talking to device makers about this partnering opportunity?

A We have been talking to various people, but I think it's early days.

Q What will happen if you don't get a partner, or you get two or three good offers?

I think a partnership can take many forms. It doesn't just have to be partnerships – it can even be licensing. Obviously, when it comes to licensing, we can have many partners. And a partnership can be in various forms, depending on what stage of the supply chain we are talking about. We could partner with the growers of a crystal, and we could partner in the production of epilayers for SiC. We will see what makes the most sense for Dow Corning, customers and the industry.

With regards to what happens if we don't find a partner, I seriously do not believe that there will be no partners. It's a matter of timing.

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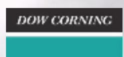

Optimising devices with wafer bonding

Wafer bonding forms high-performance devices with insulating and conducting interfaces

BY MARTIN EIBELHUBER, CHRISTOPH FLÖTGEN AND PAUL LINDNER FROM EV GROUP

STACKING different semiconductor materials together is one way to build better devices. This form of integration can be applied to solar cells, biosensing and RF chips, power and photonic devices, and it can lead to increases in efficiency and reliability while trimming size, weight and cost. The phrase 'more than Moore' has been coined for such improvements, because they are not directly related to lithographic scaling and they can unleash an ever-increasing array of electronic devices.

Heterogeneous integration can take many forms, including the marriage of mature silicon technology with compound semiconductors sporting superior properties. Significant performance increases can result, alongside novel capabilities at comparatively low costs. Note, however, that this demand for integration is not limited to CMOS wafers, and it can be applied to any form of technically or economically preferred substrate.

Growth of III-Vs on silicon is a common approach for material integration. Much progress has been made in this area, but there are still several weaknesses associated with this technology: there is a high defect density at the growth interface; deposition rates for compound semiconductors are not that fast; and epitaxial equipment is an expensive purchase.

An alternative approach that addresses these concerns is plasma-activated direct bonding of different materials. Compared to epitaxial growth, this technology offers greater freedom for device design and process implementation, and its widespread use in recent times has demonstrated that most compound semiconductors can be directly bonded on different substrates.

A key part of this bonding process is the plasma activation of the surface, which allows lower annealing temperatures that minimize material damage. Normally this process employs a SiO_2 bond interface. This can be as thin as the native oxide and may benefit the device, by cutting leakage currents or cross talk to the substrate. However, if the device operates with vertical current flow – as is the case for multi-junction solar cells and some classes of power device – the interface needs to be electrically conductive.

At EV Group of St. Florian, Austria, we have developed a technology called ComBond that is able to realize a covalent, oxide-free bond interface with ohmic behavior.

Beside thermal expansion matching and the demand for low temperature, wafer size and die differences need to be handled effectively for heterogeneous integration. One downside of wafer-to-wafer bonding is that the pitch and placement of the die on each wafer must match up with one another – and even if this is done perfectly, every time, material is still wasted when one type of die is much smaller than the other. Wafer-level die transfer abolishes this geometry matching, thereby trimming material consumption while delivering high yield and throughput, by combining fast distribution of the dies and collective die transfer using wafer level fusion handling.

The remainder of this article covers in more detail the key aspects of all the wafer bonding processes outlined above. Read on to discover the techniques needed to realize a good bond, how to form an electrically conductive bond interface, and how die can be transferred at the wafer level.

Direct bonding

One of the most common integration processes involves the forming of a silicon-on-insulator heterogeneous stack via fusion wafer bonding. Note, however, that this established, high-volume production process is not limited to this material combination, and can be used to form a wide variety of engineered substrates (see table 1 for a list of materials).

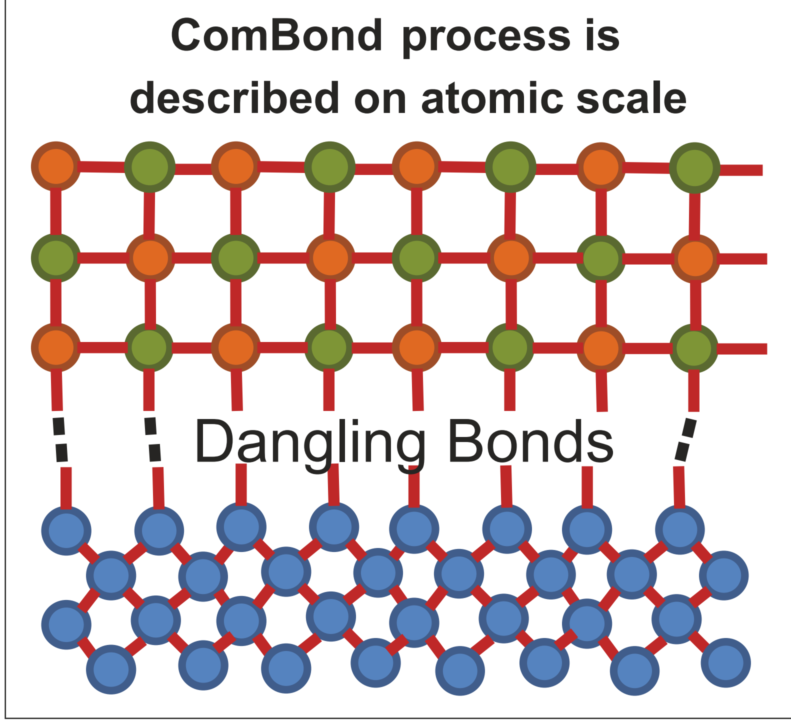

Figure 1: The ComBond process creates open bonds, which are also known as dangling bonds, on the semiconductor crystal surface. These bonds hold the key to wafer bonding of different materials covalently without an intermediate layer.

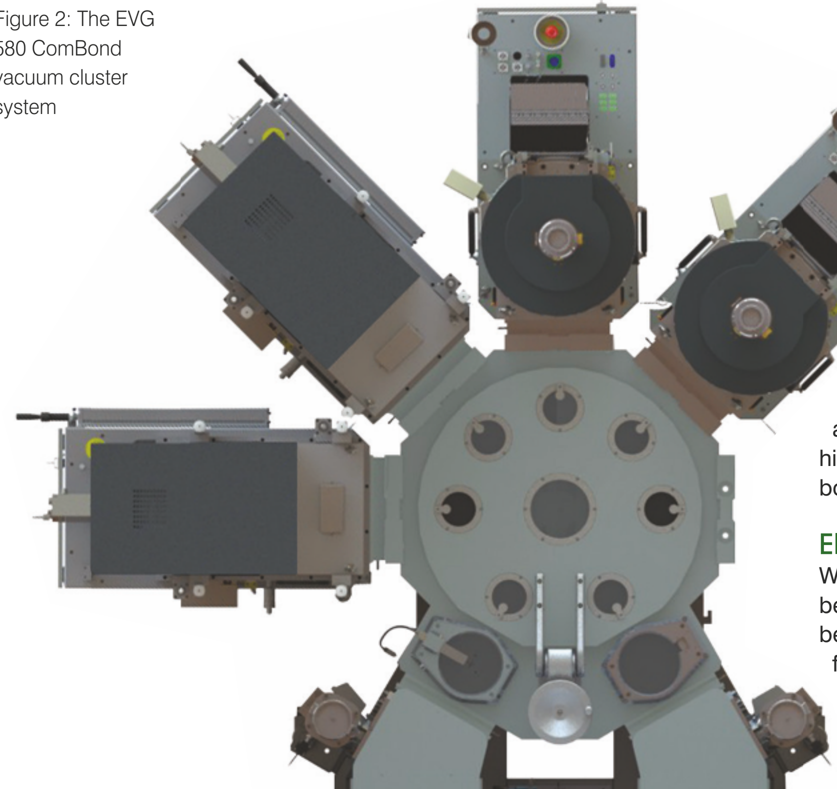

Figure 2: The EVG 580 ComBond vacuum cluster system

A key step in the bonding of compound semiconductor materials is the activation of the surface of the wafer by plasma treatment. Initial bonding takes place at room temperature, but strengthening of the bond interface requires a subsequent annealing step. Without activating the wafer surface, this takes place at around 900°C, a temperature not suitable for materials with different thermal expansion coefficients. Heterogeneous material integration falls into this category, so such high temperatures are ruled out, because the thermally induced stress would cause wafers to markedly bow, warp and even crack.

By avoiding any high temperature steps, our plasma-activated fusion wafer bonding process does not suffer a similar fate. With this approach, there is oxidation within the interface, and this allows high bond strengths with annealing at 300°C. At this much lower temperature, most material combinations do not get close to critical stress, and this allows almost any compound to be integrated on alternative substrates.

When performing this procedure, it is essential to use clean, flat wafers to realize a high-quality bond. If any particle inhibits the contact of the surfaces, voids will be present between them; and for fusion bonding to succeed, the roughness of the surface must be better than 1 nm.

The good news is that it is not that challenging to meet this pair of criteria. If wafers are too rough, they can be smoothed sufficiently with today's chemical mechanical planarization equipment. And if the interface is on SiO_2, a known CMOS-compatible material, oxide deposition and chemical mechanical polishing can be performed on practically all wafers. The bonding interface places no restrictions on further downstream processing, because additional processing steps can take place in a high vacuum or at temperatures higher than the bonding or annealing temperature.

Electrically conductive interfaces

When the interface between the wafers has to be electrically conductive, surface oxides must be removed. This is not the only requirement for the surface treatment process, however: There should also be no damage added to the underlying bulk structure. If treatment were to introduce lattice point defects, such as interstitials and dislocations, this would provide traps for charge carriers that would impair final device performance.

One option for producing oxide-free bond interfaces is to treat the wafers with hydrogen fluoride prior to bonding. However, hydrogen fluoride must be handled with great care, and disposing of the chemical is not trivial. What's more, a terminating hydrogen-layer forms on the wafer during its chemical bath, and removal of this monolayer requires a bake-out at 600 °C. Adding to the complexity of this approach, there is the need to avoid regrowth of surface oxides during handling and storage, both after the wet etch and during bake-out. Lastly, there is complexity associated with the chemical etching, which stems from different substrates and the integration with different compounds.

Our approach is much simpler to perform, using our ComBond technology to remove an undesired oxide layer with a dry process based on energized particles. It differs from the fusion bonding process that closes nanogaps via oxidation, with surface treatment taking place on an atomic scale to produce dangling bonds, the pre-requisite for the forming of covalent bonds at room temperature (see Figure 1).

The tool that we have built for this task is the ComBond Activation Module. It is ideal for wafer bonding, because it delivers effective oxide removal while simultaneously minimizing damage to the underlying substrate. Wafers are

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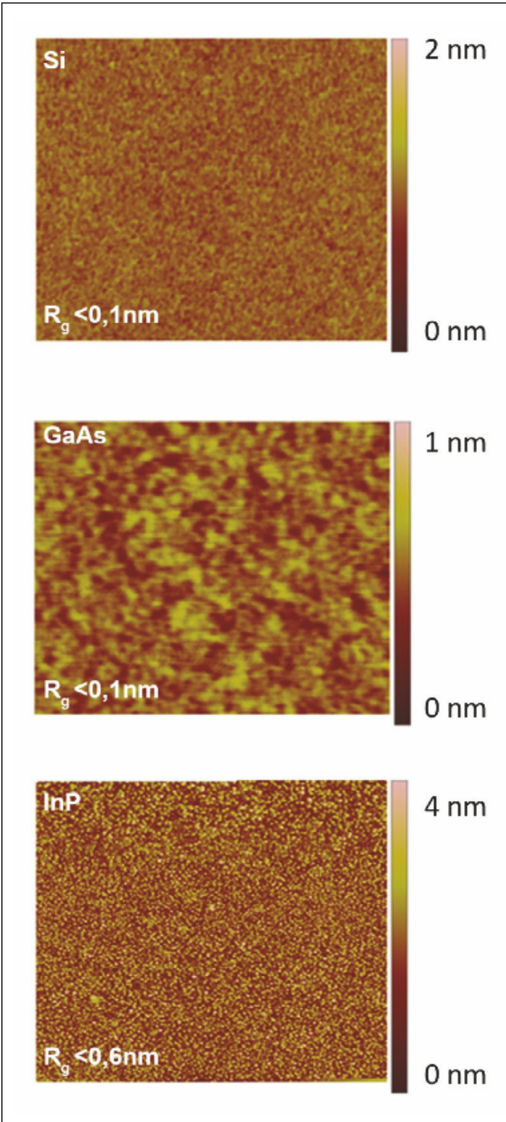

Figure 3: Atomic force microscopy images over a 2 μm by 2 μm area demonstrate that the ComBond Activation Module can produce surfaces after oxide removal that are smooth enough for bonding. To meet this requirement, the quadratic mean micro-roughness has to be significantly below 1 nm.

kept in a high-vacuum environment after surface treatment to prevent the re-oxidization of their first monolayer while undergoing further processing in the bonding cluster system (see Figure 2). With surface preparation only taking a few minutes for each wafer, re-oxidation can be prevented for several substrates and activation conditions.

All direct wafer-bonding processes require low surface roughness to ensure a uniform contact at the nano-scale. To demonstrate the high-quality of the surface treatment associated with our ComBond Activation Module, we have performed experiments on a range of materials. Scrutinizing surfaces with an atomic force microscope reveals that treatment with our tool does not roughen the surface, and might actually make it slightly smoother (see Figure 3). With a typical quadratic mean micro-roughness of less than 0.6 nm after oxide removal, these wafers exhibit excellent surface conditions for forming heterogeneous structures of the highest crystal quality.

Another virtue of our ComBond process is that it does not leave detectable residual oxides at the bond interface. Energy-dispersive X-ray spectroscopy performed on SEMI-standard silicon wafers that were bonded using the ComBond process failed to pick up any sign of oxygen at the bond interface.

Bonding of GaAs and InP wafers is a key step in the fabrication of very high efficiency solar cells with four or more junctions. We have studied this, covalently bonding GaAs to InP and inspecting the interface with a high-resolution tunneling electron microscope. Images indicate efficient removal of all the oxide and the creation of an incredibly thin amorphous layer – it has a thickness of less than 2 nm. This high-quality, electrically conductive interface is excellent at supporting vertical current flow, because it is not plagued with crystal distortions and trap states. The performance of multi-junction solar cells is enhanced by such a structure, which does not require a thick epitaxial buffer layer between the stacks and benefits from an optically transparent interface.

Multi-junction solar cells are not the only devices that benefit from a high-quality bond with a very thin amorphous layer – they aid any device that needs great electrical performance in the vertical

Table 1: Many compound semiconductor materials can be bonded by low-temperature plasma-activated wafer bonding and can be found in production today.

First Wafer	Second Wafer
Substrate with SiO_2 top layer (can be as thin as the native Oxide only)	Sapphire
	Ge
	SiGe
	InP
	GaAs
	SiC
	$LiNbO_3$
	$LiTaO_3$
	Si_3N_4

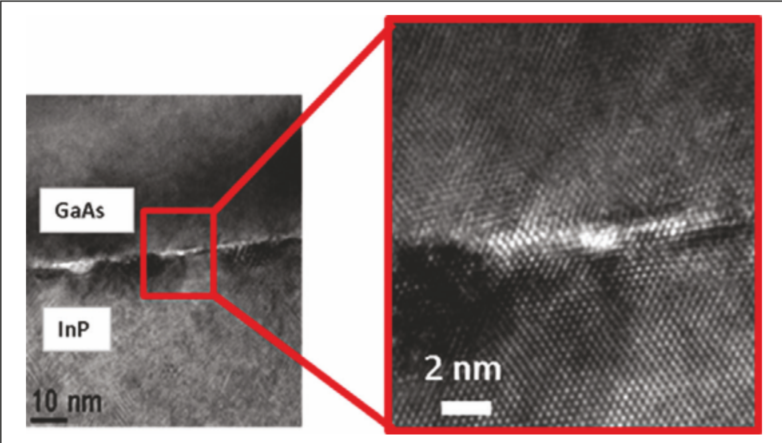

Figure 4: Transmission electron microscopy reveals that a GaAs/InP oxide-free, covalent-bonded interface has a thickness of less than 2 nm, and that the quality of the underlying crystal is not affected by the bonding process.

direction. Power devices fall into this category: bonding SiC epistructures to polycrystalline SiC can slash wafer costs and spur the penetration of these devices into a broader range of applications; and a similar scenario could occur with vertical power devices made from GaN, which are very promising, due to high electron mobilities and breakthrough voltages.

Transferring die

One downside of wafer-to-wafer bonding is that it can produce a significant loss of real estate. In some photonic applications, for example, there is a low fill factor for the target wafer that is equipped with electro-optical elements. On the other hand, the wafer sizes in CMOS technology are generally not the same as those used in the compound semiconductor industry.

Figure 5: Several types of non-uniformities have to be considered for a high-yielding, wafer-level die transfer process: (a) bow or warpage, (b) unevenness of the substrates, (c) die height variation. These issues can be overcome by applying uniform force on the backside of the die using an efficient, compliant layer while bonding.

It is important to also note that there several key advantages with wafer-to-wafer bonding, such as collective pre-processing of the dies and high bonding throughput, which are strengths that are impossible to provide with die-to-die bonding.

Fortunately, it is possible to combine the best of both worlds by employing fast distribution of known good die, using high-quality direct bonding at the wafer level. This approach reduces the sensitivity to thermally induced stress and decouples the yields to the two processes, so long as known good die are only placed on known good sites on the wafer. Tuning the bonding conditions is relatively easy, because collective bonding is possible at elevated temperatures, even in vacuum conditions.

For a wafer-level die transfer process to be successful, it is essential to apply an appropriate, uniform pressure to every single die. This is not easy, due to factors such as bow and warp of wafers, uneven substrates and differences in die height (see Figure 5). Introducing a compliant layer addresses all these challenges by enabling the application of similar force on different die, thus providing optimal transfer rates and high bonding yield.

Thanks to this process, heterogeneous integration can be scaled up to larger substrates and multiple functions can be added to the device wafer, even in volume production. This process – and that involving wafer-to-wafer bonding – will help to drive a new era for innovative device structures with novel functionalities and increased performance.

ComBond results were created with support from Dr. Dimroth at Fraunhofer ISE. EVG and his team are partnering for the development of highly efficient multi-junction solar cells.

Further reading

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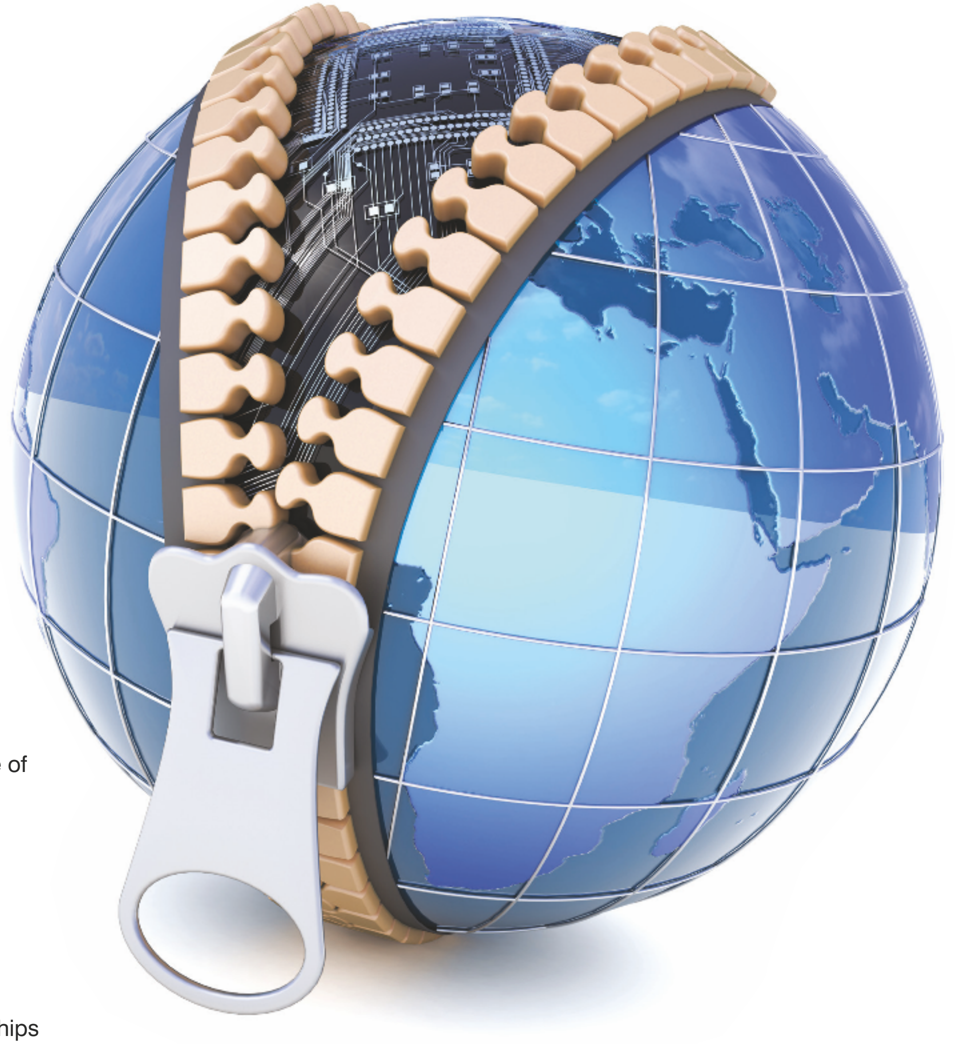
MOSFETs made from SiC can plummet in price when the cubic form of this material is grown on large silicon substrates

BY PETER WARD FROM ANVIL SEMICONDUCTORS

TO CURB carbon emissions, much effort is being directed at improving electrical efficiency. One area that is central to cutting losses is the generation, transmission and consumption of electrical power, whether it originates from the burning of fossil fuels, the rotation of blades on wind turbines, or the absorption of sunlight by solar panels. It is estimated that energy losses of up to 10 percent can be attributed to power conditioning, which takes place during electrical generation, transmi ssion and consumption and can involve the ramping up or down of voltages and the switching of current between AC and DC forms.

On top of this, there are further prospects for electrical energy savings. One area is transportation, which is witnessing growth in sales of electric and hybrid electric vehicles and the construction of more electric aircraft; and there are also opportunities in the home, where greater electrical efficiency will help to drive the uptake of alternatives to fossil fuels for heating.

It is well known within the compound semiconductor community that replacing silicon devices with those made from wide bandgap materials can deliver a tremendous hike in the efficiency associated with power conditioning. That's partly because chips built from the likes of GaN and SiC have low resistive losses, which stems from their high critical electric fields; and it is



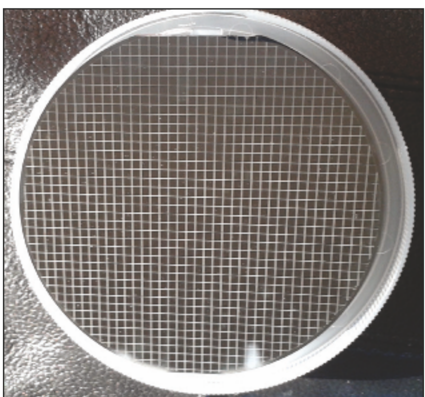
also because these devices are capable of high switching speeds. An example of the superiority of wide bandgap devices over those made from silicon comes from the Arkansas-based firm APEI, which has developed an award-winning electric-vehicle battery charger based on SiC. This product highlights how wide bandgap devices can enable more efficient, smaller and cheaper systems, mostly in the consumer area using transistors capable of handling between 600 V and 1200 V.

Cost and performance

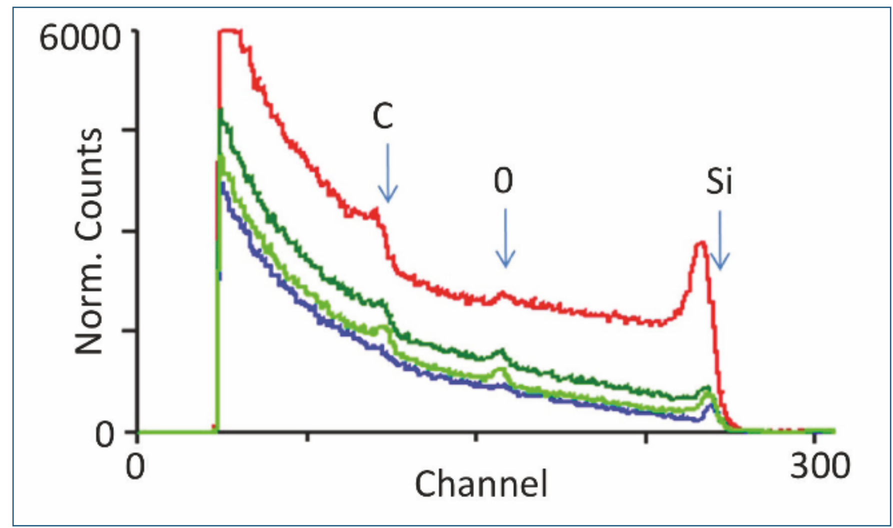
Today, the leading commercial wide bandgap technology for power electronics is based on the growth of epitaxial SiC on a native substrate – the 4H poly-type of SiC. Devices formed from this homo-epitaxial growth step can address a very wide range of applications up to 10 kV, but each area has very different requirements, in terms of performance, cost and the size of the market.

Although the sales of SiC devices are rising, silicon chips still dominate the power semiconductor market. One reason for this is that the SiC devices operating at 600 V and 1200 V, which could serve consumer applications, are seen as too expensive by many potential buyers, who are also concerned with the lack of compatible second sources. This is clearly not an issue when purchasing a silicon component.

There are two factors behind the relatively high cost of the 4H-SiC power device: 100 mm and 150 mm 4H-SiC substrates are very expensive, because growth of the crystal boules is a tremendously energy-intensive process;



Anvil's polycrystalline SiC grid holds the key to the production of MOSFETs on large 3C-SiC wafers



Rutherford Backscattering Spectroscopy is a method of assessing the defect density of a crystal by applying a beam of high-energy ions and measuring the energy of those ions which are reflected (Backscattered) by the crystal. The more perfect a crystal is, the more it absorbs the ions – defects in the crystal reflect the incident ions. In this case the Blue curve shows the backscattering from our native 3C-SiC crystal, which is dramatically increased by the defects introduced by Al ion implantation (Red curve). However after annealing at 1250°C (dark Green) or 1350°C (light Green) the RBS data suggests the defectivity has returned to the unimplanted state. This simple process is totally ineffective in 4H-SiC and demonstrates a major advantage of 3C-SiC over 4H-SiC.

and device processing is costly and complex, due to the hexagonal form of SiC. The good news is that it doesn't have to be this way, because there is a low-cost alternative, the 3C poly-type of SiC. Reports of this form of SiC started emerging in the 1990s, with the Japanese firm Hoya leading the way as it strived for lower costs by developing a growth technique to create low-defect-density SiC-on-silicon substrates.

However, this is increasingly difficult with larger wafers, such as those with diameters of 100 mm or more. A high degree of tensile stress occurs at the interface between silicon and SiC, due to a combination of the crystal lattice mismatch between this pair of materials, and the higher coefficient of thermal expansion for SiC compared to silicon.

This issue did not stop researchers from Hoya demonstrating the promise of the SiC MOSFET, by fabricating devices with an excellent set of characteristics, which were formed via growth of 3C SiC on small silicon substrates. In this study, reported in 2002, engineers showed that this form of device can slash on-resistance under the gate, even compared to the best 4H-SiC MOSFETs of today.

Early progress by Hoya amounted to nothing, however. This Japanese firm was unable to produce larger wafers, and this lack of success led to closure of activity in this area. But our team at Anvil Semiconductors – a start-up based in the UK cities of Coventry and Cambridge – has shown that there is a great future for this class of device, because it is possible to address the stress at the interface between silicon and the 3C poly-type of SiC.

To unlock the commercial potential of this class of MOSFET, we have recently installed a production process for 100 mm wafers at Norstel AB. A key part of this process involves exploiting the normal scribe lane pattern that can divide active die on a wafer. Taking this approach minimises the dimensions across which stress is developed, and gives rise to an active stress relief structure.

This patented technology involves the forming of a SiO_2 grid in the scribe lanes prior to epitaxial growth. Any SiC that is then grown in these regions takes on the polycrystalline form of SiC. Typical grid pitches are 2.5 mm and 5 mm, and thanks to the high current densities that can be realised in SiC, a 10 A vertical device can be constructed from a 2.5 mm die. Electrical resistance at the Si/SiC interface in these devices is indiscernible, due to the combination of dopant up-diffusion from the n^+ silicon substrate

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and an added dopant at the interface; and growth of layers with thicknesses up to 12 μm are more than adequate for a 1200 V transistor. Note that one of the great merits of this stress relief technique is that it is, by design, independent of wafer diameter. This will allow us to scale our process to larger wafers, which could be produced on multi-wafer Aixtron reactors.

Bow profiles acquired at the end of our epitaxy process reveal that the central area of the wafer, which is defined as that spanning the range ±50 μm high, occupies more than 70 percent of the total wafer area. We have scrutinised these layers by a variety of common characterisation techniques, including AFM, TEM, SEM, XRD and cathodoluminescence, and shown that their quality is at least as high as that produced by Hoya's engineers. That's partly because some of the crystal defects seen by the team from Japan are avoided by working with a (100) off-axis silicon substrate that drives a step-flow epitaxial growth process.

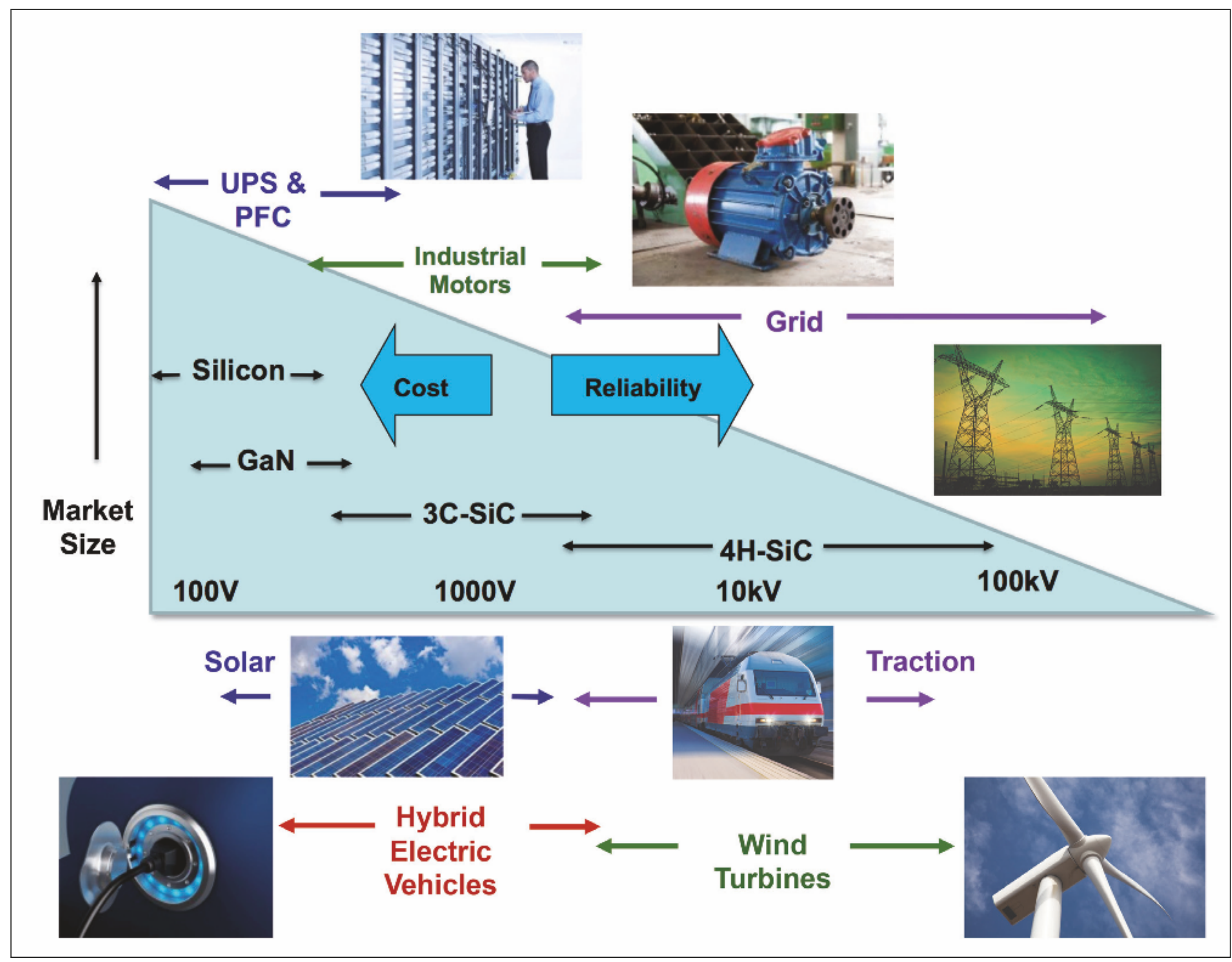
By employing all this know-how, we can produce SiC-on-silicon wafers with very low defect densities that can be processed into devices capable of handling current densities of at least 500A/cm^2. Although the growth process leads to steps that are typically 8 nm in height, chemical mechanical polishing can trim surface roughness to below 0.5 nm.

Similar to silicon

When it comes to post-growth processing, 3C-SiC has many advantages over the 4H poly-type. Switching from a hexagonal to a cubic crystal structure simplifies the introduction of dopants by ion implantation, because damage recovery of SiC is far easier to perform. What's more, implantation can be carried out at room temperature, avoiding the need for specialist high-temperature implant equipment and complex hard mask processing. Meanwhile, damage recovery only requires annealing at 1350°C, which in turn preserves the material surface.

It is also easier to put the finishing touches to SiC MOSFETs formed from the 3C poly-type, than it is to those based on the 4H form. Gate oxides grown on 3C-SiC do not suffer from an interface state problem that adds to the on-resistance of 4H-SiC transistors; and 3C-SiC is much more reactive to metals for the ohmic contact, so it is not necessary to use the extreme metal annealing temperatures required for 4H-SiC. The upshot of these advantages is that a 3C-SiC-on-silicon MOSFET process flow is very similar to that of a silicon DMOS device, making it possible to manufacture this wide bandgap transistor on a standard silicon MOSFET line with the sole addition of a high-temperature annealing furnace.

If devices are made in this manner in high volumes, the cost for making a



The primary opportunity for 3C-SiC devices in the power semiconductor market

650 V, 3C-SiC-on-silicon DMOS power transistor should be very similar to that for producing a superjunction silicon MOSFET.

The 3C form of SiC also trumps its 4H cousin when it comes to packaging and hybrid assembly. It is tricky to interface the back of a 4H-SiC die with a package or hybrid board because a typical back metallisation is a type of nickel silicide, rather than mainstream assembly metallurgy. Making matters worse, this back contact demands high-temperature processing, so it must be formed at the appropriate point during front-of-wafer processing. In sharp contrast, the back of our wafers are made from silicon, so we can use any conventional die attach technique. This enables us to thin a 100 mm wafer to 100 µm, and then employ a standard gold eutectic process.

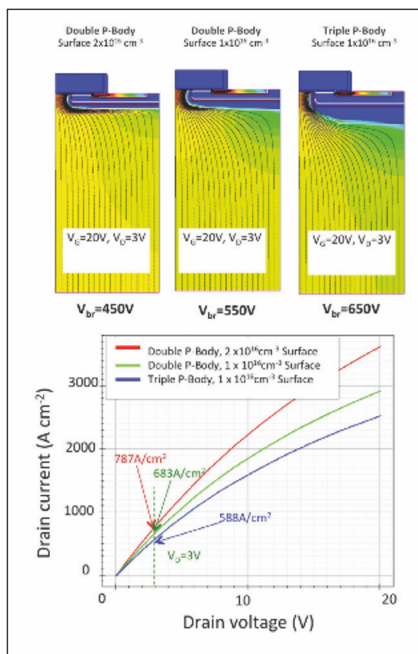


Figure 1. The fundamental compromise in MOSFET design is between on-state conduction and off-state blocking voltage. The on-state conduction is essentially set by the JFET structure formed by the edge of the P-Body and the n-epitaxy, while the blocking voltage is determined by the electric field intensification at that same edge of the P-Body. As these two effects operate against each other a compromise is required. This simulation, optimised for a 650V device, shows three different P-Body structures and a current carrying capability of the device of 588 A/cm^{-2}. This demonstrates the high current capability of this technology, for example a 10A MOSFET would only require a die of say 4 mm^2, taking account of the additional area for contacts etc.

Multi Die Test Assembly (left) and wafer on UV tape after die type selection (right)

Our prototype Schottky barrier diodes exhibit excellent material quality and verify the technology and processing steps. These devices produce ideal characteristics, are free from SiC-silicon interface effects and have good crystal quality, resulting in extremely high yield.

The next steps for us include realising further process improvements, leading to the fabrication of Schottky barrier diodes for sampling. In addition, we aim to qualify high-quality MOS gate oxides and develop the MOSFET process and device design. The latter activity involves extensive device simulation using the best numerical models (an example is shown in Figure 1, which suggests that superior channel mobility in 3C-SiC results in roughly half the on-resistance of a 4H-SiC equivalent).

Why not GaN?

As stated before, we are targeting the 650 V to 1200 V device sector with designs that should be very cost competitive. Such products would appear to be competing with those that are emerging sporting another promising technology, GaN-on-silicon. There is an abundance of MOCVD reactors capable of GaN epitaxy, and there is a considerable worldwide development effort underway in GaN HEMTs.

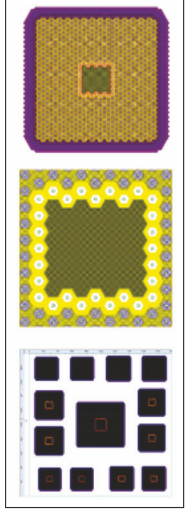
While a complete discussion of the merits of SiC-on-silicon over GaN-on-silicon is outside the scope of this article, it is worth pointing out some of the shortcomings of the latter technology. First, some very advanced technology steps have been required to turn the normally on HEMT into a MOS-like enhancement mode GaN device. However, have these new elements that have been introduced to switch off the HEMT created a truly a normally off device that can be applied in safety critical systems?

Adding to the concerns, it seems that the GaN HEMT will remain a lateral device for the foreseeable future, albeit perhaps one featuring a through-substrate via to bring the drain to the back of the device. This architecture leads to a much lower power density than a vertical device, with typical published layouts essentially incompatible with conventional packages or hybrids. In short, applying this very interesting technology in the power arena is going to be far from trivial.

Based on this reasoning, we see the future market segmentation of wide bandgap devices like this: GaN-on-silicon will certainly find applications in the 100 V to roughly 400 V segment, 3C-SiC-on-silicon should occupy the 600 V to 1200 V ground, and above 1200 V is the territory of 4H-SiC. To convince the power electronics sector of this, we plan to supply prototype Schottky barrier diodes to selected customers in the current quarter, and follow this up with prototype MOSFETs in the third quarter of this year.

Further reading

Wan et al, IEEE Electron Device Letters **23** 482 August 2002.



MOSFET Test Arrays, a hexagonal MOS cell with a central gate contact, a conventional Si-like layout enabled by the 3C-SiC processing advantages

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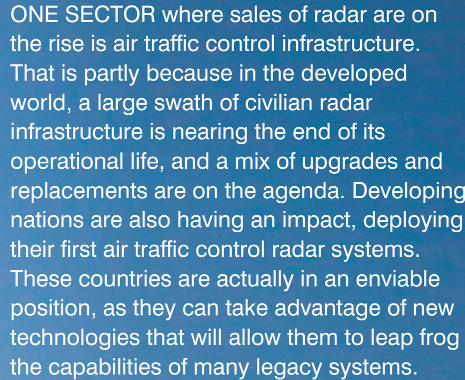
GaN gives power and flexibility to L-band radar

Increased efficiencies, superior power-handling capabilities and higher breakdown voltages give GaN the upper hand over silicon LDMOS in L-band radar

BY DOUG CARLSON AND ERIC HOKENSON FROM MACOM



ONE SECTOR where sales of radar are on the rise is air traffic control infrastructure. That is partly because in the developed world, a large swath of civilian radar infrastructure is nearing the end of its operational life, and a mix of upgrades and replacements are on the agenda. Developing nations are also having an impact, deploying their first air traffic control radar systems. These countries are actually in an enviable position, as they can take advantage of new technologies that will allow them to leap frog the capabilities of many legacy systems.

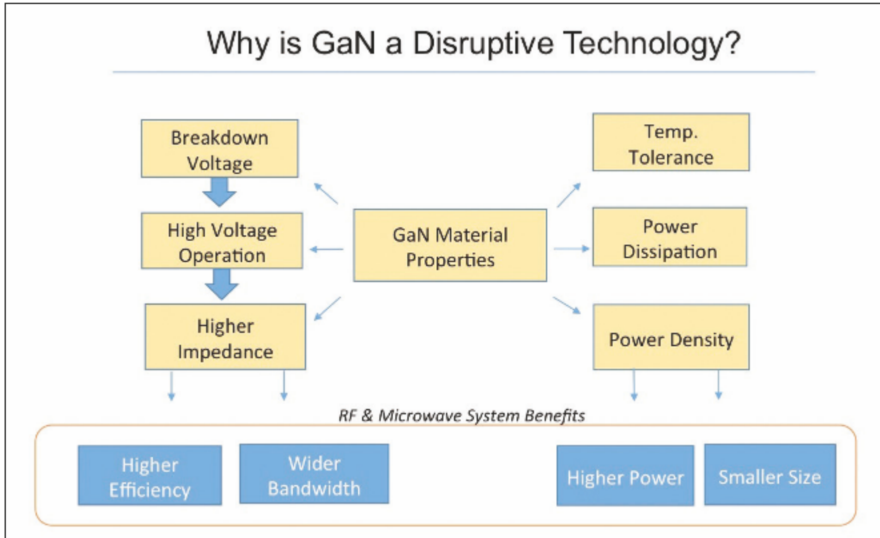
Increasing shipments of these air traffic control radar systems is spurring intensified research and development in the RF and microwave domain, with emphasis on improved performance in the L-band. Radar systems operating in this domain span 1.2 GHz to 1.4 GHz, a range of frequencies that are less prone to atmospheric interference. This asset makes L-band radar ideal for long-range monitoring and volume search capabilities that enable air traffic control stations to detect incoming and outgoing aircraft over vast distances. Augmenting this are S-band and X-band radar systems that cannot probe as far, but provide superior short-range resolution.

The growth of GaN

L-Band radar systems can require thousands of watts of pulsed power, so it is naturally advantageous to employ high-power RF transistors. Armed with high-power discrete transistor 'building blocks', designers of radar systems have the flexibility to architect multi-kilowatt products with fewer components. This simplifies the design of the system, and cuts its manufacturing cost and complexity.

Various semiconductor materials can be used to construct RF power transistors. The most promising of late is GaN, which is enabling designers of L-band radar systems to realise breakthroughs in power output capability, temperature tolerance and efficiency.

One of the great merits of GaN is that it offers an eight-fold hike in raw power density over the incumbent silicon LDMOS technology. Thanks to this, it is possible to slash RF component size, thereby allowing designers to harness higher power in smaller



enclosures. This is simplifying the development of RF transmitters capable of scaling to 10 kWs and beyond, while maintaining or trimming the system footprint.

These improvements in chip performance lead to gains in the capability of the system. By utilising the high output power enabled by GaN-based RF components, it is possible to extend the surveillance range for L-band radar systems while simultaneously boosting target resolution, leading to better aircraft detection and identification.

Another strength of GaN over silicon is its higher breakdown voltage. This unlocks the door to higher operational voltages and ultimately increased efficiency, in both the device and in the overall power supply of the radar system. Note that these gains in efficiency are far from trivial: Compared to LDMOS technology, GaN delivers an improvement in efficiency ranging from more than 40 percent to 70 percent, depending on operating frequency. This trims the running cost of the system, which is anticipated to be in service for 20-30 years. In addition to the higher efficiency, the high voltage thresholds of GaN-based RF power components allow for increased wideband impedance matching, enabling an L-Band radar system to sustain high performance across the full frequency band.

Turning to GaN for constructing the transistor also leads to greater flexibility over the shaping of the RF signal pulses.

Compared to silicon RF transistors, those based on GaN can produce far longer radar pulses – and this ensures the focusing of more energy on a target for improved resolution. While a conventional transmitter for L-band air traffic control radar will emit pulses in the range of 100 microseconds, that based on GaN can have a duration of thousands of microseconds.

Increased flexibility of pulse characteristics is another benefit of GaN. Being able to control pulse length and duty cycle is highly desirable, because it unleashes an opportunity to vary the levels of energy of the radar system, leading to improved detection of a wider array of target objects. Equipped with this capability, civilian air traffic control radar can also serve homeland security applications: Being able to distinguish between a commercial aircraft, an unmanned aerial vehicle and other airborne objects entering the airspace enables increased airspace awareness and enhances threat detection.

Thanks to all the merits of GaN that have been outlined above, this wideband semiconductor is enabling the launch of a new generation of more agile L-band radar systems that are optimised to meet the increasingly demanding performance and multifunction flexibility requirements of modern air traffic control facilities.

At MACOM of Lowell, MA, we are helping to drive this revolution in L-band radar by bringing to market a transistor with a record-breaking peak power output of 650 W. This forms part of our portfolio of GaN-on-SiC components that are offered as transistors and pallets and utilise a 0.5 μm HEMT process. This manufacturing technology yields devices with excellent RF performance with respect to power, gain, gain flatness, efficiency and load mismatch tolerance over wide operating bandwidths.

We use SiC as the foundation for high-power GaN transistors because this substrate has superior thermal properties, making it ideally suited for applications requiring high power densities.

We are not the only manufacturer of GaN-on-SiC power devices, and efforts by several vendors have showcased the capability of this class of wide bandgap chip, particularly in the electronic warfare domain. In our view, the great performance on GaN-on-SiC makes it the clear leader for performance-driven applications.

Our record-breaking transistor is a relatively new member of our family of GaN-on-SiC transistors for L-band pulsed radar applications, adding to a line-up of products delivering 125 W, 250 W and 500 W of peak RF power. We have hit 650 W by assembling a higher number of GaN transistor and silicon capacitor chips into a single package using a eutectic die attach process. Gold wire connects input resonance networks, as well as the gate, source and drain wires; and 'jumper' wires provide parallel connections to the multiple GaN and capacitor chips.

With this approach, we have been able to take an industry-standard ceramic package and fill it almost completely with GaN transistor dies, assembling a large number of cells that deliver considerably higher power than their legacy LDMOS-based cousins. This type of transistor benefits from the higher thermal conductivity of the SiC substrate that is very effective at transferring heat laterally and vertically, and ultimately allowing the component to dissipate more power.

Highlights of our GaN-on-SiC L-band radar transistor include a guaranteed

Left: MACOM's 650 W GaN L-band radar transistor in industry standard ceramic flanged package

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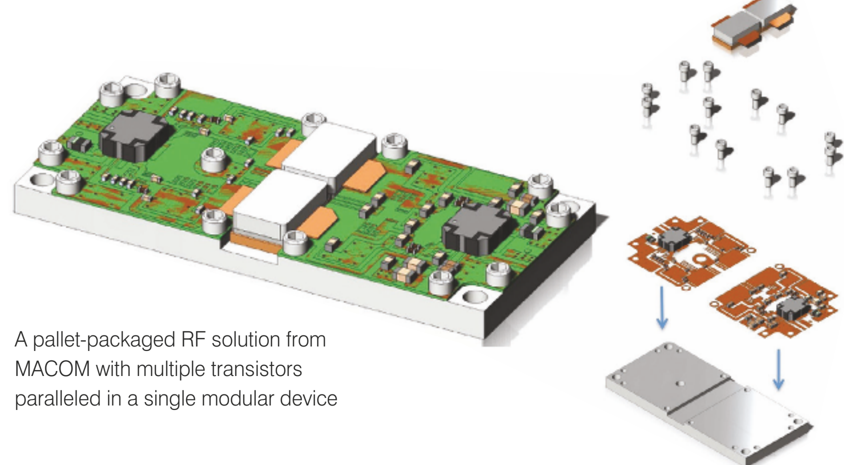
peak power of 650 W, a typical gain of 19.5 dB, and 60 percent drain efficiency. The device also boasts a very high breakdown voltage, allowing customers reliable and stable operation at 50 V under load mismatch conditions that are more extreme than those possible with older semiconductor technologies.

One of the benefits of high gain is a reduction in the driver requirements of the final stage. This leads to a further reduction in the number of components and a decrease in the power required to realise the desired performance.



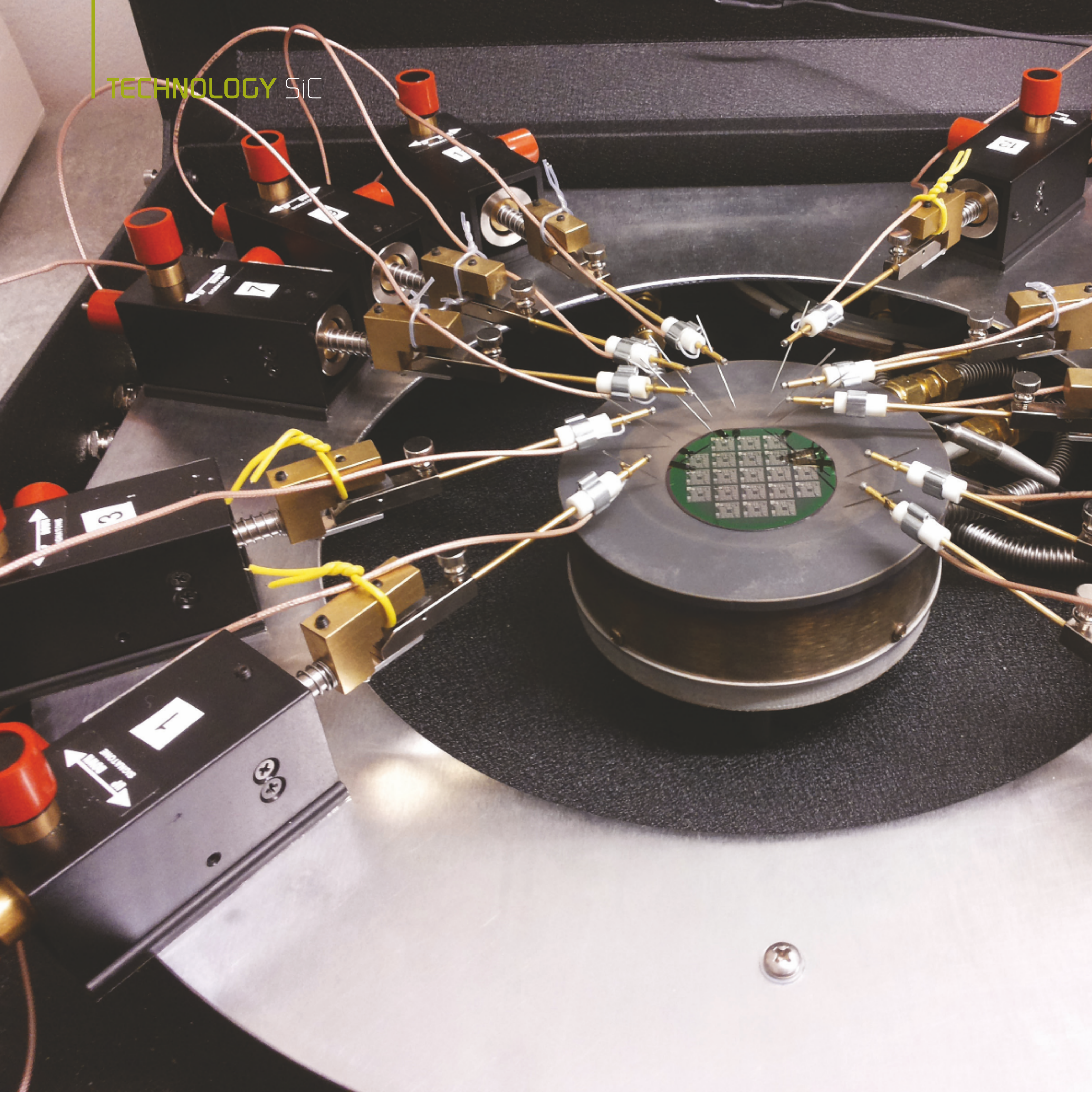
A pallet-packaged RF solution from MACOM with multiple transistors paralleled in a single modular device

Meanwhile, thanks to the high efficiency, overall power consumption is reduced, while the higher operating voltage and greater voltage standing wave ratio (VSWR) tolerance increase system efficiencies through bias advantages at higher voltage. Note that there is no significant risk of damage when operating this device in that regime, due to the higher breakdown voltage of GaN.

To ensure reliability under demanding operating conditions, we have subjected our device to rigorous testing. Based on raw RF data amassed via testing for full-lifetime operating conditions, this package demonstrates a mean-time-to-failure of 5.3 x 10^6 hours for junction temperatures of up to 200 °C.

Our launching of our 650 W GaN-on-SiC L-band radar transistor has set the stage for development of multi-kilowatt, pallet-packaged RF components designed with multiple transistors paralleled in a single modular device. We are taking an active role in this quest, having prototyped and tested a 2 kW, L-band power amplifier design that integrates four high-power GaN transistors.

Equipping system designers with high-power, GaN-based pallets will aid them in their building of next generation L-band radar systems that are based on modular RF building blocks that can easily scale to 10 kW and beyond with minimal design and manufacturing complexity. GaN-based RF power components are surely set to continue, and this will undoubtedly help to drive deployment of L-band air traffic control radar systems that defy the power, efficiency and operational agility limitations imposed by conventional RF components.



Turning to history for high-temperature integrated circuits

The bipolar junction transistor, a building block of integrated circuits of the 1960s, is given a new of life in SiC circuits operating at 600°C

BY CARL-MIKAEL ZETTERLING AND LUIGIA LANNI FROM KTH ROYAL INSTITUTE OF TECHNOLOGY, SWEDEN

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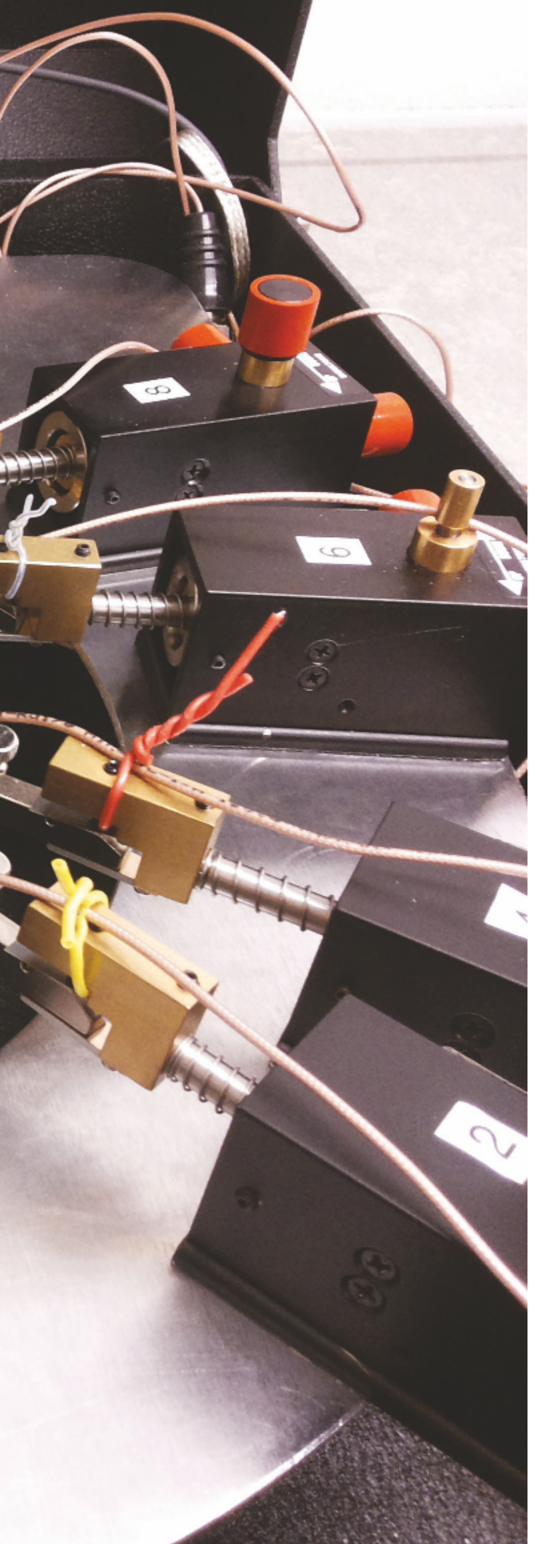


Left: Electrical characterisation is performed on-wafer in a probe station with tungsten needle probes. The stage can be heated to 600°C, but then the microscope must be moved away immediately after probing to prevent excessive heat from damaging the optics

It's not easy designing electronic components and circuits. There are many requirements that must be fulfilled, including those related to cost, reliability, and thermal management. And the latter of these is by no means the least important, because if a chip gets too hot it will fail.

Imagine for a moment, however, that you rarely had to worry about overheating, thanks to electronics that could operate at really high temperatures, such as those up to 600°C. Armed with this, what would you build?

One obvious area for the deployment of such devices is the monitoring of high-temperature processes taking place in gas turbines, jet engines and combustion chambers, including those used for waste burning.

Although many of today's gas and temperature sensors are capable of handling these temperatures, signals are often too weak, so if an amplifier could be placed right at the source it would deliver a tremendous boost to the signal-to-noise ratio.

There are also applications where silicon ICs are currently operating at their very limit, and an alternative circuit made of a different material and capable of higher operating temperatures would be highly valued. That is the case for oil, gas and geothermal drilling operations, which currently rely on commercial, high-temperature silicon-on-insulator (SOI) circuits recommended for use up to 225°C. When deployed in these applications, premature failures are very costly – and a rule of thumb says that an extension of temperature by only 10°C halves the mean-time-to-failure.

What's needed is a semiconductor material that is capable of forming circuits operating at much higher temperatures. There are several candidates for this, but the most promising by far is SiC. Great strides have already been made with this wide bandgap semiconductor: It has led to commercial discrete devices capable of handling 1700 V or more, and research has shown operation at up to 600°C. However, more work is needed to improve this technology, including the development of ICs, capacitors and packaging that can operate at extreme temperatures.

Driving efforts in this direction is our team at KTH Royal Institute of Technology, which is based in Stockholm, Sweden. We have developed a variety of analogue and digital circuits that can operate at very high temperatures.

We are by no means the first research team that has turned to SiC to realise circuits capable of operating at extreme temperatures. One of the pioneers of this field is a group at NASA, which demonstrated SiC integrated JFET circuits of low complexity more than 20 years ago. Although this class of transistor can operate over an extended temperature range, it is tricky using it as the building block for designing ICs, due to a combination of difficulties associated with threshold voltage matching, variations in threshold voltage over temperature and a limited selection of circuit topologies.

Another trailblazer of SiC circuits is James Cooper from Purdue University. He leads a group that in 1993 demonstrated SiC NMOS and CMOS ICs that could operate at 300°C.

Following these efforts, the operating temperature of SiC ICs has climbed over the intervening years. In 2014 MOSFET technology enabled the construction of circuits operating at 500°C, showing the capability of NMOS and CMOS ICs. And as is the case for silicon and SOI, it is the gate dielectric, rather than the semiconductor material itself, that limits reliability.

High gate fields of 3 MV/cm or more are needed to extract sufficient current from the SiC MOSFETs, and this exerts more strain on the device, accelerating failure.

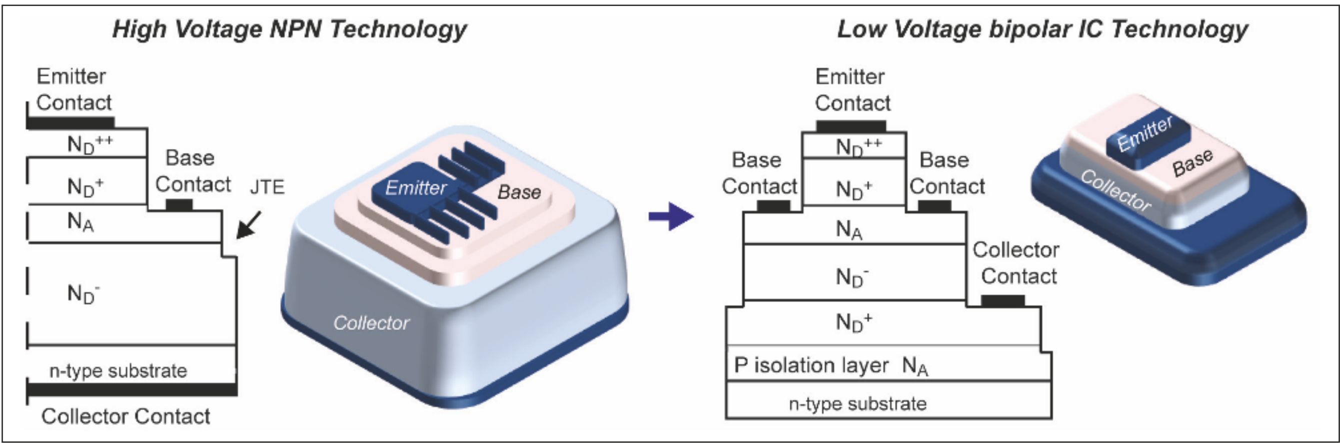


Figure 1. Cross-sections of the original high-voltage BJT and its development to a low-voltage IC technology. Physical device simulation is used to design the thickness and doping concentration of the regions. No ion implantation was used, so BJTs are etched from a SiC wafer with several epitaxially grown layers with different doping. Note that dimensions are not to scale.

Another downside of the SiC MOSFET is the lack of a simple production process. If ion implantation is used, an annealing step is required at 1600°C, and this high temperature makes self-alignment of the source and the drain to the gate incredibly challenging. Consequently, to date all SiC MOSFETs are made without self-alignment, typically limiting integration to a gate length of 1 µm.

Back to the future

To find the best way forward we have delved into the past, studying a semiconductor technology from the 1960s: The bipolar integrated circuit formed in silicon. This technology ruled the roost until silicon CMOS reached a sufficiently high level of reliability that allowed it to dominate the integrated circuit, just like it does today.

Should you open a recently written microelectronics textbook, you'll see that the focus is on the CMOS IC. But if you can get your hands on a 1960s textbook, you will find circuit topologies for every function formed from the bipolar junction transistor (BJT).

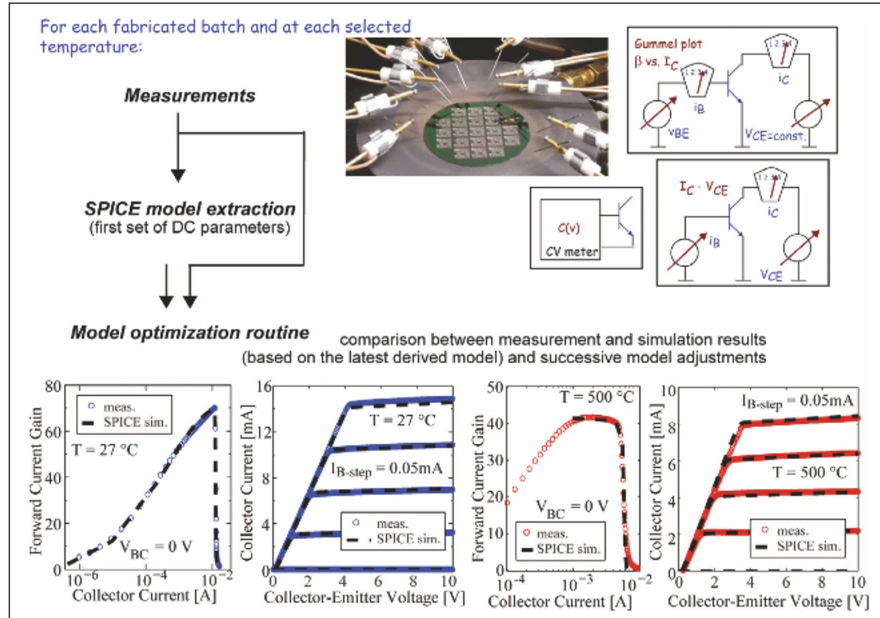


Figure 2. SPICE models are continuously improved, using measurements from each batch at several different temperatures. However, it is only mainly DC parameters that have been fully characterised, so AC performance can only be measured after completion.

One of the great strengths of the BJT is that its threshold voltage does not vary with temperature. Although that's unfortunately not the case for built-in voltage, which drops by around 2 mV/°C, this dependency can be exploited, allowing the creation of bandgap voltage reference circuits that counteract the influence from temperature variations – this is the approach that is adopted in precision analogue-to-digital converters. What's more, we have shown that discrete BJTs and entire ICs can be realized without any ion implantation, circumventing the need to perform high-temperature annealing, which causes defects and ultimately impacts performance and reliability.

We have been developing our SiC BJT technology in our own university cleanrooms for more than a decade. Milestones in this project include the development in 2005 of *n-p-n* BJTs capable of handling up to 3 kV. Since then we have refined process and device, with the peak operating voltage of our BJTs increasing to 6 kV.

There are some key differences between the design of a high-voltage switch and an IC technology. With a switch, current is conducted from the front side to the backside of the wafer, with the collector region in the substrate (see Figure 1).

In comparison, for an IC technology, the BJTs must be isolated from one another, and all contacts made to the front side. We insert an extra *p*-type isolation layer to address this need, and have turned

to thinner epitaxial layers, due to the targeting of lower voltages.

Other key building blocks for the IC are the resistor and the capacitor. With our technology, integrated resistors can be implemented in emitter, base and collector layers by accounting for the expected sheet resistance and specific contact resistance of the selected layer. Note that typical room temperature sheet resistance values for tested epitaxial structures are between 100 and 200 Ω/square for emitter and collector layers, while for the base layer, resistance ranges from 20 to 80 kΩ/square, depending on doping concentration. It is possible to form capacitors between the emitter layer and metal layer, but they are limited to tens of pF to prevent them from either taking up too much area or introducing too large a series resistance.

Starting from scratch

As this is an in-house technology, there is no design kit. Instead, everything has had to be developed, starting from the epitaxial structure and layout of the BJTs. Following this, we carried out physical device simulation that accounts for the doping and thickness of all active regions, and have also undertaken the development of specific process steps and circuit level models for the BJT, which are a pre-requisite for circuit design.

A key part of this work has been the development of a SiC etching process. This has had to realise adequate uniformity across an entire SiC wafer, initially 50 mm in diameter and now 100 mm. We have found that the first etch that isolates the emitters is critical – remove too much material and the base layer becomes too thin (or even disappears), leading to increased extrinsic base resistance. Another challenge results from the mesa-etching that takes place on a wafer containing the entire epitaxial stack, but has not been subject to ion implantation. After etching, steps between adjacent regions on the surface can be as high as 1 μm, making it challenging to add interconnects, even if they only involve one metal layer.

Before we fabricated the first batch of ICs, we developed BJT SPICE models that were at least adequate for DC simulation by drawing on measurements on our existing high-voltage BJTs. Unfortunately, temperature variation

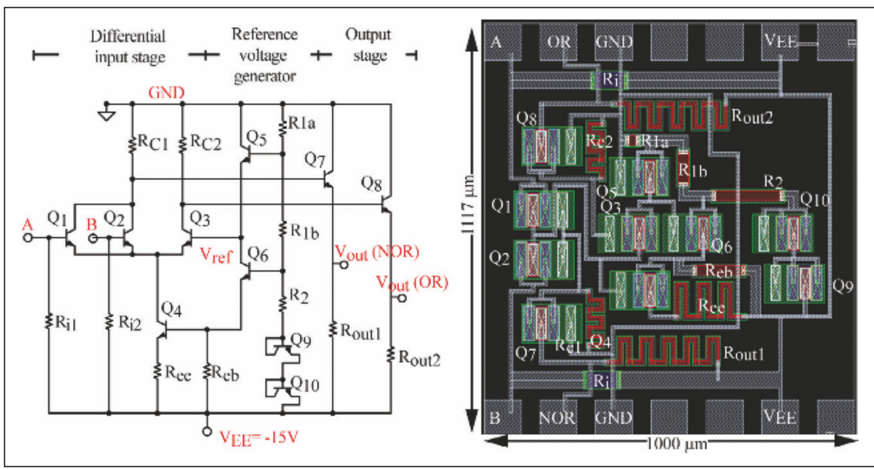


Figure 3. Manual layout of transistors and resistors is time-consuming when only one metal layer is available. Resistors have to be used sometimes to cross connections. Capacitors consume much area and are used sparingly.

models in SPICE are not suitable for SiC BJTs, so separate models had to be obtained for different temperatures. Consequently, after fabrication of the first IC batch, and for each successive batch, new BJT SPICE models have been extracted at discrete temperatures in the range 27°C to 500°C (see Figure 2 for the used methodology and models extracted at two temperatures).

Since we made our first batch, our biggest concern has been the impact of temperature variation on circuit design. Unfortunately, changes in temperature cause many problems: They impact current gain, which can fall by 50 percent when the transistor temperature rises from room temperature to 300°C (see Figure 5); and they are also behind changes in the sheet resistance of the SiC epitaxial layers and, therefore, the resistance of integrated resistors. The good news, however, is that although large variations in the resistance are expected for temperature changes of hundreds of degrees, it is possible to stabilise the DC operating point of bipolar analogue circuits with junction cancellation techniques and resistor ratios, rather than absolute values.

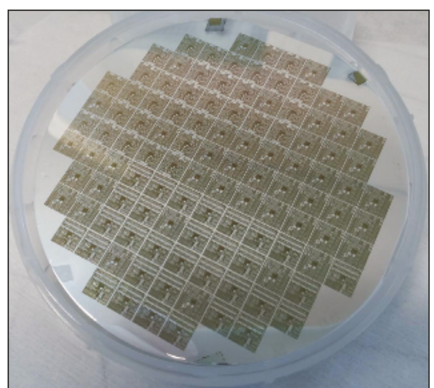
We are delighted to report that our ICs worked since the first batch. We began by making individual BJTs and digital integrated circuits using emitter-coupled logic (ECL), another 1960s technology. To assess the performance of these devices, we carried out on-wafer probing on a temperature-controlled stage that enabled testing up to 300°C. Due to the higher bandgap of SiC than silicon, the SiC ECL needs to be fed with -15 V, compared with -5.2 V for the silicon equivalent.

The current gain of these HBTs diminishes with temperature, falling from 40 at room temperature to 20 at 200-300°C. However, these digital circuits are sturdy enough to successfully operate at up to 500°C and even 600°C, as we have shown for similar gates fabricated in later batches.

To learn as much as possible from these batches, they are used to assess a variety of analogue circuits, including: several different operational amplifiers (one was covered in detail in *Compound Semiconductor* **6** 65 (2014)), Schmitt triggers, BJT drivers, digital-to-analogue converters and even a sigma delta modulator. All these elements can work at up to 500 °C.

As these circuit have just been produced for demonstration purposes, it is no surprise that they deliver an inferior performance at room temperature to those made from silicon CMOS. However, crank the temperature up to in excess of 300°C, and there is simply no alternative to the SiC IC.

Inspect our ICs in detail, and you'll also find that the level of integration is reminiscent of the 1960s: 100 transistors and 100 resistors are typical counts for the largest digital and analogue demonstrators we have made. We have also constructed smaller BJTs with higher



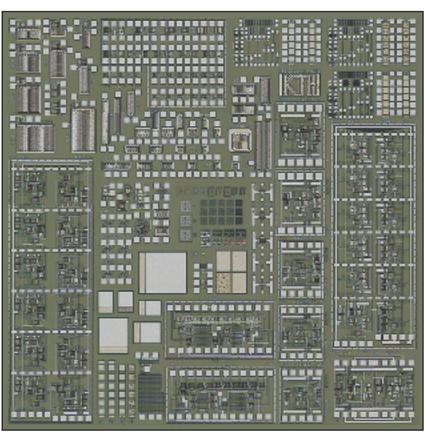


Figure 4. The finished circuit corresponding to the layout in Figure 3 is part of a test chip of 7 mm by 7 mm, and above that is the full 100 mm wafer with several different designs.

current gain, and we have developed two-layer metallisation that enables our technology to be suitable for making many analogue circuits, including complete analogue-to-digital converters.

Another recent development is that of a lateral *p-n-p* BJT formed with the same technology, aside from the addition of one mask layer. This opens the door to the creation of even more textbook circuits in our IC technology.

However, for digital circuits in ECL, scaled BJTs imply lower currents but higher resistor values and thereby larger resistors, so it is not easy to see a way forward to very highly integrated digital circuits.

Questions that we are often asked are what are the temperature limits for our devices and circuits, and what level of reliability can be expected at 600°C. Although some digital circuits have been shown to work at 600°C, the aluminium-based metallisation is not suitable for such extreme temperatures. That's because the melting point of aluminium is only just above this, at 660°C, while the metal diffusion barrier, a TiW layer, is unstable above 500°C.

An attractive alternative is platinum, and we have used this for interconnects in some test circuits. Its downside is that patterning is much more challenging, and this has led us to use lift-off rather than dry etching.

We are yet to perform complete reliability testing, because this will require packaged devices, rather than on-wafer contacting with probes. Our hot-stage on a probe station is also unsuitable for scrutinising reliability, because it is not designed for 500 hours of operation, and the needle contacts are not reliable for repeated probing.

It also makes sense to introduce hermetic packaging of the ICs, a step that would surely extend lifetime. In short, reliability testing is not relevant until our SiC technology is fully developed, including relevant ICs with final passivation layers. Overarching all of these practical difficulties is the need to find testing procedures for operating temperatures that are far higher than those employed for most of today's accelerated testing.

Often the best way to accelerate the capability of a technology is to take on a tough but achievable target. We have adopted this strategy, trying to demonstrate all electronics needed for a Venus lander. The surface temperature of this planet, the second from the sun, is around 460°C, so there will be no

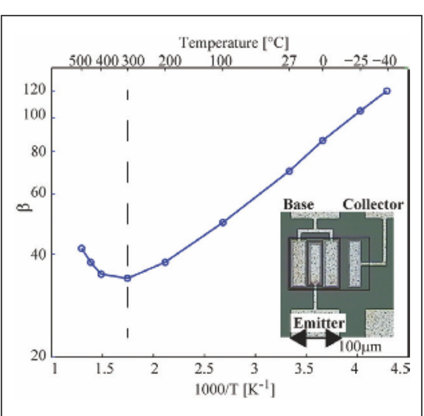


Figure 5. The *n-p-n* BJT current gain varies considerably over the entire temperature range, so circuit designers have to take this into account. A different probe station was used for characterisation down to -40°C.

human accompaniment on any mission, and all data collection and transmission will have to be automatic. To do this will require sensors, amplifiers, ADCs, a CPU, memory, a radio transceiver and power supply.

Although we don't expect to become rich from designing electronics for an exploration of Venus, we are sure that the developed high-temperature SiC electronics will find several terrestrial applications, such as aerospace, combustion monitoring, and drilling operations. This is bound to be a hot topic in the future.

Further reading

The research publications resulting from the HOTSiC project are provided from the home page www.hotsic.se More information on the Venus project can be found at www.workingonvenus.se

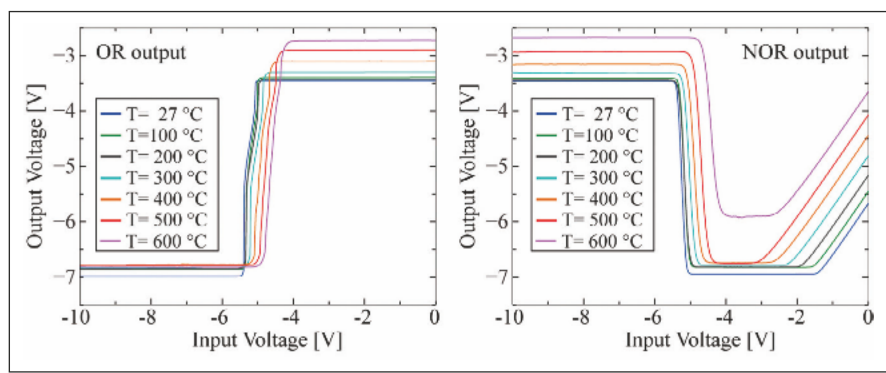


Figure 7. Transfer characteristics of a digital ECL OR-NOR gate (NOR output shown). Noise margins can be extracted from these curves, and this specific design achieves almost 1.5 V noise margin over the entire temperature range.

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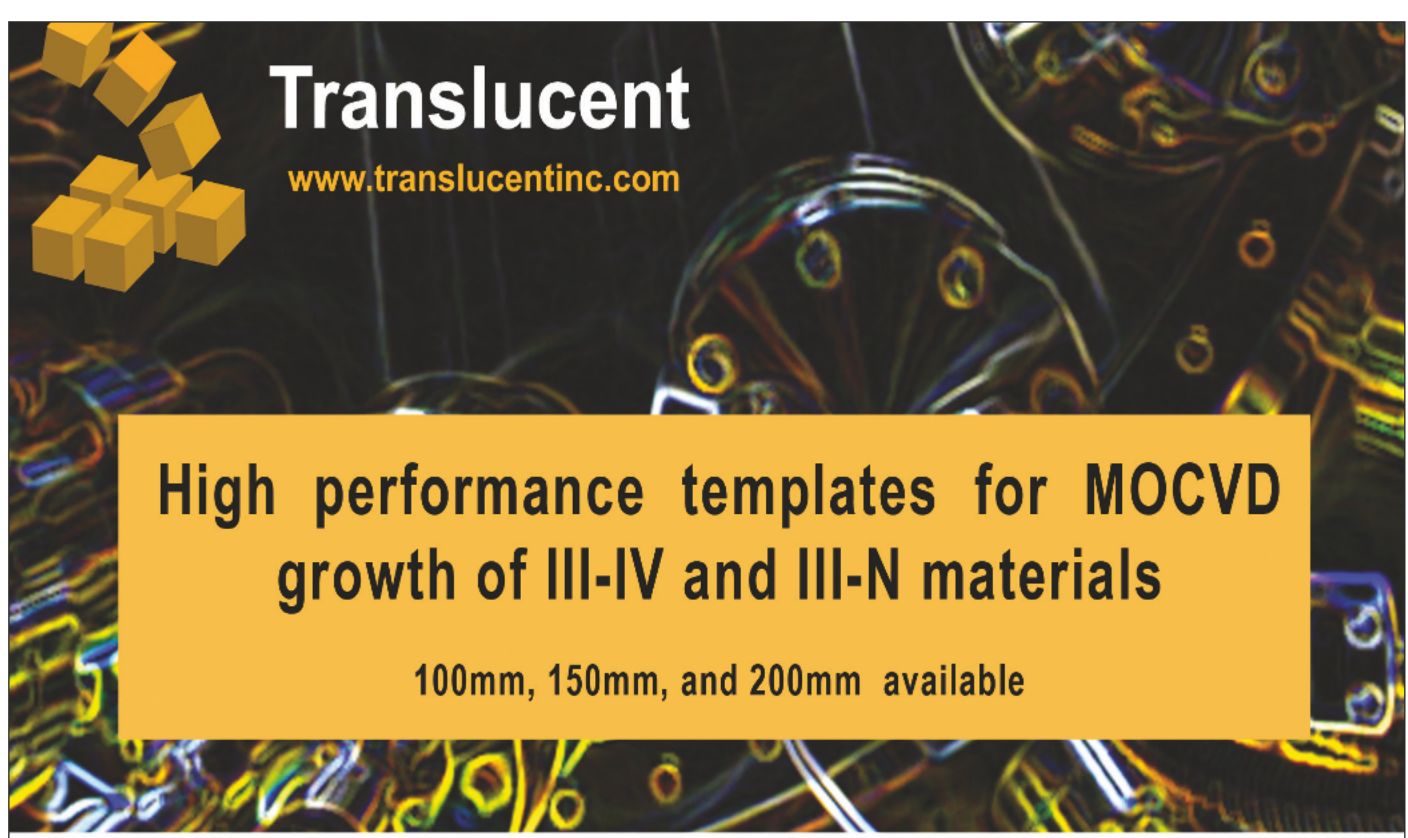

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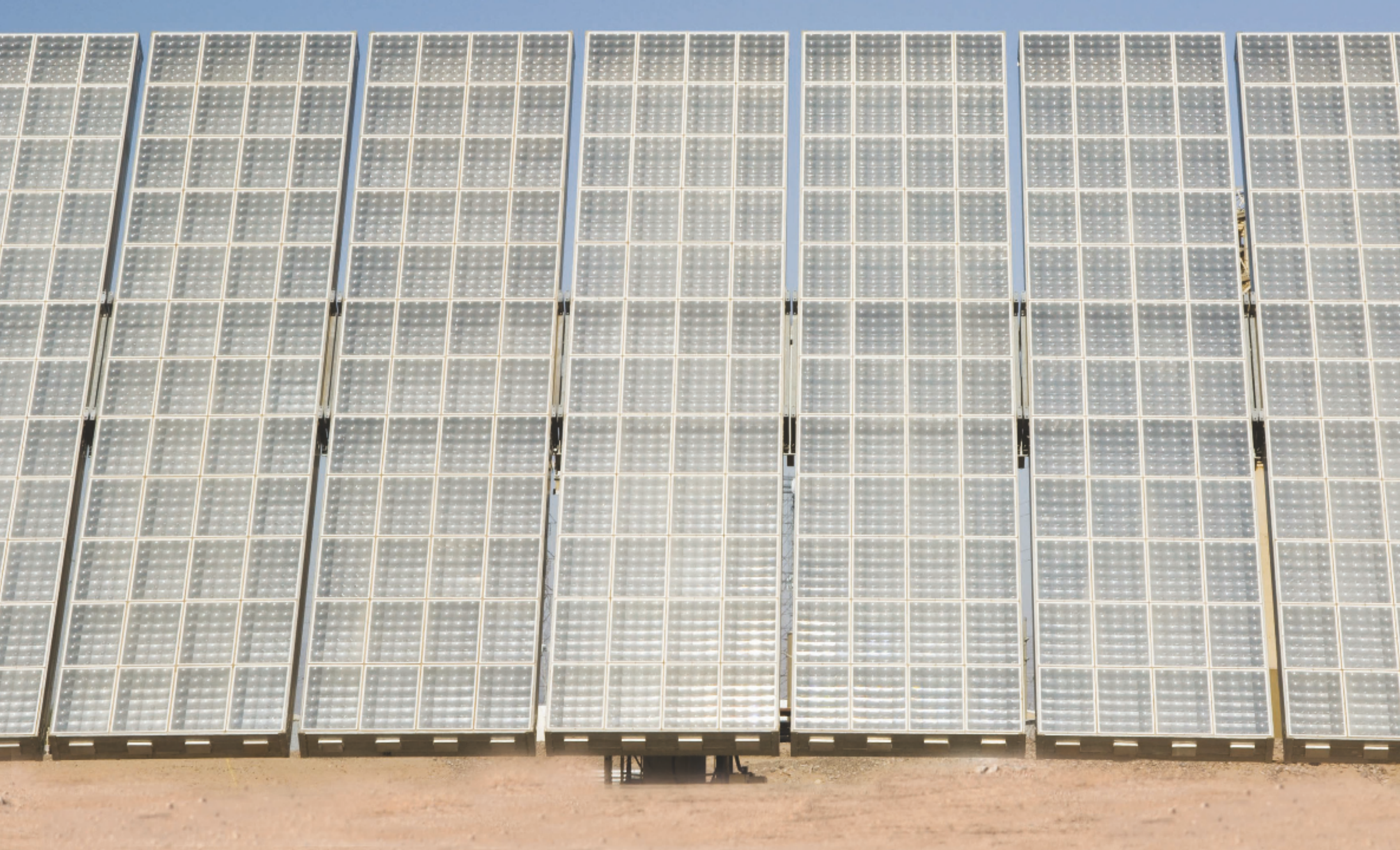
Turning to ultra-high concentrations to increase the competitiveness of CPV

Slashing the cost of CPV will not come from just edging up efficiency: It will also result from introducing ultra-high concentrations and moving to streamlined, high-volume production

BY RICHARD STEVENSON



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IN SOLAR CIRCLES, if you want to generate some positive publicity, there is little that can beat the breaking of the solar efficiency record.

It is easy to understand why such success can hit the headlines. It is partly because the breaking of a record is a clear success story – and it is also because solar technology is rather pricey, and gains in efficiency promise to allow it to be far more competitive with the likes of coal, oil and gas.

However, boosting efficiency is not the only way to bring down the cost of solar energy generation, and in the case of concentrating photovoltaics (CPVs), there are two other levers that can deliver far greater gains. One route for slashing costs is to move to ultra-high levels of concentration – that is, 1000 suns or more – and the other is to increase manufacturing volumes and streamline production.

Championing the adoption of both these approaches is Carlos Algora, Head of the III-V Semiconductors Group at the Solar Energy Institute of the Technical University of Madrid (IES-UPM). Thanks to the efforts of him and his team, those working in this field can benefit from calculations for determining how the cost of electrical generation for CPV systems depends on efficiency, the level of concentration, and a factor that Algora refers to as 'learning'.

The latter factor, 'learning', encompasses a variety of cost-reducing mechanisms. They include the fall in costs that occurs as manufacturing ramps up, and engineers involved with this introduce new approaches for cutting costs – and learning also includes the trimming of costs that result from the use of mass production plants and the negotiation of attractive discounts from suppliers.

Calculations including all of these factors are carried out by considering a starting point of low-volume production, such as 1 MW, and efforts are made to determine how far costs will fall as production climbs to far higher values, such as 1 GW.

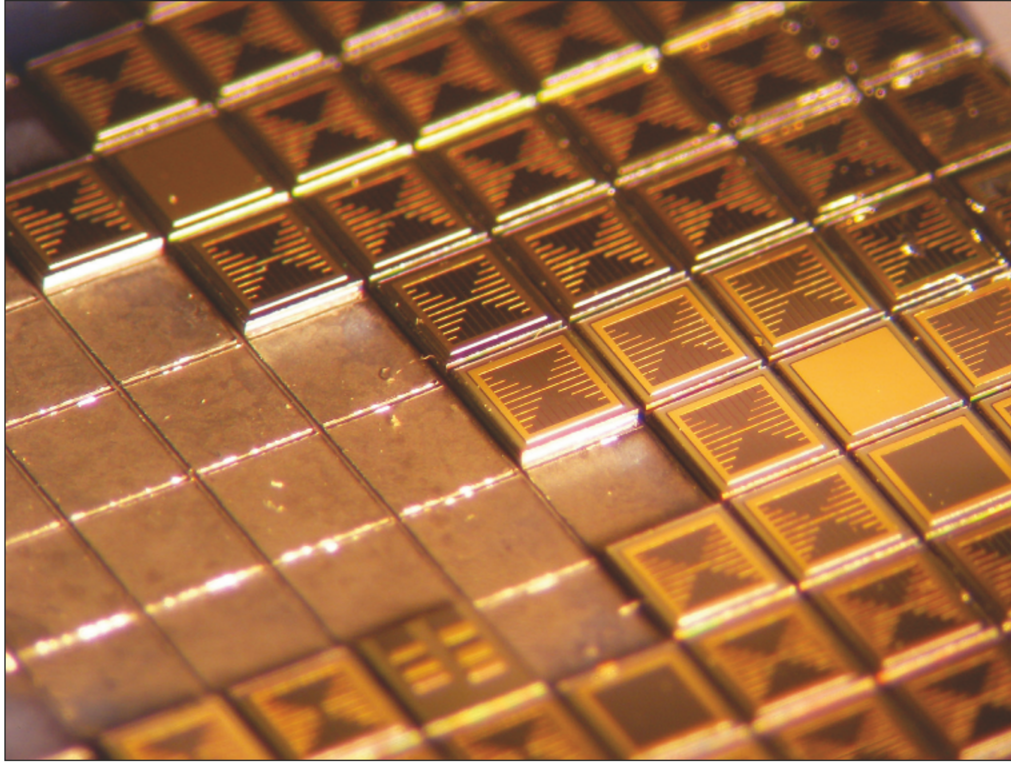
"What is important is that we apply different learning coefficients depending on the components of the CPV system," argues Algora. This means that learning associated with optoelectronics is applied to secondary optics, while the learning of motors and related components is used for trackers. The most recent set of calculations by Algora and his co-workers have determined the dividends paid by learning, higher concentrations and increasing efficiency. To judge the level of cost reduction, keep in mind a baseline figure – installation costs of 2.40 Euro-per-Watt-peak for a 500 suns CPV plant of one megawatt employing 36 percent efficiency cells.

Increasing cell efficiency will obviously bring this installation cost down, but even raising efficiency to a jaw-dropping 50 percent — 4 percent above today's efficiency record – will only deliver a fall in costs to 1.75 Euro-per-Watt-peak, according to the calculations. Such gains are possible just through learning, however, and if concentration is increased to 1000 suns, it is possible to do even better, reaching Euro-per-Watt-peak values of 1.30-1.45. But most encouraging of all, if the three levers of efficiency, concentration and learning are pulled in unison, it is possible for post-learning generation costs to nudge 0.8 Euro-per-Watt-peak at 1000 suns.

Look carefully at these calculations and you will find a hierarchy of factors influencing the cost of CPV: first learning, second the level of concentration, and third efficiency. But the bad news is that the factor that can deliver the biggest benefit, learning, cannot be the initial driver to lower costs. That's because it will only be possible to draw on the benefits of learning by first increasing demand for CPV, which must be spurred by moves to higher efficiencies and concentrations.

Rebuffing the critics

Although the benefits of moving to higher concentrations are clear from these calculations, naysayers may argue that there are many reasons why

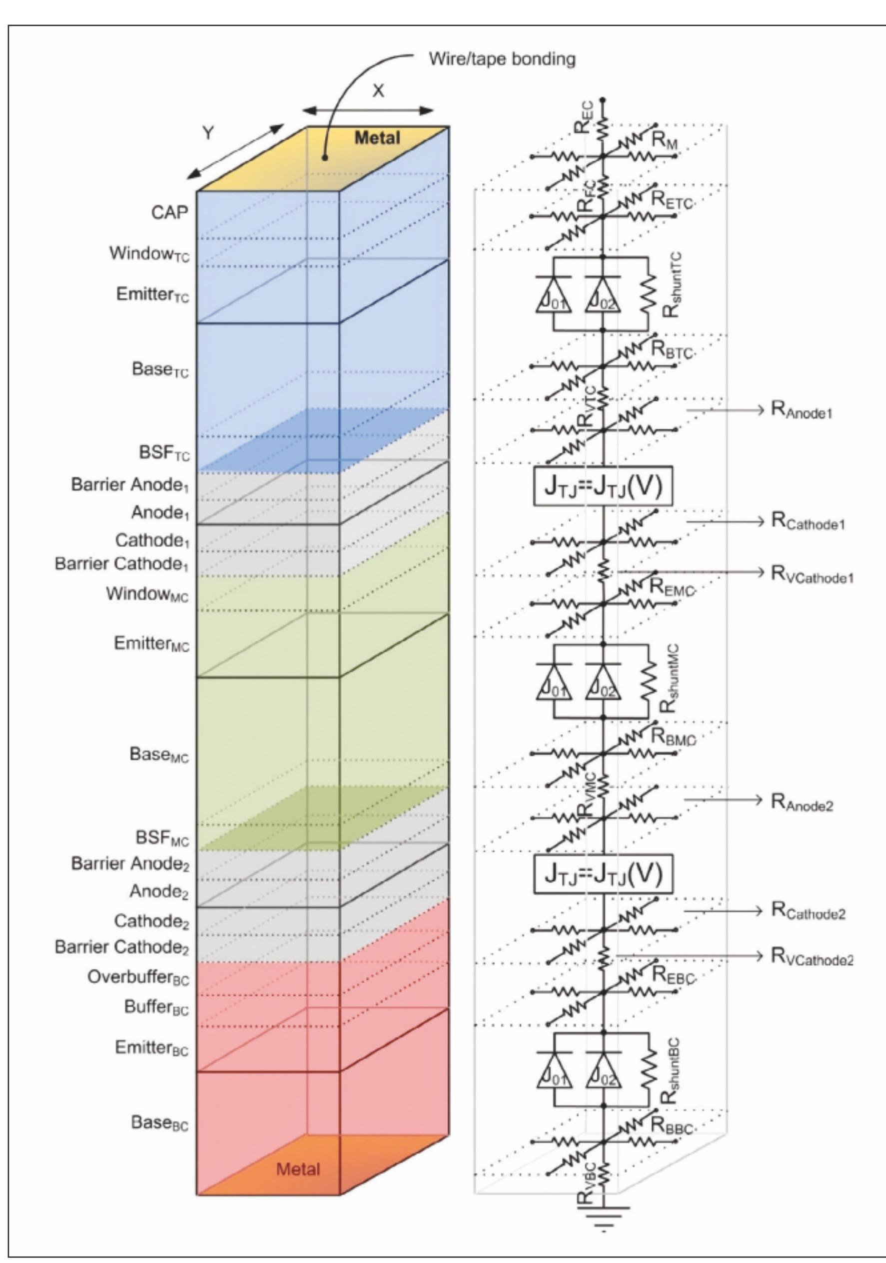


1 mm^2 GaInP/GaInAs/Ge triple-junction solar cells developed by the III-V Semiconductors Group of IES-UPM. Calibrated efficiency of these devices is 39.2 percent.

greater focusing of the sunlight is not a great idea. They might point out that ultra-high concentrations would make it very tricky to construct a stable multi-junction cell that would not overheat and would provide a sufficiently low series resistance. And they might also claim that increasing the level of concentration would place very challenging demands on the pointing accuracy for the focusing of the sunlight – after all, the most widespread CPV system built by Soitec, which operates at 500 suns, has an acceptance angle of about 0.5 degrees.

Algora and his co-workers are rebuffing these criticisms by designing and manufacturing new cells that work better at high concentrations. They are designed to work with already available high-performance focusing elements for ultra-high concentrations, such as those developed by LPI. "The market is dominated by the classical Fresnel lens, which is not specifically developed for CPV," argues Algora.

With more appropriate optics, an acceptance angle of around 1 degree at concentrations of 1000-2000 suns is possible. The rub is a move to two-stage optics, but even this has an upside: With secondary optics, an optical element covers the cell, protecting it from the environment, so reliability is further increased.



The structure of a triple junction solar cell unit under the front contact (left figure) and the corresponding 3D distributed model (right figure) developed at IES-UPM.

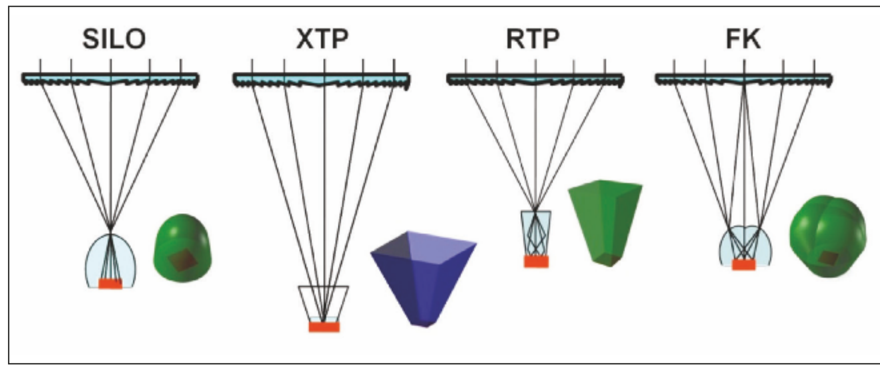
Another advantage of introducing a new optical design is that it can improve the level of uniformity of concentration impinging on the cell. Algora says that about ten years ago the situation was terrible, with non-uniformity (peak-to-average) factors of typically four or five at ultra high concentrations. Currently, this situation has improved with peak-to-average factors of now about 1.5-2.0. This means that when optics are purchased today for building CPV modules operating at 1000 suns, at the centre of the cell the level of concentration can be 1.5-2.0 times this. And that is a problem, because many of the cells designed to operate at 1000 suns have an efficiency that drops off a cliff, rather than slowly decreasing at higher values.

What's more, champion cells rarely give their best at 1000 suns: Soitec's 46 percent efficiency four-junction, wafer-bonded cell produced its best performance at 508 suns, while Sharp's inverted metamorphic structure delivered its peak efficiency of 44.4 percent at 302 suns and Spire's device topped out at 42.3 percent at 406 suns. However, a peak efficiency at higher concentrations is possible. For example, the West-coast start-up Solar Junction has produced triple-junction devices delivering 44 percent efficiency at 947 suns, and the IES-UPM team has produced even higher values for concentration at peak efficiency with cells sporting fewer junctions: it has reported 26.2 percent efficiency at 1004 suns for a GaAs single-junction solar cell and 32.6 percent efficiency at 1026 suns for a GaInP/GaAs dual-junction solar cell.

To those that believe over-heating of the cell could be a concern at ultra-high concentrations, Algora counters by pointing out that if the cell is small enough, there isn't even the need for active cooling. According to him, at 1000 suns the light power density impinging on the cell is 1 MW/m^2, so for a

cell with a surface area of 1 mm^2, incident power is just 1 W. If 40 percent of this energy is converted into electricity, that leaves 600 mW generating heat, which is easy to extract.

With small cells, one big issue today is laying hands on product. Algora says that in the brochures of the main solar cell manufacturers, the smaller solar cells are 5 mm by 5 mm or 3 mm by 3 mm. Such cells are designed to operate at 500 suns, which represents the biggest market for CPV, and in this realm thermal management is not such an issue. However, as more CPV system makers move to ultra-high concentrations, availability of smaller cells should rise.



Diagonal cross sections of different CPV systems with secondary optics elements. From left to right: Secondary lens producing Köhler integration with 1-fold (SILO), truncated inverted pyramid mirror (XTP), truncated inverted pyramid glass (RTP) and secondary lens delivering Köhler integration with 4-fold (FK). All the elements have been simulated with the 3D distributed model of IES-UPM.

Carrying currents

Moving to concentrations of 1000 suns or more places additional demands on the tunnel-junctions connecting the cells. These current-carrying bridges must not limit the flow of charge through the cells, so they should ideally have a peak current density in excess of 30 A cm^{-2} – this capability can accommodate currents associated with concentrations of up to 2,000 suns. While offering this level of performance, the voltage drop across the tunnel-junction should be as small as possible, in order to realise as high an efficiency as possible.

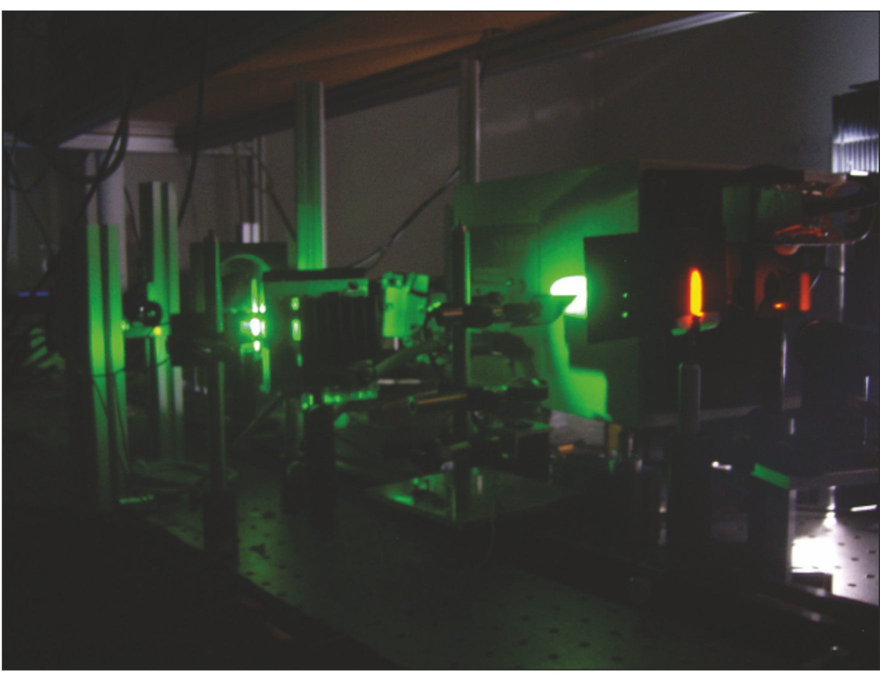
Orchestrating efforts to develop a high-quality tunnel junction is Algora's colleague, Enrique Barrigón. He explains that the material used to make the tunnel-junction governs the peak current density. "In order to have high peak current densities, you should use low bandgap materials, but that introduces a limitation into your design." That limitation is light absorption, which drags down cell efficiency of the subcell beneath the tunnel junction.

It is possible to overcome this conundrum with a special tunnel junction designed by the IES-UPM team that is built from the pairing of *p*-type, heavily doped AlGaAs and *n*-type, heavily doped GaInP. "It has a very high peak current density, and at the same time it is transparent for the light going into the middle cell."

To reach such a high current density – it is initially 996 A cm^{-2}, and falls to 235 A cm^{-2} after a thermal annealing step that simulates the growth of additional sub-cells – traps must be present in the structure. "If you try to simulate the behaviour of your tunnel junctions, it is impossible to get such high peak current densities unless you introduce some trap defects that enable the tunnelling," explains Barrigón.

Optimisation of the multi-junction solar cell also requires optimisation of other aspects of the device, such as the contacts. Algora and his team have been active in this area, developing a three-dimensional distributed model that simulates the operation of the solar cell at real conditions.

"It is compulsory to go towards a distributed model, because inside a concentrator the solar cell experiences unhomogeneous illumination in terms of intensity, chromatic aberration, etc," explains Algora. Due to these differences, there are variations in voltage losses and photocurrents, but with the distributed model it is still possible to optimise the design of the front metal grid, current



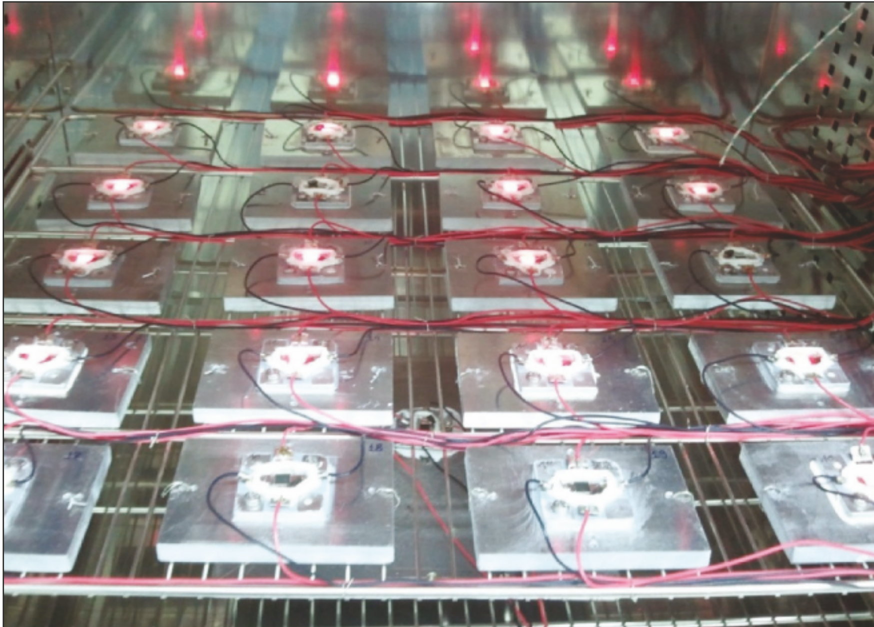
The characterization setup at IES-UPM for measuring the electro-optical properties of multi-junction solar cells

matching among the subcells and the solar cell dimensions. "It is a very useful model when you go towards the real world," claims Algora.

While undertaking all this work, the Spanish academic has been a vehement campaigner for improving the manufacturing process. Since 1997 he has been advocating a move to an LED-like approach to making CPV cells and modules that will allow a trimming of the cost of this technology. He holds a Spanish patent related to this that was granted in 2000, and he and his team have collaborated with Semprius, a pioneer of ultra-high concentrations that employs 1,111 suns on cells with sides of 0.6 mm (see *Compound Semiconductor*, July 2014, p. 34).

Algora believes that the LED industry can offer some insights into multi-junction reliability. Both species of device may incorporate similar III-V materials, and with lifetimes of 50,000-100,000 hours, the reliability of the LED is encouraging for the future of CPV.

Giving rise to further optimism, current densities in LEDs are higher than those in multi-junction cells operating at ultra-high concentrations. However, there is good reason for caution at this stage: Since CPV systems need to operate for 30 years or more, the cells must have lifetimes around two times that of LEDs.



A temperature-accelerated life test of commercial triple solar cells carried out at IES-UPM to assess the reliability of the devices.

Looking ahead

While there are compelling arguments for strong growth of a CPV industry sporting ultra-high concentrations, Algora believes that will not happen overnight, with success hinging on both the future of the PV industry at large, and the CPV industry operating at more modest concentrations. "We have the technology in the main components – solar cells, optics, trackers and modules – and we have a very brilliant future regarding improvement in all of these aspects, mainly solar efficiency," argues Algora.

The MOCVD reactor at IES-UPM.

However, for sales to rise, he believes that the cost of the technology must drop to less than that associated with silicon flat-plate technology (he says that today the cost of CPV should be as little as 20-30 percent more expensive than silicon if installed in places with 20-30 percent higher direct irradiance than those usually used for silicon systems).

The fastest way for CPV to close the gap with silicon is learning, and according to Algora, learning means production of close to half a gigawatt, or a gigawatt. At present the only companies able to do that are Soitec and Suncore, so for the benefits of learning to materialise, shipments of CPV systems from these companies must climb over the next years.

If Soitec and Suncore are successful, this will allow companies with different approaches to CPV to make an impact, including those pioneering ultra-high concentrations. "These new actors will benefit from a lower price of trackers and a low price of optics," says Algora.

"But now, CPV is in the hands of these two biggest companies, so we would very much like the success of these two companies."

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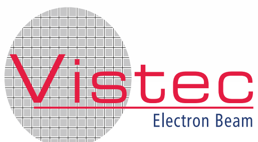

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Getting a grip on sapphire etching

Novel clamping of sapphire looks to unleash brighter, cheaper LEDs

BY MARK DINEEN FROM OXFORD INSTRUMENTS

MANUFACTURERS OF LEDs are striving to make cheaper devices that emit more light. If they succeed, sales will rise, and these chipmakers will enable the LED to increase its deployment in an ever-growing number of applications.

One common and effective route for increasing the bang-per-buck of the LED is to switch the foundation for the device from a flat sapphire substrate to one that has been etched to form a patterned surface. This alternative, known as patterned sapphire, is increasing in popularity because it delivers two key benefits to the makers of high-brightness LEDs: it increases the fraction of light emitted from the device, thanks to the controlled texture; and it leads to a lower density of defects within the film, thanks to growth on a three-dimensional landscape that spurs earlier coalescence of GaN epitaxial islands during MOCVD growth.

The downside of turning to patterned sapphire is that etching this material into useful patterns is not easy. There is a processing cost involved, and this must be low enough to not negate the benefit associated with increased LED performance.

Etching options

Two options are available for forming patterned sapphire: wet etching and dry etching. The former involves a combination of high

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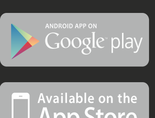

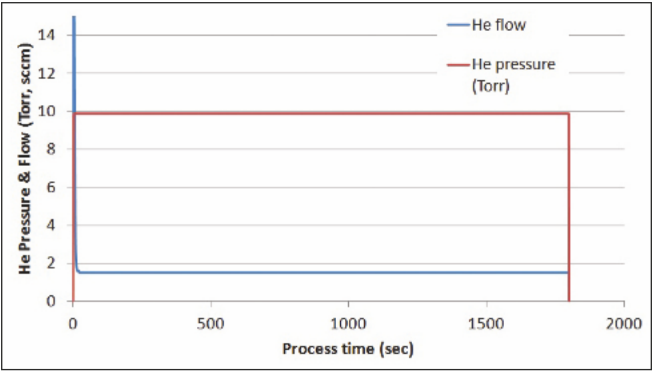

Figure 1. Good heat transfer is possible with electrostatic clamping, thanks to helium between the wafer and the electrode. Note that the helium backside pressure is constant, and the helium leakage is low and constant.

pressures and a mixture of sulphuric and phosphoric acid, with very specialised equipment needed to ensure that work takes place in a safe manner. Etch rates can be relatively high, such as up to 1 μm per minute, but there is often the need for a hard mask. Unfortunately, this is constructed using additional PECVD and etching steps.

The alternative is to dry etch the wafer, using a photoresist mask to transfer the pattern to the sapphire. One common approach is to plasma etch using a BCl_3-based recipe and employ a high density plasma source such as an induction-coupled plasma.

Moderately high ion bombardment energies are needed to realise a viable etch rate, which is in the range 50 – 150 nm per minute. Although higher etch rates are desirable, they can degrade the resist mask at wafer temperatures exceeding around 140°C.

Regardless of the etching technique, it is critical for the process to yield a uniform array of defined conical shapes across the entire wafer. Realising this is not trivial, because it cannot result from anisotropic etching, the norm for semiconductor processing.

To produce features with desired dimensions, engineers tend

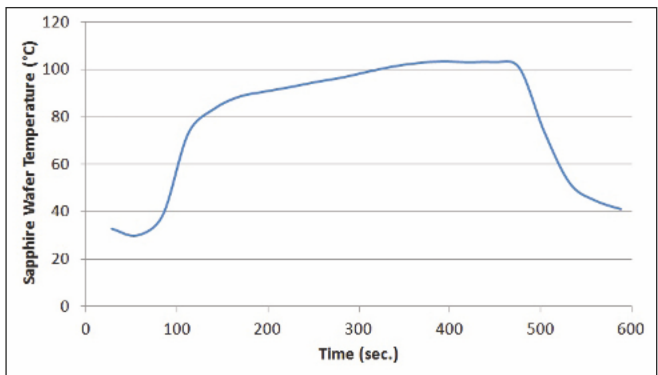

Figure 2. Maintaining wafer temperatures during aggressive plasma processing well below 140 0C prevents burning of the photo-resist.

to begin with vertical resist patterns (cylinders), and employ an etch process that transforms the shape to the desired form while etching down into the sapphire. Wet etching is typically more isotropic, leading to shapes that depend on crystallographic orientation. Meanwhile, with plasma etching, it is possible to shape the resist through either controlled resist reflow, or more commonly by faceting erosion of the resist corners – an effect normally minimised in anisotropic etching.

Moving to 150 mm

Like other sectors with the semiconductor industry, makers of LEDs are moving to larger wafers to cut costs. Benefits of making this move include increased yield, increased automation, and reduced wafer 'touch time' – many of the same gains that drove the silicon industry to adopt larger and larger wafers.

However, it would be wrong to suggest that all LED makers are making the transition to 150 mm sapphire. Although leading LED maker Lumileds, for example, has been producing devices on 150 mm lines for several years – and is enjoying order-of-magnitude improvements in both LED die capacity and process yield by moving from 3-inch to 150 mm substrates – quite a few LED manufacturers have no plans to move beyond 100 mm in the foreseeable future.

The size of the wafers that are being used by LED makers governs whether it makes sense to perform batch or single-wafer processing of sapphire. The aggressive etch process needed to etch sapphire dictates that every wafer must have cooling, and performing this on a large batch makes sense for 2-inch, 3-inch and 100 mm wafers. However, this argument doesn't hold for 150 mm sapphire, which is falling in price, and in this case a single-wafer platform may be the best way forward for some, but not all, manufacturers.

Those LED chipmakers that are using 150 mm sapphire will hope to benefit from the plasma etch tools previously developed for mainstream silicon. However, the bad news for them is that such tools are not immediately suitable for etching sapphire. Dry etching is a very aggressive process, with much energy required to break sapphire bonds and remove material, and this can lead to heating of the wafer and the photoresist mask. Heat the mask above 140°C and it is destroyed.

To prevent overheating, wafers can be clamped to a temperature-controlled electrode. However, due to the low pressure in the chamber – it is less than 10 mTorr – there is a very limited heat conduction path between wafer and etch electrode. Adding helium gas, an approach often referred to as helium backside cooling, fills the void between the wafer and the electrode, leading to an improved conduction path. However, there is a penalty to pay for this: A pressure behind the wafer of several millibar, which will cause it to move if it is not clamped down.

One option for keeping the wafer in the right place is to mechanically clamp it, but this occurs at the expense of masking the wafer edge, and it may lead to particle generation. Due to these downsides, electrostatic clamping is more appealing – this is standard for silicon, but, unfortunately, it does not work well for highly insulating substrates. That's

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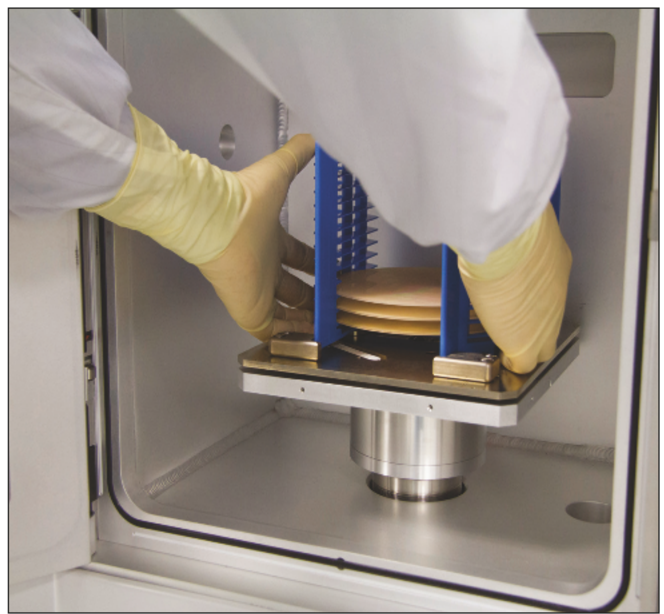
because sapphire electrostatic clamping relies on creating polarisation charges in the wafer, 'stretching' the molecules to create dipoles, rather than displacing mobile charges. Consequently, there are several weaknesses associated with electrostatic clamping: the forces are much lower at the same clamp voltage; higher clamp voltages can cause premature failures in the electrostatic clamp table itself; if the table is robust enough, higher voltages can lead to polarisation of the dielectric layer of the electrostatic clamping itself, and then clamping is lost; and polarisation charges can take more time to create and to dissipate than mobile charges in a semiconductor, so it can be more challenging with sapphire to set up clamping and achieve reliable de-clamping.

At Oxford Instruments Plasma Technology in Yatton, UK, we have overcome these issues by developing a proprietary technique that allows electrostatic clamping of bare sapphire. This patent-pending approach (the inventors on the application are Y Song, J Ferreira and M Cooke) is capable of gripping 150 mm sapphire, even during the cooling process (see Figure 1 for results demonstrating constant clamping of a bare sapphire wafer for thirty minutes during etching).

With electrostatic clamping, some helium will always flow from out of the back of the wafer. Our measurements taken during the development of our clamping process reveal that this flow of helium is stable and relatively low, which is indicative of a constant clamping force. Efficient heat removal from the sapphire is then possible, while maintaining a constant backside helium pressure. Readings of wafer temperature show that this never gets close to 140°C, the temperature at which the photo-resist can burn (see Figure 2).

Preventing damage to the photoresist has enabled us to develop and launch the PlasmaPro100 Polaris, a single wafer tool with electrostatic clamping that is capable of etch rates above 100 nm per minute. When a wafer is loaded into this tool it is clamped and cooled, before a BCl_3 plasma is created within the process chamber.



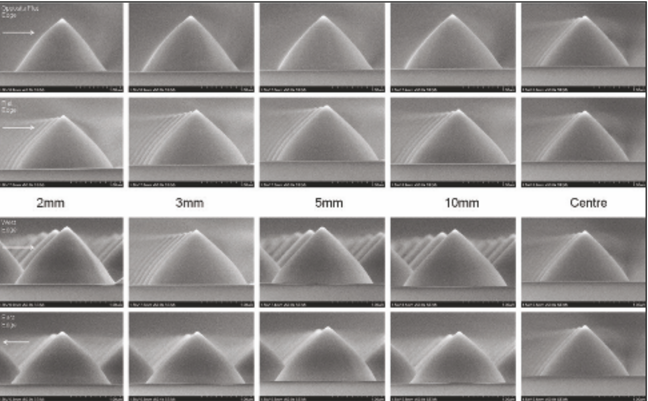


Figure 3. The PlasmaPro100 Polaris is capable of maintaining the profile of the features very close to the edge of the sapphire wafers.

Each gripped sapphire wafer is attached to an electrode, and applying RF power to this leads to the acceleration of ions generated by the plasma. These charged particles bombard the wafer, removing both sapphire and photoresist. Where photoresist remains, the area under the pattern is not etched.

However, the nature of this process and the photoresist shape means that the footprint gets smaller and smaller as the action progresses, leading to sloped features that are transferred to the surface of the sapphire wafer.

The process is completed when all of the photoresist has been removed. At this point, there are domed or pointed features across the wafer.

Optimising the dimensions of these features enables the production of LEDs with superior performance. One current trend within the LED industry is to move to higher features with a very flat sidewall, and to form cones rather than domes. In this regard, dry etching offers a key advantage over a wet etch, because the final pattern can be selected by making adjustments to the photoresist mask. With this etching technique it is possible to produce a sapphire surface with a vast array of high, sharp cones that hold the key to GaN films with a lower defect density and LEDs with increased light extraction.

To trim manufacturing costs, chipmakers use as much of the wafer as possible to produce LEDs. With our electrostatic clamping, yields can be incredibly high, because the profile shape of the features is maintained to within 2 mm of the edge of the wafer (results shown in Figure 3 were obtained with an etch rate of 150 nm per minute and a selectivity to the photoresist mask in excess of 0.7:1).

This capability will help to bring down the cost-per-LED of producing patterned sapphire. What's more, as our tool can also enable optimisation of the shape of the etched features – leading to improved film quality and increased light extraction – it will be able to play a key role in bringing cheaper, brighter LEDs to market.

Will III-Vs make an impact in **next-generation CMOS?**

Mixed messages emerge from IEDM, with experimental efforts highlighting the promise of III-V transistors and calculations unveiling some weaknesses

There is a lot to like about simple stories. They are easy to tell, remember and recite, and a lack of conflicting views means that they do not lead to any need to figure out where one stands.

Rewind the clocks a few years in the silicon industry, and it would only require a simple story to outline the path of progress associated with this technology. Back then, engineers would improve circuit performance while cutting costs by taking the existing transistor and trimming its dimensions.

Recently, however, complexity has dogged the story of silicon. There has been the introduction

of hafnium dioxide, so that the gate dielectric doesn't leak electrons. And this device has had to rise out of the plane of the substrate, so that it can maintain its traditional levels of improvement with each generation of scaling.

Even greater changes are on the cards in the next decade or so, with the silicon in the channel of the transistor expected to make way for higher mobility materials that will enable high levels of performance at lower operating voltages. InGaAs is a strong contender for taking over the nFET, while germanium is tipped for making an entry into tomorrow's pFETs.

Both of these materials were discussed at the recent International Electron Devices Meeting in San Francisco on 15-17 December, 2014, where several groups reported results of experimental work and calculations relating to post-silicon transistors. In this latest chapter of the silicon story, conflicting accounts were presented of the promise of these alternative materials for making an impact in tomorrow's silicon foundries.

Go with germanium?

One paper questioning the potential of InGaAs for improving *n*-type finFETs came from a team from Samsung Semiconductor. They have calculated that this ternary would not deliver the necessary improvement over silicon, in terms of carrier transport properties, because it would not produce the expected ballistic performance in a device with dimensions suitable for a next generation transistor.

"I was somewhat surprised [by this result]," revealed Seonghoon Jin during an interview with *Compound Semiconductor*. "Regarding the reasons, both the low density-of-states and strong surface-roughness scattering are important factors."

A key aspect of this work is that both the coupled multi-subband Boltzmann transport equation and the drift-diffusion equation are solved self-consistently to evaluate finFET performance with new channel materials. "I think that the modeling methodology is state of the art," argues Jin, who included in the calculation some features that are particularly important to III-V channel finFETs, such as surface roughness scattering, a density-gradient model, and band-to-band tunnelling.

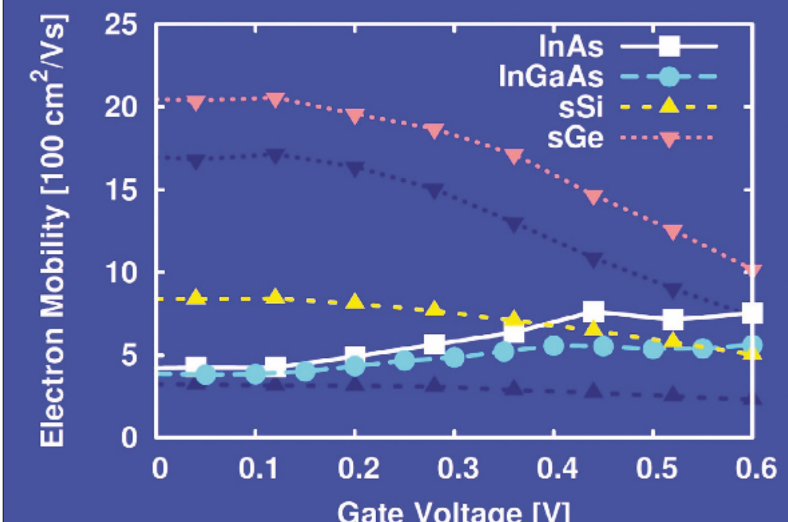


Figure 1. Calculations by a team from Samsung suggest that channels made from strained germanium can offer a higher mobility than those formed from InGaAs. Note that the darker lines with triangles are for unstrained channels of germanium and silicon.

According to Jin, one strength of the team's calculations is that by solving the multi-subband Boltzmann transport equation in the channel, the effects of band structure, quantization and quasi-ballistic transport are accounted for. The distributed contact resistance and non-uniform current path are also considered, thanks to the solving of the drift-diffusion equation in the source and drain regions.

The team calculated the performance of a device that is a simplified version of the future node finFET and has a fin width of 6 nm. Calculations considered four channel materials – InAs, $In_{0.53}Ga_{0.47}As$, silicon and germanium – and for the latter two materials, the impact of tensile stress was included (see Figure 1).

Self-consistent simulations suggest that a silicon channel provides the largest inversion charge, but the lowest injection velocity; an InAs channel offers the highest injection velocity, but the lowest inversion charge; and germanium delivers the highest mobility, which is realised with a reasonable carrier density.

Given these attributes, it is not surprising that the calculations suggest that a strained germanium channel delivers the highest on-current. However, when the team included a more realistic contact resistance in their model, drain current fell sharply, so it is imperative that this resistance must fall if *n*-type strained germanium is to become an attractive option for tomorrow's nFETs. If that does not happen, strained silicon can deliver better performance.

Or are III-Vs better?

A more positive view on the role of InGaAs in future ICs came from a paper presented by Enrico Caruso and colleagues from the University of Udine, Italy. Caruso told *Compound Semiconductor* that at a supply voltage of 0.5 V, the team's calculations suggest that on-current for InGaAs exceeds that for silicon by about 30 percent. "It must be stressed that III-V materials have a switching time smaller than silicon, so even if the current is the same, it is possible to increase the performance anyway."

Caruso believes that one of the most important aspects of the team's work is that it takes into account most of the physical effects necessary for the characterization of MOSFETs with a III-V channel. "In particular, it accounts for far-from-equilibrium carrier transport in the channel, size and bias induced quantization, and the effect of

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interface traps on the transport."

There are weaknesses of the model, however: It is semi-classical, so it does not include quantum effects in the transport direction, such as band-to-band tunneling and source-to-drain tunneling. "Simulations in this work do not consider series resistance, and thus our results should be regarded as an upper limit for device performance," argues Caruso. He also points out that although the short-device simulations are far from equilibrium, trap states along the channel are populated using an equilibrium Fermi-Dirac distribution. "We think that the interplay between strain and interface traps should be further verified with more accurate atomistic simulators."

The team from Udine has modeled the performance of strained and unstrained InGaAs and GaSb channels with an 11.7 nm gate, a length expected to be introduced in foundries in 2020 according to the *International Technology Roadmap for Semiconductors*. Using an appropriate well thickness of 6 nm, the theorists found that $In_{0.53}Ga_{0.47}As$ channels can outperform those made from strained silicon, in terms of drain current, for gate-source voltages up to about 0.55 V – beyond that, this III-V suffers from a density-of-states bottleneck. Meanwhile, GaSb fails to deliver any improvement in on-current compared to InGaAs, even in the ballistic limit. However, this antimonide could be competitive at a well thickness of 3 nm, thanks to quantization effects that produce changes in carrier mass.

One option for increasing the electron mobility of InGaAs is to introduce strain into this material. However, calculations by Caruso and co-workers show that this only delivers limited benefits up to a strain of 0.5 percent, due to Fermi-level pinning.

A consequence of the low effective mass of electrons in $In_{0.53}Ga_{0.47}As$ is that source-to-drain direct tunneling is more prevalent in these MOSFETs than those made from silicon. "It is expected that source-to-drain direct tunneling can be a major obstacle in downscaling III–V MOSFETs into channel lengths below 20 nm, but our model does not capture this effect and for this reason it is difficult to do some prevision for the design," admits Caruso. To address this weakness, the team is coordinating efforts in a European project involving eight partners, including IBM and Synopsys, that will compare the results of Monte-Carlo and non-equilibrium Green's function models.

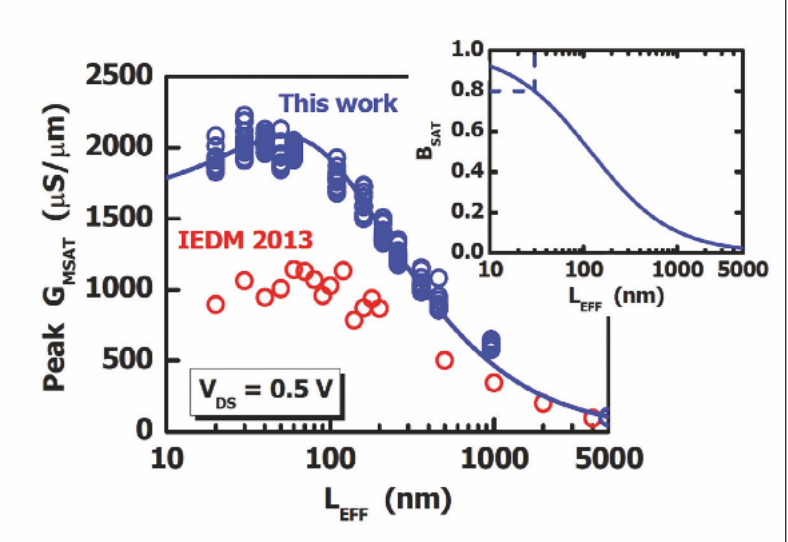
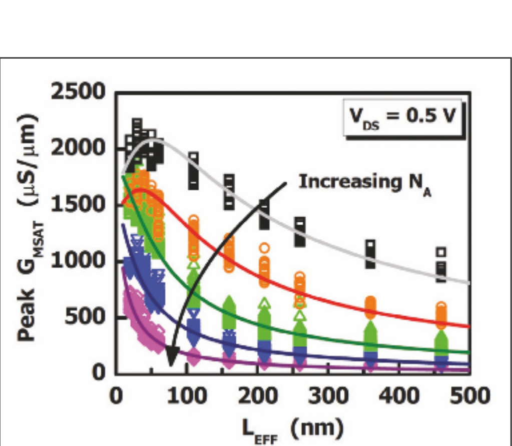


Figure 2. The team from IBM that are based at the T.J. Watson Research Centre in Yorktown Heights have improved their InGaAs channel device during the last twelve months. Results are shown for InGaAs MOSFETs with an effective channel length of 20 nm with channel/barrier doping of 1 x 10^{17} cm^{-3} and a source-drain bias of 0.5 V. The inset is the intrinsic ballistic factor.

Encouraging signs for InGaAs

Another paper offering a more positive view of InGaAs FETs came from a team from the IBM Research Division based at the TJ Watson Research Centre in Yorktown Heights, NY. Corresponding author of the paper, Yanning Sun, told *Compound Semiconductor* that she believes



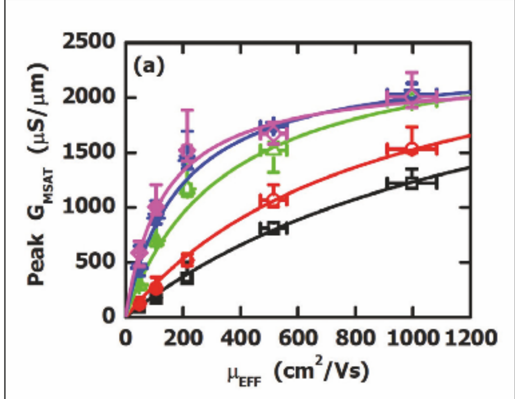


Figure 3. The plot on the left shows that the peak saturation transconductance, GMSAT, falls with increasing channel/barrier doping for MOSFETs with an effective channel length of 20 nm. The plot on the right shows the relationship between peak transconductance and mobility for effective gate lengths ranging from 30 nm to 260 nm.

that one of the most important aspects of the team's work is that it demonstrates self-aligned and scaled III-V devices using device structures and process flows that are CMOS-compatible and manufacturable. Compared to other devices reported in the literature that utilise the least damaging process conditions, but are not CMOS-compatible, Sun claims that the team's devices have performances among the best $In_{0.53}Ga_{0.47}As$ FETs (see Figure 2).

An important, recent finding by the IBM team – based on investigating the impact of barrier and channel doping – is that as gate lengths are reduced below 40 nm, the benefits of a mobility of more than 500 $cm^2 V^{-1} s^{-1}$ get smaller and smaller (see Figure 3). "At the 10 nm node, devices are expected to operate in the quasi-ballistic mode, and we believe that a mobility higher than 1200 $cm^2 V^{-1} s^{-1}$ does not add a significant contribution to device performance," says Sun.

definition, gate patterning, spacer formation, extension implantation and selective source-drain regrowth. "The detailed conditions of some modules certainly need some adjustments, such as etch time and implantation angle, due to the device topography," says Sun.

The IBM team's plan for the future is to improve device performance through a combination of further scaling, greater mitigation of short-channel effects and a cutting of parasitics.

Cutting leakage with InP

Although the last five years have witnessed substantial improvements in the drive current and transconductance of III-V MOSFETs, these devices have been plagued with high leakage currents. This is a major issue for the deployment of this class of transistor in battery-powered applications, because the large losses in standby-mode would have to be combatted with unacceptably short intervals between charging. At the recent IEDM meeting, Cheng-Ying Huang and co-workers from the University of California, Santa Barbara (UCSB), unveiled a new design of III-V MOSFET that slashes the leakage current (see Figure 4).

"Although the last five years have witnessed substantial improvements in the drive current and transconductance of III-V MOSFETs, these devices have been plagued with high leakage currents. This is a major issue for the deployment of this class of transistor in battery-powered applications, because the large losses in standby-mode would have to be combatted with unacceptably short intervals between charging."

The team is yet to make devices as small as this, but it has produced $In_{0.53}Ga_{0.47}As$ channel MOSFETs on InP substrates with effective gate lengths as short as 20 nm. The performance of these devices is better than those it reported at IEDM 2013: Transconductance has doubled, primarily due to the combination of a halving of parasitic resistance, a 50 percent increase in high-field mobility and a 25 percent gain in inversion capacitance. MOSFETs with an effective gate length of 30 nm can produce a peak saturation transconductance in excess of 2200 μS/μm, while sporting an external resistance of just 270 Ω μm, and those with an effective length below 30 nm can operate within 20 percent of the ballistic limit.

It is possible that at some point the team may wish to switch from making planar devices to finFETs. If they decide to do this, the transition should not prove too taxing, because many of the process modules are capable of forming non-planar devices, including the tools used for active-area

"High mobility channels usually result in high leakage due to band-to band tunnelling near the drain, which will eventually limit device scalability," explains Huang. "We addressed how to control the leakage current of the III-V MOSFET at VLSI relevant dimensions, eliminated band-to-band tunnelling leakage using a wide bandgap source and drain spacer, and made III-V MOSFETs feasible for low-power logic applications."

The devices made by the UCSB team are planar MOSFETs with a 4.5 nm-thick InGaAs channel and a doping-graded InP spacer that can realise an off-current of just 60 pA/μm.

Huang explains that these "ultra-thin channel

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devices" are not optimised for low-power because the thin channel has both its pros and cons: It improves electrostatics, but at the expense of inferior electron transport and on-state current.

"For the 7 nm node, we need finFET structures to improve transistor electrostatics," argues Huang. According to him, for low-power and ultra-low-power logic, leakage must not exceed 30 pA/µm and 15 pA/µm, respectively, and in this regime the gate overdrive voltage is mainly on the sub-threshold region. "Improving transistor electrostatics using finFET structures will improve sub-threshold swing, thereby increasing the on-current at a fixed off-current."

To make the MOSFET process compatible with high-volume manufacturing requires a change of substrate and device miniaturisation. "Although our devices are not on silicon and contacts not fully scaled, our process flow uses gate-last and source/drain regrowth processes," says Huang, who points out that for the last few years, gate-last and source/drain regrowth processes have already been used in silicon CMOS processes.

One of the next goals for the team is to fabricate III-V MOSFETs on silicon substrates. In addition, the West-coast researchers are trying to reduce the off-current of the MOSFETs to 10-30 pA/µm, optimise the source and drain spacers, and to increase the on-state current.

Nanowire tunnel FETs

Another form of device that is already capable of exhibiting low leakage currents – and promises to do even better in this regard – is the InGaAs/InAs single nanowire vertical tunnel FET. This class of transistor, which has been fabricated by Xin Zhao and colleagues from MIT, has been formed using a novel III-V dry etch process. At an operating voltage of 0.3 V it has an on-current of 0.27 µA/µm at a fixed off-current of 100 pA/µm.

These results highlight the protential of the tunnel FET, which is to operate at a lower voltage than a MOSFET by realising a sub-threshold swing steeper than the thermal limit of 60 mV/decade. Zhao says that the most important finding detailed in the MIT paper is the identification of a possible leakage mechanism for the tunnel FETs: tunnel-assisted generation that precludes the possibility of achieving a sub-thermal sub-threshold swing.

"This mechanism involves tunneling of electrons into the trap states and subsequent thermal generation of carriers into the conduction band," says Zhao, who argues that it is this mechanism that might explain the temperature-dependence of the sub-threshold current in many tunnel FETs. This leakage results from trap states, particularly at the interface, and it prevents the promise of a sub-thermal sub-threshold swing.

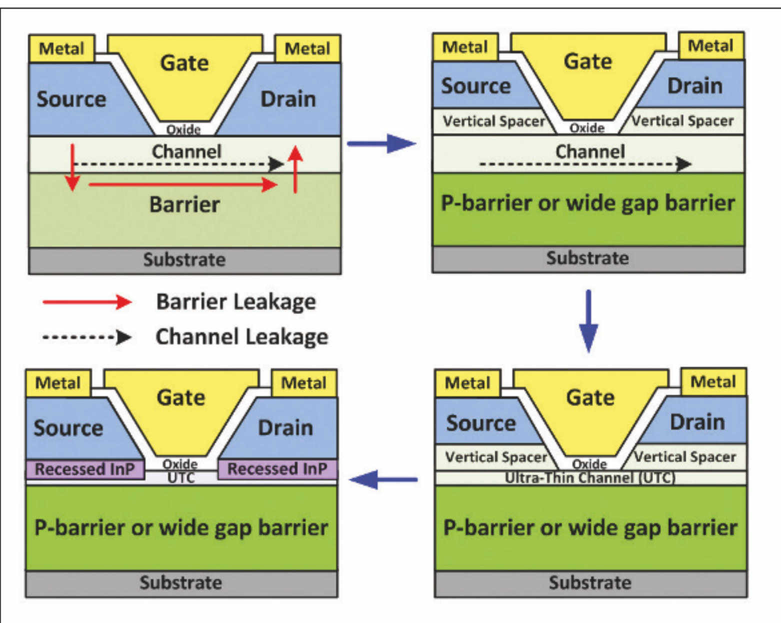


Figure 4. A team from the University of California, Santa Barbara, have developed a design of III-V MOSFET that realises a far lower leakage current, and is thus suitable for low-power applications.

To form their devices, the engineers use reactive ion etching, a technique used in the optics industry to form micron-scale structures with high aspect ratios. "To our best knowledge, our reactive ion etching technology presents the first demonstration of sub-20 nm features with vertical sidewalls in indium-based heterostructures," says Zhao.

Tunnel FETs are a relatively new technology, so there are yet to be any well-established projections for technology nodes for this device. However, Zhao says that he and his colleagues will need to make further improvements in their reactive ion technology, in terms of reduced footing and trenching, if it is to become applicable to the production of devices at the sub-10 nm node. The promise of this device and those of other III-V FETs described in experimental papers at IEDM bodes well for the future of compound semiconductor technologies for future ICs, while the work of some other groups, in particular the calculations presented by Samsung, suggests otherwise.

"The jury is up whether III-V FETs will find themselves in future chips with sub- 10 nm technology nodes," says Zhao, who points out that there are some major challenges that must be overcome, such as the construction of prototype devices with appropriate dimensions. "Theoretical papers have mixed predictions and further efforts of calibration against experiments are needed."

Huang agrees with Zhao, saying that it's not clear whether III-Vs will make an impact. He points out that for this to happen, these new materials will have to deliver a substantial performance advantage, in order to justify the expense of developing a production technology. His view, which is surely shared by many others, is that we will all just have to wait and see how the competing technologies wil evolve over the next couple of years.

Diamond-like carbon enhances GaN HEMTs

Lattice-matched diamond provides a stress-free heat extractor for GaN HEMTs

A TEAM OF ENGINEERS from Taiwan claims to have constructed the first micro-machined GaN power HEMT that incorporates a diamond-like-carbon layer.

"Based on our design, the diamond-like carbon can touch the GaN buffer layer and dissipate the heat directly during device operation," says corresponding author Hsien-Chin Chiu from Chang Gung University, Taiwan.

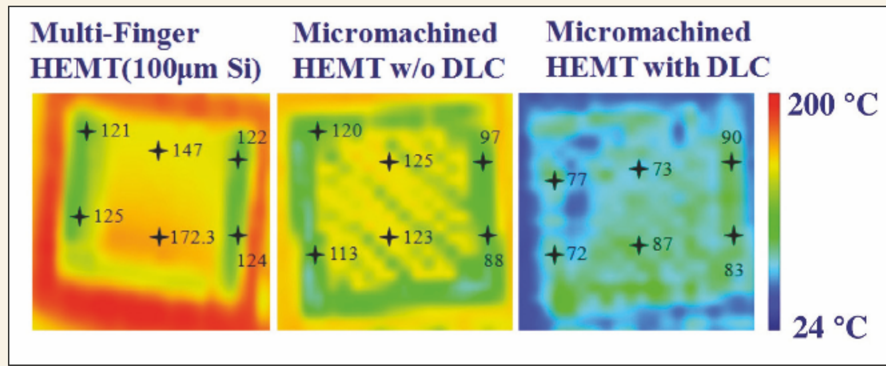
According to him, another benefit of this approach is that the silicon substrate remains beneath the pad of the device. This promises to simplify wire-bond and flip-chip packaging, and ultimately make it easier to produce the devices in high volume.

The diamond-like carbon employed by the team from Chang Gung University, Feng Chia University and RiteDia combines a high thermal conductivity of 600 W m^{-1} K^{-1} with a coefficient of thermal expansion that is similar to that of GaN.

Chiu points out that if the team had instead used pure diamond – an approach that several groups have adopted – they would have then been unable to adjust the coefficient of thermal expansion of this material so that it matched that of GaN. That is a significant issue, because it would have led to devices that were plagued with a large degree of stress at the interface between GaN and diamond. And on top of this, the team would have faced serious reliability and adhesion issues associated with their transistors.

To highlight the benefits of micro-machined diamond-like-carbon HEMTs that the team are pursuing, the engineers constructed this class of transistor and compared its performance to two others: a more conventional multi-finger HEMT, and a micro-machined device that did not have a diamond-like carbon layer.

Fabrication of all three types of devices began with the MOCVD growth on a 4-inch, *p*-type silicon (111) substrate of a 2 μm-thick AlGaN/GaN composite buffer, a 1 μm-thick undoped GaN channel layer, a 18 nm-thick undoped $Al_{0.27}Ga_{0.73}N$ Schottky layer and a 1 nm undoped GaN cap. Reactive ion etching of the wafer created isolated devices, which were given ohmic contacts by electron-beam evaporation. Following a rapid annealing step, engineers added a 100 nm-thick SiO_2 passivation layer, and created devices with a 2 μm gate length and an active area of 1.25 mm by 1.25 mm.



HEMTs can operate at lower temperatures when they incorporate diamond-like carbon (DLC)

Substrate thinning to 100 μm followed, before micro-machined devices were formed with a process that created an air-bridge matrix for improving heat distribution.

Prior to the growth of a diamond-like carbon layer, plasma etching removed the silicon beneath the active region and the partial GaN transition layer.
A diamond-like carbon layer was then added using reactive DC magnetron sputtering, using a deposition rate of 1 Å/s.

To improve adhesion and electrical conductivity, this form of carbon was paired with titanium. The resulting composite had two pairs of diamond-like carbon and titanium layers, with thicknesses of 200 nm and 550 nm, respectively.

Subjecting all three types of device to high electric fields revealed that the buffer breakdown voltage of devices on silicon substrates saturates at around 1100 V, but it is possible to increase this to 1400 V with a micro-machined HEMT featuring a diamond-like carbon layer.

According to the team, these findings indicate that the silicon substrate limits the maximum breakdown voltage of the GaN-on-silicon HEMT.

These engineers also studied current flow between the source and the drain in various types of HEMT, and found that this was highest in the micro-machined device with the diamond-like carbon layer.

They also observed that the carbon film was able to rapidly dissipate the heat at the junction, especially under high gate-voltage operation. Mapping device temperature with an infrared thermographic system revealed that the conventional HEMT with a drain-source current of 1 A and a drain-source voltage of 10 V had a peak surface temperature of more than 170°C.

In comparison, the micro-machined version without the diamond-like carbon operated with a surface temperature of 125°C, while that with diamond-like carbon operated at around 80°C.

Chiu says that the team will now introduce a new power device layout to further improve surface heat dissipation and current re-distribution.

"Then we will cascade this novel device with a low-voltage silicon control device to form a real normally-off GaN power HEMT."

H.-C. Chiu *et. al.*
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Polymer boosts deep-ultraviolet LED output

A robust polymer that is transparent to wavelengths as short as 220 nm can increase the light extraction efficiency of deep ultraviolet LEDs via encapsulation

RESEARCHERS from Japan have identified a suitable polymer for encapsulating deep-ultraviolet LEDs.

This material – polymer perfluoro(4-vinyloxy-1-butene) with a trifluoromethyl end – has almost no absorption at wavelengths greater than 220 nm, so it can be incorporated within an LED and increase the light extraction efficiency of this device. This polymer also appears to be durable, implying that it does not shorten the lifetime of the device.

The team from UV Craftory, Asahi Glass, Nagoya University and Meijo University demonstrated the capability of the polymer by incorporating it in LEDs emitting a peak wavelength of 285 nm and also those operating at 265 nm. At both these wavelengths, the *p*-contact of devices tends to be opaque, so this side of the device is attached to a sub-mount, and emission occurs through the sapphire substrate (see Figure 1). With this geometry, external quantum efficiency increases when a transparent polymer is used to encapsulate the device and fill the spaces between the silver bumps.

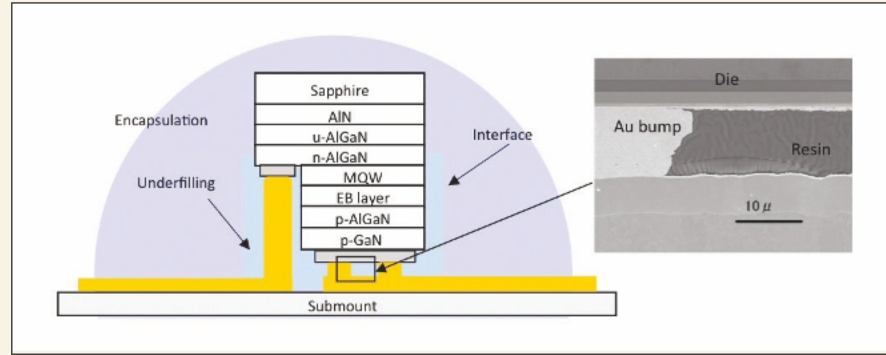

Figure 1. To increase light extraction, ultraviolet LEDs are encapsulated and underfilled with transparent polymers (also known as resins).

Corresponding author Akira Hirano told *Compound Semiconductor* that although underfilling and encapsulation processes are more complex when using this polymer than conventional resins, they still have the potential to be employed in a high-volume manufacturing environment. In his opinion, in future it might be possible to produce packaged LEDs incorporating this polymer for "several US dollars".

To assess the performance of deep ultraviolet LEDs with various fillers, the engineers encapsulated and underfilled devices with their transparent polymer, and also another variant of perfluoro(4-vinyloxy-1-butene): This has a carboxylic acid end, and starts to absorb light at wavelengths below 280 nm.

Bare 265 nm and 285 nm chips with dimensions of 800 μm by 800 μm were underfilled with both forms of the polymer, and then dies were overcoated to isolate them from the ambient atmosphere.

Driven at 20 mA, the 265 nm LED enshrouded by the polymer with a carboxylic acid end short-circuited after 95 hours of operation. Meanwhile, the device featuring the polymer with a trifluoromethyl end did not short circuit after running for 1,033 hours (see Figure 2).

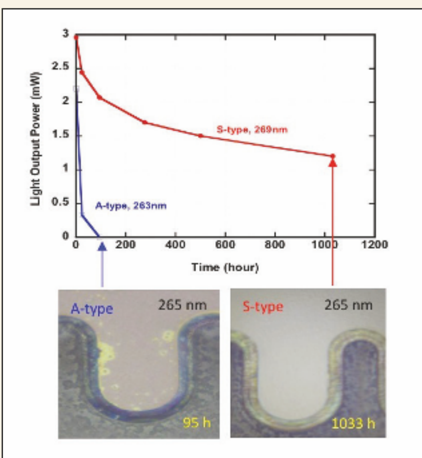

Figure 2. Easily visible damage has occurred to the ultraviolet LED enshrouded with the perfluoro(4-vinyloxy-1-butene) polymer with a carboxylic acid end. Switching to a trifluoromethyl end leads to a far more robust polymer.

The team inspected both these LEDs under a microscope. They saw no visible change in the polymer with the trifluoromethyl end after 1,033 hours of operation, but observed a significant colour change in the LED with the other polymer – and also its cousin emitting at 285 nm.

Hirano and his colleagues also assessed the robustness to heat of these LEDs. Bubbles were only seen in the device featuring the polymer with the carboxylic acid end, and they were spotted after this LED had been twice heated to 230°C for 30 minutes, suggesting that this material underwent photochemical decomposition. This led to the generation of CO, CO_2 and water, according to mass spectroscopy.

Energy-dispersive X-ray spectroscopy has also been used to scrutinise the samples, with a strong nickel spectrum detected between the *n*- and *p*-electrode pads in the short-circuited sample. It is believed that this resulted from diffusion of metal between these two pads.

According to Hirano, the team's next goal is to modify the chip design so that it delivers optimal results following encapsulation.

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