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Volume 22 Issue 3 April / May 2016 @compoundsemi www.compoundsemiconductor.net

The precarious promise of 5G

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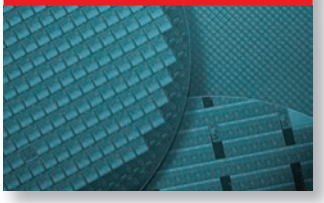

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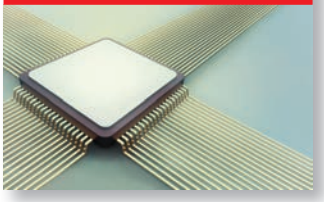

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editorial view

by Dr Richard Stevenson, Editor

5G uncertainty

THERE ARE PLENTY of good reasons for the rolling out of 5G. There is the need to accommodate the rocketing rise in wireless data, driven by increasing use of Netflix, iTunes and other applications involving the Cloud. And there is also the need to support the growth of the internet-of-things, and to help to usher in the era of machine-to-machine communication.

Given these compelling arguments for deploying 5G, one would expect to see a well-defined roadmap for this technology. But that's not the case. Great uncertainty surrounds 5G – even such fundamental specifications as the operating frequency and bandwidth are still to be defined.

This state-of-affairs is highly frustrating for many in the RF industry, including III-V chipmakers. With no specifications to target, how can one develop a front-end module for a 5G-compatible handset, or a base station amplifier providing 5G coverage?

Fortunately, there is still a little time left to resolve these issues. Roll-out of 5G is not slated to begin until the end of this decade, and as networks come under increasing strain from growth in wireless data traffic, minds will focus on the need to define the details of this next-generation technology.

What could really help the future of 5G is a successful showcasing of this technology at a high-profile, global event, such as the Tokyo 2020 Olympics. If it goes well, it could kick-start substantial deployment. But if the 5G demonstration is beset by problems – possibly due to premature release of products that could have been avoided by setting specifications earlier – the roll-out may struggle to gain momentum.

There is another cause for concern that has been raised in a recent survey of mobile operators: more than three-quarters of them have no plans for 5G deployment, primarily because of a lack of a clear return-on-investment.

The silver lining is that even if the successor of 4G is merely some form of 4G-on-steroids, which might go by the name 4.5G, it will still be good news for the makers of compound semiconductor chips. That's because demand for high-efficiency, high-linearity PAs for mobiles will aid sales of GaAs HBTs, and could even see the introduction of InP-based devices; and base-stations will benefit from powerful, efficient GaN devices.

To find out more about all these issues, take a look at the feature "The Quest for 5G" on page 36.

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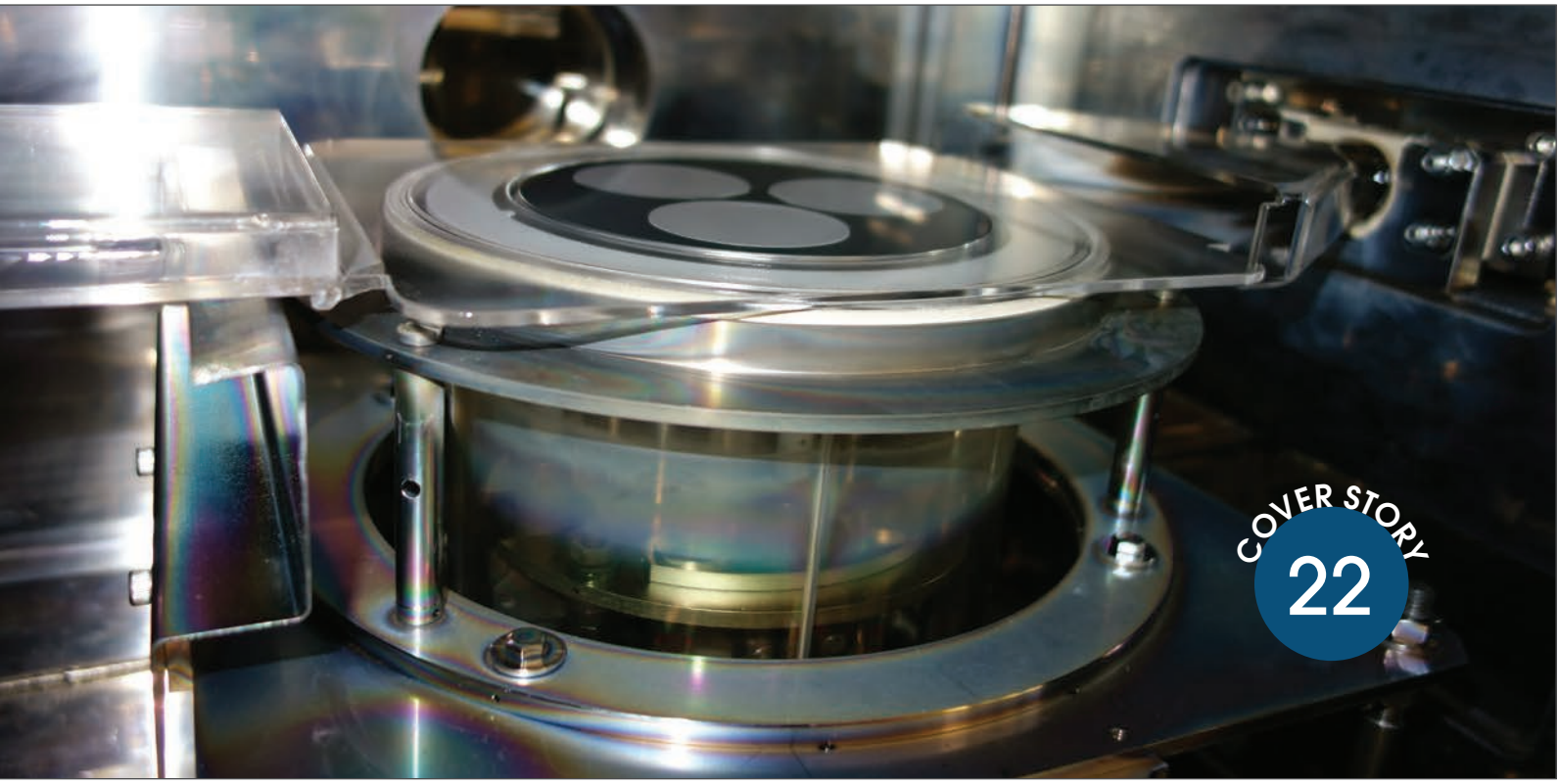

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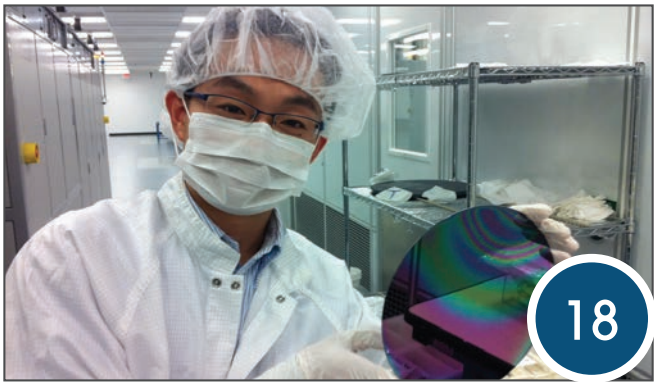
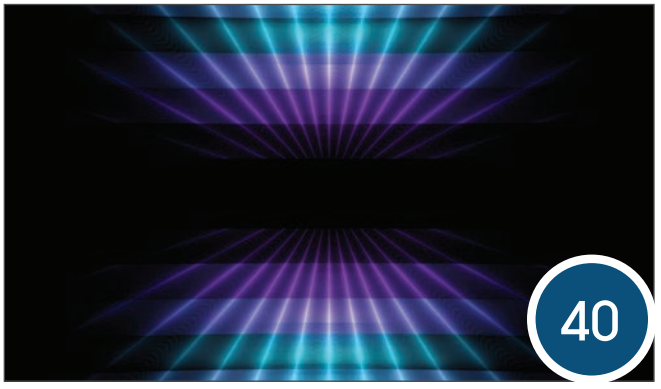
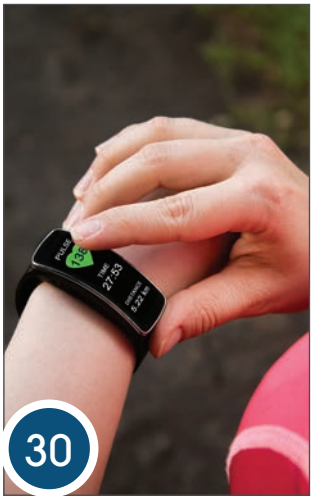
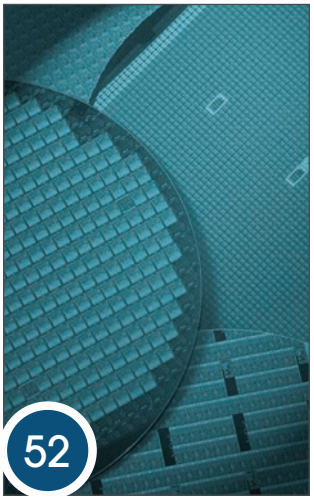








2015: Another tough year for packaged LEDs

WHEN IT COMES to pricing and market expectations, 2015 was obviously another tough competitive year for packaged LED vendors, with challenges in both backlighting and lighting, writes Jamie Fox, IHS Technology's principal analyst for Lighting and LED, in his latest analysis and commentary on packaged LED company rankings.

The US dollar was much stronger in 2015 than 2014: against almost every major currency, which largely explains why packaged LED revenue fell so much last year. When measured in Yen and Euro, the packaged LED market grew 5 percent and 10 percent, respectively. (Had exchange rates remained the same as they were in 2014, the market would most likely have been much flatter measured in US dollars.)

As global LED revenue declined 8 percent in 2015 Lumileds was the only LED manufacturer ranked in the top ten to record positive growth in 2015, gaining share as well as ranking position. Even though the company suffered significant uncertainty last year, as Philips attempted to sell the business, Lumileds managed to come in ahead of Samsung every quarter since the fourth quarter of 2014.

Lumileds continues to offer a strong competitive position in automotive LED, general lighting, and mobile camera flash categories, and the company's

market share continues to benefit from having only a small position in the soft backlighting market, which includes mobile phones, notebooks, tablets and monitors.

Revenue share for Cree, LG Innotek and Everlight declined in 2015 compared to the previous year; however, Everlight improved its ranking position, while the others did not.

Everlight's rise comes despite losing share, because Cree and LG Innotek revenues fell even further.

Cree and the major Korean players all experienced double-digit revenue declines in 2015.

Cree is increasingly focused on its lighting business, as the company's component business is no longer growing as quickly as it once was. Cree has long positioned itself - with some justification - as a higher quality vendor than others.

While this strategy has suffered as the market has commoditised, Korean companies managed to position themselves successfully as the low-cost option in general lighting in 2012 and 2013. Even so this strategy faced difficulties in 2014 and 2015, as MLS and other Chinese companies offered even lower prices with similar quality.

In 2015 Samsung, LG Innotek and Lumens were caught in the middle - offering neither the lowest price nor the best quality - with no obvious business strategy to address the issue. Seoul Semiconductor is a pure-play LED company that is committed to the market and has more experience in LEDs than the other major Korean players.

While the company gained share in 2015, revenue declined slightly. Nichia, Osram Opto and MLS all maintained their share in 2015, declining slightly in revenue in line with the market.

Consortium integrates laser on silicon with modulator

IRT Nanoelec, an R&D consortium focused on communication technologies using micro- and nanoelectronics, has announced the co-integration of an III-V/silicon laser and silicon Mach Zehnder modulator, using direct wafer bonding. The team has demonstrated 25 Gbps transmission on a single channel, a rate usually achieved using an external source over a 10 km single-mode fibre.

Current interconnect technologies, which use micro-optics integration to assemble a discrete laser and a silicon photonic circuit, will soon reach their limits and new, different solutions will have to be found to handle increasing traffic, according to the researchers. Integrating photonics capabilities on silicon chips will vastly increase bandwidth, density and reliability, while dramatically reducing energy consumption.

In the age of photonics-on-silicon, data transmission will be measured in terabits per second. To achieve these recent results, silicon photonics circuits integrating the modulator were processed first on a 200 mm SOI wafer, although 300 mm wafers also could be used in the near future.

Then, a two-inch wafer of III-V material was directly bonded on the wafer. In the third step, the hybrid wafer was processed using conventional semiconductor and/or MEMS process steps to produce an integrated modulator-and-laser transmitter.

"Jointly obtained by STMicroelectronics and Leti in the frame of the IRT Nanoelec cooperation, these results, especially fabricating the laser directly on silicon, demonstrate IRT Nanoelec's worldwide leadership in III/V-on-silicon integration to achieve high-data-rate fiber-optic modules," said Stéphane Bernabé, project manager.

"IRT Nanoelec and its partners on this project, Leti, STMicroelectronics, Samtec and Mentor Graphics, are paving the way to integrating this technology in next-generation transceivers for optical data links."

SiC amplifier achieves 200 gain at 400° C

RAYTHEON UK and Newcastle University have produced SiC-based amplifier circuitry with op amp-like characteristics that has demonstrated high-temperature gain of 200 at 400°C. Once integrated and packaged into a single device, the amplifier has the potential for use in monitoring and closed-loop control circuitry applications within a variety of harsh-environment industries, such as aerospace, oil and gas, geothermal energy and nuclear, says Raytheon. "To date, the focus on SiC semiconductors has been power electronics and exploiting the material's ability to dissipate internally generated heat," says Alton Horsfall, reader in Semiconductor Technology at Newcastle University.

"For this project though we've focussed on creating circuitry that can operate in high temperature and other harsh environments. This could therefore lead to condition monitoring circuitry mounted on gas turbines or within the primary coolant loop of a nuclear reactor, which runs at about 350°C," he adds. At the heart of the amplifier circuit is a lateral small-signal junction field-effect transistor (JFET). According to the researchers, this offers a significant improvement in reliability in hostile environments, because of the lack of a gate oxide layer.

A greater stability in the threshold voltage and a reduction in the intrinsic noise, make these structures suitable for the realisation of high-temperature, low-noise amplifier circuits. The current circuit is a fully differential, three-stage amplifier, with a source follower final stage, optimised to operate on a ±15 V supply. Modifications enable voltage supplies of ±45 V to be used to increase the voltage headroom of the circuit.

Laboratory tests have shown that the amplifier circuit has an open-circuit gain in excess of 1500 at room temperature. A high-temperature gain of 200 has been recorded at 400°C, but this is limited by the passive components used in the circuit. The recent monolithic integration of the amplifier into a single chip should deliver the kind of op amp capabilities with which electronics engineers the world over are familiar, says Raytheon.

"Though we're not the only ones to be exploring the suitability of SiC for control and monitoring applications in harsh environments, we believe this amplifier circuit represents the furthest anyone has gone down the lab-to-fab route," states Phil Burnside, business development manager of Raytheon UK's Semiconductors Business Unit.

"In this instance, it is Newcastle University's design expertise and understanding of harsh environments, combined with our SiC processing expertise, that have the potential to result in the full commercialisation of a high-temperature version of a fundamental electronic building block, the humble op amp."

Raytheon will have a technical demonstrator of the amplifier circuit at Power Conversion Intelligent Motion (PCIM) Europe 2016 in Nuremberg, Germany (10-12 May).

EPC announces 15MHz half-bridge demo boards

EPC has introduced the EPC9066, EPC9067, and EPC9068 15 MHz Half-Bridge development boards, which are configurable to a buck converter or as a ZVS class-D amplifier. These boards are said to provide an easy-to-use way for power systems designers to evaluate the performance of GaN transistors, enabling the designers to get their products into volume production quickly.

All three boards feature a zero reverse recovery (QRR) synchronous bootstrap rectifier augmented gate driver to increase efficiency at high frequency operation, up to 15 MHz. The boards can produce a maximum output of 2.7 A in the buck and ZVS class-D amplifier configurations. Loss reduction is realised across the entire current range.

The EPC9066/67/68 feature 40 V, 65 V, and 100 V-rated eGaN FETs respectively. These boards are 2-inch x 1.5-inch and are laid out in a half-bridge configuration. Each board uses the Texas Instruments LM5113 gate driver with supply and bypass capacitors. The gate driver has been configured with a synchronous FET bootstrap circuit featuring the 100 V, 2800 mΩ EPC2038 eGaN FET, which eliminates the driver losses induced by the reverse recovery of the internal bootstrap diode.The boards have various probe points and Kelvin measurement points for DC input and output. In addition, the boards provide the capability to install a heat sink for high power operation.

Cree high density LEDs double lumen output

CREE has introduced the XLamp CXB1310 and CXB1520 High Density LED arrays, which are said to deliver the highest lumen density at 6 mm and 9 mm - the most lumens in the industry for their LES [light emitting surface] sizes.

Incorporating elements of Cree's SC5 Technology Platform, the new LEDs will enable new and differentiated LED lighting form factors for applications like track lights, lamps and downlights.

For example, the CXB1520 LED packs the lumen output of seven 60 watts replacement lamps into an area much smaller than a dime, allowing lighting manufacturers to put more light where it is intended at a lower system cost.

"The CXB1310 High Density LED array delivers an impressive amount of light in a small package," said Massimo Parravicini, R&D director of Reggiani Illuminazione. "The high lumen density of the CXB1310 LED will allow us to offer LED designs with performance and form factors previously impossible."

The high performance of the CXA2 High Density LED arrays allow lighting manufacturers to reduce thermal, mechanical and optical costs at the system level. For example, when combined with a 74 mm diameter optic, the 3000 K, 80 CRI CXB1520 High Density LED array delivers over 50,000 candela in a 10-degree beam while drawing only 40 watts. This high lumen density allows lighting manufacturers to deliver the performance of a 70 W ceramic metal halide (CMH) PAR38 lamp through a much smaller PAR20-size optic using 43 percent less power. The CXB1310 High Density LED array delivers up to 3,200 lumens in a 6mm LES, allowing similar reductions in size and power from traditional light sources.

"The CXB1520 High Density LED allows us to deliver downlights that provide up to 2700 lumens with just 28 watts in a very small 4 inch trim platform. What was previously only possible in much larger platforms with much higher wattage requirements is now made possible in our VF Series Specification Grade Luminaire Downlight product line using Cree's CXB1520 High Density LEDs," said Justin Weaver, VP engineering, LF Illumination."The very high efficacy of the CXB1520 High Density LED also allows us to move many of our products that at one time were only possible with active cooling solutions to passive solutions, simplifying our design and lowering our system costs significantly."

Cree XLamp CXA2 High Density LED arrays are characterized and binned at 85˚C, available in 2-, 3- and 5-step EasyWhite colour temperatures 2700 K - 6500 K), and CRI options of 70, 80 and 90.

GaN RF market to double over next five years

GAN RF DEVICES market will double over the next five years, led by GaN's adoption across various market segments, according to Yole Développement in its 'GaN RF Devices Market: Applications, Players, Technology, and Substrates 2016 - 2022' report.

In 2015, there was a large increase in wireless infrastructure market sales driven by the massive adoption of LTE networks in China. By the end of 2015, the total RF GaN market was close to $300 million. Sales will likely not soar as high over the next two years, but growth will continue, according to Yole, mainly driven by increased adoption of GaN technology in the wireless infrastructure and defence markets.

A significant boost will occur around 2019 - 2020, led by the implementation of 5G networks. Market size will be multiplied by 2.5 by the end of 2022, posting a CAGR of 14 percent from 2016 - 2022.

Wireless infrastructure, now representing more than half of GaN's total market, will grow at expected 16 percent CAGR for 2016 - 2022. Though GaN was originally developed to support governmental military and space projects, we'll soon be able to say that mainstream commercial markets have fully embraced this novel technology.

GaN's increased implementation in base stations and wireless backhaul stems from the growing demand for data traffic and higher operating frequencies and bandwidths.

In future network designs, new technologies like carrier aggregation and massive MIMO will actually put GaN in a superior position compared to existing LDMOS. GaN products have not yet covered the wireless infrastructure market's full spectrum, and we see more opportunities in the higher-frequency range.

University of Bath installs Eulitha Phable 100

Eullitha, a Swiss startup company offering lithography equipment and services for the nanotechnology, photonics and optoelectronic markets, has announced the installation of one of its Phable 100 photolithography systems at the University of Bath, UK.

The Phable 100 exposure tool incorporates Eulitha's proprietary Displacement Talbot Lithography technology that enables robust printing of high resolution periodic patterns at low-cost. The system was purchased by the university as part of a comprehensive research program designed to develop advanced manufacturing techniques for nano- engineered semiconductors, particularly GaN.

The purchasing of this innovative system was made possible following the award of a 5-year, £2.7 million grant from the UK Engineering & Physical Sciences Research Council (EPSRC) as part of the council's Manufacturing of Advanced Functional Materials funding programme (www.ManuGaN.org).

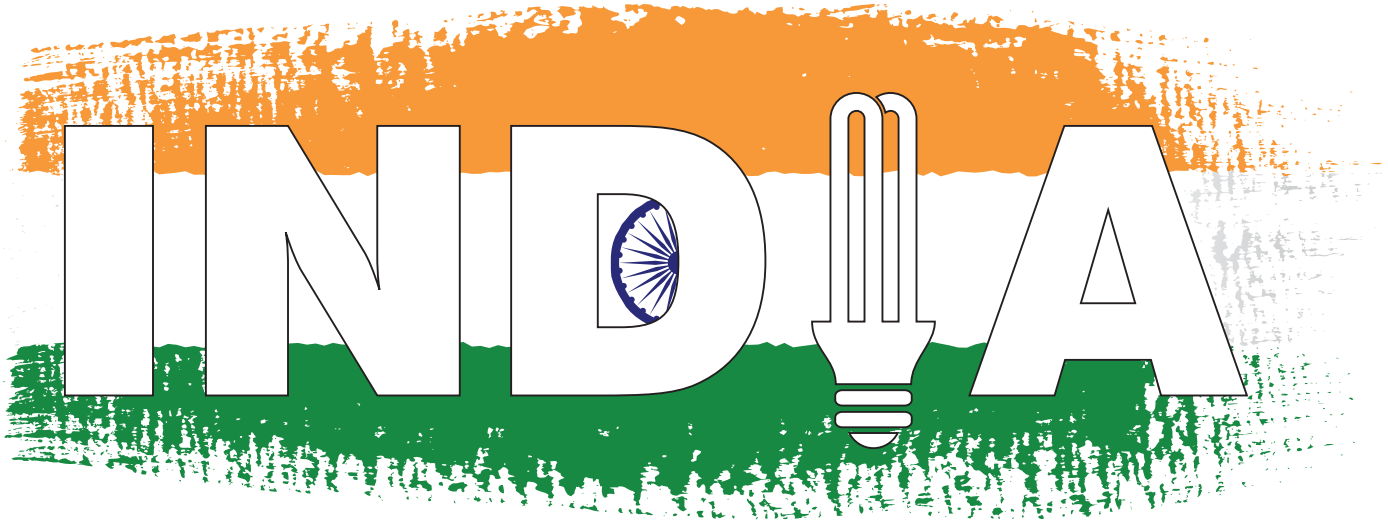
The university has been active in GaN semiconductor research since 1999 and has an excellent reputation for combining nanofabrication techniques with semiconductor growth in order to improve the performance of optoelectronic devices such as LEDs. As a result of the EPSRC investment, researchers in the Department of Electronic & Electrical Engineering now have access to a new nanolithography suite within the David Bullet Nanofabrication Cleanroom, of which the Phable tool forms part, alongside the existing access to crystal growth reactors and more conventional fabrication facilities. The Phable 100 tool was chosen as it offers the unique capability to pattern large areas up to 100mm in diameter with high fidelity in a very simple way. Its capability will be compared with another low-cost patterning technique, nanoimprint lithography as part of the research.

Lead researcher and Lecturer in the Department of Electronic and Electrical Engineering, Philip Shields, said: "We are very excited to have this new capability at Bath. Initial results from the tool have matched and even exceeded our expectations. There has been a lot of interest from other researchers to use the tool and we look forward to developing new research collaborations as a consequence."

Harun Solak, CEO of Eulitha, said: "We are very pleased by the choice of the University of Bath especially because their research program focuses on manufacturing technologies for nano-engineered semiconductors which is an area where our innovative technologies have the potential to make a significant impact."

The Phable 100 system is capable of exposing periodic patterns down to feature sizes below 150nm which rivals much more expensive high-end i-line steppers, according to the company. The patented focus-free imaging technology used by the system enables uniform printing on non-flat samples often found in photonic and optoelectronic sectors.

Eulitha had recently announced the delivery of further lithography systems to the Twente University in the Netherlands and CIOMP institute in China.



Let there be LED light

Is the Government of India's ambition to supply a $0.65 LED bulb to the masses feasible, asks Rebecca Pool.

IN JANUARY 2015, the Government of India unveiled an ambitious programme to thrust LED bulbs into the limelight by offering the energy efficient devices at a fraction of the market price.

Spearheaded by Energy Efficiency Services Limited, a joint venture of state-run power companies, the scheme has already flooded the nation's homes with millions of cheap 60 W equivalent LED bulbs. And more is to come.

As part of a competitive bidding process, EESL procures millions of LED bulbs from manufacturers and then sells the devices to households at a reduced price through power distribution companies.

These companies then repay EESL the difference from the savings accrued from the use of more efficient lighting.

And to date, the scheme has met with resounding success. Just months after starting, some ten million bulbs were installed across the nation, and today this figure has reached 54.2 million units.

Come Spring, the government intends to hit a 100 million LED bulb installation target, with a view to totally wiping out each and every one of the nation's hundreds of millions incandescent bulbs by 2018. Indeed, *The Times of India* recently reported how vans are being dispatched to the nation's more remote regions to promote LED bulb use.

Price-wise, the scheme has reached unprecedented depths. Following its first bidding round, EESL procured some 0.75 million LED bulbs that were then sold for around $4.50.

But in the latest round of June last year, 50 million bulbs were procured with prices bottoming out at $1.10 per unit – dipping well below the government's $1.50 per unit target. And EESL is now intent on pushing the price down to a mere $0.65.

But is a $0.65 LED bulb realistic? For Bangalore-based IHS lighting and LED analyst, Swapna Prakash, the answer is yes.

As he points out: "Since the first bidding process of January 2014 we have seen a decrease in price of around 75 percent and I am certain we will continue to see this."

According to Prakash, India is a net importer of energy and the government's

basic objective right now is to save energy. Clearly replacing all incandescent light bulbs with LED bulbs by 2018 is once clear route to doing so.

"Our LED bulb market is very price sensitive and from the outset we never realised the government would take so many approaches to procure LED bulbs," he says. "Two years ago consumers would pay around $10 for a single LED bulb but we've been seeing continuous decreases in prices and realistically we will see this $0.65 goal being achieved within the next couple of biddings."

And with the next bidding round expected to take place by the end of this year, this goal could be reached as early as 2017. But where exactly are EESL's LED bulbs coming from?

According to Prakash, LED bulb players from around the world enter EESL's competitive bidding process, from Western-based businesses Philips and Osram to home-grown firms including industry heavyweights Crompton Greaves, Mumbai, Havells of Uttar Pradesh, Mumbai-based Bajaj Electricals and Wipro of Bangalore.

Recently Philips, Havells, and Surya Roshni of Delhi have all ramped up production to keep pace with the government programme.

Meanwhile Orient Electric, India, has vacated incandescent bulb manufacture and shifted half of its assembly lines from compact fluorescent lamps to LEDs. The New Delhi-based lighting manufacturer also recently launched its own campaign urging Indian households to switch to LED lighting.

"Manufacturers from China and Taiwan have huge economies of scale, and to compete many India-based companies and other foreign chip makers will have to increase economies of scale to achieve the necessary reductions in cost," highlights Prakash. "The selling price is still coming down."

Crucially, Prakash asserts the LED bulbs bought through the EESL scheme are not only cheap but also perform.

"Consumers are certainly concerned by performance and EESL sets quality benchmarks to make sure there is no compromise in standards," he says. "[The organisation] has set technical standards for self-ballasted 7 W LED lamps for domestic use and all bidders provide a three-year replacement warranty certificate for every batch of bulbs."

"Bidders also submit test certificates from certified labs for the parameters set by EESL," he adds. "And in most cases the lumen intensity and brightness is better than a 60 W incandescent lamp."

So, with the next bidding round due within months, industry can only wait to see what price the next wave of EESL-procured LED bulbs come in at. In the meantime, the organisation is also promoting the retrofitting and maintenance of LED street lighting.

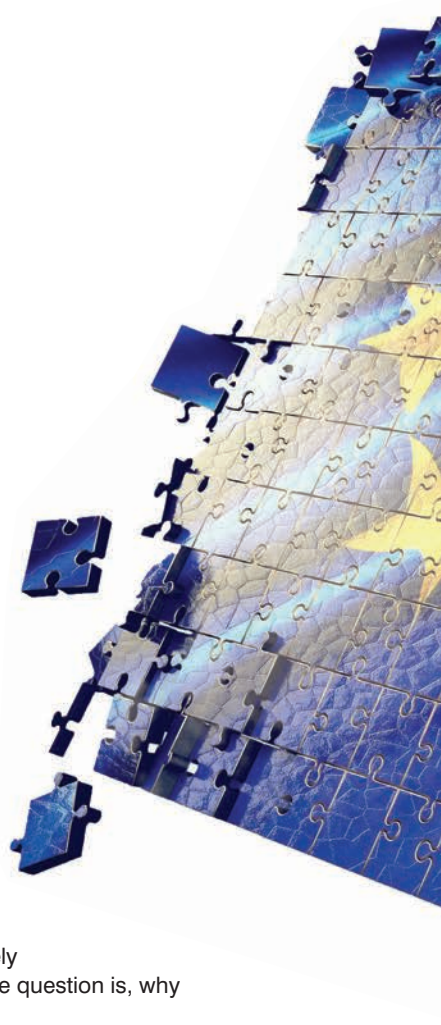
And in a new move, EESL recently clinched a deal with India's massive online marketplace, Snapdeal, to distribute 9 W LED bulbs at $1.50.

As Prakash says: "Snapdeal has a huge online presence in India and this deal will enable the Ministry of Power to further increase its distribution of LED bulbs and help to realise its goal of an energy efficient India."

Below: Government procures LED bulbs and then provides them to consumers at a lower price. Credit: Geoffrey Landis

EU referendum: in or out?

With the UK's decision on whether to leave the European Union looming, Rebecca Pool asks key industry players how they will vote.



WITH ONLY weeks until the European Union referendum and the 'Remain' and 'Leave' campaigns neck and neck, many businesses across the UK are making strong economic cases to stay in the EU.

A recent poll from CBI revealed 80 percent of its members, of which 71 percent were SMEs, believe 'in' will be best for business. At the same time, the UK employers' lobby group warns a vote to leave would cost UK economy £100 billion and 950,000 jobs by 2020.

"Even in the best case, [Brexit] would cause a serious shock to the UK economy," asserts Carolyn Fairbairn, CBI Director-General. "Without a free trade deal, 90 percent of British exports to the EU, by value, could face tariffs....and products imported from the EU into the UK could also face tariffs."

UK-base compound semiconductor industry players concur. As Michael Le Goff, chief executive of Plessey, told *Compound Semiconductor*: "The referendum does matter to the company and is a complete distraction and unnecessary risk that the government should not be taking at this time."

"There are no pressing issues here other than the British Conservative Party's own internal political objective," he adds.

Likewise, Jill Shaw, chief executive of Anvil Semiconductors, reveals concerns, saying: "The result of the referendum is very important and the uncertainty that would follow a Brexit could be a killer."

Indeed, in recent weeks, myriad UK businesses have raised concerns over potential impacts of a Brexit decision, including UK trade barriers, rising unemployment and a reduction in GDP.

Siemens chief financial officer, Maria Ferraro, recently stated: "It took seven years for Canada to negotiate their EU trade agreement. Investment wouldn't cease, but it would take time for stability to return and the UK to be an attractive place to invest."

For both Shaw and Le Goff, the economic fallout that could follow a Brexit decision is a massive worry. As Shaw highlights: "This result may be better for the UK in the long term – although I don't believe this – but the impact on Anvil in the first two years would be significant."

And likewise, Le Goff states: "The issues post a referendum [decision to leave] are completely unknown and that is the risk. The question is, why take this risk at this time?"

Yet amid the risk, distraction and uncertainty, industry players have yet to see any negative impacts on business.

As Le Goff puts it: "We attended the recent 'Light+Building 2016' conference in Frankfurt, the largest lighting show in the world, and no-one was discussing the upcoming referendum."

And Shaw speaks of a similar experience: "I've not noticed [any effects on business] that can be put down to current referendum uncertainties, except perhaps the weakness of Sterling."

"As a company with a number of European suppliers, this weakness against the Euro is really hitting our finances," she adds.

Questionable funds

For Shaw, the severed European partnerships that could follow a Brexit decision, are a thorny issue. "As a start-up, connections with European companies are key, as is access to European grants," she says.

And the Anvil Chief executive's apprehensions over the future of EU research, in the advent of a 'leave' decision, are echoed

across the industry. Earlier this month, Cardiff-based IQE stood up for the CBI and highlighted the crucial role that Europe has to play in developing and commercialising emerging technologies.

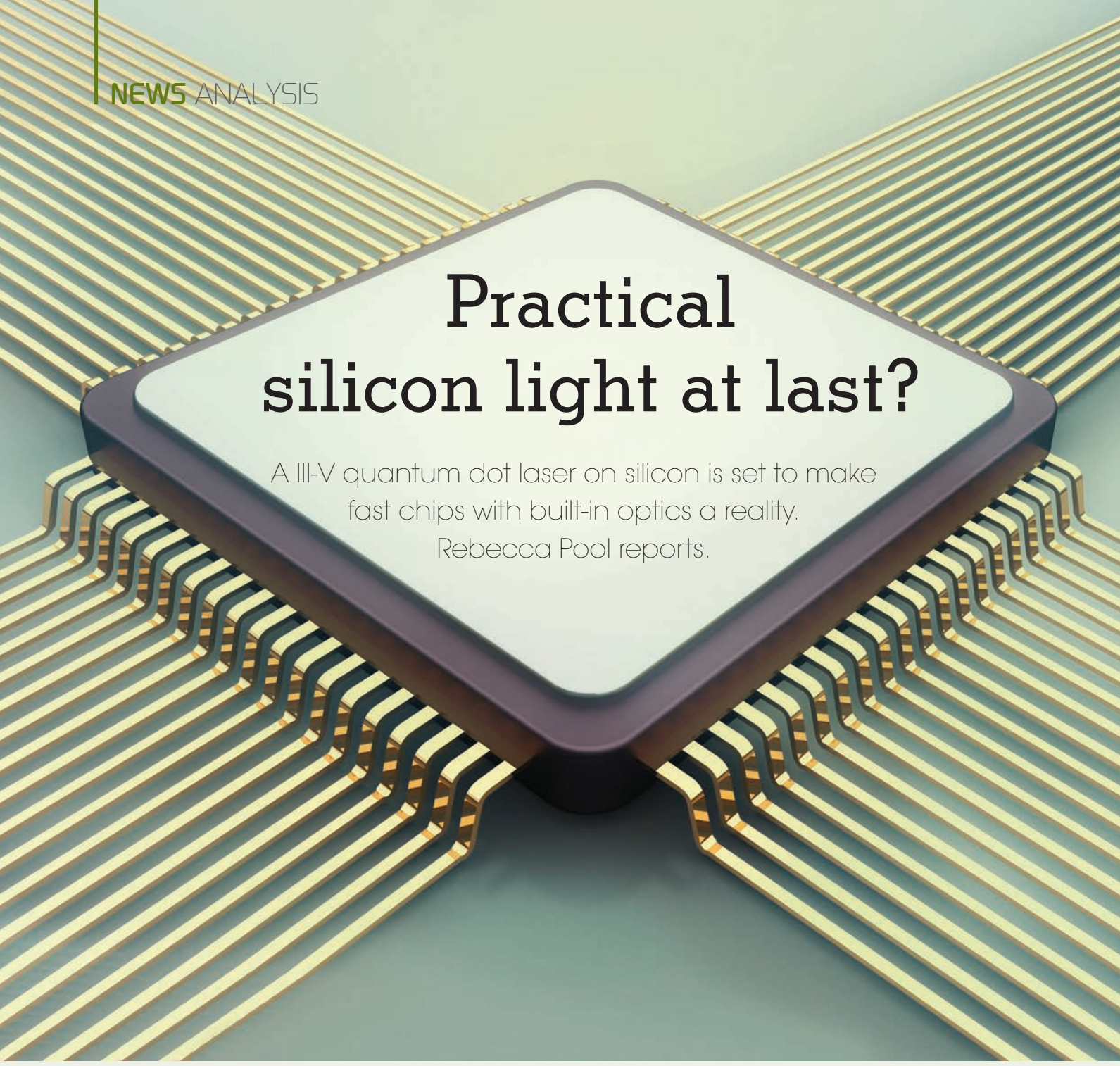
Pointing to numerous pan-European initiatives, including Horizon 2020, ECSEL pilot line initiatives, Photonics 21 and more, IQE head of open innovation, Chris Meadows, says: "Europe has strong ambitions to reshore major high technology manufacturing from other parts of the world."

"This requires a cross-border coordinated industrial strategy, involving major players across Europe," he explains. "If the UK chose to leave the EU, it would be largely isolated from these initiatives, and much poorer for not playing a significant role."

But while IQE clearly supports continued membership of the EU, Meadows is perhaps less concerned over a Brexit decision than industry peers.

"IQE trades within and outside of Europe, with Asia and the US being the Group's dominant markets, so the results on the 23rd June is unlikely to have any short-term impact on our business," he says.

"[And] while a Brexit would inevitably affect European funding mechanisms and support for UK businesses, its impact on collaborations may be less if effective trade agreements are in place, as is the case for non-member states," he concludes.



Practical silicon light at last?

A III-V quantum dot laser on silicon is set to make fast chips with built-in optics a reality. Rebecca Pool reports.

EARLIER THIS YEAR UK-based researchers revealed the first practical, electrically-driven 1300 nm quantum dot laser grown directly on a silicon substrate, paving the way to the full integration of photonic and electronic circuits.

With an overall performance to rival III-V quantum well lasers and III-V quantum dot lasers on GaAs and SiGe, the continuous wave InAs/GaAs laser has a low threshold current, room temperature output power exceeding 105 mW and operation up to 120°C.

Crucially, with more than a mighty 3100 hours of continuous wave operating time collected, Huiyun Liu from University College London (UCL) and colleagues reckon the mean time to failure of the devices will be more than 100,000 hours.

"Other photonics components have evolved and the silicon laser is the last challenge to be realised for reliable and cost-effective silicon-based photonics-electronic integration," highlights Liu. "Our demonstration opens up new possibilities for silicon photonics and the direct integration of optical interconnects on silicon microelectronics platforms."

According to Liu, the breakthrough follows six years of research, during which time he and colleagues have focused on producing high-quality GaAs-on-silicon layers, via MBE, with a low defect density.

Lattice mismatch and incompatible thermal expansion coefficients between III-V materials and the silicon substrate lead to threading dislocations, which have stifled the monolithic growth of III-V lasers on silicon.

So, with this in mind, the researchers combined an AlAs nucleation layer and InGaAs/GaAs dislocation filter layers with *in situ* thermal annealing to minimise dislocation development.

As Liu points out, the thin AlAs nucleation layer deposited on the silicon wafer first provided a good interface for subsequent

III-V material growth. Three GaAs layers were then grown onto the nucleation layer, confining most defects to the first 200 nm of the structure.

Super-strained dislocation filter layers were grown on top of a GaAs buffer layer, which enhanced lateral motion of the threading dislocations that had formed, increasing the probability of dislocation annihilation.

MBE growth was then paused to anneal these layers, again enhancing dislocation movement and annihilation.

Liu reckons these processing steps reduced dislocation density to the order of 10^5 cm^{-2} – compared to around 10^{10} cm^{-2} at the GaAs/silicon interface – with a standard five-layer quantum-dot laser then grown on top of these layers.

But for Liu, the most crucial step to achieving the laser has been to use quantum dots. As he points out, thanks to carrier localisation, quantum dots have proven to be less sensitive to threading dislocation defects than quantum-well structures.

What's more, quantum dots can either pin or propel a dislocation away, with an array of quantum dots generating a strain field that prevents dislocation motion.

As the researcher says: "Any defects in the III-V layer of a quantum-well device will grow over time, so while you might get a laser, you will not get the long lifetime to go with it."

"But for a quantum dot laser, dislocations in its active region may destroy a few quantum dots, but the massive majority will remain active and able to provide optical gain, giving you a much longer lifetime," he adds.

And with an extrapolated lifetime of more than 100,000 hours, at least double that of quantum well lasers developed by other research groups, the scheme appears to have worked.

Silicon photonics integration

From the silicon photonics' industry perspective, the fact that Liu's III-V laser is grown directly onto a silicon substrate is the key breakthrough, opening the door to the use of silicon lasers as optical interconnects on microelectronics chips.

In the past, high performance quantum dot lasers have been successfully demonstrated on germanium-on-silicon substrates, offering an indirect route to III-V and silicon integration.

But according to Liu: "It is difficult to couple light through the germanium layer to a silicon waveguide, due to the large optical absorption coefficient of germanium at telecommunications wavelengths."

"And as well as absorbing light at telecoms wavelengths, the germanium layer restricts the range of silicon circuits to which the laser can be applied," he adds. "So a high performance III-V laser directly grown on a silicon substrate is the preferred solution for silicon photogenic-electronic integration."

So the next step for Liu and colleagues is to integrate the lasers with silicon waveguides, modulators and detectors, and finally the CMOS, a process that Liu believes will take around five years.

"There is no big stumbling block here, but it will take some time and funding from industry to make it happen," says Liu. "We've always been thinking about integration, otherwise what would be the point of putting a laser on silicon?"

"It is a challenge, but it's a much smaller challenge than getting the laser on silicon," he adds.

X-FAB: making six inch SiC production a reality

Can a Texas-based silicon wafer fab accelerate 6-inch SiC production? Rebecca Pool talks to X-FAB Silicon Foundries to find out more.

TODAY, the vast majority of SiC diodes and transistors are fabricated on 4-inch wafers. But in a bid to increase device yield per substrate and cut production costs, SiC production is edging towards 6-inch wafers as the market grows.

One company intent on pushing this transition forward is Germany-based X-Fab Silicon Foundries. Since 2013, the company has been busy adapting 6-inch CMOS production at its Texas facility ready for SiC production. In early March it deemed the plant 'SiC-ready'.

"[Back in 2013] all SiC manufacturing was on four-inch wafers, but six-inch wafers were becoming available and we could see that this transition would soon be underway," says Andy Wilson, Director of Strategic Business Development at X-Fab.

"We also wanted to leverage the economy of scales of our six-inch CMOS manufacturing capacity," adds Wilson. "Converting our tools to run six inch, rather than four-inch, SiC wafers was actually easier."

So X-FAB started the not-so-trivial process of six-inch SiC wafer conversion. According to Wilson around 90 percent of SiC production processes could be supported by equipment already on X-FAB's CMOS line, while other tools needed to be adapted.

"For example, the thickness of a silicon carbide wafer is about half that of a silicon wafer, so steppers, coaters and deposition equipment needed some conversion," he says. "Also, the silicon wafer is opaque while the SiC wafer is translucent, so we made some significant changes to our [sensor-based] automated handling equipment."

The company spent the best part of 2014 developing what Wilson calls its 'hybrid' production, being able to switch capacity back and forth between CMOS and SiC manufacturing. At the time, any SiC process steps that couldn't be accommodated by CMOS equipment, such as high temperature implantation and annealing, would be outsourced. And of course, subsequent SiC steps that could be carried out on the emerging integrated CMOS-SiC line would then be brought back in-house.

But come 2015, change was afoot. The US Department of Energy had launched its massive $146 million PowerAmerica Institute, uniting academia and industry in a mission to drive wide bandgap semiconductor costs down so as to be cost-competitive with silicon power electronics devices.

X-FAB joined the Institute, alongside the likes of Cree, Transphorm, Toshiba and United Silicon Carbide, and was tasked with providing the 6-inch wafer fabrication services necessary for device production. And as part of the public-private partnership, the company received the all-important funds to invest in the specialised SiC processes it needed to run an entire 6-inch SiC production line, without outsourcing.

"Back in 2013 we were not in a position to justify the investments for these highly specialised SiC tools," points out Wilson. "But in early 2015, PowerAmerica provided matching funding, which allowed us to buy the processes that are unique to SiC, several years earlier [than planned]."

Time to invest

Indeed, since 2015, X-FAB has secured a high-temperature anneal furnace, backgrind equipment for thinning SiC wafers, backside metal sputter and backside laser anneal tools. What's more, a high temperature implanter is scheduled for installation later this year, and Wilson is now looking forward to seeing the foundry capitalise on its economies of scale.

The Texas facility can churn out up to 30,000 silicon wafers a month, and as the X-FAB director adds: "We can imagine that if we were running solely SiC discrete power devices, capacity would be even higher than 30,000 wafers a month."

Clearly X-FAB could bring unprecedented manufacturing scale to 6-inch SiC production, and, thanks to its existing CMOS processes, at an affordable cost. "We can expand our SiC capacity as demand for device increases, while our

X-FAB intends to drive the SiC industry's transition from 4-inch to 6-inch production.

silicon business will have absorbed the majority of the enormous fixed costs associated with expansion," says Wilson.

"With this cost structure, and by keeping our overheads manageable, I feel we can really accelerate the commercialisation and adoption of SiC power devices," he adds.

So where next for X-FAB? Still part of PowerAmerica, the company will continue to provide SiC foundry services to Institute members but will now offer manufacturing capabilities to SiC device manufacturers worldwide.

"We purchase six inch SiC epiwafers and perform the necessary wafer processing required to create functional devices," says Wilson.

"So we can supply to fabless vendors while device manufacturers could also add X-FAB as a second-source supplier or use us as an alternative [manufacturer] as they move from four-inch to six-inch wafer fabrication."

To date, X-FAB has focused on fabricating SiC diodes and MOSFETs, as well as other switch architectures, for automotive markets, but fully intends to move into industrial markets. What's more, the company would also consider the manufacture of GaN-on-SiC devices for RF markets.

"X-FAB is bringing something different to the market," says Wilson. "The scale of our facility and our economies of scale are certainly unique in the foundry world, especially at six inches."

X-FAB is bringing something different to the market," says Andy Wilson, Director of Strategic Business Development at X-Fab. "The scale of our facility and our economies of scale are certainly unique in the foundry world, especially at six inches."

LEDs: The compelling case for GaN-on-silicon

Following frustrating trials, chipmakers are failing to fully appreciating the disruptive potential of GaN-on-silicon LEDs. By Burkhard Slischka from Allos Semiconductors

MANY BELIEVE that the chance has gone for GaN-on-silicon to play a major role in the LED industry. They argue that GaN-on-silicon technology has taken too long to mature, and the momentum lies with LEDs on sapphire, which have costs that have fallen throughout the last decade.

However, a few firms are swimming against this tide. They include the Korean electronics giant Samsung, which in an article in last month's issue of this magazine highlighted that by combining 200 mm GaN-on-silicon epiwafers with wafer-level, chip-scale packaging it is able to produce high-quality LEDs with a staggering 60 percent lower cost. Samsung concludes that the future of LED making "surely lies with silicon".

So is Samsung a visionary, leading high-volume manufacturer of a disruptive, low-cost technology that other chipmakers are overlooking? Or is the Korean outfit misguided, and soon to be dogged by high costs and persistent low yields?

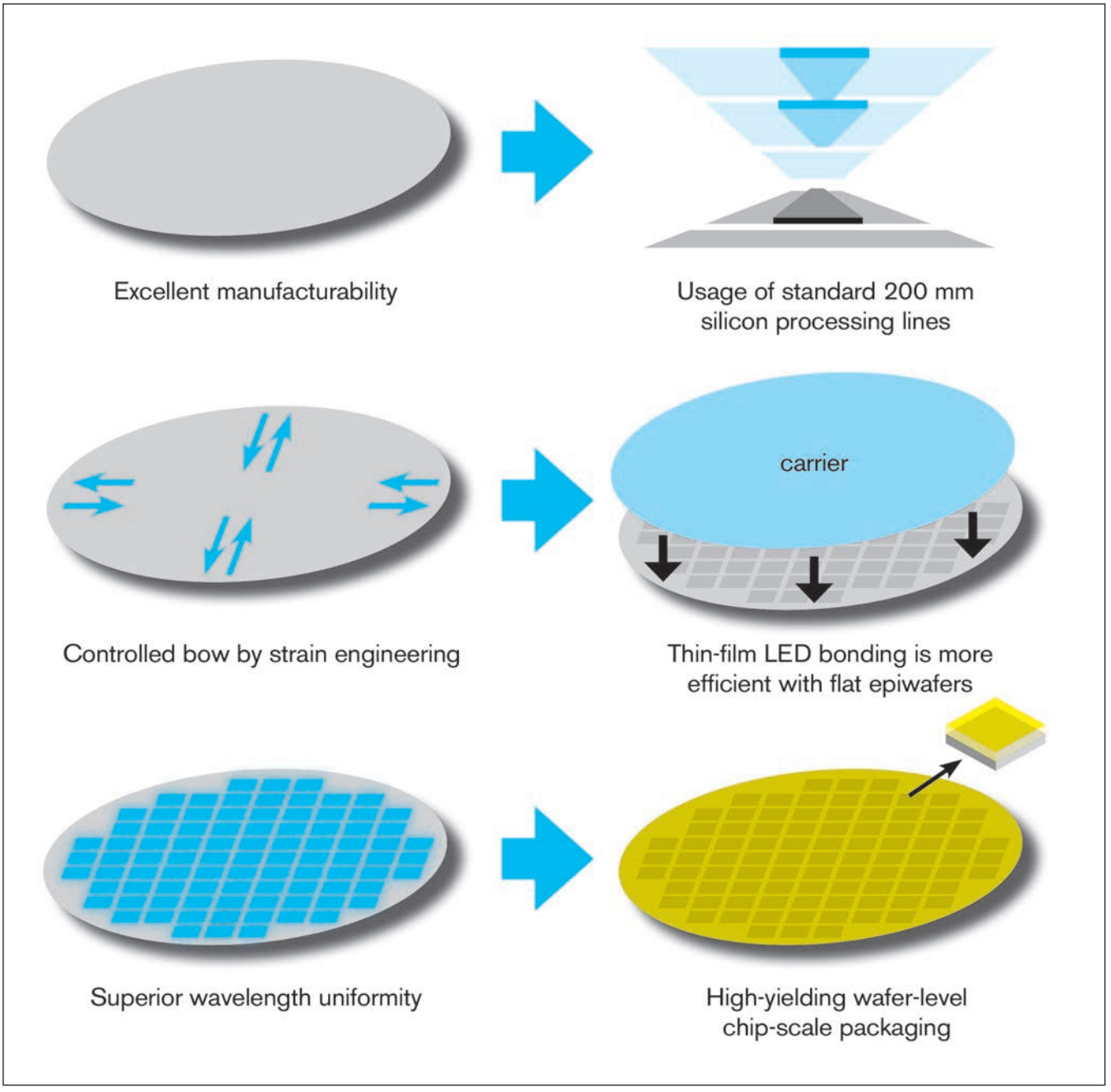
During the last decade, the promise of lower costs, resulting from bigger, cheaper wafers has been the primary driver behind GaN-on-silicon LED development. But it has been tough to turn this dream into a reality, because it is not easy to grow good-quality epiwafers and use them to make high-performance LEDs.

What makes Samsung special is that it has combined three crucial building blocks: access to the low processing cost of silicon lines, which is enabled by good GaN quality and 200 mm epiwafers designed for manufacturability; the use of thin-film LED chips, which become much easier to make when using silicon substrates rather than sapphire ones; and high-yielding, lower cost wafer-level, chip-scale packaging, which becomes possible only with the superior wavelength homogeneity of GaN-on-silicon epiwafers. It is this combination that allows Samsung to achieve the enormous benefits it claims.

Samsung's skeptics will argue that this approach is flawed. In their minds, there are too many changes associated with switching production to silicon substrates.

To back up this view, they might cite Toshiba's woes. In 2013, it invested a great deal of money in acquiring Bridgelux's GaN-on-silicon technology and then building up its capabilities in Japan and the US.

> "Is Samsung a visionary, or will it be soon dogged by high costs and persistent low yields?"

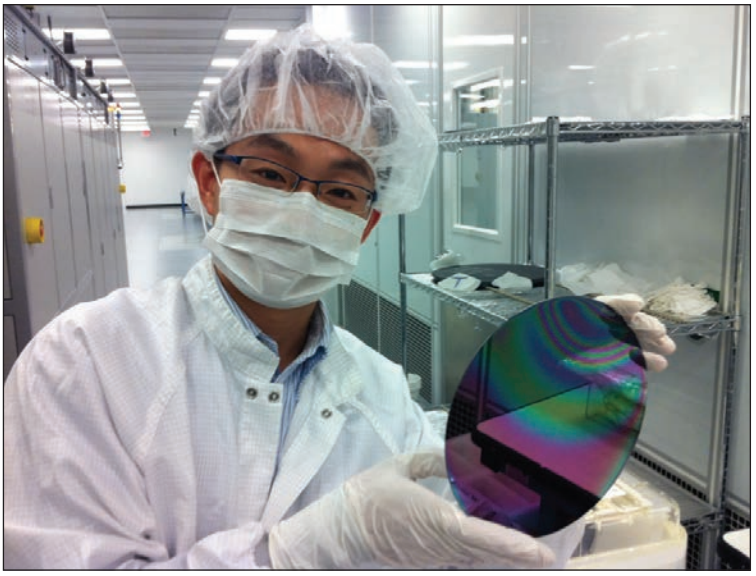


By 2015, when it started sampling GaN-on-silicon LEDs, the plan seemed to be working. Many industry insiders were won over by the unrestrained quality of the chips and the promise of low prices.

But Toshiba appears to have suffered from serious yield issues and to have failed to ship large quantities of GaN-on-silicon LED before it was forced to shut down this part of its business at the end of last year, in the aftermath of its accouting scandal.

Although Toshiba's experience highlights the challenges for GaN-on-silicon LEDs, it would be folly to discard this technology. The 60 percent cost savings claimed by Samsung are not exaggerated, according to calculations by our team at Allos Semiconductors. More importantly, we see this not just as a one-time cost reduction but rather as a shift to a fundamentally lower-cost curve. So, with such significant savings up for grabs, shouldn't LED executives allocate more time to consider this, rather

Excellent properties of GaN-on-silicon epiwafers enable high yield and cost savings in device processing and packaging.



The uniformity improvements since Bridgelux announced its development of GaN-on-silicon LEDs in 2011 have been tremendous and now enable "one bin" wafer-level, chip-scale packaging on 200 mm wafers.

than devoting all their energy on delivering a cost reduction of 'only' 5-10 percent in the next quarter?

It is clear that smaller corporations cannot invest as much in GaN-on-silicon technology as Samsung or Toshiba. And unlike this duo, most of them don't have their own silicon lines. Additionally, not all LED makers are fully vertically integrated. Companies which focus on epitaxy and chip making will have to coordinate with their customers to realize the benefits of wafer-level, chip-scale packaging that Samsung enjoys.

Nevertheless, the challenges of entering GaN-on-silicon LED production are not insurmountable. GaN-on-silicon's potential can be unleashed by engaging with technology and foundry partners. Such smart ways can reduce development and production cost, speed-up time-to-market and limit risk. They are available for all three parts of the LED production process – epitaxy, device processing and packaging.

Production of high-quality, low-cost GaN-on-silicon LEDs hinges on hetero-epitaxy. Growing GaN-on-silicon requires specialist expertise, most of all in order to achieve the required crystal quality and wavelength uniformity and to ensure manufacturability on cost-efficient, high-throughput reactors. Complicating matters, patents protect a considerably amount of know-how associated with GaN-on-silicon technology. Companies might be daunted by the challenge of developing a GaN-on-silicon epitaxial process of their own. However, they can license our patented, proprietary GaN-on-silicon technology. We will exchange their buffer for ours and help them integrate it with their light emitting structures. Such projects are typically completed within just twelve weeks allowing customers to focus their development effort on device processing and packaging.

For device processing, switching from sapphire to silicon is not just a matter of transferring to large diameter processing equipment and the need to introduce more complex thin-film production processes. The biggest challenge is having access to a 200 mm processing line. Here we see that partnering with a low-cost, high-volume silicon foundry is an attractive option: it offers a new business opportunity for the foundry, and equips the LED maker with a more variable cost structure, while at the same time reducing its capital expenditure.

Wafer-level, chip-scale packaging is a technology that many LED companies have investigated with sapphire substrates, but insufficient uniformity has prevented implementation in the manufacturing process. As Samsung has shown, this situation can change when the process is performed on uniform, 200 mm GaN-on-silicon epiwafers. Companies that are lagging behind in the development of wafer-level, chip-scale packaging technology could turn to specialized technology advisers or tap into the expertise of the packaging foundries from the IC industry.

With key technologies now in place, Samsung will refine its processes as it ramps up production. Rivals with underutilized sapphire-based capacity and a lack of silicon line experience may look on in awe, fearing that the barriers to entry are too high. But rather than being paralyzed by the challenges of bringing GaN-on-silicon LEDs to market, Samsung's actions should be viewed as a wake-up call for other LED chipmakers. The cost-saving potential of the technology is huge and there are smart ways to tackle the challenges.

> "GaN-on-silicon's potential can be unleashed by engaging with technology and foundry partners"

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Driving diversification in GaN device production

MOCVD reactors that deliver fast production of aluminium-rich epiwafers with carefully controlled doping profiles can drive a growth in shipments of UV LEDs and vertical power devices

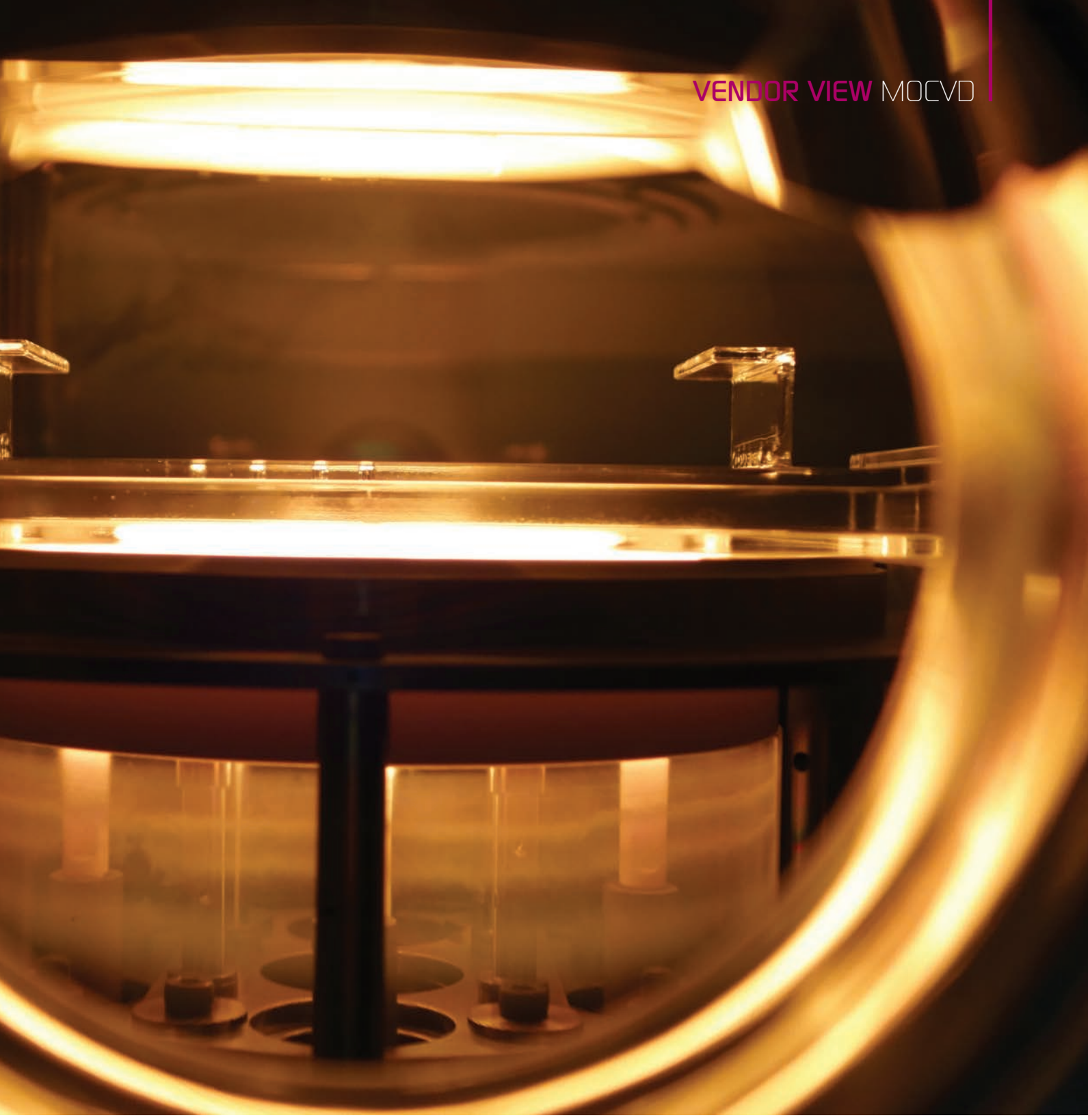
BY KOH MATSUMOTO FROM TAIYO NIPPON SANSO

BY FAR the biggest selling GaN chip of today is the LED. It is backlighting countless screens and fuelling a revolution in efficient, solid-state lighting.

Revenues for GaN LEDs will continue to grow throughout this decade, but could plateau soon after. So, if GaN chip sales are to continue increasing in the long term, the LED will have to be joined by new breeds of device delivering significant commercial success.

Two of the most promising GaN-based candidates are the UV LED and the vertical electron device. The former is an attractive replacement for mercury lamps, and could be used for various applications, including sterilizing viruses, purifying water, optical processing, curing resins, degrading environmental pollutants and preventing hospital infection. There are many good reasons for replacing mercury lamps with UV LEDs, including: increasing the lifetime of the lamp; enabling the introduction of a broader, wavelength-tuneable, more powerful source; boosting wall-plug efficiency; trimming the size of the unit; and reducing environmental impact.

Meanwhile, commercial introduction of competitive, GaN-based power devices could take market share from the incumbent silicon devices, which are held back by a smaller bandgap, a slower electron velocity and a lower breakdown electric field.



Many of the researchers that are working with wide bandgap power electronics are developing vertical GaN electron devices that are grown on bulk GaN substrates, because this simplifies wiring and enables the device to be housed in a small package.

To enable UV LEDs and power devices to generate significant and increasing revenues, it is essential for MOCVD tools to provide: control of gas-phase reactions at high aluminium concentrations; control of carbon incorporation; and deposition of high-quality layers at high growth rates. At Taiyo Nippon Sanso of Tokyo, Japan, we satisfy all these requirements with a portfolio of reactors featuring a 'horizontal three-layer' design and growth at atmospheric pressure. Our latest innovation is the introduction of a high temperature element to our GaN MOCVD tools, which have a rich history – the development of the first-generation of these reactors can be traced back to the late 1980s.

One of the biggest challenges with UV LEDs and vertical GaN power devices is the growth of high-quality layers of AlN and high-aluminium-content AlGaN. Particles tend to form, due to a gas phase reaction between trimethylaluminium (TMA), trimethylgallium (TMG), and ammonia. To overcome this issue, a few years ago we introduced a high-flow-rate MOCVD tool, the SR4000, which we described in the March 2014 edition of *Compound Semiconductor*.

THE SR4000HT can reach wafer temperatures of 1300°C or more, thanks to an effective heat shield, a high-power input and an improved inner reactor design.

Item	Detail
Wafer size	3 2 inch, 1 4 inch
Wafer Temperature	Up to 1300 ºC
Growth pressure	From 10 kPa to 100 kPa
Gas flow	Three layered horizontal laminar flow
Safety standard	Correspond to UL regulation
Options	In-situ monitor, gas concentration monitor, etc.

Table I Specification of SR4000HT.

The high-temperature element is present in our recently released SR4000HT, which is capable of reaching wafer temperatures of 1300 °C or more, thanks to an effective heat shield, a high-power input and an improved inner reactor design (see Figure 1 for temperature uniformities on the susceptor surface). Higher temperatures are ideal for forming thick, aluminium-rich layers, which are needed when fabricating UV LEDs and GaN power devices. The latter device can have an epitaxial stack with a thickness of tens of microns, while the high temperatures are beneficial for the baking of the reactor in between growth runs.

Our SR4000HT shares many of the hallmarks of our SR4000, which has proved our most popular machine for R&D and a small-scale production of InGaN-based lasers and GaN-based electron devices (the specification of the SR4000HT is summarised in Table I). The SR4000HT retains the original features of the three-layered gas ejection nozzle, wide controllability from low pressure to atmospheric pressure, and a high-flow-rate of carrier gases. Production capability per run is either three 2-inch wafers, or a single 4-inch wafer.

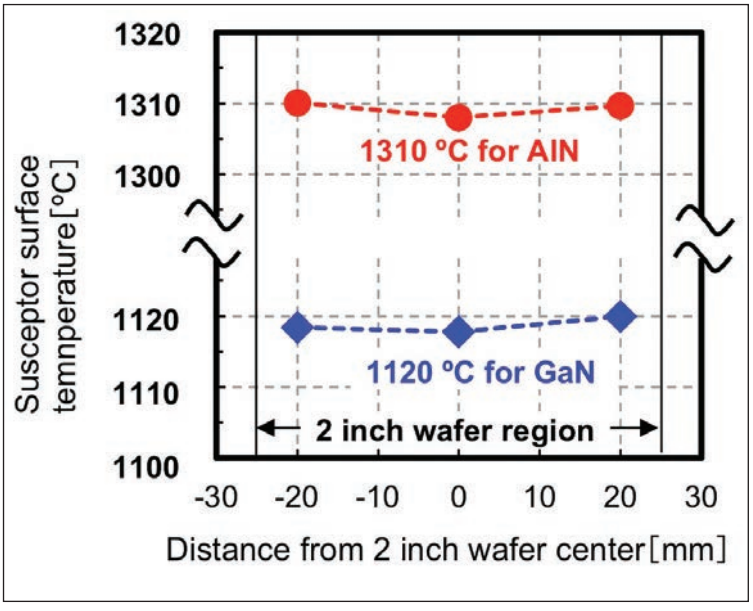


Figure 1. The SR4000HT produces an excellent degree of temperature uniformity across the susceptor surface in the 2-inch wafer region.

Making high-quality UV LED epiwafers

We have demonstrated the capability of our SR4000HT by using it to grow AlN and AlGaN films. Scrutinising the epilayers indicates a very high quality of material produced by our reactor. UV LEDs have an underlying buffer layer of AlN, plus high-aluminium-content AlGaN, so the ideal substrate is bulk AlN. However, the lack of a mature production technique for the growth of this material has led to widespread use of sapphire as a foundation for the UV LED.

Growth of high-quality AlN and AlGaN layers on sapphire demands higher growth temperatures, which enhances the migration of aluminium atoms on the growing surface, but also a parasitic vapor phase reaction. Our SR4000HT meets this need and can realise growth rates of 10.6 μm/h for AlN and 7.2 μm/h for $Al_{0.6}Ga_{0.4}N$ (see Figure 2 for growth rates at various TMA and TMG supply concentrations). The growth rate for AlGaN is almost constant for growth temperatures spanning 1000°C to 1160°C (see Figure 3), indicating that the gas-phase reaction is controlled well.

It is possible to use our SR4000HT to produce AlN template wafers, and to also carry out AlN regrowth on these engineered substrates. We have re-grown 3 μm-thick AlN films on AlN-on-sapphire templates, which were annealed at high temperatures under a mixture of nitrogen and carbon monoxide, and prepared by reserachers at Tohoku University and Mie University. X-ray rocking curve measurements on the template produce a full-width at half-maximum (FWHM) of 64 arcsec for AlN(002) and 191 arcsec for AlN(102). Similar values are obtained for a 3 μm-thick film of AlN deposited on the AlN template wafer – in this case, the FWHM is 49 arcsec for AlN(002), and 214 arcsec for AlN(102). These results indicate that high-quality AlN

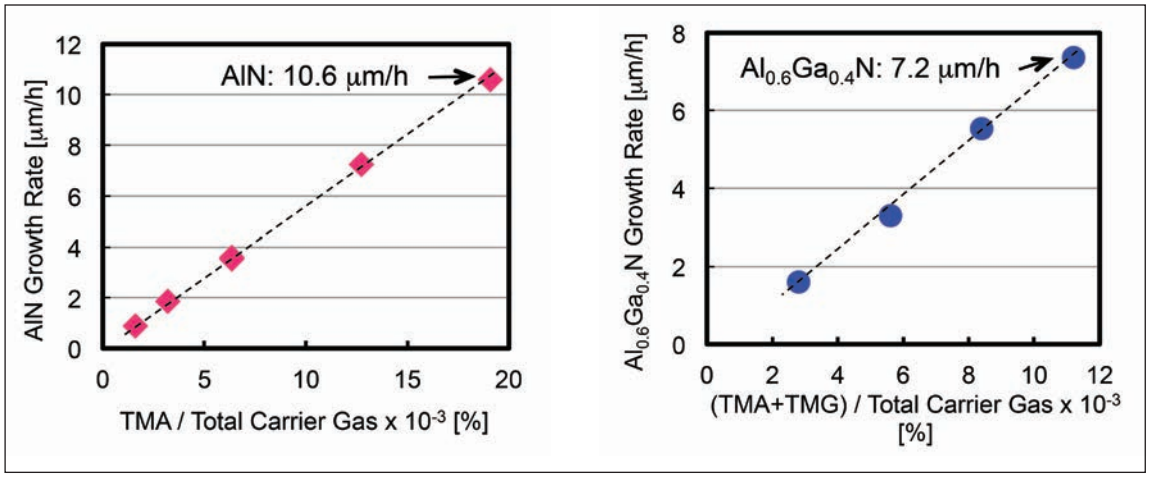


Figure 2. The high growth rates for AlN and $Al_{0.6}Ga_{0.4}N$ enable the relatively quick growth of thick epilayer structures.

with a low dislocation density can be obtained by the combination of these techniques. In addition to the narrow X-ray diffraction FWHM, good quality AlN with an atomic step on the surface was grown at 1300 °C.

Scanning electron microscopy and atomic force microscopy reveal a flat, high-quality surface for the 3 µm-thick AlN layer (see Figure 4). The surface has a root-mean-square roughness of 0.103 nm and features atomic steps, according to atomic force microscopy.

High-performance UV LEDs require *n*-type AlGaN with good electrical characteristics. To grow such a layer, it is essential to reduce impurities that can compensate for donors. Cutting out carbon is crucial, as it can be incorporated on nitrogen sites within GaN, where it acts as a deep acceptor. We have found that the carbon concentration can be reduced from 5.4×10^{18} cm^{-3} to 2×10^{17} cm^{-3}, even for growth rates as high as 7.2 µm/h. This result underlines the capability of the SR4000HT for producing UV LEDs (see Figure 5).

Further proof of the capability of our tool has come

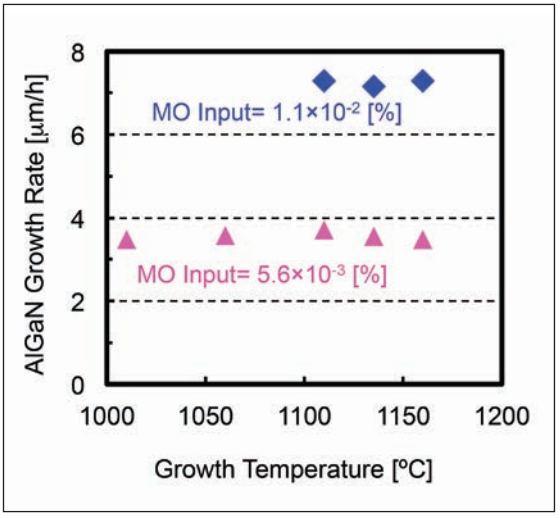


Figure 3. MOCVD process engineers will benefit from an AlGaN growth rate that produces very little variation with growth temperature.

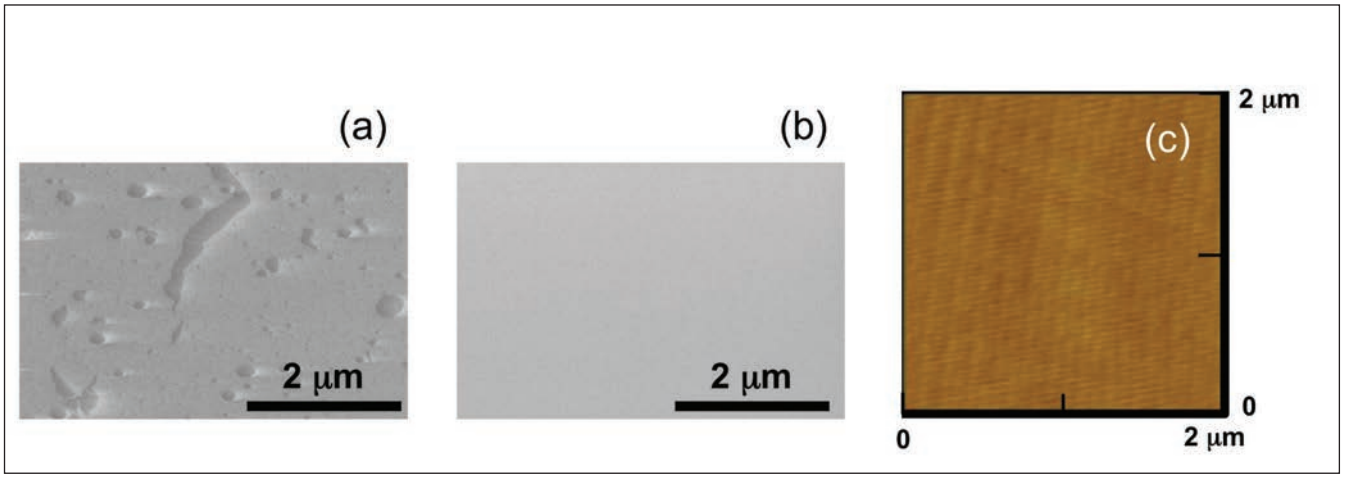
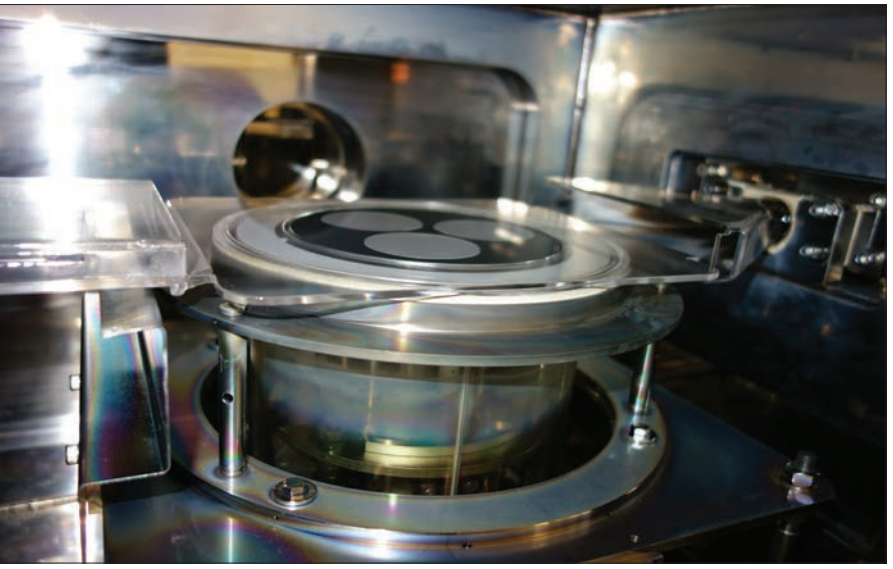


Figure 4. (a) SEM image of AlN template surface annealed at a high temperature after MOCVD growth. SEM (b) and AFM (c) images of an AlN surface re-grown on the template shown in Figure 4 (a).



With the SR4000HT, diode structures can be grown in just a few hours, thanks to low carbon concentrations at high growth rates.

from engineers at the Industrial Technology Research Institute in Taiwan. They have used our SR4000 to produce a UV LED. The electroluminescence spectrum for this device has a peak intensity at 284 nm, a full-width at half maximum of 15 nm, and a very small deep-level-luminescence (see Figure 6).

Improving diode doping

The other leading candidate for driving up GaN chip sales, the vertical electron device, has a superior efficiency over the silicon incumbent, due to a lower on-resistance. Minimising this on-resistance requires careful control of dopant concentration and minimising impurities. Another challenge for MOCVD process engineers is to produce epiwafers using high growth rates, to reduce the time taken to grow the thick layers that are needed for a high breakdown voltage.

Our reactors are ideal for growing power devices, because they accommodate a tremendously wide range of growth pressures, growth rates and V/III ratios. This flexibility equips our tool with impurity controllability at a high growth rate. In the remainder of this feature, we detail the reactor's capability to control carbon and silicon impurities, and dopant concentration, in the growth of a GaN *p-n* diode on a native substrate.

We have investigated the growth of the bipolar *p-n* diode, rather than the mono-polar Schottky barrier diode, because it has a smaller on-resistance. The carrier concentration in the silicon-doped, *n*-type layer of this bipolar device must be controlled over the range 10^{15} cm^{-3} to 10^{19} cm^{-3}, while the carbon concentration is maintained to no more than 1×10^{16} cm^{-3}. For the lower end of *n*-type carrier concentrations, silane must be supplied at a very low flow rate and carbon impurities must be very low. Meeting these requirements depends on the reactor design and growth techniques.

Conventional reactors are often unsuitable for the growth of diodes, because they have a low growth rate for *n*-type GaN that leads to total growth times of several tens of hours or more. With our reactors, however, epiwafer growth can be completed in just a few hours, thanks to the low carbon concentrations at high growth rates (see Figure 7).

At a growth rate of 2.3 μm/h under atmospheric pressure, the carbon concentration can be as low as 3.7×10^{15} cm^{-3}. Lower carbon concentration at high growth rates can be obtained at atmospheric pressure. The far higher carbon concentrations at high growth rates can be also be beneficial in some structures, such as GaN-on-silicon devices, because they introduce high resistivity.

We have used our reactor to produce vertical GaN electron devices with an architecture that has been pioneered by researchers at Cornell University and Hosei University (see Figure 8). Growth rates of

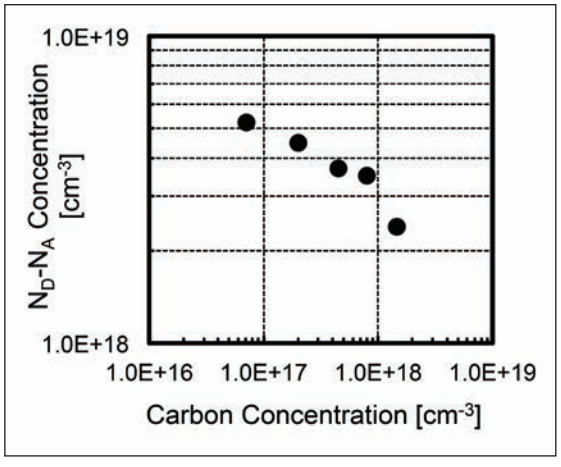


Figure 5. *n*-type $Al_{0.6}Ga_{0.4}N$ with low carbon concentrations are possible, even at growth rates of 7.2 μm/h.

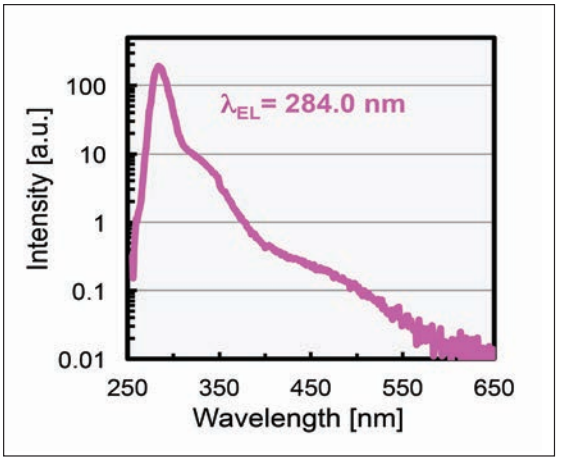


Figure 6. The sharp electro-luminescence spectrum highlights the capability of the SR4000HT for the growth of UV LEDs.

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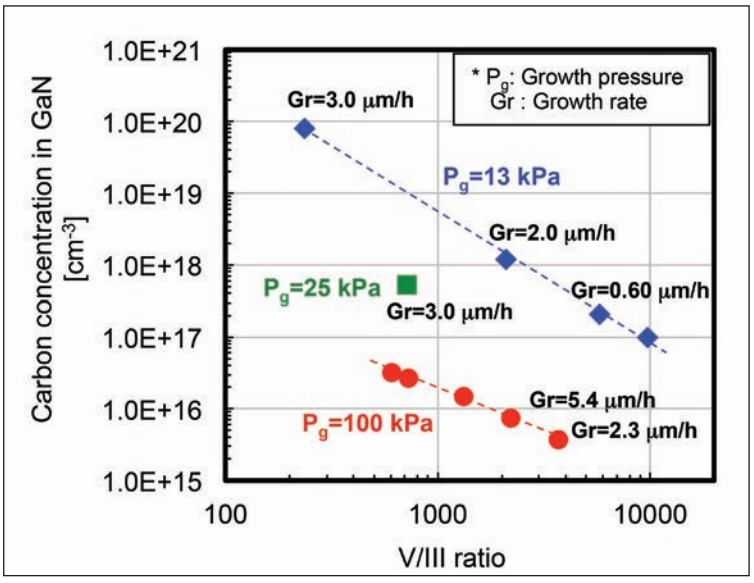


Figure 7. Even at high growth rates, the carbon concentration can be adjusted in the range 10^{15} cm^{-3} to 10^{20} cm^{-3} by appropriate selection of the V/III ratio and growth pressure.

2.3 μm/h for the undoped GaN and 5.4 μm/h for the *n*-type GaN have been used to produce *p-n* diodes on a GaN substrate. These devices have been scrutinised by secondary ion mass spectrometry (see Figure 9). This technique reveals low values for carbon and silicon concentrations in the undoped GaN, and accurate doping of these elements in the *p*-type layers. Note that it took less than four hours to grow the 20 μm-thick *n*-type GaN drift layer.

Our diodes are currently undergoing electrical characterisation. We anticipate that these results will support our case for the suitability of our reactors for growing GaN diodes. And as we have shown earlier, their high-temperature capability makes them a great choice for producing UV LEDs.

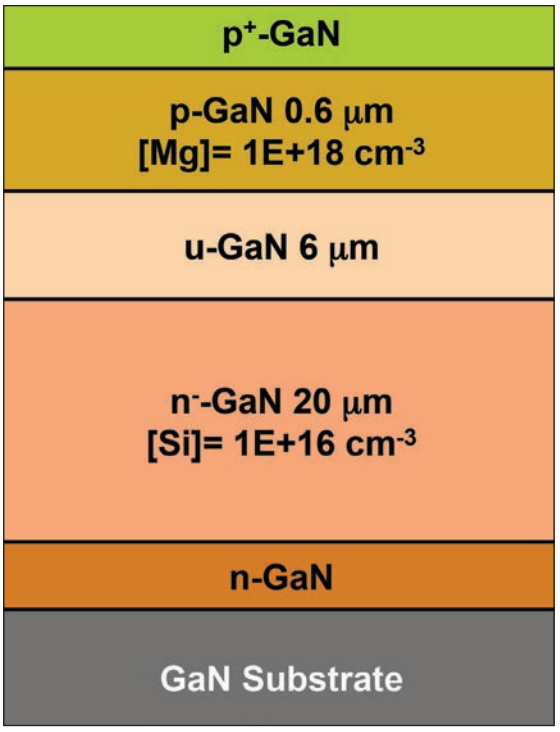


Figure 8. The *p-n* diode structure grown by engineers at Taiyo Nippon Sanso.

Further reading

H. Miyake *et. al.* Appl. Phys. Express **9** 025501 (2016)
K. Ikenaga *et. al.* to be published in JJAP (2016)
K. Nomoto *et. al.* IEDM 2015 237 (2015)

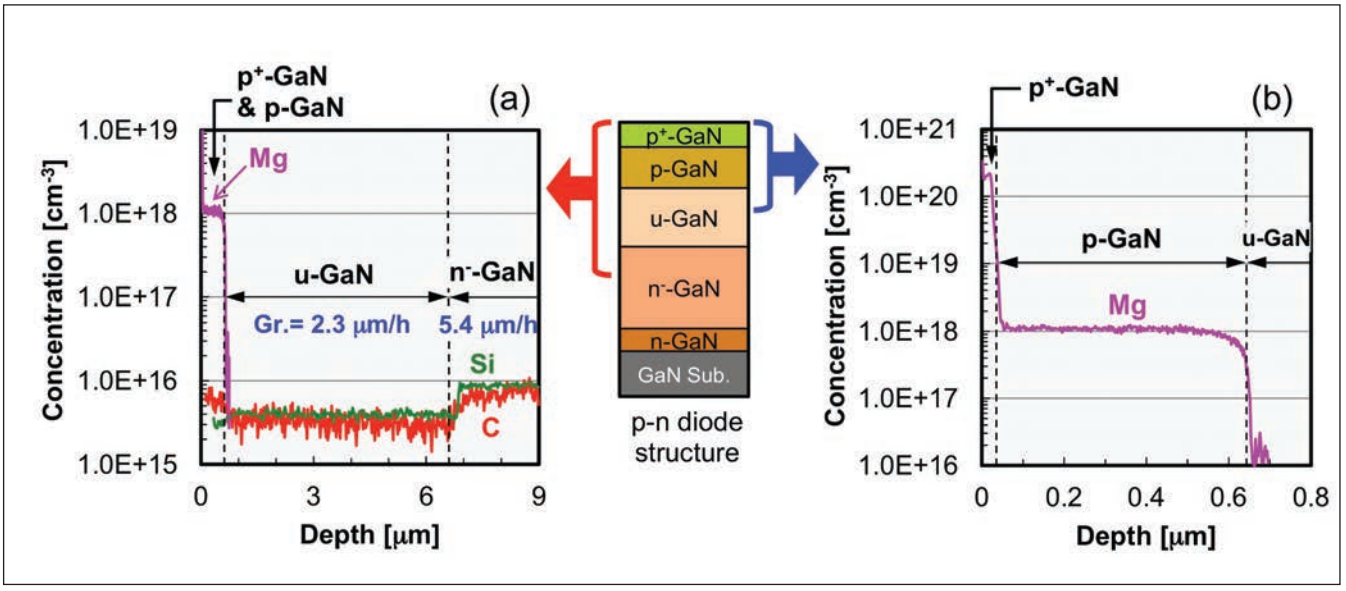


Figure 9. SIMS profiles highlight the capability of the SR4000 tool to realise material with low levels of impurities and carefully controlled doping. (a) SIMS profile to a depth of 9 μm (b) SIMS profile to a depth of 0.8 μm. The detection limits are as follows: 6 x 10^{14} cm^{-3} for carbon, 2 x 10^{15} cm^{-3} for silicon, and 1 x 10^{16} cm^{-3} for magnesium.

Dissecting prospects for CS industry

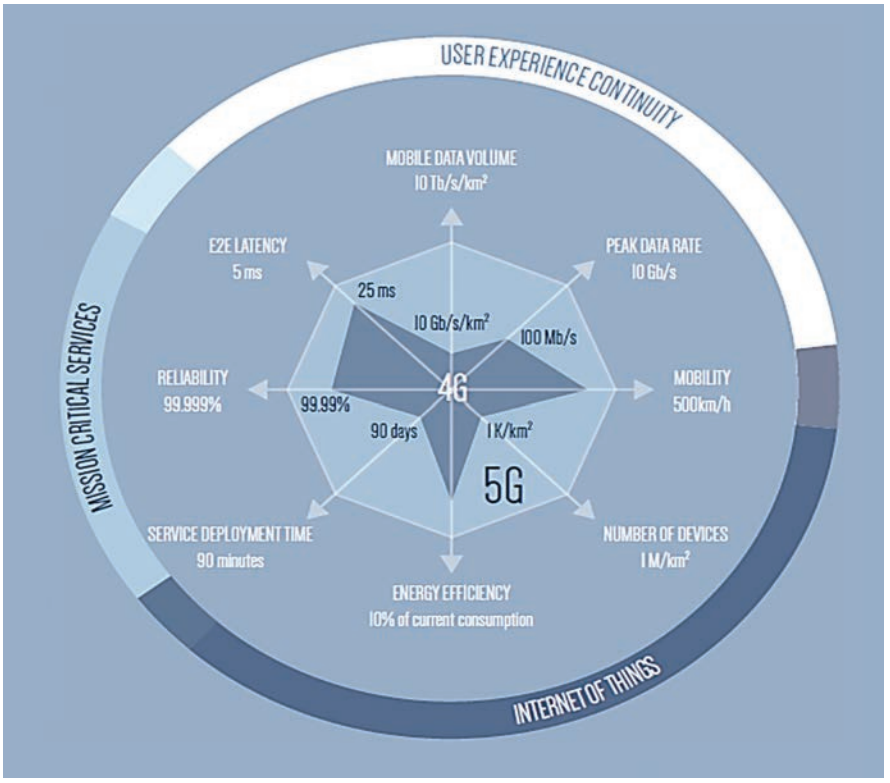
Analysts at CS International claimed that 5G will be good for GaAs, opportunities in the infrared can diversify LED sales, and space applications are dominating shipments of multi-junction cells

RICHARD STEVENSON REPORTS

OUR INDUSTRY is united, but incredibly diverse. We share the processes for making chips, which involve the selection of the substrate, the growth and characterisation of epiwafers, and subsequent processing to create compound semiconductor devices. Yet the operation of the device varies tremendously, enabling our industry to sell products to a multitude of different sectors, from security and communications, to medicine, aerospace and consumer electronics.

This diversity of sales is so great that it prevents anyone from having an intimate knowledge of our entire industry. So, if you want to know the current state of our industry, and its prospects, you want to hear from a range of experts in their fields.

One way to do this is to head to CS International, where respected market analysts and industry veterans offer their take on the opportunities for compound semiconductors. At this year's meeting, held in early March and co-located with the inaugural PIC International, insights were given into: the impact that 5G will have on the sales of GaAs chips; the opportunities for infra-red LED sales in smartphones and smartwatches; the dramatic decline in multi-junction cell shipments for concentrating photovoltaics; and the most likely architectures for incorporating III-V channels in next-generation logic.

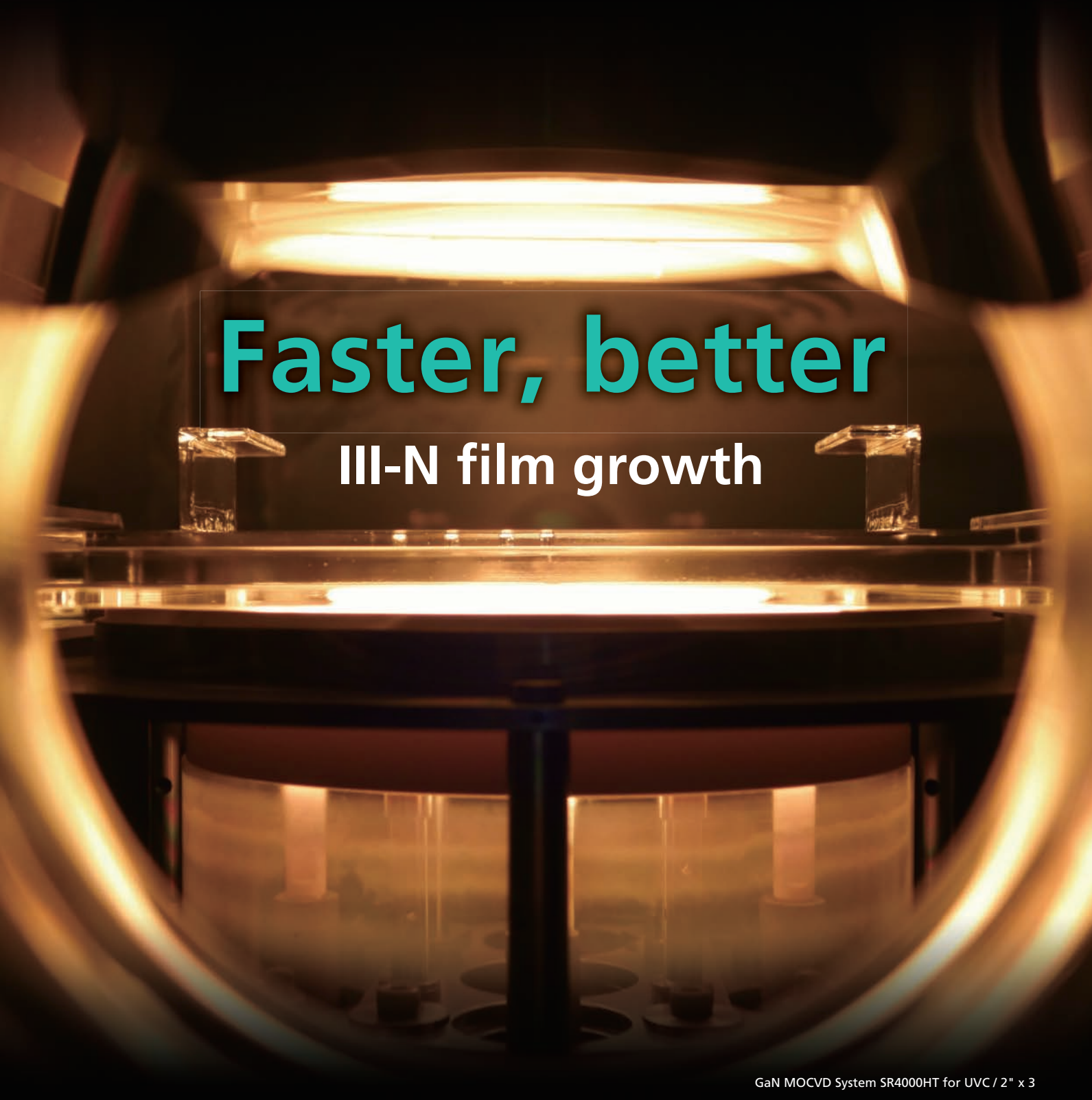


5G will deliver a rafter of performance improvements over 4G, making is better suited to serving mobile phone communication, the internet-of-things, and machine-to-machine communication.

5G: Good for GaAs

Speaking to delegates at CS International, Eric Higham, Director of Advanced Semiconductor Applications at Strategy Analytics, argued that the emergence of a 5G network should spur GaAs revenue to new highs. Higham began by explaining the great need for these new, superior networks, before stating the capability of GaAs devices for serving this application.

A major driver for the deployment of 5G is that it can accommodate the rocketing growth in mobile data traffic. Higham illustrated this point by referring to a study by Cisco Systems that projects that



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between 2009 and 2019, mobile data traffic will grow at a compound annual growth rate of 75 percent. That equates to a staggering 266-fold increase over that time frame. Cisco has also provided projections for the next ten years from now. During that time the increase in mobile data traffic will slow, but still undergo a 40-fold hike.

Higham pointed out that while this growth in traffic is one of the justifications for 5G, there are also other benefits related to its roll out. He summed this up by describing the 5G vision as: "Unlimited access to information and the ability to share data anywhere, anytime, by anyone and anything." Extreme mobile broadband will be combined with massive, incredibly reliable machine communication.

Goals that must be met for delivering extreme mobile broadband would include a peak data rate exceeding 10 Gbit/s, and coverage at 100 Mbit/s everywhere. Meanwhile, the other two pillars of the 5 G vision – which could be summed up by the phrases "instant action" and "for everything", and relate to tactile internet and the internet-of things – would involve machine-to-machine communication.

In some cases, these lines would be critical, requiring a latency of less than a millisecond, and ultra reliability; and in other cases, it would be massive machine communication, involving tens or hundreds of incredibly low-cost devices with a 10-year battery life.

A key technology for delivering the high data rates of 5G is MIMO – multiple-in, multiple-out. It increases the capacity of a link by using multiple transmit and receive antennas. Higham highlighted the progress with this technology, including a 64 element array developed by a team from Bell Labs and Rice University that operates at 28 GHz, boosts capacity by a factor of 10, and is 2.5 feet by 2 feet in size. "It's large, but you could picture it being part of a base station."

Also discussed was a 64-element array block operating at 60 GHz. It featured 22 mm by 22 mm chips produced with the TowerJazz SiGe process. Higham questioned whether these devices were too big for making a phased array for a handset.

MIMO technology has already been used for 5G trials. In a high-rise complex, Nokia has demonstrated data transmission exceeding 2 Gbit/s at 70 GHz, while Samsung topped 2.5 Gbit/s from a vehicle travelling at 60 km/hour. Even more impressive results have come from trials at Ericson, where data rates exceeded 10 Gbit/s, and at Fujitsu, where researchers delivered more than 11 Gbit/s using mobile devices as a form of base station.

Higham views 5G as a huge revenue opportunity for the GaAs industry, because it plays into the strengths of this III-V – namely a high-frequency response, good linearity, and excellent efficiency. In 2015 global GaAs revenue stood just above $7 billion, according to figures from Strategy Analytics, with sales dwarfed by estimates for the compound semiconductor industry and the total semiconductor market, which are in the region of $57 billion and $336 million, respectively.

However, Higham admitted that there are factors that could put a damper on his unabashed enthusiasm. Commercial deployment is slated for 2020, and will probably be timed to coincide with a major global sporting event, such as the Olympic Games held in Tokyo. Showcasing this technology could aid its deployment, but if there is teething trouble, or slipped schedules, the uptake of 5G could suffer.

Higham reinforced the uncertainty over the roll-out of 5G by referring to a paper from *Rethink Wireless* and *Lewis Insight*. A survey of mobile network operators revealed that 76 percent of them currently have no plans for 5G deployment. The primary reason for this is the lack of a clear return-on-investment.

The worst that could happen, according to Higham, is some form of "4G on steroids". But in his view, even that would swell GaAs revenue.

	Si solar cell today *	III-V/Si solar cell today	Required Cost for III-V/Si cells in flat plate modules
156x156 mm Mono-Si substrate	0.82 €	0.82 €	0.82 €
Growth substrate polishing/ preparation	--	5-10 € (CMP polished)	< 0.05 €
Processing: pn-junction, metal, ARC	0.66 €	0.66 €	0.66 €
5 µm III-V Ga(In)AsP growth	--	50-80 €	0.67 €
Waste treatment III-V materials	--	10 €	0.1 €
Depreciation of III-V reactor	--	Not considered	0.1 € (2.8 Mio wafers/year for 2-3 Mio € machine)
Total 156x156 mm solar cell	1.48 €	67 €	2.40 €
Efficiency	18 %		30 %
Watt Peak (Wp) @ 1000 W/m²	4.38 Wp		7.30 Wp
Solar Cell cost in €/Wp	0.34 €/Wp		0.33 €/Wp
Area for 1000 Wp	5.6 m²		3.3 m²
PV Module cost in €/Wp	0.58 €/Wp		0.47 €/Wp (due to less area)

Frank Dimroth from Fruanhofer ISE showed that in order for III-V-on-silicon to compete with silicon flat plate, there would need to a be a 100-fold fall in the costs of epitaxy, substrate preparation and waste treatment.

One of the near-term opportunities for the growth of sales of infrared LEDs is in smart watches that measure heart rates.

Figures shown by Frank Dimroth from Fruanhofer ISE reveal that the CPV industry is struggling, with deployments plummeting from over 100 MW in 2012 to below 20 MW in 2015.

LEDs: Seeking higher margins

In the LED chip industry, the largest applications are visible LEDs for backlighting and general illumination. Here, competition is incredibly fierce, and margins are squeezed. So several chipmakers – including leading players Osram, Nichia and Epistar – are trying to generate healthy revenues with devices emitting in the infrared.

At CS International, Perrick Boulay, Technology and Market Analyst for LEDs, OLEDs and Lighting Systems at Yole Développement, discussed the leading markets and the emerging applications that these infrared LEDs can serve.

In 2014, according to Boulay, the security camera provided the biggest market for the infrared LED. In this class of camera, infrared LEDs are positioned around the rim of the lens, illuminating the scene that is imaged by the camera.

Right now, consumer electronics is accounting for most of the growth in the infrared LED market. "Smart watches use infrared LED technology to measure biometric values, such as the heart rate," explained Boulay. According to him, infrared LEDs are also used in proximity sensors in cell phones, enabling the detection of the presence of the human ear. Armed with this technology, the touch screen is disabled when making a call.

Looking further ahead, Boulay believes that infrared LED sales will climb via deployment in the automotive sector. It could be used in systems to measure driver alertness via observations of the eye, and gesture recognition; but the most significant sales are tipped to come from night vision and LIDAR, which is a remote sensing technology that is the optical cousin of radar.

There are two common spectral ranges for automotive night vision systems. They can be passive, operate in the far infrared at typically 8 μm to 14 μm, and be based on microbolometers; and they can be active, using an LED or another source emitting at around 800 nm, to illuminate objects that are detected by a CMOS sensor. The latter offers superior resolution, but is not so good at detecting pedestrians and only works up to around 200 m, while the passive system can identify objects up to 500 m away, and is more pricey. Both types of infrared system have been available since 2000, but retail prices exceeding $2000 are hampering costs.

Boulay believes prices could fall, and the imaging systems become more attractive. He notes that in 2014, Autoliv starting shipping a night vision system that combined near infrared and far infrared capabilities, and was offered as an extra on the Mercedes S class. This option is currently $2,260, but prices could fall fast, driving up adoption.

The Yole analyst also briefly outlined a range of other applications for the infrared LED: in medicine, where sources emitting at 850 nm or 940 nm could be used for dermatology and neurology; in the military, where these emitters are used as tail lights that are only seen with night-vision goggles and devices; in smartphones and tablets, where they equip these devices with the capability to act as a universal remote control; and as a measure against movie pirating, with illumination behind the screen degrading the quality of illegal video recordings.

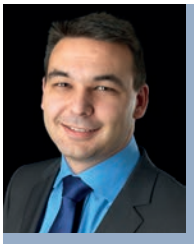
With so many opportunities for infrared LEDs, it is not surprising that more chipmakers are starting to manufacture these devices. However, Boulay warns that the production of an infrared LED is markedly different to that of a white-emitting sibling, so it is far from trivial to enter a market that has been led by the likes of Osram, Nichia and Epistar for at least five years. This challenge will be easier to overcome for the bigger players, which Boulay expects to penetrate this market in the short-to-medium term.

The collapse of CPV

Delegates were offered a view of the prospects of multi-junction solar cells from the academic Frank Dimroth from Fraunhfer ISE. He made a compelling case that multi-junction cells will continue to succeed in the aerospace market, but will struggle to make an impact in the terrestrial sector.

To show how difficult it will be for the CPV market to grow, Dimroth highlighted the selling points of the main rival, silicon technology. Its price is now very low – by 2015, a square silicon wafer with sides of 156 mm cost just $1.48. The market is also incredibly well established, with global shipments last year totalling 51 GW, equating to a mind-boggling 10 billion 156 mm-square wafers.

"The failure of CPV, to a good extent, is correlated to [silicon] overcapacity that



Yole Développement analyst Pierrick Boulay expects the market for infra-red LEDs to grow, as they are increasing used in smartphones and smart watches, and for night vision systems in cars.

was not foreseeable," remarked Dimroth. He illustrated this point by showing data from Lux Research that showed that in 2012, 2013 and 2014, excess capacity was around 104 percent, 85 percent and 50 percent, respectively (note that the last two figures were estimates), and during that time, the price of modules plummeted, destroying the fledging CPV industry. Installations of high-concentration CPV peaked in 2012, when they totalled more than 100 MW, fell to just half that figure by 2014, and last year were below 20 MW.

During his talk, Dimroth also compared the size of last year's space and terrestrial markets for multi-junction cells. He estimates that global shipments for space applications totalled about 200,000 4-inch wafers per annum, compared to just 15,000 for CPV.

At first glance, it might appear that the solution for enabling III-Vs to make an impact on the terrestrial market is to deposit these materials on silicon substrates. Dimroth pointed out the performance benefits that can result, citing work from a research group in the US, involving Steven Ringel from The Ohio State University. That team fabricated a dual-junction cell with an efficiency of more than 30 percent. It featured a 5 μm-thick, III-V epitaxial stack.

This efficiency is 12 percentage points higher than that for silicon. However, this increase in efficiency currently comes with an unacceptable hike in cost. Polisihing a 156 mm-square wafer to make it suitable for epitaxy would cost €5-10, while depositing a 5 μm film of compound semiconductor materials would add €50-80, and the waste treatment of the III-Vs would command another €10. The harsh reality is that unless the cost for epitaxy, substrate preparation and waste treatment can fall 100-fold, this technology will fail to compete with conventional silicon.

The logic of III-Vs

There are applications where it is not a battle directly between silicon and the compounds. Instead, the challenge is to get these materials to work really well together. That could well be the case in the silicon microprocessor industry. ICs made from silicon transistors are tipped to continue to the 7 nm node, but the insertion of higher mobility materials in the channels – most likely germanium for the *p*FETs and InGaAs for the *n*FETs – may be needed to maintain the reductions in power consumption per transistor that are associated with scaling.

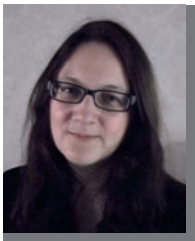
Discussing the pros and cons of different transistor architectures incorporating non-silicon channels was imec program manager for logic, Nadine Collaert, who began by discussing some of the trends outlined by Higham, such as the impact of machine learning and the internet-of-things on requirements for ICs. These wish lists vary, with ICs for data centres operating with wired connections and needing to deliver an increased performance at a constant power density; while smart mobile devices and sensors will have to operate wirelessly, with the former providing increased performance at constant leakage and the latter operating at ultra-low power.

Introducing III-Vs and silicon will "need compatibility with 300 mm silicon", argued Collaert, adding that this included the use of silicon-based processes and toolsets.

She went on to outline the fin replacement process that has been pursued by imec. Growing high-quality III-Vs on silicon is challenging, because the 8 percent lattice mismatch between these materials spawns numerous defects. They can be reduced substantially via growth of the compounds in a V-shaped trench, as many of the defects annihilate at the sidewalls. However, this cannot prevent lines of defects propagating along the channels.

Another major challenge for the developers of III-V transistors is finding a suitable material for the gate dielectric. Unlike silicon, there is no suitable native oxide, and many alternative materials lead to a high density of interface traps, which are to blame for reliability issues.

Recently, engineers at imec have switched from a finFET architecture to a gate-all-around device that improves electrostatic control of the channel. This move has proved a great success: transconductance, which reflects how quickly charge carriers move in the channel, has leapt from 500 μA/μm to more than 2000 μA/μm; and the sub-threshold swing, which is related to the switching capability of the device, has fallen from around 190 mV/decade to 110 mV/decade.



Program manager for Logic at imec, Nadine Collaert, highlighted defect densities and suitable gate dielectrics as two of the major challenges facing developers of III-V on silicon transistors.

The latest improvements to the gate stack may lead to even lower values for the sub-threshold swing. However, with any form of traditional FET, the sub-threshold swing cannot extend below 60 mV/decade. If lower values are needed, the tunnel FET must be considered, according to Collaert, who explained that with this type of device, low currents can be an issue – but can be increased by replacing silicon with lower bandgap materials, such as InGaAs. imec is active in this area, having managed to increase currents by replacing $In_{0.53}Ga_{0.47}As$ with $In_{0.70}Ga_{0.30}As$ (in the next issue, researchers from imec will detail their successes).

There is clearly far more work to do before III-Vs can make an impact in the silicon microprocessor industry. But they are playing a key role in a wide variety of industries, as shown by speakers at CS International, and it will be interesting to see where these compound semiconductor chips are being deployed towards the end of this decade and beyond.

5G: The precarious promise

A lack of standards for 5G is threatening a move to faster data rates for mobiles, and could also hinder the growth of the internet-of-things and machine-to-machine communication

RICHARD STEVENSON INVESTIGATES

THE ROLL-OUT OF 5G is anything but assured. According to speakers in the session entitled 'The Quest for 5 G' at this year's CS International, while there is substantial demand for a next-generation wireless network that sets a new performance benchmark, there is also a great deal of uncertainty that surrounds its deployment. Basic specifications, such as the operating frequency, are still to be nailed down. What's more, many operators are yet to start planning a build-out of the infrastructure, because they are yet to see an attractive return-on-investment.

Making a great case for the need for 5G networks was keynote speaker Michael O'Neal, Qorvo's Senior Director of Design and Advanced Engineering in the Infrastructure and Defense Products.

O'Neal kicked off his talk by arguing that there were three major market trends driving demand for 5G: a move to having everything on the Cloud, ubiquitous connectivity, and smart infrastructure.

The first of those, migration to data on the cloud, is well underway. After all, this is where many of us store our e-mails, access our music through the likes of iTunes, and watch movies through services such as Netflix. There are also tools in the cloud, such as those that enable GPS mapping on our phones.

O'Neal explained that is it the second major market trend, ubiquitous connectivity, that already allows gamers to play against peers over the ocean. It also underpins virtual reality and augmented reality.

The third trend, a smart infrastructure, is a key technology for connected cars – and eventually self-driving cars. "There are now 1 billion connected devices, and it's moving to 50 billion," remarked O'Neal, who explained that one of the numerous benefits of this will be the control of the heating in your home via a mobile.

According to O'Neal, migration to 5G should lead to: enhanced mobile broadband; massive machine-type communication; and ultra-reliable, low-latency communications. To make this happen, improvements associated with a shift from 4G to 5G will have to include a hike in cell edge data rates from 10 Mbit/s to more than 1 Gbit/s, a trebling of spectral efficiency, a 50 percent gain in energy efficiency, and an increase in mobility from 350 km/hour to 500 km/hour. "It's for high-speed trains – not for the autobahn," quipped O'Neal.

He does not expect 5G networks to operate below 3 GHz, due to a lack of available spectrum. Instead, he expects the use of millimetres waves, where there is more bandwidth, but a shorter reach. Data rates will also be increased by the use of multiple-input, multiple-output links, and advanced coding schemes. These 5G waveforms will be highly advanced, reducing the peak-to-average ratio of these signals, and demanding the use of high-efficiency amplification.

O'Neal concluded his talk by detailing the current status of wireless communication. The leading infrastructure of today is described as LTE Advanced, which operates below 6 GHz. It features carrier aggregation, with a few channels in a band – and can involve some channels in one band, and some in another.

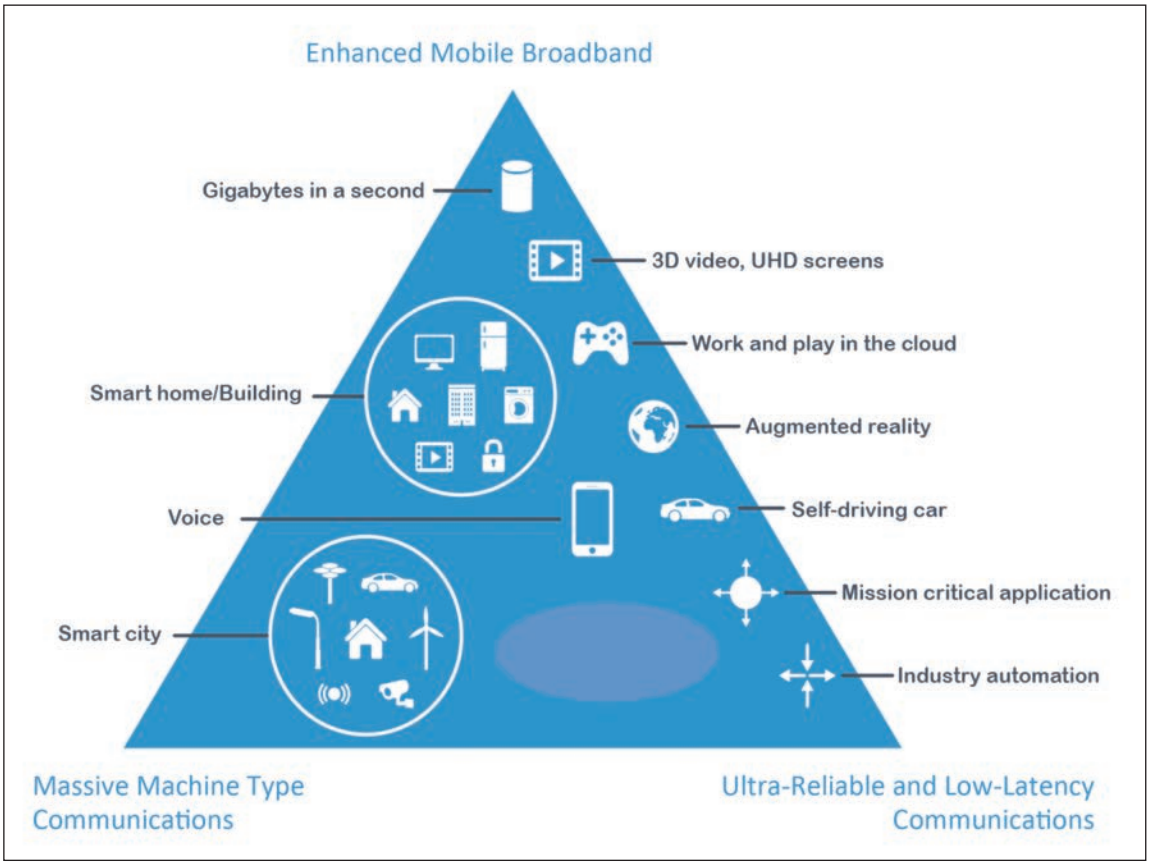
Next up could be LTE-Pro, which some people refer to as 4.5G. It can operate at 3.4-3.8 GHz. "Systems are in field trials today," revealed O'Neal. "We are getting about 1 Gbit/s with these systems."

Over the years, significant progress has been made in the amplifiers for future mobile infrastructure, which could feature massive antenna arrays. O'Neal rammed home this point by comparing a 0.25 μm pHEMT technology from 2002 that delivered a power density of 650 mW/mm from a 4.3 mm by 3 mm chip, with a recent 2.6 mm by 0.9 mm GaN HEMT chip from Qorvo, made with a 0.15 μm process and delivering 2800 mW/mm. Advances included a slashing of size by 82 percent, and a fourfold reduction in power density.

Going with GaN

Offering another perspective on how the compound semiconductor market will evolve with the emergence of 5G was Takahisa Kawai, general manager of RF device development at the Electron Devices Division of Sumitomo Electric Device Innovations.

Kawai began his talk by highlighting the dominant position that Sumitomo holds in the GaN power amplifier base station market. He first presented



5G will not just improve smartphones; it will also enhance machine-to-machine communications and aid the growth of the internet-of-things.

figures, based on ABI Research and internal estimates, that the base station RF power device market was worth $1.1 billion in 2014, with GaN taking an 11 percent share and silicon LDMOS 88 percent. He went on to predict that "GaN will overtake LDMOS within three years" and claim that Sumitomo is the world's leader in this wide bandgap technology. Sumitomo also produces GaAs devices for backhaul radio covering 4 GHz to 86 GHz, and it is developing GaN chips to supersede them.

According to Kawai, requirements for power amplifiers for 5G base stations include a low cost, RF power of between 0.2 W and 30 W, and operation in the 4 GHz to 6 GHz band and the 24 GHz to 86 GHz band. Additional requirements are low power consumption, small size, linear distortion and a broad bandwidth.

Given these requirements, GaN is the technology of choice, claims Kawai. That's because it is superior to silicon and GaAs in the most important metric for judging these classes of device, the Johnson figure-of-merit.

He noted that reductions in silicon devices to extend performance to higher frequencies lowered the operating voltage, leading to a diminished RF output power. Kawai pointed out that the biggest problem for 5G is that the specifications are still to be defined: "How do you know where to go if you don't have a roadmap?"

Like O'Neal, Kawai spoke about a technology that could provide a stepping-stone to 5G, and will use the 3.5 GHz to 6 GHz bands. The Sumitomo spokesman believes that the technology will have similarities to LTE-Advanced, and feature a wide bandwidth, carrier aggregation, and a mixture of GSM, CDMA, WCDMA and LTE technologies.

Kawai described a few of the company's products, beginning with a 3.5 GHz GaN power amplifier for LTE-Advanced networks. It adopts a Doherty architecture to improve the overall operating efficiency. In base stations, the average power is typically one-fifth of the maximum – a conventional amplifier would not be that efficient when operating in that regime. When configured in a Doherty configuration, however, the efficiency at relatively modest output powers is far higher. For an average output power, the efficiency can be 43 percent.

For amplification at 30 GHz, Sumitomo has GaAs chips that can deliver a peak power of 200 mW at a 20 percent efficiency. For multiple-in, multiple out links that are expected for 5G, the size of these chips

must be below 5 mm to ensure good beam steering. Sumitomo's devices fulfil this requirement, measuring just 1.8 mm by 1.6 mm. At frequencies of 30 GHz and above, wire bonding introduces variations that degrade yield. To address this, engineers at Sumitomo have developed a wire-free, direct-mount technology that uses solder balls to mount the chip to a printed circuit-board. This technology is also used for its 30 GHz GaN Doherty PAs that are currently under qualification. Built with a 0.15 μm process, two-stage prototype MMICs produce a peak power of 3W and 16 dB of linear gain at an efficiency of 26 percent.

Kawai revealed that in the company's research laboratory, engineers have fabricated InAlN/GaN HEMTs with a 0.1 μm process that have a cut-off frequency of 110 GHz. This technology is being transferred to the business group, where it will be used to develop 80 GHz power amplifiers for 5G base stations.

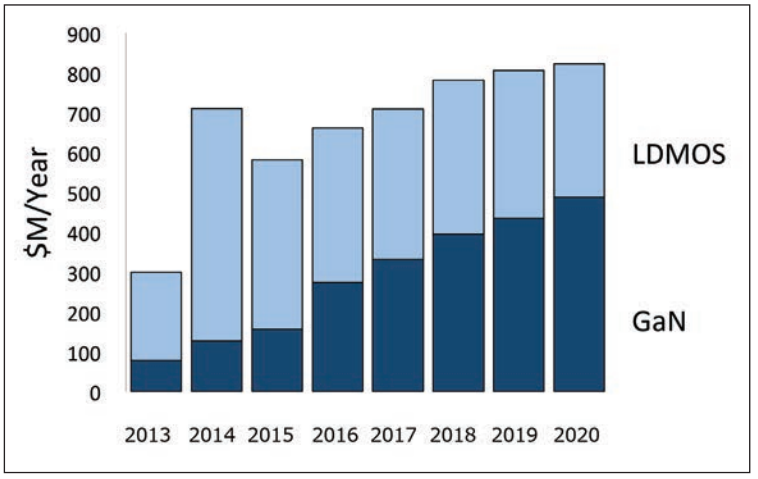
5G handset requirements

The impact of 5G on the handset was the focus of the presentation by Stephen Kovacic, Director of Technology at Skyworks Solutions. He began his talk by describing three of the biggest fears facing any teenager: that their mobile can't be connected, that it can't deliver an acceptable data rate, and that the battery will run out before it can be recharged. "We can't expect anything different when it comes to 5G,"claimed Kovacic.

According to him, one of the biggest differences between the development of 5G and its predecessors is that with this latest communication standard, the likes of Intel and Google are participating in attempts to define specifications. Like the other speakers in the session, he believes that progress is slow, citing issues that include the lack of a defined air-interface and uncertainties surrounding the frequencies used for communication links. He believes that there are very significant challenges for the front-end of the mobile, which are not being discussed at the system level.

These challenges, and the lack of standards, will hamper progress with 5G. However, Kovacic believes this form of wireless must be introduced, backing up this view with figures based on data from Cisco. They showed that cellular traffic will double from 8 exabytes per month this year to 16 exabytes per month in 2018, creating traffic volumes that will challenge mobile infrastructure.

Kovacic, like his peers from Qorvo and Sumitomo, expects the introduction of 5G to involve the use of new millimetre-wave bands, and massive multiple-input, multiple-output links. He picked up on the point raised by O'Neal that the power-to-average ratio of waveforms is set to increase, given that it has already shot up from 2:1 for 3G (WCDMA) to 5:1 for 3.5G (HSUPA) and 7:1 for 4G (LTE/OFDM).



The superior power density of GaN, compared with silicon LDMOS, will help this wide bandgap technology to dominate the RF power amplifier base station market.

To meet these requirements, Kovaic and his colleagues believe that the handset front-end is best served with a system-in-a-package, which contains a variety of technologies. It is argued that this not only leads to the best overall performance – it is cheaper, and it leads to a quicker time to market than an approach based on just one type of material. Kovacic claims that the optimum front-end for today's mobiles combines a power amplifier based on a GaAs HBT with silicon-on-insulator RF switches, filters based on SAW/FBAR technologies, and CMOS for other functions, such as the controller for the power amplifier. But when it comes to 5G, other materials will be considered. This includes InP, as HBTs made from this could replace those from GaAs, due to their faster switching time, higher power gain and superior efficiency. Note that all these benefits are available without an increase in power consumption.

The Skywork's spokesman concluded his presentation by revealing how quickly the company can respond to customer interest in new designs. Currently, following discussions, the first samples can be released in 6 months, compliancy with specifications met within 10 months, and a production ramp within just 12-14 months – and possibly sooner.

Kovacic expects these timings to not change when 5G modules are under development. That's clearly a strength for Skyworks, as given the great deal of uncertainty surrounding the specifications associated with 5G, it would not be surprising to find that its implementation will require chipmakers to rapidly move from sampling to high-volume production. Interesting times lie ahead.

Quantum tunneling boosts UV LED efficiency

High power, high efficiency UV emitters could result from the efficient tunneling injection of holes

BY YUEWEI ZHANG, SRIRAM KRISHNAMOORTHY, FATIH AKYOL AND SIDDHARTH RAJAN FROM THE OHIO STATE UNIVERSITY

EFFICIENT, COMPACT UV LEDs could serve many applications. These solid-state sources could be used for water purification, air disinfection and sensing, where they would replace bulky incumbent sources, such as those made from mercury.

Today, the UV LED is yet to fulfill this promise. Although commercial devices have been available for several years, there has been a low uptake of these sources. The primary barriers to widespread adoption are low efficiency and high cost – compared to the visible LED, efficiency is an order of magnitude lower, while cost can be more than a hundred times higher. Both inferiorities stem from fundamental differences between AlGaN, the ternary needed in UV LEDs, and InGaN, the alloy used for making blue and green emitters.

Our team at The Ohio State University is working to overcome these limitations by pioneering a novel device architecture. The emitters that we are developing are radically different from conventional UV LEDs, and employ a tunnel-junction to improve hole transport through the heterostructure. We believe that our device has the potential to slash the cost of the UV LED, while delivering a tremendous hike in its efficiency.

The lower efficiency of the UV LED, compared to its visible cousins, is highlighted in plots that graph external quantum efficiency and wall-plug efficiency as a function of wavelength (see Figure 1). For UV LEDs, the highest reported wall-plug efficiency value at 280 nm is only around 5 percent.

The root cause of this very modest efficiency can be uncovered by considering the factors that govern it: wall-plug efficiency is the product of internal quantum efficiency, electrical efficiency and light extraction efficiency.

Of these three, the internal quantum efficiency can now be a respectable 60 percent or more, thanks to efforts that have improved material quality. Carefully designed AlGaN-based buffer layers can control threading dislocation density and strain when UV LEDs are grown on non-native sapphire; while growth on native bulk AlN, grown by HVPE, offers a strong starting platform, thanks to a typical threading dislocation density of 10^3 cm^{-2}.

Dragging wall-plug efficiency down to less than 5 percent is the electrical efficiency and light extraction efficiency. Both are related to poor hole injection within the device.

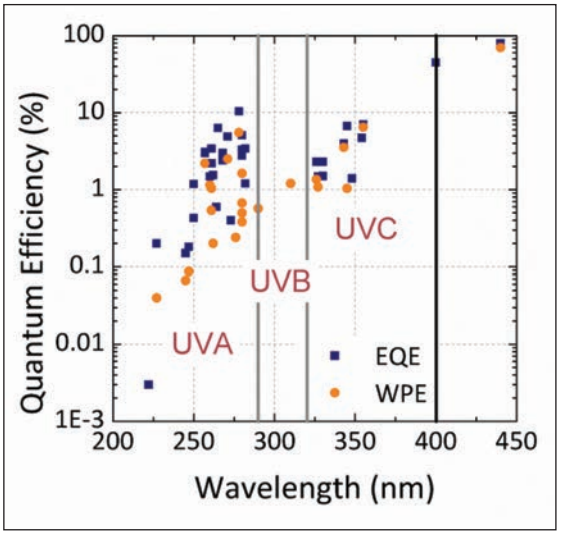


Figure 1. The highest reported external quantum efficiency (EQE) and wall-plug efficiency (WPE) values for UV LEDs.

The poor hole injection is caused by the low density of this carrier. It is a weakness that originates in the high activation energy of acceptors in high composition AlGaN – it is 0.62 eV in AlN, compared with just 0.14 eV in GaN. The upshot of the high activation energy is that it is almost impossible to make a direct *p*-contact to AlGaN in a conventional UV LED.

Popular approaches to overcoming this major limitation and improving hole injection are to add a *p*-GaN layer and to use a *p*-$Al_xGa_{1-x}N$/ $Al_yGa_{1-y}N$ superlattice (both options are illustrated in Figure 2). These solutions have their downsides, however. Although using *p*-GaN to inject holes can cut resistance and increase electrical efficiency, the bandgap of GaN is less than that of the emitted light, so absorption losses rise and extraction efficiency falls. Turning to the *p*-AlGaN superlattice avoids impacting light extraction, due to the higher bandgap, but it leads to a high resistance that reduces electrical efficiency.

The approach that we pursue, which is based on hole injection via a tunnel junction, has no major weaknesses because it does not lead to excessive absorption or electrical losses. The modification that we make to a conventional LED is to replace the hole injection layer with a UV transparent, conductive *n*-type AlGaN layer and a tunnel junction (see Figure 2). When designed correctly, the tunnel junction allows holes to 'tunnel' into the *p*-AlGaN layer, an approach that enables low resistance and ultimately high electrical-injection efficiency. Thanks to the transparency of the *n*-AlGaN top contact, this architecture also cuts optical extraction losses.

When UV LEDs that feature tunnel junctions are forward biased, by applying a positive bias on the top contact, the top tunnel-junction layer is actually reverse biased. This results in interband tunneling and hole injection into *p*-AlGaN (see Figure 3 for an energy band diagram of the device). The hole current that is injected into the active region is identical to the tunneling current, which is controlled by the voltage drop across the reverse-biased tunnel junction. So as long as the tunnel junction is well designed, it will have a low tunneling resistance, and the voltage drop across the tunnel junction layer will be far lower than that across the UV LED active region.

Converting the promise of a UV tunnel-junction LED into a reality is by no means an easy feat, because it is very tricky to make tunnel junctions work in wide band gap AlGaN. Forming a tunnel diode typically involves degenerate doping of both the p^+ and n^+ regions of the junction to form a narrow depletion barrier. Current flow through the junction originates from the quantum-mechanical tunneling of carriers through the thin depletion barrier, and if the bandgap of this layer increases, the tunneling probability decreases exponentially. Consequently, tunneling resistance increases exponentially with increases in the barrier's band gap (see Figure 4).

The major flaw with conventional AlGaN-based tunnel junctions that are suitable for UV LEDs is that they sport resistances in the 10-100 Ohm cm^2 range. This would lead to voltage drops of 1000's of volts! Obviously, such high resistances are impractical. The good news, however, is that the III-nitride system provides a unique tool – polarization – to overcome these limits.

Polarization promise

One of the key consequences of polarization is the high density of sheet charges at III-Nitride heterointerfaces. When a thin InGaN layer is inserted between *p*-type and *n*-type AlGaN layers, polarization charges at the AlGaN/ InGaN interface build up a high polarization field. This leads to dramatic band bending across the thin InGaN layer, so that the band edges of *n*-type and *p*-type AlGaN align over just a few nanometers (see Figure 3).

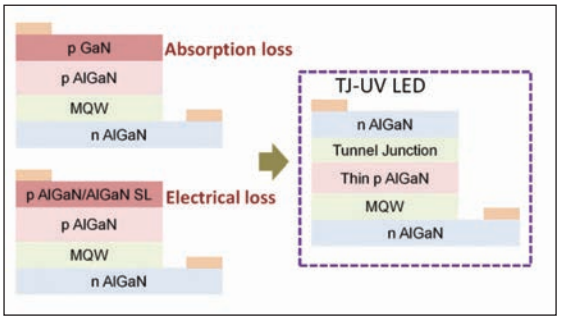


Figure 2. Switching from a conventional UV LED to a device that incorporates a tunnel junction leads to reduction in absorption and electrical losses.

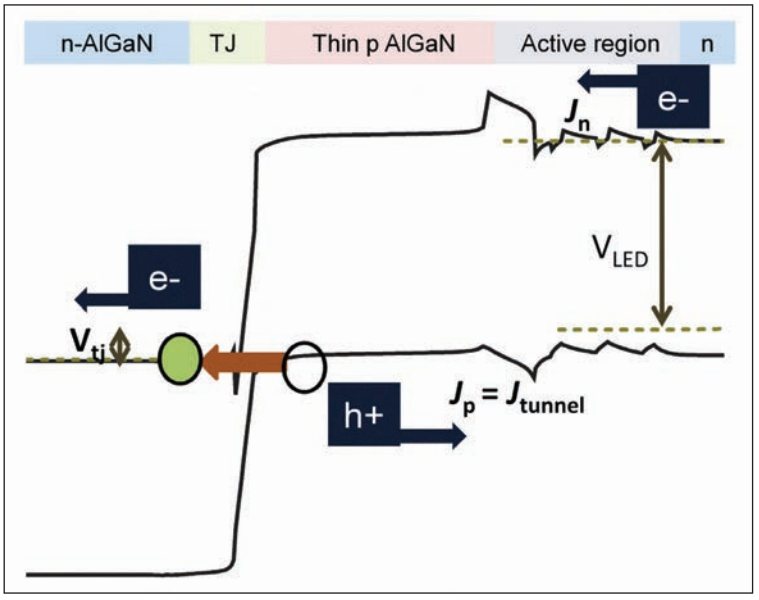
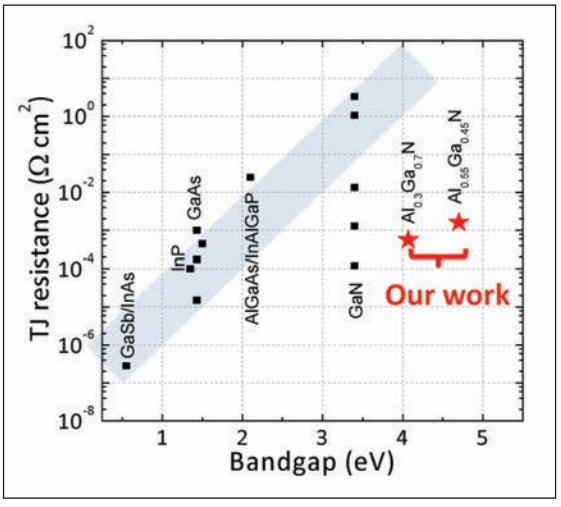


Figure 3. The band diagram of a tunnel-junction UV LED under operation.

Figure 4. Reported tunnel-junction resistances as a function of band gap energy for different material systems.



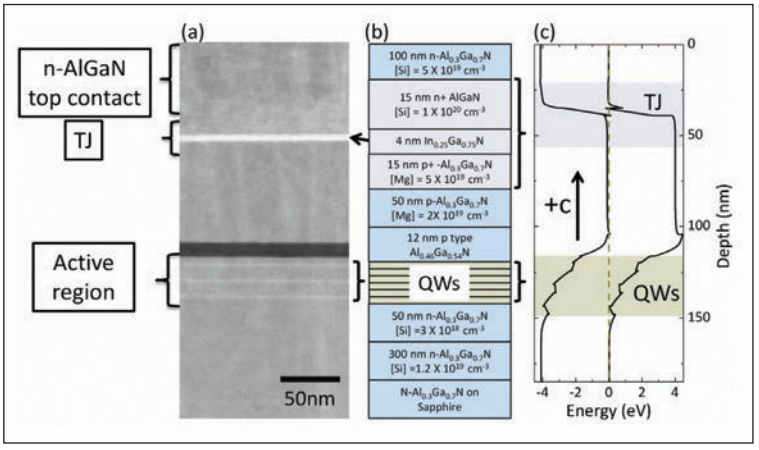


Figure 5 (a) High-angle annular dark-field scanning transmission electron microscopy (HAADF-STEM) image, (b) epitaxial stack, and (c) equilibrium energy band diagram of a tunnel-junction-based UV LED structure.

Inserting this thin layer of InGaN creates a triangular barrier that controls the interband tunneling. This is a bonus because this profile is more efficient for quantum mechanical tunneling. We combine *p*-$Al_{0.3}Ga_{0.7}N$ with an $In_{0.25}Ga_{0.75}N$ layer just 4 nm-thick and *n*-$Al_{0.3}Ga_{0.7}N$ to create a tunnel junction along the metal-face orientation. This spawns net positive and negative polarization charges at the top and bottom AlGaN/InGaN hetero-interfaces, respectively (see Figure 5).

Electrical measurements on our tunnel-junction UV LEDs reveal a sharp turn-on, with a voltage drop of 4.8 V at 20 A/cm^2. Cranking up the current density to 2 kA/cm^2 requires only 7.47 V (see Figure 6). We estimate that the resistance of the *p*-AlGaN/ InGaN/ *n*-AlGaN tunnel-junction layer is $5.6 \times 10^{-4}\ \Omega\ cm^2$, a figure that supports our view that polarization engineered tunnel junctions offer a low tunneling resistance for wide band gap materials.

Additional benefits that are demonstrated with these measurements are that the tunnel junction has a low resistance and introduces a low voltage drop, so it does not lead to a hike in LED power consumption. Another virtue of the tunnel-junction is that it cuts the overall device resistance, which trims Joule heating and increases device lifetime.

Better contacts

A further merit associated with incorporating a tunnel junction into the UV LED is that it allows a resistive, absorbing *p*-type metal contact to be replaced by one that is transparent, has a much lower contact resistance, and improves current spreading. Although the tunnel-junction introduces an absorption loss, this is estimated to be less than 4 percent, thanks to the InGaN layer being incredibly thin. In other words, photons can escape the top surface of our device with minimal absorption loss, enabling the demonstration of 327 nm devices with efficient, top-surface light emission (see Figure 7).

We have undertaken on-wafer power measurement on our devices. Results obtained without an integrating sphere reveal a maximum external quantum efficiency of 1.5 percent, and a wall-plug efficiency of 1.08 percent (see Figure 7). This indicates that the feeding efficiency – the ratio between the mean energy of the emitted photons and the voltage acquired by electron/ hole pairs – is 0.73. This high feeding efficiency is due to the voltage drop across the whole structure, which further confirms the benefit of using a tunneling contact over a conventional *p*-type contact. The low value for wall-plug efficiency is probably caused by the combination of an unoptimized active region design and a high dislocation density – it is in excess of 10^9 cm^{-2}.

We believe it is possible to address both of these weaknesses and go on to produce UV LEDs that set

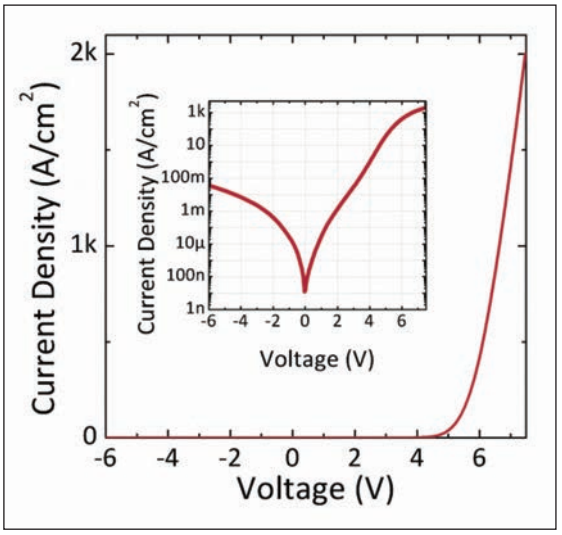


Figure 6: Current-voltage characteristics of the tunneling injected UV LED (50 μm × 50 μm).

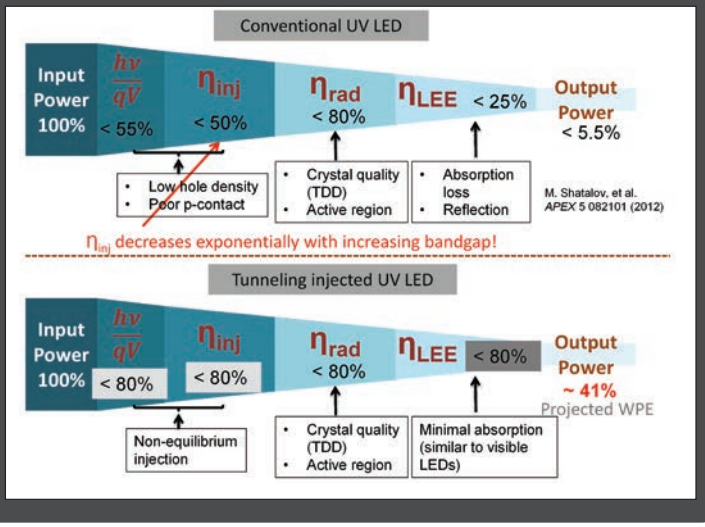
a new benchmark for wall-plug efficiency and device operation. Once this is accomplished, it should open the door to the manufacture of highly efficient UV LEDs that serve a wide-range of commercial applications.

But that's not all – the tunnel-junction might be able to inject a new lease of life into other classes of emitter, via the creation of tunneling injected laser diodes, multi-color light sources, and LEDs with multiple active regions that deliver a hike in output power while cutting chip costs. So, in the years to come, don't be surprised if you hear more about the virtues of the tunnel-junction in optoelectronic devices.

UV LED efficiency: The benefit of the tunnel junction

CONVENTIONAL UV LEDs are limited by: low electrical efficiency, due to a low thermal-activated hole density and poor *p*-type contacts; and poor light extraction efficiency resulting from high absorption loss and internal reflections. The wall-plug efficiency is limited to below 5.5 percent, and it can be even less than this at shorter wavelengths, due to more challenging hole injection problems.

In comparison, tunneling injected UV LEDs promise far higher wall-plug efficiencies – they could exceed 40 percent. Increases in efficiency over conventional UV LEDs result from a combination of high electrical efficiency that stems from non-equilibrium hole injection, and enhanced light extraction efficiency that is a result of the use of a transparent contact/ spreading layer.



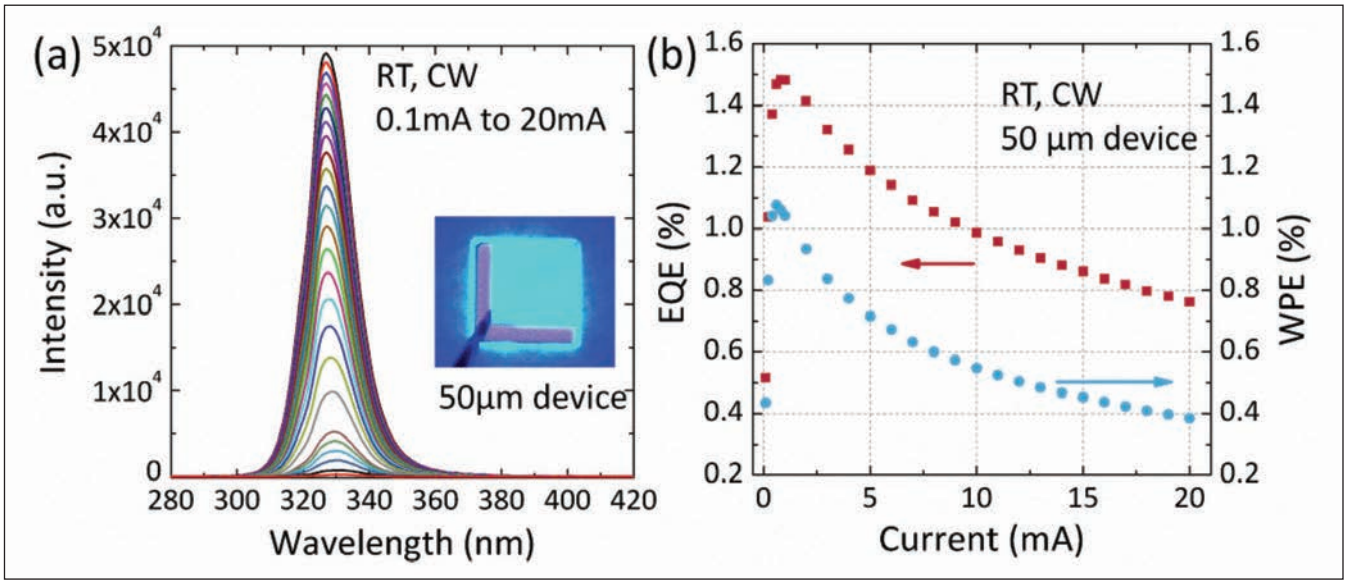


Figure 7 (a) Electroluminescence of a tunnel-junction UV LED structure with single peak emission at 327 nm. The inset shows an optical micrograph of a tunnel-junction UV LED device (50 μm × 50 μm) driven at 10 mA. There is partial top metal coverage, which appears as a dark region in the image. (b) External quantum efficiency and wall-plug efficiency of the device. Measurements are on-wafer, without using an integrating sphere.

CSindustry awards2016

WINNER

INNOVATION AWARD

SensAline tunable laser

BROLIS SEMICONDUCTORS

SensAline is a low-cost, small-footprint mid-infrared tuneable laser for spectroscopy and seeding applications. The heart of the laser is Brolis' GaSb type-I gain-chip embedded in an external cavity laser configuration.

This gain chip is based on a direct optical transition in GaInAsSb quantum wells. It combines the highest possible optical gain with a low operating voltage and an excellent gain-bandwidth product in the wavelength range at 2 μm and beyond. When integrated into an external cavity configuration, this gain chip allows more than 100 nm of wavelength access per chip with a very narrow linewidth and high output power.

Wavelength selection is achieved by rotating the diffraction grating, which provides optical feedback into the resonator. After selecting the wavelength, the grating is fixed and fine tuning is achieved by controlling the heatsink temperature, current and the piezo element which deflects the diffraction grating on a micron scale. This cretaes a monolithic, mechanically stable single-frequency laser with enhanced fine tuning capability.

This laser addresses the challenge of access to otherwise exotic wavelengths in the 2-3 μm range with unmatched performance. A single gain-chip can be used to cover more than 100 nm of spectrum, enabling less than ten gain chips to span the entire 2-3 μm range.

This allows tproduct costs to come down due to the reduced number of wafer growths and fab runs required for each wavelength access. For instance, compared to DFB lasers, covering the same spectrum would require a new wafer growth every few nanometres, resulting in high-cost.

Kristijonas Vizbaras, CTO of Brolis, and Augustinas Vizbaras, Head of Chip Technology

Since the sensing market is an early stage emerging market, products such as SensAline allow access to high-performance light sources at exotic wavelengths at otherwise unmatched cost. This enables new product and new application development that can use the availability of the new technology.

While SensAline is a discrete laser and is focused on research lab applications, the technology that is based upon can be scaled to mass-market, and is compatible with integration with silicon, to form on-chip silicon photonic devices. In order to reach such a stage there has to be a reasonable technology, application and market awareness built for which SensAline is ideal.

With SensAline on the market, customers benefit from easy access to an otherwise difficult spectral range in combination with enhanced output configurability (three tuning regimes, high CW output power and high finesse) compared to existing products.

This availability will open new horizons in the field of molecular sensing, mid-infrared laser seeding and enabling health applications.

Judges Comment:
"Brolis' devices promise to cut the cost of gas detection in the very important spectral band between two and three microns."

HIGH VOLUME MANUFACTURING AWARD

CSindustry awards2016

WINNER

AIX G5+C

AIXTRON

THE AIX G5+C is a complete solution addressing the epitaxy production needs of the GaN-on-silicon LED and power device industry. In a bridge 8 x 150 mm and 5 x 200 mm configuration it focusses on the future's most relevant wafer diameters for the production of blue LEDs and GaN power HEMTs.The product is resolving the common challenges of high-yield, high-quality and high-throughput production of AlGaN-based material on large area silicon (111) wafers in high-volume manufacturing through two key innovations.

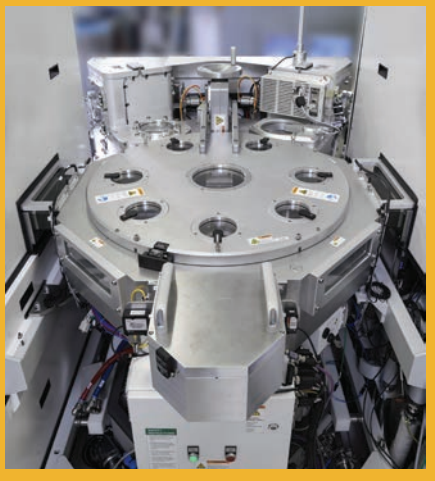
For the first time, a MOCVD batch system is equipped with a fully automated wafer cassette-to-cassette loader. This tool simplifies the handling of large silicon wafers in a fab environment and warrants production at thehighest yields. The wafers are loaded in 150 mm or 200 mm cassettes into a vacuum elevation chamber. On a customised separation station the wafer and the individual wafer carrier are combined and afterwards moved into the MOCVD chamber, which is kept ready for process at high temperature. The innovative wafer loading sequence enables a gross throughput advantage of up to 33 percent for a standard three-hour HEMT process cycle.

A thermally activated gas etch of the MOCVD chamber was developed to fully remove all deposits from the inner reactor chamber parts. This etching cycle after a process run quickly restores the original reactor conditions which is instrument for highest process reproducibility and quality.

Any cross contamination of the silicon surface during the start of the process is eliminated, leading to a defect free wafer bevel and meeting the strict defect requirements of large-area chips. The complete process flow is managed through a new user Interface enabling, for the first time, a truly fully automated production.

Frank Wischmeyer, Vice President Marketing & Business Development Power Electronics accepts the award.

LED and power HEMT device manufacturers are searching for solutions to incorporate a complex MOCVD technology into standard CMOS lines for 150 mm and 200 mm manufacturing. Up to today the 'human factor' had a strong influence on the performance of MOCVD related technology. Manual interaction with the system in process chamber maintenance actions, and the manual loading of the wafers, expose risks to system performance reproducibility, epi-defects and epi-wafer level product yield. By introducing full automation and a full chamber reset by ***in-situ*** cleaning to the MOCVD process technology the 'human' factor is reduced to a minimum.



Judges Comment:
"Two great opportunities to slash manufacturing costs are to scale to larger wafers and switch growth to silicon substrates. With Aixtron's latest tool, both options are readily available"

CS industry awards 2016

DEVICE DESIGN AND PACKAGING AWARD

WINNER

Laptop power converter using GaN

CAMBRIDGE ELECTRONICS (CEI) was founded in 2012 with the mission to reduce the world's electricity consumption by developing new energy-saving solutions based on GaN electronics.

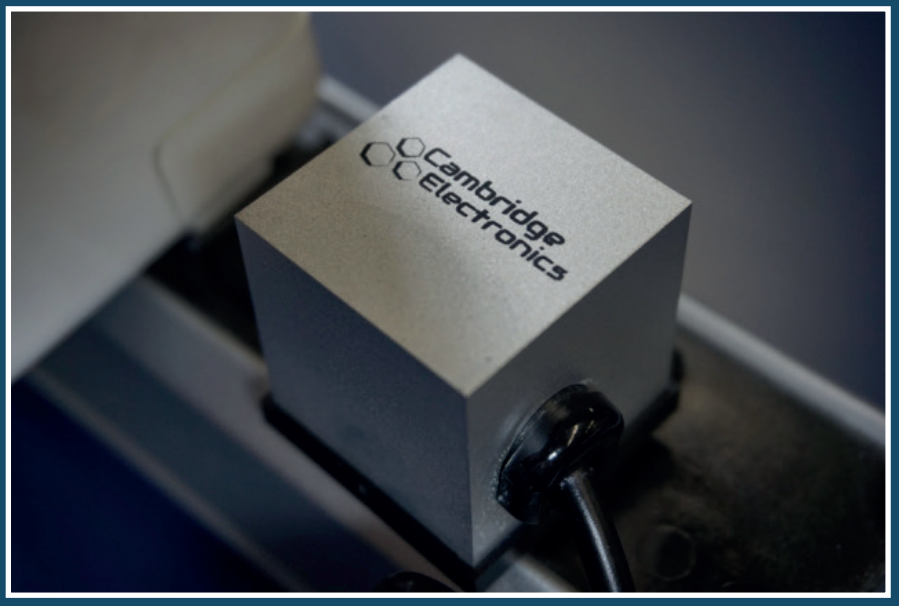
Due to its intrinsic material properties, GaN transistors have the potential of reducing losses in power conversion by more than 50 percent while providing a 10-fold increase in power density. Traditional GaN transistors are however normally-on, which makes them unsafe for power conversion.

CEI's proprietary GaN technology features normally-off operation and is compatible with existing gate drivers to allow for easier incorporation in existing power electronics applications. CEI's GaN transistors are fabricated in standard silicon fabs, which enables much lower cost than conventional GaN devices, and both normally-on and normally-off transistors can be fabricated on the same die, allowing unprecedented levels of system integration.

Thanks to all these unique features, CEI's revolutionary technology is changing the form factor and increasing the efficiency of a wide variety of applications, including laptop power adapters and other power conversion circuits.

Judges Comment:
"With developments such as Cambridge Electronics GaN transistors, the time has now arrived for GaN power electronics to fulfil its potential and start taking significant market share from silicon."

Stephen Whitehurst, COO of Angel Business Communications collects the award on behalf of Cambridge Electronics



METROLOGY AWARD

CS industry awards 2016

WINNER

inVia microscope for examining SiC substrates

RENISHAW apply innovation™

RENISHAW'S inVia Raman microscope is a high-performance spectrometer that enables the determination of crystal form, quality, and the nature of defects in SiC and other compound semiconductors, as well as the stress and free carrier concentration distribution. It acquires spectra incredibly quickly and generates Raman images that reveal chemical and physical information about samples. The properties of SiC are highly dependent on its crystal structure (it can exist in many polytypes), on the quality of the crystal, and on the number and types of defects present. Manufacturers of SiC raw material and devices need to monitor and control these attributes to enhance yield.

The first step in controlling these parameters is to measure them repeatably and quantifiably. Raman spectroscopy is a non-destructive technique that can provide sub-micrometre-resolution information on the composition, physical structure, and electronic structure of materials. Raman microscopy can expose problems that can occur during the manufacture of substrates and the growth of epiwafers.

Analysis is non-destructive, can be of a tiny region or a whole wafer, and can reveal surface, and subsurface, information in three dimensions. Defects originating in the substrate can be discriminated from those just in the epilayer. This gives valuable insights into the origin of defects and can help guide work to eradicate or control them. Thanks to its efficient optical design and fast detectors, the inVia can map a 3-inch SiC wafer in minutes.

The inVia is an automated system with a built-in health-check feature and automated calibration that ensures it is correctly aligned. This makes it an easy-to-use instrument and a quick analysis option for industrial quality control. It provides key information about SiC in practical timescales and greatly extends the potential of Raman spectroscopy in SiC research and development.

Philippe ReindersFolmer, General Manager, Benelux, collects award from Richard Stevenson, Editor of *Compound Semiconductor* Magazine.

The inVia's new LiveTrack focus tracking technology opens up even more opportunities for advanced SiC research. The bowing of some SiC wafers, caused by stress, can be problematic for Raman mapping. However, the inVia's continuous real-time focus tracking system enables even highly-bowed wafers to be successfully mapped. With no sample preparation required, whole wafers can be analysed at any stage of the production process, and without damage to the sample being analysed. The flexibility of the inVia enables it to also collect and analyse photoluminescence spectra, so both vibrational and electronic information can be obtained with just one instrument.

Whereas Raman analysis was previously considered a technique only of practical use to those versed in the art of optical alignment, the inVia confocal Raman microscope now opens up the opportunity to study all semiconductors and superconductors, improving understanding of strain, stress, defects, contaminants and crystal quality.

Judges Comment:
"Raman spectroscopy has a reputation as a difficult, time-consuming technique. The inVia changes all that, making it easy and quick to gather Raman spectra and Raman maps."

CSindustry awards2016

SUBSTRATES & MATERIALS AWARD

WINNER

GaN-on-silicon materials development with 200 mm wafers

imec

imec's R&D program GaN-on-silicon was launched to develop GaN technology towards industrialisation. It brings companies in MOCVD growth and metrology equipment, substrate suppliers and IDMs together to push GaN-on-silicon technology to a higher level of maturity and reliability, and to explore new concepts for next-generation GaN technology.

In 2015, breakthrough results have been obtained for dispersion-free buffers on 200 mm diameter substrates. imec investigated three types of buffers and individually optimized them for forward and reverse leakage from 25°C to 150°C, crystal quality and bow control. For the optimisation of the dispersion imec systematically used extensive trap spectroscopy to identify the physical nature and spatial location of the traps in the complex buffers.

imec selected the 200 mm GaN-on-silicon buffers by qualifying the buffers for large area high-performance E-mode HEMTs and low-leakage/low turn-on voltage Schottky diodes in its 200 mm gold-free and CMOS tool compatible GaN platform process. To bring the technology to a higher level of technology readiness, imec shares industrial aspects such as cost of ownership, process uniformity and repeatability, statistical process control and yield, and substrate and device qualification from 25°C to 150°C with partners.

While dedicated to continuously improve today's GaN-on-silicon technology, imec also prepares for next generation GaN technology. Based on its track record in GaN epitaxy for large diameter wafers, and the strong involvement of its industrial partners in MOCVD equipment and substrate suppliers, imec is well placed to identify the limitations and boundaries of the present GaN-on-silicon technology, and to mitigate the inherent problems with the mismatch in thermal expansion coefficient between the silicon substrate and the GaN buffers, lattice mismatch and stress management.

Denis Marcon (left), Business Development Manager and Yoga Saripalli (right), Team Leader Gallium Nitride, collect the award

Next to the development and optimisation of GaN buffers on top of engineered substrates and qualification on the power device level, engineering aspects like contamination control, substrate labelling and robot handling in the processing tools are addressed.

Judges Comment:
"These epiwafers will help to bring down the cost of GaN power electronics, and drive the growth of this sector."

CSindustry awards 2016

WINNERS

Sales of compound semiconductor chips are soaring. This is being driven by an uptake in solid-state lighting; rising revenues for smartphones, which are packed with GaAs chips in their front-ends; a build-out of capacity in optical networks; and greater use energy-saving, SiC and GaN devices in power electronics. These sectors are driven by companies making important progress. But which of them has made the biggest breakthrough this year, or the most important contribution?

High-Volume Manufacturing Award
AIXTRON SE
AIX G5+C

Substrates & Materials Award
imec
GaN-on-silicon materials development with 200 mm wafers

Metrology Award
Renishaw
inVia microscope for examining SiC substrates

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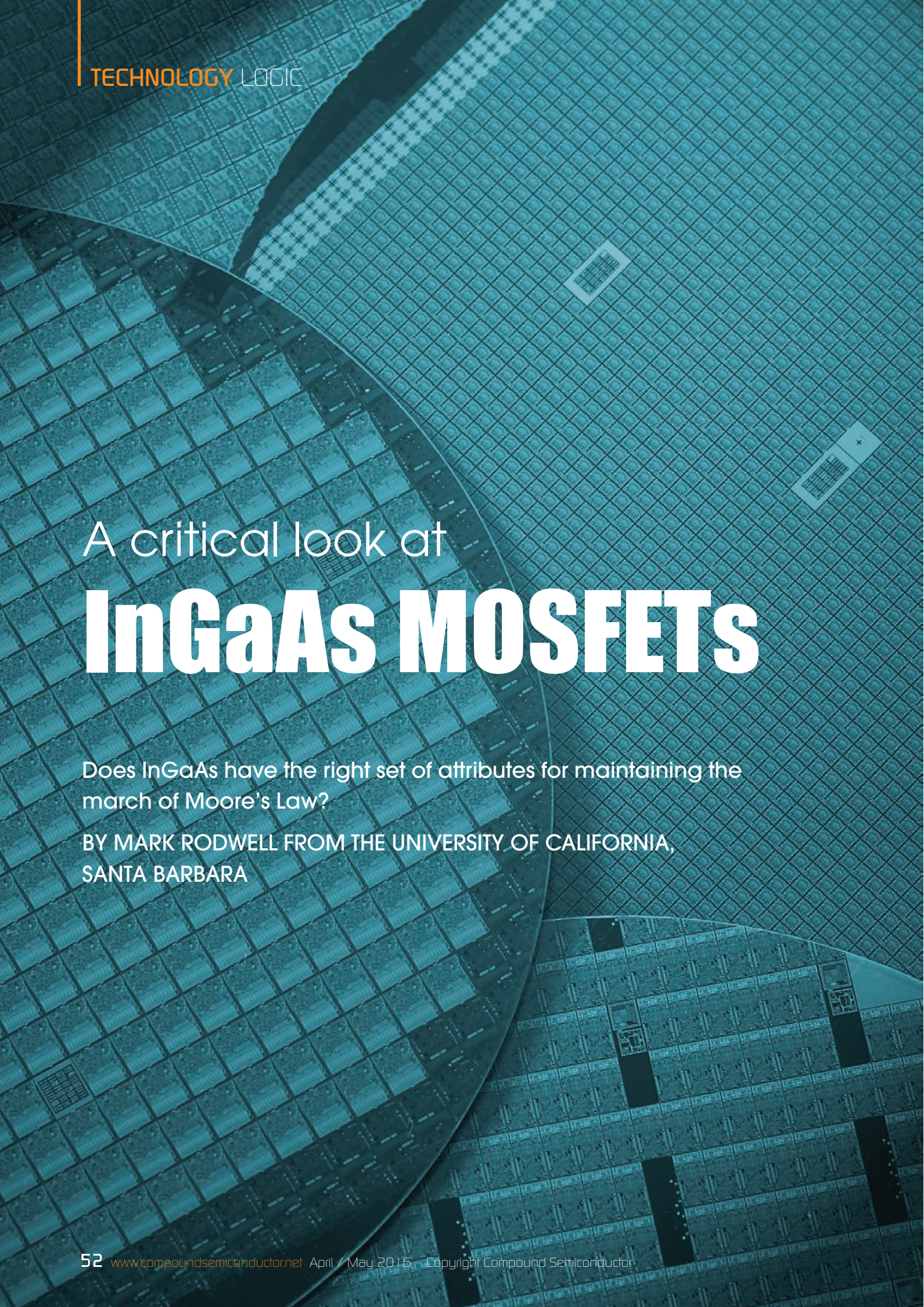

A critical look at InGaAs MOSFETs

Does InGaAs have the right set of attributes for maintaining the march of Moore's Law?

BY MARK RODWELL FROM THE UNIVERSITY OF CALIFORNIA, SANTA BARBARA

MOVING FROM one node to the next is getting ever harder. Back in the twentieth century, progress just involved shrinking the size of the silicon transistor. But since the turn of the millennium, it has required major modifications to device design to maintain performance improvements with scaling. Changes to the transistor architecture have included: straining the channel, by inserting germanium into source and drain regions; switching the gate dielectric from silicon dioxide to hafnium dioxide to prevent leakage currents from escalating; and introducing a three-dimensional finFET to helps the gate maintain control over charge carriers in the channel. Further refinements are sure to follow, and may well include the introduction of new channel materials that sport a higher mobility. For the *p*FET, germanium is the most likely successor for the channel, while for the *n*FET it is some form of In(Ga)As – $In_{0.53}Ga_{0.47}As$, or InAs layers, or $In_{0.53}Ga_{0.47}As$/InAs laminates.

At first glance, these channel replacements have a lot going for them. Compared to silicon, In(Ga)As has a higher mobility and lower effective mass. Consequently, introducing this material could enable electrons to zip through the channel as faster speeds, and ultimately allow devices to operate at a lower voltage while maintaining the currents of the predecessors. That is a big deal, as it would allow an IC to maintain its power consumption while increasing transistor count, and ultimately lead to improvements in the performance and capability of battery-powered mobile devices, such as smartphones and tablets.

However, this line of reasoning might be too simplistic, as it might be the case that introducing higher mobility materials will fail to deliver increases in transistor performance at shorter nodes. At long gate lengths this will not be observed: in this regime, it has already be proven that the on-current of the FET is proportional to the electron mobility, and it increases when a silicon channel is replaced with one made from a III-V. But in leading modern VLSI technologies, gate lengths are 20 nm or below and the on-current is not strictly mobility-limited. Instead, at the limit of extremely short gate lengths, transport approaches the ballistic limit. In this regime, the transistor on-current is determined by the injection velocity of electrons into the channel. The low electron effective mass in InGaAs can still lead to larger on-currents than comparably scaled silicon FETs, but whether this is the case depends on the thickness of the gate dielectric and channel.

A more detailed look at the issues reveals that a low electron effective mass is actually a double-edge sword. Although it gives a larger electron velocity at a given kinetic energy, this benefit goes hand-in-hand with a reduction in the number of available quantum states within a given energy range. Due to this, the charge in the channel reduces, according to simulations by Massimo Fischetti from the University of Texas at Dallas. Since the current is the product of charge and its velocity, the reduced charge can offset, in whole or in part, the increase in on-current resulting from increased electron velocity (see Figure 1 for details). However, so long as the combined thickness of the gate dielectric and channel are relatively large, there is an increase in the FET on-current associated with the use of a low-effective mass materials such as InGaAs or InAs. Note that when extremely thin channels and dielectrics are deployed, this benefit diminishes.

Another insight provided by Figure 1 is that although InGaAs cannot out-perform silicon in the most highly-scaled MOSFETs, the increase of gate leakage current by tunnelling sets a lower limit to the gate dielectric thickness. As this figure assumes a ballistic limit to transport, the relative performance of silicon and III-V transistors also depends on how close these two materials get to this limit.

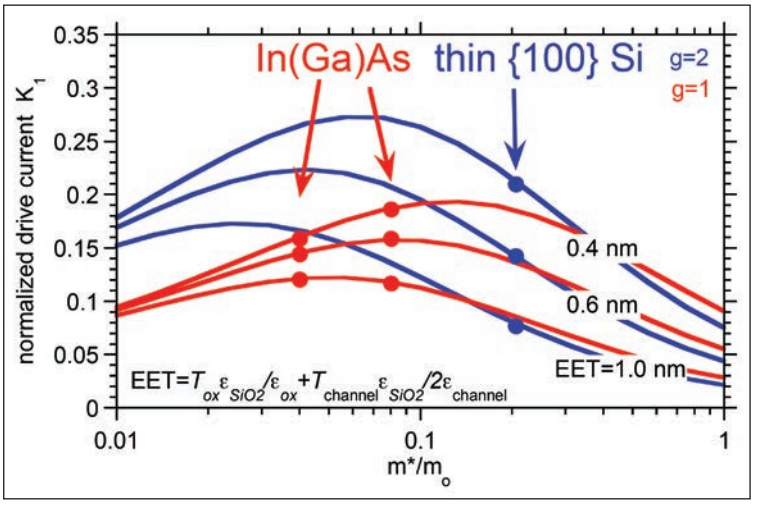

Figure 1: A simplified expression for the on-current, valid for $(V_{gs}-V_{th}) >> kT/q$, gives the FET on current, in mA per micrometer of FET gate width as $J = K_1 \cdot \left(84\frac{\text{mA}}{\mu\text{m}}\right) \cdot \left(\frac{V_{gs}-V_{th}}{1\text{V}}\right)^{3/2}$. This can be used to compare the performance of InGaAs and silicon MOSFETs, by considering the normalized drive current K_1, in the ballistic limit, as a function of electron effective mass (given as a fraction of its free-space mass, m_0), channel and dielectric thicknesses, and number of conduction-band valleys. This plot shows that on-currents in InGaAs FETs should exceed those in silicon except when the gate dielectric and channel are extremely thin. Note that for the silicon MOSFET, the favourable case of a body or inversion layer with a sufficiently small thickness has been assumed, as well as occupation of only two of the six Δ conduction-band minima. Note also that more detailed expressions for the on-current are given in K. Natori J. Appl. Phys. Lett **76** 4879 (1994) and A. Rahman et. al. IEEE Trans. Electron Devices **50** 1853 (2003).

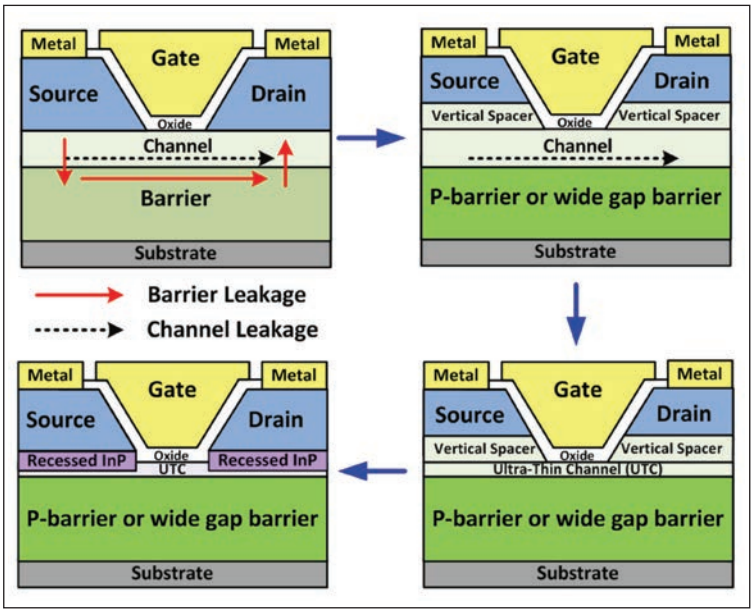

Figure 2. The progression of III-V MOSFET designs at UCSB for reduced off-state leakage current.

With silicon, thicker channels lead to the occupation of more conduction-band minima. As these valleys have a higher transport effective mass, on-current is reduced. Meanwhile, with III-V MOS, there are two key requirements for success: a low density of interfacial energy traps at the channel and gate dielectric interface, and the growth of low-defect density InGaAs layers on silicon. Ultimately, however, whether the III-V MOSFET has the upper hand over its silicon counterpart depends of a variety of device characteristics, such as injection velocity, channel mobility, the minimum technologically feasible thicknesses for the dielectric and channel, and source and drain access resistivities. The only way to determine the overall contribution is to undertake an experimental comparison of the two classes of device.

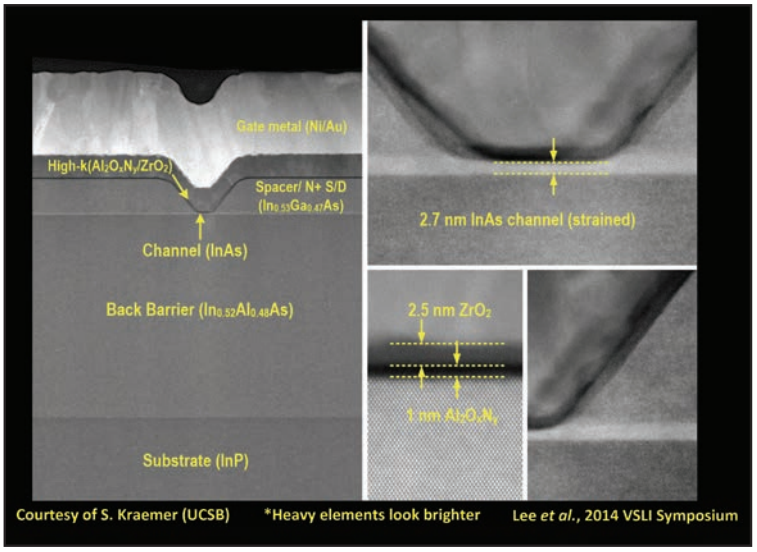

Figure 3. Transmission electron microscopy cross-section of InAs MOSFET with 2.7 nm InAs channel. Note that heavy elements look brighter. This image is courtesy of S. Kraemer, from UCSB. More details can be found at Lee et. al. 2014 VLSI Symposium

Off-state leakage

One of the biggest concerns surrounding the development of III-V MOS technology is the high off-state leakage current of these devices. The International Technology Roadmap for Semiconductors (ITRS) stipulates a maximum off-state leakage of 100 nA per micrometer of gate width for high-performance (HP) logic, 1 nA/μm for general-purpose (GP) logic, 30 pA/μm for low-power (LP) logic, and 10 pA/μm for ultra-low-power (ULP) logic. HP logic might be used in servers, GP logic in PCs and larger laptops, LP logic in smartphones and tablets, and ULP logic in ultra-long-battery-life devices such as Internet-of-things.

A major challenge facing III-V MOS is maintaining performance during channel and gate dielectric scaling. At long gate lengths, off-state currents arise in part from normal thermally-activated leakage, and sub-threshold characteristics can get as low as the theoretical limit of 60 mV/decade. But at short gate lengths, the sub-threshold swing can be far larger. To prevent this, the gate dielectric and the channel must both be thin enough to prevent any deterioration in the electrostatic control of the channel by the gate electrode. If the gate length in a planar III-V MOS has a length approaching 20 nm, then in order to maintain good electrostatic control, this transistor must have a channel that is no more than 5 nm thick, and the gate dielectric must have an equivalent thickness of around 0.8 nm. For three-dimensional devices, such as finFETs and nanowires, thicker channels and dielectrics are permitted.

One other difficulty facing the developers of III-V MOFETs is the selection of a suitable material for the gate dielectric. The chosen material must prevent high leakage currents and enable an acceptable density of traps at the dielectric-channel interface. Finding a high-κ dielectric for III-V semiconductors has been very challenging, with materials tried-to-date tending to produce high interface trap densities that lead to high sub-threshold swings.

In addition to the challenges of maintaining performance with scaling, and finding a gate dielectric that can lead to a low sub-threshold swing, developers of III-V MOSFETs need to craft devices with a low tunnelling leakage current, because this ensures a low off-state leakage. With InGaAs this is particularly tough: the low bandgaps of InGaAs and InAs cause very high band-to-band-tunnelling (BTBT) leakage currents, and the low effective mass can be to blame for very large source-to-drain tunnelling (STD) leakage currents. In In(Ga)As MOSFETs, both of these leakage mechanisms are pronounced, and get more severe as the gate length shortens. The BTBT may increase, due to a hike

in parasitic bipolar current gain, while STD leakage increases due to a shortening of the tunnel barrier.

Low-leakage III-V MOSFETs

Our team at the University of California, Santa Barbara, has been developing III-V MOSFETs for many years, and during that time we have refined the design of our devices (see Figure 2). The four architectures we have produced are different types of planar, ultra-thin-body transistors with either an InGaAs or InAs channel and a MOCVD-regrown, n^+ source and drain.

Device fabrication begins by MBE growth, patterning of a dummy gate, and a source and drain recess etch. Source and drain regions are added by MOCVD, before removing the dummy gate and adding a ZrO_2 dielectric by atomic layer deposition. A nickel gate is defined by a lift-off technique, before the addition of source and drain contacts completes MOSFET fabrication.

> One other difficulty facing the developers of III-V MOFETs is the selection of a suitable material for the gate dielectric. The chosen material must prevent high leakage currents and enable an acceptable density of traps at the dielectric-channel interface

To speed production, and hence development, our transistors are not self-aligned. This means that although we can fabricate gates as short as 10 nm, there are large overlaps between the gate electrode and the n^+ source and drain. Note also that our source and drain Ohmic contacts are more than 1 μm from the gated channel. In comparison, production III-V MOSFETs would be markedly different, because they would have: self-aligned gate, source and drain electrodes; nearly vertical sidewalls for the n^+ source and drain re-growths; and, to reduce capacitance, a low-permittivity dielectric spacer in the sidewalls between the gate and the n^+ source and drain.

The first step to address when lowering the MOSFET off-state leakage is to trim the substrate leakage current (see Figure 2, and compare top left and top right). When this is addressed by vertical confinement

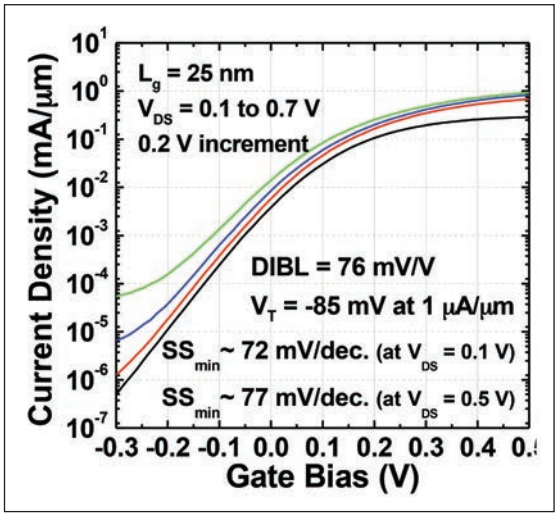

Figure 4. 2.7 nm InAs channel FET: sub-threshold characteristics at 25 nm gate length.

of the carriers to the channel by its interface with the bottom barrier, the InGaAs MOSFET has more in common with a silicon planar SOI transistor than a bulk silicon MOSFET. Yet, if the barrier is InAlAs, there is not a sufficiently large obstacle to electron injection from the n^+ InAs or InGaAs source. This hampers device performance, as it can result in significant leakage currents between the source and drain through the bottom barrier. Substrate leakage can be suppressed by inserting AlAsSb barrier layers, which have a higher barrier energy. A simple alternative is moderate p-type doping of the substrate or barrier layers.

The second major mechanism for off-state leakage in III-V MOSFETs is BTBT. This type of leakage is most severe in the high-field region. It can either be prevalent at the drain end of the channel, next to the gate edge, or at the junction between the channel and the regrown heavily-doped drain. Adding a lightly-doped spacer between the n^+ drain and the gate end of the channel can cut the BTBT leakage. This reduces the field and increases the drain-to-channel separation, leading to diminished electrostatic coupling between them. An upshot is improved electrostatic control of the channel by the gate, which enhances the transistor's turn-off characteristics.

One option for the spacer is a lightly doped lateral gap between the edges of the gate and the n^+ drain. However, if the distance of this spacer is a significant proportion of the gate length, this can cut the transistor packing density. A more attractive approach is to insert a lightly-doped semiconductor spacer during the regrowth sequence of the n^+ source and drain (see the device in the top right corner of Figure 2).

Further reductions in leakage result from the introduction of an ultra-thin channel (see Figure 2,

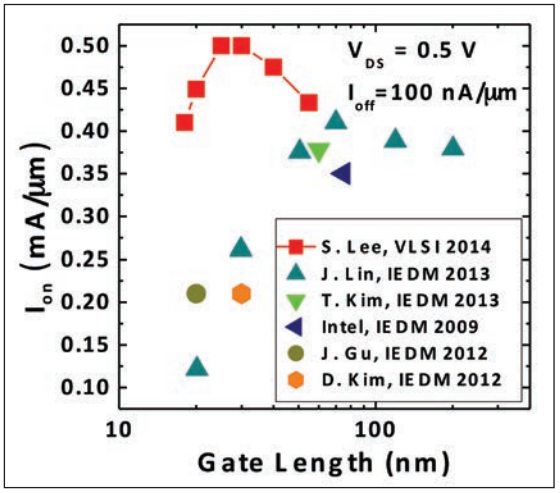

Figure 5. III-V transitors produced by the team at UCSB deliver a record on-current at a 0.5 V operating voltage.

lower right). Advantages of this include improved transistor electrostatics at short gate lengths, and an increase in the channel bandgap, via quantization, that drives down BTBT leakage.

We have produced a 25 nm gate length device with a 2.7 nm-thick InAs channel with this architecture (see Figure 3). The transconductance for this device, 2.4 mS/μm, is not a record for III-V MOS technology. However, that's not surprising, because thicker channels are needed for a higher transconductance – and that comes at the expense of larger off-state leakage currents.

The DC characteristics for this device include a (minimum) sub-threshold swing of 72 mV/decade (see Figure 4). Residual BTBT leakage is clearly evident, and when the gate is held at -0.3 V bias, the drain current ramps up with increasing drain voltage. Nevertheless, at the target 0.5 V drain bias that is expected to be used in next-generation ICs, the minimum off-state leakage is below 10nA/μm, well within the requirement for high-performance logic.

When engineers design a VLSI device, they select the gate metal for the appropriate threshold voltage and set the off-state leakage current target value defined in the ITRS. However, when producing an experimental

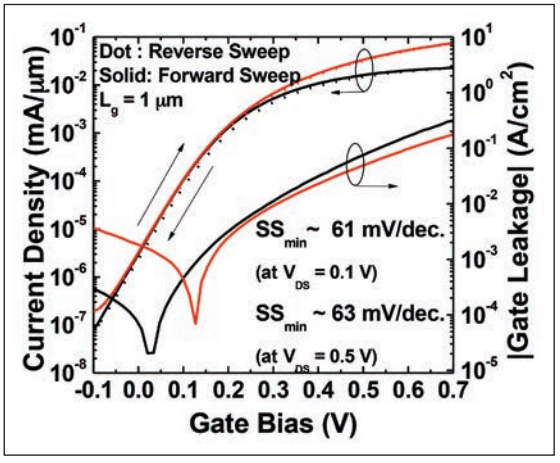

Figure 6. The sub-threshold swing for the 2.7nm InAs channel FET is very close to 60mV/dec., indicating a high-quality gate dielectric.

device in a research environment, it is inconvenient to shift the threshold. So, what we do is to numerically shift the threshold voltage in our data (see Figure 5), such that the off-state leakage becomes 100 nA/μm, the ITRS GP logic specification. This allows us to compute the on-state current at a gate-source voltage 500 mV above threshold (see Figure 5 for the resulting data, which shows, as a function of gate length, the on-current at a specified 100 nA/μm for a 500 mV power supply voltage).

Judged from a compound semiconductor perspective, this on-state current is very impressive, because it sets a new benchmark for what is possible with III-V MOS technology. However, the performance at a similar physical gate length is incredibly close to that of a comparably-scaled planar UTB silicon SOI MOSFET made by researchers from STMicroelectronics and the IBM Technology Development Alliance.

While there is no doubt that the ultra-thin channel and vertical spacers for the source and drain play a role in the high on-off ratio of our devices that are shown in Figure 3, the greatest contribution probably comes from the gate dielectric. We use a stack of AlO_xN_y and ZrO_2 formed by atomic layer deposition, a technology that has been developed by colleagues at our university, led by Susanne Stemmer.

The quality of this dielectric is highlighted by the sub-threshold swing for a long-channel device at a low drain bias. It is just 61 mV/decade, a value very close to the thermal limit, and the lowest reported for a III-V MOS technology.

If III-V MOS is to replace silicon in VLSI, it must offer a considerable performance advantage. As we have already stated, that is not the case today, as published state-of-art III-V data is only on par with the performance of the best silicon. However, it is possible that industry, with its superior fabrication resources, can demonstrate a better III-V device. One immediate opportunity for improvement exists in our non-self-aligned FET structure; with no low-ε_r dielectric spacer between the gate and the N^+ drain, leakage currents associated with gate-induced drain lowering (GIDL) are probably far higher in our devices than they would be in a properly self-aligned transistor.

At this stage, our devices at 100 nA/μm are suitable for ITRS HP (high performance but high power) applications. But if InGaAs MOS is to be a viable technology, it must also address at least the GP and LP market segments. The large mobile device markets, in particular, drive the LP and ULP technologies. To be able to meet these lower power requirements, we need to trim our BTBT leakage currents. There must be cuts in both the tunnelling leakage within the channel near the drain junction, and at the channel-drain junction itself.

One option is to replace the strained InAs channel (Figure 4) with either an $In_xGa_{1-x}As$ channel or

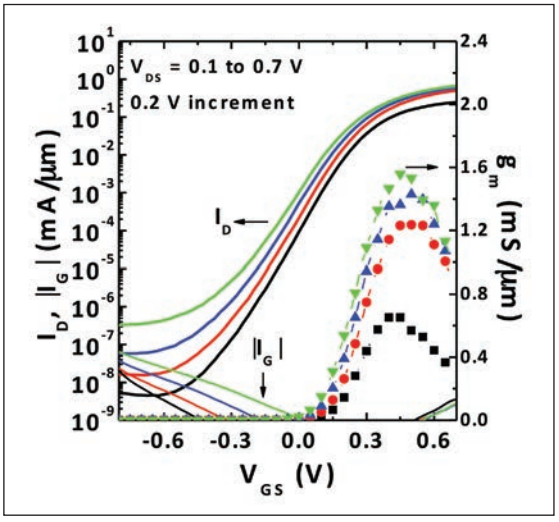

Figure 7. Sub-threshold characteristics a InGaAs/InAs-channel FET with 13 nm-thick InP source-drain vertical spacers having graded doping. The ZrO_2 gate dielectric is 3.8 nm thick, and the gate length is 30nm. The minimum off-state leakage is 60 pA/μm.

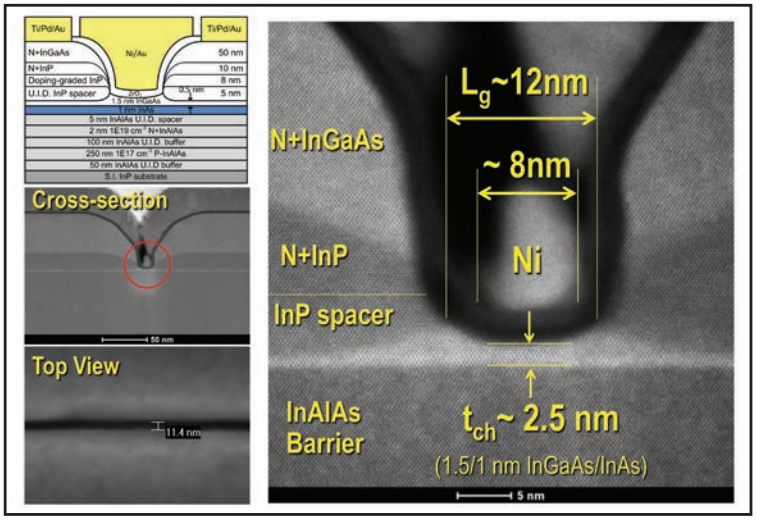

Figure 8. The structure (a) and TEM cross-sectional image, of a MOSFET with a 1.5nm InGaAs / 1nm InAs channel and a gate length of around 10 nm.

an $In_{0.53}Ga_{0.47}As$/InAs composite channel. These modifications will increase the channel bandgap, leading to a decrease in BTBT leakage within the channel and a reduction in off-state leakage. However, if the $In_{0.53}Ga_{0.47}As$ channel is thinned to less than about 5 nm, transconductance will plummet, leading to a lower on-current. The origin for this degradation is yet to be understood.

Addressing the BTBT leakage at the gate-drain junction holds the key to further reductions in the off-state leakage currents, which will enable devices to move close to the ITRS LP and ULP targets. This brings us to the final device design (Figure 2, bottom left), which features an undoped, wider-bandgap spacer layer, such as InP.

We have found that when these spacer layers are thick, this increases the source access resistance of the FET, leading to a lowering of the on-current (see Figure 7). It is possible to lower the access resistance and boost on-current by introducing a doping gradient within the InP spacer. This step ensures that the depleted region within the InP spacer is thinner in the source than in the drain. With this modification, at a drain bias of 0.5 V, the minimum off-state leakage is 60 pA/μm, which is close to the ITRS LP specification. Variations in transistor size do not lead to changes in this leakage, indicating that the figure of 60 pA/μm stems from surface leakage currents arising from inadequate device isolation. The internal transistor leakage current is smaller than this with a magnitude that is yet to be uncovered.

Further improvements in the off-state leakage are possible. According to our data, BTBT leakage can be driven below 60 pA/μm with a 5 nm InP spacer layer. Yet, we employed 12 nm-thick InP spacers, with the aim of maintaining good electrostatics – and hence a small sub-threshold swing and DIBL – at a 30 nm gate length. The downsides of such a structure are excessive source resistance and a reduced on-current.

A promising candidate for realising success on more fronts is the planar UTB device. If this were constructed with a composite spacer with an upper InGaAs layer and a lower InP layer, it might be able to combine reduced BTBT leakage with good electrostatics at short gate lengths and a low source resistance. Success would require grading of the InGaAs/InP heterointerface to suppress the influence of the barriers. An alternative is the finFET, which has superior electrostatics than the planar UTB, thanks to the double-gated structure. With this transistor architecture, a thin 5 nm InP layer in the drain re-growth would provide adequate BTBT suppression, rendering the additional InGaAs spacer unnecessary.

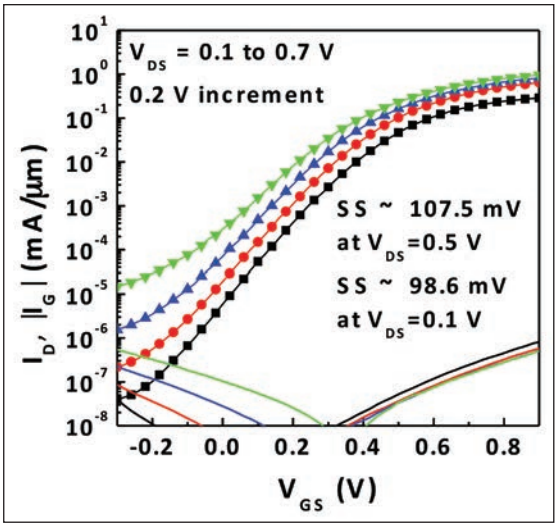

Figure 9. Log(I_D)-V_{GS} characteristics of the device of the device shown in Figure 8.

To evaluate what might be possible, we have fabricated In(Ga)As MOSFETs at the limits of the scaling of a planar UTB device. Our goal: to demonstrate that high on/off current ratios can be obtained in III-V MOS technologies, despite the potential for high band-to-band and source-to-drain tunnelling leakage currents associated with low carrier mass and small bandgap energies.

The transistor fabricated for this study has a thin composite channel with a 1.5 nm $In_{0.53}Ga_{0.47}As$ layer and a 1.0 nm InAs layer (see Figure 8). The regrown source and drain regions contain vertical InP spacers with unintentionally doped and graded-doped sections. The gate orientation on the wafer has been rotated by 90 degrees compared to earlier devices, a change that has resulted in more nearly vertical regrowth profiles on the n^+ source and drain.

These refinements have paid dividends. BTBT tunnelling is reduced by the InP spacers and the $In_{0.53}Ga_{0.47}As$ layer within the channel, while electrostatic short-channel effects and source-drain tunnelling leakage currents are reduced by the device geometric design: the transport path is curved and the channel is U-shaped, resulting in a net transport distance between the source and drain that is substantially larger than the horizontal footprint of the gate.

A curved channel is desirable, because it enables close device packing and enhanced DC performance. That's because the horizontal footprint determines the VLSI device packing density, while the transport distance governs short-channel effects and tunnelling.

DC measurements on our transistors reveal that the sub-threshold swing is too large for a production device (see Figure 9). However, our MOSFETs maintain a good control of off-state leakage, with the drain current varying by a 8.3 x 10^5:1 on/off ratio as the gate potential is swept from -0.3 V to +0.9 V.

The road ahead

Our efforts, and those of our contemporaries, have been motivated by using III-Vs in the channel, because it provides a low carrier effective mass and high carrier mobilities. Key findings that have emerged from our work include the realisation that if gate dielectrics can be further thinned, the low effective mass of such materials will fail to deliver a larger on-current than would be obtained with a silicon channel. We note, however, that it appears unlikely that gate dielectrics in VLSI can be made much thinner. We have also noted the need to address the low bandgap energies and low carrier masses associated with In(Ga)As, if this is to become a viable channel material in VLSI.

Additional insights by our team are that composite InGaAs/InAs channels with a thickness of just 2 nm to 4 nm can reduce tunnelling leakage in the channel, while the insertion of thin InP source/drain spacers can ensure low band-band tunnelling leakage in the high-field regions near the drain. Requirements for out-performing silicon are to understand and address the current collapse in sub-5 nm InGaAs channels, and to use no more than 5 nm in the drain spacer layers. Options for improving electrostatics are to employ composite InP/InGaAs spacers in planar UTB III-V MOSFETs, or to turn to finFET or nanowire geometries.

Even if III-Vs should not prove to be superior to silicon in conventional MOSFETs, efforts by ourselves and others will not have been wasted, because III-V MOS will remain an important technology for VLSI. That's because the low carrier masses and favourable energy-band alignments make III-Vs the leading contender for low-voltage, low-power tunnel-FET logic.

The author acknowledges the contributions of the collaborators on this work:
Sanghoon Lee, Cheng-Ying Huang, Varistha Chobpattana, Brian Thibeault, Bill Mitchell, Susanne Stemmer and Arthur Gossard.

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Quantum well intermixing:

The quest for orange and yellow lasers

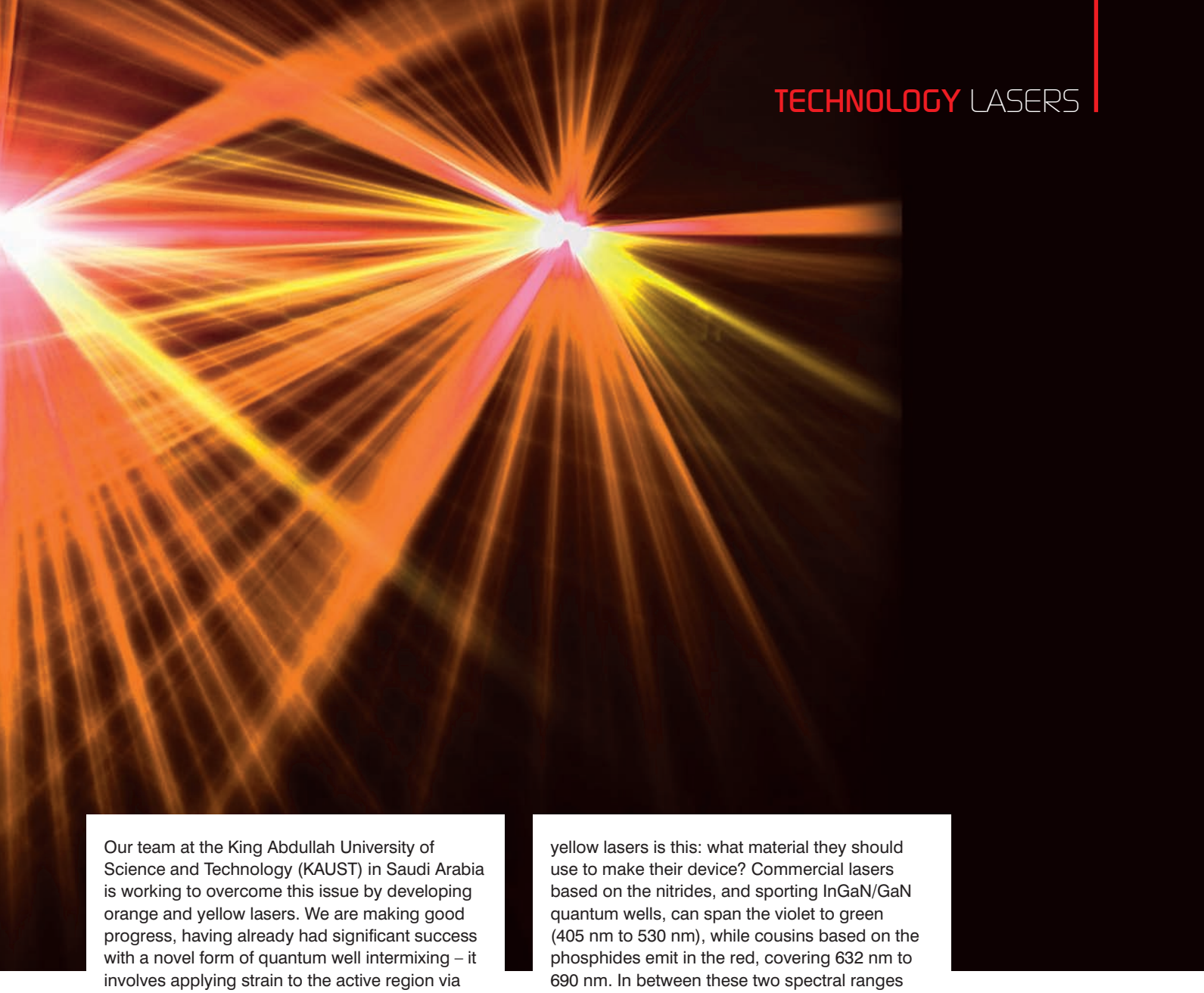
Yellow and orange sources result from the controlled annealing of phosphide material systems with a dielectric cap

BY ABDUL MAJID MOHAMMED, PREVIOUSLY WITH KAUST AND NOW AT EFFAT UNIVERSITY, AND BOON SIEW OOI FROM KAUST

THE LED LIGHT BULB is destined to consign incandescents and fluorescents to the history books. That's because this lighting source has much to recommend it – it is efficient, long lasting, and hits full brightness in an instant – and its sales are accelerating as prices plummet.

But the LED might not have the final say in the rise of solid-state lighting. In time, it could be superseded by white-light sources formed by mixing the output of diode lasers emitting at different wavelengths. Attractions of this laser-based technology are the promise of even higher efficacies, a superior colour quality and light-based communication rates that are an order of magnitude higher than those that could be produced by LEDs.

Before lasers can become the dominant source for solid-state lighting, however, there is a need to address their biggest weakness, which is their poor spectral coverage. Efficient blue and red sources are readily available, but losses rise in the green, and there are no commercial, directly emitting chips in the orange and yellow. This compromises the quality of white-light-based laser sources produced by colour mixing.



Our team at the King Abdullah University of Science and Technology (KAUST) in Saudi Arabia is working to overcome this issue by developing orange and yellow lasers. We are making good progress, having already had significant success with a novel form of quantum well intermixing – it involves applying strain to the active region via the growth of a SiO_2 film on top of the structure. Highlights of our work include fabricating a phosphide-based laser that operates down to 608 nm at room temperature, and the world's first yellow superluminescent LED. The latter produces a total output of around 5 mW at 583 nm.

What material?

One of the first questions that any researcher must face when attempting to build orange or yellow lasers is this: what material they should use to make their device? Commercial lasers based on the nitrides, and sporting InGaN/GaN quantum wells, can span the violet to green (405 nm to 530 nm), while cousins based on the phosphides emit in the red, covering 632 nm to 690 nm. In between these two spectral ranges there is the green-yellow-orange wavelengths of 530 nm to 630 nm, where no laser diodes are for sale.

If white-emitting light sources were made from what is commercially available, the colour-rendering index (CRI) would be limited to a value of 80 or less, which is not acceptable. To meet customer requirements, the CRI must exceed 90. This target can be meet, but requires lasers

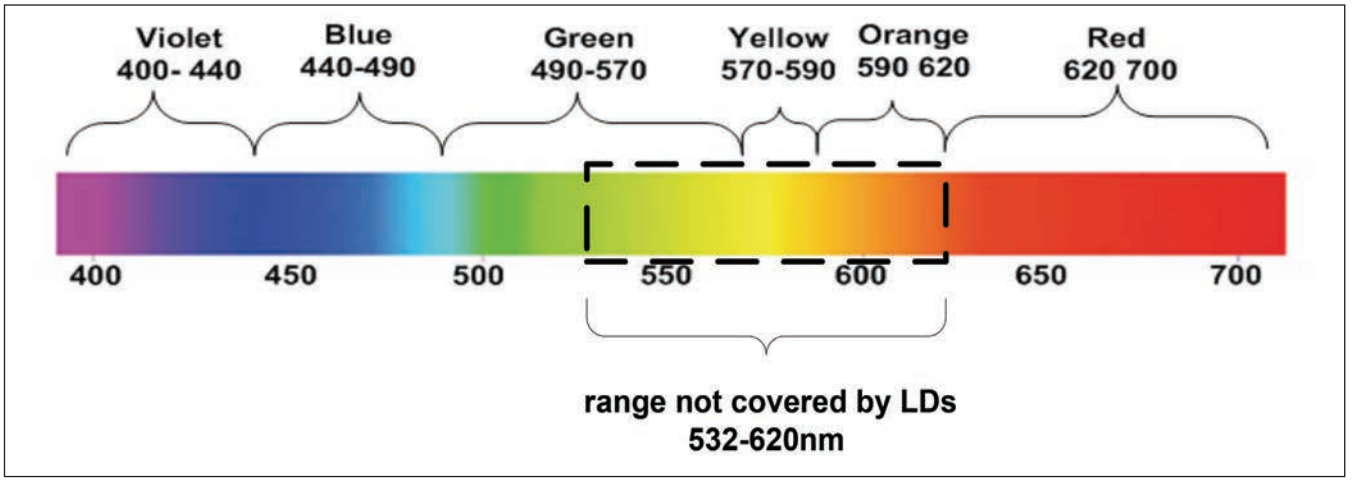


Figure 1: Neither the GaN/InGaN laser diodes (LDs), nor those made from InGaP/InAlGaP, can deliver emission in the yellow and orange.

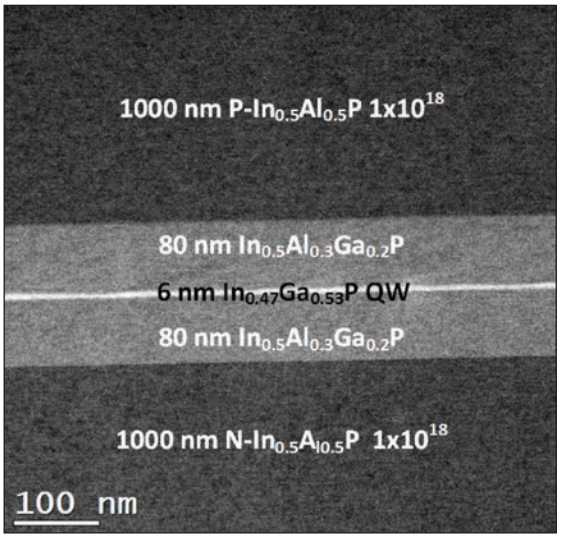


Figure 2: A transmission electron microscopy image of the InGaP/InAlGaP laser structure with an InGaP single quantum well.

to be used in conjunction with phosphors emitting in the green, yellow, and orange/red. However, this addresses colour quality at the expense of system efficiency, which falls due to the difference in energy between the photons that are pumping the phosphor and those that are being emitted by it – and also energy losses from some phosphors that are absorbing the light that other ones are emitting.

At first glance, it would appear that the best way to realise a high CRI with a phosphor-free system would be to extend the spectral range covered by either InGaP/InAlGaP or InGaN/GaN systems. With production of these classes of chips firmly established, manufacture could quickly follow development.

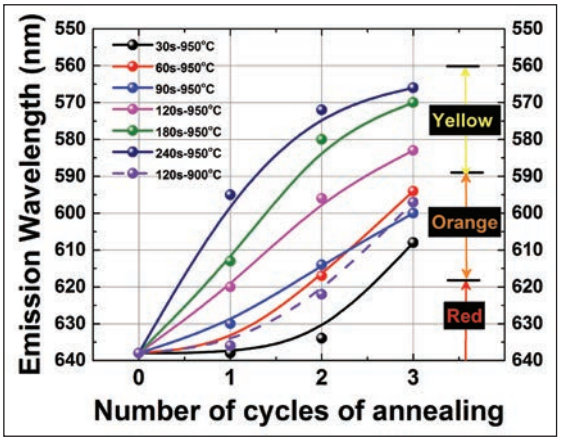


Figure 3: Photoluminescence peak emission of InGaP/InAlGaP laser samples capped with SiO_2 and annealed at 950˚C for 1,2 and 3 cycles. Also shown is the process at a reduced annealing temperature of 900˚C. Emission in orange and yellow was accomplished via different combinations of annealing time, duration and the number of cycles of annealing.

However, it is very challenging to have success with these material systems. Phosphide-based systems require an increase in the aluminium content to propel emission to the green-yellow-orange, but moving to shorter wavelengths reduces confinement of electrons and holes in the quantum wells, prohibiting the growth of efficient active regions. Efficacy takes a further knock from the tremendous hike in the density of the non-radiative centres.

With the nitrides, different issues are at play. The indium content has to increase to reach longer wavelengths, but this introduces significant strain in the quantum wells. Indium segregation can also occur, making it even harder to produce high quality green, yellow and orange sources.

Compromised solutions

Prior to our efforts, the only phosphide-based laser diodes emitting in the orange-to-green spectral range were chips held at cryogenic temperatures and subjected to high external pressures. Such devices clearly are impractical for commercial applications.

An alternative approach, which fails to tackle the issue head on, is to turn to frequency doubling of a diode-pumped solid-state laser or an infrared laser diode. One downside of this technology is that the non-linear crystals used for second-harmonic generation are not that efficient. What's more, they require an externally distributed Bragg reflector and a good heat sink, which increase complexity.

Another option is to use a gas-based laser. But these sources have sizes ranging from that of a shoebox to filling an entire room. So it is of no surprise that there is huge demand for a tiny chip that could replace these complex, expensive and power consuming lasers that emit within the colour gap.

Attempts to fabricate lasers in the colour gap date back four decades. During that time, much effort has been devoted to improving the epitaxy and design of phosphide-based material systems. The first milestone came in 1971, when a group at RCA Laboratories reported orange lasing with low-efficiency and high threshold current densities at 80 K. Two decades latter came the next significant breakthrough, when, in 1992, a team from Toshiba realised room temperature orange emission at 625 nm, with a device featuring six pairs of multi-quantum barriers. However, this emitter produced a very low output power. In 2003, another advance was reported – the fabrication of yellow-orange emitters, based on a strained InGaP quantum well, that were grown on a transparent, compositionally graded AlInGaP buffer. Although the devices did not lase, they set a new benchmark for LED power for this wavelength range, producing 0.18 μW per facet.

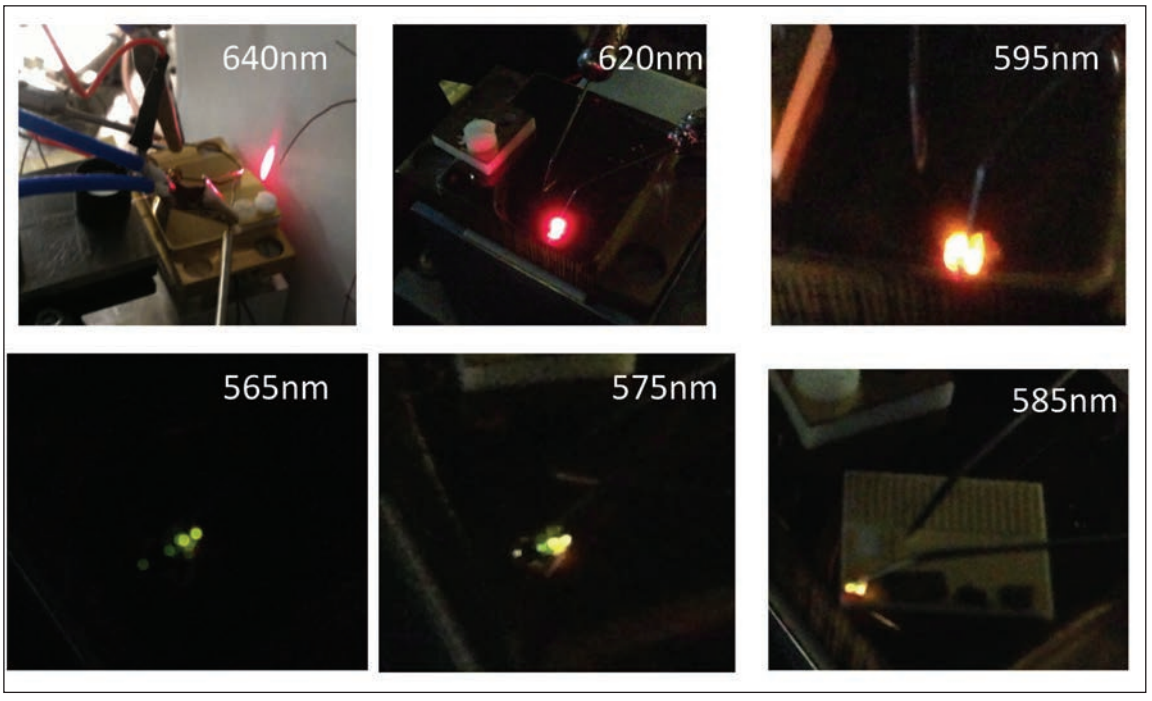


Figure 4: Intermixed laser structures with front and back contacts can span the red, orange, yellow and green.

Mixing the wells

An additional option for controlling the emission wavelength of a laser is quantum well-intermixing (QWI). This established technique is already used in the production of lasers, with pioneers including the maker of red and infrared sources, Intense of North Brunswick, NJ. Our contribution to this technology is its application to orange and yellow lasers.

The purpose of QWI is to selectively tune the band edge of a semiconductor heterostructure. The process for accomplishing this begins by forming a disordered region that is near to, but separated from, the quantum well active region. Annealing follows, driving the diffusion of vacancies/defects from the disordered region into the quantum well region, where they enhance inter-diffusion at the junctions between the well and barrier. Repeating this process of introducing disorder and subsequent annealing of the heterostructure shifts the bandgap to ever shorter wavelengths.

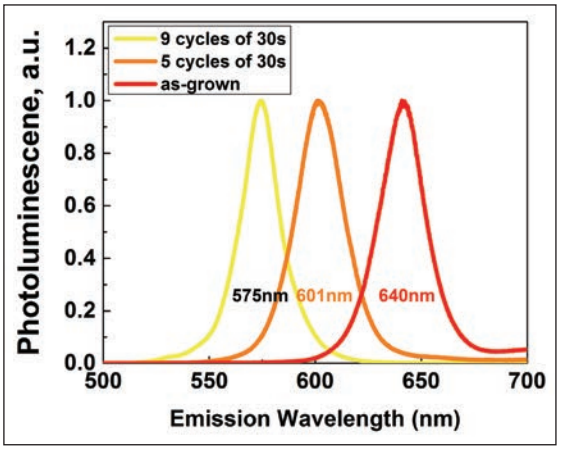


Figure 5: Optimized photo-luminescence sample after annealing at 950˚C for 9 and 5 cycles of 30s duration. These samples are used to fabricated orange laser emitting at 608nm and yellow super-luminescent diode at 583nm. Also shown is the photo-luminescence of the as-grown sample.

Only a handful of groups have applied the QWI process to devices that are made with the InGaP/InAlGaP material system and have wavelengths as short as 640 nm. These attempts have been unsuccessful, as there has been a minimal blueshift in the emission wavelength.

Multi-colour, monolithic sources

To produce monolithically integrated multiple photonic devices on a single chip, there needs to be a process for shifting the bandgap energy of a selected area to a value that is different from that of another area. With the quantum well intermixing process developed at King Abdullah University of Science and Technology (KAUST), the strain-induced disordering of the quantum well and barrier depends on the thickness of the dielectric. It is also possible to introduce different dielectrics, such as silicon nitride and silicon oxide, to induce different degrees of strain, and ultimately produce a different emission wavelength in a different area of the substrate. By adopting this type of approach, the team at KAUST have produced a multiple bandgap semiconductor light-emitting device.

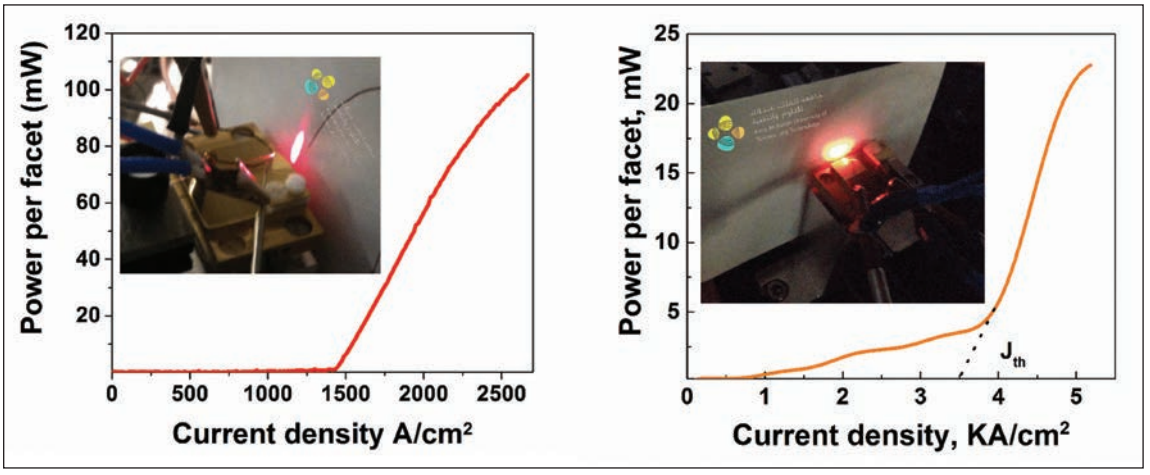


Figure 6: Power-current characteristics as a function of current density of (a) an as-grown red laser and (b) an intermixed orange laser. Inset: Red and orange lasing spot emitting at a current injection of $1.2J_{th}$.

One example of this is work by the team from Xerox:. They annealed as-grown and SiO_2 capped samples of InGaP/InGaAlP at 900˚C for four hours. The emission blue-shifted, but only by 10 nm.

It is worth noting that longer wavelengths have led to slightly more success, with a sample coated in a layer deposited by sputtering, rather than PECVD. This sample underwent a shift from 670 nm to 640 nm. However, this group from the University of Glasgow reported photoluminescence for devices cooled by liquid nitrogen, suggesting that the QWI process degraded the active layer. The researchers postulated that the intermixing created point defects at the sample surface, with damage in the *p*-cladding impairing device performance. The point defects are thought to originate from plasma-induced damage, which occurs when plasma species are accelerated across the space-charge region.

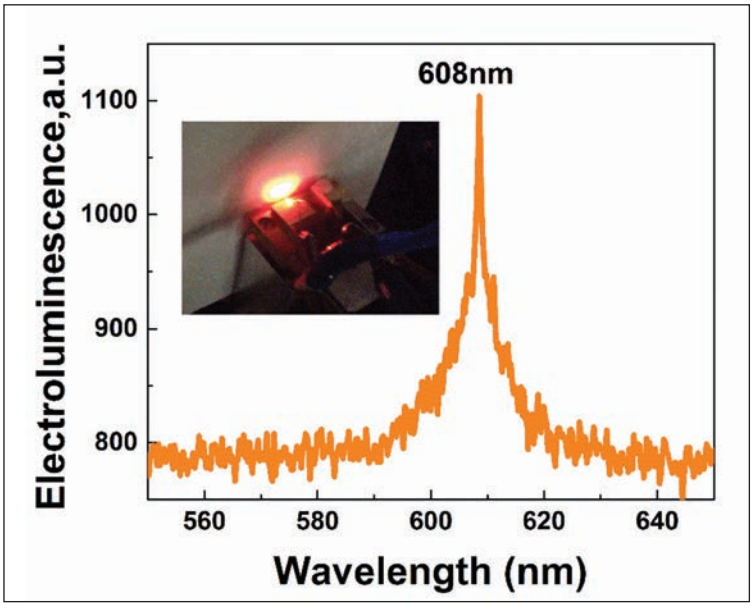


Figure 7: Room-temperature lasing spectra obtained at a current injection of 1.2Jth. . Inset: orange lasing spot emitting at 608 nm.

Our team has been much more successful, using a refined QWI process that breaks the record for the tuning of the bandgap in the InGaP/InAlGaP material system. Emission can now span from 640 nm in the red all the way to 565 nm, which is just inside the start of the green spectrum.

At the heart of our process is the PECVD of a dielectric layer. Its thickness is comparable to, or thicker than, the upper-cladding layer of the quantum well. The role of this thick dielectric layer, which is formed from SiO_2, is to induce significant strain within the quantum well region, without damaging contacts or the *p*-cladding. Note that if the dielectric is too thin, the QWI process fails to deliver a significant shift in emission wavelength, while impairing surface morphology and electrical and optical characteristics.

Using a structure with a SiO_2 layer of appropriate thickness, we undertook annealing in a rapid thermal processor that promotes quantum-well intermixing. We used multiple cycles at a relatively low temperature to reduce chances of the point defects diffusing to form cluster defects – these large imperfections are highly undesirable, as they cannot be removed by annealing, and they degrade crystal quality. A lower temperature also helps to reduce redistribution and diffusion of zinc dopants. If this occurred, it could destroy the diode's *p-n* junction.

During our low-temperature annealing process, atoms in the thin InAlGaP quantum barrier and InGaP quantum well interdiffuse, to relax the strain induced by the thick dielectric layer. This creates grown-in strain relaxation and an atomic composition change, which work together to produce a shift in the bandgap.

We have fabricated a range of emitters with our novel QWI technique. This includes simple, broad-area devices with a wavelength as short as 608 nm. They lase at room temperature, produce a total output

power of 46 mW, and break new ground for banishing the colour gap from the long-wavelength side. This success has enabled us to produce the first report of lasing action from a post-growth interdiffused process.

We have also demonstrated the first yellow superluminescence at a wavelength of 583 nm. This device has a total two-facet output of 5 mW, which is the highest optical power ever reported at this wavelength in this material system.

Our results are very encouraging, given that the cladding does not contain a complicated multi-quantum barrier to suppress carrier overflow. If we were to introduce this, it should enable a cut in threshold, plus a hike in output power.

We hope that our successes – demonstrating an orange laser and yellow superluminescent diode – will pave the way to the fabrication of the first yellow semiconductor laser. Uniting this with cousins emitting in the green, red and blue could spawn a new revolution in solid-state lighting. There is the promise of a source that combines incredibly high efficacies with a CRI that is close to 100, and a light-based replacement for WiFi that delivers breath-taking data rates.

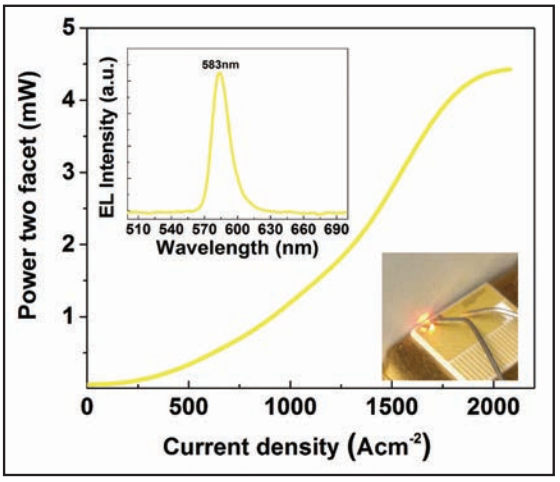


Figure 8: Power-current characteristics as a function of current density from an InGaP/InAlGaP intermixed sample. Inset: amplified spontaneous emission spectra at 583 nm.

Opportunities for green, orange and yellow lasers

COMMERCIALLY available true-green, orange and yellow laser diodes and LEDs would be attractive alternatives to the gas and diode-pumped solid-state lasers that currently serve the spectral range spanning 550 nm to 620 nm. Potential applications include:

Solid state lighting A combination of blue and yellow – or blue, green and red – can produce efficient white light for lighting applications.

Visible light communications and Li-Fi Modulating the light beam from diode lasers, rather than LEDs, has extreme advantages in the field of visible light communication. Current Li-Fi technology uses LED technology, which is compromised by its relatively slow modulation rates. It could be replaced by visible lasers with a GHz modulation bandwidth.

Displays The availability of high efficiency red, green and blue lasers would enable high-definition projectors, HD TV and micro-projector technologies.

Optical communication using plastic fibre Plastic fibre has a peak transmission wavelength at 580 nm, making yellow lasers ideal sources.

Skin care Yellow lasers can treat wrinkles, sun damage, pigmentation and other skin problems, with a dramatic improvement after just a few treatments. Success results from absorption of yellow light by melanin cells under pigmentation.

Retinal diabetes surgery This form of surgery currently uses a DPSS laser emitting at around 577 nm. Working with this wavelength allows the curing of tissues at the back of the eye. This can be accomplished without damaging tissue that the laser beam must pass through.

Flow cytometry This technique in the field of bioscience uses photoluminescence to quickly uncover the flow of species or certain type of cells. Solid-state lasers emitting at 595 nm are used for this application, but they could be replaced by laser diodes formed by quantum-well intermixing that emit at ideal wavelengths.

Horticulture LED and laser lighting can be fined tuned to deliver the optimum spectral output for different phases of the plant growth cycle. This approach could also have nutritional benefits.

Pharmaceutical Industry Lighting based on LEDs, superluminescent diodes and laser diodes could be used in the construction of genetically engineered plants for the production of pharmaceutical products (referred as Pharming). This form of lighting is ideal, because transgenic plants need particular illumination wavelengths at particular phases of their life cycle.

Connecting the photonic integrated circuits community

PIC Magazine

Business-to-business specialist publisher and event organiser Angel Business Communications, publisher of Compound Semiconductor Magazine and organiser of CS International and PIC International conferences has announced the launch of Photonic Integrated Circuits (PIC) Magazine, a new quarterly digital magazine which aims to provide timely, comprehensive coverage of every important sector within the photonic integrated circuits industry.

PIC Magazine will provide comprehensive coverage of all aspects of this industry, and each issue will carry features and research from the full spectrum of the integrated photonics community. So whether you focus on system integration, developing and manufacturing components, financing this sector, or providing the materials and equipment needed to support this industry, PIC Magazine will be your essential magazine.

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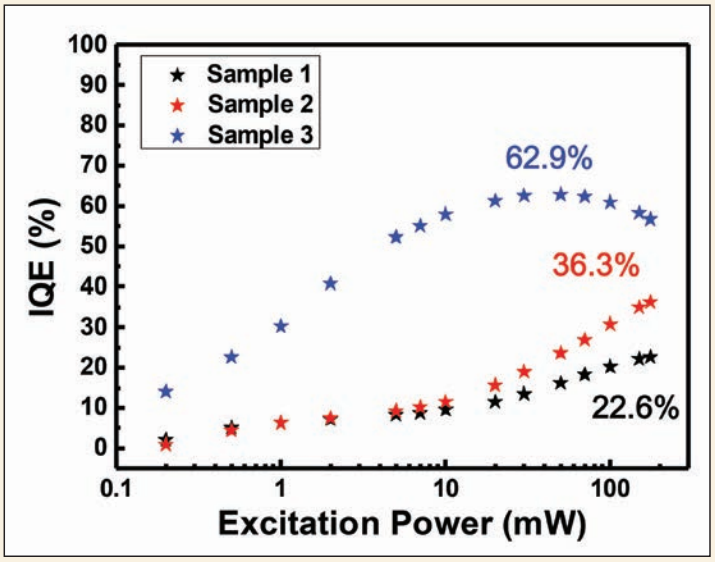
Improving GaN-on-silicon LEDs

Thinning the LED propels internal quantum efficiency beyond 60 percent

A PARTNERSHIP between researchers in Taiwan and China claims to have increased the efficiency of GaN-on-silicon LEDs to a level that is competitive with those grown on patterned sapphire.

The team's work promises to improve the LED by making it less expensive – thanks to the uses of substrates that are larger and cheaper – while not compromising performance.

Corresponding author Tien-Chang Lu from National Chiao Tung University, Taiwan, says that the most important aspect of the work is demonstrating that a high-volume manufacturing process can make devices that can overcome the quantum-confined Stark effect.



The highest IQE is produced by sample 3, which has an *n*-type GaN layer thinned so that it is just 1 μm-thick. Sample 2 has thinning of the *n*-type GaN layer to 3 μm-thick, while sample 1 is the standard LED structure.

This is accomplished by adjusting the strain in the structure. To do this, researchers thin the device with a combination of inductively coupled plasma, reactive-ion etching and chemical-mechanical polishing.

The team highlighted the benefits of thinner devices by growing an LED epistructure on silicon (111), before bonding it to another silicon wafer and then removing the original substrate by wet chemical etching. "The bonding layer also served as a reflector," explained Lu, while the use of a second silicon substrate enabled good thermal management.

Evaluations of internal quantum efficiency were made on the original epilayer structure, and also a pair of devices thinned so that the thicknesses of the *n*-type GaN layers were 3 μm and 1 μm.

Pumping all three samples with 400 nm light at 19K and 300K revealed that the thinning of the structure produced a leap in internal quantum efficiency from 22.6 percent to 62.9 percent.

Lu and co-workers have also recorded the change in photoluminescene spectra with pumping power. Emission from the multi-quantum well shifted from 436 nm to 430 nm, equating to 40 meV, due to a combination of screening of the quantum-confined Stark effect, and the Burnstein-Moss effect.

The latter, an apparent bandgap increase, occurs when more carriers are introduced into the active region, causing more states to be populated and the absorption edge pushed to higher energies.

To distinguish between the influence of the quantum-confined Stark effect and the Burnstein-Moss effect, the team recorded the peak wavelength and the full-width half-maximum of the emission spectra at various pump powers. As the excitation density increased, the full-width at half-maximum initially reduced, due to the quantum-confined Stark effect, before increasing due to the Burnstein-Moss effect.

This observation enabled the researchers to conclude that the quantum-confined Stark effect produced a 9.5 meV shift in emission in the control sample. In structures thinned to produce *n*-type GaN layers 3 μm-thick and 1 μm-thick, shifts were just 5.4 meV and a 2.4 meV shift, respectively.

Lu and co-workers postulated that thinning of the sample decreased the compressive strain in the multi-quantum well, reducing the quantum-confined stark effect and the spectral shift in emission.

To investigate this, the team turned to depth-resolved confocal Raman spectroscopy, comparing the peak from GaN in their samples to that of unstrained GaN. This revealed 0.39 GPa of strain in the control, with thinning reducing this figure very slightly – it was 0.36 GPa in the thinnest sample.

Modelling suggests that the thinning of the sample produced a very modest gain in the overlap integral for electron and hole wavefunctions, increasing from 75 percent for the control to 79 percent for the thinnest sample. To explain why this change is so small, while the gain in internal quantum efficiency is so large, Lu argues: "We believe that the strain has redistributed in the thickness-reducing process, and can enhance the localisation effect and the internal quantum efficiency."

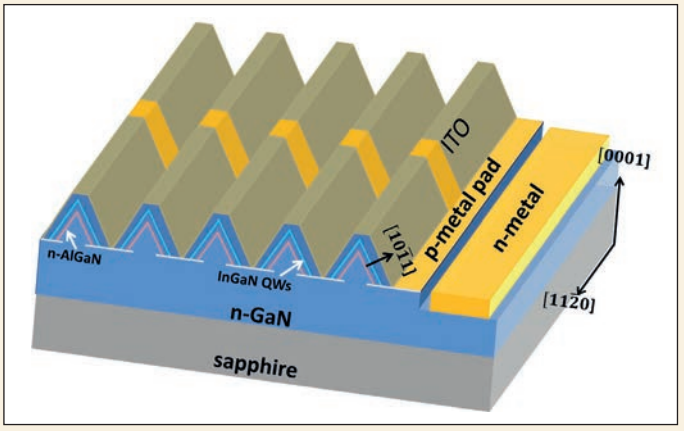
The next goal for the team is to perform spatially resolved mapping on their samples. "[This should] prove that the thinning down of the total device thickness not only suppresses the effect of the quantum-confined Stark effect," says Lu, "but also changes the strain distribution in the multi-quantum well, to enhance the localisation effect and the internal quantum efficiency."

H. Li *et. al*. Appl. Phys. Express **9** 042101 (2016)

Slashing the cost of semi-polar LEDs

Patterning sub-micron stripes on sapphire paves the way to the fabrication of low-cost semi-polar LEDs

A TEAM from the University of New Mexico has developed a process for producing low-cost, semi-polar LEDs. Cost-savings result from the use of a sapphire substrate, rather than very expensive, limited availability semi-polar GaN.



Semi-polar LEDs are formed on sapphire substrates by creating triangular-strip core-shell nanostructures.

The appeal of semi-polar sources is that they have the potential to be incredibly efficient. Impressive figures for the lumens-per-Watt could result from the substantial reduction in the internal electric fields, which pull apart electrons and holes and ultimately impair radiative efficiency.

The researchers from the University of New Mexico are not the first to explore approaches to making semi-polar LEDs on foreign substrates. Popular options are to employ either a bottom-up, catalyst-assisted vapour-liquid-solid growth mode, or a catalyst-free self-assembled approach using an *in-situ* SiN dielectric. However, with these techniques it is difficult to control the size, morphology and placement of the nanowires.

An alternative is selective-area growth. It involves *ex-situ* deposition of a dielectric, which is patterned by lithography. Following this step, etching exposes areas of the underlying GaN template, enabling growth of three-dimensional structures with non-polar or semi-polar facets.

The team from the University of New Mexico is not alone in adopting this particular approach. However, it uses stripes about 600 nm in width, compared with more than a micron by Ferdinand Scholz's group at the University of Ulm.

One of the challenges of growing nanostructures in stripes is spontaneous formation of multiple facets, each with a different surface polarity, indium incorporation and growth rate. The upshot is quantum wells with a non-uniform thickness, indium content and quality.

To address this issue, the University of New Mexico researchers grow ordered arrays of GaN-based stripes with triangular cross sections that consist exclusively of semi-polar {10$\bar{1}$1} planes. However, even by taking this approach, there are persistent non-uniformities in quantum well thickness and indium composition, according to transmission electron microscopy and energy-dispersive X-ray spectroscopy measurements.

Devices were produced by growing a 2 μm-thick film of GaN on *c*-plane sapphire that functioned as the *n*-side of the LED. After depositing a 120 nm-thick film of the dielectric SiN, the researchers patterned the wafer with interferometric lithography, before growing a nanostructure core using a III-V ratio of 2000. This led to exclusive emergence of the semi-polar {10$\bar{1}$1} plane. On this they grew a thin, *n*-type layer of AlGaN. It serves several purposes: it eliminates the reverse leakage currents in the LEDs, acts as a getter for oxygen, and fills defects in the masking pattern.

The LED structures grown on the *n*-type AlGaN consist of an *n*-type GaN layer, an active region with four 3 nm-thick quantum wells, and a magnesium-doped *p*-type GaN layer. Subsequent standard contact photolithography techniques created triangular-nanostructure LEDs, which featured a transparent indium-tin oxide current-spreading layer. Corresponding author Ashwin Rishinaramangalam believes that the fabrication of these triangular LEDs is only slightly more involved than that of conventional GaN-on-sapphire LEDs: "Since [our technology] is based on the already existing *c*-plane GaN technology, it could be beneficial for high-volume manufacturing, if the results obtained could be on a par with today's state-of-the-art LEDs."

The devices produced by the team have a broad emission linewidth. It shifts significantly with increasing current density, which is not typical behaviour for a semi-polar device.

Rishinaramangalam says that at present, the broad emission spectrum is a downside, because he and his co-workers cannot control emission from different sections of the device. However, if they can learn to tailor the spectral profile, this could enable them to make a white LED with a high colour-rendering index.

The team is now starting to investigate the droop of these devices, by measuring their internal quantum efficiency using low-temperature photoluminescence.

"Even if our internal quantum efficiency was very high, there is an injection efficiency issue on these devices, because of the non-uniform *p*-side conduction," says Rishinaramangalam. For that reason, he believes that these devices cannot produce a high external quantum efficiency.

"Further optimisation on device design is necessary to enable uniform current injection," admits Rishinaramangalam.

A. Rishinaramangalam *et. al*. Appl. Phys. Express **9** 032101 (2016)

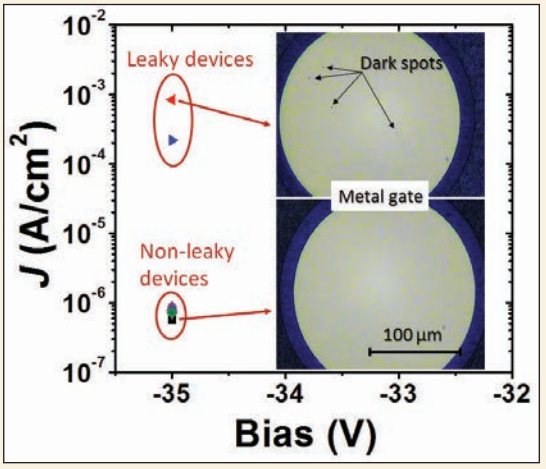
Diode's reverse leakage hits new low

Growth on bulk GaN substrates slashes lateral Schottky barrier leakage current densities

RESEARCHERS from China and Hong Kong claim to have set a new low for the reverse leakage current produced by a lateral Schottky barrier diode.

Biased at -35 V, the team's device produces a reverse leakage current density below 10^{-6} A cm^{-2}, which is more than six times lower than the previous record.

Corresponding author of the work, Xing Lu from Xi'an Jiaotong University in China, believes that the ultra-low leakage of the team's devices highlights the potential of using GaN substrates, rather than those made from SiC, for fabricating "top-quality" AlGaN/GaN heterostructures, such as lateral Schottky barrier diodes and HEMTs.



Bulk GaN leads to ultra-low leakage currents for the majority of the devices. However, for a few devices, leakage is much higher – probably caused by surface defects.

Lateral Schottky barrier diodes are far less common than those with a vertical architecture. But they are superior in several regards, according to Lu. He argues that they are more resilient to surface traps, deliver superior heat dissipation and are easier to package.

What's more, they can produce a high breakdown voltage from a limited chip area; and thanks to a two-dimensional electron gas that combines a high carrier concentration with a high electron mobility, they can deliver fast, low-loss switching.

Another merit of the lateral Schottky barrier diode is that it has a similar heterostructure to the HEMT. This makes it easy to grow, process and integrate with other devices.

Lu and his co-workers are not the first group to produce a lateral Schottky barrier diode on bulk GaN substrates. They are following in the footsteps of a Polish team that includes researchers from Unipress, TopGaN, and GaN substrate maker Ammono.

"In their work, the lateral Schottky barrier diodes on a bulk GaN substrate also exhibited a much lower reverse leakage current than the reference ones on the sapphire substrate," says Lu. "However, the reverse leakage current was as high as 10^{-4} A/cm^2."

In 2012, a team from Pohang University of Science and Technology and Samsung reported a significantly lower leakage current density of 6 x 10^{-6} A cm^{-2} for a lateral Schottky barrier diode grown on sapphire. However, this device suffered from side effects caused by plasma treatment. Weaknesses included a reduction in channel conductivity.

Lu and his colleagues began the fabrication of their devices by loading a Kyma bulk GaN substrate in an Aixtron 2400HT MOCVD reactor and depositing on this foundation a 2 µm-thick layer of undoped GaN, a 1 nm AlN spacer and a 20 nm-thick $Al_{0.3}Ga_{0.7}N$ barrier.

To form the lateral Schottky barrier diode, they realised mesa isolation with a chlorine-based inductively-coupled plasma etch, and formed an ohmic contact by using electron-beam evaporation to deposit a metal stack, which was annealing for 30 seconds under nitrogen gas at 850 °C. The addition of a Schottky metal completed fabrication of the lateral diodes.

To enable the team to benchmark their diodes, they also made devices with the same features on GaN-on-sapphire templates with a 4 µm-thick buffer.

At a -35 V gate bias, the device on the native substrate produced a reverse leakage current density below 10^{-6} A cm^{-2}, which is more than four orders of magnitude higher than that on the GaN-on-sapphire template.

Turning to atomic force microscopy enabled the team to compare the surfaces of their devices.

Those grown on bulk GaN are smooth and feature well-aligned atomic steps, while those grown on the GaN-on-sapphire templates are rougher and impaired by surface pits, which are believed to stem from extended dislocations in the AlGaN barrier.

Although the use of bulk GaN has enabled diodes with ultra-low leakage currents, some of these devices have leakage current densities of 10^{-3} A cm^{-2}. These devices come from areas where dark spots, thought to be associated with surface defects, are observed under the metal gate.

Lu says that the *n*-type substrates that they have used for this work limit the device's breakdown voltage. "We are planning to choose a semi-insulating GaN substrate with better crystalline quality to construct both AlGaN/GaN lateral Schottky barrier diodes and HEMTs in the near future."

The team hopes that this will lead to more record-breaking results. They are also hoping to study the current collapse and device lifetime of these diodes.

X. Lu *et. al*. Appl. Phys. Express **9** 031001 (2016)

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