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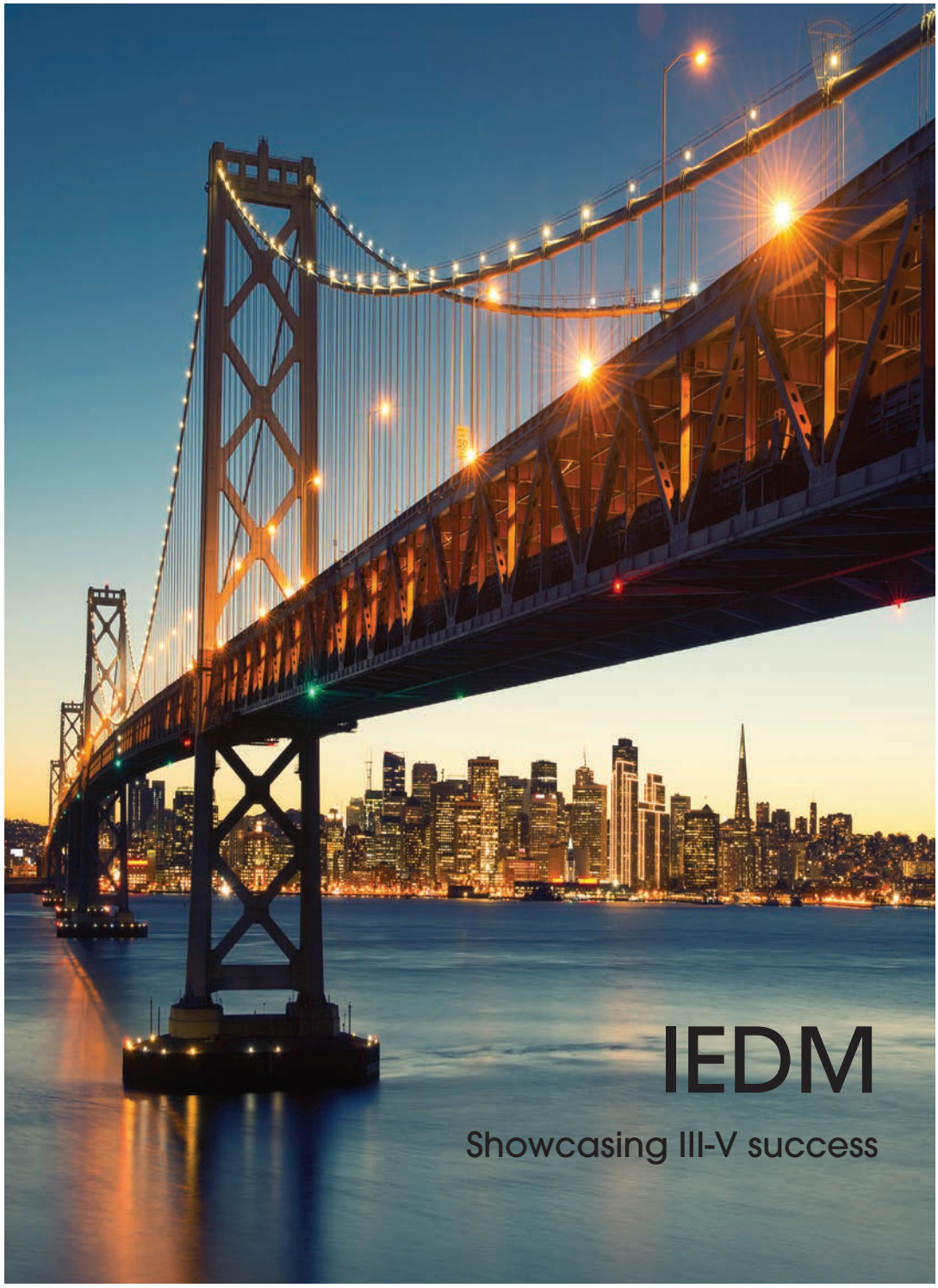

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HVM: High Volume Manufacturing

Viewpoint

By Dr Richard Stevenson, Editor

III-Vs get out and about

THE PHRASE "electron devices" strikes me as a little odd. It seems to speak of a bygone era, when key building blocks for electrical engineers included various forms of vacuum tube. Today, what we tend to talk about is the electronic device, sometimes prefaced with the term solid-state.

Where the phrase "electron devices" does crop up is in the title to the annual IEEE Electron Devices Meeting, often referred to as IEDM. It has been running for well over fifty years.

I have no idea what technologies dominated the proceedings of the early meetings, but in the ten or more years that I've been following the papers given at IEDM silicon has been dominant. However, its stranglehold is weakening, with increasing content of III-V success.

The most recent meeting continued this trend, with reports of advances in GaN and SiC power devices, greater gain in terahertz InP amplifiers and III-V MOSFETs with record on-currents. Details are given in my round-up on p22: *IEDM showcases compound semiconductor successes.*

During the last few years, there have been quite a few papers at IEDM detailing breakthroughs that could lead to improvement in MOSFET technology through the introduction of III-Vs. These higher mobility materials promise to maintain on-currents while reducing the supply voltage – and ultimately the power consumption per transistor. At the most recent meetings, there were a relatively small number of papers on this topic – I'm not quite sure what to make of that – but a group from Lund University claimed a record on-current for any III-V or silicon MOSFET. Their device sports indium-rich nanowires with a beneficial distribution of interface states.

Northrop Grumman are renowned for their pioneering efforts in InP terahertz technology, and at the latest IEDM Bill Deal claimed that the team had produced the first transistor gain at 1 THz or more. They have set the bar high: a gain of 10 dB is produced by their ten-stage amp.

Breakthroughs in GaN power technology included a novel GaN rectifier by MIT that employed field rings to slash leakage currents and boost the blocking voltage; and Panasonic described development of a gate-injected GaN transistor that slashes switching losses, and the introduction of semi-polar gates in vertical structures that increase the capability of high-current, high-voltage switching.

These papers at IEDM highlight the talent of researchers within this community. I look forward to informing you of many more advances in that vein through 2017.

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LED price drop is driving away manufacturers

ALTHOUGH residential and commercial industries are widely adopting energy-efficient LEDs, the drop in LED prices is driving away manufacturers because of decreased profitability, dramatically dislocating and restructuring the solid-state lighting marketplace, says a new US National Academies of Sciences, Engineering, and Medicine report.

Since the last Academies report in 2013 that assessed the state of solid-state lighting, the annual residential installation of LED bulbs has increased six fold between 2012 and 2014, from 13 million to 78 million.

The report *Assessment of Advanced Solid-State Lighting, Phase 2* also cites the emergence of new applications for solid-state lighting that have the potential to create new markets and commercial opportunities for the industry, as well as add value to aspects related to quality of life. For example, product and lighting designers are exploring options that collect and process data from the illuminated environment and offer additional features to consumers.

Developing new products with multiple features that offer functions beyond illumination could promise higher margins for manufacturers, said the committee that conducted the study and wrote the new report. The report warns that the successful proliferation of such applications would not focus on the reduction of energy consumption alone, but the US Department of Energy (DOE) should think of ways to continue to improve their efficiency, given their inevitable growth.

The committee recommended developing strategies for supporting broader research that enables more efficient use of light across all applications, with attention to both the lighting design process and the design of lighting products.

With the possible emergence of new applications for solid state lighting, both consumers and industry need to be more fully educated about the transformative and broader implications of solid state lighting, the report highlights. To achieve this, DOE should partner with industry, states, and utility companies to develop and implement a public outreach program to deploy solid-state lighting.

Toshiba launches second-generation SiC diodes

TOSHIBA has launched a second generation of 650 V SiC schottky barrier diodes (SBDs). Fabricated with the company's second-generation SiC process, they deliver approximately 70 percent better surge forward current than first generation products.

At the same time, they reduce the switching loss index of R_{dsON} Q_C by around 30 percent, making them suitable for use in efficient power factor correction (PFC) schemes.

The new products are available in four current ratings of 4 A, 6 A, 8 A, and 10 A, either in a non-isolated TO-220-2L package or an isolated TO-220F-2L package. These products can contribute to improving the efficiency of power supplies in devices including 4K large screen LCD TVs, projectors and multifunction copiers, and in industrial devices such as telecommunication base stations and PC servers, according to Toshiba.

Aixtron announces new CEO

AIXTRON SE has announced that the current CEO of the company, Martin Goetzeler, is leaving the company at the end of his contract on February 28, 2017.

Former Aixtron Executive Board Member and current Supervisory Board Chairman, Kim Schindelhauer, will take on Goetzeler's duties as CEO and CFO on an interim basis starting March 1, 2017, until a successor is found. The strategy adopted will continue unchanged.

Goetzeler, whose responsibilities included strategy, finances, and also personnel as industrial relations director, is leaving the company for personal reasons and in agreement with the company's Supervisory Board.

"During Mr. Goetzeler's tenure, Aixtron's technology portfolio was diversified considerably and the company oriented its strategy toward the future markets it identified. In addition, both the focus on profitability as well as the awareness of costs were successfully internalised in the company and the financial results steadily improved," explained Supervisory Board chairman Kim Schindelhauer. "

He strengthened the relationships with the Chinese market and consequently initiated the planned China deal." continued Schindelhauer. "He was greatly dedicated to this effort. We thank Mr. Goetzeler for his exemplary service to Aixtron since his appointment in March 2013 and wish him every success in his continued career."

Wolfgang Blättchen, current deputy chairman of the Supervisory Board will take over as chair during Schindelhauer's work as CEO of the company.

Peregrine introduces next-generation UltraCMOS platform

RF SOI (silicon on insulator) company Peregrine Semiconductor has announced the UltraCMOS 12 technology platform. Now in production, this next-generation RF SOI platform is claimed to have the industry's lowest $R_{ON}C_{OFF}$ performance level of 80fs – a 25 percent improvement over the last generation.

To develop the 300 mm UltraCMOS 12 platform, Peregrine collaborated with Globalfoundries, a leading full-service semiconductor foundry.

A key metric for RF switching, $R_{ON}C_{OFF}$ is Peregrine's performance benchmark for each new generation of the UltraCMOS platform. $R_{ON}C_{OFF}$ is a ratio of how much loss occurs when a radio signal goes through a switch in its ON state (RON, or on-resistance) and how much the radio signal leaks through the capacitor in its OFF state (COFF, or off capacitance). With each new UltraCMOS generation, Peregrine targets a 20-percent improvement in $R_{ON}C_{OFF}$. UltraCMOS 12 technology surpasses this target and sets a new industry standard for $R_{ON}C_{OFF}$ performance, according to the company.

"For nearly three decades, Peregrine's UltraCMOS technology platform has been at the forefront of RF SOI performance – especially for RF switching," says Alain Duvallet, vice president of RF process technology at Peregrine Semiconductor. "This legacy continues with today's introduction of the UltraCMOS 12 platform, which boasts the industry's best $R_{ON}C_{OFF}$ performance. And this technology breakthrough is on a 300 mm RF SOI wafer!" UltraCMOS 12 technology, like the two generations prior – UltraCMOS 10 and 11, uses a custom fabrication flow from Globalfoundries. UltraCMOS 11 technology, introduced in July 2015, was the industry's first RF SOI 300 mm platform, and UltraCMOS 10, introduced in October 2013, delivered the industry's best $R_{ON}C_{OFF}$ performance, at the time.

"Our joint development with Peregrine Semiconductor continues to produce remarkable results, and UltraCMOS 12 technology is the latest success story," said Raj Nair, vice president of technology development at Globalfoundries.

"This new RF SOI technology reaffirms our commitment to the RF market and is another example of how Globalfoundries can provide industry-leading levels of performance, reliability and scalability.

Start-up aims to shake up compound semi market

CARBONICS, a venture-backed Los Angeles start-up, has launched its zebra single-walled carbon nanotube (CNT)-on-silicon technology.

Aimed at RF applications, the technology is said to be 30 times more linear than GaAs; 1000 times better in power than GaAs; 100 percent CMOS compatible; and able to cut component cost by 50 percent.

With the launch of its zebra wafers, Carbonics says it wants to give design engineers, foundries, and device manufacturers access to the best and most advanced semiconducting platform for designing next-generation high speed circuits.

"Carbonics intends to shake up the billion-dollar compound semiconductor market with our superior disruptive carbon technology that is fully CMOS compatible and able to perform in the mmWave spectrum – representing perfect timing for the 5G and Internet of Things (IoT) revolution," said Carbonics CEO Kos Galatsis.

"Carbonics has achieved a unique milestone in the evolution of carbon electronics," said Ken Hansen, president and CEO of Semiconductor Research Corporation (SRC). "This is a crucial first step from Carbonics toward high performance, next-generation RF electronics using next-generation nanotechnology for high performance mmWave RF and CMOS compatibility.

It's exciting to see the progress from the fundamental material and device research sponsored by SRC and DARPA develop into the launch of a groundbreaking product technology." The zebra wafer product line includes the zebra bolt with aligned semiconducting CNT on 15 nm SiO_2 for backgated device applications such as sensors and detectors; the zebra dash with aligned semiconducting CNT on 1500 nm for top-gated devices such as memory, switch, logic and RF applications covering L-Band to mmWave and 3G, 4G, 4G, WiFi, 802.11ad and WiGig spectrums; and the zebra sprint with aligned semiconducting CNT on quartz aimed for RF applications up to 100 GHz.

Carbonics also plans to launch its viper product line made up of high performance RF devices and integrated amplifiers in 2017 and its stingray product line of RFICs and MMICs that will include high performance mmWave LNA, PAs, mixers, switches and front-end modules (FEMs) in 2018.

Carbonics was spun-out from UCLA and USC and funded by university-sponsored research from the Centre of Excellence for Green Nanotechnologies at UCLA and King Abdulaziz City for Science and Technology Center (KACST), SRC, DARPA, US Air Force and UCLA's California NanoSystems Institute Technology Incubator.

Growing thicker, more boron-rich BAIN

WITH A COMPARABLE bandgap to aluminium-rich AlGaN, BAIN is a very promising alternative for making deep UV optical devices. One of its great attributes is a smaller lattice constant that can be used to tune the strain and thus enable optical polarization engineering.

The addition of boron also reduces the refractive index, making it possible to fabricate BAIN/AlGaN distributed Bragg reflectors with reflectivity close to unity.

Up until now, utilisation of BAIN has been held back by the low boron content of the wurtzite BAIN and its thickness: boron content has been limited to no more than 10 percent by MOCVD, and thickness has been restricted to 10 nm or less.

According to reports, the root causes for these drawbacks include premature reaction, phase separation, and short diffusion length of boron atoms. The growth efficiency is also compromised as a result the premature reaction.

Recently, however, there has been a breakthrough by a team from Georgia Tech, Arizona State and KAUST, that is led by Xiaohang Li, Fernando Ponce, Russell Dupuis. By optimising growth conditions, in terms of V/III ratio and temperature, and turning to a pulse growth mode, these researchers were able to produce a 100-nm thick single-phase wurtzite BAIN thin films with boron compositions up to 14.4 percent.

Scrutinising the films with transmission electron microscopy confirmed the wurtzite crystal structure. However, determining the material composition for BAIN is not trivial. X-ray diffraction can produce large errors, due to the lack of lattice references of BAIN and existence of strain and defects.

To address this concern, the researchers utilized Rutherford backscattering spectrometry (RBS) which is a reliable and accurate method for the composition of common thin films. However, the RBS signal of boron atoms was weak, due to the small nucleus. Large errors result, so to ensure a reliable figure, composition of aluminium was determined first from the RBS measurement, and that of boron deduced by simple subtraction, since BAIN is ternary.

Another remarkable result of the study is the high boron incorporation efficiency and growth efficiency. In this study, the B/III ratios leading to boron compositions of 11 percent and 14.4 percent were 12 percent and 17 percent. This indicates that the boron atoms in the precursors were incorporated into the thin films as efficiently as the aluminium atoms. The growth efficiency, on the other hand, was determined to be 2,000 μm/mol, implying that 31 percent of the injected group-III precursors formed the thin films. This growth efficiency is similar to the ones of recent reports of efficient AlN growth, showing the suppression of parasitic reactions.

Despite the progress, the team believes that more effort is needed to improve the BAIN material quality. One interesting phenomenon described in previous reports, and observed by the team, is that a decreased growth temperature facilitates the formation of wurtzite BAIN. However, a lower temperature is undesirable for the AlN phase, which is dominant in the BAIN alloys with relative low boron compositions. This is apparently counterintuitive as a shorter covalent bond tends to result in the need for higher growth temperature for the 'conventional' III-nitride binary alloys, including InN, GaN, and AlN.

This collaborative work, which received financial support from the U.S. National Science Foundation, Georgia Research Alliance, and KAUST, is detailed in the paper: 100-nm thick single-phase wurtzite BAIN films with boron contents over 10 percent, from *Physica Status Solidi B*, 1600699 (2017).

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Lumileds claims efficiency record with Luxeon MX multi-die emitter

LUMILEDS has introduced the Luxeon MX, a multi-die emitter that is claimed to deliver industry leading efficiency and flux for outdoor fixtures and high bay lighting applications.

Lighting fixtures benefit from the emitter's 1,200 lumen, 150 lm/W efficacy, at 85°C which enables a system efficiency of 120 lm/W when driven at 700mA. "This is double the flux of comparable emitters in 120 lm/W systems. We've achieved this performance leap by optimising the LED for improved efficiency at higher drive currents up to 1.5 A with the 12 V device," explained Seth Danielson, product manager for the Luxeon MX.

With these developments, Lumileds says it has maximised emitter efficiency

and lifetime. The Luxeon MX makes it possible for luminaire makers to meet the efficiency and quality requirements of the DesignLights Consortium (DLC) Premium V4.1 at 700 mA 85°C.

"By creating products eligible for the DLC Qualified Products List, cities and municipalities can receive rebates on their LED street lighting projects, while also realising the fast return on investment from using the most efficient emitters," said Danielson.

Furthermore, the Luxeon MX uses a new, robust package that increases the projected lumen maintenance compared to the Luxeon M. The Luxeon MX is an instant upgrade to the Luxeon M, featuring identical footprint and optical characteristics.

The Luxeon MX multi-die emitter will be offered in a range of colour temperatures (3000K to 6500K) and CRIs (70, 80 and 90) in convenient 3 V, 6 V and 12 V configurations. Applications include roadway lighting, street lighting, stadium lighting and high bay fixtures.

VisIC raises over $11 million for GaN commercialisation

VisIC TECHNOLOGIES, an Israel-based start-up focused on high voltage GaN power semiconductors, has closed $11.6 million in a Series C financing led by a new investor Birch Investment with participation of existing investors.

The potential of GaN-based electronics for electrical power delivery systems, from consumer power supplies to solar inverters, UPS, power supplies for cloud/datacentres and electric motor drives, has been marketed and anticipated for years, especially for high voltage and high current switching applications.

"We are very excited by the level of support provided by VisIC's new and existing investors, who share our vision for the extraordinary potential of VisIC's GaN based products. It is an important milestone for our company.

Having achieved the best performance metrics for any GaN devices in the market, this new capital infusion positions us to accelerate commercialisation and dominate the market segment," said Tamara Baksht, VisIC Technologies' founder and CEO.

VCSEL market worth $2.4 billion by 2021

ACCORDING to a new report by Zion Research, the global VCSEL market accounted for around $760 million in 2015 and is expected to reach $2.4 billion by 2021, growing at a CAGR of around 21.3 percent between 2016 and 2021.

The VCSEL has gained a reputation as a superior technology for short reach applications such as infrared illumination, fibre channel and intra-systems links, due to the VCSEL's low manufacturing costs and high reliability.

Advancement in automotive electronics, growing numbers of datacentres and increasing demand from gesture recognition and 3D imaging are some of the major driving factors expected to propel the growth of VCSELs, according to the report *VCSEL Market by Application for Data Centers, Consumer Electronics, Automotive, Industrial, Healthcare and Others End Users: Global Industry Perspective, Comprehensive Analysis and Forecast, 2015 – 2021*. Data communication has been the leading application segment with over 57 percent of share in 2015. It is expected to maintain its dominance throughout the forecast period mainly because of the construction of new datacentres. Sensing applications are expected to exhibit high growth in China. Automotive applications are expected to grow at the highest CAGR of 25.11 percent during the forecast period.

North America was the largest market for VCSEL in 2015 and is expected to continue its dominance throughout the forecast period. Europe is expected to show high growth driven by the rising use of VCSEL in consumer electronics. Asia Pacific is considered to be the fastest growing market for VCSEL, due to the surge in datacentres paired with significant growth of the automotive sector in China and India.

Defence and aerospace continue to dominate GaN device market

THE GLOBAL MARKET for GaN semiconductor devices is largely consolidated, with the top four companies commanding a share of over 65 percent of the overall market in 2015, states Transparency Market Research (TMR) in a new report. The dominant company among these four top vendors, Efficient Power Conversion Corporation, accounted for a 19.2 percent share of the global market in the said year. The other three topmost companies of the global market, which collectively enjoyed a considerably large share in the overall global market in the said year, are NXP Semiconductors N.V., GaN Systems, and Cree.

Looking at the on-going research and development activities undertaken in the market, attempts made to eliminate issues related to reliability of GaN semiconductors is expected to be an important area of focus of key vendors in the near future. Transparency Market Research states that the global GaN semiconductor devices market will expand at a high 17.0 percent CAGR over the period between 2016 and 2024. With such exponential growth, the market, which had a valuation of US$870 million in 2015, is projected to rise to US$3,438 million by 2024. Of the key end-use industries utilizing GaN semiconductors, the aerospace and defence sector dominates, accounting for a share of over 42 percent of the global market in 2015. North America and Europe are presently the dominant regional markets for GaN semiconductor devices and are expected to retain dominance over the next few years as well. The rising focus of the Europe Space Agency (ESA) on the increased usage of GaN semiconductors across space projects and the use of GaN-based transistors in the military and defence sectors in North America will help the GaN semiconductor devices market gain traction.

In the past few years, GaN technology has witnessed rapid advancements and vast improvement in the ability of GaN semiconductors to work under operating environments featuring high frequency, power density, and temperature with improved linearity and efficiency. These advancements have boosted the usage of GaN semiconductor devices across an increased set of applications and have played an important role in the market's overall growth lately.

Along with this factor, the increased usage of GaN semiconductor devices in the defense sector has also emerged as a key driver of the global GaN semiconductor devices market. The continuous rise in defense budgets of developing and developed countries as well as the demand for inclusion of the technologically most advanced products in the arsenal of national and international armies will propel the global GaN semiconductor devices market in the near future.

GaN semiconductors are relatively expensive as compared to silicon-based semiconductors owing to the high production costs of gallium nitride as compared to silicon carbide. Further addition in the cost of GaN semiconductors is ensued due to the high cost of fabrication, packaging, and support electronics. Silicon-based semiconductors have witnessed a significant decline in their costs over the past few years, making high cost of GaN semiconductors a foremost challenge that could hinder their large-scale adoption.

The issue can be tackled by producing GaN in bulk. However, there is currently no widespread method that can be used for the purpose owing to the requisition of high operating pressure and temperature and limited scalability of the material.

Veeco sells systems to new Malaysian LED facility

OSRAM OPTO SEMICONDUCTORS GmbH has completed an agreement naming Veeco as the supplier for MOCVD and Precision Surface Processing (PSP) systems needed for its new high-volume LED production facilty in Kulim, Malaysia.
As part of the agreement, Osram Opto Semiconductors has ordered multiple TurboDisc EPIK700 GaN MOCVD, and WaferStorm 3306 PSP Wet Process systems.

Veeco's TurboDisc and Uniform FlowFlange MOCVD technologies have enabled LED manufacturers to achieve an improved cost per wafer savings compared to previous MOCVD systems through enhanced wafer uniformity, reduced operating expenses and increased productivity, according to the company. The WaferStorm PSP Wet Process System is a solvent-based platform that integrates Veeco's proprietary ImmJET technology for improved yield, higher throughput, and lower chemical cost than conventional methods for metal lift-off and other back-end compound semiconductor processes.
"We are pleased that Osram Opto Semiconductors has selected Veeco as a partner in their Diamond initiative, a clear indication that Veeco's LED manufacturing solutions are best-in-class at lowering manufacturing costs and driving high levels of productivity," said William J. Miller, president at Veeco.

"In addition to industry-leading MOCVD equipment, Veeco's WaferStorm platform provides distinct advantages to the back-end wafer cleaning process. As we move forward with this exclusive multi-year partnership, we plan to support Osram's impressive expansion plans with advanced Veeco technology and process expertise."

Philips to sell majority share of Lumileds to US firm

ROYAL PHILIPS has announced that it has signed an agreement to sell an 80.1 percent interest in LED and lighting company Lumileds, to US private equity firm Apollo Global Management. Philips will retain the remaining 19.9 percent interest in Lumileds.

In January 2016, Philips abandoned a deal to sell Lumileds to a consortium of Chinese investors (GO Scale Capital) for $2.8 billion, due to regulatory concerns. Lumileds is the biggest supplier of lamps to the automotive industry, equipping one out of every three cars in the world.

The transaction values Lumileds at an enterprise value of approximately $2 billion, including debt and debt-like items. Philips expects to receive cash proceeds, before tax and transaction-related costs, of approximately $1.5 billion and participating preferred equity.

The transaction is expected to be completed in the first half of 2017, subject to usual closing conditions and regulatory approvals.

"With this transaction, we will be completing an important phase of the transformation of our portfolio and I am satisfied that in the Apollo managed funds we have found the right owner for Lumileds," said Frans van Houten, CEO of Royal Philips.

"In line with our strategic focus on health technology, Lumileds has been operating as a standalone company within Philips since early 2015. With Apollo managed funds acquiring a majority interest in Lumileds and partnering with Philips, Lumileds is now well-positioned for further growth and value creation, building on its robust innovation pipeline, technology leadership and strong customer base."

"We are extremely excited about the opportunity for our managed funds to acquire Lumileds," said Robert Seminara, senior partner at Apollo. "We look forward to partnering with Philips and the outstanding management team and employee base at Lumileds, and bringing in Apollo's resources to support the continued growth and innovation of this industry-leading business."

"I am convinced that together with the Apollo managed funds, Lumileds will sharpen its focus and accelerate innovation in its leading product portfolio of lighting components," said Pierre-Yves Lesaicherre, CEO of Lumileds. "With our strong R&D programs and intellectual property, we are ready to address the current and future needs of our customers. Lumileds will work closely with its industry partners and customers and capture growth opportunities in an exciting industry."

Apollo is an alternative US investment manager with assets under management of approximately $189 billion in private equity, credit and real estate funds, invested across a group of nine industries. Apollo managed funds have a successful track record of acquiring and growing businesses in partnership models of co-ownership with former parent companies, according to Philips.

EPC opens eGaN FET applications centre

EFFICIENT POWER CONVERSION CORPORATION (EPC) has opened an Applications Centre in Blacksburg, Virginia, to increase the reach of EPC to support research and development for the applications of enhancement-mode GaN transistors and ICs.

In addition to traditional FET and IC power conversion applications, GaN technology has enabled emerging applications such as wireless power transfer, LiDAR for autonomous vehicles, and envelope tracking for high bandwidth 4G and 5G communications.

In support of the centre's opening, Suvankar Biswas, has been appointed as senior applications engineer. Biswas' experience includes work involving converter topology for integration of photovoltaic modules, grid-tied inverters, and storage. Additionally, Suvankar has research experience in the integration of harvested power in mobile devices, power delivery architecture in mobile platformlevel systems, and plug-in hybrid vehicles and their connectivity with the Smart Grid. He is an active member of IEEE with numerous peer-reviewed published articles. Biswas obtained his bachelor of electrical engineering degree from the Indian Institute of Technology Kharagpur and his doctorate degree from the University of Minnesota.

"The opening of the Blacksburg Applications Center is an important component of our continuous efforts to focus on customer partnerships when designing eGaN technology-based solutions and demonstrating eGaN transistors' superior performance over MOSFETs and LDMOS. We are very pleased to have Dr. Biswas joining us at this time of widespread, fast growing adoption of GaN-based solutions," said Alex Lidow, CEO and co-founder of EPC.

Continuing its growth, the EPC Blacksburg Applications Centre has several career opportunities that can be found on the EPC website.

NAsP III/V

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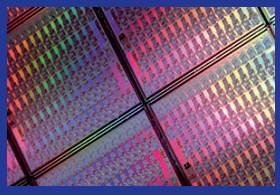

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69 Million automotive LiDAR sensors to ship in 2026

ABI Research forecasts more than 69 million automotive LiDAR (Light Detection and Ranging) sensors will ship in 2026, fuelled by declining hardware costs and the need to equip vehicles with multiple sensors to ensure 360-degree coverage. Autonomous driving functions, including obstacle detection and simultaneous localisation and mapping (SLAM), will drive adoption, says ABI .

LIDAR works on the principle of radar using light from a laser. As safety technologies evolve with regulations and autonomous driving, it is thought that LIDAR, complemented by cameras and radar, could give automakers enough information on the surrounding environment to navigate fully autonomous vehicles.

"Even the most ambitious vendors expect their solutions to begin shipping in high volume models by 2019 at the earliest, which will be too late a time for them to capitalize on the rapid spread active safety technologies that will drive shipments of other sensors, such as radar and camera," says James Hodgson, Industry Analyst at ABI Research.

"The scale and frequency of investments in established LiDAR players and more recent OEM and Tier One startups demonstrates the value that the industry places on LiDAR technology in the development of autonomous vehicles." The recent Consumer Electronics Show (CES) 2017 in Las Vegas saw a number of presentations from LiDAR developers demonstrating low-cost solid state solutions for mainstream deployment, such as Innoviz Technologies and LeddarTech, the latter of which announced a partnership with automotive manufacturer Valeo last year.

Furthermore, current market leader Velodyne received a joint investment from Ford and Baidu totaling $150 million in 2016 and recently announced its intention to develop a sub $50 solid state system for widespread implementation.

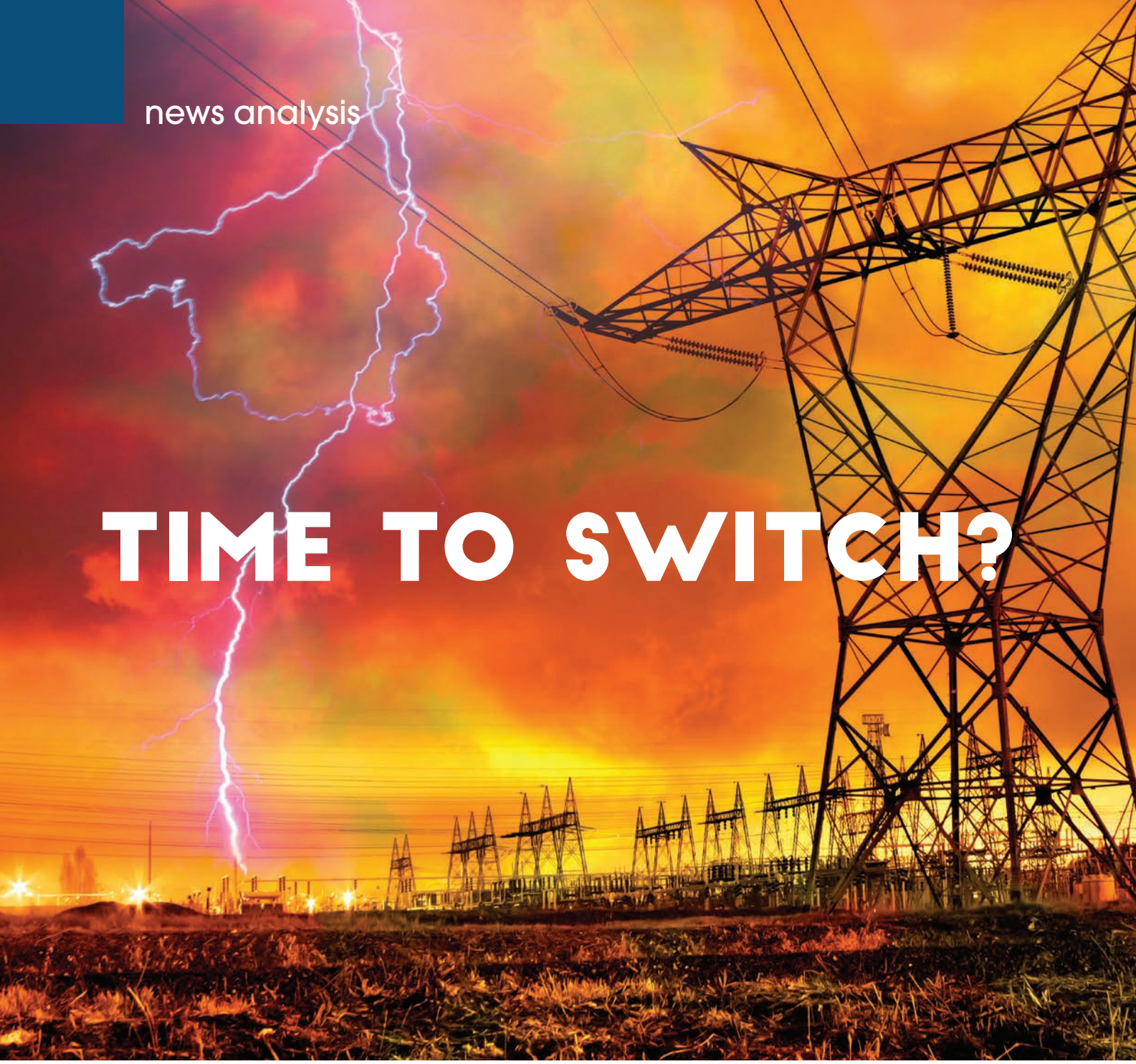
"2016 saw the necessary formation of new investments, startups, and ecosystem partnerships for LiDAR to hit the ground running in the 2019 to 2020 timeframe," concludes Hodgson. "The universal focus on low-cost solutions to enable autonomous functions on high-volume models will accelerate LiDAR shipments throughout the next decade."

Luxeon doubles performance of chip scale UV LED

LUMILEDS has introduced a new Luxeon UV LED, which it says delivers twice the irradiance power of its previous generation product in a miniature 2.2 mm^2 SMD chip scale package.

According to the company, the Luxeon UV U1, the third generation of LEDs for UV curing, counterfeit detection, analytical instrumentation, inspections and other 380-420 nm applications, maintains the same micro package size as Luxeon Z UV, but enables five times greater power density. The new LED is also said to feature a robust design that eliminates materials like silicone over mold, which tends to yellow and crack upon UV exposure, and the elimination of wire bonds that can lead to catastrophic connection failures.

"UV LED customers are reliability driven. They tend to run their equipment 24/7 and demand a proven product that will perform as expected for over 20,000 hours. The Luxeon UV U1 is that reliable product," said Yan Chai, product line director of Lumileds UV LEDs. The UV U1 is nominally tested at 500 mA but can be driven at up to 1 A to achieve higher irradiances. For the application of UV curing at 395 nm, Luxeon UV U1 achieves 700 mW at 500 mA and >1300 mW at 1A under 25°C. The footprint is a drop-in replacement for the Luxeon Z UV.



TIME TO SWITCH?

Can a cheaper SiC switch deliver next-generation power grids, asks Rebecca Pool.

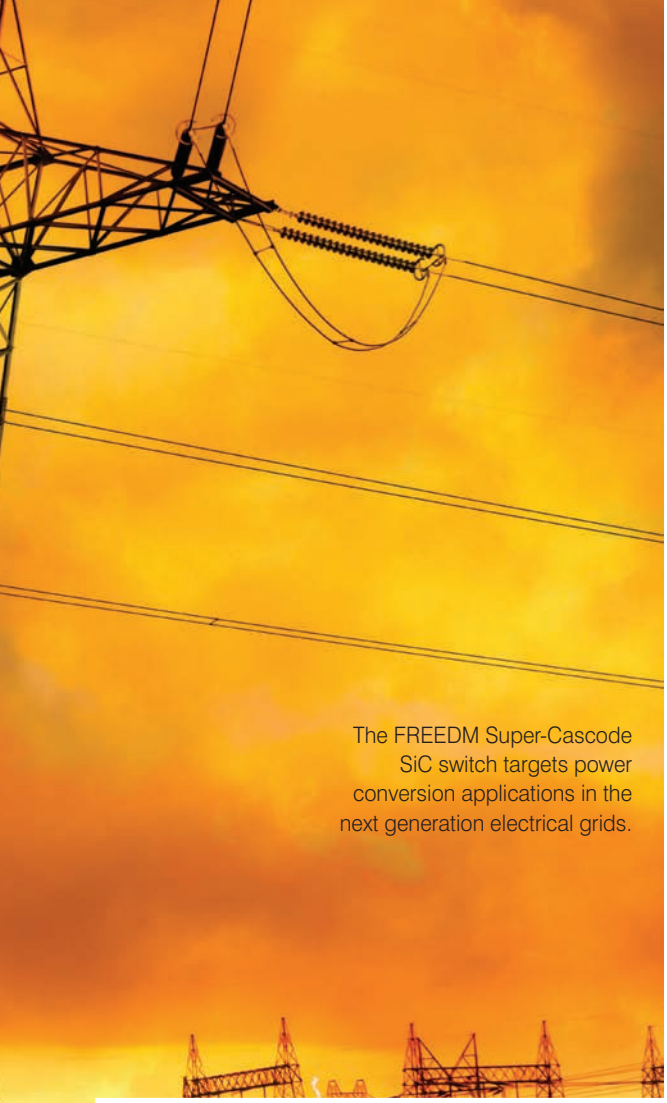
LATE LAST YEAR, researchers at US-based North Carolina State University unveiled a SiC high-voltage and high frequency power switch that they hope will gain commercial acceptance where other SiC devices have not.

The three terminal power device – called the FREEDM Super-Cascode – comprises a 1.2 kV SiC MOSFET and twelve 1.2 kV SiC JFETs, connected in series to give the 15 kV, 40 A switch. Device pioneer and group leader Alex Huang says that the switch provides the high efficiency and high switching speed of an equivalent monolithic 15 kV SiC MOSFET from Wolfspeed. Crucially, Huang also claims his switch is relatively cheap.

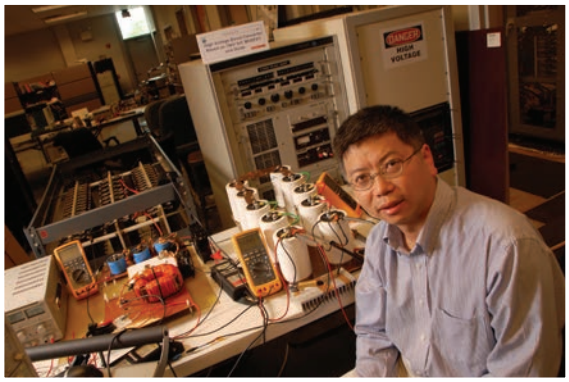
"The FREEDM Super-Cascode costs only one-third of the estimated high-voltage SiC MOSFETs," he says. "The 15 kV SiC MOSFET has attracted a lot of interest because of its potential in high voltage, high frequency power converter applications for the next generation Smart Grid."

"But devices are still under development, and high cost due to expensive materials growth and fabrication could limit future adoption," he adds.

From a system integration viewpoint, Huang also points out how the switch only requires one gate signal to turn it on and off, easing implementation and making it less complicated than more widely established IGBT-series devices. And thanks to a high thermal dissipation capability, the device can operate over a wide range of



The FREEDM Super-Cascode SiC switch targets power conversion applications in the next generation electrical grids.

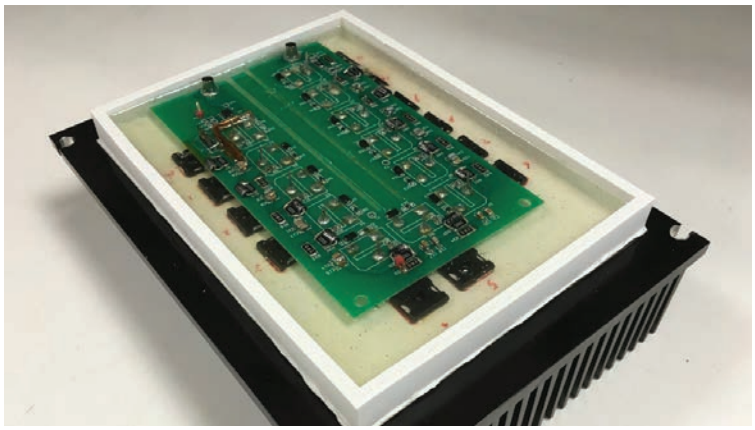


temperatures and frequencies, making it suitable for power conversion in the medium voltage drives, solid state transformers, high voltage transmission and circuit breakers of tomorrow's power grids.

The cheaper alternative

Huang established the FREEDM (Future Renewable Electric Energy Delivery and Management) Systems Center in 2008 following funding from the National Science Foundation and additional industry support to create the energy network of the future. As he puts it: "We're trying to create a new electric grid infrastructure that we call the energy Internet. We're looking at the whole distribution system; that's a huge, very complex engineering system."

Huang is intent on introducing new power semiconductors and advanced power electronics to the future power grid, and has already delivered myriad devices including a 6.5 kV silicon/SiC hybrid 'FREEDM-Pair' switch for high power applications and 6 kV SiC hybrid FREEDM Super-Cascode power switch based on a 1.2 kV SiC MOSFET and four 1.2 kV SiC JFETs.



The high power switch has the potential to work more efficiently and cost less than conventional devices.

The researcher believes such devices are more cost effective than the monolithic SiC device equivalent. As he highlights: "Lower voltage devices, for example, are more mature, in terms of manufacturing, and are already commercially available. These devices are the building blocks of our Super-Cascode devices making a clear path to commercialisation."

"We are also developing [single] high voltage devices in our laboratory, without using many devices in combination," he adds. "But the Super-Cascode design is lower risk and we can scale voltage and current very quickly."

Indeed, Huang's tests on both his latest 15 kV FREEDM Super-Cascode switch and the 15 kV SiC MOSFET from Wolfspeed reveal the former has a faster switching performance. Meanwhile, thermal analyses on each indicate the Super-Cascode device has a higher power dissipation capability than a single monolithic SiC MOSFET.

Left: Professor Alex Huang is developing cost effective SiC switches and more. [Roger Winstead, NC State University]

"We are introducing this Super-Cascode switch as a single-packaged device, but the beautiful thing is how we have made many components work together as one," says Huang. "Synchronisation is key and this is our major innovation."

"We have achieved an extremely fast switching speed with our FREEDM Super-Cascode device, and this paves the way for power switches to be developed in large quantities with breakdown voltages from 2.4 kV to 16 kV," he adds.

Huang now intends to demonstrate his switch in a power electronics operating system, a feat he expects to achieve by Spring this year. "We've demonstrated the technology as a single device but we need system-level verification as well," he says. "With this, we will be discussing the technology with potential licensees and are also looking at university start-up opportunities."

A faster slice

Will novel wafer dicing slice up SiC in time for market growth, asks Rebecca Pool.

READ ANY recent analyst forecast and it's plain to see that SiC power device businesses are poised for growth.

Recent reviews from France-based Yole Développement predict the SiC power market will swell from some $200 million in 2015 to more than $550 million in 2021. And come 2025, IHS, US, reckons these figures will mushroom to $3 billion.

But while this spells good news for device manufacturers, worldwide, a manufacturing bottleneck is already looming in the form of wafer dicing. While today's state-of-the-art mechanical blade dicing tackles silicon and many other substrates with ease, SiC is a different beast.

As Hans-Ulrich Zühlke, market development manager at Germany-based laser micromachining systems manufacturer 3D-Micromac, points out, SiC is almost as hard as the diamond saw blade itself. As a result, mechanical dicing has to take place at low feed rates – from 2 to 10 mm/s – to minimise tool wear, and what's more, your diced chip could still suffer from chipping and have rough side-walls.

"With mechanical dicing we see chips with defects, chipping at the upper edge of the die, and delamination at the lower die edge," highlights Zühlke. "Also, the entire process is very slow, making it very expensive."

And as the SiC wafer market transitions from 4-inch to 6-inch wafers, problems are set to get worse. "With six inch wafers, there is a significant risk of blade damage and you will probably need a new saw blade for each wafer, making the entire process even slower," says Zühlke.

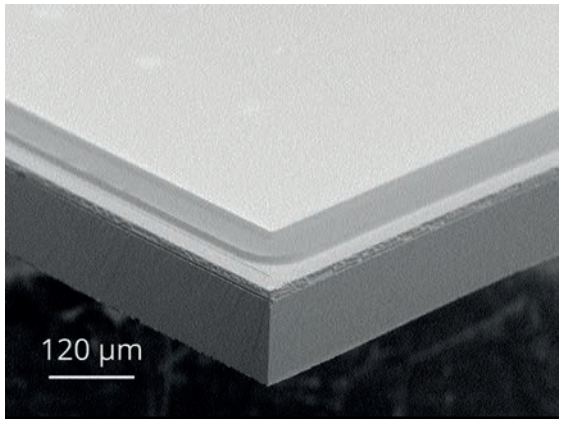
Laser ablation promises to offer light relief to SiC dicing, but Zühlke believes this alternative is also riddled with issues.

"During ablation you melt and vapourise the material, you have a significant heat-affected zone and we see so many microcracks and other defects," he says. "There are also problems with backside metallisation, so for these and other reasons, SiC needs a new dicing technology."

For Zühlke, the clear answer is thermal laser separation (TLS), which uses thermally induced mechanical forces to cleave hard, brittle semiconductor materials. Laser-based heating and subsequent water spray cooling induce a mechanical stress field within the wafer, cleaving the wafer without melting or removing material.

The process was first conceived around a decade ago by Zühlke, then at Germany-based photonics business, Jenoptik, and colleagues from the Fraunhofer Institute for Integrated Systems and Device Technology, Germany.

Development continued apace with the partners soon developing and patenting so-called TLS-Dicing. The process was designed to cleave a range of materials



TLS-Dicing on a SiC wafer promises chip-free die separation.

including SiC as well as silicon, germanium and GaAs.

Then, in early 2014, Jenoptik's Lasers and Material Processing division sold its TLS-Dicing intellectual property to laser micromachining business, 3D-Micromac. Within months, 3D-Micromac had launched its microDICE laser dicing system, based on TLS-Dicing, designed for myriad brittle materials, but targetting SiC wafers for power device and LED applications.

According to Zühlke, the latest system includes an array of software updates to enhance reproducibility, but fundamentally, it's based on the TLS two-step process.

Firstly, a short pulse ablation laser scribes a 10 μm-wide, 15 μm-deep line – dubbed the dicing street – to initiate a crack. Then, in the second step, a continuous-wave laser is passed along this line to heat up the material locally to some 100°C; which is then rapidly cooled by spraying with distilled water, cleaving the wafer.

Crucially, as Zühlke points out, the entire process takes place in a single pass. "This is very fast and entire wafer pieces are separated," he says. "Many other laser processes require many passes which reduces the throughput."

Indeed, trials reveal that fully processed 4H-SiC wafers, including the process control monitor (PCM) structures, backside metal layer stacks and the polyamide coating near to the dicing street, can be diced with feed rates as high as 200 mm/s. The temperature-sensitive polyamide coating is not affected, and as Zühlke highlights, the resulting die is chip-free with smooth side-walls.

"Our industry partners tell me that for dicing SiC, standard mechanical sawing takes place at 4 mm a second; any faster and the material gets too hot," he says. "But we run to 200 mm a second, and this is the same for four and six inch wafers."

But what about cost? 3D-Micromac's thermal laser separation tool is around three times more expensive than a mechanical sawing system. But given the tool's faster throughput, as well as reduced consumables, namely saw blades, Zühlke reckons investment will break even within a few months.

"If you are dicing more than 150 wafers a month, our system will be less expensive than mechanical dicing, and that's including investment," he says.

Laser micromachining from 3D-Micromac: ready for action?

So given the cost and throughput-benefits of thermal laser separation, Zühlke is confident that the SiC market is ready for the technology. "Nearly all customers are using mechanical sawing at the moment and this is fine if you only have a small number of wafers," he says. "But given the volume increases predicted for SiC, we know customers are now looking for new dicing technologies."

Indeed, 3D-Micromac claims its dicing system is already being used by major industrial manufacturers for volume production for power devices.

"You can use [microDICE] on other material including silicon and sapphire but we will focus on SiC right now as the difference in cost of ownership is the most distinct," concludes Zühlke.

"Our industry partners tell me that for dicing SiC, standard mechanical sawing takes place at 4 mm a second; any faster and the material gets too hot. But we run to 200 mm a second, and this is the same for four and six inch wafers."

BEYOND THE HORIZON

As GaN storms radar applications, Qorvo is taking the semiconductor to ever-higher frequencies, reports Rebecca Pool.

AS THE MILITARY'S thirst for GaN semiconductors endures, defence manufacturers are making the most of the industry-wide migration from the incumbent vacuum electronic device to the mighty III-V transistor.

In late summer 2016, Northrop Grumann signed a deal to sell GaN radar to the US Marine Corps. And only weeks later, Raytheon revealed a contract with the Missile Defense Agency to retool its long-range radar line to support GaN semiconductors.

Clearly, the steady spate of military contracts is good news for III-V device providers, with Wolfspeed, Qualcomm, MACOM and more, delivering transistor after transistor for high power radar. Case in point is Qorvo, having released two new GaN-on-SiC power amplifiers for advanced defence and civilian radar systems.

A 500 W L-band device operates in the 1.2 to 1.4 GHz range and targets high-power phased array radar, including Active Electronic Scanned Array (AESA) systems. Meanwhile a 450 W power amplifier targets 3.1 to 3.5 GHz, S-Band radar systems.

As Dean White, Market Strategy Director at Qorvo, highlights: "What is key here is that we have a GaN process that has high gain and high efficiency." "[It enables] lower power consumption and allows a large phased radar array to be air-cooled and not liquid-cooled," he adds. "The weight associated with

air-cooling can be half that of liquid-cooling, and this means a lot to the customer."

Targeting radar

Traditionally, TWTs have been the technology of choice across a broad range of radar frequencies, spanning from the L-band at 1 to 2 GHz to the X-band that covers 8 to 12 GHz. But thanks to its high voltage, high power, high frequency performance, and dogged military development, the GaN transistor is the leading light in electronic-warfare applications.

"I know it sounds crazy as the traditional travelling-wave tube has always been touted as being very broadband, but we can take GaN and design very broadband power amplifiers now," points out White.

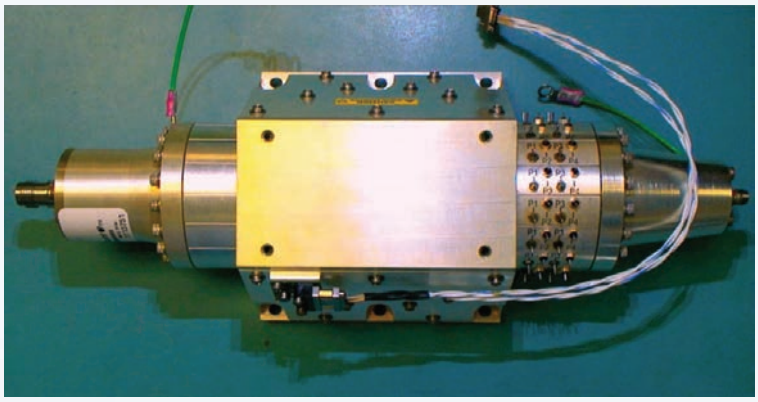
Prior to the merger of RFMD and TriQuint, the latter once delivered record-setting power density levels with its GaAs devices, but for Qorvo, GaN is now king. "We reached 1 W per mm with GaAs but with GaN we get greater than 5 W per mm," says White.

As the Director highlights, the smaller chip that ensues allows AESA radar systems to be taken to higher and higher frequencies. "With the smaller chip-size we can make smaller, lightweight arrays for fighter aircraft and unmanned aerial vehicles," he says. "And beyond the device-level we can also design MMICs with even higher efficiencies as GaN offers power and efficiency in a small space."

Importantly, the impressive power density twinned with a SiC substrate allows Qorvo to package devices in relatively small housing while dissipating heat effectively. "We can really pull the heat out [of these packages] to keep the devices cooler, and the cooler the device the better it performs," says White.

With legacy systems in mind, Qorvo can also integrate its GaN-on-SiC PAs into its so-called Spatium RF power modules, offering a straightforward replacement for TWTs in myriad military systems. These high efficiency power amplifier modules are said to deliver longer service lifetimes as well as size and weight savings.

"This tube replacement looks like a tube but operates at a much lower voltage, so you don't have the power supply reliability issues you have with tubes," says White. "You can take the [package] and fit it into the same spot as your TWT."



Thanks to its high power, high frequency performance, the GaN transistor is the leading light in electronic warfare.

And Qorvo is still seeing steady demand for its GaN-on-SiC devices in legacy and new defence programmes. "We still sell a lot of GaAs PAs but this is generally for legacy programmes," he highlights. "I would say around 90 percent of the time whenever a retrofit or new platform is built, the technology of choice for the power amplifier will be GaN, as opposed to GaAs or even LDMOS."

Beyond legacy devices, up and coming radar markets are offering more opportunities for GaN devices. US-based analyst, Markets and Markets, recently forecast the global X-band radar market to swell from today's $4.58 billion to $5.61 billion come 2021, following government investment in higher frequency radar and demand from land and naval security sectors.

White concurs, highlighting how Qorvo is now seeing demand for GaN in X-band airborne systems as well as X-band commercial radar. "As you go to these higher frequencies, the difference between GaN and GaAs becomes greater," he says. "But we are one of the few companies in the world that has production-ready GaN processes that operate up to 60 GHz."

Given these X-band radar market developments, the company recently delivered GaN-on-SiC discrete FETs that can be used for power amplifiers, low-noise amplifiers (LNAs) and drivers for RF applications at these frequencies and higher. "Everybody thinks of GaN as being high power and asks why would I use that as a low noise amplifier?" says White.

"But this high density transistor also has a very good noise figure – on par with a pHEMT device; so this is a new market and customers are getting used to this."

With legacy systems in mind, Qorvo can also integrate its GaN-on-SiC PAs into its so-called Spatium RF power modules, offering a straightforward replacement for TWTs in myriad military systems

IEDM showcases compound semiconductor successes

III-V devices deliver record on-currents, unprecedented gain at terahertz frequencies and far lower power-switching losses

BY RICHARD STEVENSON

FOR MORE THAN 50 years, the International Electron Devices Meeting (IEDM) has been highlighting advances in silicon technologies. More recently, however, this conference has also been showcasing important breakthroughs in compound semiconductor technologies. And at the most recent meeting – held in San Francisco from 3-7 December, 2016 – the coverage of innovations in III-Vs reached an all time high, with reports of success including: record-breaking currents in III-V MOSFETs; a new benchmarks for gain in InP HEMT ICs at 1 THz; unprecedented breakdown voltages and reverse leakage currents in a GaN rectifier; and the development of a novel, normally-off vertical GaN transistor and a current-collapse-free GaN gate injection transistor.

Advances in the performance of III-V MOSFETs, which promise to maintain the march of Moore's law, have been a common theme at IEDM gatherings during the last decade. And the last meeting continued this trend, with a presentation from Cezar Zota and co-workers from Lund University, Sweden detailing the breaking of the record for the on-current in any III-V or silicon MOSFET (see Figure 1). The team's InGaAs tri-gate MOSFET produces 650 mA/mm at a supply voltage of just 0.5 V.

Increasing the on-current is a significant achievement. "If it is higher than the levels required for circuit operation, then the supply voltage can be reduced so that the on-current is reduced to just the required level," explains Zota. As overall power consumption is proportional to the square of the supply voltage, the power required to operate the circuit falls dramatically – and if the circuit is used in a mobile device, this leads to a longer battery life. Another benefit of trimming the supply voltage with node size is that it can prevent an escalation of the chip power density.

The team from Lund University fabricate their devices by depositing an $In_{0.85}Ga_{0.15}As$ film on an InP substrate by MOCVD, and then defining the nanowires with a hydrogen silsesquioxane growth mask and a digital etch. Evaporation and lift-off create source and drain contacts, and the gate is formed by adding Al_2O_3 and HfO_2 and a Ni/Pd/Au gate metal.

Transistors are produced with a variety of sizes, because this can determine the limit of the material quality of InGaAs with reduced nanowire dimensions. The smallest devices are 25 nm wide, and have an 8 nm height. "Since scattering is dominated by the 8 nanometre dimension, this would correspond to the 10 nanometre node," says Zota. "However, the overall

dimensions in our nanowires are not the same as for the fins in the 10 nanometre node – therefore, the comparison must be made carefully."

If these devices are to be introduced in next-generation ICs, their substrate must switch from InP to silicon. There are plenty of options for moving to this foundation, argues Zota, pointing out that this could be accomplished by: wafer bonding techniques; selective growth, such as the template-assisted growth scheme pioneered by IBM; and the use of buffer layers, which are now capable of combining thicknesses below 100 nm with low defect densities.

As the width of the devices is scaled down from a planar architecture to 25 nm, the transconductance maximum increases to 3.3 mS/μm. This is attributed to an increase in indium richness in the nanowire and a beneficial change in the distribution of interface states.

Another advantage that stems from scaling is a reduction in sub-threshold swing: when the nanowire width shrinks from 1 μm to 25 nm, this falls from 100 mV/dec to 66 mV/dec. Short-channel effects are also addressed, and can be further reduced by introducing either a wider bandgap substrate, or a III-V-on-insulator structure.

Meanwhile, experiments with oxide scaling shows that a reduction in the equivalent oxide thickness (EOT) from 1.4 nm to 1 nm can reduce the sub-threshold swing from 81 mV/dec to 75 mV/dec. And additional improvement is possible, says Zota, arguing that other groups have realised an EOT of 0.7 nm – and he and his co-workers should be able to reproduce this. Further gains could be made by replacing the

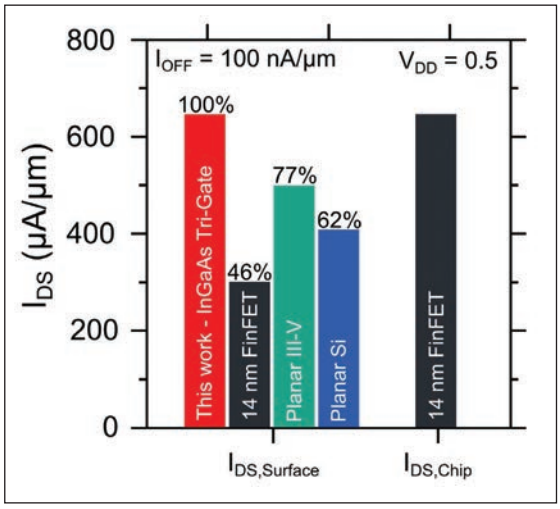


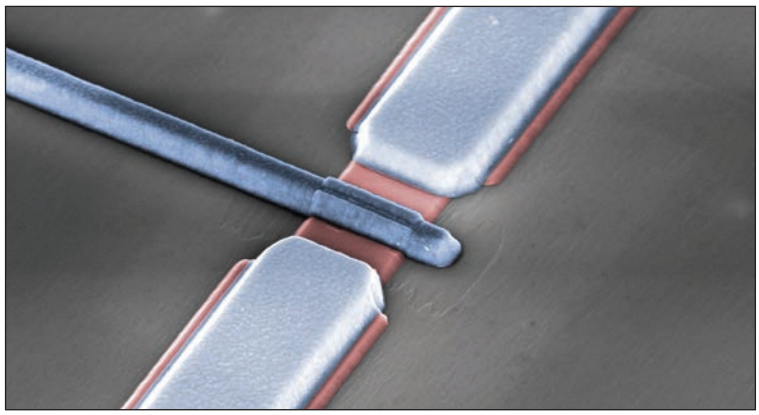
Figure 1. The InGaAs tri-gate MOSFET produced by researchers at Lund University is claimed to deliver a record on-current for any silicon and III-V MOSFET.

"sub-optimal" bilayer Al_2O_3/HfO_2 stack, which has a low κ-value for the Al_2O_3, with a single layer of HfO_2 or ZrO_2.

The team is currently developing an MOCVD selective-growth technique for realising high-aspect-ratio nanowires. Higher current-densities per chip-area could result from this approach, which involves optimisation of growth conditions and the substrate surface orientation to promote the growth of vertical side walls. "This could allow us to obtain industry-relevant fin dimensions, while maintaining our etch-free fin formation scheme and high electron mobility," argues Zota.

Terahertz gain

At Northrop Grumman researchers are developing high-frequency InP transistors for terahertz applications, and at IEDM Bill Deal revealed that they had just hit another milestone: the first demonstration of transistor amplifier gain at or above 1.0 THz. The team's ten-stage amplifier, made from 8 μm transistors, produces a gain of 10 dB at 1.0 THz.



Strength of the InGaAs tri-gate MOSFET produced by researchers at Lund University include a sub-threshold swing that can be as low as 66 mV/decade and a transconductance of 3 mS/μm.

Deal told *Compound Semiconductor* that the transistor technology is already being used for several NASA technology projects, and is expected to be commercialized in the next three-to-five years.

Radio astronomy, atmospheric sensing, and the study of material properties could all benefit from the efforts at Northrop Grumman, because all these applications involve measuring the absorption of radiation at terahertz frequencies. "Having amplifiers at these frequencies may enable new types of radiometric measurements and further our understanding of the physical world," argues Deal.

The team's InP transistor amplifiers also promise to slash the size, weight and power consumption of terahertz receivers. Today, these receivers employ diode-based technologies, and operate at low DC efficiencies. Deal claims that the direct power amplification provided by InP transistors can improve radiometric receiver DC efficiency by more than ten times, and ultimately enable new types of science missions.

A key technology in the InP transistors is a 25 nm, T-shaped gate that is defined by 100 kV, electron-beam lithography. After forming the gate, etching creates a gate recess, with the metal-semiconductor interface located less than 2 nm above the silicon doping plane. Following the gate recess process, a Ti/Pt/Au-based gate metal is evaporated by electron-beam evaporation. To improve reliability and robustness, a SiN film is added to passivate the devices.

Recently, the team at Northrop Grumman have been working on packaging their devices. This is challenging, because at terahertz frequencies it is not easy to couple the radiation between the waveguide and IC. To address this issue, the device is engineered so that an electromagnetic transition occurs on the IC. Dipole antennae are placed on the left and right side of the chip, which has had material removed from its corners.

The team's terahertz transistor is currently being investigated for its suitability for atmospheric science. This is taking place through a variety of NASA-funded research projects, which include the development of an instrument that could be mounted on a satellite to measure tropospheric water and cloud ice.

Fantastic field rings

To improve the performance of vertical GaN diodes for power applications, a partnership between MIT and the Singapore-MIT Alliance for Research and Technology has been developing a novel device with implanted field rings (see Figure 2). Detailing their

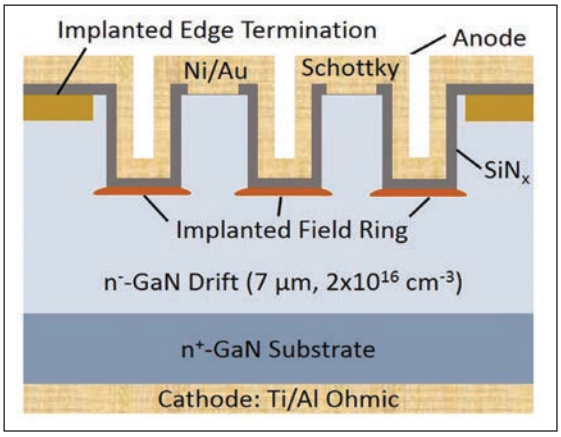


Figure 2. Trenches and field rings enable the rectifier produced by MIT and the Singapore-MIT Alliance for Research and Technology to combine a high breakdown voltage with a very low reverse leakage current.

GaN vertical Schottky rectifier at IEDM, Yuhao Zhang from MIT explained that their modifications to the device slashed the leakage current by a factor of more than 10^4 and increased the blocking voltage from 400 V to 700 V. The turn-on voltage is retained at 0.8 V – in comparison, it is typically more than 3 V for lateral *p-n* GaN diodes, which are renowned for their high blocking voltages and low leakage currents.

According to Zhang, the key to combining Schottky-like forward characteristics, such as the low turn-on voltage, with the high blocking voltages and low off-state currents that are associated with devices that feature a *p-n* junction, is to move the peak electric field away from the Schottky contact. "As *p*-type ion implantation, or selective epitaxial growth, is still very challenging for GaN devices, we designed this trench-based MIS structure with field rings, to move the high electric field without the need for *p*-GaN."

The device that results could provide high-frequency power-switching at 600 V, making it a promising candidate for deployment in electric vehicles, data centres and various power systems.

Fabrication of the device began by growing, by MOCVD, a 7 µm-thick layer of *n*-type GaN on a free-standing substrate. Multiple trenches with a depth of 2 µm were formed, before adding a metal-insulator-semiconductor (MIS) film stack to the trench bottoms and sidewalls. Inserting implanted field rings below the trench bottom followed, along with the addition of a Schottky contact on the top GaN surface.

Simulations with the commercial software Silvaco Atlas provided a great insight into the benefits of the novel architecture. With this particular design, the electric field at the Schottky interface is greatly reduced, leading to an exponential decrease in the leakage current from the Schottky contact; the peak of the electric field is shifted from the upper surface into the bulk GaN; the field rings smooth the electric field stress in the dielectrics near the trench corners of this device; and adjustments to the mesa width alter the level of electric-field shielding of the Schottky junction, and lower the electric field near the field rings (see Figure 3).

To verify these benefits, Zhang and co-workers fabricated three different structures: a Schottky barrier diode, a trench MIS barrier Schottky rectifier, and a trench MIS barrier Schottky rectifier with implanted field rings. The benefits of the trench MIS barrier Schottky rectifier over the Schottky barrier diode are an increase in blocking voltage from 410 V to 510 V and a fall in leakage current by two orders of magnitude. The introduction of field rings delivers a further hike in blocking voltage to 700 V and an additional reduction in the leakage current by two orders of magnitude. The only downsides of the field rings are a slight reduction in turn-on speed and an increase in turn-on voltage from 0.7 V to 0.8 V.

The field-ring, trench MIS barrier Schottky rectifier is also claimed to be the first high-voltage GaN vertical Schottky barrier diode capable of operating above

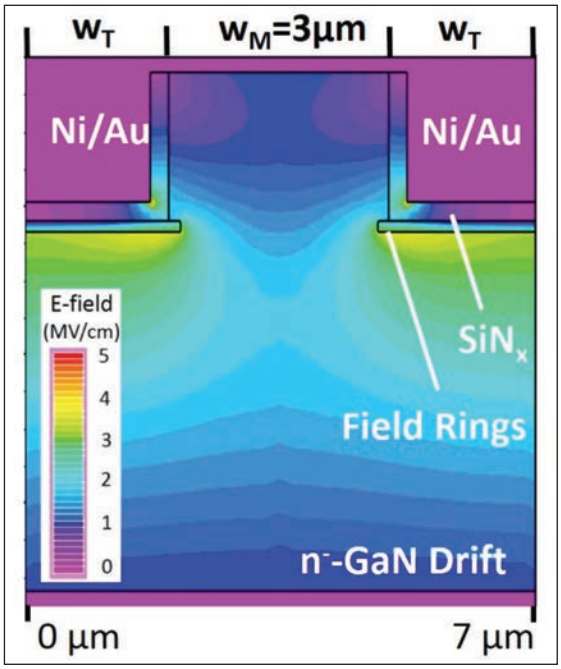


Figure 3. Improvements in the performance of a trench MIS barrier Schottky rectifier with implanted field rings stem from modifications to the electric field profile. These changes can be assessed with the commercial software Silvaco Atlas.

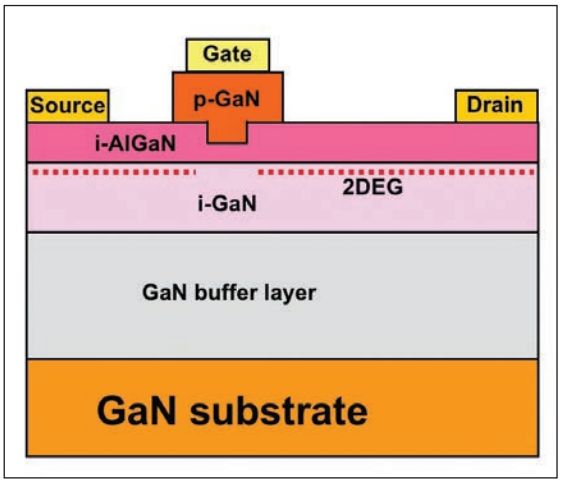


Figure 4. The GaN gate injection transistor developed by Panasonic features a recessed gate structure that reduces the series resistance.

200 °C, making it suitable for operation in some extreme environments. "The capability of operation at higher temperatures would typically enable a higher power output," says Zhang.

One of the next goals for the team is to improve the performance of the rectifier so that its breakdown voltage increases to more than 1200 V. "At the same time, we will utilise this technique to make normally off GaN vertical transistors."

Superior switching

A device that already delivers normally off operation is the GaN gate injected transistor (GIT), and at IEDM Hiroyuki Handa from Panasonic revealed how to slash its switching losses. This device, which is a promising candidate for deployment in compact inverters and converters in consumer products, is usually grown on silicon substrates. However, turning to GaN delivers a three-fold improvement in a key figure of merit for switching efficiency.

The GIT, which operates by injecting holes from the *p*-type gate over an AlGaN/GaN heterojunction to increase the drain current and maintain normally off

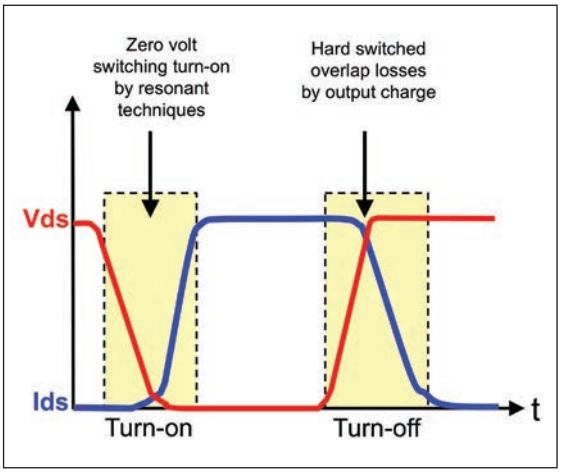


Figure 5. With a typical zero volt switching approach, only turn-off switching causes a switching loss.

operation (see Figure 4), is already being sampled in its GaN-on-silicon form.

Recently, advances in switching technology have led to the introduction of so-called soft switching, which eliminates turn-on switching loss by eliminating overlap between the current and voltage at turn-on (see Figure 5). There is still a loss – but it occurs at turn-off, due to an overlap of current and voltage. Consequently, the key criteria for the GIT is how fast it can be turned off, as this minimises switching loss and allows the use of higher frequencies – and ultimately opens the door to trimming the size, cost and weight of other components in the circuits.

Growing the GIT on a GaN substrate with a thick buffer layer increases its switching capability by cutting the output charge, reducing the on-resistance, and enabling current-collapse-free operation up to 1 kV.

To determine the level of improvement wrought with a thick buffer on a native substrate, Handa and co-workers produced a pair of devices: a GIT with a 5 μm GaN buffer, grown on a silicon substrate (this is the maximum possible thickness, due to thermal and lattice mismatch); and a variant that is identical, except for a 16 μm GaN buffer and a GaN substrate. Note that simulations suggest that the output charge reduces with increasing buffer thickness, but saturates at a thickness of 15 μm.

Measurements on both types of device reveal that using a thicker buffer, and switching from a silicon substrate to GaN, drives down a key figure of merit – the product of on-resistance and output charge – from 2745 mΩ nC to 940 mΩ" nC. Additional improvements include a reduction in the switching rate from 140 V/ns to 285 V/ns, a 60 percent increase in the drain current and a hike in the breakdown voltage from 1050 V to 2800 V.

Handa admits that one of the downsides of the superior device is a production cost that is "currently very high", due to the use of native GaN substrates and thick buffer layers. But it could come down by increasing the wafer diameter and the growth rates.

"The next plans are reliability tests, to compare with GaN-on-silicon GITs," says Handa.

Semi-polar gates in GaN

One of Handa's colleagues at Panasonic, Daisuke Shibata, also presented pioneering work at IEDM – in this case, the development of a 1.7 kV, normally off, vertical GaN transistor that is grown on a native substrate and features a semi-polar gate structure (see Figure 6). This device is claimed to be the first vertical GaN transistor to offer stable gate performance.

"Our re-grown *p*-Gan/AlGaN/GaN semi-polar gate can

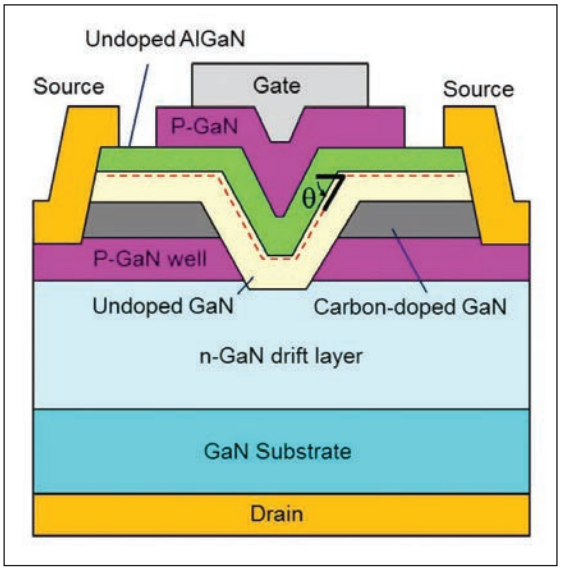


Figure 6. The threshold voltage of the vertical GaN transistor produced by Panasonic increases with the tilt angle, q.

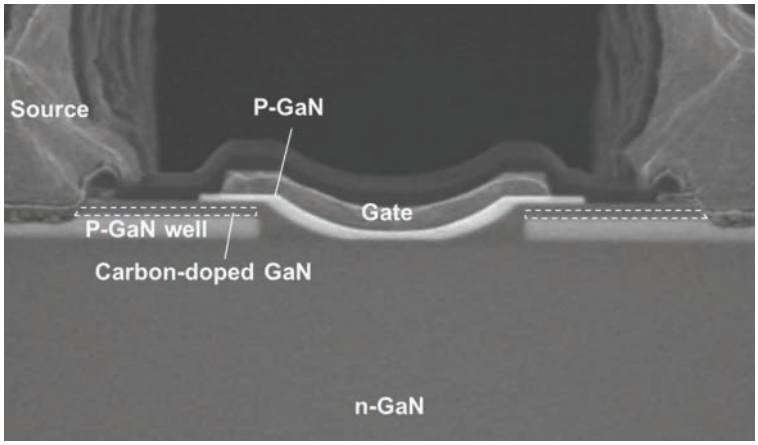


Figure 7. A cross-sectional scanning electron microscopy image of Panasonic's vertical GaN transistor, which is claimed to feature the first stable gate for this class of device.

be applied to other vertical devices," says Shibata, explaining that it could not only equip them with a more stable gate, but also a higher threshold voltage – it is 2.5 V in their device. "A higher threshold voltage is strongly desired to prevent false operation caused by circuit noise."

The 1.7 kV transistor will target power switching systems. Engineers of these systems are currently evaluating lateral AlGaN/GaN transistors that are formed on silicon substrates and have blocking voltages of up to 600 V. Shibata says that the performance of these devices, including their reliability, is good enough for practical use. However, they are held back by a limit to the total output power of several kW. The lateral geometry hampers increases to the current and the voltage, which is limited to 1 kV, due to restraints on the thickness of GaN layers grown on silicon.

Shibata and co-workers are by no means the first to turn to vertical transistors to overcome the limitations of the lateral device. But in general, efforts have been hampered by low threshold voltages, and low stability of the gate, due to instability between an oxide and GaN. With the team from Panasonic, both of these issues have been addressed.

Success results from the design of the device, which features the growth of three layers - a *p*-GaN gate, AlGaN and GaN – on a V-grooved surface that is formed in *p*-GaN well and *n*-GaN drift layers (see Figure 7).

Tilting the layers delivers a hike in threshold voltage. As the angle of the tilt compared with the plane of the wafer (shown as θ in Figure 6) increases from 0° to 90°, calculations suggest an increase in threshold voltage from just over 1 V to almost 4 V. Experiments confirm the extent of the benefit, with a threshold voltage on the *c*-plane surface of just 1 V, which is 1.5 V less than the device incorporating a semi-polar gate.

Another feature of the transistor of Shibata and co-workers is the inserted carbon-doped GaN layer. This suppresses the punch-through current and enables a hike in breakdown voltage from 580 V to 1.7 kV.

This device offers fast switching at 400 V and currents of up to 15 A. "Our next plan is realizing higher current operation in vertical GaN transistors," says Shibata.

During the next 12 months, breakthroughs in GaN transistors and other III-Vs will occur at Panasonic and elsewhere. Some of the most significant of these will be reported at IEDM 2017, which will be held in San Francisco, and is tipped to feature an ever greater coverage of compound semiconductor devices.

Another feature of the transistor of Shibata and co-workers is the inserted carbon-doped GaN layer. This suppresses the punch-through current and enables a hike in breakdown voltage from 580 V to 1.7 kV.



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Refining Communication Technologies

Will handsets be crammed with ever more III-V content?
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KEYNOTE

- **Zach Griffith: Teledyne Technologies** I InP HBTs for high-power 70 to 500 GHz amplification: its status today and where it is going

ANALYST

- **Asif Anwar: Strategy Analytics** I The foundry of the 2020's

SPEAKER

- **Dylan Kelly: Murata Manufacturing** I The all silicon handset - transforming the vision into reality
- **Bernd Heinz: Evatec** I $Al_{(1-x)}Sc_xN$ films for use in RF devices
- **David Danzilio: WIN Semiconductors** I Advancing GaAs integration

Optimising Light Emitters

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Are colossal LED fabs revolutionising chip manufacture? And what are the big opportunities for visible lasers?

KEYNOTE

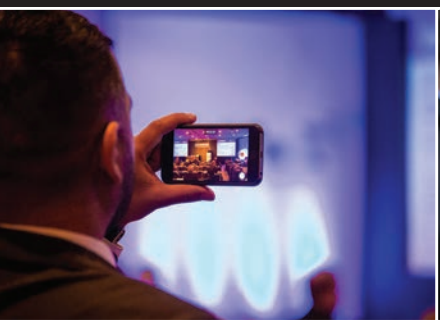
- **Hsu Chen K: Sanan Optoelectronics** I Creating the biggest and best LED chipmaker in China

ANALYST

- **Swapna Prakash** I Lighting-up India with LEDs

SPEAKERS

- **Oleg Shchekin: Lumileds** I Non-linear processes in LEDs and engineering for efficiency at high power densities
- **Martin Behringer: OSRAM Opto Semiconductors** I LED - more than just a light emitting cube
- **Tatsushi Hamaguchi: Sony Corporation** I Fulfilling the promise of the GaN VCSEL
- **Bedwyr Humphreys: Seren Photonics** I Overcoming the green gap using semipolar gallium nitride
- **Torsten Stoll: Nanometrics** I Study of Deep Ultra Violet Optical Property of AlGaN/GaN 2DEG Heterostructures



Exploiting Heterogenous Integration

What are the fruits of a marriage between silicon and the III-Vs? And can higher mobility materials improve microprocessors and memory?

KEYNOTE

- **Daniel Green: Defence Advanced Research Projects Agency – US Agency of Defence** | Advancing technology with heterogeneous integration

SPEAKERS

- **Soon-Fatt Yoon: Nanyang Technological University** | Heterogeneous integration of III-V devices on silicon with ultra-thin buffer utilising interfacial misfit dislocations
- **Jesús A Del Alamo: Microsystems Technology Laboratories** | Refining the III-V finFET
- **Nadine Collaert: imec** | Looking for the ultimate low-power switch: the promise of tunnel FETs
- **Veeresh Deshpande: IBM** | Advancing SRAM by adding III-Vs (COMPOSE project)
- **Shengkai Wang: Institute of Microelectronics of Chinese Academy of Sciences** | III-Vs and germanium for future logic
- **Arnaud Furnemont: imec** | 3D NAND scaling: an opportunity for alternative channel material
- **Gerard Colston: Advanced Epi Materials & Devices** | Silicon Carbide heteroepitaxy for mass production of semiconductor devices
- **Julie Orlando: Nanotronics** | Leveraging computer vision, machine learning, & artificial intelligence to assign causality of defects
- **Reinhard Windemuth: Panasonic** | Solutions for wafer-level packaging

Revolutionising Gallium Nitride RF Chips

Will GaN RF deliver the best bang per buck by increasing transistor voltages or making these devices on silicon? And what are the best options for really high frequencies?

KEYNOTE

- **John Palmour: Wolfspeed** | GaN-on-SiC RF: Poised for rapid adoption

ANALYST

- **Zhen Zong: Yole Développement** | GaN RF industry: landscape & future evolution

SPEAKERS

- **Rocco Giofrè: University of Rome Tor Vergata** | GaN Doherty amplifiers for backhaul radio links
- **Michael Ziehl: MACOM** | The virtues of GaN-on-silicon



Perfecting Power Electronics

Can the best devices stem from the ultra-wide bandgap of gallium oxide? Or will they emerge from foundries processing GaN and SiC on silicon?

KEYNOTE

- **Toshimi Hitora: FLOSFIA** | Unleashing the potential of gallium oxide — FLOSFIA

SPEAKERS

- **Tamara Baksht: VisIC Technologies** | High efficiency at high power density: realization of GaN's promise for power electronics — VisIC Technologies
- **Frédéric Dupont: Exagan** | Driving the GaN power device roadmap for large scale adoption — EXAGAN
- **Isik Kizilyalli: US. Department of the Energy Advanced Research Project Agency** | Current topics in electronic devices based on wide band-gap semiconductors for power applications and energy efficiency — arpa·e
- **Sujit Banerjee: Monolith Semiconductor** |Slashing chip costs with SiC-on-silicon — MONOLITH SEMICONDUCTOR INC.
- **Anthony Sagneri: FINsix Corporation** | Wide bandgap devices: the key to the world's smallest laptop charger — FINSIX
- **Markus Behet: EpiGaN** | From Hype to Reality: GaN/Si - where are we today? — EPIGAN
- **Ke Xu: Nanowin** | Bulk GaN substrate grown by HVPE — Nanowin 苏州纳维科技有限公司
- **Sudhakar Raman: Veeco** | Enabling 5G RF-GaN electronics through innovative MOCVD technology — Veeco
- **Anoop Somanchi: KLA-Tencor** | SiC and GaN defect inspection for power device market — KLA-Tencor
- **Jens Voigt: AIXTRON** | Establishing the tool-of-record for wide bandgap device manufacturing — AIXTRON

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Removing thermal barriers to GaN HEMTs

Power densities produced by GaN HEMTs can reach their full potential by integrating these devices with diamond and microfluidic cooling

BY MATTHEW TYHACH AND DAVID ALTMAN FROM RAYTHEON

THE GaN REVOLUTION is well underway, with the performance of RF systems on the rise, but ultimately limited in its full potential by thermal impediments. That's because while generating high RF output powers for signal transmission, GaN power amplifiers dissipate a commensurately large amount of power in the form of heat in the transistor and the chip area. More than 100 W of power can be dissipated by the chip, creating localized transistor hot spots with fluxes above 10 kW cm^{-2} and package-level volumetric heat generation that can exceed 100 W cm^{-3}.

Levels of power dissipation are so high that they are challenging the capabilities of conventional approaches to thermal management. It is no longer sufficient to prevent a device from overheating by positioning carefully selected materials nearby, and using them to transport heat to a local heat exchanger.

So great are the concerns of overheating that engineers are throttling back the operating voltage of the GaN HEMT and are also increasing its physical area. Such schemes limit channel temperatures to the desired operating region. An enhanced thermal management strategy would enable engineers to operate GaN HEMTs at higher voltages and in smaller areas, lowering the cost of an RF system on a cost-per-Watt basis, and opening the door to new systems that deliver more RF power while retaining their area.

At Raytheon we are researching this front under funding from the DARPA Intrachip/Interchip Enhanced Cooling (ICECool) programme. Our efforts have focused on developing a high-performance thermal management architecture. We replace a conventional GaN HEMT with one that features a high-conductivity CVD diamond substrate for enhanced heat spreading, and subterranean microchannels that improve heat removal.

With this design, material with the highest thermal conductivity known to man is positioned right underneath the GaN HEMT channel hot spot, and heat is extracted very efficiently by integrating the heat exchanger directly into the device's substrate. Thanks to these advances in thermal management, the power handling capability of today's GaN HEMTs can increase five-fold, enabling amplifiers to operate

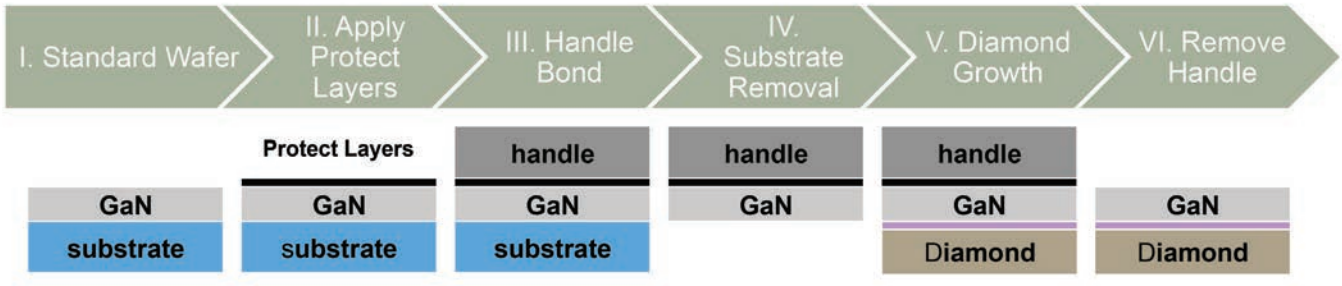
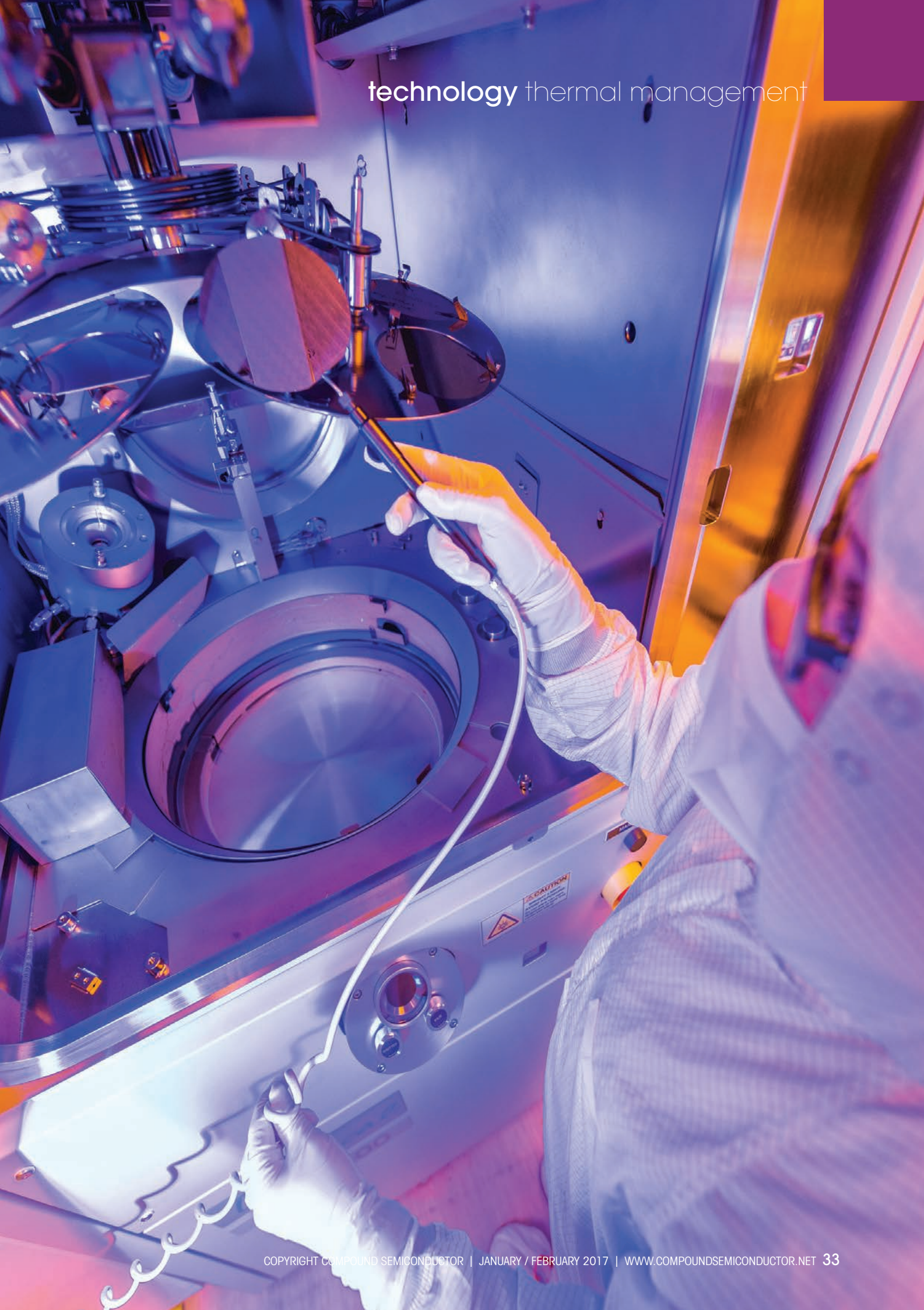


Figure 1. GaN epitaxial material is transferred from its growth substrate to a diamond substrate.



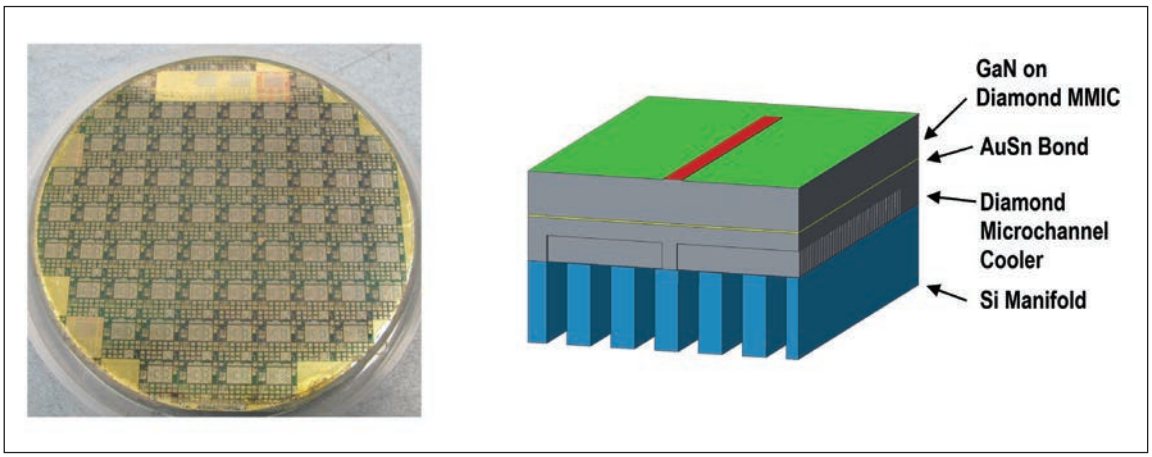


Figure 2. 100 mm GaN-on-diamond wafer after fabrication (left) and GaN-on-diamond with microchannel cooling (right).

at far higher power densities. This breakthrough ultimately has the potential to underpin yet another revolution in RF performance without inventing a new semiconductor technology.

Diamond and microfluidics

One of the great strengths of GaN-on-diamond is that it unites high-thermal conductivity CVD-grown diamond with GaN that is commercially available in production today. GaN-on-diamond substrates are created by removing the original substrate for GaN epitaxial growth – it could be silicon, sapphire, or SiC – and replacing it with CVD diamond through a direct diamond growth process (Figure 1).

To realise this, a protection layer is added to the topside of the GaN, and this is then bonded to a physical handle wafer. The protection layer allows removal of the handle wafer at the end of the process without damaging the GaN. Following substrate removal, a thin nucleation layer is applied prior to the growth of the diamond layer. This means that diamond is located just a few microns from the GaN hot-spot. The diamond dramatically improves heat spreading, thanks to a conductivity that is three times that of SiC. The pioneer of this process is Group4 Labs, since acquired by Element 6. Over the years, wafers have increased in diameter and yield, and 100 mm material is now available (see Figure 2, left).

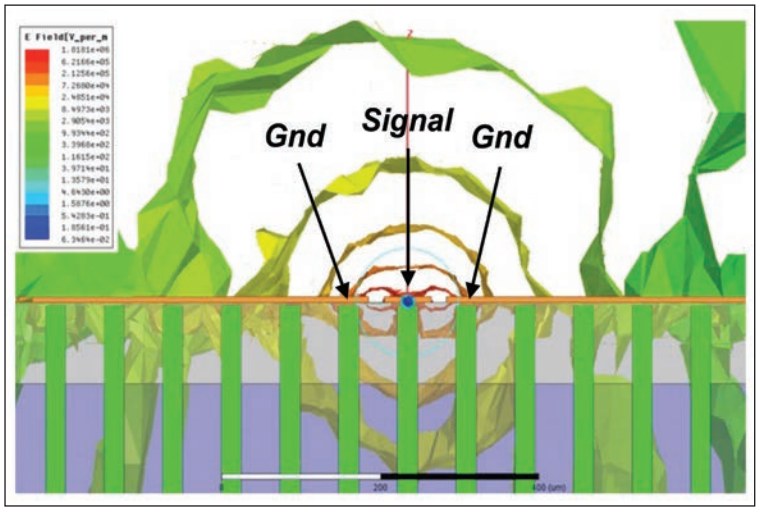


Figure 3. The ANSYS tool for high-frequency electromagnetic field has been used to assess microchannel placement (green) underneath co-planar waveguide transmission lines and the ground plane (orange).

To increase thermal performance over conventional systems that use either air cooling or fluidic cooling further downstream, we adopt a microfluidics technology that positions the heat exchanger very close to the diamond substrate. This is realised with high-aspect ratio diamond microchannels that are filled with a standard coolant (see Figure 2, right). Performance is optimised by placing the channels next to the hot spots of the GaN-on-diamond MMIC, and using a silicon manifold layer to regulate the direction, flow rate, and pressure of the coolant.

Measurements on an RF MMIC will ultimately highlight the capability of the combination of GaN-on-diamond and microfluidic cooling. Operating at the same temperature as a state-of-the-art GaN-on-SiC MMIC, our design models suggest an RF output power that is 4.9 times higher than our baseline MMIC. Superiority stems from an increase in MMIC periphery by a factor of 4.2 over the baseline, as well as a 50 percent increase in bias voltage (see Table 1). Note that the added periphery does not lead to an increase in the size of the MMIC because the gate-to-gate spacing within the transistor layout is shrunk by a factor of 4.

Conversion of the baseline design to a higher power MMIC began with consideration of the differences in electrical properties between SiC and diamond

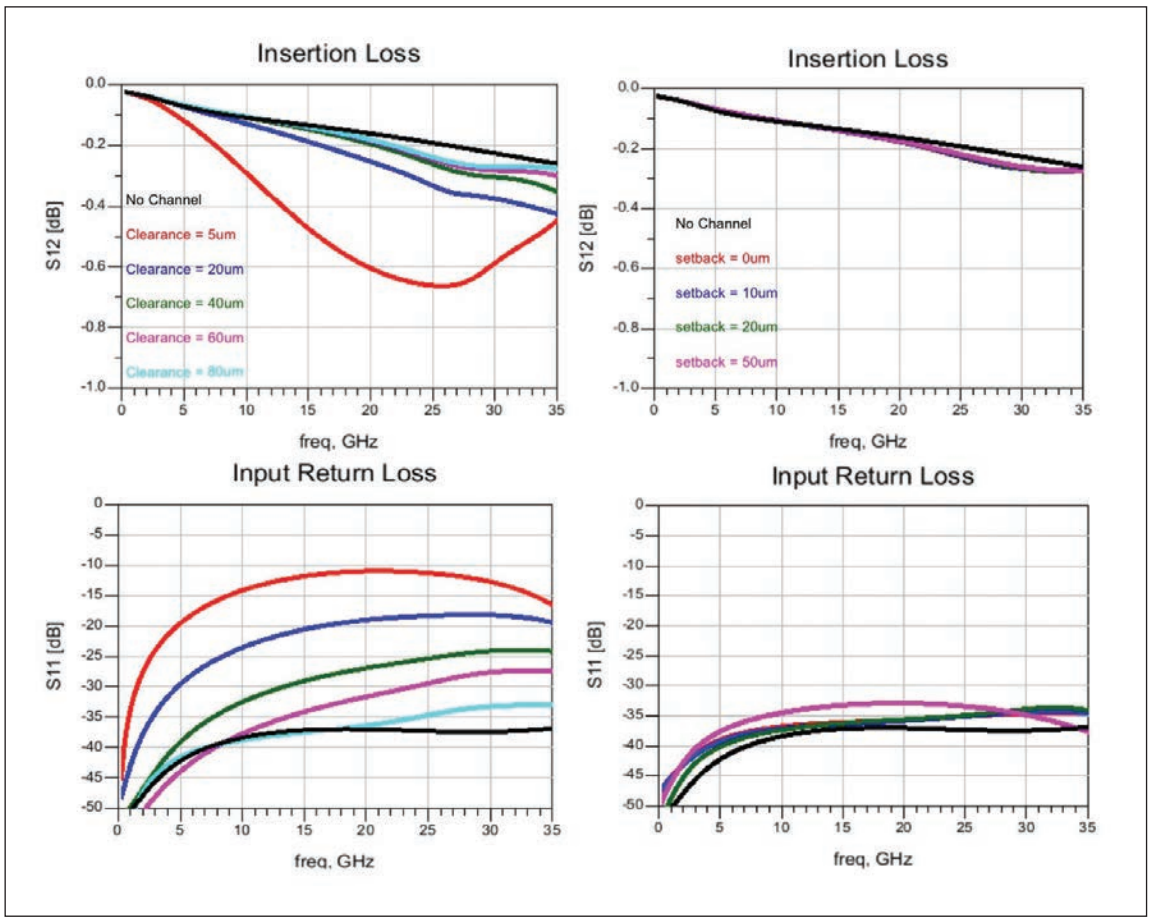


Figure 4. The ANSYS tool for high-frequency electromagnetic field simulations has provided insight into: transmission line with microchannel placement while varying depth underneath the conductor surface (left): and microchannel placement 80 μm below the conductor, while varying lateral setback from the conductor edge (right).

substrates. The baseline features co-planar waveguide transmission lines, formed on the substrate top surface by a centre-line surrounded by two ground planes. Measurement and modelling of test structures on diamond wafers revealed that CVD-grown diamond has an effective dielectric constant of 5.70, compared with 10.03 for SiC. A major impact of this difference is that the length of the transmission lines must be longer on diamond than on SiC to achieve the same electrical impedance.

Another focus of our work has been the optimisation of the location of microchannels in the substrate, to ensure maximum thermal and electrical performance. By minimizing the channel temperature and transmission line insertion loss, we increase the power-added efficiency of the MMIC.

We have used ANSYS for high-frequency electromagnetic field simulation to investigate the impact of fluid-filled microchannels in the substrate

Although the manufacture of our novel GaN HEMTs will require some new approaches, we have developed processes that address issues associated with wafer bow, wafer thickness, backside roughness and diamond etching. Our five-fold gain in performance through improved thermal management is revolutionary, and GaN MMICs operating at higher power densities should follow, as tools, processes and materials to make these devices are now in place.

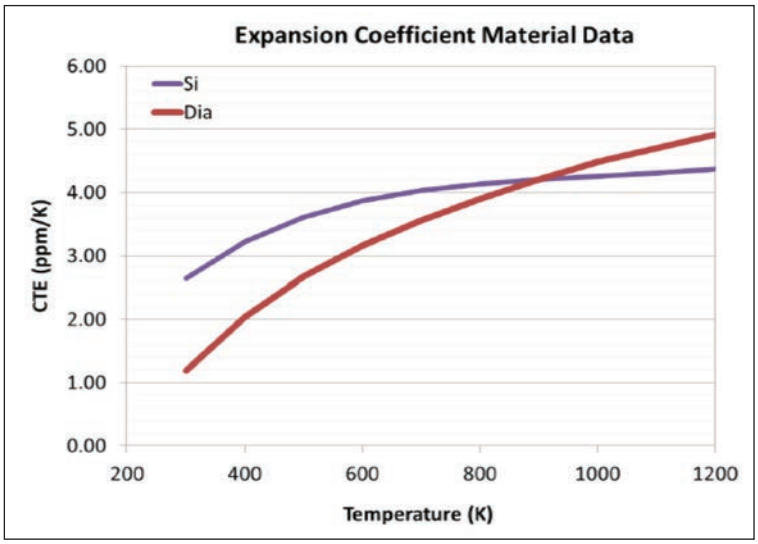


Figure 5. The mismatch in the coefficient of thermal expansion of silicon and diamond causes the wafer to bow as it cools from the growth temperature to room temperature.

on transmission line performance. These calculations allowed us to optimise the electrical placement of the microchannels (see Figure 3). Efforts began by varying the clearance depth from the top transmission line conductor surface to the top of the microchannel in the substrate. Calculations considered a baseline of no channel, and depths of up to 80 μm.

Results from these simulations reveal that a clearance of just 5 μm has a significant impact on insertion loss and impedance, while a depth of 80 μm has minimal effect at our frequency range of interest, which is X-Band (8 GHz -12 GHz) and below (see Figure 4, left). Setting clearance at 80 μm, we then analysed variable locations of the microchannels relative to the edge of the top transmission line and ground conductor surfaces, and varied the lateral setback by up to 50 μm. Results show that locating the microchannels underneath a conductive surface with any setback effectively negates any influence from having microchannels in the substrate. These insights led us to position the microchannels so that they are setback into the conductor surfaces and have a minimum clearance of 80 μm.

Production challenges

Today, GaN-on-diamond wafers present unique challenges for wafer processing foundries to create high-yielding and high-performance HEMTs and MMICs. One particular challenge arising from the unique properties of this engineered substrate is wafer bow. As growth of diamond occurs at high temperatures while the GaN is attached to the silicon handle wafer, distortion results during post-growth cooling, due to differences in thermal expansion coefficients (see Figure 5).

Another difference is that GaN-on-diamond wafers are thinner than commercially available GaN wafers, so that the increased cost of growing diamond is partially offset. Due to this, GaN-on-diamond wafers tend to be incompatible with the focal length range of most production lithography tools. To address all these issues, a supporting carrier wafer is bonded to the underside of a GaN-on-diamond wafer to reduce its bow and increase its height.

Fortunately, carrier wafers are not unique to semiconductor fabrication – they are already used in back end of line processing. However, the big difference with a GaN-on-diamond wafer is that a carrier wafer is needed for the entire fabrication sequence. This means that the bond to the carrier must be able to withstand all foundry chemicals and a wide range of temperatures, while still allowing release of the GaN-on-diamond wafer once fabrication is complete. On top of these restrictions, the carrier material must be stiff enough to reduce the bow of the GaN-on-diamond wafer; and it must have a

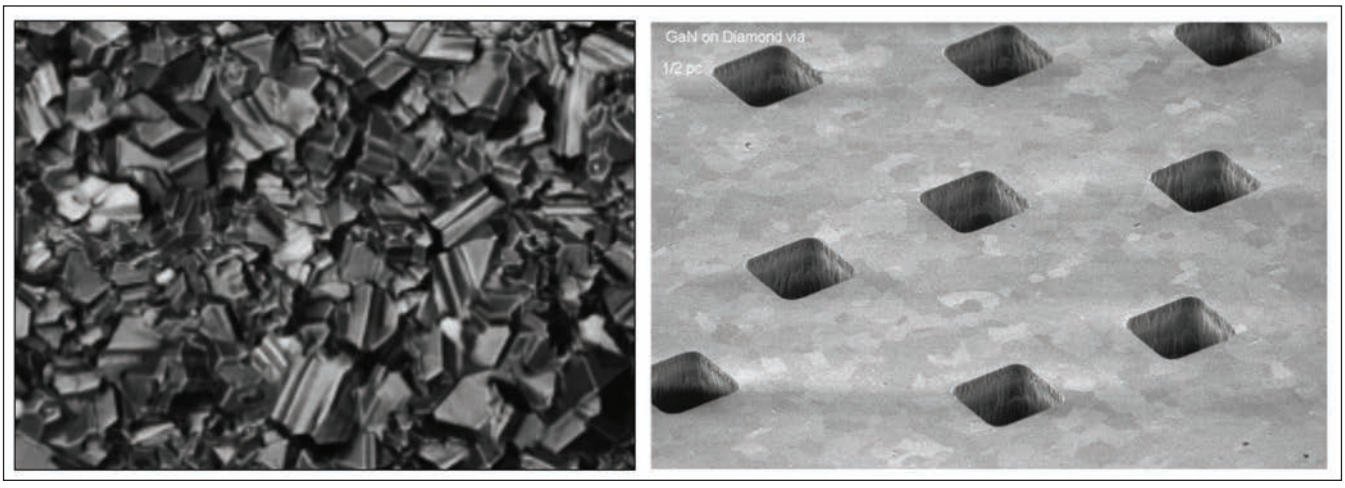


Figure 6. Diamond wafer backside surface before (left) and after (right) polishing and via formation.

thermal coefficient of expansion that is close to that of diamond, so that it does not unintentionally demount at higher temperatures during the fabrication process.

Fulfilling all these requirements narrows the selection of bonding materials and carrier wafers. We have identified what is suitable and have developed a bonding process that permits the mounting of GaN-on-diamond wafers in a manner that is compatible with high-resolution lithography.

Following completion of front-side fabrication, backside processing is undertaken, including the formation of microchannels for fluidic cooling. So far, we have worked with co-planar waveguide transmission lines, but we are also developing a backside process for forming through-substrate vias that will enable electrical grounding of designs incorporating microstrip transmission lines.

Etching diamond is required to form these microchannels and electrical grounding vias. This process is not trivial, because diamond requires different etchants from SiC, and fabricating patterned features requires novel masks that are not damaged or eroded during the etching process. Complicating matters even further, CVD diamond substrates tend to have a far higher degree of roughness than those made from crystalline silicon and SiC, so special consideration must be given to substrate preparation prior to etching. The good news is that we have demonstrated these unique backside processes that address the particular novel challenges associated with GaN-on-diamond wafers (see Figure 6).

Although the manufacture of our novel GaN HEMTs will require some new approaches, we have developed processes that address issues associated with wafer bow, wafer thickness, backside roughness and diamond etching. Our five-fold gain in performance through improved thermal management is revolutionary, and GaN MMICs operating at higher power densities should follow, as tools, processes and materials to make these devices are now in place.

	ICECool compared to current State of the Art GaN/SiC
Substrate	**Diamond**
Periphery	**4.2X increase**
Gate Pitch	**4.0X decrease**
Voltage	**1.5X increase**
P_{out}	**4.9X increase**

Table 1. Comparison of the key parameters between today's MMIC and the ICECool Demonstration MMIC.

The authors thank Dr. Avram Bar-Cohen and Dr. Ken Plaks for their leadership of the DARPA ICECool programs under which this work was performed. They also thank Dan Francis at Element 6 for assistance with GaN-on-diamond wafer material. This material is based upon work supported by the Defense Advanced Research Project Agency (DARPA) and United States Air Force under Contract No. FA8650-14-C-7469. The views expressed are those of the authors and do not reflect the official policy or position of the Department of Defense or the U.S. Government.

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UNITING III-V TUNNEL FETS WITH SILICON

Template-assisted selective epitaxy enables the construction of ultra-low power III-V TFETs on silicon substrates

BY DAVIDE CUTAIA, KIRSTEN MOSELUND, HEINZ SCHMID, MATTIAS BORG AND HEIKE RIEL FROM IBM

ADVANCES within the semiconductor industry have had a profound impact on the lives of all of us for more than 50 years. Industries as diverse as telecommunication, banking, consumer electronics, healthcare, and automotive have all benefitted from the adoption of electronic devices and information technology. This has revolutionized how we work, while re-shaping our society.

The driving force behind these significant changes has been the dramatic increase in integration density, made possible by shrinking the MOSFET. Packing smaller transistors closer together has slashed the manufacturing costs in a manner predicted by Gordon Moore back in 1965 (also known as Moore's law), and equipped end-costumers with ever increasing functionality at ever lower prices.

Unfortunately, as device dimensions have scaled, passive and dynamic power consumption has not kept pace. This has meant that reductions in supply voltage (V_{DD}) have lagged behind the rate of miniaturization at advanced technology nodes. Even for an ideal MOSFET, the off-state current (I_{off}) increases ten-fold when V_{DD} is reduced by 60 mV and the threshold voltage (V_{th}) is lowered accordingly (see Figure 1). This inherent weakness cannot be addressed by changes in material or device geometry, as it is associated with the inverse subthreshold slope (SS) of the MOSFET, which cannot be less than 60 mV/decade at room temperature, due to thermionic emission of electrons over a potential barrier.

To overcome the 60 mV/decade limit, developers of next-generation transistors are exploring novel devices that are based on different physical mechanisms. One of the most promising architectures is the tunnel FET: it resembles the MOSFET, but does not rely on thermionic emission [1]. Instead, carriers are injected into the channel via quantum-mechanical, band-to-band tunneling (BTBT).

With a TFET, BTBT acts as an energy filter, ensuring that only carriers within a certain energy range contribute to the conduction of current. With hot carriers filtered out, the steep-slope SS is no longer barred from plunging below the thermal limit of 60 mV/dec. What's more, as the TFET can operate below a V_{DD} of 0.5 V, and the passive power is proportional to V_{DD} and the off-current, a device's power consumption could plummet by a factor of 100.

The TFET consists of a *p*-*i*-*n* reverse-biased diode, with a gate overlapping the intrinsic region (see Figure 2). This device can be formed from one or more materials, and ideally it should deliver a high on-state current I_{on}, because this reduces the delay time constant RC of the circuit and therefore increases the operating frequency.

Producing a high I_{on} is not easy, however, because it depends on the tunneling probability (in contrast, for a MOSFET, I_D is proportional to the applied gate bias). To produce a higher I_{on}, materials with smaller bandgaps and lower effective masses should be used, as they provide higher tunneling probabilities; and direct bandgap materials should be selected, as they reduce interactions between charge carriers and phonons. Silicon is far from ideal, because it has a large effective mass, and its indirect bandgap leads to a lower tunneling probability, due to interactions between charge carriers and phonons.

The case for III-Vs

Turning to III-V materials for the construction of TFETs is very appealing. It provides the opportunity to use direct bandgap materials with low bandgaps and small effective masses. Furthermore, lattice matched III-V heterostructures allow the engineering of tunnel junctions with large tunnel currents. Note that to obtain a complementary logic similar to that of an *n*-MOSFET/*p*-MOSFET, band alignment for the TFETs must be designed for *p*-type conduction or *n*-type conduction.

At IBM Research, Zurich, we are developing this class of TFET. We are pursuing the pairing of InAs and silicon for the *p*-type device, and the combination of InAs and GaSb for the *n*-type cousin. The former has the smallest tunneling bandgap for holes in a staggered band alignment, whereas the latter exhibits very high electron tunneling rates in a broken-gap configuration.

One of the challenges of this approach is that it demands the integration of different materials. And in order to be economically viable, the III-V-based TFET

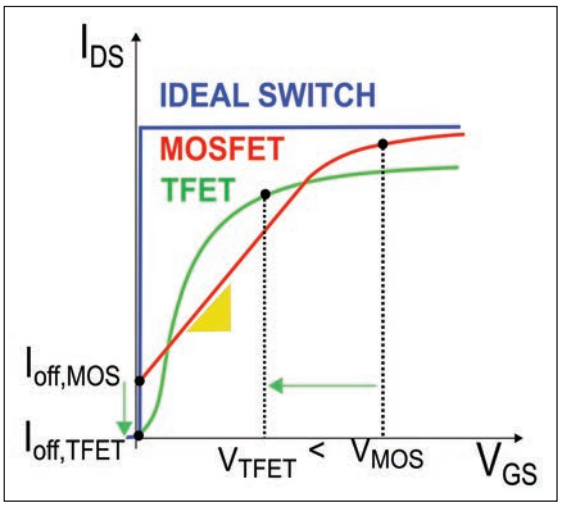

Figure 1. Typical transfer characteristics (I_{DVG}) for a MOSFET (red) and a TFET (green). An ideal switch (blue) would provide the highest on-state current at the smallest gate voltage (V_{GS}) and a large on/off ratio. The inverse subthreshold swing (SS) of a MOSFET is limited to 60 mV/dec, which precludes operation at voltages below 0.5 V. In contrast, in a TFET, the SS can be smaller, enabling the decrease of the supply voltage V_{DD} and the dynamic power consumption. In addition, the energy filtering effect in a TFET allows a further reduction of I_{off} compared with the MOSFET, which substantially reduces static power consumption.

technology must be integrated on a standard CMOS-compatible substrate.

To address these challenges, we have been developing a method for integrating III-Vs on silicon, along with a compatible process flow for *p*- and *n*-type devices.

Integrating III-Vs with silicon is very challenging, due to the significant lattice mismatch between the two materials. This difference in atomic spacing gives rise to interfacial defects, which can eventually propagate through the entire crystal and degrade electrical performance.

To address this issue, there have been attempts to integrate III-Vs with silicon using various technologies, including metamorphic buffers, wafer bonding, epitaxial lateral overgrowth, aspect-ratio trapping and selective area growth. However, all these approaches are afflicted with at least one of the four following weaknesses: exorbitant fabrication costs, unsatisfactory crystal quality, a process that is unsuitable for scaling, and a process that is not capable of integrating III-Vs with the (100) orientation of the silicon substrate.

In stark contrast, our new technology – template-assisted selective epitaxy (TASE) – is unimpeded by any of those four issues, and enables the integration of dislocation-free III-V crystals on silicon (100). Key steps in our process include: the definition of a sacrificial silicon layer on either a bulk silicon (100) or silicon-on-insulator (SOI) substrate; the formation of a SiO_2 template around the silicon; and the etching of the template at one side and of the sacrificial layer, to leave an empty tube and a silicon seed for III-V growth by MOCVD (see Figure 3 for an outline of the process, and [2],[3] and [4] for more details).

A noteworthy element of our technology is the nucleation of the III-V crystal on a small silicon seed, which yields a material with a high crystal quality. Subsequent growth is confined inside the template that defines also the device geometry. These attributes are highly valued for TFETs, because the crystal quality of the heterojunction strongly affects the tunneling current. Device performance gets an additional boost from the growth of III-Vs on a buried oxide of SiO_2, which electrically isolates the devices and reduces leakage-current paths through the silicon substrate.

Our TASE technology is suitable for the fabrication of InAs and GaSb nanowires, which can be very closely packed to each other (see Figure 4). The InAs

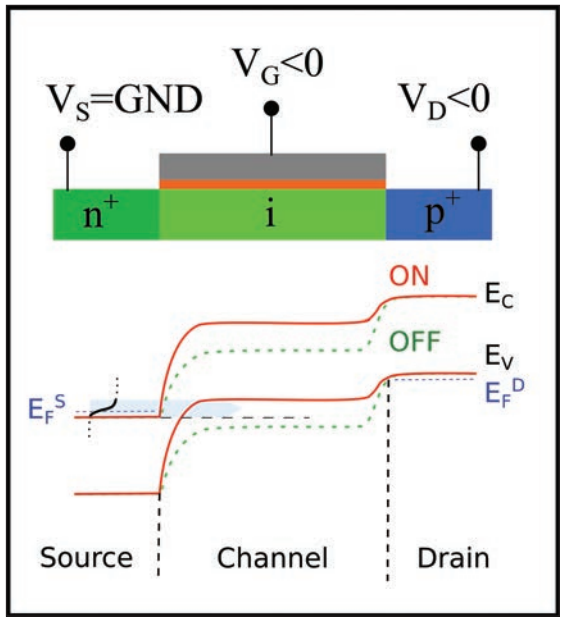

Figure 2. A *p*-type TFET, and a corresponding band diagram. In this case, the source voltage (V_S) is fixed to ground (GND), whereas the negative drain voltage V_D determines a reverse-bias operation. The gate voltage (V_G) shifts the channel bands downwards (off-state) or upwards (on-state), respectively blocking or enabling the band-to-band tunnelling current (blue-shaded area). The band alignment in the TFET is responsible for the energy-filtering mechanism that effectively cuts off the high-energy tail of the source Fermi function (E_{FS}) and enables a subthreshold swing of below 60 mV/decade.

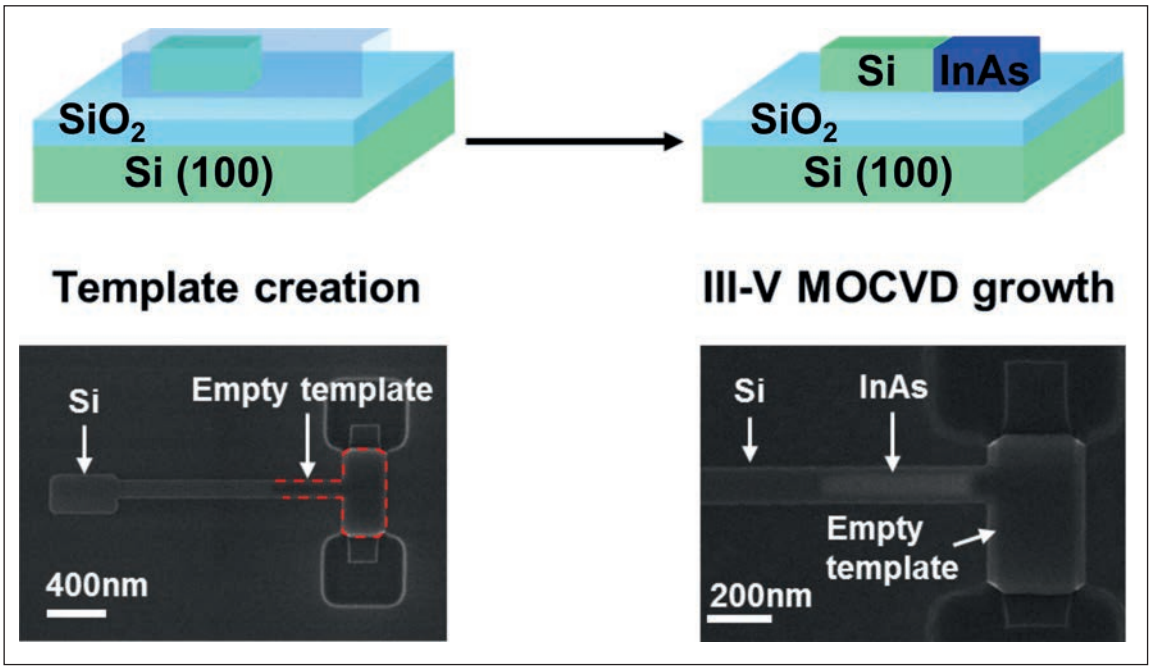

Figure 3. Templated-assisted selective epitaxy can form a lateral InAs/silicon hetero-junction (details are given in [3,5]). The silicon segment (green) inside the SiO_2 template (light blue) defines the seed for selective MOCVD growth of III-V material, such as InAs (dark blue). The heterojunction that is created lies on a buried oxide that electrically isolates the device from the substrate.

nanowires were grown first, before adjacent channels were filled with GaSb. Note that our technology is not limited to the integration of III-V TFETs – its great versatility allows it to be applied to other III-V devices, including MOSFETs, photodetectors, LEDs, and lasers. Thanks to this, it is possible to form a variety of devices on a single chip, all positioned at their desired location.

Fabrication of our TFETs continues with the definition of a pair of high-κ dielectrics, Al_2O_3 and HfO_2, and the addition of metal gates made from either TiN or tungsten. Afterwards, spacer and metal contacts for source and drain regions are defined for both polarity devices.

High-κ dielectrics are used in our TFETs, because they provide excellent charge coupling to the channel, thereby improving electrostatics and the sub-threshold slope. However, care must be taken to avoid a degradation of the sub-threshold slope through interface traps, which can be formed during the deposition of high-κ materials on III-Vs.

The narrowness of our silicon, InAs and GaSb nanowires highlights the potential of our TASE technology. Cross-section areas as small as 17 nm x 27 nm and 25 nm x 35 nm have been obtained for the *p*-TFET and *n*-TFET (see Figure 5). These devices are the first demonstration of a complementary III-V heterostructure TFET technology on silicon that yields transistors at relevant technological nodes, and employs a lateral orientation that is compatible with the state-of-the-art CMOS fabrication line. We have evaluated the performances of our *p*- and *n*-TFETs at a range of temperatures, using a standard four-probe electrical setup. Transfer characteristics were determined at a source-drain bias of 0.5 V (see Figure 6). For both devices gate leakage current is negligible, and does not affect the characteristics (not shown here, see [5]).

The InAs/silicon *p*-TFET exhibits excellent performance, with a large on-off ratio of 10^6, an I_{on} of few μA/μm, and a SS that falls from about 70-80mV/dec at room temperature to 50 mV/dec at 125K.

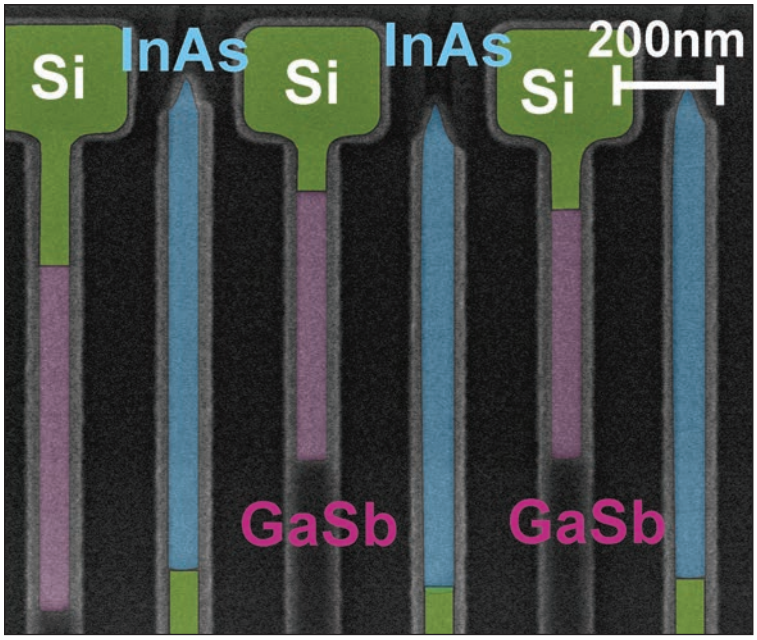

Figure 4. InAs (blue) and GaSb (pink) nanowires grown by MOCVD with a spacing of less than 200 nm between them, including the silicon nucleation seed (green). Using templated-assisted selective epitaxy, it is possible to obtain a very tight integration density of diverse III-V materials and devices for increased on-chip functionality.

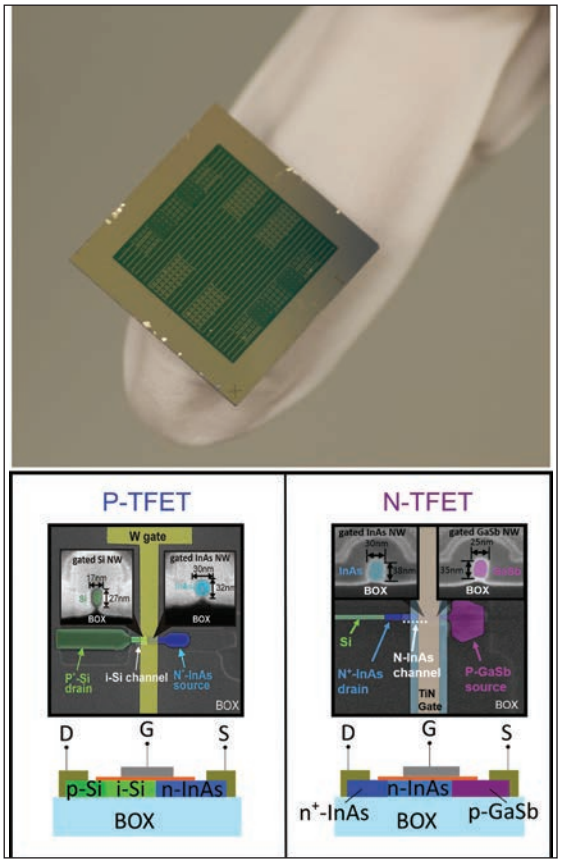

Figure 5. A 2 cm x 2 cm chip containing TFETs fabricated by templated-assisted selective epitaxy, and a corresponding false-coloured top-view scanning electron microscopy image of *p*-type (bottom left) and *n*-type (bottom right) devices. For simplicity, *p*- and *n*-TFETs have been implemented on two different wafers, but as shown in Figure 4, the processes are compatible. The dimensions achieved are 17 nm x 27 nm and 25 nm x 35 nm for *p*- and *n*-TFETs, respectively.

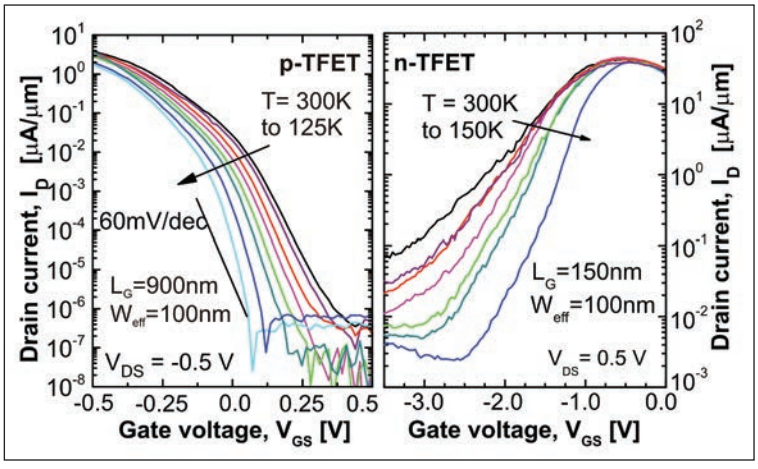

Figure 6. Temperature-dependence characteristics of *p*-TFETs (left) and *n*-TFETs (right). The subthreshold swing improves at lower temperatures, because traps at the heterojunction and at the high-κ/III-V interfaces are frozen out.

The SS improvement with cooling occurs because a fraction of the traps present at the InAs/silicon heterojunction are frozen out, leading to a trimming of the trap-assisted tunneling current.

Our InAs/GaSb *n*-TFET also exhibit an improvement in SS at lower temperatures. However, BTBT is inhibited by the presence of traps at the hetero-junction, which prevent the SS dropping below 60 mV/dec [6,7]. We aim to address this by reducing the number of traps at the heterojunctions and the high-κ/III-Vs interfaces.

Following more than 50 years of integration technology that has revolved around the silicon MOSFET, our work, along with that of some of our peers, shows that there is the possibility of a new form of transistor for low-power applications. There are many challenges that still need to be overcome, but this development will bring hope to engineers that need to build ultra-low power circuits for the likes of the Internet-of-Things (IoT) market.

In this particular market, numerous devices will collect and transmit large amounts of data simultaneously. This will be partially analyzed on the chip, and further in the cloud. However, a major concern surrounding the IoT is the power consumption of the electronics. Energy harvesting to power sensors in buildings would allow power to be distributed efficiently and wirelessly to where it is needed. Still, the power consumption of the electronics on chip should be as low as possible to enable real-time communication among devices. For these requirements, TFETs could have an edge over the so far most successful device concept, the MOSFET.

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GaN ON ANYTHING

Giving GaN freedom from SiC with Nb_2N

BY DAVID MEYER, BRIAN DOWNEY, D. SCOTT KATZER, MARIO ANCONA, SHAWN MACK AND LAURA RUPPALT FROM THE U.S. NAVAL RESEARCH LABORATORY

GaN devices are transforming our lives. Leading the way is the LED, which is lighting our homes, offices and public spaces, thanks to its competitive pricing, great efficiency and ability to hit full brightness in an instant. But there is also a significant and growing market of GaN electronics, where devices are becoming increasingly attractive for efficient power switching and amplifying RF power. Within this sphere, GaN is enabling the construction of DC-AC inverters with unprecedented efficiencies of above 95 percent that can serve solar photovoltaics and electric/hybrid cars; and it is providing power amplifiers for radar systems and communication networks with RF output power densities that are ten times that of those based on more conventional III-V compound semiconductors, such as GaAs and InP. Impressively, for this application, the level of superiority provided by GaN spans nearly all microwave and millimetre-wave frequencies.

Despite all the material advantages that GaN brings, it would be naive to believe that this wide bandgap technology can provide all the microelectronic functionality desired for today's mixed-signal systems, and do so at low power consumption levels and acceptable costs. Why would anyone choose GaN for high-density digital logic or memory, when silicon CMOS is so far advanced and widely available?

In a circuit designer's ideal world, the optimal solution would involve a seamless mixing of disparate technologies/materials, in a manner that mirrors the construction of objects with coloured LEGO blocks. However, this concept of heterogeneous integration remains far from being fully realized.

One major roadblock is that the best substrates for ensuring high-quality growth of electronic materials tend to be incompatible with critical design goals, such as low thermal resistance and cost.

To tackle this issue head on, our group at the Naval Research Laboratory has recently developed a versatile technique that releases III-N devices from their costly SiC substrates. This technology has the potential to form freestanding GaN and AlN.

The pivotal enabler is a thin layer of niobium nitride, Nb_2N. It has several important attributes: a close lattice-match to GaN; temperature-compatibility with III-N growth; and a selective etch character over GaN, AlN and SiC. Using Nb_2N as a sacrificial layer allows simple processing, based on standard fabrication equipment, for the lift-off and transfer of III-N devices to any desired substrate after completing front-side processing and yield screening.

There are numerous opportunities arising from this new technique. Potential uses range from enhancing discrete device performance via improved thermal management to reducing cost through substrate re-use and achieving superior hybrid circuit performance with device-level heterogeneous integration.

Developing niobium nitride

Our efforts focus on the β phase of Nb_2N. This metallic allotrope has a hexagonal crystal structure similar to that of SiC, GaN, and AlN (see Figure 1 for details of how it compares with common wide bandgap, hexagonal materials).

Aside from their similar crystal structures and common anion, Nb_2N and other III-N materials have very little in common. As opposed to GaN, where there is a wide thermodynamic stability window that tolerates large variations in the gallium-to-nitrogen ratio during crystal growth, the Nb-N compound family has as many as nine different phases, making the growth of the desired β–phase very difficult and strongly dependent on stoichiometry. Making matters even more challenging, niobium has to be heated to nearly 2500 °C before it melts. That's substantially higher than the temperature limits of conventional effusion cells used in MBE – they typically top out at 2000 °C.

The good news is that the MBE process does not take place in thermodynamic equilibrium. This allows the window for the growth of a thin film of single phase β–Nb_2N to be expanded via growth kinetics. This is the route we have taken in our plasma-assisted, nitride MBE system that incorporates an electron-beam evaporator source. Armed with this tool, we can overcome the temperature limitation of conventional effusion cells and generate a sufficient flux of niobium in its metal form to gain control and flexibility over the growth kinetics of the material. Extensive MBE growth development and materials characterization led us to uncover a window of conditions that produce atomically-smooth, single-phase β-Nb_2N films on SiC substrates between 775 °C and 850 °C – temperatures that are compatible with standard MBE III-N growth.

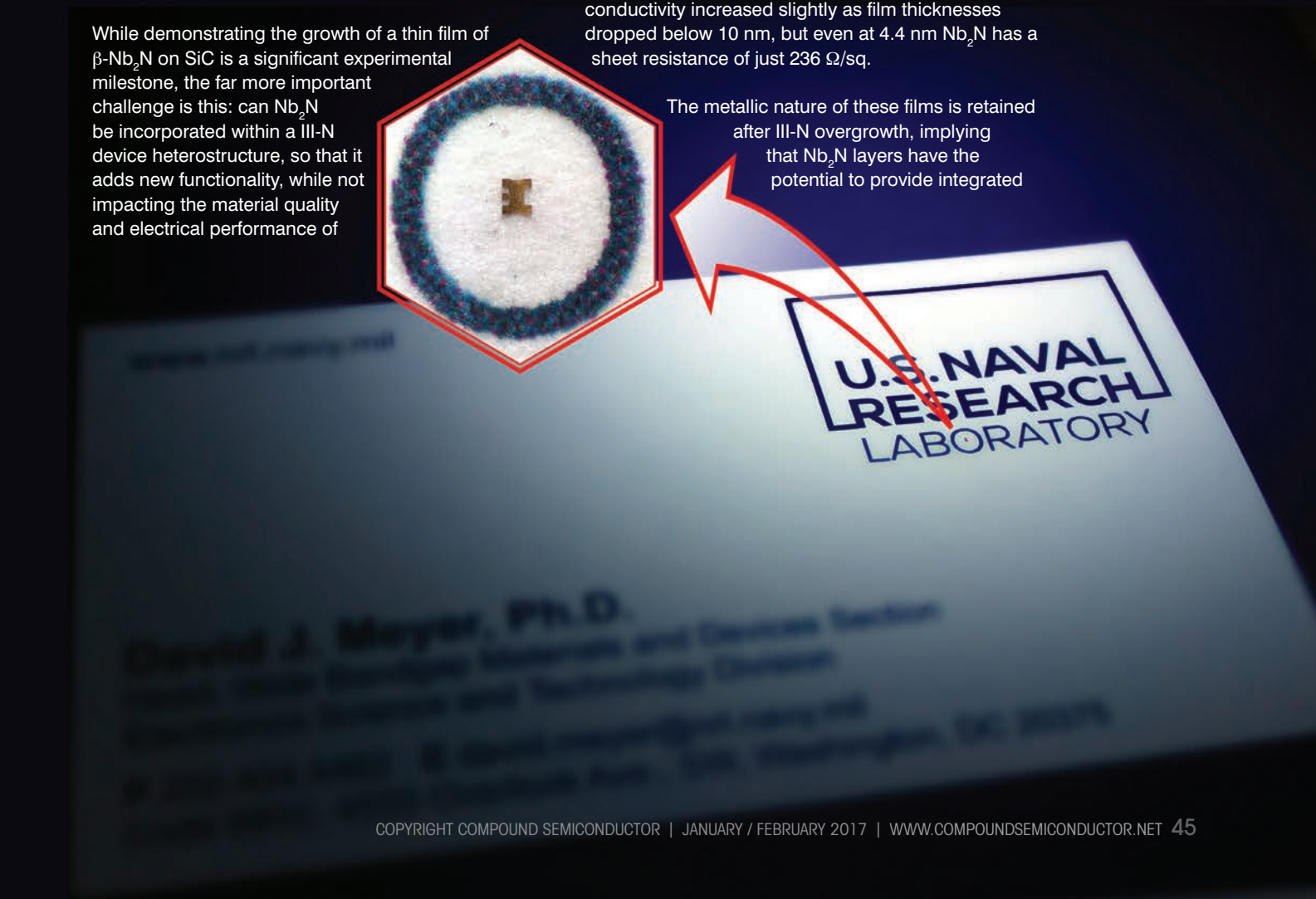
While demonstrating the growth of a thin film of β-Nb_2N on SiC is a significant experimental milestone, the far more important challenge is this: can Nb_2N be incorporated within a III-N device heterostructure, so that it adds new functionality, while not impacting the material quality and electrical performance of the subsequent III-N layers? Fortunately, it can, with our work showing that AlN and GaN heterostructures with high crystallinity and electrical quality can be grown on Nb_2N/SiC templates, much in the same way these films can be grown directly on SiC.

One example that confirms device-quality epitaxy is possible is our fabrication of high-performance N-polar GaN/$Al_{0.4}Ga_{0.6}N$ HEMTs, grown on Nb_2N/6H-SiC (silicon-face). These devices feature a two-dimensional electron gas with a sheet resistance of 350 Ω/sq., a sheet carrier density of 1.30×10^{13} cm^{-2}, and Hall mobility of 1400 cm^2/Vs. The mobility results are within 10 percent of those measured on similar N-polar HEMT structures grown directly on 6H-SiC (carbon-face).

Interestingly, the standard growth conditions that generate metal-polar films on silicon-face SiC have a tendency to produce N-polar films on Nb_2N. However, by adjusting the growth parameters of the AlN nucleation layer on Nb_2N, it is possible to realise polarity control and obtain the metal-polar orientation.

The capability to produce a thin layer of single-crystal metal adds a new instrument to the III-N device designer's toolbox. Exploring Nb_2N films of varying thickness in a series of experiments confirmed that the material was indeed metallic, with a 'bulk' conductivity of approximately 40 μΩ·cm. This conductivity increased slightly as film thicknesses dropped below 10 nm, but even at 4.4 nm Nb_2N has a sheet resistance of just 236 Ω/sq.

The metallic nature of these films is retained after III-N overgrowth, implying that Nb_2N layers have the potential to provide integrated



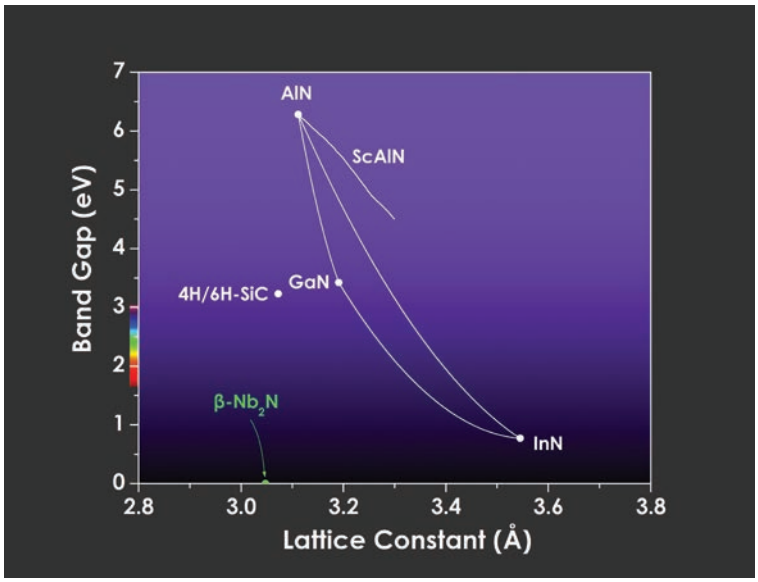


Figure 1: Energy bandgap and lattice constant of several hexagonal crystalline materials.

ground planes for microstrip transmission, or buried contacts for active or passive vertical devices. Since Nb_2N and AlN are predicted to be in thermodynamic equilibrium up to 1500 °C, buried or top-side Nb_2N electrodes should be able to tolerate high thermal budgets and exhibit high reliability, due to the limited solid-state reaction. This means that they should be able to support higher junction temperatures than conventional Schottky gate contacts.

Piquing the interest of solid-state physicists, our Nb_2N films undergo a superconductivity transition at around 10 K. This opens up interesting possibilities for novel devices that integrate a nanometre-thick superconducting material within an ultra-wide bandgap semiconductor material system that features polarization.

In addition to the potential of Nb_2N as an electrode material, it has a very promising attribute that may ultimately deliver a far greater impact: it can be easily and selectively removed from other III-N materials. Etching with the reactive non-plasma gas XeF_2, which is commonly used in silicon micro-electro-mechanical system processing, Nb_2N can be rapidly removed vertically – and laterally, in the case of a buried layer. While this proceeds, there is virtually no etching of GaN, AlN, or most common metals and dielectrics. Alternatively, selective wet chemical etching based on nitric and hydrofluoric acid can remove Nb_2N. In either case, by inserting a thin Nb_2N layer, a fully processed III-N device can be completely separated from its substrate.

Transfer techniques

Capitalizing on the selective etch capability of Nb_2N, we have developed an epitaxial lift-off (ELO) technique that enables the transfer of III-N material, devices, or circuits to an alternative substrate (an overview is provided in Figure 2). Starting with an Nb_2N/SiC template, epitaxy creates a III-N heterostructure prior to conventional front-side processing steps to produce devices or circuits. Subsequent electrical test and/or yield screening can then identify known-good devices or circuits for transfer. After this, a masking layer is patterned over the devices intended for ELO, before a deep mesa dry etch exposes the buried Nb_2N layer. Prior to the XeF_2 release etch step, photoresist

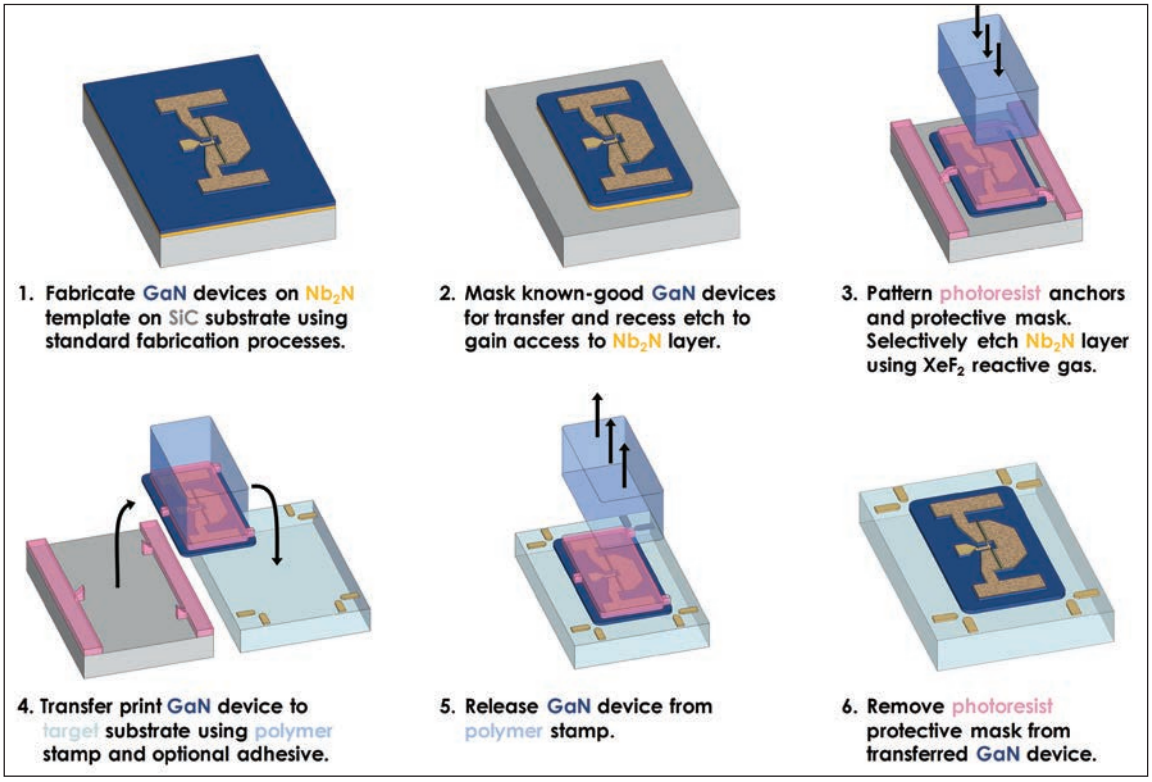


Figure 2: The epitaxial lift-off (ELO) technique developed at the Naval Research Laboratory can be applied to a GaN HEMT grown on Nb_2N/SiC.

anchors and a top-side protective layer can be patterned to temporarily tether devices in place.

One promising technique for manufacturable transfer of tethered devices is micro-transfer printing. It is a process that has been pioneered by John Rogers' group, previously at University of Illinois and now at Northwestern University, and commercialized by X-Celeprint, Inc. The key technology is the use of a polydimethylsiloxane (PDMS) elastomer stamp to retrieve devices from a source wafer and place them on a target substrate.

There is a great deal of freedom with this approach, because the PDMS stamp can be moulded into custom shapes and sizes to define the area of contact between the stamp and individual released devices. What's more, it allows the batch transfer of multiple devices.

During retrieval, the stamp is brought into contact with the tethered device intended for transfer. Stamp retraction then preferentially breaks the device tethers, leaving the device adhered to the stamp and completely separated from the source wafer. To transfer to a target substrate – this could be another semiconductor wafer, or glass, paper, metal, or just about anything – the device-laden elastomer stamp is brought into contact with the new substrate. Once this occurs, the stamp is retracted at a slow speed with a degree of lateral (shear) motion to reduce the adhesion force of the stamp and ultimately leave the device behind on the target substrate.

Bonding may be improved by applying a thin adhesive layer to the target platform prior to transfer. If further processing of the substrate with transfer-printed devices is required, this is possible, thanks to a placement accuracy for the transferred devices that is better than 2 μm.

We have evaluated the electrical performance of our N-polar HEMTs after their transfer to target substrates using ELO. To improve adhesion to the target substrate, an 80 nm-thick, spin-on interlayer dielectric polymer was included in the process.

Electrical measurements have compared the performance of devices bonded to different substrates (see Figure 3, which also includes a scanning electron micrograph of a transferred device on silicon). Reductions from pre-release values are probably caused by device self-heating, which can be traced back to the thermal resistance at the device/substrate bonding interface, as well as thermal conductivity differences across target substrates.

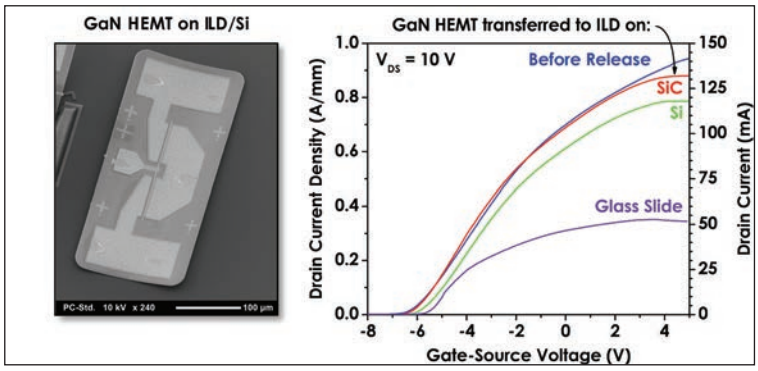


Figure 3: (Left) Scanning electron micrograph of a 2 × 75 μm N-polar GaN HEMT transferred to an 80 nm interlayer dielectric on silicon and (right) device transfer characteristics after bonding to various substrates with an interlayer dielectric adhesive. The slight curvature in the 1.5 μm-thick bonded device is caused by stress induced by device alloyed metal electrode processing, as released regions of unprocessed III-N heterostructure material are relatively flat and exhibit excellent bonding to target substrates. Mitigation strategies are being investigated for residual stress. Modifications to the released device membrane geometry and/or the application of a temporary external strain compensation photoresist or dielectric layer are expected to help reduce curvature during the bonding step.

Evaluating opportunities

As the idea of using Nb_2N as a sacrificial layer for ELO is new, it is difficult to predict the impact it will have on the compound semiconductor community. However, it certainly has great promise in several areas, including: the fabrication of RF power amplifiers with improved heat-sinking; the provision of a new route to heterogeneous integration; the housing of LEDs on flexible substrates; and improved RF filters at higher frequencies, for next-generation wireless communication. All of these opportunities are now discussed in turn.

One of the biggest weaknesses of GaN-based MMICs is that the performance, while surpassing that of conventional III-Vs by a significant margin, is limited by power de-ratings that are imposed to reduce peak junction temperatures and prevent early chip failures. To address this shortcoming, several recent research initiatives have been launched to improve the thermal management of GaN HEMTs, such as the DARPA Near-Junction Thermal Transport (NJTT) and Intrachip/Interchip Enhanced Cooling (ICECool) programmes. One option enabled by our technology – and similar to the NJTT approach – is to transfer a device or a MMIC membrane from a SiC substrate

Possibly the greatest benefit could come in the deep UV, as our ELO process would allow the removal and recycling of the bulk AlN substrate, which can compromise efficiency by absorbing UV emission from the LED

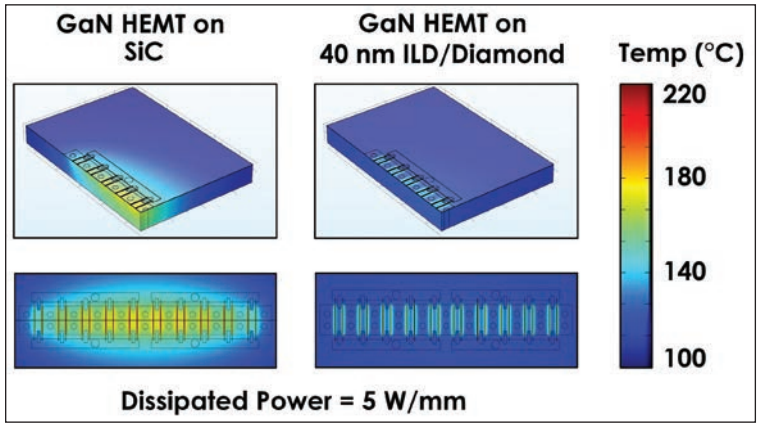


Figure 4: Thermal simulation of 20 × 150 μm GaN HEMT on SiC (left) and 40 nm of interlayer dielectric on single-crystal diamond (right).

to a single-crystal diamond wafer. This would situate the device on a substrate with a thermal conductivity that is five times higher, and lead to improved thermal management for the chip. Simulations suggest a significant benefit, even when the interlayer dielectric between the GaN device and diamond is 40 nm-thick (see Figure 4).

Our ELO process for heterogeneous circuitry could aid the construction of circuits that employ the best material for each function. DARPA is backing efforts in this area via its Diverse Accessible Heterogeneous Integration (DAHI) programme, which involves the integration of GaN power amplifiers with other semiconductor technologies, such as silicon CMOS, InP and SiGe.

Transferring GaN circuits or devices directly to silicon with ELO could enable additional front-side processing to cost-effectively create hybrid circuits with very short signal routing. If through-device vias were processed after transfer, this could facilitate vertical connections within this heterogeneous technology.

Wearable displays, a sector continuing to gain popularity, could also benefit from our technology. Here, the incentive to produce micro-LED displays on flexible substrates is increasing. This market could be served by growing and fabricating high-quality III-N LEDs on SiC, and then using our ELO process to transfer these devices to glass or plastic. Since the released LEDs are lithographically defined, they can combine a similar pitch with a very small pixel size – on the order of a few microns. Possibly the greatest benefit could come in the deep UV, as our ELO process would allow the removal and recycling of the bulk AlN substrate, which can compromise efficiency by absorbing UV emission from the LED.

Another opportunity for our technology exists in the wireless sector, which is facing ever-greater crowding of the allocated frequency bands within the electromagnetic spectrum. This is being addressed with smarter bandwidth management, and a key technology for accomplishing this is the reconfigurable, miniaturized, high-Q filter operating above the S-band. Such filters are in high demand, but are challenging to produce due to the poor material quality of the sputtered AlN films used in modern cell phone duplexers. The quality of these films, which are only a few tenths of a micron thick, are so poor that it is difficult to increase the centre frequency in bulk acoustic wave (BAW) and contour-mode resonator (CMR) filters much above a few gigahertz. Turning to our Nb_2N template technology can address this: it enables the growth of high crystalline quality AlN, or improved piezoelectrics like ScAlN, at thicknesses of less than 200 nm. These films can then be suspended

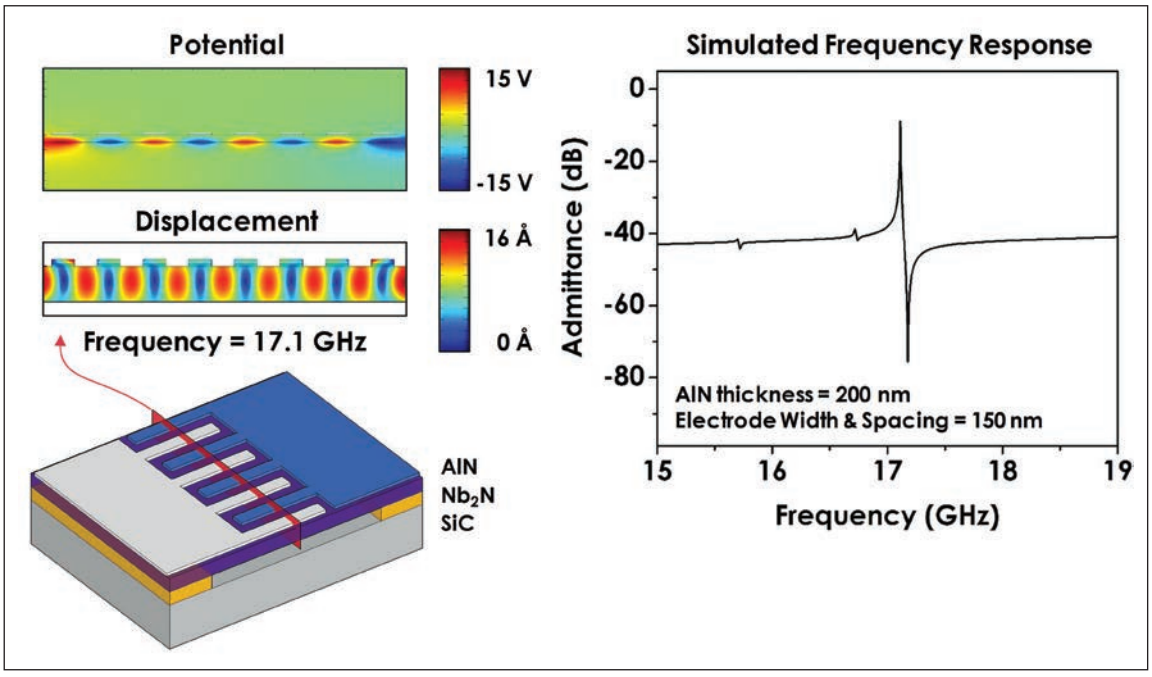


Figure 5: Simulation of a single-crystal AlN contour mode resonator, which could provide a filter for wireless communication at several GHz.

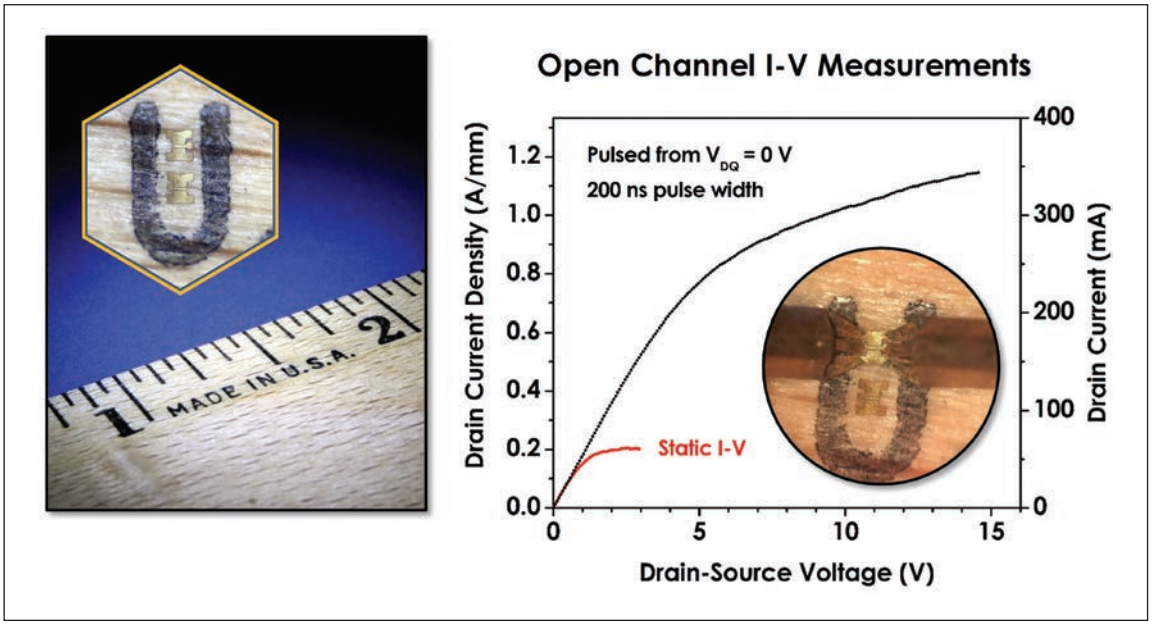


Figure 6: Static and pulsed current-voltage open-channel characteristics for an ungated N-polar GaN HEMT that has been transferred to a wooden ruler.

via partial removal of the underlying Nb_2N layer. To assess the potential of such devices, we have simulated the performance of a 200 nm-thick AlN CMR. Results are summarized in Figure 5.

In addition to all of these promising opportunities for our Nb_2N technology, it could also have a role in bringing together III-Vs with vastly different materials, such as paper and plastic. As the ELO technique is compatible with micro-transfer printing, one could imagine ways to populate a sheet of paper with an LED display or to integrate a power amplifier and antenna into the glass windshield of a car.

New energy and medical applications could also emerge, based on the micro-assembly of multi-junction photovoltaics on flexible plastic or the formation of high data-rate wireless communication circuitry on bio-resorbable polymers. To showcase the potential of the transfer of devices to different foundations, we have transferred one of our N-polar GaN HEMTs to a wooden ruler (see Figure 6 for static and pulsed open-channel, drain-current curves).

We are very excited to be exploring the impact that Nb_2N can have on III-N applications and technology. When applied to ELO and transfer, Nb_2N offers a number of important advantages over competing lift-off methods involving ion implantation or photo-electro-chemical etching. Aside from producing an atomically-smooth, bonding-ready released device or circuit backside, our ELO process can recycle substrate material indefinitely, potentially leading to significant cost savings.

With a predicted thermodynamic stability for Nb_2N and AlN of up to 1500 °C, typical III-N growth methods should be capable of producing standard device heterostructures that tolerate a high thermal budget during subsequent processing. Although epitaxial conductors are a relatively unexplored frontier in microelectronics, it's easy to envisage many applications.

The authors are grateful for research funding support from the Office of Naval Research and from the Defense Advanced Research Projects Agency (D. Green). The views, opinions and/or findings expressed are those of the authors and should not be interpreted as representing the official views or policies of the Department of Defense or the U.S. Government. The authors would also like thank D. Jena, S. Mohney, C. Bower, K. Ghosal, N. Nepal, V. Wheeler, M. Hardy, D. Storm, J. Champlain, and N. Green for research support and helpful discussions.

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KEYNOTE

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ANALYST

- **Vladimir Kozlov: LightCounting Market Research** | Impact of integrated photonics on the optical communications market

SPEAKERS

- **Mehrdad Ziari: Infinera** | Large scale coherent PICs in optical networks
- **Martin Guy: Ciena Corporation** |Strategies for photonic integration for metro and long-haul networks
- **Tom Williams: Acacia Communications Inc.** | Putting silicon photonics to work on metro and long haul applications
- **Le Binh: Huawei Technologies** | Integrated photonics systems to meet challenges in optical and wireless system convergence
- **Michael Wale: Oclaro Technology** | PIC-enabled telecommunications and data centre interconnects: state of the art and future prospects

Supporting Data Centre Growth

Short reach communications could be a major win for PICs. But what are the customer priorities? And how can photonic integrated circuits come out on top?

KEYNOTE

- **Richard Pitwon – Seagate Technology** | Opportunities for data centre optical interconnects

SPEAKERS

- **James Regan: EFFECT Photonics** | InP as a platform for photonic integration
- **Karen Liu: Kaiam Corporation** | Perspectives on hybrid integration as a rapid and flexible route to upgrading today's datacenters
- **Bert Jan Offrein: IBM** | Scalable integration concepts to drive down the cost of data centre photonics
- **Robert Blum: Intel Corporation** | Silicon photonics and the future of optical connectivity in the data centre
- **Jörg-Peter Elbers: ADVA Optical Networking** | Silicon photonics for inter-data centre interconnects




Optimising PIC Design, Manufacturing & Packaging

What are the best resources for creating and delivering photonic integrated circuits?

KEYNOTE

- **Michael Watts: MIT** | Bringing resources together to drive photonic integration

SPEAKERS

- **Peter O'Brien: Tyndall National Institute** | Overcoming packaging hurdles for PIC devices
- **Suresh Venkatesan: POET Technologies** | Realizing gains in energy efficiency, component cost and size-reduction through photonic integrated solutions
- **Peter de Dobbelaere: Luxtera** | The design and processing of advanced transceiver integrated circuits
- **Gilles Lamant: Cadence Design Systems** | Providing mainstream design flow for PICs
- **André Richter: VPIphotonics** | Advances in layout-aware schematic-driven design automation for integrated photonic and optoelectronics
- **Twan Korthorst: PhoeniX Software** | Research-centric to product-centric
- **Ignazio Piacentini: ficonTEC** | Testing as part of the manufacturing chain: photonics wafers, singulated dies, and fully packaged devices
- **Ronald Broeke: BRIGHT Photonics** | Is PIC design difficult? A survival guide
- **Pieter Dumon: Luceda Photonics** | Lean PIC design for innovators: a reality check
- **Scott Jordan: Physik Instrumente** | Recent advances in industrial photonic alignment automation: An emerging enabler for test and packaging economics

New markets: Sensing, Medical?

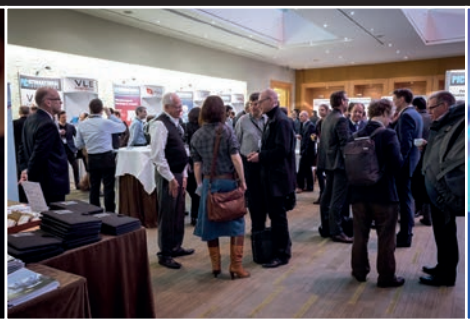
What are the prospects for developers more broadly? And how does the supply chain need to adapt?

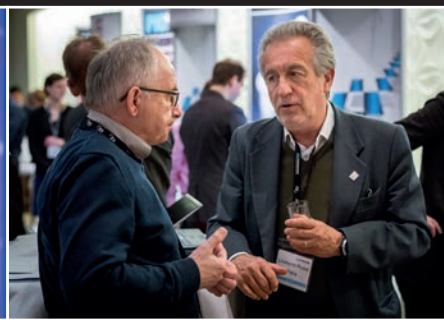
KEYNOTE

- **Liesbet Lagae: imec** | imec's progress as the pix4life project in the field of SiN photonics in the visible range for life science applications

SPEAKERS

- **Pim Kat: Technobis Group** | Extreme fibre sensing: PIC opportunities beyond datacoms and telecoms
- **Iain McKenzie: European Space Agency** | PICs: The final frontier
- **Ewit Roos: Photon Delta** | Why European photonics is undervalued and a fast-track plan of how to change it



PIC Platforms

What are the key materials systems driving photonic integration? And how should these platforms evolve to unlock greater performance?

KEYNOTE

- **Graham Reed: University of Southampton** | Ion implantation of Ge into silicon to form photonics devices

SPEAKERS

- **Roel Baets: Ghent University** | Silicon photonics beyond transceivers
- **Timo Aalto: VTT Research** | Thick-SOI for PICs and I/O coupling
- **Dimitris Tsiokos: Phosnet Research Group, Aristotle University of Thessaloniki** | CMOS compatible plasmo-photonics for mass-manufactured, powerful PICs
- **Michael Geiselmann: LIGENTEC** | Applications for thick film silicon nitride integrated circuits
- **Arne Leinse: LioniX International** | TriPleX™: The low loss industrial silicon nitride waveguide platform. Application examples from VIS to IR
- **Zhihong Huang: Hewlett Packard Enterprise** | Silicon photonics as a PIC platform for next generation datacentre architectures
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- **Ruth Houbertz: Multiphoton Optics** | Topic to be announced

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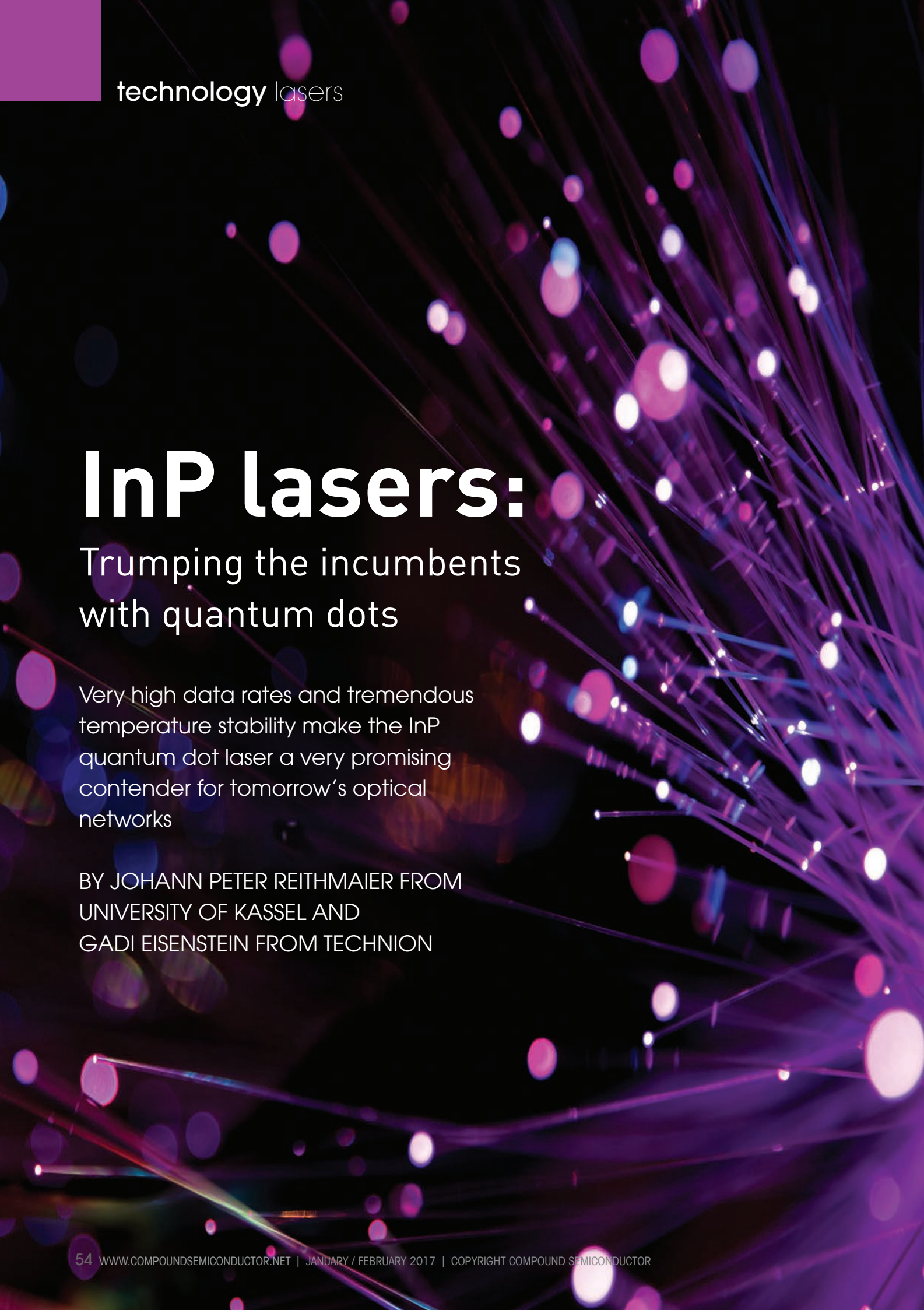

InP lasers:

Trumping the incumbents with quantum dots

Very high data rates and tremendous temperature stability make the InP quantum dot laser a very promising contender for tomorrow's optical networks

BY JOHANN PETER REITHMAIER FROM UNIVERSITY OF KASSEL AND GADI EISENSTEIN FROM TECHNION

THE SEMICONDUCTOR LASER is netting annual sales of billions of dollars, thanks to its deployment in an ever growing number of applications that include optical communication, material processing, medical applications and sensing technologies.

Since the 1980s, sitting at the very heart of this device has been the quantum well. This replaced the bulk material employed beforehand, delivering hikes in reliability and performance. Improvements resulted from the utilisation of a degree of quantum size effects to tailor carrier confinement and tune emission wavelength.

One should not think, however, that the quantum well active region is ideal. It suffers from severe intrinsic problems, and is a far from perfect gain material. Flaws include a laser performance that is strongly dependent on the device's operation temperature, due to the occupation of carriers in states that fail to contribute to laser oscillation. This non-efficient use of carriers makes the threshold current density much higher than one would want it to be. Making matters worse, this limitation is exacerbated with InP based materials emitting in the 1.3 - 1.6 μm range, which is the most important wavelength domain for optical fibre communication.

Another drawback of quantum-well gain material is its asymmetric gain profile. This broadens the emission linewidth of CW lasers and increases their frequency chirp under modulation. If the well could be replaced with a superior gain material that has a symmetric gain profile, emission broadening could be fully suppressed, immediately enabling the fabrication of CW lasers with a narrow linewidth and essentially chirp-free modulation capabilities.

Ideally, an optical gain material is atom-like, with discretized energy levels and occupation restricted to the ground state. To accomplish this, energy separation between the ground state and the excited states must be large enough to prevent the excitement of carriers to these higher energies at any operational temperature. Fulfil this requirement and optical gain will peak at the ground state transition, with no carriers 'wasted' through the occupation of other levels. Quantum dots that exhibit atom-like behaviour can accomplish this (see Figure 1).

The fundamental advantages of atom-like or quasi zero-dimensional gain material are well-established, and were known to developers of semiconductor lasers shortly after the introduction of quantum well materials. However, back then no-one knew how to fabricate a quantum dot laser.

A major breakthrough came in the mid-1990s, through the introduction of the so-called Stranski-Krastanov growth technique. It enables defect-free epitaxy of high-density quantum dot layers (see Figure 1 for an atomic force microscopy image). Unfortunately, the size of the dots within these layers varies, resulting in transition linewidth broadening, due to the quantum size effect. This is a major impediment, because it increases spectral gain significantly. The bottom line is that the predicted intrinsic advantages of ideal quantum dot lasers are masked by the imperfections of nanoscale structures.

In the intervening years, the properties of quantum dot material have vastly improved. 1.3 μm GaAs quantum dot lasers were first produced at the start of this decade, and more recently our partnership between the Univeristy of Kassel and Technion has extended this technology to longer wavelengths, pioneering InP-based quantum dot lasers that operate at 1.55 μm. This material is actually better than GaAs for making quantum dots lasers, as the built in strain is just 3.2 percent, rather than 7.2 percent. This makes InP-based quantum dot lasers mechanically much more robust, and it is also possible to compensate for the compressively strained quantum dot layers with tensile-strained barriers.

Superior temperature stability

Our success hinges on two major breakthroughs in InP-based quantum dot material. Firstly, we have trimmed size fluctuations. This has led to an emission

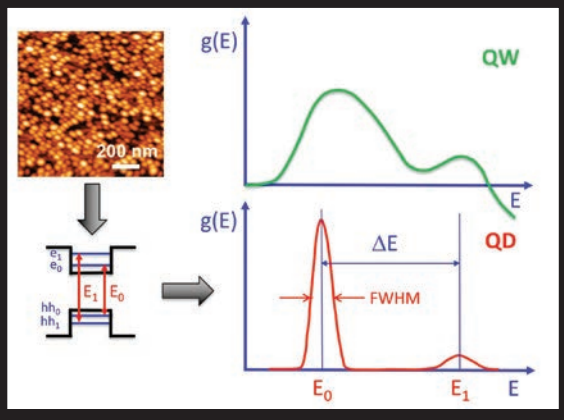

Figure 1. Schematic gain spectra of a quantum well (QW) and quantum dot (QD) material, respectively. The left top picture shows an atomic force microscope image of a high-density QD layer. The figure below illustrates schematically the confined electronic and hole states in a QD and the related ground (E_0) and first excited state (E_1) transitions. FWHM denotes the full width at half maximum.

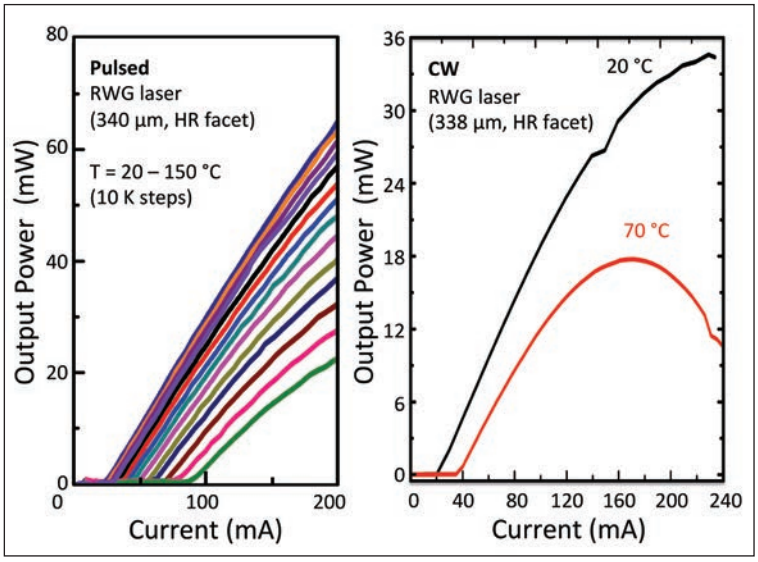

Figure 2. Light output characteristics of pulsed (left) and CW (right) operated short-cavity ridge waveguide quantum dot lasers for different operation temperatures. The back facets are high-reflection (HR) coated, the front facets are as-cleaved.

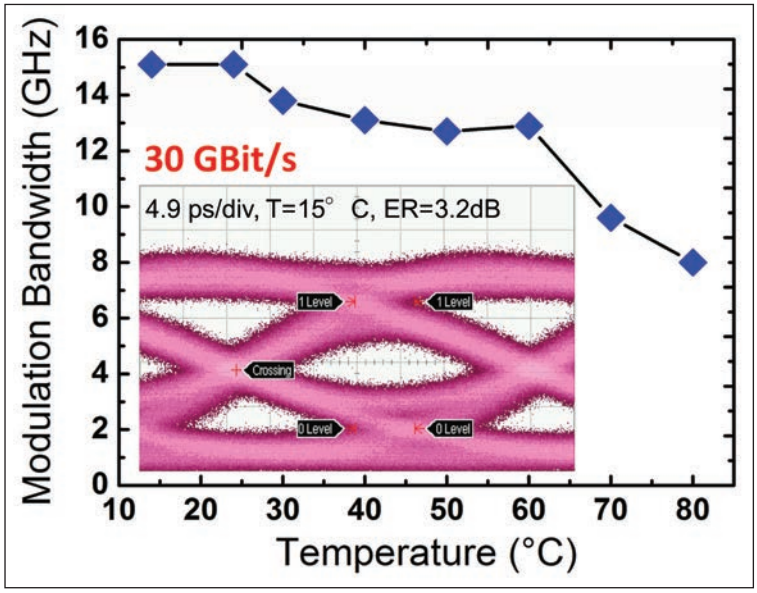

Figure 3. Small signal modulation bandwidth as a function of temperature with nearly constant small signal modulation response between 10 °C and 60 °C. The inset shows an eye-diagram for 30 Gbit/s direct digital modulation.

linewidth for a single quantum dot layer of just 17 meV at 10 K, and a corresponding value of 30 meV for a six-layer stack used as the gain region in laser structures. Secondly, we have increased the density of dots to 6 x 10^{10} cm^{-2}.

These advances have had a strong impact on the modal gain of this class of device – our laser has produced record values of up to 14 cm^{-1} per dot layer, or more than 80 cm^{-1} for an entire structure. So high are these values that they prevent gain saturation, even in the very short laser cavities needed for high-speed devices. Another attribute is that the splitting energy in the dots is high enough to slash carrier losses that come from thermal excitation (see Figure 1).

Thanks to these superb material properties, our lasers have a far higher temperature stability than their quantum well predecessers. Operating in pulsed current mode to avoid parasitic heating effects, ridge waveguide lasers that feature eight quantum dot layers have a characteristic temperature (T_0) of 136 K up to 75 °C, and 110 K up to 150 °C (see Figure 2, left).

This figure of merit, which characterizes the temperature dependence of the threshold current, exceeds that of a typical quantum well laser by factors of two to two-and-a-half. Over operating temperatures that span 20 °C to 100 °C, the external differential efficiency – that is, the slope of the curves – is essentially constant.

We have also characterised the CW output of our quantum dot lasers (see Figure 2, right). Devices with a short-cavity ridge waveguide and six quantum dot layers produce an output in excess of 35 mW at 20 °C, but are restricted to below 20 mW at 70 °C.

Our lasers have been dynamically characterized in small- and large-signal modulation. Plots of small-signal -3dB bandwidth as a function of operating temperature reveal high temperature stability of the modulation bandwidth, which is 14±1 GHz between 15 °C and 60 °C (see Figure 3). The high degree of stability stems from the high temperature stability in threshold current and the consistency in the slope of light output characteristics.

Eye diagrams for this laser have been obtained under digital modulation (an example at 30 GBit/s is shown in the inset of Figure 3). The eye closes at 36 GBit/s, which is a record for any quantum dot laser.

Manufacturers of high-volume, high-performance components for data-com applications spanning 1.25 - 1.65 µm will take note of this record value, because it demonstrates that our lasers can fulfil the demand for 25 or 28 GBit/s directly modulated data channels without temperature control. Freedom from temperature control and operation at elevated temperatures are highly valued, because they enable our devices to be deployed in low-cost, small form-factor optical cables using course wavelength division multiplexing or simple multi-wavelength pulse amplitude modulation (PAM4) formats.

Encouragingly, the best is still to come for our quantum dot lasers, because they have the potential for even high temperature stability and far faster modulation speeds. Through optimization of the epitaxy and laser design, inhomogeneous gain broadening should reduce, improving spectral gain by a factor of three to four. In turn, the higher gain should lead to doubling of the modulation bandwidth, so that direct modulation rates exceed 60 Gbit/s. Temperature stability should also improve, thanks to a narrowing of the gain peak and an increase in the energy splitting to the excited states.

Uniting with silicon

To realise high-volume production, we must combine our technology with that of silicon, so that these devices are manufactured on high-yield, large-wafer fabrication facilities that are already used in silicon photonics. Up until now, the most common approach for hybrid integration of III-V components involves the construction of individual devices using flip-chip technology. However, die and wafer-bonding techniques are under development for devices with more complex functionalities, such as multi-channel transmitters. An example of this approach has been undertaken in the European project SEQUOIA, which includes members of our team at the University of Kassel. Part of this programme involves the development of bonding processes for GaAs- and InP-based quantum dot laser materials on silicon photonic chips (see Figure 4 for an example of wafer and die bonding).

One of the goals for SEQUOIA is to demonstrate data-com transmitter chips for 400 Gbit/s point-to-point communication. Efforts will involve two approaches: 16 directly modulated 25 Gbit/s channels, and a quantum dot, laser-based frequency comb with a 16 channel on-chip ring modulator array. On-chip integration will be with either silicon-based photonic circuits, or together with driver or logic circuits. Regardless of the approach, it is imperative that the process yields a highly reliable, temperature-insensitive, high-performance light source. Our latest quantum dot laser material is better suited to fulfilling those demands than its quantum well counterparts.

Narrow linewidths

As previously mentioned, one of the merits of atom-like gain material is its symmetric gain function (see Figure 1). Ideally, this results in emission with an incredibly narrow linewidth, which can be quantified by a Henry linewidth enhancement factor, α, of zero. In comparison, the value of α in a standard quantum well laser is 3-4, which broadens the linewidth by about an order of magnitude. This indicates that while the linewidth of a III-V laser depends on features of its design – such as the cavity length, coupling strength of feedback gratings and quality factor of the cavity – it can be trimmed by an order of magnitude by substituting a quantum well active region with an appropriate quantum dot structure.

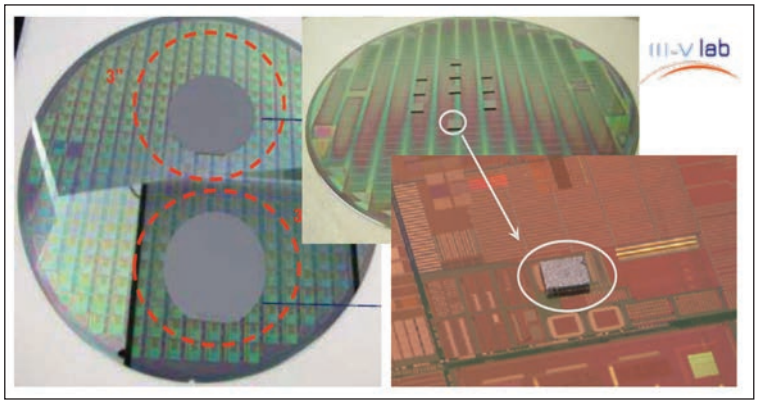

Figure 4. Examples of 3-inch wafer bonding on a silicon-wafer (left) and of die bonding (right) [Courtesy of III-V Lab].

Measurements on our 1.2 mm-long distributed feedback lasers with two quantum dot layers show that as injection current increases to 200 mA, photon density in the cavity rises and linewidth falls to about 110 kHz (see Figure 5). This laser, which has lateral index gratings on both sides of its ridge waveguide, can produce an output power exceeding 9 mW, and realise a stable side-mode suppression ratio of more than 40 dB.

The narrow linewidth above 200 mA makes this laser an attractive candidate for higher order modulation formats in coherent communication, such as quadrature phase shift keying or quadrature amplitude modulation (QAM). With these technologies, the number of detectable symbols depends on the

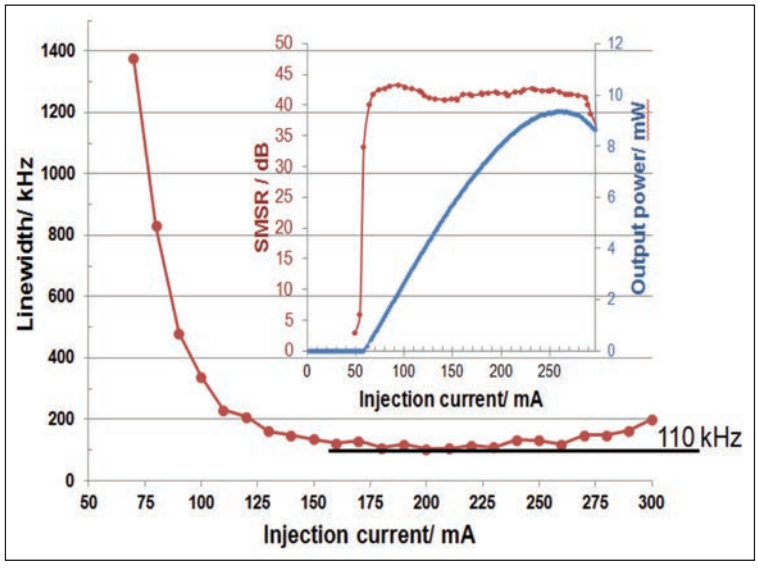

Figure 5. Emission linewidth of a quantum dot, distributed feedback laser as a function of the injection current. The inset shows the light output characteristics in CW operation and the side-mode suppression ratio (SMSR).

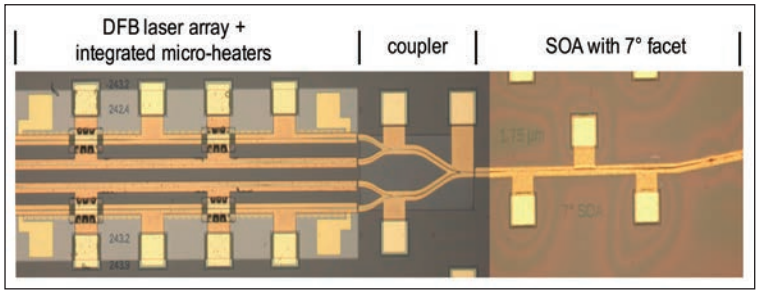

Figure 6. An integrated optoelectronic chip with four arrayed QD DFB lasers, integrated micro-heaters, 3dB coupling network and a subsequent amplifier section. The total chip length is about 4 mm.

frequency resolution of the reference laser. In high-capacitance transmission lines, modulation formats up to 256 QAM are used – they must distinguish 256 states and allow parallel transmission of 8 bits per channel. Further increases in the data transmission rate can come from the Baud rate and the number of wavelengths used in a dense wavelength division multiplexed system. However, for the latter, the reference laser must to be precisely tuned to each channel wavelength, which needs a widely tuneable, spectrally pure light source.

Working within the European EUREKA project SASER, we developed a quantum dot laser that is based on a tuneable light source and utilises the intrinsic quantum features of this zero-dimensional gain material. Our integrated optoelectronic light source contains a distributed feedback laser array with different grating periods (see Figure 6). Applying thermal tuning to this chip – that features a quantum dot semiconductor amplifier section to equalise the power levels before boosting them higher – allows emission to cover the entire C+ communication band between 1525 and 1570 nm (see Figure 7). Following amplification, the emission linewidth is about 130 kHz, with a value that depends on the laser current, but is independent on the SOA current.

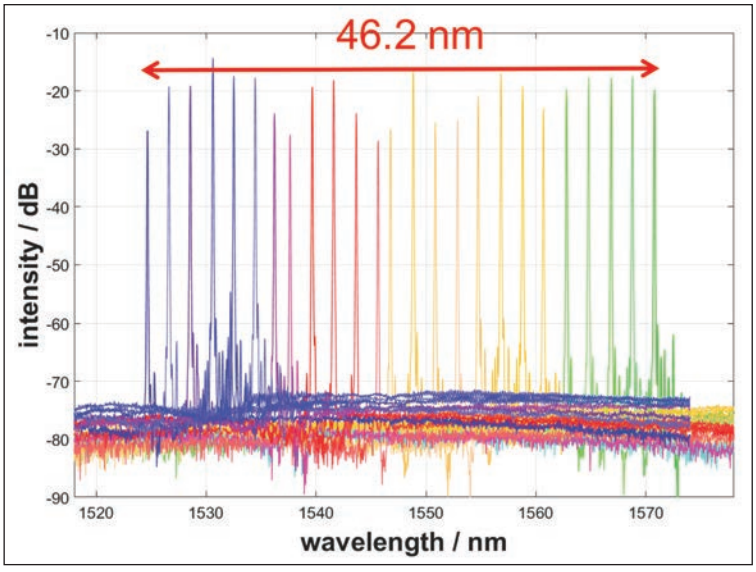

Figure 7. Emission spectra of the laser covers more than the C+ communication band. Each colour shows the operation of one DFB laser out of the four. The wavelength tuning is done by temperature control, either with micro-heaters or the operation current itself.

Given the complexity of this chip, which is still in its infancy, it is not surprising that it suffers from many imperfections, including high losses in the coupling region. However, it demonstrates the potential of our quantum dot material, which can accomplish a reduction in emission linewidth compared to quantum well gain material without being fundamentally restricted in chip design or laser performance.

The upshot of all our success during the last few years is that quantum dot lasers are now competing with quantum well incumbents in many key areas, while exceeding them in others. Our lasers are comparable to quantum well designs in terms of threshold current density, external differential quantum efficiency, modal gain and output power; and thanks to the atom-like gain material, they have the upper hand in temperature stability, dynamical properties, noise and linewidth.

Armed with all these attributes, InP-based quantum dot laser material seems to be the leading candidate for wafer or die bond processing in hybrid integrated silicon-photonics technology, in particular in regard to reliability issues.

The authors we would like to acknowledge the financial support by the European Commission and the German Ministry of Education and Research (BMBF) through the SEQUOIA and SASER projects, respectively, as well as the Israel Science Foundation.

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Turbocharging LiFi with semi-polar lasers

A record-breaking bandwidth makes the violet semi-polar laser well suited for visible light communication

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Indoor and outdoor applications for laser-based visible light communication

A RADIO-FREQUENCY famine looms. Usage of mobile wireless is rocketing, and compromises must be made to meet this demand within the allocated spectrum. Introducing more complex systems are on the agenda, alongside new coding to support a surge in mobile data, but whichever path is taken will be challenging and inefficient.

One way to mitigate the impending RF crisis is to shift to the visible spectrum. This is not a new idea, as visible light communication has been studied since the emergence of blue LEDs with incandescent-level output powers. But recently this technology has been gathering pace, spurred on by the first demonstration of light-fidelity – commonly known as LiFi – in 2011, by Harald Haas' group at the University of Edinburgh, UK.

Although the data rate of LED-based visible light communication is increasing, thanks to advances in both device design and the technology of the communication system, the modulation speed is limited by the relatively slow response of the LED. A typical commercial device requires a chip size of about 1 mm^2 to produce sufficient light for illumination, and this leads to a high capacitance. And that's bad news for LiFi, because a high degree of charge trapping occurs, limiting the bandwidth and ultimately applying the brakes to the switching speed of data transmission.

Trimming the size of the LED increases data transmission speeds. MicroLEDs have a bandwidth that is predominantly limited by the lifetime of carriers, which is of the order of nanoseconds, and their modulation bandwidth can approach 1 GHz. However, while the data transmission rate may be suitable for visible light communication, the output power falls woefully short. Cutting device size is actually something of a double-whammy, with light

output falling through a reduction in chip size, and taking a further hit through a more severe efficiency droop.

A panacea for both these ailments – that is, the low modulation bandwidth and the significant efficiency droop – is a switch to a laser-diode-based lighting system. Efficiency droop is eliminated, because the carrier density clamps above the lasing threshold, while emission is then governed predominantly by photon density – and that means that faster data transmission is possible, because laser diodes can be modulated at far higher speeds than LEDs (see Figure 1). Take this approach, and bandwidth is no longer shackled by carrier lifetime, but instead limited by the photon lifetime of the cavity, which is of the order of picoseconds. What's more, impacts of capacitance and resistance on switching speed are also diminished, because a comparable light output power is possible with a smaller chip.

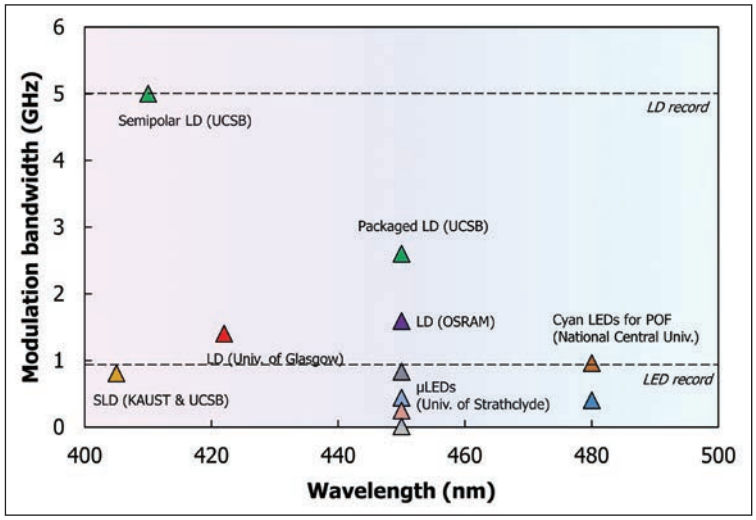

Figure 1. Modulation bandwidths for laser diodes in the blue-violet spectrum are far higher than those for comparable LEDs.

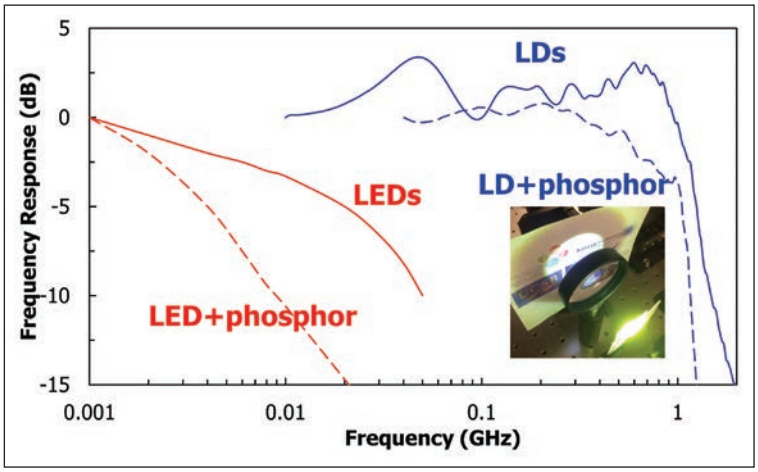

Figure 2. Phosphors are detrimental to the modulation bandwidths of white lighting systems based on LEDs and laser diodes.

Due to these strengths, the laser diode lies at the heart of optical telecommunication systems. Devices based on GaAs and InP have been deployed in vast numbers over many decades, and are now delivering bandwidths of up to around 100 GHz.

Multiple opportunities

One of the biggest opportunities for laser-based LiFi is in homes and offices, where it can simultaneously provide communication links and lighting. But its promise extends beyond this. The multi Gbit/s data rates equip the technology for large-capability broadcasting, vehicle autopilot for smart traffic, and real-time telesurgery. In addition, it could be used outdoors, as it can operate at high powers, thanks to the capability of laser-based white-light sources to generate a luminous flux above 1000 lumens.

Another feature of visible light communication is the creation of a line-of-sight optical network. Light cannot penetrate through walls, so there is a high level of privacy and security associated with this form of free-space data communication. Conventional RF based communication techniques, including Wi-Fi, Bluetooth, and cell phone networks, can't offer this. These networks have a high risk of being hacked, making them undesirable for commercial and military use. With laser-diode based communication, a further attribute is the higher emission power per unit area. The small footprint reduces packaging costs, and there is the promise of incorporating LiFi in mobile devices.

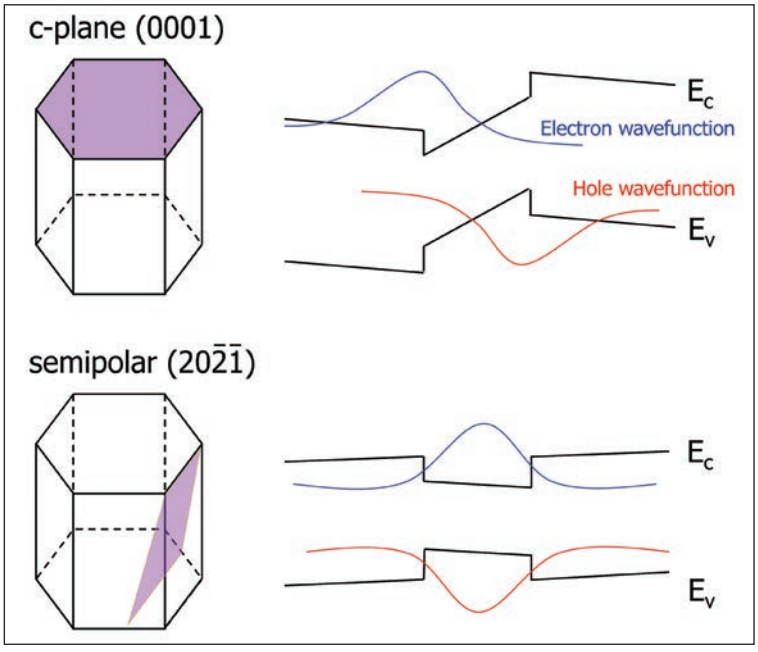

Figure 3. Switching from the polar c-plane to a semi-polar plane improves the wave-function overlap for InGaN/GaN quantum well structures. Results shown for a structure under bias.

Working with the phosphor

If violet or blue LEDs are used to make high power white-light communication systems, they can incorporate phosphor materials to span the longer wavelengths (this is a common approach in LED lighting, where blue LEDs are coated with yellow phosphors). There is a significant downside with this combination, however: the modulation bandwidth is significantly limited by the slow phosphor relaxation lifetime, which is typically less than 100 ns, and it cannot exceed a few megahertz. Rejecting slow phosphor-converted colour components with optical filters overcomes this limitation, but at the expense of increased complexity of the system.

A more elegant approach is a laser-based white-light communication system, because this is not restrained by the phosphor response at high frequency. This would be possible by combining several lasers at different wavelengths to generate a source with a high colour-rendering index. An alternative is to use a blue laser in phosphor-based white-light system and modulate at gigahertz frequencies – this is a vast improvement on the megahertz domain for phosphor-converted signals that would then only constitute the background noise.

At University of California, Santa Barbara (UCSB), our team is developing high-speed III-nitride laser diodes and photonic devices for visible light communication, in collaborating with researchers at the Photonics Laboratory at King Abdullah University of Science and Technology (KAUST) and King Abdulaziz City for Science and Technology (KACST).

To determine what is possible with commercial technology, we have assessed the capabilities of a commercial laser diode. It produces a 2.6 GHz modulation bandwidth with a Gbit/s on-off keying data rate. That's a 100-fold improvement in bandwidth over a commercial LED – and even higher rates are possible by turning to a spectral-efficient modulation scheme, such as orthogonal frequency division multiplexing.

Identifying the best laser

We have compared these modulation rates with those of a class of laser that we have pioneered in our department – an edge-emitter on either a semi-polar or non-polar plane of GaN. These devices differ

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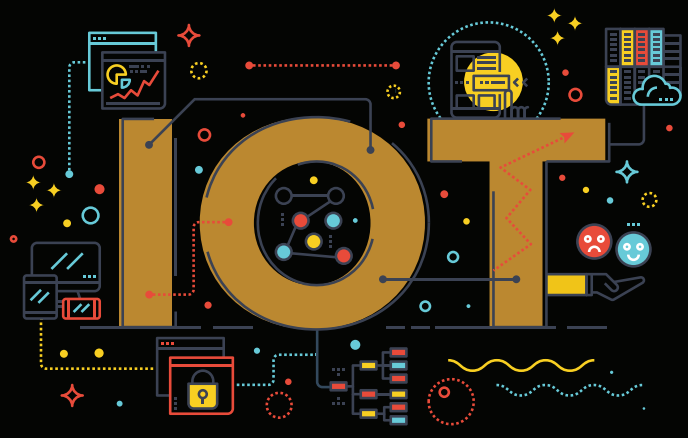

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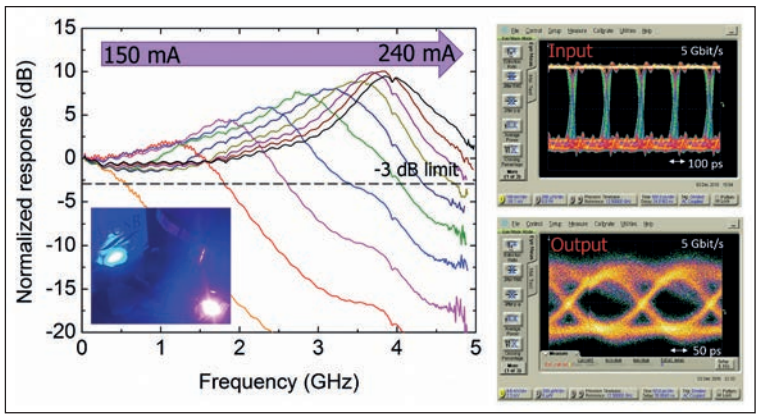

Figure 4. A 5 GHz bandwidth by small signal modulation (left) and 5 Gbit/s of on-off keying large signal modulation (right) for a 410 nm semi-polar laser diode.

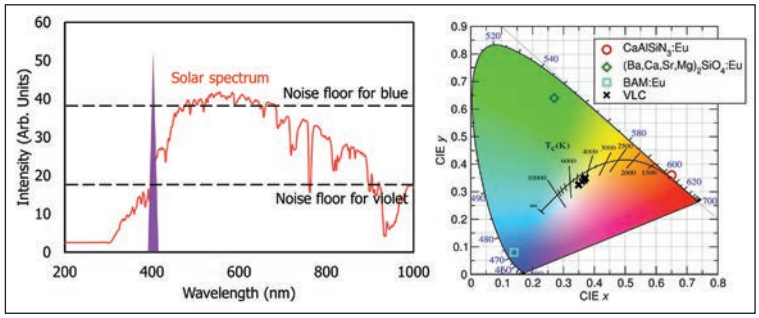

Figure 5. Violet spectrum overlapping with solar spectrum (left) and the CIE plot of white emission by pumping a red-green-blue phosphor with a violet laser diode (right).

from conventional LEDs and lasers diodes, which are grown on the *c*-plane of the Wurtzite crystal structure of GaN and plagued by polarization-induced electric fields in the quantum wells (see Figure 2). These fields cut the overlap of the electron and hole wave-functions, driving down the internal quantum efficiency of conventional devices.

Our lasers have far weaker polarization-induced electric fields, and thus a much higher wave-function overlap. Advantages stemming from this include less droop, a higher output power, a higher optical gain, and a higher differential gain. The latter is hugely beneficial for LiFi, because it should lead to a higher modulation bandwidth.

Putting this theory to the test, we have measured the modulation bandwidth of one of our violet semi-polar laser diodes. It is capable of operating at 5 GHz, setting a new benchmark for all blue-violet lasers and LEDs (see Figures 3 and 4). Using on-off keying, a data rate of 5 Gbit/s is possible, which is the highest value in this spectral range for this transmission technology. Note that the bandwidth of the photodetector in our system limits our measurement, and our devices could reach even higher bandwidths through optimization of the epitaxial structure and device design.

To evaluate the capability of our laser-based visible light communication, we have considered the physical parameters of our semi-polar lasers. Calculations indicate an intrinsic maximum bandwidth of up to 27 GHz, limited by the photon lifetime in the laser cavity, rather than values for device capacitance and resistance. This theoretical limit exceeds that for the LED by more than one order of magnitude.

Selecting a violet laser for the source delivers several benefits, including those associated with data transmission, material growth, and lighting. As sunlight has a lower irradiance in the violet than at longer wavelengths, this laser allows data signals to have a lower background noise level under sunlight (see Figure 5) – and it's a similar story under indoor lights. This means that visible light communication provides a robust form of communication, regardless of whether it is night or day.

Additional strengths of the violet laser include a lower cost than its blue cousin and superior performance, thanks to a lower indium content in the quantum well (typically 10 percent, rather than 20 percent). What's more, the use of a violet laser improves colour quality. If lighting systems are formed using phosphors and lasers, the combination of an ultra-violet source and red-green-blue emitting phosphors deliver a higher colour-rendering index and a warmer colour temperature than the pairing of a blue laser and yellow phosphor. The colour-rendering index can exceed 90, while the correlated colour temperature is less than 3000K.

Our efforts will now focus on developing a higher speed laser through improvement in the epitaxial structure and the device architecture. Also, we will develop InGaN-based photonic passive components, such as a modulator, optical amplifier, and photodetector, as the absence of high-speed photonic components for the blue-violet spectrum would be a bottleneck for visible light communication systems in the near future.

Further reading

C. Lee et al., Opt. Express **23** 29779 (2015)
C. Lee et al., Appl. Phys. Lett. **109** 101104 (2016)
C. Shen et al., Opt. Express **24** 20281 (2016)
C. Shen et al., ACS Photonics **3** 262 (2016)

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Annealing boosts green laser efficiency

Interface defects disappear when a quantum well is capped with GaN and annealed at elevated temperatures

RESEARCHERS in Suzhou, China, have increased the efficiency of green laser diodes by annealing InGaN quantum wells during heterostructure growth.

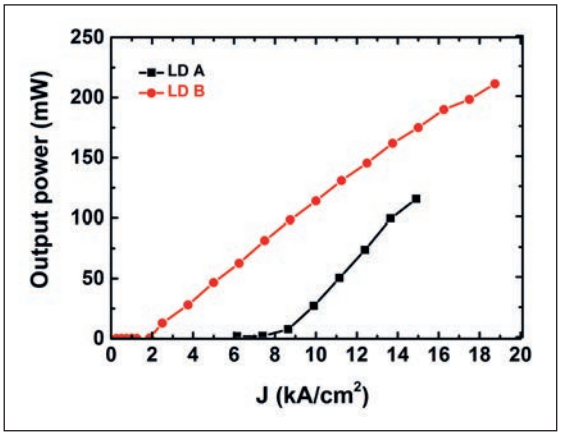
Their approach could help to improve the performance of green lasers emitting beyond 500 nm, which can combine with red and blue cousins to form full-colour projection displays. Today, the efficiency of the green laser lags behing the red and blue, due to weaknesses that include indium segregation and a high density of defects in the indium-rich InGaN quantum wells.

By heating the well shortly after its growth, the Chinese team increased the internal quantum efficiency of its lasers from 39 percent to 59 percent.

Spokesman for the team, Jianping Liu – who is affiliated to both Suzhou Institute of Nano-Tech and Nano-bionics and the Key Laboratory of Nanodevices and Applications – explains that heating is applied to reduce the number of metallic indium clusters that form at the top of the wells, due to indium segregation. "Annealing can remove excess indium adatoms, since they can desorb from the surface," says Liu.

It is possible that he producers of green laser diodes already em ploy an annealing process, says Liu, who points out that it is rare for the growth details of green quantum well lasers to be disclosed.

The efficiency of the quantum wells of green lasers is held back by various imperfections, including dislocations, trench defects and indium clusters. Transmission electron microscopy is an ideal tool for revealing dislocations and trench defects, but it cannot expose indium clusters. "We found that optical measurements are one way to characterize this type of defect," says Liu.



Annealing the laser (LD B) leads to a substantial reduction in the threshold current density and an increase in the output power. Measurements were made using 400 ns pulses and a repetition rate of 10 KHz.

He and his co-workers have obtained photoluminescence spectra at various temperatures on a control device, and another on their annealed sample. In the latter structure, they had deposited a 1.8 nm GaN cap on each of the two quantum wells, with the temperature ramped from 700 °C to 850 °C in 240 seconds, and then maintained at this higher temperature for 30 seconds.

Plotting the position of the photoluminescence peak as a function of temperature produced an S-shaped curve, indicative of potential fluctuations in the quantum wells. This is to be expected – many other groups have reported this phenomenon. Analysis of the team's data revealed that localisation is weaker in the annealed wells. The researchers attribute this to improved interface quality.

Measuring the integrated photoluminescence intensity at various temperatures determined the internal quantum efficiency in both samples, with curve fitting uncovering the energy of non-radiative recombination centres.

Both types of active region have a non-radiative recombination centre with an activation energy of about 50 meV. It is attributed to dislocations. The control has another feature at 10 meV, due to interface defects caused by indium segregation. Ridge-waveguide lasers with a 10 μm ridge and a 800 μm-long cavity were formed from both samples. Cleaving along the *m*-plane produced mirror facets, which were coated with dielectric films.

Annealing caused the laser's threshold current density to plummet from 8.5 kA cm^{-2} to 1.85 kA cm^{-2}, according to measurements with 400 ns pulses with a 10 kHz repetition rate. "The threshold current density is comparable to that of [lasers from] Osram and Nichia," claims Lin.

The output of the annealed laser can exceed 150 mW (see figure). When this device is packaged, it should be capable of room-temperature CW operation, says Lin.

He and his co-workers are now trying to increase the output power of their laser so that it meets the requirements for a laser projector casting a 100-inch image.

Reference

A. Tian *et. al*. Appl. Phys. Express **10** 012701 (2017)

Nano-antenna enhance terahertz sensitivity

Equipping transistors with tiny antenna boosts their terahertz sensitivity

A COLLABORATION between researchers at MIT and the National University of Singapore is claiming to have built the first GaN HEMT detector for terahertz detection that features asymmetric nano-antennae.

The addition of nano-antennae delivers a dramatic hike in sensitivity, with the team's detector producing a detection responsivity of 15 kV/W at 0.14 THz.

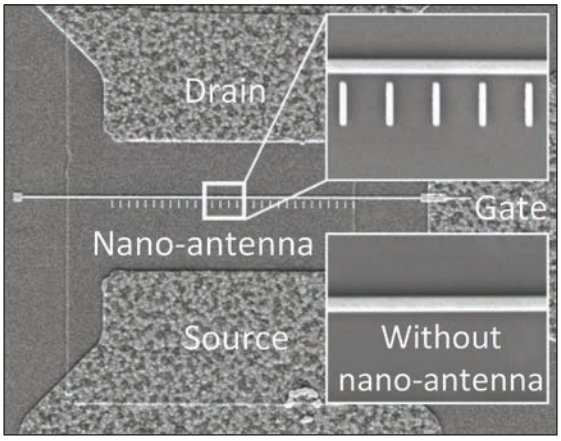
Soon-Jin Chua, who is affiliated to both institutions and is the spokesman for the team, says that their detector is a good candidate for terahertz imaging systems. Other potential applications are in terahertz communication and terahertz spectrometry systems, where they could be used to investigate a wide range of substances, including biomaterials.

Efforts at using GaN HEMTs for terahertz detection date back many years, with success initially held back by inefficient coupling of the radiation into the device. Progress required the routing of energy to just one side of the gate to prevent symmetric signals from cancelling each other out. A breakthrough came in 2012, when a team led by Taiichi Otsuji from Tohuku University, Japan, showed that switching from symmetric to asymmetric antennae increases detector sensitivity by more than two orders of magnitude.

"Based on this concept, we looked for new ideas to further improve the electric field coupling along the gate," says Chua. Success followed: dividing a continuous gate into small pieces, known as nano-antennae, enhanced the electric field of the terahertz radiation.

Simulations, using the software package COMSOL multiphysics, reveal a significant increase in the electric field strength of incident 0.14 THz radiation near the gate edge of a HEMT equipped with 100 nm by 1 μm nano-antennae. In these devices the width of the electrodes is far less than the wavelength of the terahertz radiation, with nano-antennae increasing the localisation of electric fields, due to strong carrier oscillation in the nanoscale materials.

Calculations show that the level of enhancement of the electric field intensity is governed by the gap between the nano-antennae and the gate edge. Shrink this from 200 nm to 50 nm and enhancement increases from two-fold to eight-fold.



Nano-antennae with dimensions of 100 nm by 1 μm increase the sensitivity of a GaN HEMT terahertz detector through improvements in the coupling of the electric field to the device and local enhancements in electric field strength.

To verify the benefits of nano-antennae, Chua and co-workers measured the sensitivity of a range of detectors formed from GaN HEMTs. Using devices with a 250 nm long gate, the team produced a nano-antenna-free control, and a detector with 100 nm by 1 μm nano-antennae separated from the gate by a gap of 200 nm.

Using 0.14 THz radiation produced by a diode operating by impact ionization, measurements revealed that the introduction of a nano-antenna detector increased sensitivity from 8.3 kV/W to 15 kV/W. Due to a lack of optimisation of the gap between gate and nano-antennae, and its width, Chua believes that even higher values of sensitivity are possible. "We used [these values] in this work for ease of fabrication with our facility."

According to Chua, shrinking the space between the nano-antennae and the gate will strengthen the coupling of the electric field, while a thinning of the nano-antennae will enhance the electric field. Further gains could result from different geometries, such as triangular antennae.

Recently, the team has evaluated the capability of its detector at elevated temperatures, and found that it excels in this regard, operating at up to 200 °C. "Normal terahertz detectors, like bolometers, needs 4K operation," explains Chau, "and silicon FETs and Schottky diodes cannot work higher than 100 °C."

Reference

H. Hou *et. al*. Appl. Phys. Express **10** 014101 (2017)

Smoothing non-polar AlGaN films

Alternating injection sources yields flat films of non-polar AlGaN

RESEARCHERS in China have developed a novel MOCVD growth process that slashes the surface roughness of non-polar, *a*-plane AlGaN epilayers. Their technique, which involves alternating the injection of the nitrogen and aluminium precursors, reduced the film's roughness by nearly an order of magnitude.

This work, conducted by researchers at Southeast University and Changshu Institute of Technology, could provide a superior foundation for deep ultraviolet LEDs. Growth on the polar *c*-plane is currently holding back the output power of these devices, which emit at wavelengths less than 300 nm and can be used to provide chemical-free disinfection of water and air.

LEDs that are grown on the *c*-plane are hampered by the quantum-confined Stark effect. Strong internal electric fields pull apart the electrons and holes in the quantum wells, and ultimately reduce emission efficiency.

"Efficiency is also dependent on the well width, the strain, the injection current and the emission wavelength of the device, so it is hard to estimate the QCSE-induced reduction quantitatively" says corresponding author Xiong Zhang from Southeast University. He points out that narrow wells are often used to combat the effects of the quantum-confined Stark effect in polar, ultra-violet LEDs.

Several groups have developed processes for producing non-polar nitride films, but they are used for GaN. Progress with AlGaN is lagging behind, with Zhang and co-workers describing reports on the epitaxial growth of $Al_xGa_{1-x}N$ with an aluminium content of 0.5 or more as "conspicuously lacking".

The team from China has highlighted the capability of its growth process by measuring the surface roughness on three different samples: *a*-plane non-polar AlGaN grown on *r*-plane sapphire with a conventional, continuous flow technique; a normal pulsed-flow approach, which is based on the pulsing of ammonia; and their novel two-way pulsed-flow growth technique.

All three samples were formed by heating *r*-plane sapphire under hydrogen gas to 1060 °C to remove surface contamination, depositing a 20 nm-thick AlN nucleation layer at 600 °C, heating the wafer to 1100 °C, and then growing an 800 nm-thick film of aluminium-rich AlGaN.

The two-way pulsed-flow process involves alternatively turning on and off flows of ammonia and tri-methyl-aluminium for a duration of 6s. During this process, the flow of tri-methyl-gallium is maintained.

"The six second delay time was just our preliminary result, and might be further optimized," admits Zhang.

X-ray diffraction revealed that the sample created by conventional flow has a composition of $Al_{0.6}Ga_{0.4}N$, while the pulsed and two-way pulsed processes produced $Al_{0.66}Ga_{0.34}N$ and $Al_{0.68}Ga_{0.32}N$ films, respectively. Increases in aluminium content are attributed to enhanced aluminium incorporation efficiency.

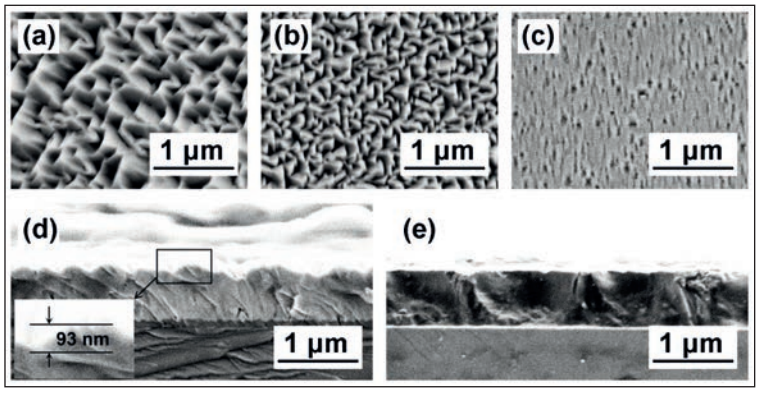
Scanning electron microscopy reveals that when AlGaN is deposited with a conventional flow, it forms a rough surface with deep pyramids along the [0001] direction. These pyramid-shaped defects can be as deep as 93 nm. Pulsing of the ammonia flow leads to coalescence of the large pyramid-shaped defect, but smaller pyramidal defects with a high density still exist on the surface, and there are also new types of defects with varied sizes and irregular shapes. With the two-way pulsed flow, both the large and small pyramid-shaped defects coalesce well to create a film with large defect-free areas.

Zhang and co-workers believe that the two-way pulsed flow produces the best films, because this approach provides more time for the aluminium adatoms to reach their appropriate lattice sites under aluminium-rich growth conditions.

To quantify the degree of surface roughness, the team used atomic force microscopy to study the morphology of all three films. Using scan areas of 10 μm by 10 μm, the root-mean-square surface roughness fell from 15.4 nm for growth with a conventional process to 6.9 nm with ammonia-pulsed flow and 2.0 nm for two-way pulsed flow.

Reference

J. Zhao *et. al*. Appl. Phys. Express **10** 011002 (2017)



Scanning electron microscopy highlights the improvements in film quality associated with a switch from conventional growth processes (a) to pulsing ammonia (b) and alternately pulsing the nitrogen and aluminium sources (c). Cross-sectional images of films (a) and (c) are shown in (d) and (e), respectively.

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