COMPOUND SEMICONDUCTOR

Connecting the Compound Semiconductor Community

Volume 22 Issue 6 August/ September 2016 @compoundsemi www.compoundsemiconductor.net

MACOM

Getting GaN into RF energy markets

AIXTRON

Our technology. Your future.

YOU THINK,

GaN POWER DEVICE MANUFACTURING REQUIRES HVM SOLUTIONS.

WE THINK THAT TOO.

THE NEW AIX G5+ C

DISCOVER THE NEW AIX G5+ C.

Introducing the G5+ C: built on Award Winning Planetary technology for best Single Wafer performance with Batch Reactor benefits – now coming with Cassette to Cassette wafer loading, In-Situ Reactor Cleaning and pre-qualified device processes.
Enabling full automation of your processes and a seamless integration into your Silicon line.

AIXTRON SE · info@aixtron.com · www.aixtron.com

HVM: High Volume Manufacturing

editorialview

by Dr Richard Stevenson, Editor

Droop: Are we missing the point?

FOR MORE THAN A DECADE the GaN LED community has been ensnared in a debate concerning the origin of droop (it is the mysterious malady that leads to reduction in the efficiency of an LED as the current that passes through this device is cranked up).

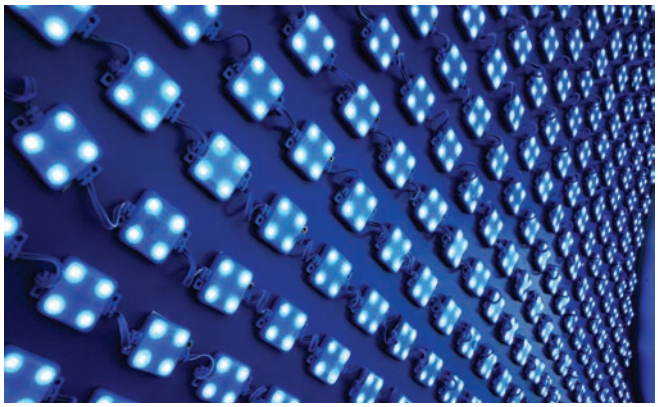
To get to the bottom of the cause of droop – and ultimately find a way to make more efficient LEDs that trim the cost of solid-state lighting – many groups have been running carefully designed experiments on these devices. To eliminate the effects of heating, they often involve pulsed measurements, which are carried out on just the blue-emitting chips that pump phosphors to create white-light sources.

The approach of all these researchers is admirable. After all, the scientific method involves understanding how variations in one measurable influence another, so it is beneficial to eradicate extraneous factors.

But – and it's a big but – if too much is stripped away, the results will overlook some important issues. That's the case with the LED, with measurements on the blue chip failing to consider two significant contributions to droop in white-light sources.

At Philips Lumileds they have measured droop in various phosphors, finding it to be particularly strong in europium-doped red nitrides that are preferred for making sources with a high colour-rendering index (see p26).

While droop cannot be eliminated in the phosphor, it can be minimised. Switching to a ceramic form helps, as does the introduction of LED architectures that reduce the light intensity in the phosphor, by distributing it over a larger area.



It might appear that a better way forward is to avoid using phosphors all together, and instead generate white light by colour mixing red, green and blue LEDs. But even with this approach there are two contributions to droop – the well-known efficiency droop, which is particularly severe in green LEDs; and the lesser-known thermal droop.

At the University of Padova, in Italy, a team has been studying the latter. A survey has shown its prevalence in green LEDs made by all the major manufacturers, with the reduction in efficiency produced by thermal droop always topping 10 percent. Modelling by these researchers has revealed that this form of droop is due to defect-enhanced carrier escape, which increases with temperature (see p52).

So, droop in real light sources is complex, with contributions coming from the chip, the phosphor and the temperature of the light source.

Editor Richard Stevenson richardstevenson@angelbc.com +44 (0)1291 629640
Contributing Editor Rebecca Pool editorial@rebeccapool.com
News Editor Christine Evans-Pughe chrise-p@dircon.co.uk
Publisher Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Senior Sales Executive Robin Halder robin.halder@angelbc.com +44 (0)2476 718979
Sales Manager Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215
USA Representatives Tom Brun Brun Media tbrun@brunmedia.com +001 724 539-2404
Janice Jenkins jjenkins@brunmedia.com +001 724-929-3550
Amy Rogers arogers@brunmedia.com +001 678-714-6775
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214

Circulation Director Jan Smoothy jan.smoothy@angelbc.com +44 (0)1923 690200
Chief Operating Officer Stephen Whitehurst stephen.whitehurst@angelbc.com +44 (0)2476 718970
Directors Bill Dunlop Uprichard – CEO, Stephen Whitehurst – COO, Jan Smoothy – CFO, Jackie Cannon, Scott Adams, Sharon Cowley, Sukhi Bhadal, Jason Holloway.

Published by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK. T: +44 (0)1923 690200 F: +44 (0)1923 690201 E: ask@angelbc.com

Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. T: +44 (0)2476 718 970 F: +44 (0)2476 718 971 E: info@angelbc.com

contents

CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

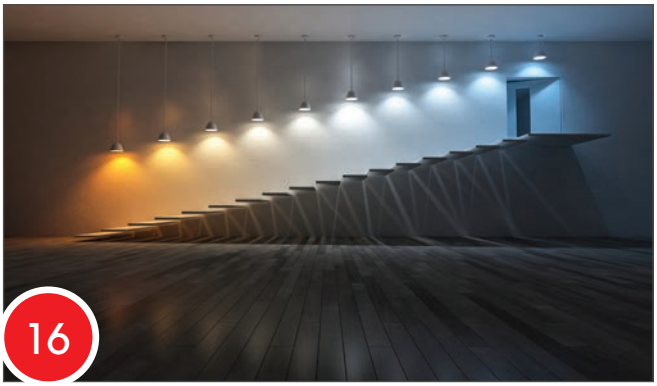
Volume 22 Issue 6 2016

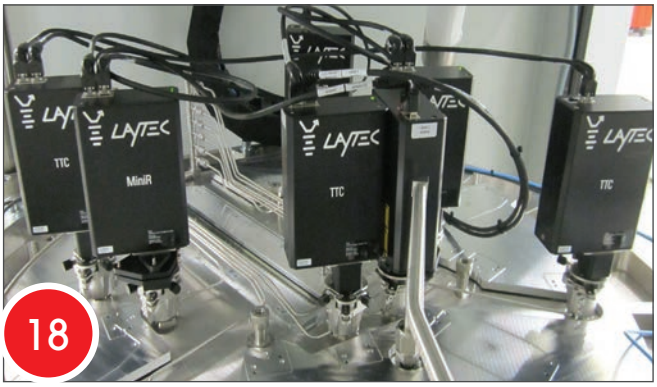
features

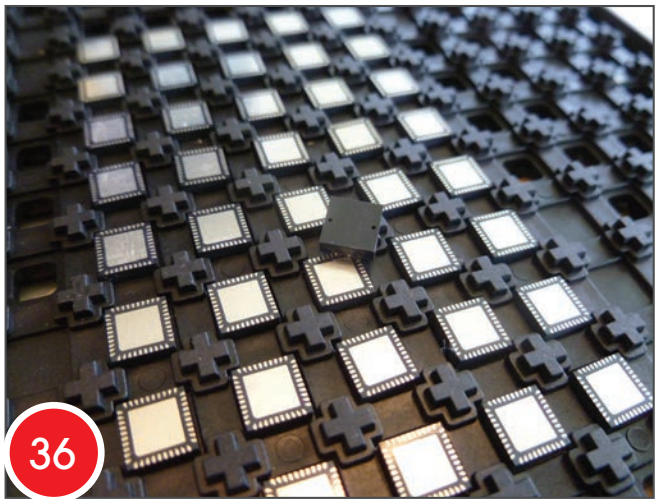
news

news analysis

research review







POET takes next step towards optoelectronic integration

POET TECHNOLOGIES, a developer of opto-electronics fabrication processes, says it has taken a significant step toward its goal of developing a fully integrated commercial opto-electronic technology platform.

The step is the first demonstration of functional HFETs down to 250 nm effective gate lengths on the same proprietary epitaxy and using the same integrated process sequence that was previously used to demonstrate high-performance detectors. This milestone is the latest in POET's initiative to integrate a detector, HFET and laser together into a single chip, the three key components of an active optical cable, a current market target for POET.

"Two of the three critical individual pieces of an integrated opto-electronic product are now in place and undergoing their respective optimization cycles," said Subhash Deshmukh, POET's COO. "As reported earlier, we have encountered delays in completing the VCSEL milestone."

According to Deshmukh, the VCSEL continues to be the focus for POET, while the company simultaneously make progress on other aspects of the technology.

"The characterisation that has been done to date on the VCSEL points to required optimisation of a few layers in a very complex and unique epitaxial stack and fine tuning of the resonant cavity mode," said Deshmukh. The new and optimised epitaxial structure is expected to be delivered to the foundry for processing over the next couple of months."

"We have not uncovered any fundamental show-stoppers,"added Deshmukh. "We are charting new territory here and as pointed out at the recent town hall meeting and at the annual meeting of shareholders, technical issues are commonly encountered throughout the R&D process and we are systematically understanding and addressing these issues."

POET has already demonstrated electrical functionality of the VCSEL with desired thyristor characteristics and demonstrated lasing modes through optical pumping of the VCSEL cavity (in other words light emission was detected on the epitaxial wafer surface).

However, in order to enable electrical pumping of the VCSEL, the team has had to redesign some aspects of the epitaxial stack. VCSEL functionality was previously verified in a lab setting and the functionality of that original laser has been retested and reconfirmed.

POET's current IP portfolio includes more than 34 patents and 9 pending. Core principles of the company's technology have been in development by Chief Scientist Geoff Taylor and his team at the University of Connecticut for more than 20 years, and are claimed to be now nearing readiness for commercialization opportunities.

Skyworks introduces IoT switches

SKYWORKS has introduced two new RF switches for the Internet of Things (IoT) applications including the connected home.

In addition to the connected home, the SKY13587-378LF, which is a pHEMT GaAs SPDT switch, can be used for transmit and receive switching in industrial, lighting and smart energy applications, as well as 802.11a/b/g/n WLAN networks that operate at 2.4 GHz and 5.8 GHz.

The SKY13588-460LF is a CMOS silicon-on-insulator SP3T switch made for antenna selection in Wi-Fi applications in IoT systems.

These switches feature an operating temperature range up to 105 °C, making them ideal for applications that require extended temperature. They also have high isolation and low insertion loss which is best for low-power transmit/receive applications, according to the company. Their positive voltage control provides low current and optimal efficiency for battery-operated IoT applications and their broadband frequency ranges from 20 MHz to 6.0 GHz (SKY13587-378LF) to 0.1 GHz to 6.0 GHz (SKY13588-460LF).

The devices are available in compact MLPD/QFN packages (6-or 12-pin).

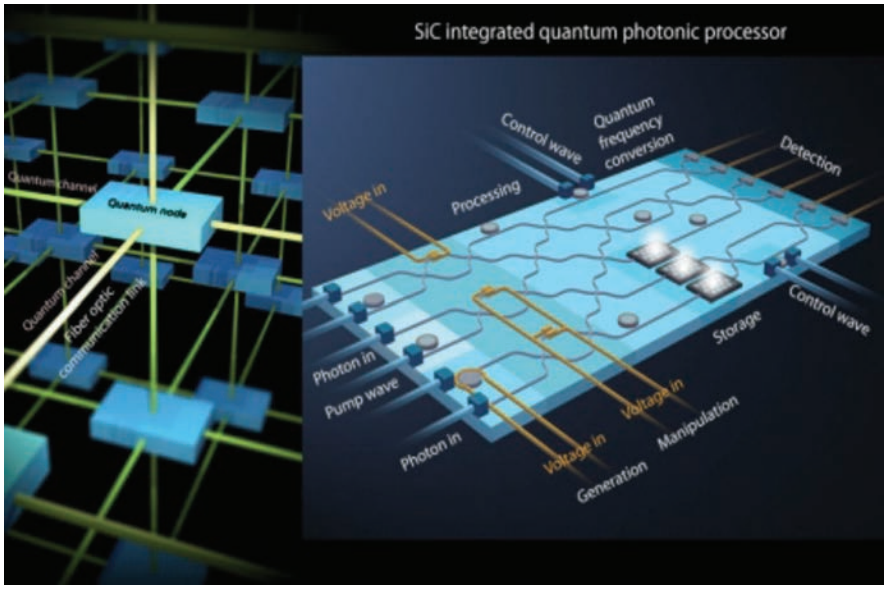
NSF Awards $2 million to build SiC-based quantum photonic processors

UNDER a four-year, $2 million US National Science Foundation grant, Rochester University will lead a photonics system integration research project to reduce the complexity and increase the capacity of quantum information processing for secure communication, metrology, sensing, and advanced computing.

"Our team will build chip-scale integrated SiC quantum photonic processors for high-fidelity and energy-efficient quantum information processing, which interface seamlessly with fibre-optic links for secure communication and distribution of quantum information," said Lin, principal investigator of the project and director of the University's Laboratory for Quantum, Nonlinear and Mechanical Photonics.

"We have a very strong, multidisciplinary, multi-university team of experts for this project, coming together in a shared vision," said Lin.

Co-principal investigators are John Howell, professor of physics and optics, David Awschalom of the University of Chicago, Case Western Reserve University's Philip Feng, and MIT's Jurgen Michel – all experts in chip-scale integrated SiC quantum photonic processors. Members of the National Institute of Standards and Technology, Thomas Gerrits, Sae Woo Nam, and Richard Mirin, are also collaborating on this project.



Artist's conception of a quantum node lattice with a detailed inset of the SiC integrated photonic processor within one of the quantum nodes

The research is expected to result in a new class of device technologies with previously inaccessible attributes and merits that may eventually have profound commercial impact on the industrial sectors. SiC combines excellent linear optical, nonlinear optical, point defect, electrical, mechanical, and thermal characteristics into a single material with mature wafer processing and device fabrication capability, thus representing a promising material system for integrated quantum photonics.

Research such as this also feeds into the work of the AIM Photonics (American Institute for Manufacturing Photonics) consortium of the US Department of Defense, of which the University of Rochester is a partner.

Infineon and Wolfspeed - who next?

INFINEON TECHNOLOGIES' recent acquisition of Wolfspeed for $850 million has caused a stir in the compound semiconductor industry.

With very recent mergers of International Rectifier and Infineon Technologies, Fairchild Semiconductor and ON Semiconductor, Wolfspeed and APEI, the power industry is evolving fast. So who will be next?

"At Yole, we see this acquisition as the beginning of a series of impressive collaborations within the SiC power business in the coming years," says Pierric Gueguen, business unit manager at the market research company Yole Développement." And this industry trend is likely to continue and to further increase in the future."

This latest acquisition comes in a power electronics industry where SiC technology benefits are well-known and where business opportunities have been clearly identified by industrial companies. Both Wolfspeed and Infineon Technologies are market leaders and this pact reinforces their dominant market position, according to Yole. The deal also includes the related SiC wafer substrate business for power electronics and RF power electronics.

According Hong Lin, analyst at Yole Développement, Infineon Technologies

market share should increase more than 50 percent if the full acquisition is confirmed.

"Wolfspeed and Infineon Technologies are leaders in the SiC power devices industry. The combination of both players will clearly strengthen the leading position of Infineon Technologies in the SiC power business," explains Lin, Technology and Market Analyst at Yole. "This is a win-win acquisition."

Lin argues that Infineon and Wolfspeed are both established SiC diode players, with the latter having developed a powerful SiC MOSFET solution that is clearly more advanced than that from Infineon. Wolfspeed's Gen 3 has already been commercially available for two years, and it has a good reputation. From its side, Infineon Technologies just released its MOSFET component in May 2016. Within a SiC MOSFET market that is just taking off, Infineon's acquisition of Wolfspeed ensures its development in this market segment.

In parallel, as number one in the incumbent silicon power business, Infineon Technologies has a well-established client portfolio. The German company has a strong understanding of the market's needs, its players, and the technical specifications related to power electronics applications.

The company also has significant experience in power packaging for semiconductors, which is considered the main SiC business bottleneck for power electronics today. Last year, Cree's division, Wolfspeed, acquired APEI to reinforce their packaging capability. Today, with the support from Infineon Technologies, Wolfspeed can further accelerate their product development and reaffirm the leadership of its technology approach.

Finally, Infineon's investment and large-scale production capability could support Wolfspeed in ramping up production and expansion.

This acquisition includes more than just Wolfspeed's SiC devices for power electronics applications. It also includes the company's activities focused on GaN on SiC for RF applications.

HexaTech demos high-performance ultraviolet LEDs

HEXATECH has demonstrated its first generation UVSure UV-C LED, based on the company's proprietary AlN substrate material.

The 263 nm wavelength device achieves 6 mW in a 0.15 mm^2 active area die. When scaled to its second generation larger footprint, the die is expected to produce approximately 24 mW, which is twice the radiant flux of competitive products. Further, when driven in pulse mode to 300 mA, the same 0.15 mm^2 active area die is able to reach 19 mW, or approximately 76 mW in the large die format.

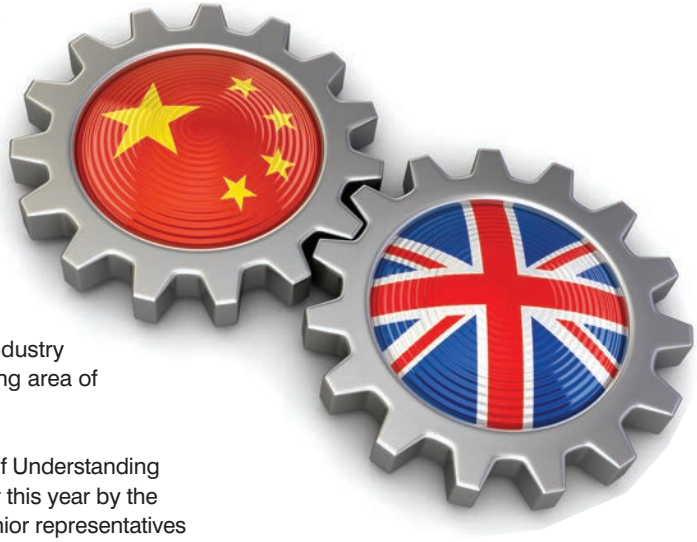
"This demonstration is a milestone in our business, and is the direct result of intense device R&D coupled with the use of our exclusive high-quality AlN substrate material," stated HexaTech CEO John Goehrke.

He added, "This capability allows us to engage the UV-C LED market at the right moment, linking together incredibly strong interest with cutting-edge performance. It also clearly demonstrates our continued assertion that the best substrate material yields the best device performance, and this first generation result is just the beginning."

"We are truly excited to be in a position to support the rapidly expanding UV-C LED customer interest seen over the last several years," remarked Gregory Mills, HexaTech's director of business development. "With point-of-use sterilization applications alone representing a $400 milion plus opportunity in the coming years, we anticipate significant corporate expansion and strategic customer engagement," he noted.

Joseph Smart, director of LED development commented: "HexaTech's world-leading, high-quality bulk AlN substrates are the essential foundation for attaining these results, enabling near perfect epitaxial growth quality throughout the active region of the device, essential to produce both high internal quantum efficiency and long component lifetimes. This is something that competing sapphire substrate technology simply cannot sustain at these wavelengths."

University of Glasgow joins forces with China to promote optoelectronics



THE UNIVERSITY OF GLASGOW has signed a partnership agreement with a Chinese state-owned enterprise company to develop an international optoelectronics industry base in the Lingang area of Shanghai.

A Memorandum of Understanding was signed earlier this year by the University and senior representatives of the Shanghai Lingang Science and Technology Innovation City Economic Development Co. Ltd – a subsidiary of the Lingang Group which specialises in industrial park development – and the Shanghai Shunmao Information Technology Co., a private company established to manage and commercialise some of the technology which will be developed by this exciting new initiative.

John Marsh, professor of optoelectronic systems and dean of the University of Glasgow-University of Electronic Science and Technology of China Partnership, attended an inaugural event at Lingang representing the University of Glasgow.

The agreement has led to the establishment of the Shanghai Lingang International Photonic Integrated Circuit Joint Laboratory (PIC Lab) which will foster collaboration between the University of Glasgow and its partners in Lingang.

PIC Lab aims to accelerate the development and commercialisation of optoelectronic integrated chip technology, integrating multiple optical components on a single chip and packaging the chips with high-speed electronics, to address the demand for high-speed network connections for the next generation of the Internet. Marsh said: "The University of Glasgow is delighted to be working with our new partners to strengthen international links relating to optoelectronic devices and the development and integration of an optoelectronic integration platform and industry incubation base in Lingang.

We shall also be working to create a Scottish platform. This is international recognition of Glasgow's long term commitment to optical research."

A spokesman for the Shanghai Lingang Science and Technology Innovation City Economic Development Company said the new PIC Lab would capitalise on the combination of domestic and foreign skills and resources to develop "an effective concentration of high-end technical and commercial talent in the field of photonics to deliver a world-leading, cutting-edge technology and industrial capital".

The partnership would also give clear leadership to the global PIC industry and offer a strong impetus to optoelectronic integrated chip technology research and development and attract further domestic and foreign optoelectronic talent technology, added the spokesman.

The Chinese partners plan to visit the University of Glasgow later this year to promote and cement the project.

Mobile phone LED market to decline between 2015 and 2021

ACCORDING to the latest information from IHS Markit Mobile Phones in *Packaged LED Market Brief*, the market for LEDs used in mobile phones – including backlighting behind the display, keypad illumination, and camera flash – will decline at a compound annual growth rate (CAGR) of 2.6 percent from 2015 to 2021. Increased penetration of organic LED (OLED) is a primary reason for this decline.

The OLED panel penetration rate for mobile phone displays is forecast to grow from 13 percent in 2015 to 34 percent in 2021, due to strong demand from Chinese brands. LED revenue for backlighting in mobile phones was estimated at $686 million in 2015, but will decline to $455 million in 2021.

Nearly all mobile phones shipped in 2015 had at least one camera – and 86 percent also had a secondary camera – although not every camera was equipped with a flash. IHS expects the mobile phone flash LED market to decline slightly in 2016, due to fewer mobile phone shipments.

However, the market will begin to grow again from 2017 to 2020, thanks to increased penetration of colour LEDs and secondary camera flash applications. LEDs used in mobile phone keypads will also decline, but they comprise only a very small part of the market.

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry.

7th CS International Conference

SPEAKERS ANNOUNCED!

CS International 2017 will provide timely, comprehensive coverage of every important sector within the compound semiconductor industry.

The 7th CS International conference will be held at the Sheraton Brussels Airport Hotel, in Belgium on Tuesday 7 & Wednesday 8th March 2017.

CS International will build on the success of its predecessors, including the leaders of the world's biggest chipmakers and the most promising start-ups providing 30 presentations spanning 5 key themes.
Together, these talks will detail breakthroughs in device technology; offer insights into the current status and the evolution of compound semiconductor devices; and provide details of advances in tools and processes that will help to drive up fab yields and throughputs. Attendees at this two-day conference will gain an up-to-date overview of the status of the CS industry, and have many opportunities to meet many other key players within this community.

Early bird discount
Book your place before 30.11.2016 and receive a €100 discount.

FIVE KEY THEMES LIE AT THE HEART OF CS INTERNATIONAL 2017

Five key themes:
- Refining handset architectures for the 2020's
- Perfecting Power Electronics
- Optimising Light Emitters
- Revolutionising RF Chips
- Exploiting Heterogenous Integration

Within each topic there is a key-note presentation from one of the most influential companies within this sector; one talk by a leading market analyst who will discuss trends within the industry and presentations by the leaders of firms developing cutting-edge technology in this field.

Book your place NOW !

www.cs-international.net/register to secure your place

PLATINUM SPONSORS

EPIGAN evatec process systems FerroTec

GOLD SPONSORS

CS CLEAN SYSTEMS IQE

DELEGATE BAG SPONSOR

qorvo all around you

PORTFOLIO SPONSOR

Plasma-Therm A LEADING SUPPLIER OF PLASMA PROCESS EQUIPMENT

EXHIBITION SPONSOR

Panasonic

SUPPORTED BY

EPIC European Photonics Industry Consortium

This two day event covers five themes

Refining Handset Architectures for the 2020's

Will handsets be crammed with ever more III-V content? And could GaN appear in the front-end in the coming years?

KEYNOTE

- **Stephen Kovacic: Skyworks Solutions**
  Taking the front-end into the 2020's

ANALYST

- **Eric Higham: Strategy Analytics**
  The foundry of the 2020's

SPEAKERS

- **Bert Schmitz: Qorvo**
  TBC
- **David Danzilio: WIN Semiconductors**
  Meeting customer demands in the 2020s

Perfecting Power Electronics

Can the best devices stem from the ultra-wide bandgap of gallium oxide? Or will they emerge from foundries processing GaN and SiC on silicon?

KEYNOTE

- **Toshimi Hitora: FLOSFIA**
  Unleashing the potential of gallium oxide

SPEAKERS

- **Tamara Baksht: VisIC Technologies**
  Making the best GaN transistors for power electronics
- **Frédéric Dupont: Exagan**
  Driving the GaN Power Device roadmap for large scale adoption
- **Isik Kizilyalli: US. Department of the Energy Advanced Research Project Agency**
  Vertical GaN devices for better power supplies
- **Sujit Banerjee: Monolith Semiconductor**
  Slashing chip costs with SiC-on-silicon
- **Anthony Sagneri: FINsix Corporation**
  Wide bandgap devices: the key to the world's smallest laptop charger
- **EpiGaN**
  TBC

Optimising Light Emitters

Sponsored by JSC Technology Park Pulsar

Are colossal LED fabs revolutionising chip manufacture? And what are the big opportunities for visible lasers?

KEYNOTE

- **Hsu Chen K: Sanan Optoelectronics**
  Creating the biggest and best LED chipmaker in China

ANALYST

- **Swapna Prakash**
  Lighting-up India with LEDs

SPEAKERS

- **Oleg Shchekin: Philips Lumileds Lighting Co**
  Non-linear processes in LEDs and engineering for efficiency at high power densities
- **Martin Behringer: OSRAM Opto Semiconductors**
  LED - more than just a light emitting cube
- **Tatsushi Hamaguchi: Sony Corporation**
  Fulfilling the promise of the GaN VCSEL

Revolutionising RF Chips

Will GaN RF deliver the best bang per buck by increases transistor voltages, or making these devices on silicon? And what are the best options for really high frequencies?

KEYNOTE

- **John Palmour: Wolfspeed**
  GaN-on-SiC RF: Poised for Rapid Adoption

ANALYST

- **Speaker:** Yole Développement

SPEAKERS

- **Zach Griffith: Teledyne**
  InP HBTs for high-power 70 to 500 GHz amplification: its status today and where it is going
- **Rocco Giofrè: University of Rome Tor Vergata**
  GaN Doherty amplifiers for backhaul radio links
- **Michael Ziehl: MACOM**
  The virtues of GaN-on-silicon
- **Bernd Heinz: Evatec**
  TBC

Exploiting Heterogenous Integration

What are the fruits of a marriage between silicon and the III-Vs? And can higher mobility materials improve microprocessors and memory?

KEYNOTE

- **Daniel Green: Defense Advanced Research Projects Agency – US Agency of Defence**
  Advancing technology with heterogeneous integration
- **Soon-Fatt Yoon: Nanyang Technological University**
  Heterogeneous integration of III-V devices on Silicon with ultra-thin buffer utilising interfacial misfit dislocations

SPEAKERS

- **Jesus A Del Alamo: MIT**
  Refining the III-V finFET
- **Nadine Collaert: imec**
  Looking for the ultimate low-power switch: the promise of tunnel FETs
- **Jean Fompeyrine: IBM**
  Advancing SRAM by adding III-Vs (COMPOSE project)
- **Shengkai Wang: Institute of Microelectronics of Chinese Academy of Sciences**
  III-Vs and germanium for future logic
- **Arnaud Furnemont: imec**
  3D NAND scaling: an opportunity for alternative channel material

Consumer-grade LED bulbs used for Comms Links

RESEARCHERS at Disney Research and ETH Zurich have demonstrated that consumer-grade LED bulbs can, with some modifications, do double duty both illuminating a room and providing a communications link for devices in that room.

This visible light communication (VLC) system would be suitable for connecting the many devices, such as appliances, wearable devices, sensors, toys and utilities, that could comprise the Internet of Things, or IoT, said Stefan Schmid, a researcher at Disney Research and ETH Zurich.

By having individual LEDs alternate between sending modulated light signals and serving as receivers of signals, it is possible to create a network of bulbs that can send messages to each other and connect to devices, while having no discernible effect on room lighting. Schmid and his colleagues shared details of the system they designed, called EnLighting, at the IEEE International Conference on Sensing, Communication and Networking (SECON) 2016 in London.

"Interconnecting appliances, sensors and a wide variety of devices into the Internet of Things has many potential benefits, but using radio links to do so threatens to make the radio spectrum an even scarcer resource," said Markus Gross, vice president at Disney Research. "Visible light communication networks conserve the radio spectrum, while also making it difficult to eavesdrop for anyone out of line of sight of the network."

"LED light bulbs mounted on the ceiling or in free-standing floor lamps easily cover a room, serving as illumination while at the same time creating a room-area network that allows data exchange between light-emitting devices," he said. Even if the bulb is not needed for lighting and is switched off, it can still serve as a receiver of signals from those devices, he added.

"We used commercially available, off-the-shelf LED light bulbs as our starting point," Schmid said. "They are readily available at low cost and can be used in any lamp with standard sockets. This leads to an easy-to-setup and flexible testbed that can be readily duplicated."

The bulbs were modified, however. A System-on-a-Chip, or SoC, running an embedded version of Linux was added to each bulb, as well as photodiodes to enhance sensing of incoming signals and an additional power supply for the added electronics.

The researchers deployed four such bulbs for their proof-of-concept system. They showed that their system architecture and protocols enabled the bulbs to create stable networks that could support the low bandwidth applications typical of most IoT devices.

They also showed it was possible to use the system to estimate the position of devices in the room, an example of the additional applications that the system could support.

Cree expands into new high bay applications

CREE has introduced the HXB Series LED High Bay Luminaire, said to be the first of its kind to operate in extreme ambient temperatures spanning -40 °C to +65 °C and delivering 70,000 lumens at up to 140 lm/W.

The luminaire can be mounted at heights of 30 feet and higher, and comes with optical options including flood and aisle distributions. The HXB High Bay Series brings Cree technology to new applications such as cold-storage spaces with sub-zero temperatures and high-heat climates like warehouses and airplane hangars.

«Cree continues to provide better light experiences by delivering on the true potential of LED technology,» said David Elien, Cree senior vice president, lighting. "The HXB Series redefines the high-bay category with extraordinary rated lifetimes and industry-leading lumens per watt even in extreme operating temperatures that are found in distribution centres, gymnasiums and field house applications."

The HXB Series withstands freezing cold and severe heat, all at less than half the weight and double the warranty of competing LED high-bay fixtures. It is engineered for performance today and for 100,000 hours of use, with a virtually maintenance-free design, zero restrike time and lightweight construction, says Cree.

An aluminium bonded zipper fin heat sink provides thermal management for long lifetime and exceptional efficacy in extreme operating temperatures. With less material than cast aluminum heat sinks, the HXB Series is said to be half the weight of competing luminaires, for easier installation.

The series is available with 35,000 lm and 70,000 lm output options of exceptional illumination performance, offering one-for-one replacement of 500 W and 1000W HID luminaires at colour temps of 3500K, 4000K or 5000K at up to and beyond 80 CRI.

Imec sets up Florida branch

IMEC, the Belgian research centre, will be opening Imec Florida, a new entity focusing on photonics and high-speed electronics IC design based in Osceola, Florida.

Imec Florida kicked off with the signing of a collaboration agreement with the University of Central Florida (UCF), Osceola County and the International Consortium for Advanced Manufacturing Research (ICAMR), that is setting up fab facilities for the development and production of innovative III-V-on-silicon solutions for a broad range of applications including sensors, high-speed electronics and photonics.

Imec Florida will be established as a design centre facilitating the collaboration between Imec's headquarters, based in Leuven, Belgium, and US-based semiconductor and system companies, universities, and research institutes. Imec Florida's initial focus will be the R&D of high speed electronics and photonics solutions, starting with an offering of IC design research for a broad set of semiconductor-based solutions such as THz and LIDAR sensors, imagers, and a broad range of sensors. It will also provide IC design needs that will be driving the ICAMR manufacturing research.

Through Imec Florida, Imec's design, prototyping and low-volume production service – also named Imec IC-link – will provide the US market low-cost access to advanced foundry services, helping entrepreneurs to (industry and academia) design innovative products and get them to market.

Funding for Imec Florida will come from Osceola County, and the University of Central Florida. The aim is for the new centre to attract top talent through future strategic partnerships, with the aim to employ about ten scientists and engineers by the end of the year and increase to 100 researchers in the next five years. Heading up the facility as general manager will be Imec's VP Bert Gyselinckx who previously served as general manager at Imec in Eindhoven, the Netherlands and helped to co-invent many technologies deployed by innovative semiconductor and consumer electronics companies.

"As the US semiconductor market continues to strengthen with semiconductor manufacturing, equipment, materials and system innovation, we are extremely pleased to collaborate with partner organisations in Florida and see Osceola County in the Orlando region as an interesting location to drive the next phase of Imec's growth and innovation," stated Luc Van den hove, president and CEO of Imec. "Together with industrial and academic partners, we want to develop sustainable solutions and technology to accelerate innovation and stimulate economic growth within Osceola County and the State of Florida."

"Imec's international prestige gives us the opportunity to leverage its standing in a field that is growing exponentially in order

to recruit more partners and funding for our work at the new Design Centre and the Florida Advanced Manufacturing Research Centre," said Osceola County Commission Chairwoman Viviana Janer.

"The relationships and people that Imec brings to our operation are tangible ways that Osceola County's 5-year, $15 million investment will be more than re-paid. It's important to realise that the new Design Centre is going to capture the attention of everyone in this field, thereby ensuring maximum utilisation and value of the FAMRC."

"The Imec Design Center is the funnel that will fill ICAMR with high-value manufacturing opportunities and we will work closely with them to make sure our capabilities tightly align with their technology direction, said ICAMR CEO Chester Kennedy.

"This partnership is poised to shine the global high-tech spotlight on Central Florida."

ASCATRON:

HEFTY FUNDS FOR HIGH VOLTAGE DIODES

Following a €4 million investment, SiC power device developer Ascatron intends to deliver very high voltage diodes to market in a year. Chief executive, Christian Vieider, reveals plans to Rebecca Pool.

EARLIER THIS SUMMER, Sweden-based SiC power semiconductor developer Ascatron revealed that it had raised a hefty €4 million in financing from investors in Italy and China, as well as reactor supplier, LPE, Italy.

Now intending to complete development of its initial SiC devices – the first of which will be a high voltage SiC diode – the company will split funds between materials production and product development.

As Ascatron chief technology officer, Adolf Schöner, said at the time: "Forty percent of the market for power electronic components is in China and we see a lot of interest in SiC for energy saving."

"We've already started to implement our advanced material technology in production equipment for SiC epitaxy," he adds. "The next step is to optimise device design and outsource the remaining manufacture of the chip to a foundry with capacity for volume production."

Burying issues

From the late 1990s, researchers at Swedish research institute, Acreo, had been developing SiC epitaxy, spinning out Ascatron in 2011. During this time, Acreo had offered SiC epitaxy as a service, providing multi-layer structures and re-growth on non-planar surfaces.

At the same time, development of SiC device concepts, including a normally-off SiC JFET rated to 1.2 kV and 50 A, was well underway. And collaborations with HOYA, Japan, had led to a 3C-SiC process for power MOSFETs.

Fast-forward to today and progress has clearly continued. Ascatron has developed many processes for manufacturing SiC semiconductors for power electronics, including substrate buffers, SiC epitaxy, deep trench etching and more.

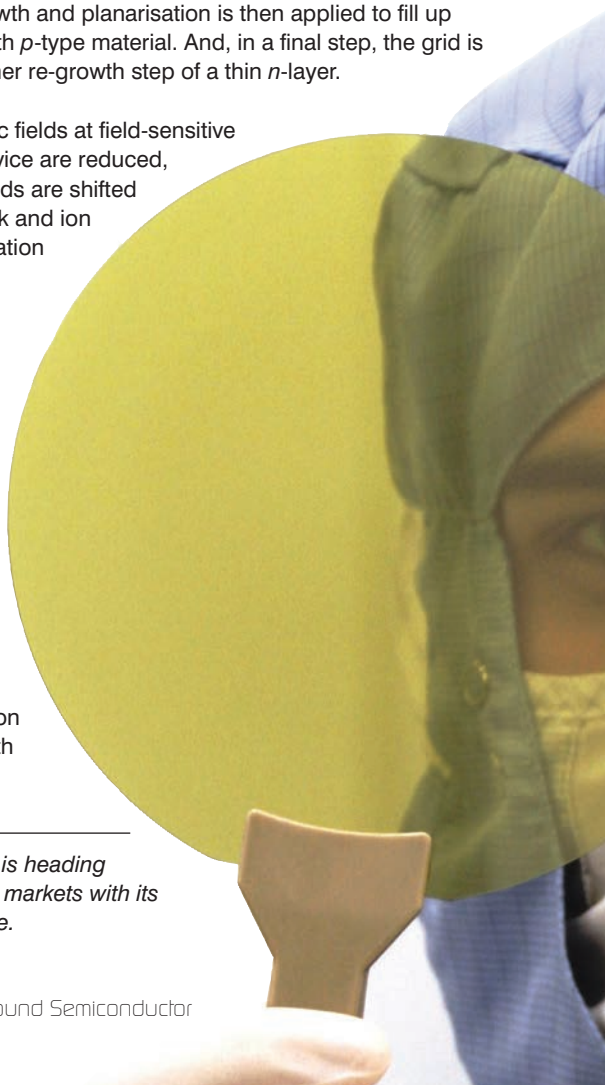
At the heart of these breakthroughs lies so-called 3D-SiC technology, based on embedded epitaxial growth methods that replace the conventional process of doping with ion implantation during SiC device fabrication. When fabricating SiC devices, doping via ion implantation can bring problems. Ion diffusion is slow, preventing healing of defects, and inhibiting current density and high-voltage performance. And in a separate issue, electric fields at Schottky contacts and MOS interfaces also stymy device performance.

To side-step these issues, Ascatron epitaxially grows doped material within etched 3D structures, such as trenches, producing high-performance, high-voltage SiC devices. For example, when fabricating a Schottky diode, a *p*-type grid is first fabricated on the substrate surface, via trench etching.

Epitaxial re-growth and planarisation is then applied to fill up the trenches with *p*-type material. And, in a final step, the grid is buried by another re-growth step of a thin *n*-layer.

Crucially electric fields at field-sensitive areas of the device are reduced, high electric fields are shifted into the SiC bulk and ion doping implantation damage simply doesn't exist.

As Ascatron's managing director, Christian Vieider says: "We've been working on this technology to make very efficient doping structures which replace ion implantation with epitaxy."



Right: Ascatron is heading for high-voltage markets with its epitaxy expertise.

"Losses are much lower in our devices and we can design [structures] to handle very high voltages in an efficient way," he adds.

So with the process honed and cash in hand, Ascatron is currently working with pilot customers and intends to deliver its first device – a high-voltage, buried-grid SiC Schottky diode for industrial process markets – in a year.

"We're targeting high-voltage applications – 10 kV devices – for industrial processing as we see some specific needs that we think we can fulfill," says Vieider. "We've identified that IGBT [modules] are available up to 6.5 kV, but above this there are no real switching power devices, so we think this is a good place to start our product range."

But how exactly will Ascatron compete with the likes of Infineon, Cree, ST Microelectronics and Rohm? Vieider reckons his company's technology can provide advantages at the higher voltages that competitors' devices haven't yet reached.

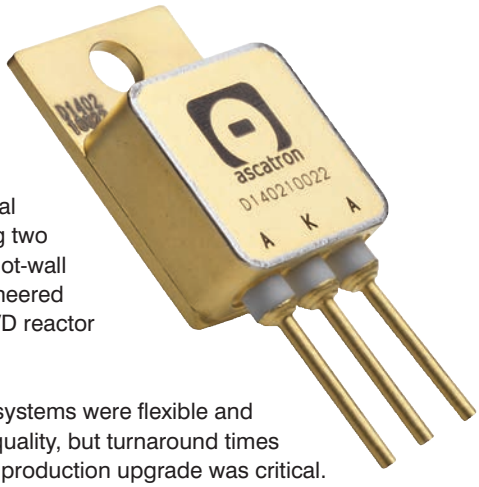
"We already have a customer that is looking for high-voltage devices, but just can't find a device," he adds. "Silicon devices can be coupled together in series perhaps, but right now there is really nothing on the market, so this is where we are starting."

And with higher-voltage devices in place, the company will then look to broadening applications to lower voltages. Indeed, Ascatron recently bought shares in Italy-based start-up, PileGrowth Technology, to develop MOSFETs based on cubic SiC grown on silicon.

The move could open up markets for 300 V to 600 V applications and also allow Ascatron to compete with rival technologies, including GaN-on-silicon.

"We had a choice and could have targeted lower voltages from the beginning, but there are already competitors in this market," says Vieider. "So once our technology has been adopted at the higher voltages, then we will move to lower voltage applications."

To kick-start its journey to commercial devices, the company recently bought a single-wafer, 6-inch production reactor system, manufactured by investor LPE. Past development has centred around several reactor systems, including two prototype 4-inch Aixtron hot-wall CVD reactors, initially pioneered by Sweden-based SiC CVD reactor supplier, Epigress.



According to Vieider, the systems were flexible and produced good material quality, but turnaround times weren't fast enough, so a production upgrade was critical. "We're now ready to scale up our fabrication processes for production," he says. "Our latest reactor has load lock, a good turnaround time and very short cooling times".

"We need to do very thick epitaxy – from 0.1 micron to 100 micron – and have an epitaxy process for advanced grid doping," he adds. "This system produces [structures] with good doping, uniformity and performance."

Past company plans had included the purchase of a multi-wafer reactor system, but Vieider reckons his team will get better material quality with a single-wafer system.

"In principle you can buy three single-wafer reactors for one multi-wafer reactor," he explains. "So, as our needs arise we can add more reactors to production."

The company currently buys in substrates from commercial suppliers, and going forward, will keep fundamental epitaxy processes in-house while outsourcing remaining production to a commercial foundry.

"In two years we will have a product on the market and will target more and more applications from higher to lower voltages, addressing broader and broader markets," says Vieider. "Beyond this, our target is to be a supplier of SiC power devices for broad applications."

INFINEON WITH WOLFSPEED: THE FUTURE

What does a stronger Infineon mean for power and RF markets, asks Rebecca pool.

IN A MOVE to raise resources and become a more focused LED lighting company, Cree has sold its power and RF arm, Wolfspeed, to Infineon for $850 million in cash.

In the words of Cree chief executive, Chuck Swoboda: "This [decision] unlocks value, increases management focus and supports our mission to build a more valuable LED lighting technology company." But for Infineon, the move could mean so much more.

While the Germany-based semiconductor vendor is already the power market leader, acquiring Wolfspeed's SiC-based product portfolio, strengthens its dominance even further.

For years, the company has focused on high performance SiC JFETs, only delivering its first SiC MOSFET earlier this year following customer demand. But acquiring Wolfspeed provides instant access to MOSFET production that can be introduced to company fabs around the world.

As Richard Eden, senior analyst of power semiconductors at IHS Technology, highlights: "It's taken Infineon a few years to realise that end users are more comfortable with MOSFETs, but this acquisition speeds up the introduction of Infineon SiC MOSFETs."

"The SiC MOSFET market has been dominated by Cree/Wolfspeed and Rohm, so Rohm will be feeling the pressure by now," he adds. Meanwhile, the acquisition also strengthens Infineon's RF power presence. The company already has a strong silicon-LDMOS offering and is developing GaN-on-silicon products. But now it also has access to Wolfspeed's GaN-on-SiC products.

Each technology is critical to next-generation cellular communications, from high-end LTE and 4.5G to 5G, but GaN-on-SiC will now allow Infineon to deliver products for 80 GHz frequency, 5G applications of 2020 and beyond.

Indeed, Infineon chief executive, Reinhard Ploss, has said that Wolfspeed will help his company's target of leading the entire RF market. However, the latest deal will also extend Infineon's reach into high growth sectors, including IoT infrastructure, renewable generation and electric vehicles.

"For example, electric vehicle and charging station development is massive

in China with DC-to-DC conversion of battery charging and plug-in station markets moving rapidly," highlights Eden. "This is a big growth sector for SiC due to its efficiency benefits over silicon, and Infineon would now like to use Wolfspeed products to build the strength and position of its sales network across China."

But MOSFETs and RF markets aside, the latest deal provides one final, over-riding advantage; Infineon now owns Cree's SiC wafer substrate business for power and RF applications.

Wolfspeed had been a leading market supplier of wafers on which to manufacture SiC devices. But as Eden points out: "Infineon is now vertically integrated and can offer everything in house. It can make the wafers, process the wafers in its own fabs, and make the modules from the devices that have been formed on its wafers."

Infineon's Ploss has stated that Wolfspeed will continue to supply wafers to third parties in, say, mobile network base station markets. But in-house wafer production will likely lead to Infineon's device prices falling.

"This applies to MOSFETs but Infineon's existing range of diodes could also probably become cheaper as the company will get wafers at cost rather than sourcing them from a commercial third party supplier," says Eden.

Cost aside, Infineon's vertical integration could also have ramifications on power and RF markets around the world. According to Eden, silicon vendors have developed SiC and GaN power devices to defend market positions, while companies such as GaN Systems, Cree, EPC and Transphorm have delivered devices to disrupt the silicon supply chain.

"By buying Wolfspeed, Infineon is firmly positioning itself for the future," says Eden. "It's not just defending sales, its looking forward to expanding GaN and SiC sales; to try and push the market ahead like this is a very forward view."

So, with the acquisition scheduled for completion by the end of this financial year, what next?

For power markets, better quality devices could be on the cards. Eden's sources tell him that SiC MOSFETs from General Electric are more reliable and can switch at higher currents than offerings from Wolfspeed and Rohm. "Infineon will know what to do to enhance these MOSFETs from the Wolfspeed acquisition," he says.

Below: Reinhard Ploss, CEO of Infineon Technologies, and Chuck Swoboda, Cree Chairman and CEO (right).

And eventually, industry can expect Wolfspeed to be fully integrated to Infineon. The company acquired International Rectifier in early 2015, and has since maintained the company's established brand. But for the shorter-lived Wolfspeed, integration is expected to be cheaper and easier. Ploss has been reluctant to provide detail on the acquisition process, but has publicly stated the company is aiming for complete integration in the long-term.

"I hadn't seen this acquisition coming, but when you think about it, it's not surprising," concludes Eden. "Infineon has the money, it's now removed the competition from the market and it's strengthened its product range, so why not?"

METROLOGY:

MAKING THE MOST OF MARKET GROWTH

As III-V markets gather momentum, LayTec is chasing the opportunities, reports Rebecca Pool.

IN LATE JUNE Berlin-based instrumentation supplier, LayTec, announced its first order for its *in-situ* metrology tool, EpiTT/VCSEL.

Designed for VCSEL applications, the tool measures wafer temperature and growth rate of epitaxy layers during MOCVD, but also monitors the spectral reflectance of the evolving distributed Bragg reflectors and cavity structures. As chief technology officer, Kolja Haberland, highlights: "We look at the spectroscopic position of the stop-band and see if there is any mis-matching between the cavity and Bragg reflectors."

"Mirrors, for example, have to reflect at the same wavelength and even with a mismatch of only a couple of nanometres, device performance will suffer," he adds. "We are trying to bring new tools into the market that serve customer needs, and we see great growth potential in the VCSEL market."

The company's first *in-situ* product, so-called EpiRAS, monitored epitaxial growth of cubic semiconductors. Primarily a research tool, the system is still used by many academic organisations to provide data on wafer temperature, growth rate, composition, doping levels and more. But while it has infiltrated myriad research organisations, the leap to industry didn't quite happen.

"This is a very valuable tool and measures so many parameters on the wafer surface, but it has been just too complex," says Haberland. "Also it only works with cubic materials, such as arsenides and phosphides, so for example, we can't access the nitride market with this tool."

Given this, the last few years have been a hive of activity for LayTec, with the company developing tools, largely for use with Aixtron reactors, to take advantange of growing III-V markets.

For example, EpiTT described as the 'workhorse of mass production', has predominantly targeted industry production of GaAs and InP laser diodes, edge-emitting lasers and VCSELs. The tool measures temperature and reflectance at three wavelengths and can be supplemented with 'EpiCurve' to detect wafer bow.

Meanwhile, the company, also keen to glean business from GaN LED and laser diode markets, developed 'Pyro400' to measure surface temperature during the epitaxial growth of GaN on sapphire or SiC.

As Haberland highlights, such tools have proven crucial to manufacturers in these markets as well as developers of InP and GaAs RF devices, but in October 2015, LayTec upped its game by introducing a new generation of these tools. Described as being more customisable, crucially, the latest 'Gen3' tools can be used beyond Aixtron reactors.

"These standalone products fit into virtually any brand of MOCVD system," says Haberland. "So we're not just talking about the Aixtron R6 and Aixtron Planetary, these can also be used with the Veeco K 700 and Taiyo Nippon Sanso UR 25K, in smaller research systems or retrofits from, say, SMI and Agnitron, as well as in a variety of plasma-based etching and deposition systems."

The move follows the integration of LayTec's OEM metrology tools to Aixtron's systems just over a year ago. Then, in June this year, Aixtron qualified LayTec's Gen 3 software so users can also access the latest metrology tools on its MOCVD platform.

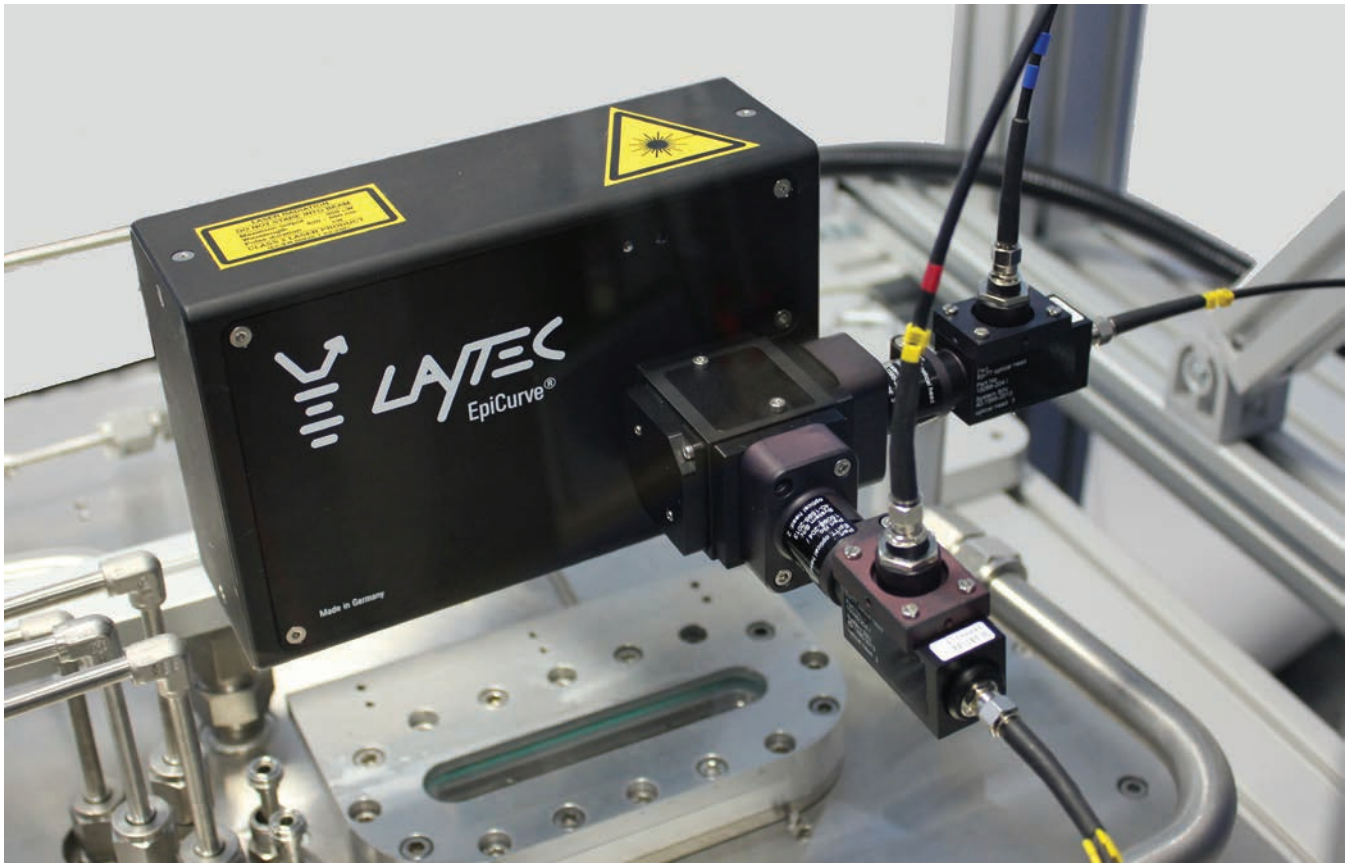
But be it integrated or standalone, the growing demand for *in-situ* metrology is all good news for LayTec, and as Haberland says: "These developments are bringing us deeper into more markets."

Market developments

Clearly, LayTec is intent on capturing business as III-V markets grow. The recent delivery of the VCSEL-specific metrology tool follows customer demand to monitor progress of VCSEL growth during the many hours of deposition of the III-V materials.

As Haberland says: "If *in-situ* data indicates that growth isn't on track, the user can implement a control loop to bring growth back on track and optimise yield and throughput."

And as VCSEL markets grow, LayTec has



As III-V markets grow, LayTec is delivering more *in-situ* metrology tools

also spotted a second market to focus efforts on; the UV-LED market.

"Again we see good growth here," says Haberland. "UV-LEDs are grown on different materials, AlN, AlN buffers or AlGaN buffers with a high aluminium content, so straightforward temperature measurement will not work. We are bringing a specialised version of the tool, as we did with the EpiTT VCSEL, for UV-LEDs to the market."

Looking to the future, LayTec is expecting growing demand from Taiwan and China as, for example, LED manufacturers turn to the latest generation of Pyro400 to monitor epitaxial growth. Global LED players have already adopted the tool but according to Haberland: "[Asia-based manufacturers] are catching up and will integrate these tools to their control loops to bring more value to mass production."

The company also recently revealed that epiwafer manufacturer, IQE, has equipped its fab with LayTec Gen3 metrology systems for MOCVD process monitoring. The move is just one of several partnerships that LayTec has forged with foundries, which Haberland sees as all being crucial to the company's future.

"These foundries run on many tools and have a huge variety of growth processes for different customers, products wafer sizes and materials," he says. "Calibration is so important here, so *in-situ* metrology makes sense."

Still, for LayTec, there is much more beyond MOCVD. "Our market studies look at the number of MOCVD tools sold in different markets and there is a lot of growth predicted for UV LEDs, GaN-on-silicon power devices, with GaAs and InP markets remaining steady," says Haberland.

"But we see ourselves also reaching broader markets, and these will include plasma-enhanced CVD, ALD and MBE of lots of materials from pure silicon and SiGe to III-V-on-silicon and CMOS integration." he adds.

GaN gets set for mainstream adoption into RF energy markets

Products made from GaAs and LDMOS will be superseded by GaN variants that will penetrate new markets such as heating systems for microwave ovens, power sources for plasma lighting and automotive ignition

BY MARK MURPHY FROM MACOM

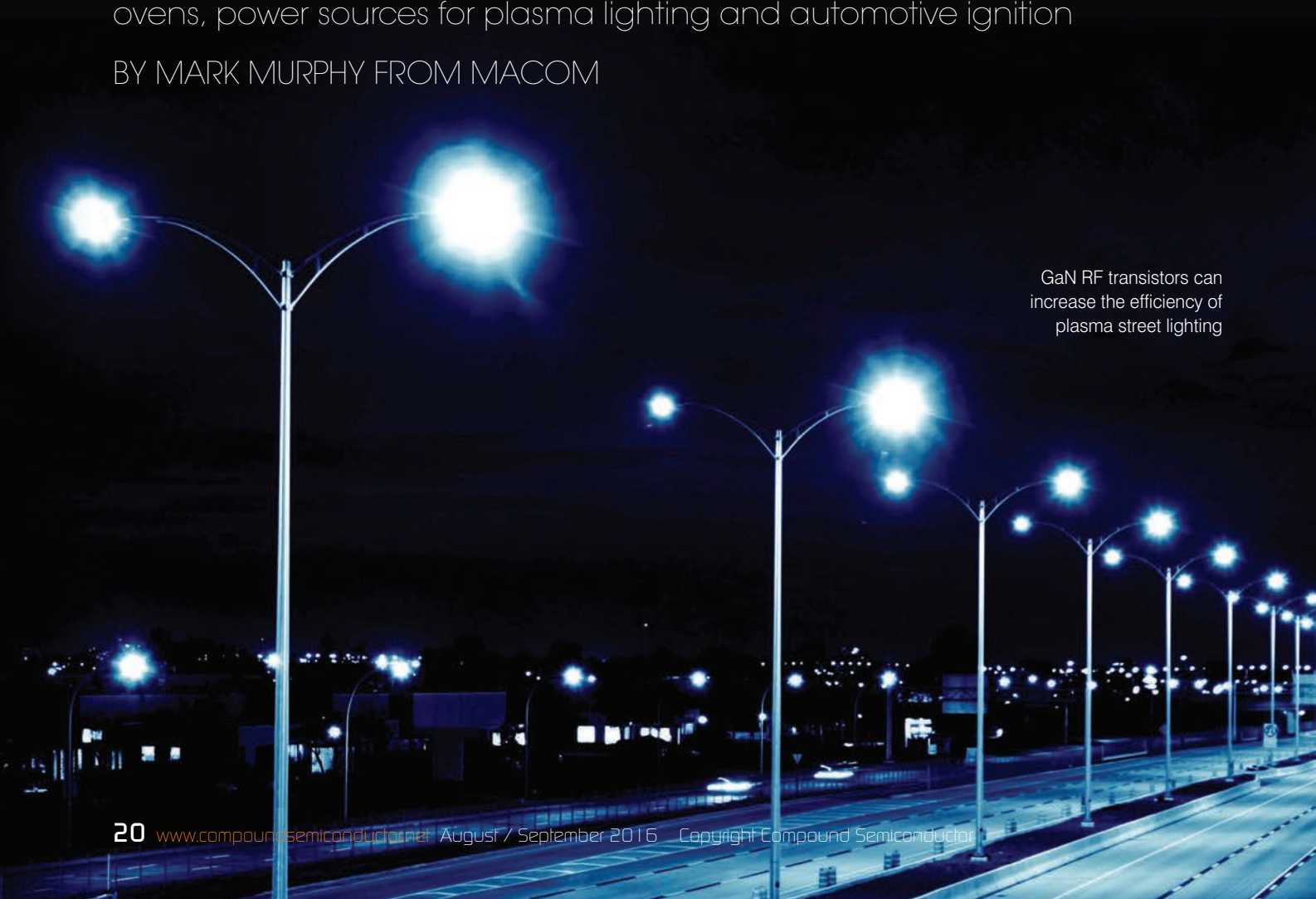
A NARROW SUBSET of semiconductor technologies has always serviced the RF and microwave domain. This approach allows the most appropriate technology to meet the unique requirements of a host of complex applications, ranging from consumer wireless handsets to military radar infrastructure.

As with any technology, different candidates must be assessed in terms of performance, reliability and cost. Do this, and it is clear that there is an absence of a one-size-fits-all solution for adequately addressing the needs of every RF application. Instead, a spectrum of semiconductor solutions has evolved for meeting specific technology challenges while fulfilling cost requirements.

Two of the most established technologies for serving many commercial applications are GaAs and silicon LDMOS. But they are now under threat from a new challenger, GaN, that is poised to deliver a ground-breaking transformation. Products based on this wide bandgap semiconductor are now commercially available from several companies, including ourselves – MACOM of Lowell, MA.

To fully appreciate this wide bandgap technology, and its supply chain dynamics that are propelling its industrial uptake, it is helpful to consider the evolution of GaAs from an esoteric technology to high-volume market mainstay – a trajectory that parallels what we are seeing with GaN.

And in addition, it is worthwhile to consider the role that LDMOS has played in the evolving RF market.



GaN RF transistors can increase the efficiency of plasma street lighting

Back in the 1990s, GaAs was in a formative stage, similar to where GaN has been positioned in recent times. It was an emerging technology, underpinned by strong government funding and targeting applications that could pay a premium for high performance.

This state of affairs turned on its head with an explosion in demand for wireless handsets. GaAs had found its 'killer application', and economies of scale were soon at play. Compound semiconductor companies drove the industry towards establishing robust, reliable and scalable GaAs supply chains, through investment of hundreds of millions of dollars in large-scale GaAs fabs. Thanks to this, GaAs chip manufacture shifted from boutique production to high-volume production in just a few years.

Now, GaAs is under threat from silicon-based technologies such as CMOS and SOI, which are both gaining market share in handsets. Several leading silicon industry vendors have announced initiatives to supplant most GaAs production, leveraging economies of scale that dwarf even the largest GaAs factories.

Like GaAs, LDMOS has undergone incremental growth and multi-decade longevity in the RF market, particularly in wireless infrastructure. Thanks to the maturity of the LDMOS supply chain and attendant manufacturing efficiencies, costs have been kept relatively low.

Up until very recently, the performance of GaAs and LDMOS products – evaluated in terms of power, efficiency, bandwidth and thermal stability – have been sufficient for their target applications. But both technologies have their flaws. GaAs is limited to a power output below 50 W, while LDMOS is incapable of operating above 3 GHz.

GaN compares extremely favourably to both incumbents, combining high output powers with a very wide frequency range. It also offers several other attractive attributes, but despite all its virtues, it has been held back by high prices. Devices can be as much as ten times more expensive than products based on GaAs or LDMOS.

GaN at the tipping point

Today, the performance advantages of GaN are well known to everyone involved in the RF and microwave industry. This wide bandgap semiconductor delivers a raw power density that is considerably higher than that of GaAs and LDMOS, and devices can be scaled to high frequency. Armed with these attributes, device designers can realise broad bandwidths while maintaining high efficiency.

Our team at MACOM has been developing and commercialising GaN technologies and devices for several years. Our latest technology, fourth generation GaN-on-silicon (Gen4 GaN), can be used to manufacture products that combine a peak efficiency in excess of 70 percent with a gain of 19 dB, for modulated 2.7 GHz signals. This level of efficiency exceeds that of LDMOS by more than 10 percentage points, and if properly exploited, it can have a tremendous impact at the system level in military, commercial and industrial applications.

The high power densities and great efficiencies of GaN make it a great source for RF basestation transmitters.

Historically, the sticking point for GaN has been its high price. But this should change, given the very high power densities and scalability to 8-inch substrates. With our Gen4 GaN, we are planning to produce GaN-based devices in volume production levels that undercut the cost per watt of comparable LDMOS products, and are significantly less than that of GaN-on-SiC variants, which are far more expensive. Working with partners, we are leaders of 6-inch silicon wafer production, and we intend to move to 8-inch production in 2017. The growing capacities, allied to lower cost structures, should break barriers to widespread GaN adoption in mainstream commercial markets.

Delivering GaN performance at a cost that's far closer to that of silicon will drive innovation within the RF domain and ultimately open massive market opportunities. Chief among them will be RF energy applications. Here, controlled electromagnetic radiation will heat items and drive all kinds of processes. Today, magnetron tubes tend to generate this energy, but they are set to be displaced by an all solid-state RF semiconductor chain.

There are several compelling reasons behind a switch to solid-state RF energy. They include a low-voltage drive, semiconductor-type reliability, a smaller form factor, and an 'all-solid-state electronics' footprint. But perhaps the greatest attributes are fast frequency, phase and power-agility, and hyper-precision. Taken

Benefits of switching the RF source in a microwave oven from a magnetron to a GaN RF unit include a longer system life, a constant output power and zone controllable heating.

together, these strengths result in an unprecedented process control range, even energy distribution, and fast adaption to changing load conditions.

Microwaves and lighting

One common consumer product that will be transformed by the arrival of Gen4 GaN is the microwave oven. Prototype magnetron replacements have already been produced using LDMOS technology, but they fall significantly short of the minimum performance level. Our GaN devices bridge that gap, providing an additional 10 percent efficiency. HEMTs can deliver 70 percent efficiency at 2.45 GHz, and do so at a cost that is competitive with a tube-based legacy technology that launched in the 1940s and has undergone manufacturing optimization over many decades. The strengths of GaN ensure a longer system life, constant output power and zone-controllable heating.

Another sector that will be transformed by the arrival of affordable, high-performance GaN products is plasma lighting. It is slowly making inroads in the overall lighting market, with the greatest success coming in grow lighting applications. Here it makes an ideal lighting source, thanks to a colour-rendering index that provides a very close match to that of natural sunlight.

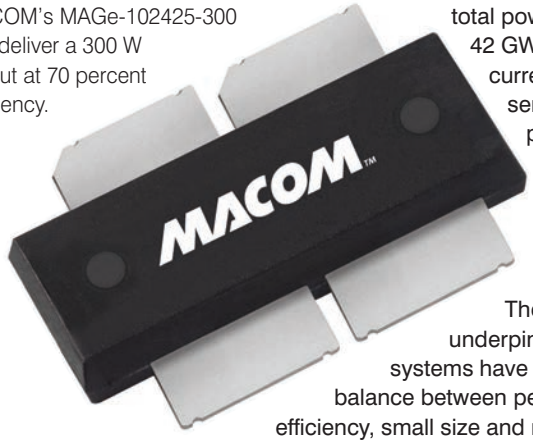
Today, LDMOS technology is widely used to provide RF power excitation at frequencies of hundreds of megahertz. However, developments are underway to increase the frequencies of RF excitation towards 6 GHz. This must be accompanied by efficiencies in excess of 70 percent – requirements that are very tough to meet with LDMOS technology, but a given for GaN. Turning to this wide bandgap technology also enables a trimming of transistor dimensions. This helps the vendors of plasma lighting produce competitive products that will battle with LED lighting for the indoor light bulb replacement market.

Further opportunities for GaN exist in automotive ignition, heating and drying, and industrial, scientific and medical markets. In all these, the strengths of GaN make it a highly compelling alternative to LDMOS. In conventional vehicles, RF-based ignition systems are poised to replace spark plug technology. Channelling RF energy into a vehicle's combustion chamber provides a more even ignition distribution, and in turn produces a considerable boost in fuel efficiency and a cut in carbon dioxide emissions. When it comes to heating and drying, using RF energy enables uniform heating and drying of materials. Undesirable temperature gradients resulting from conventional approaches are then avoided – these can be particularly severe in materials with poor heat transfer characteristics. Benefits that follow include accelerated production processes for manufacturing applications, improved medical procedures and processes that involve blood and/or organ warming, and enhanced chemical processing techniques in scientific applications.

Massive markets

The total addressable market for RF energy applications is enormous. Just consider the microwave oven market, where annual sales exceed 70 million units, each of which requires a transmit power ranging from 0.6-1.5 kW. That equates to a

“Today, LDMOS technology is widely used to provide RF power excitation at frequencies of hundreds of megahertz. However, developments are underway to increase the frequencies of RF excitation towards 6 GHz. This must be accompanied by efficiencies in excess of 70 percent – requirements that are very tough to meet with LDMOS technology, but a given for GaN”



MACOM's MAGe-102425-300 can deliver a 300 W output at 70 percent efficiency.

total power demand of 42 GW to 105 GW. At current mainstream semiconductor price structures, that is a market opportunity of $10 billion to $25 billion.

The RF devices underpinning these systems have to strike an optimal balance between performance, power efficiency, small size and reliability – and they must do this at a price point that promotes mainstream commercial adoption. Championing the full potential of GaN for RF energy is a non-profit technical association, the RF Energy Alliance. It anticipates that the market can take off with the introduction of 300 W power amplifier modules that combine 70 percent efficiency with a price of just 4 cents per watt.

We are addressing this challenge with our recently released MAGe-102425-300. This is a rugged 300 W, GaN-on-silicon power transistor housed in a cost-effective plastic package optimized for use in commercial-scale solid-state RF energy applications. Incorporating Gen4 GaN technology, our MAGe-102425-300 delivers a performance that defies the inherent power efficiency and density limitations of LDMOS, while retailing at an equivalent price profile at scaled volume production levels. The MAGe-102425-300, which provides a 300 W output power at 2.45GHz, at an efficiency of 70 percent, leads the industry in meeting the core technical requirements for next-generation power amplifiers proposed by the RF Energy Alliance.

As a member of the Alliance, we are committed to advancing the organization's charter to standardize solid-state RF energy technology and its associated components and sub-module roadmaps – an effort that will reduce complexity, cost, and the development time associated with bringing related products to market. The mainstream adoption of solid-state RF energy hinges in part on the cooperation and collaboration of Alliance member companies and the industry at large.

Advances in the technology of GaN and its supply chain have taken us to a position where we can deliver breakthroughs in manufacturing scale and cost structures. This will spur the mass market adoption of this technology. Its great performance at a competitive price will open up many new markets, ranging from heaters for microwave ovens and large-scale drying to new units for automotive ignition systems and horticultural lighting. There is no doubt that GaN-on-silicon RF transistors have a bright future ahead of them.

your

EPITAXIAL GROWTH

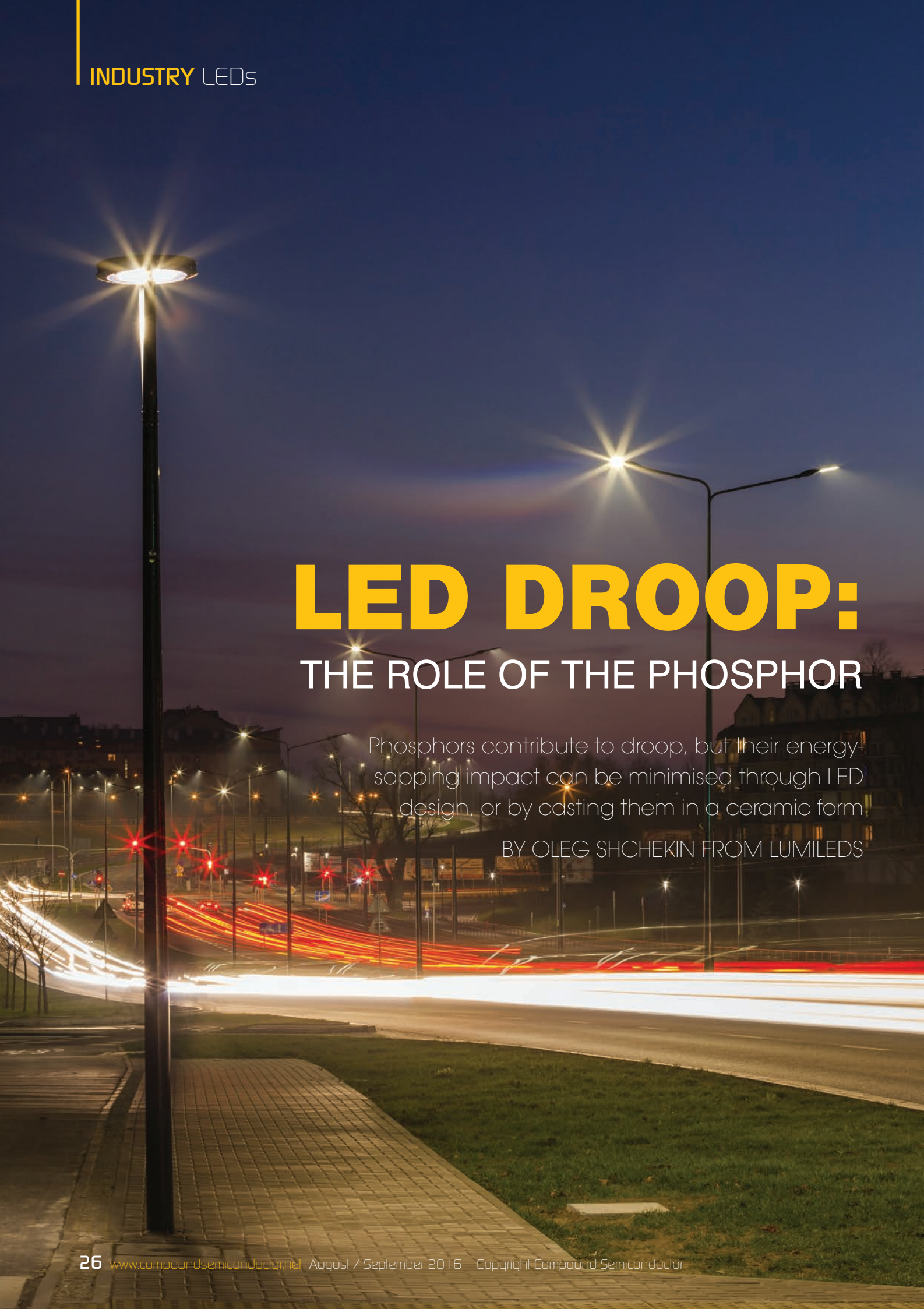
partner

Enabling advanced technologies

- World leading technology
- Complete materials range
- MOCVD, MBE, CVD
- Advanced semiconductor wafer products
- Advanced R&D capabilities
- Multiple, manufacturing sites (Europe, Asia, USA)

IQE

www.iqep.com



LED DROOP:

THE ROLE OF THE PHOSPHOR

Phosphors contribute to droop, but their energy-sapping impact can be minimised through LED design, or by casting them in a ceramic form.

BY OLEG SHCHEKIN FROM LUMILEDS

DURING THE LAST DECADE, there has been a widespread, on-going debate over the origin of droop. Attempts to uncover the cause of droop have focused on the blue-emitting chip, which overlooks one of the key processes in the solid-state light bulb. As white light is produced by mixing the blue emission from the chip with that generated by an optically pumped phosphor, it is crucial to consider whether the phosphor is also prone to droop.

One way to illustrate that droop in white LEDs can be appreciably higher than that produced by the blue pump LED alone is to compare the normalized external quantum efficiency of a warm-white, 1mm^2 thin-film-flip-chip LED and its constituent blue pump LED at a range of drive currents (see Figure 1). Pulsed driving conditions distinguish between the impact of drive current density and thermal effects, and reveal that droop is significantly more severe in a white LED than a blue-emitting chip.

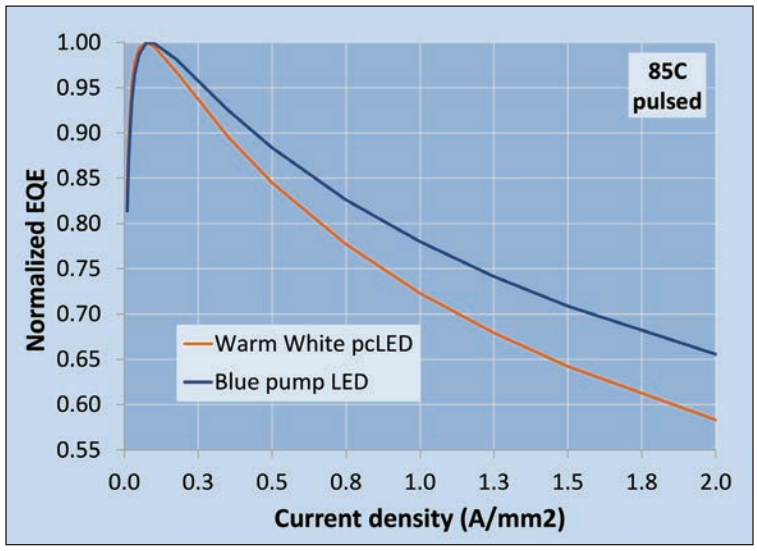


Figure 1. Efficiency droop is more severe in white LEDs than it is in blue-emitting chips.

These measurements have led our team at Lumileds to scrutinise Europium-doped red nitride phosphors, which are commonly used in state-of-the-art LEDs to provide emission at longer wavelengths. This investigation involved measurements of quantum conversion efficiency for the LED phosphor at different temperatures and different intensities of blue light irradiance. To distinguish between the influence of temperature and irradiance, we employed pulsed excitation. Laser pulses were long enough to account for phosphor luminescence rise and fall times, and heating was avoided with a 1 kHz duty cycle.

Our study has not been limited to the europium-doped nitride red phosphors, and includes the commonly used cerium-doped aluminium garnets. Both phosphors suffer from droop, but this is more pronounced in the europium-doped nitride reds – here phosphor photo-quenching is severe enough to contribute between 20 percent and 25 percent of the droop in warm-white LEDs. Compounding matters, the phosphor-related droop produces a shift in spectral output towards higher colour-correlated temperatures.

As cerium-doped aluminium garnet is less prone to droop than europium-doped nitride red phosphors, at first glance it would appear that the solution is to use this in white-emitting LEDs. But such an approach is not practical, because the spectral output of this phosphor is not suitable for realising a high colour-rendering index. A better way forward is to understand the limitations of europium-doped nitride red phosphors and devise approaches to minimising the droop associated with them.

To gain greater insight into the underlying physics of europium-doped nitride reds, and the impact of photo quenching on LED performance, we prepared $(Ba,Sr)_2Si_5N_8$: Eu^{2+} powders with varying europium concentration. Our quantum efficiency measurements revealed that the rate of quenching in $(Ba,Sr)_2Si_5N_8$:Eu^{2+} increases with temperature and europium concentration (see Figure 4). These findings can guide phosphor material and LED architecture design, and lead to a better understanding of the physics of the quenching mechanism.

We have fitted the experimental rate of phosphor quenching in our samples with a model for radiative and non-radiative recombination processes. This gives a close fit when using a term that is close to the quadratic of the concentration of excited Europium activators. This model replicates results for different concentrations and thicknesses, so long as the non-linear, non-radiative coefficient is kept constant.

These insights suggest that of the two most probable candidates for the non-radiative processes – Foerster/Dexter cross relaxation and excited state absorption – it is the latter that is the likely culprit in phosphor quenching. As excited state absorption is excitation dependent, it is similar to the very familiar non-linear process of droop in InGaN quantum wells. This intrinsic loss mechanism for the phosphor cannot be

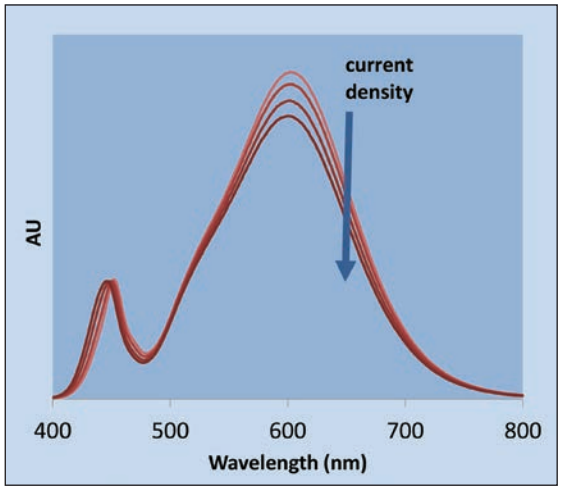


Figure 2: The droop in efficiency is accompanied by the shift in white LED spectra, which gives insights into the process of photo-quenching in phosphors.

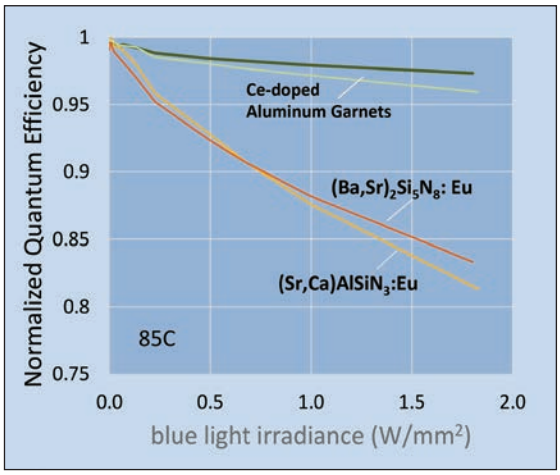


Figure 3: The drop in quantum efficiency with excitation varies with the phosphors used in state of the art LEDs.

eliminated, but it is possible to minimise its impact via engineering at the material and device level.

Our experiments point to an approach for reducing phosphor droop – cutting the activator concentration. The downside is that to realise a desired colour point, there must be a longer optical path for pump light through the phosphor. In practice, this means thicker or heavier-loaded converting layers, which lead to excessive scattering and heating and ultimately lower LED efficiency.

One way to mitigate these unwanted consequences is to turn to ceramic phosphor materials. Their attributes include excellent thermal properties and greatly reduced optical scattering, which allows for thicker converting layers without efficiency penalties. This is a solution that we have adopted in a number of products that feature our Lumiramic phosphor technology (see Figure 5).

LED devices can also be designed to minimise the quenching and its increase with temperature (the effect revealed in our measurements (see Figure 4)). The key is to reduce blue light irradiance and to draw the heat out of the phosphor layer as effectively as possible, while maintaining a low overall temperature.
An illustration of this mitigation of photo-thermal quenching through LED design is provided by a comparison of two die-on-ceramic LED packages – one is a thin-film flip-chip, and the other a flip-chip architecture. With the thin-film flip-chip design – and any thin-film LED architecture for that matter – blue light is extracted through one side of the die. So, due to this, phosphor particles are positioned near the emitting surface of the die, in a thin layer of silicone.

In contrast, with a flip-chip architecture, the phosphor-filled converting layer can be placed on all five sides of the transparent sapphire substrate. This means that the blue light emitted by the active region of the pump LED can be distributed over a larger area than it would be with a thin-film design. What's more, with a flip-chip, the heat of down-conversion is conducted through a larger contact area.

The superiority of the flip-chip architecture over the thin-film flip-chip design is proven in our measurements of normalized optical power output (see Figure 6). As expected, the reduction in the intensity of the pump light on the phosphor, as well as better phosphor heat-sinking in the flip-chip LED, enables this type of design to be less afflicted by droop than its thin-film flip-chip cousin.

For both designs, droop is more prevalent when the device is driven continuously, rather than in pulsed operation. That's because the device driven continuously runs at a higher temperature, and photo-thermal quenching of the europium-doped nitride phosphors is more prevalent.

It is worth noting that at 1.5 A, which is a typical maximum operating current for a 1 mm² active-area high-power LED, although the junction temperatures of both classes of devices are within 5°C of the estimated 125 °C, the difference in phosphor temperatures is significantly higher. This contributes to the difference in light output and efficiency between the two architectures, which is more than 15 percent.

The merits of a lower phosphor temperature and a lower irradiance of phosphor are very welcome,

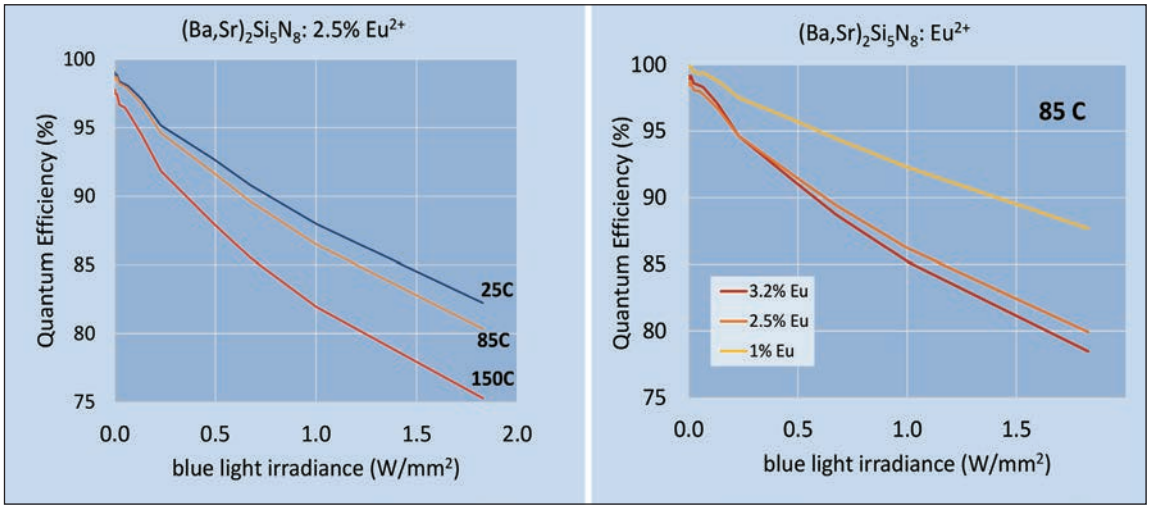


Figure 4: Photo-quenching in Eu2+ red nitrides shows strong dependence on temperature and activator concentration.

because they enable the flip-chip design to maintain high efficiency into even higher current densities. The flip-chip design is not the only architecture for reducing photo-quenching. There are also the remote-phosphor configurations that are often seen in lighting modules, and mid-power LED or chip-on-board-type emitters. In these architectures, blue light is distributed over a large phosphor volume, which helps to maximize efficiency. The downside is a compromise in source brightness, limiting emitter usability.

For high brightness applications – such as automotive LEDs, laser-based sources, and forms of architectural lighting that require narrow, collimated beams – photo-thermal quenching of phosphors is a basic limitation. In these applications there is a need for sources with the lowest etendue possible, which means minimizing the emitting area and the angle of the source.

In short, as photo-thermal quenching is a basic property of phosphor materials, it will impact LED efficiency. While LED architecture design can be used to mitigate this form of droop, ultimately, the best solution is at the material level. We have shown success in this area through the use of ceramic phosphors.

Oleg Shchekin wishes to thank Peter J. Schmidt, Frank Jin, Nathan Lawrence, Ken. J. Vampola, Helmut Bechtel, Danielle R. Chamberlin, Regina Mueller-Mach and Gerd O. Mueller for their assistance with this article.

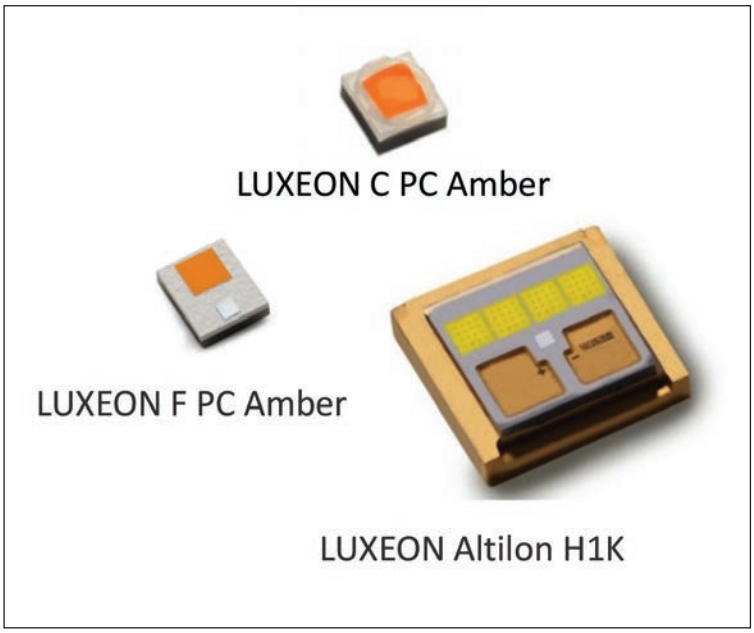


Figure 5: Lumiramic phosphor technology is well suited for high power high temperature applications. Here are some examples of Lumileds automotive LED products which leverage the Lumiramic technology.

Further reading

O. B. Shchekin *et al*. Phys. Status Solidi RRL **20** 273 (2016)

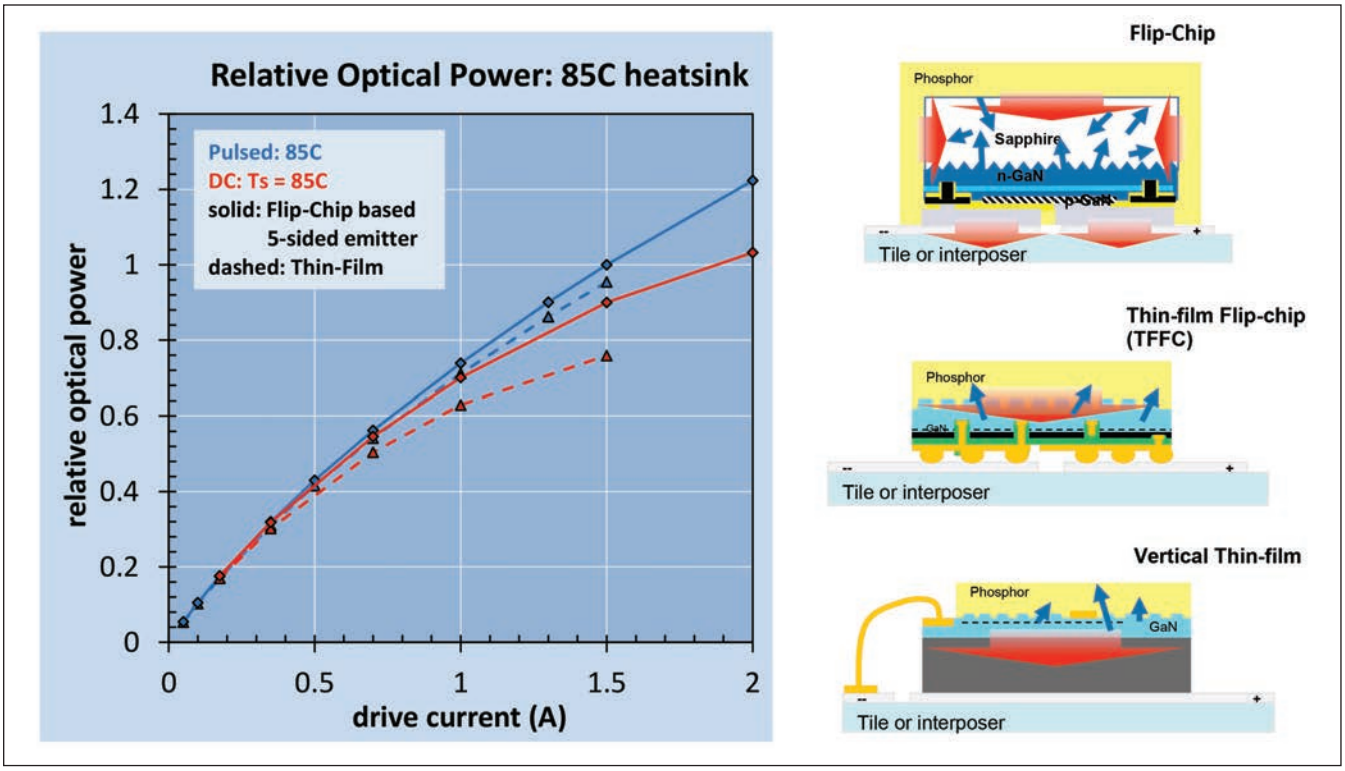


Figure 6: Thin-film architectures excite and dissipate phosphor heat through 'one side', roughly equal to the pump-die area. Multiple sides of a flip-chip allow lower average irradiance and a larger area to conduct out the heat of conversion for the same die area as thin-film. Thanks to these benefits, in DC operation, the five-sided flip-chip emitter is over 15 percent more efficient at 1.5 A.

Getting the GaN VCSEL to market

The output power of the GaN VCSEL hits a new high with the introduction of epitaxial lateral overgrowth

BY TATSUSHI HAMAGUCHI FROM SONY CORPORATION

GaN IS A GREAT MATERIAL for making optoelectronic devices. Global sales of GaN-based blue, green and white LEDs are netting billions of dollars every year, and there is also a substantial market for in-plane lasers emitting in the blue, blue-violet and green. This makes the GaN VCSEL the only obvious omission in the GaN optoelectronic portfolio. But if this device can follow in the footsteps of that made from GaAs, it should enable the production of a class of GaN laser that combines a very low threshold current with the capability to operate at high frequencies and form an emitter array.

Armed with these attributes, GaN-based VCSELs are destined to replace conventional LEDs and lasers as light sources in many applications, including optical storage, laser printers, projectors, displays, solid-state lighting, optical communications and biosensors. And if green and blue forms of this device are united with red-emitting GaAs VCSELs, this could spawn incredibly small, wearable projectors and high-power light sources for full-colour displays.

However, fulfilling this dream will not be easy. Peruse through the scientific literature and you'll soon realise that making a GaN-based VCSEL is far harder than producing a GaAs-based cousin. Multiple issues plague the production of mirrors and cavities, and it is tough to realise sufficient current confinement in the active region to ensure lasing. However, significant

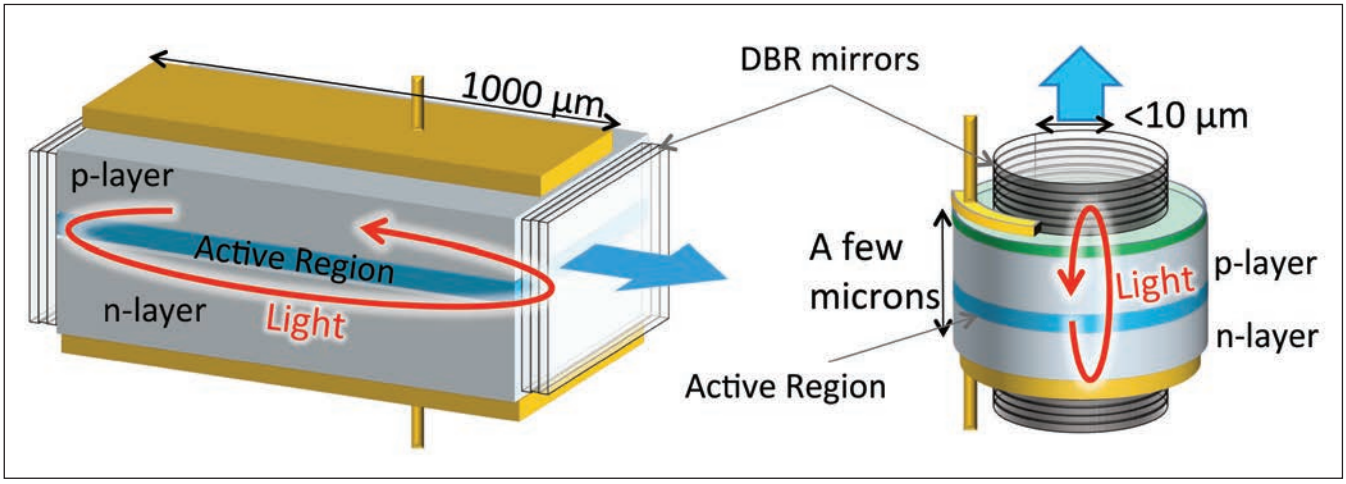


Figure 1. In a VCSEL (right), light travels in the vertical direction to the active region, while in an in-plane laser diode (left) it travels parallel to the active region. This key difference comes from their structures. In a VCSEL, all layers, mirrors and active regions are parallel to each other, so that the direction of photon propagation is vertical to those layers.

breakthroughs are being made, including those by our team at Sony. We are taking output powers to new highs by turning to epitaxial layer overgrowth for the production of high-quality active regions close to the mirrors.

Many of the challenges associated with GaN VCSEL production are absent with GaAs because it can be paired with AlGaAs, a ternary with a negligible difference in lattice constant. Together, these arsenide alloys can form low-defect-density, distributed Bragg reflectors (DBRs) that sit either side of the active region and ensure sufficient optical gain for lasing. What's more, because these materials can be made conductive by doping, carriers can be injected into the active region via deposition of an electrode on each DBR.

Another attribute of the GaAs-based material system is that partial oxidation of AlAs can transform it from a semiconducting to an insulating form. So, when AlAs is inserted next to the active region, it can be oxidised to create a current-confined aperture. This structure is essential, because it enhances induced emission, a pre-requisite for lasing.

With GaN, the situation is markedly different. First and foremost, it is very difficult to produce semiconductor DBRs. When GaN is paired with AlGaN – an approach that is similar to that employed in GaAs-based VCSELs – cracks appear, due to the large lattice mismatches associated with changes in aluminium composition. One promising solution is to pair GaN with $Al_{0.8}In_{0.2}N$, which has a very similar lattice constant. This can ensure the production of crack-free mirrors. However, the price to pay for this success is a low throughput. Reports suggest that the growth rate for AlInN is so low that it would take 12 hours to form a 40 AlInN/GaN DBR with a peak reflectivity exceeding 99 percent. Such a long time is unacceptable for the growth of just one section of a commercial device.

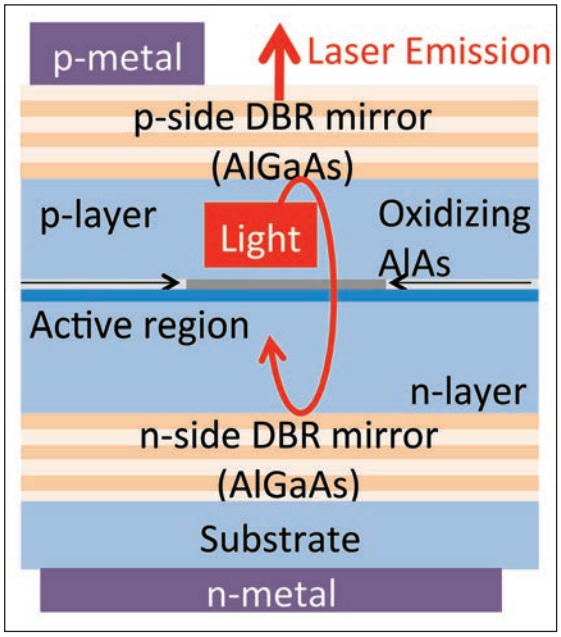


Figure 2. In a GaAs-based VCSEL, the active region is sandwiched between two DBRs. All of the layers are formed by epitaxial growth, permitting both DBRs to be placed near the active region. AlAs can be partially oxidized to leave a current convergence spot that confines carriers.

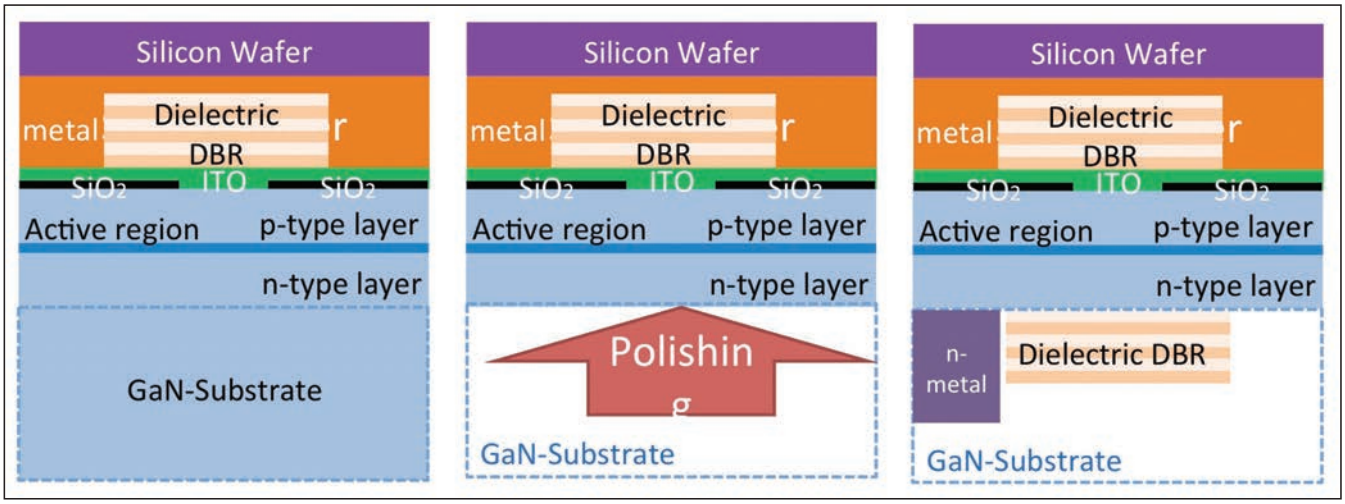


Figure 3. Several groups, including a team from Nichia, have fabricated GaN-based VCSELs by thinning the GaN substrate to a few microns, prior to *n*-side DBR deposition. There are several papers on this type of VCSEL, for lasing wavelengths from the UV to the green. However, almost all were published before 2012. The commercial success of this method appears to be hampered by difficulties associated with polishing a GaN wafer to a thickness of just a few microns.

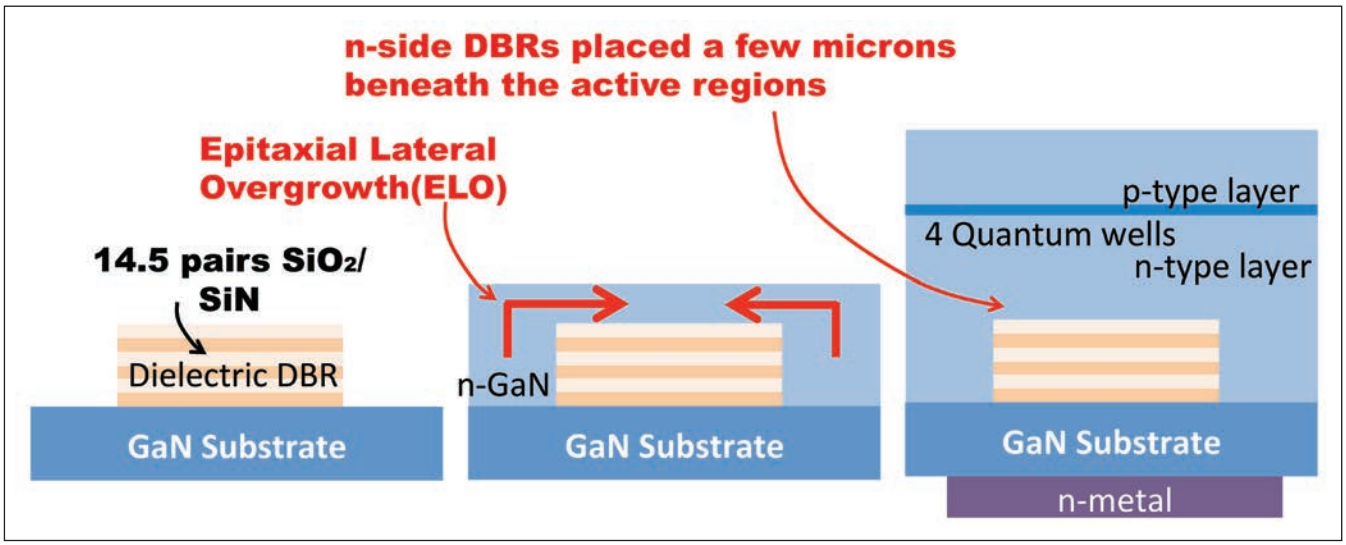


Figure 4. At Sony, GaN-based VCSEL fabrication involves an epitaxial lateral overgrowth process. This assists the placement of the *n*-side DBR just a few microns beneath the active region, as it does not involve a severe process. Prior to this breakthrough, similar structures could only be formed with a delicate thinning process.

Even if such long times could be tolerated, there is still a major issue with the GaN-based DBR: severe thickness control is required. With AlInN and GaN, the small difference in refractive index between these two alloys produces a sharp reflectance spectrum. This is awkward, because a thickness variation in the DBR layer of just ±3 percent can shift the reflectivity peak out of the lasing wavelength and prevent lasing. As a ±3 percent fluctuation in growth rate is very likely in an MOCVD reactor for GaN growth, it is clear that low yields would plague mass production of GaN VCSELs with AlInN/GaN DBRs.

Based on this reasoning, we believe that dielectric materials are a better alternative to wide bandgap alloys for GaN-based VCSEL production. The likes of SiO_2, Ta_2O_5 and SiN can be deposited by common methods, such as electron-beam deposition and sputtering, and there are no concerns relating to growth rates.

If dielectric mirrors are to be a success, they must be incorporated into the fabrication process of the GaN VCSEL. This means that these mirrors must be positioned close to the active region, within a distance of a few microns. Failure to do this will prevent the device from lasing, due to considerable diffraction loss and material absorption in a cavity with a length of 10 μm or more

One advantage of taking this route is that it allows the pairing of two materials that have large refractive indices and produce broad reflectivity spectra. A thickness range in excess of 10 percent can then be tolerated, which is within the process capability of those conventional deposition methods named above.

If dielectric mirrors are to be a success, they must be incorporated into the fabrication process of the GaN VCSEL. This means that these mirrors must be positioned close to the active region, within a distance of a few microns. Failure to do this will prevent the device from lasing, due to considerable diffraction loss and material absorption in a cavity with a length of 10 μm or more.

At Nichia, researchers have tackled this challenge by thinning a GaN wafer, which contains an active region, to just a few microns thick, and then sandwiching it between two dielectric DBRs. As the thin wafer cannot be free-standing, it is bonded to a support wafer, such as silicon, prior to the thinning process.

Difficulties associated with this production process include the development of a highly sophisticated technique for thinning the wafer, and avoiding damage to the active region – according to reports from Nichia, damage within this region appeared after just 10 minutes of device operation. We think that this might be due to mechanical stress in the active region of the thinned structure. Note that Nichia has not published any papers on GaN VCSEL development since 2012, suggesting that the issues associated with this class of VCSEL were serious enough to stifle the project.

We are pursuing an alternative approach to wafer thinning that involves epitaxial lateral overgrowth, with dielectric DBRs forming masks for selective growth. This technique begins with deposition of dielectric

Book your place at the

PIC International Conference

Tuesday 7 & Wednesday 8 March 2017

PIC International will provide comprehensive coverage of all aspects of the integrated photonics industry

This industry is currently debating a handful of key questions: -

- How can PICs support traffic growth? And how can they deliver value to operators? PICs are a solution to the rocketing demands facing datacentres. But what do they need to deliver, and how can they be put to best use?
- Short reach communications could be a major win for PICs. But what are the customer priorities? And how can photonic integrated circuits come out on top? Can companies afford to make PICs in-house? And if they do outsource, what should they look for from a foundry?
- What are the key materials systems driving photonic integration? And how should these platforms evolve to unlock greater performance?
- What are the best resources for creating and delivering photonic integrated circuits?
- What are the prospects for developers more broadly? And how does the supply chain need to adapt?

Our 2nd PIC conference is hotly anticipated and bringing together the best in class of the integrated photonics community worldwide so:

Book your place NOW!

Sheraton Brussels Airport Hotel, Belgium

Register: www.picinternational.net

PIC INTERNATIONAL CONFERENCE

Creating and strengthening links between chipmakers and network builders

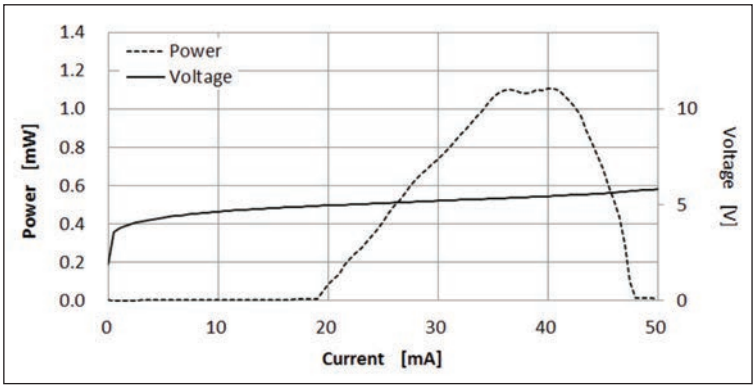


Figure 5. With a maximum CW output of 1.1 mW at room temperature, Sony's VCSEL has broken the power output record for a GaN VCSEL. This 453.9 nm laser has an 8 μm aperture.

DBR islands directly on the GaN substrate. These islands are engulfed in *n*-type GaN by epitaxial lateral overgrowth.

With this approach, seed crystals grow in the window area, where the GaN substrate is exposed between DBR islands. Further growth embeds the DBR islands in an *n*-type film, which provides the foundation for depositing the active region, *p*-type GaN layers and *p*-side DBRs.

The cavity, created by placing the *n*-side dielectric DBR just a few microns beneath the active region, is formed without the need for delicate processes, such as polishing. This is advantageous, because no undesirable mechanical stress is imposed on the active region. The epitaxial layer overgrowth process is uniform over the entire wafer, making it suitable for mass production.

Our VCSELs have set a new benchmark for optical output power of more than 1 mW. This result is very encouraging, and even higher output powers may follow through refinements to the epitaxial layer overgrowth process – remember that it was developed to reduce threading dislocations in GaN grown on sapphire, for the production of GaN-based in-plane lasers. Epitaxial layer overgrowth may also enable the growth of GaN VCSELs on cheaper substrates, such as silicon. This could drive greater deployment of these devices.

Controlling current flow

Another big challenge for GaN VCSEL developers is to realise lateral current control, so that carriers are confined. With GaN VCSELs this is not trivial because there are no equivalents of the conductive DBRs and AlAs layers found in GaAs-based cousins. The good news is that a team led by Tien-Chang Lu from National Chiao-Tung University, Taiwan, has shown that it is possible to control the injection of holes into GaN-based VCSELs by making a transparent electrode from indium tin oxide, and using SiO_2 for insulating regions. Lateral current spreading results from placing ITO between a *p*-side dielectric DBR and *p*-type GaN, while current confinement at a limited part of the active region is realised from partially inserting a thin SiO_2 layer between the ITO and *p*-GaN layers.

Care is needed when taking this approach because ITO could absorb enough light to prevent lasing. The trick is to suppress absorption to negligible levels by adjusting the vertical configuration in the device so that ITO is located at the null point of the resonating mode standing wave.

Another concern is electrical stability at the ITO/*p*-GaN interface. Although ITO is widely employed as a *p*-contact in GaN-based LEDs, the current density in these devices is hundreds of times lower than that expected in a VCSEL. But we have shown that ITO contacts are sufficiently durable in aging tests at current densities as high as 60 kA cm^{-2}. This indicates that ITO can be used in GaN VCSELs.

An alternative approach, for example, pursued by a team from the University of California, Santa Barbara, is to use a tunnel junction to inject holes. With this architecture, a transparent layer is formed by highly conductive *n*-GaN laid over *p*-GaN. An appealing aspect of this technology is that it mirrors the approach used in GaAs and InP. However, because GaN has a far higher bandgap than GaAs, it is difficult to reduce the operating voltage of the GaN-based tunnel-junction. When GaN VCSELs incorporate this, the operating voltage is higher by 1 V or more, due to the large built-in voltage at the tunnel-junction. It is our understanding that to ensure reliable operation in a laser diode, the voltage drop at the tunnel-junction should be no greater than 0.1 V at the operating current density. So the tunnel-junction must be improved by an order of magnitude before it can be considered as a replacement for ITO in GaN VCSELs.

Multiple markets

Thanks to the recent breakthroughs, it is now appropriate to consider potential applications for the GaN VCSEL. There are many, as this device can span

Our VCSELs have set a new benchmark for optical output power of more than 1 mW. This result is very encouraging, and even higher output powers may follow through refinements to the epitaxial layer overgrowth process – remember that it was developed to reduce threading dislocations in GaN grown on sapphire, for the production of GaN-based in-plane lasers

the UV through to the green, which is a spectral range that has not been reached with GaAs-based VCSELs. At the shorter end of this range is the 375 nm VCSEL, which could be paired with ytterbium ions to deliver greater accuracy in chip-sized atomic clocks – they currently employ GaAs-based near-IR VCSELs and rubidium gas. At the slightly longer wavelength of 405 nm, the GaN VCSEL could replace the GaAs-based VCSEL in laser printers, where it would enable a finer resolution; while at 488 nm, the VCSEL could be used in bio-sensing applications; and in the green, it could expand the use of optical communication in plastic optical fibre. These low-cost waveguides have a high optical loss in the red and IR, but not in the green.

Even more exciting is the combination of the classic red GaAs VCSEL and its blue and green GaN variants. Working together, they can provide full-colour light sources for displays. Arrays allow an increase in the output of VCSEL sources, and a path to watt-class red-green-blue modules.

At far lower powers, these modules are good candidates for retinal-scanning wearable displays. As it is easier to maintain small peak powers with VCSELs than in-plane devices, this form of laser is ideal for keeping retinal projection systems safe for eyes. With an in-plane laser, the addition of a neutral-density filter ensures eye-safety; however, such a configuration drives up energy consumption, resulting in a need for higher-capacity batteries. This is highly undesirable, because it increases the dimensions of wearable displays and reduces the usability of the device. Further opportunities for GaN VCSEL arrays include reinforcing functions of electronic devices, where single-beam scanning of in-plane lasers is currently used. For example, arraying a 405 nm VCSEL could speed optical storage and 3D printing.

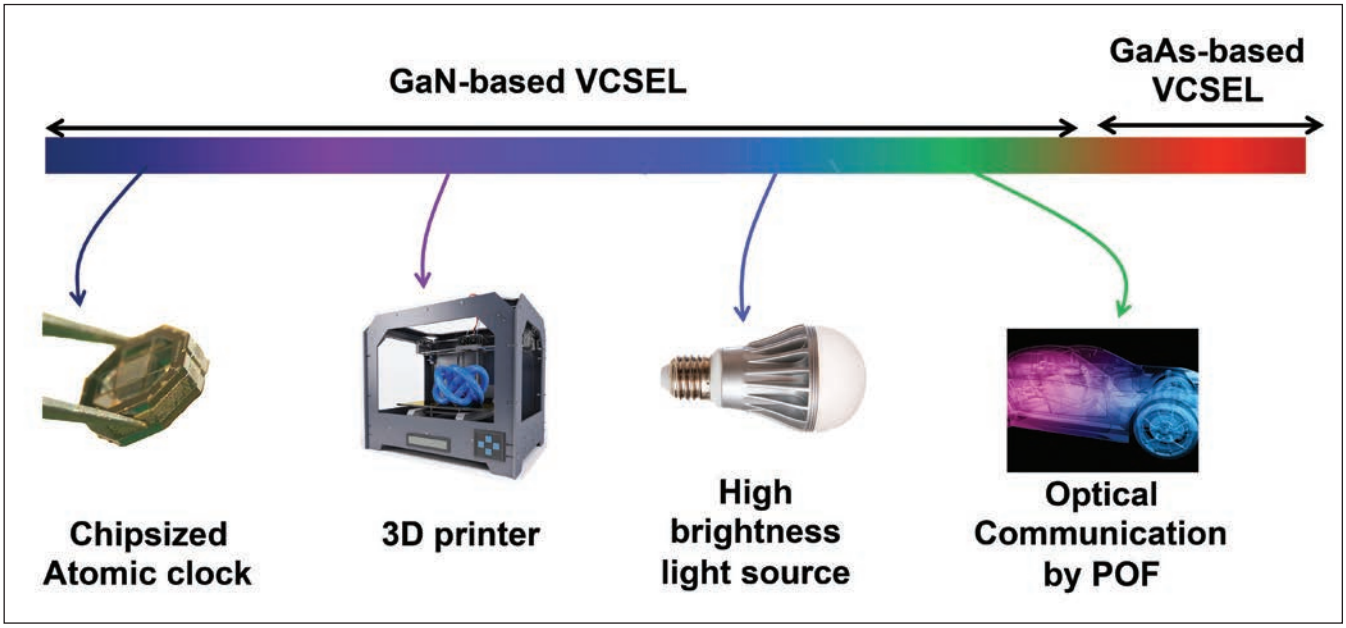
Some of the other virtues of the GaN VCSEL should enable improvements in applications currently using 445 nm LEDs. They include visible light communication, where the higher frequency operation of the VCSELs provides a broader band; and the light source for car headlamps, where efficient operation under large current injection improves high brightness.

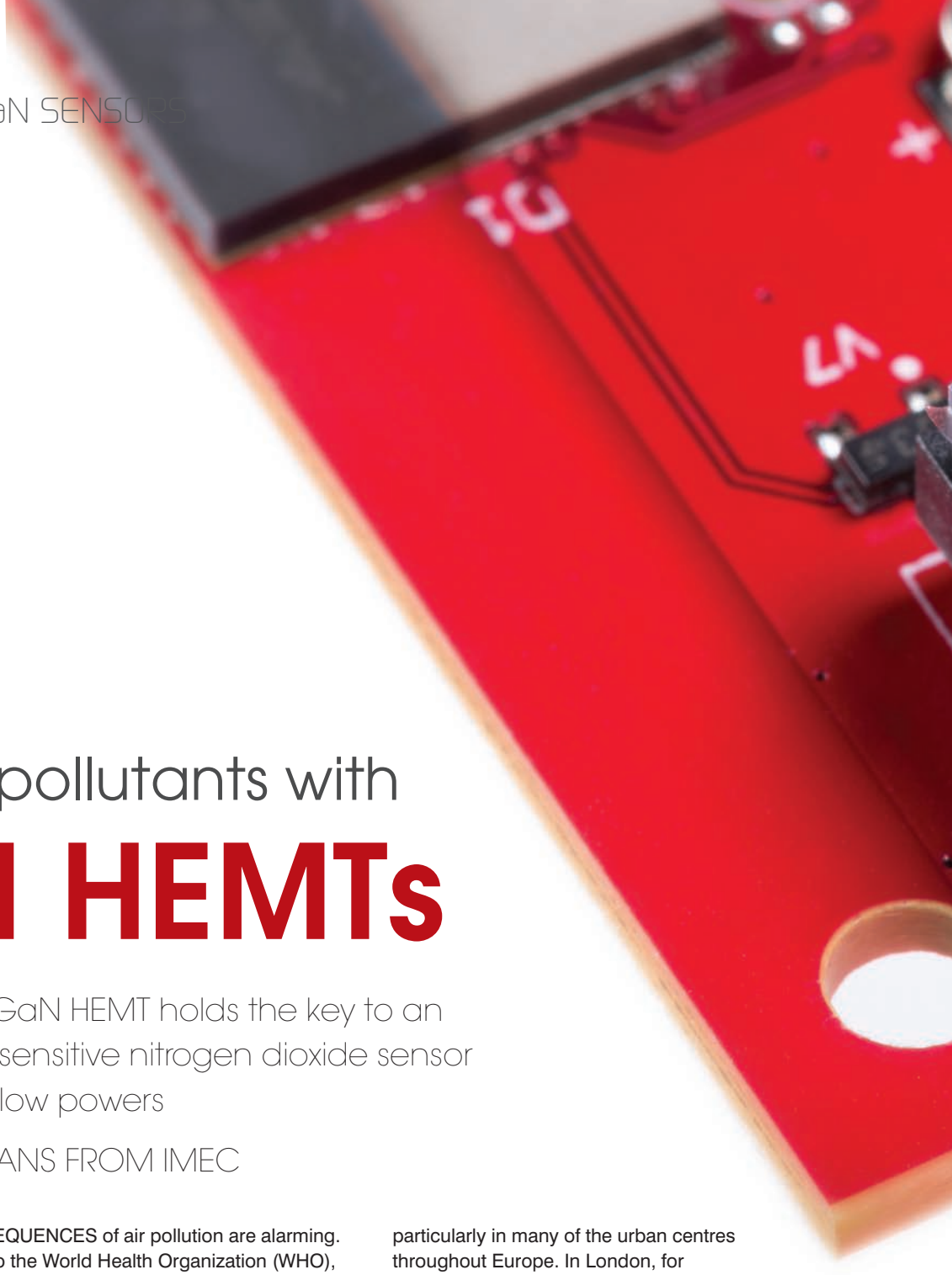
The market for VCSELs is already worth hundreds of millions of dollars, and analysts are predicting further growth. We believe that this could be spurred by the introduction of GaN VCSELs, following successful efforts to address issues that have held back the performance of this very promising device.

If you wish to contact the author, they can be reached at tatsushi.hamaguchi@jp.sony.com

Further reading

T. Hamaguchi *et. al.* Physica Status Solidi A **213** 1170 (2016)
Y. Kozuka *et. al.* "Growth of AlInN Single Layers and Distributed Bragg Reflectors for VCSELs." MRS Proceedings 1736 Cambridge University Press, (2015)
Y. Higuchi *et. al.* Appl. Phys. Express **1** 121102 (2008)
T.-C. Lu *et. al.* Appl. Phys. Lett. **97** 071114 (2010)
J. T. Leonard *et. al.* Appl. Phys. Lett. **107** 011102 (2015)





Exposing pollutants with GaN HEMTs

The freestanding GaN HEMT holds the key to an affordable, highly sensitive nitrogen dioxide sensor operating at ultra-low powers

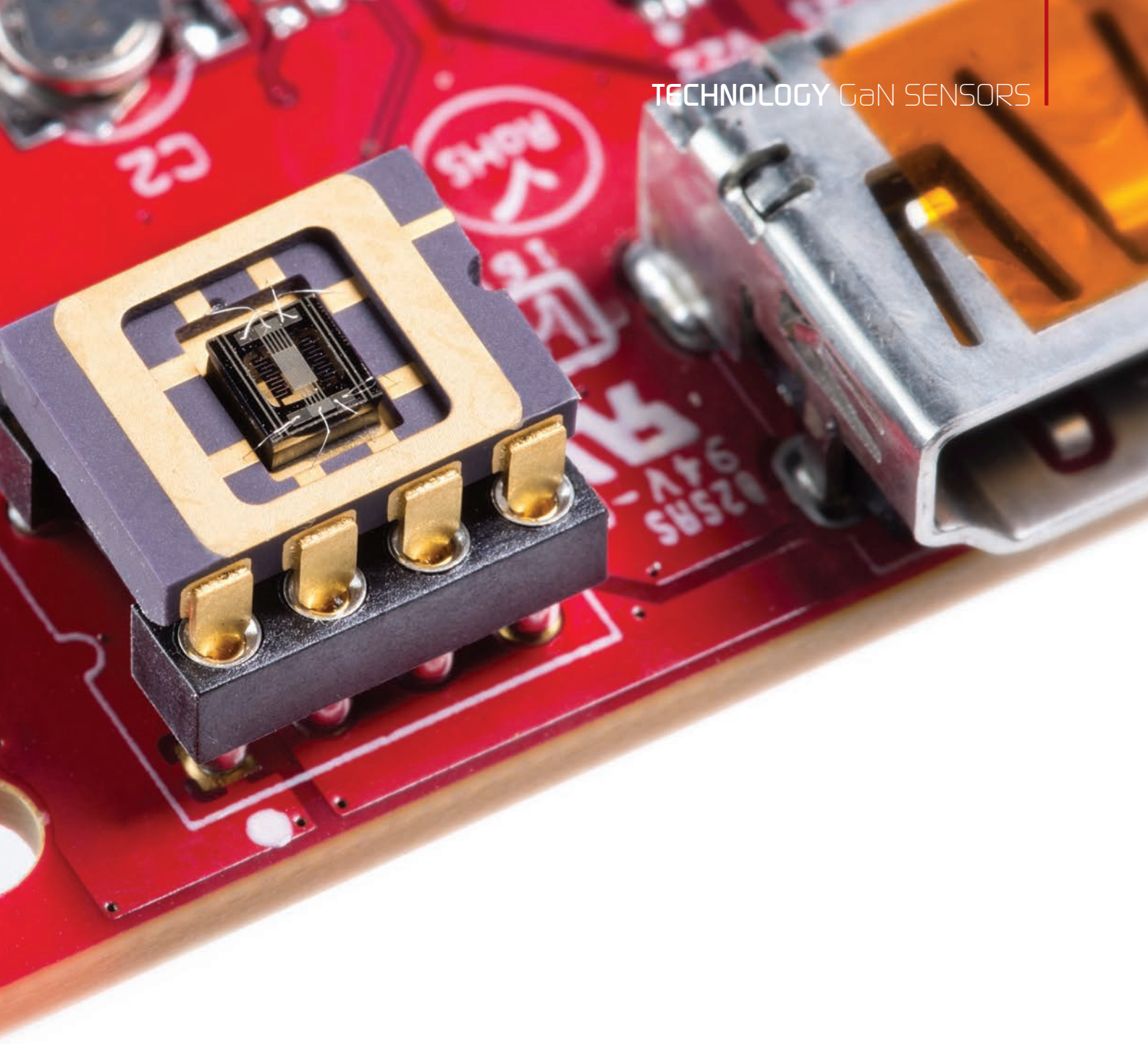
BY PETER OFFERMANS FROM IMEC

THE CONSEQUENCES of air pollution are alarming. According to the World Health Organization (WHO), each year a staggering 3.7 million loose their lives to outdoor air pollution, of which 80 percent die from a heart disease or a stroke, and the remainder have fatal respiratory illnesses and lung cancer.

Two pollutants are to blame for many of these deaths: dangerous airborne particles with diameters of several microns or more and NO_2. Long-term exposure to the latter has been linked to bronchitis in asthmatic children, and it is known to impair lung growth in concentrations currently found in cities of Europe and North America. Another downside of NO_2 is that it is the primary source of nitrate aerosols, which form an important fraction of dangerous airborne particles with diameters of 2.5 μm or less.

To curb deaths, the WHO has set an annual mean guideline for exposure to NO_2 of 40 $\mu g/m^3$, which equates to 20 parts-per-billion. However, this recommended upper limit is often exceeded, particularly in many of the urban centres throughout Europe. In London, for example, in just the first eight days of 2016, the far higher legal limit of an hourly mean of more than 200 $\mu g/m^3$ of NO_2 was breached on 18 occasions. One of the primary causes of these high levels of NO_2 is the diesel engine, which may generate more of this oxide than one would expect, given the revelations emerging from the Volkswagen scandal.

In several big European cities, air quality monitoring networks are in place to monitor urban background and roadside emissions. These measurements, obtained with highly accurate but expensive analyzers, are combined with computer models to assess concentrations in places where monitoring sites are absent. It would be better to deploy more monitors. And thanks to the advent of the Internet-of-Things this might happen, because there is a growing interest in the use of miniaturized, low-cost air quality sensors that could create denser wireless networks. Such sensors could provide valuable complementary



information to the existing monitoring sites. Progress has already been made in this field. Low-cost miniaturized sensors are now on the market, typically based on electrochemical cells or metal-oxide based devices (see “State-of-the-art miniaturized sensors” for details).

However, their sensing performance is not as good as that of conventional analyzers, according to air quality field testing campaigns, such as those organized by the European Network on New Sensing Technologies for Air-Pollution Control and Environmental Sustainability (EuNetAir). Weaknesses of these sensors include limited sensitivity, as well as cross-sensitivity to other gases, such as humidity and ozone.

More research has to be done to integrate these new technologies into smart sensing networks that can deal with some of their limitations. At the same time, demand for sensors that are selective, sensitive, and draw ultra-low-power is driving the research and development of a next-generation of sensors, known

In London, air quality measurement stations show NO_2 levels often exceed the recommended maximum level set by the World Health Organisation.

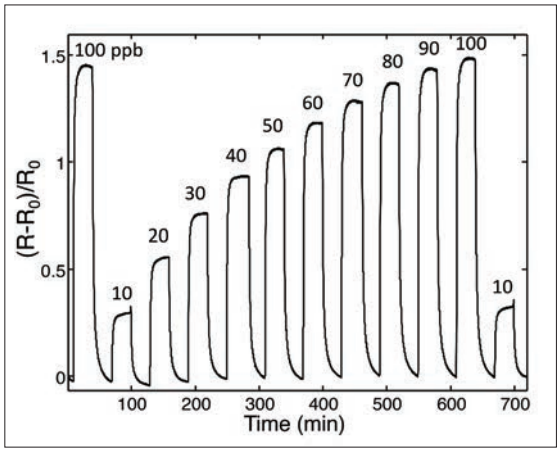


Figure 1. Operating at 250°C using an integrated heater, imec's GaN HEMT can distinguish between various concentrations of NO_2 in humidified cleaned air. Upon NO_2 exposure, the resistance increases until reaching a concentration and temperature-dependent equilibrium between NO_2 absorption and desorption. Between NO_2 exposures, the sensor recovers to the baseline by thermally induced desorption.

as microsensors and nanosensors. At the European microelectronics centre imec we are involved in this effort through the development of a novel gas sensor platform. It is based on the suspended AlGaN/GaN membrane and can combine operation at ultra-low-power with high sensitivity to NO_2 and low interference from humidity.

As many of the readers of this magazine know, the GaN material system is already used to churn out billions of chips every year. Manufacture of blue, GaN-based LEDs is a well-established global industry, while, in comparison, sales of GaN HEMTs are not as high. However, they are being used to make RF and power electronics devices, and they show great promise as a generic platform for developing high-performance sensing devices.

Exploiting the electron gas

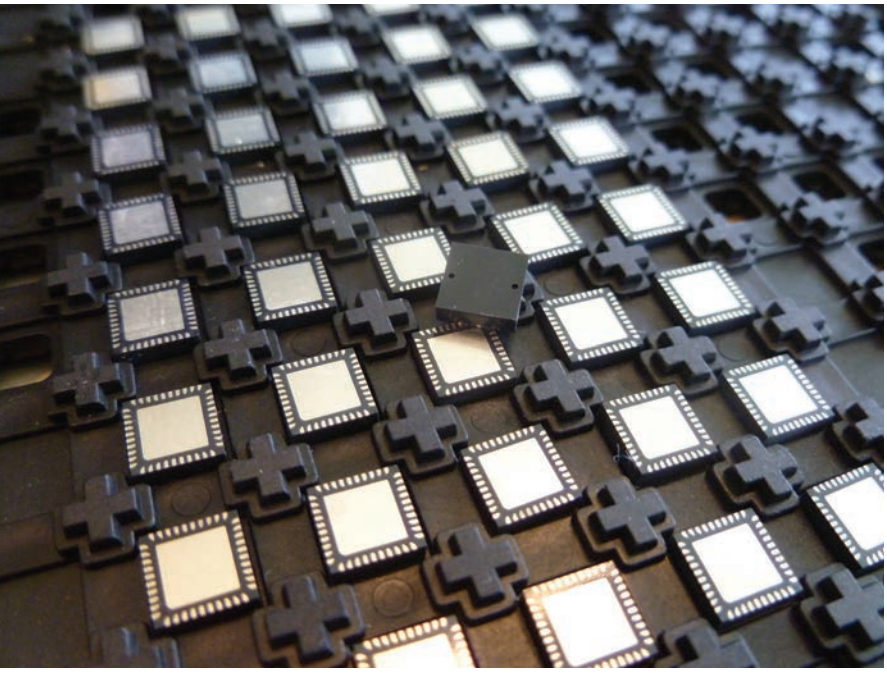
Our sensors exploit the sensitivity of the highly mobile two-dimensional electron gas (2DEG) formed at the AlGaN-GaN interface. Thanks to the high sensitivity of the induced 2DEG to changes in surface charge it is possible to have a direct electrical readout of surface interactions involving charged species.

A search through the in scientific literature reveals that the GaN HEMT has already been used to form a variety of gas, chemical and health-related sensors. Surface functionalization of the gate area has enabled the detection of: certain gases, such as hydrogen; polar vapours and liquids, such as alcohols; biomolecules, including antigens and DNA; and electrochemical detection of pH and other ions, such as mercury.

We have found that these devices can be incredibly sensitive to NO_2. Their response, defined as the change in device resistance, normalized by the baseline resistance (the device resistance before exposure to NO_2) can reach the low-parts-per-billion range through precise recessing of the AlGaN layer at the gate area. Thinning this ternary dramatically improves performance, with sensitivity increasing by nearly three orders of magnitude as AlGaN is trimmed from 25 nm to less than 10 nm. Note that recessing is a known technique in gated devices, where it is used to improve HEMT characteristics.

With our sensor, the response to NO_2 exposure is an increase in signal until it reaches a concentration dependent steady-state (see Figure 1). At that point, the sensor is in a state of equilibrium between gas adsorption and desorption. Following exposure the sensor recovers to the baseline due to gas desorption from the surface.

Our sensors are capable of detecting differences in NO_2 concentration as small as a single part-per-billion, thanks to the extremely low noise level of the buried 2DEG (see Figure 2). This level of sensitivity is comparable to that of state-of-the-art chemiluminescent analyzers.



Sensor packaging using film-assisted molding by APC/ Boschman

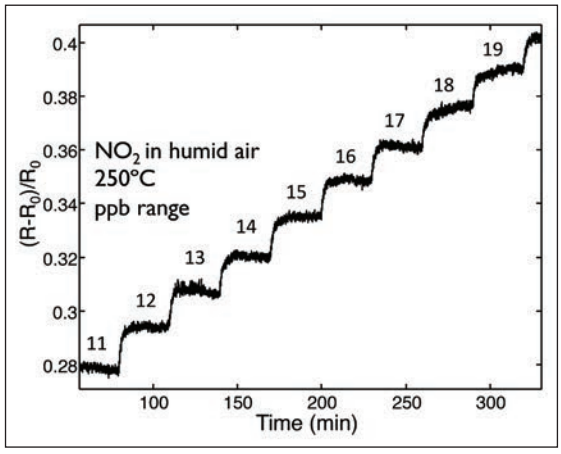


Figure 2. imec's sensor can resolve single parts-per-billion steps for NO_2 concentrations between 11 ppb and 200 ppb. The device was operated at 250°C in humidified cleaned air. The steps in the relative response are well above the noise level, indicating a sensor resolution below 1 ppb in the low ppb range.

The response and recovery times for our detector are strongly governed by a thermally activated process. Due to this, there is an exponential decrease in response and recovery rates with temperature. When the sensor is at room temperature response times can be as long as 1 hour, while recovery is very limited; but when the sensor is heated to 300°C, the steady-state response times (t_{90}) can be as fast as 1 minute for NO_2 levels as low as parts per billion. Heating is a double-edged sword, however, as faster response and recovery times resulting from heating must be weighed against increased power consumption.

We tackle this weakness by exploiting a unique feature of GaN-on-silicon technology – it allows removal of the substrate via plasma etching. We fabricate devices on 200 mm GaN-on-silicon (111) wafers with a mature process flow that is based on that of a power HEMT. But instead of processing the usual gate structure, we fabricate a tungsten resistive heater around the gate area. This provides integrated heating. The final processing step, as shown in Figure 3, is to plasma etch the silicon substrate below the active area to create freestanding AlGaN/GaN membranes – so called micro hotplates.

With this design, the power needed for heating is slashed 100-fold. Thermal losses to the substrate are

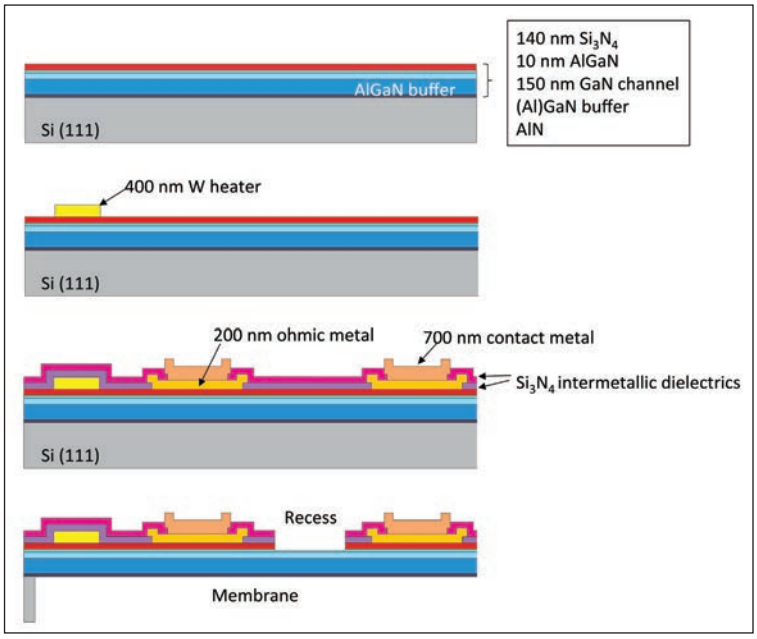


Figure 3. Fabrication of imec's NO_2 sensor begins with growth of an AlGaN/GaN heterostructure on an 8-inch silicon (111) wafer. The tungsten heater surrounding the structure is processed first, followed by the source/drain contacts and contact leads. Recessing the sensing area between the source and drain strongly enhances gas sensitivity. The final processing step is the etching away of the silicon substrate below the active region.

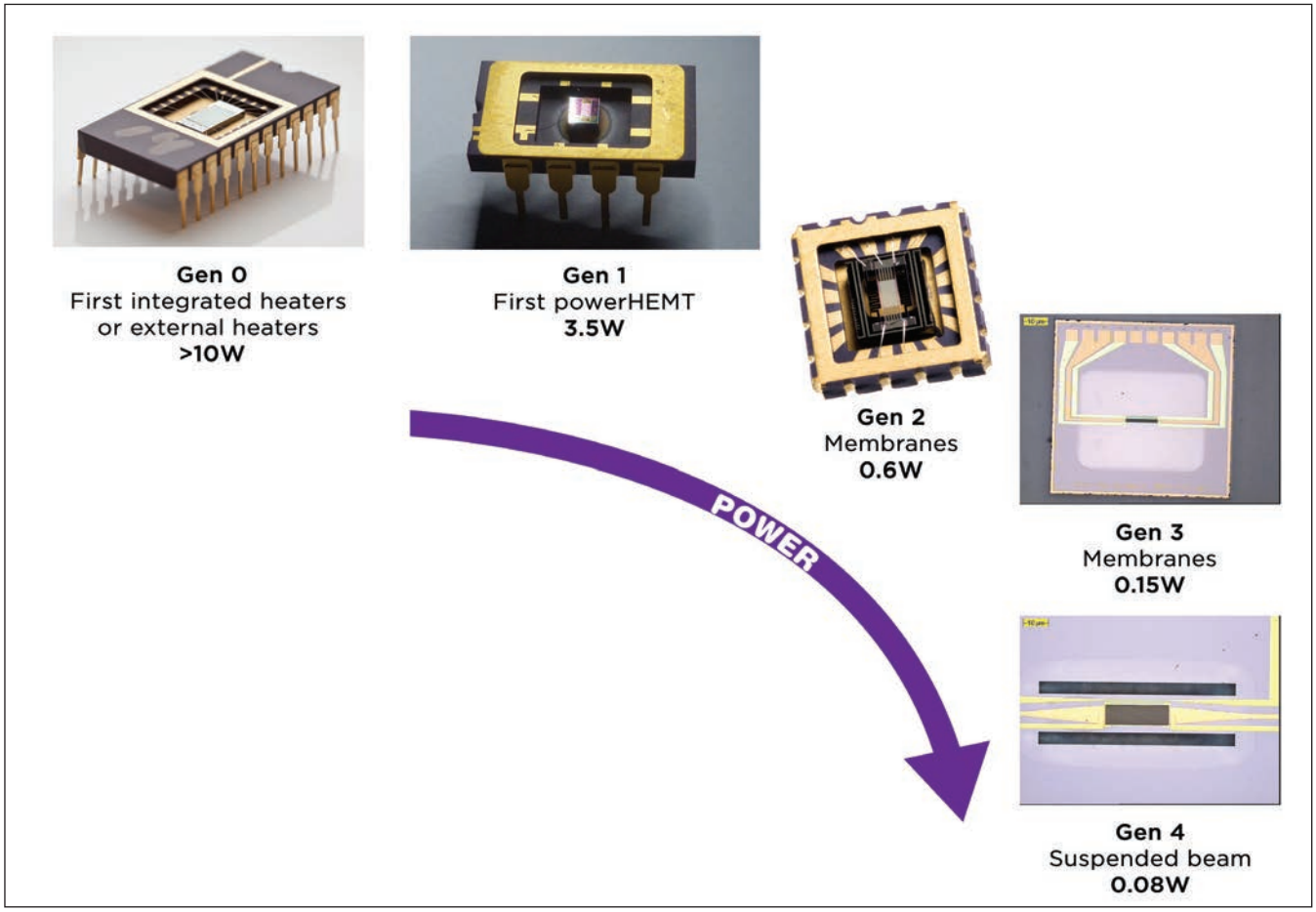


Figure 4. The NO_2 sensor's power consumption has been slashed by introducing a membrane architecture.

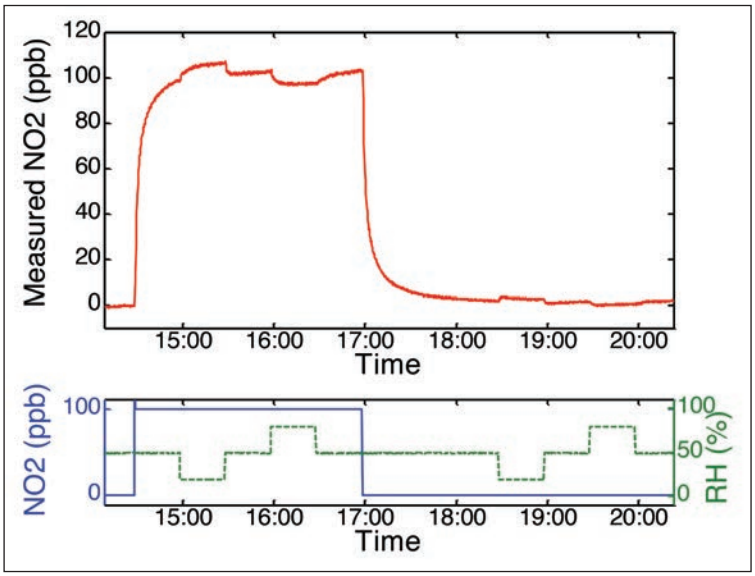


Figure 5. One of the key advantages of imec's HEMT-based device, compared with a conductive metal-oxide sensor, is the small interference from humidity. The graph shows the calibrated NO_2 response for humidity levels of 20 percent, 50 percent and 80 percent. The effect of humidity on the baseline is insignificant. Note that humidity competes with NO_2 absorption, decreasing the NO_2 sensitivity at higher levels of relative humidity.

eliminated, and heating requirements are restricted to just that of the active area within the membrane. Additional power savings result from duty cycling, facilitated by the ultrafast heating and cooling of the thin membranes. This enables power consumption to be trimmed to just a few milliwatts (see Figure 4).

Another strength of our design is its superior rejection of humidity-based interference compared to state-of-the-art, metal-oxide-based sensors. Measurements of NO_2 at relative humidity levels of 20 percent, 50 percent and 80 percent show that this has an insignificant impact on the baseline (see Figure 5). The NO_2 response, meanwhile, is shifted by less than 10 percent by these variations in humidity.

The superiority of our sensors stems from their design. With metal-oxide-based sensors, conductivity takes place across grain boundaries at the surface; but with our devices, the transduction mechanism is notably different, due to the burying of the conductive 2DEG beneath the surface. Nevertheless, the 2DEG density is balanced by the surface charge, so it is influenced by interactions of electron accepting or reducing gases with surface states. For example, our sensor is sensitive to ammonia in the parts-per-million range, but the response is opposite to that of NO_2 – that is, resistance falls rather than increases. That's because ammonia acts as an electron donor, while NO_2 is an electron acceptor.

A rigorous assessment of the capability of any sensor has to involve field trials. We have taken our devices to a parking garage at our High Tech campus, where we compared their response to that of a chemiluminescent analyser.

Results show that the sensitivity of our device compares very well (see Figure 6). Both sensors reveal peaks in NO_2 concentration that correspond to greater traffic at the start and the end of the work day, and variations in the background NO_2 concentration. Unfortunately, these trials have also uncovered limitations with our devices. After several days of testing, significant interference in our sensor response appeared, probably caused by the presence of an

State-of-the-art miniaturized sensors

TODAY'S typical electrochemical sensor consists of a sensing electrode and a counter electrode, separated by a thin electrolyte layer. The gas of interest diffuses through a porous hydrophobic barrier, before reacting at the surface of the sensing electrode, via either an oxidation or a reduction mechanism. This creates an electrical current between the electrodes that is proportional to the gas concentration.

In practice, electrochemical sensors are only fairly selective, even though the electrode materials that act as catalysts for the reactions are specifically developed for the gas of interest. Electrochemical sensors also suffer from: lower sensitivities compared to expensive analytical equipment; and a limited lifetime, due to slow evaporation of an aqueous electrolyte that results in the need for periodic recalibration of the sensor. However, these devices do combine ultra-low power operation with a linear response and comparatively low cost.

Metal-oxide based sensors are gaining popularity. They can be fabricated on silicon wafers, which trim costs and cut sizes. Detection of the gas results from oxidation or reduction reactions with a conductive metal-oxide film deposited over two electrodes. These reactions take place at grain boundaries within the metal oxide film, leading to an increase or reduction in the potential barriers between those grains. This modulates the current flowing between the electrodes. The chemical reactions depend strongly on the working temperature of the sensor. It is often several hundreds of degrees Celsius, so structures are typically made on so-called microhotplates. The tiny suspended membranes are produced from silicon wafers using sophisticated micromachining techniques. They minimize heat loss to the substrate, and therefore power consumption, which is typically tens of milliwatts.

One disadvantage of many metal-oxide based sensors is that they produce a nonlinear response and drift. However, this may be compensated for by intelligent read-outs. Additional drawbacks, similar to electrochemical cells, are limited sensitivity and interference from other gases, such as humidity.

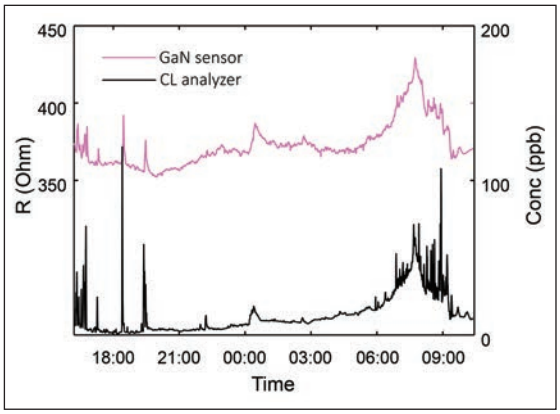


Figure 6. Field trials provide a rigorous assessment of the capability of the sensor. Engineers at imec evaluated their HEMT-based device in a car park.

unknown gas or vapour. This should not come as a surprise, given the large variety of gaseous and vaporous compounds that can be produced by burnt and partially unburnt fuel.

It is not easy to address this issue, because it is related to the chemical properties of the sensor surface. Solutions include tuning properties or resorting to a filter. Another option is surface functionalization, involving the addition of chemically active structures – they could be (metal) nanoparticles, polymer layers, self-assembled monolayers, or advanced structures such as metal-organic-frameworks. This modification can deliver an additional benefit, as it extends detection to other interesting gases, such as CO_2 and H_2 (see Figure 7). However, although surface functionalization enables high tunability of the sensor surface, its practical application is a matter of on-going research.

Dicing and packaging

Fabrication of imec's sensors involves removal of silicon substrates to yield GaN membranes. Although the wafers are fragile, they can be saw-diced by simply protecting device with a UV sensitive dicing foil. This foil can be removed from the diced wafer using a second peel-off foil after UV exposure and heating.

Another issue addressed by imec's engineers is the light sensitivity of the devices. Although the fabricated membranes are transparent to visible light, they are still sensitive in the UV, due to the wide bandgap of GaN. To address this, prototype packages were introduced that shield the device from light, but allow undisturbed gas flow.

This work has been partially realized within the project "MSP - Multi Sensor Platform for Smart Building Management" (FP7-ICT-2013-10 Collaborative Project, No. 611887)

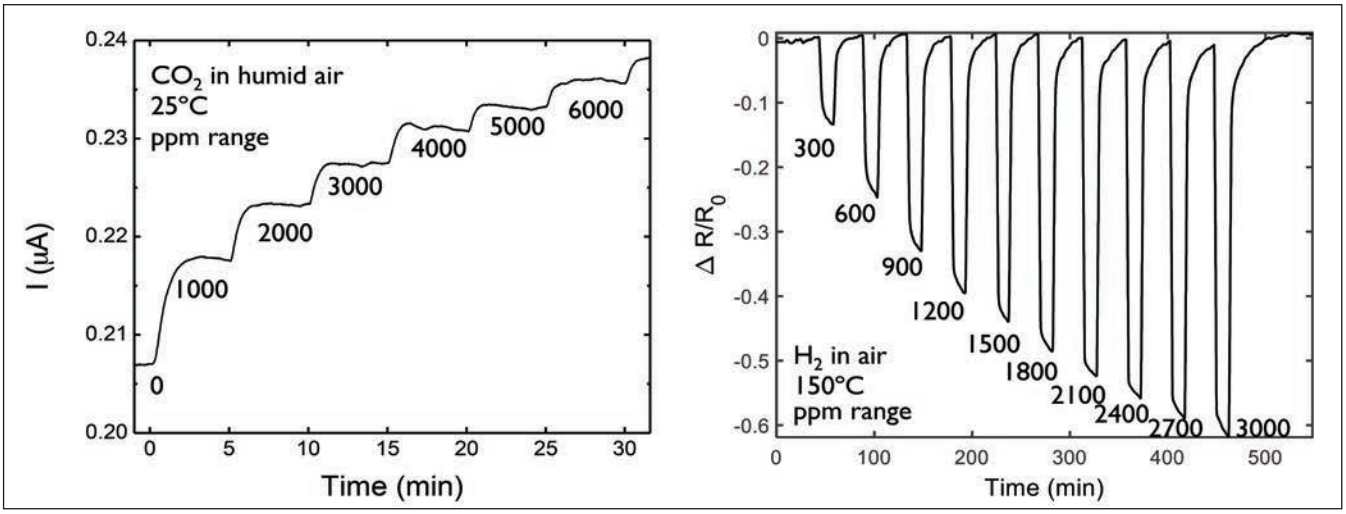


Figure 7. The high sensitivity of the 2DEG to surface charge can be employed for the detection of CO_2, a gas that is currently gaining interest for indoor air-quality monitoring. In contrast to NO_2, CO_2 does not interact directly with the sensor surface: even exposure to 10 percent CO_2 does not result in any response. However, after simply coating the surface with a pH sensitive polymer, such as polyethylenimine, concentrations well below 500 ppm can be detected. This is sufficient for indoor use. The sensor is able to detect CO_2 because it induces pH changes within the coated layer. Specifically, the absorption of CO_2 results in protonation of polymer side groups, which effectively gate the recessed 2DEG channel and increase device current. Note that detection of hydrogen concentrations in the ppm range is possible via thermal evaporation of a 5 nm-thick platinum layer on the recessed gate area.

InGaAs finFETs for future CMOS

Regardless of its form, the silicon transistor is tipped to offer diminishing returns at the 7 nm CMOS node and beyond. Can the InGaAs finFET step in and maintain the march of Moore's Law?

BY JESÚS DEL ALAMO, ALON VARDI AND XIN ZHAO FROM MASSACHUSETTS INSTITUTE OF TECHNOLOGY

THE LAST FEW YEARS have witnessed an explosion of interest in exploring the use of III-Vs to advance logic CMOS beyond the point of diminishing returns for silicon technology. There is now a tantalizing possibility that these compound semiconductors will enter the CMOS roadmap. If they do, the benefits could be huge – they could extend Moore's Law by two or three more nodes, a huge contribution in itself, and they could also hold the key to revolutionary new technologies that are enabled by the integration of III-Vs on silicon. This combination could create systems that combine logic, terahertz sensing, imaging and communications, as well as optical functions.

When it comes to prototyping III-V based transistors for silicon integration, InGaAs is attracting the most attention. Its greatest virtue is its outstanding electron velocity that has enabled the fabrication of record-breaking HEMTs and HBTs. But interest in this ternary goes beyond its high speed credentials. By adjusting its composition, InGaAs can span a wide range of lattice constants, effective masses and bandgaps. This allows the fine-tuning of its electrical properties. What's more, this alloy can be paired with other III-Vs, such as InAlAs and InP, to provide the possibility for flexible, powerful, bandgap and strain engineering.

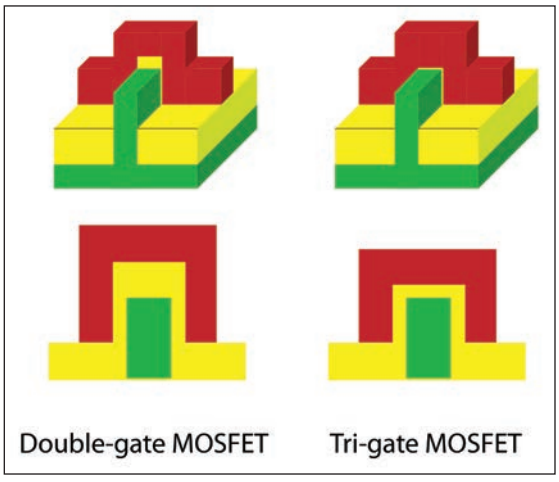


Figure 1. Two breeds of finFETs: a double-gate MOSFET and a trigate MOSFET.

InGaAs also has the merit of forming oxide-semiconductor interfaces of excellent quality when partnered with a high-κ dielectric.

Armed with all these attributes, InGaAs has recently been used to form planar MOSFETs with impressive characteristics. Their fabrication, which has fuelled further confidence in the potential of this material system, has drawn on the development of highly scaled MOS gate stacks with excellent interfacial characteristics, ohmic contacts with low contact resistance, and very tight self-aligned designs.

While the planar InGaAs MOSFET has been an excellent platform for exploring process development and device physics, its scaling potential is limited – gate lengths below 40 nm do not seem feasible. That is not a major concern, though, as three-dimensional transistor structures, such as finFETs, trigate FETs, or nanowire MOSFETs, will be needed at the most likely point of insertion into the CMOS roadmap. Only these architectures can attain the footprint that will comply with Moore's Law transistor density goals.

As its name suggests, the conducting channel in a finFET resides in a thin 'fin' of semiconductor that sticks out of the wafer surface. With this architecture, the transistor gate can either be placed on two sides to create a double-gate MOSFET, or on three to form a trigate MOSFET. Both geometries yield a high degree of electrostatic control, enabling scaling of the gate length to very small dimensions (see Figure 1). Of the two, it is the trigate structure that is used today in state-of-the-art silicon MOSFETs in the most advanced CMOS nodes.

During the last few years, several groups have demonstrated finFETs with an InGaAs channel. Unlike planar InGaAs MOSFETs, performance is rather unimpressive, due to challenges that are unique to finFETs and yet to be tackled. At MIT we are working on these issues, and have made significant strides, with successes including an etching process that can yield high-quality, vertical fins and a novel approach

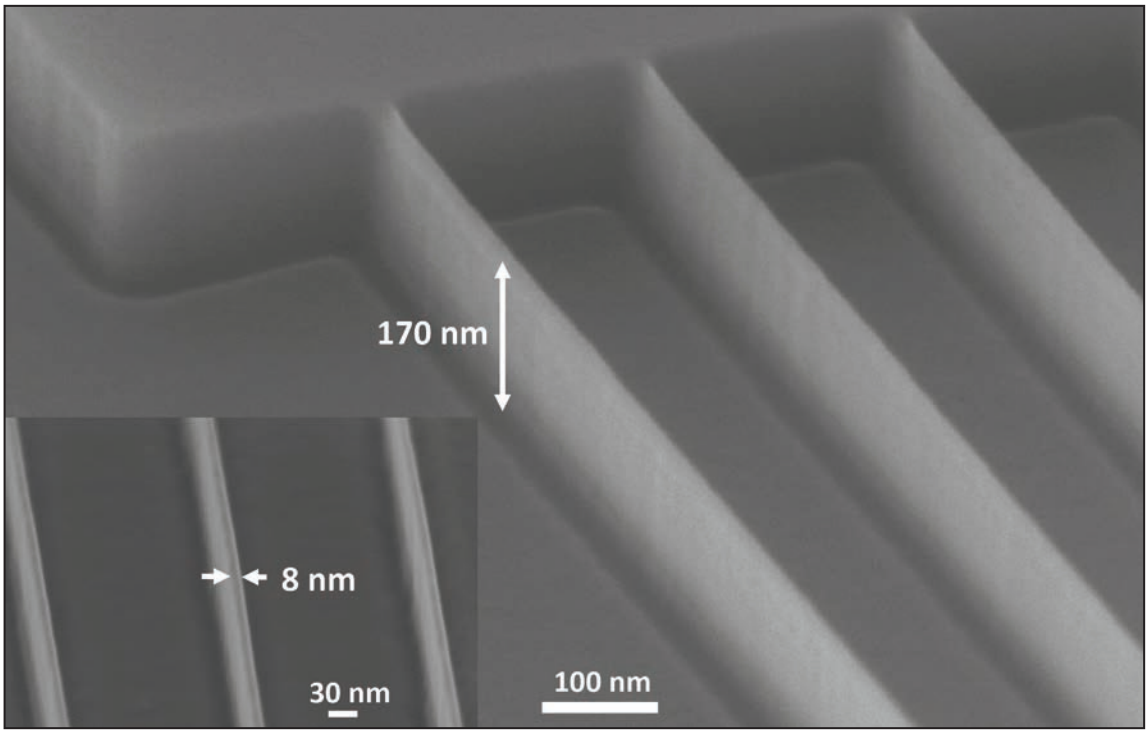


Figure 2. InGaAs fin array etched by reactive ion etching followed by three cycles of digital etch. The final fin width is 8 nm and the fin height is 170 nm (aspect ratio = 21).

for adding metal contacts. The devices that result are setting a new benchmark for this class of transistor, when judged in terms of key metrics.

InGaAs fins

With the finFET, device performance depends a great deal on the quality of the fin. At the point of insertion into the CMOS roadmap, transistors must sport a fin width of less than 10 nm and an aspect ratio in excess of 5 – in other words, the channel must be at least five times as high as it is wide.

To produce fins with this geometry, several teams have pursued bottom-up techniques based on aspect-ratio trapping. This approach, which involves the growth of compound semiconductor heterostructures in a narrow dielectric trench, is attractive because it enables relatively straightforward integration of III-Vs on a silicon wafer. Dislocations arising from lattice mismatch between silicon and the III-V heterostructure are annihilated at the sidewalls, leading to defect-free material towards the top of the fin. Well, that's the promise. In practice, however, the fin contains residual defects and atomic intermixing, resulting in poor transistor isolation and bad performance.

Approaching the challenge from the opposite direction are top-down techniques. They include reactive ion etching, a process that can yield high-aspect-ratio fins with vertical sidewalls.

We have refined this technique, using a combination of BCl_3, $SiCl_4$ and argon to etch III-Vs and form fins. We have also demonstrated trimming of the fin and smoothing of its sidewalls through so-called 'digital etch'. This highly controlled, self-limiting process preserves fin shape while smoothing the sidewalls. Combining our two techniques has enabled us to form InGaAs fins with a width of less than 10 nm and an aspect ratio in excess of 5 (see Figure 2).

With the finFET, the quality of the sidewall is critical. If it is excessively rough, or riddled with a loss of stoichiometry, the transistor can suffer from poor charge control and unsatisfactory transport characteristics.

To determine whether this could be the case in our devices, we have produced sidewall capacitors. These are special-purpose test structures that isolate the charge-control characteristics of the fin sidewalls. This investigation revealed that our digital etch process enhances the electrical quality of the sidewalls. Encouragingly, we also found that with proper treatment, the etched sidewall can produce a minimum interface state density on the order of 3×10^{12} eV^{-1} cm^{-2}. Although this is still on the high side of what is desirable, it is nevertheless a very promising result.

Unfortunately, our study has uncovered an additional concern associated with the use of very thin etched InGaAs fins in finFETs. We found that the electron mobility rapidly degrades when the fin width drops below about 15 nm. We are still to perform a detailed study of this phenomenon, which should not raise eyebrows, given that similar observations have been made in highly scaled, ultra-thin-body silicon SOI-MOSFETs. Note that the implications of our finding may not be as severe as they initially appear, because at these length scales, the electron velocity has far greater impact on device performance than electron mobility.

Producing a high-performance InGaAs finFET is not simply a matter of making a fin with a high aspect ratio and vertical, high-quality sidewalls. Additional features must include low-resistivity ohmic contacts,

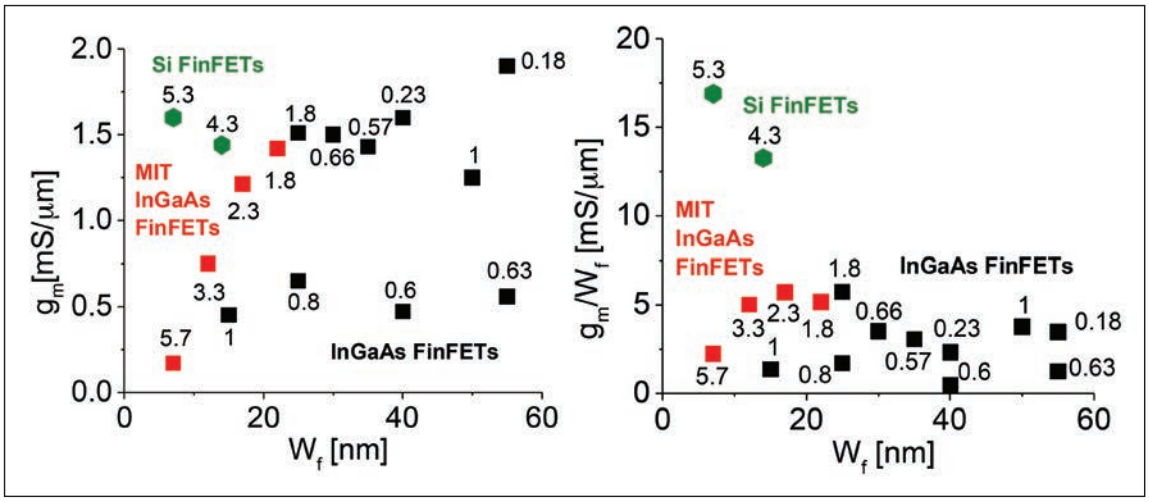


Figure 3. Benchmark of transconductance of InGaAs finFETs. Left: Transconductance normalized by conducting gate periphery. Right: Transconductance normalized by fin width. State-of-the-art silicon finFETs are included for reference. The red squares are recent results from MIT.

a tight self-aligned design and uniform, reproducible characteristics. Bringing all these elements together at the nanometre scale is very challenging, and an honest appraisal of the performance of today's InGaAs finFETs shows that there is still much work to do.

Benchmarking III-V finFETs

One key figure of merit for judging the performance of state-of-the-art transistors is transconductance. This characteristic, which reflects how quickly charge carriers move in the channel, is a critical metric in any transistor application.

We have benchmarked the transconductance of InGaAs finFETs with two different approaches: the conventional approach, which is to normalise transconductance by the conducting gate periphery; and an alternative method, where the same data is normalized by the fin width (see Figure 3). The latter approach makes a great deal of sense, because it relates to transistor density, which, in the end, is what Moore's Law is all about. Both graphs include estimations from selected state-of-the-art silicon finFETs (22 nm and 14 nm CMOS from Intel), along with our recently published results.

Several interesting observations can be made from these graphs. First is the realization that while the latest generation of silicon finFETs already feature fins with a width of less than 10 nm and an aspect ratio in excess of 5, until our most recent results, the narrowest InGaAs finFETs presented in the literature had a fin width of 15 nm and an aspect ratio less than two. So, in reality, the vast majority of InGaAs finFETs are just barely so - in fact, they are almost planar devices! Our benchmarking also reveals that when normalized by conducting gate periphery, the transconductance of the best InGaAs finFETs are almost a match for silicon finFETs. This is in spite of the widely different aspect ratio, and the fact that planar InGaAs MOSFETs have demonstrated a very high transconductance – the current record, which is held by our group, is 3.45 mS/μm.

This discrepancy exposes a noteworthy difference between the silicon finFET and its InGaAs cousin. Sidewall charge control is successful in the silicon finFET, but in the InGaAs finFET it is far less effective. This is clear to see when transconductance is normalized by the fin footprint (see Figure 3 (b)). Normalising in this manner highlights the importance of extracting a lot of current drive out of a tiny transistor footprint, the essence of Moore's Law. When normalized in this way, the gap between silicon finFETs and InGaAs finFETs is clear, indicating that the development of the InGaAs finFET is in its infancy. Included in the benchmarking data are our recent devices results, which we revealed earlier this summer

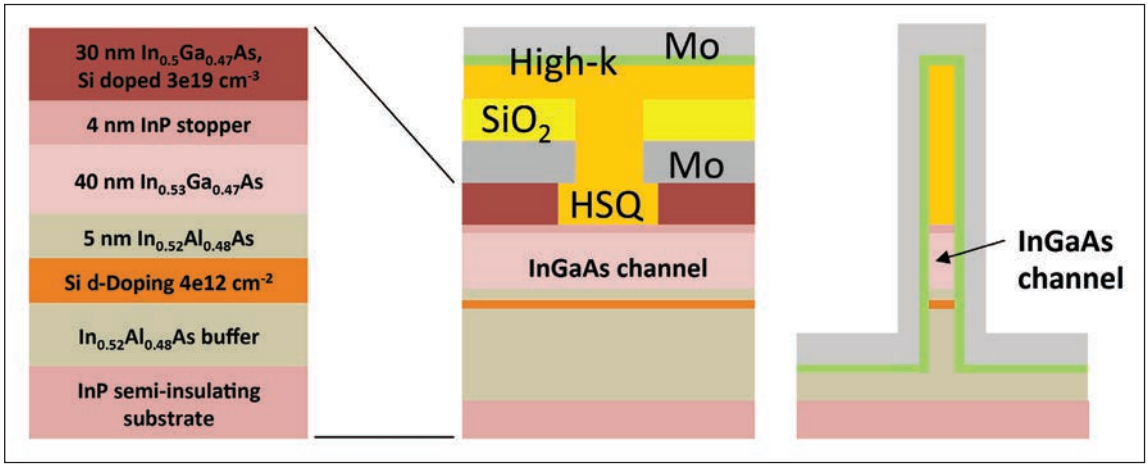


Figure 4. Longitudinal and transversal cross-sections of MIT's InGaAs finFETs.

Book your place at the

CS International Conference

Tuesday 7 & Wednesday 8 March 2017

Sheraton Brussels Airport Hotel, Belgium

Co-located with the 2nd PIC International Conference

Speakers include the leaders of the world's biggest chipmakers and the most promising start-ups.

Presentations include:

- **San'an:** The creation of the biggest LED chipmaker in China
- **Flosfia:** Unleashing the potential of gallium oxide
- **Skyworks:** Front-end architectures for tomorrow's smartphones
- **IBM:** The latest efforts to develop III-V logic

FIVE KEY THEMES:

Over 30 inspiring presentations

- Refining handset architectures for the 2020's
- Perfecting power electronics
- Optimising light emitters
- Revolutionising RF chips
- Exploiting heterogeneous integration

Early Bird Discount!

Book your place before 31 October 2016 and receive a €100 discount.

Register: www.cs-international.net

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry

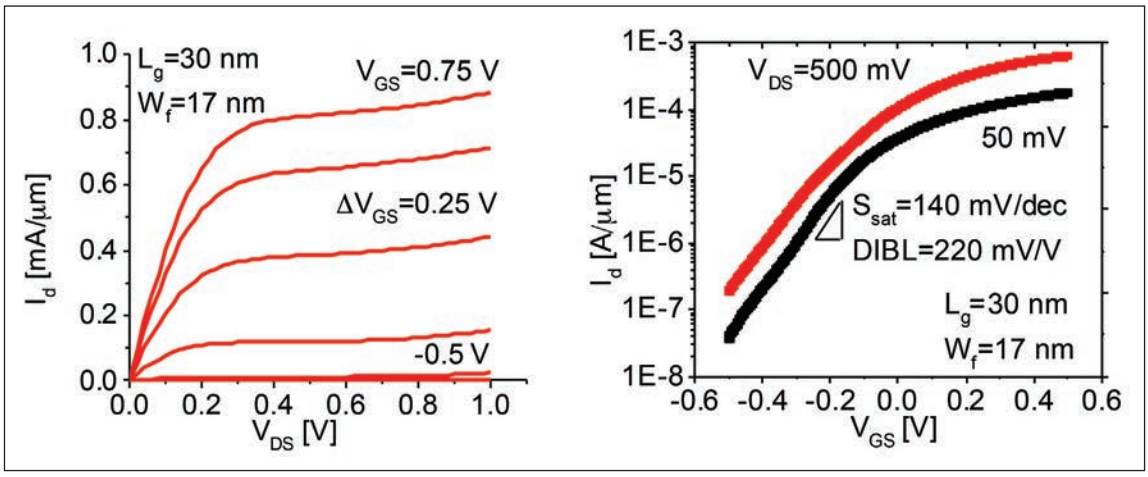


Figure 5. Output characteristics and sub-threshold characteristics of InGaAs finFET made at MIT (W_f=17 nm, L_g=30 nm)

at the VLSI Technology Symposium. These devices have fin widths as narrow as 7 nm, aspect ratios in excess of 5, and gate lengths as short as 20 nm. Although these devices are inferior to state-of-the-art silicon finFETs, the transconductance, when normalized by fin width, is more than 50 percent higher than that of any other InGaAs finFET previously reported. So what is unique about these devices?

For starters, the design of our finFET breaks new ground. Its unique elements include ohmic contacts that are fabricated first, using low-resistivity molybdenum sputtered on the as-grown pristine surface. Our experience with planar InGaAs MOSFETs suggests that this approach yields record contact resistivities in the mid 0.1-1 $\Omega.\mu m^2$ range. Ultimately, values below 0.1 $\Omega.\mu m^2$ will be required.

The fins that we produce are formed by a combination of reactive-ion etching and digital etch. This yields smooth, highly vertical sidewalls. One feature of our process is that the reactive-ion etching mask used to define the fins is left in place. Consequently, after gate stack fabrication through atomic layer deposition of Al_2O_3 and HfO_2 and molybdenum gate sputtering and definition, the resulting device has a double-gate design. This means that the gate modulates only the electron concentration at the sidewalls, rather than also through the top, the situation that occurs in a trigate transistor.

This could be viewed as a deficiency, because the trigate design should provide better electrostatic control and current drive than the double-gate architecture. However, for very thin fins, the theoretical difference is very small. There are also significant upsides to our device geometry: the practical implementation of a trigate MOSFET is much harder, and it demands serious compromises in process and transistor design. Both take their toll, leading to increases in parasitic resistance, capacitance and leakage that impair transistor performance.

We have performed additional electrical characterisation of our finFETs, involving a device with 17 nm wide fins (see Figure 5). This shows that although our devices are record setting, they are still far from what can be accomplished with silicon. Clearly, a lot of work lies ahead of us.

Our research on highly scaled InGaAs finFETs reveals an additional issue of concern, which could impact future manufacturing. Due to strong quantum confinement in very thin fins, there is a steep dependence of the threshold voltage on fin width. This behaviour, which stems from the very low electron effective mass in InGaAs, produces a positive shift in threshold voltage when fin widths decrease below 10 nm. The same trend occurs in silicon finFETs, but in InGaAs the sensitivity of threshold voltage to fin thickness is about four times higher. This greater sensitivity creates a great challenge for process control in a future manufacturing environment.

As we have shown, in the last few years, great progress has been made with the InGaAs finFET. Although its performance is inferior to that of state-of-the-art silicon transistors, that should not be too concerning, as the technology is still rather immature. Given the impressive strides made by planar InGaAs MOSFETs in recent times, there is good reason to believe that there is tremendous, pent-up potential with the InGaAs finFET.

Further reading

J. A. del Alamo Nature **479** 317 (2011)
J. A. del Alamo CS MANTECH, Palm Springs, CA, May 16-19, 2011, pp. 17-22
H. Riel *et. al.* MRS Bulletin **39** 668 (2014)
J. Lin *et. al.* IEEE Electron Dev. Lett. **37** 381 (2016)
X. Zhao *et. al.* IEEE Electron Dev. Lett. **35** 521 (2014)
A. Vardi *et. al.* "High aspect ratio InGaAs FinFETs with sub-20 nm fin width." Symp. VLSI Technology, 2016
A. Vardi *et. al.*"InGaAs Double-Gate Fin-Sidewall MOSFETs." 72nd IEEE Device Research Conference, Santa Barbara, CA, June 22-25, 2014, pp. 219-220
A. Vardi *et. al.* "Quantum-Size Effects in Sub 10 nm Fin Width InGaAs FinFETs." IEEE International Electron Devices Meeting, Washington, D.C., December 6-9, 2015, pp. 807-810
A. Vardi *et. al.*, "Sub-10 nm fin-width self-aligned InGaAs FinFETs." To be published in IEEE Electron Device Lett., September 2016

SEMICON® EUROPA

25–27 OCT 2016, ALPEXPO, GRENOBLE, FRANCE

SEMICON Europa 2016: New Opportunities in a Mature Industry Environment

SEMICON Europa enables companies to reach new audiences and business partners across the European microelectronics industry and from around the world. Connect to the conversations. Connect to opportunities. Connect to new business.

Key Focus Areas/Topics at SEMICON Europa 2016

SEMICONDUCTOR TECHNOLOGY

- 20th Fab Management Forum
- Lithography Session
- Advanced Materials and Processes Session
- Sustainable Manufacturing Session
- Photonics Session
- MEMS Session

PACKAGING AND TEST

- Advanced Packaging Conference
- Integrated Test Sessions

NEW: CO-LOCATION WITH IOT-PLANET

IoT planet® CONNECTING YOUR LIFE!

EXECUTIVE AND MARKET

- Executive Keynotes
- SEMI Market Briefing
- SEMI Gala Dinner
- European Semiconductor Cluster Activities
- CXO Luncheon

2016FLEX EUROPE

2016 FLEX Europe

- Silicon Electronics & Flexible Systems
- Flexible Electrical Components
- Materials Advancements
- Applications and New Developments

APPLICATION & INNOVATION PROGRAMS

- Imaging Conference
- Power Electronics Conference
- MedTech Session
- Automotive Electronics Session
- Innovation Village + Start-up pitches
- What's Next...? Session
- SMART Manufacturing Session

70% of visitors involved in buying decisions

45% of visitors represent engineering job functions

REGISTER NOW!

Contact

Jerome Boutant
Tel: +33 4 56 59 30 58
jboutant@semi.org

ADVANCING WIRELESS WITH THE DIGITAL GaN PA

Digital GaN-based power amplifiers can deliver a revolution in wireless communication infrastructure

BY ANDREAS WENTZEL FROM FBH BERLIN

MANY OF US got our hands on our first mobile phone in the late 1990s. Back then we could make calls, send text messages, and play some very basic games.

In comparison, today's smartphones are incredibly powerful devices. In addition to calling and texting, they can take pictures and video, send e-mails, open documents and surf the web – and the price for doing all of this compares very favourably with the tariffs of yesteryear.

The foundation underpinning this evolution in the bang-per-buck provided by the mobile is an ever-advancing wireless infrastructure. It supports, in a cost-effective manner, higher transmission rates and increases in data traffic.

To continue to accommodate the growth in wireless traffic throughout the 2020s and beyond, there will be further changes to networks. They will have a denser spatial distribution, with greater deployment of smaller base stations, such as picocells and femtocells; and they will increase bandwidth by exploiting spatial diversity – with multiple-in, multiple-out transmissions. In addition, the transmitter amplifier will be integrated into the antenna to increase compactness and improve energy efficiency, via a reduction in cable losses. And to top it all, hardware components will support multi-band, multi-mode operation (MIMO) to deliver frequency and service agility.

However, just increasing data rates is not good enough. A major issue is base station inefficiency, which is a major contributor to the higher levels of energy consumption in wireless communication. This stands in the way of demands for a 'green IT'.

Today's mobile base station architectures for 3G and the first 4G are moving in the right direction, as there are requirements for a higher efficiency for the RF PA, as well as the needs for an output power of more than 100 W and a speed in

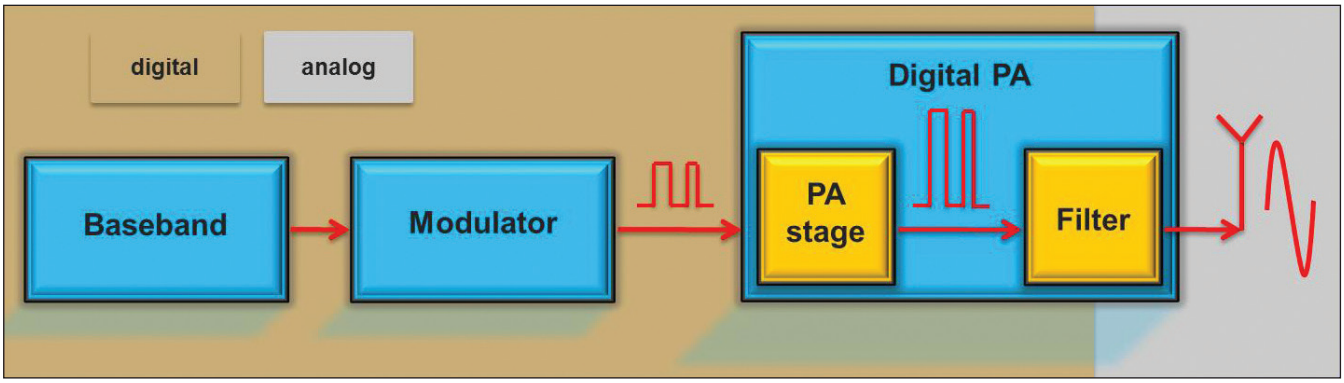


Figure 1.Digital transmitter concept, including modulator, (digital) PA stage and filter.

excess of 2 GHz. The good news is that GaN is now fulfilling these requirements in real systems, thanks to progress in semiconductor technology and PA design.

However, it is not clear how sales of GaN PAs will fare when delivering the move toward distributed power in MIMO systems for 4G and 5G communication, and the associated increase in picocell and femtocell deployment. Critics argue that GaN devices are pricey, particularly when formed on a SiC substrate, and savings can be made with SiGe, silicon-BiCMOS and even GaAs technologies. These are cheaper, and they offer a high level of integration.

However, silicon-based millimetre-wave PAs suffer from a low power density, an inferior efficiency and larger parasitics. When judged in these terms, GaN has the upper hand. What's more, it has reached a level of maturity where it is possible to reliably fabricate larger designs with a higher level of integration. For these reasons, our team at FBH Berlin is investigating potential applications of GaN in future wireless networks, especially for smaller cells.

Base station woes

High levels of operating loss in base station PAs are compounded by the need to satisfy increasing bandwidth requirements in modern communication standards, such as 4G and 5G. This means that the amplifiers are operated well below their full-scale input power – typical values for power back-off are 6 dB or 12 dB. Consequently, for common analogue PAs optimised for maximum input power, the energy efficiency drops below 10 percent, with efficiency values for the whole base station being even smaller.

Due to the high total power consumption of base stations, interest is growing in novel system concepts for next-generation communication infrastructure that combine improved efficiency at power back-off with very high modulation bandwidths.

Of these designs, the most disruptive is that of our digital transmitter (see Figure 1). We have been developing GaN-based digital PAs, a technology that is well very known within the audio industry, for almost a decade. Now this digital GaN PA is piquing interest in the mobile communications sector.

With our approach, a digital baseband signal feeds the modulator, which generates the input voltage bit sequence to the digital PA. The digital input signal is amplified by a highly efficient PA switching stage, and the analogue filter at the output reconstructs the wanted signal.

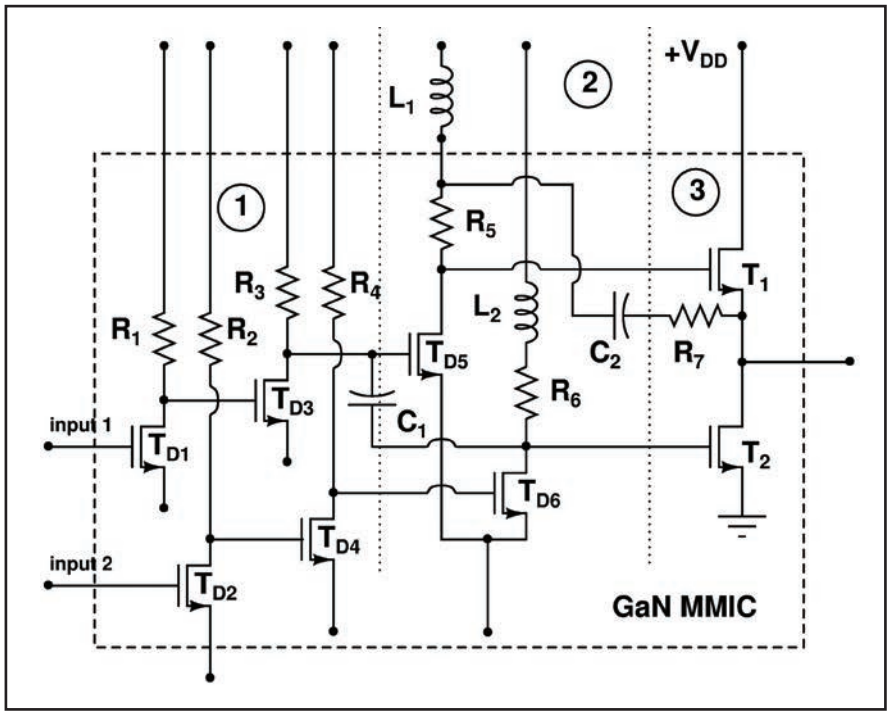


Figure 2. Circuit schematic of a four-stage digital PA building block in push-pull configuration ($T_{1/2}$) and realised H-bridge digital PA module (top right, next page; area: 68 x 42 x 15 mm³). Two preamplifiers in source configuration (1) amplify the very small input voltage swing of 0.5 V_{pp} only, which feeds the input of the differential PA (2). This part generates the different voltage swings for the final-stage transistors (3).

A great strength of this technology is that a very high power-added efficiency can be realised independently of the power back-off level. Losses are low, thanks to GaN HEMTs only being in either the on-state or the off-state. There is also a high degree of flexibility, because a broadband approach eliminates the requirement for narrowband impedance matching techniques, which are found in the likes of class AB and class E amplifiers.

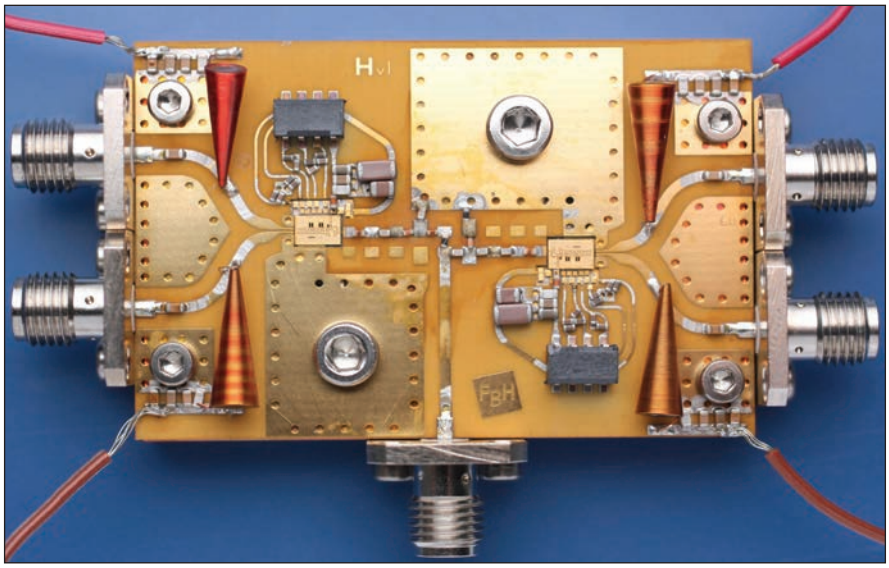
GaN has several great attributes for a digital PA. It can form very fast, broadband transistors that are needed to cater for applied advanced modulation schemes, which may include frequency components down to kHz and up to several GHz, depending on the signal frequency encoded. The devices can also combine high speed with a low output capacitance for a given current.

We have made major contributions towards establishing the digital approach in mobile communications. Our successes include, in collaboration with NEC Corp. in Japan, the world's first digital transmitter for a 450 MHz signal frequency.

One of our key findings is that the final-stage configuration with the highest potential is the voltage-switching, push-pull approach. Unfortunately, complementary GaN HEMTs for the efficient driving of the final-stage are not available. So, working within this restriction, we have built a module with our 0.25 µm GaN-HEMT process (see Figure 2 (a) for a typical circuit diagram, and 2 (b) for the corresponding module).

This module features a pair of preamplifiers in source configuration that amplify the very small input voltage swing – it is just a TTL-level input voltage swing of 0.5 V_{pp}. The amplified signal is fed into the input of the differential PA, which generates swings for final-stage transistors. Combining this PA with an off-chip, 800 MHz band-pass filter has enabled us to set a new benchmark for the microwave amplification with a digital approach: a maximum power-added efficiency of 60 percent. This PA also produces a very high power gain of 40 dB.

One of the great strengths of the digital power amplifier is that it provides a versatile building block with multi-band



capability. Currently, the only suitable candidates for the core amplifier of such a digital PA are those of the class-D/S type. These essentially act as power switches.

We have used our latest generation of GaN MMICs as building blocks for the construction of various power amplifier modules with increased digital content. They include the first tri-band amplifier of class-S type for the 0.8/1.8/2.6 GHz band, and an H-bridge and a single-chip class-D/S PA for the 800 MHz band. Our portfolio of digital amplifiers has a maximum output power of 14 W and final-stage drain efficiency of up to 90 percent.

Although full-scale output powers in the 10 W-range are insufficient for today's macrocell base stations, they are more than adequate for smaller cells, such as picocells and femtocells.

Moreover, by applying a digital Doherty operation to the H-bridge PA enables final-stage drain efficiencies of 75 percent at power back-off levels of 6 dB, and 40 percent at 12 dB.

These results demonstrate the benefits of the digital PA for realising a range of circuits with the same IC, formed with changes that just involve the periphery. The high flexibility and compactness of the circuits, combined with the performance of our digital power amplifiers, demonstrates that our technology is a very promising candidate for inclusion in picocells and femtocells for next-generation mobile communication infrastructure.

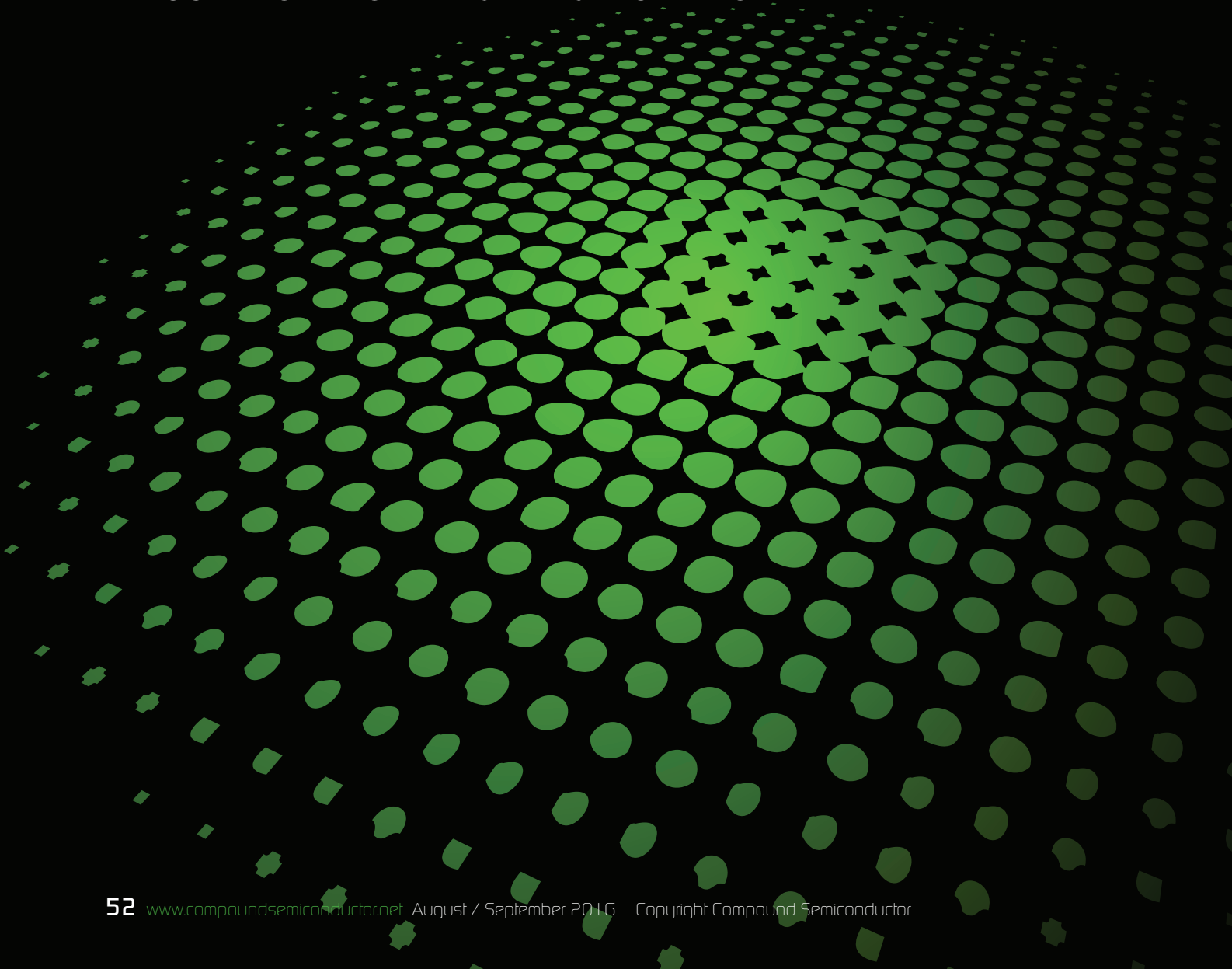
Further reading

A. Wentzel *et. al.* "RF Class-S Power Amplifiers: State-of-the-Art Results and Potential", IEEE MTT-S International Microwave Symposium Digest 2010, pp. 812–815, Anaheim, USA.
A. Wentzel *et. al.* Int. J. Microw. Wirel. T. **3** 311 (2011)
A. Wentzel *et. al.* "Envelope Delta-Sigma Modulated Voltage-Mode Class-S PA", Proceedings of the 42nd European Microwave Conference 2012, pp. 120-123, Amsterdam, The Netherlands.
A. Wentzel *et. al.* "A GaN Voltage-Mode Class-D MMIC with Improved Overall Efficiency for Future RRH Applications", Proceedings of the 43rd European Microwave Conference 2013, pp. 549-552, Nuremberg, Germany.
A. Wentzel *et. al.* "A Flexible GaN MMIC Enabling Digital Power Amplifiers for the Future Wireless Infrastructure", IEEE MTT-S International Microwave Symposium Digest 2015, TH2B-5, Phoenix, USA.
A. Wentzel *et. al.* "A Compact Tri-Band Voltage-Mode Class-D/S PA for Future 0.8/1.8/2.6 GHz LTE Picocell Applications", Proceedings of the 45th European Microwave Conference (EuMC) 2015, pp. 1160 - 1163, Paris, France.

UNCOVERING THE ORIGIN OF THERMAL DROOP

At high temperatures LED losses increase due to a rise in defect-enhanced carrier escape

BY CARLO DE SANTI, MATTEO MENEGHINI, GAUDENZIO MENEGHESSO AND ENRICO ZANONI FROM THE UNIVERSITY OF PADOVA



GaN-BASED LEDs are rapidly increasing their share of the lighting market. And this trend should continue, so long as LED lighting becomes even more appealing by retailing for less and offering even higher efficiencies.

One option for trimming the cost of solid-state lighting is to drive LEDs at higher current densities, because this slashes the semiconductor content in the lighting unit. But this approach does not deliver as great a benefit as might first appear due to a mysterious malady known as efficiency droop, which causes a decline in the efficiency of the LED at higher bias. In some applications, this energy-sapping mechanism is so severe that it has motivated a move to droop-free, laser-based lighting, even though the complexity of these systems is higher.

Efforts to understand the decline in LED output when the device is driven at higher current densities have focused on the efficiency droop. But there is also a reduction in optical power at higher temperatures, a phenomenon known as thermal droop. It is being investigated by our team at the University of Padova. Understand its cause, and an improvement in the overall efficiency of GaN-based lighting systems could follow.

The aims of our work are not actually limited to highlighting the strong effect of thermal droop in real applications. In addition, we are keen to: underline the importance of standardized measurement conditions, which will aid comparisons between different devices; provide technical solutions; and increase the performance of end-user products.

Surveying the LED

We have surveyed the temperature-dependent behaviour of high-performance green LEDs produced by every major manufacturer. This has revealed that under nominal operating conditions thermal droop always exceeds 10 percent (see Figure 1). Its magnitude is only slightly less than that of the efficiency droop, and it also plagues laser-based lighting systems, because temperature influences a laser diode's threshold current and its slope efficiency.

Note that the data in Figure 1 is not intended to provide a comparison of the overall quality of LEDs grown by different chipmakers. For this reason, the manufacturers are not disclosed, but blindly represented, using letters "A" to "G". As optical power losses have been extrapolated from datasheets of specific LED models, they lack statistical relevance. Moreover, even though all models under analysis are high-power green LEDs, the nominal operating current and maximum rated junction temperature vary, as

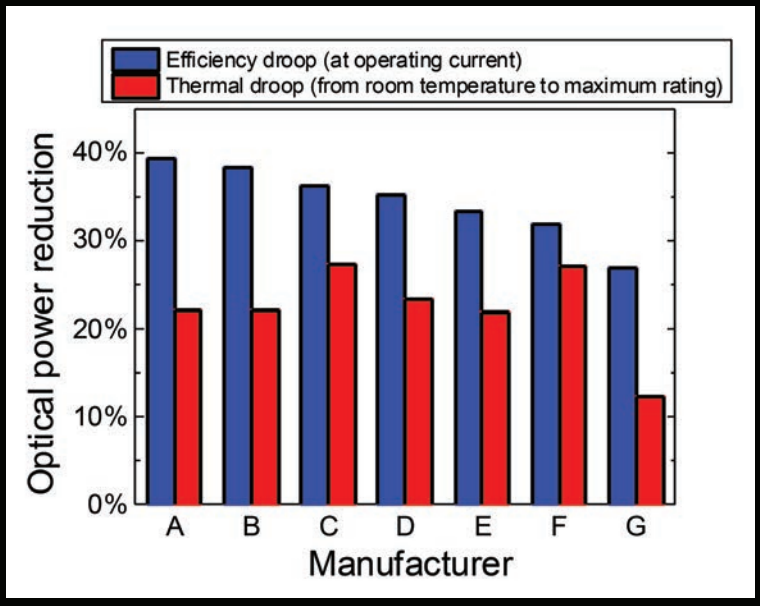


Figure 1: Efficiency droop and thermal droop vary significantly between high-power green LEDs produced by different manufacturers (data extracted from datasheets). Note that this figure does not allow for absolute chip quality comparison between manufacturers, since (i) it refers to only one LED model and (ii) the measurement conditions in every datasheet are different.

does the bias for measurements of thermal droop. Experiments by our team have uncovered a correlation between the extent of thermal droop in the LED and its defect density, evaluated by capacitance deep-level transient spectroscopy. It is well known that defect-related, Shockley-Read-Hall non-radiative recombination is enhanced by temperature. But could this explain our experimentally-detected variations in the optical power of the LEDs? To determine whether it is a possible explanation, we ran computer-aided numerical simulations to estimate the possible impact of this process. Our conclusion: Shockley-Read-Hall recombination fails to account for the entire experimental reduction in optical power (see Figure 2).

To confirm that Shockley-Read-Hall recombination cannot, in itself, account for thermal droop in these devices, we carried out some additional tests. It is possible to increase Shockley-Read-Hall recombination using an aging test methodology that creates new defects inside the active region. For this reason, we measured the variation in the thermal droop with stress time, observing a decrease in photoluminescence intensity from the quantum well, which is a clear indication of a higher concentration of defects caused by stress. We were even able to directly measure an increase in the Shockley-Read-Hall recombination with differential

lifetime measurements. Surprisingly, we found that increases in non-radiative recombination had no impact on thermal droop, which remained constant over the whole test. So, clearly, a different mechanism accounts for thermal droop.

One of the key findings from other groups that have studied the role temperature plays in LED efficiency is that when electron-blocking layers are thicker, or improved, they cut thermal droop. This observation suggests that carrier escape from the quantum well may be the origin of thermal droop. However, before this contender is to be taken seriously, there is a need to clarify the actual physical process, and to understand why defect density has a strong impact.

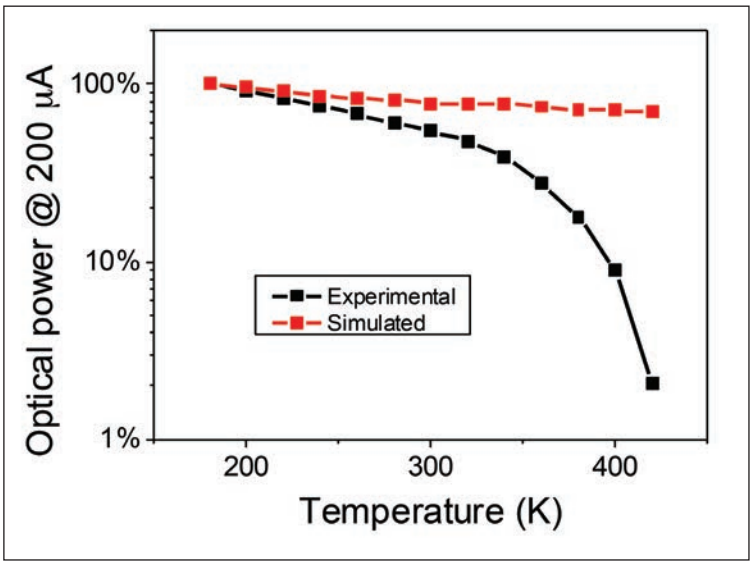


Figure 2: The experimental reduction of the optical power with increasing temperature cannot be fitted with a model based on just Shockley-Read-Hall recombination, so this mechanism alone is unable to account for thermal droop.

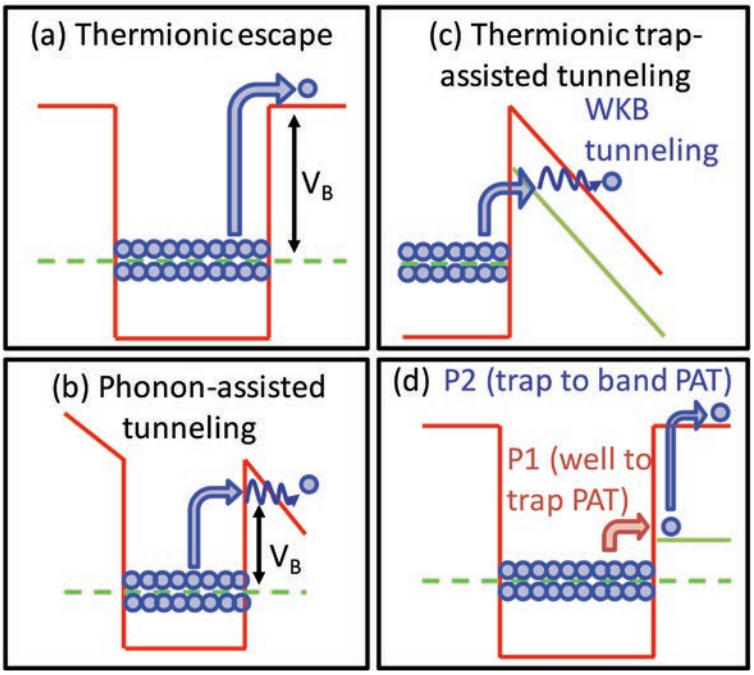


Figure 3: Sketches of different temperature-dependent escape processes: (a) pure thermionic escape, (b) phonon-assisted tunnelling (PAT), (c) thermionic trap-assisted tunnelling (TTAT) and (d) the suggested extended thermionic trap-assisted tunnelling (ETTAT). The confining potential barrier is denoted V_B.

A choice of models

Within the scientific literature there are several possible models for this mechanism, including: pure thermionic escape, phonon-assisted tunnelling, and thermionic trap-assisted tunnelling. A pictorial representation of all three, plus our own model, is provided in Figure 3.

The pure thermionic escape model is based on the idea that the average energy of the electrons inside the quantum well increases with temperature, with some escaping by overcoming the confining potential barrier. With this model, higher temperatures lead to a lower electron concentration in the quantum well, and therefore a lower optical power. But this model has some weaknesses. Significantly, it offers no correlation with the defect density, which is needed to explain our whole available dataset. What's more, the modelling of the electron fails to consider its wave-like nature, which can allow it to tunnel outside the quantum well.

An improvement is the phonon-assisted tunnelling model, which provides a better description of the quantum behaviour of the electron. Again, higher temperatures increase the average electron energy, but this time electrons are allowed to tunnel out of the quantum well and through the potential barrier to reach the conduction band. Higher temperatures and stronger electric fields enhance this process. However, this model still fails to account for the impact of defect density on thermal droop.

With the thermionic trap-assisted tunnelling model, defects provide a limiting element for the escape rate. In this case, every electron exits the quantum well via a two-step process. First, it is promoted from the quantum well to a defect located at an energetic position between the quantum well and the conduction band. The likelihood that an electron is promoted increases with temperature and the strength of the electric field. The second step involves the tunnelling of the electron from the intermediate deep level to the border of the conduction band. This is a purely field-assisted tunnelling process, according to the Wentzel-Kramers-Brillouin (WKB) approximation, and is independent of temperature.

A very important feature of this model is the intermediate deep level, which acts as an electron reservoir to the second part of the process. This intermediate level limits the escape rate and allows defects to influence device behaviour. However, since the second step of the process is not thermally-assisted, even this model is not capable of reproducing the experimental behaviour.

To include the effects of temperature and defect

density on LED behaviour, we have developed a new model, called extended thermionic trap-assisted tunnelling. It includes the influence of the intermediate deep level, which appears in the thermionic trap-assisted tunnelling model. However, we use a completely new analytical formulation of the two steps of the process: the equations for thermionic trap-assisted tunnelling are discarded, and replaced with those based on phonon-assisted tunnelling. These new equations include the role of thermal emission at zero bias – that is, pure thermal emission that is not field-assisted – whose importance is stated but not computed in the original formulation.

The basic idea behind our model is that electrons inside the quantum well increase their energy with temperature, via interaction with phonons, and then tunnel towards an intermediate deep level under the influence of a local electric field (shown as P1 in Figure 3 (d)). Once inside the deep level, the same process can move electrons to the conduction band (see P2 in Figure 3 (d)). The upshot is the loss of one electron from the quantum well, and therefore one photon from the output optical power.

With our model, the loss of optical power is proportional to the density of the intermediate deep level. This occurs because the greater the density of defects, the greater the number of destination states for each electron, and the greater the number of electrons that are removed from the quantum well. The second part of the process is needed to remove the electrons from the deep level. Without this step, electrons would fill up the deep level until no more could be removed from the well, leading to the absence of a reduction in optical power.

A simple electrical model allows us to understand the impact of this process on the optical power. Let's imagine it as a current leakage path shunting the quantum wells. The maximum current that can flow through this path is fixed, since it corresponds to the maximum number of electrons that can travel through the intermediate deep level. It is also known that the maximum current is proportional to the defect density. With this model, part of the bias current is drained by the shunt path, leading to a reduction in optical power that is proportional to defect density and temperature.

One virtue of this model is that it predicts an additional feature of the thermal droop mechanism: it should be stronger at a lower bias current, because the proportion of the bias current leaked by the escape process is higher. Experimental data follow this trend: comparing the optical power data in Figure 2 and Figure 4 reveals that the detected thermal droop has a higher impact under low bias.

We have used this last mechanism to model our experimental data. Carrying out these calculations correctly requires a great deal of knowledge about the active region, including the activation energy of the deep level, the position of the lowest allowed electron energy level inside the quantum well, the phonon energy, the Huang-Rhys factor and the electron effective mass. We have obtained some of these values with experimental measurements: capacitance deep-level transient spectroscopy has revealed the deep-level activation energy; and values for phonon energy, and for the Huang-Rhys factor, have been determined from electroluminescence spectra at 83 K. Meanwhile, the energetic structure inside the quantum well has been computed by numerical simulations, and the electron effective mass has been estimated from a critical analysis of the literature. With our model, the main fitting parameter is the strength of the electric field inside the quantum well, because its estimate or computation is not straightforward.

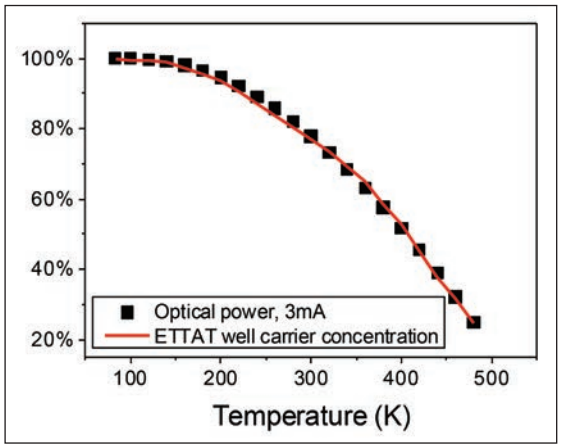


Figure 4: The extended thermionic trap-assisted tunnelling model developed by the team from the University of Padova can provide a good fit to the experimental data.

The results of our efforts show that our model is able to fully reproduce the experimental behaviour of the LED (see Figure 4). The implication is that device efficiency is significantly influenced by carrier escape.

We believe that our work offers a new insight into the role of carrier escape on device efficiency. Our findings may prove invaluable in designing new devices and luminaires for droop-free lighting applications, even when they involve the use of lasers.

The authors would like to thank Marco La Grassa from the University of Padova and Michele Goano, Stefano Dominici, Marco Mandurrino and Francesco Bertazzi from Politecnico di Torino for their contribution in the research in this field. The authors also thank Bastian Galler and Roland Zeisel from Osram Opto Semiconductors for contributions to the discussion.

Further reading

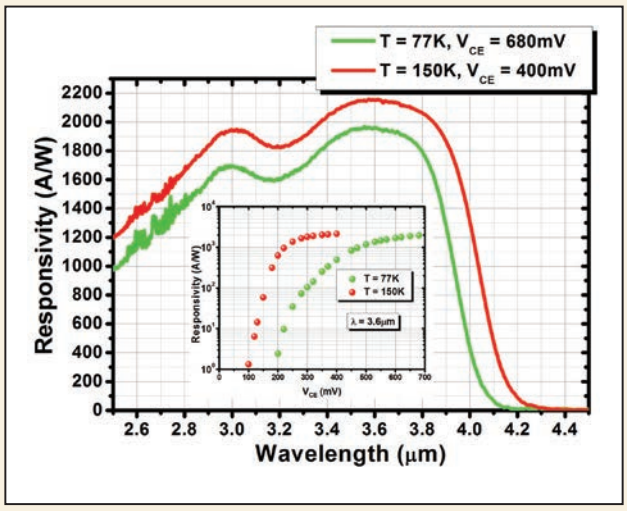
C. De Santi *et. al.* J. Appl. Phys. **119** 094501 (2016)
C. Huh *et. al.* Electrochem. Solid State Lett. **7** G266 (2004),
K. S. Kim *et. al.* Appl. Phys. Lett. **96** 091104 (2010)
K. T. Lam *et. al.* J. Display Technol. **10** 1078 (2014),
D. Pons *et. al.* Journal of Physics France **40** 1161 (1979)
D. M. Sathaiya *et. al.* J. of Appl. Phys. **99** 093701 (2006

Phototransistor targets free-space communication

Producing an optical gain of more than 600, a type-II mid-infrared phototransistor shows promise for free-space communication

RESEARCHERS at Northwestern University, Illinois, have fabricated an infrared type-II phototransistor with impressive characteristics, including a specific detectivity four times that of a comparable photodiode.

The team's phototransistor, which when cooled can deliver an optical gain of more than 600 at 4 μm, is a promising candidate for laser-based, free-space optical communication networks. This optical technology could divert traffic from fibre-optic networks by providing alternative links over distances of up to a mile.



Front-side illumination of devices that do not include an anti-reflection coating shows that responsivity saturates at around 3.9 μm.

"The main selling point of [free-space optical communication] is that you don't need to allocate any RF bandwidth, which is really precious in crowded areas," explains team-leader Manijeh Razeghi. What's more, unlike WiFi networks, free-space optical communication can provide inherently secure links for users requiring a high degree of security, such as financial institutions.

Ideally, this optical communication technology should avoid near infrared wavelengths between 800 nm and 2 μm, due to concerns related to eye safety – they are associated with the need for high-power laser sources. The phototransistor produced by Razeghi's team adheres to this by operating within the mid-wavelength infrared region, which spans 3 μm to 5 μm. This spectral range is very attractive for free-space optical communication, because atmospheric scattering and absorption are relatively weak at these wavelengths.

One weakness of the type-II phototransistor produced at Northwestern University is that it requires cooling, which adds cost. "However, recent improvements in manufacturing micro-coolers have brought down the cost of these coolers, as well as expanding their lifetime," argues Razeghi.

The class of device that Razeghi and co-workers are developing, the heterojunction phototransistor, is a variant of the HBT. The phototransistor was once considered for fast detection in the near infrared, but success did not follow, due to difficulties associated with uncovering a suitable material combination for that spectral range.

"Thanks to type-II superlattices, we revisited the heterostructure phototransistor and gave it another chance to prove itself as an excellent candidate for high-speed infrared detection in the mid-wavelength and long-wavelength infrared regime," explains Razeghi.

She believes that the greatest significance of her team's work is the construction of a heterojunction bipolar transistor made entirely from a type-II superlattice. This approach delivers a great deal of freedom by allowing the selection of different bandgap energies for the different sections of the transistor, and the opportunity to tune the bandgap offset between them.

"All these tunings can be done while the hole structure is lattice-matched to the GaSb substrate," enthuses Razeghi.

The team's MBE-grown detector combines an *n*-type, wide bandgap emitter with a *p*-type base and a lightly doped *n*-type collector that are both based on a type-II superlattice. The emitter is based on periods of InAs/GaSb/AlSb/GaSb with 7, 1, 5 and 1 mono-layers, respectively; and the base and collector have a similar structure, but with each period featuring 6.5 monolayers of InAs and 12 monolayers of GaSb.

Phototransistors were formed with standard photolithographic techniques for type-II superlattice photodetectors. Measurements revealed peak responsivity of more than 2000 A/W at 150 K (see Figure for details). At 77 K, optical gain reached unity at a 200 mV applied bias, and increased with voltage to saturate at 668 at around 600 mV. Meanwhile, at 150 K, optical gain hit unity at 110 mV, and saturated at 639 at 350 meV.

One of the targets for the team is to measure the speed of their device. "Evidence from other experiments suggests that we can expect a gigahertz range," says Razeghi.

Other goals include producing phototransistors for longer wavelengths, increasing the speed of the device through refinements to chip design and processing, and developing dual-band detectors for wavelength-division multiplexing.

A. Haddadi *et. al.*
Appl. Phys. Lett. **109** 021107 (2016)

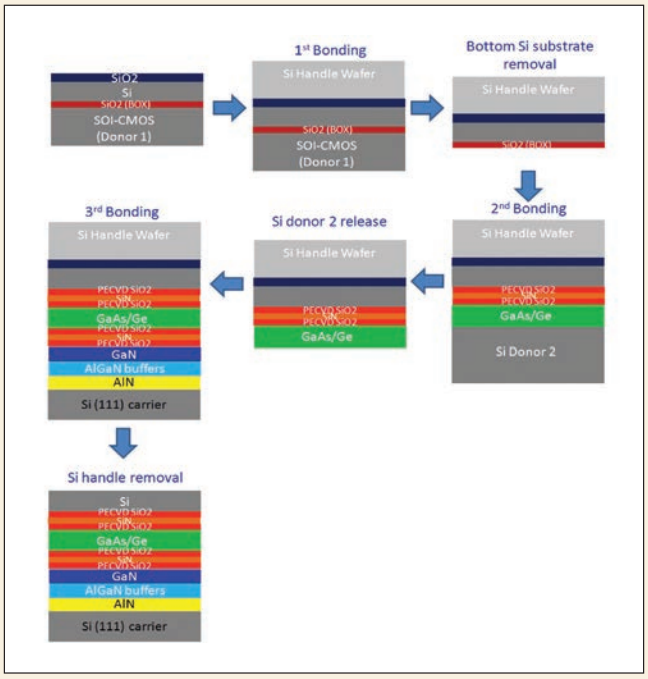
Integrating nitrides and arsenides with silicon CMOS

Wafer bonding combines GaAs and GaN layers and silicon CMOS on a 200 mm silicon wafer

A US-SINGAPORE partnership has set a new benchmark for the integration of different semiconductor materials. It has used wafer bonding to unite GaAs, GaN and silicon CMOS on a 200 mm silicon substrate.

This effort surpasses the previous best by this team from the Singapore-MIT Alliance for Research and Technology – the integration of silicon CMOS and either GaAs/silicon or GaN/silicon on a 200 mm platform.

Lead author of the paper describing the recent breakthrough, Kwang Hong Lee, believes that the greatest significance of the work is that it enables the opportunity to combine the best functionalities of different materials on a silicon CMOS design platform.



Engineers at the Singapore-MIT Alliance for Research and Technology produce wafers that combine GaN, GaAs and silicon CMOS on 200 mm silicon using a triple-bond layer transfer process.

"Hence, high-frequency InGaAs HEMTs, high-power GaN amplifiers and inexpensive silicon digital control circuitry can be combined into a single platform," claims Lee.

Four of the benefits of uniting these materials on a single platform are: cutting the number of packages at the board level, which could enable the likes of a single-chip RF front-end; a drastic reduction in power consumption, which could aid developments in products for 5G wireless; lower costs, thanks to smaller chip footprints; and the introduction of novel IC designs, such as envelope tracking.

"In addition, non-phosphor, full-colour active-matrix displays can be realised by combining InGaP LEDs, InGaN LEDs and silicon CMOS driver circuits," says Lee. These displays could feature in smart lighting, where they combine illumination with light-based communication, and they could also be used in the production of wearable devices.

The wafer-bonding approach employed by the team to unite materials has a major advantage over direct epitaxial growth: it is carried out at room temperature. This prevents degradation to CMOS transistors that would occur during the growth of GaN at temperatures of typically 1350 °C, and the growth of arsenides and phosphides at 650 °C.

Lee and co-workers unite wafers using plasma-activated fusion-bonding. This is carried out at atmospheric pressure, is compatible with CMOS processing, and has a relatively high degree of tolerance with mismatches in the coefficients of thermal expansion. What's more, it is suitable for use in foundries because it just involves a few low-cost steps – and it is already widely used today for the production of silicon-on-insulator wafers.

To form the multi-material hybrid wafer, the team prepare four sets of wafers: a silicon handle; a silicon-on-insulator wafer; a GaAs/germanium/silicon donor; and a GaN-on-silicon carrier. For the donor, germanium and GaAs are directly grown on silicon. Formation of the SOI-GaAs/germanium/GaN/silicon structure requires a series of seven steps, including three bonding processes and the removal of the silicon substrate, the silicon donor and the silicon handle (see Figure).

The team assessed interface quality of these multi-material wafers with an infrared camera. Inspection uncovered unbounded areas caused by particles on the wafer surface.

According to Lee, particle issues are more prevalent in a research environment than a foundry: "Modern wafer-bonding equipment minimise particles, due to reduced human handling, controlled clean environments and *in-situ* cleaning."

Wafers produced by the team contain bonding layers that are about 500 nm thick, and GaAs and GaN layers buried several microns beneath the surface. The thickness of all these layers can be varied, with Lee claiming that, in principle, the bonding dielectric can be as thin as 100 nm.

One of the plans for the team is to switch the order of their process, fabricating devices on the III-V-on-silicon wafer first, and then bonding wafers with an aligner. "In addition to integrating devices in this fashion," says Lee, "we will try to integrate batteries, solar cells and other electronic devices, to realise a complete electronic system on a common silicon platform."

K. H. Lee *et. al.*
Appl. Phys. Express **9** 086501 (2016)

Dual layer ITO boosts LED brightness

Varying the angle between the ITO source and the wafer leads to a significant increase in LED output power

ENGINEERS from South Korea have increased the intensity of LED electroluminescence by one-fifth by switching from a single layer of ITO to a pair of these layers.

The team from Gwanju Institute of Science and Technology (GIST) formed the dual layer of transparent, conductive ITO by depositing a layer at normal incidence, adjusting the angle of the sample and then adding a second layer. Optimising the thickness of both layers, which have significantly different refractive indices, lowered reflectivity. This increases LED output by reducing the proportion of the light generated within the active region that is reflected back into this section of the device.

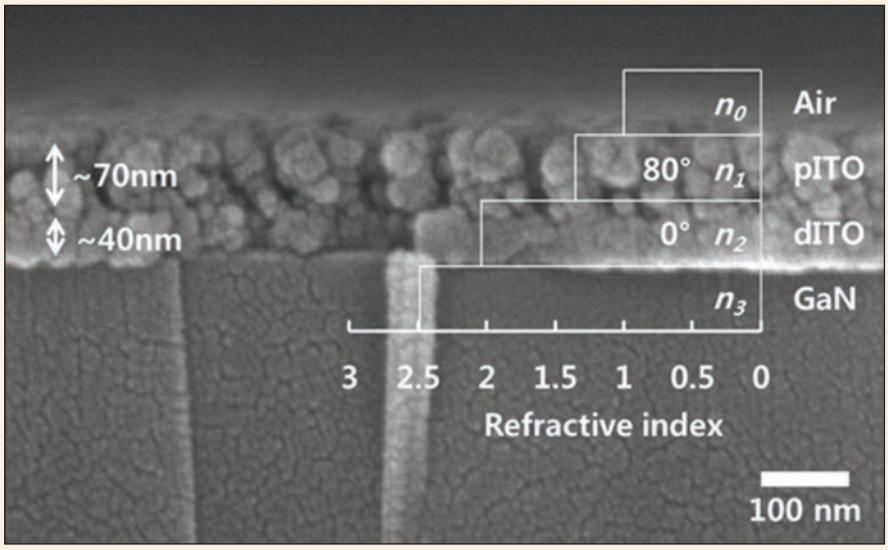
Low reflectance at a broad wavelength range can also be realised by nano-texturing with a sub-wavelength scale. "[But] this approach requires more complex fabrication procedures," says Dong-Seon Lee from GIST.

Lee believes that the simplicity of the dual-layer ITO approach makes it suitable for use in high-volume manufacturing. Layers can either be deposited in one growth tool, or using separate tools for growth of ITO at different angles.

The team from GIST demonstrated the benefit of their dual layer approach by fabricating an LED with this structure, and comparing its performance with that of a conventional device with a single layer of ITO. Both variants were formed by growth on typical GaN-on-sapphire LED structures. "We bought commercialised epiwafers without an ITO layer," explains Lee.

On these wafers, Lee and co-worker Dong-Ju Seo deposited a 40 nm-thick film of dense ITO by electron-beam evaporation. They then adjusted the wafer in the chamber so that it formed an oblique angle of 80°, before adding a 70 nm-thick film of porous ITO.

The researchers completed device fabrication by annealing their samples under atmospheric pressure at 600 °C for 5 minutes, and then adding a metal contact. It comprised a 30 nm-thick layer of chromium and 300 nm of gold.



LED output increases with dual layer ITO, due to destructive interference that results in a significant cut in reflectance.

Adjusting the deposition angle of the ITO produced a significant change in refractive index. At 450 nm, the target wavelength for minimal reflection, the conventional ITO had a refractive index of 2.0, while that deposited at the oblique angel had a refractive index of 1.35. The engineers from GIST measured the reflectance produced by the pair of ITO layers. At 450 nm, it was about 3 percent, while that for a standard, 200 nm-thick ITO film was more than 15 percent.

To determine whether the lower reflectance led to a superior LED performance, Lee and Seo compared the current-voltage and electroluminescence characteristics of both types of device. Driven at 3 V, the current in both devices was similar – 26.0 mA for the standard device and 27.1 mA for the LED with the dual layer of ITO.

However, driven at 20 mA, the device with two ITO layers produced an electroluminescence intensity 19.7 percent higher than that of the control. This is attributed to a reduction in reflectance of more than 13 percent, which stems from destructive interference in the thickness-optimised ITO composite.

The Korean researchers also studied the impact of using just one of the thinner, single layers of ITO employed in the high-performance LED. In both cases, reflectance at 450 nm is lower than that for the 200 nm ITO film: for 40 nm-thick, dense ITO it is about 10.5 percent; and for 70 nm-thick porous ITO it is about 7.5 percent.

Unfortunately, electrical performance is compromised in both of these thinner films. The device with the 40 nm-thick ITO has a higher resistance than both the dual layer device and the control with the 200 nm-thick ITO, while the device with the 70 nm-thick layer of porous ITO produces an even poorer electrical performance, due to a lower conductivity that originates from the porous nature of the film.

Lee says that the next goal is to study dual-layer transparent conductive layers that include dielectric materials, such as SiO_2 and SiN.

D. -J. Seo *et. al.*
Appl. Phys. Express **9** 082103 (2016)

Reasons to sponsor CS International Conference 2017

- ✓ Senior management networking opportunities
- ✓ Increased company and brand awareness
- ✓ Access to the top strategists within the compound semiconductor industry
- ✓ Create, develop and support customer relationships
- ✓ Engage in debate, share insight and expertise on industry challenges
- ✓ Gain visibility and recognition as an industry leader
- ✓ Leverage exposure in multiple industry media
- ✓ Demonstrate market innovation and leadership by launching new services, products and systems



www.cs-international.net

CALL NOW +44 (0)24 76718970

email **event@cs-international.net** or view the online sponsorship pack at **mediapack.cs-international.net**

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry

PIC INTERNATIONAL CONFERENCE

Creating and strengthening links between chipmakers and network builders

2nd PIC International Conference

SPEAKERS ANNOUNCED!

PIC International 2017 will provide timely, comprehensive coverage of every important sector within the Photonic integrated circuits industry.

Sales of PICs are soaring, with their deployment helping to boost the capacity of networks and data centres. To aid this industry, we are strengthening the relationships between the makers and the users of these integrated circuits by organising the 2nd PIC International, a global conference dedicated to this industry.

In 2017, the conference grows to a new auditorium to welcome more industry leaders and rising stars driving the next generation of Photonic integrated circuits.

Key themes include a deep dive into PIC platforms, manufacturing solutions, device deployment in data centres, telecoms and a full update on activity in emerging markets such as life sciences.

“Over two days, PIC International gives you an incredibly valuable perspective on what it takes to realise the benefits of integrated optoelectronic devices, and I think that’s why this conference has captured the imagination of the photonics community, ” added James Tyrrell, programme manager for the 2017 show. Just like in 2016, the event is co-located with CS International to bring you the best of the compound semiconductor industry. Also, we’ve matched the scheduling to make it even easier for delegates to jump between tracks and pick the speaker sessions that suit you best.

Early bird discount
Book your place before 30.11.2016 and receive a €100 discount.

Just like in 2016, the event is co-located with CS International to bring you the best of the compound semiconductor industry. Also, we’ve matched the scheduling to make it even easier for delegates to jump between tracks and pick the speaker sessions that suit them best.

Join us at the Sheraton Brussels Airport Hotel, in Belgium on Tuesday 7 & Wednesday 8 March 2017.

TWO DAYS, FIVE THEMES

Book your place NOW !

www.picinternational.net/register

PLATINUM SPONSORS

ficontec micro assembly machines
LIONIX INTERNATIONAL
LUCEDA PHOTONICS
PhoeniX Software
PhotonDelta Integrated Photonics Ecosystem
VPIphotonics DESIGN AUTOMATION

GOLD SPONSORS

IQE
SMART Photonics III-V foundry services

LANYARD SPONSOR

IQE

SUPPORTED BY

EPIC European Photonics Industry Consortium

This two day event covers five themes

Leveraging PICs in long-haul and metro networks

How can PICs support traffic growth? And how can they deliver value to operators?

KEYNOTE

- **Geoff Bennett: Infinera**
  An in-depth look at the practical implications of PIC technology in long haul networks, plus a perspective on how PICs could be deployed in other areas of the network, and in other platforms (such as core routers)

SPEAKERS

- **Vladimir Kozlov: LightCounting Market Research**
  Impact of Integrated Photonics on the Optical Communications Market
- **Martin Guy: Ciena Corporation**
  Strategies for photonic integration for metro and long-haul networks
- **Tom Williams: Acacia Communications Inc.**
  Putting silicon photonics to work on metro and long haul applications
- **Le Binh: Huawei Technologies**
  Integrated photonics systems to meet challenges in optical and wireless system convergence
- **Michael Wale: Oclaro**
  State of the art PIC-enabled telecoms

Supporting Data Centre Growth

Short reach communications could be a major win for PICs. But what are the customer priorities? And how can photonic integrated circuits come out on top?

KEYNOTE

- **Richard Pitwon – Seagate Technology**
  Opportunities for data centre optical interconnects

SPEAKERS

- **James Regan: EFFECT Photonics**
  InP as a platform for photonic integration
- **Karen Liu: Kaiam Corporation**
  Perspectives on hybrid integration
- **Bert Jan Offrein: IBM**
  Driving down the cost of datacentre photonics applying novel scalable integration concepts

PIC Platforms

What are the key materials systems driving photonic integration? And how should these platforms evolve to unlock greater performance?

KEYNOTE

- **Graham Reed: University of Southampton**
  Challenges left on the table regarding silicon photonics

SPEAKERS

- **Roel Baets: Ghent University**
  Silicon PIC-platforms: silicon-on-insulator and silicon nitride
- **Timo Aalto: VTT Research**
  Progress in PIC platforms at VTT
- **Dimitris Tsiokos: Phosnet Research Group, Aristotle University of Thessaloniki**
  CMOS-compatible plasmo-photonics for mass-manufactured PICs: New markets in semiconductor, medical and ICT industries
- **Michael Geiselmann: LIGENTEC**
  Applications for thick film silicon nitride integrated circuits
- **Arne Leinse: LioniX International**
  TriPleX™: The low loss industrial silicon nitride waveguide platform. Application examples from VIS to IR

Optimising PIC Design, Manufacturing & Packaging

What are the best resources for creating and delivering photonic integrated circuits?

KEYNOTE

- **Michael Watts: MIT**
  Bringing resources together to drive photonic integration

SPEAKERS

- **Peter O'Brien: Tyndall National Institute**
  Overcoming packaging hurdles for PIC devices
- **Suresh Venkatesan: POET Technologies**
  Realizing gains in energy efficiency, component cost and size-reduction through photonic integrated solutions
- **Peter de Dobbelaere: Luxtera**
  The design and processing of advanced transceiver integrated circuits
- **Gilles Lamant: Cadence Design Systems**
  Providing mainstream design flow for PICs
- **André Richter: VPIphotonics**
  Advances in layout-aware schematic-driven design automation for integrated photonic and optoelectronic applications
- **PhoeniX BV**
  TBC

New markets: Sensing, Medical?

What are the prospects for developers more broadly? And how does the supply chain need to adapt?

KEYNOTE

- **Liesbet Lagae: imec**

imec's progress as the pix4life project in the field of SiN photonics in the visible range for life science applications

SPEAKERS

- **Pim Kat: Technobis Group**
  Extreme fibre sensing: applications landscape for PIC beyond datacoms and telecoms
- **Iain McKenzie: European Space Agency**
  PICs: The Final Frontier
- **Ewit Roos: Photon Delta**
  Why European Photonics is undervalued and a fast-track plan of how to change it

CORPORATE PARTNERS DIRECTORY

AIXTRON
Tel: +49 2407 9030 0
Fax: +49 2407 9030 40
Email: info@aixtron.com
www.aixtron.com

Non Contact Measurements
Resistance, Resistivity
Wafer Thickness
KITEC microelectronic technologie
Tel: +49 (0)8122 86676
Fax: +49 (0)8122 86652
Email:info@kitec.de
www.kitec.de

Temescal
Tel: +1 925 245 5817
Fax: +1 925 449 4096
Email: lwarren@ferrotec.com
www.temescal.net

EPIGAN
Email: info@epigan.com
www.epigan.com

Phasix ESD
Tel. No: +44 (0)1420 565634
e-mail: sales@phasix.co.uk
website: www.phasix.co.uk

Lake Shore CRYOTRONICS
ADVANCING SCIENCE
Tel: +1 614 891 2244
Fax: +1 614 818 1600
Email: info@lakeshore.com
www.lakeshore.com

brewer science
Tel: +001 573-364-0300
Email: sales@brewerscience.com
www.brewerscience.com

CCS
CALIFORNIA COATING SYSTEMS
Tel: +1 510-501-4031
Fax +1 360-723-5368
Email: sales@cal-coating.com
www.cal-coating.com

WATLOW
www.watlow.com

PROTON
THE LEADER IN ON SITE GAS GENERATION
Tel: 203-949-8697
Fax: 203-949-8016
Email: info@protononsite.com
www.protononsite.com

ESSENTRA
Tel: 001 800 628 8606
Fax: 001 413 592 4112
www.essentraporoustechnologies.com

TYSiC
1st SiC-epi Foundry in China
Tel: 86-769-2289 3350
Fax: 86-769-2289 3355
Email: enquiry@sicty.com
www.sicty.com

III/V-Reclaim GaAs InP
Tel: +49 8728 911 093
Fax: +49 8728 911 156
Email: sales@35reclaim.com
www.35reclaim.de

GATAN
Tel: +1 925 224 7355
Email: info@gatan.com
www.gatan.com

UMC UNITED MINERAL & CHEMICAL CORP.
MBE Specialists
Tel: +1 201 507 3300
Fax: +1 201 507 1506
Email: inquiry@umccorp.com
www.umccorp.com

kSA k-Space Associates, Inc.
Thin-Film Characterization
Tel: +1 734-426-7977
e-mail: requestinfo@k-space.com
www.k-space.com

化合物半导体
CS COMPOUND SEMICONDUCTOR · CHINA
Tel: +44 (0)1246 718 979
Fax +44 (0)1246 718 971
Email: robin.halder@angelbc.com
www.compoundsemiconductor.net

NANO-MASTER
Cleaning • Deposition • Etching
Tel: +1 512-385-4552
Fax: +1 512-385-4900
Email: r.andrade@nanomaster.com
www.nanomaster.com

evatec
process systems
Tel: + 41 81 403 8000
Fax: + 41 81 403 8001
www.evatecnet.com

Vistec
Electron Beam
Tel: +49 (0) 3641 79980
Fax: +49 (0) 3641 7998222
www.vistec-semi.com

SEOUL SEMICONDUCTOR
Tel: +49 89 450 3690 0
Fax: +49 89 450 3690 45
Email: info.europe@seoulsemicon.com
www.seoulsemicon.com

CS COMPOUND SEMICONDUCTOR
Tel: +44 (0)1246 718 979
Fax +44 (0)1246 718 971
Email: robin.halder@angelbc.com
www.compoundsemiconductor.net

CAMSTAR
A Siemens Business
Big Data Product Performance Intelligence Solutions
Tel: 704-227-6600
Email: sales@camstar.com
www.camstar.com

Veeco
Tel: 516-677-0200-1222
Fax: 516-714-1231
Email: jpina@veeco.com
www.veeco.com

CORPORATE PARTNERS DIRECTORY

SUBMIT YOUR LAB & FAB ARTICLE

Research is the foundation for the growth of the compound semiconductor industry.

If you want to highlight the important breakthroughs that you make, submit your latest research stories to: RichardStevenson@angelbc.com

It is imperative that Compound Semiconductor remains a timely resource for this industry, so we are only interested in highlighting very recent work reported in academic papers.

Therefore, please only consider writing a short piece highlighting your work if you have a journal paper that has been accepted and about to appear in press, or a paper that has been published within the last month.

CS COMPOUND SEMICONDUCTOR
Connecting the Compound Semiconductor Community

www.compoundsemiconductor.net

MACOM GaN...Delivered

Enabling RF Energy with Leading Efficiency & Gain

Qualified for basestation applications, over 1 million GaN on Si parts shipped, and industry's first 300 watt 2.45 GHz RF Power Device offering

Only MACOM has taken GaN mainstream by combining an industry-leading RF portfolio with strong partnerships and unrivaled applications expertise. For nearly five decades, our engineers have been redefining RF power and are successfully applying their GaN ingenuity in commercial, ISM and wireless.

MACOM's MAGe-102425-300 enables RF energy solid state cooking.

Leading manufacturers in a wide range of industries are now leveraging MACOM GaN in an array of form factors to realize cost, bandwidth, power density and efficiency advantages.

- Power levels from 2 – 1000 W
- Frequencies from 890 MHz – 2.45 GHz
- Packages from QFN to TO-272 to ceramic

MACOM™

Partners from RF to Light

Learn more and get datasheet:
www.macom.com/gan