COMPOUND SEMICONDUCTOR

January/February 2008 Volume 14 Number 1

CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

GREEN GAP

Making whites brighter

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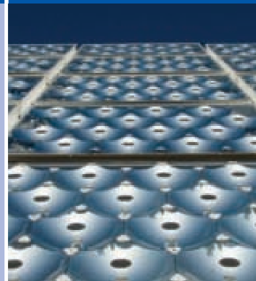

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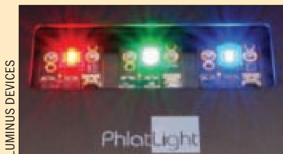

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Going places
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Main cover image: *Massive improvements in the efficiency of green emitters could be needed to overcome the limitations of phosphor technology and deliver cost-effective solid-state lighting. See p25. Credit: Sandia National Laboratories.*

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Time for more collaboration

Now passed into law, the US Energy Act (or, to give it its full title, the Renewable Fuels, Consumer Protection and Energy Efficiency Act of 2007) is a welcome, if expected, boon for the global LED industry. Its impact will not be felt overnight, though. With incandescent bulbs set to be phased out over the next decade and replaced by more efficient alternatives, it will likely be compact fluorescent lamps (CFLs) that come to the fore initially.

Unfortunately, CFLs have limitations too and have already sparked some scare stories themselves. Genuine concerns have emerged over both their mercury content – which, unless you like tucking into a plate of CFLs for breakfast, is primarily a worry for waste authorities rather than individuals – and the quality of the light that they produce.

But with energy savings of only 25–30% over incandescents demanded for regular bulbs by 2012–2014, we will likely be well into the middle of the next decade before solid-state technology takes a major slice of the US lighting market. The part of the latest legislation that ought to make a difference is the standard calling for a 75% energy saving over incandescents. It is not set to come into effect until 2020, but such a major hike in efficiency only looks like it will be possible with LEDs.

> "Some challenges are just too big for any single organization to take on"

For the LED industry, the challenge is to drastically cut the cost of each lumen emitted by lamps based on semiconductor chips. To do that is going to require a lot more collaboration, something that the US Department of Energy (DoE) is hoping that its high-profile, $20 million "prizes" for new lighting technology will ignite. Jim Brodrick, one of the key figures at the DoE's lighting program, says that every part of the supply chain, from epitaxy specialists to lamp makers, needs to be involved to meet the challenging goals set out in the prize specifications.

That kind of approach is also going to be needed if III-V materials are to find their way into future generations of silicon CMOS technologies. Despite an upsurge in activity in this area (see our IEDM conference report on p13 for details), there are myriad technical problems that still need to be solved. Some challenges are just too big for any single organization to take on, so the message is simple – more collaboration.

Michael Hatcher *Editor*

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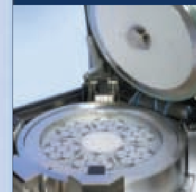

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POLICY

US Bill energizes solid-state lighting

By Andy Extance

Measures that restrict the use of incandescent lighting and promise incentives for their replacement with solid-state technologies have become law in the US, as an important part of the country's energy policy.

The Renewable Fuels, Consumer Protection and Energy Efficiency Act of 2007 was signed by President Bush in late December, and its LED-related provisions are now being enacted by the US Department of Energy (DOE).

Performance standards for general service light bulbs demand 25–30% energy savings compared with today's incandescent bulbs by 2012–2014. In the longer term a standard for 75% savings will come into effect in 2020, which will likely only be met by solid-state technologies.

In the shorter term the DOE is planning "visible and large activity" surrounding the $20 million Bright Tomorrow Prizes. These prizes will be awarded to the first LED lamps directly replacing their incandescent rivals, as stated in the 2007 act.

"The prizes will stimulate a lot of thinking and get a lot of publicity," said Jim Brodrick, lighting program manager at the DOE.

This incentive-focused approach typifies and intensifies the efforts that the DOE is making in order to support the LED industry's improvement of lighting technologies. "The big driver is the market play," said Brodrick. "LED lighting will perform much better than an incandescent. The price may be high at the start but can come down. The prizes are a way of getting that rolling in a formal public way. Sure, you can legislate standards and that's fine, but the market can and will take off for the LED lamps regardless."

The competition, which is expected to start within two months, will eventually be launched by a high-profile US politician. "The prize specifications are challenging, and if someone wins they will certainly merit it, and the notoriety from winning," said Brodrick. "Everybody – from circuitry or drivers, the LED, the die-makers, the epitaxial growth – will be involved in this."

The prizes represent just one aspect of the DOE's efforts to draw together people who are involved in moving the LED lighting industry forward.

As *Compound Semiconductor* went to press, the DOE was about to announce the recipients of a further $20 million in funding, granted in its annual solid-state lighting Core Technology and Product Development programs. There is also a solid-state lighting category in the DOE's latest Lighting for Tomorrow competition.

Brodrick says that creating a better understanding between those involved in making lighting fixtures is the main challenge for increased penetration of the general illumination market by LEDs.

"Communicating well is important," he said. "There needs to be planning and communication between semiconductor and luminaire industries to get the best performance."

TDI

The compound semiconductor industry lost a high-profile, popular figure in January with the untimely death of Technologies and Devices International (TDI) CEO Vladimir Dimitriev.

In recent weeks, Dimitriev appeared to be getting close to realizing his goal of developing low-cost methods for producing high-quality nitride semiconductors. According to TDI, the company had just been awarded a key US patent covering the hydride vapor phase epitaxy manufacturing approach. TDI is also expecting to announce a deal with a "major partner" to help to introduce this equipment commercially in the near future.

Dimitriev co-authored an article on p-doping in GaN-based semiconductors, which appears on p19 of this issue.

CONSUMER ELECTRONICS

LED backlights sparkle in Vegas

The annual Consumer Electronics Show (CES) gadget-fest saw a number of major consumer electronic firms showcase LCD televisions with LED backlights.

Korean giants Samsung and LG were among those firms, with Samsung launching its F96 line of "smart" 70 and 52 inch LCD televisions. In these, LEDs enable a locally dimmable screen and very high contrast, resulting in a much clearer picture. LG's 47 inch screen is based on an LED backlight featuring 128 individual chips. It also features local dimming.

The innovative LED chip maker Luminus Devices was exhibiting at CES. Its PhlatLight technology (see right) featured in a 67 inch rear-projection TV that was launched by Samsung.

Luminus showed off its new backlight unit, designed specifically for LCD televisions. According to the Massachusetts company, only eight of its high-brightness LED chipsets are required to edge-light a large display. Luminus believes that by reducing the number of chips dramatically, it can offer a much lower cost for the LED backlight unit.

LUMINUS DEVICES

Backlight LEDs from Luminus Devices featured in Samsung and Sharp TVs at the annual CES.

Luminus is also aiming to break into the emerging market for "pocket" projectors. Korean firm Innoswell showed a Luminus-powered LCD projector with a brightness of 180 lm, which is thought to be a record for this type of display.

CES also witnessed the latest round of the HD DVD and Blu-ray format war. Both optical-storage formats rely on GaN-based lasers, but it now appears that the Sony-backed Blu-ray has the upper-hand. Sony claims that, thanks largely to sales of the PlayStation 3 console, its format is outselling Toshiba's HD DVD by a ratio of 6:1.

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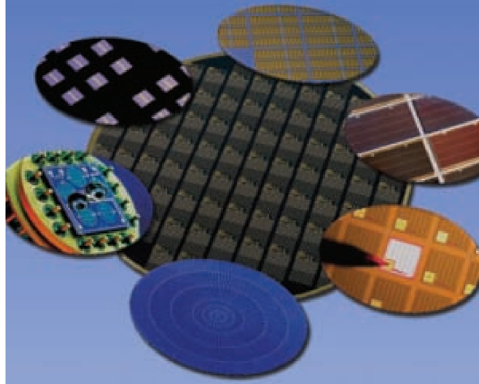

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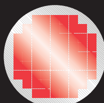

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MERGERS AND ACQUISITIONS

RFMD sets up Filtronic expansion

RF Micro Devices (RFMD) appears to have allayed fears over the future of Filtronic's GaAs-fabrication facility with a definitive agreement to purchase the UK company's compound semiconductor business by February 29.

The £12.5 million ($24.8 million) cash deal should bring welcome relief to the workers at the Newton Aycliffe wafer fab, which was put up for sale earlier this year when RFMD announced plans to end its outsourcing contract with Filtronic.

However, with increasing demand for GaAs-based components from 3G cellular handsets and wireless LAN applications, RFMD needs to make sure that it has sufficient capacity in place before it completes another wafer fab in Greensboro towards the end of next year.

Dean Priddy, RFMD's CFO, told *Compound Semiconductor* that the company is already looking to expand production at Newton Aycliffe. "We're going to turn this thing around and ramp it up," he said.

Although this expansion will not require any major capital expenditure, it is expected to demand an increased workforce. The operation situated in the north east of England currently employs about 300 people. However, Priddy believes that approximately 75 new jobs could be created as part of the volume ramp.

"The plan is to fully utilize the existing equipment base," Priddy said. "But we will need more operator talent, technicians and engineers. Filtronic has been a good supplier to RFMD and we're comfortable with the current management structure there."

Despite already being the world's largest manufacturer of GaAs RF components, RFMD clearly feels that owning the additional facility is preferable to merely ramping up its purchase order at Filtronic and will improve its profit margins compared with the prior outsourcing arrangement.

Priddy estimates that, once fully utilized, the Newton Aycliffe fab will add an extra 20% on top of RFMD's existing wafer production capability.

RFMD will also be offering foundry services following the acquisition, the first time that it has publicly revealed this side of its business strategy. Chief among its initial customers will be Filtronic, which – in a complete role reversal – RFMD will now supply with PHEMT devices for use in point-to-point wireless communications.

The agreement between the two companies stipulates that this supply deal will run for a minimum of three years.

APPLICATIONS

GaN brings weather radar into digital age

The world's first weather radar to use a high-power semiconductor module based on GaN components has been installed at Japan's Nagoya University.

Toshiba Corporation says that its GaN field effect transistors (FETs) allow it to replace the electron tubes that are usually used in weather radar transmitter modules, resulting in a much more compact system.

Measuring 2 × 2 m, the new radar system is only one-sixth of the size of electron-tube radars that are currently in use and it matches the incumbent technology for price. By propagating a signal with a 200 W transmit power, the radar can scan a total range of 64 km.

Made for Nagoya's Hydrospheric Atmospheric Research Center using Toshiba's existing X-band GaN FET technology, the initial 9 GHz radar began operation in late November. Further individual X-band GaN radars will be made to order, including some based on C-band FETs to operate in the 5 GHz spectrum.

A Toshiba spokesperson says that the development of semiconductor weather radar was made possible by its GaN products, because they offer twice the power output over similar-sized silicon devices.

The FETs are more reliable than electron tubes, which often need replacing during the lifetime of a system, and therefore the running costs of the semiconductor radar should be much lower. By moving to GaN transistors, weather radar will also be able to make more efficient use of the radio spectrum because the frequency range scanned is much narrower.

According to Toshiba the switch to solid-state will also improve radar performance. "The new radar also enhances the precision of rainfall estimation by capturing the shape and size of raindrops and clouds," the company explained. "[It] detects air conditions, including wind speed, even in very clear weather – a very difficult task for most weather radars."

TRANSISTORS

Terahertz milestone 'within reach'

US and Swiss research teams are inching ever closer to the production of RF and digital components capable of operating at terahertz speeds for high-end satellite and military applications.

At the International Electron Devices Meeting (IEDM) held in Washington, DC, in December, groups working on both HEMT and HBT designs revealed their latest progress, with Northrop Grumman's Richard Lai reporting the first transistor with a maximum oscillation frequency (termed f_{max}) in the terahertz regime.

Although that figure is calculated by extrapolation from genuine measurements, Lai told IEDM delegates that reaching the 1.2 THz milestone with an InP-based PHEMT was "ground breaking".

The team's cutting-edge device designs have allowed a record-breaking three-stage amplifier with a gain of 16 dB at 340 GHz.

Key features of the latest transistors, which Lai says are being fabricated in volume with a wafer yield of more than 90%, include improved electron-beam lithography and a refined epitaxial structure. Previous designs with a 70 nm gate had delivered an f_{max} value of 700 GHz, but Lai and colleagues have scaled the gate down to just 35 nm (the actual gate size varies between 30 and 50 nm) to make the faster transistors.

The pseudomorphic epitaxial structure, which has been similarly scaled down, features an InAs/InGaAs composite channel grown by MBE, and a highly doped cap layer that reduces ohmic contact resistance.

Another team from Northrop Grumman's Redondo Beach, California, operation has been working on InP-based HBT designs, where the emphasis is more on the f_t figure of merit (the cut-off frequency). It has now produced double HBTs with an InGaAs base that show an f_t of 400 GHz. Using 1100 of these HBTs, fabricated in a high-yielding process, Cedric Monier and colleagues have also made a 35 Gb/s integrated circuit and demonstrated a static divider with a record speed of 153 GHz.

Milton Feng's group at the University of Illinois at Urbana-Champaign has long targeted the terahertz regime, and at IEDM William Snodgrass described the team's latest achievement – an InP HBT with an f_t measured at 745 GHz.

This is similar to the figures of merit that Feng's laboratory has produced previously, but the team has now been able to scale up the breakdown voltages of HBTs – a characteristic that is inherently traded off against raw speed. Scaling its GaAsSb base layer to 20 nm yielded an f_t of 630 GHz, with an accompanying breakdown voltage of 3.2 V.

Outside the US, Colombo Bolognesi's group at ETH Zurich in Switzerland has also been pursuing super-fast InP HBT structures, based on a graded GaAsSb base layer deposited using MOCVD.

For those devices, it has now extrapolated an f_t of 612 GHz when they are measured at room temperature.

START-UP

E-mode makes noise with high-speed radio

The gigabit-per-second data transmission promised by E-Band Communication Corporation's pioneering GaAs-based systems is earning it plenty of attention, from both investors and potential customers.

Systems designed at E-Band's San Diego base have been deployed commercially and are now being sold in earnest, according to chief marketing officer Saul Umbrasas.

E-Band says that it uses GaAs PHEMT technology to make a highly integrated set of millimeter-wave chips. They transmit data at rates of 1–10 Gb/s using the 70–80 GHz, or "E-band", region of the electromagnetic spectrum, from which the company derives its name.

"Our radio performance is reliable, easy to install and maintain, integrates into carrier networks and we have superior technology as well as cost structure," said Umbrasas. "You can see this reflected in our investors, which include two major carriers, one major telecom equipment manufacturer and a bank that has lots of investments in telecommunication areas."

These investors, which include Indian communications group Reliance and another unnamed "major wireless carrier", have just ploughed an additional $10 million into E-Band's coffers. Also contributing was telecom equipment manufacturer ADC Telecommunications.

E-Band's systems are, in part, based on high data transmission rate GaAs MMIC technology developed at Northrop Grumman and exclusively licensed by E-Band. They transmit data over frequency bands opened by the US Federal Communications Commission in 2003 for high-speed wireless.

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LED BACKLIGHTS

AU Optronics discredits MOCVD rumor

By Andy Extance

Taiwan's biggest manufacturer of thin-film transistor LCD displays – AU Optronics – has refuted claims in the Chinese-language press that it is "planning to buy 100 units of MOCVD equipment".

A story originally published in the *Economic Daily News* and reported in English at *Digitimes* on December 20 said that AU Optronics has already placed bookings for this equipment.

However, when speaking recently to *Compound Semiconductor* about these reports, the company said: "They are not true and we would like to clarify that we have no concrete timetable for LED development so far."

According to the *Digitimes* report, equipment makers had said that if AU Optronics did order the suggested number of tools, it would require an investment of some NT$10 billion ($300 million). It slates Miaoli County, Taiwan, as the site for the LED-making venture that it was rumored to be establishing.

The company, which made NT$9 billion profit on sales of NT$263 billion in 2006, is expected to outline plans for its next-generation displays shortly.

AU Optronics says that it anticipates increased LED backlight usage in the future. The company currently purchases LED backlight units, which it then assembles into its various displays.

As one of the world's top-three thin-film transistor LCD makers, the Taiwanese firm has already begun using LED backlights in many of its products. These include displays for cameras, mobile devices and portable media players, in-car displays, and LCD screens for notebook computers. The displays that are using LED backlights range in width from 1.5 inch for small devices, such as cameras, to 15.4 inch for notebook computers.

LED backlights allow for thinner and lighter display modules, the Taiwanese firm says, although up until recently their extra cost had been the major factor limiting uptake in a notoriously cost-driven industry. LEDs also offer environmental benefits by doing away with mercury-containing compact-fluorescent backlights and offering improved power-saving features.

START-UP

Goldeneye's chips ease LED manufacture

LEDs manufactured using just epitaxy will be able to provide illumination at a fraction of the cost of their competitors, thanks to the simple process used to make them.

That's the word from Carlsbad, California, where a company called Goldeneye, Inc. is touting its EpiChip, ahead of commercial introduction in the fall of 2008.

"Based on improved efficiencies, a reduced number of process steps and associated yield losses, the cost of manufacture is significantly less than conventional methods," the company told *Compound Semiconductor*. "Our intention is to use this technology in the design and fabrication of complete packaged light sources, not the sale of bare die."

Founded in 2004, Goldeneye is headed up by CEO and semiconductor equipment specialist Ken Livesay, with additional technical expertise provided by vice-presidents Scott Zimmerman, who leads the EpiChip development, and Karl Beeson.

They say that the general lighting market will benefit from the first packages featuring these die, which promise improved extraction efficiencies and thermal management.

To date, Goldeneye has made blue and green GaN EpiChips, with high-quality, robust epilayers ranging from 10 to 50 µm in thickness. Driving currents are better spread across these thick layers than in thinner LEDs and the chip's contacts are better separated, making packaging much more straightforward.

The typical measured output for one of Goldeneye's 520 nm-emitting 200 × 200 µm EpiChips is 5 mW at 20 mA driving current. The company has also made larger EpiChips measuring 1 mm^2 in area to demonstrate the process, although currently it does not have any detailed performance data for these larger chips.

EpiChips were originally developed to go into Goldeneye's "light-recycling systems" – reflective cavities where the brightness of outputs from the similarly reflective LEDs that they accommodate are enhanced. However, the company has now patented its "epi-only" approach for a wider range of applications.

Although Goldeneye is reluctant to release details about how and where its thick epilayer LEDs are made, its patents suggest that HVPE is used. Otherwise, the company says that it outsources to an "ensemble of strategic partners, contract manufacturers and primary vendors".

The company's first products should appear later this year and will be aimed at the general illumination market. Goldeneye is planning to sell RGB lamps that combine the EpiChip with other technical innovations, such as its patented "light-recycling" optical cavity. According to the company this cavity is capable of producing more than double the light output of a typical high-brightness LED.

HELLA

Bling-conscious quarterbacks may soon become unwitting early adopters of solid-state headlamps, following automotive lighting specialist Hella's development of a full LED system for the new Cadillac Escalade Platinum model.

When series production begins in summer 2008, the top-end car will become the first mass-produced sports utility vehicle (SUV) to be fitted with full solid-state forward lighting.

The SUV's low beam features five white LED units that are stacked vertically. These also provide the daytime running lamp function, which works by simply dimming the output from the LEDs.

The high beam, sometimes also known as the "full" beam, features two optical elements and a ventilator for active cooling of the new multichip white LEDs that are used in the low- and high-beam functions.

SAPPHIRE SUBSTRATES

Rubicon makes $94 m Nasdaq debut

Despite a volatile financial market, the stock price of sapphire substrate specialist Rubicon Technology has seen healthy growth since the Illinois company's initial public offering (IPO) in November 2007.

After hitting the market at $14 per share on November 16 in an offering worth approximately $94 million, shares in Rubicon rose to $19 and peaked at $24 in the recent holiday period before settling back slightly. The IPO value was based on the sale of the company's first 6.7 million shares.

The flotation appears to have come at a good time, because the company recently hit 100% utilization at its Illinois manufacturing facilities and needs the funds to continue its expansion.

CFO William Weissman pointed out in an online investor presentation that the company's 2007 revenues were up by 60% compared with the equivalent period in 2006. He expects a further 40% hike this year and says that the company already has $40 million in orders to support that prediction.

According to Weissman, Rubicon became profitable in the first three months of 2007 and that financial performance has improved further since then.

Rubicon's profitability appears to have been driven partly by the company's large wafers, with which it can achieve higher operating margins. The company claims to be the only manufacturer of 6 inch sapphire wafers, which are used in silicon-on-sapphire RF applications, and it is now working on upgrading its processes to 8 inch wafers. Australian RFIC switch manufacturer Peregrine Semiconductor is a key customer of Rubicon's.

However, Rubicon is also confident of benefiting from the growth potential of the LED market, where sapphire is used as an economical substrate for GaN-based devices. Success in this much larger market will be vital for its advancement. Although most LEDs are still made on 2 inch wafers, Rubicon's CEO Raja Parvez asserted that "the market is moving towards us", regarding larger substrate diameters.

The IPO price, which was at the high end of the expected range, together with what looks to have been a successful flotation thus far, suggests that Parvez and Weissman succeeded in grabbing investors' attention.

Parvez in particular went to great lengths during a recent investor presentation to tie Rubicon's fortunes to the rising star of the LED industry. "Sapphire is to the LED as silicon is to the microprocessor," he emphasized repeatedly.

The optimistic outlook that Rubicon painted for sapphire is backed up by an iSuppli report, which predicts that the value of the GaN LED market will be more than double its 2007 level by 2010.

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SHAREHOLDER LAWSUIT

Jury clears former JDSU execs of fraud

A jury in Oakland, California, has found JDSU and four of its former executives not guilty of fraud and insider trading.

The case against ex-CEOs Jozef Straus and Kevin Kalkhoven, former CFO Anthony Muller and former COO Charles Abbe was brought by the state of Connecticut, whose public pension funds lost millions of dollars when JDSU's stock price nosedived in 2000–2001 amid the wider telecoms crash.

The class action lawsuit alleged that the JDSU executives had known all about the impending slump but that, rather than warning investors, it had instead profited by dumping its own stock while covering up the industry's problems.

Kevin Kennedy, JDSU's current CEO, welcomed the result: "We are extremely gratified by the jury's verdict as we have always believed that the plaintiffs' claims were without merit."

Though he may have been confident of the outcome, Kennedy will no doubt also be somewhat relieved, as a decision against JDSU could have financially crippled the Milpitas-based maker of optoelectronic chips and modules. In its 10K filing with the US Securities and Exchange Commission, JDSU had said of the lawsuit: "Although the complaint does not specify the amount of damages sought, plaintiffs stated in recent court filings that they seek more than $20 billion in alleged damages."

In the fiber-optic boom of the late 1990s, JDSU's stock price, along with many of its peers, rocketed to previously unthinkable highs. The company's paper value enabled its senior managers to make a series of major acquisitions, culminating in July 2000 when JDSU announced its intention to buy the laser chip maker SDL in a stock deal valued initially at a staggering $41 billion. At the time, SDL was reporting quarterly sales in the region of $75 million.

As it turned out, JDSU's share price had peaked before the SDL deal – at more than $1200 in early March 2000. But only one year later, JDSU stock had plummeted by more than 80% to around $200, while in mid-2005 it bottomed out at close to $10, representing a fall of more than 99%.

Though cleared of all charges, there is no doubt that the executives profited from what, with the benefit of hindsight, looks like an absurd boom period during 1999–2000.

Venture capitalist Kalkhoven, for example, became the CEO of Uniphase, as it was then known, in 1992. At that time, Uniphase was a privately held industrial laser manufacturer. After shifting the firm into fiber optics and creating JDSU through a merger with JDS Fitel in July 1999, Kalkhoven retired as company CEO in May 2000.

Then in 2003 the motor sports fan set up his own race team, called PKV Racing, later entering the Champ Car World Series. After that, in a move that echoed his vertical integration strategy while at JDSU, Kalkhoven and a colleague also bought engine maker Cosworth Racing.

For the record, PKV drivers Neel Jani and Tristan Gommendy finished 9th and 12th, respectively, in the 2007 Champ Car rankings. At the Nasdaq closing bell on January 9, a share in JDSU was worth $11.49.

PHOTOVOLTAICS

Emcore lines up more terrestrial solar deals

Emcore has two large deals to provide GaAs-based solar cells for concentrating photovoltaics in the pipeline. Each of the deals could exceed the size of the company's largest single-deployment order to date.

A memorandum of understanding for a three-year, 150 MW supply agreement with a project spanning Spain, Italy and Greece will likely become the first firm order.

"At this point we have gone through a rigorous technology review by third-party consultants," said Emcore's CEO Reuben Richards in late December. "They've issued a commitment to fund us and we are moving forward on that. Expect closure in a relatively short timeframe."

The second project, which could amount to a 200 MW supply in California, is less certain and is dependent on an existing tax credit scheme continuing beyond 2008. Several other smaller deals, totaling at least 38 MW, are expected in the near future.

The Alberquerque firm will also deploy 60 MW of solar power systems in Ontario, Canada, from mid-2008 onwards.

PANASONIC WORLD SOLAR CHALLENGE

A team of students from Delft University in the Netherlands won the 2007 Panasonic World Solar Challenge using a car covered with GaAs-based triple-junction solar cells. Nuon Solar's car, the Nuna4, completed the 3000 km race across Australia in 33 h, beating its closest rival by 1 h 36 min.

The car used cells originally designed to power satellites. Operating at 26% power-conversion efficiency, these cells covered 6 m^2 of the car's surface. Thanks to improvements in the cell efficiency, this is less than the cell area needed to power previous versions of Nuna, meaning that the latest incarnation was much lighter.

As a result, the car hit a top speed of 137 km/h as it dodged kangaroos on the road from Darwin to Adelaide.

FIBER-OPTIC COMPONENTS

Oplink shuts Taiwan InP facility

Optical network component vendor Oplink Communications is to shut down its InP wafer fab, the site in Taiwan that it acquired last year in a takeover of chip maker Optical Communication Products (OCP).

Closure of the fab, which formerly belonged to Gigacomm, will see 120 employees lose their jobs as part of a wider restructuring by the parent firm, which is switching to a fabless business model. The Taiwan fab, which was founded in 2000, is expected to be closed down by March 31.

Other measures include closing a research and development laboratory in the UK, with the loss of 10 jobs, and slashing another 150 from the payroll at OCP's Woodland Hills, California, headquarters.

The move has been on the cards since former OCP director Robert Shih resigned, following a heated exchange with Oplink CEO Joe Liu last September. While Liu favored the fabless approach now being implemented, Shih, who was vice-president of business development at Oplink, said that closing the fab would reduce the OCP division's 2008 sales by half, seriously compromising its future viability.

With some of OCP's product lines being sold for less than the manufacturing cost of the components, Liu clearly felt that the fabless option was the only way forward. While Oplink will retain some of OCP Asia's operations, manufacturing will be transferred to Oplink's Zhuhai, China, site.

OVERCAPACITY

Still too many fabs, says Rawls

Seven years since the telecom meltdown of 2001, there are still twice as many III-V fabs than are needed to meet the current demand for lasers and photodetectors, Finisar CEO Jerry Rawls says.

"This is a very challenging market sector," Rawls told investors at a conference call to discuss the firm's latest financial quarter, in which it missed its initial revenue guidance significantly.

"There are still too many of us [suppliers]," said the CEO. "Overcapacity and consolidation among our customers' customers means that there is a lack of pricing power, while we need to spend lots of money on research and development."

Ironically, given Rawl's comments, one key problem in Finisar's most recent quarter was that it was unable to meet expected sales of 10 Gbit/s transceivers because of a shortage of certain fixed-wavelength lasers used in C-band wavelength division multiplexing applications. Finisar does not make these chips, and the shortage forced it to qualify a second source of the lasers.

This and other problems meant that Finisar missed its initial revenue target by around $6 million, eventually posting just under $101 million in sales.

A key part of Rawls' future strategy is to expand the company's range of products so that Finisar can address some key applications that it does not currently serve.

One example is in the tunable laser sector, now worth some $400 million per year, according to some estimates.

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...Wins for Arima and Emcore
US solar-cell maker Emcore and Taiwan's Arima Eco were among four companies selected to complete a 3 MW concentrating photovoltaic project in Spain. Emcore's systems will provide 300 kW when installed.

...Mitsubishi ramps GaN
Mitsubishi Chemical Corporation is planning a 10-fold production capacity expansion of GaN substrates, to 1000 2 inch wafers per month.

...€35 m photonics center
Germany is setting up a center of excellence to develop novel photonic components based on compound semiconductors. Headed up by GaN expert Michael Kneissl at the Technical University of Berlin, the new center will receive total funding of €35 million ($52 million) from the National Science Foundation over 12 years.

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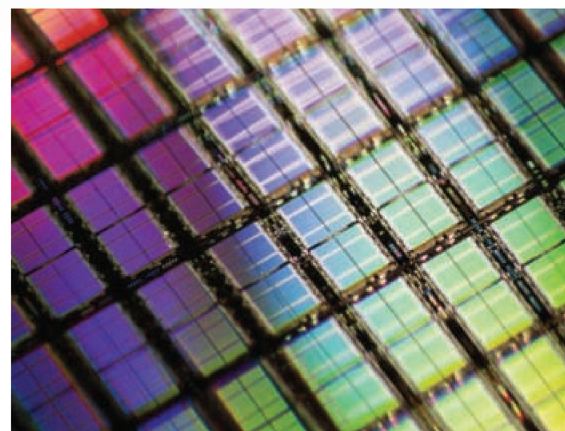

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IEDM

III-Vs and CMOS: the logical choice?

Traditionally the conference where future silicon processes first emerge, it was standing room only for "III-V CMOS" at the 2007 International Electron Devices Meeting held in Washington, DC.

If you want to peek at the future of silicon CMOS processing, the International Electron Devices Meeting (IEDM) is the place to start. Alternating between Washington, DC, and San Francisco each December, and running for more than 50 years, it is where key semiconductor technologies often emerge.

The researchers in attendance are facing what some are calling the greatest problem in microelectronics technology in a generation – finding a replacement for silicon logic.

At the 2007 event in Washington, compound semiconductors were making their biggest impression yet on the CMOS research community. While Intel's presentation on its commercial implementation of high-k gate dielectrics drew much attention, the atmosphere in a tiny conference room crackled with anticipation as the same company presented details of GaAs-on-silicon epitaxy that has produced a defect free quantum-well transistor.

Although many view Intel as a company apart within the wider CMOS community, there was evidence to suggest that compound materials will play a significant role in the future – perhaps by 2015.

Eight years might seem a long way off, but the semiconductor industry roadmap demands that a solution is "on the table" in just three years. Jesus del Alamo from the Massachusetts Institute of Technology (MIT) was chairman of the compound semiconductor subcommittee at IEDM. After the event he said that the conference was notable for the upsurge in attention now paid to III-V CMOS.

"There was definitely much more interest this year than in previous years," said del Alamo. "The concept of III-V CMOS started being mentioned at IEDM in 2005 through a couple of papers. In 2006 we had some intriguing papers that suggested significant promise. In 2007 we saw a lot of good work and serious debate. There is no question that this is a hot topic now."

IEDM 2007 kicked off with a Sematech workshop entitled "III-V CMOS on Silicon: Technical and Manufacturing Needs". Convened by Robert Chau – Intel's director of transistor research – the Aixtron-sponsored workshop drew a small but keen band of attendees, who decided that the scalability of MOCVD makes it the most promising manufacturing approach. And while InGaAs is the leading candidate for channel material, dual-channel devices may feature germanium in the PMOS structure.

Chau was part of the team that worked with IQE's

2007 iedm International Electron Devices Meeting

The 53rd IEEE International Electron Devices Meeting took place on 9–12 December 2007 at the Hilton Washington, attracting approximately 1600 delegates. The 2008 event will take place on 15–17 December at the Hilton San Francisco and Towers.

"We need more collaboration and coordination."

Jesus del Alamo, MIT, on III-V CMOS.

Bethlehem, PA, operation on the new GaAs-on-silicon transistor. It appears to have overcome a key problem – the huge lattice mismatch between these two materials – to produce active quantum-well device layers that are virtually defect free.

Chau and his team did that by forming a composite InAlAs buffer layer to "filter out" the defects and stop them extending into the quantum wells. Although this has been done before, the Intel and IQE researchers have been able to reduce the thickness of this buffer layer, deposited using MBE, to 1.3 µm.

The enhancement mode quantum-well transistor (QWFET) it then fabricated, which featured an 80 nm gate, had a much higher cut-off frequency than standard 60 nm gate silicon n-MOSFETs. That additional speed could be exploited directly in logic circuits or, if it operated at the same speed as the all-silicon device, the QWFET would allow a 10-fold reduction in DC power dissipation.

However, despite this and other promising research at IBM, Freescale and the University of Glasgow, many remain unconvinced by the Intel work and there is a big divide among the III-V proponents and the nay-sayers. "By 2012 we should have a real working solution for III-V," suggested Chau, while others in the industry argue that the sheer number of technical issues that still need to be addressed would make the complexities of III-V CMOS impossible to resolve fully in time for devices at the 22 nm node. Scaling up to 12 inch wafers and switching to MOCVD deposition are just two of the key goals, and there are some fundamental question marks over the Intel device – like how to switch it off.

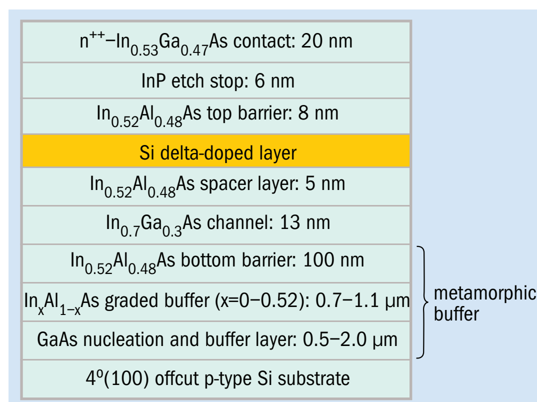
That split was also reflected in a packed panel session hosted by Dimitri Antoniadis from MIT, in which he asked the audience whether looking beyond silicon in logic applications would remain a pipe dream, or whether it really is the inevitable next step in CMOS evolution.

By the end of that discussion around half of the audience said that, aside from gate structures, they believed that non-silicon materials would feature in CMOS by 2020 – hardly a ringing endorsement of the approach, but a more favorable proportion than you could have expected just a couple of years ago. Del Alamo certainly thought so: "There is a rapid change of opinion on this topic, as the difficulties for further silicon scaling become more obvious."

"A couple of years ago, it was nearly a ridiculous idea to entertain the notion of III-V CMOS," he added. "Today, it's no longer ridiculous. The topic is being seriously debated."

As the guest luncheon speaker at IEDM 2007, TSMC chairman and CMOS industry veteran Morris Chang listed what he called the six disruptive developments that have shaped the business over the last 40 years: first the transistor; then the integrated circuit; Moore's Law; CMOS itself; the microprocessor; and – unsurprisingly – the foundry-based manufacturing business model.

High-k gate dielectrics might be the next break-



Intel's GaAs-on-silicon structures rely on a graded buffer layer that "filters out" defects caused by the huge lattice mismatch between GaAs and silicon. In recent work, Intel and IQE have collaborated to reduce the buffer layer thickness from 3.2 to 1.3 µm, without impacting the crucial quantum-well device layers.

through to be added, and it would certainly be premature to include III-V materials on such a list any time soon. But, given the upsurge in attention that a growing element of the mainstream CMOS community is now paying compound materials, IEDM 2007 could eventually come to mark a watershed moment for the semiconductor industry.

For that to happen will require far more involvement from semiconductor manufacturers outside Intel and IBM. Del Alamo believes that the recent upsurge of interest in III-V CMOS is largely due to these two companies, but also that much more is needed. "Everybody else is sitting on the fence," he said. "[But] the challenges that this technology faces are enormous. We need more people to be engaged and we need more collaboration and coordination."

While IEDM was in full swing, there was a timely suggestion that this may be happening, with Iain Thayne's University of Glasgow group announcing that it had received $2.5 million to work with the US-based Semiconductor Research Corporation on a III-V n-channel for next-generation CMOS.

Another company with some involvement is Freescale, for whom Matthias Passlack delivered an invited presentation. Collaborating with Thayne's team, Passlack and colleagues have now made MOSFETs on both GaAs and InP platforms. In his first IEDM visit since 1995, Passlack was clearly struck by the upsurge of interest in III-V CMOS, joking that 12 years ago he was one of just a couple of "nerds" working on it. "Now we have a few more nerds," he grinned at the packed conference room, which by then had become standing room only.

At the moment it is not clear whether the likes of TSMC, Samsung, ST Microelectronics and the other big hitters are prepared to follow the lead and help to solve the various problems. But, if the next few months see more companies launch research programs in this area, and more government-sponsored work at locations such as the Glasgow laboratory, then III-V CMOS could become the real deal. ●

Emerging Standardization for Sapphire Substrate Inspection

By Frank Burkeen

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The HBLED industry continues to thrive driven by market demand from mobile devices, automobiles, computer screens, and niche exterior and interior lighting applications. As HBLED device technology evolves and fabrication techniques become more advanced, defect detection and process control are critical to improving device yields. Sapphire substrate contaminants such as particles, scratches, pits, bumps, stains and residues from CMP processing are known to impact subsequent epi deposition processes and substantially degrade device performance and yield. As such, the need for higher quality sapphire substrates is of critical concern for HBLED device manufacturers.

The adoption of optical surface analyzer (OSA) technology is gaining momentum for use in HBLED manufacturing, specifically sapphire substrate inspection.

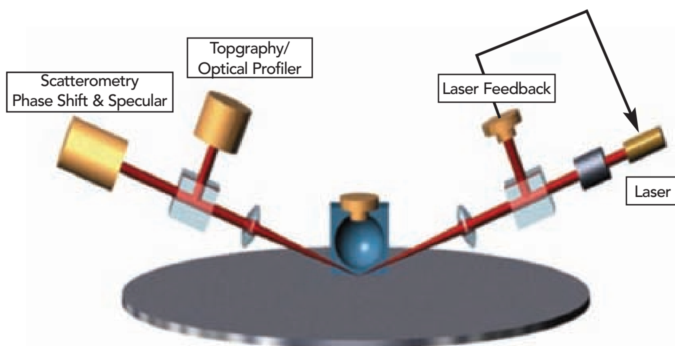

Figure 1: OSA technology combines four signal detection channels, enabling a wide range of inspection applications.

The design of OSA technology combines reflectometry, optical profilometry, scatterometry, and phase shift to measure topographic variations and detect a wide variety of surface defects. The inspection method achieves full surface coverage in minutes to produce high-resolution imaging, wafers maps, and automated defect classification.

At a throughput exceeding 40wph, an OSA system is the only wafer inspection method amenable to volume production and capable of advanced inspection of transparent sapphire substrates. Other inspection tools based solely on scatterometry cannot effectively measure transparent materials due to scattered light interference from the backside of the substrate. An OSA system is designed specifically for defect detection and classification of transparent materials including sapphire, GaN, SiC, and glass.

Figure 2 illustrates a sapphire substrate defect map after OSA inspection. Particles, scratches, pits, and stains are detected and classified in user-defined bins. The defect traceback images show a scratch as detected in the topography channel and two different types of stains as detected in the phase channel.

Scratches are known to transfer to the subsequent epi layer thereby degrading or killing device performance. Substrate stains have been reported to cause poor epi layer adhesion or result in rough epi morphology.

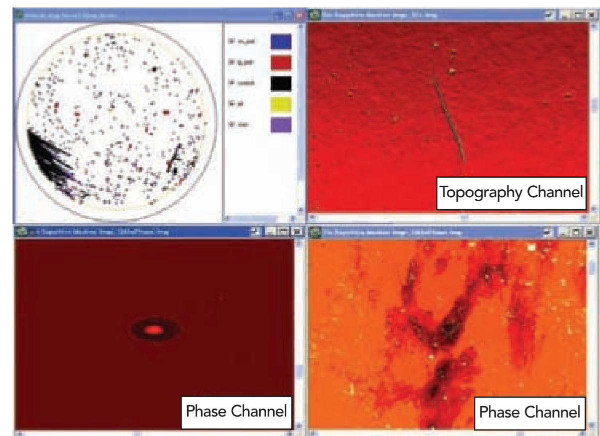

Figure 2: KLA-Tencor's Candela™ OSA defect map and traceback images of scratches and stains as detected in topography and phase channels, respectively.

As HBLED competition tightens and margins are squeezed, manufacturers are relying more on automated OSA inspection technology for process control and yield improvement. The emergence of sapphire substrate reclaim is also driving the need for advanced automated inspection. As supply is strained and material costs rise, the sapphire reclaim business is becoming more prevalent — whether for captive consumption or merchant supply. The reclaim business is even more dependant on OSA inspection as reworked material is highly susceptible to yield impacting defects.

Optical surface analyzer technology is setting the benchmark for automated inspection of sapphire substrates, and is emerging as the industry standard for overall sapphire quality control. HBLED device manufacturers and sapphire substrate suppliers are together converging on OSA inspection specs for quality assurance. Moreover, manufacturer's utilizing OSA technology are the beneficiaries of higher quality sapphire substrates passing distinct inspection specs.

Optical surface analysis technology enables manufacturers and suppliers to automate defect inspection and define objective-controlled process control limits. OSA technology can be employed at incoming substrate inspection, post-clean inspection, and after epi and film deposition processes.

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Wafer-scale approach sim

Hermetic wafer-level packaging can cut the cost and weight of III-V MMIC protection and offer a route to combining different types of chip in a single compact module, say **Patty Chang-Chien**, **Xianglin Zeng**, **Yun Chung** and **Jeff Yang** from Northrop Grumman Space Technology.

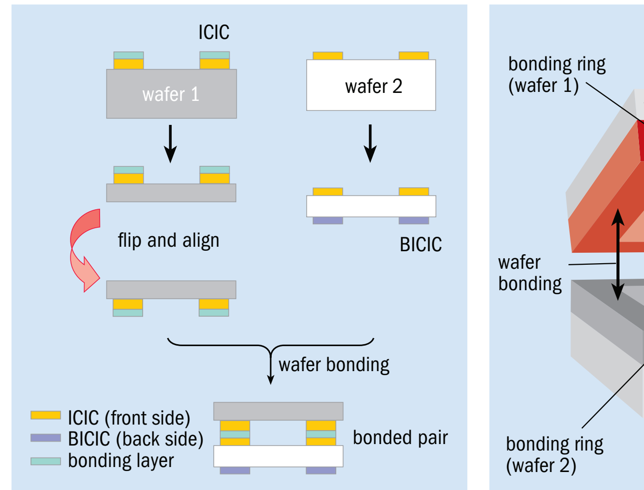
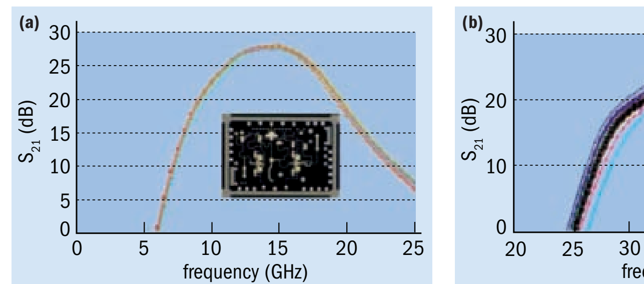


Fig. 1. (above left) Low-temperature wafer bonding involving the addition of together. **Fig. 2.** (above right) The circuits are protected by hermetic cavities used its wafer-level packaging technology for the fabrication of a range of lo



Tough environments are the norm for RF electronics employed in space and military applications. Moisture, mechanical vibrations and temperature extremes can all degrade performance, so chips are protected by packages featuring airtight hermetic sealing that improve device lifetime and reliability.

Traditionally, the process used for making sealed packages begins with semiconductor chip fabrication, which includes a passivation step to provide minor protection. These "bare" MMICs are then packaged in ball grid arrays – an assembly of pins for parallel soldering to devices – before being placed in integrated microwave assemblies (IMAs) for hermetic sealing at the submodule level. Sealing is carried out on each unit after several MMICs have been mounted on a board. Electrical connections to the board are then made by wire bonding, or use of the ball grid array, and the device is finally subjected to a series of pre- and post-seal tests to assess electrical, mechanical and hermeticity properties.

Unfortunately, this approach suffers from a major weakness. If any device does not meet its specification, or if any IMA fails a test, then the IMA has to be broken apart and any offending parts replaced. Consequently, this process for hermetic packaging is costly, labor intensive and time consuming.

However, substantial cost savings are possible by employing the hermetic seal at the wafer level instead of at the IMA stage. Hermeticity is then restricted to the sensitive, high-performance microelectronics that are sealed at the wafer level in die form using batch fabrication. This is cheaper, because there are fewer assembly steps and tests, and it has the added benefit of compatibility with non-hermetic IMA materials that are cheaper, lighter and easier to use. Failed chips are also easier to deal with because bad parts can be replaced and several steps associated with conventional packages are avoided, such as resealing and testing of the IMA module. The removal of seam sealing also simplifies system diagnostics, which cuts module-level test times and costs.

The bulky, heavy packages and metal housings used in conventional modules to meet the IMA's hermeticity requirement can also be eliminated with wafer-level packaging (WLP). This is a major plus point for space applications as it cuts the system's weight and launch costs – an IC-based hermetic WLP transceiver can weigh just 100th of an equivalent packaged with ball grid arrays.

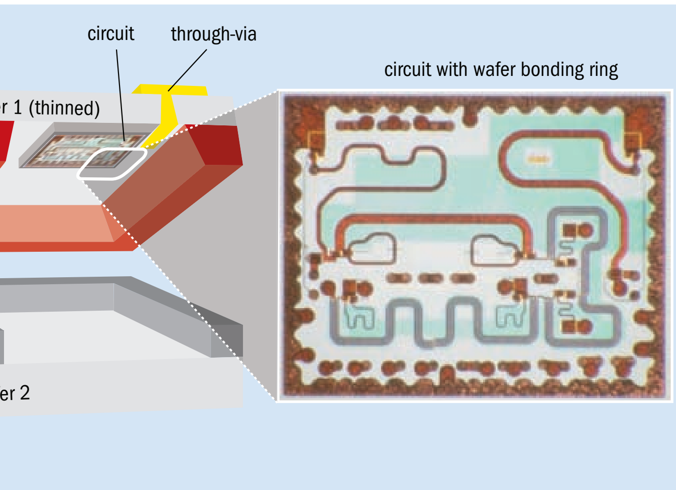
WLP techniques are already being employed in silicon-based systems, such as the accelerometers in automobile air-bags. At Northrop Grumman Space Technology, Redondo Beach, CA, we have extended this technology to high-performance, high-frequency RF MMICs made from III-Vs. This process features new wafer-level bonding techniques.

We have focused our process development around four key issues: process and device compatibility, hermeticity, package reliability and cost.

Heat can degrade MMICs and modules, so this must be avoided during packaging. High-temperature wafer bonding leads to thermal stresses between dissimilar materials and if MBE-grown III-V circuits get too hot, thermal diffusion between epilayers compromises device reliability. To prevent these problems, we have developed a process that combines the low-temperature solder bonding with the thermodynamic stability of metal alloy bonding.

About the authors
Patty Chang-Chien (top left; patty.chang-chien@ngc.com), **Xianglin Zeng** (top right), **Yun Chung** (bottom left) and **Jeff Yang** (bottom right) wish to thank the entire engineering, processing and testing team at NGST's Microelectronics Product Center for MMIC fabrication, package fabrication and testing.

plifies hermetic packaging

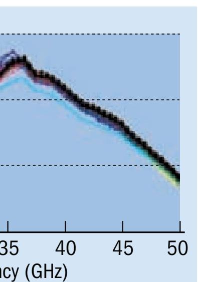


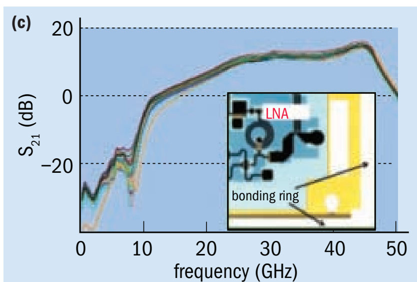
acavity interconnection layers is used to fuse the substrate and cover wafers t can be accessed by through-via holes. **Fig. 3.** (below) Northrop Grumman has oise GaAs HEMT amplifiers operating in the Ku **(a)**, Ka **(b)** and Q-bands **(c)**.

Military testing

Northrop Grumman's WLP packages have been evaluated with various military tests.

- Helium leak tests probed the hermeticity of vias and WLP packages. The MIL-STD 883 F test (method 1014.9, condition A4 [flexible method]) stipulates a leak rate for the via of below 1×10^{-8} atm-cm^3/s. Our devices measured 2.2×10^{-9} atm-cm^3/s, which was close to the detection limit of the apparatus. Group testing of up to 30 packages was a success (MIL-STD 883, method 1014.9, condition A2 [flexible method]), with the pass mark of less than 5×10^{-8} atm-cm^3/s being bettered on all occasions.
- Pyroshock and vibration tests (MIL-STD 883, method 2002.4, condition B, and method 2007.3) assessed the package's mechanical integrity and found no changes in functionality and performance.
- Thermal cycling from −55 to 125 °C for 50 cycles (military standard 883, method 1010.8, condition B) produced no noticeable changes in the performance of the device.
- Tests in an environmental chamber at 85 °C and 85% humidity evaluated environmental integrity and found no evidence of electrical degradation.





Rugged topographies are not a problem and high bonding and interconnect yields are possible at 180 °C. This technology is also versatile – it can be used for standard assembly processes, such as solder bumping and the bonding of multiple wafer stacks – which makes it suitable for packaging MMICs and multiwafer heterogeneous integration.

High-quality hermetic seals are essential for MMIC packaging because they enclose devices in an environment that is free from moisture and undesirable organic materials. This is particularly important for packages immersed in liquid or high-humidity environments, which often fail due to moisture penetration and condensation on the active regions of devices. Out-gasing can jeopardize cavity hermeticity, ruling out the use of certain polymers and materials. Oxygen can also degrade MMIC performance, although this can be avoided by filling the cavity with an inert gas, such as nitrogen.

Reliable packaging is essential for long-term performance, so sealing must be chemically and physically stable over the product's lifetime. A mismatch between the material properties of the packaging and device – which come together during wafer bonding – can lead to cracking, deformation and an unstable MMIC with noisy performance. To combat this, the packaging must employ an appropriate design that is compatible with low-temperature processes.

Cost is obviously a key issue. This can be driven down with a high-volume batch fabrication and the use of mature packaging methods that only require a few processing steps. Although the WLP process is expensive at the MMIC/device level, this is outweighed by the savings made at the submodule or module level, where time-consuming assembly and tests dominate the cost.

Our WLP process, which is suitable for batch fabrication and single-module production, starts with substrates and cover wafers (figure 1). Both are processed with standard MMIC fabrication techniques, before matching metallic rings are added using intracavity interconnection (ICIC) layers. A bonding layer is applied to the top of one of the wafer's ICIC layers, before backside processes produce ground vias to complete MMIC fabrication. Low-temperature bonding follows, resulting in circuitry that is encapsulated in sealed cavities between the wafer surfaces and bonding rings. These chips are then accessed by through-wafer vias formed by our MMIC backside fabrication processes. Vertical rather than lateral RF feed-through approaches are adopted to minimize the parasitic feed-through losses at high frequencies.

To demonstrate our technology's capability,

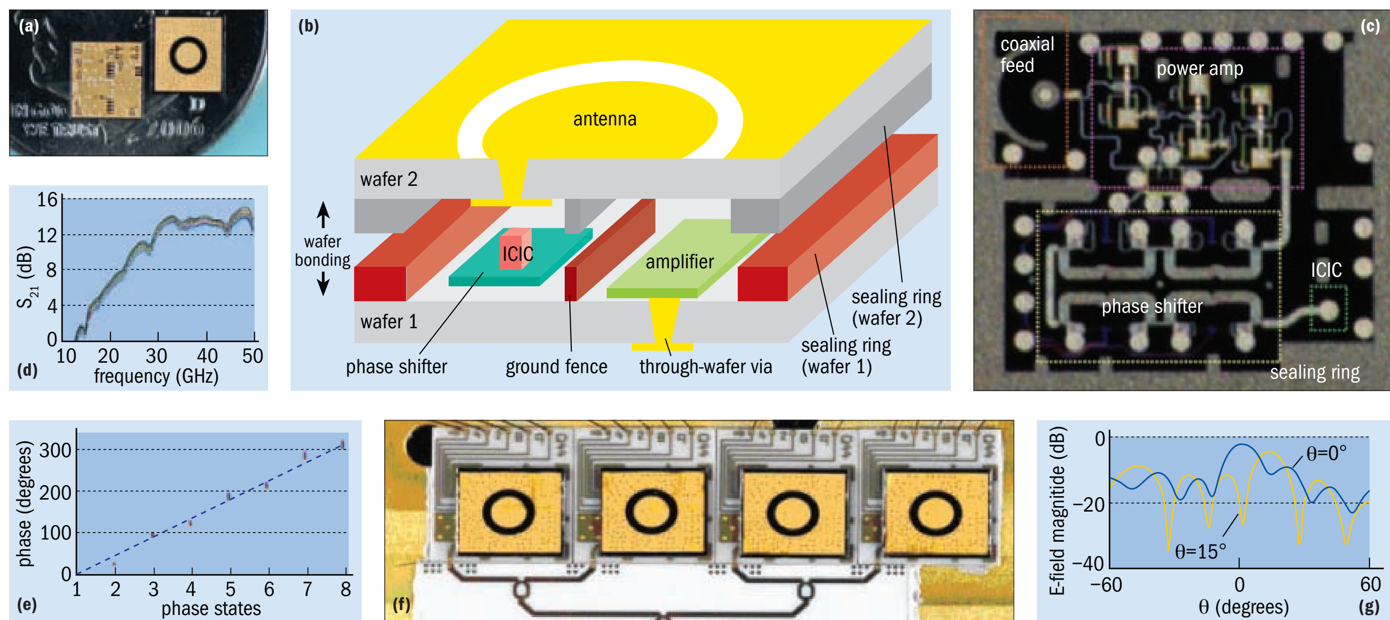


Fig. 4. (above) Northrop Grumman has built tiny packages with its wafer-level technology that feature an antenna and an IC **(a, b, c)**. On-wafer probe measurements reveal key characteristics of the Q-band GaAs HEMT and the 3-bit phase shifter, respectively **(d, e)**. Four of the modules can be combined to form a four-element linear electronically steerable array that produces beam patterns that demonstrate the system's full functionality **(f, g)**.

we have also built MMICs operating from the UHF-band to the W-band. Wafer-level testing demonstrates the complete compatibility of our technology with existing III-V production processes and its suitability for high-frequency, high-performance RF MMIC packaging (figure 3, p16).

Hermetic sealing of individual MMICs can deliver submodule or IMA assembly cost savings, but further reductions and performance enhancements are possible by combining multiple chips/functions within a single package. This can be delivered by combining multiple chips with the same III-V fabrication technology into a multifunctional chip; or by uniting different semiconductor technologies in a vertical stack; or by building more complicated assemblies that draw on both of these themes.

All of these approaches can lead to three-dimensional heterogeneous ICs that benefit from the interplay of different devices. For example, high-performance, low-noise InP amplifiers can be built into circuits also featuring GaAs or GaN power amplifiers without any performance degradation. This involves a relatively simple, low-cost process, thanks to shared packaging steps. In fact, it is possible to extend this heterogeneous integration capability by uniting silicon-based digital circuits with RF MMICs using the same processes.

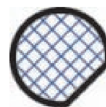
This type of wafer-level packaged IC can deliver significant cost and system-level performance enhancements over today's state-of-the-art packaging, which relies on multilayer, densely packed ball grid array modules. The WLP process can bring different circuits into close proximity without the need for additional board material and MMIC pick-and-place assembly. In addition, fewer components and component-to-component interfaces and interconnections are required, such as wire bonds. This ultimately cuts ohmic loss and wire-induced parasitics in the ICs, which is a significant benefit for high-frequency circuits.

To show this heterogeneous integration capability, we have built an integrated antenna RF front-end module. The assembly consists of a GaAs HEMT, a Q-band power amplifier, a 3-bit phase shifter and ICICs that provide RF and DC routings. A ring slot antenna is integrated on the outside of the package and is connected to the circuitry by a through-wafer via on the cover wafer and an ICIC within the cavity. Tests confirmed the expected performance levels and were used to construct a four-element linear electronically steerable array (figure 4).

A variety of WLP circuits have been tested under criteria laid out by the US military. They passed all of the tests, which are designed to assess mechanical, thermal and environmental integrity and hermeticity (see box "Military testing" for details, p17).

To date, we have demonstrated the functionality and compatibility of our WLP technology with many III-V technologies, including GaAs and InP HEMT and HBTs, and antimony-based HEMTs. We are now extending our work to cover silicon and GaN circuitries. Currently, multiple projects are underway to develop our WLP technology; to investigate multilayer, multisemiconductor technology module construction using this WLP assembly technology; and to incorporate more functional blocks into compact integrated RF front-end modules.

Our current WLP processes produce devices with a DC functional yield exceeding 99%, while the RF yield is typically limited by the particular semiconductor technology employed for packaging within the cavity. Our packages also have excellent mechanical and thermal robustness, according to various military tests, and we are now conducting long-term device/package reliability tests to qualify the technology for military and space use.



GaN

Argon aids p-doping in GaN LEDs

If you want p-type GaN with sharp doping profiles and low resistivity, then consider switching your carrier gas from hydrogen to argon, say **Vladimir Dmitriev** and **Alexander Usikov** from Technologies and Devices International.

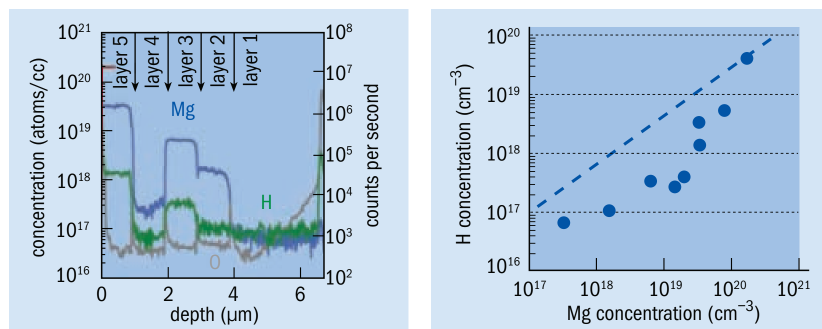


Fig. 1. (left) SIMS measurements on multilayer structures with intentional magnesium doping in the second, third and fifth layers reveal abrupt doping profiles and little magnesium in the unintentionally doped fourth layer. The sample surface is shown to the left. **Fig. 2.** (right) The magnesium doping concentration is higher than the hydrogen background, according to SIMS. The dashed line corresponds to an equal atomic concentration of magnesium and hydrogen.

Although GaN LEDs are a great success, the MOCVD process used to make them cannot deliver p-type regions with ideal characteristics. What is needed for really bright emitters, such as those targeting solid-state lighting, are heavily doped p-type regions with minimal electrical resistivity and abrupt doping profiles in the epilayer stack. But today's processes produce high-resistivity material that hampers current spreading, alongside poor ohmic contacts that increase the operating voltage and prevent high drive currents.

This state of affairs stems from the inherent properties of p-type GaN and AlGaN grown by MOCVD using the standard dopant – magnesium. These nitrides have a high electrical resistivity, which is partially addressed by post-growth thermal activation. However, even after this treatment, p-type GaN still has electrical resistivities of 0.1 Ω-cm or more, which limits the efficacy of the brightest LEDs, due to the high operating voltages required.

The high electrical resistivity probably results from passivation by hydrogen – the standard MOCVD carrier gas. Post-growth thermal activation breaks the magnesium–hydrogen complexes and boosts electrical conductivity, although if too much magnesium is added it can degrade material quality.

Magnesium-doped nitrides grown by MOCVD also suffer from a "memory effect". This dopant resides in the growth chamber after shutting the line valve and is then absorbed in subsequent growth layers that should be free of magnesium.

To address these issues we have been developing a growth process that uses no pure hydrogen. This effort, which has been funded by the US Department of Energy's Solid-State Lighting program, uses a HVPE process that delivers faster growth rates and lower dislocation densities. NH_3 and HCl are employed as the active gases and argon as the carrier.

MOCVD growth with argon as the carrier gas would not be as effective, because this would demand far higher ratios of NH_3 to the group-III source, which would lead to more hydrogen in the grown layer.

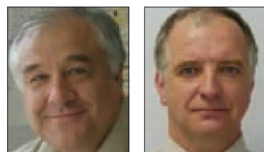
Our proprietary multiwafer HVPE reactor was used to deposit p-type GaN layers on (0001) *c*-plane sapphire at typical rates of 1 μm/min and 1050 °C. The group-III source was high-purity gallium, and magnesium provided the dopant.

We produced GaN layers with thicknesses of 3–15 μm and magnesium atomic concentrations of 2×10^{16} cm^{-3}–2×10^{20} cm^{-3}, according to secondary ion mass spectrometry (SIMS) measurements. All epilayers had a smooth surface, and X-ray diffraction measurements showed that high doping concentrations did not affect crystal quality. Activation was not required to produce p-type conductivity in the samples. Capacitance-voltage (C-V) measurements with a mercury probe showed p-type conductivity for magnesium atomic concentrations of 1×10^{17} cm^{-3}. C-V tests also revealed net acceptor concentrations (number of acceptors minus number of donors) as high as 3×10^{19} cm^{-3}, a level that is suitable for forming a good ohmic contact.

Electrical measurements on layers with carrier concentrations in the range 4×10^{17}–1.5×10^{18} cm^{-3} revealed resistivities of 0.02–1.00 Ω-cm. Hole mobility was at least as good as those for MOCVD-grown material, which indicates that HVPE-grown LEDs should have excellent current-spreading characteristics. SIMS measurements also show that our material is less susceptible to the memory effect (figure 1).

The high conductivity and net acceptor concentration of our material results from higher levels of magnesium than hydrogen (figure 2). Minimizing hydrogen concentrations is critical for very high doping, according to our measurements on two magnesium-doped samples with atomic concentrations of $(1–3) \times 10^{19}$ cm^{-3}. A sample with a hydrogen concentration of 4×10^{17} cm^{-3} had a net acceptor concentration of 1.2×10^{19} cm^{-3}. The film with a hydrogen concentration of 1×10^{18} cm^{-3} had a net concentration of just 1.3×10^{18} cm^{-3}. The variations in hydrogen concentration caused magnesium in one sample to be almost entirely active and in the other to be only 10% active.

We have also demonstrated the versatility of our HVPE growth approach. "Upside-down" LEDs that cannot be made by MOCVD were fabricated on p-GaN-on-sapphire templates. These structures contained InGaN layers with 15–30 mole % of InN and produced emissions in the 450–515 nm range.



About the authors
Vladimir Dmitriev (left) was TDI's president and CEO. He passed away on January 6, 2008. **Alexander Usikov** (right) is TDI's R&D director and senior scientist. His current research focuses on the physics and novel technology of III-N semiconductors. The authors greatly appreciate LED processing assistance provided by the Army Research Laboratory and Palo Alto Research Center. They also thank the US Departments of Energy, Commerce, and Defense for financial support, and the team of engineers and scientists at TDI for their research efforts. Oleg Kovalenkov, Vitaly Soukhoveev and Vladimir Ivantsov made significant contributions to this work.

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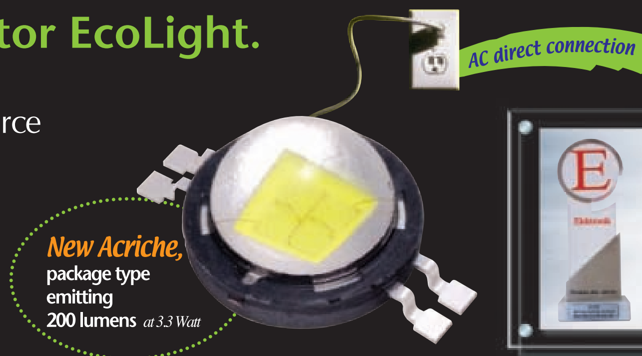

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Quantasol exploits quantum effects

Photon recycling and quantum wells enhance single-junction solar cell efficiencies and will boost tandem cell performance to triple-junction levels, say Quantasol's **Kevin Arthur** and **Keith Barnham**.

Rising concerns over global warming and energy security are fueling a ramp in solar cell manufacture. Global production is increasing at 47% a year in terms of power, and independent market analyst Peter Lynch claims that this industry is now growing faster than any other.

This rapid expansion has led to a temporary shortage of polycrystalline silicon, the dominant material used for making solar cells. Supply of this semiconductor has struggled to keep up with recent demand and this has opened the door for thin-film technologies, such as amorphous silicon-on-glass. These alternatives offer a lower cost-per-unit-area and a faster production process, but have the drawback of low efficiencies. While traditional silicon solar cells can typically deliver efficiencies of 15%, thin-film versions can only yield single-digit values.

Martin Green from the Photovoltaics Research Center at the University of New South Wales, Australia, claims that any further reduction in the solar cell's key metric – the dollar-per-peak-watt cost ($\$/W_p$) – will be restricted by the large, fixed, balance-of-systems costs of a photovoltaic power system, such as the inverter that converts the electricity from DC to AC form. So, the best way to reduce the $\$/W_p$ ratio is to use more-efficient cells.

The high-efficiency triple-junction solar cells produced by the likes of Emcore and Spectrolab offer one solution. These devices were mainly developed for space applications where high costs are not a concern, but they are now starting to be deployed into high-concentration systems that focus sunlight onto small cells with cheap lenses and mirrors.

The market for these systems is being stimulated by feed-in tariffs for renewable electricity. These have recently been introduced in a number of countries, with Germany and other parts of Europe leading the way. However, the booming market is also attracting other forms of innovative concentrator technologies, such as large dish systems and novel solar combined-heat-and-power systems.

At Quantasol – a UK spin-out of Imperial College London, based in Richmond upon Thames – we are also planning to enter this market with our patented high-efficiency concentrator cells. These devices share the hallmarks of the triple-junction cell – high efficiencies at high concentrations. However, we avoid problems with material dislocations by strain balancing the entire epistructure. As a result, we can offer unique features that boost efficiency, such as photon recycling and hot-electron effects.

SOLFOCUS

Quantasol's cells are designed for concentrator systems, such as those produced by SolFocus.

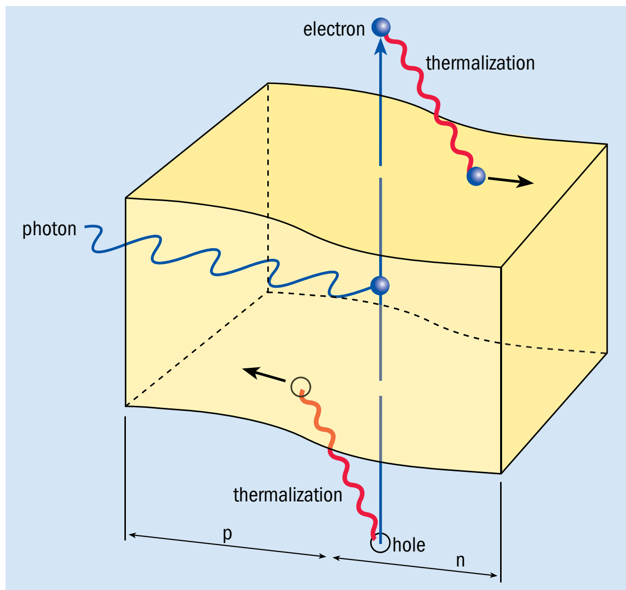
One of the primary advantages of our quantum well-based solar cells is the wider spectral absorption range. This extension occurs in the infrared, with absorption of sunlight that would pass straight through a conventional GaAs cell.

If our cell material quality is sufficiently high, photons with energy greater than the host bandgap will "see" an epistructure that behaves like a conventional GaAs cell (figure 1a, p22). For radiation with that energy, incident light is absorbed and an output current results from the separation of electron-hole pairs by the junction's built-in electric field.

However, unlike a conventional cell, our design also absorbs photons that have an energy that is less than the GaAs bandgap (figure 1b, p22). The additional electrons and holes that result have a very high probability of escaping from the wells and boosting the output current.

For our design to be effective, the material quality must be high, while the structure must contain a sufficient number of quantum wells. That is because the additional current must be delivered with a minimal reduction in voltage, so that the output power, the product of these two quantities, increases.

This growth challenge is compounded by a lack of low-bandgap alloys that are lattice matched to GaAs. InGaAs is not suitable, even though it is used in the quantum wells of the low threshold-current lasers, because the larger atomic spacing of InGaAs



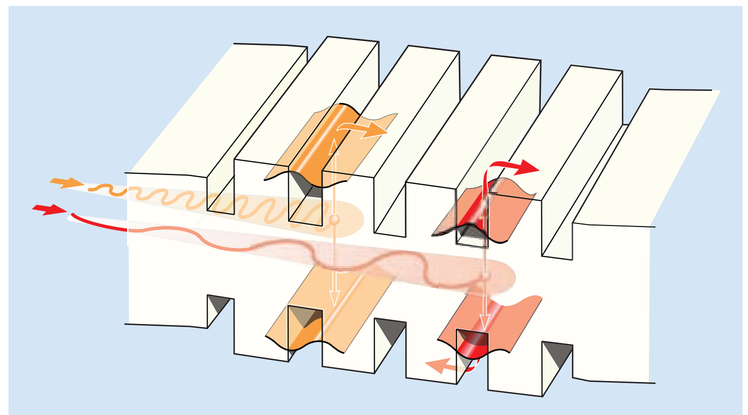
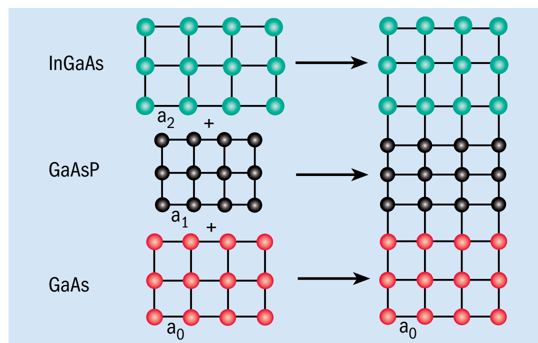


Fig. 1. (a) (left) Conventional solar cells can only generate power from photons that have energy above the GaAs bandgap. Such photons (shown in blue) are absorbed and create free electrons and holes that thermalize to the band edges. These carriers are separated by the built-in field to produce an output current. **(b)** (above) When quantum wells are added into the structure, photons with energy that is less than the bandgap of the host cell can also be absorbed to form confined electron-hole pairs in the well.



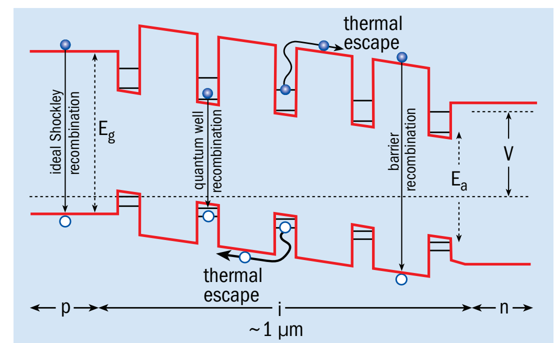


Fig. 2. (right) Large numbers of quantum wells are needed to deliver sufficient absorption. An InGaAs/GaAs structure would lead to too much strain so Quantasol employs a strain-balanced structure with GaInP barriers that are several tens of nanometers thick and InGaAs wells that are a few nanometers thick. **Fig. 3.** (far right) Quantasol's strain-balanced approach can produce epistructures with up to 65 quantum wells in the intrinsic region.

leads to compressive strain in the active region. This works for a laser requiring a few quantum wells, but is unsuitable for solar cells that demand 50 wells to provide sufficient absorption in the undoped region.

Our approach avoids this issue and draws instead on the work carried out by ourselves, co-founder Massimo Mazzer, colleagues at Imperial College, and John Roberts, a co-founder of Quantasol who is also a researcher at the EPSRC National Centre for III-V Technologies at the University of Sheffield, UK. By sandwiching GaAsP barriers between InGaAs wells, we can form structures that balance the tensile and compressive strain (figure 2). Characterization techniques, such as X-ray diffraction and electron microscopy, reveal that the material quality is excellent and free from crystal dislocations. Up to 65 quantum wells can be grown in an intrinsic region using patent-pending growth recipes.

Our technology promises significant efficiency enhancements in both single-junction and tandem solar cells. Carrier loss mechanisms are kept to a minimum by producing good-quality material and employing high-bandgap semiconductors in the p-type, n-type and barrier regions (figure 3).

The only loss mechanism that cannot be avoided is quantum-well radiative recombination, which is the dominant loss mechanism at the high current levels employed in concentrator systems. This loss results from the photons generated by the recombination of conduction band electrons in the bottom of the quantum well with valence band holes in the top of this well (figure 4, p23). Fortunately, the unique feature of our particular design means that these photons will only be absorbed by the substrate. So if a mirror is inserted between the quantum wells and the substrate (figure 4, p23), a high proportion of the photons generated can be reabsorbed in the wells and contribute to the output current.

The way that we exploit this in our first product is to grow the device on top of a Bragg reflector (DBR). This mirror can reflect one-third of the photons that would be lost and convert them into current-generating carriers.

We think that this feature gives us the greenest photovoltaic cells around – we even recycle our waste photons! This photon recycling has enabled us to produce single-junction cells delivering more than 27% efficiency at a concentration factor of up to 500. This is just shy of the record for any concentrator single-junction solar cell, which stands at 27.8% for a concentration factor of 216.

We are also working on another type of mirror, a "chirped" DBR, which will improve the proportion of reflected photons. Calculations show that this

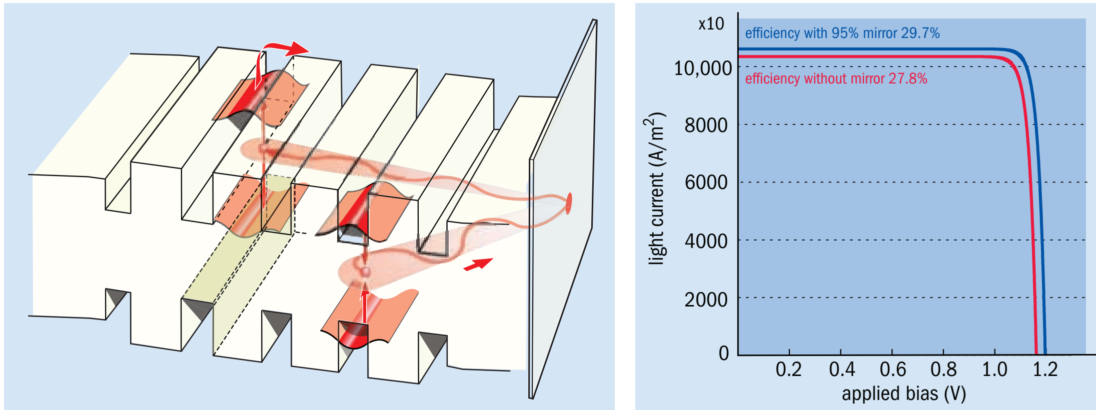
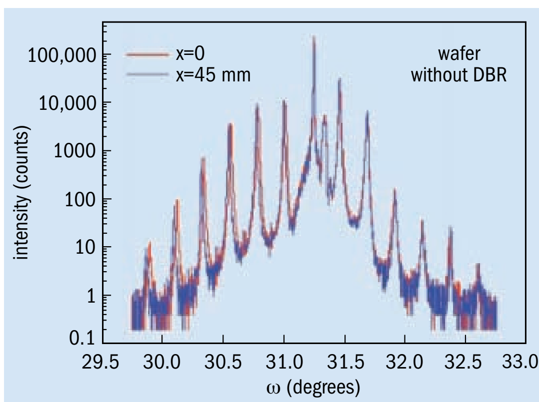


Fig. 4. (above left) Photon recycling can reduce the power losses produced by unavoidable radiative recombination. Some of the photons generated by this process can be reflected by a mirror beneath the wells and reabsorbed in the quantum wells, leading to increased power output. **Fig. 5.** (above right) Calculations suggest that photon recycling can boost the efficiency of Quantasol's devices at 500-sun concentration. **Fig. 6.** (below) Quantasol's epistructure can be grown on high-throughput reactors at commercial foundries. X-ray diffraction rocking curves exhibit narrow satellite peaks that are indicative of good multiquantum-well quality. Uniformity is also excellent, according to the similarity of the curves at the wafer's center (x = 0) and near to its edge (x = 45 nm).



could lead to single-junction efficiencies close to 30% at a concentration factor of 320 (figure 5).

Our strain-balanced design was developed on research reactors at the University of Sheffield with a maximum capacity of three 75 mm wafers. As this throughput is insufficient for high-volume manufacturing, we have also scaled up our process at a UK-based epiwafer foundry. Subsequent device processing is also carried out off-site, alongside important lifetime qualification tests at the Centre for Integrated Photonics, Ipswich, UK.

Our single-junction cell's epistructure is relatively complicated, as it consists of a thick quantum-well stack and a DBR region, so we were very encouraged by the good material quality produced on the first attempt in an 8 × 4 inch reactor platform. This material had a similar quality to that grown on the research reactor and an excellent quantum-well uniformity across the wafer (figure 6).

We will now develop production processes for tandem cells that can deliver even higher efficiencies. They feature an InGaP-based top cell epitaxially grown on a GaAs-based cell with a lower bandgap. Both cells contain quantum wells that extend the spectral response. In a tandem cell the two subcells are connected in series and their current output can be tuned by adjusting the quantum wells.

The Quantum Photovoltaic group at Imperial has demonstrated that quantum wells in the GaAs cell alone can produce tandem efficiencies above 30%. We are targeting a production efficiency of 35% at 500-sun concentration by mid-2008. This is comparable to the performance of triple-junction cells.

Our development of single and tandem cells with quantum wells is backed by £1.35 million ($2.7 million) of seed funding from investors, including Imperial Innovations and Low Carbon Accelerator. We aim to raise a significantly larger series A round in spring 2008 to finance high-volume manufacturing capability and capacity development, alongside significant additions to product development, operations and global customer support. We are planning to continue to pursue a "fab-lite" business model to keep costs low and enable a quick ramp up in production, which will involve the outsourcing of epigrowth and cell processing. Although we are currently working with UK partners to fulfill these roles, we are keen to develop overseas partnerships to provide additional production capacity.

We believe that our approach will allow us to tailor our designs to meet the precise needs of our customers. We are also free from any restrictions that face terrestrial concentrator solar-cell manufacturers that also serve the space and/or military sectors. Alpha-sampling of our single-junction cells will begin soon, with tandem cells to follow in the first half of this year. ●

Further reading

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About the authors

Kevin Arthur (left) (kevin.arthur@quantasol.com) is Quantasol's chief executive officer. He has nearly 25 years of experience in the semiconductor manufacturing industry and has previously held the roles of vice-president of global sales at Mitel, and director of European sales at Raytheon Semiconductor and TRW LSI Products. **Keith Barnham** (right) is Quantasol's chief technology officer. He is also Emeritus professor of physics and senior research investigator in the physics department at Imperial College London. He leads the department's quantum photovoltaics group, which has spent 15 years pioneering the application of quantum wells and quantum dots to photovoltaics.

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Four-pronged attack promises ultra-high efficiency lighting

Ultra-high efficacy white-light sources can be built by carefully mixing efficient blue, green, yellow and red LEDs, say Sandia National Laboratories researchers. **Richard Stevenson** investigates.

The efficacy of white LEDs is advancing at breakneck speed. In 2004 engineers were proud to quote values of almost 60 lm/W at 350 mA, but today the research record is more than 130 lm/W.

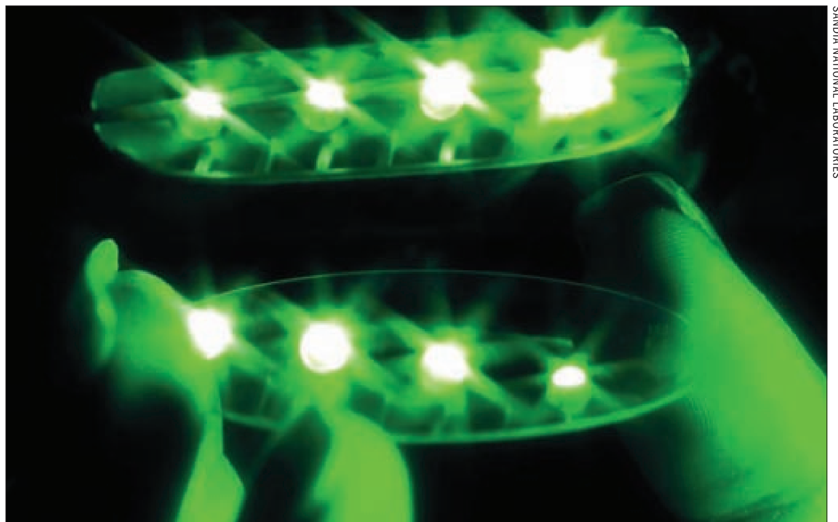
This lighting efficiency, which is almost double that of compact fluorescents, and an order of magnitude better than incandescents, has positioned the white LED as a very promising candidate for general lighting applications. However, further improvements could strengthen the case for solid-state lighting, while leading to substantial energy savings and reduced lighting bills.

Unfortunately, the headroom left for improving conventional white-LED performance is vanishing all the time. The process that turns blue or ultraviolet emission from a chip into yellow light via a down-converting phosphor wastes energy and ultimately limits efficacy. Nichia, for example, estimates a theoretical maximum of 263 lm/W for a phosphor pumped with blue light, and just 203 lm/W for an ultraviolet-sourced equivalent.

Higher efficacies are possible with alternative LED-based schemes, according to Jeffrey Tsao and colleagues at Sandia National Laboratories. This team has shown that it is theoretically possible to deliver efficacies of more than 400 lm/W at a color rendering index (CRI) of 90 by color mixing four carefully selected LEDs emitting at different wavelengths. A CRI of 90 is excellent, says Tsao, and would satisfy virtually all white-light applications.

At first glance this all seems very encouraging, but Tsao makes it clear that getting there is no cakewalk. For starters, electrical-to-optical power efficiencies of almost 100% are required to get close to the theoretical efficacy. And, although infrared lasers with efficiencies of 80% have been made, two of the wavelengths selected by Tsao, 530 and 573 nm, are in a region of relatively poor performance known as the "green gap". Even the best LEDs in this spectral range are incapable of delivering modest efficiencies (figure 1, p26).

Substantial improvements in the performance of green-gap LEDs are obviously required and the first step towards this involves establishing a clear understanding of what is hampering device output.



SANDIA NATIONAL LABORATORIES

Today's best green LEDs are highly inefficient and a substantial hike in performance is required if these devices are to be used in ultra-efficient white-light sources based on color mixing.

This question is a hot topic of debate within the scientific community and Tsao suggests that various types of defects could be playing a role.

The InGaN/GaN epilayers upon which these devices (and their blue brethren) are based are grown on foreign substrates, such as sapphire and SiC, which cause strain and high threading dislocation (TD) densities that are typically in the range 5×10^8 to $5 \times 10^9 \text{cm}^{-2}$. Despite these high defect densities, InGaN LEDs can produce external quantum efficiencies of up to 70%. However, some evidence suggests that defects might still limit efficiency: cathodoluminescence studies have revealed that TDs are non-radiative, while calculations have indicated that screw dislocations can induce strain fields that can localize one type of carrier and ultimately restrict radiative recombination.

In addition, point defects, such as gallium and nitrogen vacancies and carbon and oxygen impurities, could act as non-radiative recombination centers. Positron annihilation studies of GaN show that certain defects are incorporated with gallium vacancies, which can limit photoluminescence efficiency. Since point defects are more prevalent at

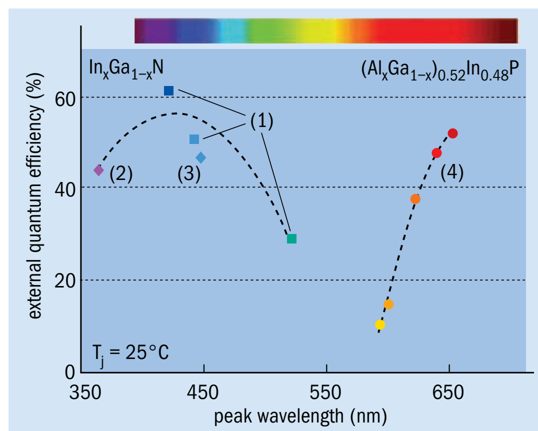


Fig. 1. Today's visible high-power LEDs are based on two material systems: InGaN, which is used for the blue and green emission; and AlGaInP, which covers the red part of the visible spectrum. State-of-the-art LEDs can deliver external quantum efficiencies of around 50% at certain wavelengths, such as 400 and 650 nm, but performance is poor in the green and yellow. The data come from Lumileds (1) InGaN thin-film flip chip LEDs at 350 mA, (2) InGaN vertical thin-film LEDs at 1 A, (3) InGaN conventional LEDs employing patterned substrates, and (4) AlGaInP truncated-inverted-pyramid LEDs.

lower growth temperatures – which are required for the higher indium compositions used to fabricate green and yellow LEDs – they may account for the lower LED efficiencies at longer wavelengths.

Green and yellow LED efficiency is also impacted by intrinsic polarization fields, which get stronger with higher indium content. The polarization helps to red-shift the emission, but the benefit is offset at higher drive currents by carrier-induced screening of the internal fields. This means that the emission wavelength varies with temperature, which is a major hindrance for color-mixing approaches.

One promising route that could overcome the polarization-related problems involves a switch to growth on GaN's non-polar planes. Work in that direction is still in its infancy, but researchers at the University of California, Santa Barbara, have made significant progress in the past year and produced devices with external quantum efficiencies of 45%. However, even if this figure can improve substantially, there will still be the problem of wafer size. These devices are made on Mitsubishi Chemical's 1 cm^2 substrates, and it is not yet clear whether this particular process could be scaled up to the larger diameters demanded by LED production.

InGaN templates that feature a thin InGaN layer on another material, such as sapphire, could also provide a basis for bright-green LEDs. Compared with conventional LEDs, this material system would suffer less from intrinsic polarization fields, and 2 inch diameter substrates are being sampled by Technologies and Devices International of Silver Springs, MD.

Another problem lurks, however: "As well as the green gap there is a red gap," said Tsao. The most common compound used to access this spectral range is AlInGaP, which is grown on GaAs. In the deep-red spectrum this material is estimated to have an internal quantum efficiency of almost 100% but performance drops rapidly at shorter wavelengths, such as 614 nm – the ideal emission wavelength for the orange-red component of a white-light source.

Tsao believes that this red gap may be an even harder problem to solve than the green one. The material system used for these devices has an indirect bandgap at a high aluminum content, and carriers start to occupy indirect valleys at compositions far removed from this cross-over point. Magnesium-doped layers in high-aluminum-content LEDs also suffer from electron leakage, which reduces internal efficiency. Lastly, the output falls off at the higher device temperatures associated with high-power LEDs and the emission wavelength is very temperature dependent.

According to Tsao, the great deal of effort already expended on addressing these issues has brought very little, if any, improvement. However, he believes that more radical approaches might be able to deliver a breakthrough. One possibility is the creation of hybrid systems that unite AlInGaP with a wide-bandgap material, and another is the development of InGaPN LEDs on GaP substrates.

Back to phosphors

Substantially improving the efficiency of 530, 573 and 614 nm LEDs is going to be tough, to say the least. However, it might be possible to produce an ultra-efficient white-light source by using different combinations of chips and phosphors. "If you could hit a home run by addressing the green gap, through the use of a primary semiconductor like InGaN, then maybe you could use a phosphor for the red, [alongside a blue LED]," explained Tsao.

This approach might seem absurd, since the motivation for moving on from the blue LED and yellow phosphor is the elimination of down-conversion losses. However, energy loss can be minimized if there is just a small difference in wavelength between the excitation source and the phosphor's emission – the case for a green chip and red phosphor.

Tsao and his colleagues have considered several different combinations of chips and phosphors, and made calculations assuming 95% conversion efficiency, less a Stokes down-conversion loss. Using a combination of red and blue emitters and a broad-emission, green phosphor can deliver an overall efficiency of 70% (286 lm/W) if the primary emitters are 80% efficient and the red emission is at 615 nm. But if this source is pushed out to 626 nm, the primary semiconductors must be 90% efficient to hit the same overall efficiency.

What's clear is that it's going to take substantial improvements in LED technology to make ultra-efficient white-light sources, regardless of whether they are based on a combination of different colored LEDs, or a mixture of LEDs and phosphors. Achieving this will not only require advances in the materials themselves, but also improvements in extraction efficiency that could require the development of new device designs. The potential reward for these efforts is a great motivator, but the path to get there looks long and hard.

Further reading

J M Philips *et al.* 2007 *Laser and Photonics Review* **1** 307.

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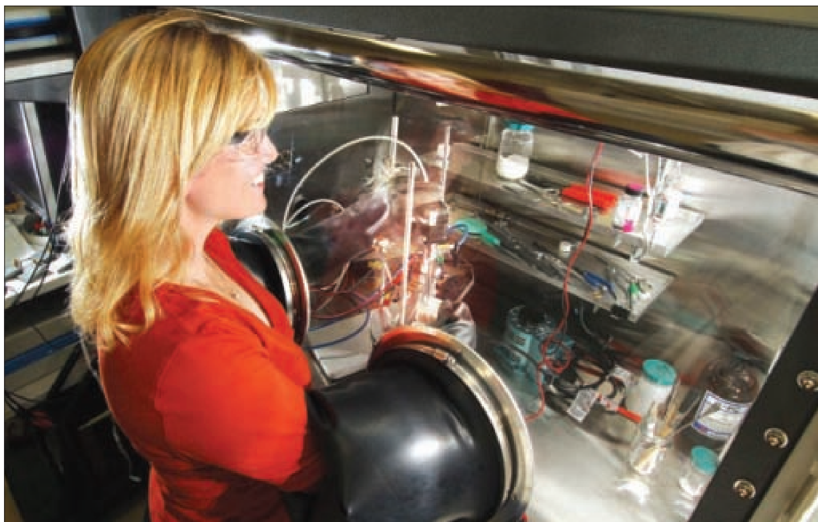
Electrolysis: a surprising method for scaling GaN crystal growth?

Conventional crystal growth methods don't work well for manufacturing GaN, but it is possible to produce small particles by electrolysis. With some minor changes this relatively fast process might be scaled to the manufacture of GaN substrates, says Sandia National Laboratories' **Karen Waldrip**.



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Initial electrolysis experiments have created particles of wurtzite GaN in test tubes. Rotating the seed crystal could scale the process to a size that's suitable for substrate production.

Native substrates are the ideal platform for GaN lasers and high-power LEDs. But manufacturing this material is tricky, to say the least. If standard melt-based techniques are employed, bulk growth of high-quality single-crystal GaN and InN demands incredibly high melting points and nitrogen gas vapor pressures. For GaN, nitrogen's vapor pressure at its equilibrium melting point exceeds 6 GPa and for InN it is even higher.

This melt-type approach also suffers from very slow growth rates that ultimately restrict the size of the boule that can be produced. Even the most successful exponents of this technique, the Unipress group at the Institute of High Pressure Research Center in Warsaw, Poland, can only produce crystals up to 25 mm in size.

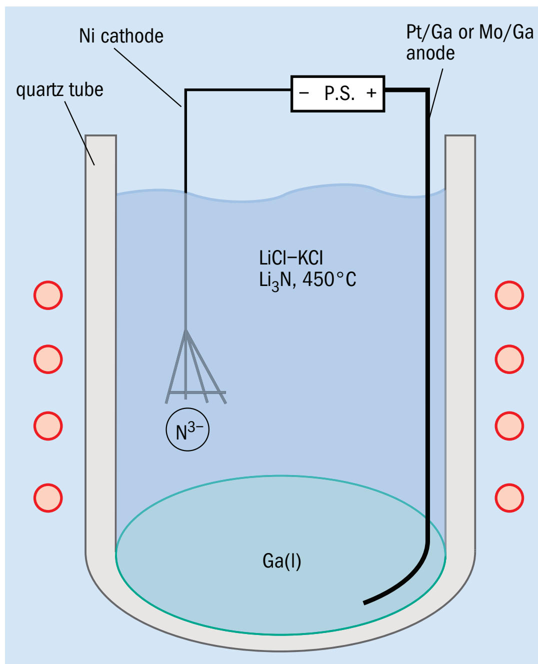
At Sandia National Laboratories in Albuquerque, NM, we have started to investigate an alternative process for producing bulk GaN – electrochemical solution growth. Funded by the Department of Energy's solid-state lighting program, this approach promises to produce bulk GaN from a molten salt. If the technique is successful, it will offer a fast and simple method for bulk growth of all forms of metal nitride, including InN, AlN and GaN. This is because growth from ionic precursors in solution can eliminate the high overpressures that are essential for conventional techniques, while simultaneously addressing the issue of slow kinetics.

One obstacle facing any solvent-based approach is the difficulty associated with dissolving GaN. The most successful approach to date is ammonothermal synthesis, which involves a liquid ammonia solvent and mineralizers, such as sodium-based materials, which are added to increase GaN solubility. The awkward conditions required for this form of growth make the technique difficult to scale, so a batch approach is often adopted, with numerous seeds added to each growth run. The requirement for forming liquid ammonia at the typical growth temperatures of 500–800 ºC is particularly irksome because this requires pressures of 4000–5000 atm. However, it is worth noting that significant progress has been made through refinements to the growth apparatus. Fumio Kawamura and co-workers from Osaka University, Japan, have managed to produce 2 inch material by this method.

The traditional method for making other refractory materials, such as SiC and oxides of magnesium, also tend to require precursors to be dissolved at high temperatures. With this approach, the solid crystal forms as the solution cools. High temperatures are needed at the start, so that as the crystal grows and the precursor concentration falls, lower temperatures can be introduced to maintain the supersaturated solution and ultimately ensure continual growth. But there is an inherent drawback – it is not possible to use the ideal crystal growth temperature throughout the process.

A key advantage of our approach is that it avoids all of these problems and forms precursors *in situ* by electrochemical means. GaN is difficult to dissolve in molten chloride salts, but its ionic precursors are highly soluble and these can be continuously formed in solution by oxidizing gallium metal and reducing nitrogen gas. This means that the molten chloride salt acts as both a solvent and an electrolyte.

A key part of our process is a nitrogen reduction reaction to form negatively charged nitrogen



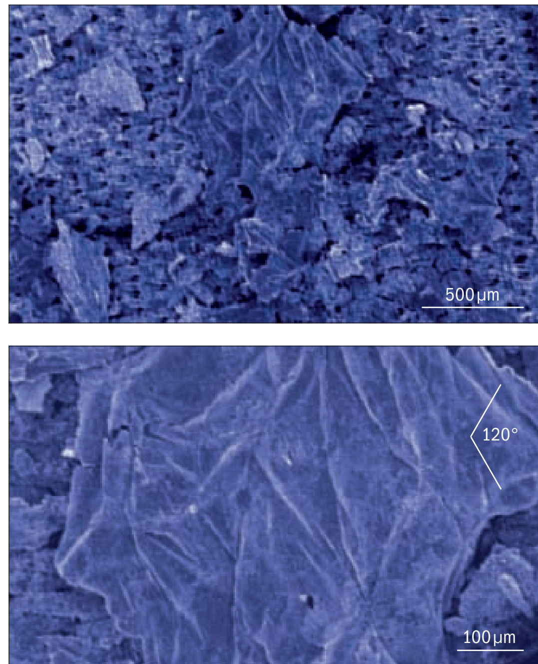


Fig. 1. (far left) Sandia's initial experiments were carried out in test tubes containing Li_3N dissolved in a LiCl–KCl eutectic solution. A Ni cathode and a Pt/Ga or Mo/Ga anode were placed into the test tube and connected to a potentiostat (P.S). Small particles of wurtzite GaN were formed, but they suffered from contamination that resulted from the design of the apparatus. **Fig. 2.** (left top and bottom) Scanning electron microscopy images of the GaN particles formed by electroplating reveal the material's wurtzite crystal structure.

ions. This reaction has previously been studied by Takuya Goto and Yasukio Ito from Kyoto University, Japan. They have demonstrated that it is possible to continuously reduce nitrogen gas to N^{3-} ions in a molten chloride salt at 450 °C. However, they had some very different applications in mind from GaN growth. Nuclear fuel reprocessing and hardness coatings were their main research themes, and they used the reduction reaction to electroplate nitride films on the surface of several transition, lanthanide and actinide metals.

If conversion of the nitrogen gas to ions is very slow, it could restrict the GaN growth rate. But it is possible to produce nitride ion concentrations of 2.9 mol% or greater in LiCl at 650 °C, according to the research by Wataru Utsumi and co-workers from the Synchrotron Radiation Research Center at Japan's Atomic Energy Research Institute. This means that if the creation of nitrogen ions is the growth-limiting process, then the GaN crystal's growth rate would still exceed 1 mm/h under diffusion-limited conditions. Such a high growth rate could be great news for our community – it could ultimately lead to cheaper substrates for low-cost, high-throughput commodity applications such as LEDs for solid-state lighting.

Early steps

We are aiming to use this type of reaction to develop a process for making large, high-quality bulk nitride crystals. Our preliminary experiments have focused on the reaction of nitride ions with gallium in molten salt. We used electrolysis to create GaN at the interface of a molten gallium pool (figure 1), with Li_3N providing the nitride ion source.

Under atmospheric pressure and an inert gas environment, we dissolved Li_3N in a fused LiCl–KCl eutectic solution at 450 °C. A current of 5 mA was swept for two hours to oxidize the gallium in the presence of nitride ions. The melt was then cooled to room temperature before the salt was rinsed away with deionized water and the gray insoluble GaN submillimeter-sized particles were filtered.

Scanning electron microscopy and X-ray diffraction (figure 2) revealed GaN with the required and expected wurtzite crystal structure. No photoluminescence was observed under optical excitation at 266 nm, but this was not surprising. We believe that this experimental configuration will produce lithium reduction at the cathode and gallium oxidation at the anode. Since lithium is a liquid at the growth temperature, and it is suspended above the gallium pool in this experimental configuration, it is possible that this metal could have dripped into the pool and contaminated the GaN. Or, the crystals might simply be defective due to the very low growth temperature (450–500 °C) that is used in this unoptimized experiment.

A light gray powder was also produced during our first attempt at making GaN from the reduction of nitrogen gas. The growth of larger crystals was probably hindered by the bubbling of nitrogen gas near the surface of the molten gallium pool in the small quartz test-tube reactor, which continually disturbed the growth surface.

However, even though this particular electroplating process is unsuitable for growing high-quality, thick, insulating crystals, the formation of GaN by this relatively simple method is very encouraging. This is because the ability to reduce nitrogen to nitride ions, which can be present in large concentrations in solution, could provide the key pathway to controlled bulk growth of large-diameter GaN.

Our next-generation reactor, which should enable

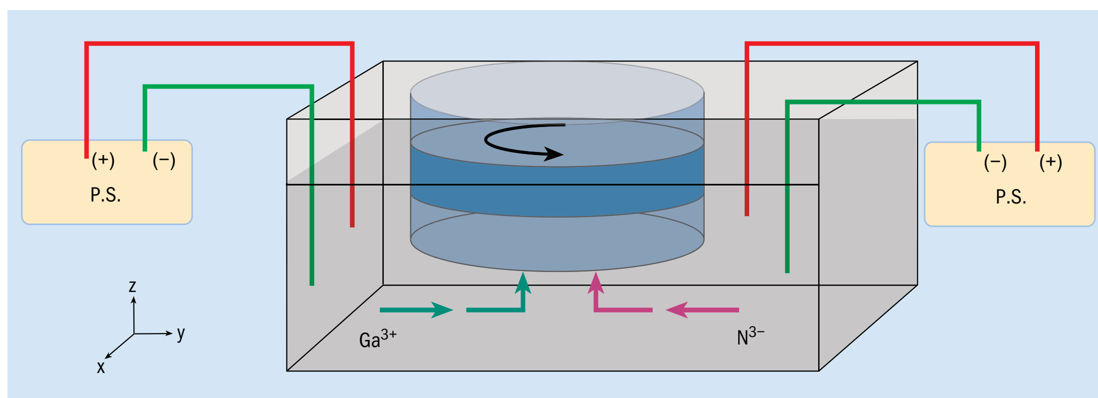


Fig. 3. Sandia has designed a new technique to overcome the limitations of the initial process. This involves the addition of a rotating seed crystal that prevents gallium or GaN plating at the electrodes. The scheme promises to maintain the concentrations of the ions in the solution during growth and should allow a boule to be pulled from the melt.

scaling of our GaN growth (figure 3), involves the formation of N^{3-} ions from nitrogen at the cathode, which is balanced by the production of Ga^{3+} ions from gallium at the anode. In a motionless solution this would cause gallium and GaN plating at the electrodes. However, this situation is avoided by a rotating seed crystal that is held just below the surface of the melt. This scenario is analogous to both the MOCVD vertical rotating disk reactors used for nitride growth and the rotating disk electrode, which has been used to study electrochemical reactions and diffusion rates of species in solution.

We plan to use our spinning seed crystal to control the fluid dynamics and draw the ionic precursors to the seed surface. These ions can then diffuse across the boundary layer and react on the seed's surface. Continuing the analogy with the rotating-disk MOCVD reactor, the electrodes substitute for the mass-flow controllers and the molten salt takes the place of the carrier gas.

This process promises stable growth because the ionic precursors can be introduced into solution at precisely the same rate that they are being consumed by the growing crystal. This process takes place at or near atmospheric pressure, so there are no obvious barriers that could prevent scaling of the crystal dimensions in the horizontal plane.

It should be possible to pull a boule from the surface of this melt because the growth region is close to the solution's surface. The precursors can also be replenished while they are being consumed, so their concentration should not waiver. This means that steady-state conditions are maintained throughout the process and the growth surface can be set to a constant, optimum growth temperature. If a thermal gradient is required, this can be introduced and maintained throughout the growth. In fact, we cannot see any barrier to prevent boule growth continuing for as long as is practically desired.

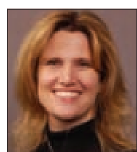
The process that we are proposing would have a reaction rate controlled by the nitride ion, which is encouraging from a reaction kinetics perspective. Our GaN electroplating experiments showed that GaN can grow at a rate of 1 mm in two hours under non-ideal conditions. This suggests that the reaction will proceed at a fast enough rate to yield high growth rates, but slow enough to prevent small crystals from forming in solution.

One potential pitfall for our process is the reaction of the gallium and nitrogen ions outside the boundary layer, rather than on the seed crystal. This reaction is a distinct possibility with the fluid flow patterns we expect to have in our crucible, but we believe that this scenario can be avoided by inserting a divider between the electrodes. This would isolate the gallium and nitrogen ions until they reach the boundary layer. Under such a scheme, separate potentiostats or power supplies would be used to control each reaction.

We are currently characterizing all of the electrochemical reactions – in particular the nitrogen reduction – as a function of temperature and several other relevant criteria. This will be followed by attempts to demonstrate GaN growth on a seed at the desired location in the melt. If this is successful, the last milestone will be to replicate this growth process on a high-quality template, such as a HVPE-grown seed crystal. This will require optimization of temperature, which will most likely have to be increased from 450 °C.

Under our current program, which is being funded by the National Energy Technology Laboratory, we will ignore the role of impurities present in the molten salt, and thermal management. Both of these factors could have a detrimental impact on growth quality. Nevertheless, the experiments that we have planned will determine whether our technique has the potential to deliver affordable high-quality, large-area GaN for our community.

Our technology has tremendous potential, and although it is still in its infancy, we are already collaborating with a small company in Silicon Valley to develop manufacturing methods in conjunction with the research at Sandia. This will ensure that our technology will be compatible with mass production processes.



About the author

Karen Waldrip (knwaldr@sandia.gov) is a research scientist at the Advanced Power Sources Technology R&D department at Sandia National Laboratories (SNL), Albuquerque, NM. She performed her doctoral research on MOCVD of AlGaN/GaN for ultraviolet VCSELs and her postdoctoral work on bulk GaN synthesis in the Semiconductor Device Sciences department at SNL. She thanks the Department of Energy's (Energy Efficiency and Renewable Energy) National Energy Technology Laboratory solid-state lighting program for funding.

Further reading

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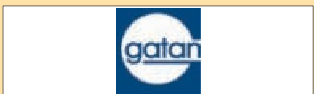

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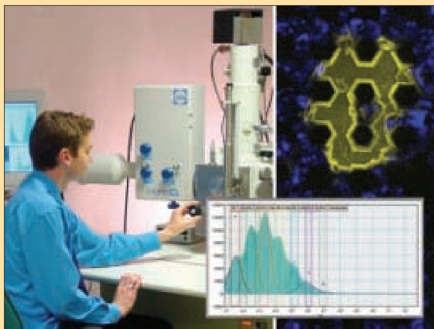

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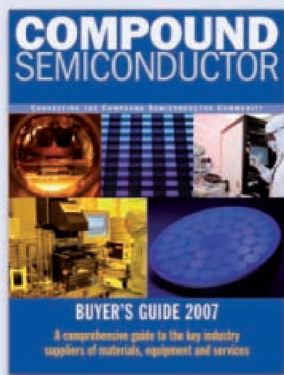

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UV EMITTERS

AlN mask simplifies laser fabrication

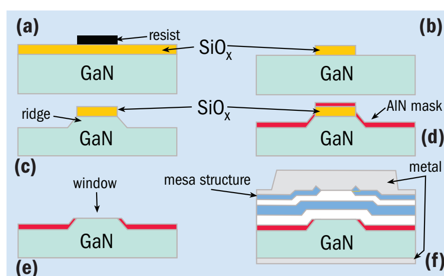
It is possible to simplify GaN laser production by employing a substrate with a partially relaxed AlN mask and stripe-shaped windows, claim a team of researchers from Warsaw, Poland.

"Our technique is much simpler than epitaxial layer overgrowth (ELO) and it gives device designers new possibilities in the field of UV lasers," said Martin Sarzyński from the Institute of High Pressure Physics.

Although ELO is a very common technique for laser diode fabrication, it is complicated and requires several processing steps.

The new approach also addresses cracking in the AlGaN layers, which can hinder conventional laser diode performance.

"When a certain thickness – termed the critical thickness – of the AlGaN cladding is exceeded, the layer cracks," explained Sarzyński. But by switching to the team's process (see figure for details), it is possible to increase the critical thickness of this AlGaN layer if it has a fixed composition, or boost the aluminum content. Both of these changes are beneficial, as they lead to improved optical confinement in the device.



Patterned substrates with 7 µm wide SiO_2 stripes are formed by photolithography and wet-etching **(a, b)**. Reactive ion etching creates 0.5 µm high ridges **(c)** coated with 30 nm of AlN and a 10 nm AlGaN cap **(d)**. The remaining SiO_2 is removed by wet-etching **(e)** before a laser structure is added **(f)**.

MOCVD was used to make laser structures on the processed substrates. These designs contained AlGaN in the lower cladding, electron blocking layer and upper cladding.

These devices featured a 7 µm wide laser stripe and a 500 µm cavity, and contained AlGaN layers with an aluminum content of 8, 13 and 16%, and a total thickness of 1, 1 and 0.9 µm, respectively.

All of the 408 nm emitters had a slope efficiency of 0.44 W/A. Increasing the aluminum content reduced the threshold current from more than 10 to 6.5 kA/cm^2.

Journal reference
M Sarzyński *et al.* 2007 *Appl. Phys. Lett.* **91** 221103.

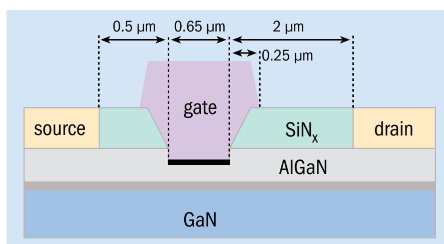
GaN HEMTs

Slanted gate boosts output power density

Researchers from the University of California, Santa Barbara (UCSB), have built a so-called "recessed slant gate" GaN HEMT that raises the power density record for 10 GHz transistors to 20.9 W/mm.

The device – which could potentially serve in advanced radar systems for military applications – employs the novel slant gate geometry to reduce the peak electric field, minimize dispersion and increase breakdown voltage. A fluorine and chlorine plasma treatment also cuts gate leakage.

"With this technology only a brief fluorine treatment is needed to reduce the gate leakage current by 1–2 orders of magnitude, while damage to the 2DEG underneath is avoided," explained team member Yi Pei.



Just one photolithographic step is required to build UCSB's high-power recessed slant gate HEMTs.

According to Pei, conventional GaN HEMTs also tend to receive an unintentional fluorine treatment thanks to "over-etching" of the SiN film in the gate region. However, the lower leakage currents that result are lost during a subsequent recess etch.

UCSB used MOCVD growth on SiC to produce the devices (see figure for details). Source and drain contacts were made from Ti/Al/Ni/Au, before a SiN layer was added for passivation. The shape for the bottom of the gate was formed by photolithography and etching.

The evaporation of Ni/Au into this void completes the fabrication of the gate, which has a 55° slant wall that acts as a field plate and reduces the maximum electric field strength without increasing parasitic capacitance. Just 10 nm of AlGaN is left below the gate. This moves the peak electric field away from the SiN/AlGaN interface and into the AlGaN layer, which has a higher breakdown field.

Employing this design feature enabled the HEMT to deliver 20.9 W/mm at a drain bias of 83 V, a power-added efficiency of 40% and a linear gain of 12 dB.

The team is now applying its slant gate technology to millimeter-wave devices.

Journal reference
Y Pei *et al.* 2007 *Jap. J. Appl. Phys.* **46** L1087.

EPITAXY

Silicon-on-insulator platform brightens LEDs

Brighter GaN-on-silicon LEDs can be produced by switching to a silicon-on-insulator (SOI) platform, according to researchers from Singapore and Germany.

The team from the Institute of Materials Research and Engineering in Singapore and the Otto-von-Guericke University of Magdeburg, Germany, says that the increased output results from a reduction of light absorption in the silicon substrate. The Si/SiO_2 layers beneath the buffer are claimed to act as a backside reflector for improved light extraction.

This new design should also simplify the removal of GaN devices from the substrate via sacrificial etching and make it easier to site LEDs on good thermally and electrically conductive materials, such as copper.

Comparative studies of GaN-on-silicon and GaN-on-SOI LEDs were carried out by growing 2.7 µm thick buffer layers and conventional LED structures on both types of platform. The electroluminescence spectrum of the SOI device had several strong interference peaks due to multiple internal reflections and its emission was substantially brighter than its silicon-based equivalent.

Journal reference
S Tripathy *et al.* 2007 *Appl. Phys. Lett.* **91** 231109.

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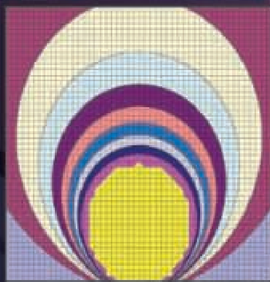

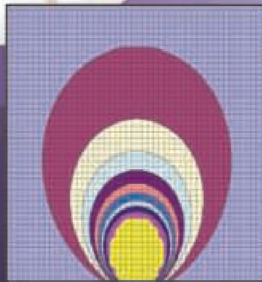

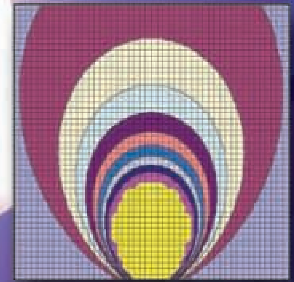

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