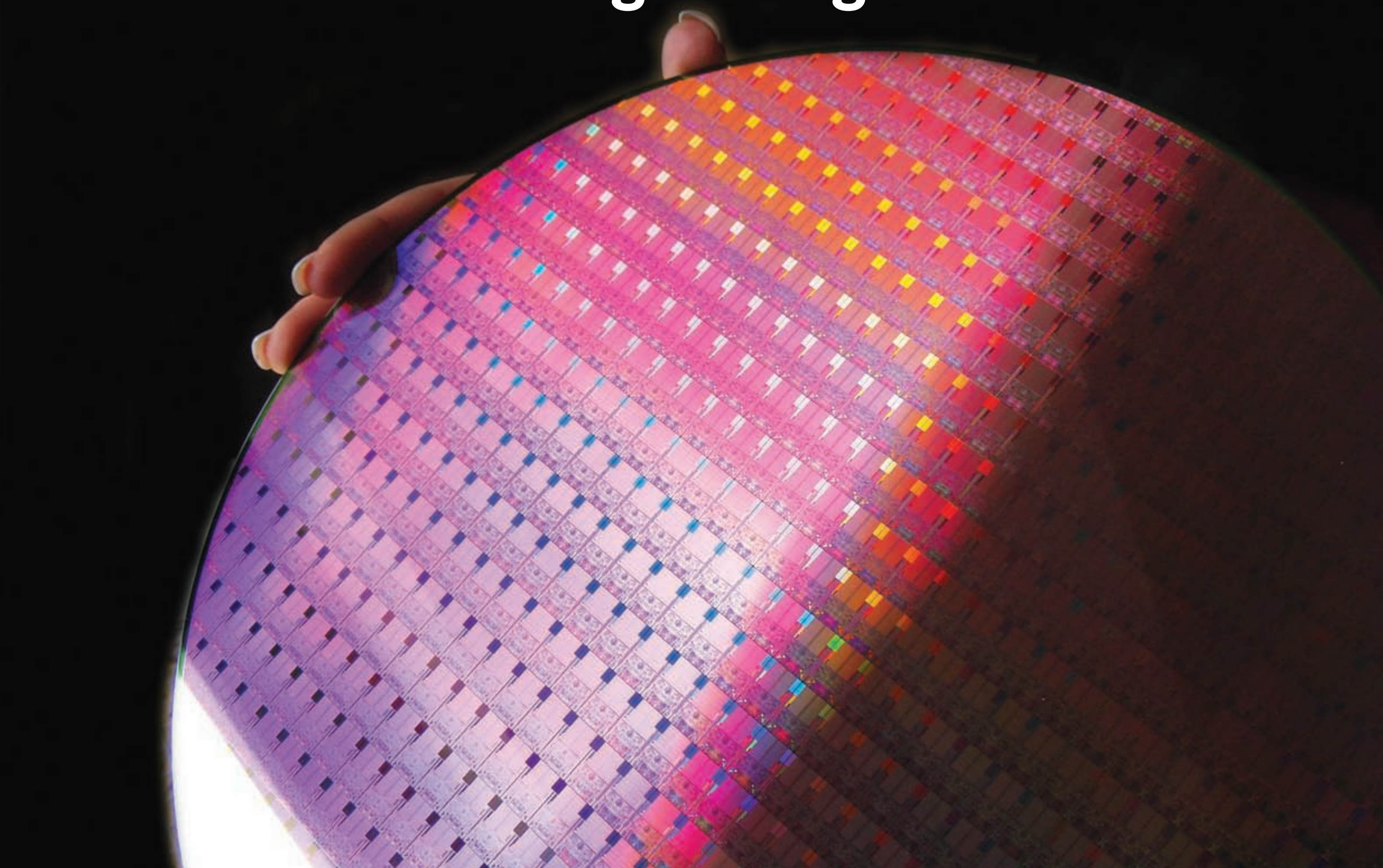
COMPOUND SEMICONDUCTOR

April 2008 Volume 14 Number 3

CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY

CMOS CONVERGENCE

Can III-Vs and silicon get it together?



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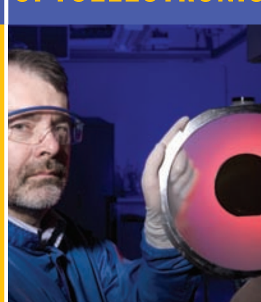

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Main cover image: *Intel's 12 inch "Penryn" wafers represent the latest CMOS technology. The same company is at the forefront of efforts to integrate III-V materials in the future. See p25. Credit: Intel.*

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EDITORIAL

Believe (some of) the hype

Here's a statistic I bet you've heard recently. It goes along the lines of "the energy from sunlight that reaches the Earth each hour is enough to meet our power demands for an entire year." In short, that fiery orb is a huge and almost entirely untapped resource. The trouble is that capturing, storing and distributing the electricity generated by photovoltaics is both technologically challenging and economically unconvincing.

Here's the problem. The real cost of solar energy, depending on whose analysis you look at, is currently anywhere between $0.18 and $0.28 per kilowatt-hour. To be truly competitive that figure needs to be between $0.05 and $0.10. In fact, the only reason that a market for solar energy even exists is because of generous subsidies. And, while helpful in the short term, these cannot last forever.

But photovoltaics is already big business and now, it seems, everybody wants a piece of the action. Venture capitalists in North America invested some $400 million in solar energy companies in the third quarter of 2007. And, First Solar – whose modules are based on the compound CdTe – is, astonishingly, now a firm with a higher market valuation than the Ford Motor Company.

> "Photovoltaics is big business and everybody wants a piece of the action."

Which begs the question: how much of this solar phenomenon is based on real business opportunity and how much is simply hype? It's certainly something that has vexed Dave Holland, the managing director of Australian solar firm Solar Systems. As we report on p5 of this issue, Holland cares less about the PR puff and more about building power stations that are capable of delivering a reliable electricity supply.

Nobody could doubt that creating an economically competitive solar industry would be a fantastic achievement, and one capable of making a huge contribution toward meeting increasing global energy demand. But achieving this goal will not be helped by over-exaggerated claims and unrealistic investors. The last thing we need is another "bubble".

Michael Hatcher *Editor*

Advertisers' Index

SOLAR POWER

Photovoltaics firms told to 'grow up'

By Andy Extance

Australian concentrating photovoltaics (CPV) company Solar Systems has issued a caution to fellow companies in the industry: stop getting carried away with supply deals and focus on the key challenge of electricity generation.

"What we're all trying to produce is units of electricity in large scale, and the market needs to grow up and realize that," said Dave Holland, managing director at the system maker.

He believes that he's well positioned to say this because, other than US-based Amonix, Solar Systems is the only CPV company whose products are already generating electricity commercially. He's willing to welcome other players into the sector, but says that they must be realistic about the potential of their technology.

"The thing we, and the whole solar industry, have to be careful about is being perhaps a bit more conservative in our claims," Holland said. He is concerned that deals between other companies in the industry will not be as lucrative as they believe. He suggests that those companies would be better served following Solar Systems' more conservative example, rather than talking about the size of their supply deals.

"I took over the running of the business in 2001, and I said: 'No more talking to the press'," Holland explained. "I said, 'We're going to sit down, shut up and build a power station. Until we've got one running it's still imaginary. Are we going to spend money on PR campaigns, or are we going to spend it building power stations?' "

He added: "It's not as easy as it looks in any way – there's a huge difference between a prototype and a real system."

Holland's comments came on the back of a AUS$40 million ($37.6 million) investment in Solar Systems from Australian power firm TRUenergy – funding that could grow to more than AUS$290 million long-term.

The deal revolves around a 154 MW plant that Solar Systems is intending to build in Australia's Victoria state, which TRUenergy's parent, China Light and Power, will ultimately take ownership of. These two companies bring energy industry expertise to the relationship, allowing Solar Systems to focus more on developing its technology.

Solar Systems has a long history in CPV, working in the field since 1991 and starting with silicon cell technology before switching to Spectrolab's GaAs-based cells.

The high cost of III-V cells means that to produce power economically, CPV must operate on a very large scale. Solar Systems believes that it now knows how to operate at such a scale, with Holland stressing that even the figures of merit used to describe the technology must move away from the conventional solar industry terminology.

"The dollar-per-watt metric comes out of an industry that's aimed at the roofs of houses," the managing director said. "In the power market, the real measure is dollar-per-megawatt hour. We expect, if all goes well, to be in the market near to $100/MWh in a few years – and that's providing a commercial return to the power station owners."

EQUIPMENT

Wary Aixtron expects another bumper year

PHILIPS

Continued strong demand for high-brightness LEDs drove a 25% increase in Aixtron sales during 2007.

Driven largely by a rapid increase in demand for MOCVD equipment used to manufacture high-brightness LEDs, total sales at equipment vendor Aixtron could hit €300 million ($467 million) in 2008.

Orders placed with the Aachen, Germany, company reached another high in the final quarter of 2007, totaling €89.4 million. But CEO Paul Hyland warned that this could represent the peak of the current cycle, with a slight slow-down in quotation enquiries emerging in recent weeks.

Whether that results in a genuine slowdown in orders will not be known for some time, but what does look certain is that Aixtron will record another large increase in total revenue during 2008, on top of an excellent 2007. Last year, the firm posted total revenue of €214.8 million, of which €146 million resulted from sales of compound semiconductor manufacturing tools. Aixtron, which also sells advanced silicon deposition tools, said that total 2008 sales should fall in the €270–300 million range.

SUBSTRATES

LED boom pushes substrates past $1 bn

Compound semiconductor substrates will expand the niche that they occupy in the wider electronics industry as their overall market grows to $1 billion by 2010.

LED demand will combine with a strong RF electronics sector to drive sales up from $822 million in 2007, according to French market analysts Yole Développement.

Yole says that the proportion of compound substrates within the total semiconductor business increased from 0.53% in 2005 to 0.64% in 2007 – as measured by wafer area. The analyst company points out that lower cost and wider-diameter substrates will help expand this proportion further, to reach 0.84% by 2012.

Sales of sapphire substrates will increase by 20% year-on-year, through to 2012. "Sapphire substrates for GaN LEDs will grow their total share of the compound semiconductor [substrate] market from 27% in 2005 to 32%," said Yole's Philippe Roussel.

MANUFACTURING

RFMD halts diggers on expansion

RF Micro Devices (RFMD) has changed its manufacturing expansion strategy. The GaAs chip maker says that its $25 million acquisition of Filtronic Compound Semiconductors, completed in early March, will delay the need for a $200 million capital investment in North Carolina.

"Filtronic gives us instant capacity, rather than waiting until we get the factory built and people trained in Greensboro," said Jerry Neal, RFMD's executive vice-president of marketing and strategic development.

Neal told *Compound Semiconductor* that after the March 3 completion of the deal, development of the previously announced $103 million US processing fab is now postponed until an unspecified date.

"We have a huge amount of additional unused space at Filtronic so we have the option of expanding there before we would start back at the Greensboro facility," he said. The experience that the 300 new Filtronic employees acquired by RFMD have gained in point-to-point and military communications will also help bring forward the company's technology agenda.

"The advanced processes that we're talking about are not going to be delayed or stopped, they're going to be accelerated," Neal said. "The process development group there will be working very closely with our group in Greensboro."

RFMD

RFMD co-founder Jerry Neal wants to utilize the huge unused space in Filtronic's UK GaAs fab.

"This development group will complement what we bought at Sirenza and we think that's going to help us further diversify the company into high-performance GaAs applications."

Construction in Greensboro will now either continue very slowly or stop altogether and hence RFMD's current equipment needs will also drop considerably, until building is restarted in earnest.

Neal says that the $25 million Filtronic deal has immediately cut the cost of the PHEMT switches used by RFMD.

SUBSTRATES

AXT invests in 6 inch GaAs capacity again

A growing share of the GaAs market and qualification of germanium substrates by more LED and III-V solar customers suggest that 2008 will be a good year for AXT.

The Fremont, CA, materials and substrate vendor has grown its market share in semi-insulating GaAs substrates and will expand its 6 inch crystal growth capacity by a quarter to accommodate further expected share gains. The expansion will be the main focus of AXT's $6 million anticipated capital expenditure for 2008, and is due to be completed sometime in the third quarter.

"We are making tremendous progress in market share gains," said Phil Yin, the CEO of the company. "In 2007 alone we added 10 new semi-insulating customers." This momentum helped AXT to a profit of $5.3 million, up from $0.86 million in 2006, although this figure included $3.3 million gained by trading in Finisar shares.

The final quarter of 2007 brought the substrate maker $17.6 million in revenues, which it expects to repeat or slightly exceed in the first quarter of 2008.

AXT's sales of semiconducting GaAs for use in LED manufacture increased by 37% in 2007, as the company closed in on regaining a major North American solid-state lighting customer that it has not done business with for years.

Yin said: "With additional testing of our material we expect to obtain official vendor approval and expect production release in late Q2 or early Q3."

The firm is also expecting newly developed liquid-encapsulated Czochralski GaAs growth facilities to be online late in 2008 or early in 2009. This will enable the company to grow substrates for the LED market more profitably and rapidly than with its existing vertical gradient freeze method.

AXT is also in qualification with four European photovoltaics companies and has three cell manufacturing customers demanding germanium substrates for volume production.

FINANCIAL RESULTS

TriQuint closes gap on rivals. . .

A strong fourth quarter in 2007 saw TriQuint post revenues of $128.5 million, up more than 12% from the same quarter in the previous year and indicating market share gains from its competitors.

"If you look at our two major competitors, we just did much better," said Ralph Quinsey, TriQuint's CEO. "We did okay in [market] share in 2007 and the fourth quarter was our strongest quarter of the year."

Overall for 2007, TriQuint made $23.4 million in profit, compared with $21.4 million for 2006. The company's annual sales grew 18% to hit $475.8 million.

Of the two companies that record greater sales than TriQuint, RF Micro Devices' most recent quarter saw revenues drop below the same period in the previous year. Skyworks Solutions' fiscal 2007 saw lower total sales than 2006, although this was partly related to its exit from the baseband product area.

According to data from Strategy Analytics, TriQuint's share of the $3 billion 2006 GaAs market was 10% – lagging behind RFMD on 24% and Skyworks on 21%.

TriQuint expects to see a similar rate of growth in 2008, which would lift sales above $540 million and further close the gap on its two main rivals. "Revenue will be driven by strong wireless LAN opportunities in our network business and share growth in our handset business," explained Steve Buhaly, TriQuint's chief financial officer.

In the most recent quarter, the company's sales from wireless LAN revenue were up 143% over the same period in 2006. TriQuint has just begun shipping high-value Wi-Fi front-end modules to a major chip manufacturer, in a deal that will continue to ramp-up throughout 2008.

For the first quarter of 2008, the company expects its sales to drop back to less than $115 million. This is in part due to seasonal variations, however, and Quinsey conceded that TriQuint could temporarily relinquish some market share over this period.

This will see levels of utilization at the company's high-volume Hillsboro, OR, fab drop back from the 85% level that it struck at the end of 2007 towards 70%.

However, to reach the overall sales target for 2008, TriQuint will have to increase revenues by 10–15% for each quarter of the coming year. In light of these ambitious plans, the firm says that it could economically expand capacity in Oregon by 20% if needed, while it also has spare capacity at its lower-volume fab in Richardson, TX.

MERGERS AND ACQUISITIONS

...and snaps up WJ design talent

TriQuint Semiconductor is to acquire fabless RFIC design company WJ Communications in a deal valued at approximately $72 million. The acquisition will primarily boost TriQuint's presence in the wireless infrastructure market, where WJ's chips and multichip modules (MCMs) are used in base-station amplifiers.

WJ has also managed to penetrate the Chinese base-station market, which uses the local 3G protocol called time division synchronous code division multiple access (TD-SCDMA). In January of this year, WJ announced that it had received an initial production order worth $0.5 million for its InGaP HBT-based MCMs, to be used in TD-SCDMA applications.

CEO Ralph Quinsey believes that although WJ is a much smaller enterprise than TriQuint, the combination will prove highly complementary. "In summary, one plus one makes more than two in this case," Quinsey said. "We're delighted to have a Silicon Valley design center."

Based in the heart of Silicon Valley, WJ – formerly known as Watkins-Johnson – closed its GaAs fabrication facility a year ago in a move designed to cut costs. Prior to that, it had been working closely with the high-end pure-play GaAs foundry Global Communication Semiconductors (GCS), which is based further south in Torrance.

And although TriQuint will have the option of switching wafer manufacturing for WJ out of the GCS foundry and into one of its own GaAs fabs, Quinsey says that the amount of disruption that this would involve did not justify making the transfer.

Welcoming WJ's pool of RF design talent to the TriQuint fold, the CEO remarked on the wider difficulty of hiring top designers, saying: "We couldn't hire RF designers fast enough. [And] finding high-performance solutions is all about talent."

In its most recent quarter, WJ posted a loss of $0.8 million on sales of $10.6 million.

SOLID-STATE LIGHTING

LED research gets $28 m funding boost

In February the US Department of Energy funded a further 13 core research and product development projects in its fourth round of awards focused on solid-state lighting (SSL) technology.

The total value of the new projects was $27.9 million, although a substantial portion of that total will be provided as a cost-share by the contributing companies involved.

Selected as part of the National Energy Technology Laboratory's goal to develop SSL for general illumination by the year 2025, the awards include five projects focused on core LED technologies – of which three directly involve compound semiconductor research.

They include a collaboration between Philips Lumileds and Crystal IS to develop AlN substrates that are suitable for blue-LED fabrication. The goal of this project is to produce GaN-ready material with a defect density of less than $10^5 cm^{-2}$ for high-quality LED fabrication.

Other basic technology projects with funding involve Luminus Devices and Georgia's Institute of Technology, who will work together to gain a better understanding of the impact that strain, defects, polarization effects and Stokes loss have on the internal quantum efficiency of LEDs.

Meanwhile, researchers at Lehigh University will tackle one of the enduring problems in LED technology – that of fabricating high-efficiency green emitters. The team at Lehigh will work on improving green LEDs by growing what they describe as "staggered" InGaN quantum-wells.

In a separate funding stream, Sandia's National Laboratory will also focus on the green gap. It is set to develop a novel analytical platform called deep-level optical spectroscopy – an approach that should be capable of interrogating deep levels throughout the InGaN bandgap.

Under the more commercial focus of six projects selected for product development awards, Cree has won backing to develop a high-efficiency, low-cost white-LED component that is capable of replacing conventional lights.

One of Cree's rivals, Philips Lumileds, has also won funding for product development and is slated to deliver prototype warm-white LEDs with a luminous efficacy of 135 lm/W and a color rendering index that is higher than 90.

General Electric's Lumination subsidiary and Osram's Sylvania Development will also be working on SSL luminaire development with new funds.

Following in his father's footsteps, Rensselaer Polytechnic Institute graduate student Martin Schubert has won a $30,000 prize for developing the first LED polarization method that avoids the use of conventional polarizers. This research, performed in conjunction with Samsung and his father Fred's world-leading group, could one day find commercial deployment in LCD displays, which operate by transmitting polarized light. "Polarized light can be obtained by combining conventional LEDs with polarizers, but this drastically reduces the total light output," Schubert said.

CHIPS

Seoul touts ultra-bright white LED package

A four-chip white-LED package from Seoul Semiconductor is claimed to produce a maximum luminous flux of 900 lm – more than a 60 W incandescent lamp.

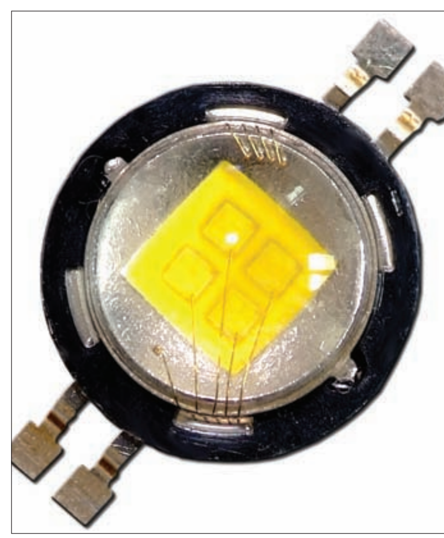
The Korean company, which has just moved the products into volume production, says that with a luminous efficacy of 90 lm/W, the Z-Power P7 "can replace a conventional bulb". Seoul is hoping to see the 10 W-rated emitters applied in high-end flashlights and streetlamps, as well as in residential lighting.

Electro-optic characteristics of the new product include a forward voltage of 3.6 V and a forward current of 2.8 A, with each individual LED chip driven at 700 mA.

Although the maximum luminous flux is 900 lm, the more typical value is significantly lower, at 700 lm. Further details show the P7 to be cool-white in nature, with a correlated color temperature of 6300 K and a color rendering index of 70.

In comparison, Philips Lumileds' Luxeon Rebel range includes a cool-white (6500 K) emitter with a typical luminous flux of 180 lm at 700 mA. Four of these chips could theoretically deliver a flux of 720 lm.

Seoul also claims to have some further performance improvements in its locker. Hyuk Won Kwon from the company said:



SEOUL SEMICONDUCTOR

With a maximum luminous flux of 900 lm, Seoul's latest four-chip LED is comparable in brightness to a 60 W incandescent bulb – although the cool-white light that it produces is different to that of the conventional source, which produces a warm glow.

"We will develop new ultra-high-power products emitting more than 1000 lm during the third quarter of this year."

● General illumination was one of the fastest-growing applications of the LED industry in 2007, according to recent analysis by Strategies Unlimited. Overall the industry registered market growth of nearly 10% over 2006 to reach $4.6 billion, the fastest rate of growth seen for four years.

SILICON CARBIDE

Substrate firm strives to expand SiC material

The SiC world has gained an additional player. Called SiC Systems, the US firm says that it will crash onto the substrate market with its 6 inch 3C-SiC wafers later this year.

Incorporated in July 2007, SiC Systems says that it has already developed an economical crystal growth process thanks to a small business grant.

The prototype process now in place at the company's Golden, CO, fab gives it a big advantage, according to the company's third founder and CEO, Ken Whelan.

"The two popular methods for growth of SiC crystal today have issues with keeping level heat across the diameter of the substrate, which makes their ability to do larger diameters highly suspect," Whelan explained. "Our process solves that. We have better control over all of the parameters that go into improving the quality of SiC growth than any of our competitors."

Whelan also says that part of the intention in producing 6 inch 3C-SiC is to provide a low-cost alternative to sapphire substrates for the LED market.

SAPPHIRE SUBSTRATES

Rubicon fully booked for the rest of 2008

Despite having only just started production at its second sapphire substrate manufacturing facility, Rubicon Technology is already very near to completely filling its order books for 2008.

"Our 2008 backlog is up to $45 million," said Rubicon's CEO Raja Parvez at the company's first investor call since its IPO in November. "Based on our projected production ramp for 2008 we are very close to being sold out for the year."

Over the past three months – prior to the opening of the new Bensenville, IL, factory – the company had been capacity-constrained. Nevertheless, it still managed to boost revenues by moving to larger-diameter 3 and 4 inch wafers for LED manufacture and 6 inch wafers for RF applications.

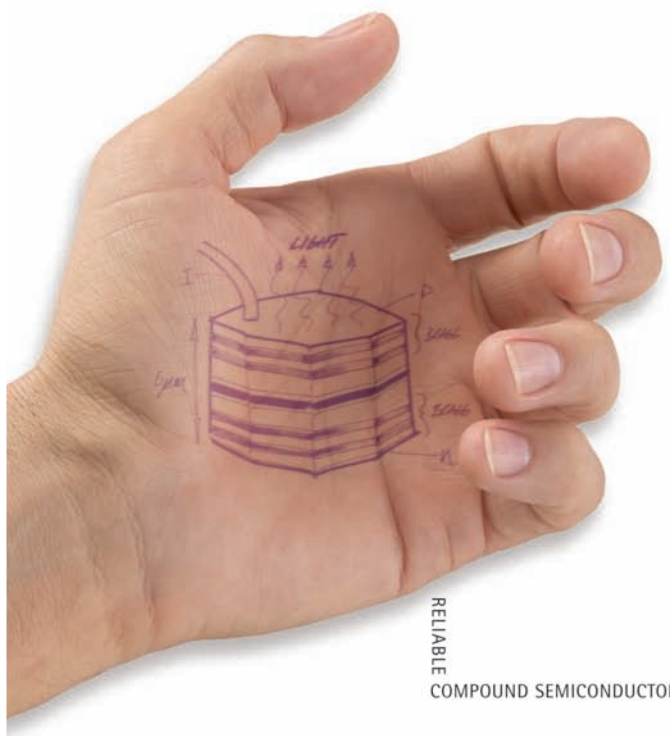
Although the company increased its annual sales by 64% to record a total of $34.1 million for 2007, it expects the figure to exceed $46 million this year. For the whole of 2008, it estimates an overall profit of more than $10 million.

The eye-catching figures were released at the end of Rubicon's first quarter after listing on the Nasdaq exchange, which ended in a $16.5 million loss – largely due to charges arising from its flotation.

In the last three months, 70% of Rubicon's $9.5 million revenues came from substrate purchases made by LED companies. 20% came from sales of sapphire substrates to producers of silicon-on-sapphire RF electronics companies.

Five of the company's LED-making customers are buying 3 or 4 inch diameter substrates and Parvez believes that the trend to larger wafers will continue. He says that several other LED manufacturers are considering making a similar migration soon.

On the RF side, where Rubicon is a key supplier to silicon-on-sapphire specialist Peregrine Semiconductor, 8 inch substrates are set to go into production this year. Qualification should follow in 2009.



PHOTONIC INTEGRATED CIRCUITS

Infinera touts 'Kish's law' for optical ICs

The term "Kish's law" could one day be lauded much like Gordon Moore's seminal vision of silicon semiconductor development, following the introduction of a photonics roadmap by California's Infinera.

The company, which manufactures InP-based photonic integrated circuits (PICs) that condense huge amounts of optical functionality onto a single semiconductor chip, launched the roadmap to coincide with the recent Optical Fiber Communication (OFC) conference held in San Diego.

Fred Kish, the firm's vice-president of PIC development and manufacturing, and formerly an innovative force in high-brightness LED research at Hewlett-Packard, is the key architect of the roadmap.

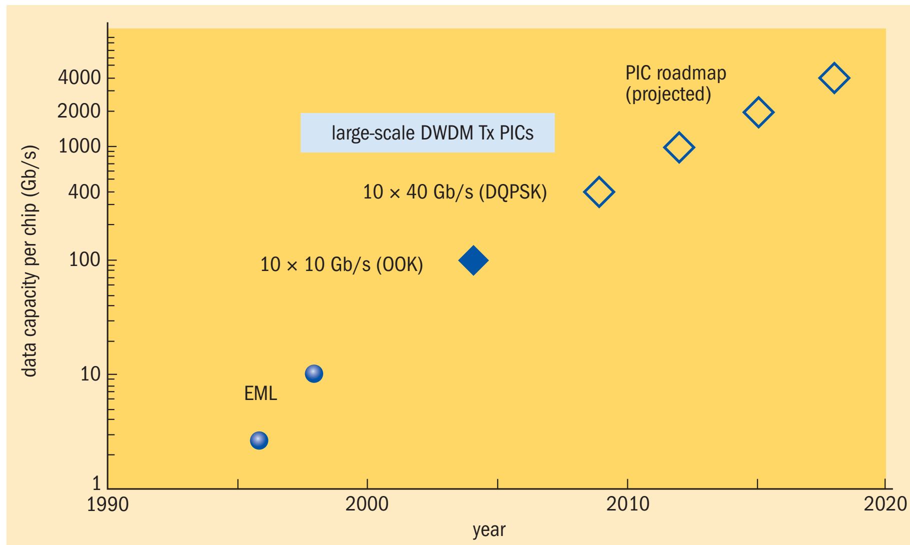
Imitating the International Technology Roadmap for Semiconductors (ITRS), Kish's vision anticipates that the capacity of PIC chips will double every three years for the next decade. The firm's current PIC, introduced in 2004, offers 10 wavelength channels, each operating at 10 Gb/s to give an overall capacity of 100 Gb/s. The next step is 400 Gb/s, a capacity that Infinera demonstrated (in a 10 × 40 Gb/s channel form) at this year's OFC, and which it plans to launch commercially in 2009.

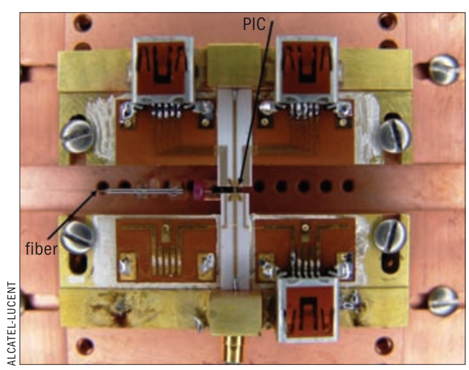
Unlike the ITRS, the photonics roadmap is not a document ground out of extensive collaboration between myriad chip makers, materials suppliers and equipment vendors. Rather, it is unique to Infinera, which appears to be positioning itself as the Intel of the photonics world and aiming to commercialize PICs with a capacity of 1 Tb/s in 2012 and 4 Tb/s per chip in 2018.

According to vice-president of technical marketing Serge Melle, it is not so much the overall data rate that matters, but the density of components on each chip – conceptually similar to the way that semiconductor makers have squeezed more transistors onto silicon chips via scaling with lithography.

However, the much greater complexity of photonic components compared with silicon transistors means that the company's 400 Gb/s chip is slightly larger than the current generation.

Getting from 10 to 40 Gb/s channels has been a challenge, Melle says. The jump in speed demands the use of differential quadrature phase-shift keying to handle the faster modulation frequency. This would usually be done with a number of discrete optical components, but in a PIC this isn't an option.





On the map: (top) Infinera is aiming to increase the data capacity of PICs to 4 Tb/s by 2018. The next scheduled step on the roadmap is a 400 Gb/s chip currently in development and scheduled for commercial release next year. It isn't just Infinera working on InP-based PICs. Researchers at Alcatel-Lucent's Bell Laboratories believe that they will be able to greatly reduce the size of high-speed photonic components. Chris Doerr and colleagues integrated a delay interferometer with two pairs of high-speed photodetectors in this design (left). The PIC is at the center of the photograph and is a similar size to the optical fiber adjacent to it.

"40G requires things like splitters, receivers and so on," said Melle. "The component count is huge."

Kish and his team have consolidated all of the required optical functions on the same PIC, with all of the necessary active components like lasers, photodetectors and arrays of Mach-Zehnder modulators.

What's new in the 40 Gb/s channels is that semiconductor optical amplifiers (SOAs) now feature inside the PIC. And, because they operate over a much wider wavelength span than conventional erbium-doped amplifiers, these devices could provide the key to future increases in chip capacity.

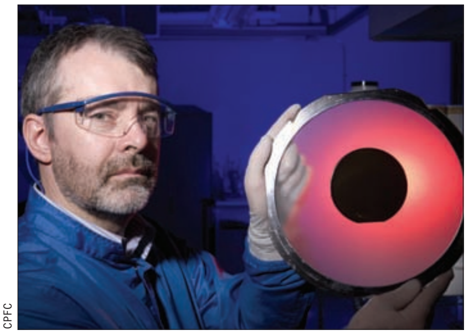
Erbium-doped fiber amplifiers only operate in the 1530–1560 nm wavelength range. In contrast, says Melle, the SOAs can operate at any wavelength across the fiber window of 1240–1650 nm. Using the entire fiber window rather than a small portion of it might allow for further multiplexing, with lots more wavelengths available to carry data down optical cables.

Although the roadmap is currently Infinera-specific, Melle believes that it may stimulate the photonics industry towards greater collaboration, in much the same way as the silicon industry has progressed. "The roadmap is not about hero experiments, it is about commercial products," he said.

At its InP fabrication facility in California, Infinera has witnessed a huge increase in "good PIC" output, thanks partly to increased demand, but also to a massive improvement in die yield. "We have improved defect densities and therefore have much better [fab] utilization," Melle explained. He estimated that the company has increased PIC output by a factor of 50 since it began manufacturing the components back in 2004, and attributed the improvement to Infinera's extensive use of statistical process control to monitor its fab operation.

FOUNDRY SERVICES

Photonics foundry gets funding


CPFC

The III-V foundry operation at Canada's Photonics Fabrication Center is establishing new lithography processes and a second shift to meet demand.

The Canadian Photonics Fabrication Center (CPFC) has gained a C$22.3 million ($22 million) governmental funding boost, rewarding it for helping Canada's photonics industry bounce back from the telecoms crash.

"CPFC has been a success really beyond the dreams of most people four or five years ago when it was first started," said Brian Ventrudo, the foundry's business development officer. "We see this as a vote of confidence for what we've done for the industry and the business model that we have."

Awarded at the end of January, the new money will be predominantly spent on "leading edge" stepper and electron-beam lithography systems, and establishing a second shift at the foundry. The increased output targets reflect the high level of interest in CPFC's services, built around demand for InP and GaAs fabrication from the strong photonics community in Ottawa.

Further to this traditional expertise, CPFC has experienced an increasing demand for its services to manufacture devices for solid-state lighting and photovoltaics. The foundry is also considering proposals to move away from its core photonics expertise and begin work making GaN devices for high-power switching applications.

The funding emphasizes CPFC's role as the fulcrum that allows Ottawa to operate as the dedicated Canadian photonics cluster. In the past year, this cluster has thrown up photovoltaic firm Cyrium and optical networking business BTI Photonic Systems, each propelled by multimillion-dollar venture backing.

According to Ventrudo, venture capitalists are particularly keen on the kind of business models that CPFC enables its customers to use. "We have a lot of VCs coming through here to look at the fab and they just love this model, because their companies will just pay for what they need," he said.

FIBER-OPTIC COMPONENTS

Tunable laser competition hots up

A raft of tunable lasers released at the 2008 Optical Fiber Communication (OFC) conference in February will create excessive competition in this niche market, and may even stunt its growth.

That's according to Daryl Inniss, market analyst for communications components at Ovum RHK. The future growth rate for tunable lasers will now only match the overall component industry, despite their currently lucrative position, he says.

Sales of tunable lasers will grow at 11% through 2012. But Inniss says that there is evidence that the high prices of tunables are in decline. "When Bookham introduced its tunable lasers, the prices started to fall," he said. "Just one new entrant had a significant impact." At OFC, held in San Diego, Bookham, Eudyna, Pirelli, Luna and NeoPhotonics all announced tunable lasers.

Inniss sees the market for these components expanding from $85 million in 2006, to $154 million in 2012. But if tunable lasers are successfully integrated into the XFP form factor, as JDSU and others are striving to do, the market could grow more quickly.

The analyst felt that this was one contributor to a mixed outlook on the business landscape at OFC. Overall, the trading outlook is good, he says. However, companies are concerned about a poor stock market reaction to their efforts and the possibility of a recession in North America.

On the optimistic side, Inniss applauded the inaugural demonstrations of 100 Gb/s technologies at OFC and explained how they could provide a new opportunity for chip makers. "The same tunable lasers could go into 100 Gb/s products, but on the shorter reach, say 40 km or less, there is substantial development needed for transmitters," he said. "What suppliers are going to have to do is integrate four lasers onto one InP chip."

RESEARCH

Record cell sets IMEC's III-V solar agenda

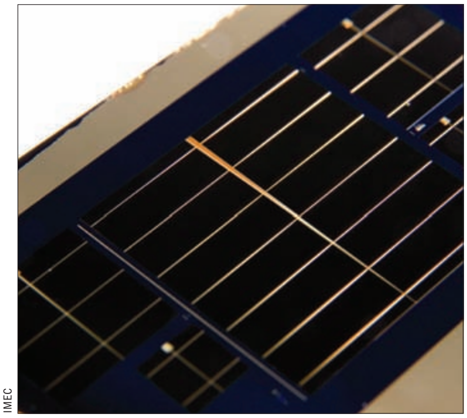
Belgian researchers have produced a record-breaking single-junction GaAs solar cell, thanks to high-quality germanium substrates, which they aim to fully exploit in future triple-junction design.

Made at the Interuniversity Microelectronics Center (IMEC) in Leuven, using a high-quality germanium substrate, the cell achieved 24.7% conversion efficiency under one-sun concentration of the standard terrestrial spectrum.

IMEC's compatriot Umicore had developed the high-performance substrates under a research project with the European Space Agency, called ESA-IMAGER.

"They asked us to make standard single-junction cells on those substrates to check the quality, which turned out to be very good," said Giovanni Flamand, leader of the IMEC III-V solar team.

Having confirmed the improved performance of the standard cells with lower defect levels at the US National Renewable Energy Laboratory in November 2007, Flamand now hopes to translate this to non-standard triple-junction cells for use in highly concentrating photovoltaic systems.



IMEC

A high-performance germanium substrate developed by materials giant Umicore provided the basis for IMEC's record-breaking single-junction cell.

The IMEC team intends to grow InGaP and GaAs subcells monolithically on one germanium substrate, which would be removed prior to mechanical bonding with a high-efficiency germanium subcell. This allows the bonded germanium layer to be connected in parallel rather than series with the other subcells, in an assembly the same thickness as existing triple-junction cells.

"We can, in that construction, make full use of the current generated by the germanium bottom cell. This is not fully used in a monolithic stack, as it is limited to the lowest current generated by one of the top cells that are connected in series," Flamand said.

"By stacking them mechanically on top of each other we can win another 1.5–2% in overall efficiency and thereby attain a higher efficiency than can be reached with present state-of-the-art."

Flamand concedes that achieving this will take some time, but he still hopes to produce competitive III-V solar cells that IMEC could license out for commercial sale.

"The 24.7% cell that we have now, it's a nice result, but it's not something we can commercialize," he said. "It's just an intermediate step in the further development of our multijunction approach."

FUNDING

McMaster plan aims for a solar breakthrough

Materials scientists in Canada are to receive $4.1 million to develop a novel solar cell that combines silicon with a secret compound semiconductor to double the efficiency of conventional cells.

Solar Energy firm ARISE Technologies and the Ontario Centres of Excellence are funding the work of John Preston and Rafael Kleiman, who head up the McMaster University team.

They are aiming to combine the ubiquity and low cost of silicon-based solar cells with the high efficiencies that are associated with more expensive compound semiconductor technologies.

"We are aiming to develop cells suited for one-sun applications – to create what appear to be regular silicon panels, but which have a much higher efficiency because of the novel materials approach taken," Kleiman told *Compound Semiconductor*.

The exact nature of that materials system is being kept a closely guarded secret, although it is expected to double the efficiency of typical silicon cells. However, Kleiman did reveal that the team would be making use of McMaster's in-house MBE facility to deposit single-crystal layers of a compound semiconductor on top of the silicon host.

The professor added that GaAs will not be the material used because, at 1.45 eV, its bandgap is not wide enough to provide the best conversion efficiency in a double-junction device alongside silicon.

Kleiman and colleagues have done some theoretical modeling to work out what the best match would be. "Our plot tells us clearly that for a double-junction device with silicon as the substrate, we would like our second (upper) junction to have a bandgap of about 1.68 eV," explained Kleiman, adding that the design would have a maximum theoretical efficiency of 43.5%.

While triple-junction cells designed for high-concentration photovoltaic systems have already been measured to deliver a real-world efficiency close to that theoretical mark (at a 240-sun concentration), the maximum figure for triple-junctions under unfocused sunlight is much lower, and – in theory – is comparable to that of the silicon/III-V hybrid.

"We are targeting a more modest 30% efficiency," Kleiman said, on the assumption that it would be possible to make a cell work at three-quarters of the theoretical maximum. He believes that the approach will only add a modest incremental cost to the processes currently used to make single-junction crystalline silicon cells.

Kleiman freely admits, however, that MBE will not be the ideal deposition method for the intended focus on high-volume, low-cost applications: "The later part of the project will focus on transferring the technology to a manufacturable process, such as MOCVD."

Although the practical side of the research is only at a very early stage right now, the team will be able to draw on the experience gained during the photonics boom, where Canadian researchers and companies were at the cutting edge of compound semiconductor chip technologies designed for fiber optic communication networks.

Ambitiously, the team is hoping to transfer the technology out of the lab and into a commercial fab in just three years.

However, interfacing a compound semiconductor with silicon is notoriously difficult, as Kleiman acknowledges: "I think that the central goal is a detailed microscopic understanding of the III-V-to-silicon interface," concluded the researcher. "Structurally, chemically and electronically."

HIGH-BRIGHTNESS LEDs

Emerging sectors speed LED recovery

Now much less reliant on mobile phone backlighting, the market for high-brightness LEDs is bouncing back from two years of sluggish growth, writes **Michael Hatcher**.

Thanks to increasing penetration in products such as digital cameras, notebook PC backlights and cars, the market for packaged high-brightness LEDs grew by nearly 10% in 2007 to reach $4.6 billion.

According to Bob Steele, whose annual update traditionally opens the Strategies in Light conference each February, the acceleration showed that the market is recovering from "slow growth" through 2004–2006. Steele now expects the industry to maintain this recovery as the HB-LED market grows to more than $11 billion over the next five years.

While a staggering 39 billion units were shipped during 2007 (up 26% on 2006), it is now clear that HB-LED makers are becoming much less reliant on the mobile phone industry.

That's good news for chip makers, because price erosion in the mobile phone sector is a major influence on the overall market and a key reason why market growth has languished at only 6% for the past couple of years. Steele told delegates that the HB-LED product mix is shifting significantly as new, more lucrative applications come to the fore.

And while mobile applications still represent a 44% chunk of the overall market, digital camcorders, MP3 players and portable DVD players are pushing back the reliance on the basic mobile phone.

In 2007, the mobile phone market for HB-LEDs grew by only 3.3%, to approximately $1.6 billion. In contrast, the market for all other mobile applications jumped 21% to $264 million. Steele expects this trend to be a strong one over the next few years, predicting that by 2012 notebook PCs will represent the biggest mobile application outside of the humble phone.

That shift is already happening, judging by the large number of notebook PC makers now using white LEDs in their backlights. Apple, Dell, Acer and HP were four big-name brands to come out with LED-backlit models during 2007, as LED market penetration more than quadrupled to 3.2%.

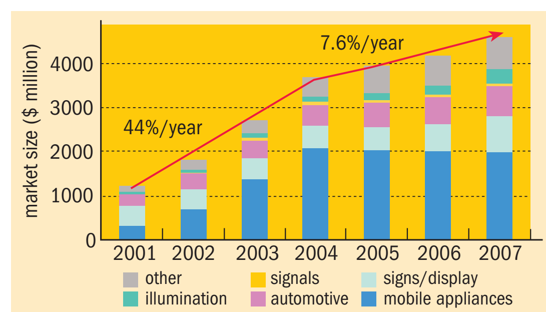
While the display backlight market is moving quickly, the same cannot be said of the automotive market for LEDs, which is showing a more gradual, somewhat stuttering shift to solid-state technology.

Despite white-LED headlamps now appearing in series production, some lighting functions have switched from LEDs back to incandescent lamps, most notably the latest version of Honda's popular Accord. While certain automotive applications are dominated by LEDs, market penetration in stop, turn and tail lights remained flat in 2007 at just 8.5%.

Steele is predicting much more rapid growth in the "signs and displays" sector, which he says will come to dominate the overall HB-LED market by 2012. While the market for large-scale video screens is continuing to grow, with events such as the Beijing Olympics providing its predicted boost, the big driver expected in this sector is in large-scale LCD panel backlighting, for desktop PCs and televisions.

PHILIPS

Following its $800 million acquisition of LED lighting specialist Color Kinetics last year, Philips has kitted out its Burlington, MA, solid-state lighting headquarters with the latest LED technology. Its conference rooms incorporate both colored and white LEDs.



STRATEGIES UNLIMITED

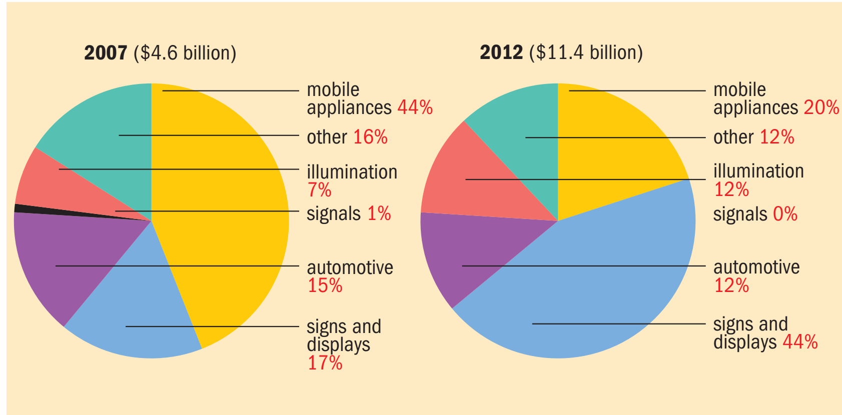
Savage price declines and an over-reliance on the mobile phone sector combined to slow the growth of the HB-LED market between 2004 and 2006. However, with applications now spreading, a five-year period of stronger growth is expected.

Korean giant Samsung is behind much of the existing market for LED-based TVs. But while its rear-projection sets use high-specification emitters from the US company Luminus Devices, this is a market in decline, having been usurped by the LCD panel.

For LCD TVs, cold-cathode fluorescent lamps (CCFLs) have proved to be a tough backlight to beat. As well as declining in cost, CCFL makers have improved their technology to yield high-quality TV pictures. As a result, proponents of LEDs have changed their marketing tack to focus on other advantages of the solid-state approach, such as the ability to dim the screen locally and the lower energy consumption of LEDs compared with CCFLs.

While Samsung is again forging the path in the LCD TV space, it is not using the Luminus emitters, preferring phosphor-based white LEDs to RGB. But with up to 1000 LEDs still required to illuminate a

PHILIPS



STRATEGIES UNLIMITED

Applications in general illumination, such as this white-LED downlight from Philips Solid-State Lighting (left), are growing fast, but with a number of "rogue" suppliers trying to capitalize on the demand for energy-efficient products, the lighting industry must work hard to adopt standards and avoid consumer disappointment. By 2012, LED-backlit LCD TVs and desktop PC screens are expected to boost the "signs and displays" sector into a dominant position (above).

40 inch TV, this remains an expensive technology to deploy. Samsung's entry-level 40 inch screen with LED backlighting costs $2800.

"CCFLs are getting better and cheaper, and [LED] cost is the main issue," Steele said, although he describes the picture quality as "outstanding" and something for which high-end customers will pay a premium. And because it is such a large market, even modest penetration in TVs will create a substantial business for the successful LED providers.

Of the different types of LEDs, high-power emitters (with a drive current of more than 150 mA) are growing fastest – representing 10% of the market for the first time in 2007, and now the second-biggest sellers behind standard LEDs and ahead of high-current (50–150 mA drive current) and RGB multichip sales.

For high-power chips, the two biggest applications by far are mobile (39%) and general illumination (37%). The latter was another fast-growing submarket for HB-LEDs in 2007, leaping 60% over the previous year to $330 million.

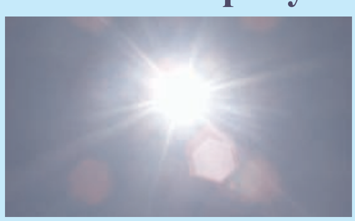
With standards still to be finalized, LED-based general lighting is in its early gestation period and the quality of available luminaires is highly variable – as evidenced by the early findings of the US Department of Energy's CALiPER testing program. Steele highlighted LED Lighting Fixtures, now part of the Cree empire, as the company leading the way in this sector, as far as energy efficiency is concerned.

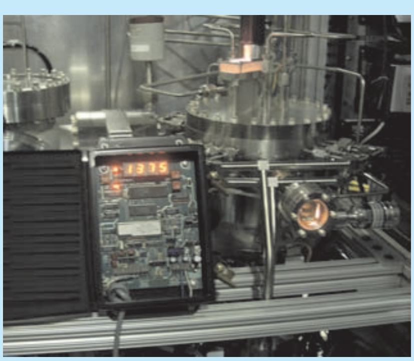
With a 60 lm/W warm-white LED lamp already on the market, and a NIST-verified 113 lm/W warm-white prototype in development, the Cree subsidiary is selling mostly to commercial and institutional, rather than residential, customers right now. Part of the secret behind the high efficacies achieved is the unique color combination used. It mixes a phosphor-converted yellow-green emission with that from red LEDs to reach the market-leading figures.

But although the energy efficiency of solid-state lighting is not in any doubt, Steele reminded his audience that many challenges remain – again, chiefly, the high up-front investment required. While London in the UK and Tianjin in China are the most recent assignees to LED streetlighting programs, the payback period of today's commercially available technologies does not yet make much economic sense and will require hefty subsidization. Aside from that, there remain issues over color consistency, electrical control and the need for high-efficiency lamp design to make the most of the LEDs' intrinsic capability.

Steele's forecast for the HB-LED market predicts that the accelerating growth this year, to 12% and a total value of $5.15 billion, will be built upon between now and 2012. With rapid growth expected in 2011 and 2012 as LCD backlights begin to make an impact, Steele expects a market size of $11.4 billion in 2012.

By then, portable electronic applications should represent only a quarter of that total, divided almost equally between phone handsets and non-handset applications like notebook PC backlights. In its place as the dominant application ought to be the signs and displays sector, fuelled largely by LCD backlights.





GaN Schottky barrier diode

Manufacturers of switch-mode power supplies can get exactly what they want with Velox's GaN-on-sapphire Schottky diodes: the performance of SiC at a fraction of the price. **Michael Murphy**, **Linlin Liu**, **Milan Pophristic** and **Boris Peres** detail the advantages of the technology.

Soaring energy prices and an increased awareness of environmental issues are spurring the development of products that consume less energy. For computers and other consumer and industrial electronic products, one area with the potential for improvement is the switch-mode power supplies (SMPSs) that convert AC mains into various DC formats. Ideally, these supplies would now be delivering higher efficiencies through the employment of SiC high-voltage Schottky barrier diodes, but the high price of these devices is preventing them from displacing the less efficient silicon equivalents that still dominate the high-power semiconductor market.

However, it will soon be possible to enjoy the benefits of a wide-bandgap semiconductor – high breakdown fields, good thermal conductivities, and high electron mobilities and saturation drift velocities – by turning to GaN instead. On sapphire substrates, GaN promises to be a much cheaper alternative to SiC. This combination of materials may raise a few eyebrows, because it is widely believed to suffer from sapphire's low conductivity – something that ultimately leads to poor thermal resistances and hot, unreliable devices. But at Velox Semiconductor, located in Somerset, NJ, we have demonstrated the folly of this argument with GaN-on-sapphire diodes that are incorporated in an insulating frame.

The compatibility with an insulating frame is a big advantage over SiC, because it reduces the cooling demands of the heat sinks employed in the SMPSs. In these modules we have found that our devices deliver efficiencies comparable to SiC and significantly better than those of silicon.

The manufacturing cost-savings over SiC equivalents stem from cheaper, larger substrates and a lower epiwafer growth temperature. We are building our devices on 100 mm sapphire, which has primarily been developed for the multibillion-dollar GaN LED industry as it transitions away from 2 and 3 inch wafers. Multiple vendors are now supplying the larger-sized material, and prices are falling thanks to healthy competition and continuous manufacturing improvements. There might also be an option of scaling to even larger substrates in the near-term, as 150 mm research and development material is already available from leading manufacturers.

Switch-mode power supplies, such as this 350 W supply, are used to conver electronics products. Today all of the manufacturers of these supplies use Si sapphire equivalents by the end of the year, which are being developed by Ve packages. If silicon or SiC devices are used, one of the electrodes must be po GaN is used both contacts are made on the top of the device, making the fra sapphire, which can provide more than 2400 V of isolation from the frame if t

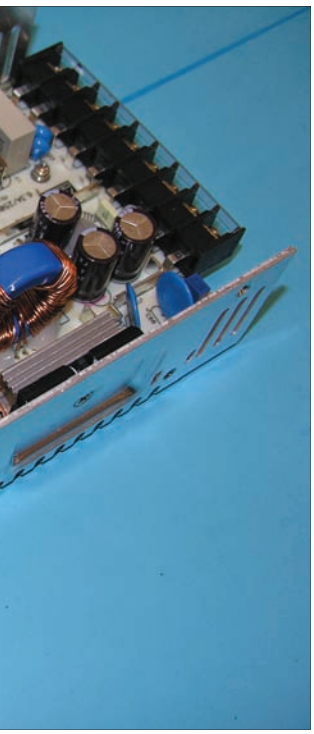
In contrast, 100 mm SiC substrates are only available in limited quantities at outrageous prices, so manufacturing and development is undertaken on the 75 mm platform. This smaller size is still pricey and we have found that its cost per unit area is typically four times that of sapphire (table 1).

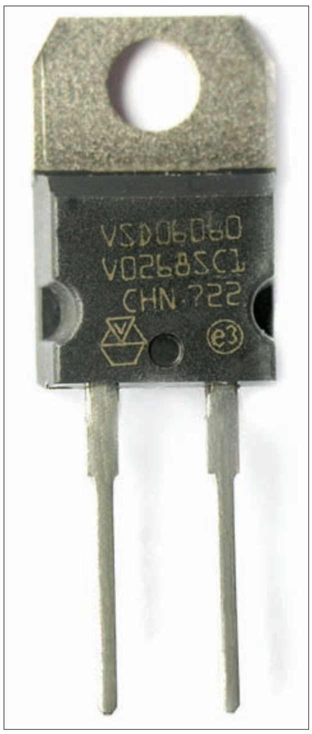
Working with larger wafers brings an obvious advantage – more chips per wafer. However, there is a secondary benefit, as the majority of semiconductor equipment available is developed for substrates with diameters of 100 mm or more. This means that it is easier to equip a fab with production equipment and there is more choice for outsourcing processes.

Further gains are realized from GaN's lower growth temperature (1000–1100 °C versus 1500–1600 °C for SiC). Reactor parts for SiC growth are also very expensive, not particularly reliable and suffer from a much smaller supply base.

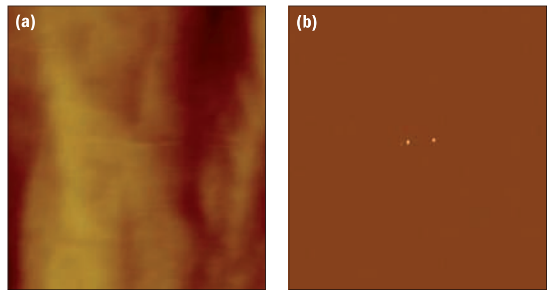
Producing marketable nitride power devices requires the growth of high-quality, uniform thick epitaxial layers. GaN does not suffer from "micropipe" defects that plague SiC, but disloca-

s threaten to overturn SiC





C mains into DC outputs for computers and other consumer and industrial
nd silicon devices, but they will also have the option to select GaN-on-
Semiconductor. All three types of device tend to be housed in TO-220
oned at the bottom of the device and make the contact with the frame. When
solated. This advantage stems from the excellent insulation properties of
wire bonds are made to the legs that are not connected with the frame.



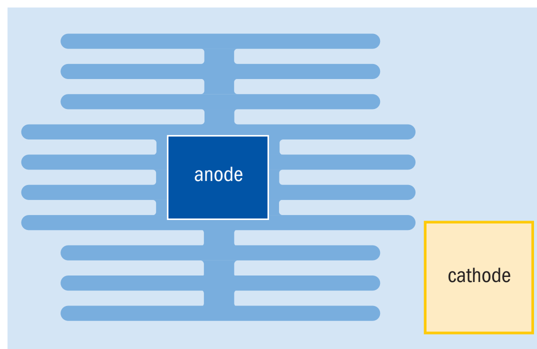


Fig. 1. (left top) Conductive atomic force microscopy images reveal that Velox's GaN-on-sapphire films are reasonably flat **(a)** and typically have just a couple of conductive dislocations in one of the 20 scans of a $50 \times 50\,\mu m$ area **(b)**. These dislocations, which appear as white dots on the background, have a density of $10^3\,cm^{-2}$.
Fig. 2. (left center) Velox employs a patented interdigitated geometry for its GaN Schottky diodes, which cuts the lateral spreading resistance and boosts the conducting current.

Table 1. Substrate costs

Substrate size and material	*Cost per centimeter-squared*
75 mm SiC	~$9
100 mm sapphire	~$1.9
150 mm silicon	~$0.11

tions can result from lattice mismatches between the substrate and the epilayers. This problem is also encountered by LED manufacturers, and like them we have developed proprietary nucleation and buffer growth techniques to reduce dislocation densities.

Conductive atomic force microscopy images reveal the high quality of our nitride film, which has a typical conductive dislocation density of $10^3\,cm^{-2}$ (figure 1). These dislocations are probably responsible for reverse leakage currents, but their low density allows us to manufacture reliable low-leakage devices.

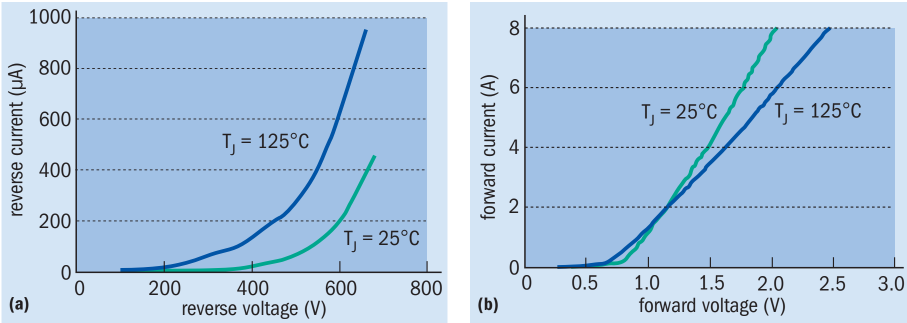
We produce our Schottky diode epiwafers in-house by growing thick GaN and AlGaN layers on insulating sapphire substrates. A patented interdigitated geometry is used to add contacts that maximize the conducting current for the smallest possible chip size (figure 2). This design also minimizes the lateral spreading resistance – the resistance due to current flowing from the bond pads to the device's corners – and this in turn reduces the diode's forward voltage and improves its efficiency when deployed in a SMPS.

Our Schottky diode leakage current is reduced through proprietary surface preparation and passivation techniques. At room temperature these devices have a leakage current of less than 200 µA at 600 V reverse bias, but this rises to 600 µA at 125 °C (figure 3a, p20). Forward voltages of 1.7 and 2.0 V are required to deliver 6 A at room temperature and at 125 °C, respectively (figure 3b, p20). I-V curves show that the behavior of these diodes is close to that of an ideal diode.

Our GaN devices, like their SiC cousins, have a very short, temperature-independent reverse recovery time that is vastly superior to silicon diodes (figure 4, p20). The device's behavior is essentially the same at room temperature and at 125 °C.

Better packages

A major additional advantage of GaN devices over their SiC equivalents is compatibility with an insulating frame, something that stems from the excellent insulation that is provided by sapphire. When these devices are housed in the very common



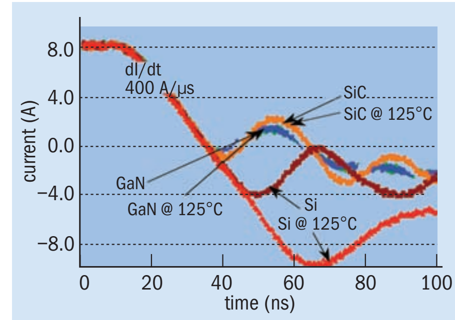


Fig. 3. (left and center) Velox's GaN-on-sapphire Schottky diodes are designed to deliver up to 6 A and block voltages of up to 600 V. **Fig. 4.** (right) Velox's GaN-on-sapphire diodes deliver excellent switching performances. Variations with current as a function of time are superior to silicon devices and very similar to SiC diodes.

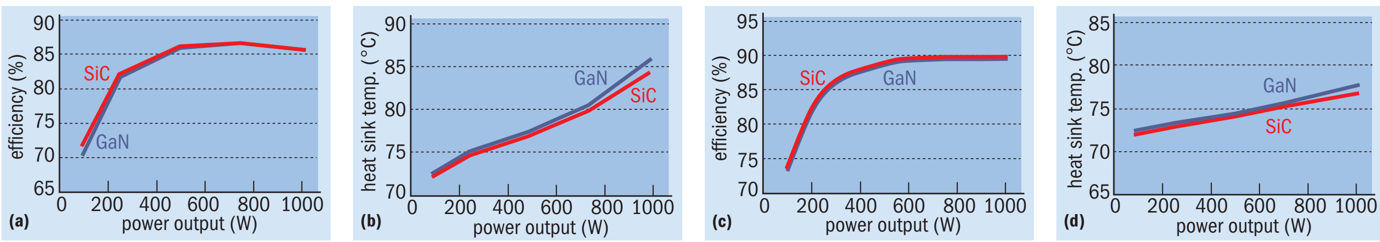


Fig. 5. A 1000 W, 48 V switch-mode power supply was used to test the capability of Velox's GaN-on-sapphire diodes. These 6 A devices, which have a 100–400 μA room-temperature leakage current at 600 V and a forward voltage of 1.6–2.0 V, replaced SiC equivalents with the same current rating and forward voltage, but a leakage current range at 600 V of 50–200 μA. The efficiency of the entire power supply at 100 V **(a, b)** and 230 V **(c, d)** inputs was measured by a Yokogawa WT3000 power analyzer. This unit was held at 72 °C, and the electrical load was adjusted for 1000, 750, 500, 250 and 100 W output power. A thermocouple was used to measure the temperature of the diodes and their heat sinks. No difference in performance could be measured between the systems employing SiC and GaN diodes.

lead-framed plastic TO-220 packages they can be screwed directly to the heat sink and produce a thermal resistance that is typically just 1.8 °C/W.

SiC devices, in comparison, have a much higher thermal resistance. If non-isolated lead frames are used, then an isolating pad must be inserted between the package and the heat sink, and this increases thermal resistance by 1.0–1.5 °C/W. This additional pad can be avoided by switching to an isolated frame, but any benefit is marginal because this design has a 3 °C/W thermal resistance.

The significant reduction in thermal resistance provided by our diodes is a major plus point for SMPS designers. That's because it can allow heat sinks to operate at higher temperatures, or devices to run cooler for an equivalent heat-sink temperature.

The benefit is significant for diodes operating at 8 A and 2.5 V, which will dissipate 20 W. If the heat sink is operating at 100 °C, typical silicon or SiC devices with a thermal resistance of 3 °C/W will have a junction temperature of 160 °C. This compares to 136 °C for a GaN diode under the same conditions, thanks to the lower thermal resistance. The low operating temperature improves GaN diode reliability.

We evaluated our devices by inserting them into two SMPSs that normally incorporate SiC diodes. These 1000 W, 48 V power supplies originally featured two of Infineon's SDT06S60 diodes (6 A, 600 V) in the power factor correction circuits. We replaced them with our equivalent, the GaN VSD06060 diodes.

Our GaN diodes perform as well as their SiC equivalents at room temperature and at 72 °C, according to measurements comparing the performance of the SMPSs employing both device types (figure 5). The tests used thermocouples to measure the temperatures of the diodes and heat sinks at various input voltages and loads. We also recorded the total power supply efficiency at these operating conditions. No difference in system performance was measured between the GaN and SiC devices.

We have also conducted standard RF emission tests for our power supplies, which have been measured in modified and original forms and compared against standards for class B equipment. No difference was observed between supplies featuring GaN and SiC diodes, and in both cases the equipment easily passed the class B requirements.

This series of tests demonstrates that our GaN diodes deliver the performance of SiC, but at a fraction of the cost. This product is at the final stages of qualification and should make the transition to production at the end of this year. STMicroelectronics is helping us with the qualification and marketing of these diodes. Future versions of the device operating at high currents and voltages could be used in hybrid electric vehicles and we are developing diodes for this application. However, our next product will be a GaN-on-silicon transistor that promises to deliver very low on-resistance and superior switching characteristics compared to silicon devices.

About the authors
Michael Murphy (top left), Velox's director of epitaxial growth, is in charge of GaN epigrowth, characterization and modeling. **Linlin Liu** (top right) the company's principal engineer, is responsible for process design and development. **Milan Pophristic** (bottom left) is the director of contract research and heads the development of advanced GaN devices. **Boris Peres** (bottom right), the chief operating officer, is responsible for product introduction and marketing.

Further reading

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Substrates & Epiwafers Suppliers Guide

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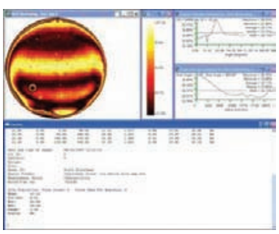

GaN on sapphire epi uniformity map

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NON-POLAR EMITTERS

Rohm shoots for a green diode laser

Rohm believes that it is impossible to make conventional nitride laser diodes that emit in the green, so it has turned its attention to non-polar equivalents. Is this strategy starting to pay dividends? **Richard Stevenson** investigates.

MITSUBISHI

Mitsubishi intends to launch the first laser TV in North America this fall. Pictures will be formed by combining the output of red, green and blue lasers. III-Vs can directly provide the emission for two of these sources, but the green version will be based on a frequency doubled infrared laser.

After years of sterling service, color TVs with cathode ray tubes and 20-something inch screens are on their way out. Larger and cheaper LCD-based screens are now the biggest seller, according to market researcher iSuppli, and this technology is even eating into the "40 inch plus" market that is served by plasma screens. However, laser-based displays threaten to replace all of these technologies thanks to the delivery of even higher-quality pictures.

These displays require affordable red, green and blue lasers, which makes semiconductor devices the preferred option. Red and blue sources already exist in the form of AlInGaP- and nitride-based lasers. However, no III-V design can emit close to 520 nm, the wavelength required for the green component. Although nitride-based lasers are the most promising candidate to reach this wavelength, no-one has even broken the 500 nm barrier. For example, Nichia, the pioneer of the nitride laser, has been increasing the emission wavelength by just a few nanometers each year and has only just released a 488 nm laser.

Extending a conventional nitride laser diode's emission from around 400 nm is not easy because the intrinsic polarization fields cause a large and unhelpful blue-shift of the lasing wavelength. However, this problem can be avoided by growing the epilayers on *m*-plane GaN, which produces non-polar devices that are free from strong internal fields.

Rohm has been following this tack since January 2006, after it decided to turn away from developing *c*-plane laser structures. The company began with the easier task of making a 405 nm device, which contains less strain. Fast progress followed and just over a year later the company published the first ever account of continuous-wave (CW) non-polar lasers in the February 23, 2007, edition of the *Japanese Journal of Applied Physics*. This would have been the first ever report of any non-polar laser if the University of California, Santa Barbara, hadn't published a paper on a pulsed mode *m*-plane laser in the same issue.

Once they had built a blue laser, the Rohm engineers turned to developing longer-wavelength equivalents. Unfortunately, epiwafer cracking prevented this structure from being extended beyond 430 nm. At longer wavelengths more aluminum is needed in the cladding layer to maintain the structure's optical confinement and this leads to more strain in the epiwafer.

However, the researchers managed to overcome this issue by switching the guiding layer from GaN to InGaN. With this change, optical confinement could be maintained while reducing epiwafer strain, because less aluminum is required in the cladding.

This has extended emission, and last summer Rohm reported a 452 nm laser driven in pulsed mode, with a threshold current of 22.3 kA/cm^2 and a threshold voltage of 11.1 V. Since then the researchers have started to refine this device. Distributed Bragg reflectors have been added to the laser facets, reducing the threshold current and producing CW operation.

Already this year, the team has reported better results in *Applied Physics Express*. Pulsed and CW threshold current densities for a 400 µm long laser cavity are just 4 and 5 kA/cm^2, respectively. Emission wavelengths are also moving towards the green – at 457 nm in pulsed mode and 459 nm for CW operation. This shift in wavelength between the two modes of operation is claimed to result from self-heating, which is caused by a relatively high operating voltage of 6 V.

Kuniyoshi Okamoto, a member of the Rohm team, says that there is room to improve the latest laser's threshold currents, but points out that such values are already low enough for commercialization. Obviously there is still work to do to extend the emission to 520 nm and he believes that changes to the composition of the guiding and cladding layers are needed to produce crack-free epiwafers for green emission.

The CW output also has to increase significantly. The 459 nm laser produced 5 mW and Okamoto believes that more than 30 mW will be required for a 20 inch projection display. This is a tough target, but there is no denying that Rohm is making rapid progress and you would not want to bet against them hitting these goals over the next few years.

IQE's epiwafers unite III-Vs and silicon

Attempts at growing III-Vs on conventional silicon tend to end in failure. But germanium-based composites and off-axis silicon can provide a platform for high-performance chips for digital logic and broadband RF applications, say **Dmitri Lubyshev**, **Joel Fastenau** and **Amy Liu** from IQE Inc.

Uniting III-Vs and silicon promises to offer the best characteristics of both materials, while enjoying the benefits of large wafer sizes. However, despite more than 20 years of effort, this marriage is still experiencing some teething trouble.

Initially, development focused on GaAs and its lattice-matched and strained ternaries, such as AlGaAs and InGaAs. These materials were promising candidates for RF applications because they could perform some of the functions traditionally associated with silicon CMOS. But this goal was never fulfilled, despite significant efforts from several research groups and major semiconductor manufacturers, such as IBM and Motorola. The poor material quality of the III-V-on-silicon wafers has thwarted progress, alongside the inferior technology for scaling down III-V feature sizes.

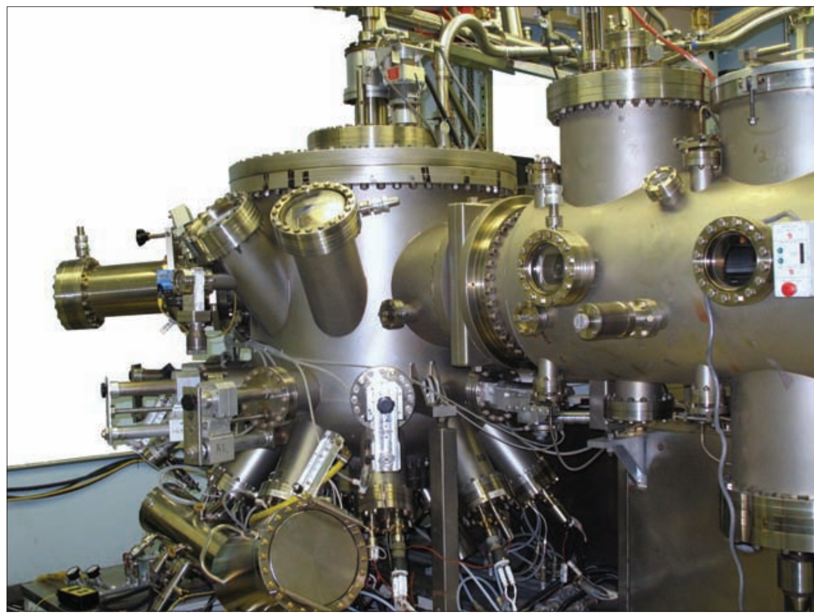
The semiconductor industry is now seeing something of a renaissance in the development of III-Vs-on-silicon, which is viewed as the leading candidate for future high-speed digital logic. At IQE's North America manufacturing plant in Bethlehem, PA, we are supporting this effort by providing customized MBE-grown epiwafers for three different projects: a program run by the US Defense Advanced Research Projects Agency (DARPA) called Compound Semiconductor Materials on Silicon (COSMOS); a separate venture led by Intel to build III-V CMOS; and a similar effort led by Peide Ye from Purdue University, which he details on p29 of this issue.

The COSMOS project, which is led by Raytheon and includes contributions from Teledyne Scientific and MIT, involves monolithic integration of clusters of compound semiconductor devices into silicon CMOS chips. These III-Vs equip the silicon wafers with a level of broadband RF performance that is not possible with conventional CMOS.

In Raytheon's case the clusters are made from III-V circuits based on traditional InP double-heterojunction bipolar transistors and HEMTs. These must be compatible with CMOS and III-V fabrication processes on the same wafer.

High-quality III-V epitaxy is carried out in window openings on a substrate compatible with the silicon CMOS, followed by the final fabrication of multi-level integrated silicon CMOS and III-V circuitry.

The effort led by Raytheon is just one of many projects that are investigating a variety of techniques for cluster integration, from pick-and-place die level



IQE

IQE is using GaAs and graded InAlAs buffers to produce InP HEMTs and HBTs on silicon wafers.

or wafer-level bonding to direct growth of III-V on CMOS substrates. The key considerations for any approach include the vertical and lateral isolation of the III-V devices from silicon, acceptable levels of power dissipation, compatibility of the epigrowth process with CMOS fabrication, and efficient interconnection schemes between all of the devices.

We also supply epiwafers to the project run by Intel. This effort, which is similar to that being pursued by IBM and Sematech, revolves around the substitution of silicon with III-V devices in the critical circuits of future high-speed digital CMOS logic applications. The building blocks for this type of approach are high mobility modulated doped structures with both n- and p-type channels.

High indium-content InGaAs is a clear focal point for these higher-mobility channels, although some groups are also working with lower-bandgap InAs/Ga(In)Sb alloys. In Intel's case, III-V buffers are used to enable growth of a high-quality InGaAs channel on silicon. Any III-V CMOS transistors that are produced must be compatible with high-k dielectrics for gate isolation and must also employ a structure that is thin enough for device processing with traditional CMOS fabrication techniques.

For all of the projects that we are involved in,

Table 1. Hall-van der Pauw measurements

Substrate	n_s=300 K (cm^{-2})	μ=300 K (cm^2/Vs)	n_s=77 K (cm^{-2})	μ=77 K (cm^2/Vs)
InP	2.98×10^{12}	10,252	2.90×10^{12}	36,107
GaAs	2.96×10^{12}	10,115	2.74×10^{12}	29,138
GeOI/Si	3.04×10^{12}	10,851	2.91×10^{12}	35,445

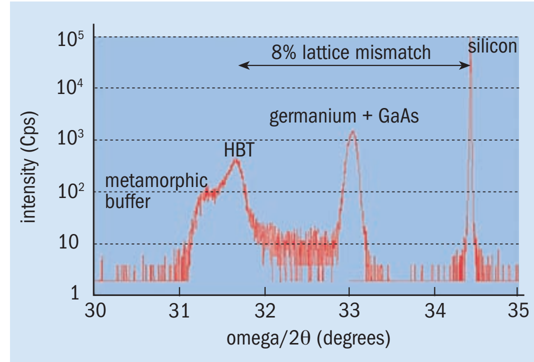


Fig. 1. The COSMOS project led by Raytheon is employing InP transistors that are grown on Soitec's germanium-on-insulator-on-silicon wafers. The thin germanium layer in the GeOI substrate is nearly lattice matched to GaAs, which means that the full span to InP is cut in half to 4%.

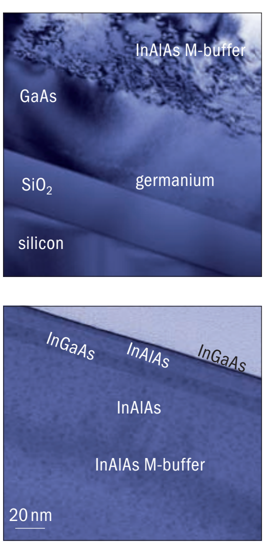


Fig. 2. These cross-sectional transmission electron microscopy images of an InP-HEMT structure grown on a GeOI/Si substrate show no discernable dislocations in the active device layers. The dislocation density at the top of the device active layers is estimated to be 3.5×10^7 cm^{-2}.

integration is only a success if there is no degradation in the performance of the III-V components. After all, if device performance were to drop off this would offset any of the potential benefits that come from the integration of these materials.

However, producing high-quality epiwafers isn't easy, because growth involves a switch from non-polar silicon to a polar compound semiconductor. This transition often leads to antiphase boundaries and stacking faults in the crystal layers.

An additional challenge is the engineering of the lattice parameter from silicon to the particular III-V alloys employed. This must be carried out while efficiently filtering the threading dislocations that result from growth of mismatched crystal structures. These dislocations – which can be formed at the epilayer-substrate interface or during the growth of the buffer – can propagate into the device's active layers and degrade performance and reliability. The growth process must also prevent cracks and additional dislocations in the epiwafer's surface, which can result from significant differences in the thermal expansion coefficient between the host substrate and the active layers. The surface and layer interfaces must also be smooth enough to ensure good transport properties and high-quality device fabrication.

Selecting the substrate

The advent of specially engineered compound substrates has equipped us with a range of CMOS-compatible alternatives to the standard silicon substrate. However, whatever platform is used, it is still essential that the defect density is minimized during initial nucleation of III-V materials. The growth must also restrict the number of misfit and treading dislocations caused by lattice mismatch.

The most straightforward scheme for uniting the materials is direct growth of GaAs on silicon. However, this approach has a major drawback: issues relating to the polar to non-polar switch and the misfit dislocation have to be attacked simultaneously at the interface between the substrate and the epilayers. With alternative forms of substrate, however, it is possible to address one issue at a time.

It's this latter option that we've adopted for our role in the COSMOS project, where we have employed growth on Soitec's germanium-on-insulator-on-silicon (GeOI/Si) wafers, which are made by proprietary SmartCut technology. This composite's great strength is that it provides separate, mutually acceptable platforms for the creation of III-V devices side-by-side with silicon CMOS.

Growth of III-Vs on germanium, the top surface of this wafer, is already used for the manufacture of solar cells. It's easier to deposit high-quality GaAs on this surface rather than silicon, due to the smaller lattice mismatch between the materials.

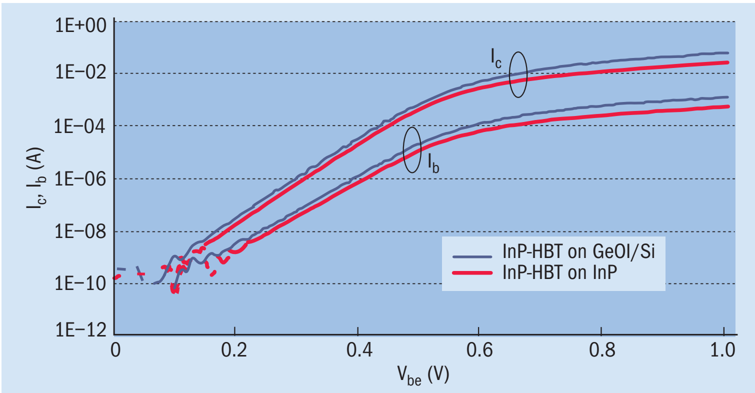
The germanium layer in the composite substrate is just 100 nm thick and is perfectly isolated from the silicon substrate by an amorphous SiO_2 layer. This allows the wafer to be put through standard CMOS fabrication processes, so long as the III-V devices can be successfully grown and fabricated within masked windows on this wafer, and these areas can be subsequently masked. The CMOS and III-V devices are electrically isolated by the SiO_2 layer, but it is relatively simple to connect them.

A commercial production MBE system with 8 inch diameter substrate capability carries out our InP-based growths on GeOI/Si substrates. The 8% shift in lattice constant from silicon to InP is revealed by X-ray diffraction spectra of this epiwafer (figure 1).

Growth of the epistructure begins with a 0.6 µm thick GaAs buffer and a 1.1 µm thick graded metamorphic buffer that adjusts the lattice parameter to that of InP. Linear grading of InAlAs is used for this layer, which features an inverse graded step that helps to compensate for residual strain from plastic relaxation and thermal expansion. Ideally, this metamorphic structure provides a smooth, defect-free surface that is electrically resistive, as these characteristics are wanted for growth of the active layers.

We independently optimized this buffer for InP HBTs and HEMTs. Our epiwafers were cross-hatched, as are those of InAlAs metamorphic structures grown on GaAs. These InP on GeOI/Si structures are suitable for lithography and device processing as their root-mean-square roughness is only 3 nm, according to atomic force microscopy images.

Our epiwafers also have a clean interface between GaAs and germanium, according to cross-sectional transmission electron microscopy images that reveal the scarcity of anti-phase boundaries, dislocation nucleation and propagation (figure 2). Closer



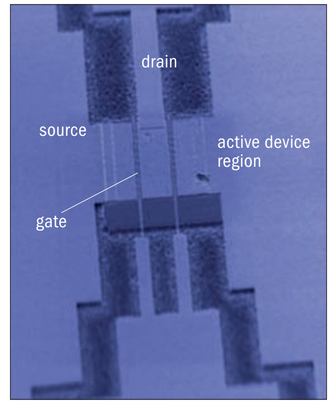


Fig. 3. (far left) InP-HBT large-area devices fabricated by GeOI/Si substrates deliver a performance that's very similar to equivalent structures built on InP, according to measurements of DC characteristics and Gummel plots. **Fig. 4.** (left) IQE has provided the epiwafers for Intel's effort at developing III-V CMOS. This program revolves around quantum-well field-effect transistors, which are shown in this scanning electron image.

Table 2. Large-area device DC measurements

Substrate	*Gain (ß)*	*Base R_{sh} (Ω)*	*V_{offset} (V)*	*BV_{ceo} (V)*	*B-E: V_f/V_r (V)*	*B-C: V_f/V_r (V)*	*Ideality factors (n_c/n_b)*
InP	60	647	0.10	5.0	0.51/2.7	0.42/7.0	1.08/1.29
GeOI/Si	55	644	0.12	4.9	0.52/2.4	0.42/6.5	1.10/1.28

examination of the GaAs layer shows that the anti-phase boundaries quickly annihilate. This layer has a dislocation density below the instrument's lower limit for detection, which stands at 1×10^7 cm^{-2}. The active layers of the InP-HEMT (figure 2) are essentially dislocation free and exhibit abrupt, smooth interfaces. More recent plan-view images on HBT structures with our metamorphic buffer show residual dislocation densities as low as 3.5×10^7 cm^{-2}.

We have evaluated our material with Hall transport measurements and built large-area devices that we have compared against the same device stacks grown on InP. The mobility, μ, and carrier concentration, n_s, of our InP HEMTs on GeOI/Si are nearly identical to our reference transistors grown on lattice-matched InP (table 1).

Our InP HBTs on GeOI/Si are vertical transport devices, which makes them more sensitive than their HEMT equivalents to threading dislocations in their active layers. These dislocations are expected to degrade current gain and breakdown voltage. However, our HBTs on GeOI/Si wafers deliver a comparable performance to those grown on InP, according to large-area DC device test structures with 100 μm × 100 μm emitter mesas (figure 3). Both devices have nearly identical base sheet resistance, and very close breakdown voltages, ideality factors, Gummel plots and I-V curves. The HBT that's built on GeOI/Si has an inferior current gain, but the difference is less than 10%.

Small-area HBTs with an f_T of 170 GHz have been fabricated from these wafers by our collaborators, Teledyne Scientific. Details of these devices will be presented at this year's InP and Related Materials conference, which is held in Paris on May 25–29.

Results from one of our other projects, Intel's effort at developing III-V CMOS, were reported at last year's International Electron Devices Meeting. This program focuses on the fabrication of InGaAs quantum-well field effect transistors (QWFETs) for digital applications (figure 4), which have already been shown to deliver a superior performance to all-silicon n-type MOSFETs. Gain is double that of the silicon MOSFET when both devices run at the same power, and power dissipation is just one-tenth when both transistors operate at the same speed.

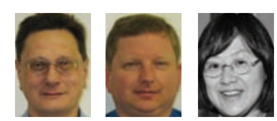
The QWFET is fabricated by direct nucleation of GaAs on misoriented, 4° off-cut silicon. Growth of a graded InAlAs layer follows to reach the InP lattice constant. Careful selection of the growth conditions for nucleation is required once again, due to the switch from non-polar to polar material and the large lattice mismatch between GaAs and silicon. An enhancement-mode HEMT structure is grown on this buffer, which features a strained $In_{0.7}Ga_{0.3}As$ quantum-well. The device has a low density of dislocations, because they are generally confined to the buffer, which is just 1.3 μm thick.

The projects that we are involved with are delivering promising results, but there is more to do. For example, our next contribution to the CMOS project will involve the development of HBT growth processes on patterned silicon-based CMOS wafers.

The integration of III-Vs and silicon is clearly an important goal. Success promises to lead to commercial applications in high-speed mixed analogue and digital circuits for military customers as well as in advanced microprocessors and supercomputers, and also military applications. A few years ago the thought of uniting silicon and the III-Vs would have been just a pipe dream, but now the concept is even appearing on several silicon roadmaps.

Further reading

D Lubyshev *et al.* 2007 *NAMBE.*
M K Hudait *et al.* 2007 *IEDM.*
T Yang *et al.* 2007 *Electronic Materials Conference.*



About the authors

Dmitri Lubyshev (left; dloubychev@iqep.com) is the principal scientist at IQE, **Joel Fastenau** (middle) is the company's MBE engineering manager and **Amy Liu** (right) is the director of research and development. They have been working on III-V epigrowth development for eight years.

InP-HEMT and HBT on GeOI/Si work was carried out in collaboration with Ying Wu at IQE, Bill Hoke, Jeff LaRoche, Katherine Herrick and Tom Kazior at Raytheon, Mayank Bulsara and Eugene Fitzgerald at MIT, and Miguel Urteaga, Wonill Ha, Joshua Bergman and Bobby Brar at Teledyne Scientific. The InGaAs QWFET results published at the 2007 IEDM conference were co-authored by Mantu Hudait, Gilbert Dewey, Suman Datta, Jack Kavalieros, Ravi Pillarisetty, Marko Radosavljevic, Titash Rakshit and Robert Chau of Intel.

InGaAs revolutionizes III-V MOSFETs

Several decades of research have failed to boost the tiny currents in inversion-mode III-V MOSFETs. However, massive improvements are possible by combining indium-rich InGaAs channels with high-k dielectrics grown by atomic-layer-deposition, explains **Peide Ye** from Purdue University.

It's impossible to deny that silicon is an incredibly successful semiconductor because it forms the key ingredient in a microelectronics industry worth more than $500 billion a year. However, this material still has its weaknesses, and its MOSFETs are limited by their relatively slow mobility. III-Vs, such as GaAs, InSb and InAs, are substantially better in this regard, and this advantage has fueled more than 40 years of development of a compound semiconductor MOSFET. These decades of research have produced several minor successes, but any real progress has been held back by the complexities associated with unraveling the physics and chemistry of compound semiconductor surfaces and interfaces.

The story of the III-V MOSFET began in 1965, when the Radio Corporation of America announced that it had built the first GaAs MOSFET. This transistor produced a very low current, so efforts were soon under way to boost this key characteristic. SiO_2 was quickly discarded as a good gate dielectric for GaAs and since then the search has been on for low-defect, thermodynamically stable alternatives.

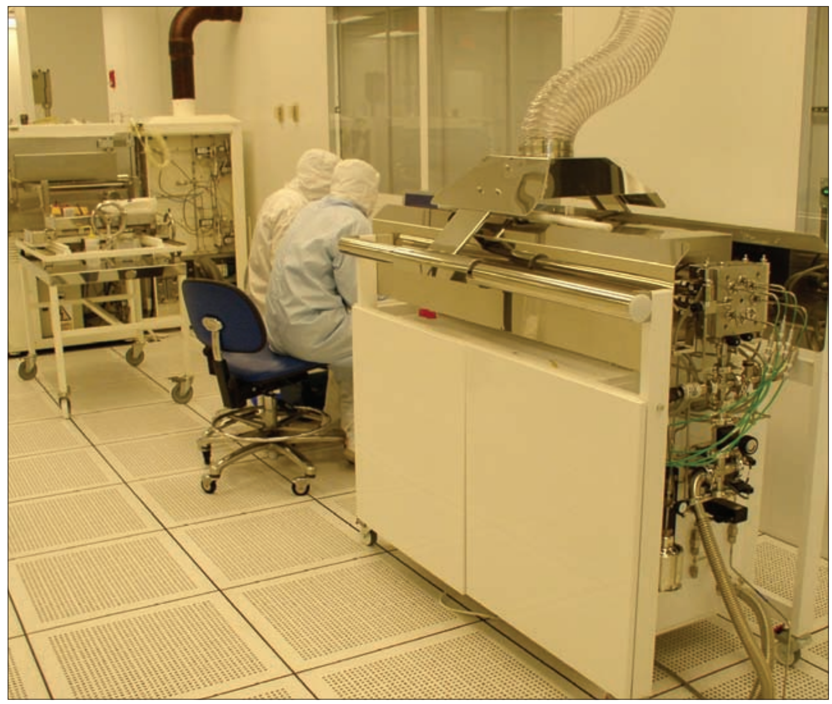
The most significant advances have occurred approximately every 10 years and have focused on GaAs MOSFETs. Initial breakthroughs included the development of pyrolytically deposited silicon dioxide, silicon nitride, silicon oxynitride and aluminum oxide in the 1970s. Sulphur passivation followed in 1987, which improved the device by cutting the GaAs surface recombination velocity, and 1996 saw the introduction of Ga_2O_3 and Gd_2O_3 oxides. These films produce good-quality interfaces, but require a multichamber MBE technique that is unsuitable for high-volume manufacturing.

Recent advances

We have now entered the fifth era of advancement for III-V MOSFETs. This has been led by Intel, which is seeking alternative technologies beyond silicon CMOS. These could include germanium, III-Vs, carbon nanotubes and possibly graphene.

Today's efforts on III-V MOSFETs have expanded beyond GaAs and can be subdivided into those based on arsenides, phosphides, nitrides and antimonides. These compounds have a wide range of bandgaps and carrier mobilities, so they are suited to different applications.

The antimonides, a material system that Intel has been working on in collaboration with the UK defense and technology company Qinetiq, is well suited to high-speed, low-power digital applications. High mobilities are the key here and InSb devices can deliver electron mobilities of 77,000 cm^2/Vs.



PEIDE YE

Peide Ye's team at Purdue University is producing inversion-mode InGaAs MOSFETs with minority carrier currents of more than 1 A/mm. These transistors feature gates made from Al_2O_3, HfO_2 and HfAlO dielectrics, which are grown by atomic-layer-deposition in an ASM ALD F-120.

Phosphides are also suitable for logic applications, whereas GaN-based MOSFETs could potentially improve the output power, dynamic swing and reliability for RF power applications. Meanwhile, GaAs-based MOSFETs promise to deliver higher mobilities and higher breakdown voltages than the silicon LDMOSFETs that are currently being employed in wireless base stations.

The lack of progress made with all types of III-V MOSFET stems from their relatively poor interfaces. Silicon is blessed with a high-quality, thermodynamically stable native oxide that produces very little carrier trapping – its mid-bandgap interface-trap density is typically just $10^{10}/cm^2$-eV. The quality of this interface results from the passivation of 99.999% of the surface's dangling bonds.

This very high degree of passivation must be

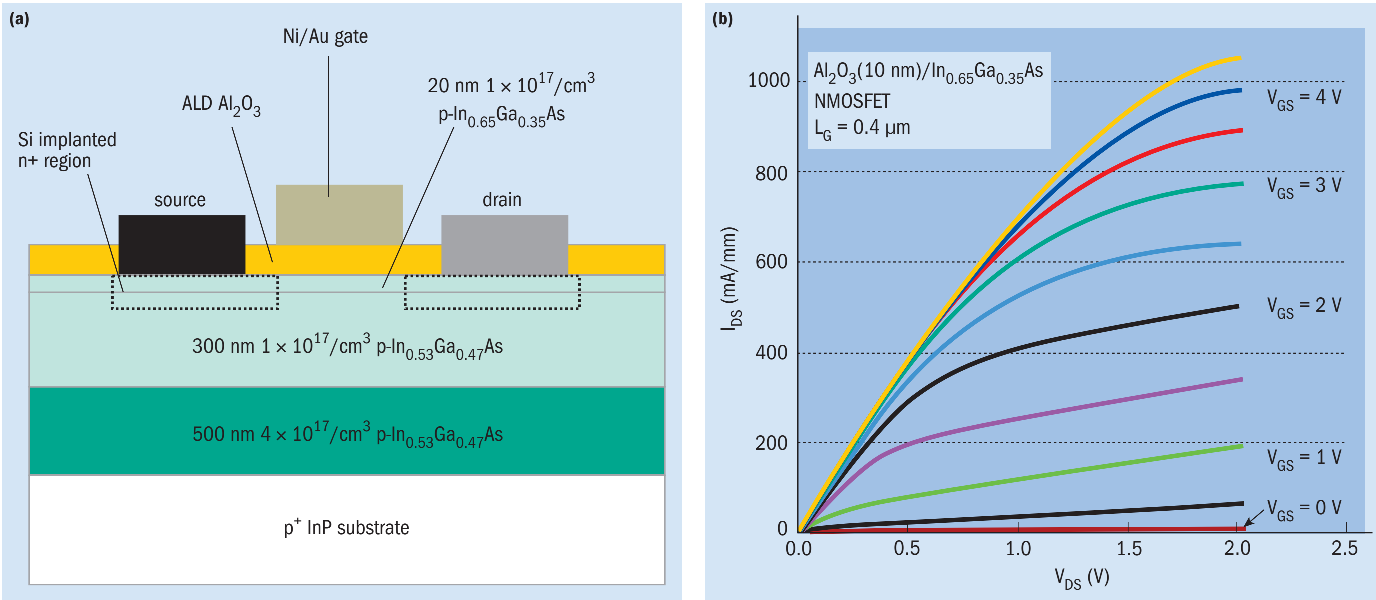


Fig. 1. Switching the GaAs to InGaAs has been the key to improving III-V MOSFETs **(a)**. Current-voltage curves **(b)** show that the inversion-type E-mode $In_{0.65}Ga_{0.35}As$ MOSFET is normally off at zero bias, which makes it suitable for digital applications. This transistor has a 10 nm thick Al_2O_3 gate dielectric and a 0.4 µm gate length.

replicated in the III-Vs if they are to deliver a similar performance to their silicon cousins. However, this is a real challenge for compound semiconductors because their native oxide is far more complicated. In the case of GaAs, it is a leaky and defective mixture of Ga_2O_3, As_2O_3 and As_2O_5. Such a material causes pinning of the Fermi level, which nullifies the device performance by preventing any bending of the surface potential.

Finding a material that perfectly passivates all of the dangling bonds of gallium and arsenic is a real challenge. Decades of effort in industry and academia has focused on this very problem, which has involved attempts to demonstrate a GaAs MOSFET working under inversion operation – the configuration that's suited to digital applications and employed in silicon. However, all of the researchers have had very little to show for their toil and have tended to turn their back on this field after only producing poor-performing transistors. High currents are a key measure of device quality and these versions have only delivered in the nanoamp or microamp range. This lack of success has left a bad legacy – even today young researchers tend to avoid this field after hearing scare stories of years of effort lost to Fermi level pinning.

The interface issue doesn't just plague III-Vs – it is starting to become something of a headache for silicon. That's because the dielectric properties of silicon dioxide are not good enough for CMOS at the 45 nm node, which has forced this community to search for other compounds that could provide a high-k dielectric solution.

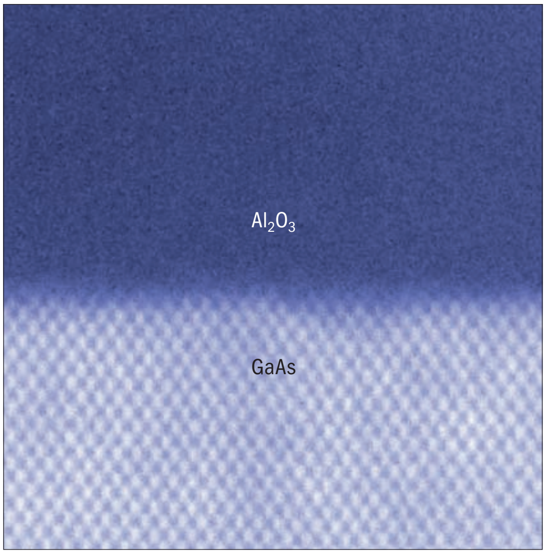
Well funded research in this field began in the late 1990s and has had great success. It is now possible to deposit high-k dielectrics on silicon using atomic-layer-deposition (ALD), a technique that involves the growth of a single-atomic layer of one element, followed by purging of the growth chamber and growth of a second single-atomic layer of another element. Purging follows again and the growth is repeated to form a film. This approach is now a manufacturable technology that can be applied to the 45 nm CMOS node and beyond.

Borrowing from silicon technology

At the end of 2001, while working at Bell Labs/Agere Systems in Murray Hill, NJ, I applied ALD to III-V devices. This was carried out in collaboration with my colleague Glen Wilk, in the same building where the transistor was first invented, and involved the growth of MOS structures with high-k dielectrics Al_2O_3 and HfO_2.

We got off to a great start, with a shocking but very pleasing result. Our first GaAs capacitor – which was fabricated to evaluate interface quality – produced channel modulation, even though it was grown without the prior removal of the native oxide. The reasons behind this success are now understood, because ALD has been shown to produce a "self-cleaning" effect, according to researchers at various institutions including IBM, Rutgers, the National Tsinghwa University in Taiwan, the University of Texas in Dallas and the University of Texas in Austin.

The early successes with ALD sparked a dramatic growth of the III-V MOSFET community, which now includes many leading universities and the industrial giants Intel and IBM. However, transistor currents are still languishing in the 1–100 µA range when operated in the inversion-mode configuration that is required for digital applications (this mode of operation involves the generation of a minority carrier current between the source and drain, which



PURDUE

An abrupt transition occurs between the GaAs and Al_2O_3 layers grown by atomic-layer-deposition at 300 °C, according to cross-sectional high-resolution transmission electron images. The native oxide is etched away by ALD's "self-cleaning" process.

is introduced by the field-effect from the gate bias). These currents are hardly any better than those reported 20 or 30 years ago.

However, vast improvements are possible by employing an InGaAs channel, rather than one made from GaAs, according to research by myself and my colleague Yi Xuan. In 2005 we started to work with InGaAs – a ternary alloy that is already being employed for the conduction channel in GaAs PHEMTs and InP HEMTs. The bandgap of this ternary can be reduced from 1.42 eV (no indium content) to 0.36 eV (no gallium content), which improves characteristics such as mobility and saturation velocity.

We have built a range of inversion-mode surface channel $In_xGa_{1-x}As$ MOSFETs with an indium content, *x*, of 20, 53 and 65%. These transistors, which contain Al_2O_3, HfO_2 and HfAlO dielectrics deposited by ALD, behave in the same way as silicon MOSFETs, but are expected to show a far higher mobility. The version with the least amount of indium produces a current of 1 mA/mm, but this rockets to 0.4 A/mm and more than 1 A/mm for MOSFETs with an indium content of 53 and 65%, respectively. Our $In_{0.65}Ga_{0.35}As$ transistor is the first III-V surface channel MOSFET that is a real field-effect device with an inversion current of more than 1 A/mm. It even exceeds the upper measurement limit for a standard semiconductor parameter analyzer, which is 100 mA for a 100 µm wide device.

The performance of our 0.4 µm gate length Al_2O_3/$In_{0.65}Ga_{0.35}As$ MOSFET, which has a conduction channel directly underneath the high-k dielectric, is shown in figure 1. The DC current-voltage characteristics show the variations in the inversion current with gate bias. It is suitable for digital applications because it is normally off at zero bias. Turning it on at a positive gate bias provides a drain current of 1.05 A/mm. This drain current is far higher than GaAs PHEMTs and InP HEMTs, and comparable to GaN HEMTs grown on SiC.

Our device's most promising characteristic is its ability to scale down to a submicron gate length. Hopefully this scaling will continue down to the length scales associated with silicon MOSFETs, because this would lead to 10 A/mm or 10 mA/µm III-V MOSFETs at a III-V 45 nm technology node.

Our III-V MOSFET is in its infancy and there is a lot to learn regarding materials, structures and devices. However, we believe that our advances have resulted from an $In_{0.65}Ga_{0.35}As$ channel that has a very high electron mobility and saturation velocity.

We have found that the changes in surface potential for strong inversion are much less for InGaAs channels than those made from GaAs. More importantly, $In_{0.65}Ga_{0.35}As$ has a charge neutrality level that is typically just 0.15 eV less than the conduction band minimum. This prevents the build up of a large number of negative trapped charges at the interface, which can inhibit the introduction of additional inversion carriers by the field effect.

One of our next goals is to cut the mid-bandgap interface-trap density to 10^9–10^{10}/cm^2-eV. Our current ALD-based process can reduce this density to 10^{11}–10^{12}/cm^2-eV, which equates to the passivation of 999 dangling bonds out of 1000. But a manufacturable III-V MOSFET technology demands passivation of 99,999 dangling bonds out of 100,000.

Applications in the community

The silicon CMOS community, which is looking for an alternative device technology for high-speed low-power digital applications, is likely to welcome the introduction of III-V MOSFETs. However, they will insist that they can be produced on silicon wafers of at least 300 mm in diameter. But there may well be a time when it is possible to locally grow germanium and InGaAs on silicon. This could form germanium PMOSFETs and InGaAs NMOSFETs, the building blocks for a new generation of CMOS that still employs silicon substrates, but is not held back by this material's low mobility. However, before we get carried away, we must remember that there is still plenty of work to do to make silicon, germanium and the III-Vs happy bedfellows.

There are also some other potential applications for our high-performance InGaAs MOSFETs. This device could serve low-power RF applications that are less demanding on interface quality. These surface channel MOSFETs can deliver a low gate leakage, large dynamic swing and high linearity.

I am optimistic about the future and I hope that the progress of III-Vs in the silicon CMOS community will parallel that of the high-k dielectrics that were introduced in the late 1990s. That technology is now paying dividends for chip manufacturers and hopefully the III-V MOSFET can follow that path over the next few years. ●

About the author
Peide (Peter) Ye has been an associate professor of electrical and computer engineering at Purdue University since 2005. He previously spent four years at Bell Labs of Lucent Technologies and Agere Systems in Murray Hill, NJ, where he pioneered an atomic-layer-deposition process on III-Vs. His current research focuses on high-k integration with novel channel materials for device applications. He thanks the US National Science Foundation and the Semiconductor Research Corporation Focus Center Research Program for funding his current research.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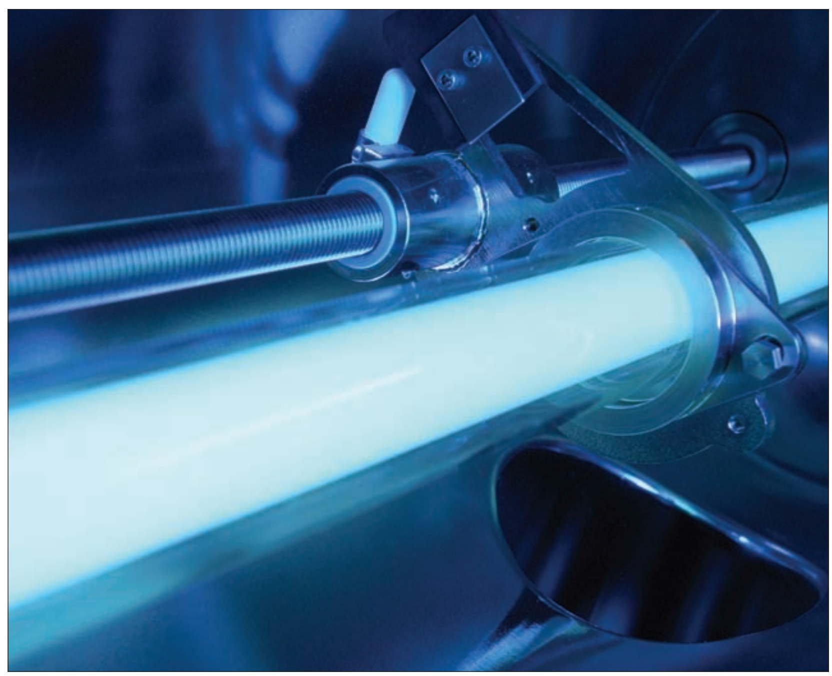
Vertical conduction strategy cranks up UV LED output power

Vertical conduction ramps up the drive currents and output powers of ultraviolet LEDs. Such devices will soon enter the market through Nitek Inc, where they will take on bulky high-voltage UV lamps for use in purification and curing applications, says **Asif Khan** from the University of South Carolina.

Mercury lamps are the dominant source in numerous applications requiring UV light of less than 340 nm. They are used to purify air, water and food, cure polymers, and provide the emission that pumps the blue-white phosphors of fluorescent lamps.

But success has not resulted from a product that totally fulfills the customer's wish list. In fact, this lamp is simply the only option available today and users are forced to put up with its bulky size, high operating voltage, and its use of mercury. This toxic element raises environmental concerns, particularly for the food and medical industries.

What's needed is a solid-state replacement – a high-efficiency LED operating within the UVB and UVC parts of the solar spectrum (see figure 1, p34, for details of the spectral ranges). This would provide an ideal replacement for all of the applications outlined, thanks to its compactness, lack of mercury, low driving voltage and straightforward integration with silicon control electronics. Pulsed-mode operation could also be used to drive the LEDs, leading to significantly enhanced performance in many optoelectronic systems, such as those used for biochemical detection and identification.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The UV disinfection industry has experienced tremendous growth over the last 20 years and purification by this method now amounts to 3 billion liters of water a day globally. Mercury lamps are the leading source, but UV LEDs promise to deliver improvements in lifetime and size.

Developing a solution

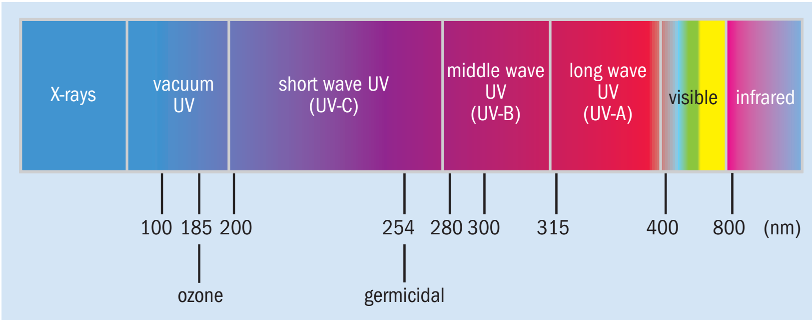
Efforts have been under-way to develop such a source since the beginning of this decade. In the US, research has been driven by the Defense Advanced Research Projects Agency, which guided a program entitled Semiconductor UV Optical Sources (SUVOS). Our team at the University of South Carolina was involved in this four-year, $50 million project. At about the same time Japan started to develop UVB and UVC LEDs through research at various institutions, including RIKEN, the Tokyo Institute of Technology, Meijo University and the University of Tokushima.

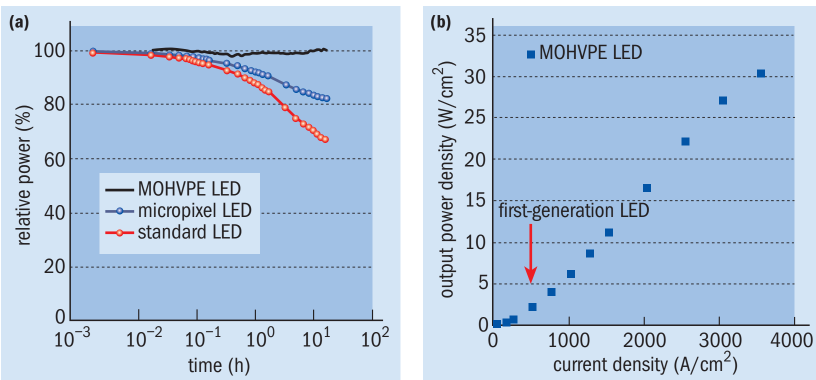
This work initially employed sapphire substrates and AlGaN or AlInGaN multiple-quantum-well-based p-n junctions (figure 2a, p34). Sapphire is available in large sizes and is completely transparent in the deep UV, which enables the use of a flip-chip packaging geometry that features light extraction through the substrate.

However, this combination of materials has its drawbacks. It is difficult to dope AlGaN, and this nitride has a large lattice mismatch with sapphire, particularly at the high aluminum mole fractions of 30–70% needed to produce deep-UV emission.

Between 2000 and 2004 our group developed three innovative approaches to overcome these problems. The first of these was the introduction of AlN buffer layers on sapphire, which were grown by using a pulsed MOCVD approach. This growth process produced films with excellent crystal quality and a very smooth surface.

Our pulsed MOCVD process was also used to fabricate AlN/AlGaN superlattices that reduce





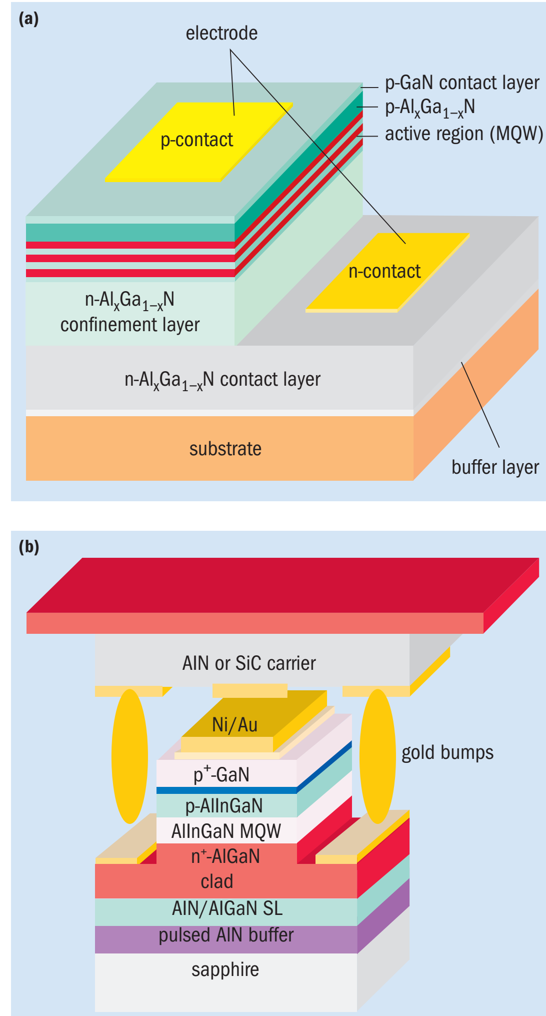


Fig. 1. (top left) The UV spectrum can be divided into three parts: UVA, UVB and UVC. Applications, such as purification and curing, require sources operating in the UVB and UVC spectral ranges, which are currently met with mercury lamps. LEDs, however, provide a more compact alternative that could be integrated with silicon electronics. **Fig. 2.** (right top and bottom) The first UV LEDs from the University of South Carolina were relatively conventional structures **(a)**. These devices suffered from a large lattice mismatch with sapphire and difficulties associated with the doping of AlGaN. But improvements can be made by using a pulsed growth process to produce an AlN buffer and an AlN/AlGaN superlattice, alongside the addition of a p-GaN and p-AlGaN heterostructure **(b)**. **Fig. 3.** (above) Increases in device lifetime **(a)** and output power **(b)** resulted from a switch to metal-organic hydride vapor phase epitaxy (MOHVPE) growth.

epilayer strain and enable the growth of crack-free thick layers of n-type AlGaN. These layers improve device conductivity and reduce current crowding. On top of this we introduced a heterojunction comprising p-GaN and p-AlGaN, which increased p-type conductivity and hole injection.

These improvements led to the fabrication of 280–340 nm devices producing continuous-wave (CW) output power in excess of 1 mW at 20 mA. These LEDs feature flip-chip device packaging that improves thermal management, something that was previously limited by sapphire's poor thermal conductivity (figure 2b).

These first-generation deep-UV LEDs suffered from small output powers, low efficiencies and relatively short lifetimes. Although the flip-chip geometry improves thermal handling, CW output powers saturate at relatively low drive currents due to device heating. Efficiencies are also poor – typically just 1–2% – due to the high dislocation densities in the AlGaN-on-sapphire films. These weaknesses combine to cause premature device degradation – CW lifetimes are only about 200–400 hours at 20 mA. Yet, despite these major shortcomings, these devices are being sold for air, water and food purification, deployment in miniaturized biomedical instruments, polymer curing and deep-UV spectroscopy. Sensor Electronic Technology (SET) – a spin-off of our group that manufactures these devices – is selling them, alongside its strategic partner Seoul Opto-Devices Company of Korea, which also undertakes processing and packaging.

Today we are aiming to address all of these weaknesses, along with other researchers in this field. Considerable effort has been directed at processes for making templates with thick layers of GaN or AlGaN on sapphire, which can form a better platform for UV LEDs. Our research has involved the development of two growth methods: pulsed air-bridge assisted lateral epitaxy (PLOG) and metal-organic hydride vapor phase epitaxy (MOHVPE), which can produce low-defect AlN buffer layers on sapphire that are at least 15 µm thick.

PLOG is a technique that is similar to epitaxial layer overgrowth, but involves pulsing the delivery of one reactant. This variation, which is compatible with both MOCVD and HVPE growth, prevents the growth of adducts, a major cause of defects in high-aluminum-content nitride epilayers.

The MOHVPE technique can bring together the

Research outside of South Carolina

Several major breakthroughs outside of Asif Khan's group at the University of South Carolina have also contributed to improvements in UV-LED technology. These include the high-temperature (1500 °C) air-bridge assisted lateral growth technique developed by Hiroshi Amano and co-workers from Meijo University, Japan. This is an alternative method for growing very thick, low-defect AlN buffer layers over sapphire.

Meanwhile, deep-UV LEDs with vertical conduction geometry have been developed by a partnership between Philips Lumileds, Yale University and Palo Alto Research Center, and a team at the Tokyo Institute of Technology. These devices are made on sapphire substrates with a GaN buffer layer. A vertical geometry is employed and the buffer enables the lift-off of sapphire and formation of a backside n-type contact. However, this GaN buffer also degrades the overall quality of the LED epilayers, leading to a performance well below that of lateral geometry devices.

Efforts are also under way at Crystal IS and Hexatech to fabricate deep-UV LEDs on bulk AlN substrates. This platform is produced using a high-temperature vapor transport growth process that involves slicing substrates from a boule and polishing them.

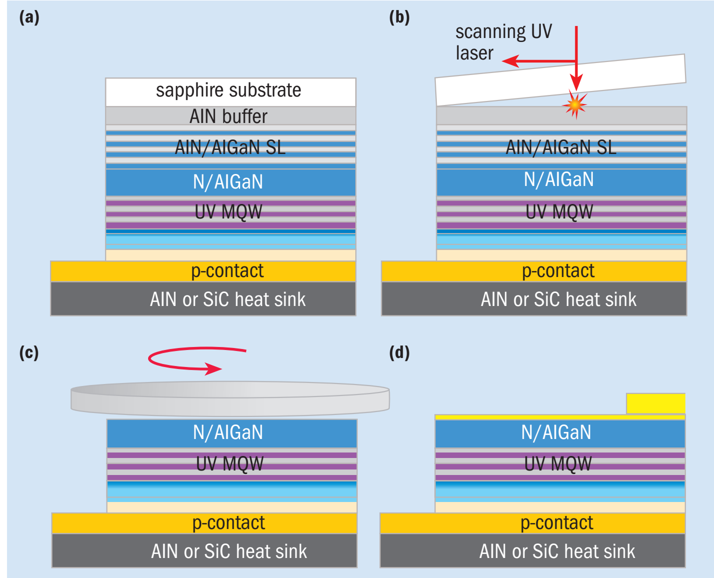


Fig. 4. A vertical conduction geometry promises to boost UV-LED output. This design can be fabricated by growing the epistructure on sapphire and then bonding the top of the epiwafer to a p-contact that is connected to a heat sink **(a)**. Sapphire can be separated by laser lift-off **(b)** and the superlattice removed by mechanical means **(c)**, before a metallic contact is deposited over part of the remaining structure **(d)**.

benefits of MOCVD and HVPE in a single chamber. MOCVD can be used where slow, controlled growth is required, such as the deposition of the buffer, and HVPE can form thick layers in a reasonable time.

Combining PLOG and MOHVPE has led to the production of deep-UV LEDs on AlN-on-sapphire templates that deliver a significantly superior performance to our first-generation devices. Peak power output is increased as higher pump currents can be tolerated, thanks to the better thermal conductivity of AlN epilayers. LED lifetimes also receive a boost, due to reductions in defect densities and improvements in thermal handling capabilities. And 280 nm emitters hardly deteriorated during a 2000 hour lifetime test (figure 3).

Vertical conduction

Recently we have made further improvements to our 280 nm LEDs by introducing a vertical conduction geometry that is similar to that employed by several makers of visible-range LEDs. Again, this approach begins with the growth of the epilayer structure on an AlN-on-sapphire template, but in this case the top surface is bonded to a p-contact connected to a heat sink. The sapphire is then removed by laser lift-off (figures 4a and 4b).

The vertical conduction design is ideal for producing large-area LEDs, including deep-UV lamps. High output powers are possible because this type of device is capable of handling much higher drive currents. In our case, we have built devices that can operate at 1 A. We are currently packaging and testing emitters that will have similar efficiencies to our lateral current LEDs, but total output powers that are 1–2 orders of magnitude higher, thanks to the higher drive currents.

Our improvements in UV performance, which have been driven by optimization of the design, will be implemented in commercial products. Nitek Inc, a spin-off of our research group that is developing deep-UV technologies, is planning to market second-generation deep-UV LEDs made with the PLOG and MOHVPE processes. Patents have been filed for these and other Nitek proprietary technologies. (SET, in comparison, employs a migration-enhanced MOCVD approach). These devices should deliver lifetimes that are well in excess of 5000 hours, thanks to the incorporation of new device geometries that will improve thermal management.

Progress to date has raised the performance of deep-UV LEDs to a level comparable with that of visible nitride LEDs of the mid-1990s. In that community, large-area visible LED lamps were one of the next steps and UV-LED researchers seem to be following a similar path. Indeed, we are not the only research group to develop vertically conducting deep-UV LED lamps. There is a massive market pull for commercialization of such devices, which would offer a welcome alternative to the mercury-based lamps that are employed today.

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About the author
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INFRARED LASERS

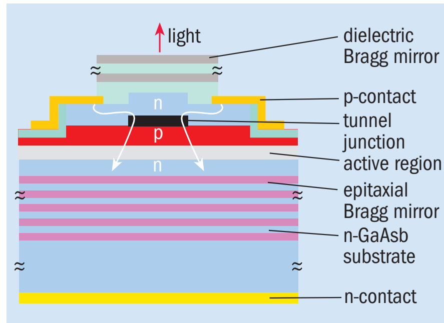
GaSb VCSELs execute CW operation

German researchers have made the first electrically pumped GaSb VCSEL to emit in a continuous-wave mode at room temperature.

The device could efficiently sense gases that absorb in the 2.3 µm region, where the more common InP VCSELs have problems. And although its power is a relatively weak 87 µW, this is expected to improve soon.

"Until now, InP-based devices have shown better output power and wall-plug efficiency," said Alexander Bachmann from the Walter Schottky Institute (WSI) of the Technical University, Munich. "Lasers with GaSb-based active regions show a high gain for emission above 2 µm and due to this our device's performance will catch up to InP within months."

The VCSEL was fabricated by MBE on a GaSb substrate, starting with an n-doped distributed Bragg reflector (DBR) made up of 24 pairs of AlAsSb and GaSb layers. On top of this the active region was deposited, comprising five 11 nm thick GaInAsSb quantum wells and 8 nm thick AlGaAsSb barriers.



A buried tunnel junction allows n-type GaSb to be used above the VCSEL's active region, reducing optical absorption and reverse current flow.

Next came a p-doped layer that the WSI team grew a narrow, highly doped GaSb/InAsSb buried tunnel junction (BTJ) onto to form a conductive current aperture through the upper layers. "This permits the effective pumping of the active region and yields low threshold currents," said Bachmann.

Bachmann and his colleagues then grew an n-doped layer that encapsulates the BTJ and abuts the p-doped layer, forming a diode that prevents reverse current flow. Using n-doped material above the active region rather than p-doped material that typically shows high optical absorption improves optical as well as electrical performance.

After the BTJ-diode layers, which are designed using know-how shared between WSI and commercial VCSEL manufacturer Vertilas, the epitaxy is completed with a four-pair Si/SiO_2 dielectric DBR. The device operated with a threshold current of 3.3 mA, with ongoing research suggesting "robust" lifetimes and single-mode operation.

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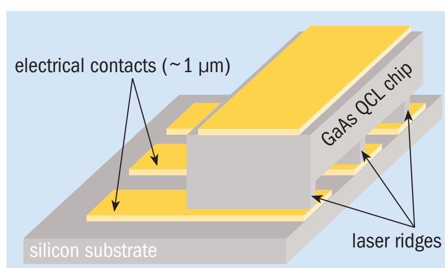
III-V/SILICON INTEGRATION

Heterogeneous bonds get to grips with QCLs

Unlike other light sources that have undergone heterogeneous bonding, the operation of quantum cascade lasers remains unaffected by mechanical attachment to silicon.

The gold-based thermocompression bonding used by researchers from the Technical University (TU) of Vienna and the State University of New York to achieve this could also be used in volume manufacturing. "This technique fits very well into the workflow of a standard silicon fab," said Daniela Andijasevic from the TU Vienna team.

Andrijasevic and her colleagues thermally sputtered 1 µm thick layers of gold onto a 4 inch boron-doped p-type silicon substrate and an MBE-grown GaAs laser, before flipping the laser and aligning it onto the substrate. The bonding was performed under vacuum at 330 °C with a 450 N force used to push the different components together.



Gold thermocompression bonding of QCLs brings the integration of optical communications with silicon CMOS on the chip level a step closer.

After bonding, the threshold current density of the laser remained unchanged from that recorded using an unbonded laser at $4.6\,kA/cm^2$. Both bonded and unbonded lasers operated in pulsed mode, using 100 ns pulses with a repetition rate of 5 kHz.

The collected optical power of the bonded laser was lower than the unbonded laser, which Andrijasevic puts down to reflection from the gold surface.

In future the group hopes to use the silicon to fabricate waveguides for the laser and better align the hybrid chip parts to address the reflection problem.

Journal reference
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GAAS TRANSISTORS

Native oxide increases cut-off frequency

A self-aligned InAlP thermal oxide can help leakage problems seen in GaAs MOSFETs with submicron-length gate electrodes, says a group from the University of Notre Dame.

Thanks to this, Patrick Fay and co-workers have made a GaAs-channel MOSFET with a measured cut-off frequency, f_t, of 31 GHz – an 11% improvement on their previous efforts. Also, the actual device manufacture is straightforward and suitable for mass production, says Fay. "The fabrication process results in the foot of the T-gate electrode, InAlP oxide formation and gate recess region being self-aligned with a single, common lithographic exposure," he explained.

Fay's team used electron-beam lithography to cut the "foot" pattern for the 0.25 µm gates on top of the MOCVD-grown GaAs MOSFET. The pattern was cut down into the MOSFET's top SiN_x layer using reactive ion etching and then into the GaAs layer with wet chemical etching. This exposed an InAlP layer that was then oxidized by wet thermal oxidation at 440 °C to a thickness of 5 nm. The SiN_x acted as a mask, limiting oxidation to the InAlP in the gate region.

"These devices have promise for wireless communication and phased-array radar," Fay said. "They could be utilized through the X-band and extended through the K_a band."

Journal reference
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