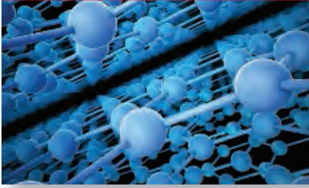
COMPOUND SEMICONDUCTOR

Connecting the Compound Semiconductor Community

Volume 21 Issue 3 2015 | @compoundsemi | www.compoundsemiconductor.net

Graphene unites GaAs with silicon

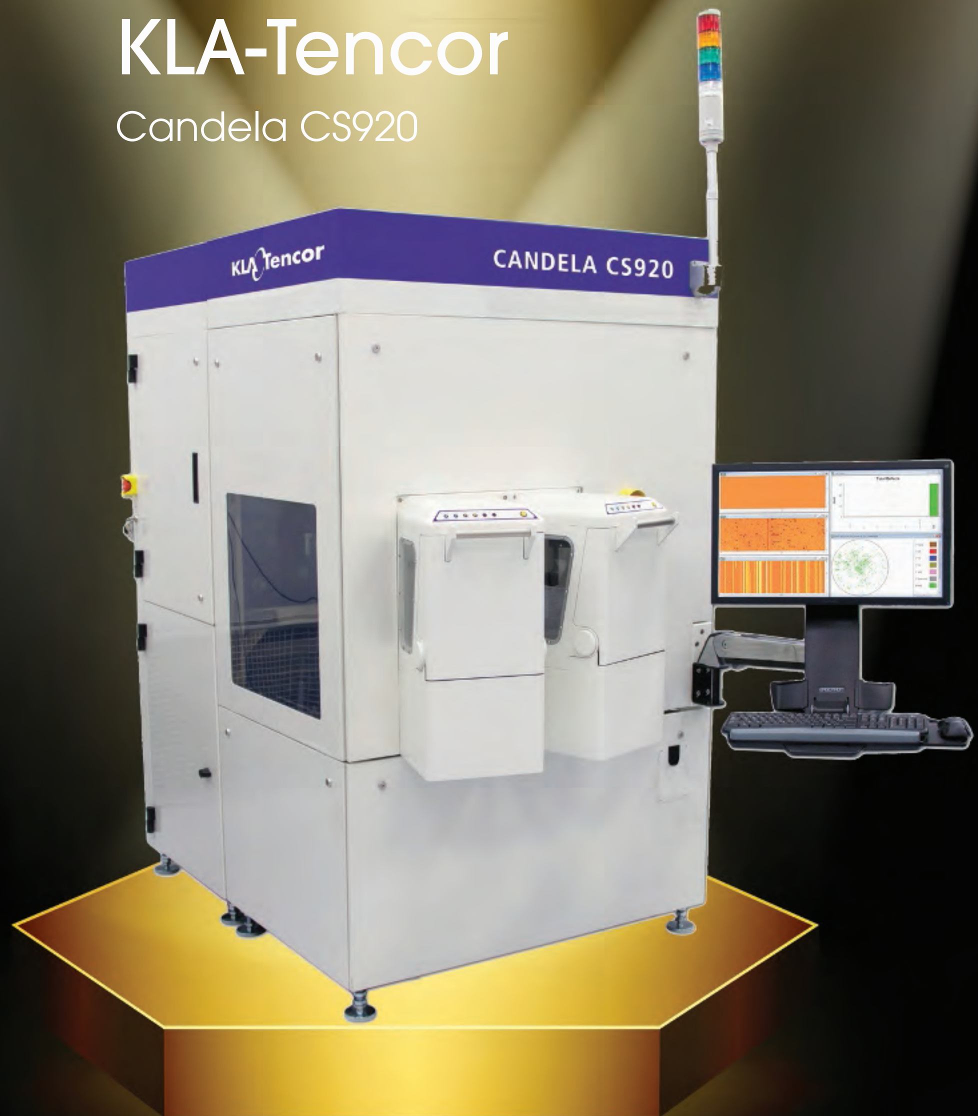


Opportunities for infrared LEDs

Amps target the terahertz domain

CMOS and GaAs wage an amp war

Optimism reigns for III-V chip sales



inside CS COMPOUND SEMICONDUCTOR

News Review, News Analysis, Features, Research Review and much more.

Free Weekly E News round up , go to www.compoundsemiconductor.net

AN ANGEL BUSINESS COMMUNICATIONS PUBLICATION

AIXTRON

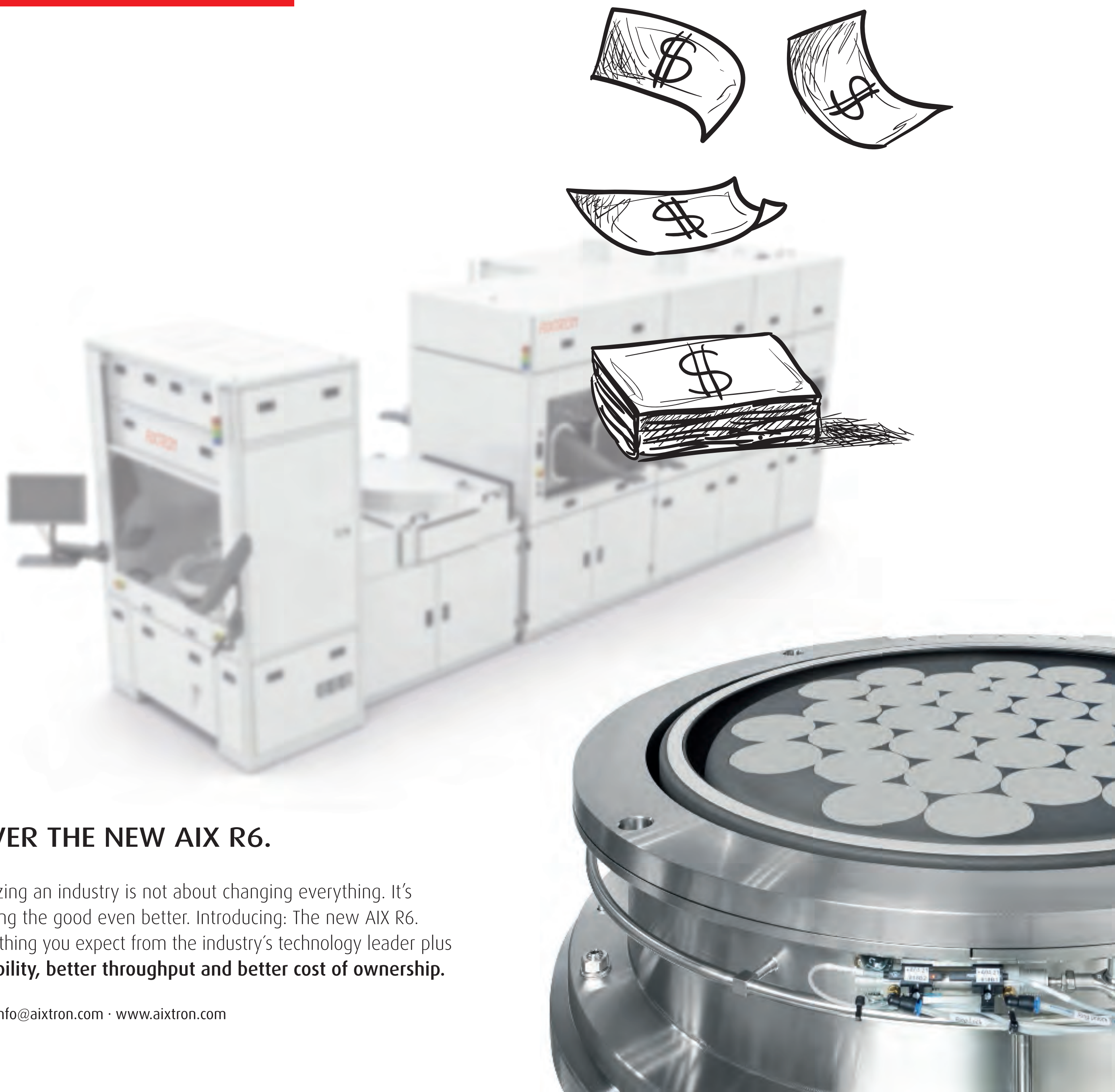
Our technology. Your future.

YOU THINK,

AIXTRON SYSTEMS SHOULD OFFER YOU THE BEST COST OF OWNERSHIP.

WE THINK THAT TOO.

THE NEW AIX R6.



DISCOVER THE NEW AIX R6.

Revolutionizing an industry is not about changing everything. It's about making the good even better. Introducing: The new AIX R6. It has everything you expect from the industry's technology leader plus **better usability, better throughput and better cost of ownership.**

AIXTRON SE · info@aixtron.com · www.aixtron.com

editorialview

by Dr Richard Stevenson, Editor

Power amps

WHAT DO YOU THINK of when you hear the phrase power amp?

Assuming that you are not an audiophile drooling over hi-fi components with eye-watering price tags, you probably think of a chip amplifying wireless signals in a handset.

In this issue, we cover that form of amplifier, reporting on a fascinating session at CS International where Jim Cable, head of UltraCMOS pioneer Peregrine, went head-to-head with representatives of two of the world's leading GaAs chipmakers, Skyworks and Qorvo (see p.32).

Both of these sides made a formidable case for their approach. Cable extolled the benefits of CMOS, a peerless technology when it comes to integration. However, the makers of GaAs power amplifiers fought back by championing the higher efficiencies this offers, and argued for the benefits of a front-end sporting the 'best tech for the spec'.

Although it's not clear which approach will be the long-term winner, III-Vs will reign for the next few years – and they will also be used to build other forms of amplifier.

Within the pages of this magazine you can also learn about efforts at Teledyne Scientific, which have enabled the fabrication of amplifiers operating at far higher frequencies. These can be used for superfast point-to-point data links, imaging systems that can expose hidden weapons, and advanced forms of radar.

Technologies often take time to develop, and that's certainly the case with Teledyne's amplifiers, which are constructed from InP HBTs. The amplifiers now operating in high-frequency

atmospheric windows, such as those found at 140 GHz and 220 GHz, are the fruit of efforts dating back a decade.

In terms of performance, highlights so far would include record-breaking peak output powers of up to hundreds of milliwatts at 220 GHz, using three-stage amplifiers that are constructed from several cells. Taking this approach requires tremendous transistor uniformity, which is possible because unlike the HEMT, junction characteristics for the HBT are defined by epitaxial design and growth.

Teledyne's program is on going. If, after reading their story, you'd like to catch-up with their very latest results, try to get along to the International Microwave Symposium in Phoenix, Arizona. If you do, hopefully when you hear an account of 200 GHz amplifiers operating at power levels not far short of one Watt, it will captivate the audience as much as those talks by Peregrine, Skyworks and Qorvo enthralled delegates at CS International.

Editor Richard Stevenson richardstevenson@angelbc.com +44 (0)1291 629640
Contributing Editor Rebecca Pool editorial@rebeccapool.com
News Editor Christine Evans-Pughe chrise-p@dircon.co.uk
Publisher Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Senior Sales Executive Robin Halder robin.halder@angelbc.com +44 (0)2476 718109
Sales Manager Shehzad Munshi shehzad.munshi@angelbc.com +44 (0)1923 690215
USA Representatives Tom Brun Brun Media tbrun@brunmedia.com +001 724 539-2404
Janice Jenkins jjenkins@brunmedia.com +001 724-929-3550
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214
Circulation Director Jan Smoothy jan.smoothy@angelbc.com +44 (0)1923 690200

Chief Operating Officer Stephen Whitehurst stephen.whitehurst@angelbc.com +44 (0)2476 718970
Directors Bill Dunlop Uprichard – CEO, Stephen Whitehurst – COO, Jan Smoothy – CFO, Jackie Cannon, Scott Adams, Sharon Cowley, Sukhi Bhadal, Jason Holloway.

Published by Angel Business Communications Ltd, Hannay House, 39 Clarendon Road, Watford, Herts WD17 1JA, UK. T: +44 (0)1923 690200 F: +44 (0)1923 690201 E: ask@angelbc.com

Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. T: +44 (0)2476 718 970 F: +44 (0)2476 718 971 E: info@angelbc.com

Compound Semiconductor is published eight times a year on a controlled circulation basis. Non-qualifying individuals can subscribe at: £105.00/€158 pa (UK & Europe), £138.00 pa (air mail), $198 pa (USA). Cover price £4.50. All information herein is believed to be correct at time of going to press. The publisher does not accept responsibility for any errors and omissions. The views expressed in this publication are not necessarily those of the publisher. Every effort has been made to obtain copyright permission for the material contained in this publication. Angel Business Communications Ltd will be happy to acknowledge any copyright oversights in a subsequent issue of the publication. Angel Business Communications Ltd © Copyright 2015. All rights reserved. Contents may not be reproduced in whole or part without the written consent of the publishers. The paper used within this magazine is produced by chain of custody certified manufacturers, guaranteeing sustainable sourcing.US mailing information: Compound Semiconductor, ISSN 1096-598X, is published 8 times a year, Jan/Feb, March, April/May, June, July, August/September, October, November/ December by Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Rd, Coventry CV5 6SP. UK. The 2015 US annual subscription price is $198. Airfreight and mailing in the USA by agent named Air Business Ltd, c/o Worldnet Shipping Inc., 156-15, 146th Avenue, 2nd Floor, Jamaica, NY 11434, USA. Periodicals postage paid at Jamaica NY 11431. US Postmaster: Send address changes to Compound Semiconductor, Air Business Ltd, c/o Worldnet Shipping Inc., 156-15, 146th Avenue, 2nd Floor, Jamaica, NY 11434, USA. Printed by: Pensord Press. ISSN 1096-598X (Print) ISSN 2042-7328 (Online) © Copyright 2015.

contents

CONNECTING THE COMPOUND SEMICONDUCTOR COMMUNITY
Volume 21 | Issue 3 2015

features

32 What future for the PA?

Will ease of integration spur eventual dominance of the CMOS power amplifier, or will GaAs continue to reign, thanks to superior performance?

36 Bright future awaits compound semiconductor industry

From integrated circuits to solar, UV curing and electronic systems in electric vehicles, deployment of compound semiconductor chips is going to rise throughout this decade

42 Graphene gets GaAs onto silicon

What's the trick to growing high-quality GaAs on silicon? It's inserting a layer of graphene between them

48 Power amplifiers: Getting to the G-band and beyond

Vertical electron transport and a well-defined junction make the InP HBT the best building block for powerful, high frequency amplifiers

55 Improving *p*-type nitrides

A novel form of MBE known as metal-modulated epitaxy could improve the performance of LEDs, transistors and solar cells, by delivering a breakthrough in *p*-type doping

60 Intense infrared LEDs

Perfected packages housing advanced emitters are yielding brighter, more efficient sources

 Copyright Compound Semiconductor

news

06 SiC and GaN power market to grow by factor of 17 during the next decade

08 Transistor Laser research gets $657k grant

09 EU HiPoSwitch project delivers GaN power switches

10 Osram to coordinate 'InteGreat' LED project

12 Sensorex evaluates Crystal IS UVC LEDs

13 Cree introduces highest performing LED module

14 POET appoints two new directors

16 JePPIX sees a multi-billion market in Integrated Photonics by 2020

news analysis

18 A dazzling future for diamond GaN?

20 Extreme testing

22 Riber homes in on US markets

24 Rare earths ready for GaN power electronics

research review

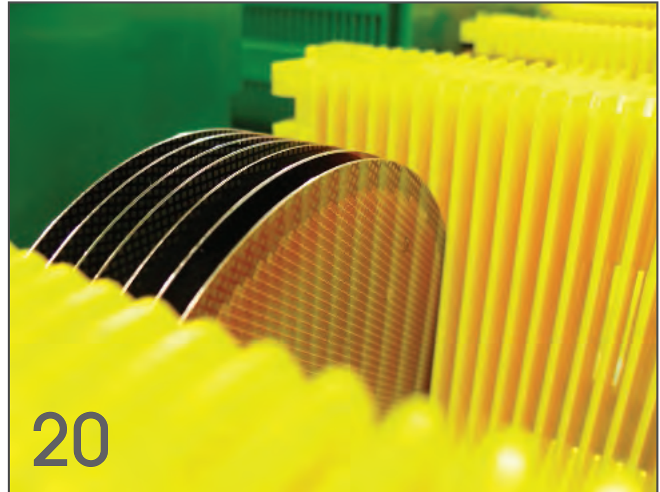
67 Photoelectrochemical etch improves nitride lasers

68 Debut for epitaxial InGaPBi

69 Probing buried interfaces in Schottky contacts

CS Industry Awards 2015

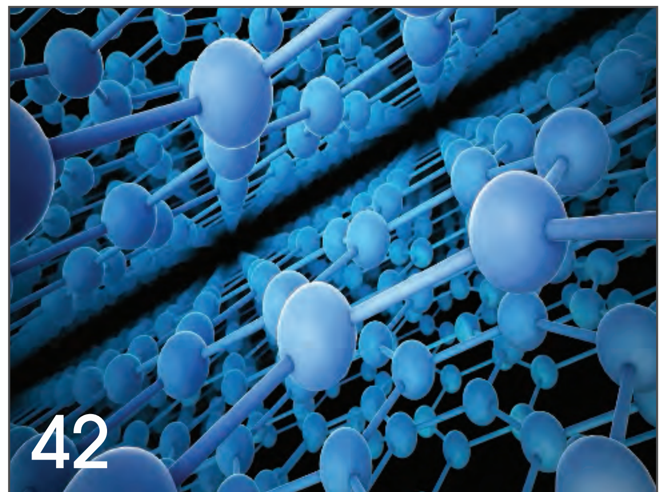
26 The winners are...



20

32

36



42

SiC and GaN power market to grow by factor of 17 during the next decade

THE EMERGING MARKET for SiC and GaN power semiconductors is forecast to grow by a factor of 17, during the next 10 years, energised by growing demand for power supplies, hybrid and electric vehicles, photovoltaic (PV) inverters and other established applications. Worldwide revenue from sales of SiC and GaN power semiconductors is projected to rise to $2.5 billion in 2023, up from just $150 million in 2013, according to 'The World Market for SiC & GaN Power Semiconductors - 2014 Edition' a new report from IHS Inc.

SiC and GaN power semiconductors have been establishing themselves in key applications, however, for a few years, approximately 15 percent of the eventual market could be made up of new applications using these device technologies that are still two or three years away from production, according to Richard Eden, Senior Analyst - Power Semiconductors, IHS Technology
In addition to the market the hybrid and electric vehicles themselves, it is now apparent that the electric vehicle charging infrastructure market - including battery charging stations for plug-in hybrid and battery-electric vehicles - is also a potentially interesting area for SiC and GaN power devices.

There is no agreed global standard for hybrid-electric vehicle (HEV) charging infrastructure, so there are various competing standards describing the various levels or modes for AC and DC charging. All of the assorted AC levels can be considered to be for electromechanical systems, which require few, if any, power semiconductors. The IHS report therefore only considers DC or 'fast charging' because these systems are AC-DC power supplies, converting power from the mains (typically three-phase) into very high currents of up to 125-400A at voltages up to 480 to 600 direct-current voltage (VDC), delivering a maximum power of 240kW.

Wireless power charges battery-powered appliances by transmitting power through the air instead of through power cables. Although proximity within a specified range is required, this technology is gaining in popularity in mobile phones, game controllers, laptop computers, tablets, electric vehicles, and other commodity products.

The adoption of SiC and GaN power semiconductors will be negligible in inductive charging solutions, which are designed to comply with the Wireless Power Consortium (WPC's) Qi or Power Matters Alliance (PMA) standards, because silicon metal-oxide-semiconductor field-effect transistors (MOSFETs) are adequate for the low frequencies involved. In contrast, the fast switching capabilities of SiC and GaN power semiconductors are ideal for magnetic-resonance power-transfer applications, which perform well at the higher frequencies of the Alliance for Wireless Power (A4WP) standard.
As numerous consumer-electronics applications use fairly low voltages, they will be more suitable for GaN devices. The only area of this application thought suitable for SiC power devices is wirelessly charging battery-powered electric vehicles, such as plug-in hybrid vehicles (PHEVs), etc.

Two more applications that could potentially use SiC power modules are wind turbines and traction. In both cases the biggest barriers to SiC power module adoption are their high cost; unproven reliability; and a lack of availability of high current-rated modules, in general, and of full SiC modules, in particular. Both applications typically require 1700V modules; a voltage at which few SiC transistors have already been developed. Trials are underway, but commercial production is not expected to start until 2016 or 2017.

For high-voltage SiC technologies, there are a host of new medical applications and other potential industrial applications. For low-voltage GaN devices, the new applications include many emerging technologies that will drive significant growth in the future, such as wireless envelope tracking, light detection and ranging (LIDAR), Class-B audio amplifiers, and medical devices . The key factor determining market growth will be how quickly SiC and GaN devices can achieve price parity with -- and equivalent performance of - silicon MOSFETs, insulated-gate bipolar transistors or rectifiers. Price and performance parity is forecast to occur in 2020, and the SiC and GaN power market is subsequently expected to experience tremendous growth through 2023.

220 GaN MOCVD reactors to be installed in 2015

DUE TO THE MAJOR aggressive expansion plans of some Chinese LED companies, IHS forecasts that 220 GaN reactors will be installed in 2015, according to the latest data in the IHS LED Intelligence Service.

It forecasts that the large number of MOCVD tool shipments will result in a 28 percent increase in the level of excess supply in the LED market. This new capacity expansion is slightly different from what happened several years ago, when large numbers of LED companies in China purchased government-subsidised tools, says Alice Tao, senior analyst. IHS forecasts that this year only large and publicly traded companies will purchase MOCVD phase epitaxy tools. The graph above shows the largest 20 MOCVD customers, by the end of 2014: eight of them were Chinese companies and three of those companies - Sanan, HC Semitek and Aucksun - have announced expansion plans for 2015.

Most of the new reactors purchased in 2015 will be new generation tools, providing double capacity per reactor. Sanan is projected to lead in 2-inch equivalent wafer capacity share, by the end of 2015; although, Epistar would still own the largest number of MOCVD tools. The largest three Chinese companies will achieve a combined market share of 27 percent in 2015.

 Copyright Compound Semiconductor

your
EPITAXIAL GROWTH
partner

GaN InGaN InAlN AlGaN GaSb InSb InP InGaP InAlGaN GaAs AlGaAs

Enabling advanced technologies

- World leading technology
- Complete materials range
- MOCVD, MBE, CVD
- Advanced semiconductor wafer products
- Advanced R&D capabilities
- Multiple, manufacturing sites (Europe, Asia, USA)

www.iqep.com

Transistor laser research gets $657k grant

MILTON FENG, a professor of Electrical and Computer Engineering at the University of Illinois, has recently received a $657,000 grant from the US Air Force Office of Scientific Research (AFOSR).

The aim is to enhance the modulation speed performance of the transistor laser (a novel 3-terminal device that he and ECE colleague Nick Holonyak Jr. invented in 2004) to terahertz speeds. The transistor laser offers the potential for much faster broadband communications, both for long-haul telecommunications networks and for short-haul connections between and within chips for photonic integrated circuits (PICs).

Feng's group has demonstrated a transistor laser with a fast (30 ps) recombination lifetime and modulated optical output with a 22 Gb/s error-free transmission. By incorporating multiple quantum wells and reflectors and even coupling them with quantum dot regions, Feng is optimistic about reducing the recombination lifetime to 5 ps.

An expert in high-frequency devices, Feng owns the world record for fastest (800 GHz) heterojunction bipolar transistors (HBTs). He aims to leverage this expertise with advanced processing techniques to produce this ultra-low-threshold, high-speed transistor laser.

Over the course of the three-year grant, Feng and his students are investigating ways to reduce the average recombination lifetime (light generation) and push the laser's modulation speed into the terahertz range.

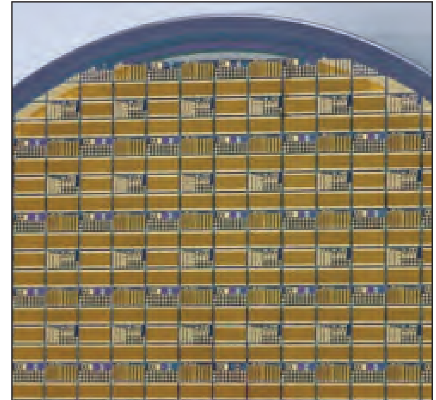
"In the first year, we'll establish the theoretical framework for pushing the modulation speed of the transistor laser into the terahertz and beyond," said Feng, who is also affiliated with MNTL. "In the second year, we'll pursue the epitaxial design for optimising the quantum wells necessary to reduce recombination lifetime below 10 ps. In our final year, we'll demonstrate a transistor laser made of quantum dots and quantum wells with a lifetime below 5 ps and modulation of 0.3 THz."

Feng and Holonyak have received more than 20 US patents covering the transistor laser for optical interconnects, photonic integrated circuit signal mixing, and feedback control of the laser and collector outputs.

Since 2013, Feng and his students have also produced record-setting research on 850nm oxide vertical cavity surface emitting lasers (VCSELs) with low relative intensity noise and 40 Gb/s error-free data transmission. Widely used by the datacom industry for short-distance (< 300 metre s) applications, VCSELs have limited modulated bandwidth below 30 GHz due to a relatively slow recombination lifetime of ~0.5 ns.

Based on the picosecond recombination lifetime of a THz transistor, the transistor laser modulates very quickly, making it a good candidate to compete with oxide VCSELs in a variety of optical interconnect applications.

EU HiPoSwitch project delivers GaN power switches



HIPOSWITCH, an EU group project, has successfully developed lightning-fast, high-efficiency enhancement mode GaN power switches. Eight European institutional and industrial project partners led by the Ferdinand-Braun-Institut, Leibniz-Institut fuer Hoechstfrequenztechnik (FBH) were involved.

"The single transistor measures only 4.5 x 2.5 mm and is optimised for switching 600 V. It has an on-resistance of 75 mΩ and handles a maximum of 120 A. We are the only ones in Europe who can manufacture these kinds of normally-off transistors at present," says Joachim Würfl, head of both the HiPoSwitch project and the GaN Electronics Business Area at FBH.

GaN has already been used in microwave transistors for a long while, while applied in thin layers mostly on SiC substrates. This technology has been further developed by FBH over the last few years for 600 V-rated power transistor switches.

"This works well, but it is too expensive for mass markets. As an alternative, the processes developed for SiC can be transferred to considerably more cost-effective, but technologically more challenging silicon substrates," Würfl explains.

FBH was so successful in optimising the processing of GaN switching transistors on SiC and silicon that nearly ideal components became feasible. Among others, comprehensive investigations of drift and degradation effects carried out by University of Padua and University of Vienna provided the foundation for this. The finished transistor chips were finally assembled into low-induction ThinPAK housings by Infineon in Malaysia. The Belgian company EpiGaN together with Aixtron moved the epitaxy to silicon - so that the manufacturing costs for the substrates drop by more than a factor of ten. At the same time, the wafer diameter increased to 6 inch or even 8 inch, a necessary step towards cost-effective industrial production.

Chip-manufacturer Infineon matched up the newly developed GaN technology with a silicon process line for industrial production of power semiconductors at their Austrian location in Villach. Part of the project possessed a decidedly "exploratory character", as Würfl puts it, due to the completely new techniques and processes for implementing GaN power transistors that had never before been tried. Promising ideas for producing semiconductors were successfully tested together with colleagues at the University of Vienna and the Academy of Sciences in Bratislava, Slovakia.

The Austrian company Artesyn is positioned at the end of the value-added chain as a systems – level partner. They developed a 3 kW rectifier for telecommunications applications including cellular base stations. This unit converts line voltage to DC with an efficiency of 98 percent.

A specialised switching topology was developed and implemented that is matched to the properties of the GaN switching transistors; their smaller size and weight also makes them highly attractive for aerospace applications.

One milllion Euros for US-Ireland GaN research project

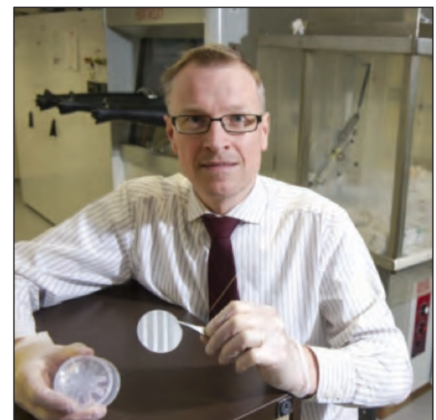
A RESEARCH PARTNERSHIP, called the Nano-GaN Power Electronic Devices project, involving institutes in Ireland, Northern Ireland and the US has secured €1 million in funding to develop new ways of harnessing converted electricity. The project will seek to improve the efficiency of converting electrical power by up to 25 percent.

The US-Ireland Collaborative Research on Nano-GaN Power Electronic Devices will be led by Peter Parbrook and Anne-Marie Kelleher in Tyndall; John Shen at the Illinois Institute of Technology; and Miryam Arredondo-Arechavala of Queens University Belfast.

"This will be the first time nanostructures using GaN will be used for power electronics," said Parbrook, Stokes Professor of Nitride Materials & Devices at Tyndall National Institute. "We will attempt to bend out the material's defects, making it more stable and hence more reliable in the conversion process. It has the potential to produce significant energy saving efficiencies that will benefit people in the home and at work."

Improving the efficiency of converting electrical power by up to 25 percent would represent a huge financial saving to the consumer and could substantially reduce global carbon emissions.

This issue is of immense importance to all the countries involved in this research, with Ireland in particular importing nearly 90 percent of its energy, leaving it very perceptible to changes in the international markets.



Osram coordinate 'InteGreat' LED project

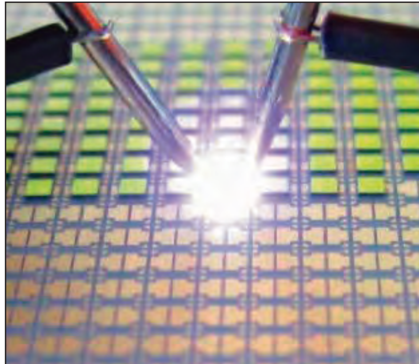
OSRAM OPTO SEMICONDUCTORS and five partners from industry and research are combining their know-how for a project called 'InteGreat' (Integrated High-Volume Production along the LED Value-Added Chain for Large Wafers and Panels) with the aim to fully optimise production for LED components and light modules.

Due to run until November 30, 2017, InteGreat is supported by the German Ministry for Education and Research as part of the Photonic Process Chains initiative.

The aim of the InteGreat project is to research new approaches to the production of high-efficiency LEDs along the entire production process, to remove the boundaries between the individual value-added stages and as a result to create new functionality and high flexibility.

A holistic view of the manufacturing process – from epitaxy (crystal growth) to the light source itself – should enable synergies to be exploited for maximum effect and new approaches and procedures to be developed that could give rise to completely new types of LED and cut their manufacturing costs.

"For the duration of the project we will be researching completely new concepts for LED production and allow ourselves to question the traditional paradigms of



the manufacturing process", explained Jürgen Moosburger, Project Coordinator at Osram Opto Semiconductors. Established technologies and processes from the classic microelectronics industry will be used and adapted to the specific requirements of LED production. Steps that up to now have been isolated will be networked, which will allow cost-intensive sorting and testing processes to be replaced by comprehensive routines. This could enable production of modern high-power LEDs to be a unified process for the first time. "With the new production concepts we want to be in a position to develop both low-cost miniaturised LEDs and highly integrated modules", added Moosburger.

To achieve the objective of this project, Osram Opto Semiconductors as the coordinator and the five other partners, namely Osram, Fraunhofer-Gesellschaft, LayTec, Würth Elektronik and Mühlbauer are working closely together. Osram Opto Semiconductors is bringing experience and know-how in LED technologies to the table, and is responsible for the integration and evaluation of the new processes. Osram GmbH as a specialist in lighting solutions will integrate the newly developed LED components into low-cost luminaires and is also supporting the project with its expertise in process technologies.

Mühlbauer, a technology partner for the Smart Card, ePässe, RFID and Solar Backend sectors, is contributing know-how in engineering to the high-precision processing of electrical components on flexible and fixed substrates including the development of new processes. Würth Elektronik is making its experience in individual solutions for pc board production available. Specifically, it will be researching the ways in which the LED chip can be connected to the pc board. The Berlin based instrumentation expert LayTec is analysing innovative process control systems for LED manufacture.

The Fraunhofer Institute for Reliability and Microintegration IZM and the Fraunhofer Institute for Integrated Systems and Device Technology IISB are researching the basic technological principles of process control and mounting technology. IZM will contribute its experience in connection technology, and IISB will work on the intelligent control of production processes.

Halogen ban postponed until 2018

THE EUROPEAN COMMISSION has voted to postpone the ban on energy-inefficient halogen bulbs until September 2018. This ban was originally planned for September 2016, as part of the wider strategy to promote more energy-efficient technologies, like compact fluorescent (CFL) and LED bulbs.

Fabian Hoelzenbein, IHS market analyst for Lighting and LEDs, writes in his latest research note that any delay of the planned 2016 date was going to be controversial. Traditional big lighting companies lobbied heavily for a delay, until 2020 or even 2022, to give them more time to adapt their businesses to fit the new guidelines, while newer, smaller companies with a focus on LED bulbs were – for obvious reasons – against an extension.

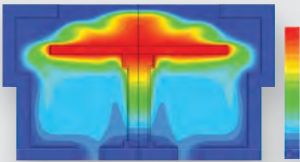
The European Commission voted for a compromise, because it came to the conclusion that September 2016 "would be too early for LED technology to fully replace halogen lamps" and it made sense to wait for "lower LED prices and a better LED performance" in 2018.

For the overall lighting market, says Hoelzenbein, the delay on the ban is a double-edged sword. Yes, it does give companies more time to adapt their business models and perfect their LED offerings; however, at the same time, it might force smaller, more innovative companies out of the market, because consumers are averse to change and smaller companies might not have the stamina to survive until 2018.

Most people did not switch to the available energy-efficient CFL and LED alternatives, when halogen's big brother, the incandescent light bulb, was progressively banned between 2009 and 2012; instead, they opted for halogen bulbs, which are only slightly more efficient than incandescent bulbs, but are inexpensive and boast a light quality and look that closely matches incandescent bulbs.

 Copyright Compound Semiconductor

Optimize the Thermal Performance of your Process Equipment.



Extensive computational tools enable product designs to be highly refined for ultimate performance.

Multi-zone circuit layouts in a polyimide construction are highly customized to deliver exacting performance up to 250°C.

EZ-ZONE® RM Multi-loop controllers are fully scalable with up to 152 PID Loops and 256 monitor points per system.

ASSURANT™ gas and pump line heaters feature high temperature capabilities with low outgassing.

Watlow provides innovative solutions to help process tool manufacturers meet the needs of the semiconductor technology roadmap. Our approach is to work collaboratively to help solve complex thermal challenges associated with state-of-the-art manufacturing processes; helping to improve yield, throughput and cost of ownership. This includes innovative heaters, controllers and sensors for use in front-end and back-end applications such as CVD, PECVD, Etch, Diffusion, Bonding, IC test and more.

Contact Watlow® today for the latest thermal solutions for semiconductor applications.

European Technical Sales Offices

Germany +49 (0) 7253-9400-0 info@watlow.de

France +33 1 41 32 79 70 info@watlow.fr

Italy +39 02 4588841 italyinfo@watlow.com

Spain +34 91 675 1292 info@watlow.es

UK +44 (0) 115-964-0777 info@watlow.co.uk

Sensorex evaluates Crystal IS UVC LEDs

SENSOREX, a manufacturer of sensors for water applications, has evaluated Crystal IS UVC LEDs as a light source replacement to mercury-based lamps. Testing confirmed that brighter, longer lifetime UVC LEDs were a significant contribution to a UVT monitoring instrument that is able to achieve full intensity instantly; optimises UV disinfection dosage guaranteeing that systems are not under- or over-dosing water and reveals cost savings greater than the one-time cost of purchasing the UVT monitor.

"With Crystal IS, Sensorex can manufacture state-of-the-art sensors for water monitoring" says Larry Felton, CEO of Crystal IS. "Their willingness to test and implement new light sources proves why they continue to be a market leader." The Crystal IS UVC LED allows manufacturers to fully exploit the power of UV-based technology to improve productivity, increase accuracy and create greater flexibility in product designs. Crystal IS UVC LED technology, made possible by the unique, low defect AlN substrate, delivers superior

light output, better spectral quality and best-in-class reliability and lifetimes, a game changer for environmental monitoring, life sciences and analytical instrumentation.

"The small footprint, long lifetime and low power consumption if Crystal IS deep UV LEDs is ideal for the UVT-LED product," said Dan Shaver, new business manager at Sensorex. "This makes for a versatile product with extremely stable readings in all conditions, over an extended lifetime."

8 benefits of sponsoring CS International 2016

- ✓ Senior management networking opportunities
- ✓ Increased company and brand awareness
- ✓ Access to the top strategists within the compound semiconductor industry
- ✓ Create, develop and support customer relationships
- ✓ Engage in debate, share insight and expertise on industry challenges
- ✓ Gain visibility and recognition as an industry leader
- ✓ Leverage exposure in multiple industry media
- ✓ Demonstrate market innovation and leadership by launching new services, products and systems

www.cs-international.net

CALL NOW: +44 (0)24 76718970
email **event@cs-international.net** or view the online sponsorship pack at **mediapack.cs-international.net**

CS INTERNATIONAL CONFERENCE
Connecting, informing and inspiring the compound semiconductor industry

GE and SUNY could process 30,000 wafers annually

IF General Electric Co. and SUNY Polytechnic Institute's New York Power Electronics Manufacturing Consortium takes off, their manufacturing line could process 30,000 wafers a year, GE's Danielle Merfeld told the Northeast Semi Supply Conference this week at SUNY Poly campus. Merfeld, who is leading GE's SiC program, said the facility would capture about 10 percent of the market for SiC power chips, which is about $150 million annually. Moreover, if needed, the consortium could double its capacity, she said. Any factory, however, would be built nearby to be close to the research done at GE Global Research in Niskayuna and at SUNY Poly.

GE and SUNY Poly announced the creation of the Albany consortium in July 2014 to commercialise GE's SiC technology for use in power electronics chips. The venture will invest over $500 million in the next five years. It is building a manufacturing line at SUNY Poly's Albany campus that is expected to be ready by 2017 and would serve a variety of industrial customers, including GE.

Cree introduces highest performing LED module

CREE has expanded its LMH2 LED module family with the introduction of the LMH2+, which it claims is the industry's highest performing LED module, delivering 30 percent better performance than the previous generation in the same form factor. It provides 125 lumens per watt with colour-quality greater than 90 CRI.

"Cree's dedication to LED innovation is evident in the LMH2+," said Wesley Johnson, sales director, Hi-Lite Mfg. Co. "This product is just what we are looking for to satisfy the higher efficacy requirements of our customers."

Featuring elements of Cree's SC5 Technology Platform, the efficacy of the LMH2+ drives new applications, enables smaller luminaires and lowers system cost, according to Cree. The LMH2+ allows lighting manufacturers to address more challenging installations such as those with space constraints or higher ambient temperatures.

"The LMH2+ is another breakthrough innovation from Cree that delivers more than just an incremental improvement," said Paul Thieken, Cree director of marketing, LED Components. "The LMH2+ enables lighting manufacturers to continue to lead the market in performance and light quality without incurring the time and expense of a major design change."

The LMH2+ is a drop-in upgrade for LMH2-based designs, providing an immediate boost in performance compared to the previous generation. Like all LMH2 modules, the LMH2+ delivers the same efficacy across all colour temperatures. According to Cree, lighting manufacturers can use existing ecosystems, tooling and optic design elements to accelerate time to market and lower design cost. In addition, UL rating will be available for maximum and nominal currents to provide more driver options and design flexibility.

The LMH2+ LED Module is available at 1250, 2000 and 3000 lumens and in colour temperatures of 2700 K, 3000 K, 3500 K and 4000 K at 90+ CRI. Designed for 50,000 hours of operation and dimmable to five percent, the LMH2+ is backed by Cree's five year warranty.

EPC introduces monolithic GaN half bridge

EPC has announced the EPC2104, 100 V enhancement-mode monolithic GaN transistor half bridge. By integrating two eGaN power FETs into a single device, interconnect inductances and the interstitial space needed on the PCB are eliminated, resulting in a 50 percent reduction in board area occupied by the transistors.

This increases both efficiency (especially at higher frequencies) and power density, while reducing assembly costs to the end user's power conversion system. The EPC2104 comes in a chip-scale package for improved switching speed and thermal performance, and is only 6.05 mm x 2.3 mm for increased power density. The EPC2104 is ideal for high frequency DC-DC conversion and motor drive applications.

A 2 inch x 2 inch development board (EPC9040) is also available containing one EPC2104 integrated half-bridge component using the Texas Instruments LM5113 gate driver, supply and bypass capacitors. The board has been laid out for optimal switching performance and there are various probe points to facilitate simple waveform measurement and efficiency calculation.

San'an acquires LED portfolio patent

SAN'AN OPTOELECTRONICS has licensed the US patents of an LED patent portfolio it recently acquired from a major Japanese company to its subsidiary, Luminus Devices, Inc. The portfolio comprises over 125 issued patents, including over 30 United States patents as well as issued patents in China, Japan, Korea, Taiwan, and Germany. The earliest patents in the portfolio have priority dates reaching back to the mid-1990s, and more recent patents are from the mid-2000s.

Patents in the portfolio are directed to a range of fundamental LED chip and wafer level technology, such as *p*-type branch electrodes (for example US Patent Nos. 6,881,985 and 6,384,430), transparent ZnO layers, and reflecting electrodes, barrier layers (US Patent No. 6,265,732), spacer layers, doped active layers (US Patent No. 6,081,540), optimised MQWs (US Patent No. 6,501,101), direct-bonded substrates, and GaInP current spreading layers.

According to San'an president Zhiqiang Lin: "We were quite pleased to acquire this well-respected LED patent portfolio as it complements the San'an patent portfolio nicely in time and subject matter and increases the San'an patent holdings to over 280 issued patents and published applications. San'an recognises the importance of a strong patent portfolio in the LED industry and we are committed to growing our patent base organically and by strategic acquisition."

The license of the United States patents to Luminus Devices is exclusive, subject to prior issued licenses, with the right to enforce. "The addition of the licensed patents to our existing patent portfolio further reinforces the position of Luminus Devices in the LED market," said Decai Sun, the chief executive officer of Luminus Devices.

POET Technologies appoint two new directors

POET TECHNOLOGIES - developer of the technology platform for monolithic fabrication of chips containing both electronic and optical elements - has announced the appointment of two new directors. One of these is to fill the vacancy left after Adam Chowaniec resigned due to illness leading to his death.

Peter Copetti, Executive Co-Chairman and Interim CEO, said: "Adam's loss left a very deep gap to fill, however, the Corporate Governance and Nominating Committee has been engaged in an extensive search to find suitable candidates to fill the role of permanent CEO and supporting executive staff and directors."

John O'Donnell, the Chairman of the CGNC, added: "The search has provided a short list of extremely capable and impressive candidates." Final decisions are not expected to be made until May with respect to the top executive roles, however the process has produced, to date, two very exceptional new directors with the semiconductor industry experience and relationships to help propel the company through its lab-to-fab transition.

Subject to regulatory approvals, the board has approved the following appointments: Todd A. DeBonis is a veteran semiconductor executive with over 27 years of expertise in sales, marketing and corporate development. For the last decade, Mr. DeBonis was the Vice President of Global Sales and Strategic Development at TriQuint Semiconductor. During his tenure TriQuint experienced dramatic growth and recognition in the industry as the technology leader in RF solutions.

DeBonis played an integral part in the recent merger with RFMD and subsequent creation of Qorvo, Inc. DeBonis previously held the position of Vice President, Worldwide Sales and Marketing at Centillium Communications.

DeBonis also served as the Vice President, Worldwide Sales for Ishoni Networks and Vice President, Sales & Marketing for the Communications Division of Infineon Technologies North America. DeBonis has a B.S. degree in Electrical Engineering from the University of Nevada.

David E. Lazovsky is the founder of Intermolecular and served as the company's President and CEO and as a member of the board of directors from September 2004 to October 2014.

Lazovsky has an in depth knowledge of the semiconductor industry, technology and markets. Lazovsky raised significant amounts of venture capital and other strategic private investments in Intermolecular's initial public offering.

Prior to founding Intermolecular, Lazovsky held several senior management positions at Applied Materials. From 1996 through August 2004, Lazovsky held management positions in the Metal Deposition and Thin Films Product Business Group where he was responsible for managing more than $1 billion in Applied Materials' semiconductor manufacturing equipment business.

From 2003 until 2004, Lazovsky managed key strategic accounts in Business Management where he worked closely with leading integrated circuit manufacturers to ensure Applied Materials was developing and providing cutting_edge technology solutions.

From 2002 until 2003, Lazovsky served as the Technology Program Manager for the Endura 2 Platform, Applied Materials' flagship 300mm metal deposition platform.

From 2000 until 2002, Lazovsky was based in Grenoble, France and served as Director of Business Management for the European region in the Metal Deposition Product Business Group. Previously, Lazovsky served as a Business Manager from 1997 to 2000, Account Product Manager from 1995 to 1997.

Qorvo's new GaAs process aims high

QORVO has announced a new GaAs pHEMT technology that it claims provides higher gain/bandwidth and lower power consumption than competing semiconductor processes.

Qorvo's TQPHT09 is a 90nm pHEMT process that supports Qorvo's next-generation optical product portfolio. This new process is said to be ideal for next-generation high frequency, high performance amplifiers required for 100G+ linear applications.

Manufactured in Qorvo's GaAs fabrication facility in Richardson, Texas, TQPHT09 is the newest offering in the company's well-established pHEMT process portfolio. Qorvo's TQPHT09 serves as the basis for several new optical modulator driver products including the TGA4960-SL, the company's most advanced quad-channel 100G modulator driver.

The TGA4960-SL is available in the CFP2 form factor for Metro and long haul applications, and is also well suited for upgrading the 100G linear dual-channel drivers for line card applications. It is optimised for high performance, low power dissipation and high channel-to-channel isolation, and is packaged in a 14.0 x 8.0 x 2.6mm SMT module, the smallest footprint in the industry.

James Klein, president of Qorvo's Infrastructure and Defence Products group, said, "Qorvo continues to invest and develop the most competitive semiconductor process technologies in the industry, enabling best-in-class components for next-generation products.

Qorvo's new 90 nm pHEMT process exemplifies our leadership in providing components for high-speed market applications with the quality, reliability and dependable source of supply our customers expect."

 Copyright Compound Semiconductor

III/V-Reclaim GaAs InP

The most cost effective method to excellent quality.

"Now offering Germanium Reclaim"

III/V-Reclaim
Wald 10
84568 Pleiskirchen / Germany
Telefon: +(49) 8728-911093
Telefax: +(49) 8728-911156
E-Mail: sales@35reclaim.com
Internet: www.35reclaim.com

- **We recycle your GaAs and InP wafer (all formats and sizes)**
- **One and double side polished wafer**
- **Best surface quality for direct use in Epitaxy**
- **Backside thinning of fully structured wafer**
- **Thin wafer (60 μm)**
- **Single wafer processing possible**
- **We buy used wafer and sell recycled wafer**

2015 IEEE Compound Semiconductor IC Symposium
October 11-14 at the Sheraton Hotel, New Orleans, Louisiana, USA

Late news submission deadline 10 July 2015.
See the Call for Papers for more details.

2015 IEEE CSICS Website

Plenary Speakers

Bruce Wallace (DARPA)
Zoya Popovic (Univ. of Colorado)
Ian Betty (Ciena)

Sunday Short Courses

Short Course I: *Transmit and Receive IC Design for Fiber Optic Links*, taught by industry experts The' Linh Nguyen (Finisair), Kumar Lakshmikumar (Ciena), and Mark Webster (Ciena), covers the basics of high speed IC design

Short Course II: *Microwave Package Design Fundamentals* taught by industry experts and covers the basics of microwave packaging for high speed and high power microwave applications.

Primer: *Introduction to Si RFIC Design* taught by Dr. W. Khalil (Ohio State University).

Register Now

Advanced Registration Deadline: 18 Sept 2015

TOPIC AREAS

- GaAs, InP, GaN, SiGe, and nanoscale CMOS technology
- Advanced Devices and modeling
- RF and Microwave ICs
- mm-Wave and THz ICs
- High-Speed Digital, Mixed-Signal & Optoelectronic ICs

FEATURES

- 3 day dual track conference
- 4 panel sessions on controversial topics of the day
- 2 day technology exhibition
- 2 Sunday short courses
- 1 Sunday primer course

For more information, contact the Symposium Chair:
Charles Campbell
Qorvo
Ph: +1 972 994 3644 E-mail: Charles.Campbell@qorvo.com

We bring quality to light.

LED test & measurement

Solutions from the world leader

Instrument Systems continues to set the benchmark in LED metrology. Whether testing individual LEDs (standard or high-power), LED modules, or OLEDs – the global LED industry relies on us to engineer superior measurement equipment for high-speed production testing applications.

Instrument Systems
light measurement

www.instrumentsystems.com

JePPIX sees a multi-billion market in integrated photonics by 2020

THE JOINT EUROPEAN PLATFORM for InP Photonic Integration of Components and Circuits' (JePPIX) latest roadmap predicts a 1 Billion Euro market for Photonic Integrated Circuit (PICs) enabled products in 2020.

So far, most PIC applications have been in the field of telecoms and datacoms, but they are becoming broader, says JePPIX. Examples are fibre sensor readout units, gas sensors, medical diagnostics, metrology, THz and antenna systems.

The business case for many companies targeting PICs in novel or improved products is also strong one, it says. It also sees a rapidly growing market for PIC designers.

JePPIX assists organisations around the globe to get access to advanced fabrication facilities for PICS. It aims at low-cost development of application specific PICs using generic foundry model, and rapid prototyping via industrial Multi-Project Wafer runs. Its closely collaborates with Europe's key players in the field of photonic integration, including manufacturing and packaging partners, photonic CAD software partners, R&D labs and photonic ICs design houses.

For foundries manufacturing generic PICs there will be an increasingly attractive business case as the market volume of PICs grows, JePPIX predicts. However, in the start-up phase, which may last a few years, foundry operation will ideally be combined with other chip based products and services.
In the coming years JePPIX foresees a further increase in the performance and the maturity of the four JePPIX foundry platforms (provided by Oclaro, Fraunhofer HHI, SMART Photonics and LioniX), to a level where the technology will be extremely competitive with application-specific processes.

The development of process capabilities and performance will be accompanied by the development of sophisticated, fab-calibrated, process design Kits which will provide the users with models and tools for accurate and efficient design of Photonic ICs. Standardised packages are also being developed within the JePPIX community. Access to a high performance package available at a reasonable cost is equally important for rapid prototyping and product development.

Through the application of the generic foundry model the entry costs for development of a PIC prototype are dramatically reduced, down to a level that is affordable for many SMEs and universities. It is shown that for developing prototypes, and also for low to medium volume manufacturing, InP PICs may be more cost effective than silicon photonics PICs, contrary to the widespread belief that InP technology is inherently much more expensive.

The first generic PIC based products will become commercially available this year (2015). Based on the rapid development of industry participation in MPW runs, JePPIX expects that the PIC enabled market will develop into a billion euro market before 2020.

The anticipated growth of the market will demand a rapidly growing number of PIC designs and hence designers. A more than tenfold increase of the present design capacity will be required within the next few years. Training and educational activities must, therefore, have high priority.

Very significant investments in photonic foundries have been announced recently in the US. For Europe to retain its competitive edge, continued public and private investment is important.

Funding should focus on raising awareness of the opportunities that Photonic ICs offer for novel or improved products for a wide range of applications, increasing training and education capacity and creating proper conditions for enabling PIC foundries to provide the required manufacturing services.

CSindustry awards2015

WINNERS ANNOUNCED

The CS Industry Awards recognise success and development along the entire value chain of the compound semiconductor industry from research to completed device, focusing on the people, processes and products that drive the industry forward. The CS Industry Awards remind us what is good about the industry - the people who drive it with their technical expertise and customer orientated perspectives.

The winners are:

SUBSTRATES & MATERIALS AWARD

Element Six
GaN-on-Diamond Wafers

DEVICE DESIGN & PACKAGING AWARD

Cree, Inc
C2M0025120D

R & D CHIP DEVELOPMENT AWARD

DARPA
Terahertz Electronics program

INNOVATION AWARD

Veeco Instruments Inc
TurboDisc EPIK700 GaN MOCVD System

METROLOGY, TEST & MEASUREMENT AWARD

KLA-Tencor Corporation
Candela CS920

Awards Sponsor

The winners were presented at the CS International Conference, Frankfurt, Germany, on March 11th 2015

For more information: www.csawards.net

A dazzling future for diamond GaN?

In March this year, Martin Kuball scooped a Royal Society award for his GaN-on-diamond electronics breakthroughs. Rebecca Pool talks to the UK researcher about his research, its applications, and more.

GAN-ON-DIAMOND electronics pioneer, Martin Kuball, hadn't intended to work with diamonds. On joining the University of Bristol, UK, nearly two decades ago, he had already spent several years studying GaN materials, including GaN-on-SiC devices, but diamond-related research was not on his agenda.

"The person that hired me was working in diamonds, and I said at the time, 'I will never do diamonds'," he says. "But now I am, which I think is probably the irony of life."

Today, the Professor of Physics heads up the Micro and Nanomaterials Group as well as the Centre for Device Thermography and Reliability at Bristol.

Research focuses on GaN microwave and power electronic devices grown on SiC, silicon and synthetic diamond substrates. Kuball and his twenty-strong team of researchers explore and develop the materials properties of the semiconductors, and apply novel thermal and electrical analysis techniques to build better devices.

And while, in Kuball's words, 'for me diamond research was accidental', the material is becoming increasingly important to the high power, high frequency GaN-based transistors that microwave designers crave.

Thanks to its high electron mobility and power density, GaN is now the technology-of-choice for RF electronics, from radar and satellite to communications and electronic warfare, and for power conversion systems. However, progress for even higher power devices is stalling as engineers struggle to design a device to adequately dissipate heat through its thermally resistant-silicon or SiC substrate.

So instead, researchers worldwide have turned to GaN-on-diamond. As Kuball puts it: "If you push GaN-on-SiC devices too hard, they heat up too much and fail early. So researchers decided to use the 'mundane' property of diamond – its high thermal conductivity – and incorporate this to these devices."

Come the early 2000s, US-based Group4Labs, recently acquired by Element Six, had bonded diamond to GaN, with pleasing results, and so process development started apace.

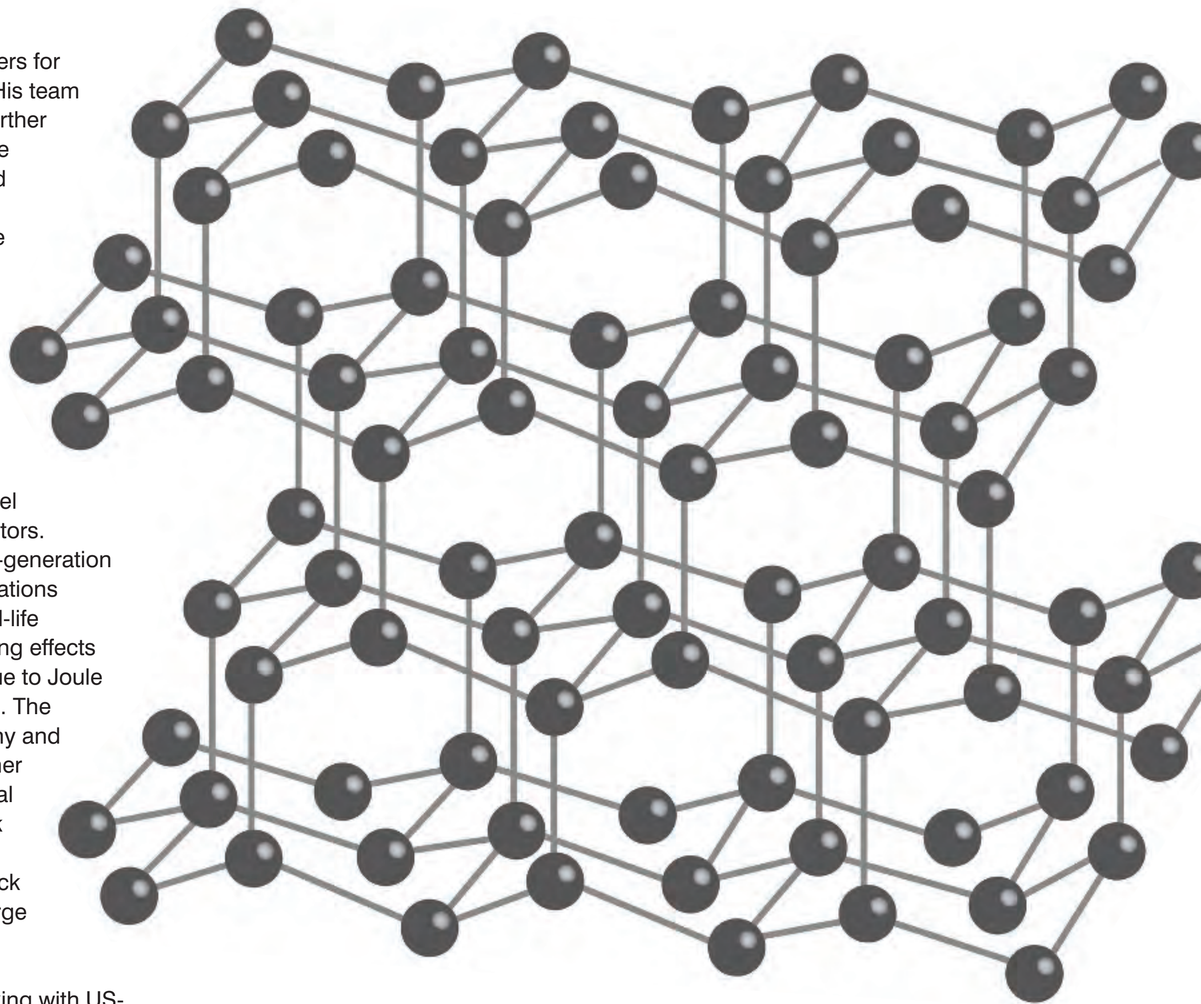
In today's processes, pioneered by Element Six and other organisations, a silicon substrate is removed from a GaN-on-silicon wafer, and replaced with a 100 m-thick layer of chemical vapour deposited diamond. Typically, with the host silicon layer removed from the AlGaN/GaN epitaxy, a thin dielectric material is first deposited onto the exposed surface, with CVD diamond then grown onto the dielectric surface.

And the results have been good. In 2013, TriQuint claimed a GaN-on-diamond breakthrough, demonstrating transistors with power densities some three times greater than the GaN-on-SiC equivalent. Meanwhile, Raytheon has developed transistors, also based on Element Six's GaN-on-diamond wafers, that show a three times improvement in RF areal power density and nearly a three times reduction in thermal resistance compared to GaN-on-SiC devices.

So, with the technology on the cusp of commercial success, research continues at speed. As Kuball simply states: "From a physics point of view, there's a lot of thermal transport in the dielectric and diamond layers."

"And of course, there's still a lot of engineering too," he adds. "For example, how do you modify diamond growth so the device works properly? I call this minimising the effects of the not-so-fortunate parts of the diamond microstructure and dielectric."

Right now, Kuball and colleagues are working with myriad companies and organisations, including, for example, Element Six and the US-based Naval Research Laboratory on how to seed,



and grow, the diamond layers for best device performance. His team is also exploring ways to further minimise thermal resistance between GaN and diamond layers, by, for example, altering the thickness of the dielectric layer.

Instrument success

GaN-on-diamond research aside, as early as 2005, Kuball was already developing techniques to probe channel temperature of GaN transistors. GaN-based HFETs for next-generation millimetre-wave communications lacked the reliability for real-life applications, and self-heating effects – temperature increases due to Joule heating – were a key issue. The then available thermography and spectroscopy methods either lacked the necessary spatial resolution to measure peak device temperatures or were simply too slow to track thermal changes across large surface areas.

With this in mind, and working with US-based Quantum Focus and Renishaw, UK, Kuball integrated an infrared camera into a Raman microscope to investigate micrometre-scale local heating in AlGaN/GaN HFETs, with astounding results.

Using the combined Raman spectroscopy-IR thermography system, the researchers produced infrared temperature maps of devices, alongside Raman temperature linescans, pinpointing hotspots, dislocations and other imperfections, to a resolution of better than 0.5 μm.

According to Kuball, while the instrument has proven crucial to research successes, he and colleagues are still building on the original system for future GaN-on-diamond device research. For example, reflectance measurement components have recently been added to the system, to further assess the thermal resistance of the interface between GaN and diamond layers on a wafer.

"This is for wafer-screening," says Kuball. "But we are also trying to improve the spatial resolution beyond its central half-micron spot."

Eventually, the researcher hopes to push instrument resolution to 200 nm, which would remove the need for thermal simulations for channel temperature determination during reliability testing. Critically, this would also allow researchers to directly study inhomogeneities within GaN layers, and design more reliable devices.

Only weeks ago, Kuball won the Royal Society Wolfson Research Merit Award for his development of GaN Diamond electronics and novel thermal management concepts. Research continues, and for him, better understanding and quantifying heat transport from GaN to diamond layers will be essential to the future of reliable devices.

As he says: "If you have this knowledge you can redesign diamond growth and the whole design of a structure to make the material even more workable."

But it's not all GaN-on-diamond. GaN-on-silicon and GaN-on-SiC research is also important, with for example, his team exploring the impact of carbon-doping in GaN-on-silicon high voltage devices. This includes gaining a detailed electrical understanding of how the devices work, including the role of charge trapping and transport within the buffer layer of the devices, as well as the physics of device failure.

Across the substrates, Kuball's team is working with a host of companies, from NXP and OnSemi to Qorvo and United Monolithic Semiconductors. And looking to the future, Kuball expects each technology platform to be of importance in its respective application. For example, he anticipates seeing GaN-on-silicon, in low-cost power electronics application for some time yet.

And as he adds: "GaN on silicon carbide works very well, we've had a hell of a lot of investment here, while for GaN-on-diamond we already have reasonably priced, good-sized wafers."

"These things always happen in parallel but working with companies is important," he says. "You get access to really good devices and you really get to understand what the challenges are."

Extreme testing

As more and more power semiconductors reach mass production, can test systems take the strain, asks Rebecca Pool.

EARLIER THIS YEAR, US-based test and measurement manufacturer, Reedholm Instruments, unveiled a DC test system to characterise power devices at the wafer level.

Based on a modern parametric tester, the instrument promises precise and fast device measurements that quickly weed out defective devices prior to packaging.

What's more it can handle voltages up to a hefty 10 kV, at a compliance current of 10 mA, and currents of 50 A. And high current can be reversed to make body diode measurements to 50 A without second pass measurements.

For Joe Reedholm, president of Reedholm Instruments, testing high power semiconductors is a 'continuum' of silicon device testing that demands the same parametric tester but with a difference.

As he highlights, these devices are used in extreme conditions and have to switch a great deal of power.

High voltage testing at the wafer level demands a properly designed safety system, with for example, interlock mechanisms between the prober and instrument, to protect the user from these voltages.

But to date, manufacturers of high power semiconductors have largely relied on commercial instruments, used to test silicon devices, reconfiguring these for GaN or SiC testing.

For example, several instruments are often combined to extend the range of a single instrument.

"It's really difficult when you are inventing something to specify your test system, so of course the engineer starts testing and adding pieces to a collection," says Reedholm. "So a lot of test systems wind up being put together like laboratory systems yet many engineers just don't have the experience to deal with [the challenges] of high power testing."

As he points out, devices can rupture while under test, generating a very large radiated energy field.

"This gets into the electronics of the test system, disrupting programming and instrumentation, a lot of which is now microprocessor based," he says. "It can also get through the wiring into the test probe, causing the prober to lose control and it's not necessarily easy to deal with that."

And as more and more GaN and SiC devices head for commercial production, safe and efficient testing is only going to get more and more critical.

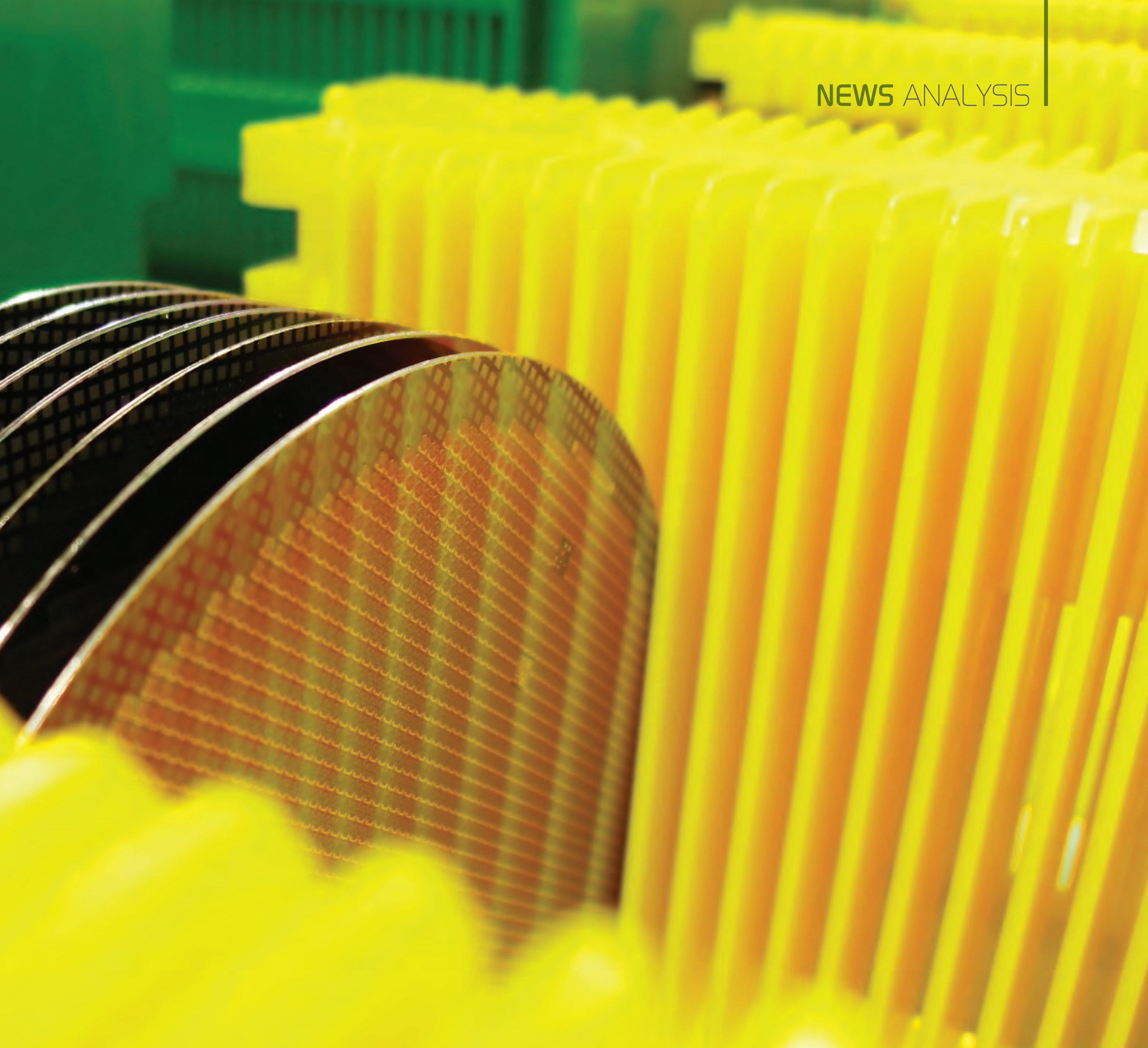
"[Engineers] end up with something that may be functional but can't be replicated easily or brought under control once you need high volumes of test data," points out Reedholm. "And we're now finding that they need high enough volumes of data to sample and prove to potential customers that they have a robust process that can deliver the product when its needed."

Ready for action

But are today's test instruments ready for high power semiconductors? Reedholm thinks so.

For starters, he highlights how his company's latest 10 kV/50 A DC power parametric analyser contains software to enable precise measurements at production speeds. "No compiling is needed... to perform complex

 Copyright Compound Semiconductor



calculations," he says. "Engineers don't have the time to amend tests as they go, so this system has a toolset to do that; you literally just fill in cells for testing."

Meanwhile, he is adamant the equipment is coping with rising market demands. As he points out, the rise of SiC and GaN semiconductors has been relatively slow, giving, for example, manufacturers of test interface equipment enough time to modify the latest test probes for high voltage and high current testing.

"Given the demand for, say, solar power inverters, it's inevitable there is going to be a need for these high power devices," says Reedholm. "But while we see the demand for SiC and GaN increasing, it hasn't exploded in the way it was forecast to."

And while the market really gets going, suppliers of parts for test equipment are developing innovative ways to handle higher currents and voltages.

As Reedholm highlights, Austria-based TIPS, for one, has developed probe cards for testing power semiconductors, at a wafer level, under a protective atmosphere.

Here, the wafer area under test is covered with a pressure chamber and flooded with gas to avoid high voltage flashovers. What's more probecards can now be used to protect probe tips and bond pads beneath and around contacts from thermal damage due to current overload.

But why not simply skip wafer-level testing and test the packaged device? Indeed, much development is also underway to test the many different packages of high power semiconductors.

Reedholm admits this is an option saying: "Wafer-level testing can be a science-based art... and you could just say I'm not going to worry about the wafer, package everything and then live with the waste of packaging defective devices."

But as he adds: "Wafer-level test instruments can eliminate defective devices and we have the high speed tests to do just that."

Riber homes in on US markets

As Riber outlines plans to buy MBE Control Solutions, Rebecca Pool asks president Frederick Goutard what the future holds for the MBE industry heavyweight.

FREDERICK GOUTARD, president of France-based MBE equipment supplier, Riber, has recently unveiled plans to buy MBE Control Solutions, US. The California-based developer of MBE research systems is also a prolific supplier of MBE-related components, electronics and control software, and as Goutard is quick to point out, makes a 'good match' for the France-based industry heavyweight.

"The US is a key area for MBE-related research and production and so far our presence has included sales and customer service activities but not manufacturing, repair or development," he explains. "MBE Control has a lot of customer support and product development expertise, and with this company we can reinforce our geographical presence by having operations on the East and now the West coast as well."

Setting up a California-based 'MBE Centre of Expertise' that will draw on the experience of both companies is central to Goutard's acquisition plans. And, as the president points out, this can only be achieved with everybody on board, starting with Andy Jackson, MBE Control Solutions founder and former University of California Santa Barbara researcher.

"By creating this centre, we want to harness the extensive expertise of Andy Jackson and his team," he says. "Riber has a very competent sales organisation and customer service structure in the US, and we will now reinforce this with Jackson's manufacturing infrastructure to provide customer support and repair, and to develop and improve products."

MBE Control Solutions' operations and employees will remain in California with Riber maintaining its presence on the East coast. But a complementary US presence aside, what exactly does the relatively new MBE business bring to one of the industry's most established players? Set up just over a decade ago, MBE Control Solutions generated $1.2 million in revenue in 2014 and employs five people. Crucially, the company has delivered a strong set of equipment and products including custom thin film deposition equipment, control software, electronics and instrumentation, as well as remote control monitoring and automation systems. And this will prove critical to Riber.

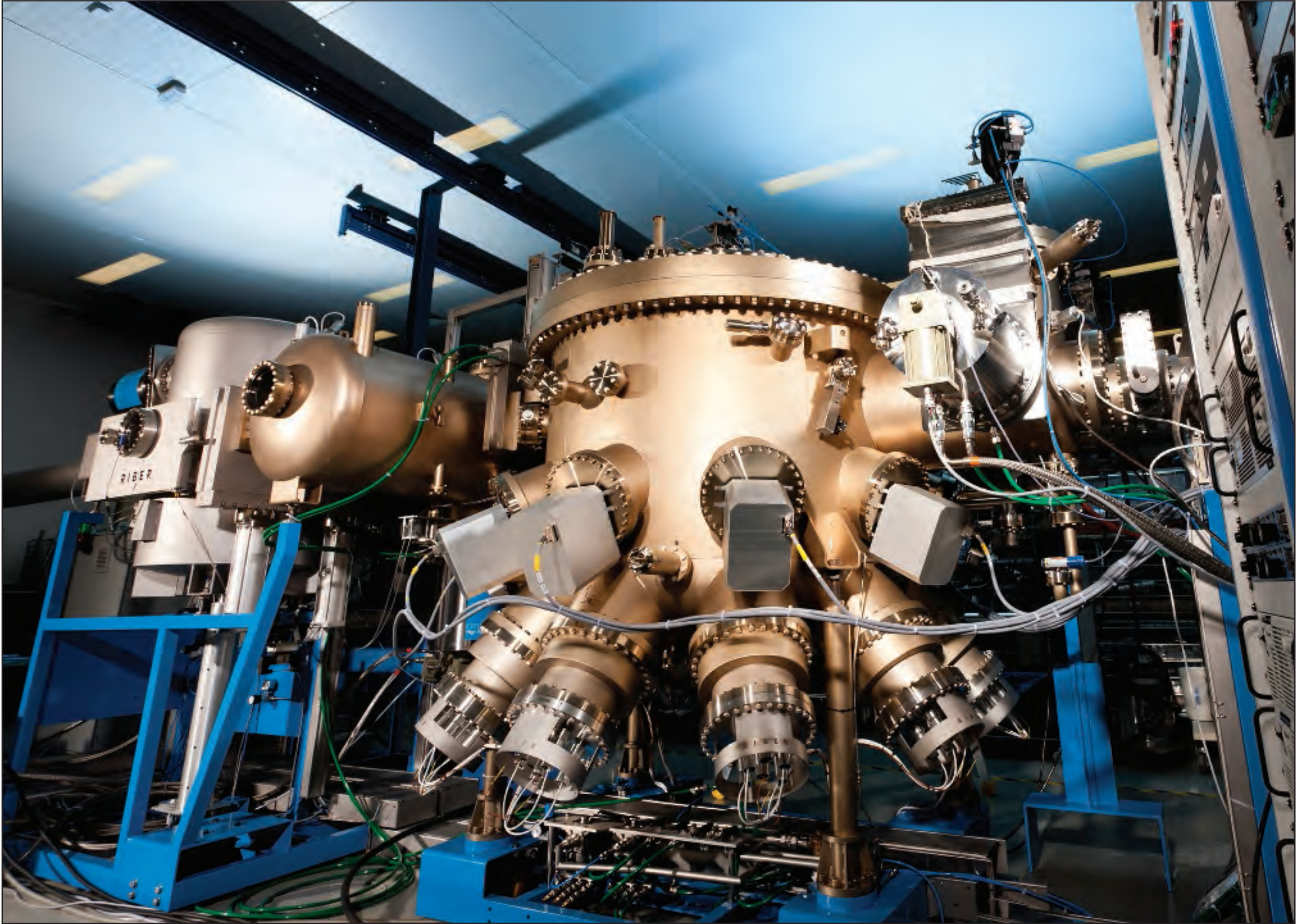
As well as providing MBE systems, Riber has a significant services, accessories and cells business segment that grew, bolstering revenues in its last financial year. According to Goutard, the company now intends to use these assets to strengthen its services and components business and raise revenue in North America.

Importantly, MBE Control Solutions has also set up extensive repair and refurbishment services, which Riber will exploit. "Jackson and his team bring an ability to operate complex refurbishment operations so customers can upgrade older MBE tools," says Goutard. "We now have the supply chain to provide a very thorough and competitive refurbishing service for customers in the US, and this is very important."

Clearly, acquiring MBE Control Solutions will strengthen Riber's position against Veeco, the only other significant MBE equipment supplier in the marketplace. However, Goutard refrains from commenting on his company's new-found US market strength.

"Our focus remains on what we believe the MBE user wants, and this is to bring expertise to their MBE problems, no matter what the brand of their system," he asserts. "With a Centre

 Copyright Compound Semiconductor



of Excellence with Andy Jackson in the middle we can create very strong communication streams with MBE users to resolve issues that affect the daily use of their MBE tools."

"Our vision for the industry goes beyond branding," he adds.

Looking to the future, Goutard now expects to see a rise in MBE research systems sales in 2015 as economic growth stimulates research and development in the semiconductor industry. His company recently clinched deals with Asia, Europe and Japan-based laboratories and the president anticipates more growth from Europe, China and India.

"Europe, for example, has a development programme as part of its Horizon 2020 programme and of course, macroeconomic growth has historically driven research," he says. But Goutard is also hopeful that industry development will fuel market growth.

As he points out, the mobile industry, with its thirst for faster RF components for wireless communications and cell phones, is still a driver for equipment makers even though MBE is experiencing pressure from new technological competition in this field.

However, optoelectronics devices, including lasers and detectors, now demand tools for III-V and II-VI materials epitaxy, and of course, MBE equipment can handle such complex materials deposition. Likewise, the slow but steady integration of III-V materials on silicon could also bring opportunities for manufacturers of MBE equipment.

"These opportunities are more remote but they exist and we can't help but think that a breakthrough in III-V-on-silicon would be important for MBE in a production environment," concludes Goutard.

"Europe, for example, has a development programme as part of its Horizon 2020 programme and of course, macroeconomic growth has historically driven research"

Rare earths

ready for GaN power electronics

As power electronics players turn to GaN-on-silicon epiwafers to manufacture high performance devices, Translucent has unveiled a stress-free alternative. Rebecca Pool reports.

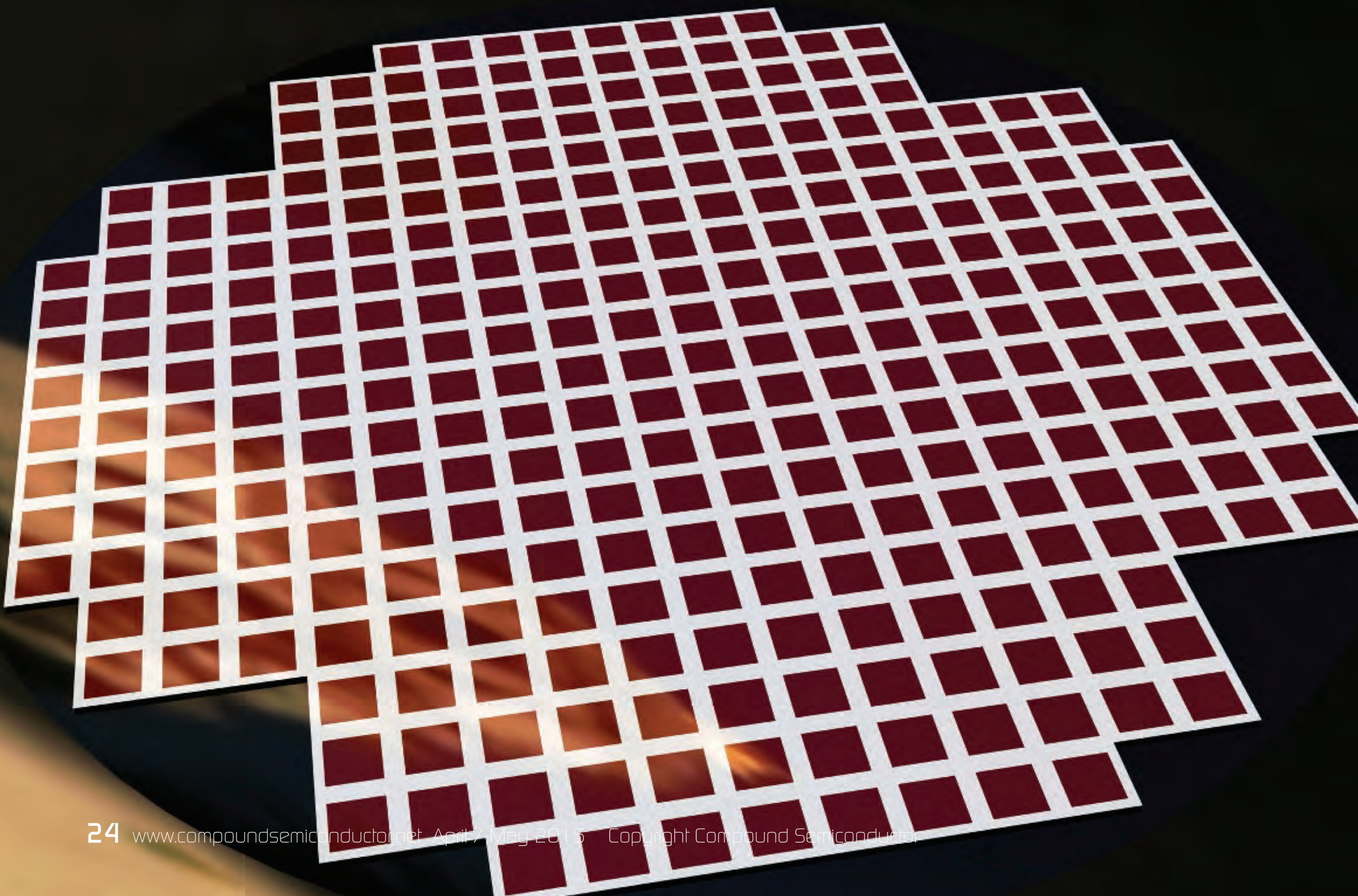
EARLIER THIS YEAR, up and coming developer of templates for III-V and III-N epitaxy, Translucent, unveiled 300 mm silicon templates with a rare earth oxide buffer layer.

Unique in the growing world of GaN-on-silicon, the US-based company hopes manufacturers of power devices, keen to embrace the technology without the stress of lattice mismatches, will adopt the template.

"GaN-on-silicon has matured and many companies now consider it to be an established technology, but we looked at it and asked, is the current method the best that can be used?" says Andrew Clark, vice president of engineering at Translucent.

"We've been working with rare earth oxides for many years now, and realised that a new buffer material between the GaN and silicon would help," he adds.

As Clark explains, the insulating buffer layer of crystalline rare earth oxide (REO) – typically erbium oxide – is lattice matched



 Copyright Compound Semiconductor

with the silicon on its lower surface. As a result, the upper surface can be engineered so defect growth during GaN epitaxy is more akin to GaN-on-sapphire than GaN-on-silicon, reducing wafer curvature and bowing. This also spells good news for manufacturers looking for an easy transition from GaN-on-sapphire to GaN-on-silicon.

The REO layer is also an insulator, and as such, will increase a transistor's breakdown voltage while blocking the interactions between the silicon substrate and III-nitride layers that kill device performance.

Consequently, Clark reckons the buffer layer could trim GaN thicknesses by at least 25 percent and even remove the need for the AlN interlayers commonly used to minimise silicon-GaN interactions. And of course, this reduces III-V materials and epitaxy process costs while offsetting the additional cost of the rare earth oxide layer.

"When you use an AlN buffer... you also have to clean the MOCVD chamber and platen inbetween runs," highlights Clark. "But we will supply the rare earth oxide on silicon as the starting wafer, so we're reducing the cycle times for MOCVD processes."

"Rare earth materials are now relatively cheap materials to buy, and having done cost analyses at volume, [a manufacturer] is going to save dollars on cycle times," he adds.

But benefits aside, will device manufacturers bite? After all, Translucent is introducing what is fundamentally a new GaN-on-silicon epitaxy concept. Clark remains confident.

For starters, the technology comes relatively free of the GaN-on-silicon IP infringement issues that plague industry newcomers.

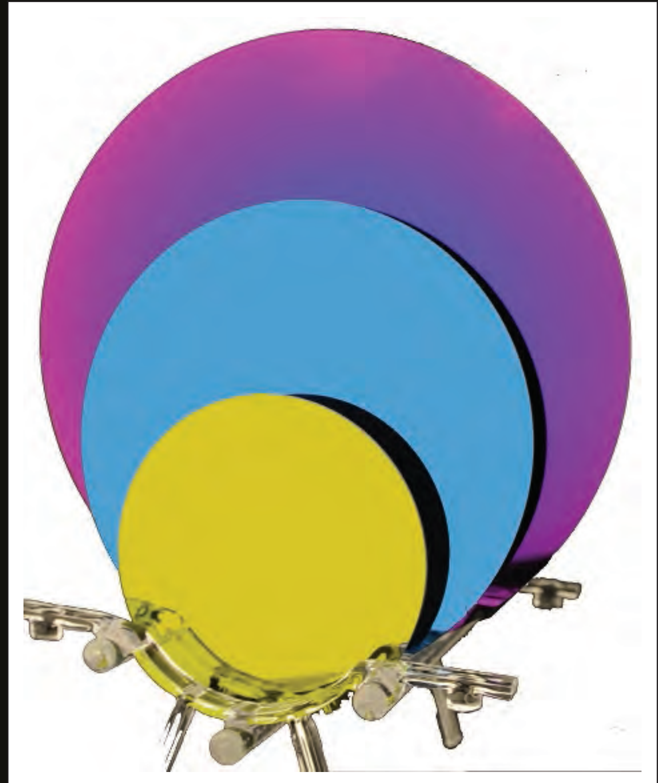
"This is clean IP," says Clark. "If you are a new company looking to get into GaN-on-silicon, do you take a risk and copy [existing fabrication methods] or do you invest in new IP and build your product on this?"

Importantly, the company has also worked with development partners to produce a solid process. Strong materials data has been well received by a number of companies and European consortia working on GaN-on-silicon, especially those focusing on 200 mm wafers.

"The infrastructure for [GaN-on-silicon] technology is established and many in the industry believe the next two years will be a critical phase in which the market should grow and stabilise," he says.

"Importantly for us, these companies are now returning to development cycles and looking to improve performances with a better process," he adds.

What's more, demonstrating that their REO buffer layer can stretch to 300 mm without succumbing to the dreaded wafer bow bodes well for manufacturers looking to fabricate the devices of the future.



With the key driver behind the move from native wafers to silicon substrates being to use depreciated 200 mm CMOS fabs and slash manufacturing costs, Clark and colleagues realised that they had to develop templates of this size from word go. But as the vice president of engineering points out, times have changed.

"This was a good place to start... but people are already saying that 200 mm CMOS fabs are pretty full from other processes," he says. "We've demonstrated we can move from 100 mm to 150 mm to 200 mm and have now processed 300 mm [templates] to prove that when GaN-on-silicon moves to these sizes, we can go with it."

"Increasingly we are also seeing a willingness to modify these CMOS fabs for GaN-on-silicon processes," he adds. "This is encouraging as it indicates that GaN-on-silicon is an accepted technology...and is no longer totally driven by working in a depreciated fab."

So where next for Translucent? For now, the company will concentrate on selling its templates to power device manufacturers; as Clark puts it: "LEDs is a hard market to break with a new technology."

Given this, the vice president of engineering would now like the technology to be adopted by a larger manufacturer of power electronics devices that could provide feedback, on for example, specific materials specifications.

"This is an interesting point of evolution for us and we're seeing a lot of traction," he says. "This technical input in conjunction with new investment would really help us to scale-up and grow."

CS industry awards 2015

WINNER

KLA Tencor

Metrology, Test and Measurement Award

Candela CS920

Right: Richard Stevenson, Editor Compound semiconductor, presents Brian Crawford, Sales Director

WITH GROWING performance requirements in compound semiconductor-based power devices, device manufacturers are looking for improved ways to cost-effectively achieve faster development and product ramp. Comprehensive characterization of yield-limiting defects is a key component in helping power device manufacturers drive higher product yields, while lowering device costs.

Full-surface, high sensitivity defect inspection and accurate process feedback has enabled the industry to improve SiC substrate quality as well as optimize the epitaxial growth yields on both SiC epi and GaN-on-silicon processes. As device makers continue to push the boundaries of process designs, the requirements for defect inspection and overall yield management become increasingly more stringent and critical. The Candela CS920 offers the latest inspection technology for power device manufacturing. The Candela CS920 enables high sensitivity inspection and defect classification at production throughputs for a wide range of critical defects (e.g. microscratches, stacking faults, basal plane dislocations) and effectively separates front-surface defects and buried defects on transparent substrates and epitaxial material. In addition the Candela CS920's automated defect classification capabilities reduce the time required to identify, source and correct various yield-limiting defects such as carrots, triangles, sub-micron pits and others.

SiC and GaN "wide bandgap" power device manufacturers require advanced inspection technologies that help cost-effectively ramp production. With advantages over traditional silicon-based power devices for high-voltage applications, and improving wafer defectivity and cost, SiC epi technologies are becoming the driving growth material in the power device segment.

A key challenge for inspection of SiC substrate/SiC epi is that they are typically transparent to visible light. The Candela CS920's design solves this challenge by leveraging SiC absorption in the ultra-violet (UV) regime – providing excellent sensitivity to micro-scratches/micro-pits and enabling photoluminescence contrast on otherwise invisible epi layer defects.

The Candela CS920 technology provides a comprehensive solution – integrating simultaneous, industry-proven Candela OSA (Optical Surface Analyzer) technology (reflectometry, optical, profilometry, scatterometry and phase-shift interferometry) with a newly-developed photoluminescence measurement channel. Using the multiple channels the Candela CS920 captures not only the yield-critical surface defects and buried defects but also the yield-impacting crystal defects which are invisible using visible-light illumination. The novel innovation around the Candela CS920 is the integration of surface defect detection and photoluminescence (PL) defect detection capabilities into one unified platform. Recently many groups have started using infrared (IR PL) 700nm- 1000nm technologies to detect PL defects utilizing full wafer scans. There are, however, some cases where the detection and screening of these defects becomes challenging. This happens when the defects propagate in the buffer layer to just below or just into the active layer. This is because there is a lack of IR PL signal from the typically high doped buffer layers. The Candela CS920 operates one of the two PL detection channels in the UV regime. This enables the detection of defects by naturally luminescing and revealing the absence of PL, thus giving a negative contrast as compared to the IR PL spectra. Hence, any defects that can cause radiative and non-radiative recombination will show up using this PL imaging technology.

By integrating, for the first time, surface defect detection and photoluminescence technology into a unified platform, the Candela CS920 enables high sensitivity inspection and defect classification for a wide range of critical defects at production throughputs.

Richard Stevenson, editor of Compound Semiconductor comments:
"The Candela CS920 has taken the surface inspection of SiC to a new level. Engineers using this tool now have a better idea of the range of defect types that need to be addressed."

 Copyright Compound Semiconductor

WINNER

Veeco

Innovation Award

TurboDisc EPIK700 GaN MOCVD System

VEECOS TurboDisc EPIK700 MOCVD GaN System combines the industry's highest productivity and best-in-class yields with low cost of operation further enabling lower manufacturing costs for LEDs for general lighting applications. Available in one-and two-reactor configurations EPIK700 features breakthrough technologies to drive higher yields in a tighter bin. EPIK700 offers a 2.5 times throughput advantage over other systems due to its large reactor size. Designed for mass production EPIK700 accommodates 31x4 inches 12x6 inches and 6x8 inches wafer carrier sizes.

Customers can easily transfer processes from existing TurboDisc systems to the new EPIK700 MOCVD platform for quick-start production of high quality LEDs. Because of the flexible EPIK700 MOCVD platform more upgrades added benefits and future enhancements will continue to differentiate this world-class system. LED manufacturers are under pressure to lower manufacturing costs while adding MOCVD system capacity to meet growing consumer demand. Therefore they need high productivity high yield and reliable MOCVD systems.

By combining the advanced TurboDisc reactor design with proven automation, low consumable costs and improved footprint efficiency, the EPIK700 can significantly improve the cost per wafer for customers. Based on Veeco's proven TurboDisc technology the EPIK700 MOCVD system enables customers to achieve a cost per wafer savings of up to 20 percent compared to previous generations through improved wafer uniformity reduced operating expenses and increased productivity.

The EPIK700 system features a reactor with more than twice the capacity of current generation reactors. This increased volume combined with productivity advancements within the reactor results in a 2.5 times throughput advantage over previous generation MOCVD systems. Veeco is the first company to introduce a reactor size that is significantly larger than the previous industry standard.

The large reactor size coupled with technological advancements enable our customers to obtain the highest throughput and the lowest cost of ownership - key metrics in accelerating adoption of solid-state lighting. EPIK700 features breakthrough technologies including the new IsoFlange center injection flow and TruHeat wafer coil that provide homogeneous laminar flow and uniform temperature profile across the entire wafer carrier.

These technological innovations produce wavelength uniformity to drive higher yields in a tighter bin. EPIK700 offers a 2.5 times throughput advantage over other systems due to its large reactor size.

Veeco has a long history of introducing game-changing systems that enable adoption of LED lighting. The EPIK700, the first of its kind with a 700mm reactor, combines best-in-class yields and highest productivity to lower LED manufacturing costs. Designed for mass production, EPIK700 can accommodate twelve 6-inch substrates or six 8-inch substrates.

Richard Stevenson, editor of Compound Semiconductor comments: "Making LEDs with good margins is tough in the current environment. Increasing yield and productivity holds the key, making the latest multi-wafer tool from Veeco an attractive option."

This category was sponsored by UMS

Right: Dr. Ulf Meiners, Managing Director UMS GmbH presents to Sudhakar Raman, VP and Country GM

CSindustry awards2015

WINNER

Substrates & Materials Award

Element Six - GaN-on-Diamond Wafers

AS DEVICES BECOME smaller size and require higher reliability in the presence of extreme power densities, new solutions are needed. Nowhere is this more evident than with the transition to wide-bandgap GaN transistors, where engineers have struggled with the thermal barriers limiting the ability to achieving the intrinsic performance potential of GaN semiconductor devices.

Element Six, the world leader in synthetic diamond supermaterials and member of The De Beers Group of Companies, has developed GaN-on-diamond semiconductor wafer technology— the first-of-its-kind to be developed and commercially available. In the approach, the GaN epitaxy is transferred to diamond by first removing the host silicon and transition layers beneath the AlGaN/GaN epitaxy, depositing a 35 nm dielectric onto the exposed AlGaN/GaN, and finally growing a 100 micron thick CVD diamond onto the dielectric adhered to the epitaxial AlGaN/GaN. The resulting 100 mm GaN-on-diamond composite wafer offers a cost-effective and efficient thermal management solution for GaN radio frequency (RF) semiconductor devices, enabling the intrinsic power performance capability of GaN devices.

Currently, Silicon Carbide (SiC) is the most commonly used semiconductor substrate for RF GaN devices. However, the diamond in GaN-on-diamond wafers has a thermal conductivity of 1600 W/mK, which is four times that of SiC. Rigorous test results by Raytheon Company revealed it achieved a three times improvement in GaN-on-diamond's RF areal power density, compared to GaN-on-SiC devices. The GaN-on-diamond devices also demonstrated more than 40 percent reduction in thermal resistance. Additional beta customers include Air Force Research Lab (ARFL) and Qorvo, which was a recipient of the 2013 CS Industry Award for its GaN-on-diamond achievements through DARPA's NJTT program.

Transistor engineers have struggled for years to surpass the thermal barriers that stand in the way of achieving the intrinsic performance potential of GaN semiconductor devices. Element Six's chemical vapor disposition (CVD) diamond thermal management solution holds the potential to enable the next generation of high power RF and high voltage devices.

GaN-on-diamond substrates bring diamond within less than a micron of the gate-junctions where all the heat is generated, and does so with a minimal thermal barrier resistance between the GaN epi and diamond. This enables more than a three times increase in areal power density, compared to GaN-on-SiC, to enable more power in a military radar system, for instance. GaN-on-diamond's ability to operate at ambient temperatures more than 40 percent higher than GaN/SiC devices results in costs savings from smaller cooling subsystems and less energy use.

Critical to Element Six's GaN-on-diamond technology is the diamond synthesis that leverages its proprietary microwave CVD process. The diamond synthesis recipe must optimize the diamond's thermal conductivity while not damaging the GaN epi. In addition, the interface layer between diamond and GaN buffer must minimise thermal barrier resistance while handling CTE mismatches and preventing leakage. And finally, wafer bow and thickness variation must be minimized. Through its microwave CVD synthesis, Element Six is able to tightly control growth conditions to meet all of these challenges.

Richard Stevenson, editor of Compound Semiconductor comments:
"It's great to see that the upper limit for GaN transistor performance is extending, thanks to the introduction of a high-quality diamond layer."

Left: Henk de Wit, General Manager

WINNER

Device Design and Packaging Award

C2M0025120D

CREE has shattered the on-resistance barrier of traditional 1200V MOSFET technology by introducing the industry's first commercially available SiC 1200V MOSFET with an $R_{DS}(ON)$ of 25mΩ in an industry standard TO-247-3 package. The new MOSFET designated the C2M0025120D is expected to be widely adopted in PV inverters high voltage DC/DC converters induction heating systems EV charging systems and medical CT applications.

Based on Cree's proven C2M SiC MOSFET technology the new device has a pulsed current rating ($I_{DS\ Pulse}$) of 250 A and a positive temperature coefficient providing engineers with greater design flexibility to explore new design concepts. The high pulsed current rating ($I_{DS\ Pulse}$) rating makes the device suitable for pulsed power applications and the positive temperature coefficient allows the devices to be paralleled to achieve even higher power levels.

The higher switching frequency of the new C2M0025120D SiC MOSFET enables power electronics design engineers to reduce the size weight cost and complexity of power systems. For medical applications such as CT systems Cree's C2M MOSFETs provide a 5 times reduction in switching losses and enable much higher power density.

Combined with the lower switching losses the added benefit of low $R_{DS}(ON)$ greatly improves the thermal characteristics and can potentially even eliminate system fans resulting in quieter and more cost effective medical imaging systems.

Cree has also demonstrated that by implementing the C2M0025120D in a PV string-inverter it is possible to develop a highly efficient and compact 50kW grid-tied solar inverter with a power to weight ratio of 1kW/kg. This results in a string inverter that is significantly more efficient and half the weight and size of the state-of-the-art commercial 50kW systems available today. Additionally for rooftop PV inverters the smaller size and lighter weight greatly reduce the installation costs.

Cree's C2M0025120D provides greater design flexibility in PV inverters high voltage DC/DC converters induction heating systems EV charging systems and medical CT applications enables the reductions of the size weight cost and complexity of these power systems and due to the combination of lower switching losses and a low 25mΩ $R_{DS}(ON)$ greatly improves the thermal characteristics and can potentially even eliminate system fans resulting in quieter and more cost effective systems.

Cree's C2M0025120D SiC MOSFET has an ($I_{DS\ Pulse}$) of 250A and a positive temperature coefficient which allows the devices to be paralleled to achieve even higher power levels. The higher switching frequency (and up to 5 times lower switching losses of the device enables power electronics engineers to reduce the size weight cost and complexity of power systems. Combined with the lower switching losses the added benefit of the low 25mΩ $R_{DS}(ON)$ greatly improves the thermal characteristics and can potentially even eliminate system fans resulting in quieter and more cost effective systems.

Richard Stevenson, editor of Compound Semiconductor comments:
"Cree is the pioneer of the SiC MOSFET, and this latest device should help to drive a revolution in power electronics"

Right: Dieter Liesbeths, European Sales Director

CSindustry awards 2015

WINNER

R&D Chip Development Award

Terahertz Electronics program

ACCOMPLISHMENTS in Terahertz Electronics program could pave way for new areas of research and unforeseen applications in the sub-millimetre wave spectrum.

Last year officials from Guinness World Records recognised DARPA's Terahertz Electronics program for creating the fastest solid-state amplifier integrated circuit ever measured.

The ten-stage common-source amplifier operates at a speed of one terahertz – 150 billion cycles per second faster than the existing world record of 850 gigahertz set in 2012.

Terahertz circuits promise to open up new areas of research and unforeseen applications in the sub-millimetre-wave spectrum, in addition to bringing unprecedented performance to circuits operating at more conventional frequencies. This breakthrough could lead to revolutionary technologies such as high-resolution security imaging systems, improved collision-avoidance radar, communications networks with many times the capacity of current systems, and spectrometers that could detect potentially dangerous chemicals and explosives with much greater sensitivity.

Developed by Northrop Grumman Corporation, the Terahertz Monolithic Integrated Circuit (TMIC) exhibits power gains several orders of magnitude beyond the current state of the art. Gain, which is measured logarithmically in decibels, similar to how earthquake intensity is measured on the Richter scale, describes the ability of an amplifier to increase the power of a signal from the input to the output. The Northrop Grumman TMIC showed a measured gain of nine decibels at 1.0 terahertz and 10 decibels at 1.03 terahertz. By contrast, current smartphone technology operates at one to two gigahertz and wireless networks at 5.7 gigahertz.

This level of gain moves the technology from the laboratory bench to practical applications – nine decibels of gain is unheard of at terahertz frequencies and will open up new possibilities for building terahertz radio circuits.

For years, researchers have been looking to exploit the tremendously high-frequency band beginning above 300 gigahertz where the wavelengths are less than one millimetre. The terahertz level has proven to be somewhat elusive though due to a lack of effective means to generate, detect, process and radiate the necessary high-frequency signals. Current electronics using solid-state technologies have largely been unable to access the sub-millimetre band of the electromagnetic spectrum due to insufficient transistor performance.

To address the "terahertz gap," engineers have traditionally used frequency conversion – converting alternating current at one frequency to alternating current at another frequency – to multiply circuit operating frequencies up from millimetre-wave frequencies. This approach, however, restricts the output power of electrical devices and adversely affects signal-to-noise ratio. Frequency conversion also increases device size, weight and power supply requirements. DARPA has made a series of strategic investments in terahertz electronics through its HiFIVE, SWIFT and TFAST programs. Each program built on the successes of the previous one, providing the foundational research necessary for frequencies to reach the terahertz threshold.

Richard Stevenson, editor of Compound Semiconductor comments: "The record-breaking results are impressive, but that will only be part of the success story - these developments will also deliver improvements in chip performance at lower frequencies."

Right: Dr. Daniel Green, Program Manager, Microsystems Technology Officer

 Copyright Compound Semiconductor

United Monolithic Semiconductors (UMS)

UNITED MONOLITHIC SEMICONDUCTORS (UMS) is the European leader in offering RF MMIC products and foundry services for specialised markets, including defence and space, telecommunications, automotive radar and industrial sensors. With major locations in both France and Germany and a network of sales offices and representatives supporting a global customer base, the Company has revenues of exceeding €70 million, of which more than 80 percent are to export markets and has a key position as a strategic supplier to the European Defence and Space industries.

UMS' has a comprehensive offer based on the supply of either ASIC or catalogue products, in the main based on the Company's internal III-V technologies and through the provision of a comprehensive foundry service, allowing customers to directly create their own product solutions.

The full range of catalogue products from DC to 100GHz is based on GaAs, GaN, SiGe technologies and encompasses power amplifiers up to 200 W, mixed signal functions, very low noise amplifiers, and complete transceiver systems. These products are offered in die form but are more commonly packaged and in multichip module form. In-house GaAs and GaN processes provide the technology platform to allow the design of leading edge products and form the basis of foundry service offer to external design centres. These technologies and their associated Process Design Kits (PDK) are very robust, extensively proven and kept up to date through their use in internal products. They enable customers to achieve first-pass success for the majority of their designs. Strong partnerships are in place with Keysight Technology and AWR to provide the latest tool needed to address their design challenges.

Comprehensive training in the use of the technologies is also provided along with close support throughout the whole design cycle, from the selection of the most appropriate technology through to the final delivery. UMS also provides a range of back end services to foundry partners including on wafer testing, die sorting, visual inspection, packaging and the delivery of known good dies or packages.

Continuous and customer led innovation is at the heart of UMS' continuing success. UMS has strong relationships with many of the major R/D centres and Universities throughout Europe, actively participating in many advanced and collaborative developments to create the technologies and products needed for future markets.

Recent innovations include multi-chip transceiver modules, using a combination of SiGe and GaAs technologies for the latest 24 GHz automotive radar sensors which give customers extended functionality at a significantly lower cost, and also GaN based high power devices including general purpose transistors in SMD DFN packages and internally matched power quasi MMIC amplifiers from L to C band in ceramic and QFN packages.

Power applications are the main drivers for in-house technology development. A 0.25 μm GaN HEMT high power technology has been recently qualified and released and has seen extensive use both internally to create new products up to 20 GHz and also by foundry partners with excellent results.

The current GaN technology range will be extended in the future to higher frequencies with the development of a 0.15 μm technology. There continues to be power applications where GaAs technology remains the optimum choice and to address these, UMS is releasing a high breakdown voltage GaAs *p*HEMT (PPH15X-20) process for linear power applications up to Ka band with the capability to be packaged in a standard QFN.

UMS has a reputation for and a long heritage of supplying high quality products to the most demanding markets and is certified ISO 9001, ISO 14001 and ISO TS16949. The majority of the UMS III-V internal technologies are approved for space use and form part of the ESA EPPL list.

What future for the PA?

Will ease of integration spur eventual dominance of the CMOS power amplifier, or will GaAs continue to reign, thanks to superior performance?

RICHARD STEVENSON INVESTIGATES

IF YOU HAD HAPPENED to be following the stock market on Thursday 21 February 2013, you would have witnessed a bad day for the compound semiconductor industry. Shares in two of the world's leading makers of GaAs microelectronics, Skyworks and RFMD, plummeted by more than 10 percent, and valuations of global epiwafer supplier IQE, Taiwanese GaAs foundry WIN Semiconductors and III-V substrate maker AXT also took a knock.

What was the reason for this? Was it breaking news of a supply shortage for gallium? Or a report of an impending decline in smartphone sales? No, neither were the cause – instead, a shot had been fired across the bows of the III-V industry by a leading maker of silicon chips for handsets, Qualcomm. On that day, during Mobile World Congress 2013, this company launched the RF 360, a single chip claimed to provide all of the functionality required for the front-ends of leading smartphones.

In hindsight it is clear that the stock market over-reacted. Qualcomm's release didn't deliver an instant death to the GaAs power amplifier. Instead, in recent times GaAs chipmakers have actually had considerable success, with share prices of the biggest players trading much higher than they were after the hit they took two year's ago. Shares in Skyworks are now hovering at around $100, about five times that on black Thursday, and the valuation of RFMD has also climbed – although it's not possible to know how much of that rise has been driven by positive expectations relating to the merger with TriQuint.

While this indicates that GaAs is in a healthy state, with sales on the up, it would be careless to ignore the threat faced by the silicon PA. And it maybe that it is not Qualcomm, but Peregrine, a pioneer of silicon-on-insulator technology, that is going to be the toughest opponent.

Speaking to a packed hall, president and CEO of Peregrine, Jim Cable, outlined the virtues of a CMOS front-end during the opening session of CS International, held in Frankfurt on 12 and 13 March, 2015. As one might expect, Cable didn't have it all his own way, however, with Skyworks' Ed Anthony, Vice President, Engineering, delivering a compelling case for the inclusion of GaAs in handsets sporting a variety of technologies. Qorvo – the company that formed this January from the TriQuint-RFMD merger – supported this view, with Sean Riley, Vice President, Strategic Marketing, revealing how fast the value of GaAs and filter content will rise in the coming years. Meanwhile Eric Higham, market analyst at Strategy Analytics, argued that although GaAs will continue to dominate amplification in cell phones, silicon CMOS will steadily increase its presence there.

Cable is convinced that Peregrine's technology will play a major role in handsets, arguing: "CMOS wins in every market. It's because of integration." He is not singling out GaAs when expressing this view, and points out that integration is the reason for CMOS success against PMOS, NMOS and bipolar technologies.

CMOS does not guarantee success, however. Cable believes that if a CMOS PA that to match the performance provided by GaAs, it will not win significant sales, because handset makers are not prepared to compromise performance. Products by Peregrine are claimed to meet that demanding benchmark of a CMOS product delivering GaAs performance.

Founded in 1990, Peregrine has focused on what it describes as "intelligent integration". What this means is to use one technology – silicon-on-insulator (SOI) CMOS – to produce highly capable, flexible single die that trim the overall footprint. Cable admits that the development costs for these chips can "skyrocket", but the flipside is that the production costs for the components are very low.

To illustrate the potential of CMOS within the front-end of handsets, Cable described the evolution of the company's switch products. Initially, these switches made with an UltraCMOS technology lagged those built with GaAs in the key figure of merit, the product of on-resistance and off-capacitance. But in 2011, UltraCMOS caught up, and has

since overtaken by a meaningful margin, leading to a hike in sales. Shipments have more than doubled between 2011 and 2013.

At Mobile World Congress 2015, held in early March, Peregrine launched the UltraCMOS Global 1 Initiative. This is claimed to integrate the PE56500 all-CMOS front-end solution, unveiled 12 months earlier, with filter's made by Murata, which recently acquired Peregrine. The Global 1 includes a three-path multi-mode, multi-band PA, post PA switching and an antennae switch and tuner. "Any band can do any frequency, all controlled by tuning on the chip," explains Cable.

The head of Peregine drove home the benefit of the CMOS PA by comparing the Ultra CMOS Global 1 PE56500 with an equivalent GaAs-based product made by Skyworks. "The differences are pretty clear", remarked Cable, pointing out that while his company's single-package product just had two flip-chip ICs, 17 surface-mount technology passives and no wire bonds, the two-package rival had 9 ICs, 43 surface-mount technology passives and 136 wirebonds. Reduced component count is claimed to lead to far shorter design times, with the design-time-per-band plummeting from 2-4 days to less than an hour.

Upper hand for GaAs?

Whether CMOS PAs can actually deliver the same performance as those based on GaAs was questioned by Anthony, who offered a mixture of simulated results and measured performance.

By both metrics, GaAs PAs are quite a way ahead. Highlighting results presented at the 2014 RF-SOI Workshop, simulated and measured power-added efficiency (PAE) for the GaAs HBT was 71 percent and 66 percent, respectively, while for the SOI equivalent, the simulated figure was 60 percent, and performance, measured by Peregrine, 57 percent.

HBT efficiency continues to improve, with the PAE for Skyworks 2015 products hitting 78 percent. "This resets the bar on what is possible," argued Anthony, who added that GaAs also holds the upper hand over CMOS in terms of linearity, size of footprint and cost.

Skyworks philosophy is to combine the GaAs HBT with other components that are built from the best technology for the part, because this is argued to lead to a system-in-a-package that is outstanding in terms of cost, performance and time to market. The company has various in-house technologies, including SOI capability, having shipped more than 6.5 million devices – it views this as the

The surge is wireless traffic is helping to drive up revenues for GaAs microelectronics towards $7 billion, with just over half that figure associated with power amplifier sales.

best option for making an RF switch. Anthony explained that SOI offered the best bang-per-buck, with MEMS technology providing a far lower insertion loss, but being far too pricey to be considered today.

The dollar content for this switch, plus that for filters and PAs, was given in the talk by Riley, who compared a typical 2G and a 3G phone with those offering regional and global LTE capability. These figures, given in the table below, show that the advancing sophistication of phones is good news for makers of PAs – and even better news for those that make filters.

Everyone a winner?

Implications of the emergence of the silicon PA, and the evolution in wireless networks, were discussed by Higham, who offered his take on the GaAs RF market. He argued that the backdrop to what is happening in this industry is the rapid rise in mobile data consumption, which is increasing at a staggering compound annual growth rate of 78 percent, according to data from Cisco.

Driving the explosion in mobile data consumption is the rising sales in cellular terminals. Shipments of tablets and E-readers are outpacing handsets, although the latter will continue to occupy the lion's share of cellular terminal sales for the foreseeable future. Sales of handsets within the handset market will continue to rise, but increasingly slowly. "Smartphones are starting to saturate – some areas can't support the technology," argued Higham.

The analyst went on to underline the importance of cellular revenue to the GaAs microelectronics industry: in 2013, it was worth 53 percent of the market, which totalled just under $6.6 billion. And in the wireless era, defined as 2004 and beyond, revenue has climbed by an average of 11 percent per year. An initial estimate for total revenue for 2014 is $ 6.6 billion, but this could be revised upwards. "It could be $7 billion," admitted Higham.

This makes the current market for the PA, which needs to sport multi-band, multi-mode capability, worth $ 3.5 billion. The majority of this will continue to go to GaAs for the foreseeable future, but silicon PAs will have an impact, increasing in market share from just a few percent in 2013 to 20 percent in 2018.

The view that the CMOS PA will not have substantial success overnight is shared by Cable. "Adoption will take time, but numbers will be much higher than 20 percent," claims the Peregrine CEO.

It is not just this threat from silicon that could squeeze margins of those in the GaAs RF business. The move to multi-band, multi-mode PAs makes the GaAs offering more competitive, but the size of the chip is much smaller than a family of single-band PAs, leading to changes in epitaxial volumes and revenue. With the exception of 2009, recent growth in revenue has outpaced production, implying that the revenue per square inch of epitaxial material is falling, making it tough for makers of substrates and epiwafers.

The one issue that wasn't discussed in detail by any of those speakers is the emergence of 5G. This might be good for GaAs – and it might even be good for GaN. To hear the arguments for and against, get along to next year's CS International, where it may well be one of the biggest talking points of the conference.

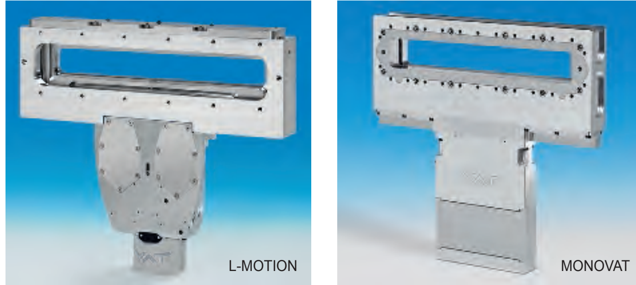
	Typical 2G	Typical 3G	Regional LTE	Global LTE
Filter Content	$0.25	$1.25	$4.00	$7.25
Switching / Tuning	$0.00	$0.25	$1.50	$2.25
Power Amplifiers	$0.30	$1.25	$2.00	$3.25
Other	$0.00	$0.00	$0.50	$0.50
Total RF content	$0.55	$2.75	$8.00	$13.25 +

Handsets capable of operating at higher data transfer rates have a higher bill of materials for front-end components. Source: Qorvo.

High-end valves for MOCVD

www.vatvalve.com

Transfer valves and gates with L-MOTION and MONOVAT technology



- Withstand full atmospheric differential pressure and contaminating processes
- Designed for high cycle life and high temperature applications
- Emergency door locking and pressure control
- Sizes up to 100 × 800 mm (4" × 32")

Butterfly control valves

- High pressures with low flows
- Wide range of interfaces, sizes and heated and non-heated versions
- Withstand full atmospheric differential pressure and contaminating processes

New CS APP ready for Download NOW!

Continuing our aim of 'connecting the compound semiconductor industry', Compound Semiconductor has a Free app for Android, iPhone and iPad to allow you keep up to date wherever you are.

Available **FREE** from the App Store or Google Play, the app allows you to access:

- Latest Compound Semiconductor, CS China and CS Taiwan magazines
- Latest features
- Latest news and more...

For further information contact:
scott.adams@angelbc.com

www.compoundsemiconductor.net

MBE GROWTH SPECIALISTS

Growth and device fabrication of arsenide/antimonide based III-V semiconductors notably:

- Narrow bandgap materials (InSb up to AlAs)
- Antimonide doping capability
- InGaAs/AlInAs structures lattice matched to InP substrates
- AlInGaAsSb lattice matched to InAs, GaSb or InP substrates
- Quantum dots/wells on GaAs substrates
- Antimonides on GaAs substrates using relaxed buffer layers

Supplier of low volume wafer requirements. Research work enquiries welcome.

Contact Tel - + 44 (0) 141 579 3020
Email – sales@quantumdevicesolutions.com
West of Scotland Science Park, Glasgow, G20 0SP

Right: Despite Soitec's decision to exit the concentrating photovoltaic business, deployment of this technology is tipped to rise and should spur sales of multi-junction III-V cells.

Bright future

awaits the compound semiconductor industry

From integrated circuits to solar, ultraviolet curing and electronic systems in electric vehicles, deployment of compound semiconductor chips is going to rise throughout this decade.

RICHARD STEVENSON REPORTS

ONE OF THE STRENGTHS of CS International is its broad coverage of our entire industry. Thanks to this, delegates attending this two-day meeting are given an accurate snapshot of the state of, and prospects for, the compound semiconductor industry.

And the good news is that the outlook is very positive – after hearing a range of talks from analysts on GaAs power amplifiers, III-V CMOS, LEDs, concentrating photovoltaics and wide bandgap devices, delegates would have concluded that sales of all forms of compound semiconductor chip should soar throughout this decade.

The most upbeat talk came from Mike Corbett, Managing Partner at Linx Consulting, who argued that the CMOS industry will turn to III-V MOSFETs to maintain the march of Moore's Law. "We believe that this is likely to be used at the 7 nm node, first by Intel," explained Corbett.

This would be a radical step, but maybe the silicon industry is more accepting of change than ever before, given the recent measures to improve IC performance while shrinking the dimensions of the transistor. As Corbett pointed out, innovations that have already been used include straining the channel to increase carrier mobility, and preventing a rise in electron leakage at the 45 nm node with the introduction of a high-κ dielectric and a gate-last process. The latter was a "big deal," according to Corbett, because it required three-to-four new processing steps.

Since then, the most radical move has been the switch from a planar transistor to an architecture with a fin protruding out of the plane of the substrate. Intel has pioneered this three-dimensional alternative that enables greater control over the carriers in the channel. The US chipmaker introduced the finFET at the 22 nm node in 2011, and three year's later it launched a variant at the 14 nm node. "So far, no-one else is using the finFET, but foundries are pursuing this," explained Corbett, who believes that the introduction of high-mobility materials will come next, probably beginning with a switch from silicon to either germanium or SiGe in the channel in the *p*FET, a step that Intel might introduce at the 10 nm node.

 Copyright Compound Semiconductor

A number of challenges will have to be overcome to produce this device, before overcoming additional obstacles that will allow insertion of a III-V *n*FET at the 7 nm node. Forming high-quality materials on silicon is a tremendous challenge, but Corbett did highlight some promising approaches, including imec's growth of III-Vs and germanium in the trenches of silicon wafers.

After Intel introduces transistors sporting new channel materials, the three foundries with the highest incomes are expected to follow suit: TMSC, the world's biggest foundry, which produces 100,000 wafers per month; Global Foundries, which is buying IBM's microelectronics business; and the independent device manufacturer Samsung. According to Corbett, these are the only three foundries keeping up with the *The International Technology Roadmap for Semiconductors* - smaller rivals are off the pace by one or two nodes.

The new technologies employed for scaling will drive up wafer costs. Calculations by Linx suggest that the transition from planar transistors at the 20 nm node to 16 nm finFETs adds 13 percent to wafer costs, while the move to germanium and III-V FETs at the 5 nm node will add another 39 percent. Higher costs results from additional steps for chemical mechanical polishing, cleaning, MOCVD growth, and formation of the fin – the latter will be the largest fab processing cost, accounting for 2 percent of the total wafer cost.

Production of wafers incorporating III-Vs should begin around 2018, with Intel launching a new generation of transistors at the 7 nm node, and high-volume manufacturing of such wafers lasting for two nodes, until the mid 2020s. Foundries will follow, introducing III-V channels at the 5 nm node in 2022, with production continuing throughout that decade.

Sunny outlook for CPV

Another positive outlook for III-Vs, in this case as a material system for making cells used in concentrating photovoltaic (CPV) systems, was given in a presentation by Karl Melkonyan from IHS Technology. Although Soitec, a leading maker of multi-junction III-V CPV cells, as well as modules and systems based on them, has decided to exit this business, Melkonyan still believes that revenue for CPV will increase substantially throughout this decade.

He kicked off his talk by discussing the entire PV industry, arguing that understanding this is an essential pre-

Wide bandgap devices are tipped to be deployed in electric and hybrid electric vehicles by the end of this decade.

requisite to grasping the opportunities for CPV. According to him, 2014 was a tough year for PV, with many companies exiting the business. However, despite this, installations increased by 20 percent to 45.1 GW last year, and total deployment in 2015 could hit 52.7 GW.

This growth is not universal. In continental Europe cuts in incentives have contributed to a reduction in installations between 2013 and 2014, but during that time there has been increasing uptake in Asian and US markets. This is driving an increase in PV revenue from areas that are sunny and dry – they are said to have high levels of direct normal irradiance – and in such areas, CPV has its best chance of competing with other solar technologies. Here, just over 3 GW of ground-mount solar was installed in 2013, and by 2018 this is tipped to rise to almost 8 GW.

How much of this will go to CPV depends on its cost, and how this compares to other technologies. The incumbent technology, silicon, became far more competitive in 2011 and 2012, with prices plumetting to such an extent that gross margins fell to less than 5 percent. Since then this margin has increased slightly, while the cost-per-Watt has gradually declined. “Cost declines of conventional PV will continue,” claimed Melkonyan, “but there will be no dramatic drop in prices.” This is because there is no significant overcapacity, and margins are already very small for companies operating in this sector.

Installations of CPV hinge on winning funding from investors, with decisions based on the levelised cost of energy – this takes into account the cost of deploying the system and its lifetime.

On this basis, CPV already undercuts PV by about 20 percent in regions with high irradiance, and generation costs are tipped to fall from 0.1 $/kWhr in 2013 to about 0.07 $/kWhr in 2018. This has led Melkonyan to forecast a rise in all forms of CPV – that includes cells made from III-Vs and from silicon – from less than 200 MW in 2014 to more than 450 MW in 2018.

The best-case scenario, argues Melkonyan, is that CPV will outperform silicon in the levelised-cost-of-energy stakes by 30 percent. This could change the perception of investors, spurring CPV deployment to 700 MW in 2018.

Taking a liking for LEDs

Another chip that will be shipped in greater numbers throughout this decade is the LED. Its growth in lighting was highlighted by Will Rhodes from IHS Technology, while Pars Mukish from Yole Développement outlined a wide variety of opportunities for the ultraviolet LED, including water treatment and curing adhesives.

Rhodes began by reviewing the state-of-play in the light bulb market. The biggest seller of the twentieth century, the incandescent, now accounts for only one-fifth of the installed base, and this figure is falling fast as many countries outlaw this inefficient source.

“The vast majority of lamps go to consumers, so price is the number one [issue],” added Rhodes, which explains why the most common purchase today is a form of fluorescent bulb. This is much cheaper than that based on LEDs, and now accounts for more than half of the working bulbs in the world. It will continue to dominate for several years, because it is competitive, combining a low retail price with lifetimes of up to 25,000 hours and reasonable efficiency. Although the cool white light that most brands produce is not favoured in Europe and the US, it is popular in China and India.

In the long term, fluorescent bulbs face the greatest competition from those made from LEDs. Sales of these solid-state sources will continue to rise over the coming years, with installations ramping from just a few percent of all lamps today to around one-quarter by 2022. By then, about a third of all the lamp sales will be LEDs, and they will account for about two-thirds of total revenue, due to their relatively high price tag. This is declining, however, and during the last year it dropped by about 20 percent.

Driving down prices will require a reduction in the cost of the LEDs, which typically account for more than 40 percent of the bill of materials in high-quality bulbs. The good news is that total chip costs should fall by 30 percent by 2019, thanks to increasing use of mid-power LEDs, a hike in GaN-on-silicon

 Copyright Compound Semiconductor

chip production, and oversupply within this industry. By the end of the decade there will also be a considerable market for chips emitting at shorter wavelengths. “The UV LED market will increase from $90 million in 2014 to $500 million in 2019,” claimed Mukish. “This market is really going.”

The opportunities for the UV LED depend on emission wavelength. Devices operating in the deep UV, which is also known as the UVC region (200 nm to 280 nm), have opportunities in air, water and surface purification; while those emitting in the UVB (280 nm to 315 nm) can find deployment in medical phototherapy; and cousins operating in the UVA (315 nm to 400 nm) can be used for curing, counterfeit detection, tanning and photocatalytic purification.

At present, many of these applications use traditional UV lamps. A high proportion of these are low-pressure mercury lamps, which generated sales of $220 million in 2014, and can be used for tanning, counterfeit detection, and residential disinfection and purification. There are also high-power mercury, deuterium and xenon lamps, which netted total sales of $370 million, finding deployment in curing, analytical instruments, and municipal and industrial disinfection and purification.

Mukish made a very strong case for the superiority of UV LED sources over the traditional lamp. Switching to solid-state allows fragile mercury-containing tubes, which last for an average of 2000 hours and take up to 10 minutes to warm up, to be replaced by a more robust source that hits full power in an instant, promises to last for tens of thousands of hours and has a size of up to 1 cm^2. The only area where the traditional lamp has the upper hand is efficiency: It ranges from 10 percent to 45 percent, while that of the UV chip can be just a few percent in the UVC and UVB, and up to 35 percent in the UVA.

These strengths have driven the incorporation of the UV LED into quite a few curing systems. Mukish highlighted examples of this, showcasing a total of 11 products from US, German and UK companies that had been brought to market since 2011. Mukish expects UV LEDs to be deployed in a wide variety of applications by the end of this decade: UVA sources are already adopted for nail gel curing, will be used in general lighting from 2016, and the year after that will appear in biomedical devices; UVB LEDs have just started to speed plant growth, and by the middle of this year will be used in medical phototherapy; and at around that time, UVC LEDs might start to be deployed in cell phone disinfection systems.

Packaging problems

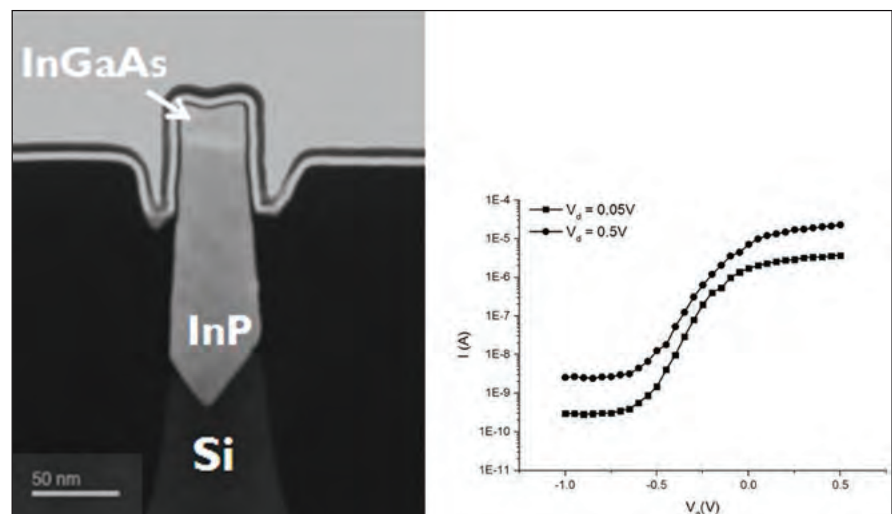
While the UV LED is still in its infancy, the compound semiconductor sector based on SiC and GaN power electronics is far more advanced. Pierric Gueguen from Yole Développement even went so far as to say that the era of wide bandgap power electronics is well underway, having been going for a couple of years.

Before detailing the successes to back up that claim, Gueguen considered the big picture, reviewing changes in the power electronics market and offering a prediction of where it is heading. Global revenue for the combination of power ICs, power modules and discretes totalled just over $10 billion in 2012 and 2013, but grew by 8 percent in 2014, and will steadily climb to around $17 billion by 2020. Although silicon dominates this market, chips made from wide bandgap materials are playing an increasing role. The SiC diode has now been available for more than a decade, and it has been joined in the last few years by various forms of transistor, including the SiC BJT, the SiC JFET, the SiC MOSFET and the GaN HEMT.

Many of these devices are already available from more than one supplier, and buyers will have even more choice in future, as chipmakers launch products now in development. The competition between these makers of wide bandgap devices will be fierce, and include many formidable firms that have established themselves as silicon chipmakers – that’s the case for Infineon, Rohm, Panasonic, Toshiba, Hitachi, and Furukawa Electric.

The battle between these silicon giants and some specialists in SiC and GaN will fuel improvements in chip performance, but widespread adoption of wide bandgap products is not guaranteed to follow, argued Gueguen, unless packaging improves so that it can ensure reliability at high temperatures and deliver low stray inductance.

If devices can be armed with these attributes, engineers can then build products operating at higher frequencies and temperatures, and deliver benefits at the system level – such as lower cost, smaller size, and reduced weight – that can offset the research and development costs associated with introducing new forms of diodes and transistors.



The growth of InP in trenches in a silicon wafer offers one promising route to increasing channel mobility, and ultimately maintaining the march of Moore’s Law at the 7 nm node and below.

Right: Many countries have outlawed the incandescent bulb, due to its low efficiency. Fluorescent sources are now popular, due to their long lifetimes, low retail price and high efficiency. LED lamps will be the long-term winner, however, with sales rising as the price of these efficient, instant-on bulbs fall.

Gueguen went on to discuss the packaging of power modules, revealing that the majority of failures are associated with interconnection, die attach and substrate attach. To address this, efforts are being directed at: connecting die using innovative wire-bonding approaches such as aluminium ribbon bonding, or techniques that use no wires; and attaching the parts that form the module using new materials, such as copper-tin eutectics.

Although improvements in packaging would be welcome, SiC devices are already being used in PV inverters and rail traction, and in the next couple of years they will start to be deployed in uninterruptable power supplies, industrial motor drives and wind turbines. But it will be 2018 before SiC is seen in electric vehicles. Meanwhile, for GaN, its use in DC-to-DC convertors and wireless charges is underway – and this material is about to be used in power supplies and PV invertors, and it should see deployment in electric vehicles from 2017. However, it is not yet clear whether chips based on GaN will be used for uninterruptable power supplies and industrial motor drives.

These developments are good news for substrate and epiwafer manufacturers. According to Gueguen, global sales of SiC substrates should grow from just over $100 million in 2015 to almost $300 million by 2020, while annual revenue for GaN-on-silicon epiwafers should rocket from $30 million for this year to $280 million by the end of the decade.

The fifth CS International, held at Sheraton Frankfurt Airport Hotel and Conference Centre on Wednesday 11th and Thursday 12th March, attracted over 300 delegates and featured more than 30 presentations, including seven from leading market analysts.

Opportunities in defence

Growth is heading in a similar direction for RF compound semiconductor chips, although increases in sales will be more modest, according to projections presented by Eric Higham and Asif Anwar from Strategy Analytics.

Higham revealed that growth of global revenue for GaAs microelectronics has been increasing at around 11 percent per year since the birth of the wireless era in 2014, and last year it might have been worth as much as $7 billion. The majority of this is associated with sales of power amplifiers, which are increasingly multi-band, multi-mode products that will face increasing competition from those based on silicon – a detailed report of Higham's presentation, and those by CMOS PA maker Peregrine and GaAs-based rivals Skyworks and Qorvo is provided in the feature *What future for the PA*, on p. 32 of this issue.

Meanwhile, Anwar considered the opportunities in the defence and military markets for compound semiconductor devices, and began by reviewing global defence spending. This is growing at just over 2 percent per year, but thanks to an emphasis on improving capability at the system level, spending will grow much faster in areas where III-Vs have a role to play, such as radar and communication.

One example of this is the growing deployment of active electronically scanned radar. This form of radar, which may contain GaN transmit modules, is being fitted in warplanes and military vessels, and is helping to increase worldwide spending on radar from just under $14 billion in 2015 to more than $18 billion in 2023. Spending on electronic warfare is expected to follow a similar trend, rising from just over $8 billion this year to almost $11 billion by 2023, and there are also opportunities for III-Vs in military communication, which is growing at more than 3 percent per year, and will be worth $35 billion in 2024.

Thanks to growth in all these areas, Anwar predicts that sales of GaAs devices, which account for about three-quarters of all III-V revenue related to defence systems, will increase at 11 percent per year through to 2019. Meanwhile, GaN, accounting for all of the remaining compound semiconductor sales over that time frame, will increase in revenue at 28 percent per annum.

Success in these markets, plus the likes of solar and mobile devices, indicates that revenue for many III-V chipmakers should rise throughout this decade and beyond. While it's hard to predict the future, it clear that it is going to be underpinned by compound semiconductor devices.

 Copyright Compound Semiconductor

COMPLETE
THIN FILM
DEP & ETCH
SOLUTIONS

Let Evatec engineers help you solve your manufacturing puzzles. From raising throughput in Under Bump Metallisation (UBM) processes on 12 inch, to delivering plasma damage free sputter processing on GaN for LEDs and Power Devices, Evatec platforms with Advanced Process Control (APC) raise yields and lower Cost of Ownership. For more information about Evatec visit our website at **www.evatecnet.com** or contact **your local sales agent**.

MORE INFO

LEDs • ADVANCED PACKAGING • POWER DEVICES • MEMS • TELECOMS • PHOTOVOLTAICS • EVATEC - THE THIN FILM POWERHOUSE

www.evatecnet.com

Reprints are a valuable sales tool

Benefit from a reprint featuring your company

They can be ordered after publication and can be customised to your exact needs

For more information and prices please contact the sales team.

Robin Halder
T: +44 (0)2476 718970 E: robin.halder@angelbc.com

Shehzad Munshi
T: +44 (0)1923 690215 E: shehzad.munshi@angelbc.com

Lasertec

Defect Inspection/Review tools
for compound semiconductor

WASAVI Series

SiC Wafer Inspection / Review System

SICA 6X

OQC/IQC/Process Monitor
for SiC wafer mass production

Transparent Object Inspection System

TROIS 33

High speed defect inspection of transparent wafers
such as GaN on Si

www.Lasertec.co.jp

Graphene

gets GaAs onto silicon

What's the trick to growing high-quality GaAs on silicon? It's inserting a layer of graphene between them.

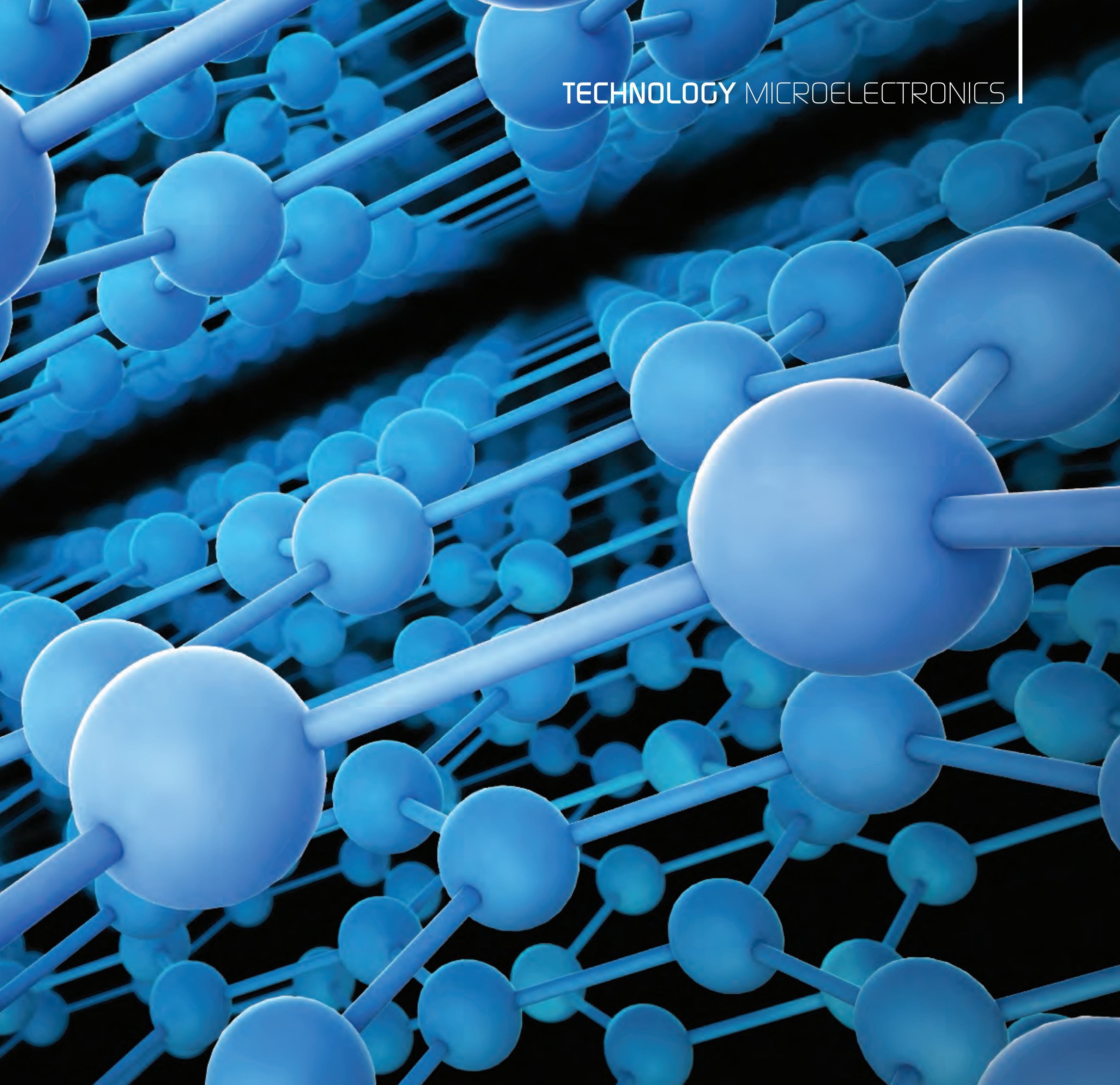
BY SHAMSUL ARAFIN FROM UCLA

OUR COMPUTERS don't operate anywhere near their potential. Instead, their microprocessors spend a lot of time waiting for data. Even if we invest in the state-of-the-art – an Intel Core i7 processor with high-speed RAM or liquid cooling – the problem persists, because the speed of the computer is not governed by the processing power, but by the physical connections between the processor and the incoming data.

The solution, which is well known but challenging to implement, is to turn to photonic integration. By taking this path, trimming the power consumption can go hand-in-hand with a hike in system performance: Greater speed, wider bandwidth and superior reliability. What's more, by using photons rather than electrons, more efficient data transfer is possible from module-to-module or chip-to-chip.

Given these advantages, it is easy to understand why there is a worldwide research effort underway to replace the existing, old-fashioned, electron-carrying copper with a technology that routes photons around chips. Super-fast computers could follow, but this requires the pairing of silicon substrates containing matured CMOS electronic circuits with a material that can emit light.

Light-emitting GaAs is the leading candidate for monolithic integration with silicon, and since the 1980s efforts have been underway to bring these two materials together. Accomplishing this is no mean feat, however: Anti-phase domain boundaries can formation during growth of polar GaAs on nonpolar silicon; and a high density of threading dislocations can result from a combination of a 4.1 percent lattice mismatch and a 62 percent thermal expansion coefficient mismatch between these two materials.



At the Univeristy of California, Los Angeles (UCLA), our team led by Kang L. Wang, the Raytheon Professor of Electrical Engineering, is working in collaboration with colleagues at UC Irvine and UC Riverside to develop a growth technique that can deposit GaAs on silicon using an intermediary material – graphene. With this bridging material, MBE can form ultra-smooth, almost-epitaxial films of GaAs on top of a single-layer sheet of carbon atoms that sports many attributes, including breath-taking electron mobility, high conductivity, and great flexibility and strength.

The approach that we have taken is often referred to as van der Waals epitaxy, and thanks to the one-atom thick pure-carbon buffer layer, we are relieved of material-related intrinsic challenges, such as lattice mismatch and thermal expansion coefficient mismatch. The very weak physical bond between the MBE-grown GaAs and the graphene buffer layer is the key to this success, because it can accommodate thermal mismatch and strain due to inplane lattice mismatch (see Figure 1).

Our efforts follow in the footsteps of the pioneers of van der Waals epitaxy, Atsushi Koma's group from Akita Prefectural University, Japan. In the mid 1980s, that team constructed layered material systems, such as selenium/tellurium and $NbSe_2/MoS_2$, with this growth technology.

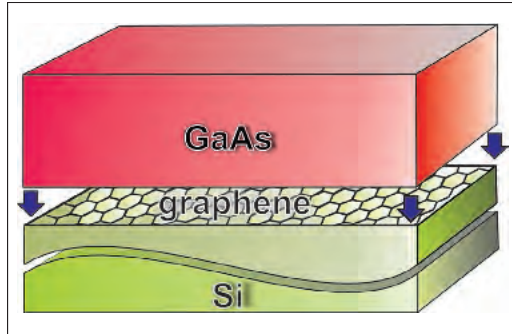


Figure 1: An intermediary single graphene layer allows the growth of GaAs on silicon.

Since then, there has been a growing acceptance of van der Waals epitaxy as a useful route to heteroepitaxy. Recently, even heterostructures with a lattice mismatch as high as 40 percent have been grown with reasonably good crystal quality. The technique has also been extended to enable the growth of three-dimensional materials on top of layered materials by researchers at IBM T. J. Watson Research Center.

Although production of inexpensive, large-scale graphene is now possible, we have used a mechanical exfoliation technique to deposit graphene onto silicon substrates. This approach begins with a 5 minute rinse of a 1 cm by 1 cm piece of silicon in acetone and isopropanol, before graphene flakes are mechanically exfoliated onto non-HF-treated silicon by the well-known scotch-tape technique. The silicon substrate with the monolayer of graphene is then cleaned in acetone and isopropanol to remove any residual organics from the exfoliation process (see Figure 2 for images of the mechanically exfoliated graphene).

The quality of the epitaxial growth hinges on the nucleation step, which influences film properties, morphology, homogeneity, defect densities, and adhesion. Growth of our nucleation layer was performed using a room-temperature-deposited gallium-prelayer and a very low growth rate. We set the GaAs growth temperature to just 350 °C to avoid islanding and to enhance the nucleation process. This yielded ultra-smooth GaAs thin films on graphene-on-silicon that can serve as a nucleation (seed) layer for subsequent growth.

Quality of our as-grown films has been assessed by Raman spectroscopy, which exhibited two GaAs Raman signature peaks corresponding to the TO and LO vibrational bands at 268 cm^{-1} and 292 cm^{-1}, respectively (see Figure 3(a)). The forbidden, but intense TO mode results from defects in the nucleation layer, indicating the need for further improvement in material quality.

A comparison of the quality of our films with those formed by conventional growth is possible by comparing full-width at half maximum (FWHM) values of X-ray diffraction rocking curves (see Figure 3 (b)). The results of this are very encouraging, with 25 nm-thick films made by us having a FWHM of 240 arcsec, which is the same value as micron-thick GaAs films deposited on silicon by conventional means. This two-orders-of-magnitude improvement is due to mitigation of the lattice and thermal mismatch between GaAs and silicon by the graphene buffer layer.

We have built on this success by creating a two-step nucleation process, followed by a raising of the temperature to 600 °C to grow a further 200 nm of GaAs. A polycrystalline film with a faceted surface results, due to thermal degradation of the nucleation layer (see Figure 4).

We have tried to prevent the island growth in the high-temperature epitaxy step by increasing the nucleation layer thickness to 100 nm. However, this has not been successful,

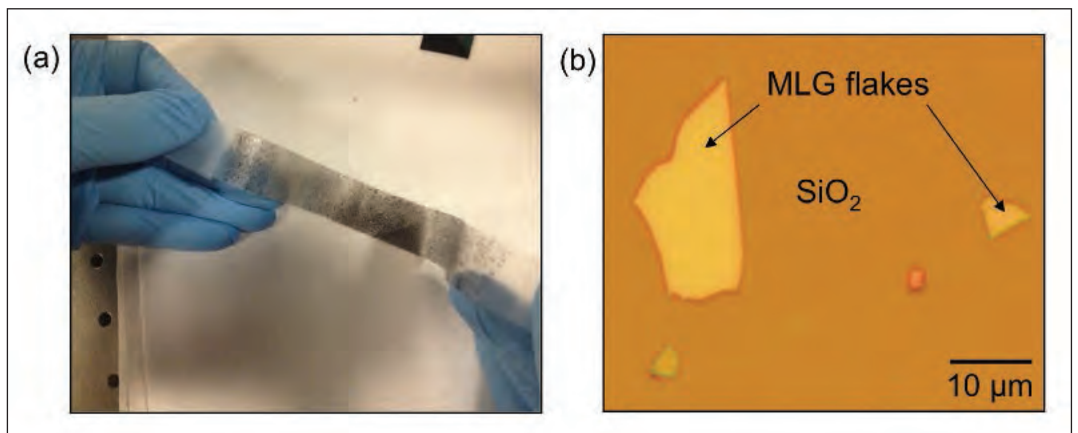


Figure 2: (a) Mechanical exfoliation of multi-layer graphene (MLG) flakes using scotch-tape, and (b) optical microscope image for the exfoliated MLG lying around a silicon substrate with a native oxide. Figure adapted from Alaskar ***et. al.*** (2014)

SEMICON® West2015 | JULY 14 – 16 MOSCONE CENTER SAN FRANCISCO

Register Now

The Marketplace for Microelectronics Innovation

SEMICON® West is the premier destination for the people, products, and companies driving the future of microelectronics design and manufacturing, and is the global marketplace for microelectronics innovation.

SEMICON West is brought to you by

Sample of Programs for 2015

Enabling the IoT: Opportunities and Challenges for the Semiconductor Sector—These new devices will need lower cost and lower power. This program will examine strategic issues, such as new sensors, energy harvesting, and options for heterogeneous integration of multiple devices.

What's Next for MEMS—Industry thought leaders will discuss what to expect next in this dynamic market, including new sensing technologies, new packaging and integration requirements, plus new players and business models.

What's New in Flexible Printed Electronics—This program will examine the impact of flexible, hybrid electronics on new products and innovation, and investigate flexible hybrid manufacturing techniques. Industry leaders will discuss the latest thinking about electronics on plastic, paper, and glass, also the implications of flexible electronics designs for long-lasting and always-on IoT.

Next Generation Non-volatile Memory: MRAM, RRAM and 3DNAND—Learn about the state of emerging memory technologies and the challenges for high volume manufacture.

Challenges for Getting to 5 nm, Photolithography and Transistor Scaling—Explores high volume manufacturing solutions, including the role that EDA tools will play. Examines lithography cost and productivity issues in achieving 5 nm and below.

The Path to Future Interconnects, Co-sponsored by the Electron Devices Society of IEEE—Reviews challenges in materials and processing to manufacture interconnects needed for high performance computing.

Packaging for Digital Health and Automotive Devices—Explores packaging implications for new IoT devices.

65 HOURS of Technical Programs

650+ Exhibitors

www.semiconwest.org

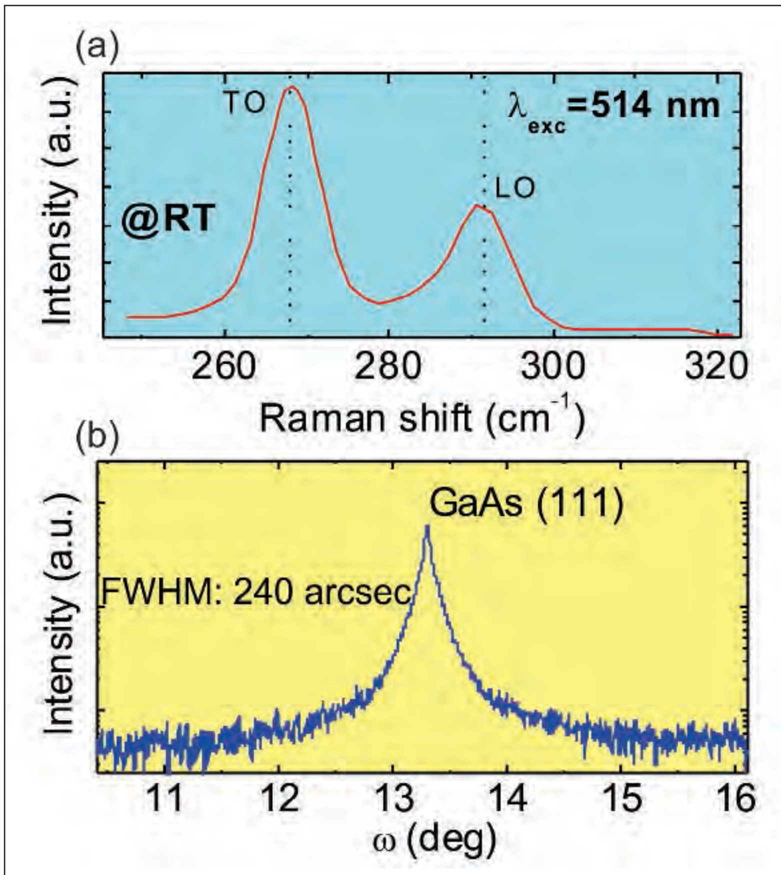


Figure 3: (a) The room-temperature micro-Raman spectrum for the low-temperature-grown GaAs nucleation layer, and (b) the X-ray diffraction rocking-curve scan of the GaAs (111) peak for such nucleation layer. Figure adapted from Alaskar *et. al.* (2014)

suggesting that the GaAs/graphene interface is not stable at high temperatures – and that's unfortunate, because high temperatures hold the key to crystalline GaAs, and to the suppression of defects and dislocations through migration.

It is our view that the root of the problem is the low adsorption and migration energies of gallium and arsenic on multi-layer graphene, which lead to cluster-growth at high temperature. However, it may be possible that by optimising the growth parameters, in terms of the pre-layer, or by turning to an alternative van der Waals material, it would be possible to produce a single-crystal GaAs thin film on silicon. We are looking into this, and also considering a low-temperature or modified deposition technique that would eliminate three-dimensional islands at high growth temperatures.

As our growth of graphene on GaAs improves, it could lead to cheaper, high-performance light sources. What's more, it might pave the way for the formation of other III-Vs on silicon, such as InP and GaSb, and ultimately spur a vast range of lower cost, high-performance semiconductor devices.

Before this might happen, we expect that thanks to its compatibility with current silicon planar CMOS technology, our novel growth technique will be used in the silicon photonic industry. Here it could be used for the realization of an electronics-photonics integrated circuit on a single chip, for applications ranging from on-chip photonics to optical transceivers, free-space laser communications and microwave photonics.

Such efforts form part of a global effort to develop electronic integrated circuits that incorporate optical emitters and detectors and will underpin the transition from CMOS to optics. The silicon industry is searching for ways to introduce optical capabilities onto the silicon IC, and our GaAs-on-silicon technology is one option for doing this in an economically viable manner.

- Shamsul Arafin now works at UCSB

Further reading
Y. Alaskar *et. al.* Adv. Funct. Mater. **24** 6629 (2014)
J. Kim *et. al.* Nat. Commun. **5** 4836 (2014)

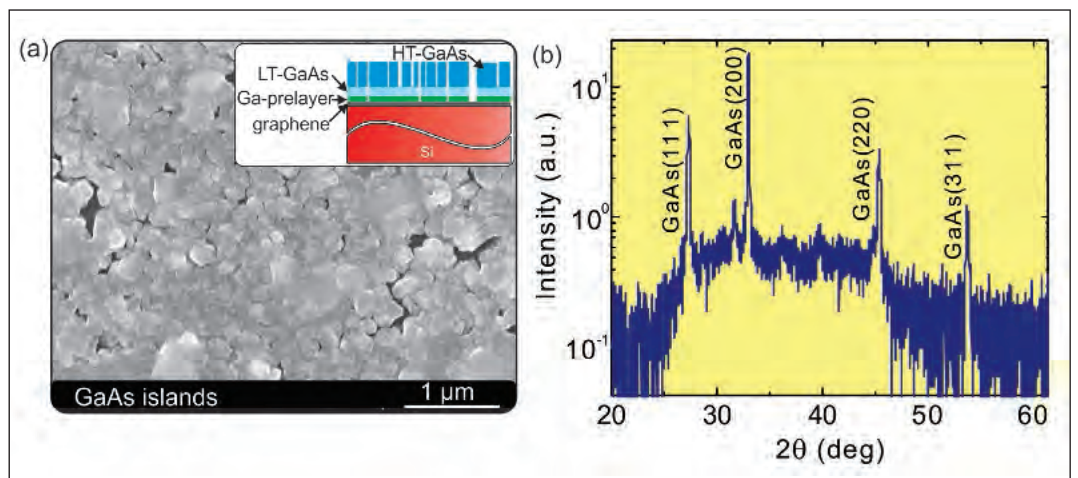


Figure 4: SEM image of (a) 200 nm high-temperature grown GaAs on top of a 25 nm-thick nucleation layer, with a gallium prelayer showing cluster growth and (b) X-ray diffraction ω/2θ scan for GaAs grown by the two-step growth scheme, showing polycrystallinity with the presence of GaAs (111), (200), (220) and (311). Figure adapted from Alaskar *et. al.* (2014)

 Copyright Compound Semiconductor

www.csmantech.org

2015 International Conference on Compound Semiconductor Manufacturing Technology

May 18 - May 21, 2015
Hyatt Regency Scottsdale Resort & Spa at Gainey
Scottsdale, Arizona, USA

Conference Chair
Paul Cooke
chairman@csmantech.org

Technical Program Chair
Glen "David" Via
tpcchair@csmantech.org

Registration Chair
Travis Abshere
registration@csmantech.org

Local Arrangements Chair
Alex Smith
local@csmantech.org

Exhibits Chair
Ruediger Schreiner
exhibitor@csmantech.org

Workshop Chair
Patrick Fay
workshops@csmantech.org

Publicity Chair
Kelli Rivers
publicity@csmantech.org

Publication Chair
Thorsten Saeger
publication@csmantech.org

University Liaison
Shiban Tiku
student.aid@csmantech.org

Sponsorship
Jansen Uyeda
sponsorship@csmantech.org

CS ManTech will celebrate it's 30th Year

Visit www.csmantech.org for

Advanced Program, Conference Registration and Hotel Information

AT THE TURN OF THE TWENTY-FIRST CENTURY, engineers could grab the headlines with claims of a monolithic IC working at hundreds of gigahertz. Fast-forward fifteen years to today, however, and the fabrication of such a device doesn't even raise eyebrows – there are ICs operating within the G-band at 140 GHz and 220 GHz that are finding deployment in a wide range of applications.

What is special about both these frequencies – 140 GHz and 220 GHz – is that they are at low-loss operational 'windows' in the Earth's atmosphere. Consequently, radiation at these frequencies can travel substantial distances, underpinning

Power amplifiers:

Getting to the G-band and beyond

Vertical electron transport and a well-defined junction make the InP HBT the best building block for powerful, high frequency amplifiers

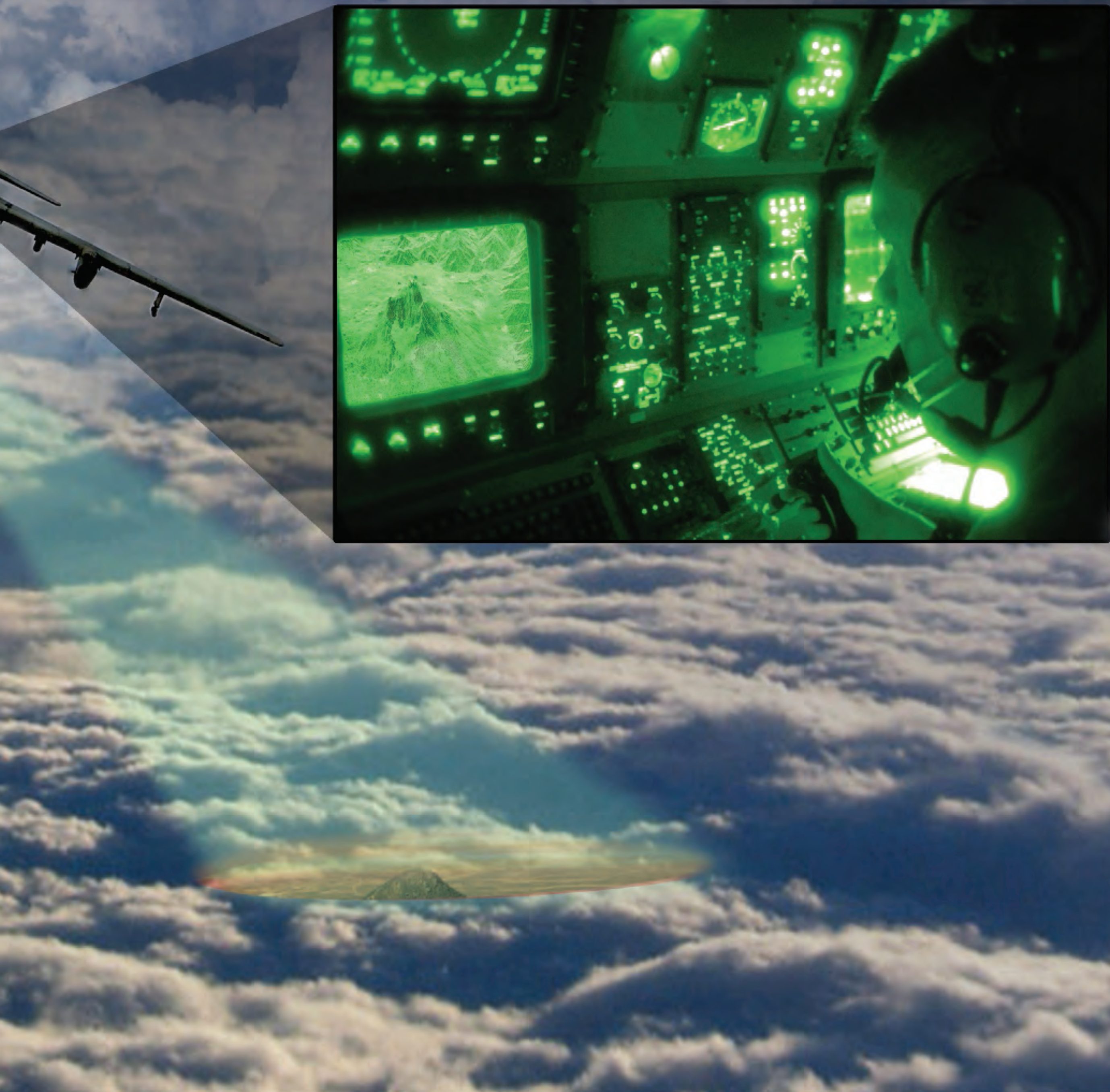
BY ZACHARY GRIFFITH AND MIGUEL URTEAGA FROM TELEDYNE SCIENTIFIC

the construction of a wide variety of systems, including: very high data rate point-to-point links; personal imaging systems for detecting concealed weapons; synthetic aperture radar (SAR) systems operating with multiple frame rates per second, which can track manoeuvring targets and image scenes on the battlefield; and power amplifiers driving brethren based on vacuum electronics, and ultimately enabling sources of up to 100 W.

In the US, the Defense Advanced Research Projects Agency (DARPA) has supported the quest to develop G-band ICs by devising, funding and co-ordinating several programmes, including TFAST, SWIFT, FLARE, HiFIVE, and THz Electronics. Such efforts have provided the proof that InP, which has a higher electron transport velocity than silicon and SiGe, is well suited for the construction of G-band circuits with sufficient gain and bandwidth – and it is also capable of yielding terahertz transistors.

At Teledyne Scientific of Thousand Oaks, California, we have played our part in many of these DARPA programmes, developing during the last decade an InP-based double heterojunction bipolar transistor (DHBT) technology with high-frequency capability. Compared to its cousin, the InP HEMT, the DHBT has more than double the breakdown voltage, and it holds the key to fabricating state-of-the-art G-band power amplifiers. That is not the only merit of this class of transistor, however, as it also sports superior device uniformity, thanks to its vertical electron transport.

 Copyright Compound Semiconductor



Laying the foundations

Our efforts at developing an InP-based G-band amplifier began with the development of the DHBT technology. This was not trivial, because it is not permissible to substitute InP into a SiGe HBT process. Instead, our engineers had to design and have grown an epitaxial structure with two separate heterojunctions: one between the InP collector and InGaAs base, and the other between the InGaAs base and InP emitter. In both cases, the junctions could not be abrupt, with alloy grading needed to eliminate conduction band discontinuities. Extensive studies led to the fabrication of such structures, which also had to provide to the semiconductor terminals contacts that are ohmic and exhibit a very low parasitic resistance.

To ensure adequate bandwidth and gain, delays associated with parasitics had to be minimised by adopting narrow transistor features. This was accomplished with recipes developed for e-beam lithography and i-line photolithography. Device fabrication followed, using 100 mm wafers and multi-level interconnects. Such efforts have enabled the construction of MMICs

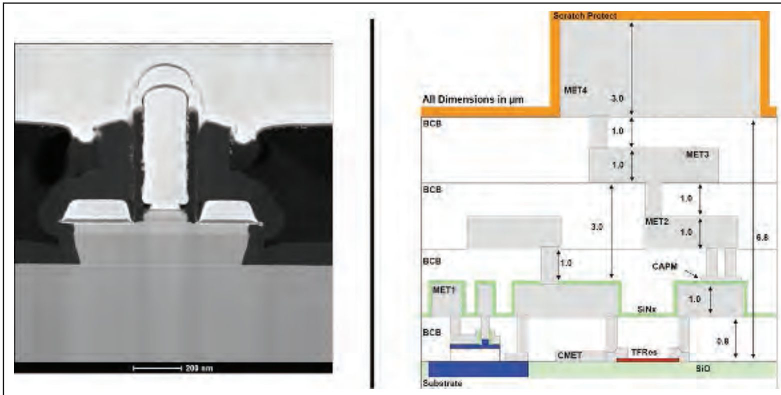
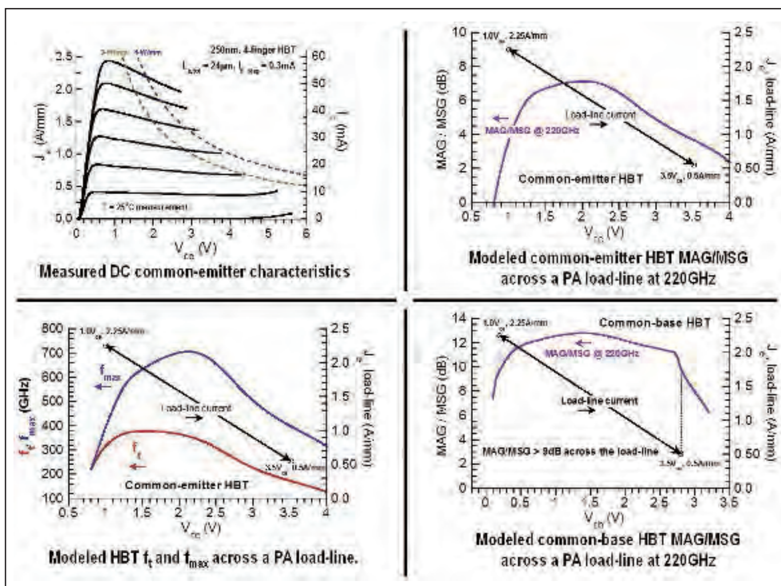


Figure 1. A scanning electron microscope cross-sectional image of the Teledyne 250 nm InP HBT and MMIC technology. MBE on 100 mm InP substrates forms epistructures featuring a highly doped, 30 nm-thick graded InGaAs base. High breakdown is ensured with a 150 nm InP collector that employs super-lattice grading between InGaAs and InP. High semiconductor doping at the collector, base, and emitter metal-semiconductor interfaces permits very low parasitic ohmic contact resistance – this is critical for achieving high gain and high f_{max} transistors.

with a bandwidth exceeding 670 GHz, formed using the 1.1 THz f_{max}, 125 nm technology. This is a tremendous accomplishment that involved overcoming many challenges on the way to the fabrication of world class G-band and THz MMICs.

Development of these highly capable integrated circuits has included efforts to shrink transistor dimensions. This has spawned a portfolio of technologies: 500 nm transistors, our most mature technology capable of producing MMICs with thousands of DHBTs; 250 nm transistors, a mature technology for MMICs with upwards of 500 DHBTs; and, under development, transistors at a node with a 125 nm emitter that can be used to form MMICs with 50-100 DHBTs. Note that for G-band sources and frequencies up to 300 GHz, the 250 nm node has a great set of attributes, combining an f_t of more than 350 GHz with an f_{max} that tops 600 GHz and breakdown voltage of 4 V.

Figure 2. Measured DC and modelled RF performance of the Teledyne 250 nm InP HBT technology for 220 GHz PA applications.



In order for this technology to be useful, there must be accurate predictive modelling of the transistor, passive components and the wiring environment. This has been realised by developing, through numerous iterations, a scalable large-signal model of the DHBT. Accurate predictions of the performance of this transistor over a range of currents and voltages are then possible; and in turn, this aids the designing of a power amplifier, because it is possible to calculate the optimal impedance to the DHBT for the highest output power.

Another requirement for high-performance MMICs operating in the G-band and beyond is to have low loss interconnects. To realise this, we use 1 µm-thick benzocyclobutene intermetal layer dielectric spacing with an electrical permittivity of 2.7 within the four-metal layer interconnect (see Figure 1 for an example of this technology). One downside of such a device is that its foundation, InP, is not as sturdy as silicon or GaAs. To address this we have a robust process for thinning 100 mm InP wafers to either 75 µm or 50 µm. We are able to incorporate thru-substrate vias and metallization, enabling backside grounding of the chip and suppression of parasitic modes at G-band and terahertz frequencies.

Ensuring uniformity

The construction of precision analogue and comparator circuits, as well as highly combined power amplifiers, is only possible with MMICs that are formed from devices with identical DC and RF characteristics. Such a requirement plays into the hands of the HBT, which has two key advantages over the HEMT: the characteristics of the *n-p-n* transistor are well defined by epitaxial design, growth, and drift-diffusion electron transport theory; and electrons traverse vertically inside the device, and tend to be within the width of the emitter feature.

In contrast, electron transport in the HEMT is horizontal, with carriers traversing from source to drain via the channel. One implication is that for the construction of transistors that could be used in G-band and terahertz MMICs, gate feature sizes of only 20 nm have to be defined by lithography and metal deposition. Any variations in how the gate is formed, in the separation of gate electrode and channel, will modify HEMT performance and

 Copyright Compound Semiconductor

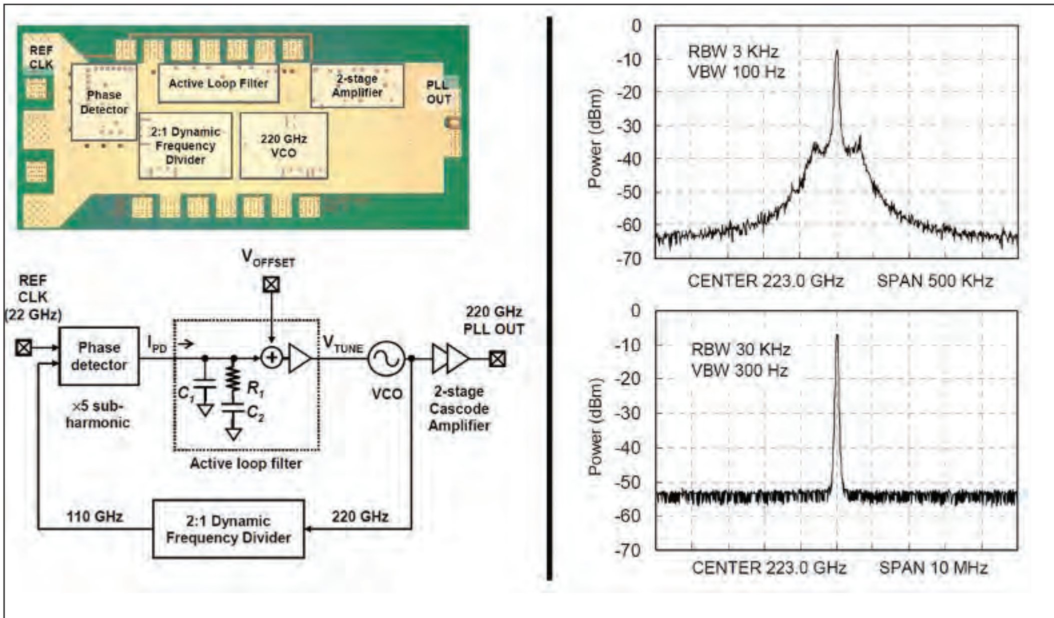


Figure 3. Teledyne's 220 GHz phase-locked loop is formed with 250 nm InP HBT technology and has a 220.0 to 225.9 GHz locking range. The output from the 220 GHz voltage-controlled oscillator drives a 2:1 dynamic divider to supply a fifth-order sub-harmonic phase detector a 110 GHz signal, using a 22 GHz reference clock.

place an upper limit on the number of devices that can be used within such a high-frequency MMIC.

Thanks to the nature of the electron transport in the HBT, the accuracy of predictive and scalable large-signal models, which are based on the Agilent-ADS III-V HBT model, is superior to those for the InP HEMT (the latter are either empirical or small-signal models, which are compromised by limited bias range and accuracy). Having access to a highly predictable, large-signal model is incredibly valuable, because when a designer has to consider and potentially adopt a new technology to their MMIC, mixed-signal, and system needs, they can slash the time and cost of this project. These savings result from a trimming of design variations and a reduction in the number of fabrication runs.

Assessing performance

Transistors are often judged by their values for maximum oscillation frequency f_{max} and the breakdown voltage, but for MMIC designers, other figures are more useful. More valuable is the gain that the DHBT has in common-emitter and common-base configuration at a given operating frequency, and the on-state destructive voltage at different operating currents. These values are much better than those for SiGe HBTs and InP HEMTs (see Figure 2). Common-emitter characteristics show a peak current density of 2.5 A/mm (10 mA/μm^2) at a 0.8 V knee voltage, while at low-voltage operation, the device may be operated up to a power density of 4 W/mm. At a 4 V bias, a DC current of 0.75 A/mm is feasible.

A noteworthy feature in these plots is how the gain varies with the configuration employed for

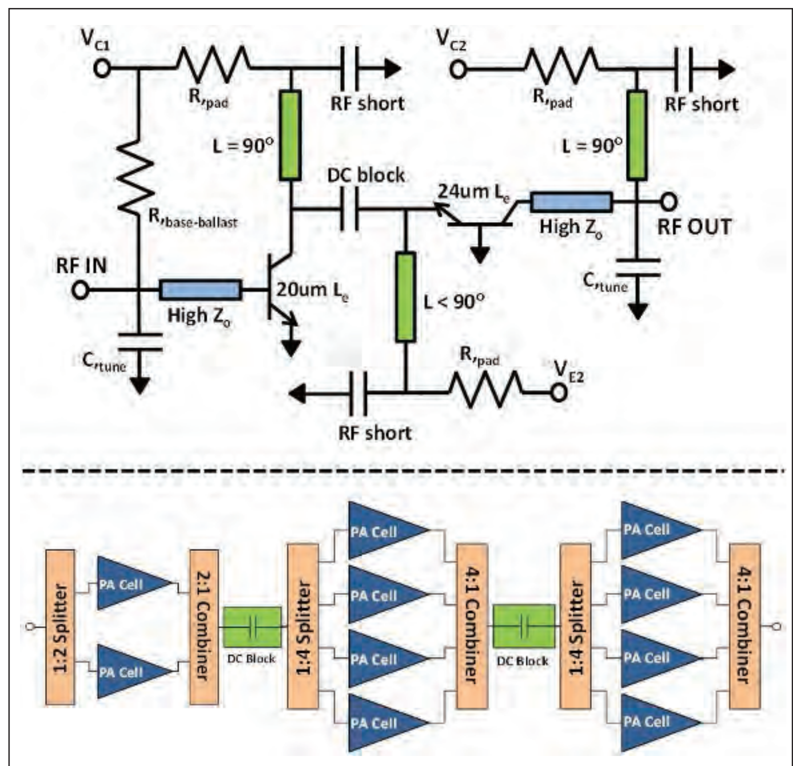


Figure 4. The cascode power cell (top) and a block diagram of the three-stage, 4-cell output combined PA (bottom). This three-stage, 4-cell combined amplifier is the basis for Teledyne's 8- and 16-cell combined amplifiers, where the 2:1 combiner structure is used to add them together.

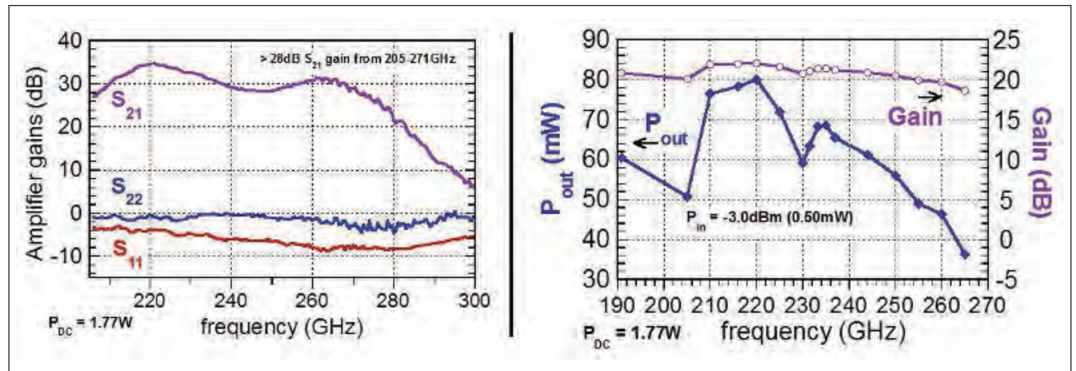


Figure 5. The RF performance of Teledyne's high-bandwidth, three-stage, 190-260 GHz PA. Gain, determined by the S-parameter S_{21}, is greater than 28 dB from 205-271 GHz. Large-signal data shows output power and gain across frequency, where the PA input power is constant at only -3.0 dBm (0.5 mW P_{in}). Output power is greater than 50 mW from 190.8-254 GHz, and hits 80 mW at 220 GHz.

the transistor. In common-emitter configuration at 220 GHz, plots of gain have a peak of 7.5 dB, and much lower values at the power amplifier load-line endpoints. Turn to a common-base configuration, however, and gain is 9dB at the operating endpoints, and peaks at 12.5 dB. This performance, which is superior to that of the SiGe HBT and InP HEMT, is partly due to very high collector-to-emitter RF isolation. In addition, there is an absence of Miller multiplication of the base-collector junction capacitance, which does play a role when the HBT is common-emitter configured.

Before MMICs operating at these G-band and terahertz frequencies can be designed, engineers need to have in their toolkit a low-loss interconnect environment and passive components. One issue with the 250 nm InP HBT, which has very high gain at G-band, is that it is prone to instability when the traditional design approaches and interconnect schemes used for Ka-band to W-band MMICs are employed. Our solution is to turn to thin-film microstrip wiring. Compared to grounded coplanar waveguide and thru-substrate microstrip, this approach has four advantages: there is lower loss; there are more interconnect layers, which can be spaced much more densely; there is no need for wafer thinning and dicing prior to MMIC evaluation; and the accuracy of electromagnetic modelling is higher, thanks to tremendous simplification of the modelling of the ground-return currents.

Our thin-film microstrip technology employs either the top-most or bottom-most metal layer as the ground-plane, with the remaining metal layers used for DC and RF interconnect routing. With this approach, measured insertion loss is just 1.1dB/mm at 220 GHz for a 50 Ω transmission line.

Armed with this knowledge of the capability of this technology, combined with very accurate modelling of the transistor, we have built a range of 220 GHz MMICs and PAs. One of their features is that they avoid the traditional approach for making signal sources that are needed to construct transmitters and receivers. The conventional, effective approach for generating an LO source at these frequencies is to multiply up the frequency reference. Unfortunately, however, multiple chips are needed to incorporate this LO into a transmitter or receiver architecture – and using multiple chips adds to cost and introduces complexity. There are several reasons for this, including the need to evaluate each chip, and the need to machine multiple waveguide blocks

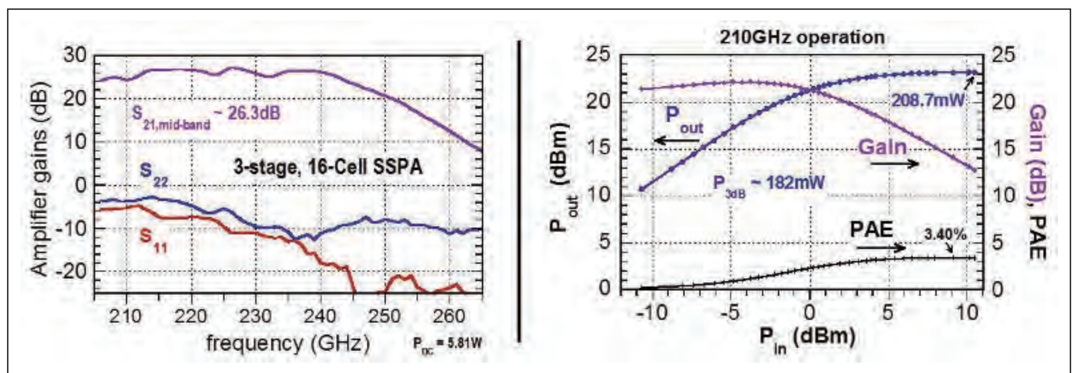


Figure 6. Teledyne's high-gain InP HBT PA can deliver more than 200 mW. Formed by taking three-stage 4-PA cell MMICs and stacking them for a total of 16-PA cells – and combining the outputs using 2:1 combiners – this is the highest power G-band 220 GHz MMIC ever. The S_{21} mid-band gain is 26.3 dB from 205-243 GHz, and at 200 GHz, output peaks at 220 mW.

or channels and load chips. In addition, the waveguide block has to be re-evaluated prior to shipping the final transmitter or receiver assembly.

We avoid these issues with our 250 nm InP HBT technology. With this, we make a monolithic single chip receiver or transmitter that contains a PLL frequency source, mixer, and either LNA (receiver) or PA (transmitter). The most sophisticated part of this is the PLL circuit, which employs a phase-detector, active loop filter, voltage-controlled oscillator (VCO), and 2:1 dynamic divider (see Figure 3 for details).

An advantage of this PLL approach is that it does not require an additional frequency division of the (VCO) signal to the phase detector. Thanks to this, power dissipation falls, and there is also a reduction in MMIC transistor count. Operation of this part of the circuit involves feeding the phase-detector output into the active loop filter, with the output of this supplied to the VCO control node to phase-lock the VCO operation. Note that one implication of the inverted thin-film microstrip is that the ground plane conceals the circuit blocks – labels show where they reside.

Measurements of the output of the PLL reveal a centre frequency of 223 GHz, which is close to the simulated value of 220 GHz. Phase noise at 220 GHz, 223 GHz, and 225.9 GHz is very similar, with values for 10 kHz and 100 kHz offset of -61 dBc and -83 dBc. The PLL may be integrated, on-chip, with a mixer and an amplifier to construct a transmitter or receiver. Such a chip requires just one waveguide block, making it much cheaper than products based on multi-chip, frequency-multiplication approaches.

High-frequency amplification

The development of our high-frequency InP DHBT technology has been applied to high-power PAs operating at 220 GHz and the upper end of the WR04 frequency band (it extends from 170 GHz to 260 GHz). These amplifiers produce far more power than those formed from either InP HEMTs or large diode multiplication units, an advantage that is highly valued at the system level. Thanks to packaging advances at G-band frequencies, modules can be constructed from a battalion of PAs, increasing the RF power. The key to realising this is being able to produce and select MMICs with identical gain, phase, and saturated output power.

By avoiding the need for wafer thinning prior to RF evaluation, we can carry out automated wafer probing of the PAs. Thanks to advances in high-frequency wafer probes from GGB Inc., more than 11,000 PAs can be evaluated before the probe-tips require maintenance. The probing

> “Thanks to DARPA’s sponsorship, we are now seeing our 220 GHz amplifiers based on 250 nm InP DHBT technology leaving the lab in volume levels to construct Watt-level solid-state power amplifier modules operating at 210-230 GHz. This milestone, and the ‘productization’ of the G-band MMIC, indicates that the InP HBT is well-positioned to address MMIC requirements that will spur commonplace G-band and terahertz systems”

determines values for S-parameters, and with software sifting through this data, just a ‘spot-check’ of large-signal performance is needed. This is a tremendous breakthrough, because testing can account for up to 40 percent of the total cost of production for MMICs operating in the G-band and terahertz range. With our approach, the costs associated with testing are far less than this.

We have built our 220 GHz PA using a cascode topology. We arrived at this decision after considering the footprint of the HBT PA cell and the wiring layout. By taking this approach, we

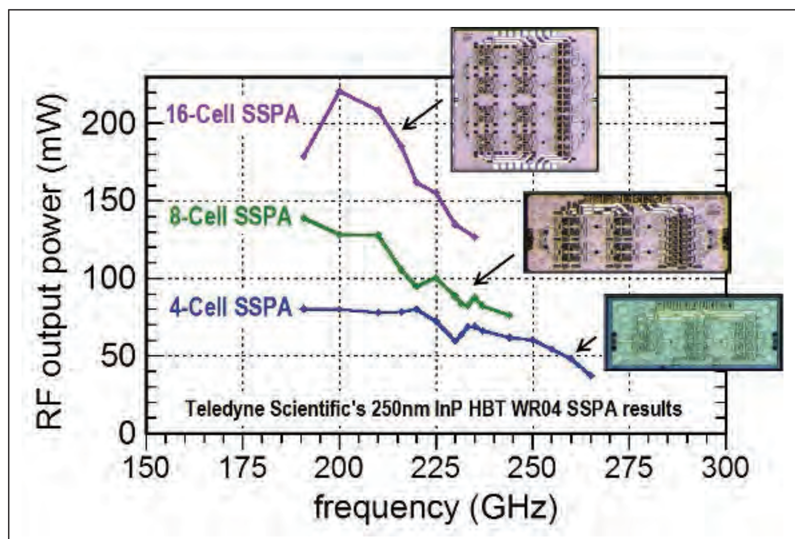


Figure 7. A performance summary of output power across frequency for Teledyne's 250 nm InP HBT WR04-band solid-state PAs.

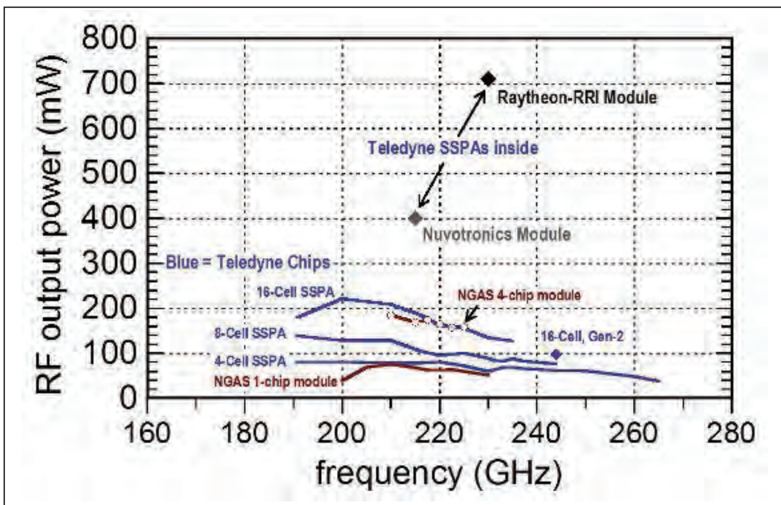


Figure 8. A performance summary of state-of-the-art PAs at the MMIC die and module-level. The modules from Raytheon and Nuvotronics will be presented as part of the technical program for the International Microwave Symposium 2015, held in Phoenix, AZ.

can ensure that the PA is stable and will allow an increase in power by combining monolithically up to 16 PA cells on a single chip. This level of integration is possible because interconnect loss is only 1.1 dB/mm, while the 2:1 and 4:1 combiners have insertion losses of just 0.45 dB and 0.5 dB, respectively (see Figure 4 for an example, a three-stage amplifier based on four cells).

Our three-stage, 4-cell amplifier delivers a very impressive level of performance, including a gain in excess of 28 dB from 205-271 GHz (see Figure 5). At 220 GHz, this gain is a record-breaking 35 dB. Output power peaks at 80 mW at 220 GHz; and it is 56.0 mW at 250 GHz and 46.5 mW at 260 GHz – these are the first reported data points greater than 15 mW for a solid-state PA at these frequencies. Even higher powers are possible with a three-stage amplifier formed from 16 cells, made from a stack of four 4-PA cells united with 2:1 combiners. Creating a MMIC using 1.41 mm of HBT led to the highest power G-band 220 GHz MMIC demonstrated to date. Output is 208.7 mW at 210 GHz, and while a power-added-efficiency of 3.4 percent may seem low, it is respectable given that at this high output power the large-signal gain of the amplifier exceeds 13 dB (see Figure 6 for details of performance, and Figure 7 for a summary of the output powers of 4-, 8-, and 16-PA cell combined amplifiers targeting 220 GHz).

Thanks to DARPA's sponsorship, we are now seeing our 220 GHz amplifiers based on 250 nm InP DHBT technology leaving the lab in volume levels to construct Watt-level solid-state power amplifier modules operating at 210-230 GHz (see Figure 8). This milestone, and the 'productization' of the G-band MMIC, indicates that the InP HBT is well-positioned to address MMIC requirements that will spur commonplace G-band and terahertz systems.

The views expressed here are those of the authors and do not reflect the official policy or position of the Defense Advanced Research Projects Agency or the United States Department of Defense. The work presented here was sponsored by DARPA under the following programs: TFAST (N66001-02-C-8080), FLARE (N66001-02-C-2025), HiFIVE (W911NF-08-C-0500), THz Electronics (HR0011-09-C-060), Mobile HotSpots (FA8750-12-C-0279), as well as HR0011-13-C-0013 and HR0011-13-C-0015. The authors sincerely thank all of the Program Managers of these programs for their support.

Further reading

J. Hacker *et. al.* "InP HBT Amplifier MMICs Operating to 0.67 THz", Proc. IEEE MTT Int. Microwave Symposium, Seattle, WA, June 3-6, 2013

Z. Griffith *et. al.* "Multi-finger 250 nm InP HBTs for 220 GHz mm-Wave Power", Proc. Indium Phosphide and Related Materials Conference, Santa Barbara, CA, August 26-30, 2012

M. Seo *et. al.* "A 220-225.9 GHz InP HBT Single-Chip PLL", Proc. IEEE Compound Semiconductor IC Symposium, Kona, Hi, Oct. 16-19, 2011

Z. Griffith *et. al.* "A 50-80 mW SSPA from 190.8-244 GHz at 0.5 mW Pin", Proc. IEEE MTT Int. Microwave Symposium, Tampa, FL, June 1-6, 2014

Z. Griffith *et. al.* "A 23.2 dBm at 210 GHz to 21.0 dBm at 235 GHz 16-way PA-cell combined InP HBT SSPA MMIC", Proc. IEEE Compound Semiconductor IC Symposium, La Jolla, CA, Oct. 19-22, 2014

D. Gritters *et. al.* "200-260 GHz Solid-State Amplifier with 700 mW of Output Power", to be presented at the IEEE MTT Int. Microwave Symposium, Phoenix, AZ, May 17-22, 2015

H. Kazemi *et. al.* "350 mW G-band Medium Power Amplifier Fabricated through a New Method of 3D Copper Additive Manufacturing", to be presented at the IEEE MTT Int. Microwave Symposium, Phoenix, AZ, May 17-22, 2015

Teledyne 190-245 GHz SSPA MMIC product: http://www.teledyne-si.com/ps-mmic-power-amplifier.html

 Copyright Compound Semiconductor

Improving p-type nitrides

A novel form of MBE known as metal-modulated epitaxy could improve the performance of LEDs, transistors and solar cells, by delivering a breakthrough in p-type doping.

BY BRENDAN GUNNING AND ALAN DOOLITTLE FROM GEORGIA INSTITUTE OF TECHNOLOGY

SALES OF III-NITRIDE CHIPS are soaring, and will continue to do so as new power electronics and RF products flood the market. However, this commercial success should not obscure a major weakness in the III-nitride device portfolio – realizing high-levels of *p*-type doping. Even in state-of-the-art devices, hole concentrations are limited to the low-10^{18} cm^{-3} range, a doping level that is trivial to reach in traditional III-Vs.

Poor *p*-type doping cannot be taken lightly, because it holds back the performance of every leading III-nitride device. In LEDs, it is to blame for weak hole injection, as well as high series and contact resistances; and in HBTs, which have the potential for massive power handling for RF applications, it is the cause of high base and base access resistances. Meanwhile, when it comes to solar cells, the lack of a *p-n* tunnel junction hampers the development of multi-junction cells providing strong absorption over a very wide spectral range. So it is clear that if III-nitride devices are to continue to evolve, improvements in *p*-type doping are essential.

The workhorse for the manufacture of III-nitride devices is the MOCVD reactor. Engineers operate this at temperatures of 900°C or more to ensure sufficient cracking of the source of nitrogen, the ammonia precursor. Such high temperatures are a double-edged sword, ensuring high crystal quality but also making *p*-type doping challenging.

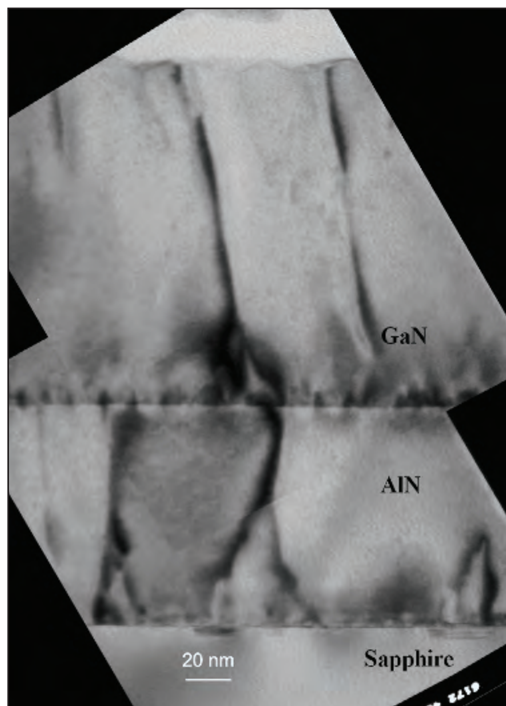


Figure 1. A transmission electron microscope image reveals the absence of inversion domains and magnesium precipitates in *p*-type GaN films grown by MME. Magnesium concentration is 2.6×10^{20} cm^{-3}.

These *p*-type doping issues are associated with the high density of point defects, such as nitrogen vacancies that compensate the magnesium acceptor. If high levels of magnesium doping are introduced, the nitrogen vacancy is even more energetically favourable – and this is disastrous, because it forms an electrically inactive complex

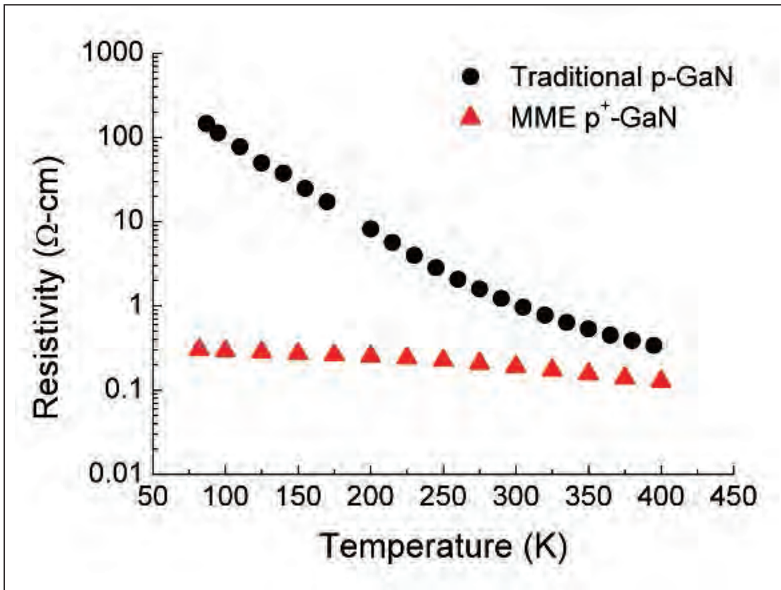


Figure 2. Temperature-dependent resistivity of traditional *p*-type GaN (black circles represent a hole concentration 2.2 x 10^{18} cm^{-3} at 300K) and highly magnesium-doped *p*-type GaN grown by MME (red triangles, represent a hole concentration of 1.9 x 10^{19} cm^{-3} at 300K).

with the magnesium dopant. What's more, at high magnesium doping levels, crystal quality tends to degrade, due to the combination of inversion domains and magnesium precipitation, which can even result in cubic inclusions and stacking faults.

Adding to the list of drawbacks, the hydrogen-rich atmosphere employed for MOCVD growth produces Mg-H complexes that lead to highly resistive *p*-type films in the as-grown state. A post-growth annealing step is needed to address this, with Mg-H complexes broken to yield conductive, *p*-type films.

Circumventing some of these problems is MBE. The two common forms of this growth technology, plasma-assisted MBE and ammonia MBE, use substantially lower substrate temperatures that typically range from 600 °C to 900 °C. Thanks to this, vacancies are less energetically favourable, magnesium incorporates more freely, and films can be conductive and measurably *p*-type without post-growth annealing steps, simplifying fabrication processes and reducing the thermal budget.

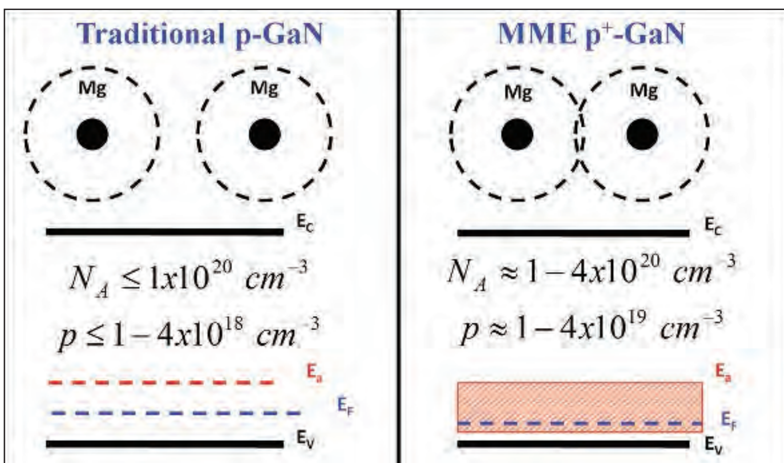


Figure 3. The Bohr orbital overlap results in acceptor band formation for highly magnesium-doped GaN (right), compared to the traditional isolated acceptor for lower magnesium concentrations (left).

However, turning to traditional MBE is by no means a perfect solution. Inversion domains are still an issue for magnesium concentrations of 5 x 10^{19} cm^{-3} or more at growth temperatures of 700 °C to 750 °C, and this places an upper bound on hole concentrations of the low-10^{18} cm^{-3} range.

So, to sum up, mediocre *p*-type doping is a thorn in the side of MOCVD and traditional MBE techniques. So what is the way forward? Well, certainly not higher temperatures, because this regime has been exhaustively explored already. Turning to lower temperatures might pay dividends, however, and it is there that our team from Georgia Institute of Technology believes that the most significant advances can be made.

Going down in temperature

We have been investigating growth at lower temperatures for several years. One of our first breakthroughs has been to demonstrate magnesium concentrations of greater than 10^{20} cm^{-3} in films of GaN that are free from inversion domains and magnesium precipitation. This involved the use of low-temperature, plasma MBE under nitrogen-rich conditions, which resulted in rough surfaces and poor crystal quality.

To address these weaknesses, we then moved to a variant of MBE that is known as metal-modulated epitaxy (MME). With this approach, growth of nitrides at around 600 °C involves periodic opening and closing of shutters for the group III and dopant sources, while the nitrogen plasma continuously impinges on the surface. When the metal shutters are open, the incident metal flux exceeds that for nitrogen, with excess metal accumulating on the surface; and when the metal shutters close, nitrogen, which continues to flow, consumes this excess metal.

It is important to realise that the liquid metal that is formed on the surface by this process is not fixed in position, but moves freely in a highly mobile pool. This produces two favourable outcomes: large diffusion lengths for both metals and nitrogen and thus, very smooth films. However, if there is no excess metal on the surface, the incoming metal atoms fail to migrate far enough, resulting in rougher films. Note that an excess of metal is particularly important for ensuring smooth films at low temperatures, because atom diffusion lengths are shorter in this growth regime.

Turning to MME has enabled us to produce *p*-type GaN films at 600 °C that have magnesium concentrations exceeding 2 x 10^{20} cm^{-3} and an

absence of inversion domains and magnesium precipitation (see Figure 1). According to Hall measurements, the hole concentration of this particular film shown in Figure 1 is 4.5×10^{19} cm^{-3}. That is not our best result, however, as we have formed films with a hole concentration as high as 7.9×10^{19} cm^{-3} and a resistivity below 0.2 Ω-cm. Although under certain growth conditions this hole concentration contains a small contribution to the charge density from a polarization induced charge at the interface between the *p*-type layer and the AlN buffer layer, this makes a small contribution to the *p*-type doping, which has a level that is more than an order of magnitude higher than that found in today's commercial III-nitride devices. Most of the hole conduction is via impurity band conduction not 2D hole gas conduction.

When we select MME growth conditions for highly *p*-type GaN, we are now able to routinely produce hole concentrations of $1\text{-}3 \times 10^{19}$ cm^{-3}, alongside a resistivity of 0.2-0.4 Ω-cm, for 100 nm-thick films held at room temperature. Mobility is just 0.5-5 $cm^2 V^{-1} s^{-1}$, but that is to be expected, given the extremely high magnesium concentration, which results in substantial ionized impurity scattering and a mobility dominated by an impurity band, rather than being governed by the valence band.

The characteristics of these films at cryogenic temperatures are very encouraging. There is minimal carrier freeze-out, with hole concentrations of $8\text{-}9 \times 10^{18}$ cm^{-3} near 77K, and conductivity is retained, with a resistivity of less than 0.5 Ω-cm (see Figure 2). In comparison, traditional *p*-type GaN films are resistive at 77K, with hole concentration plummeting with temperature.

Formation of an impurity band accounts for the lack of carrier freeze-out in these *p*-type GaN films with a magnesium concentration exceeding 10^{20} cm^{-3}. In a traditional *p*-type GaN film with a lower magnesium concentration, acceptors are isolated, rather than being close enough to interact. But when the acceptor concentration exceeds 10^{20} cm^{-3}, the Bohr radii of the holes overlap, allowing magnesium acceptors to interact and form a band, rather than a single acceptor energy within the band gap (see Figure 3).

This switch from a single acceptor energy to a band leads to an increase in ionization efficiency, because the lower part of the band gets closer to the valence band, lowering the effective activation energy of the magnesium acceptor. Such a situation is well known in highly doped traditional III-V semiconductors, and accounts for the change in carrier freeze-out in these materials. We have also obtained photoluminescence spectra from films with a high level of magnesium doping to provide further evidence for the formation of an acceptor band. Spectra from a 100 nm-thick film with a room temperature hole concentration of 5.8×10^{19} cm^{-3} feature a 3.28 eV peak with a full width at half maximum of 240 meV. Of particular interest is the high-energy tail of the peak, which intercepts the band edge. This overlap, and the broad width of the photoluminescence, is consistent with the formation of a broad impurity band. The spectra are indicative of high-quality material, as there are no signs of yellow or other deep level defect luminescence.

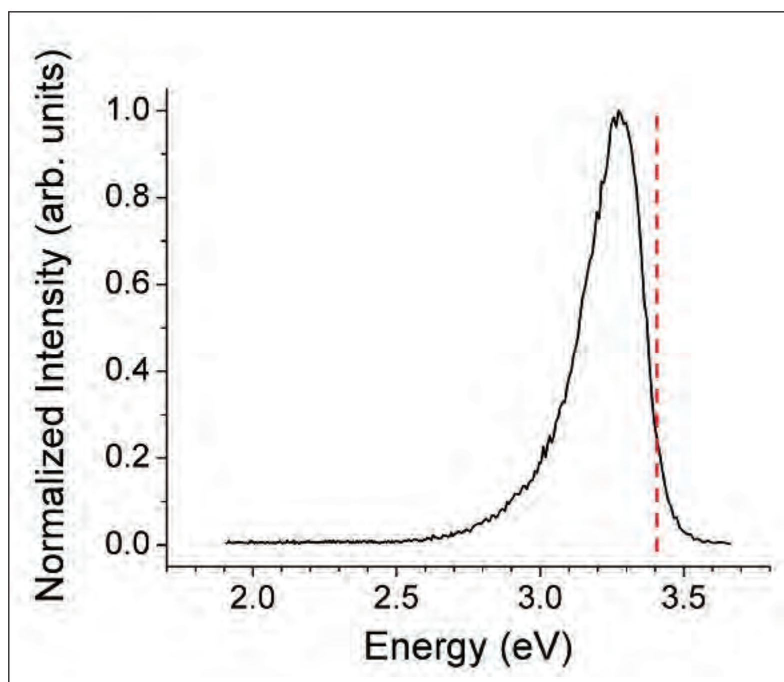


Figure 4. Room temperature photoluminescence spectrum of highly magnesium-doped GaN grown by MME exhibits only a broad, ultraviolet emission that crosses the valence band edge marked by the dotted red line.

To demonstrate the capability of our MME technology more fully, we have grown several *p*-type AlGaN films on AlN templates. Using growth temperatures of 620 °C and 640 °C, we have grown 100 nm-thick films with compositions of $Al_{0.11}Ga_{0.89}N$ and $Al_{0.27}Ga_{0.73}N$, respectively. Both ternaries exhibit highly *p*-type conduction with hole concentrations of approximately 2.6×10^{19} cm^{-3}. Resistivity is just 0.3 Ω-cm in the $Al_{0.11}Ga_{0.89}N$ film, rising to 1 Ω-cm in the $Al_{0.27}Ga_{0.73}N$ variant, due to reduced mobility.

We have also investigated the photoluminescence produced by the $Al_{0.11}Ga_{0.89}N$ film (see Figure 5). Its spectra has similar characteristics to that produced by the GaN film, with a broader peak that again intercepts the valence band edge.

Building prototypes

To determine whether this highly *p*-type material is viable for making devices, we grew a very basic, non-optimized LED and a *p-i-n* diode. The LED features 2 nm-thick $In_{0.13}Ga_{0.87}N$ wells separated by 10 nm-thick unintentionally doped GaN barriers, and also a 20 nm thick *p*-type $Al_{0.1}Ga_{0.9}N$ electron

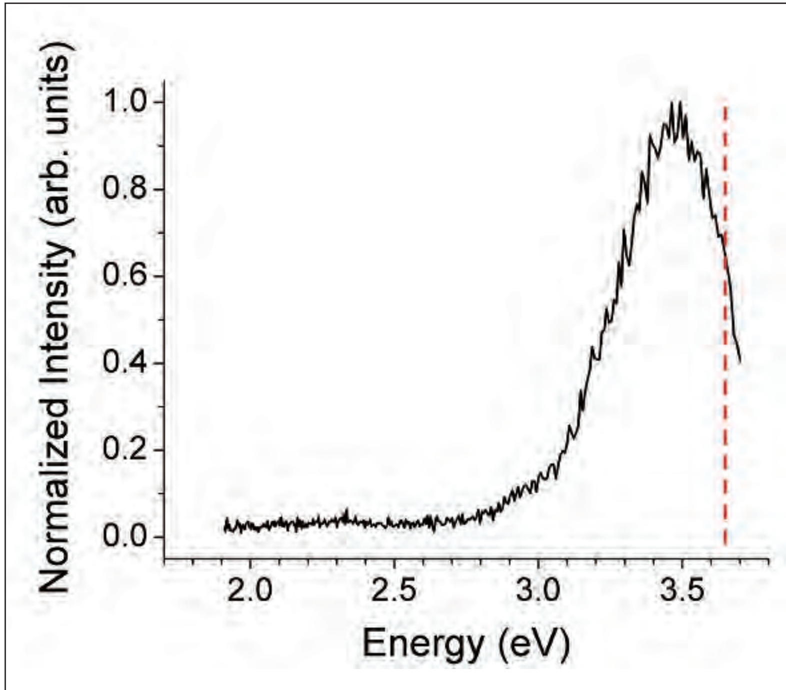


Figure 5. Room temperature photoluminescence spectrum of *p*-type $Al_{0.11}Ga_{0.89}N$ grown by MME. A broad ultraviolet emission (the full-width at half-maximum is nearly 440 meV) is seen and the high energy tail intercepts the band edge marked by the dotted red line.

blocking layer and a 50 nm thick *p*-GaN contact layer. Both of the *p*-type layers in this device were grown using conditions similar to those described above, and lead to hole concentrations that are typically greater than 2 x 10^{19} cm^{-3}. Meanwhile, the *p-i-n* diode comprised only GaN, with an intrinsic region just 20 nm thick, followed by 50 nm of GaN that is highly doped with magnesium.

Current-voltage measurements on both of these 660 μm-diameter devices revealed a proper-turn on at around 3 V, and a series resistance of 6 Ω for the *p-i-n* diode and 10 Ω for the LED. Note that these values are for devices subjected to no annealing whatsoever; there was no post-growth anneal, nor any contact anneal during or after device fabrication, owing to the extremely high doping of the films.

Operating at room temperature, peak emission from the LED occurs at 425 nm, while that for the *p-i-n* diode is at 381 nm. Emission at this latter wavelength has been seen in photoluminescence measurements on GaN (see Figure 4), indicating that it probably originates from recombination within the *p*-type layer. A broad visible luminescence also emanates from this *p-i-n* diode, and this is not seen in any GaN grown by MME, regardless of doping. We believe this emission results from hole injection into the *n*-type region and subsequent diffusion through the 200 nm MME-grown *n*-type region into the underlying MOCVD-grown GaN template.

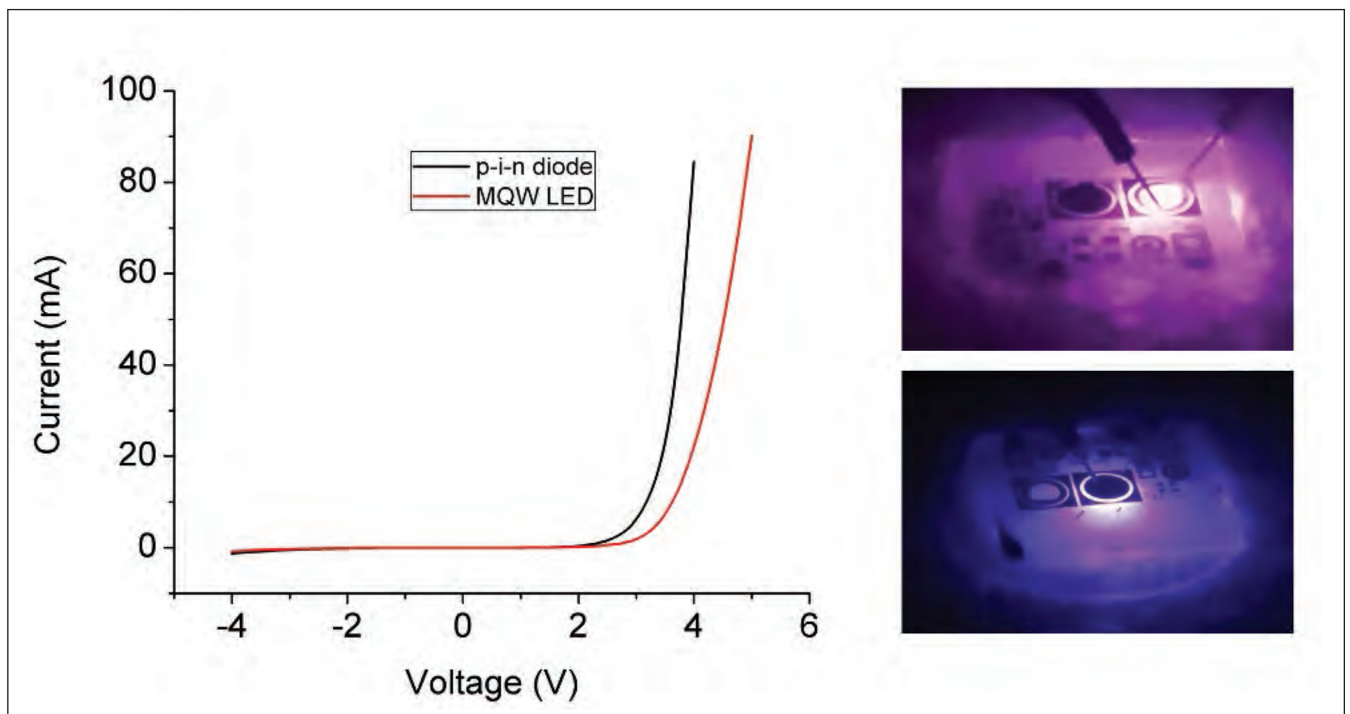


Figure 6. Current-voltage curves (left) for non-optimized *p-i-n* diode (black) and LED (red), and images of both devices operating while submerged in liquid nitrogen (*p-i-n* diode is top right, LED is bottom right).

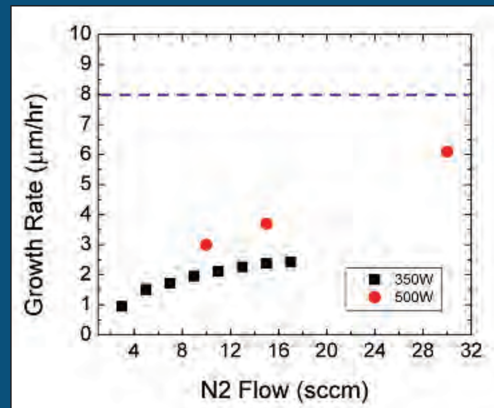
 Copyright Compound Semiconductor

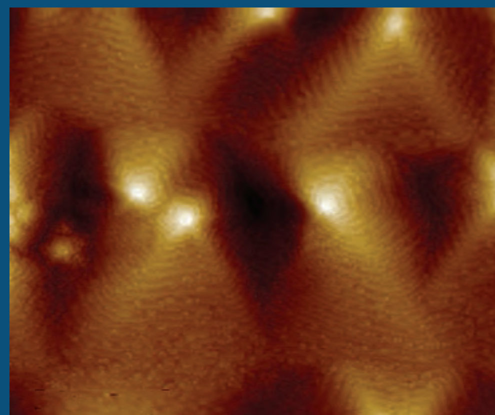
Record GaN growth rates

A PARTNERSHIP between the group at Georgia Tech and Veeco is claiming to have broken the record for MBE growth rates for GaN. This team has deposited films at up to 8 µm/hour using a high water flow UNI-Bulb RF plasma source. A modified high-conductance aperture plate allows for higher nitrogen flow and increased growth rate, while added pumping capacity results in lower chamber pressures and acceptable effusion cell lifetime compared to other efforts.

By combining a splayed aperture, a nitrogen flow of 30 sccm and an RF power of 500 W, the researchers could deposit films with a typical growth rate of 6 µm/hr. These epilayers feature a uniformity of around 2 percent over a 2-inch wafer. Increasing the growth rate to 8 µm/hour, using a chamber pressure of 6 x 10^{-5} Torr, resulted from a modification that will shortly be revealed in a paper.

This new record growth rate represents more than an order of magnitude increase compared to typical MBE GaN growth rates, and proves the scalability of GaN MBE for production. Altering growth conditions by switching to nitrogen flows of just 3 sccm and RF power of 350 W reduced growth rates to around 1 µm/hour. So, in other words, growth rates can be varied by almost an order of magnitude (see Figure 1). Most importantly, across this range films remain smooth with step-flow growth and clear atomic steps, even for epilayers grown at a low substrate temperature of 600 °C and at a growth rate of 6 µm/hour (see Figure 2).





Top right: Figure 1. Growth rate of GaN with varied nitrogen flow for RF power of 350 W and 500 W.
Bottom Right: Figure 2. 2 µm by 2 µm atomic force microscopy scan showing smooth, step-flow growth with root-mean-square roughness less than 1 nm (height scale of 7 nm).

The lack of carrier freeze out in our MME-grown GaN allows devices to emit light at cryogenic temperatures. Both types of devices can emit light while submerged in liquid nitrogen, indicating the presence of sufficient hole concentrations at 77K (see Figure 6).

These results on preliminary devices illustrate the promise of highly *p*-type material. It offers a hole concentration that is nearly 30 times that of the previous state of the art, and is a breakthrough that might seem to good to be true – it has been accompanied by some justifiable scepticism. Hopefully, however, the naysayers will be persuaded that these films have great *p*-type performance, thanks to demonstration of properly rectifying devices exhibiting electroluminescence, even at cryogenic temperatures, and the formation of ohmic contacts without contact annealing.

There is still a long way to go, despite our successes to date. Our devices are certainly not state-of-the-art – in either design or operation – and the function that they fulfil is to simply demonstrate the viability of this highly *p*-type material for device applications.

On top of this, they also suggest that there is a need to revisit MBE as a tool for making green/and ultraviolet LEDs. After all, in addition to producing great *p*-type film, this growth technology offers benefits of low temperature growth, such as high indium incorporation, extremely high uniformity, high source material utilization, and excellent interface and dopant diffusion control. And GaN growth rates are comparable to MOCVD, with deposition at more than 8 µm/hour – while for InGaN, MBE can top 1 µm/hour, enabling faster growth than that occurring in an MOCVD tool.

Further reading

B. Gunning *et. al*. Appl. Phys. Lett. **101** 082106 (2012)
B. Gunning *et. al* J. Appl. Phys. **17** 045710 (2015)
M. Moseley *et. al* J. Appl. Phys. **112** 014909 (2012)
M. Moseley *et. al* Appl. Phys. Lett. **97** 191902 (2010)
A. M. Fischer *et. al* Appl. Phys. Lett. **103** 131101 (2013)

Intense infrared LEDs

Perfected packages housing advanced emitters are yielding brighter, more efficient sources

BY MARTIN BEHRINGER, MARKUS BRÖLL, JÖRG HEERLEIN, CLAUS JÄGER AND THOMAS KIPPES FROM OSRAM OPTO SEMICONDUCTORS

THERE ARE PARALLELS between what is happening in the mainstream LED industry and that associated with the 850 nm chip, which emits at wavelengths far enough into the infrared to be virtually invisible to the human eye. Both the visible and the infrared classes of chip can serve myriad applications, and makers of these emitters are trying to set a new benchmark for performance to win sales in new markets.

For the 850 nm LED, one of the biggest markets is providing illumination for infrared cameras, which can be used for the likes of various forms of surveillance, license plate recognition and industrial image processing. In addition, the infrared LED can be deployed in 3D systems and biometric identification – all these applications are outlined in more detail in the panel "Opportunities for infrared LEDs".

To address all these applications, our team of engineers at Osram Opto Semiconductors launched infrared LEDs and subsequently expanded this portfolio. We have many sources operating at 850 nm, an ideal wavelength for infrared cameras and gesture-recognition, and we have also brought to market a cousin emitting at 810 nm, designed to deliver more reliable results for iris scanning.

In 2008, we brought our first 850 nm high-power LEDs, housed in the Dragon package, to market. Since then we have increased output at 1A from 440 mW to 800 mW (see Figure 1). Even high powers are possible with our nanostack technology, which we have developed in-house. By turning to two emitters per chip, single-chip LEDs can exceed an output of 1W by a significant margin.

Of all the gains in output over the last six years, the greatest hike came in 2014, with the introduction of the Oslon SFH 4715A (see Figure 2). This boosted the emitted power by 30 percent, with new developments in chip technology accounting for two-thirds of the increase and the remainder resulting from refinements to package design. Another attribute of this particular chip is a 48 percent electrical efficiency, defined in terms of electrical input to optical output. This level of efficiency makes the SFH 4715A the most efficient infrared power LED on the market at a 1A drive current.

This record-breaking LED and its predecessors are based on an AlGaInAs thin-film technology (see Figure 3). This architecture is superior to that of a conventional chip, and delivers two major benefits: far less light is absorbed in the chip, enhancing optical output; and emission occurs from almost all of the top surface of the LED, eliminating the need for reflectors within the package. With this design, the area of this surface is proportional to the output from the chip – for our high-power devices we use a surface of 1 mm^2.

One defining feature of our thin-film technology is the highly reflective dielectric mirror between substrate and light-emitting region. To create such a structure, the light-absorbing substrate is removed after epitaxial growth, and is replaced by a new carrier and mirror (see Figure 3). Turning to this geometry lowers light absorption, but radiation can still be trapped in the chip, bouncing back and fourth between the mirror and the surface. So, to enhance extraction, the surface of the chip is roughened to increase light output.

The spectral width of our 850 nm LEDs is relatively narrow. This

Right: Powerful illumination for optimum image quality. Applications such as video surveillance of public places call for infrared LEDs with a wavelength of 850 nm and extremely high optical output.

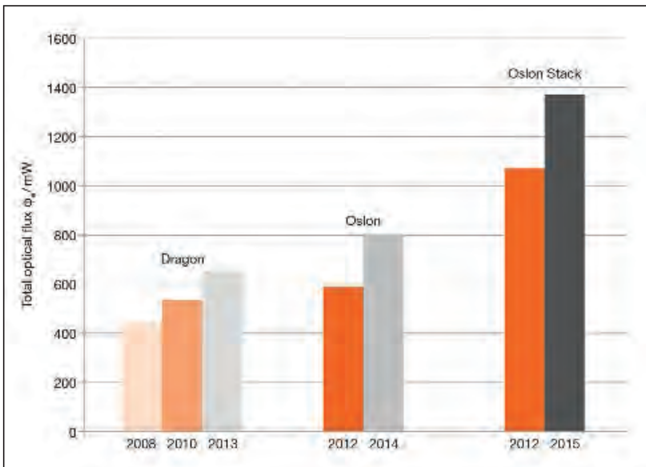


Figure 1. Since the launch of Osram's first 850 nm high-power LED in 2008, optical output has almost doubled, and even trebled, when stack chip technology is considered.

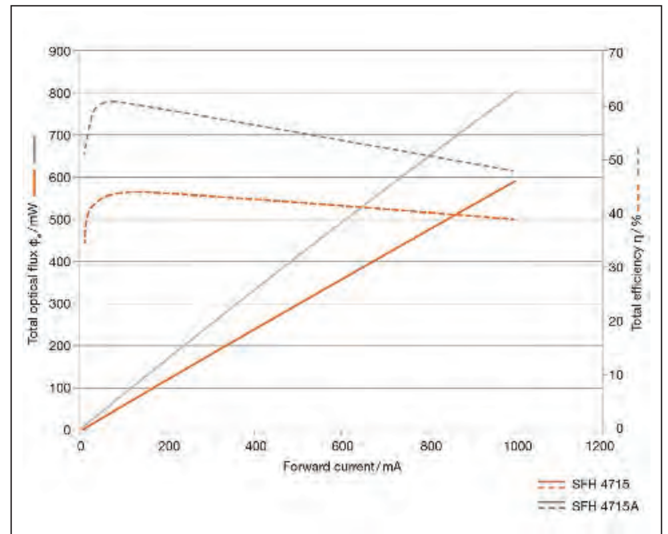


Figure 2. The optical output of the 850 nm emitter has been increased by 30 percent, and efficiency by 20 percent. Improvements in chip technology account for two-thirds of this increase, with the remainder resulting from an improved package.

is intentional: With the half-value width of the emission peak at just 30 nm, the lower wavelength tail cannot deliver visible illumination (note that only 4 percent of peak output occurs at 800 nm, implying that the latest chips do not produce any red glimmer detectable to the human eye).

Over the last few years we have devoted much effort into increasing the current-handling capability of our high-power LEDs. One goal has been to develop components that could be driven by either 5 A pulses or a DC current of 1 A. After realizing this by trimming substrate thickness and consequently thermal resistance, the target for our latest generation of thin-film chips has been to retain this current-handling capability while delivering high efficiency, especially when the LED is driven in DC mode.

These efforts have not involved reducing the light path, as this is already as short as possible, thanks to the roughened surface. Instead, there has been a cutting of the internal absorption of the epitaxial layer and an increasing of the reflectivity of the mirror between the substrate and the epitaxial layers. On top of this, by reducing the area of the *p*-type contacts, we have minimized absorption losses at the metal-semiconductor boundary.

Making these electrical and optical refinements has driven up device performance. Brightness, measured with a chip mounted in a silicone-encapsulated package without a lens, is up 25 percent. The smaller surface of the *p*-contacts impairs forward voltage, which rises by 7 percent at 1 A, but the key figure of merit is an 18 percent increase in electro-optical efficiency. Testing in a lab produces impressive results, including a record efficiency of 72 percent at 70 mA for a chip with a mounted lens. Optical output can hit 930 mW at 1A, and when mounted in our Oslon package, the latest 850 nm thin-film flip chip provides a 10 percent increase in efficiency and a 20 percent hike in output compared to its most recent predecessor.

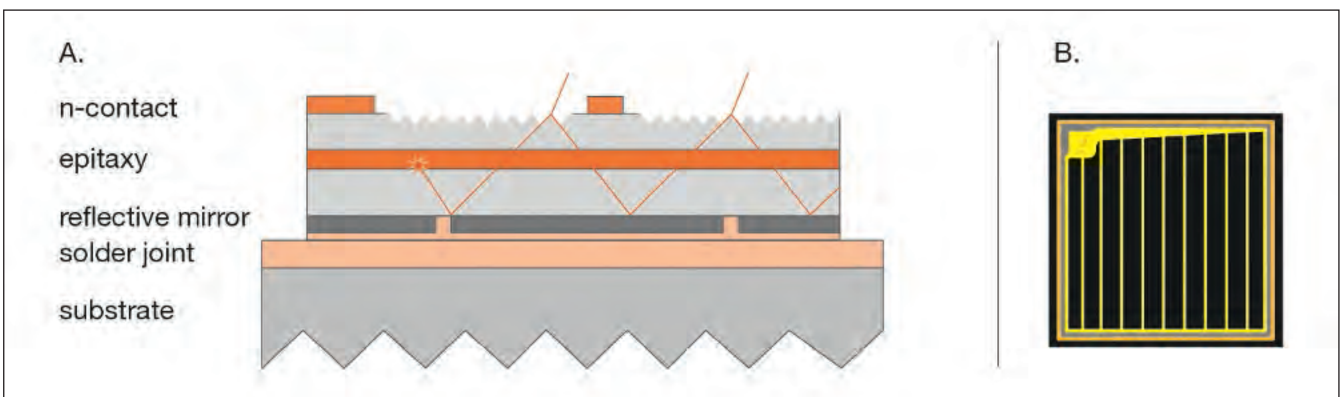


Figure 3. Thin-film chip technology: A highly reflective mirror between the substrate and the epitaxial layer prevents light being absorbed by the carrier; a roughened surface extracts the light efficiently (a). Thanks to improvements in the mirror, at the *p*-contacts and in the epitaxial layers, the optical output of the chip (measured in the package) has been increased by 20 percent (b).

Reasons to sponsor CS International Conference 2016

- ✓ Senior management networking opportunities
- ✓ Increased company and brand awareness
- ✓ Access to the top strategists within the compound semiconductor industry
- ✓ Create, develop and support customer relationships
- ✓ Engage in debate, share insight and expertise on industry challenges
- ✓ Gain visibility and recognition as an industry leader
- ✓ Leverage exposure in multiple industry media
- ✓ Demonstrate market innovation and leadership by launching new services, products and systems

www.cs-international.net

CALL NOW +44 (0)24 76718970
email **event@cs-international.net** or view the online sponsorship pack at **mediapack.cs-international.net**

CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry

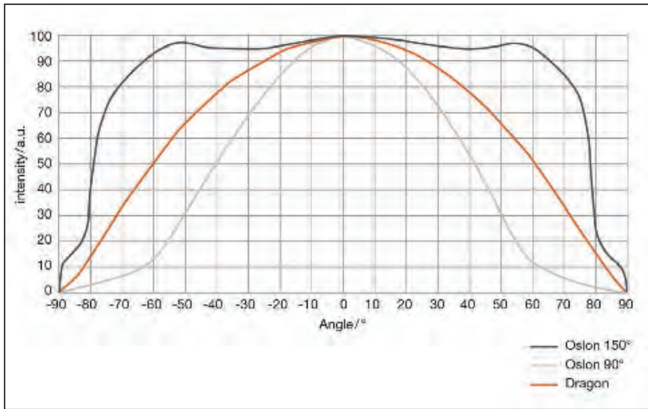


Figure 4. Angular distribution of the optical output of the Oslon Black series for a beam angle of ±45° and ±75° compared to a Lambertian emitter (± 60°) in the Dragon package. The Oslon Black series is one of the most compact designs for infrared LEDs with an optical output of more than 500 mW. It has been used by Osram for high-power LEDs of all colours and chip technologies, and by employing a silicon lens specially adapted to the package and the chip, it can emit around 15 percent more optical output than a comparable low-profile LED, such as the Dragon. Other strengths of this package are good heat dissipation, which ensures that the chips are highly resistant to aging, and a low thermal resistance of typically 6.5 K/W that is optimised for continuous operation with high currents.

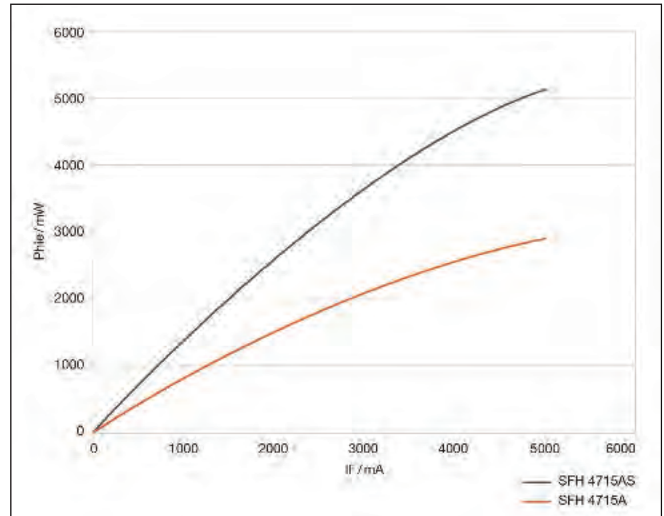


Figure 6. The output of the 850 nm Oslon Black remains virtually linear for moderate pulse lengths of 100 μs up to a current of 5 A.

Another of our improvements is to optimize the *n*-contact of our new chip for continuous current and high efficiency. This involved switching from a centrally located bond pad to a contact in the corner, with current distribution via a thin metal grid (see Figure 3). The new geometry eliminates the bond wire from the optical path, allowing more uniform illumination to be delivered by the chip.

Perfecting the package

An additional 10 percent increase in optical output has been driven by improvements to the package. This was accomplished by changing the material composition of the silicone lens in the Oslon Black series. Results are an increase in output efficiency and a trimming of scatter losses. This has led to the release of improved Oslon Black sources with two different options for the lens: beam angles of ±45° or ±75° (see Figure 6).

The narrow beam angle is suited to coupling to external lenses, allowing the resultant beam angle to be shaped to suit the particular application.

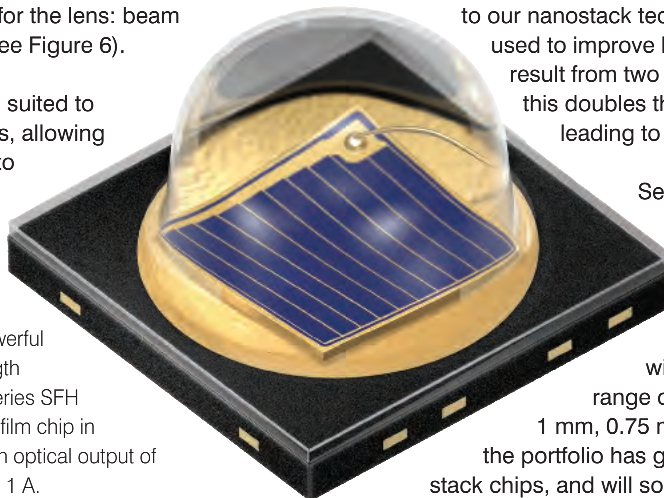


Figure 5. One of the most powerful infrared LEDs with a wavelength of 850 nm: the Oslon Black series SFH 4715AS features a 1mm^2 thin-film chip in stack technology and emits an optical output of around 1370 W at a current of 1 A.

Meanwhile, the ±75° version enables far broader illumination in the near field over distances of only a few meters, making it well suited to gesture recognition. This option is also ideal for forming compact designs that realise very narrow-angle emission characteristics, thanks to reflector-based optics that fill the reflector with light, due to the wide emission of the +/-75° design. Such a source can produce a narrow light beam for sending light over long distances.

Our latest version of the infrared Oslon Black features the latest-generation chip, which is distinguishable by the contact in the corner (see Figure 5). This particular design is ideal for optical imaging applications, because the bond wire and contact are no longer in the centre of the beam, thereby eliminating interference effects from the detected light signal. Turning to the combination of the Oslon package and the latest thin-film flip chip increases current electro-optical efficiency by 20 percent at 1 A and optical output by 30 percent.

Setting up a stack

To squeeze even more light out of our chips, we have turned to our nanostack technology, which we have previously used to improve laser diode performance. Brighter chips result from two *p-n* junctions in the epitaxial layer, as this doubles the number of regions generating light, leading to a higher total output.

Several years ago we transferred our stack technology from laser diodes to infrared LEDs, and this increased output from the component by 70 percent (see Figure 7). In 2009, we started to offer 850 nm LEDs with our chip stack technology on a range of LEDs – those with edge lengths of 1 mm, 0.75 mm, 0.3 mm and 0.2 mm. Since 2013, the portfolio has grown to include large-format 940 nm stack chips, and will soon include the SFH 4715AS, a latest-

 Copyright Compound Semiconductor

Opportunities for infrared LEDs

THERE ARE MANY commercial opportunities for the 850 nm LED.

One of the biggest markets for this device is the illumination of areas that can be captured by cameras fitted with CMOS or CCD sensors, which both have good sensitivity in the near infrared. Such a set-up is used in closed-circuit TV (CCTV), providing video surveillance of public spaces, museums, banks and industrial premises. Here chipmakers must offer a strong permanent infrared light source to ensure good image quality in low ambient light. However, when the camera is used outdoors, the requirements are more complex. In this case, the LED may have to allow the viewer to identify objects at distances of 100 m or more, so it must combine a very high level of brightness with high radiant intensity – that is, tremendous power per solid angle.

Makers of 850 nm LEDs are also selling devices that are used within infrared camera systems, including those that provide license plate recognition, access control and industrial image processing. In these instances, image data is evaluated in great detail, so high-quality images – realised by additional illumination – are absolutely essential. And on top of this, infrared camera systems may be used in different ways in cars. This includes active night vision driver assistance systems and attention assistants, which notify a driver that they are distracted or tired (this is possible by mounting a camera behind the steering wheel and monitoring the frequency with which the driver blinks).

The other big market for the makers of 850 nm LEDs is in 3D systems that measure the distance to an object, and thus record movement in all directions. A familiar example of this is gesture recognition for either gaming or controlling computers.

However, 3D cameras are also used in industry, where they might, for example, provide smart detection of objects on production lines; and there may come a time when they are used in cars, with gesture recognition providing control of the many different functions in the cockpit.

Additional examples related to distance monitoring are automotive safety systems that protect pedestrians from harm by detecting their movement.

Cameras based on time-of-flight and photonic-mixing may be used here in conjunction with an infrared light source. Two modes of operation are possible: for each pixel, timing the propagation of the light pulse from the source to the object and back to the detector; or modulating the light at 20 MHz or more, and measuring the phase shift of the signal. Development of the latter technology has hinged on the launch of high-power infrared LEDs.

On top of this, infrared LEDs can be used for biometric identification. Iris scanners can identify a person by illuminating the eye with infrared light, thereby providing another level of security for unlocking smartphones and tablets and withdrawing money from cash machines.

generation thin-film flip chip with stack technology that delivers 1370 mW at 1 A.

Another breakthrough associated with this product is that it is the first infrared thin-film chip on a silicon substrate. We have used this foundation for some time in our blue and green InGaN chips, but our infrared emitters have been traditionally mounted on a germanium substrate. Switching to silicon slashes the typical thermal resistance of 5.5 K/W by around 1K/W, and thus reduces the rise in LED temperature, allowing these devices to be driven at higher currents before they hit the maximum allowed operating temperature. Alternatively, the component can be run under the same operating conditions as before, as this will make it more efficient and longer lasting than its predecessor.

Our plans for the future include increasing the range of wavelengths of devices exploiting our new generation of thin-film technology, so that we increase the portfolio of higher power, more efficient products. These high-power infrared chips will migrate to a silicon substrate, with packages further optimized for operation at high currents. We will also listen to our customers, and if there is demand for new versions of infrared LEDs with different emission angles, we will bring such devices to market. The opportunities for this class of LED appear to be endless, and we will continue to innovate and set new benchmarks for these infrared emitters.

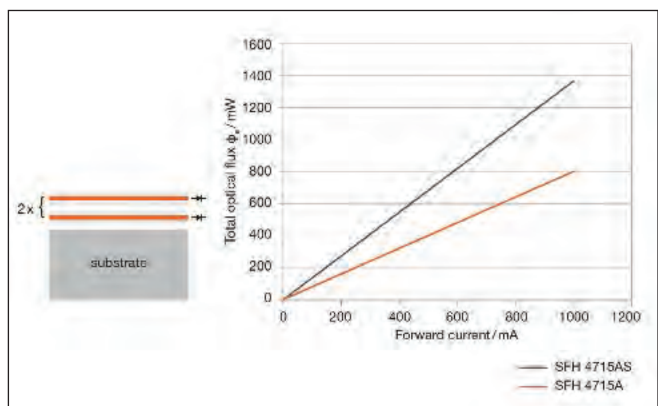


Figure 7. Nanostack chip technology features two *p-n* junctions in one chip. A component with a stack chip has an output that is 70 percent higher for the same forward current.

Further reading

M. Broell *et. al.*, New developments on high-efficiency infrared and InGaAlP light-emitting diodes at OSRAM Opto Semiconductors, SPIE Proceedings 9003 Feb. 2014

Angel
BUSINESS COMMUNICATIONS

IS EMAIL MARKETING DEAD?

DON'T BELIEVE IT! EMAIL MARKETING IS NOT DEAD, IT'S JUST EVOLVING

- 94% of adults check their email every day
- 74% of online adults prefer email for commercial communication

Email is still the quickest and most direct way to reach customers with critical information. Why? Because email is the one channel your audience accesses regularly. **We consumers are addicted to email.**

EMAIL MATTERS MORE TODAY THAN EVER BEFORE, LET US HELP YOU TO TRANSFORM YOUR EMAIL MARKETING CAMPAIGNS.

Visit: www.angelbc.com/angelonline/email
E: sukhi.bhadal@angelbc.com T: +44 (0)24 76718970

Photoelectrochemical etch improves nitride lasers

Etching a current aperture with potassium hydroxide creates a more powerful laser that turns on at lower voltages

FOR THE MANUFACTURERS of nitride laser diodes, ridge etching offers a fair trade-off between performance and cost. But the selection of the etch depth involves compromise: if it is shallow, that is, it leaves a *p*-side waveguide thickness of 100 nm or more, a high lateral current leakage and optical mode instability in the waveguide will impair performance; but if it is deep, the benefits of a decrease in threshold current density, strong index guiding and a high slope efficiency must be weighed against the challenges of realising high etching quality and good thermal management.

This dilemma for makers of laser chips could soon disappear, however, thanks to recent work by researchers at the University of California, Santa Barbara (UCSB). They have revealed promising results for an alternative design of blue-emitting laser, featuring a current aperture formed by photoelectrochemical etching (see figure for chip architecture).

Ludovico Megalini, spokesman for the UCSB team, claims that one important aspect of this work is that it shows that selective lateral etching, in a controllable way, is possible in a complex nitride-based structure, such as a laser diode.

"We selectively etched an InGaN-based active region from GaN-based bottom and top epilayers, but this could be applied also to etch GaN layers from AlGaN-based bottom and top epilayers," explains Megalini.

According to him, the other big breakthrough of this work is that it shows how to make nitride-based optoelectronic devices – and eventually electronic devices – that deliver superior performance to those made with traditional dry etching techniques. "Reactive-ion etching and inductively-coupled-plasma etching are known to cause sub-surface damage to the epitaxial structure."

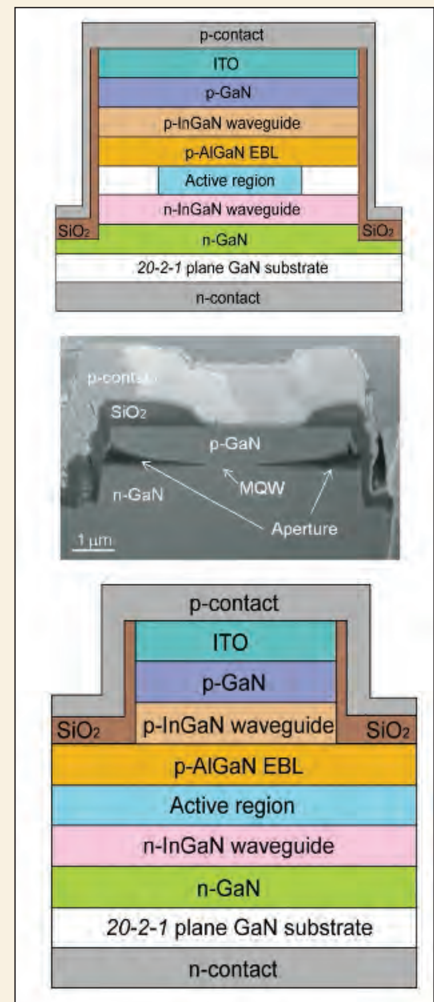
Megalini believes that another advantage of photoelectrochemical etching, which is an established technique for etching silicon and zinc blende III-Vs, is that it is not just a technique for the lab – it can be used for high-volume manufacturing. "Being a wet-etched based technique, photoelectrochemical etching does not require expensive dry etching tools, and in general it is low cost, easy to do, and doesn't involve hazardous gases, like chlorine."

The researchers at UCSB fabricated their novel laser by applying a photoelectrochemical etch to an epistructure with an InGaN/GaN active region formed on the $(20\bar{2}\bar{1})$ plane of GaN. To create the current aperture, they added an opaque metal mask. This blocked light needed to generate carriers during the photoelectrochemical etching step involving potassium hydroxide.

After etching, Megalini and co-workers formed 1800 μm stripe-length lasers with an 8 μm wide ridge width and an active region width of 2.5 μm. Comparisons were then made between this chip and a shallow-etched laser with an identical strip-length. This control had a *p*-GaN ridge width and active region width of 2.5 μm and an etch depth of 420 nm (the remnant *p*-side thickness is 220 nm).

Switching to this novel design wrought many improvements in performance: It cut series resistance from 6 Ω to 4.7 Ω, trimmed threshold current density from 8.1 kA cm^{-2} to 4.4 kA cm^{-2}, reduced threshold voltage from 7.6 V to 6.1 V, and increased slope efficiency from 0.07 W/A to 0.13 W/A.

Photoelectrochemical etching of the aperture to a narrower width resulted in further improvement. A device with a 1.5 μm-wide active region produced 15 mW, the highest single-mode CW output power for this type of laser.



Current aperture, edge-emitting blue laser diodes made using photoelectrochemical etching (top) differ from conventional designs (bottom)

One of the weaknesses of the photoelectrochemically etched lasers is their injection efficiency, which is just 65 percent. Much higher values should be possible, according to Megalini, who believes that nitride lasers produced by other groups may have injection efficiencies of 90 percent. To improve their lasers, the UCSB team will try to refine the design of the chip and reduce optical scattering from the rough edge of the device.

"I am working on both the material aspect – that is, I am trying to improve the general epitaxial structure of my laser diodes – and also on the fabrication side, trying to improve the photoelectrochemical etching technique," explains Megalini.

L. Megalini *et. al.*
Appl. Phys. Express **8** 042701 (2015)

Debut for epitaxial InGaPBi

Adding a little bismuth to InGaP creates a promising quaternary that allows tuning of bandgap and strain

RESEARCHERS from China are claiming to have grown a new III-V epilayer by incorporating bismuth into InGaP to form InGaPBi, a quaternary alloy that is nearly lattice matched to GaAs.

"[InGaPBi] provides a new building material to tune the bandgap and strain of InGaP on GaAs, and thus can be of significance for optoelectronic devices," argues corresponding author Shumin Wang, an academic at Shanghai Institute of Microsystem and Information Technology, Chinese Academy of Sciences, and also the holder of a position at Chalmers University of Technology, Sweden.

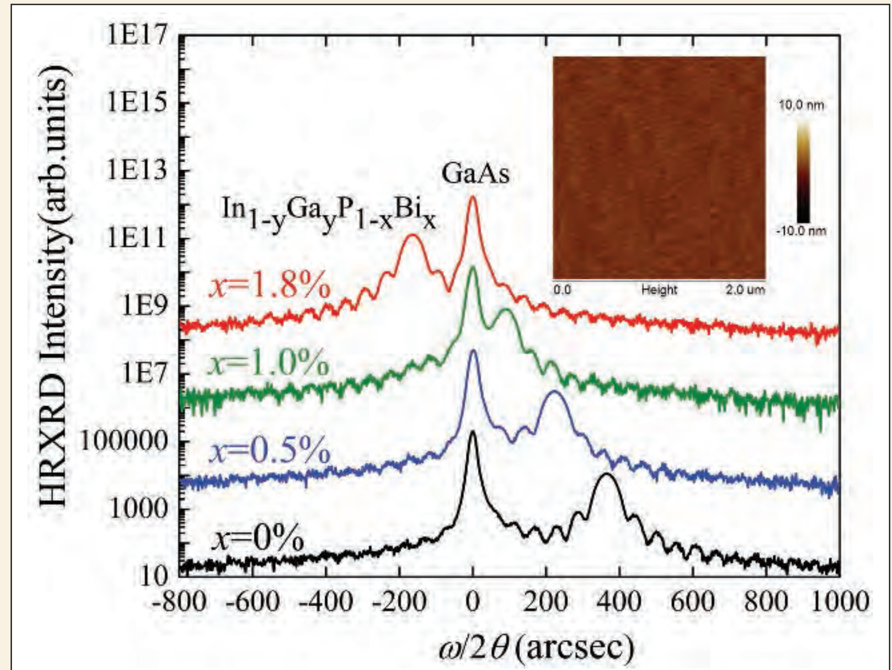
Adding bismuth to InGaP is expected to lead to a large change in bandgap. That is the case when bismuth is added to InP, with every percent of bismuth producing a 56 meV shift in bandgap.

One particularly interesting possibility, according to Wang, is that the characteristics of InGaPBi might mirror those of InPBi, which produces mid-bandgap photoluminescence signals. "This might be achieved by introducing bismuth clusters forming deep levels," enthuses Wang. According to him, current levels of incorporation of bismuth, which are up to 2 percent, are insufficient for clustering.

"If high bismuth incorporation were successful, it could provide a new route for making intermediate band solar cells on GaAs," adds Wang.

The team produced a series of InGaPBi films by gas source MBE. After loading GaAs substrates into the growth chamber and removing the surface oxide, they deposited an undoped, 100 nm-thick GaAs buffer at 580°C, before lowering the temperature to 300°C and depositing 330 nm-thick InGaPBi films that contained either 0.5 percent, 1.0 percent or 1.8 percent bismuth.

Incorporation of these levels of bismuth was confirmed with Rutherford backscattering spectrometry, while high-resolution X-ray diffraction offered evidence of excellent crystal quality, producing peaks for InGaPBi with low values of full-width at half maximum.



High-resolution X-ray diffraction produces peaks with a full width at half- maximum of 54 arcsec, 49 arcsec and 50 arcsec, for InGaPBi alloys with a bismuth content of 0.5 percent, 1.0 percent and 1.8 percent, respectively.

Adding bismuth did not impair material quality, according to atomic force microscopy measurements. InGaP and InGaPBi with varying degrees of bismuth all have a root-mean-square roughness of 0.4 nm for a scan area of 2 μm by 2 μm.

Raman spectroscopy has also been used to scrutinise samples. This technique uncovers phonon modes associated with InBi and GaBi and reveals that atoms of bismuth replace those of phosphor to create covalent bonds. Adding more bismuth creates more InBi and GaBi bonds, leading to stronger signals.

Room-temperature photoluminescence measurements produced a peak at 1.78 eV for the quaternary with 0.5 percent bismuth. The intensity of this peak did not improve after one minute of sample annealing at 450°C and then at 500°C. Wang says that the challenge is to now understand the nature of the photoluminescence – whether it is related to the bandgap, or to deep levels.

InGaPBi films with more than 0.5 percent bismuth did not produce detectable photoluminescence. The researchers believe that this is due to a disorder effect induced by bismuth clusters.

Wang admits that the lack of strong photoluminescence is a concern for the use of this quaternary in LEDs and lasers. "If the observed photoluminescence is from carrier recombination at the bandgap, it can be enhanced when the quantum well is formed," argues Wang, who warns that if the luminescence is related to deep levels, enhancement via quantisation may not be as effective.

L. Yue *et. al.* Appl. Phys. Express **8** 041201 (2015)

 Copyright Compound Semiconductor

Probing buried interfaces in Schottky contacts

Laser emission that impinges contacts from the back of the wafer enables non-destructive analysis of electrical characteristics within SiC Schottky contacts

A NOVEL MICROSCOPE has enabled Japanese engineers to uncover variations in the electrical properties within metal contacts to wide bandgap materials.

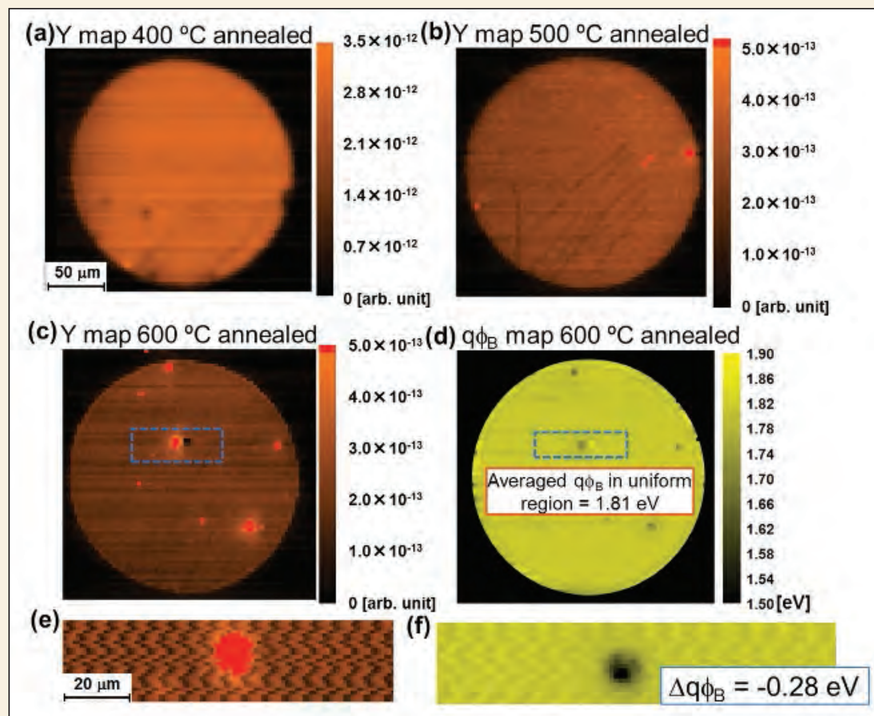
Exposing these variations will aid the development of Schottky contacts in SiC and GaN devices. These power electronics chips suffer from electrical non-homogeneity at metal-semiconductor interfaces, which can stem from crystallographic defects, process-induced damage, surface contamination, device design and temperature variations.

Lead author of the paper reporting this study, Kenji Shiojima from the University of Fukui, says that the insights provided by the team's scanning internal photoemission microscope make it easy to see what is bad and what is good in the electrode area.

Shiojima developed the first generation of the tool with Tsugunori Okumura in 1987, with the pair using it at Tokyo Metropolitan University to examine silicon and GaAs Schottky contacts.

"We have totally rebuilt the microscope for wide bandgap semiconductors, with modern electrical, mechanical and optical components," says Shiojima.

One of the devices that the engineers have studied with their tool that incorporates red, green and blue lasers is a high-power vertical diode with a 9.7 μm-thick layer of SiC, deposited on a 4H, *n*-type SiC substrate. This device, which should be capable of a breakdown voltage of around 1000 V, features a Schottky contact that is inserted by first treating the surface with HCl, and then depositing a 200 μm-wide circular contact made from a 50 nm-thick film of nickel.



Measurements of the photo-yield (the photocurrent per number of incident photons) *Y*, for a nickel/*n*-SiC contact dot with a diameter of 200 μm after annealing at (a) 400°C, (b) 500°C, and (c) 600°C. A map of the Schottky barrier height, $q\phi_B$, is provided for the dot annealed at 600°C (d). Magnified views of (c) and (d) are shown in (e) and (f).

To allow subsequent investigations to uncover early-stage interfacial reactions in the contacts, engineers applied moderate annealing temperatures of 400°C, 500°C and 600°C. Annealing lasted for 10 minutes, taking place under nitrogen gas.

Measurements with the scanning internal photoemission microscope involved recording internal photoemission from the metal-semiconductor interface. When light impinges on this interface with energy greater than the Schottky barrier height, electrons surmount the barrier, generating a photocurrent. The ratio of photocurrent to that of incident photons is referred to as the photo-yield, and measuring this at different wavelengths enables the construction of a map of the Schottky barrier height.

Mapping the contact with a red laser produces photo-yield profiles that are uniform for annealing at 400°C, and non-uniform at higher temperatures (see figure). There are some spots associated with annealing at 500°C, and their number and size increases at 600°C. For contacts annealed at that temperature, the Schottky barrier height map has an average of 1.81 eV, except in regions with large spots, where it can be smaller by about 0.28 eV.

The lower barrier height in the spots leads to a higher current density and creates an electrode featuring parallel conduction. Shiojima and co-workers have modelled the current-voltage curves that would result from such a contact, and found it to be in good agreement with measured values.

Recently, Shiojima and his co-workers have using their scanning microscope to study thermal and electrical degradation of Schottky contacts and FETs, including those in other wide bandgap materials, such as diamond and oxide semiconductors.

K. Shiojima *et. al.* Appl. Phys. Express **8** 046502 (2015)

To promote your Products and Services contact:
Robin Halder
T: +44 (0)2476 718 979
E: robin.halder@angelbc.com

Tel: +49 2407 9030 0
Fax: +49 2407 9030 40
Email: info@aixtron.com
www.aixtron.com

Tel: +49 (0)8122 86676
Fax: +49 (0)8122 86652
Email:info@kitec.de
www.kitec.de

Tel: +1 925 245 5817
Fax: +1 925 449 4096
Email: lwarren@ferrotec.com
www.temescal.net

Email: info@epigan.com
www.epigan.com

Tel. No.: +49 (0) 30 89 00 55 0
Fax No: +49 (0) 30 89 00 55 180
e-mail: info@laytec.de
website: www.laytec.de

Tel: +1 614 891 2244
Fax: +1 614 818 1600
Email: info@lakeshore.com
www.lakeshore.com

Tel: +44 [0] 1925 445225
Fax: +44 [0] 1925 416518
Email: info@hiden.co.uk
www.hidenanalytical.com

Tel: +44 (0)1934 837000
Fax: +44 (0)1934 837001
Email: plasma.technology@oxinst.com
www.oxford-instruments.com

www.watlow.com

Tel: +41 52 304 22 00
Fax:+41 52 304 22 12
Email: info@meister-abrasives.ch
www.meister-abrasives.ch

Tel:+1 603 595 8900
Email: sales@masimo.com
www.masimosemi.com

Tel: 86-769-2289 3350
Fax: 86-769-2289 3355
Email: enquiry@sicty.com
www.sicty.com

Tel: +49 8728 911 093
Fax: +49 8728 911 156
Email: sales@35reclaim.com
www.35reclaim.de

Tel: +1 650-213-9311 Ext.229
Fax: +1 650-213-9511
Email: sales@translucentinc.com
www.translucentinc.com

Tel: +1 201 507 3300
Fax: +1 201 507 1506
Email: inquiry@umccorp.com
www.umccorp.com

Tel: +1 734-426-7977
e-mail: requestinfo@k-space.com
www.k-space.com

Tel: +49 33398 696592
Fax: +49 33398 696594
Email: jp@bachrc.de
www.bachrc.de

Cleaning • Deposition • Etching

Tel: +1 512-385-4552
Fax: +1 512-385-4900
Email: r.andrade@nanomaster.com
www.nanomaster.com

Tel: + 41 81 720 1080
Fax: 41 81 720 1161
www.evatecnet.com

Tel: +49 (0) 3641 79980
Fax: +49 (0) 3641 7998222
www.vistec-semi.com

Tel: +1 617-227-1133
Fax: +1 617-742-0686
Email: paula@filtech.com
www.filtech.com

Tel: +49 721 50997-0
Fax: +49 721 50997-5654
www.bruker.com

Tel: +49 (089) 45 49 43 - 0
Fax: +49 (089) 45 49 43 - 11
Email: info@instrumentsystems.com
www.instrumentsystems.com

Tel: 516-677-0200-1222
Fax: 516-714-1231
Email: jpina@veeco.com
www.veeco.com

To promote your Products and Services contact:
Robin Halder
T: +44 (0)2476 718 979
E: robin.halder@angelbc.com

PLANSEE
Tel: +43 5672 600 2944
Email: led@plansee.com
www.plansee.com

Tel: +81 44 589 5894
Fax: +81 44 541 1326
Email: moreinfo@ntt-at.com
www.ntt-at.com

Tel: +1-408-236-7560
Email: asaharah@diccny.com
www.dowa-electronic.co.jp

Tel No: +49 (89) 96 24 00-0
Fax No: +49 (89) 96 24 00-122
Email: sales@csclean.com
www.cscleansystems.com

Tel. No: +82-62-602-7857
Fax No: +82-62-972-0483
www.hisolarled.co.kr
e-mail: chonhh@hanmail.net
e-mail: david@hisolarled.com

Tel: + 7 812 601 06 05
Email: sales@semiteq.ru
www.semiteq.org

Tel: 800-762-3468
www.durexindustries.com

Tel: + (510) 384 1118
Fax +(510) 887 0626
Email mwise@mdcvacuum.com
www.mdcvacuum.com

Tel: +86-592-7767288
Email: sales@epiworld.com.cn
www.epiworld.com.cn

Tel: + (001) 407 422 3171
Fax +(001) 407 648 5412
Email orlandosales@googchandhousego.com
www.googchandhousego.com

A Siemens Business
Big Data Product Performance Intelligence Solutions
Tel: 704-227-6600
Email: sales@camstar.com
www.camstar.com

Tel: +44 (0)1246 718 979
Fax +44 (0)1246 718 971
Email: robin.halder@angelbc.com
www.compoundsemiconductor.net

Tel: +1 510-501-4031
Fax +1 360-723-5368
Email: sales@cal-coating.com
www.cal-coating.com

Tel: 203-949-8697
Fax: 203-949-8016
Email: info@protononsite.com
www.protononsite.com

Tel: +44 (0)1246 718 979
Fax +44 (0)1246 718 971
Email: robin.halder@angelbc.com
www.compoundsemiconductor.net

Submit your Lab & Fab article

Research is the foundation for the growth of the compound semiconductor industry.

If you want to highlight the important breakthroughs that you make, submit your latest research stories to **RichardStevenson@angelbc.com**

It is imperative that Compound Semiconductor remains a timely resource for this industry, so we are only interested in highlighting very recent work reported in academic papers.

Therefore, please only consider writing a short piece highlighting your work if you have a journal paper that has been accepted and about to appear in press, or a paper that has been published within the last month.

www.compoundsemiconductor.net

TEMESCAL
UEFC-4900
Near Perfect Uniformity with Auratus™ Deposition Enhancement Methodology

Rock it like the big boys.

The Temescal UEFC-4900—ultimate lift-off metallization performance like the UEFC-5700, but optimized for smaller wafers and smaller production volumes.

Temescal
UEFC–4900

We all have dreams. With our Auratus™ deposition enhancement methodology and the UEFC-5700, we transformed near perfect uniformity into a science. Now we're bringing this performance to a mid-sized system, harmonizing your process to the vapor cloud and enabling you to deliver better products. In less time. Using less material. So you'll have more money. Realize your dreams.

Let's jam! Find out how Temescal can bring near perfect uniformity to your lift-off metallization coating process.

To find out more, visit **www.temescal.net/auratus-rocks** or call **1-800-522-1215**.

FerroTec

© 2015 Ferrotec (USA) Corporation. All rights reserved.
Temescal is a registered trademark and Auratus is a trademark of Ferrotec (USA) Corporation.