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Viewpoint

By Dr Richard Stevenson, Editor

Telling our story

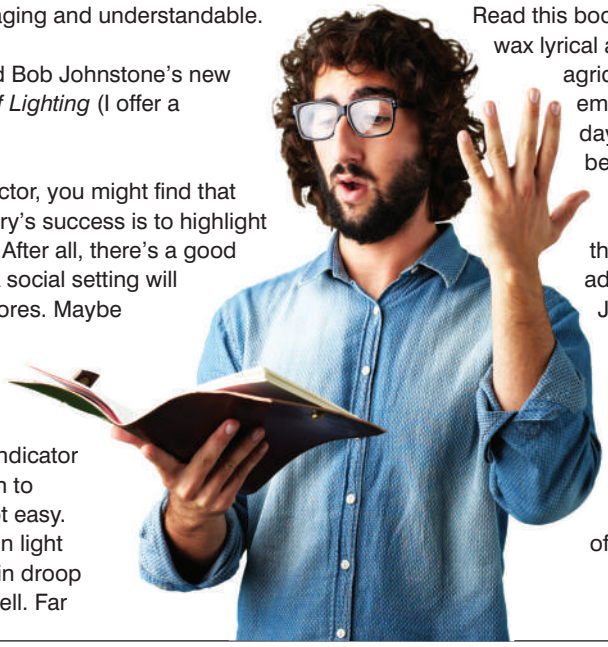
POPULAR SCIENCES BOOKS aim to educate the layman. By eradicating equations, offering analogies and telling a story with a human touch, Joe Public can be entertained while learning the basics of a subject.

But that's not the only benefit of these books. They can be read by experts, so that when they are at social gatherings and are asked what they do for a living, they can draw on what's been written to give an answer that's engaging and understandable.

It is for that reason that I recommend Bob Johnstone's new book *L.E.D. A History of the Future of Lighting* (I offer a review on p.36)

Even if you don't work in the LED sector, you might find that the best way to talk about our industry's success is to highlight its key role in the lighting revolution. After all, there's a good chance that those that you meet in a social setting will have seen LED bulbs in hardware stores. Maybe they even own some. And are they impressed by how long they last?

If they are rather astute, they might ask what it took to take those puny indicator lamps and make them bright enough to light up a room. Answering this is not easy. You could talk about improvements in light extraction efficiency and reductions in droop – but don't expect this to go down well. Far better is to tell the story the way Johnstone does. It begins with a meeting of visionaries that plot out the rate of improvement in these devices, see where they are destined to go, and put plans in place to make this happen. Instrumental in the success is the backing by government, which uses its money very effectively, alongside the introduction of standards that quash the availability of inferior bulbs.



Read this book and you will also be able to wax lyrical about the benefits of LEDs in agriculture, and how the tuning of the emission spectrum throughout the day can help schoolchildren to learn better.

So don't ignore this book – or, for that matter, others that cover great advances in our industry, such as Jerry Neal's personal account of the growth of RFMD. It is given in *Fire in the Belly: Building a World-Leading High-Tech Company from Scratch in Tumultuous Times*. Armed with anecdotes from books such as this one you'll be able to do your bit to promote the benefits of our industry.

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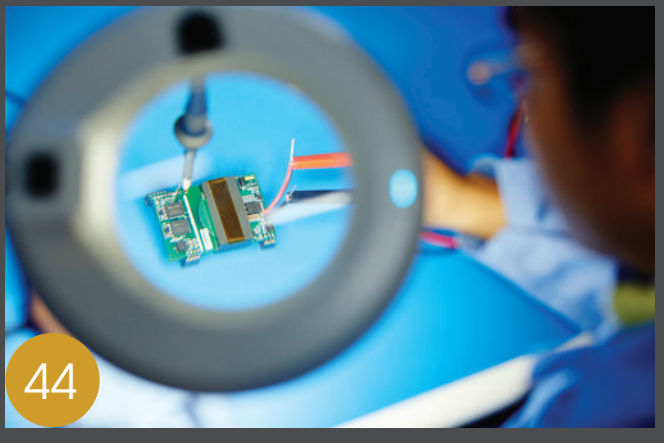

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Lighting not driving LED growth in 2017

STRONG GROWTH in packaged LED lighting revenue from 2007 to 2014 was the result of consumers replacing incandescent and fluorescent lighting with LED lighting. However, price erosion due to competition and the trend toward less robust, inexpensive 2835 packages caused revenues to decline by 9 percent in 2015 and only 1 percent in 2016, according Jamie Fox, principal analyst, lighting and LEDs group, IHS Markit.

Starting in 2017, revenue growth is expected to increase by 3 percent as prices settle. In 2017, automotive and signage segments are growing as much as lighting, with each of the three applications forecast to be $200 million higher than packaged LED revenue in 2016. Horticulture is projected to see the fastest growth in 2017, although lower compared with automotive, lighting and signage.

Automotive is boosted by increasing LED use on vehicle exteriors, in headlamps and other areas such as daytime running lights, rear lighting, turning lights and interior vehicle illumination for both cars and heavy vehicles such as trucks and buses. Automotive packaged LED revenue is forecast to grow 9.2 percent in 2017, from $1.9 billion to $2.1 billion. Signage use is boosted by the trend towards finer pitch displays and the fact that LED displays are not a mature market; growth is possible by finding new business, not only replacement. Signage markets include large full colour displays known as videowalls, as well as road signs, traffic lights and building lettering. Signage is forecast to grow 11.5 percent from $1.8 to $2.0 billion. Horticulture is a smaller market but in percentage terms will grow even faster in 2017 than signage and automotive.

Lighting growth from 2018 to 2022 is forecast to increase 6 to 7 percent per year due to a strong forecast for LED lamp shipments and reduced price erosion at the packaged LED component level. Due to basic material costs, company overheads and the slow reduction of subsidies in China, it will not be possible for prices to fall as quickly as they did from 2007 to 2014. In CAGR terms, lighting still is forecast to have a slightly lower 2016-2022 CAGR (6.1 percent) than automotive exterior

(7.9 percent) and signage (8.5 percent). LED manufacturers are no longer focused on only packaged LEDs for lighting for growth. Now most companies have entered automotive, signage or horticulture segments, or are considering doing so. The era of specialists is over; now, everyone does everything.

Lockheed Martin unveils GaN-based radar technology

LOCKHEED MARTIN unveiled its next generation air and missile defence radar demonstrator at the annual Space & Missile Defense Symposium in Huntsville, Alabama. Based on active electronically scanned array (AESA) technology, it incorporates GaN transmitter technology and advanced signal processing techniques including recently developed 360 degree sensor/fire control algorithms based on advanced threat sets.

These technologies and concepts have been integrated into both demonstration and production systems resulting in the industry's first fielded ground based radars with GaN technology.

The fractional array is representative of Lockheed Martin's potential Lower Tier Air & Missile Defence Sensor solution, built on a modular and scalable architecture to scale to the Army's requirements, once finalised, to replace the aging Patriot MPQ-65 radar. The array on display in Huntsville will be used to mature technology and verify performance to ensure uniform 360-degree threat detection and system performance.

"Incremental upgrades to the existing Patriot radar no longer address current sustainment issues, current threat performance shortcomings, or provide growth for future and evolving threats," said Mark Mekker, director of next generation radar systems at Lockheed Martin. "Lockheed Martin is prepared to offer a next generation missile defense system that will leverage advances in radar technology to provide a modular, scalable architecture and reduce the total cost of ownership well over its 30-year lifecycle."

The AESA technology is also in use in the AN/TP/Q-53 radar system, which Lockheed Martin designed, developed and delivered to the Army on an urgent need timeline in under 36 months, and which continues to be scaled to address emerging threats.

"Our solution for the US Army's new air and missile defense sensor is not a new-start program. It's a combination of technology maturation over several years and includes capability leveraged from our current development programs and battlefield-proven radars. We rely heavily on our modern radar systems such as the Q-53 and the Long-Range Discrimination Radar to rapidly bring low-risk, proven technology to the warfighter," Mekker said. "We look forward to the opportunity to participate in this competition that will ultimately drive up performance and reduce costs for the US Army."

ARPA-E awards $30 million to develop better power converters

THE US Department of Energy's (DoE) Advanced Research Projects Agency-Energy (ARPA-E) has announced $30 million in funding for 21 innovative projects as part of the Creating Innovative and Reliable Circuits Using Inventive Topologies and Semiconductors (CIRCUITS) programme. The programme will use power converters based on wide bandgap (WBG) semiconductor technology like SiC or GaN to accelerate the development and deployment of innovative electric power converters that save energy.

Previous efforts by ARPA-E have focused primarily on WBG material and device development. CIRCUITS focus on new circuit topologies and system designs, ensuring the performance benefits of these new WBG devices are maximised. "Hardware built with WBG devices has the potential to be smaller, lighter, and much more energy-efficient, with applications across valuable sectors including transportation, information technology, the grid, and consumer electronics," said ARPA-E Acting Director Eric Rohlfing. "Developments from CIRCUITS projects could one day lead to super-fast, compact electric vehicle chargers, more efficient ship propulsion systems, and lighter, aerodynamic aircraft that can carry more passengers with less fuel."

Examples of selected CIRCUITS projects include Imagen Energy, which received $847,888 to develop a SiC-based compact motor drive system to efficiently control high power (greater than 500 kW), high performance permanent magnet electric motors operating at extremely high speed (greater than 20,000 rpm). Imagen Energy's design seeks to address a major roadblock in operating electric motors at high speed, namely overcoming large back electromotive forces (BEMF). If successful, the project team will demonstrate a motor drive capable of handling large BEMF and increase motor system efficiency over a broad range of operating speeds.

The University of Arkansas has received $2,163,630 to develop a 2 by 250 kW power inverter system for use in the electrification of heavy equipment and other higher volume transportation applications (e.g., trucks, buses, cars).

EPC introduces wireless charging demo kit

EFFICIENT POWER CONVERSION CORPORATION (EPC) has announced the availability of a complete class 4 wireless power charging kit, the EPC9120. The system can transmit up to 33 W while operating at 6.78 MHz (the lowest ISM band). The purpose of this demonstration kit is to simplify the evaluation process of using eGaN FETs for highly efficient wireless power transfer. The EPC9120 uses the high frequency switching capability of EPC GaN transistors to facilitate wireless power systems with full power efficiency between 80 percent and 90 percent under various operating conditions. The EPC9120 wireless power system consists of four boards: Source Board (Transmitter or Power Amplifier); EPC9512 Class 4 Air Fuel compliant Source Coil (Transmit Coil); Category 4 AirFuel compliant Device Coil with rectifier and DC smoothing capacitor; and Category 3 AirFuel compliant Device Coil with rectifier and DC smoothing capacitor. The popularity of highly resonant wireless power transfer is increasing rapidly, particularly for applications targeting portable device charging. The end applications are varied and evolving quickly from cell phone charging, to handheld tablets, and laptop computers. Delivering up to 33 W supports these applications. The source board is a Zero Voltage Switching (ZVS), Class-D amplifier configured in an optional half-bridge topology (for single-ended configuration) or default full-bridge topology (for differential configuration), and includes the gate driver(s), oscillator, and feedback controller for the pre-regulator.

Wolfspeed develops all SiC modules for high voltage applications

WITH FUNDING assistance from PowerAmerica, SiC device and power module company Wolfspeed has developed first-of-its-kind SiC power modules for 3.3 kV and 10 kV applications.

According to the company, this is the first SiC power module at these voltage levels to use exclusively the MOSFET built-in body diode as the anti-parallel rectifier.

PowerAmerica funding helped the company manufacture and test the modules. During testing, Wolfspeed was able to demonstrate the power improvement gained by not having the additional diodes. Currently, these Wolfspeed power modules are being offered to PowerAmerica members and select customers.

A built-in diode has numerous advantages over an external and additional diode device. The built-in diode or 'body diode' design maximises the performance of SiC MOSFET modules by freeing up space in the power module, allowing for more power capability and therefore increased performance in a smaller space. It also makes assembling a power module easier, boosting long-term reliability and optimising costs.

"Essentially, we're doubling the power and therefore increasing supply chain capability by providing another solution at higher power levels – specifically at the 3.3 kV and 10 kV applications," said Ty McNutt, director of business development at Wolfspeed's Fayetteville, AR location.

Hanergy and Audi to integrate GaAs solar panels into their range of cars

ALTA DEVICES, a subsidiary of Hanergy Thin Film Power Group, has signed a Memorandum of Understanding with Audi AG on strategic cooperation in flexible GaAs thin film cell technology. Audi and Hanergy will introduce the solution of integrating thin-film solar cells in the panoramic roof of Audi models. It is aimed to prolong the endurance mileage by feeding solar energy into the internal vehicle electrical system – including air conditioning and other electrical appliances.

In the long term, by using technologies from both sides, the two parties plan to gradually transition to use thin film solar technology to feed solar energy into the drivetrain battery to provide additional primary power for vehicles.

The project will not only contribute to Audi's clear vision of emission-free mobility, but also advance the application of thin-film solar technology for global primary energy generation. The two sides plan to jointly present an Audi vehicle prototype featuring an integrated prototype solar roof solution by the end of 2017. Electric drive systems are essential for future automobiles at Audi. By 2020, the product range will include three battery-electric cars. By 2025, Audi intends to deliver one third of its cars with fully electric drivetrains to customers. Based on this strategic setting, renewable energy – especially solar energy with the characteristics of mobile energy – has become very attractive for Audi to achieve sustainable mobility. Since light vehicle bodies and limited vehicle roof areas require solar cells with a high power-to-weight ratio. GaAs, a high-efficient, thin, flexible and lightweight thin film solar technology has therefore stood out as the primary option for Audi's panorama sunroof solution. Chairman Yuan Yabin of Hanergy remarked at the signing ceremony, "As the automotive industry is striving for green mobility, I believe that the cooperation between the two sides will convey the message of green development to the world through the efforts from the traditional and emerging industries, while revealing the confidence and action from both sides in protecting the environment."

Ding Jian, senior Vice President of Hanergy, CEO of Alta Devices and co-leader of the Audi/Hanergy project, said: "This partnership with Audi is Alta Devices' first cooperation with a high-end auto brand. By combining Alta's continuing breakthroughs in solar technology and Audi's drive toward a sustainable mobility of the future, we will shape the solar car of the future."

"The range of electric cars plays a decisive role for our customers. Together with Hanergy, we plan to install innovative solar technology in our electric cars that will extend their range and is also sustainable," stated Audi board member for procurement Bernd Martens. At a later stage, solar energy could directly charge the traction battery of Audi electric vehicles. "That would be a milestone along the way to achieving sustainable, emission-free mobility," continued Martens.

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Osram IR LEDs feature in FOVE Eye-tracking VR headset

CHIP LEDs from Osram Opto Semiconductors are providing the infrared illumination in a new virtual reality headset built by the Japanese start-up company FOVE that integrates eye tracking as a novel means of interaction. FOVE is a high-end virtual reality (VR) system that allows users to immerse themselves in another world, with enclosed headsets shutting out their real surroundings.

To provide an authentic virtual experience, sensors keep track of users and integrate their position and movements into the virtual action. Now eye tracking provides another, novel and intuitive way of interacting with virtual reality. Users can select or move an object by just looking at it.

They can establish eye contact with virtual characters or trigger actions by focusing their gaze at a certain spot. Moreover, the technology allows for 'foveated rendering', a technique which significantly reduces demands on computing power and graphic cards. Based on the information about the user's point of gaze, VR systems can adjust the resolution and render areas in the direct field of vision in high resolution while allowing for lower resolution in the periphery.

"We chose Osram IR LEDs because they are high-quality products. They meet all our specifications. One of our main deciding factors was that only very little light lies outside the central emission spectrum and is therefore lost, which meant we could streamline our optical filter design process and maximize our sensor performance," said Lochlainn Wilson from FOVE.

Eye tracking systems illuminate the user's eyes with infrared light, register the reflections with an IR sensitive camera sensor and employ special algorithms to determine the user's direction of gaze and eye movements.

To realise the function inside a headset, several infrared LEDs are mounted around the two lenses. FOVE uses SFH 4053 ChipLEDs from Osram Opto Semiconductors, which are only 0.5 mm x 1.0 mm x 0.45 mm in size.

Their emission wavelength of 850 nm matches the spectral sensitivity of the camera sensor and their beam angle of +- 70° ensures an even illumination of the eyes.

"Through collaboration with FOVE, we are the first supplier to provide an eye tracking solution for a VR headset," said Hiroshi Okuma, marketing manager for ELS (Emitter, Laser, Sensors) at Osram Opto Semiconductors.

Luna sells optical receiver business to Macom

LUNA INNOVATIONS, a manufacturer of products for the aerospace, automotive, energy, defence, and telecommunications markets, has announced that Macom Technology has agreed to buy the assets and operations related to its high-speed optical receivers (HSOR) business. The sale includes the operations associated with Luna's development, manufacturing and sales of products such as high-speed integrated coherent receivers and photodiodes. Luna originally acquired these operations as part of its merger with Advanced Photonix Inc. (API) in May 2015. The assets and employees associated with Luna's Terahertz operations are not transferred in this transaction.

"Since the merger with API, we have invested substantial time and resources into the HSOR business as a significant growth area," said My Chung, president and CEO of Luna. "As a result of that investment, we have developed leading products and technologies in that marketplace.

"Macom has recognised the value that we have created in this space and earlier this year approached us with this transaction opportunity. With their larger scale of operations, broader suite of product offerings and global footprint, we believe that Macom provides a greater opportunity to drive long-term growth for the HSOR business, and the completion of this sale maximizes the value we would receive from the HSOR business."

As part of the transaction, employees associated with the company's HSOR operations and administration in the company's location in Ann Arbor, Michigan, will transfer to Macom.

"Similar to our High Performance Analog and 25G laser products, Luna's industry-leading high speed optical receiver products and technology are well-aligned with Macom's previously-announced growth strategy in Cloud datacentres and other high-speed networking markets, and we are excited to be able to add these products to our growing portfolio through this tuck-in acquisition," said John Croteau, Macom's president and CEO.

"We expect the transaction to be neutral to accretive in the first year of combined operations, and to contribute meaningfully to growth in our Fiscal Year 2018. We look forward to bringing this talented group of individuals into the Macom organisation as we move ahead in meeting the evolving demands of the communications markets."

"We are delighted with the outcome of the transaction and the value we have created for Luna's stockholders," Chung said. "We are especially grateful to the dedicated employees in the HSOR business whose skills and efforts have resulted in building this valuable business."

II-VI acquires UK compound semiconductor fab for $80 million

II-VI Incorporated, a US optoelectronic component company, has bought Kaiam Laser's 6-inch wafer fab in Newton Aycliffe, UK for $80 million. The acquisition is expected to be break even at the EBITDA level within 12 months. The 300,000-square foot facility hosts a state of the art 100,000 square foot clean room designed for high-volume manufacturing of compound semiconductor devices based on GaAs, SiC and InP materials.

Chuck Mattera, president and CEO of II-VI said: "This facility hosts one of the best clean rooms in the entire compound semiconductor industry and augments our capabilities at a time when industry capacity is rapidly becoming fully subscribed.

"Given the demand we anticipate, this acquisition will allow us faster time to market than building a proprietary green field site and will enhance our leadership position in the supply chain. It adds to our in-house capacity for VCSELs, and is also as part of a broader strategic move to provide a versatile 6-inch wafer fab for GaAs, SiC and InP-based devices.

"This acquisition will significantly expand our capacity and is expected to enable us over time to penetrate high growth markets driven by, for example, 3D sensing, 5G wireless, the electrification of the car, and datacentre communications."

Bardia Peseshki, the CEO of Kaiam, added: "II-VI will be using this fab more effectively by leveraging its full capacity and multi-purpose use. I am looking forward to working with II-VI to establish a commercial relationship that includes having II-VI provide InP-based epitaxial wafers and wafer fabrication services for our products as we continue to expand our transceiver business in the rapidly growing 100G and impending 400G datacentre markets."

Showa Denko to acquire SiC Tech

SHOWA DENKO has announced that it will acquire assets concerning the sublimation-recrystallisation method of manufacturing SiC wafers from Nippon Steel & Sumitomo Metal Corporation (NSSMC) and Nippon Steel & Sumikin Materials (NSMAT) by the end of January 2018. Showa Denko began research and development of SiC epitaxial wafers in 2005, and now produces and sells 3,000 epitaxial wafers per month.

The company aims to improve the quality of its products through the acquisition of assets currently owned by Nippon Steel & Sumitomo Metal Group.

NSSMC has been researching and developing 150-mm (6-inch) SiC single crystal wafers for power semiconductor devices at the Advanced Technology Research Laboratories under the R & D Laboratories. In addition, NSMAT has been developing a business for 100-mm (4-inch) wafers. NSSMC succeeded in developing 4-inch SiC wafers in 2007 by drawing on the technologies nurtured through steelmaking.

Then, NSMAT started business development towards establishing a practical manufacturing technology and quality for such wafers based on the success.

NSMAT has been offering SiC wafers to customers. However, as it would take more time to develop this market, the NSSMC group decided to terminate the research and business development as part of the selection and concentration of business operations.

In its ongoing medium-term business plan 'Project 2020+' Showa Denko positions its business to produce and sell SiC epitaxial wafers for power devices as an 'Advantage-establishing' business. It aims to further strengthen its product development and supply system for SiC epitaxial wafers, aiming to contribute to the spread of SiC-based power devices.

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Speakers announced to date

Wrestling Market Share from Silicon Power Devices

What are the next opportunities for SiC? And how can GaN gain significant traction in the market place?

ANALYST

- **Richard Eden: IHS Markit**
  The SiC & GaN power semiconductor market: Forecasts and drivers

SPEAKERS

- **Philip Zuk: Transphorm**
  Shifting gears: The "GaN-ification" of automobiles
- **Peter Friedrichs: Infineon**
  Exploiting the merits of GaN and SiC
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- **Tamara Baksht: VisIC Technologies**
  High efficiency at high power density: realisation of GaN's promise for power electronics
- **Andy Sellars: Catapult**
  Accelerating the commercial application of compound semiconductors
- **Mohamed Alomari: IMS Chips**
  Fast-loop assessment of GaN/AlGaN epitaxial layers for power applications

Finding Solutions with Heterogenous Integration

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ANALYST

- **Zhen Zong: Yole Développement**
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SPEAKERS

- **Jean-Pierre Locquet: GaNonCMOS EU Project**
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- **Wolfgang Stolz: NAsP III-V**
  Building III/V-devices on CMOS-compatible Si (001)
- **Lars-Erik Wernersson - Lund University**
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5G: Where are we and What's Next?

What form will 5G take? And how good will 5G be for GaAs and GaN?

ANALYST

- **Eric Higham: Strategy Analytics**
  Is 5G roll-out a certainty? And will it be good for GaAs and GaN?

SPEAKERS

- **Roger Hall: Qorvo**
  Building the industry's first 5G front-end
- **Liam Devlin: Plextek RFI**
  MMICs - what is needed to get mmWave 5G to work?

LEDs: Magnifying Margins

Which sectors offer the best returns? Does the bottom line get the biggest benefit from streamlining manufacturing, or from optimising the chip?

ANALYST

- **Pars Mukish: Yole Développement**
  Revolutionising displays with MicroLEDs

SPEAKERS

- **Andreas Weisl: Seoul Semiconductor**
  Improving LEDs with a Wafer Level Integrated Chip on PCB (WICOP) architecture
- **J.C.Chen - Ostendo Technologies**
  The monolithic full-colour LED and its applications
- **Keith Strickland – Plessey Semiconductors**
  Horticultural lighting offers growth opportunities

Ramping Revenues from RF Devices

What are the opportunities for III-Vs in defense and civilian markets? Will higher frequencies open up new sales?

ANALYST

- **Asif Anwar, Strategy Analytics**
  Defense sector trends and the associated market outlook for compound semiconductors

SPEAKER

- **Nick Cataldo, Efficient Power Conversion**
  Wireless charging with GaN devices




Ultraviolet LEDs take aim at disinfection

As Osram Opto pours more resources into deep UV LEDs, are the devices nearing commercialisation? asks Rebecca Pool.

WHILE LONG-WAVELENGTH, ultraviolet LEDs have swiftly penetrated curing applications worldwide, shorter wavelength deep UV LEDs, designed for disinfection, have faltered.

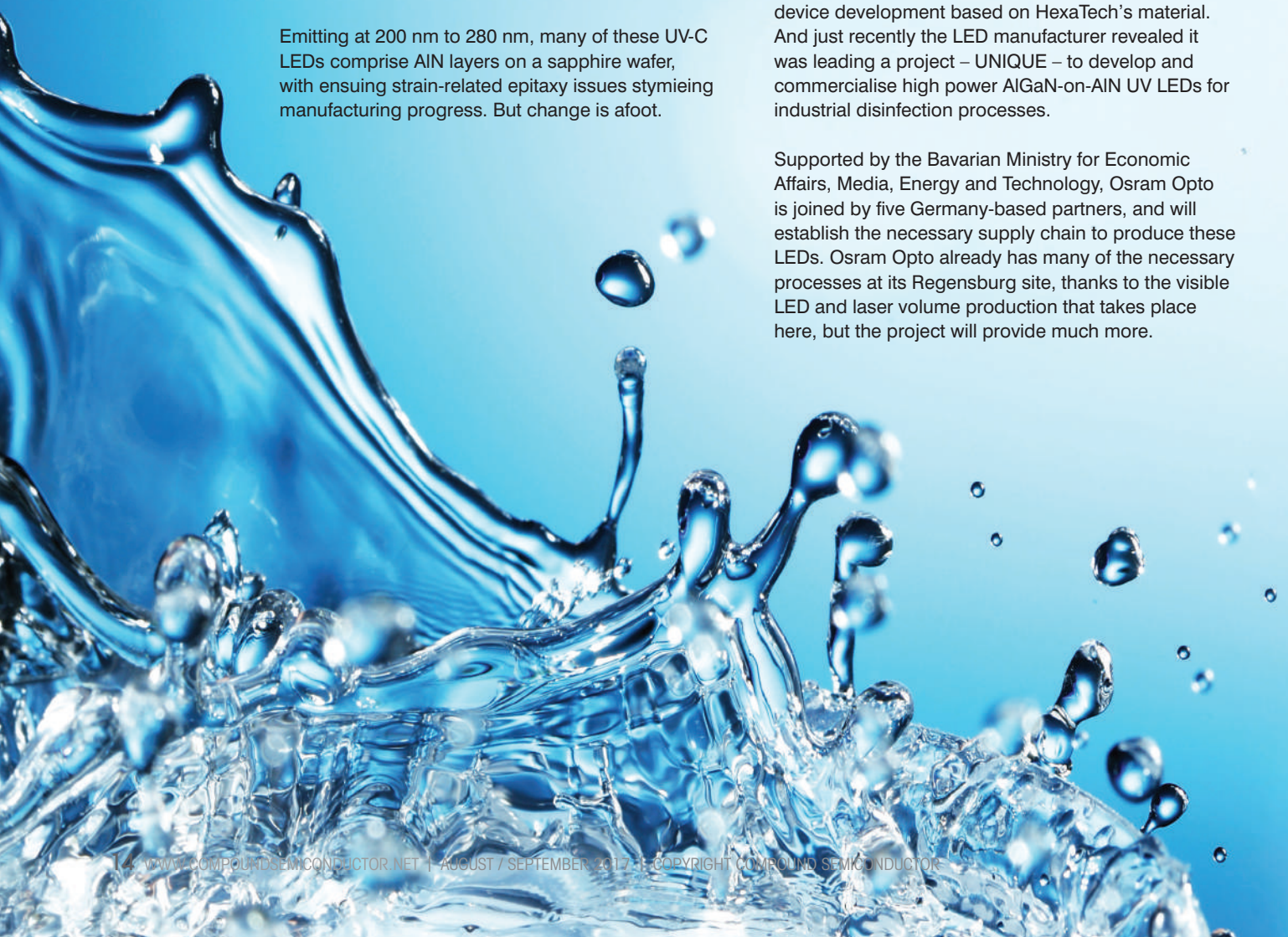
UV-A LEDs, emitting at 315 nm to 400 nm, are fabricated by growing InGaN-based epilayers on sapphire substrates via the tried-and tested MOCVD methods used in visible LED markets. But the deep UV LED is different.

Emitting at 200 nm to 280 nm, many of these UV-C LEDs comprise AlN layers on a sapphire wafer, with ensuing strain-related epitaxy issues stymieing manufacturing progress. But change is afoot.

As UV LEDs markets have gathered momentum, AlN substrate manufacturers such as CrystAL-N, Germany, Crystal IS and Hexatech, both of the US, have been quick to ensure native, lattice-matched wafers are positioned to take on the readily available sapphire rival. And device manufacturers are biting.

Earlier this year, Germany-based Osram Opto Semiconductors signed a long-term licensing deal with US-based Hexatech to accelerate UV-C LED device development based on HexaTech's material. And just recently the LED manufacturer revealed it was leading a project – UNIQUE – to develop and commercialise high power AlGaN-on-AlN UV LEDs for industrial disinfection processes.

Supported by the Bavarian Ministry for Economic Affairs, Media, Energy and Technology, Osram Opto is joined by five Germany-based partners, and will establish the necessary supply chain to produce these LEDs. Osram Opto already has many of the necessary processes at its Regensburg site, thanks to the visible LED and laser volume production that takes place here, but the project will provide much more.



Aprotec is set to manufacture the crystal growth furnace while the Fraunhofer Institute for Integrated Systems and Device Technology will coordinate AlN crystal growth processes.

Osram Opto itself will develop the UVC LED chip and associated epitaxy and processing, Schott is to develop the much-needed vacuum-tight packaging, and UV LED system developer, Dr Hönle AG, will integrate the LED modules to the disinfection system.

As Hans-Juergen Lugauer, Head of UV-LED Research and Development at Osram Opto, asserts: "From AlN substrate production and chip fabrication to packaging and the final product for the end user, we will establish the complete value chain necessary for deep UV LEDs and related products in Bavaria."

Lugauer doesn't anticipate that AlN wafers will be available in the necessary volumes for volume production as the project closes, but as he puts it: "The Hexatech agreement was an independent move to secure access to high quality AlN wafers as soon as possible."

Wafer dilemma

Right now, Osram Opto is using two inch sapphire wafers for UV LED epitaxy and chip development, implementing a AlN buffer layer to manage lattice strains. However, researchers at the company have already been busy experimenting with epitaxy on AlN substrates, and work will continue as part of the UNIQUE project.

"We've been performing the epitaxy experiments in parallel, to be ready to transfer all processes to 2-inch wafers as soon as they are available in quantities," highlights Lugauer.

As part of its work, Osram Opto is using MOCVD to fabricate AlGaN thin films for deep UV LEDs. As Lugauer points out, dislocation densities on an AlN/sapphire templates are currently around 109/cm^2 but drop to less than 104/cm^2 for structures on AlN substrates.

"It is not yet clear whether the dislocation densities on AlN/sapphire templates are low enough to achieve the high efficiency and reliability needed for high current density disinfection applications," says Lugauer.

And as the head of UV-LED R&D points out, the efficiency of AlGaN-based structures is very sensitive to defects and dislocations. He questions whether or not even shorter wavelength applications, such as gas sensing, would be able to use sapphire substrates at all.

Osram Opto is using two inch sapphire wafers for UV LED epitaxy and chip development, implementing a AlN buffer layer to manage lattice strains. However, researchers at the company have already been busy experimenting with epitaxy on AlN substrates, and work will continue as part of the UNIQUE project

"The AlN substrates offer a very low dislocation density, which should have a positive effect on device efficiency and lifetime, and provide us with the high performance, high quality devices Osram Opto is known for," he adds.

Lugauer also highlights how using the native AlN substrates with AlGaN layers reduces thermally induced stresses and wafer bow after epitaxy. "The large bow of deep UV LEDs on sapphire sometimes completely prevents automated wafer handling in our chip processing line but [using AlN wafers] eases wafer handling," he says.

"The bow issue increases significantly as wafers scale up in size, which currently makes the use of 4 and 6-inch sapphire substrates more or less impossible for deep UV LEDs processing," he adds. "In contrast, as soon as larger AlN substrates are available, the processes can be straightforwardly transferred to the [bigger] size."

Still, Lugauer admits sapphire substrates are a lot cheaper, so Osram Opto will be pursing both substrate routes until the materials advantages and limits are clearer. "Then we will decide on the most practical approach," he says. "It might turn out that we will use both substrates to cover different application requirements."

In the meantime, Lugauer has his eyes firmly fixed on the epitaxy and chip processes. He believes the key steps to cost effective volume production of deep UV LEDs are to develop an epitaxy process that yields LEDs with a high internal quantum efficiency as well as a chip process that produces devices with high current stability and light extraction to deliver an external quantum efficiency of more than 10 percent.

"Both of these processes are now being developed within our project, but we don't expect production to be ready before 2020," he says.

Enabling breakthroughs in optical bandwidth density

Integrated optical components for long haul, metro and cloud data centres are benefiting from excellence in analogue and photonics technology

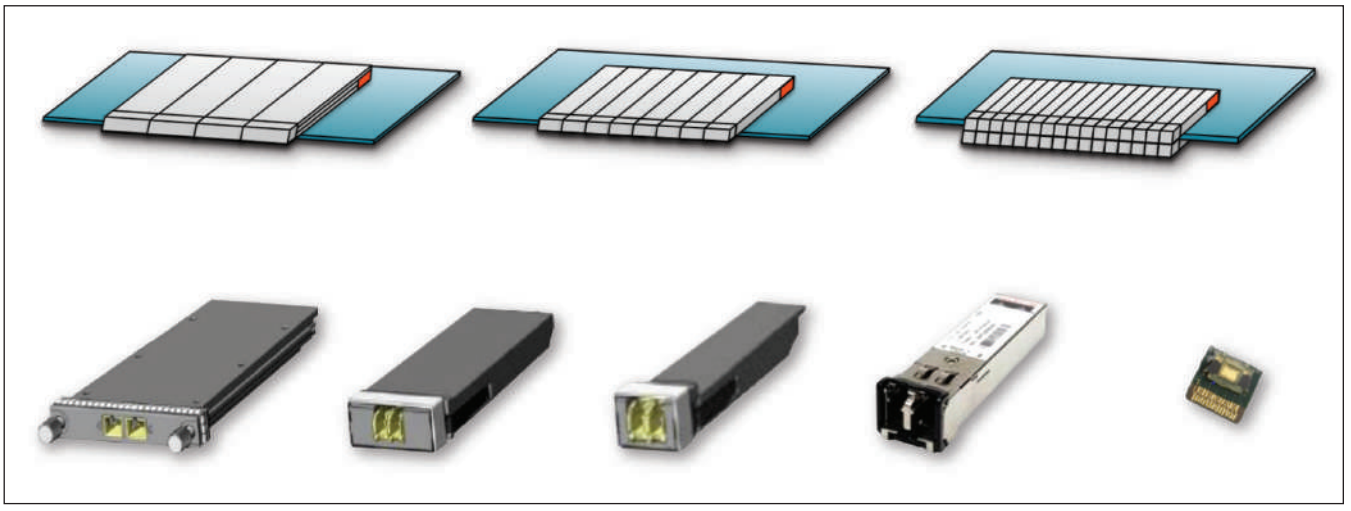
BY MACOM

THE CAPABILITY of the Internet continues to grow. In its formative years, the Internet was essentially a source of information, providing pages of text and a few images. Fast forward to today, and it is now the place to look for information, images and videos on all manner of things; a great option for buying anything from books to food, to holidays and to homes; and the link to storing data in the cloud.

To cope with the vast and growing number of users of the Internet, and the rising amount of data each of them downloads and uploads, the technology behind it – the optical network – has to undergo a never-ending increase in capacity.

At MACOM Technology Solutions (MACOM) of Lowell, MA, we are supporting demand by equipping service providers and cloud data centres with high-performance analogue and photonic products. Our solutions deliver breakthrough gains in bandwidth density, and can target a total addressable market for physical layer interconnect components that we estimate to be a $1 billion opportunity for us.

Cloud data centres: 10 times to 100 times larger than the opportunity with service providers



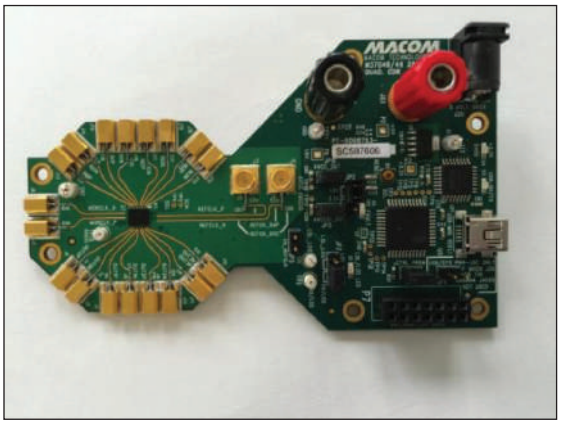
MACOM's portfolio of products in different form factors enables continued improvements in spectral efficiency and reductions in transceiver module size

Long haul and metro

Today's service providers are trying to increase the bandwidth of existing fibre links through improvements in spectral efficiency. Underpinning the move to 100G has been the use of coherent technology, and the continued evolution in dense wavelength division multiplexing, which provides the pathway to 200G, 400G and beyond.

In parallel, service providers are addressing a shortage of rack space and power by deploying increasingly compact, thermally optimized optical transceiver modules. Legacy CFP form factor products are being removed, to be replaced by today's CFP2 and the future-proof CFP4. These are just one-half and one-quarter of the size of their predecessor, respectively.

It is the analogue and photonic technology within these optical modules that determines their size and power requirements, and ultimately their competitiveness. Over the last few years we have made breakthroughs in integration and power efficiency, enabling denser module form factors. These advances have enabled us to establish a leading market position in long haul and metro networks: we estimate that we have secured a 50 percent market share for coherent modulator drivers.



The M37046: Industry leading, four-channel 25G / 28G CDR with integrated limiting amplifier

In long haul, we had our first big breakthrough with our MAOM-003405 driver, the industry's first quad-channel, surface-mount driver for 100G coherent applications. The space and power savings provided by this device have propelled the transition to smaller form factor transponders and higher density line cards, enabling service providers to achieve significant gains in bandwidth density. We continue to build on this success, with our current long haul driver portfolio giving us a 50 percent share in this market.

In the metro market, we broke new ground with the MAOM-03409B modulator driver. It is the first product to meet the size and power consumption requirements of the CFP2 analogue coherent optical (CFP2ACO) module specification, which is today's de-facto standard for metro systems.

The combination of our breakthrough surface mount packaging integration and first-to-market CFP2-ACO support has contributed to a lowering of the cost-per-bit ratio in metro applications. Here, reducing power and size ensures higher port densities, conserving valuable rack real estate. We are now providing a comprehensive range of limiting and linear drivers for QPSK and 16QAM modulation formats, and we are positioned to take more than a 75 percent design-win share in this segment. Shipments of metro products should continue to drive our growth for several years.

We believe we are well positioned for the future, and should extend our market leadership with our breakthrough products, such as the MAOM-006428, the industry's first 64 Gbaud linear modulator driver. It enables data-rates up to 600G. By increasing the data rate on a single wavelength from 100G to 600G, service providers can dramatically increase their bandwidth density while reducing their cost-per-bit.

Thanks to the strengths of our analogue and photonics technology portfolios, we expect sales of our products for long haul and metro networks to total more than $1 billion over the next five years.

Data centres: riding the tsunami

Back in 2015 data centre traffic had almost hit a staggering five trillion gigabytes, according to Cisco's Global Cloud Index, and today it will be even higher. The external traffic that enters the data centre generates a lot of data. For every kilobyte entering the data centre, an estimated 930 kilobytes of internal traffic is generated. Almost 80 percent of that traffic is East-West, or remains within the data centre, where it can contribute to a bandwidth bottleneck.

To handle this tsunami of data traffic, cloud data centre operators such as Amazon, Microsoft, Google and Facebook are rapidly increasing the capacity of their data centres, while boosting connectivity through increases in data delivery speed to 100G, 400G and beyond. Improvement to their key figure of merit, the average per-bit delivery cost, depends on realising space savings, reducing power consumption and lowering the cost in the infrastructure of their data centres.

Consequently, these cloud data centre operators are focusing on maximizing the data throughput per faceplate in their switches, while minimising cost. This effort maximises the bandwidth density, and hinges on the integration of analogue and photonic content within the module, be it a CFP, CFP2, CFP4, QSFP28, OSFP or a QSFP-DD form factor.

Another objective facing the owners of cloud data centres is to maximize the data throughput over their installed fibre in a cost-efficient manner. This is possible with advanced modulation schemes, which are efficient to implement in silicon. One leading option is PAM-4, which increases the amount of data transmitted over each existing fibre connection while reducing the cost per bit significantly.

To meet resiliency and data redundancy requirements, cloud data centres are linked together via interconnects spanning up to 100 km. These connections are rapidly moving from 100G to 400G, driving a tremendous demand for high-speed, metro-optical links. Here we hold a leading market position

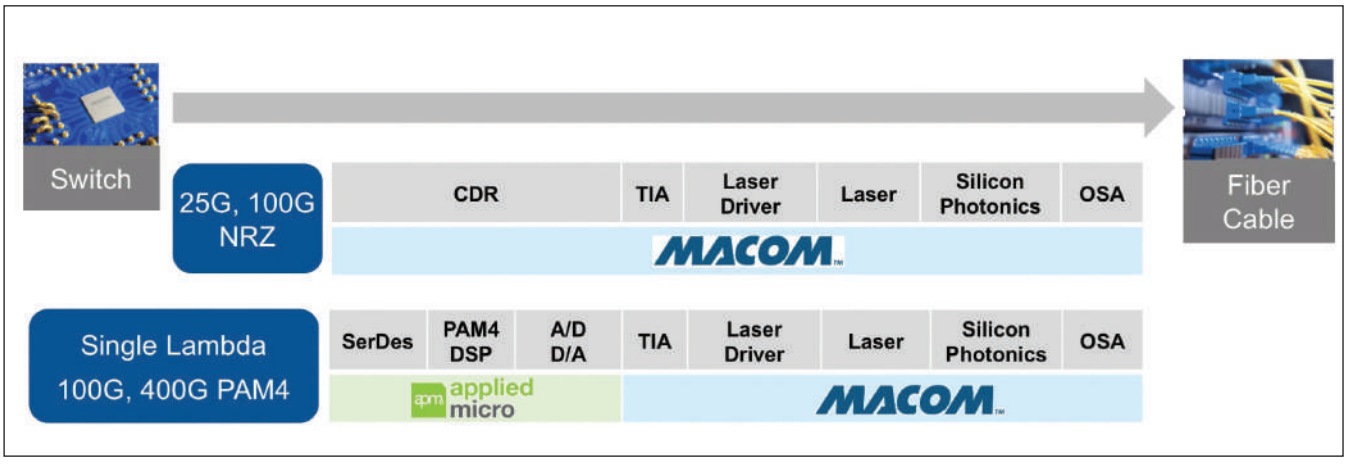
The MAOM-003401: The industry's first quad-channel, surface-mount driver for 100G coherent applications

in various product categories, including laser drivers, transimpedance amplifiers and clock and data recovery integrated circuits.

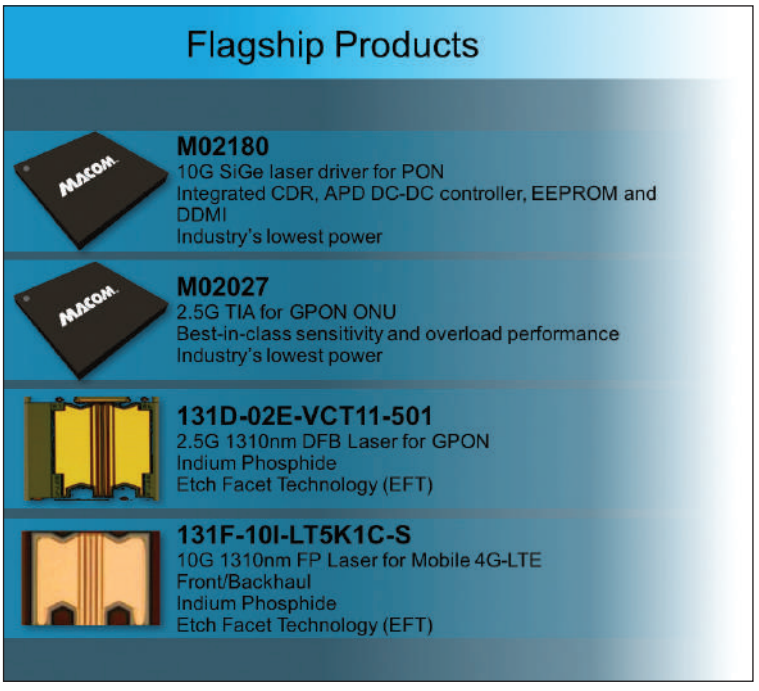
Our strong position in this sector is illustrated by our shipment of more than a million 100G modules into data centre and enterprise applications. This number exceeds the largest total addressable market reported by any market analysts to date, and stems from our leadership in long-reach and short-reach laser and VCSEL drivers, CDRs and TIAs. What's even more exciting is that this is just the beginning of a ramp in demand. Over the next four years, volumes of products supporting 100G connectivity within data centres should triple.

We believe that we already have more than a 60 percent share of the high-performance analogue content going into these applications. And this share may increase, as in the second half of this year port shipments into these applications are expected to more than double. Our view is that the growth in the 100G optical market will continue to exceed the forecast of analysts for the next two-to-three years, primarily driven by cloud data centre demand for high-bandwidth connectivity.

Building on top of this strong foundation in high-performance analogue content, while drawing on our advanced etched facet technology (EFT), we are optimally positioned to capitalize on the 100G opportunity in cloud data centres. Such a move will



The full portfolio from switch to fibre



MACOM's broad portfolio of flagship products

replicate the breakthrough we had in reducing costs in passive optical networks – this is the world's largest-unit-volume, InP-based laser market. In this cost sensitive market we estimate that we've claimed over a 70 percent share.

The inherent benefits of our EFT are embodied in our portfolio of 25G lasers for 100G cloud data centre applications. By making best use of our in-house, wafer-scale InP manufacturing, we have developed a 25G laser portfolio that is produced with cost and capacity advantages over incumbent laser suppliers. The edge that we enjoy solidifies our industry leadership, and puts us in a great position to support the explosive growth of cloud data centres.

We are now exploiting our EFT laser technology, using it to enable the seamless integration of various optical devices onto a single chip, which can feature lasers, modulators and multiplexers. We are producing the industry's first silicon photonic integrated circuit (PIC), integrated with lasers capable of 100G and beyond. By solving the key challenge of aligning lasers to the silicon PIC with high yield and high coupling efficiency, we have laid the foundation for the adoption of silicon PICs that provide high-speed, high-density optical interconnects in cloud data centres.

To strengthen our position, we acquired Applied Micro Circuits Corporation of Santa Clara, CA, in early 2017. This move enables the marriage of APM's PAM-4 100G single-lambda PHY technology, which delivers a four-fold increase in bandwidth density, with our laser-incorporating PIC technology. Combining with the PHY enables a highly streamlined 400G transceiver that quadruples data throughput over existing fibre infrastructure.

One of the key merits of this acquisition is that it creates a portfolio of PAM-4, analogue and photonic technology that positions us for PAM-4 adoption that is not limited to just 100G, but extends to 400G. There are two standards within data centres: to date everything has been NRZ, which is served by our 25G lasers, 100G laser drivers, VCSEL drivers and CDRs; and there is the emerging PAM-4 modulation, a key element moving to 400G. We believe that more than half of the industry will be moving forward with PAM-4 within data centres at 100G. As we incorporate Applied Micro's technology into our own, we will be able to combine our analogue and photonic content for the complete front-end capability, along with the DSP in the PHY with SerDes as well as data converters.

The wisdom of this approach was further advanced by the IEEE, which has unveiled standardization based on a proposal championed by Applied Micro and Cisco to implement single lambda PAM-4 as the industry standard again for both 100G and 400G.

Our expanding product portfolio for cloud data centres encompasses key protocols and spans all formats, giving us the agility to respond quickly to evolving market dynamics. Flagship products are technology agnostic, and can be readily deployed to meet the unique needs of our tier-one customers.

Thanks to our competency in many aspects of cloud data centre connectivity, we have a unique ability to provide customers with the entire optical subassembly. We are able to draw on our portfolio of transmit optical subassemblies and receive optical subassemblies, and this enables us to optimize and validate chip-level semiconductor integration and packaging. If customers lack in-house optical packaging expertise, we can assist them by providing subassembly and/or reference designs. Armed with this, customers can take advantage of our advanced optical components and speed their development of next-generation optical transceivers.

In short, our unique combination of expertise in analogue and photonics technology equips us with an unrivalled ability to provide the seamlessly integrated content required for cost-optimized optical components that light the path from 100G to 400G in long haul, metro and cloud data centres. Our role is to deliver the enabling technologies that allow our customers to lead the industry with breakthrough advancements in bandwidth density. This improves next-generation network infrastructure and transforms global connectivity.

Lighting up silicon with quantum dots

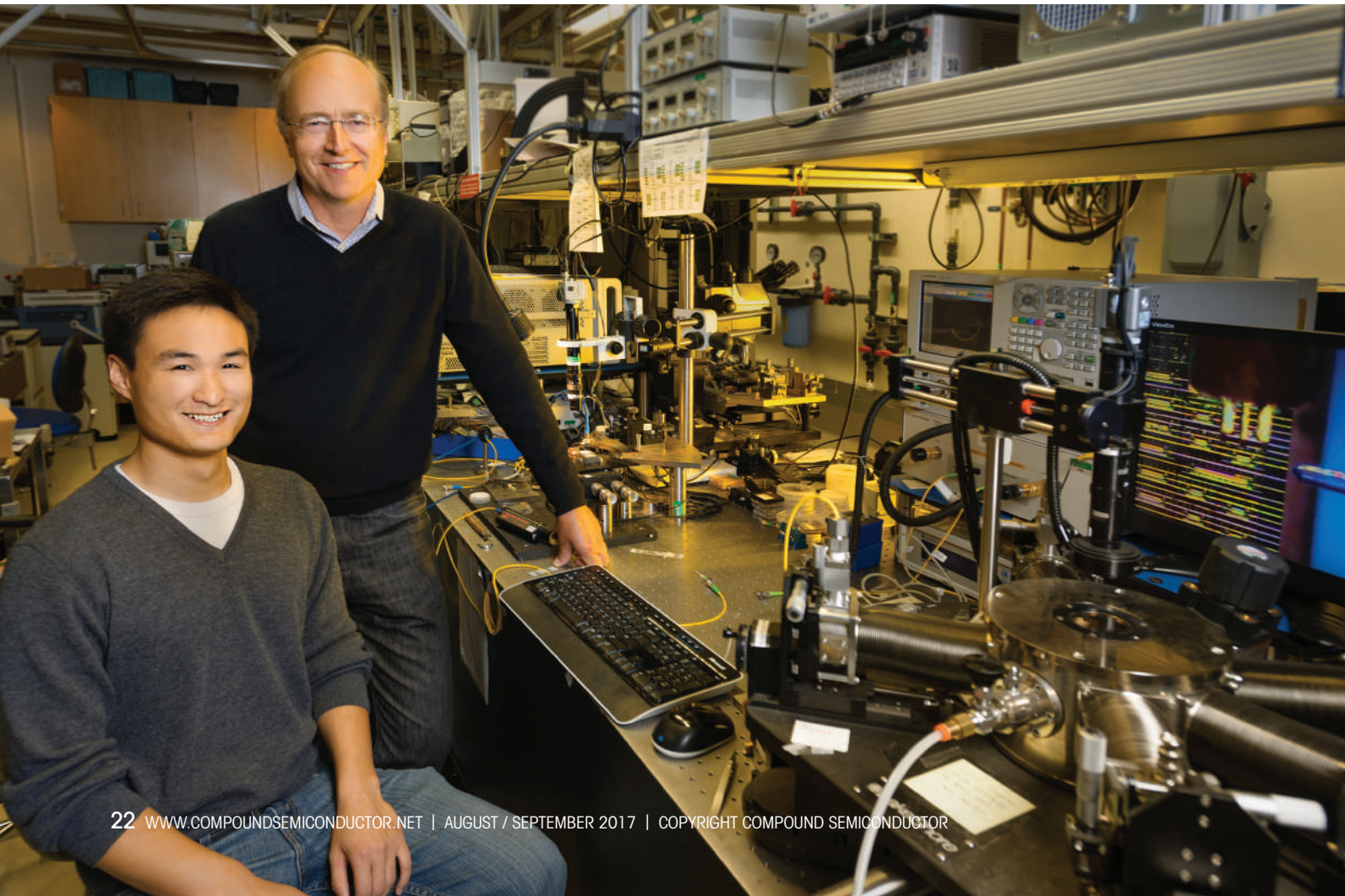
InAs quantum dots lasers are ideal for silicon photonics: they draw very little power, take up very little space, and can operate over a wide temperature range

BY JUSTIN NORMAN, DAEHWAN JUNG, YATING WAN, ARTHUR GOSSARD AND JOHN BOWERS FROM UCSB

QUANTUM DOT LASERS have a great deal of promise, and are getting better all the time. Thanks to this, they are tipped to revolutionize silicon photonics and optical technologies by enabling the scalable manufacture of densely integrated photonic systems on a single chip.

Merits of the quantum dot laser include its small form factor, low power consumption, and multi-functionality. These attributes have great appeal, and could allow this laser to serve in various applications, including: datacentre and high-performance computing interconnects; chemical and bio-sensors for medical diagnostics; leak detection; and security purposes, in highly precise, GPS-free navigation systems.

All these opportunities arise through the absence of an efficient silicon light source for silicon photonics.



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  What form will 5G take? And how good will 5G be for GaAs and GaN?
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  Which sectors offer the best returns? Does the bottom line get the biggest benefit from streamlining manufacturing, or from optimising the chip?
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Richard Stevenson, Programme Manager and Editor of Compound Semiconductor

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CS INTERNATIONAL CONFERENCE

Connecting, informing and inspiring the compound semiconductor industry

	GaN	InAs	InP	GaAs	SOI	Silicon
Substrate Cost ($/cm^2)	144.41	18.25	4.55	1.65	1.30	0.20
Maximum size (mm)	51	76	150	200	450	450

Table 1. The cost of native substrates for laser growth is far higher than that for silicon, while size is more limited.

This material is plagued by an indirect bandgap, making it a poor light emitter. Despite much effort, researchers are yet to produce an electrically injected silicon laser delivering continuous-wave output at room temperature.

Getting III-Vs onto the chip

Today, engineers within the silicon photonics community address this weakness through the heterogeneous integration of III-V materials. This includes the growth of laser materials on III-V substrates, followed by bonding to patterned silicon-on-insulator (SOI) substrates. CMOS processes turn the bonded material into laser cavities, which are aligned with silicon waveguides in the SOI active layer. The light that is generated by the quantum dot laser is evanescently coupled into the waveguide, and routed to other photonic components.

One of the strengths of this approach is that it can yield complex photonic integrated circuits with hundreds of high-performance, on-chip components. However, there are downsides: manufacturing scalability is limited; bonding adds complexity; and as the III-V substrates used for laser growth are removed and discarded after bonding, this adds significantly to production costs (see Table 1 for details).

A far better approach is to form the lasers via the direct growth of III-Vs on silicon. However, this is challenging, because the inherent mismatch in lattice constant between the two materials spawns a high density of threading dislocations, which propagate in the growth direction and act as non-radiative recombination centres, hindering laser performance.

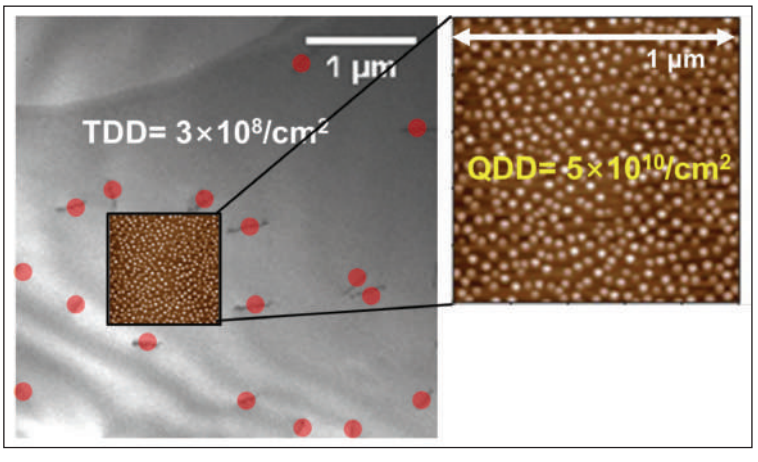

Figure 1. Plan-view transmission electron microscopy of GaAs grown on silicon. Red dots indicate threading dislocations. The inset, an atomic force microscopy image of a layer of InAs quantum dots, illustrates their relative density compared to dislocations.

In addition, two more obstacles must be addressed to enable a commercially viable performance from the quantum dot laser: the polarity mismatch between silicon and the III-Vs, which drives the formation of antiphase domains that act as extended planar defects; and a mismatch in the thermal expansion coefficients. The latter results in more defects, and imparts a residual strain as the wafer cools from the growth temperature to room temperature. Due to a hike in defects, degradation increases and device lifetime shortens.

Fortunately, it is possible to produce efficient III-Vs lasers on silicon by turning to InAs quantum dots. Devices incorporating these low-dimensional structures feature particle-in-a-box like carrier confinement, making them inherently tolerant to defects. As these charge carriers are confined within a plane and trapped by quantum dots, they don't tend to diffuse to a defect, so non-radiative recombination diminishes. Note that the likelihood of trapping a carrier by a dot rather than a defect is very high: the dot density is typically 4-6×10^{10} cm^{-2}, while defect density is no more than 10^8 cm^{-2} (see Figure 1 for an illustration of this concept).

Another attribute of the InAs quantum dot laser is its ability to span a very wide spectral range. Careful selection of the dots' size and cladding composition allows sources to produce an emission wavelength from around 1 μm to 1.6 μm. This wide range enables devices to serve datacom and telecom applications.

The tremendous tolerance of the quantum dots to defects is highlighted in photoluminescence measurements of various structures on native and foreign substrates. While the dots grown on silicon do not deliver the intensity they would do on a native substrate, they emit far more light than wells grown on the same foundation (see Figure 2). The recombination characteristics are so good that they can be used to make high output power lasers with low thresholds. In comparison, devices made from quantum wells grown on silicon fail to lase.

While defects don't prevent the lasing of quantum dot lasers, their presence is still undesired. They do impact lasing performance by impairing material quality, and they should be managed as far as possible in III-V nucleation and buffer layers deposited on the silicon substrate.

Historically, the heteroepitaxial growth of III-Vs on silicon has been undertaken on planar (100) silicon with a 2-6° miscut in the surface orientation toward the [111] direction. This geometry is favoured, because

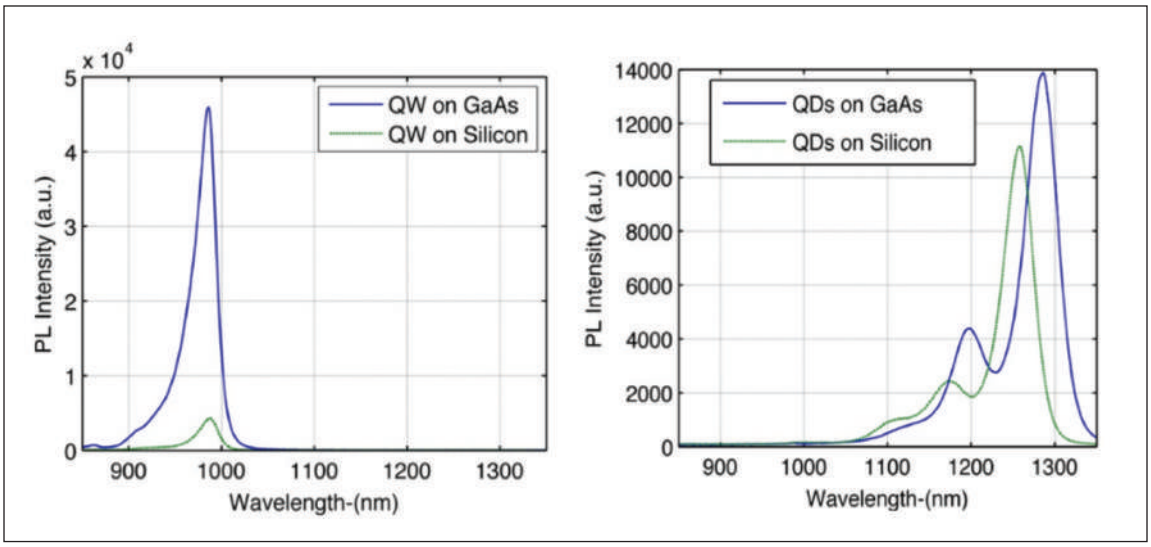

Figure 2. Photoluminescence spectra of as-grown InGaAs quantum well (QW) and InAs quantum dot (QD) material on GaAs and silicon substrates. Switching from a native to a foreign substrate leads to significant degradation in material quality for the QWs.

it makes the formation of double atomic steps on the silicon surface energetically favourable. This inhibits antiphase domain formation and improves material quality. However, there is a significant downside: the miscut silicon is incompatible with the CMOS platform, preventing wafers formed in this manner from enjoying the manufacturing advantages needed to drive silicon photonics.

A two-pronged attack

To address this weakness, our team at the University of California, Santa Barbara, has started to develop growth techniques for III-Vs on CMOS-compatible, on-axis (001) silicon. Working in partnership with researchers at other universities, we have pioneered two different approaches: the use of a 45 nm GaP-on-silicon template for the regrowth of GaAs; and the patterning of silicon with {111} v-groove trenches, followed by the direct growth of GaAs, which coalesces to form a smooth GaAs-on-silicon template. Both approaches, and the success they have delivered, are discussed in the remainder of this article.

For the first of these two approaches, Minjoo Larry Lee's group at the University of Illinois at Urbana-Champaign has pioneered the initial development of GaAs/GaP/silicon. Our role has been to continue this work.

Efforts with this GaP-on-silicon template make use of a highly developed process developed by NAsP$_{III/V}$ GmbH of Marburg, Germany. The technology is based on the growth, by MOCVD, of nearly lattice matched GaP on silicon. By carefully controlling the silicon surface preparation and nucleation conditions, uniform, smooth, defect-free GaP-on-silicon can be realised across a full 300 mm wafer with a GaP thickness of only 45 nm.

We and our colleagues have used these commercial, engineered substrates as the foundation for MBE growth of InAs quantum dot lasers. With the antiphase domain issue solved at the GaP/silicon interface, we only have to contend with dislocations arising from lattice mismatch between GaAs and GaP. Threading dislocations densities of 3×10^8 cm^{-2} have been

The tremendous tolerance of the quantum dots to defects is highlighted in photoluminescence measurements of various structures on native and foreign substrates. While the dots grown on silicon do not deliver the intensity they would do on a native substrate, they emit far more light than wells grown on the same foundation

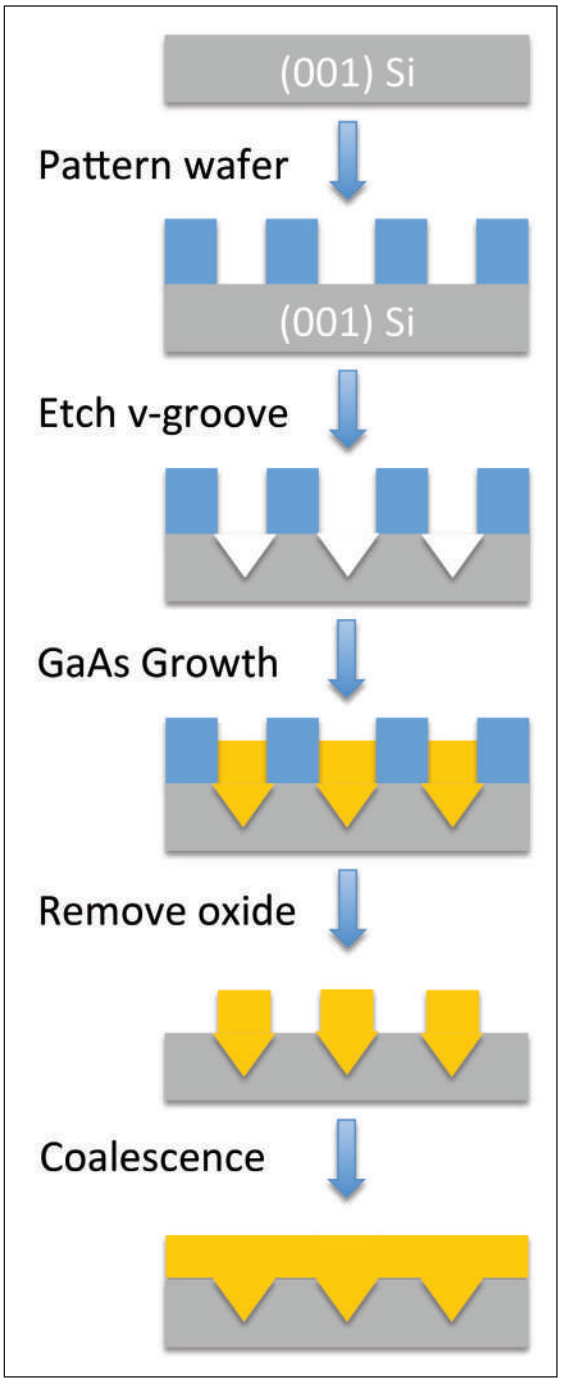

Figure 3. The growth procedure for producing GaAs on a v-groove silicon (GoVS) template.

realised in our lasers, with performances detailed in the scientific literature. By refining the growth conditions and introducing dislocation filtering layers, dislocations can be far lower – now they are down to 6×10^6 cm^{-2}, and even lower values may follow as further optimization is in progress. A point of reference is the threading dislocation densities in commercial III-V substrates: it is typically of the order of 10^4 cm^{-2}.

The other approach that we are pursuing – growth of GaAs on v-grooved silicon – is being undertaken through a collaboration with Kei May Lau's group at the Hong Kong University of Science and Technology (HKUST). With this approach, the primary benefits are that the v-groove {111} surfaces suppress antiphase domain formation and it relaxes the strained GaAs material, largely through stacking fault formation, without generating high threading dislocation densities.

Proceeding in this manner, 300 mm CMOS-compatible silicon wafers are patterned with oxide delineated trenches 90 nm wide, separated by 40 nm SiO_2 stripes (see Figure 3). These wafers are diced, etched in potassium hydroxide to create crystallographic {111} v-grooves, and loaded into an MOCVD chamber for the regrowth of GaAs, which forms nanowires. Following *ex-situ* removal of the oxide, further growth of GaAs causes nanowires to coalesce and yield smooth films. The inclusion of AlGaAs/GaAs superlattices smooths the film and filters defects, enabling higher material quality.

With this series of steps we have formed structures that have a dislocation density of 7×10^7 cm^{-2} in the final 1.5 μm of the film. Surface roughness, judged in terms of the root-mean-square value, is just 0.9 nm. As with the GaAs/GaP/silicon templates, growth conditions are refined day by day. Threading dislocation density has now fallen to the low 10^7 cm^{-2} range, with a stacking fault density of 2×10^7 cm^{-2}.

Making lasers

Quantum dot lasers emitting near the datacom wavelength of 1.3 μm have been grown and fabricated on templates just described. MBE growth forms the heterostructures, while standard CMOS-compatible etching, deposition, and lithography processes define the architecture.

One feature of our design is the use of top *p*-contact and bottom *n*-contact layers within an AlGaAs graded-index separate-confinement heterostructure, which provides optical and electronic confinement to the active region (see Figures 4 and 5). At the heart of these devices are multiple layers of InAs quantum dots within $In_{0.15}Ga_{0.85}As$ quantum wells that assist in carrier capture.

We have produced a range of devices, including those with a narrow ridge, a broad area, and a micro-ring based laser cavity. Ridge lasers range from 2 μm to 50 μm in width and 500 μm to 3000 μm in length, while micro-rings combine outer diameters of 5 μm to 50 μm with widths of 2 μm to 7 μm. The micro-ring devices enter new territory by providing the first demonstration of micron-scale laser cavities in epitaxial material on silicon. Note that the ridge devices were fabricated on both of the III-V-on-silicon templates, but micro-rings were only fabricated on V-groove based substrates (see Table 2 for a summary of the template and epi design parameters, and Figure 6 for images of fabricated devices).

All of these devices can deliver continuous wave emission under electrical injection. For the ridge lasers on GaP/silicon, *p*-modulation doped active layers are

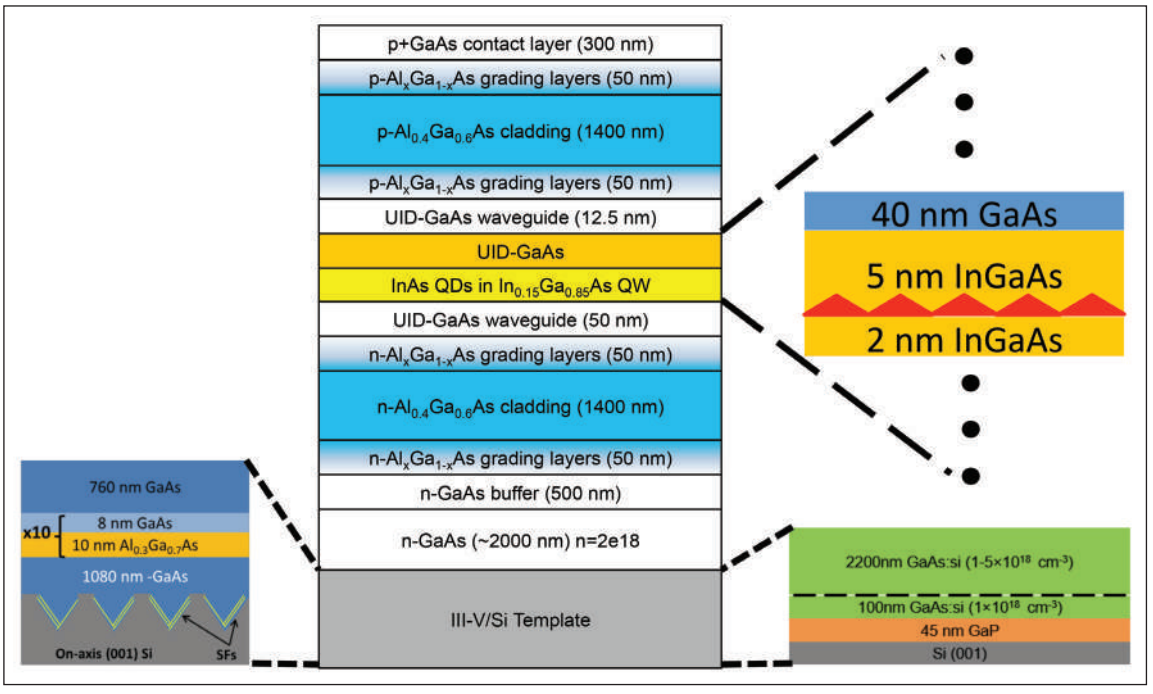

Figure 4. The laser epi structure, including the multilayer active region, and two III-V/silicon template designs.

incorporated to improve high-temperature performance. This comes at the cost of a higher threshold current.

We have fabricated and measured hundreds of devices, formed using the three designs and two templates (see Table 3 for a summary of the best lasing characteristics).

All devices have a low threshold current design. In ridge lasers they can be as little as 30 mA, while for a 5 μm micro-ring they can be a record-setting 0.6 mA. Note that the previous record for low threshold, held by our team for efforts in 2014 on miscut silicon, was 16 mA.

Ridge devices are capable of a single-facet output power in excess of 100 mW, and can produce continuous-wave lasing from the quantum dot ground state at temperatures of up to 80 °C. In comparison, micro-ring devices can achieve this feat up to 100 °C. Unfortunately, with this class of laser, an accurate output power cannot be extracted from the micro-ring without an additional out-coupling structure to guide the light. Instead, output powers have to be simply measured from what is scattered from the ring sidewalls into an adjacent integrating sphere. This is only a small fraction of the total scattered light.

If quantum dot lasers are to serve any practical application, they must combine high performance with high reliability. Fortunately, the signs are promising. Our devices formed on miscut silicon have demonstrated extrapolated lifetimes of more than 4,000 hours at 30 °C and a high current density of 1.1-1.2 kA cm^{-2}. Far longer lifetimes of more than 100,000 hours have been determined in separate work at University College London, using the relaxed condition of 130 A cm^{-2}.

While these results are very encouraging, the defect density for on-axis templates is still higher than it is with miscut silicon. So more work is needed to propel performance, so that these devices deliver a commercial lifetime of 10,000 hours at conditions relevant to a given application, such as operation at 80 °C for datacentre and high-performance computing applications. To put these requirements in perspective, the preliminary results for our ridge lasers on the GaP/silicon templates reveal a lifetime in the several hundred to 1,000 hour range at 30 °C, using a drive current of a few kA cm^{-2}.

Given the combination of promising lifetimes, low threshold currents and high output powers, it is clear that epitaxial III-V materials and devices show significant promise for silicon photonics. Results to date by our team are ground-breaking, and they

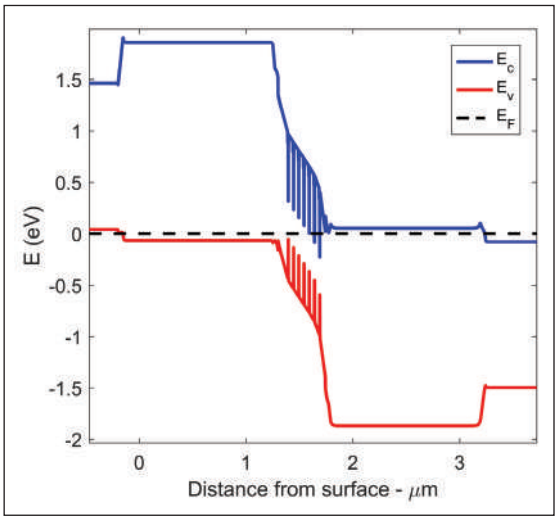

Figure 5. The band diagram for laser material at zero-bias.

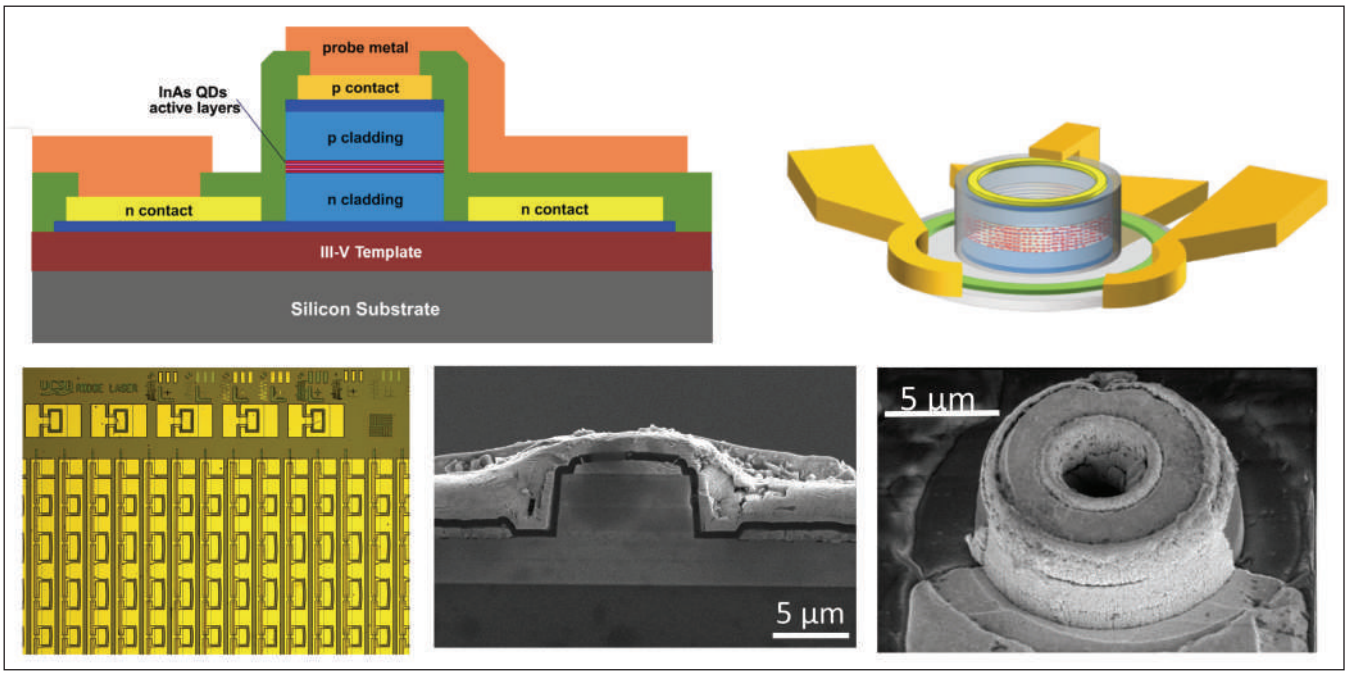

Figure 6. The structure of a Fabry-Pérot ridge laser (top left) and a micro-ring laser (top right). A top-down optical micrograph of ridge lasers on a chip (bottom left), and scanning electron microscope images of a ridge cross-section and top-down of a micro-ring laser with 5 µm radius (bottom middle and bottom right, respectively).

		GaP/Si	GoVS	Micro-ring on GoVS
GaAs template	TDD	3×10^{8} cm^{-2}	7×10^{7} cm^{-2}	7×10^{7} cm^{-2}
	SFD (cm^{-2})	N/A	2×10^{7} cm^{-2}	2×10^{7} cm^{-2}
	AFM RMS roughness	5 nm	0.9 nm	0.9 nm
Active region	# of QD layers	7	5	7
	p-doping (cm^{-3})	5×10^{17}	N/A	5×10^{17}

Table 2. A comparison of the epi parameters for quantum dot lasers formed on GaP-on-silicon and on GaAs grown on v-groove silicon.

	GaP/Si	GoVS	Micro-ring on GoVS
λ at RT	1280 nm	1250 nm	1300 nm
Lowest I_{th} (CW RT)	30 mA (3×750 µm^2)*	36 mA (6×1200 µm^2)*	0.6 mA (5 µm radius, 3 µm width)
Lowest J_{th} (CW RT)	862 A/cm^2 (20×2000 µm^2)	498 A/cm^2 (12×1000 µm^2)*	1 kA/cm^2 (5 µm radius, 3 µm width)
Output power (CW RT)	110 mW (20×2000 µm^2)	107 mW (8×1200 µm^2)*	N/A
Max T (CW)	80 °C	80 °C	100°C (50 µm radius, 4 µm width)

* Indicates HR coated devices.

Table 3. Results for lasers formed on silicon are promising, with micro-ring lasers delivering ground-breaking threshold currents.

should continue to improve as our material gets better and better. Note that since obtaining these results, the defect density in the GaP/silicon template has fallen by nearly two orders of magnitude, while the v-grooved template is making similar progress. Spurring on performance improvement is continual refinement to laser designs at the device and epi level. This should lead to much lower threshold currents, higher output powers, and higher-temperature CW operation.

When ready, transfer of our technology to a manufacturing environment should be relatively easy, as we have obtained our results on CMOS-compatible 300 mm silicon substrates, diced to fit research-scale growth reactors, and undertaking processing of the laser material with standard CMOS lithography and etching techniques. We are confident that our small-footprint micro-ring structures can realise high integration densities, with coupling of these sources to waveguides with established silicon photonics designs. This will allow direct integration of our ground-breaking lasers with existing components and other epitaxial III-V devices.

Further reading

A. Liu *et al.* Photonics Research **3** B1 (2015)
A. Liu *et al.* Optics Letters **42** 338 (2017)
J. Norman *et al.* Optics Express **25** 3927 (2017)
Y. Wan *et al.* Sub-mA threshold 1.3 µm CW lasing from electrically pumped micro-rings grown on (001) Si, CLEO: Applications and Technology. Optical Society of America, 2017

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An abundance of key elements

If demand for GaAs, InP and germanium substrates grows, it can be fulfilled, thanks to sufficient availability of gallium, germanium, and indium

BY MAX FRENZEL FROM THE HELMHOLTZ INSTITUTE FREIBERG FOR RESOURCE TECHNOLOGY

WE TEND TO THINK OF the substrate as the starting point for chip production. Much thought is given to the selection of its size, orientation, and doping level; there can be haggling over its price; and it is the foundation for the growth of epilayers that form the heart of the device.

But there is another way to look at this, where the substrate is not the starting point. Instead, the production of any chip begins further back, with the mining of raw materials, and the extraction of elements that are used to produce substrates and metal-organics.

Viewed in this light, a first glance would suggest that our industry is in a rather precarious position. That's because many of our key elements – including gallium, indium and germanium – are not the primary focus in mining operations. Instead, they are produced exclusively as by-products, extracted from the ground when mining major industrial metals. For example, the mining and processing of aluminium ores accounts for most gallium production. The by-products are worth far less than their host materials, so they do not impact mining or production decisions – and their primary production is strongly limited by the production of the host materials.

Nevertheless, over the past decades, the primary production of many by-products has been growing far faster than that of their corresponding hosts (see Figure 1). This raises the question of how sustainable such accelerated growth is. Any slowing would be a concern, as it could potentially apply the brakes to a ramp up in chip production.

The most common approach to evaluating the stocks of industrial metals is to determine the levels of reserves and resources. But when it comes to by-products, this approach is flawed. Instead, the amount of available by-product is determined by what can be recovered from the extracted host-ore streams. This is not well-known, but while the primary production of some by-products lagged the theoretical capacity in the 1970s, this is not necessarily true today.

A reliable figure for how much gallium, germanium and indium is available cannot be determined with back-of-the-envelope calculations. Instead, it requires a more sophisticated approach, considering both the supply potential and the supply curve, terms that will be explained in due course.

Taking this tack, our team at the Helmholtz Institute Freiberg for Resource Technology has found that plenty of affordable gallium, germanium and indium should be available for the compound semiconductor industry for the foreseeable future.

Supply potentials

To determine the availability of a by-product, one must know its supply potential. This corresponds to the amount of by-product that can be economically extracted per year from the ongoing primary production of relevant host ores, depending both on price and extraction technology. Due to these economic and technological constraints, the supply potential is always far less than the total amount of the by-product contained in host-ore streams.

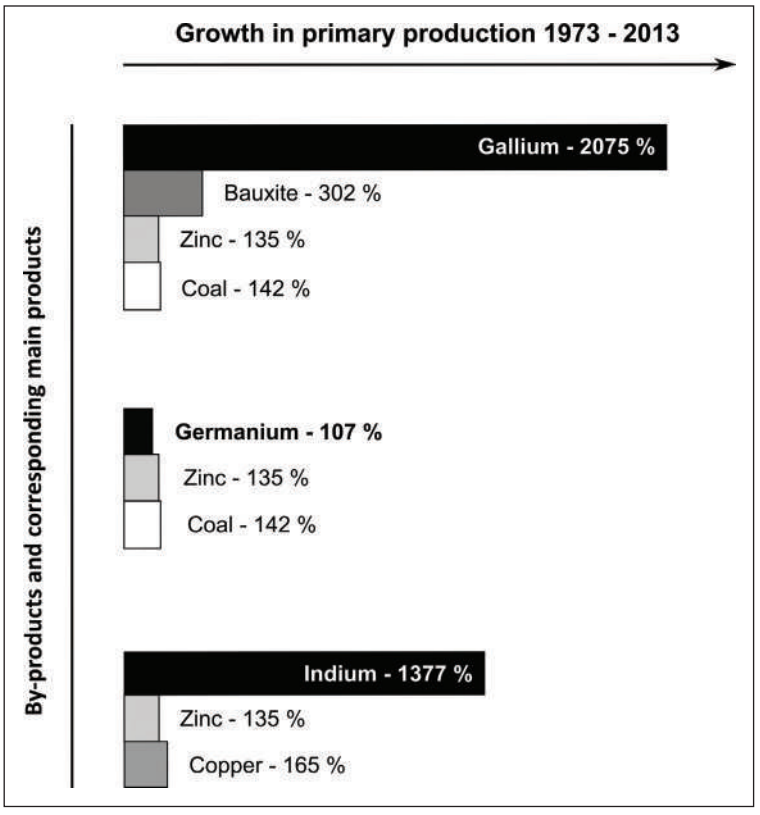

Figure 1. Relative growth in the primary production of gallium, germanium and indium from 1973 to 2013, compared to their corresponding host materials. Reproduced from M. Frenzel *et al.* Resour. Policy **52** 327 (2017).

Whether it is worth extracting a by-product from a given batch of host ore is governed mostly by its concentration. Essentially, extraction is only feasible above a certain threshold concentration, the so-called cut-off grade. The concentrations of different by-products vary significantly across different mines, so not all mines are suitable sources for a given by-product (for example, see Table 1, listing compositions of zinc concentrates from different mines). Furthermore, mines also vary greatly in terms of their annual production volumes.

Due to the innate heterogeneity of geological materials, and variations in the size of mines, it is impossible to produce a sensible estimate of the supply potential by multiplying the total annual volume of a host-ore stream with an average concentration of the by-product, and perhaps an estimated recovery. Instead, supply potentials must be calculated on a mine-by-mine basis. The sum over all relevant mines then gives the global total.

Table 1. Gallium, germanium and indium in zinc ore concentrates from different mines. Data from M. Frenzel *et al.* Ore Geol. Rev. **76** 52 (2016).

Mine/Deposit	Gallium (ppm)	Germanium (ppm)	Indium (ppm)
Bleiberg	26	344	< 1
Groundhog	< 1	< 1	30
Toyoha	180	3	3,700
Tsumeb	200	240	< 1

Unfortunately, it is not quite as easy as that in reality. The stumbling block is the general lack of publicly accessible data on the composition of mined ore concentrates. Due to this, supply potentials can only be assessed probabilistically. We have approached the task in this manner. Using probability distribution functions for concentrations of by-products in host ores from different geological types of mines, we have constrained the probable range of supply potentials with Monte Carlo simulations.

Estimates of the probability distribution functions were made using analytical data from the scientific literature. We considered the following host ores: bauxite (gallium), sulphidic zinc ores (gallium, germanium, indium), coal (gallium, germanium) and sulphidic copper ores (indium). This approach has much merit, as it closely mirrors current primary production sources.

Estimated supply potentials for gallium, germanium and indium are shown in Figure 2, showing that they significantly exceed current production. According to our results, gallium and germanium production could increase at least five-fold and indium production could double, assuming factors such as price and technology remain the same.

This begs the question of why there is such a large discrepancy between current production and supply potentials. Primarily, it results from a lack of extraction capacity at the smelters. Here, the focus is on the core business of extracting the main products, so investment tends to be directed at either increases in main-product capacity or efficiency improvement, rather than improving the extraction of by-products.

Another factor at play is the limited demand for these by-products. Their markets are relatively small, so the installation of extraction capacity at a large smelter could have unwanted consequences: it could easily result in oversupply, driving down prices and leading to financial losses for the smelter.

Such a scenario is by no means inconceivable, given the sensitivity of these markets. This is illustrated by the collapse of Fanya Metal Exchange in China in 2015 that led to a tumbling of the indium price. The collapse eliminated a relatively large buyer, creating a considerable oversupply of indium, and ultimately depressing prices in recent years. If a new producer entered the market, a similar effect could take place.

Future availability

Supply potentials vary with market conditions because they depend directly on the interplay of concentration, extraction technology and market price. Therefore,

stationary estimates of supply potentials are of limited use for considerations of future availability.

Producing supply curves for gallium, germanium and indium allows us to understand how availability might evolve in the future. These plots, examples of which are given in Figure 3, show how higher market prices can support extraction from lower-grade materials, and therefore correspond to higher values of the supply potential. Any improvements in technology will shift the curves downwards, since they lower extraction costs. This also equates to an increase in supply potential, but at constant prices.

The supply curves have an inelastic region where the price does not affect the supply potential (the vertical parts of the curves). When considering future availability, it is important to know how far the current supply potentials are away from this inelastic region. According to Figure 3, gallium from bauxite is clearly in the elastic region, while germanium and indium (from sulphidic zinc ores) are very close to the inelastic part. The implication is that it should be easy to increase the gallium supply potential in the future, and more difficult to increase supply potentials for germanium and indium. As indium also has a more limited current supply potential than the other two, it will be the hardest to provide a major increase in future production.

This situation could change markedly if there is a significant hike in the price, making the by-product as valuable as the main product in the corresponding host ores. In this scenario, denoted by the 'break-down points' in Figure 3, the by-product supply curves cease to apply, with higher production coming from mines producing these elements as their main products. It is worth noting that the break-down points only occur well into the inelastic supply regime. The implication is that it would take a significant price-hump to expand production beyond by-product limits.

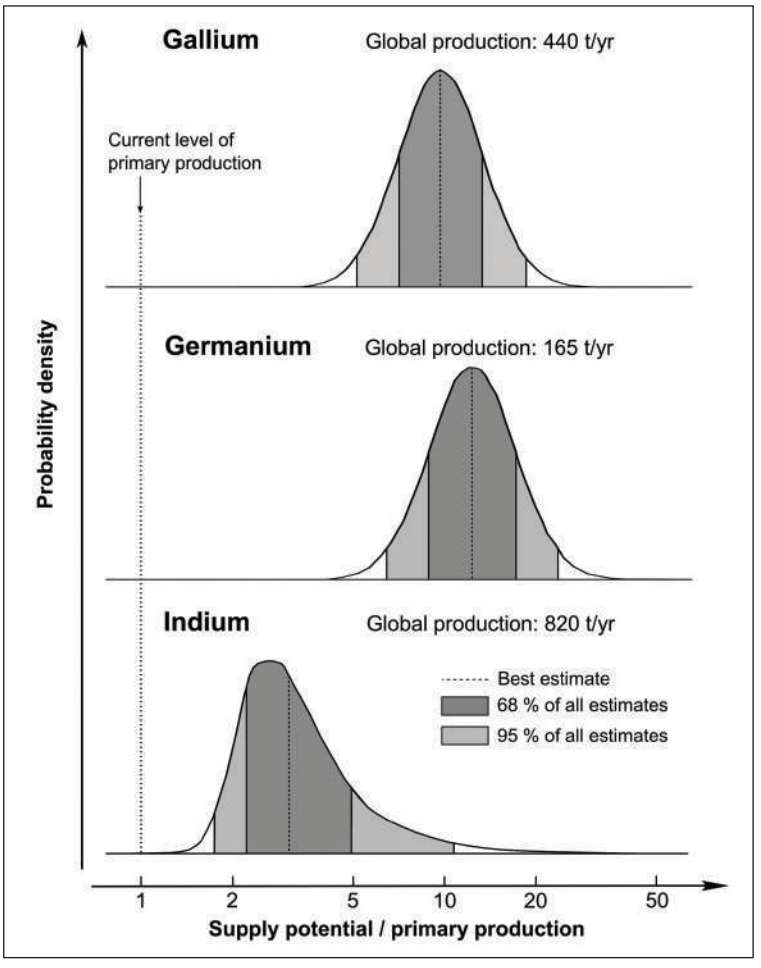

Figure 2. Probability distribution functions, based on Monte Carlo simulations, describing estimated supply potentials of gallium, germanium and indium relative to current primary production (for the year 2014). The probability distribution functions are normalised to the current primary production of these elements. Note that a value of 2 on the *x*-axis corresponds to about double current primary production. (Graphs adapted from M. Frenzel *et al.* Resour. Policy **52** 327 (2017)).

Implications

A key finding emerging from our work is that there are currently no issues of availability associated with gallium, germanium or indium. What's more, given the relatively large potential for future increase in the supply of these elements, it is improbable that such issues will develop over the next decade. If there are to be any constraints in the longer term, they will most likely arise with indium, due to its comparatively limited capacity for increases in primary production.

Our findings may be integrated into product design studies that assess whether raw material availability has the potential to constrain the market penetration of a particular product. Consider, for example, one of the biggest potential consumers of indium: the copper-indium-gallium-selenide (CIGS) thin-film solar cell. This class of photovoltaic, which has a current maximum conversion efficiency of about 20 percent, typically requires 2.5 g of indium for every square

Sphalerite (with chalcopyrite) zinc ore, a source of gallium, germanium and indium

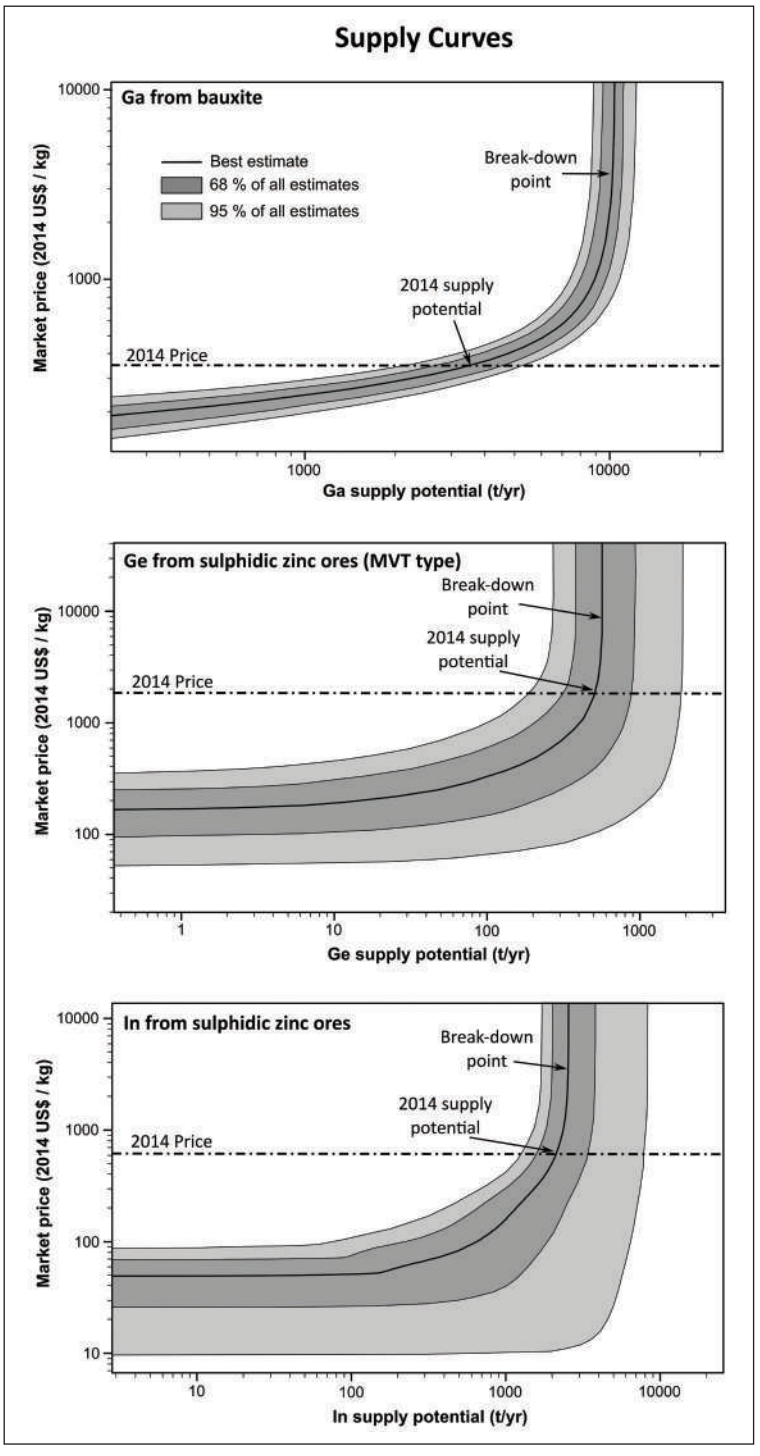

Figure 3. By-product supply curves of gallium, germanium and indium from different raw materials for the year 2014. The extractable amount is ultimately limited by the total amount of by-product contained in host ore streams. This is reflected in the sharp rise towards the right-hand side of the curves. The vertical part of the curves is called inelastic. Data is taken from M. Frenzel *et al.* Resour. Policy **47** 38 (2016); M. Frenzel *et al.* Resour. Policy **46** 45 (2015); and M. Frenzel *et al.* Resour. Policy **52** 327 (2017).

Element	Supply potential (tonnes/year)
Gallium	5,200 (2,900 – 10,400)
Germanium	2,000 (1,200 – 4,300)
Indium	2,500 (1,500 – 9,200)

Table 2. The global supply potentials of gallium, germanium and indium in 2014. Data from M. Frenzel *et al.* Resour. Policy **52** 327 (2017).

metre. Strengths of these cells include a lower cost than traditional crystalline silicon and less energy intensive production. Of the four elements in the device, indium has the lowest supply potential.

To prevent major climate change, about 4000 GW_p of photovoltaic capacity must be installed by 2040, according to the International Energy Agency (IEA). This equates to 20,000 km^2 of cells with an efficiency of 20 percent. So, if CIGS cells were used exclusively to hit this target, 175 GW_p of them would have to be installed each year. This would require 2,200 tonnes of indium per annum.

Is this feasible? Well, 2,200 tonnes is about three times current primary production, and about 50 percent higher than the current minimum supply potential of indium, which is 1,500 tonnes per year (cf. Table 2). Note also that there are other applications that consume a significant amount of indium.

Consequently, one must conclude that CIGS technology may not be capable of providing the lion's share of the required solar panel installations. However, it can still have a role to play: the availability of indium is high enough to support a significant share (tens of percent) of this technology in the global photovoltaic market.

While gallium, germanium and indium may be the most important metals in the compound semiconductor industry, they are not the only ones. For example, there is also tellurium, the group VI metal used in long-wavelength detectors. It might have a significantly more limited supply potential, but this is hard to tell, because there is currently a lack of reliable quantitative data. Consequently, there is more work to do.

Further reading

G. A. Campbell, Resour. Policy **11** 267 (1985)
F.-W. Wellmer *et al.* Raw Materials for New Technologies, Proceedings of the 5th international symposium, Hannover, pp 71-122 (1992)
M. Frenzel *et al.* Resour. Policy **46** 45 (2015)
M. Frenzel *et al.* Resour. Policy **47** 38 (2016)
M. Frenzel *et al.* Resour. Policy **52** 327 (2017)

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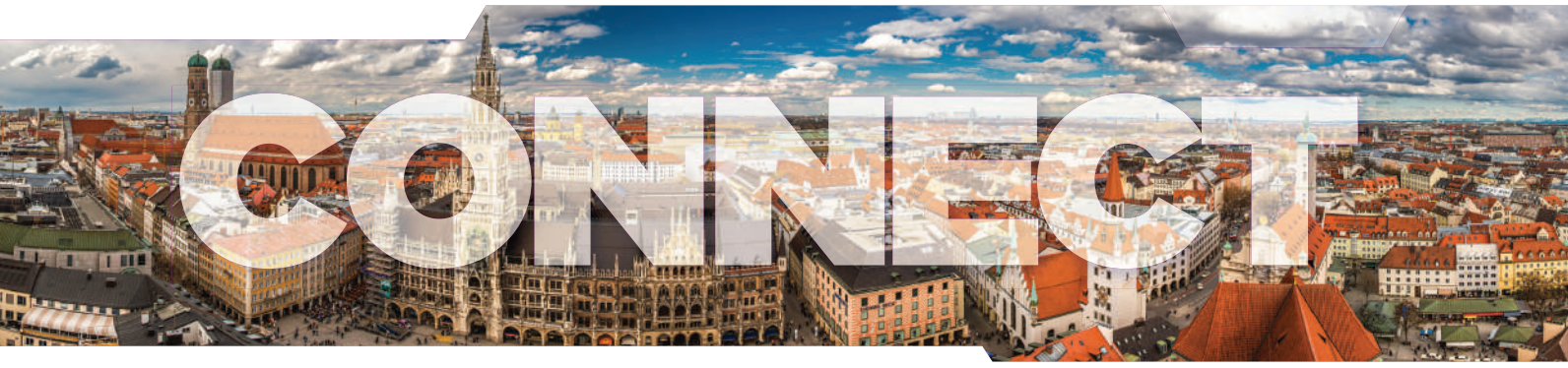

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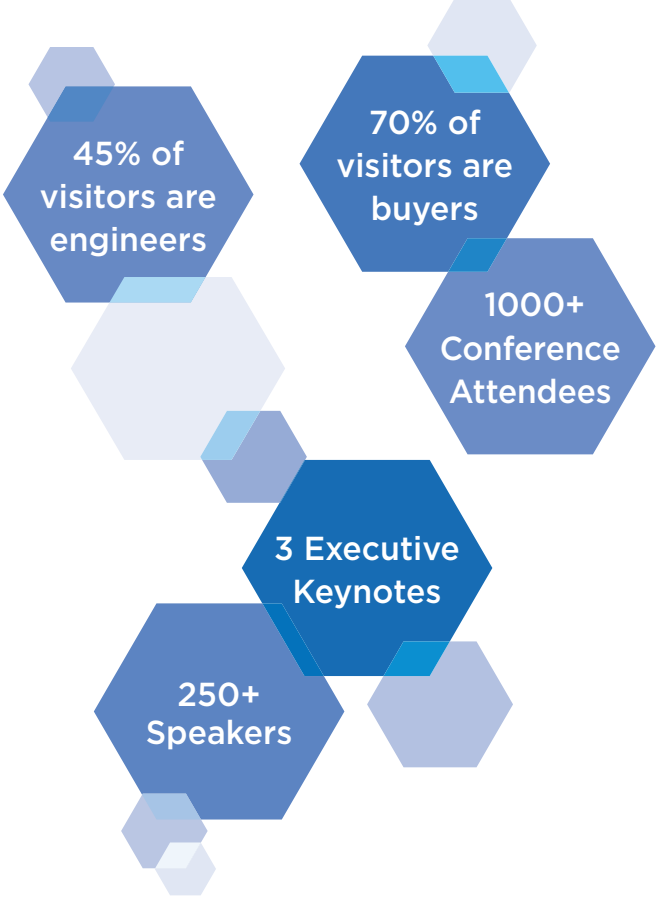

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So, what do you do?

Do you dread trying to explain what we do as an industry? If so, try re-counting Bob Johnstone's new book on the LED lighting revolution

BY RICHARD STEVENSON

WHEN you're introduced to someone new at a party, it will not be long before they'll be asking you what you do for a living.

Even if you've been asked this countless times before, it is not easy to know what to say. And it's particularly tough if you don't know their line of work: maybe they are technical, or maybe there not. So it might be best to begin by saying that you work in the compound semiconductor industry, and see what follows.

If they don't have a science or engineering background, you'll probably draw a look that convinces you that you've lost them. But you can probably regain their interest by mentioning the LED light bulb, the new kid on the block at their local hardware store.

Assuming that works, it is definitely not the time to tell them about two hotly debated issues within our industry: the green gap and the cause of droop.

Discussing the quantum confined Stark effect, Auger recombination and electron spillover is likely to bore them to tears – and will do nothing to promote the importance of our industry.

Far better is to tell the story of the evolution of the LED. Not easy, maybe, but fortunately we'll assume that you are up to the task, having just read Bob Johnstone's latest book: *L.E.D. A History of the Future of Lighting*.

Before you can start you are asked if the LEDs used in the portable radios and stereos of yesteryear have anything to do with today's lighting.

Recalling parts of Johnstone's book, you offer a compelling answer. You point out that back in the 1990s the prevailing view within the LED industry was that these devices would only ever be indicators, despite their increasing efficiency; and makers of light bulbs didn't see LEDs coming. In that era it took a visionary to see the potential of the LED as a source of lighting.

Telling the tale of the transformation of the LED is easy after reading Johnstone's book. You engage your companion with a description of the visit in the early 1990s of Roland Haitz, head of Hewlett Packard's Semiconductor Products Group that made leading LEDs, to Ton Begemann at Philips. At the time Philips was a world-leading lightbulb manufacturer, with Begemann tasked with identifying technology trends.

You explain that during the meeting Haitz had a tour of Philip's Lighting Laboratory. Haitz, an expert in LED manufacturing, knew nothing about lighting – but he was learning fast. And while he learnt from Begemann, Begemann badgered him for details of current LED efficiency, and how fast it was improving.

These questions got Haitz thinking, and it was not long before he dug out a couple of decades of historical performance data. Plots revealed that with the passing of every decade there is a ten-fold reduction in the price per lumen and a twenty-fold hike in output power. Extrapolation indicated that LEDs would be competitive with conventional lighting by 2005.

At that point Haitz started to consider the energy savings that could result from a switch to LED lighting. The gains were phenomenal. In the US, replacing just half of the incandescent and halogen bulbs with LEDs would trim annual electricity bills by nearly $10 billion.

However, making this happen would not be easy. Haitz figured out that it would take billions of dollars of investment in the LED industry, and that was only going to happen if efforts were backed by government funding.

"But why would the government bother", argues your companion. "Don't you remember those fluorescent bulbs. Not great, but there were efficient, weren't they?"

You agree, but point out their many weaknesses. They were bulky, early products produced a ghoulish green blue light that put many customers off for good, and they flickered – possibly causing migraines. What's more, they were incompatible with dimmer switches.

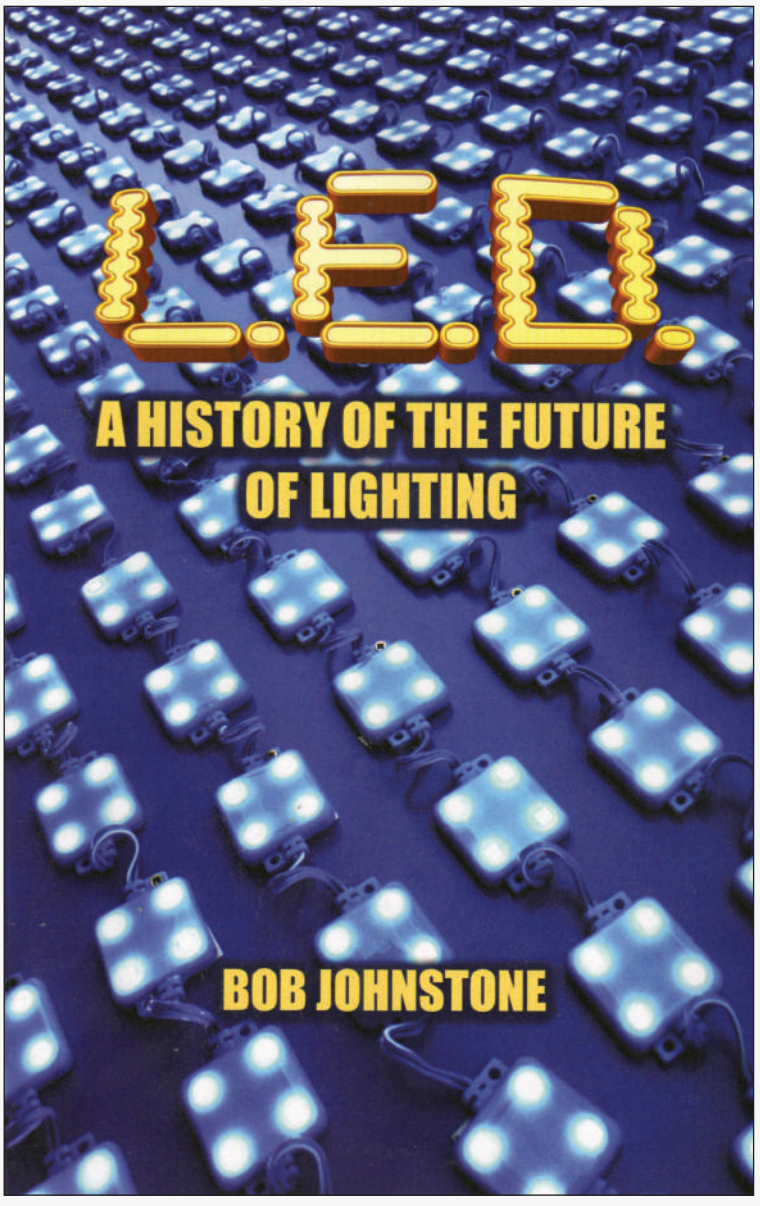
Johnstone points out that to prevent poor products from thwarting sales of LEDs, and to accelerate the development of this technology, the US government launched a competition known as the L-prize. To net $10 million and the kudos that went with it, the winner had to produce a bulb that combined many of the appealing attributes of the 60 W incandescent, such as its particular colour, with drawing less than 10 W and lasting for 25,000 hours – about 15 years – rather than 1,000.

You go on to explain that Philips won the competition, before going on to launch the bulb. At $50 a pop it wasn't going to appeal to the masses, but through refinements and competition, prices have tumbled. You say that last time you looked, a four pack of Philips 60 W-equivalent LEDs from Home Depot would set you back less than $10.

And it's not just in homes where LEDs are making a difference. Recounting one of the stories in Johnstone's book, you mention the success of LEDs in streetlights. In particular, you recall the statistic of 96,000 lights being tested over five years, with no failures whatsoever.

"Wow, that's impressive," says your companion. "But with such long lifetimes, is anybody making any money?"

That's a perceptive, painful question. You have to admit that it's a bit of a blood bath right now – it's even got its own name, illumigeddon. What's not helped is



L.E.D. A History of the Future of Lighting is written by Bob Johnstone and published in May 2017 by the CreateSpace Independent Publishing Platform.

a glut of LEDs made for backlighting TVs, tablets and laptops, leading to more chips for sale for lighting.

As you dwell on this, you're asked: "Is that light up there powered by an LED?"

It is, you reply, as you gaze at what is beyond doubt a rather fine fixture. It enthuses you, and you explain that sales of LEDs used in lighting fixtures offers longer term growth and better margins. Before you continue, a fine plate of hors d'oeuvres appears in front of you.

The bright cherry tomatoes, out-of-season, remind you of another application of the LED described by Johnstone: agricultural lighting. Not only is the lighting more efficient, saving money, but the colour can be tuned to be as effective as possible, allowing a lengthening of the growing season.

"I can see that getting the lighting just right is good for plants, but you can't beat sunshine for making you feel good, can you?"

You nod in approval, impressed by such awareness of the impact of light. You mention that earlier this year Lufthansa had fitted tuneable LED lighting in its latest Airbus 380 super-jumbo to give the right light at the right time. That's warm light for relaxation, and cooler light for passengers to work.

Tailored lighting can also help children to learn better, you add, according to a study recounted in Johnstone's book. When Philips installed a dynamic lighting system in schools that had four settings – using differences in intensity and colour to either invigorate students, help them to focus, or aid relaxation – the results were very impressive. Reading speed increased by one-third, and hyperactive behaviour declined by more than 75 percent.

You point out that encouraging results have also come from trials in care homes. But this field is still in its infancy, with much more work needed before any claims of the health benefits of LEDs can be justified. However, you point out that whatever the outcome, it is fun to be able to control the colour of the lights in your home.

"Yes, I can see that. And I'm just about to buy a rundown apartment that will need gutting. Maybe now is the time for me to embark on installing an LED lit home."

At this point you are tempted to encourage them, arguing that it is definitely the way forward. But then you remember the epilogue in the book, a cautionary tale of Johnstone paying for an installation of LED lighting during the refurbishment of his loft apartment. While the final results were a success, the installation was a nightmare. The architect didn't trust the lighting designer, the electrician was not proficient with the technology, and attempts to prevent the budget from getting out of hand by securing cheaper products led to delays and compromise. A new electrician had to be appointed to complete the job.

While they thank you for your honest advice, you get a tap on your shoulder. You turn to see that it's the host of the party that wants your attention.

"I've got someone I want you to meet. They've been telling me that they've been stock-pilling incandescent bulbs, because all the alternatives are no good. I'm sure you convinced me to get that LED bulb in the hall. Can you talk to them?"

Off you go to shake their hand and put them straight, armed with a few more anecdotes from Johnstone's book.

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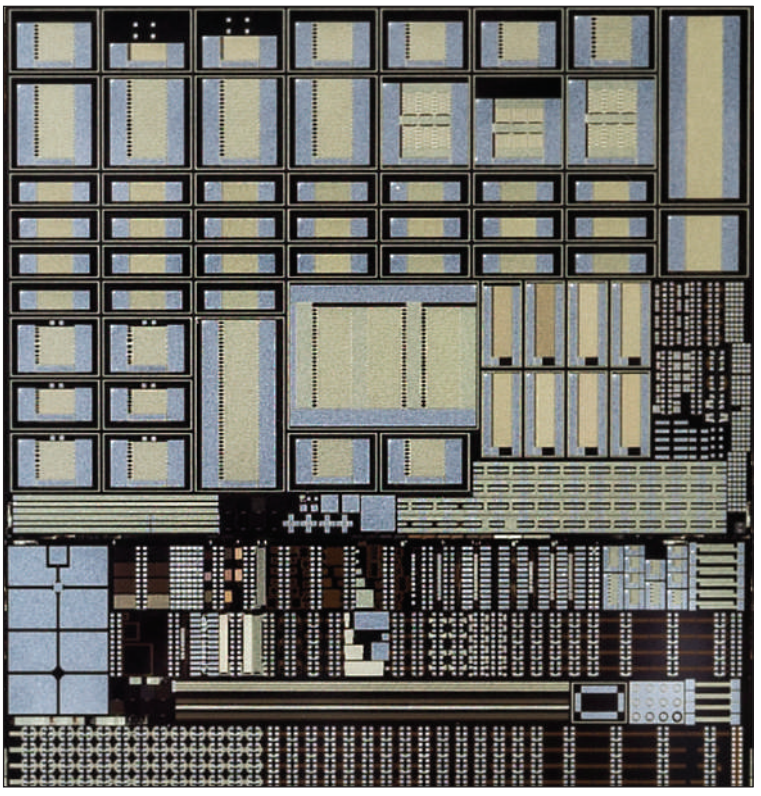
Creating and strengthening links between chipmakers and network builders

The monolithic integration of GaN

Combining trench isolation with silicon-on-insulator technology enables monolithic integration of fully isolated power devices

BY KAREN GEENS, MARLEEN VAN HOVE AND STEFAAN DECOUTERE FROM IMEC



GaN is destined to revolutionise the power semiconductor industry. It is tipped to displace the traditional silicon-based power chip, thanks to its higher breakdown strength, faster switching speed, higher thermal conductivity and lower on-resistance.

Development of this technology began with lower-voltage DC-DC converters and high-voltage (600 V) power-switching applications. Due to this, first-generation GaN-based power devices are going to play a key role in power conversion within battery chargers, smartphones, computers, servers, the automotive industry, lighting systems and photovoltaics.

GaN power devices are not grown on native substrates, which are pricey and limited in availability. Instead, various alternatives are employed, with sapphire, SiC and silicon the most popular. The latter's appeal is its cost, allied to the opportunity to use larger wafer diameters – 200 mm or more – and run the material through standard semiconductor processing lines.

Today, most GaN power systems are formed from multiple chips. GaN-based components – or devices, such as HEMTs – are assembled as discrete components, before they are united on a printed circuit board.

The downsides of this approach are that it is complex and expensive. A better option is to monolithically integrate GaN power devices on a single chip, because this yields a lower-cost, simpler system. What's more, monolithic integration promises better control of parasitic capacitances and inductances, and a superior power conversion efficiency.

A typical example of a convertor topology that would benefit from monolithic integration is a half bridge – it is one of the most common switch circuit topologies used in power electronics today. A half bridge consists of a low-side switch (with the source at a low potential), and a high-side switch (with the source at a high potential). The pair of switches are connected in an electrical circuit and turned on and off in a complementary fashion during operation. So the switches have to be biased differently, which requires isolating high-side and low-side devices.

Realising this is far from easy with GaN-on-silicon. If lateral isolation is adopted, different components must be separated by an isolation implant or mesa etching; and if vertical isolation is pursued, partially

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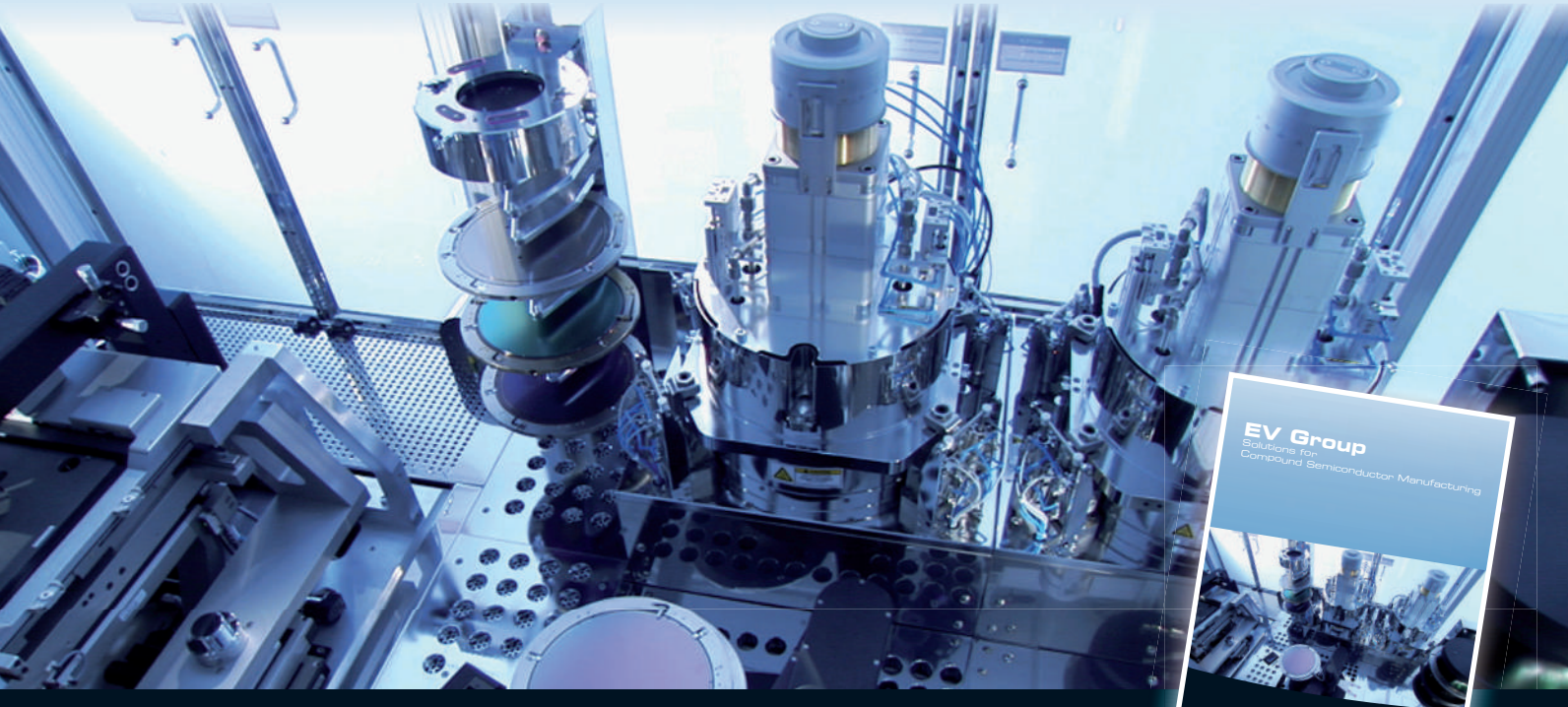

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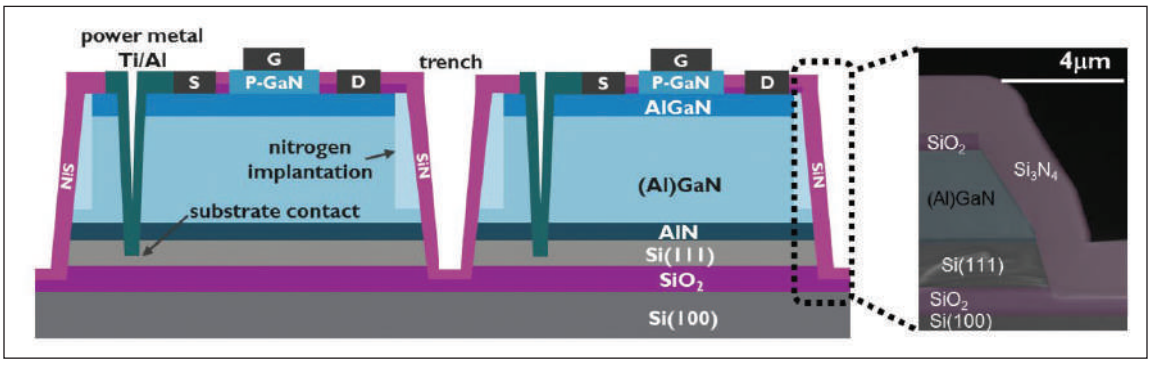

Figure 1. The architecture of imec's E-mode *p*-GaN HEMT.

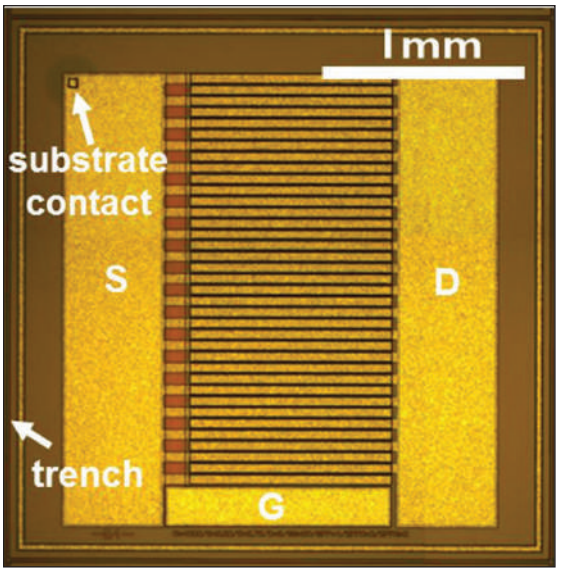

Figure 2. Top view of an imec device. A box-like isolation structure is created around each HEMT.

realisation is possible with a high-resistive buffer. Note that with the latter topology, devices still share a common conductive silicon substrate, which can only be referenced to a single potential at a time.

An SOI solution

At imec of Leuven, Belgium, we are breaking new ground by isolating devices through growth on silicon-on-insulator (SOI) wafers, followed by trench isolation. SOI wafers contain a layer of SiO_2, sandwiched between two layers of silicon. This composite, designed to improve insulating characteristics, is used in the silicon industry to try and improve performance at the nanoscale.

That's not the only use of SOI, however – many teams, including our own, are investigating its potential as a foundation for improving the crystal quality of GaN. It is not trivial to switch from silicon to SOI for GaN growth, however: there are more layer parameters to tune, such as the thickness of the silicon (111) layer and the compliant SiO_2 layer; and dedicated strain engineering is required to control stress during epitaxy.

By turning to SOI, we can isolate devices by trench etching through GaN and silicon and into the SiO_2 buried layer. Ultimately, that has enabled us to demonstrate the monolithic integration capabilities of GaN-on-SOI technology, such as its use in half-bridge circuits. To form this circuit, we use enhancement-mode (E-mode) *p*-GaN HEMTs: they have a *p*-type gate and operate in normally off mode. That method of operation is preferred to normally on for power efficiency and fail safety.

Fabrication of our monolithic, GaN-based circuits begins with MOCVD of a GaN epi-stack on a 200 mm SOI wafer – a structure with a layer of silicon (111), on top of SiO_2 and silicon (100). Epitaxial growth adds an AlN nucleation layer, followed by an (Al)GaN buffer

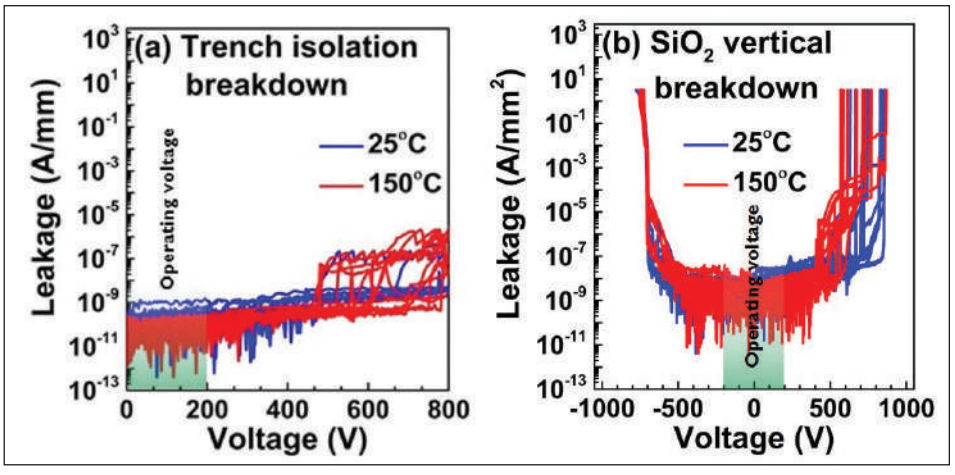

Figure 3. (a) Horizontal breakdown of the trench isolation and (b) vertical breakdown of the SiO_2 buried layer on the 200 mm GaN-on-SOI at 25°C and 150°C.

imec's work on power GaN

imec's research on GaN-on-SOI is part of its Industrial Affiliation Program on GaN power devices. Within this program, imec aims to take today's GaN-on-silicon technology to a higher level of maturity and reliability, and explore new concepts for next-generation GaN technology.

Research at imec is also carried out within the framework of the European ECSEL PowerBase project. PowerBase aims to develop next-generation energy-saving chips based on materials such as GaN. Co-ordinated by Infineon, 39 project partners are preparing these semiconductors for mass industrial use in smartphones, laptops, servers and many other applications. Within this project, imec is looking beyond traditional substrate technologies for GaN-based devices, and exploring novel isolation technologies. PowerBase receives funding from the Electronic Component Systems for European Leadership Joint Undertaking, under grant agreement 662133.

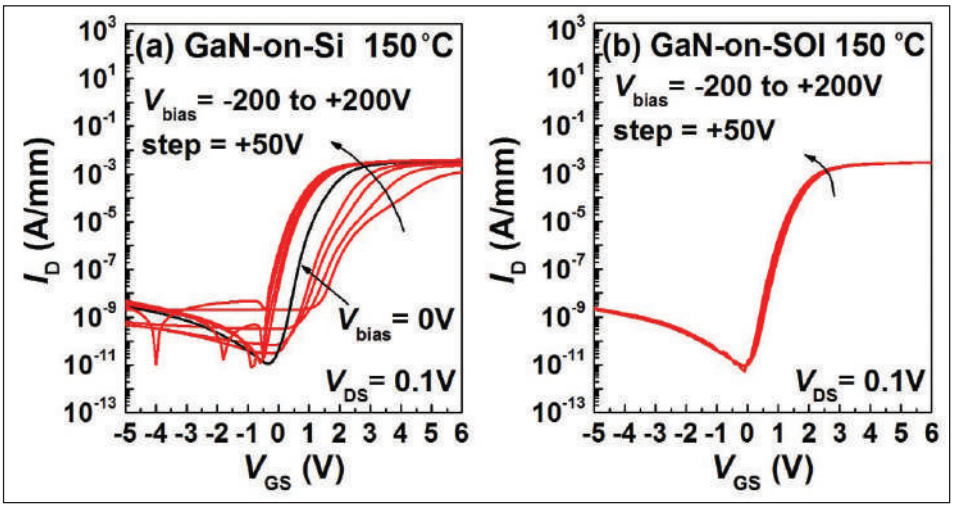

Figure 4. Transfer characteristics of a HEMT at 150°C (a) with a common silicon substrate biased from -200 V to 200 V (GaN-on-silicon) and (b) while simultaneously biasing the neighbouring silicon (111) HEMT layer at different voltages (GaN-on-SOI).

layer, a GaN channel layer, an AlGaN barrier layer and a magnesium-doped *p*-GaN layer.

To control the stress built up in the wafer during growth, we undertake delicate strain engineering. This enables production of a GaN-on-SOI wafers with a controlled warpage and good mechanical strength. E-mode *p*-GaN HEMTs are formed, using a TiN/*p*-GaN stack for the gate.

Horizontal and vertical isolation of the HEMTs is realised with a combination of nitrogen implantation isolation and etching of a trench through to the SiO_2 buried layer. A box-like isolation structure results, with HEMTs surrounded on all sides by an insulating dielectric (see Figures 1 and 2).

Our *p*-type GaN HEMTs have been fully qualified for 200 V switching applications. Both the horizontal breakdown voltage of the trench isolation, and the vertical breakdown of the SiO_2 buried layer, are typically as high as 500 V at 150°C (see Figure 3).

Benefits of device isolation are highlighted by the transfer characteristics of our GaN-on-SOI HEMT (see Figure 4). With this foundation, transfer characteristics undergo very little change when the substrate of the neighbouring device is biased between -200 V and 200 V. In stark contrast, when this occurs on a silicon substrate, transfer characteristics shift, highlighting performance degradation in these devices.

Our results reveal, for the first time, that the combination of GaN-on-SOI and trench isolation is a promising approach to monolithically integrate GaN power systems on the same wafer. Our next steps will be to study the thermal performance of GaN-on-SOI, and to optimise the composition of the SOI substrate and the GaN epitaxial stack. In addition, we will move to higher levels of monolithic integration, and increase the operating voltage to 650 V.

Further reading

Xiangdong Li *et al*. IEEE Electron Dev. Lett. **38** 918 (2017)
https://www.imec-int.com/en/200mm-GaN-on-Si-technology
https://www.imec-int.com/en/articles/imec-s-200mm-gan-on-si-e-mode-power-devices-withstand-heavy-ion-and-neutron-irradiation
http://magazine.imec.be/data/74/reader/reader.html?t=1493275079050#!preferred/1/package/74/pub/80/page/4
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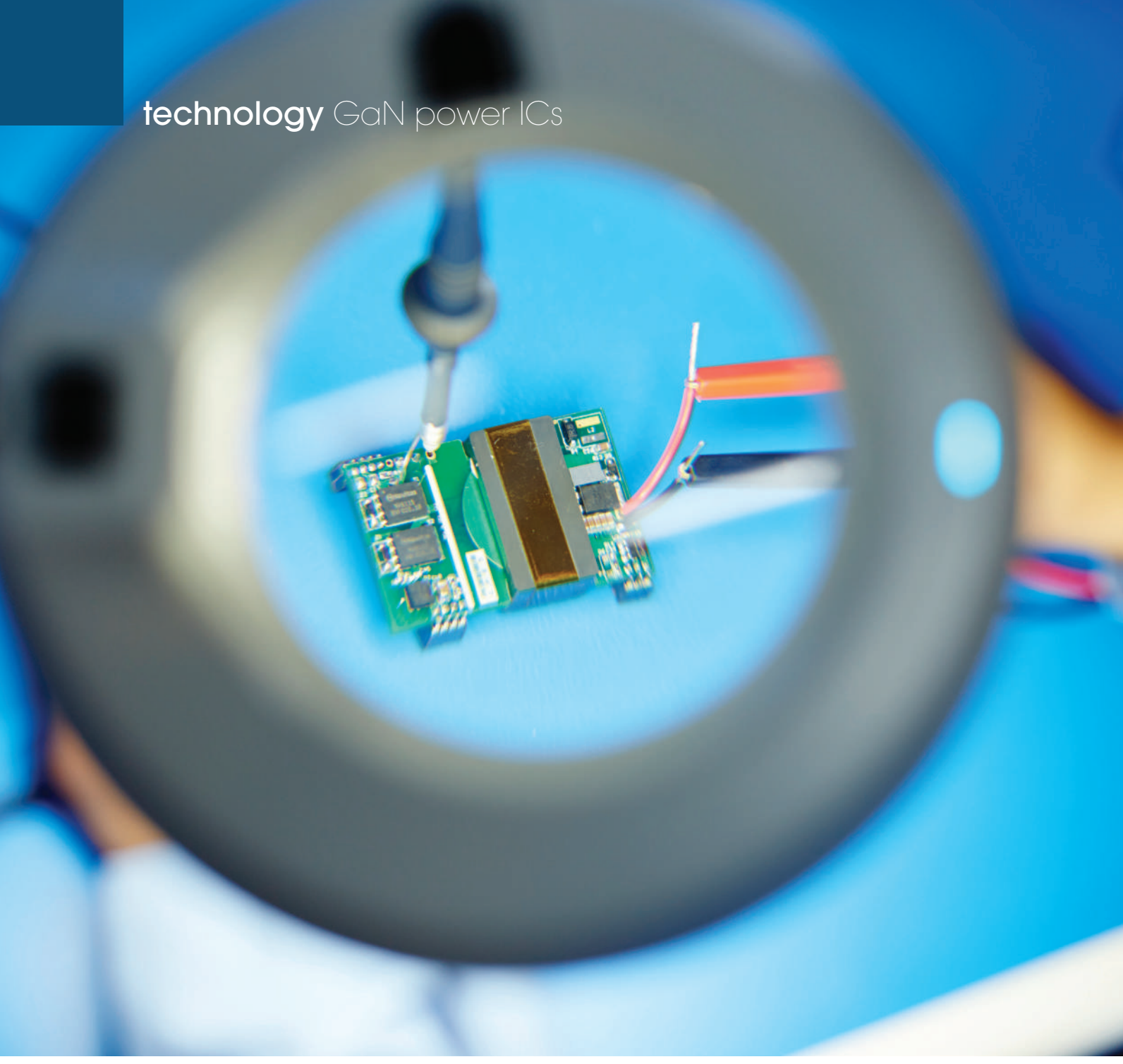
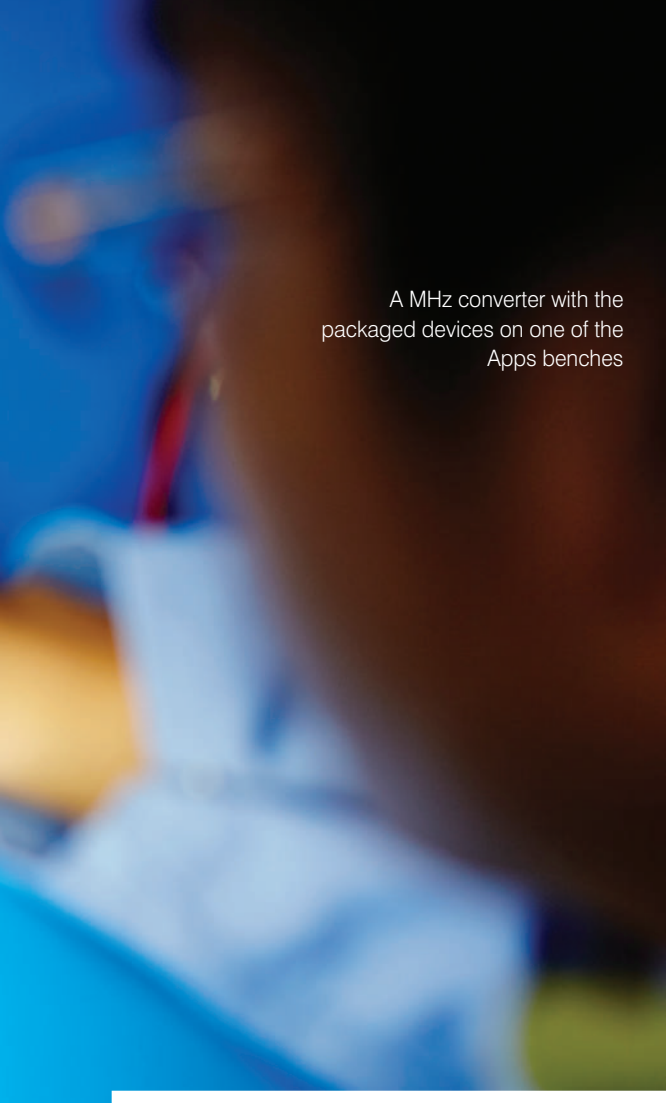


Power electronics:

Easing the use of GaN

Simplifying a designer's life with a process design kit for GaN-based integrated circuits

BY NICK FICHTENBAUM FROM NAVITAS SEMICONDUCTOR



A MHz converter with the packaged devices on one of the Apps benches

Not that long ago, designers of power systems had no choice over the material in their components: it had to be silicon. Recently, however, they have had their interest piqued by the promising properties of GaN. The appeal is that discrete FETs, in either the form of cascoded depletion-mode (D-mode) devices or enhancement-mode (E-mode) variants, have the potential to deliver a superior performance at the individual component-level.

Unfortunately, theory is not borne out in practice. The 'real world' has various system challenges, including vulnerable gate drive, level-shifting, parasitic impedances and complexity. All increase cost and risk, while reducing switching speeds and impairing power density benefits.

Due to these issues, designers that are under-pressure – and that is the norm – tend to desert the new-fangled wide band-gap devices and retreat to their comfort zone: silicon FETs, serving in low-frequency circuits. However, that doesn't have to be the case. Thanks to efforts by our team at Navitas Semiconductors of El Segundo, CA, power designers can enjoy the benefits of GaN by turning to the industry's first GaN power IC Process Design Kit (PDK). It allows monolithic integration of GaN IC circuits with GaN FETs.

Different architectures

Lying at the heart of every GaN FET is a two-dimensional electron gas, formed at the GaN-AlGaN interface (see Figure 1). This gas creates a very high mobility in the channel and drain drift region, leading to a far lower resistance than that for devices made from silicon or SiC.

Devices made from GaN can withstand high electric fields. This allows depletion regions to be very short or narrow, and devices to operate at high carrier densities while being packed very densely.

For the GaN FET with a lateral architecture, devices with a rating of 650 V can typically handle more than 800 V. In this FET, the drain drift region is 10-20 μm thick, so the field strength is around 40-80 V/μm. This is well above the theoretical limit of silicon that is about 20 V/μm, but still well short of the bandgap limit for GaN, which is about 300 V/μm. So there is substantial room for improvement for the lateral GaN FET.

Better results may be possible with vertical GaN FETs. In terms of development, they lag their lateral cousins, being held back by the need for epilayer growth on bulk GaN substrates. This foundation is very expensive, and predominantly limited to diameters of 3-inch or less.

Additional challenges facing vertical GaN are: the need to win share from the more established SiC FET market; and that the lateral E-mode (normally off) GaN device can now be produced on 150 mm production-quality GaN-on-silicon wafers using existing foundry processes. The latter breakthrough opens the door to manufacture of high-volume, cost-effective switches and power ICs.

Production of FETs that are E-mode, rather than D-mode, is a big deal. Development of these transistors began with D-mode, with devices kept in an off-state through pairing with a silicon FET in 'cascode' configuration. That's not a good solution – it increases packaging inductance and cost.

Early E-mode FETs addressed this issue, but they had vulnerable gates and a very low threshold voltage. Due to this, they were susceptible to noise and voltage spikes that stemmed from the surrounding switched-mode converter circuit. The upshot was that E-mode devices required complex, expensive control and gate drive circuits. That solution held back the high-frequency performance of the GaN switch to the point

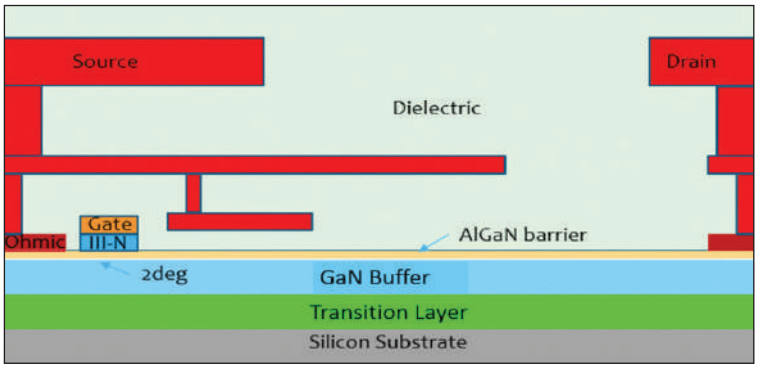


Figure 1. Lateral GaN-on-silicon devices feature a two-dimensional gas that enables high channel mobility and a low resistance.

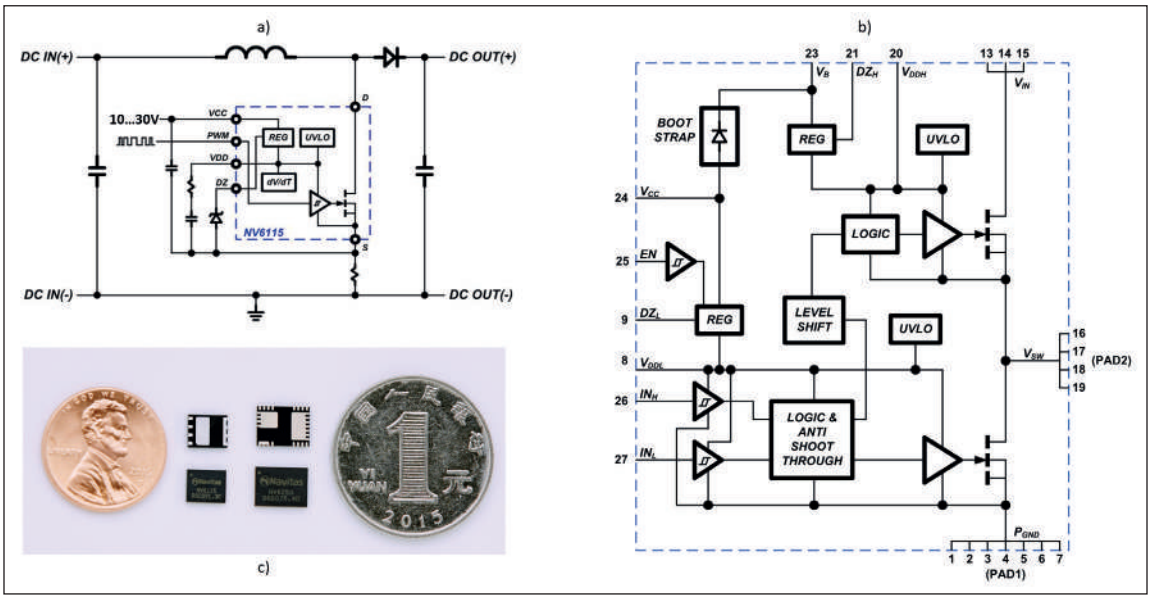


Figure 2. The AllGaN is the industry's first GaN Power IC process design kit, according to its developer, Navitas. It can be used to form (a) single and (b) half-bridge circuits, and (c) packaged devices.

where there is minimal, if any, advantage over silicon. With a small edge at best, market adoption is limited.

We overcome these issues and unlock the potential of the GaN FET via the integration of lateral device structures. Power designers that adopt our AllGaN, which is the industry's first GaN power IC Process Design Kit (PDK), benefit from monolithically-integrated 650 V GaN FETs with GaN IC circuits, including those with drive and logic functions.

The proprietary AllGaN PDK is remarkable, given its restricted device-level tool-set, which includes the absence of *p*-channel devices and diodes. For this monolithic integration technology, which is impossible to realise using vertical GaN, D-mode GaN and SiC technologies, we have 30 patents that are granted or are pending. They are covering the device, packaging and application/system innovations.

The 'ideal switch'?

We know that we need to convince frustrated, skeptical power designers of the capability of our technology. How are we able to remove risks, complexity and speed limits, so that we can give these engineers performance and confidence, and ultimately enable them to deliver the next-generation of power converters? Well, the answer is to revisit the concept of the 'ideal switch', and see how well our GaN power ICs perform. Here they deliver a high-performance, easy-to-use, rugged, digital-in, power-out building block.

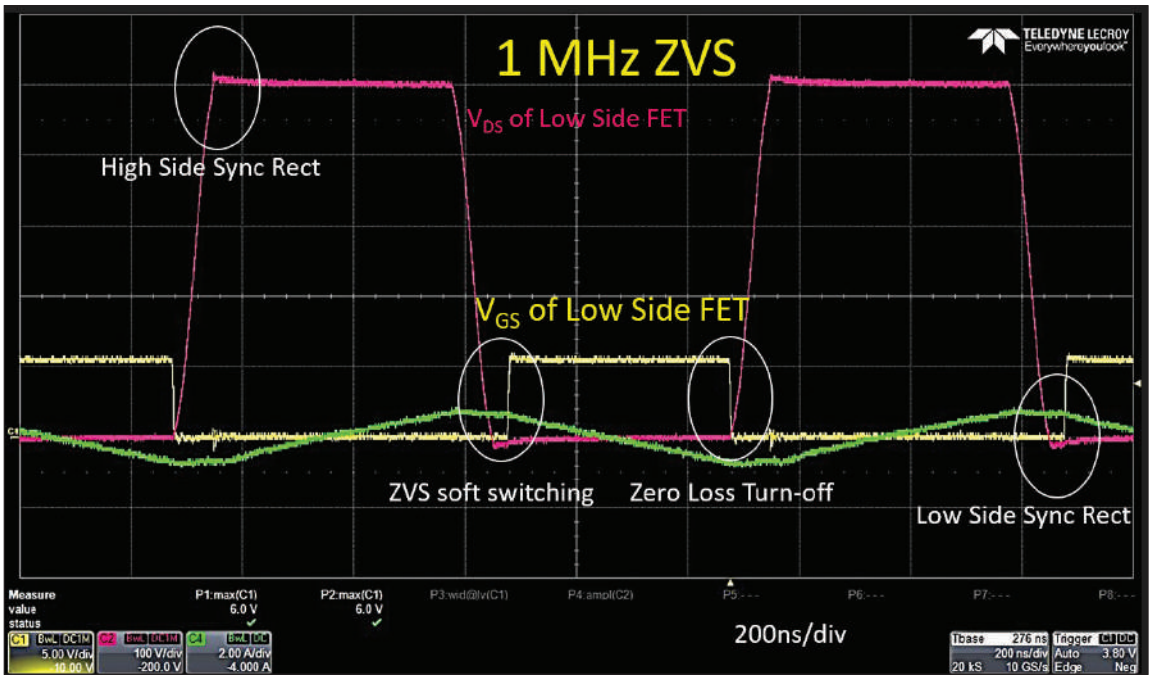
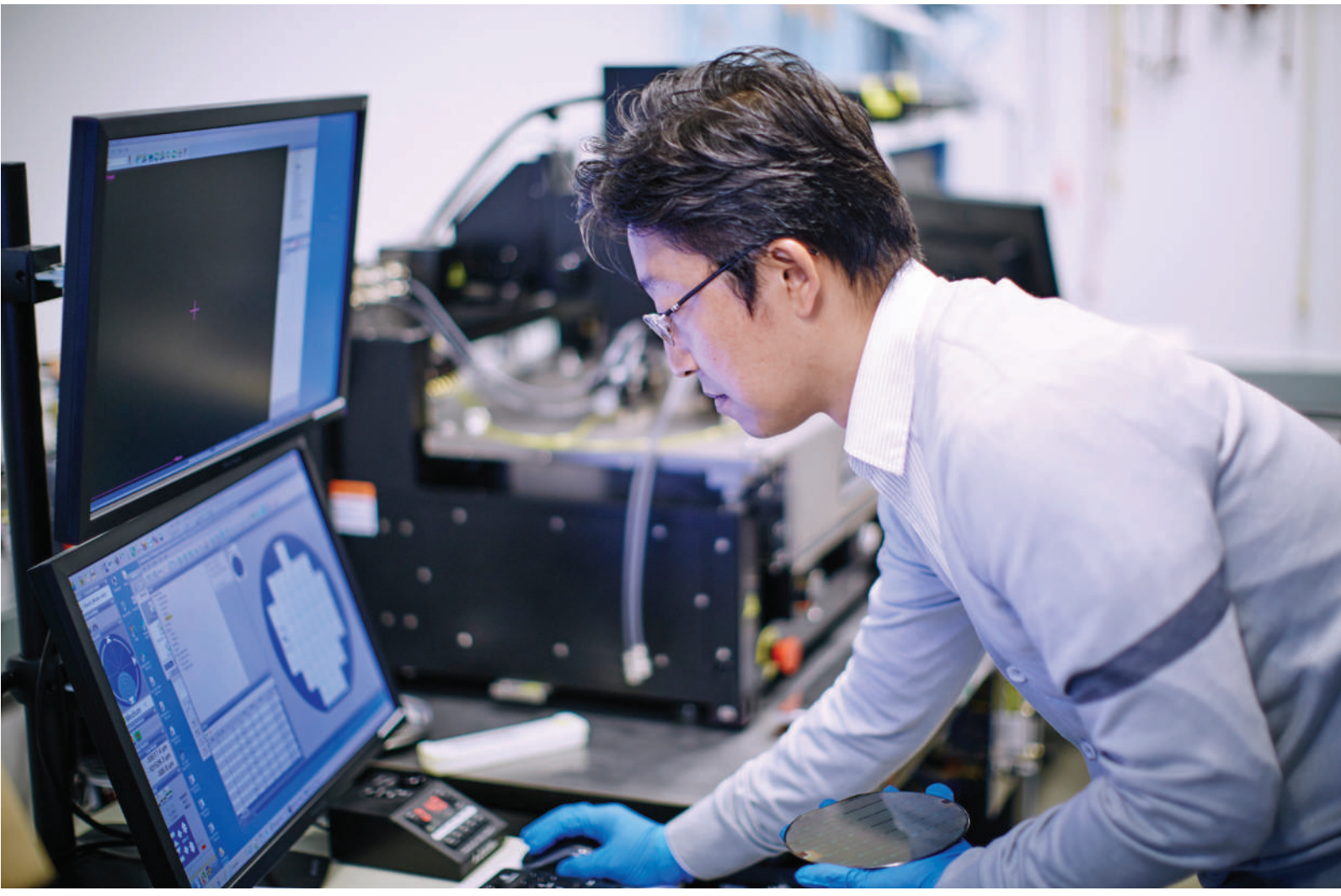


Figure 3. A 1 MHz half-bridge topology using Navitas GaN Power ICs.



A multi-project wafer (MPW) or 'pizza-mask' at probe test

It is clear that the days are numbered for the normally-on, D-mode GaN FET. It is compromised by its multiple die and highly-inductive, costly packaging.

E-mode parts operating from 80 V to 650 V have now been qualified to JEDEC standards, allowing these lower cost, higher-speed devices to open new circuit possibilities. But there is one major caveat: exposed GaN gates are vulnerable, so designers must carefully control voltages and system noise, while using dedicated discrete or co-packed drivers, voltage regulators and level-shifters. This adds to component count, size, cost and complexity.

Problems associated with the vulnerable gate of discrete GaN are avoided with our GaN power ICs. The combination of monolithic on-board voltage regulators and high-speed drivers directly and carefully feed the GaN gate with no parasitic impedance, no voltage spikes, no false turn-on and no external exposure.

With AllGaN technology, we exploit the fundamental lateral capability of E-mode GaN, to integrate multiple device structures on a single, monolithic die. This enables a GaN Power IC to be created with a high supply voltage of 30 V, and simple, logic input.

The capability of monolithically-integrated circuits is clear in the waveforms they produce. They have a true 'text book' feeling with very clean rising and falling edges, no ringing, and extremely fast turn-on and turn-off propagation delays (see Figure 3). Integration eliminates gate overshoot and undershoot, while zero inductance on-chip ensures no turn-off loss.

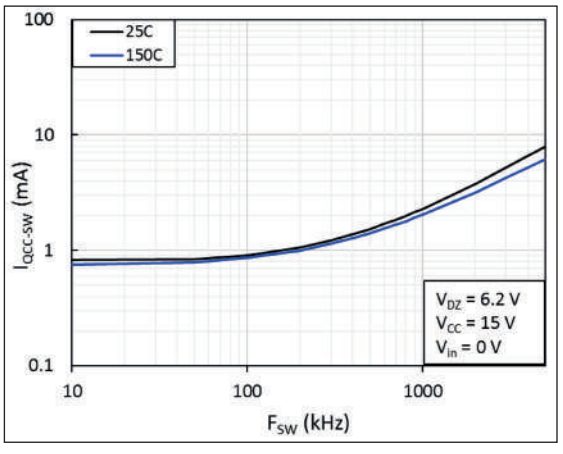


Figure 4. V_{CC} operating current (I_{QCC-SW}), as a function of operating frequency (F_{SW}), for a Navitas 160 mΩ GaN Power IC.

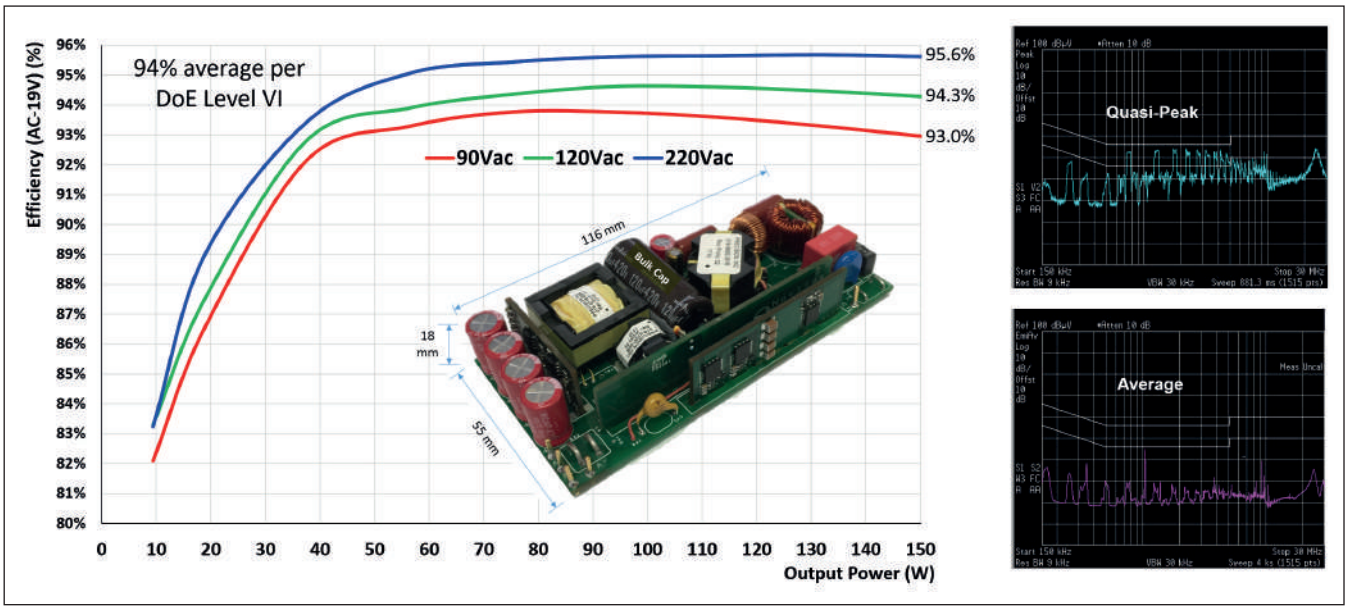


Figure 5. A Navitas 150 W AC-12 V_{DC} reference design at 21 W/inch^3 (uncased). This features CrCM PFC and LLC topology.

This lack of ringing/overshoot simplifies tight control of deadtime in half-bridge circuits. This very fast, incredibly quiet switching performance, combined with an integrated gate drive and simple PWM input, enables the design of a variety of different high-frequency power converters, raising practical speeds more than ten-fold. No more are they limited to 65 kHz, or 100 kHz – now more than 1 MHz is possible.

Housed in industry-standard, low inductance, surface-mount QFN packaging, our GaN Power ICs provide high-performance, low-cost circuits with the highest power density. A digital input offers flexibility in design. The GaN devices can be placed on the main board, or positioned on the daughtercard, close to or far from the control IC.

One key concern for the circuit designer is the area of the printed circuit board. Our GaN half-bridge power IC – incorporating all functions, including powertrain – excels in this regard, delivering a 20-fold reduction in area compared to silicon-based alternatives.

Another strength of our approach is its ability to handle fast-moving voltage waveforms. This is getting more important as system switching frequencies increase to take advantage of GaN and slew-rates rise correspondingly. With our AllGaN technology, changes as fast as 200 V/ns are possible.

There are additional safety features associated with lateral integration, which are not possible for discrete devices. If FETs are discrete, they are not rated for electrostatic damage (ESD), as they don't have any ESD structures. In contrast, our GaN power ICs technology can create ESD diode structures that are capable of withstanding 1 kV. We can also incorporate topology-related protections, such as undervoltage-lockout and shoot-through protection, to ensure robust circuit performance.

One of the merits of integration is a greatly-reduced component count. Simplified designs have fewer interconnects and thus increased reliability. By constructing circuits on a single, heterogeneous AllGaN platform, variation in system parameters is small. This reduces the chance of disparate component/technology interactions or wide, worst-case application parameter distributions.

Digital in, power out

As already stated, our GaN power ICs have simple logic PWM inputs – either 3.3 V, 5 V or 12 V signals – that are produced by industry-standard, low-cost, low voltage 'no driver' control ICs, such as ASICS or DSPs. Due to the natural low-charge structure of GaN, combined with careful driver design, the input current consumption is small, rising only slightly with frequency. For example, at 15 V, the quiescent operating current for a 160 mΩ single GaN power IC increases from a mere 0.9 mA at 10 kHz to only 1.1 mA at 1 MHz. That's a rise of only 20 percent for an increase in switching frequency of two orders of magnitude.

Designers that select our half-bridge GaN Power ICs also benefit from the elimination of external analog elements, like the bootstrap charging diode and expensive level-shifter/drivers. All they need to do is simply drive the two, low-side referenced PWM inputs directly from the controller.

The effectiveness of the powertrain is governed by the performance of the overall system. To fulfil the Department of Energy's Level VI requirements, benchmarks must be met for average efficiency and standby-power, plus statutory requirements for the likes of EMI, PFC and safety compliance. Note that the benefits of higher efficiency include the use of low case temperatures, while the low standby-power requirements can be met by enabling / disabling the

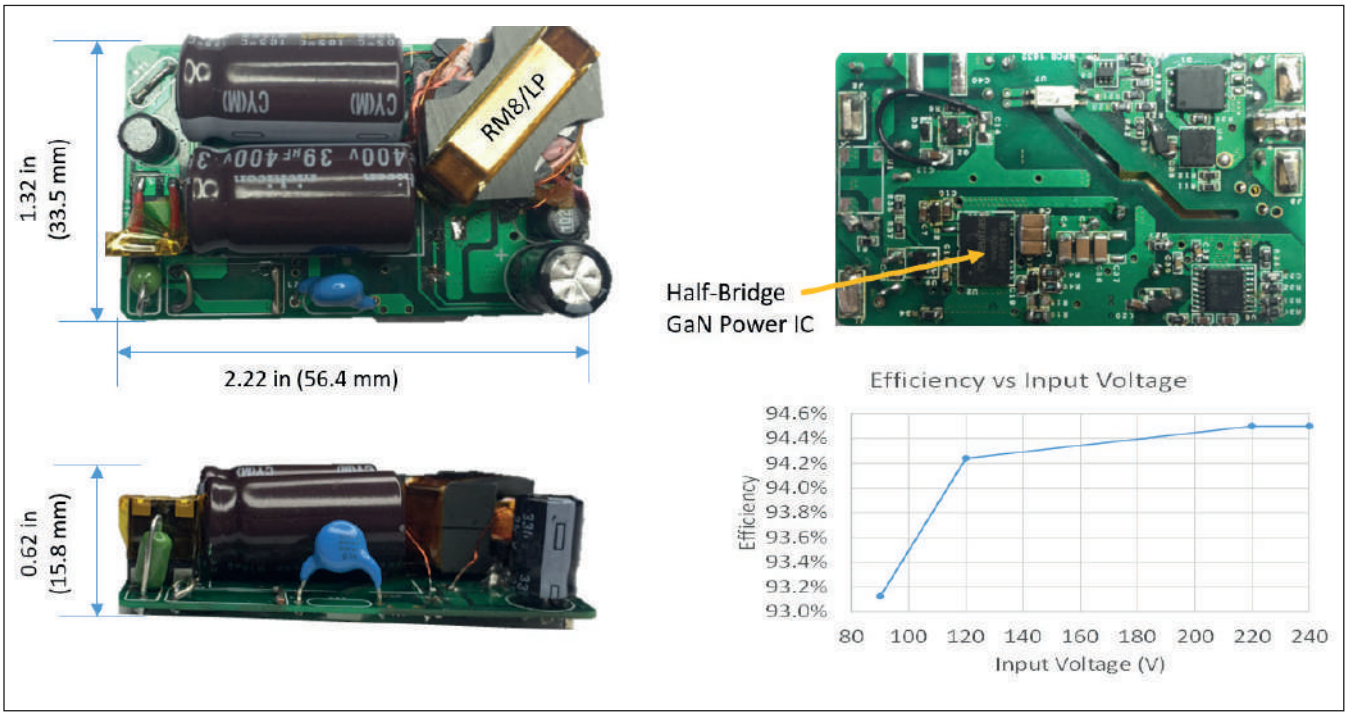


Figure 6. A Navitas 45 W ACF at 25 W/inch^3 (uncased).

GaN power ICs in burst-modes. Once efficiency and standby-power are addressed, circuits can operate at higher frequencies, allowing the use of new high-frequency magnetic materials for higher power density.

AllGaN's technological capability is demonstrated by measurements on AC-DC power converters. These results don't tell the whole story, however, because GaN Power ICs are rated at 2 MHz or more, while commercially available control ICs are currently limited to typically 300-400 kHz. This situation is set to change, with high-frequency controllers in development that will exploit GaN's fundamental high-frequency capability.

The first of our two examples involves the use of single GaN Power ICs in a 150 W, AC to 12 V DC converter (see Figure 5). It delivers a power density of 21 W/inch^3, and higher values should be possible following more optimisation by power designers. Efficiency reaches 95.6 percent, and there is a very controlled, quiet EMI spectrum, thanks to a soft-switching, no-overshoot topology.

Our other example involves the use of a half-bridge GaN Power IC in the soft-switching active clamp flyback topology of a 45 W, AC to 20 V DC adapter. Here, the active clamp flyback realises a power density of 25 W/inch^3 while delivering 93 percent efficiency at the critical 90 V_{AC} input point – this is where currents are highest, so thermal performance takes its biggest hit.

By introducing the AllGaN PDK and monolithically-integrated GaN power ICs, we have removed the barriers that have prevented power system designers from enjoying the theoretical performance of GaN. No longer are they having to work with discrete FETs, and suffer from issues such as poor-reliability, high-complexity, and high-cost restrictions.

Does that mean that the GaN power IC is now the ideal switch? Well, not quite, because there are still losses associated with Ohmic heating. However, that does not stop power system designers from revelling in the availability of a rugged, high-performance, digital-in, power out building block.

Further reading

GaN as a Displacement Technology for Silicon in Power Management", Lidow, EPC, IEEE ECCE 2011

Breaking Speed Limits with GaN Power ICs, Kinzer, Navitas, keynote, APEC 2016

Monolithic HV GaN Power ICs: Performance & Application, Kinzer & Oliver, Navitas, IEEE Electronics Magazine, Vol. 3, No. 3, September 2016

Step Up to Half-Bridge GaN Power ICs, Sharma *et al*. Navitas, Bodo's Power, March 2017

Efficiency standards for external power supplies, CUI Inc., Aug 2016

Active Clamp Flyback Using GaN Power IC for Power Adapter Applications, Xue & Zhang, Navitas, APEC 2017

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Refining the PIC: Achieving the Next Milestone in Performance

What are the leading approaches for integrating key building blocks at the chip-level and how can we bring together electronics and photonics more efficiently?

SPEAKERS

- **Michael Lebby: Lightwave Logic**
  Scalable PIC platforms: The impact of using polymer PICs for 100 and 400Gbps datacom applications
- **Wim Bogaerts: Ghent University/imec**
  Programmable photonic ICs: making optical devices more versatile
- **Luis Henrique Hecker de Carvalho: BrPhotonics**
  Converging photonics and microelectronics: applying advanced technologies to ramp up PIC performance
- **Tan Yong Tsong: Institute of Microelectronics**
  Coupling electronics and photonics – promising paths for device-makers to explore
- **Radha Nagarajan: Inphi**
  Highly integrated silicon photonics to push PICs to the next level
- **Sasan Fathpour: CREOL, The College of Optics & Photonics**
  Silicon photonics beyond silicon-on-insulator - emerging solutions for integrated photonics
- **Yvain Thonnart: CEA-Leti**
  Integrating photonic building blocks towards complete electro-optical computing
- **Shinji Matsuo: NTT Photonics**
  III-V membrane lasers on silicon for datacom and computercom applications

Moving the Data: PICs for Cloud Computing and Telecoms

Data centres and networks need smart solutions to manage the sharp growth in traffic. What can integrated photonics bring to the table and how can developers make sure their products appeal to key customers?

SPEAKERS

- **Katharine Schmidtke: Facebook**
  PIC opportunities for datacentres
- **Yuichi Nakamura: NEC Corporation**
  Big data analysis - a golden opportunity for silicon photonics
- **Martin Schell: Fraunhofer HHI**
  The Zettabyte is not enough: Volume handling for InP, silicon photonics, and hybrid photonic integration
- **Weiming Yao: JePPIX/PITC**
  III-V photonic integrated circuits for telecoms and beyond
- **Peter Winzer: Nokia Bell Labs**
  Massive array integration and the need for a holistic digital/analog optics/electronics co-design
- **Eric Mounier: Yole Développement**
  Data centre technology - the big PICture, opportunities for energy efficient photonics

PIC Design, Simulation and Packaging: A Blueprint for Future Success

How can we implement ideas faster and what needs to be considered to keep the final device cost on track?

SPEAKERS

- **Peter O'Brien: Tyndall National Institute**
  PIXAPP – Open Access Opportunities for Advanced PIC Packaging
- **Christopher Cone: Mentor Graphics**
  From schematic to layout – overcoming today's PIC design challenges
- **André Richter: VPIphotonics**
  Scalable design of integrated photonic and optoelectronic circuits

PIC Horizons: New and Emerging Applications for Integrated Photonics

How can developers capitalize on opportunities for optical platforms in growth areas such as medical diagnostics, industrial sensing and biological analysis?

SPEAKERS

- **Milan Mashanovitch: Freedom Photonics**
  Low size, weight and power (SWaP) instruments for sensing applications - cutting edge PICs
- **Sascha Geidel: Fraunhofer ENAS**
  Adding the 'tech' to biotech - opportunities for photonic integrated circuits
- **Andrew Sparks: Analog Devices**
  Putting liquid crystal waveguides in the fast lane automotive applications for PICs

Delivering the goods: Advances in PIC Manufacturing

What are the latest tools and techniques that can be deployed in the fab? And what are the options when it comes to evaluating the output?

SPEAKERS

- **Jessie Rosenberg: IBM**
  Inline wafer-scale photonic testing to boost PIC manufacturing efficiency
- **Jack Xu: Finisar**
  Meeting the challenge of producing PICs at high-volume
- **Arne Leinse: LioniX International**
  Silicon nitride based TriPleX PIC modules in a broad range of applications
- **Henk Bulthuis: Kaiam Corporation**
  Vertical integration: bringing key elements together to match PICs to the market

Panel: Has Silicon Photonics got the Required Scalability to Displace InP?
Silicon photonics has attracted the interest of many in large corporations, SMEs, and academics as a potential replacement to the incumbent PIC technology InP. Given these conditions, the question remains to ask if SiP can be truly scalable towards $1/Gbps at 400Gbps data rates and above (for any distance)?
Bert Jan Offrein – IBM
Robert Blum – Intel
Sean Anderson – Cisco
Di Liang - Hewlett Packard Enterprise

Panel: High Volume Transceiver Opportunities for PICs
Will transceivers ever achieve super high volumes to allow scalability in cost and performance, and if so, what would be the common large volume platforms, and more specifically, what would be the transceiver format/form factor?

Katharine Schmidtke – Facebook
Aref Chowdhury – Nokia

Additional panel speakers to be confirmed

Novel cooling aids high-power lasers

An efficient cooling architecture holds the key to trimming the size, weight and power of diode-pumped laser systems

BY JENNA CAMPBELL, PAUL LEISHER, MILAN MASHANOVITCH AND DANIEL RENNER FROM FREEDOM PHOTONICS AND TADEJ SEMENIC AND AVIJIT BHUNIA FROM TELEDYNE SCIENTIFIC COMPANY

A VARIETY of applications are served by high-power solid-state lasers, pumped by diode laser arrays. They include a wide range of commercial and military uses, from the welding and cutting of materials to the enabling of precise surgery.

As well as delivering a high output power, many applications require the laser systems to have a low size, weight, and power consumption (SWAP). To realize this, diodes have to operate efficiently, so they generate less waste heat; and it is helpful if they operate at elevated temperatures, because this eases cooling demands.

When diode lasers are cooled with a liquid coolant, the diode's operating temperature is directly proportional to both the coolant temperature and the heat generated during lasing. Operation at a high coolant temperature is advantageous from a thermal management perspective, but there is often a downside – an excessive diode temperature.

Addressing this weakness is our team from Freedom Photonics of Santa Barbara, CA, and Teledyne Scientific Company of Thousand Oaks, CA. Working together, we have developed a technology that involves a low-thermal-resistance cooler with industrial coolant, and high-performance laser diodes operating at a higher temperature. This combination slashes the SWAP.

To illustrate the advantage of high temperature diode operation, imagine the following scenario: a 50 percent efficient diode pumping a solid-state laser with 50 percent efficiency. For this system, wall-plug efficiency is 25 percent. So, if the system provides a 10 kW source and uses batteries and a closed-loop chiller, both the batteries and the chiller will be tremendously heavy.

Increasing the coolant temperature is a good solution. When it is higher, the chiller, which is very heavy and consumes a lot of energy, can be replaced with a lightweight heat exchanger and a fan. Further gains are possible with an increase in the efficiency of the diode laser, because this decreases the number of batteries required to power the laser and reduces waste heat, allowing the use of a smaller cooling system. Realizing these improvements in performance hinges on careful engineering of the laser chip and the thermal management system. Within the high power laser community, it is well known that the laser's heatsink is a significant barrier to power scaling in high-efficiency, broad-area semiconductor laser arrays. An ideal heatsink is one that delivers a minimum temperature rise between the coolant and the laser diode emitter at a given heat load.

For diode laser bar arrays, state-of-the-art technology is based on microchannel cooling. A liquid coolant flows along the underside of a thin metal layer in narrow fluidic channels formed between layers of copper or copper tungsten alloy sheets. The diode laser is soldered to the thin metal layer, and cooled during its operation. This approach, which allows for compact cooling and is scalable through stacking in two dimensions, produces a low thermal resistance – it can be below 0.2 K/W for a 1.0 cm wide bar with a 3.5 mm resonator length.

Unfortunately, there are several drawbacks associated with microchannel coolers: small channel dimensions place strict requirements on coolant filtration and the working fluid viscosity; delivery of an adequate coolant flow demands a large pressure drop, and therefore a high pumping power in scaled-up systems; and erosion of the cooler limits the lifetime of microchannel-cooled lasers to about 5000 hours.

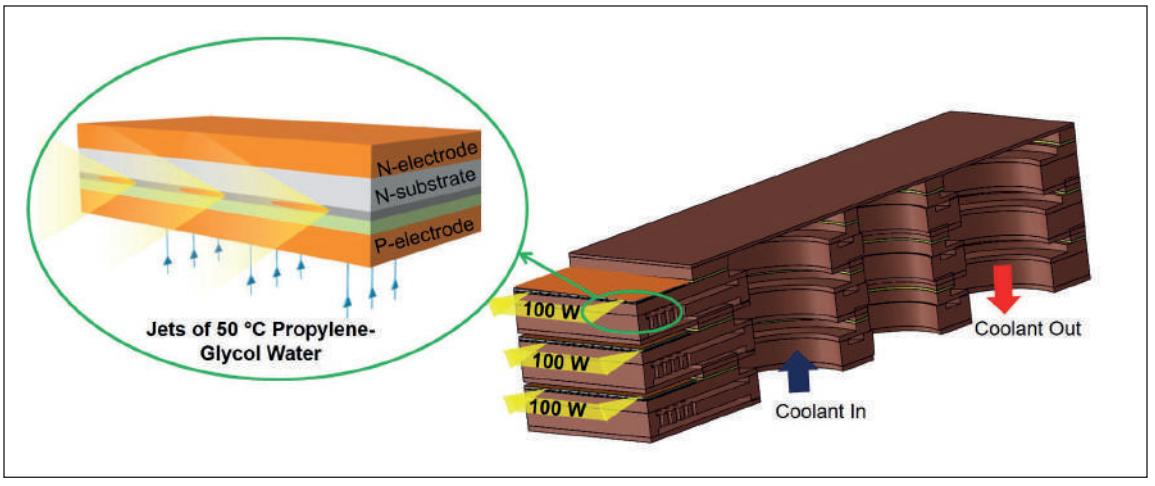

Figure 1. The conceptual design of the cooling system for diode laser arrays. On the left is a zoomed-in picture of an individual laser array, with cooling jets of propylene-glycol-water impinging on the *p*-side of the diodes. On the right is an illustration of a cooling manifold for a two-dimensional stack of laser bars. Each bar contributes 100 W of output power.

Due to all these issues, during the last decade there has been a drop in the number of diode laser vendors using this cooling technology. In its place are conductively cooled approaches, which have inferior thermal management and significant weight and size penalties.

Different fluids

With our novel semiconductor laser cooling approach we are able to deliver greatly improved performance while avoiding issues that plague conventional microchannel coolers. Out goes the deionised water coolant and in its place is an industrial fluid, such as a refrigerant or a corrosion-inhibiting glycol-water mixture. These alternatives are preferred to deionized water in many applications, because they operate over a wide temperature range and are less prone to corroding the cooling system. Due to the higher viscosity of glycol-water fluids than water, we replace the small micro-channels with macro-channels that have diameters of hundreds of microns. To aid cooling, these channels are brought very close to the emitters – they are separated by a gold-plated copper wall that is as thin as it possibly can be while maintaining structural stability.

Another innovation of ours is that instead of having the coolant flowing parallel to the laser array, we employ a jet impingement technology, with the coolant impinging perpendicularly. This approach has the edge over the conventional one, producing the highest possible heat transfer coefficient and ensuring the minimum temperature rise from the coolant to the laser emitters. Reducing the temperature rise, in conjunction with enabling chip operation at a high junction temperature, allows pump operation at high heatsink temperatures. Operated in this regime, the laser chip is cooled effectively by liquids at a relatively high temperature.

We have fabricated and verified our thermal management architecture with laser systems based on one-dimensional laser diode arrays. However, our approach is scalable, and could be used to cool a two-dimensional stack of high-power laser diode arrays, such as those used in a diode pump module (see Figure 1 for an outline of our cooling architecture with diode lasers, using high temperature propylene-glycol-water). Our team optimises the laser structure and the cooler using an opto-electro-thermal-fluid co-design approach. Applying an iterative sequence, we

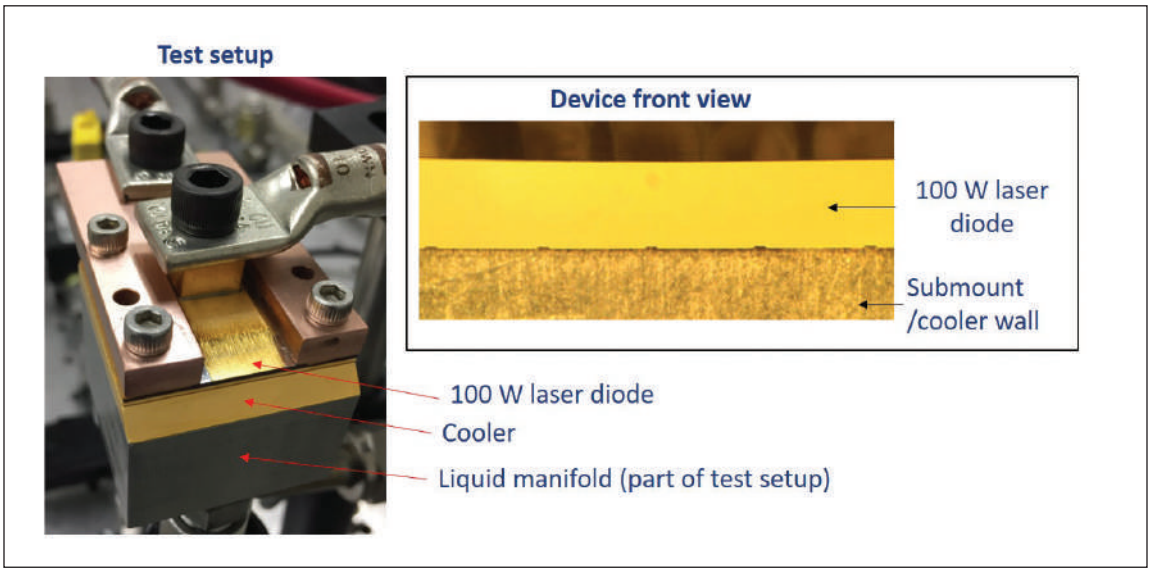

Figure 2. Images of laser devices. On the left is a photo of a laser bar on a sub-mount, attached to the liquid manifold, and installed in the thermal management test setup. On the right is a microscope image of a laser diode with multiple emitters.

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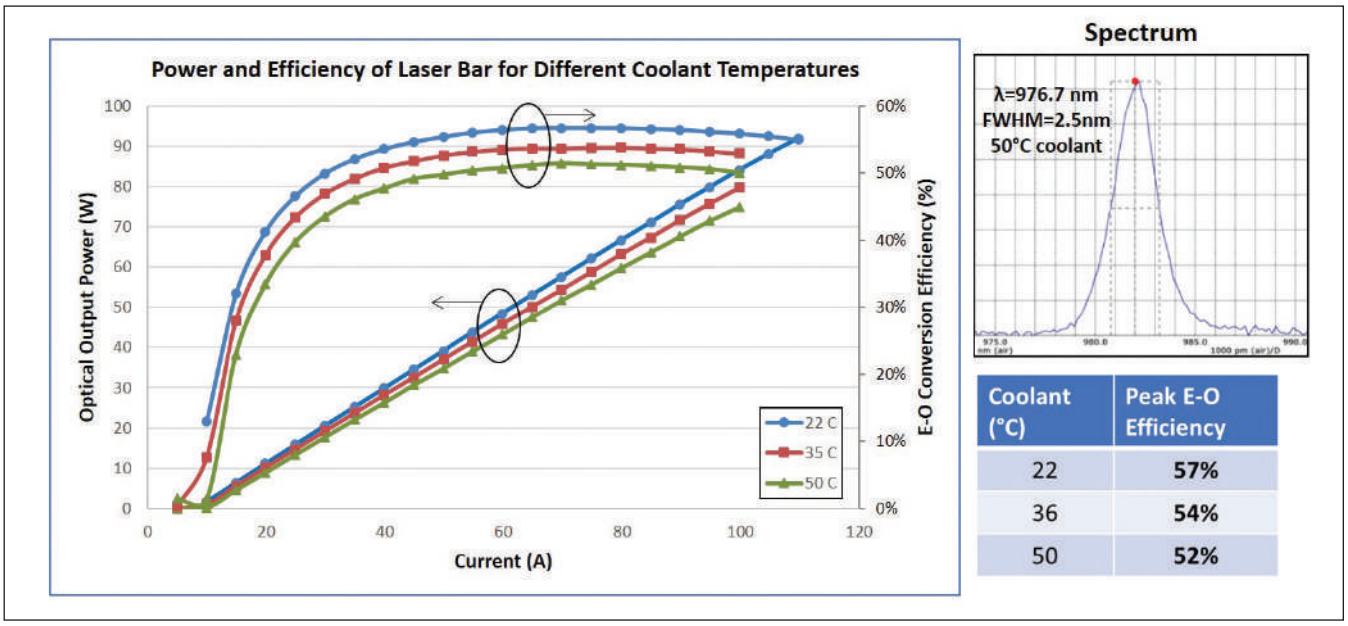


Coolant (°C)	Peak E-O Efficiency
22	57%
36	54%
50	52%

Figure 3. High-power laser test data. Left: Optical output power and electrical-to-optical (E-O) conversion efficiency as a function of drive current. The device under test shows more than 90 W of output power at 57 percent efficiency and a 22 °C coolant temperature. As the coolant temperature is increased to 35 °C and 50 °C, power and efficiency decrease. Top right: Example spectrum from a laser array. Light emission is at a peak wavelength of 976.7 nm, with a full-width-half-maximum (FWHM) of 2.5 nm. Bottom right: Table of peak E-O efficiency for different coolant temperatures. As the coolant temperature is increased from 22 °C to 50 °C, peak efficiency decreases from 57 percent to 52 percent.

feed results from semiconductor laser simulations into thermal and fluid simulations, and vice versa.

This allows us to fully customize each component for a specific application. When designing the cooler geometry, we explore different jet impingement patterns and channel sizes via extensive thermal modelling simulations. These impingement patterns and channel sizes are modified, depending on the laser array geometry.

We have focused our efforts on the development of improved 976 nm laser chip architectures that combine a high junction temperature with high efficiency. Benchmarking these chips is relatively straightforward, because semiconductor laser pumps for solid-state systems have been studied for several years. The pumps span 800 nm to 2100 nm in wavelength, and can achieve electrical-to-optical efficiencies in excess of 70 percent. However, these record-breaking efficiencies have been realized with a deionised water coolant at a temperature of less than 6 °C, and such a low operating temperature is impractical for many laser system applications, because it requires large chillers.

To optimise our epitaxial structures and laser designs for high-efficiency performance at elevated temperatures we employ phenomenological laser modelling tools and rigorous full-physics simulations that utilize the finite-difference-time-domain method. In modern high-power diode lasers, free carriers in the active region are the primary culprit for optical absorption loss. To cut this loss, we engineer the optical mode – and this leads to higher device efficiency. Note that our laser designs are based on best practices employed by the high-power diode laser community, but we use additional optimization for our specific application.

Once we have finalized our laser designs, we grow the device's heterostructures on GaAs wafers in an MOCVD chamber, and then fabricate the devices using standard semiconductor processing techniques. Chips are cleaved into 19x1 emitter array bars, before high-reflectivity and anti-reflectivity coatings are applied to back and front facets, respectively. A typical device geometry has a 100 μm emitter width and a fill factor of 20 percent.

Following wafer fabrication, we flip-chip mount 19-emitter bars *p*-side down onto sub-mounts. Multiple wirebonds connect the back *n*-side of the laser bar to the *n*-electrode of the sub-mount. The resulting structure is attached to the jet impingement orifice plate and fluid manifold before high power, high temperature testing begins (see Figure 2 for the test set-up).

Higher powers

We have evaluated many of our 976 nm, 19-emitter laser bars, using coolant temperatures from 22 °C to 50 °C (see Figure 3 for some examples of our data). Tests involve driving lasers in continuous-wave mode and using a thermopile to measure the output power

as a function of drive current. Spectra are captured with a fibre-coupled spectrometer positioned at an oblique angle from the laser output.

At a 50 °C coolant temperature, one of our 19-emitter laser bars produced an output in excess of 73 W and a peak electrical-to-optical efficiency of 52 percent. Reducing the coolant to room temperature propelled the output power to over 90 W, with electrical-to-optical efficiency climbing to 57 percent. Output is produced from a single emission peak with a full-width-half-maximum of just 2.5 nm.

We have also tested our cooling technology using laser bars from commercial suppliers. The good news is that our technology has a universal benefit, with lasers from these suppliers showing a comparable performance at these elevated coolant temperatures to those that we have designed and fabricated at Freedom Photonics. Future design improvements are planned, which promise to spur another hike in the high-temperature efficiency of laser bar arrays produced by ourselves and other manufacturers.

The key result of our work is that our jet impingement cooler delivers a superior performance over commercial state-of-the-art microfluidic coolers, when industrial fluids or deionised water is used (see Figure 4 for a side-by-side comparison of cooler performance using a 10 mm by 4 mm uniform heat source that mimics the footprint of the 19-emitter laser diode array). This is highlighted by a measurement showing that our jet impingement cooler, filled with industrial fluid coolant, has a thermal resistance at the operating point that is more than three times lower than that of a commercial cooler designed for industrial fluid.

It is significant to note that our jet impingement cooler using industrial fluid also outperforms a commercial micro-channel cooler using deionised water – it requires only half the pumping power to achieve the same thermal resistance. This benefit of a lower fluid pumping power is magnified in larger multi-array diode pump systems. As discussed previously, the deionised water micro-channel cooler is not a good choice for many applications, due to its susceptibility to freezing, corrosion and clogging.

Our results show that our jet impingement cooler technology can achieve a lower thermal resistance than commercial state-of-the-art coolers, allowing for high-efficiency laser diode performance at elevated coolant temperatures. This technology enables diode pump systems with low size, weight, and power consumption, which target commercial and military applications requiring a broad range of high power lasers.

The authors would like to thank the High Energy Laser Joint Technology Office for their financial support of this work.

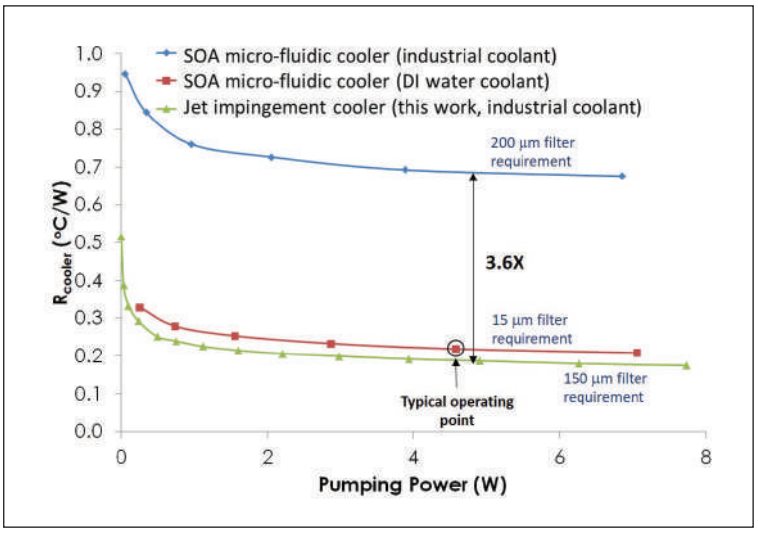


Figure 4. Data comparing different cooler types. The jet impingement cooler pioneered by Freedom Photonics and Teledyne is compared to two state-of-the-art (SOA) commercial coolers: one compatible with industrial coolants and one that requires deionised (DI) water only. Data was collected using a 10 mm x 4 mm uniform heat source that mimics the footprint of the 19-emitter laser diode array. The jet impingement cooler produced by Freedom Photonics and Teledyne (green triangle curve) shows 3.6-times lower thermal resistance at the operating point compared to a conventional commercial micro-channel cooler designed for industrial fluid (blue diamond curve). Both coolers can be used with industrial fluids, so they have 150-200 µm filtering requirements, which would be a robust and reliable design for use in a harsh environment. The jet impingement cooler also performs slightly better than a commercial micro-channel cooler for DI water (red square curve), even though the cooling mechanisms are quite different. The DI water cooler has a very strict 15-µm filtering requirement and is not suitable for many applications, due to its susceptibility to freezing, corrosion and clogging.

Further reading

P. Crump *et al.* Proc. Of SPIE **6104** 610409-1 (2006)

K. Boucke "Packaging of Diode Laser Bars," in High Power Diode Lasers, edited by Bachmann F., Loosen P. and Poprawe R., Springer Series in Optical Sciences (2007)

P. Crump *et al.* "Advances in High Efficiency Diode Laser Pump Sources Suitable for Pumping Nd:YAG Systems," OSA CLEO/PhAST (2007)

Y. Karni *et al.* High-Power Diode Laser Technology and Applications VI, edited by M. S. Zediker, Proc. Of SPIE **6876** 687604 (2008)

C. Feng *et al.*, J. of Semiconductors **30** 064005 (2009)

A. K. Chin et al. High-Power Diode Laser Technology and Applications IX, edited by M. S. Zediker, Proc. of SPIE Vol 7918, 79180L (2011)

Understanding microLED deficiencies

Decreasing LED size impacts efficiency, due to a hike in Shockley-Read-Hall recombination

A TEAM FROM Leti at CEA-Grenoble and the III-V Lab has undertaken the most comprehensive study to date of the relationship between the size of a microLED, its efficiency, and the contributions to its non-radiative recombination.

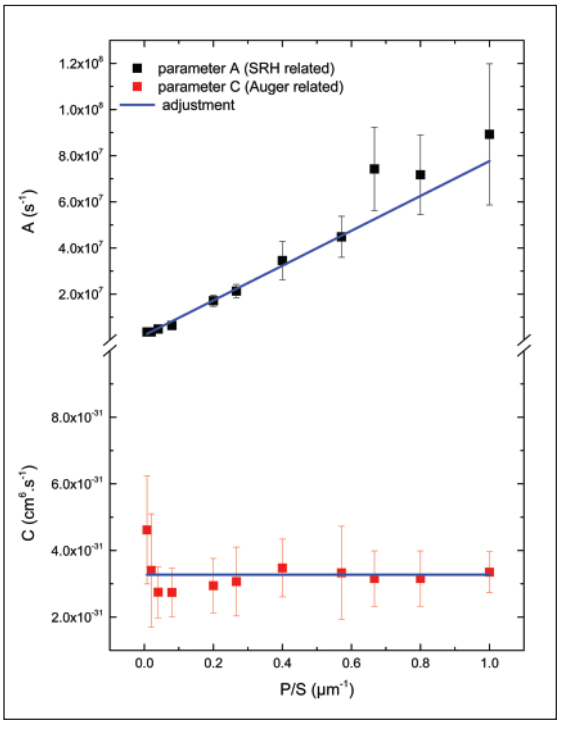
Lead author of the paper describing the effort, Francois Olivier, believes that the work is the first quantitative study of the interplay between the efficiency of the microLED and its size.

"We have in this study related the parameter *A*, of the well-known and accepted *ABC* model, to the geometry of the LED," says Anis Daami, a co-author of the paper.

The team found that the *A* coefficient, which represents Shockley-Read-Hall recombination, is strongly related to LED size. Meanwhile, the *C* coefficient, an indicator of LED droop, is independent of the size of the chip. The findings imply that sidewall defects have a massive impact on LED performance.

This insight will help to underpin the development of microLEDs, which can serve in virtual- and augmented- reality devices.

To understand the losses in microLEDs, the researchers undertook quantum efficiency measurements, at a range of current densities, on devices with dimensions ranging from 4 μm by 4 μm to 500 μm by 500 μm. These devices were made by applying a self-aligned process to MOCVD-grown, 4-inch GaN-on-sapphire epiwafers. The LEDs featured five 3 nm-thick InGaN quantum wells, and included an electron-blocking layer. "As of today, we do not have a specific study on the impact of the electron-blocking layer on LED performance," says Olivier.



As the dimensions of the microLED get smaller – and the ratio of its perimeter to its surface area increases – Shockley-Read-Hall recombination is more prevalent. This indicates that sidewall defects impair LED performance. The *C* coefficient, related to droop, is nearly independent of LED size.

Using the *ABC* model, and estimating light extraction efficiency from ray-tracing software, Olivier and co-workers obtained values for *A* and *C* coefficients that are consistent with those found in the literature.

They state that the *B* coefficient, on their devices, is independent of LED size, because photoluminescence intensity is uniform across the pixel surface, even for very small pixel sizes.

In stark contrast, the *A* coefficient increases by almost two orders of magnitude when the size of the LED is reduced from 500 μm to 4 μm. This reveals that non-radiative recombination at a low current density is related to the sidewall of the LED, rather than its volume.

The inherent downside of sidewalls and interfaces is that they introduce discontinuities in the lattice. In turn, these discontinuities lead to defects, which act as non-radiative recombination centres.

Oliver and Daami argue that the better the quality of the LED sidewall, the lower the defect density. "This has a major implication, which is a better LED efficiency, by improving the ratio of radiative to non-radiative recombination." One option for increasing microLED efficiency is to passivate the sidewalls.

The *C* coefficient for the microLED is nearly independent of its size. This indicates that droop, whatever its cause, is independent of size of the device.

Auger is probably the main cause of this droop, according to the team. However, they believe the debate in the literature is still open.

The team is currently working on improving its LED process technology. "Smaller pixel sizes and multi-colour displays are currently under investigation."

Reference

F. Olivier *et al.*
Appl. Phys. Lett. **111** 022104 (2017)

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UV LEDs exceed 1W output

Minimising imperfections enables GaN-silicon LEDs to deliver record-breaking powers

RESEARCHERS at Lattice Power and Suzhou Institute of Nano-Tech and Nano-Bionics (SINANO) claim to have set a new record for the output power of AlGaN-on-silicon LEDs. Their 385 nm devices, which have a chip size of 1.1 mm by 1.1 mm, deliver 1766 mW at 1A.

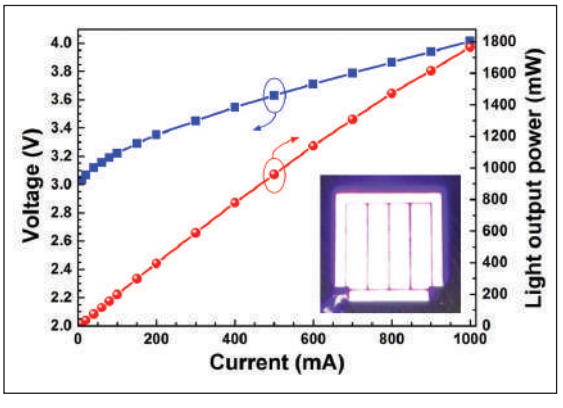
The insights obtained when developing these devices could be used to increase the performance of Lattice Power's UVA LEDs, which span 365 nm to 405 nm. These devices are used for LED curing, and are paired with phosphors to make lighting products that provide a broader spectral coverage than those based on the conventional combination of blue LEDs and phosphors.

Spokesman for the team, Qian Sun from SINANO, argues that one of the benefits of their approach is that it can slash the cost of production of high-power UV LEDs, thanks to the use of large-diameter silicon substrates.

"Secondly, the silicon substrates can be easily removed by wet etching, with little damage to the UV LED chips."

With the more common alternative, sapphire, laser lift-off is required to make high-power vertical chips. That's not ideal, according to Sun, as it can cause issues related to electrical leakage and reliability.

Regardless of the substrate, fabrication of deep UV LEDs is challenging, due to the need to grow AlGaN layers. Wafers can warp, bow and even crack, due to differences in the lattice constant and the coefficient of thermal expansion of the substrate and AlGaN. Complicating matters, the higher the aluminium content in the ternary, the greater the deterioration in crystal quality. This is a major impediment, as threading dislocations have a far bigger impact on the internal quantum efficiency of the UV LED than its blue cousin.



Driven at 1 A, UVA LEDs emitting at 385 nm produce more than 1.75 W at an external quantum efficiency of 44 percent.

To address all these issues, Sun and co-workers underpin their devices with an AlN/AlGaN multi-layer buffer that introduces compressive strain. Growth begins with a 300 nm-thick AlN layer, followed by 400 nm-thick $Al_{0.65}Ga_{0.35}N$, 600 nm-thick $Al_{0.17}Ga_{0.83}N$, 700 nm-thick $Al_{0.10}Ga_{0.90}N$, and finally a thick layer of $Al_{0.05}Ga_{0.95}N$.

By adding compressive strain, this structure not only compensates for the tensile strain that arises during cooling, but also induces the inclination and annihilation of threading dislocations. The filtering of these defects is seen in images obtained with a cross-sectional transmission electron microscope.

On top of the buffer structure is added a strain relief layer, in the form of an InGaN/AlGaN superlattice. It nucleates and enlarge V-pits in the light-emitting region, and improves device performance by increasing output power and reducing forward voltage.

Deposited on top of the superlattice and buffer structure is the device structure, which features a five-period multi-quantum well. UVA LEDs with a vertical thin-film architecture are then formed by adding to the epiwafer a metal stack – including a bonding layer and a silver-based layer that acts as a *p*-type electrode and mirror – and then attaching this structure to a conductive silicon carrier that provides subsequent mechanical support. Chemical etching removes the substrate, before etching with potassium hydroxide roughens the *n*-type AlGaN, enabling an increase in extraction efficiency.

Driven at 500 mA, using a forward voltage of 3.63 V, encapsulated LEDs produce 960 mW at an external quantum efficiency (EQE) of 53 percent. Increasing the voltage to 4.1 V propels drive current to 1 A and output to 1766 mW, but EQE falls to 44 percent.

These UVA LEDs have a differential series resistance of 0.76 Ω, which is a little higher than the best blue high-power LEDs. To trim this resistance, Sun and co-workers will optimise silicon and magnesium doping.

Another of their goals is to develop short-wavelength devices, such as those emitting in the UVB and UVC. "All these efforts will greatly reduce the cost of UV light emitters," argues Sun.

Reference

Z. Li et al. Appl. Phys. Express 10 072101 (2017)

Uncovering the origin of stacking faults

Transmission electron microscopy pinpoints the origin of stacking faults in bipolar SiC power devices

ONE MYSTERY surrounding the SiC bipolar device is this: Where is the origin of the expansion of its stacking faults?

Following years of speculation, there is now a definitive answer – the faults stem from Basal plane dislocations in the substrate, which have been exposed by a series of high-spatial-resolution transmission electron microscopy images obtained by a team from Japan.

The collaboration between researchers at the Advanced Power Electronics Research Center, Toray Research Center, Showa Denko and Fuji Electric, arrived at this conclusion after scrutinising bipolar devices riddled with long stacking faults. These faults extend from basal plane dislocations, and are converted into threading edge dislocations.

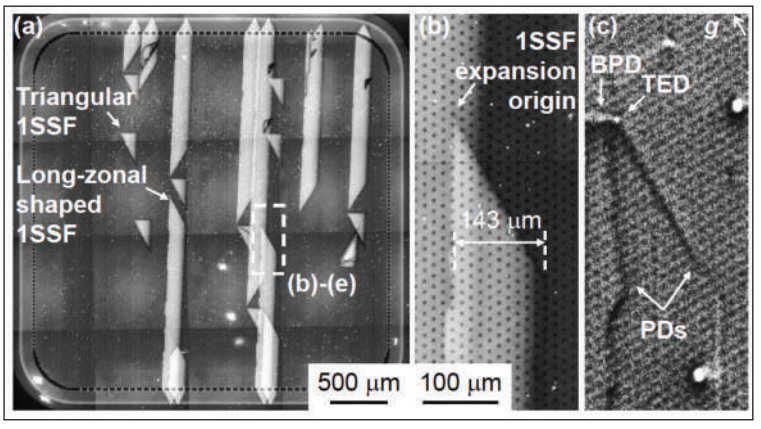
Spokesman for the team, Shohei Hayashi from the Advanced Power Electronics Research Center, points out that the conversion process can suppress Basal plane dislocations within the epitaxial layer. However, conversion to threading edge dislocations cannot prevent forward-current degradation, which arises from an electron-hole recombination process that causes stacking faults to increase. Current degradation is a major issue as it impacts long-term device reliability.

These findings are a significant concern because bipolar devices, such as *p-i-n* diodes and IGBTs, are promising candidates for improving the performance of power electronics. For example, SiC diodes based on a *p-i-n* junction, rather than a Schottky barrier, can realise higher voltages – although this is at the expense of greater switching losses.

The team produced the *p-i-n* diode that it has investigated. On a 345 μm-thick *n*-type substrate with a doping of 6.4 x 10^{18} cm^{-3}, the researchers grew a 10 μm-thick *n*-type layer with a doping of 1 x 10^{16} cm^{-3}, and then formed a *p*-type anode region via aluminium implantation at 500 ˚C and subsequent annealing.

After adding electrodes, the researchers subjected their *p-i-n* diode to a constant-current stress test, using a current density of 600 A cm^{-2}. After the electrodes were removed, the device was investigated with photoluminescence and X-ray topography.

Single Shockley-type stacking faults (1SSFs) were seen in photoluminescence images with a 420 nm band-pass filter. This revealed triangular and long-zonal-shaped faults (see Figure (a)). The later causes a greater increase in resistance, due to the larger area. Inspection of an enlarged area of this photoluminescence image (b) reveals that the 1SSF width in the step-flow direction is 143 μm, which indicates that the long-zonal-shaped 1SSF has expanded on the basal plane over the entire epitaxial layer.



(a) Photoluminescence, using a 420 nm band pass filter, identifies single Shockley-type stacking faults (1SSFs). (b) An enlarged photoluminescence image shows that the long-zonal-shaped 1SSF has expanded on the basal plane over the entire epitaxial layer. (c) X-ray topography reveals that a Basal plane dislocation (BPD) in the substrate has dissociated into two partial dislocations (PDs) near a threading edge dislocation (TED), resulting in a long-zonal-shaped 1SSF.

X-ray topography of the area shown in (b) reveals that a Basal plane dislocation in the substrate has dissociated into two partial dislocations near a threading edge dislocation, resulting in a long-zonal-shaped 1SSF (see (c)). This finding, along with images from different diffraction conditions, reveals that the 1SSF expansion originated from the Basal plane dislocation, which was converted into a threading edge dislocation near the interface between the epitaxial layer and the substrate.

Transmission electron microscopy shows that the 1SSF expansion originates from a Basal plane dislocation converted into a threading edge dislocation. This technique also reveals the expansion of the 1SSF into the substrate. Hayashi suggests that to prevent this from happening, a recombination–enhanced layer can be inserted between the drift layer and the substrate: "Because the electron-hole recombination occurs in the recombination-enhanced layer, minority carriers cannot reach into the substrate."

Reference

S. Hayashi *et al.* Appl. Phys. Express 10 082101 (2017)

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VENDOR VIEW Proton Site

On-site hydrogen generation: smart choice to improve process results

Hydrogen is widely used to support a variety of industrial applications worldwide, due to its ability to meet the specific needs of high purity industrial applications, ranging from semiconductor manufacturing and epitaxy to heat treating and materials processing.

Relying heavily on hydrogen to maintain process results, many operations personnel are responsible for evaluating which gas supply method will best suit their operation. Over time, this task can become daunting, because as businesses grow, increasing amounts of hydrogen are needed to satisfy elevated levels of production demand. This spike in hydrogen usage has translated into a collection of issues for facility operation.

Hassles such as inefficient production practices, fire permit restrictions, space limitations, increased costs, dangerous hydrogen storage and handling can make gas sourcing especially problematic.

Offering clear advantages over older, conventional methods of hydrogen supply such as delivered gas, dissociated ammonia and exo or endo gas, hydrogen generated on-site is a drier and safer alternative.

A high performance solution to suit businesses small and large, on-site gas generators satisfy demand by producing hydrogen at its point of use with no inventory of flammable or poisonous gas. Hydrogen generation systems are easy to permit, easy to install, and operate automatically.

Market data shows more and more stakeholders are making the switch to gas generators, eliminating the need for delivery and storage of hazardous gases within the industry.

With more than 2,500 systems installed in over 75 countries, Proton OnSite hydrogen generators are consistently creating value around the world. Utilizing advanced Proton Exchange Membrane (PEM) electrolysis, with a high differential pressure design, our on-site hydrogen generators produce very pure hydrogen in a safe, reliable, and cost effective package.

Our industrial customers are particularly impressed with the fact that they are able to realize rapid paybacks while dramatically improving facility safety. The on-site generators eliminate the need for stored hydrogen, while meeting the daily requirements of various industrial processes. Thus, providing an attractive return on investment for customers and improving site security, safety and personnel productivity.

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