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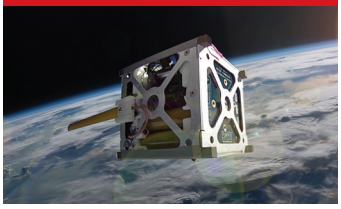
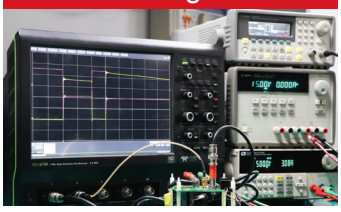
Diamond draws the heat from GaN HEMTs

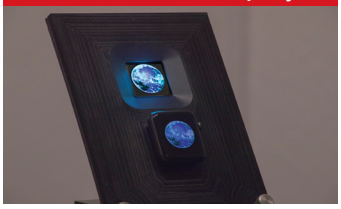


Creating transparent circuits with GaN

Obliterating dynamic on-resistance degradation



Making smart watches with microLED displays



Electric vehicles enhance the prospects for SiC

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Viewpoint

By Dr Richard Stevenson, Editor

GaN-on-diamond gathers pace

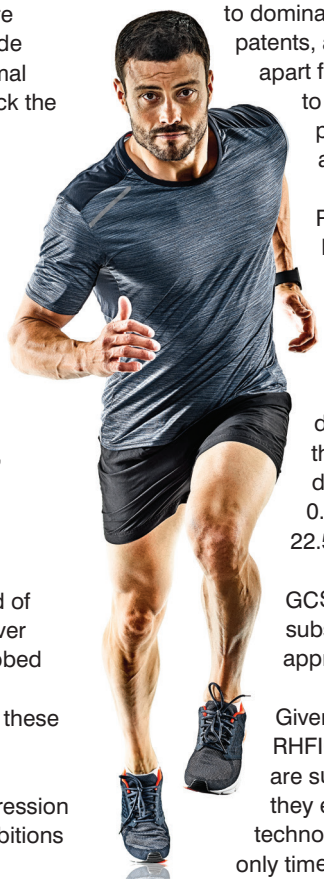
YOU AND I both know that the uses of diamond are not limited to jewellery. Unlike those working outside our industry, we are aware of the exceptional thermal conductivity of this material, and its capacity to suck the heat out of devices placed on top of it.

Championing the capability of GaN-on diamond is Felix Ejeckman. He invented the technology at Group4Labs, took it to new heights when this company was bought by Element Six, and more recently has co-founded Akash Systems, which is working on getting GaN-on-diamond products on board satellites (see p 20 for details).

But Akash is by no means alone in advancing this technology. Other companies are getting involved, creating a strengthening supply chain, as I discovered when attending the inaugural Diamond D-Day meeting.

At this one-day gathering, held in Bristol at the end of January and attended by 120 delegates from all over the world, makers of diamond deposition tools rubbed shoulders with the suppliers of GaN-on-diamond epiwafers and those that offer foundry services for these materials.

One company that made a particularly strong impression was the South Korean outfit RHFIC, which has ambitions to dominate the GaN-on-diamond market. It has over 60 patents, and intellectual property that covers all markets, apart from the commercial satellite sector. Its vision is to see GaN-on-diamond replace GaN-on-SiC, with products serving in self-driving cars, military radar, and industrial, medical and scientific sectors.



RHFIC produces GaN-on-diamond epiwafers at both its R&D facility in the US, and its production line in Korea. At the latter, the aim is to crank up production to 100 wafers per month.

One company capable of processing these wafers into devices is GCS. This foundry has developed techniques for running this material through its automated lines, and has produced devices with encouraging results. These include 0.65 μm HEMTs producing a power density of 22.5 W/mm at 2 GHz when biased at 100 V.

GCS is also developing a process to realise through substrate vias. Initial results are validating the approach.

Given the impressive efforts by the likes of Akash, RHFIC and GCS, sales of GaN-on-diamond devices are sure to grow over the next few years. But will they ever overtake GaN-on-SiC, and be the dominate technology in the GaN RF market? Probably not, but only time will tell.

Editor Richard Stevenson richardstevenson@angelbc.com +44 (0)1291 629640
Contributing Editor Rebecca Pool editorial@rebeccapool.com
News Editor Christine Evans-Pughe chrise-p@dircon.co.uk
Sales Executive Jessica Harrison jessica.harrison@angelbc.com +44 (0)2476 718209
USA Representatives Tom Brun Brun Media tbrun@brunmedia.com +001 724 539-2404
Janice Jenkins jjenkins@brunmedia.com +001 724-929-3550
Publisher Jackie Cannon jackie.cannon@angelbc.com +44 (0)1923 690205
Director of Logistics Sharon Cowley sharon.cowley@angelbc.com +44 (0)1923 690200
Design & Production Manager Mitch Gaynor mitch.gaynor@angelbc.com +44 (0)1923 690214

Circulation Director Jan Smoothy jan.smoothy@angelbc.com +44 (0)1923 690200
Chief Executive Officer Stephen Whitehurst stephen.whitehurst@angelbc.com +44 (0)2476 718970

Directors Bill Dunlop Uprichard – EC, Stephen Whitehurst – CEO, Jan Smoothy – CFO, Jackie Cannon, Scott Adams, Sharon Cowley, Sukhi Bhadal

Published by Angel Business Communications Ltd, Unit 6, Bow Court, Fletchworth Gate, Burnsall Road, Coventry CV5 6SP, UK. T: +44 (0)2476 718 970 E: info@angelbc.com

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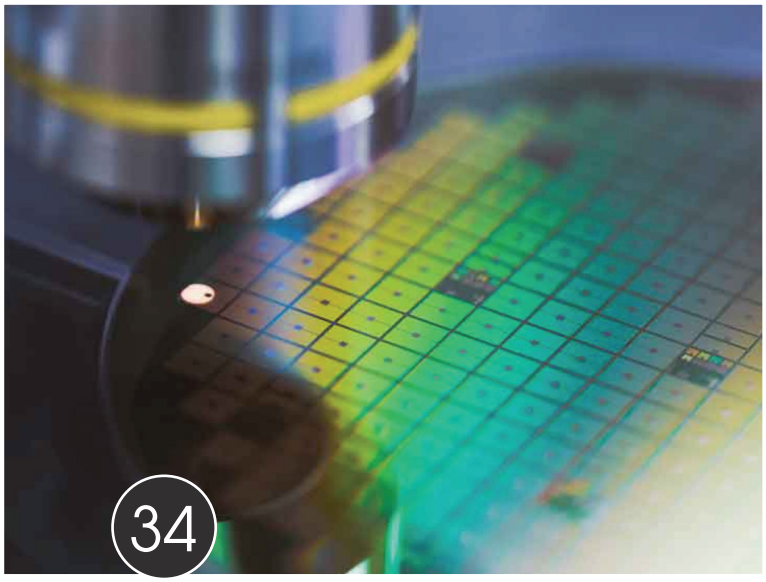
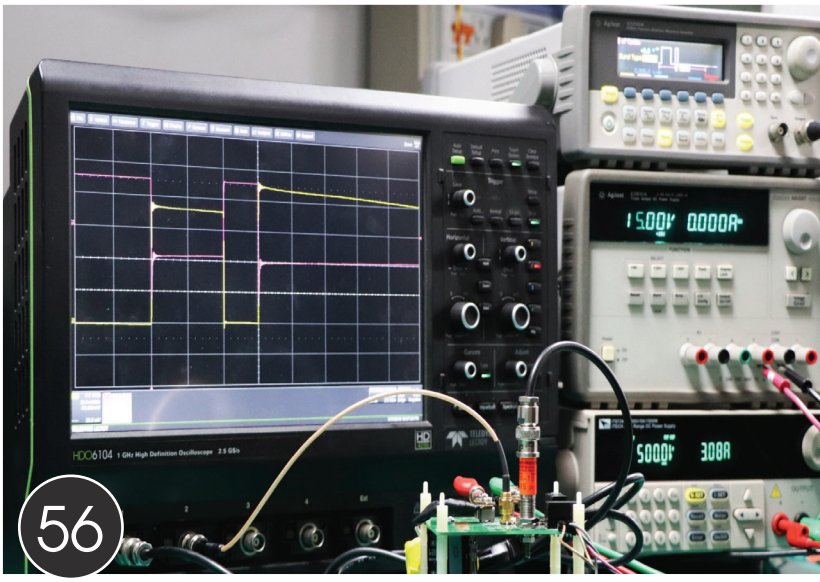
Volume 25 ISSUE 2 MARCH 2019

CONTENTS





news

news analysis

research review

ARPA-E awards $35 million for power device research

THE US DEPARTMENT OF ENERGY has announced $35 million in awards for 12 projects that find new ways to harness medium-voltage electricity for applications in industry, transportation, on the grid and beyond.

The selected projects are part of ARPA-E's Building Reliable Electronics to Achieve Kilovolt Effective Ratings Safely (BREAKERS) programme, as well as the latest OPEN+ cohort, Kilovolt Devices.

"America's energy landscape is constantly evolving, and as new ways to generate and distribute power gain popularity, it's critical we develop the tools to maximise their utility," said US Secretary of Energy Rick Perry. "These ARPA-E projects serve first and foremost to modernise how we move power around safely, reliably and efficiently, creating a new set of capabilities for tomorrow's utilities and industry. "

The eight BREAKERS projects will work to develop new direct current (DC) devices to better manage power by eliminating electrical faults, improving efficiency and reaction times, and potentially enabling greater proliferation of energy storage and renewable resources. The four Kilovolt Devices OPEN+ projects will focus on a variety of challenges facing power electronics

in the medium-voltage space, with a particular eye toward grid security and reliability.

Today's power distribution networks are primarily powered by alternating current (AC) electricity, but DC can provide lower distribution losses and higher power carrying capacity. BREAKERS projects will develop DC devices that prevent electric arcing, a safety hazard, while handling large amounts of power and voltage.

Medium-voltage DC circuit breakers could enable significant improvements in the United States' electrical system, transforming how electricity is delivered and managed across the entire power grid, as well as critical applications in industry, transportation, and resource production.

Example projects include $3,760,000 awarded to Eaton to develop a DC Wide Bandgap Static Circuit Breaker. Eaton will develop a SiC-based direct-current circuit breaker design that boosts efficiency and can scale up or down medium-voltage application requirements. The team's comprehensive approach includes a robust design that effectively dissipates excess energy and autonomously coordinates fault protection across multiple devices. The project results will extend to future ultra-wide bandgap power semiconductor devices and other advances affecting future generations of devices and power electronics.

Ohio State University has been awarded $2,211,712 to develop GaN semiconductor materials suitable for high voltage (15-20 kV) power control and conversion. The team will develop a unique method to grow thick GaN films with low background impurity contamination, necessary to allow high voltage operation with high efficiency.

The thick GaN layers will be deposited on high-quality bulk GaN base materials with reduced defects, critical to depositing high-quality GaN films on top, and perform high-voltage device design, fabrication, and testing to provide feedback for further GaN material growth and optimisation.

Macom and STMicro ramp GaN-on-silicon support for 5G

MACOM TECHNOLOGY and STMicroelectronics have announced the 2019 expansion of 150 mm GaN-on-silicon production capacity in ST's fabs, and 200 mm as demand requires. The expansion is designed to service the worldwide 5G Telecom buildout. This builds upon the broad GaN-on-silicon agreement between Macom and ST announced in early 2018.

The global rollout of 5G networks and move to Massive MIMO (M-MIMO) antenna configurations is expected to create a substantial increase in the demand for RF Power products. Specifically, Macom estimates there will be a 32x to 64x increase in the number of Power Amplifiers required. In turn, this is expected to more than triple dollar content over the course of a 5-year cycle of 5G infrastructure investment and thus drive an estimated 10x to 20x decrease in the cost per amplifier.

"Major base station OEMs understand they need wide bandgap GaN performance with transformational cost structures and manufacturing capacity to meet 5G antenna cost, range and energy efficiency targets in the field. By teaming with ST, we believe Macom is uniquely poised to provide it all — performance, cost and high-volume supply chain," said John Croteau, President and CEO of Macom. "We anticipate that our joint investment at this early stage in bringing on more capacity positions for us to service up to 85 percent of the global 5G network buildout."

"ST has built a strong foundation as a global leader in SiC and we are now moving forward with RF GaN-on-silicon, which will enable OEMs to build a new generation of high-performance 5G networks," said Marco Monti, president of the Automotive and Discrete Product Group, STMicroelectronics. "While SiC is ideal for certain power applications such as automotive power conversion, GaN-on-silicon provides the necessary RF performance, scale, and commercial cost structures to make 5G a reality. With this move ST and Macom aim to unlock the industry bottleneck and fulfil the demand for 5G buildouts."

Cree boosts horticulture efficiency with new red LEDs

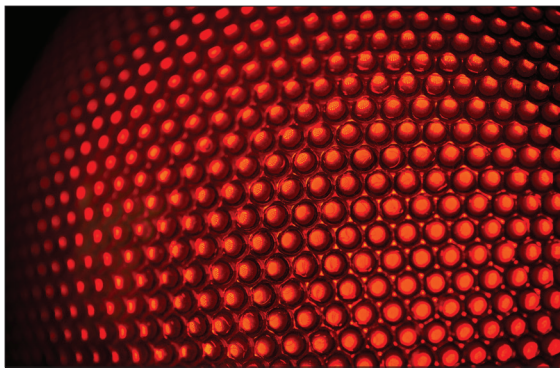
CREE has announced the next-generation XLamp XP-E2 Photo Red (660 nm) and Far Red (730 nm) LEDs, delivering higher performance for horticulture applications.

The new Red XP-E2 LEDs provide a drop-in upgrade for the previous generation that outperforms competing LEDs by up to 68 percent. These higher-performance horticulture LEDs make it more affordable to grow food under optimised lighting, according to Cree.

"Lettuce and tomato farmers in the UK, the Netherlands and Belgium are choosing our Hyperion grow lights, powered by Cree's horticulture LEDs, as the primary light source for their large indoor, state-of-the-art growing facilities," said Jonathan Barton, director of Grow Lighting at Plessey Semiconductors.

"Our customers like that the Hyperion lights replace 1000 W sodium lights one-for-one with up to 40 percent energy savings that are enabled by Cree LEDs. We are pleased that Cree is delivering this efficiency upgrade in a form that's easily integrated, so that we can quickly improve our product's performance." The new XP-E2 LEDs are a drop-in upgrade for existing XP-based horticulture designs with the same mechanical and optical characteristics as the previous generations.

With up to 57 percent improvement in Far Red and up to 21 percent improvement in Photo Red, this new generation of XP-E2 LEDs delivers industry-leading output levels and efficiency within their performance class. "LEDs for specialty applications, including architectural lighting and horticulture, are a core part of our product strategy," said Claude

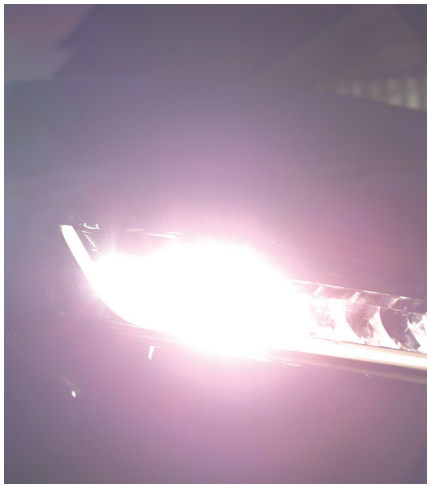


Demby, Cree LEDs senior vice president and general manager. "Cree is first to enable full spectrum luminaires that employ Photo Red and Far Red LEDs to deliver 50 percent energy savings over sodium-based lighting systems. This upgrade to our horticulture LEDs demonstrates our commitment to delivering industry-leading high-power LED performance."

Laser light for cars

OSRAM has introduced the PLPT9 450D_E A01 – a second generation blue multi-mode laser diode designed to be a light source for auxiliary high beam that doubles the range (compared to previous LED solutions) to 600 meters. It also simplifies the system design, according to the company.

"With our newly developed laser diode, car lights can be designed and built even smaller than before– without compromising light output. It combines powerful light with compact dimensions," explains Walter Rothmund, marketing manager automotive for Emitter Laser Sensor at Osram Opto Semiconductors. In terms of brightness, laser diodes offer advantages compared to LEDs.



At a typical operating current of 2.2 A, the blue PLPT9 450D_E A01 laser reaches an optical output of 3.5 W and emits blue light with a wavelength of 447 nm. With the help of appropriate optics, the laser light is focused at a point only a few micrometers in diameter. A special phosphor converter converts the blue light into white light required for front lighting applications. The luminance achieved is three times higher than that of an LED light source. In comparison, the laser produces 600 cd/mm^2 while LEDs deliver around 200 cd/mm^2.

The PLPT9 450D_E A01 laser diode qualified for use in cars is approved for an operating temperature range of -40°C to 120°C. Compared to the first generation with three pins, the TO90 package contains only two pins, which allows for much easier connection and heat dissipation. The laser's compact dimensions of 9 mm in diameter and a height of < 4.5 mm (without contact pins) mean that headlights can be built much smaller in the future, says Osram.

II-VI introduces 56 Gb/s PAM4 VCSEL arrays

OPTICAL COMPONENT FIRM II-VI has introduced its 56 Gb/s PAM4 VCSEL arrays for 400 gigabit Ethernet (GbE) short reach transceivers and active optical cables (AOCs) deployed in data centres.

The availability of Ethernet equipment with greater than 12 Tb/s of switching capacity enables hyperscale data centres to accelerate the migration from 100 to 400 GbE transmission. II-VI's 8-element VCSEL arrays can be modulated at 56 Gb/s using 4-level pulse amplitude modulation (PAM4) to achieve a combined 400 Gb/s over short reach multimode links.

"Customers come to II-VI because of our ability to deliver differentiated VCSEL technology without ever compromising on reliability," said Karlheinz Gulden, general manager, II-VI Laser Enterprise. "Our new 56 Gb/s PAM4 VCSEL arrays represent the leading edge in VCSEL technology for AOCs and transceivers, which are in high demand in data centres for server to server connectivity."

AOCs and transceivers based on VCSELs offer the most cost effective solution for datacenter links that span from 10 to 300 meters. They enable new applications in consumer electronics to connect ultrathin HDTV screens to remotely located driver electronics. The demand for VCSELs is expected to accelerate, driven by a growing number of 3D sensing applications in automotive and consumer electronics.

Qorvo ships 100 million RF devices for 5G

RF COMPANY Qorvo has announced that it has shipped over 100 million 5G wireless infrastructure components since January 2018. It released the news at Mobile World Congress 2019, February 25-28, in Barcelona.

Qorvo's 5G portfolio includes solutions for both the receive and transmit RF front end, enabling customers to use beamforming with massive multiple-in/multiple-out (MIMO) base stations to achieve higher data capacity, wider coverage, and indoor penetration using sub-6 GHz frequencies.

The installation of new 5G networks using massive MIMO architectures have created demand for new products supporting higher frequencies and increased integration. Qorvo's portfolio includes dual-channel low noise amplifiers (LNAs) integrated with high-power-handling switches, high linearity transmit pre-drivers, and final stage power amplifiers (PAs). Qorvo's GaN-based PAs for all sub-6Gz 5G bands feature fully integrated Doherty solutions that support the higher frequency, small size, weight, power consumption and thermal management requirements for 5G equipment.

Roger Hall, general manager, Qorvo High Performance Solutions, said: "Qorvo is enabling mobile operators to enhance their existing network capacity and transition to 5G with minimal effort. Our technology leadership with massive MIMO based on beamforming is revolutionizing the base station market and accelerating the path to 5G."

New Qorvo products that are available now to wireless infrastructure customers include the QPB9337 Dual-Channel Switch LNA module, the QPL9057 Ultra-Low NF LNA, and the QPA3503 Doherty Power Amplifier module.

RF GaN growing at 23 percent CAGR

THE RF GaN industry is showing an impressive growth with a 23 percent CAGR between 2017 and 2023, driven by telecom and defence applications.

By the end of 2017, the total RF GaN market was close to $380 million and 2023 should reach more than $1.3 billion with an evolving industrial landscape. Telecom and defence are looking for innovative technologies and RF GaN-based devices are directly answering to the market demand.

Defence remains a major RF GaN market segment, as its specialised high-performance requirements and low price sensitivity offer many opportunities for GaN-based products. In 2017-2018, the defence sector accounted for more than 35 percent of the total GaN RF market, and the global defence market shows no signs of slowing down.

“We believe this important GaN market segment will continue growing along with GaN’s overall penetration rate,” says Hong Lin, senior technology and market analyst at Yole Développement (Yole), part of Yole Group of Companies.

Yole’s partner, Knowmade, has recently looked at more than 3,750 patents published worldwide up to October 2018 and produced a report based on its analysis. The patents apply to RF GaN epiwafers including GaN-on-SiC and GaN-on-silicon, RF semiconductor devices, including HEMTs and HBTs, integrated circuits, including RFICs and MMICs, operating methods and packaging, for all functions, such as RF PAs, RF switches and RF filters and from radio frequencies <6GHz to microwaves >6GHz and mm-waves >20GHz.

“Cree (Wolfspeed) indisputably has the strongest IP position, especially for GaN HEMTs on SiC substrate,” says Nicolas Baron, CEO and co-founder of Knowmade. “Sumitomo Electric, the market leader in RF GaN devices, is well positioned but far behind Cree.”

Furthermore, Sumitomo Electric has been slowing down its patenting activity while other Japanese companies like Fujitsu, Toshiba and Mitsubishi Electric are increasing their patent filings and thus today have strong patent portfolios as well.

Intel and Macom are currently the most active patent applicants for RF GaN, both especially for GaN-on-silicon technology, and are today the main IP challengers in the RF GaN patent landscape.

Other companies involved in RF GaN market, such as Qorvo, Raytheon, Northrop Grumman, NXP/Freescale, and Infineon, hold some key patents but do not necessarily have a strong IP position. CETC and Xidian University dominate the Chinese patent landscape with patents on GaN RF technologies targeting microwave and mm-wave applications. And the emerging foundry HiWafer, entered the IP landscape three years ago, is today the most serious Chinese IP challenger.

From a device perspective, Cree (Wolfspeed) has also taken the lead in the GaN HEMT IP race for RF applications. “The analysis of Cree’s RF GaN patent portfolio shows it can effectively limit patenting activity in the field and control the freedom-to-operate of other firms in most key countries,” explains Baron from Knowmade.

Intel, which entered the GaN HEMT patent landscape later, is currently the most active patent applicant and it should strengthen its IP position in coming years, especially for GaN-on-silicon technology. New entrants in the GaN RF HEMT related patent landscape are mainly Chinese players: HiWafer, Sanan IC and Beijing Huajin Chuangwei Electronics.

Other noticeable new entrants are Taiwan’s TSMC and Wavetek Microelectronics, Korea’s Wavice and Gigalane, Japan’s Advantest, and America’s Macom and ON Semiconductor.

SUSS opens excellence centre in Switzerland

SUSS MICROOPTICS is setting up an excellence centre in Neuchâtel Switzerland for manufacturing wafer-level optics (WLO) in order to meet the increase in demand for precision optics applications.

Among the various structures that can be manufactured at wafer-level, freeform micro-optic arrays are one of the most challenging, as they have no rotational symmetry. Thanks to this property, they can generate new light distribution patterns, correct for aberrations, as well as improve miniaturisation of the optical systems.

This will be key for driving the volume production of new optics for volume markets such as automotive, transportation, lighting, augmented reality, medical, datacom, consumer electronics etc. The excellence centre will be part of 800m^2 of new cleanroom space currently built in Neuchâtel and certified for the main markets targeted by SUSS MicroOptics.

The European photonic industry Consortium (EPIC) has consistently shown strong support for European funded Photonics Pilot Lines manufacturing photonic devices. EPIC is already the dissemination partner of the MIRPHAB pilot lines (manufacturing of MID-IR photonics sensors), PIXAPP (manufacturing of packaged integrated photonic devices) and InPULSE (manufacturing of photonic integrated circuits based InP).

Jose Pozo, EPIC's CTO, claims "these European pilot lines, whether funded or not by the EU, are essential for the exploitation of the great innovations in photonics in Europe.

Photonics21 and the Photonics public private partnership, are playing the necessary role for manufacturing of Photonics, as a key enabling technology, in Europe. We strongly believe that such pilot lines are the best way of enabling the manufacturing of photonics in Europe to customers worldwide and of valorising and monetising the photonics innovations which have positioned Europe in the lead of photonics R&D."

The expertise of SUSS MicroOptics, based on imprint technologies, enables the production of the last mile in optics: the so-called freeform micro-optics, mainly optical diffractive, refractive or reflective components with no rotational symmetry. Until now most freeform optics applications have been in niche markets, such as space and others.

Recently however, high volume applications in consumer markets especially in automotive, mobile phones, lighting and high-end cameras have emerged. According to SUSS MicroOptics, the goal is to enable volume manufacturing from pilot production all the way to high-volume production in Europe and in particular in Neuchâtel.

Neuchâtel was chosen as the location because of the city's long-standing connection with the high-end watch industry and its role in transforming expensive, low-volume technologies to higher volumes, keeping high quality standards while reducing costs.

CSEM, a Research Technology Organisation (RTO), has traditionally been the link between R&D lines and user applications. Rolando Ferrini, Section Head MicroNano Optics & Photonics at CSEM has been appointed in charge of linking wafer-level R&D lines to volume manufacturing.

As he says: "finding synergies between the huge technological developments in wafer-level micro-optics, which have happened in Europe in the last decade, mostly funded by European H2020 grants and regional funds, positions today Europe as a leader in bringing freeform micro-optics to higher volumes: it is now or never to create volume manufacturing capabilities in Europe in this strategic field, which is foreseen to have strong impact in several application domains."

The SUSS Excellence Centre will use SUSS MicroTec's manufacturing equipment to provide manufacturing services which can be scaled up to contract manufacturing. SUSS MicroOptics CEO, Reinhard Völkel says: "the best way of bringing high-quality freeform micro-optics in applications such as microlens arrays for cameras, is to prove the pilot production of such micro-optics in Neuchâtel and other locations in Europe.

The goal must be to convince high-volume companies that they can start pilot production with us and scale to volume production either by licensing or by replicating SUSS's production process in their own facilities by using European equipment. This is key for European innovation and most importantly for the smart use of R&D innovation funds"

JEDEC WBG committee publishes first document

JEDEC Solid State Technology Association, a standards development organisation for the microelectronics industry, has published JEP173: Dynamic On-Resistance Test Method Guidelines for GaN HEMT Based Power Conversion Devices. This is the first publication developed by JEDEC's newest main committee, JC-70 Wide Bandgap Power Electronic Conversion Semiconductors.

The document is available for free download from the JEDEC website. JEP173 addresses a key need of the user community of GaN power FETs, namely a method for the consistent measurement of Drain-to-Source Resistance in the ON-state ($R_{DS(ON))}$ encompassing dynamic effects. These dynamic effects are characteristic of GaN power FETs, and the value of the resulting measured ($R_{DS(ON))}$ is method dependent.

"JEP173 demonstrates how quickly the GaN industry came together to address this important topic and begin to establish standards across suppliers for datasheet, qualification, and test methods," noted Stephanie Watts Butler, technology innovation architect at Texas Instruments and the chair of JC-70. "The release of JEP173 will help accelerate industry-wide adoption of GaN by ensuring consistency across the supplier base."

Formed in October 2017 with twenty-three member companies, JC-70 now has over fifty member companies, which underscores industry interest in the development of universal standards to help advance the adoption of wide bandgap (WBG) power technologies.

Global multinational corporations and technology startups from the US, Europe, Middle East, and Asia are working together to bring to the industry a set of standards for reliability, testing, and parametrics of WBG power semiconductors. Committee members include industry leaders in power GaN and SiC semiconductors, as well as prospective users of wide bandgap power devices, and test and measurement equipment suppliers. Technical experts from universities and national labs also provided inputs into the new JEP173 guideline.

"Strong commitment from the committee members was required to complete this work to set up universal standards to help advance the adoption of wide bandgap (WBG) power technologies." remarked Tim McDonald, senior advisor to Infineon's CoolGaN programme and the chair of the JC-70.1 subcommittee. "Our Task Groups are diligently making progress on other key GaN and SiC guidelines in the areas of test, reliability, and datasheets."

Glo on cusp
of commercialization

A smart watch made from Glo's micro-LEDs could be on your wrist very soon, reports Rebecca Pool.

THEY'VE BEEN QUITE A WHILE coming but later this year, smart watches with microLED displays, manufactured by Glo, should be commercially available.

Based on red, green and blue microLEDs, Glo's prototype wearable display measures 1.5 inches in the diagonal and packs in 264 pixels per inch. Crucially, the 20 μm InGaN microLEDs deliver extraordinary clarity on the same low-temperature polycrystalline silicon backplane used in liquid crystal and organic light emitting diode displays.

And while today's OLED displays produce a brightness of 1000 nits, Glo's display generates a dazzling 4000 nits, draws less than 1 W of power, and combines a wide colour gamut with a 120 Hz refresh rate.

"Our displays deliver ten times more brightness and five times more power efficiency than an OLED display," highlights Glo chief executive, Fariba Danesh.

"We are working with our manufacturing partners to launch in the latter half of this year, and we feel very confident and comfortable with this," adds Glo executive chairman, Aniruddha Nazre.

Since spinning out from Sweden-based Lund University back in 2005, Glo has attracted more than US$150 million in funds from numerous investors including pan-European venture capital firm, Wellington Partners, Sweden-based Foundation Asset Management and most notably, Google Inc.

As Danesh points out, the company now comprises 65 employees, the majority of which are technologists, and many with in-depth experience in compound semiconductors. Since the Google cash injection – the tech giant took a 13 percent stake in Glo – employees have been focused on producing devices, especially the smart watch, on low-temperature polycrystalline silicon (LTPS) backplanes.

"If the microLED display is to compete with OLED displays, it really has to leverage the existing LTPS backplane infrastructure," says Nazre. "So we've been working with the major suppliers of these backplanes and have a manufacturing agreement in place, with a second following soon."

Crucially, Glo's microLEDs, operate efficiently at very low currents – they are one-hundredth of that of typical LEDs. Operating at these microamp currents makes Glo's devices suitable for use with displays that are driven by transistors on LTPS glass substrates, as well as CMOS substrates. Indeed, as Nazre emphasises, Glo is, right now, the only company making microLED displays using off-the-shelf commercial LTPS backplanes.

At the same time, the company has also been scaling LED manufacture of its red, green and blue microLEDs. As Nazre puts it: "Customers will want half a million, a million, five million or even more watches; if you cannot solve the capacity problem for them they will never touch you and commercialisation will always just be a pipe dream."

To this end, Glo's microLEDs have, from word go, been designed with standard LED equipment at the company's pilot line in Sunnyvale, California. As a result, Danesh reckons the company can 'import' its processes into a high-volume LED facility very easily.

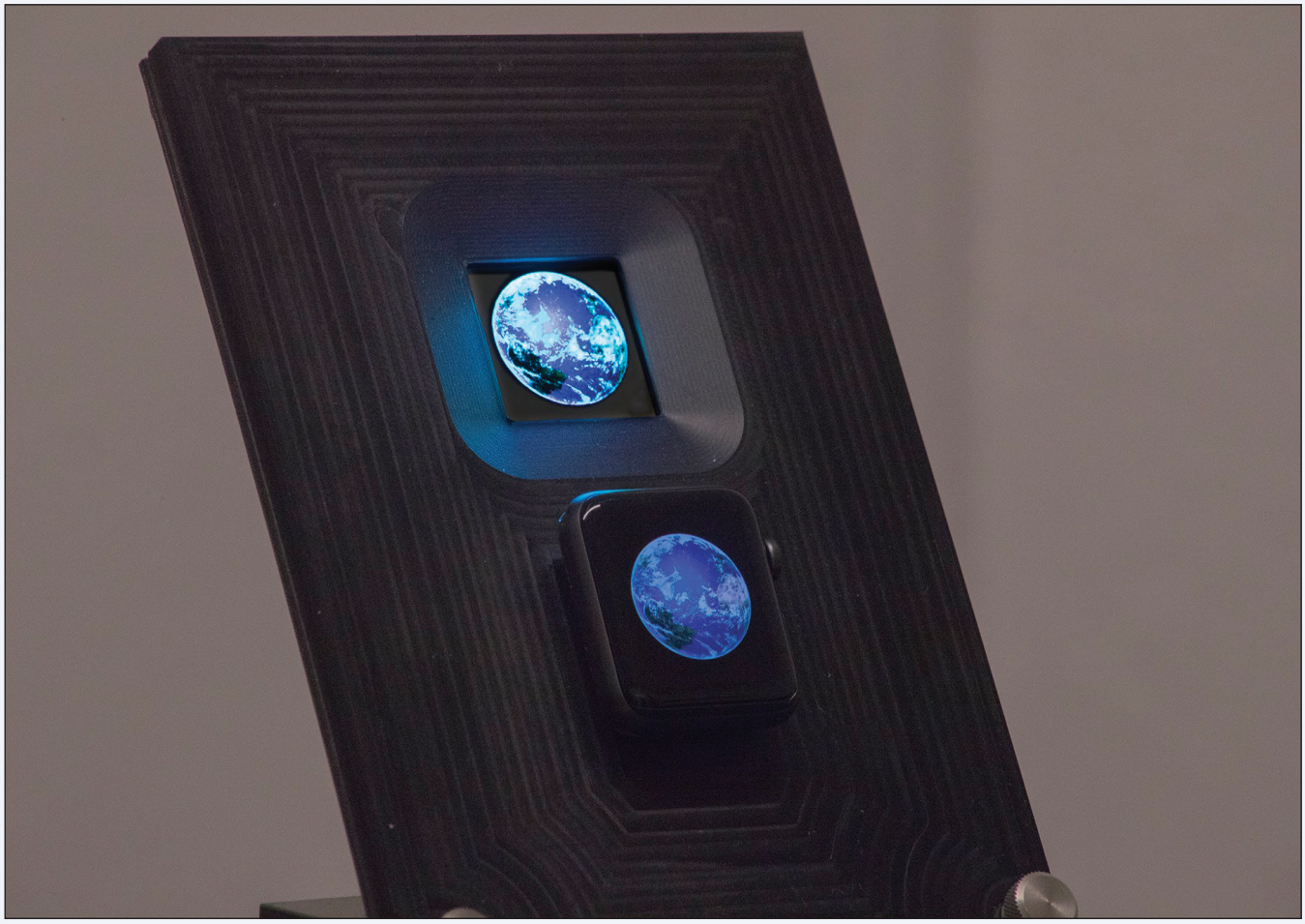
"Go into any LED shop and you will see that, in essence, they have the same tools as us; our focus has been to not customise anything that could create difficulties when scaling," she says.

"Factor in that we can also use the backplane that is available in the market at high volumes and then you can see that we have a very simple supply chain."

At the same time, Glo has used GaN to fabricate all of its microLEDs – red, green and blue – simplifying the display circuitry. And as Danesh asserts, device cost structures are good, relative to OLED displays.

"We don't use these complex OLED lines, giving us significantly better costs," says the chief executive.

"We have been able to leverage the existing economies of scale that are available to the display companies," she adds. "We really have opened a door for them to create new technologies that can compete with existing OLEDs while using their existing infrastructure, and this is also a huge opportunity for them."



Still, microLED displays have been notoriously difficult to manufacture using traditional pick-and-place transfer processes, in which each sub-pixel is placed onto a backplane one at a time. To counter this, many companies have been developing mass transfer processes, including Glo. The company's scaleable, direct-wafer-transfer process allows it to manufacture 0.1-inch to 75-inch displays with resolutions up to 3000 ppi on both LTPS and CMOS backplanes.

Indeed, as well as its 1.5 inch wearable display, Glo has also showcased a 0.7 inch 1000 ppi red, green and blue display for artificial reality and head-up displays on a CMOS backplane. And the company has produced displays, more than 8-inch in the diagonal, with up to 200 ppi for tablets, laptops, wall displays and more.

"One of the differences with our 'mass transfer' process, compared to other processes out there, is that we use a completely selective direct wafer transfer," says Nazre. "So you can transfer the microLEDs from the wafers onto the backplane without using any intermediaries, and you can do this selectively."

"This is unique and we have been doing it successfully for two years and counting on both silicon and glass substrates," he adds.

Glo, alongside the likes of Sony and Samsung, will construct its larger displays from 'tiles' of microLEDs. But according to Danesh, thanks to the high precision of the company's mass transfer process, the so-called stitch lines between tiles that plague this modular approach aren't visible to the naked eye. "One of the challenges of tiling is these stitch lines which you just don't want to see," she says. "With Samsung's tiles, you can see these lines if you stand close enough, but using our process, the stitch lines are not even visible under 50X magnification."

So with the microLEDs and the mass transfer process in place, where next for Glo? Success would seem to be the way forward.

Given the much anticipated demand in the smart watch market, as well as head-up displays, industry analyst, Boris Kobrin from n-tech Research, recently predicted that the global microLED market will swell from $2.7 billion in revenue in 2019, to a hefty $10.7 billion in 2022. And while competition from the likes of Apple with Luxvue, Aledia, Sony, Samsung Electronics and many more is rising, Glo's leaders are not fazed.

As Danesh and Nazre point out, Glo has both the InGaN microLEDs and mass transfer process in place, unlike many rival companies, and is set to produce bright, stable displays that can scale in size and production volumes.

"Like everyone else, we think we're smarter than the rest," says Danesh. "But we've met the [key] technical challenges that allow us to make displays at a much larger scale than anyone else that we know."

Wolfspeed:

From strength to strength

Since joining Cree, chief executive, Gregg Lowe has bolstered its power and RF business beyond belief. Where next for Wolfspeed, asks Rebecca Pool?

When Gregg Lowe joined Cree as chief executive in September 2017, he decided to make more of Wolfspeed.

At the time, the power and RF subsidiary was still smarting from its failed sale to Infineon, while at $220 million, yearly revenues paled compared to the incomes of $700 million and $550 million from Lighting and LED businesses.

Fast forward to 2019, and Cree has reported stronger than expected financial results, driven by revenue growth from Wolfspeed. The company has also acquired Infineon's RF business and announced a $250 million SiC wafer supply agreement with STMicroelectronics.

As Lowe tells *Compound Semiconductor*: "Our entire Wolfspeed business was worth a little over $200 million in 2017 and here we are now, announcing a deal that's actually bigger than that."

"When I arrived at Cree, we re-evaluated strategy and looked for the company's key differentiators," he adds. "Thanks to its SiC and GaN capability, Wolfspeed nailed it. We set out to quadruple Wolfspeed revenues to $850 million by 2022, and we are well on the way to achieving this ambitious goal."

Lowe's confidence in Wolfspeed is linked to the huge

potential for silicon carbide growth in key markets. Demand for SiC inverters in photovoltaics is gaining traction while the use of SiC in, say megahertz switching, is set to prove instrumental to the rollout of 5G infrastructure.

But for the Cree chief executive, electric vehicles is where the real excitement lies. "In terms of growth, the electric vehicle market is exploding right now," he says.

Lowe reckons that since joining Cree, he has seen car manufacturers such as Volvo, BMW, GM and Toyota invest more than $170 billion in electric vehicles, with SiC destined for inverters, onboard chargers and charging stations.

"I feel that SiC has hit the perfect window here and in terms of power electronics adoption, the tipping point has really happened," he says.

Facing challenges

But high wafers costs and limited supply remain key hurdles to SiC adoption. Right now the cost of a SiC wafer is at least double that of a silicon wafer, a thorny issue that is only exacerbated by capacity constraints.

Still, industry players have been tackling problems head on. For example, Infineon recently bought Germany-based Siltectra, which has devised a technology to split SiC wafers and double the number of chips produced from one wafer. Meanwhile, SiC wafer supplier, II-VI has expanded capacity, and Dow has revealed similar intentions.

For its part, Cree has been scaling capacity accordingly. In February 2018, the company started to divert research and development, and capital expenditures from its Lighting and LED businesses to Wolfspeed, and capacity has more than doubled since this time.

What's more, long-term supply agreements with Infineon, an unnamed partner, and now STMicroelectronics, will also help. As Lowe says: "I am pretty bullish that we will double capacity again within the next two years, and one of the ways that we are doing this is through long-term supply agreements."

"These give us the capability to invest more capital in our business," he explains. "We've [secured] three agreements and have a number of others that we are working on that we'll hopefully announce soon."

Currently, industry players are also transitioning from 4-inch to 6-inch SiC wafer manufacturing, with an eventual shift to 8-inch manufacturing necessary to optimise output and yields. In the past, such a transition has caused short-term shortages, but according to Lowe, his company's shift from 4-inch to 6-inch wafers has been 'fantastic' with every issue tackled without any major set-backs.

"When you are doubling capacity there is much that can go wrong, but the wafer quality on our 150 mm wafers is excellent and that's from customer feedback," he says. "Our doubling in capacity has also given us more feedback on the quality of crystal growth, which we are using to improve the entire fleet and raise yields."

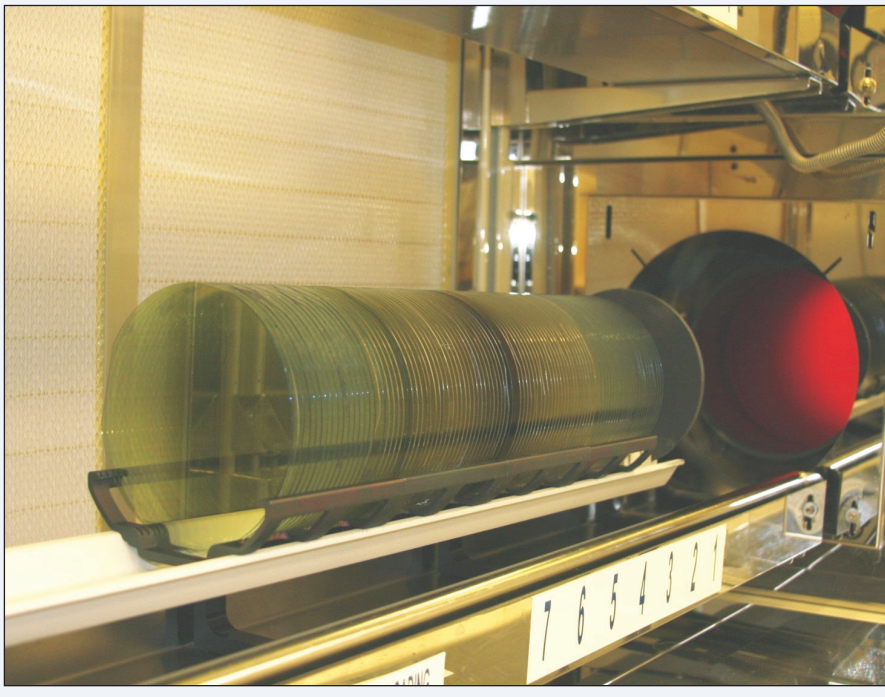
"Our increase in capacity also gives us a better cost base as we have more scale," he adds. "We have chosen to drive costs and yields very hard to decrease the price differential between silicon and SiC, in order to increase market adoption, and we will continue to do this over the coming years," he adds.

So where next for Wolfspeed? Without a doubt, the competition for SiC market share is increasing with other key players, including Infineon, STMicro, Rohm and ON Semi, all striving to fulfil growing market demands.

Still, as Lowe highlights, Cree grows crystals, produces wafers and performs epitaxy, giving it a 'unique advantage' in the market.

"We are fostering the adoption of SiC in the marketplace by providing materials to ST and Infineon, the folks that we effectively compete against in chip and power MOSFET markets," he says. "But this market could be worth many billions of dollars, so there is plenty of room for a number of semiconductor businesses converting from silicon to silicon carbide."

"This is the first time I've been at the heart of such a dramatic industry transition and it's so exciting to be a part of this," he adds. "We're converting an entire industry; how cool is that?"



Wolfspeed has doubled its silicon carbide production capacity by moving from 100 mm wafers to 150 mm wafers

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  Increasing the blocking voltage of GaN HEMTs – **KEYNOTE**
- **Richard Eden – IHS Markit**
  Is the infrastructure in place to ramp SiC and GaN production? - **ANALYST**
- **Ralf Lerner – X Fab**
  Printing GaN HEMTs onto silicon CMOS
- **Cem Basceri – Qromis**
  200mm GaN Power: Technology and Commercialization Status on QST Platform
- **Mohammed Alomari – IMS Chips**
  Enabling GaN/Si in an Industry 4.0 environment
- **Torsten Stoll – Nanometrics**
  Process control solutions for maximum yield in HVM for SiC and GaN power devices
- **Thomas Uhrmann – EV Group**
  Direct wafer bonding for GaN devices
- **Ke Xu – Suzhou Nanowin Science & Technology**
  Bulk GaN substrate growth by HVPE technology for GaN-on-GaN devices
- **Rob Rhoades – Revasum**
  Presentation Title TBC
- **Julie Orlando – Nanotronics**
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Can the MicroLED make an impact? And what are the emerging markets for visible lasers

SPEAKERS

- **Masahiro Murayama – Sony – [KEYNOTE]**
  Watt-class blue and green lasers
- **Pars Mukish - Yole Développement – [ANALYST]**
  3D Imaging/Sensing: The next killer application for laser diodes?
- **Hiromi Fujita - Asahi Kasei**
  Antimonide LEDs for gas sensing
- **Mark McKee - Veeco**
  Accelerating Photonics growth through advances in High Performance As/P MOCVD and Wet Processing technology
- **Liyang Zhang - Enkris Semiconductor**
  Mastering the manufacture of microLEDs on silicon
- **Norbert Lichtenstein - II-VI Incorporated**
  The tremendous opportunities for the VCSEL
- **Babu Dayal Padullaparthi - Sanan IC**
  Semiconductor lasers and detectors for DCI, 5G Front-haul, 3D Sensing & beyond
- **Joe Wu - Sino Nitride Semiconductor**
  The fabrication of high quality low cost free-standing GaN substrates and GaN templates

SPEEDING COMMUNICATION

Are faster lasers going to lead us into a new era of communication? Or will it be the build out of 5G?

SPEAKERS

- **Roger Hall – Qorvo [KEYNOTE]**
  Pushing Performance in RF for 5G Networks
- **Eric Higham – Strategy Analytics [ANALYST]**
  More data: More wireless or more fibre
- **Valery Tolstikhin – Intengent**
  Fabless PICs in InP: Why, What, and How?
- **David Danzilio - WIN Semiconductors**
  GaN-on-SiC Technologies for 5G Radio Access
- **Edward Wasige - EU Project-IBROW Project**
  Mm-wave/THz Multi-Gigabit Wireless Links – the iBROW Project
- **Gong Xiao - National University of Singapore/MIT Alliance**
  Targeting mm-wave communications with wafer-level integration of InGaAs HEMTs and silicon CMOS
- **Mikko Soderlund – Beneq**
  ALD for Compound Semi Power and RF industrial applications

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SPEAKERS

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  III/V Nano-ridge Engineering for novel Device Integration on Si **[KEYNOTE]**
- **Remy Comyn – Knowmade**
  Innovators in Power SiC - **[ANALYST]**
- **Gabriele Formicone – Integra**
  Increasing the Power of Solid-State RF Amplifiers
- **Marco Malinverni – Exalos**
  Superior superluminescent LEDs
- **Markus Behet – EpiGaN**
  GaN on Si – A Key enabling technology for 5G
- **Andy Sellars – Compound Semiconductor Applications CATAPULT**
  Accelerating the commercial application of compound semiconductors
- **Gerald Klug – DISCO HI-TEC EUROPE**
  Laser-lift-off (LLO) and CONDOx for wafer ultra-thinning process f or 3D stacked devices, TSV, eWLB and WLCSP wafers
- **David Lishan – Plasma-Therm**
  Extending performance in advanced packaging with low temperature, low damage plasma technologies
- **Jens Voigt – AIXTRON**
  Enabling Global Mega Trends with Compound Semiconductors
- **John Ghekiere – ClassOne**
  Advancing Performance of Compound Semiconductor Devices Through Advanced Plating Processes
- **Mukundkrishna Raghunathan – KLA Corporation**
  Presentation Title TBC

TARGETING TRANSPORTATION

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Can the strengths of SiC drive its adoption in electric vehicles? And what are the opportunities for III-V optoelectronics in the cars of today and tomorrow?

SPEAKERS

- **Aly Mashaly - Rohm Semiconductor [KEYNOTE]**
  Giving Formula E racing cars an edge
- **Hong Lin – Yole Développement [ANALYST]**
  SiC and GaN adoption by EV/HEV market

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Drawing the heat with diamond

Sucking the heat out of a GaN transistor with diamond film is to become ever more common, thanks to a strengthening supply chain for this technology

RICHARD STEVENSON REPORTS

DIAMOND has many fine attributes. It is renowned for its brilliance, which makes it a very fine choice for making jewellery; and it is blessed with great hardness, allowing it to be used in tools for cutting, drilling and sawing, and on the tip of cantilevers, to trace the modulations in vinyl records.

Lesser known, but equally exceptional, is diamond's thermal conductivity. Thanks to strong covalent bonds and low phonon scattering, its conductivity is around 2000 W m^{-1} K^{-1}, a value five times that of copper.

This incredibly high conductivity has piqued the interest of the electronic community, which has been investigating diamond's capability for extracting the heat out of a GaN HEMT. Efforts in this direction can be traced back to 2003, with the first successful attempt to produce a GaN-on-diamond structure. Milestones since then include the first GaN-on-diamond transistor in 2006, and DARPA's Near Junction Thermal Transport (NJTT) programme, kicked off in 2011, that has aided the development of this technology.

Recently, further strides have been made that put in place the groundwork to support the commercialisation of GaN-on-diamond technology. Several companies are now playing a significant role in this fledgling industry, with many in attendance at Diamond D-day, a one day conference held in Bristol, UK, towards the end of January. Those at this gathering, organised by Martin Kuball from the University of Bristol, included suppliers of tools for depositing diamond, providers of GaN-on-diamond epiwafers and foundry services, and makers of devices.

Up in space

One of the pioneers of the GaN-on-diamond HEMT is Akash Systems. This outfit, based in San Francisco, CA, devotes its efforts to developing small satellites, satellite transmitters, and the RF power amplifiers that serve them.

Speaking on behalf of Akash, the company's vice president of materials, Daniel Francis, began his talk by claiming that diamond is a satellite's best friend. He argued that the addition of a diamond foundation produces a three-fold hike in power density, and a considerable reduction in operating temperature. He cited work by the Air Force Research Laboratory, showing that the addition of a diamond layer reduced the channel temperature by between 40 percent and 50 percent, compared with GaN-on-silicon and GaN-on-SiC devices.

That reduction is a big deal. Note that the rays of the sun can propel satellite temperatures to as high 180 °C – and radiation is the only option for dissipating heat, so it is crucial to get as much of it as possible out of the device.

Akash is producing its GaN-on-diamond devices from 4-inch wafers. "If it's not full wafer, it's not production," said Francis.

He outlined three potential options for forming GaN-on-diamond structures. One is to grow GaN layers directly on diamond, but this requires the use of intermediate layers, and is ruled out by the relatively small the size of the diamond substrate. Another option is bonding, but a 'glue' is needed to bond the GaN and the diamond. Amorphous SiN is a popular choice,

but it has a thermal conductivity of just 1 W m^{-1} K^{-1}, compromising the benefits of the diamond layer.

The third way, pursued by Akash, is to grow diamond on GaN-based epistructures. Engineers at the west-coast firm start with GaN-on-silicon epiwafers with a SiN transition layer – it is less than 35 nm-thick, has a conductivity of around 10 W m^{-1} K^{-1}, and provides a good dielectric interface. Fabrication of devices involves separating the epilayers from the silicon substrate.

Efforts associated with improving production have led to a greater consistency associated with removal of the AlGaN buffer, better control of the thickness of the adhesion layer – it is now controlled to within 5 nm – and a reduction in wafer bow to less than 20 μm.

Engineers target a thickness for the diamond layer of 125 μm. To ensure that they realise this, they deposit more material, and then apply a polishing step to thin the diamond to the required thickness.

Francis revealed that when the growth of diamond begins, it can create nanocrystals, which have a low thermal conductivity. But as growth continues, grains get larger, increasing thermal conductivity.

Capacitance-voltage measurements on the processed wafers reveal a "low, flat capacitance". This is attributed to low interface charging. Plots are much closer to those for GaN-on-SiC, than for GaN-on-silicon.

Results on recent multi-finger devices reveal a power-added efficiency of around 60 percent. According to Francis, this figure is comparable to that of standard devices operating at 10 GHz.

GaN-on-diamond epiwafers

If developers of GaN-on-diamond devices prefer to start their fabrication work with epiwafers of this

The Diamond D-day conference, held at the Bristol Mari ot Hotel, attracted 120 delegates. About half of those that attended came from overseas.

material, they have the option of buying 4-inch material from RFHIC.

At Diamond D-Day, RFHIC's Director and General Manager, US, Won Sang Lee, began his presentation by claiming that the market for epiwafers of GaN-on-SiC HEMTs is "strong". But he believes that GaN-on-diamond will be "the next step".

RFHIC wants to be the pioneer of the GaN-on-diamond semiconductor industry. It is well-placed, having 63 patents associated with this technology, and exclusive intellectual property that is said to cover everything except the commercial satellite sector. The company has identified several potential markets for GaN-on-diamond, including self-driving cars, military radar, and industrial, medical and scientific sectors.

Lee compared what he considers to be the three main technologies for RF, high-power devices: silicon LDMOS, GaN-on-SiC, and GaN-on-diamond. He argued that the it is only the latter that is capable of providing operating frequencies up to 100 GHz, making it the leading candidate for the future.

He predicts that the success of GaN-on-diamond will begin with deployment in 5G base stations. The merits of this material combination are not limited to a substantial power density, but also include: greater linearity, stemming from superior carrier transport; and better reliability, due to the lower operating temperature of the chip.

RHFIC, which started developing its GaN-on-diamond technology back in 2015, is now capable of producing GaN-on-diamond material in substantial volumes in Korea, and in smaller quantities at its R&D facility in the US. The plan is to start shipping engineering samples to its customers in the second quarter of this year.

Goals for the future include increasing the production quantity of GaN-on-diamond to 100 epiwafers per month, optimising device layers to improve performance, and increasing yield – currently it's just 40 percent.

Device foundry

One company with the capability to process RHFIC's GaN-on-diamond epiwafers into devices is compound semiconductor foundry service provider GCS. In Bristol Daniel Hou, a spokesman for the company, detailed some of the challenges and the rewards of this approach.

A downside is that in an automated fab, some tools may be unable to handle these epiwafers. This can be caused by tensile strain in the material, leading to a wafer bow of up to a few millimetres. Such a distortion

can wreak havoc with printing processes for i-line steppers. The solution, explained Hou, is to choose a carrier with the right coefficient of thermal expansion. Using a combination of a perforated SiC carrier, dry and wet etching steps, thermal release tape bonding and high-temperature polymer bonding, bow can be slashed to just 20 μm.

Hou revealed that another issue is that the implant isolation step can lead to a "huge" leakage current. It rockets by six orders of magnitude.

The engineers at GCS address this hike with an additional step for treating the surface. This results in DC characteristics that are similar to those for GaN-on-silicon: maximum current is 1 A/mm, peak transconductance is 250 mS/mm, breakdown voltage exceeds 100 V, and the on-off ratio is in excess of 10^6.

RF measurement on these devices are encouraging. Applying a 10 percent duty cycle to 0.65 μm HEMT, and cranking up the voltage from 50 V to 100 V, produces an increase in the power density at 2 GHz from 15.5 W/mm to 22.5 W/mm.

Efforts at GCS have also been directed at developing a through-substrate via process. This involves: laser drilling from the frontside; plating with gold to partially fill the via; sputtering a seed metal; and then gold plating, both on the front side and the back side.

Multi-finger devices made with this process are capable of producing an output of 11.2 W, and 15-19 dB of gain. Hou describes these results as "respectable", and says they provide proof that the via process is "working".

An all-diamond device

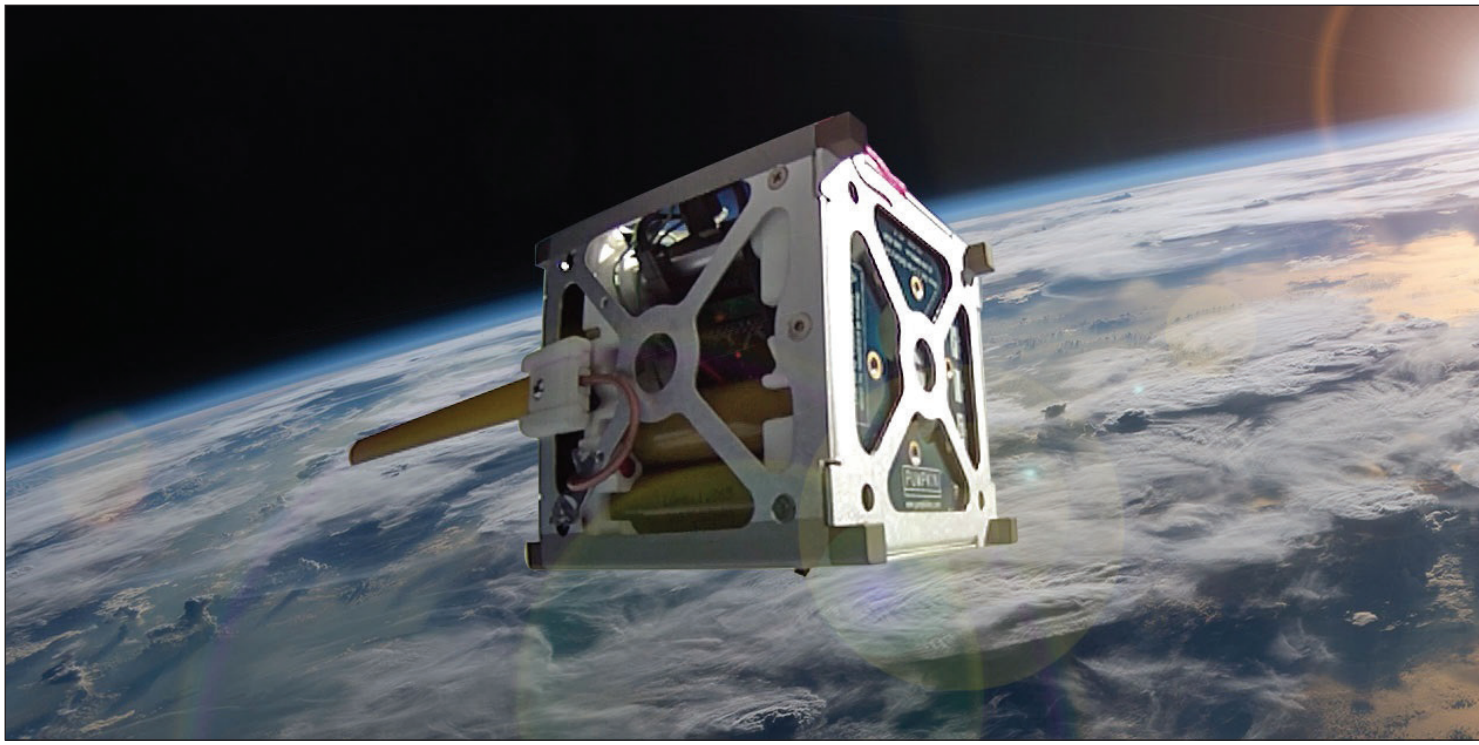
With a bandgap of 5.45 eV – that is even higher than that of gallium oxide – diamond can also be viewed as a promising material for making high-power devices.

Some of the results obtained with diamond devices were briefly discussed in a talk given by Andrew Barnes from the European Space Agency. He mentioned transistors with a maximum oscillation frequency of 20 GHz, and a cut-off frequency of about 7.7 GHz. This enabled up to 22 dB of gain, a result Barnes described as "quite encouraging".

However, he warned the audience that diamond has its drawbacks, including being very expensive, and very difficult to dope.

An even stronger case for steering clear of diamond devices came from Oliver Williams from Cardiff University, who said: "I did my PhD on diamond devices and it didn't go well." In his view, *n*-type doping doesn't work, and the diameter of the native substrate is stuck at half an inch, despite promises dating back two decades that 1-inch material is just around the corner.

So, based on the presentations at Diamond D-day, it is best to restrict diamond's role within the compound semiconductor industry to extracting the heat out of the GaN HEMT. Used for this, it can do a great job. And with a strengthening supply chain taking place, there is a good chance that GaN-on-diamond devices will start to see widespread in space, along with increasing deployment in applications far nearer to home.

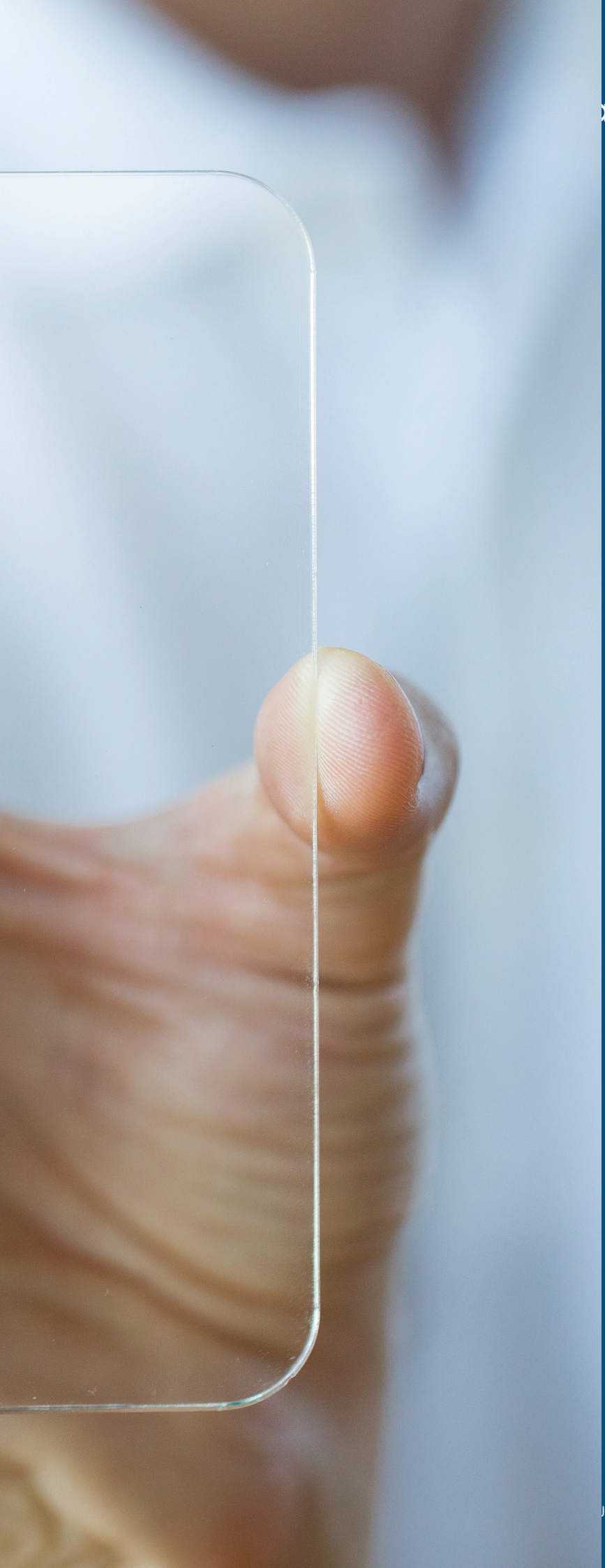


As the small satellite space race takes off, Akash Systems is set to send GaN-on-diamond systems into orbit.

Invisible contacts

Transparent GaN circuits are on the horizon, thanks to transfer processes for shifting the transistors onto glass, and the creation of see-through contacts, based on indium tin oxide and ion implantation

BY ZHIHONG LIU FROM SINGAPORE-MIT ALLIANCE FOR RESEARCH AND TECHNOLOGY, GEOK ING NG FROM NANYANG TECHNOLOGICAL UNIVERSITY AND EUGENE FITZGERALD FROM MASSACHUSETTS INSTITUTE OF TECHNOLOGY



aN transparent transistors

EVER MORE EFFORT is being devoted to the development of invisible electronic circuitry and optoelectronic devices. This field, known as either transparent electronics or see-through electronics, promises to spawn many new products and businesses. To name but a few, it could lead to: smart wind shields in automobiles, smart building windows, transparent flat panel displays, and see-through solar cell panels.

A key component in many transparent electronic systems is this transistor. Today, this device is often in the form of a thin-film transistor, made from a transparent conductive oxide, such as In_2O_3, ZnO_2 or SnO_2.

Unfortunately, the performance of those thin-film transistors is vastly inferior to the more common visible transistors, such as the silicon MOSFET. Inferior intrinsic physical properties are to blame, including the polycrystalline structure, lower thermal conductivity, and lower electron mobility – in In_2O_3, ZnO_2 and SnO_2, the mobility is typically just 100 $cm^2 V^{-1} s^{-1}$, one quarter of the value of that of silicon. The low mobility hampers the current that is available to transparent transistors. They are held back by a low current, a low speed, and the need to be driven by a high voltage. What is needed are alternative materials for producing transparent, high-performance devices.

Candidates for replacing the conductive oxides include carbon nanotubes, graphene, and two-dimensional transition metal dichalcogenides. But they all have their own weaknesses, which are difficult to overcome in real applications. Carbon nanotubes are held back by agglomeration, dispersion, purification and sorting; graphene is compromised by fabrication issues for yielding high-quality material, and its intrinsic bandgap limit prevents the transistor channel from fully closing; and two-dimensional transition

Material	Bandgap (eV)	Mobility (cm^2/Vs)
In_2O_3	3.75	~100
ZnO_2	3.35	~100
SnO_2	3.6	15
GaN	3.42	>1500 (2DEG)

Table I. Comparison of carrier mobilities in transparent conductive oxides commonly used in GaN and in today's transparent transistors.

metal dichalcogenides are impaired by carrier mobilities that are typically even lower than those for transparent conductive oxides.

At the Singapore-MIT Alliance for Research and Technology, we are pioneering a promising alternative: GaN. From an optical perspective, the bandgap of GaN of 3.42 eV is similar to that of the other contenders (for In_2O_3, ZnO_2 and SnO_2, values are 3.75 eV, 3.35 eV and 3.6 eV, respectively), giving GaN an absorption wavelength of 362 nm that enables transparency over the whole visible range. And from an electrical performance perspective, GaN wins hands-down. Mobility is more than double that of silicon in the bulk, and four times that in the form of a two-dimensional electron gas. The saturation velocity is also far higher, as is the critical breakdown field and the thermal conductivity.

Hurdles to a transparent transistor

At the heart of a typical GaN transistor is a conducting channel, formed by creating a two-dimensional electron gas at the interface between an AlGaN barrier and the GaN buffer (see Figure 1). This device tends to be produced on a foreign substrate, typically silicon or SiC, and sport three electrodes: a source, a drain and a gate. To ensure transparency, transparent active materials – that is, GaN-based materials – have to be used alongside a transparent substrate and transparent electrodes.

It is not difficult to use a transparent substrate. While a lot of GaN devices are formed by growing nitride layers on an opaque substrate, for example, silicon, there are plenty of transparent options to choose from, including SiC, sapphire, AlN and native bulk GaN. However, all of them are pricey, while the most commonly used substrate for transparent circuits applications – glass – is very cheap.

Our solution is a two-step process that leads to the formation of GaN transistors on glass. Our first step is to deposit GaN materials on a cheap-but-visible silicon substrate, before we transfer the GaN layers onto the glass. Alternatively, we can directly sputter GaN materials on a glass substrate, using a technology developed recently by Hiroshi Fujioka's group at Tokyo University.

What about the electrodes? Normally, GaN transistors have the pairing of nickel and gold as the gate metal, and employ either a Schottky contact or a metal-oxide-semiconductor (MOS) structure. To ensure transparency, we can modify this design, moving from these opaque metals to a transparent conductive material, such as indium-tin-oxide, which is widely used in transparent electronics. This oxide is a good choice, as it can form a good Schottky contact to the AlGaN/GaN and work as a gate in a GaN transistor. Encouragingly, there are a few reports demonstrating an indium-tin-oxide (ITO) gate in a GaN transistor, and it has been shown that a MOS structure with ITO can also be employed as a transparent gate in a GaN device.

For the source and drain electrodes, we have to form an ohmic contact between the source and drain material and the channel material. The conventional choice are metals, such as the pairing of titanium and aluminium. Just replacing these opaque materials with ITO is not an option, as the oxide cannot form

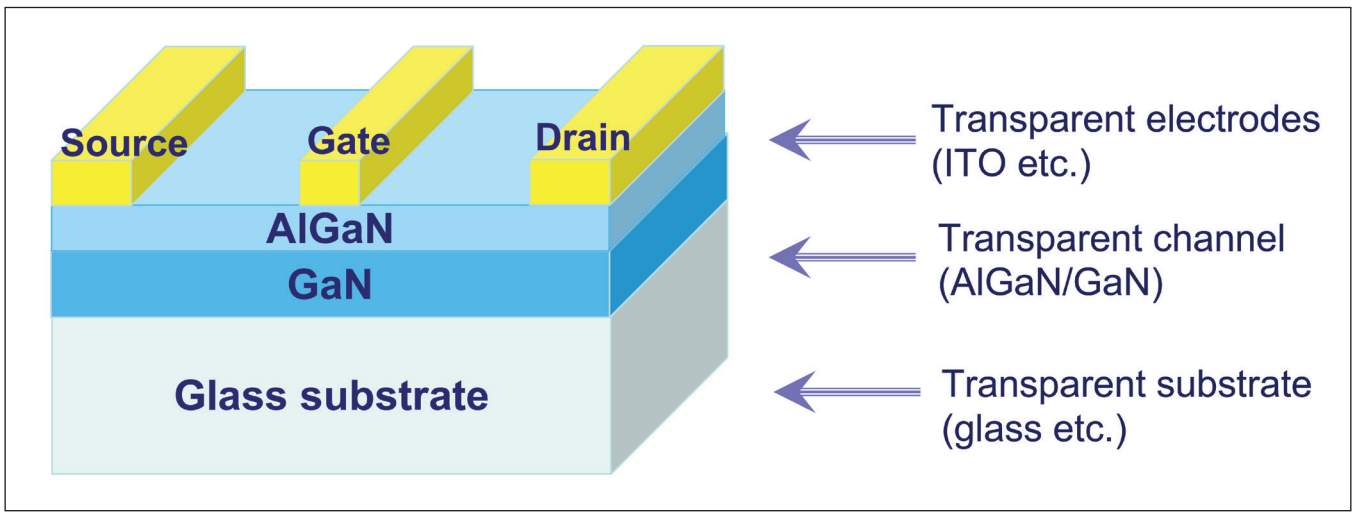


Figure 1. A typical GaN transistor must be modified to form a transparent device.

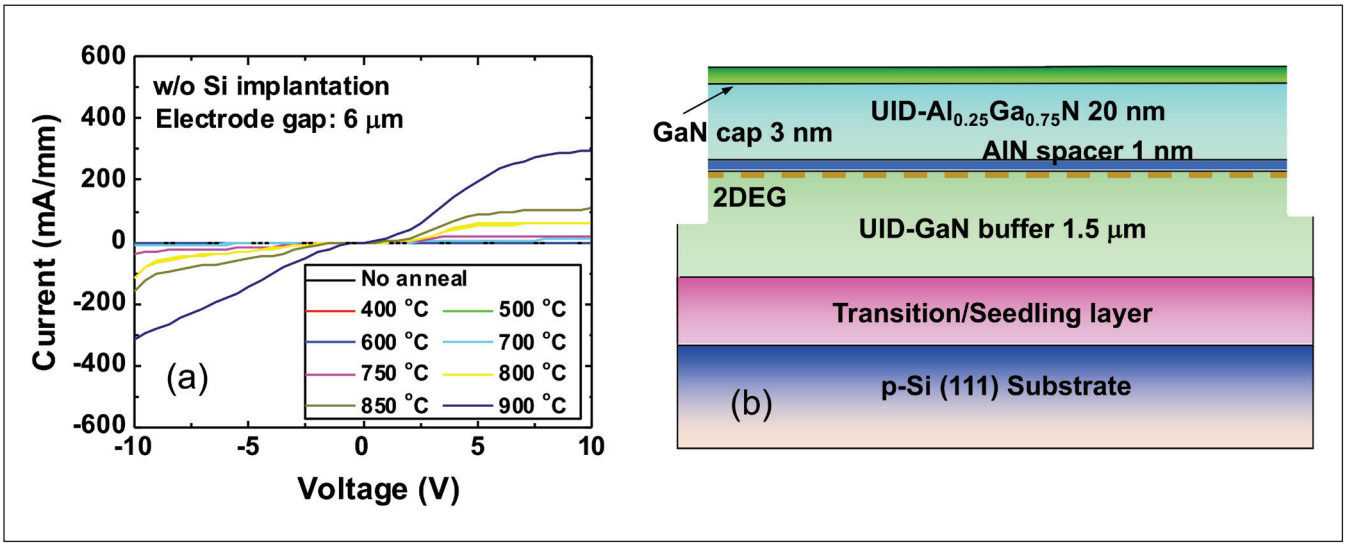


Figure 2. (a) A current-voltage (I-V) curve measured for a pattern with two electrodes made of ITO after different annealing temperatures. The plots show that when the annealing temperature is lower than 600 °C, the current is very small and can be neglected. Increasing the temperature to 700 °C causes current to appear, but ohmic contacts cannot form, even with an annealing temperature as high as 900 °C. The nitride materials in this transistor (b) were grown by the epiwafer supplier IQE, by loading a 200 mm *p*-type silicon wafer into an MOCVD chamber.

an ohmic contact with the two-dimensional electron gas (see Figure 2). Note that although upping the annealing temperature increases the current, even at 900 °C, it does not lead to an ohmic contact.

Transparent ohmic contacts…

Simulations of the energy bands reveal why ITO fails to form a good ohmic contact in a GaN transistor. They show that there is a high energy barrier between the ITO and the two-dimensional electron gas at the interface between AlGaN and GaN (see Figure 3(a)). This barrier prevents electrons from travelling smoothly between the ITO and the triangle well in the GaN – and thus prevents the formation of a good ohmic contact. To make one, an approach is needed that pulls down the conduction band of the AlGaN/GaN materials close to the ITO and minimizes the energy barrier (see Figure 3(b)).

One effective approach to pulling down the electron conduction band is to use ion implantation to dope AlGaN and GaN. We have a lot of experience with this, having optimized ion implantation technology to form highly-doped AlGaN/GaN regions and realize good CMOS-compatible ohmic contacts in GaN transistors. Our efforts include the development of an activation annealing method, using ammonia rather than the more common nitrogen to reduce the surface damage

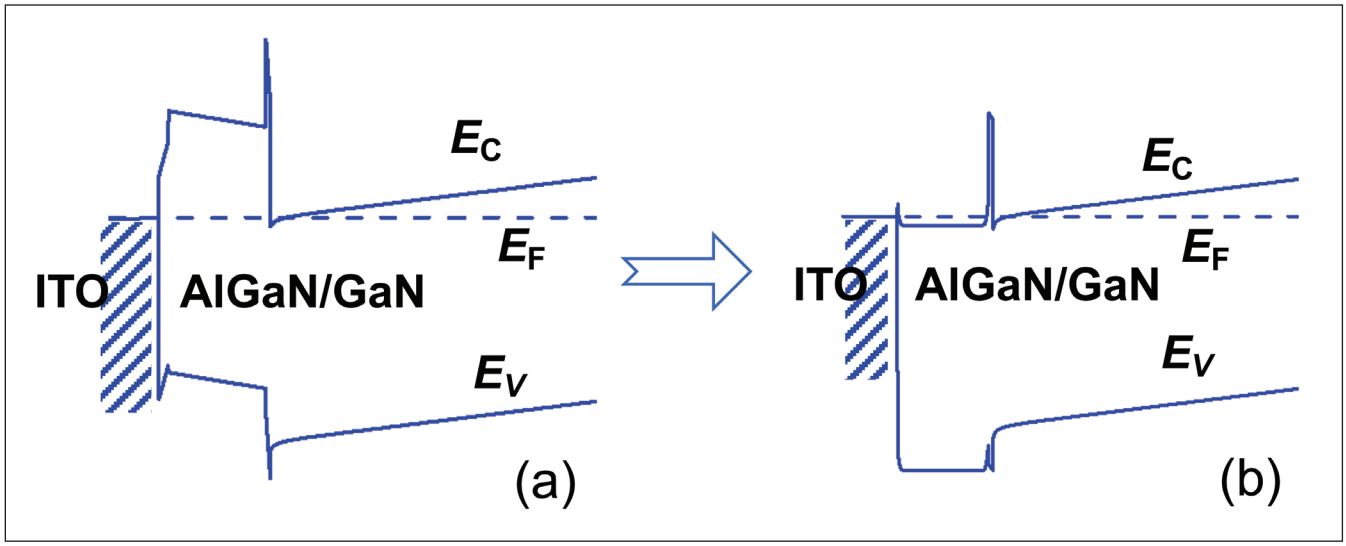


Figure 3. (a) For the energy band diagram for ITO and the AlGaN/GaN heterostructure, there is a high energy level between the ITO and the two-dimensional electron gas (2DEG) at the interface of AlGaN/GaN heterostructure. (b) To form a good ohmic contact, there is a need to pull down the conduction band of the AlGaN/GaN materials close to the ITO and minimize the energy barrier.

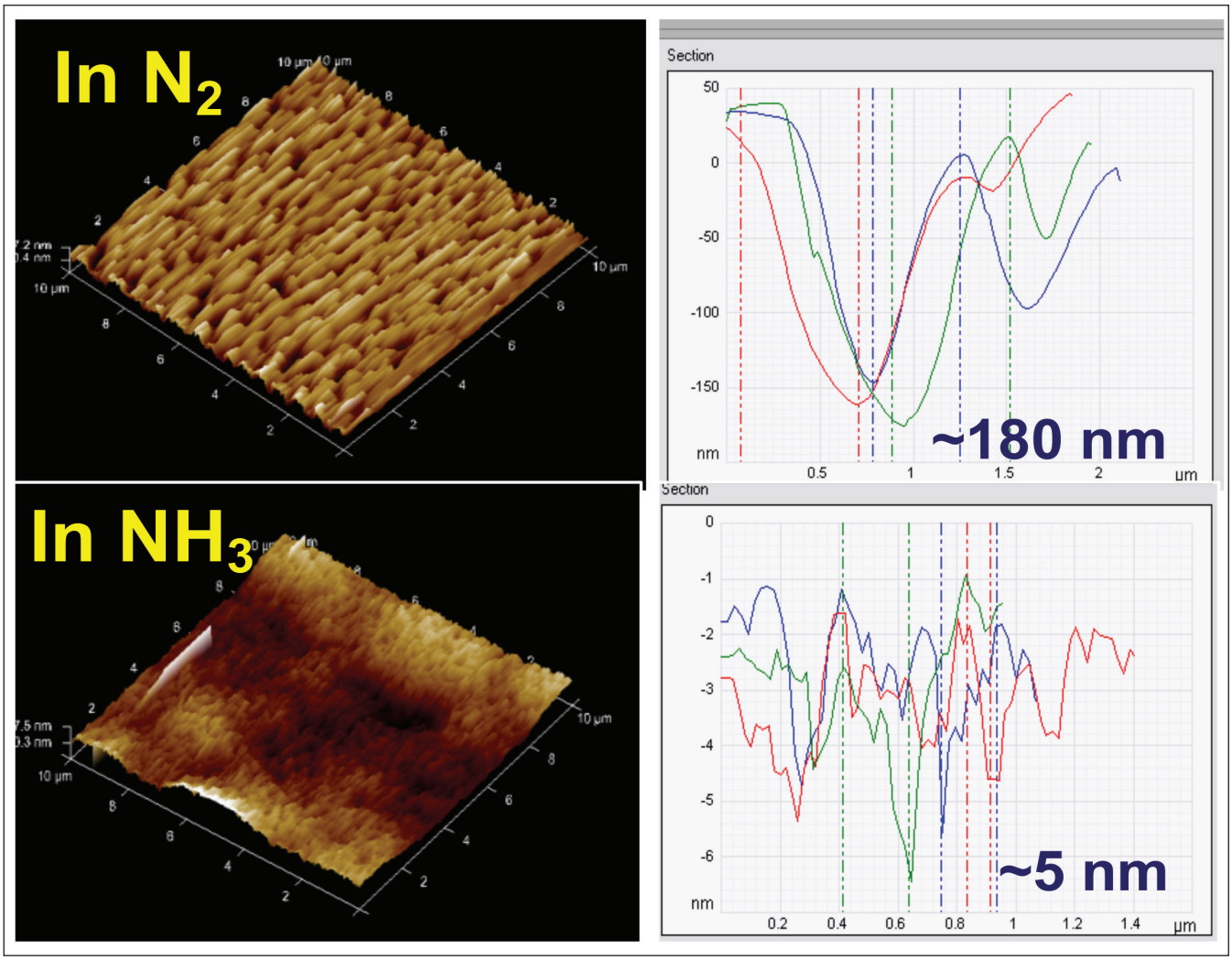


Figure 4. Activation annealing in ammonia can greatly suppress the surface damage caused by high temperature (1200 °C, 2 minutes)

Group	Substrate	R_{sh} (Ω/□)	R_C (Ω mm)
Mitsubishi	SiC	215	0.28
Mitsubishi	SiC	N.A.	0.16
UCSB	SiC	N.A.	0.2
Hosei Univ.	sapphire	140	0.045
Our work	sapphire	50	0.07
Our work	silicon	58	0.07

Table II. Excellent results in both sheet resistance (R_{sh}) of the implanted regions and ohmic contact (R_C) have been achieved using silicon ion implantation and CMOS-compatible (Ti/Al metals) ohmic contact technology developed at the Singapore-MIT Alliance for Research and Technology.

during high-temperature annealing of the GaN transistor surface (see Figure 4). By optimising the ion energy, dosage, activation annealing thermal budget and the post-metal annealing thermal budget, we have realised excellent results for the ohmic contact and the sheet resistance of the implanted regions (see Table II).

More recently, we have transferred these silicon ion implantation techniques to our transparent devices. The implantation conditions that we have adopted are a 30 keV energy, with a 2 x 10^{15} cm^{-2} dosage, plus a 80 keV energy with a 2 x 10^{15} cm^{-2} dosage, at 7° tilt, using a 300 nm layer of SiO_2 as a hard mask for protection. This is deposited by PECVD. We activate the silicon ions by heating to 1200 °C for 5 s in an ammonia atmosphere. The last step is the sputtering of an ITO film, followed by annealing in a nitrogen atmosphere.

This approach can form good ohmic contacts between the ITO and the silicon-implanted AlGaN/GaN heterostructure (see Figure 5). Note that good ohmic contacts are even formed when annealing at just 400 °C. Recall that this is in stark contrast to

the lack of any current in samples without silicon implantation that are annealed at temperatures below 600 °C (see Figure 6). So there is no doubt that silicon implantation is highly beneficial for the formation of ohmic contacts between ITO and GaN materials.

… and working transistors

To test our approach, we have applied our transparent source and drain ohmic contact technology to real GaN transistors, which use the design shown in Figure 1. In these devices, the two-dimensional electron gas Hall density and mobility are about 8 x 10^{12} cm^{-2} and 1500-1600 cm^2 $V^{-1}s^{-1}$, respectively. The ITO ohmic contact is formed with the assistance of silicon ion implantation, followed by annealing under nitrogen for 1 minute at 600 °C.

DC tests on our devices show excellent results, highlighting the potential that GaN has to be applied in tomorrow's future transparent electronic systems. Our transistors, which have a gate-to-source distance of 1.5 μm, a gate length of 2 μm, and a gate-to-drain distance of 9.5 μm, exhibit a maximum drain current of 602 mA/mm, a maximum transconductance of 121 mS/mm and a threshold voltage of typically -3.0 V. These values are similar to those found in devices with conventional metal electrodes, indicating that the ITO gate and fabrication process does not introduce obvious extra charges on the device surface. The Schottky barrier height between ITO and AlGaN/GaN is 0.7 eV, which is a little higher than 0.62 eV, a value reported elsewhere.

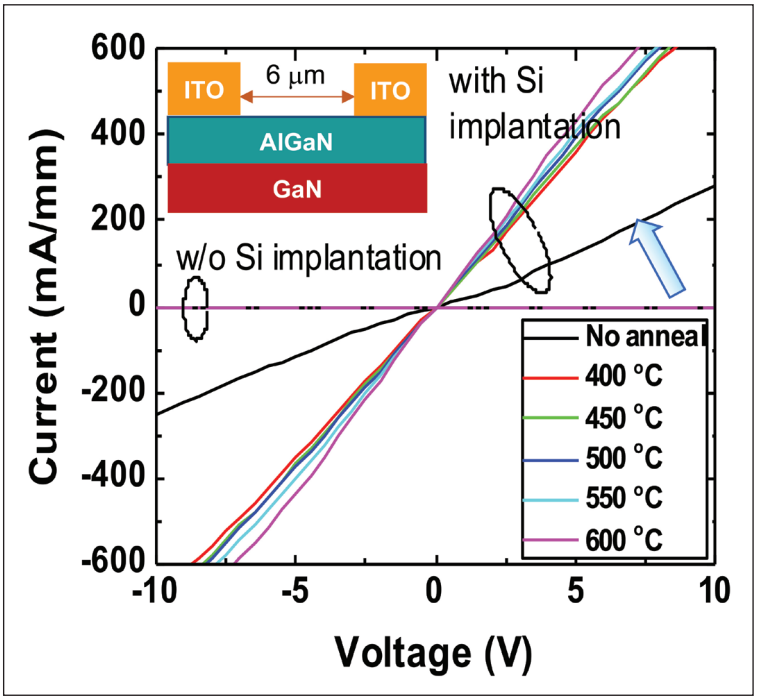


Figure 5. Good ohmic contacts were formed between ITO and the silicon implanted regions in the AlGaN/GaN heterostructure.

Our work underscores the potential of transparent GaN transistors. To spur their development, we will now try to further optimize the transparent ohmic contact and reduce the contact resistance. This should lead to fully transparent GaN transistors with excellent RF or power performance, and ultimately enable the production of GaN transparent circuits and systems.

Further reading

Z. Liu *et al*. Proc. of IWN, 2018
B. Lu *et al*. Electron. Dev. Lett. **31** 951 (2010)
T. Itoh *et al*. Sci. Reports **6** 29500 (2016)
Z. Liu *et al*. Proc. of IWN, 2016

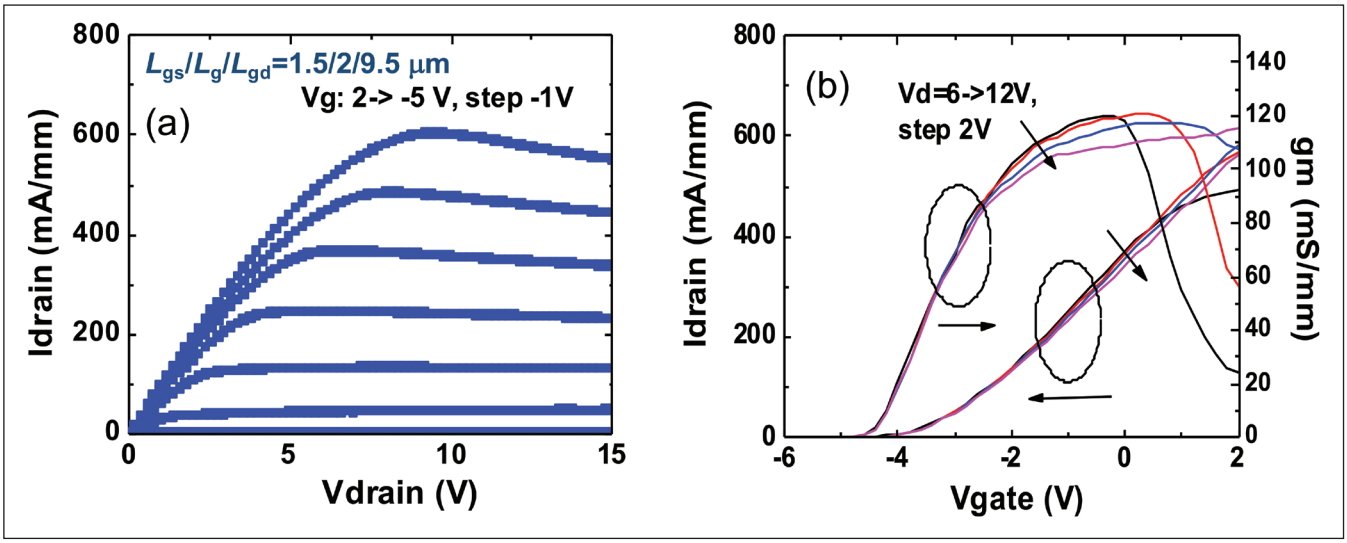


Figure 6. Measured DC performance including (a) output (b) characteristics of a GaN transistor with ITO source/drain (S/D) and gate electrodes.

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PICS TODAY – DATACOM, IMAGING AND TRANSPORT

Today's primary PIC applications in data centers and telecom are foundations for new opportunities. We will explore PICS for healthcare, diagnostics, imaging/ranging and vehicle automation as well as new approaches for data transport.

SPEAKERS

- **Katharine Schmidtke – Facebook – [KEYNOTE]**
  Achieving high quality 100G data center PIC Integration
- **Mehrdad Ziari - Infinera**
  Large scale PICs, integration with InP lasers and PICs across future networks and markets
- **Michael Liehr – AIM Photonics**
  AIM Photonics' role in developing next generations of PICs and TAP manufacturing expertise
- **Pauline Rigby - Lightcounting – [ANALYST]**
  New VCSEL opportunities in 3D sensing and beyond
- **Henk Bulthuis – Kaiam Corporation**
  The future and economics of PICs and PLCs in data center applications
- **Callum Littlejohns - CORNERSTONE**
  Device prototyping using the CORNERSTONE platform
- **Ignazio Piacentini – ficonTEC**
  PIC differentiation, emerging markets, and common modular platforms for assembly and test.
- **Rene Penning de Vries – PhotonDelta**
  Presentation Title TBC

PIC INNOVATION – EPDA, TAP & PICS BEYOND DATACOM

Electro-photonic design automation (EPDA) paired with automated test, assembly and packaging (TAP) are essential for ensuring rapid PIC development cycles and quality control. We will explore how tools and processes will enable greater yield, reliability and sector growth.

SPEAKERS

- **Tom Daspit, Mentor ... A Siemens Business**
  Photonics and EDA – Round Hole and Square Pegs
- **Albert Hasper, PHIX**
  Large scale assembly and packaging foundry for PICs
- **Scott Jordan, Physik Instrumente**
  The Emergence of Non-Position Positioning in Fast Manufacturing Automation
- **Martijn Heck - ePIXfab/Aarhus University**
  Presentation Title TBC
- **Ronald Broeke – BRIGHT Photonics**
  Rethinking the photonics IC design flow to make high-quality PIC design easier, cheaper and faster
- **David Cheskis - IQE**
  VCSELs in 3D facial recognition
- **Remco Stoffer – Synopsys**
  How Synopsys Is Driving the PIC Revolution with a Trusted and Scalable Design Flow?
- **André Richter - VPIphotonics**
  Hybrid PICs - Technology Alternatives and Design Implications
- **James Pond - Lumerical**
  Scalable PIC design: increasing yield of components, circuits and systems
- **Luc Augustin – SMART Photonics**
  Open access integration platform: versatile solution for photonic integrated circuits
- **Peter O'Brien – Tyndall National Institute**
  Presentation Title TBC
- **Pieter Dumon – Luceda Photonics**
  Presentation Title TBC

PICS REIMAGINED – HYBRIDS AND MATERIALS INNOVATION

PIC innovation is already linked to hybrids – InP lasers are driven by silicon chips and die-level devices are combined into modules. While silicon photonic (SiP) optimization continues we will concurrently explore the benefits of bringing compound semiconductor technologies such as GaAs, GaN, lithium niobate, and silicon carbide into PIC development programs.

SPEAKERS

- **Jochen Zimmer – Nanoscribe**
  Additive manufacturing by two-photon-polymerization for photonic integration
- **Arne Leinse – LioniX International**
  Vertical Integration in Silicon Nitride (siN) based foundry enables new applications
- **Michael Geiselmann – LIGENTEC**
  New advances in Silicon Nitride (siN) PIC Applications
- **Arnaud Rigny – Teem Photonics**
  Optical passive device platform to enhance photonics performances
- **Di Liang – Hewlett Packard Enterprise**
  Presentation Title TBC
- **Michael Lebby – Lightwave Logic**
  Polymer PIC opportunities in Applications Beyond 100G
- **Kei May Lau – Hong Kong University of Science & Technology**
  III-V lasers directly grown on Silicon

Other speaker presentation themes to be confirmed include:

- **Multiphoton Optics**
  TBC

HOW DOES THE PIC INDUSTRY DELIVER ON THE PROMISES OF SIZE, SPEED, AND ECONOMY WITH HIGH QUALITY?

Today's PIC-based transceivers or PIC transceiver components are often assembled, packaged and tested manually. Is it possible to drive demand while the infrastructure needed to support it is still being conceived, designed and built?

SPEAKERS

- **Robert Blum, Intel – [Moderator]**
- **Katharine Schmidtke, Facebook – [Panelist]**
- **Mehrdad Ziari, Infinera – [Panelist]**

Additional panelists to be confirmed

WILL PICS BE THE ENGINE OF GROWTH OVER THE NEXT DECADE? IS THE GROWTH SUPPORTED IN OUR ROADMAPS WORLD-WIDE?

Can PICs support advanced datacom and long-distance telecom applications as reflected in our global technology roadmaps?

SPEAKERS

- **Michael Lebby, Lightwave Logic – [Moderator]**
- **Michael Liehr, AIM Photonics – [Panelist]**
- **Werner Steinhögl, European Commission Photonics Unit – [Panelist]**
- **Takahiro Nakamura, PETRA – [Panelist]**

PIC ROI – SHOW ME THE MONEY

While manufacturers are working to automate PIC assembly, packaging and test, we will examine how existing and future sector investments will reap dividends. What cycles should investors anticipate? How can financiers accurately gauge product potential within emerging PIC sectors?

SPEAKERS

- **Dirk van den Borne – Juniper Networks**
  Coherent DWDM router interfaces: Opportunities for photonic integration
- **Eric Higham – Strategy Analytics – [ANALYST]**
  Assessing the long-term growth and market potential for PIC devices in datacom, transport and networks

PICS BEYOND 100G – EVOLUTION AND REVOLUTION

PICs are poised to transform many end use markets as global semiconductor innovation shifts resources from electrons to photons. We'll explore near-term opportunities and potentially disruptive, long-range advantages that PICs can offer today's service providers and end users with a focus on healthcare, autonomous driving, defense and security; artificial intelligence, AR/VR and the IoT.

SPEAKERS

- **Martin Zirngibl – Finisar**
  The role of PICs in Tb/s datacenter environments: Is pluggability dead?
- **Twan Korthorst – Synopsys**
  Driving the PIC Revolution – Case Scenarios
- **Jose Pozo – EPIC**
  The benefits of low-barrier access to new production services for PICs today and tomorrow
- **Martin Guy – Ciena**
  Photonic Integration Opportunities for Next-Generation Coherent High-Capacity Systems
- **John Magan – European Commission Photonics Unit**
  The critical role that EC support for photonics and PIC devices plays in our manufacturing future.
- **Nick Psaila – Optoscribe**
  3D laser written glass components for advanced photonic integration
- **Thomas Liljeberg – Intel**
  Integrated Silicon Photonics for future Datacenter Applications

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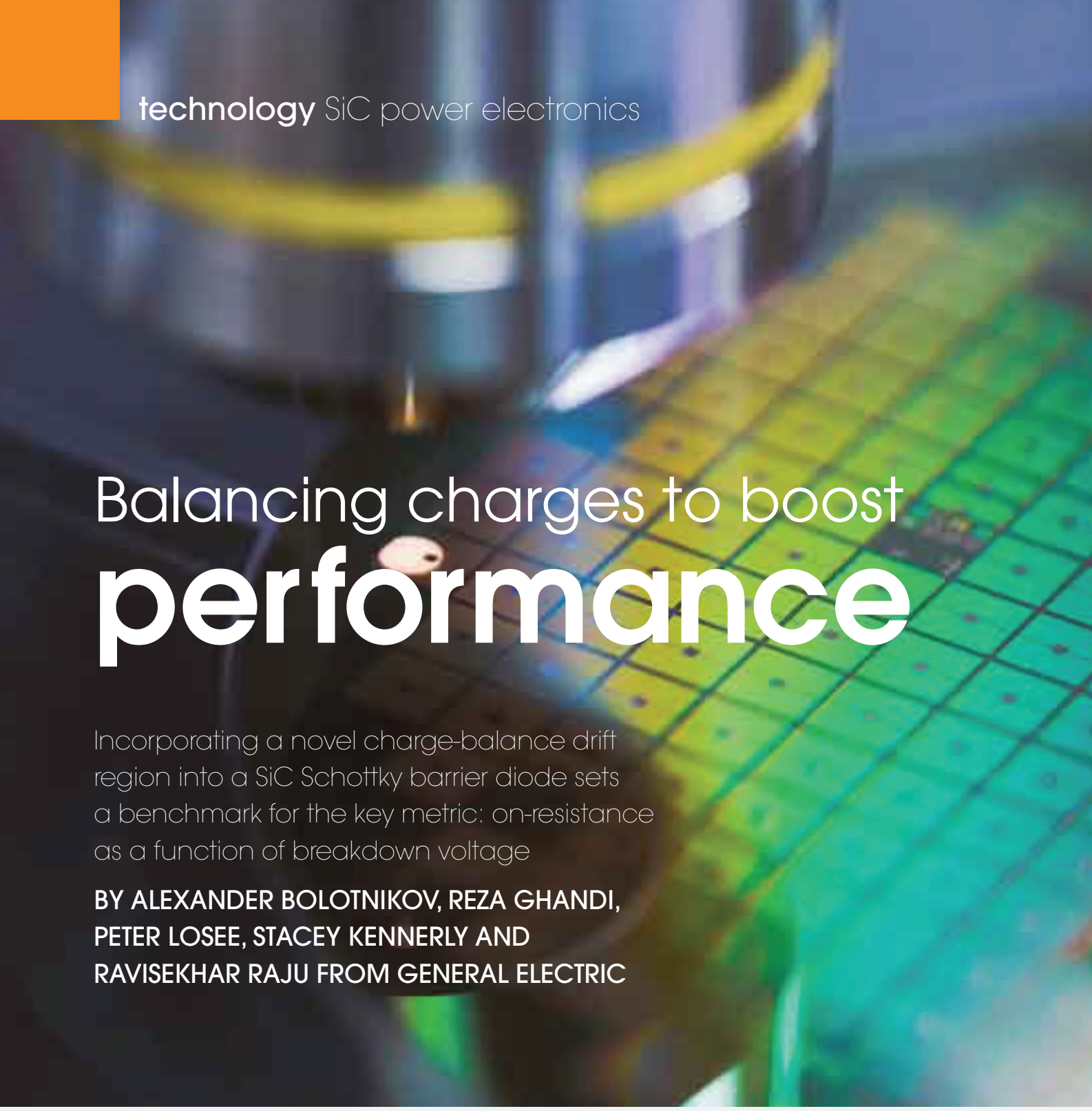


Balancing charges to boost performance

Incorporating a novel charge-balance drift region into a SiC Schottky barrier diode sets a benchmark for the key metric: on-resistance as a function of breakdown voltage

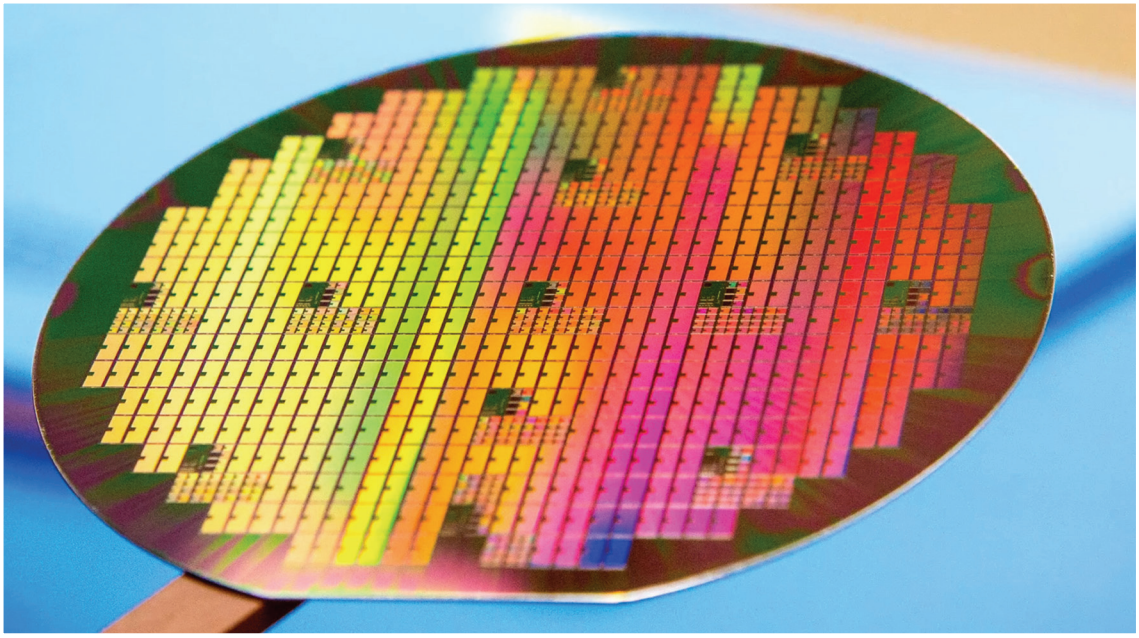
BY ALEXANDER BOLOTNIKOV, REZA GHANDI, PETER LOSEE, STACEY KENNERLY AND RAVISEKHAR RAJU FROM GENERAL ELECTRIC

THERE ARE SIGNIFICANT drawbacks associated with today's medium-voltage power conversion systems. These converters – installed on ships, used in wind turbines, fitted on solar farms and appearing in traction drives in transportation – are held back by a maximum switching frequency of no more than several hundred hertz. This limitation, stemming from solid-state switch and diode losses, dictates that the transformer, as well as the components for the converter filter, are very large and heavy. In turn, this leads to high costs for the system and its installation, and restrains design flexibility.

What's needed are highly efficient, lightweight power-conversion systems that can handle many megawatts while running at switching speeds of several kilohertz. Such converters are only a dream today, but they could become a reality if solid-state devices could switch at frequencies from one kilohertz to hundreds of kilohertz, while handling hundreds of amps.

Those that are developing these devices include our team at General Electric. Our successes to date include a SiC junction barrier diode with a novel, charge-balanced architecture that slashes conduction losses.

The benchmark for judging our devices is the incumbent technology in medium-voltage power conversion applications: silicon insulated-gate



GE is developing SiC Schottky barrier diodes with an impressive on-resistance for the given operating voltage

bipolar transistors (IGBTs) and diodes made by the likes of Infineon Technologies and ABB. In these bipolar devices, injected carriers are stored in the device's lightly doped blocking layers. In the on-state, these carriers increase the background carrier concentration, and enable a low forward-voltage drop (see Figure 1). And in the blocking-state, high voltages are possible, thanks to drift layers that are hundreds of microns thick and doped to levels of just 10^{13} cm^{-3}. For silicon IGBTs, these layers can lead to a blocking voltage as high as 6.5 kV.

The penalty to pay for these stored carriers in high-voltage silicon power devices is extreme losses, even at switching speeds of just 1 kHz. Consider, for example, a silicon IGBT module designed to handle up to 6.5 kV and 400 A. It has a turn-off loss of 2.1 J, equating to 1 kW of dissipation for switching at 500 Hz.

Note that designers of these modules are not just trying to minimise this switching loss. Their overriding goal is to find the sweet spot between realizing low switching losses and a low conduction loss. So, for example, in modules made by ABB the on-state voltage ranges from 2.7 V to 5.4 V, well beyond the entitlement for a silicon turn-on voltage of 0.7 V. This high on-state voltage is chosen to ensure switching loss reduction, but it constrains current density to typically between 30 A/cm^2 and 60 A/cm^2.

Yet another limitation stems from the high on-state voltage drop associated with the bipolar devices' *p-n* junction. This drags down converter efficiencies under partial load operation.

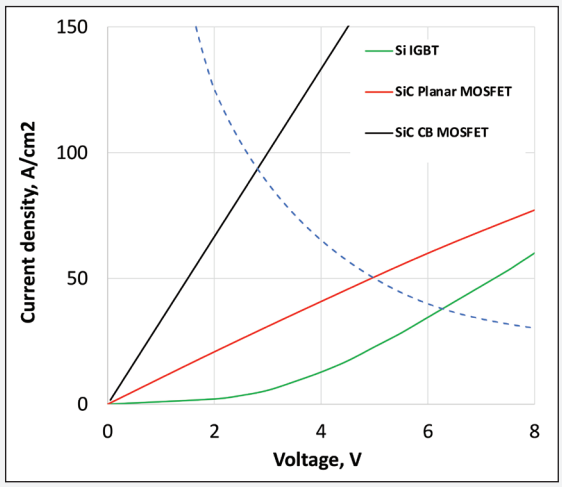


Figure 1. Comparison of typical forward characteristics of 6.5 kV devices at 125 °C. The SiC charge-balanced (CB) MOSFET offers a relatively high current density for a given forward voltage.

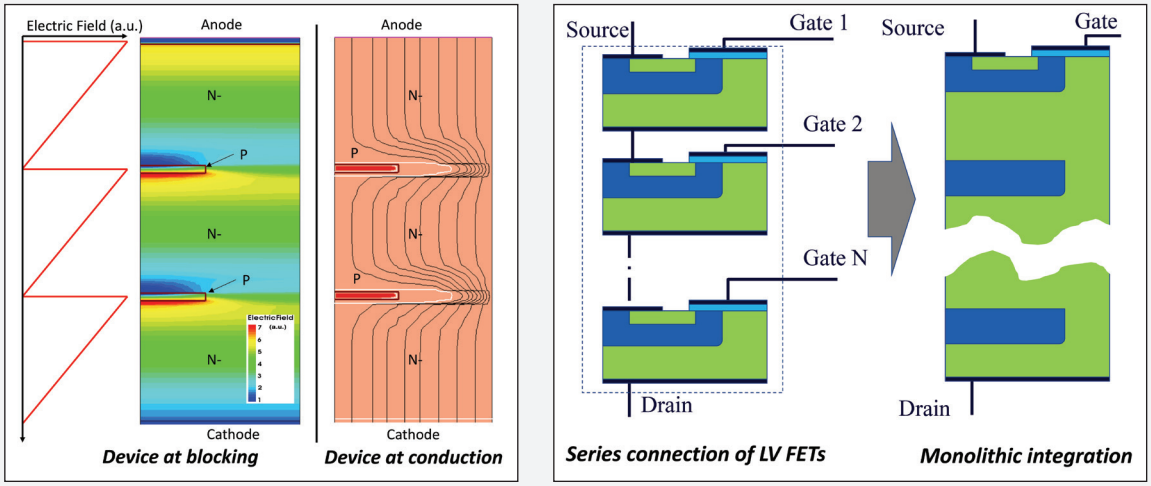


Figure 2. The operation (a) and design (b) of the charge-balance device.

The solution to all these problems is to turn to wide bandgap power switches and diodes. Devices made from GaN and SiC promise far lower switching losses and more efficient power conversion in a wide range of applications. What's more, for lower-voltage applications – that is those between 650 V and 2.5 kV – SiC devices also tend to operate with lower conduction losses.

However, when it comes to the devices typically deployed in medium-voltage converter applications, SiC is currently failing to fulfil its potential. One issue is that the conduction loss found in the drift layers of SiC unipolar devices is, at elevated temperature, often only marginally better than that of silicon IGBTs and diodes – and it can be even worse. Compounding matters, in SiC IGBTs, the large bandgap leads to an on-state voltage drop of more than 4 V at all operating current densities. And last but by no means least, the low current densities in SiC MOSFETs, IGBTs, and diodes results in the need for large die areas for handling the power levels required for megawatt applications. This is bad news, as it exacerbates chip costs.

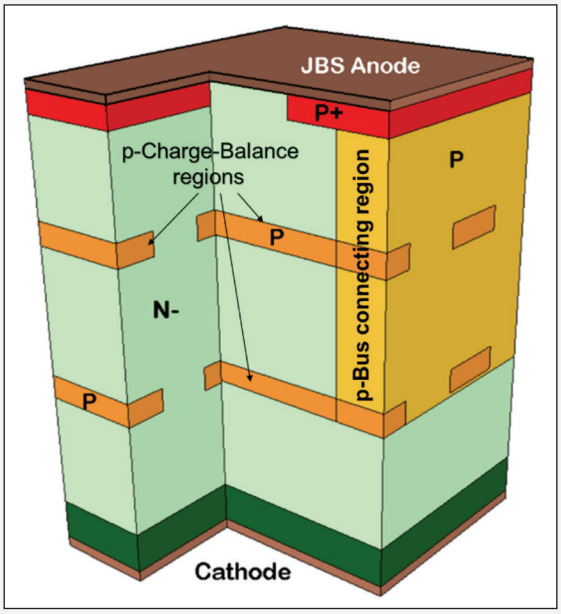


Figure 3. Engineers at General Electric are pioneering the SiC charge-balance junction-barrier Schottky diodes. They feature p-charge balance and p-connecting regions.

Two options for addressing the decline in the performance of SiC devices at increasing voltages are the series connection of lower-voltage devices, and drift layer engineering that utilizes 'superjunction' technologies. The latter is preferred, as it does not require multiple devices. Instead, it features a drift/blocking region that consists of multiple, alternating *n*- and *p*-type doped pillars with a relatively high doping that allow a high breakdown voltage. This is in stark contrast to the standard approach for realising a high blocking voltage: a single, lowly and uniformly doped blocking region that when depleted results in a nearly uniform electric field distribution in the drift region.

Several groups, including that headed by Paul Chow from Rensselaer Polytechnic Institute, have modelled the SiC superjunction vertical power device. But the realisation of these devices has remained elusive until now. While trench and refill approaches have garnered some interest, it is challenging to realise high aspect ratios, doping controllability, and scalability to higher voltages. These barriers have held back the experimental demonstration of a fully functional device.

We have broken through, by addressing the key challenge of achieving deep/high-aspect-ratio pillars of dopants in SiC superjunction devices with a novel, yet practical, SiC charge-balance drift region architecture. Armed with this technology, we have produced the first ever SiC junction-barrier Schottky diode.

How does charge-balancing work?

In our devices, the buried *p*-type charge-balance regions compensate for the higher *n*-drift doping concentration under reverse bias (see Figure 2). When the charge-balance regions are designed correctly, they act as electric field dividers, allowing an increase in doping in the drift region for a given breakdown voltage. The upshot is a reduction in conduction losses. Note that this concept is very similar to that of the serial connection of low-voltage devices that are monolithically integrated on the same chip.

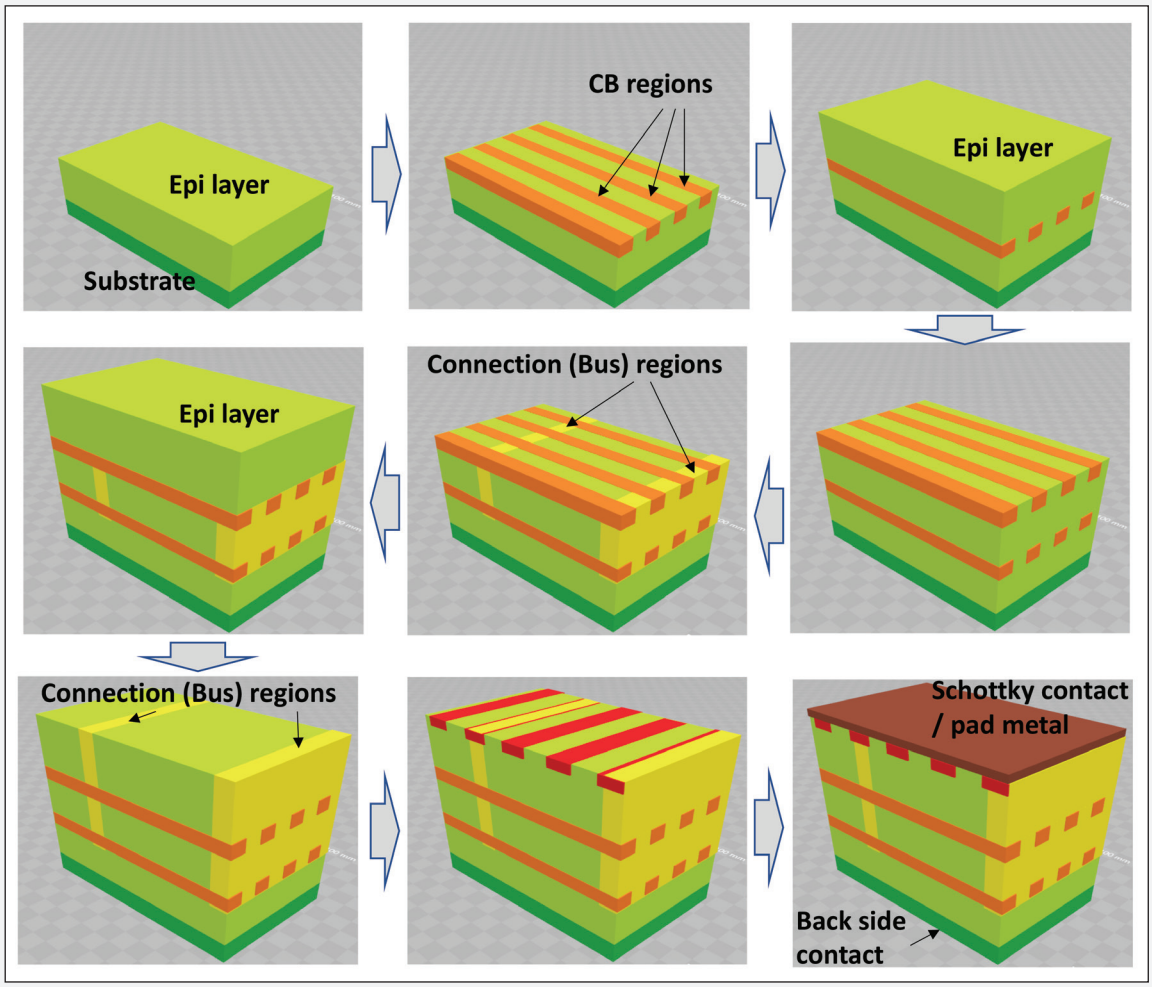


Figure 4. Several steps are required to fabricate SiC charge-balance junction-barrier Schottky diodes.

The drawback of such a structure is its poor dynamic response. The charge-balance regions require holes in the *n*-type drift layer to transition from blocking to conduction. Unfortunately, this cannot occur quickly enough when relying only on the recombination-generation rates of the carriers. To alleviate this bottleneck, our design also employs *p*-Bus connecting highly doped *p*-type regions (p^+) of the planar device to each of the charge-balance regions (see Figure 3). This refinement allows holes to flow into and out of the charge-balance regions during switching events.

The challenge with our architecture is to make the *p*-Bus connecting region sufficiently narrow, and with low enough doping, to minimize the alteration of the electric field distribution of the charge-balance drift region; but to make this region conductive enough to establish a good connection between the p^+ and charge-balance regions.

We have exceeded in this endeavour with our 2 kV and 3 kV SiC charge-balance, junction-barrier Schottky diodes, which were fabricated from 4H-SiC wafers with 10 μm-thick epitaxial layers doped at 1×10^{16} cm^{-3}. Our fabrication process began with the formation of *p*-type charge-balance regions fabricated by ion implantation of aluminium. After this, we undertook additional epigrowth, before adding *p*-connecting regions via high-energy implantation of aluminium using Tandem Van de Graaff facility at Brookhaven National Lab.

Our 2 kV diodes feature two 10 μm-thick epilayers and a single charge-balance region, while their 3 kV

Our results show that SiC Schottky barrier diodes with a novel architecture featuring a charge-balanced drift region can break the one-dimensional limit for on-resistance as a function of breakdown voltage. This success should pave the way to medium-voltage-class SiC unipolar switches with on-state and dynamic losses that are well below those of their silicon counterparts.

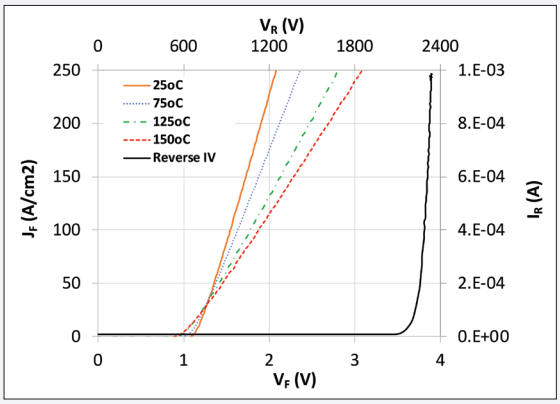


Figure 5. Forward and blocking current-voltage characteristics of a 2 kV SiC charge-balance junction-barrier Schottky diode.

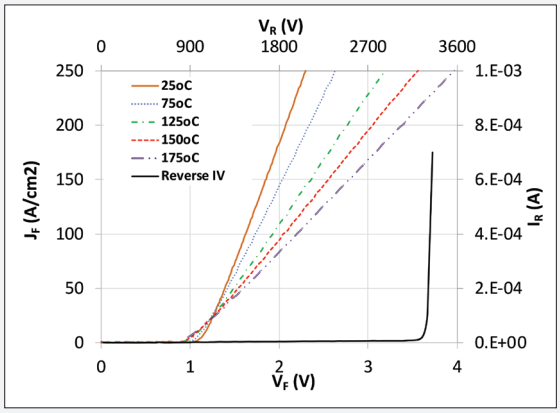


Figure 6. Forward and blocking current-voltage characteristics of 3 kV SiC charge-balance junction-barrier Schottky diodes.

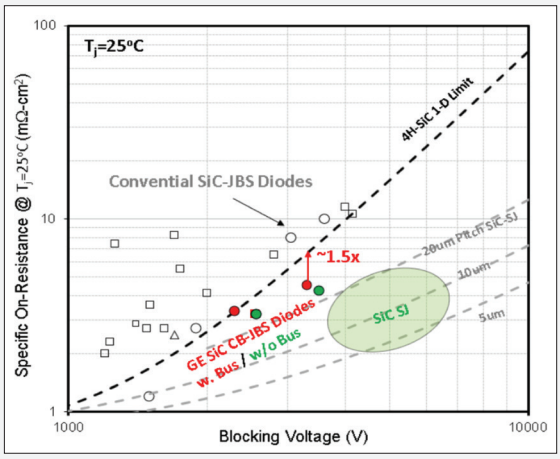


Figure 7. Differential on-resistance versus breakdown voltage for reported SiC FETs and diodes.

cousins have a total of three 10 μm epilayers and two charge-balance regions. Due to these differences, the steps for making 3 kV diodes include the fabrication of an additional charge-balance region, and further epitaxial growth and bus region implantation. In both cases, device fabrication is completed by forming a nickel-based Schottky junction-barrier diode on the top surface, and joining p^+-regions to p-connecting regions.

After packaging these devices, we have tested them at both room temperature and elevated temperatures to evaluate their static and dynamic characteristics.

Equipped with a nickel contact, the turn-on voltage for our diodes is around just 1 V (see Figures 5 and 6), while the differential room-temperature on-resistance is as low as 3.5 mW-cm² and 4.3 mW-cm² for the 2 kV and 3 kV versions, respectively. These measurements also uncover sharp breakdown voltages at more than 2.3 kV and 3.3 kV. Note that these values are far higher than would be possible with a conventional vertical device architecture sporting a drift layer doped at a concentration of 1 x 10^{16} cm^{-3}.

We have compared the performance of our devices, both with and without connecting regions, to conventional SiC MOSFETs and diodes. Plotting the specific on-resistance as a function of blocking voltage revealed that at more than 3 kV, our devices outperform the theoretical one-dimensional unipolar limit by up to 50 percent, while the level of superiority over commercial devices is even higher (see Figure 7).

Double-pulse switching tests have been used to assess the switching characteristics of our diodes (see Figure 8 for details of the circuit, which features the 2.5 kV/35 A SiC MOSFET, providing an active switch that is capable of turning on and off faster than 100 ns). Traces on an oscilloscope show that during the turn-on of the active switch there is reverse recovery in the charge-balanced junction-barrier Schottky diodes, followed by turn-on of the freewheeling diode during turn-off of the active switch.

These measurements enable us to estimate switching losses from forward recovery and reverse recovery of 12.91 mJ/cm² and 1.9 mJ/cm², respectively, for the 2 kV devices, and 23.65 mJ/cm² and 2.49 mJ/cm², respectively, for the 3 kV devices. For nominal conditions of a forward current of 125 A/cm², a 50 percent duty cycle, and a

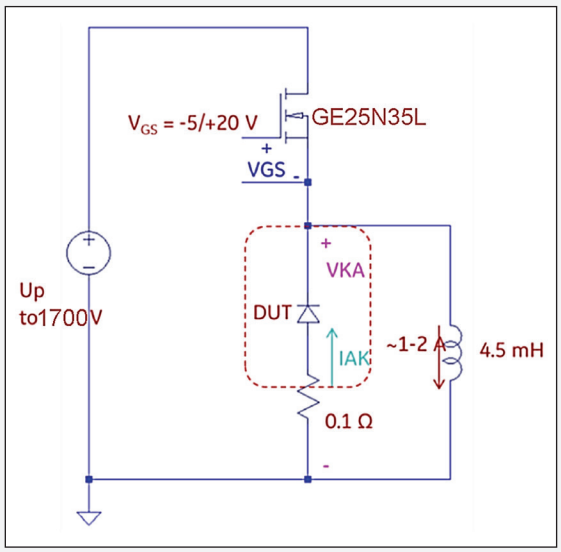


Figure 8. The high-voltage, double-pulse circuit used at General Electric to characterize its SiC charge-balance junction-barrier Schottky diodes assembled in TO-247 moulded packages.

junction temperature of 150 °C, total switching loss for a rated DC-link voltage is approximately 6.2 mJ/cm² for the 2 kV device and 12.5 mJ/cm² for the 3 kV device. Assuming a thermal limit of 250 W/cm², these findings suggest that diodes could operate at frequencies of up to 20 kHz, and thus deliver a disruptive performance in many high-voltage power-conversion applications.

Our results show that SiC Schottky barrier diodes with a novel architecture featuring a charge-balanced drift region can break the one-dimensional limit for on-resistance as a function of breakdown voltage. This success should pave the way to medium-voltage-class SiC unipolar switches with on-state and dynamic losses that are well below those of their silicon counterparts. However, in order to capitalize on these benefits, there needs to be development of disruptive low-inductance and high-voltage packaging and converter topologies with improved thermal performance – and these technologies must accommodate the higher power densities and magnetics associated with the severe changes in voltage and current with time.

We will focus on scaling our developed, charge-balance device drift architecture to higher voltages. This has the potential to disrupt the existing units deployed in many applications that use switching frequencies of less than 1 kHz to more than 10 kHz. Look out for the next device we plan to demonstrate: a 4.5kV SiC charge-balanced MOSFET with a targeted room temperature specific on-resistance of less than 12 mW-cm².

The information, data, or work presented herein was funded in part by the Advanced Research Projects Agency-Energy (ARPA-E), U.S. Department of Energy, under Award Number DE-AR0000674 advised by Program Director Isik Kizilyalli. The views and opinions of authors expressed herein do not necessarily state or reflect those of the United States Government or any agency thereof.

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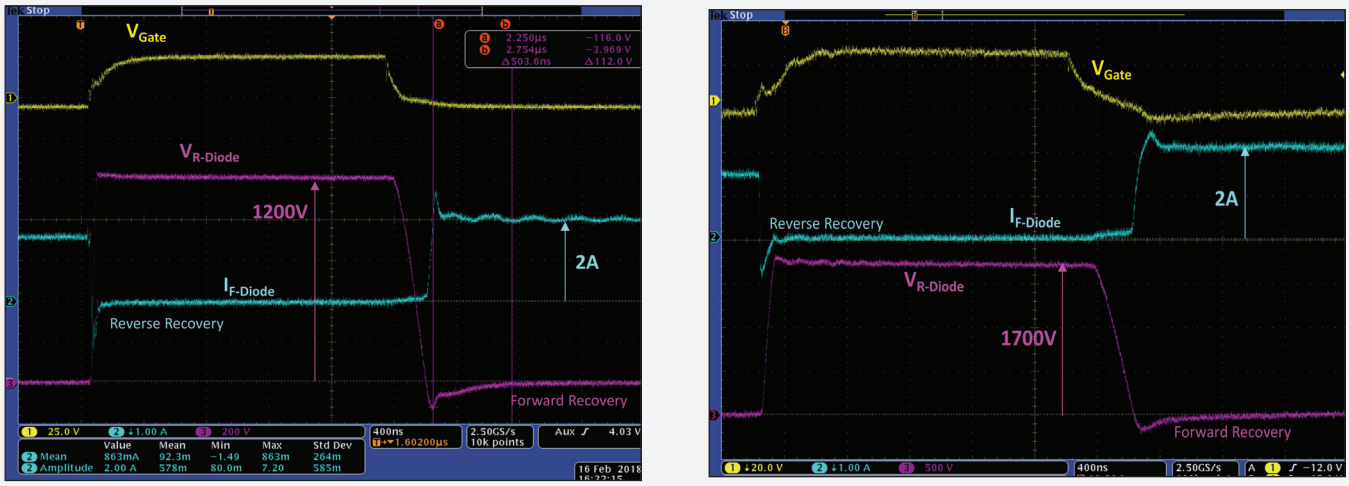

Figure 9. High-voltage double-pulse, diode-clamped inductive switching waveforms using a 2 kV (left) and 3 kV (right) charge-balance junction-barrier Schottky diode as the free-wheeling diode with reverse voltage of either 1200 V or 1700 V and a forward current of 2 A (forward current density is 250 A/cm²). The yellow trace represents the gate-source voltage of the MOSFET, used to turn-on the active switch and drive the freewheeling diode into reverse recovery until the diode current returns to zero and the load current flows through the switch. The reverse recovery phase of SiC charge-balance junction-barrier Schottky diodes is virtually indistinguishable from those of conventional SiC Schottky diodes. Beyond the reverse recovery phase, the reverse voltage on the charge-balance junction-barrier Schottky diode is 1200 V (left) and 1700 V (right) (these values are about 60 percent of the rated voltage). After some duration, the active switch is turned off and the load current begins to commute to the SiC charge-balance junction-barrier Schottky diode. With the active switch now in the off state, the forward current through the free-wheeling diode quickly ramps from zero to the full load current of 2 A. When turned on from blocking state to conducting state with a fast ramp, the SiC charge-balance junction-barrier Schottky diodes have an observable forward recovery phase. The waveforms show that the forward voltage across the diode has a large peak, before decaying back to nominal value for the forward voltage approximately 500 ns after turn-on. It is believed that this delay is due to the resistance from the p^+ anode to the buried charge-balance regions via the deep p-bus regions. This view is consistent with a decrease of one-fifth in turn-on loss at 150 °C.

Superior silicon carbide

Solution growth eliminates basal plane dislocations in high-quality single crystals of bulk SiC

BY KAZUHIKO KUSUNOKI, KAZUAKI SEKI AND YUTAKA KISHIDA FROM NIPPON STEEL AND SUMITOMO METAL CORPORATION AND HIRONORI DAIKOKU, HIROAKI SAITO, ISAO KOBAYASHI AND HIROSHI MIHARA FROM TOYOTA MOTOR CORPORATION

THE GLOBAL DEMAND for electricity is rising far faster than that for all forms of energy. According to the International Energy Agency, worldwide energy demand increased by 2.1 percent in 2017, while that for electricity climbed by 3.1 percent.

As electricity usage rises, the total gains resulting from more efficient power devices will become ever more significant. This makes it more attractive than ever for humanity to invest in SiC diodes and transistors, which have much lower losses than their silicon siblings.

Right now, sales of SiC devices are climbing fast. But even more success is possible, along with a greater share of the power semiconductor market, if SiC manufacture were to include the production of substrates that are cheaper, larger, and exhibit a higher crystal quality. Read on to discover how this can be accomplished.

Growing single crystals of SiC is far from easy. The 4H-SiC single crystal substrates that are on the market today are plagued by various dislocations – in total, the density of imperfections is in the range of thousands to ten thousand per cm^2 (see Table 1 for a list of common dislocations, and Figure 1 for an illustration of how they may appear in 4H-SiC single-crystal substrates). These dislocations are a menace, driving down device manufacturing yield and applying the breaks to far greater deployment of SiC power devices.

By far the most troublesome class of dislocations are the line defects in the 4H-SiC{0001} basal planes. Known as basal plane dislocations, these killer defects wreak havoc with device performance. It drops when a forward voltage is applied across 4H SiC MOSFETs and *p-i-n* diodes, and basal plane dislocations are driven from the SiC single-crystal substrates to the epitaxial layers, where they expand and turn into Shockley-type stacking faults. There they act as high-resistance layers, increasing the on-state voltage and driving a deterioration in device performance.

One way to address this issue is to convert the basal plane dislocations into threading-edge dislocations at the interface between the epitaxial stack and the substrate. This conversion must take place during the epitaxial growth, by CVD, of layers on the SiC substrate. Note that the threading-edge dislocations that are formed are harmless, as they don't degrade

Types of Dislocations	Direction of dislocation	Burgers Vectors	Density (cm^{-2})
			Commercially available wafer
Threading Screw Dislocation (TSD)	// c-axis	n<0001> (n=1, 2)	500-3000
Threading Edge Dislocation (TED)	// c-axis	1/3<11-20>	3000-10000
Basal Pane Dislocation(BPD)	⊥ c-axis	1/3<11-20>	500-7000

Table 1. Types and density of dislocations in 4H-SiC crystals

device characteristics. However, as it is not possible to convert every single basal plane dislocation into a threading-edge dislocation, this is an imperfect solution. It would be far better to completely eliminate the basal plane dislocations in SiC.

Unfortunately, it is challenging to produce SiC crystals, the starting point for substrate production. At normal pressure, there is no liquid phase of SiC with a chemical composition for the melt that matches that of the solid state. Consequently, it is theoretically impossible to carry out melt growth by solidification, which is the approach adopted for making silicon boules.

Due to this limitation, today's SiC substrates are manufactured with a gas phase method that can produce 4H-SiC bulk single crystals. Sublimation takes place at temperatures of at least 2,300 °C. Stresses associated with the high temperatures, and cooling down from them, give rise to thermal stress. This is released by movement in 4H-SiC basal planes, which are easy slip planes, and results in basal plane dislocations with a density of hundreds per cm^2 or more.

The highest quality crystals formed by the sublimation method are those that have been made by a team from Toyota Central R&D Labs, Japan, using repeated *a*-face (RAF) growth. However, this material is not free from basal plane dislocations.

To eradicate these dislocations, an alternative growth method is required. That's the approach that our team from Nippon Steel and Sumitomo Metal Corporation and Toyota Motor Corporation is taking, using a solution growth technique to realise ultra-high-quality SiC single crystals.

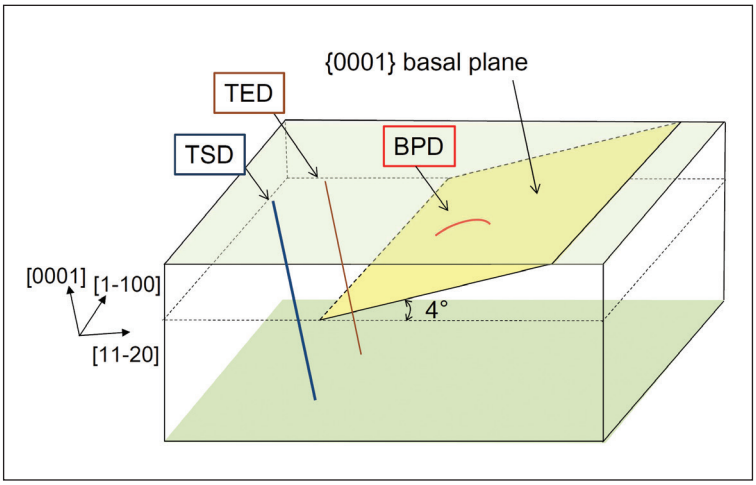

Figure 1. Dislocations in a 4H-SiC single crystal substrate (4° off-axis)

Our approach is a form of liquid phase growth. SiC is dissolved in a metallic melt that contains chromium or titanium, with supersaturation driving the formation of the crystal. With this approach, the reaction takes place at close to the thermodynamic equilibrium state, enabling the crystal growth to proceed at a temperature that is lower, by a few hundred degrees Celsius, than it would be for a sublimation method (see Figure 2).

Suppressing solvent inclusions

One of the challenges with our approach is that as the SiC crystal forms from a liquid phase, we must prevent the surface from roughening as the material thickens. This threat, known as surface morphology instability, can create concavities and convexities with dimensions of several hundred microns to several millimetres. In the fine concavities, any solvent microdrops that are left can spawn macroscopic defects, known as solvent inclusion.

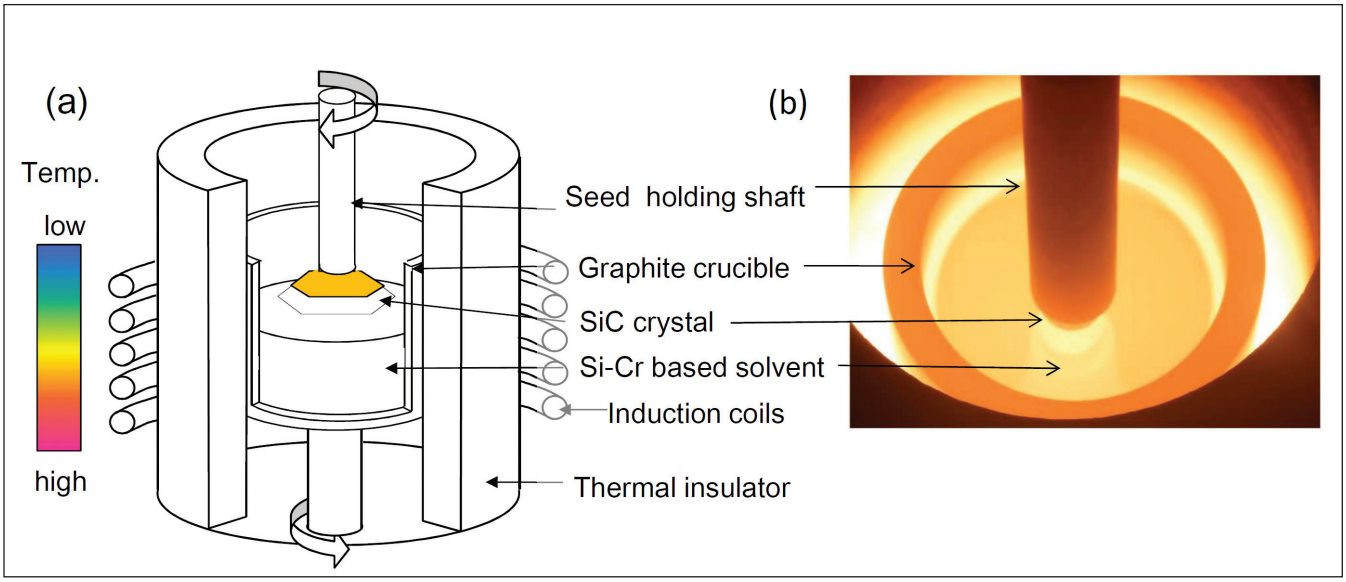

Figure 2. (a) The SiC solution growth set-up used by engineers at Nippon Steel and Sumitomo Metal Corporation and Toyota Motor Corporation. The graphite crucible, which provides a container for the solvent and a carbon source, is directly heated by induction. Growth, typically at 2000°C, is conducted under atmospheric pressure in a mixture of helium and nitrogen gases. (b) Inside a crystal growth furnace.

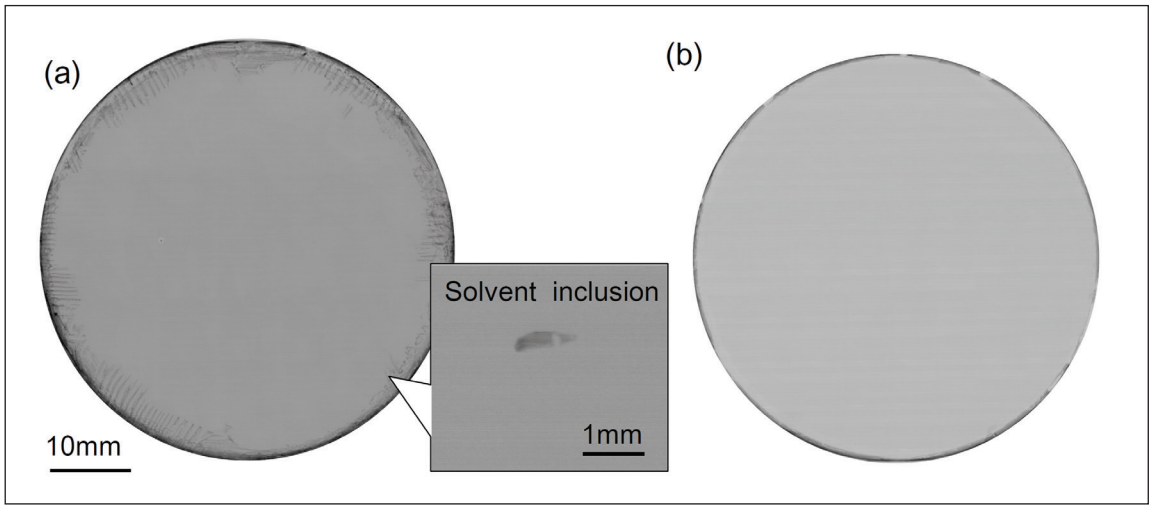

Figure 3. Transmission X-ray images of 2-inch-diameter 4H-SiC ingots (a) before optimising crystal growth conditions, and (b) after optimisation. It is clear that several dark domains exist at the peripheral part on the crystal, formed using the conventional growth technique. These domains are ascribed to a metal solvent that has a lower X-ray transmittance compared with the SiC matrix. Note that no dark domains are observed for the whole volume in the crystal after optimising growth conditions, indicating that this material is free from solvent inclusion.

Substrates with this form of imperfection are unsuitable for making power devices. So, to prevent them forming, the growing surface has to be smooth for extended periods of time during crystal growth. That's a very demanding technical challenge that has remained elusive for many years.

We have overcome this challenge by considering the numerous process factors associated with crystal growth. Taking this approach reveals that it is possible to stabilise the surface morphology, and ensure a smooth surface, by controlling the growing interface outline while suppressing changes in supersaturation over time. By adopting these findings, we have produced the first 2-inch bulk crystals that are free from solvent inclusion (see Figure 3).

Using the solution growth method, we have also

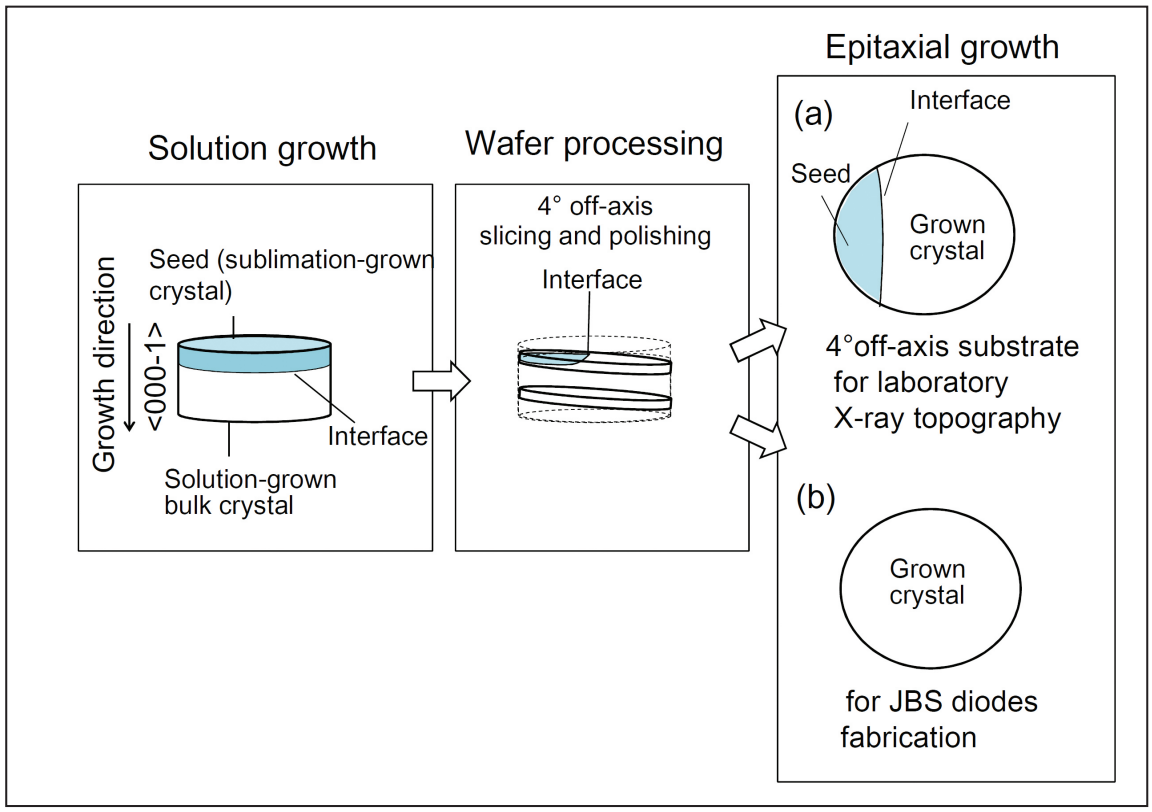

Figure 4. Slicing the material produced by the solution growth method creates (a) wafers for evaluating dislocations, and (b) wafers for prototyping junction barrier Schottky diodes.

produced 4-inch crystals that are more than 10 mm-thick. An obvious next step is to apply the solvent inclusion elimination technology that we have established for 2-inch diameter crystals to the growth of those that are 4-inch in diameter.

Those of us at Nippon Steel and Sumitomo Metal Corporation are drawing on this growth technology to produce, from ingots, 2-inch diameter 4H-SiC substrates with an off-angle of 4°. These can provide a great foundation for making for power devices.

To evaluate the quality of our SiC substrates, we have compared the dislocation density of our crystals produced by the solution growth method – from now on referred to as solution-grown crystals – with that of a seed crystal. This has been accomplished by using the solution growth method to grow a crystal on the on-axis plane (000$\bar{1}$) of a seed crystal. Tilting this at 4°, and slicing and polishing wafers from it, creates a sample that includes the interface between the seed crystal and solution-grown crystal.

We deposited a 10 μm-thick layer on this sample by CVD, before scrutinising the material with X-ray topography (see Figure 4). This reveals that the seed crystal area features a high-density mesh contrast, originating from basal plane dislocations. Meanwhile, in the solution-grown crystal area, no such contrast is observed.

These findings indicate that there are no basal plane dislocations in the solution-grown crystal (see Figure 5). In addition, they show that when the basal plane dislocations in a seed crystal in the {0001} plane intersect at right angles with the crystal growth direction, they do not propagate into the solution-grown crystal. Yet another insight provided by X-ray topography is that the solution growth and cooling processes do not generate any new basal plane dislocations. We attribute this to the lower temperature for solution growth than for sublimation growth.

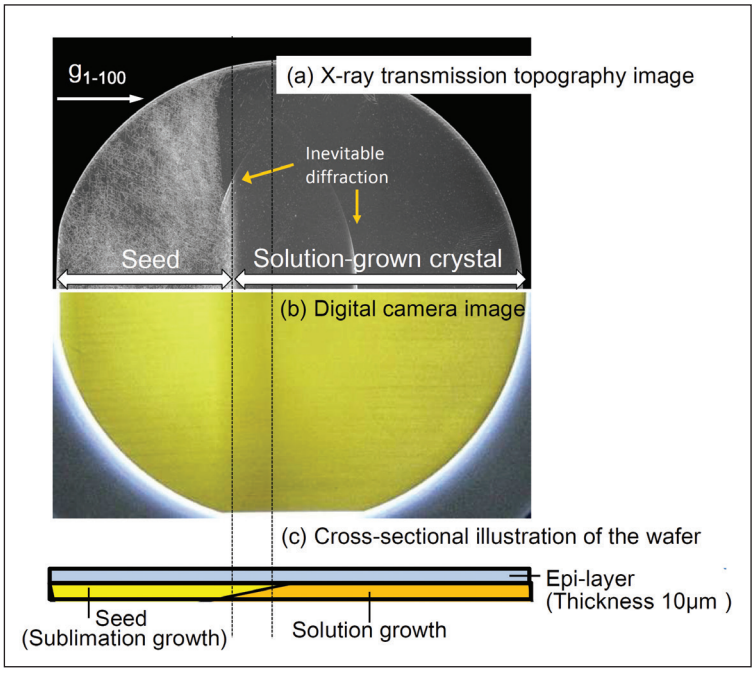

Figure 5. 2-inch diameter 4H-SiC wafers have been analysed by (a) transmission X-ray topography, (b) digital camera images, and (c) by taking cross-sections.

To ensure high-performance devices, the surface of SiC must be impeccably clean. This includes incredibly low levels for metallic contaminants on the surface, as their presence can degrade the characteristics of a power device, and compromise yield.

As our solution growth involves a chromic solvent, there is a danger that this might impair the quality of our material. To see if that is the case, we have quantified the metallic impurities on the front and back sides of our of epitaxial wafers, using inductively

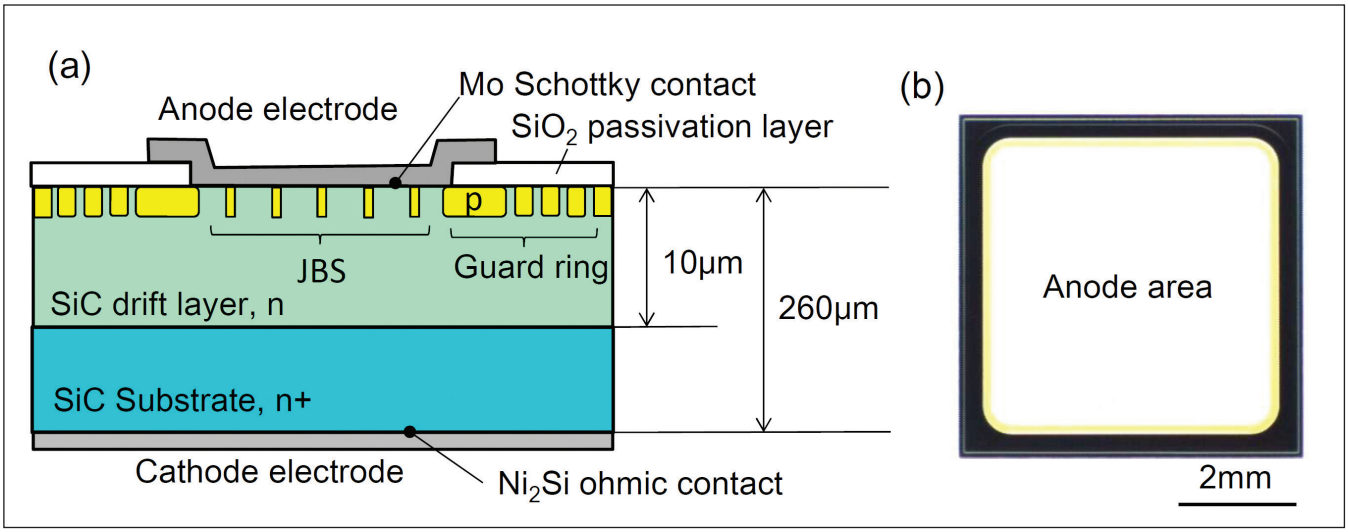

Figure 6. (a) A vertical cross-sectional view of junction barrier Schottky diode. (Taken from H. Fujiwara *et al*. Appl. Phys. Lett. **100** 242102 (2012). (b) Plan view of a junction barrier Schottky diode. Active area is 6 mm by 6 mm.

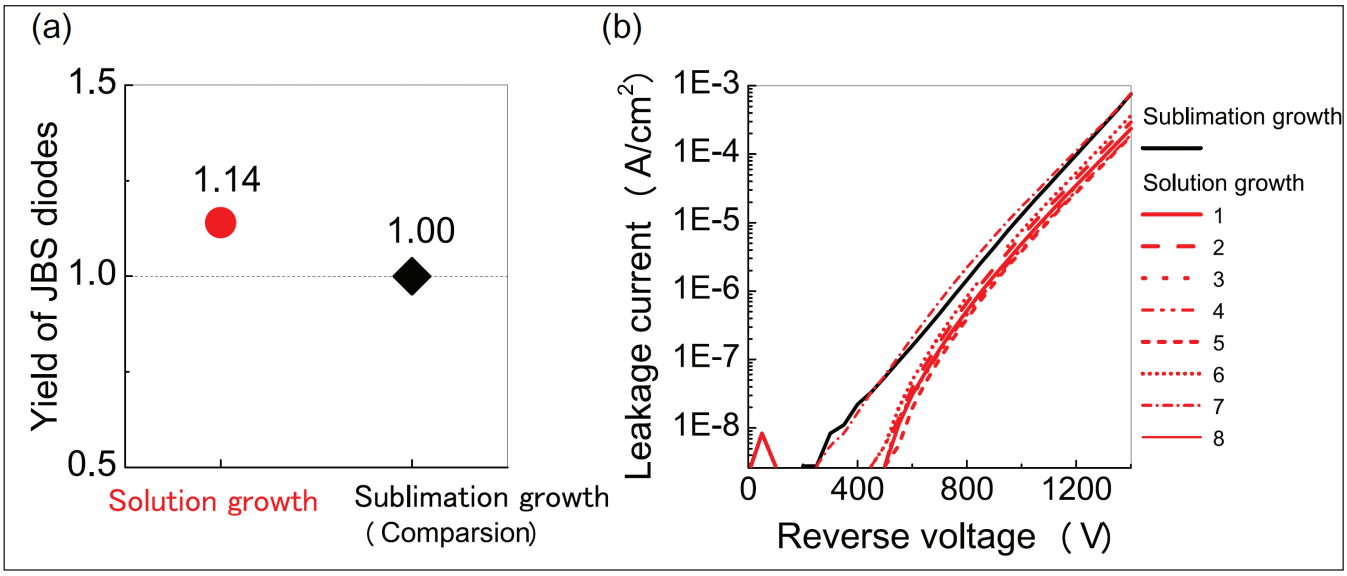

Figure 7. (a) A comparison of the proportion of efficient junction-barrier Schottky diodes fabricated on solution-grown and sublimation-grown SiC substrates. Note that the yield of the junction-barrier Schottky diodes fabricated on the solution growth substrate was normalized by that obtained on the sublimation-grown substrate. (b) Relationship between reverse current and voltage characteristics for the junction barrier Schottky diode.

coupled plasma mass spectrometry and direct acid droplet decomposition.

This technique reveals that the front and back sides of our wafers have negligible levels for many common metals – values were below 3.5×10^{11} atoms/cm^2 for more than a dozen common elements: calcium, sodium, potassium, magnesium, titanium, chromium, manganese, iron, cobalt, nickel, copper, zinc and aluminium. We believe that the extreme cleanliness of the surfaces of our solution-grown SiC wafers could result from the availability of bulk crystals without solvent inclusion. Such low levels of contaminants confirm that there are no concerns associated with using solution-grown SiC epitaxial wafers in device manufacturing lines.

Building better devices

We have fabricated the world's first junction-barrier Schottky diodes at the wafer level on solution-grown SiC. For the production of these devices, we used a 2-inch diameter solution-grown 4H-SiC substrate (see Figure 6).

To evaluate the electrical performance of the diodes, we compared their performance with equivalents grown on commercially available, high-grade substrates manufactured by sublimation. The efficiency and electric characteristics of devices grown on our substrates are equal to, or higher than, those grown on the alternative foundation (see Figure 7).

This test is not ideal for highlighting the superiority of our substrates. That's because basal plane dislocations in the substrate have little effect on the degradation of electric characteristics of a junction barrier Schottky diode. Where our substrates promise to make a far bigger contribution is to improving the performance of diode-built-in MOSFETs and 4H-SiC *p-i-n* diodes. When prototypes of these devices are made on our substrates, they will demonstrate the overwhelming superiority of solution-grown SiC crystals.

We have made much progress, but there is still work to do. Today, sublimation is used for high-volume manufacture of 6-inch diameter SiC, while the diameter of solution-grown wafers is still small, delaying success in the marketplace.

However, when solution grown SiC material hits the market, success could be rapid. This form of substrate will be in much demand, thanks to its absence of basal plane dislocations, a known killer defect that is an obstacle to obtaining high-performance, highly-reliable SiC power devices. What's more, for this form of substrate, costs have the potential to fall below those made by sublimation, as growth takes place at normal pressure and under lower temperatures.

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- **ENERGY –** POWERING ADVANCED SYSTEMS
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The automotive sensor market is expected to reach $37 billion by 2022. Automotive sensors detect, measure, and transmit data within and between vehicles to maintain high performance, increase safety and automate driving. While today's vehicles have as many as 700 significant electronic components, this tally could exceed 2,000 once active driver assistance and vehicle automation technologies proliferate. Key companies including Google, Tesla Motors, Facebook and Apple, along with all major automobile and truck manufacturers, are focused on the research and development of driverless cars, further expanding the need for advanced automotive sensors including imaging, radar, LiDAR, pressure, temperature, navigation, communications and secure data devices. We will explore the wide range of automotive sensors and critical factors affecting growth opportunities including sensor fusion.

SPEAKERS

- **Nicolas Sauvage – TDK-Invensense**
  Sensing for autonomous mobility – KEYNOTE
- **Wade Appelman – ON Semiconductor**
  Sensors for Long-Range Automotive LiDAR
- **Alexis Debray – Yole Développement**
  LiDAR – From space to roads
- **Heinz Oyrer - Leddartech**
  Leverage Ecosystem Collaboration to Create a Versatile and Scalable LiDAR Solution
- **Holger Hegner - TDK Electronics AG**
  Temperature sensors solutions for passenger comfort
- **Stephen Fendyke - FiveAI**
  Transforming Europe's cities: An Introduction to FiveAI
- **Tobias Bahnemann - Toposens**
  Near-field sensing for autonomously moving vehicles
- **Mike Dempsey - Claytex**
  Sensor models enabling autonomous vehicles to perceive the road ahead more clearly
- **Marc Schillgallies – First Sensor**
  LiDAR receivers for automotive applications
- **Erich Smidt – Velodyne**
  Presentation Title TBC
- **Julien Fabrègues - TDK Micronas**
  Magnetic sensors solutions to address EV and autonomous vehicle platform

ENERGY – POWERING ADVANCED SYSTEMS

Sensor nodes dependent on wireless connectivity face a common yet critical problem: battery lifetime. While energy harvesting cannot benefit every wireless sensing scenario, it is being successfully applied in industrial and consumer applications. Converting available energy from a variety of sources to electricity provides an alternative to frequently changing batteries or complicated low voltage wired solutions that negate the benefits of wireless connectivity. When paired with advanced thin-film batteries, capacitors or emerging power storage technologies, energy harvesting can significantly extend operational lifetimes for highly efficient power management. We will explore popular energy harvesting techniques including photovoltaic, thermoelectric, piezoelectric, electrodynamic and wind resources.

SPEAKERS

- **Matthias Kassner - EnOcean**
  Energy harvesting options for wireless sensors
- **Edsger Smits - Holst Centre**
  Autonomous sensing surfaces for smart buildings
- **Viktor Börjesson - ReVibe Energy AB**
  Vibration energy harvesting for the Industrial IoT
- **Mathieu Bellanger – Lightricity**
  Presentation Title TBC

IMAGING – DETECTION, IDENTIFICATION AND RANGING

Active optical devices, photonic integrated circuits and emerging imaging solutions that leverage RF or Hall effect technologies are advancing the role that imaging plays across almost every imaginable market and industry. Like other sensors, imaging devices need high resolution, linearity, low power consumption, network security and dependable performance. This session will explore ways that new device designs, photonic integration, silicon photonics and III-V hybrids are advancing state-of-the-art performance while indium phosphide (InP), VCSELs, gallium arsenide (GaAs) and other key technologies will continue to play significant roles in near- and long-term sensor evolution.

SPEAKERS

- **Kris De Meester – Xenomatix**
  Best Practices for integrating solid state lidar in serial cars
- **Paul LeClaire – Knowmade**
  Gesture Recognition and 3D Sensing Technologies for Mobile Devices
- **Mohamed Missous - University of Manchester**
  Microstructural Imaging and characterisation of metallic structures using Quantum enabled Semiconductor devices for NDT applications.
- **Iwan Davies - VIDaP Consortium**
  Presentation Title TBC

HEALTH – SOCS FOR DIAGNOSES AND WELLBEING

Advancements in low-power, compact wearables that incorporate sensors, actuators, antennas and smart textiles are significantly impacting the evolution of healthcare, diagnostic and treatment tools. When melded with inexpensive computing SoCs, data storage and wireless access, the road has been paved for low-cost and unobtrusive health monitoring and treatment systems built around advanced sensor technologies. The global medical sensors market is estimated to reach $15.01 billion by 2022, with the disposable/ingestible medical sensors market expected to reach $12.3 billion by 2025. We will explore the impact of sensor technologies across major sectors of healthcare as governments, industry and universities focus massive resources on exciting new ways to diagnose, treat and prevent diseases.

SPEAKERS

- **Valer Pop - Lifesense Group**
  Carin: a global rising star
- **Susanne Oertel – Fraunhofer IISB**
  Don´t hesitate to sweat – sensors for analysis in sport wearables
- **Paul Galvin - Tyndall National Institute**
  Smart sensor systems - an impending revolution in digital healthcare
- **Tristan Rouselle – Aryballe Technologies**
  Presentation Title TBC

FLIGHT – AVIATION AND AEROSPACE FRONTIERS

Advanced sensing technologies play increasingly critical roles in not only the operational performance of advanced aircraft and aerospace vehicles, but throughout planning, development, fabrication and flight test stages. We will explore sensor technologies that support these requirements to satisfy wide-ranging needs through assessing critical variables to ensure passenger and crew safety while meeting high performance standards.

SPEAKERS

- **Vincent Gaff - TDK Tronics Microsystems**
  Inertial sensors for precise navigation, stabilization and motion control



IIOT – LEADING INDUSTRIAL AND CONSUMER (IOT) STRATEGIES

Sensing technologies owe much of their growth to networking and internet connectivity including the burgeoning (IoT) market. While the IoT is just beginning, the Industrial IoT (IIoT) is already reshaping business on the manufacturing floor as part of 'Industry 4.0' movements. This session will explore wireless networking standards / protocols, licensed and unregulated spectrum, and the success stories that can lead to optimal networking choices for new IoT / IIoT sensors. We will also delve into ways that Industrial IoT applications rely upon advanced sensors to automate factory and industrial operations, ensuring safety, increasing productivity and providing a wealth of data that enables fast-to-market strategies, cost reduction, waste elimination and continuity between manufacturing centers regardless of their physical proximities.

SPEAKERS

- **Wolfgang Schmitt-Hahn – Bosch Sensortec**
  Beyond smartphones: Ultra-low power and smart CE sensors
- **Barbara Panella – ABB Research**
  IoT sensing technologies enabling digital transformation in industry
- **Rainer Minixhofer – AMS AG**
  AI in Sensors for IoT
- **Martin Eibelhuber, EV Group**
  Wafer Level Fabrication of Micro and Nanostructures for Optical Sensing
- **Thomas Dawidczyk - Lux Research**
  The emergence of new sensing capabilities from commercially available sensors
- **Danny Hughes - VersaSense**
  Selecting the Right IoT Network for Industrial Applications
- **Pim Kat - Technobis**
  Mobile commodity fiber optic sensing devices

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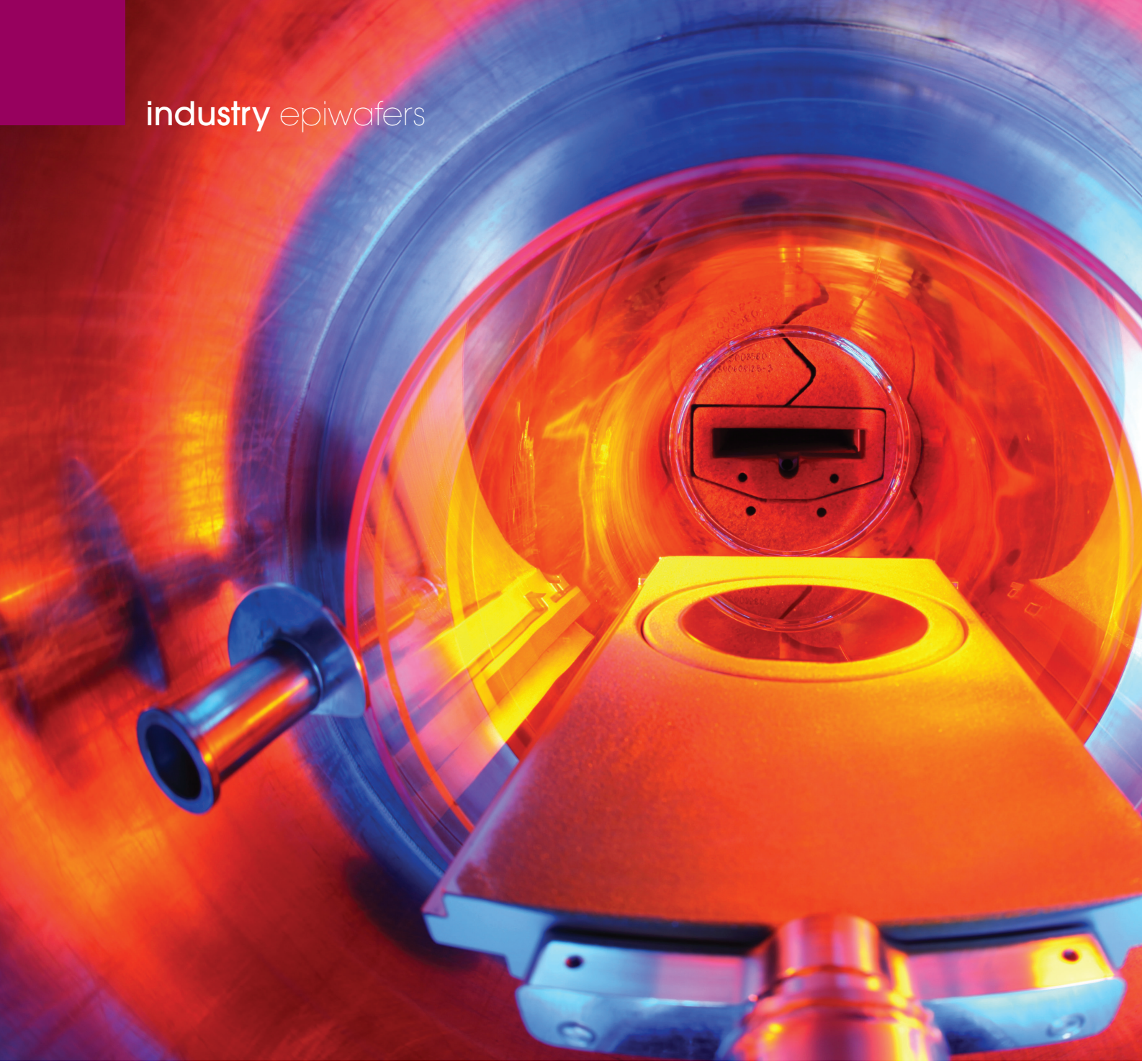
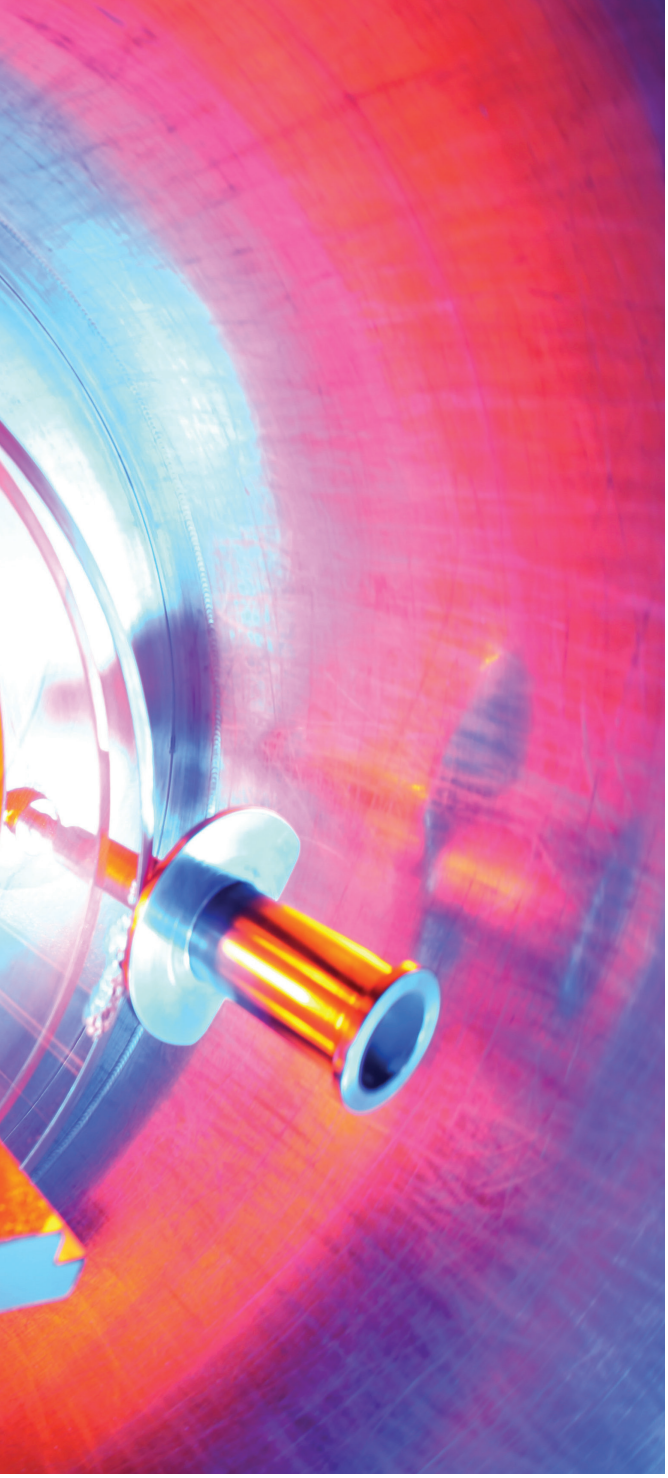


Scrutinising SiC epilayers

Careful control of the growth process limits the carbon vacancies that govern the carrier lifetimes, but some extended defects and point defects in epilayers are determined by the substrate quality

BY BIRGIT KALLINGER FROM FRAUNHOFER IISB



LYING AT THE VERY HEART of every SiC power device is a stack of homoepitaxial layers. Each of them has a carefully selected doping concentration profile and thickness, because this determines the key characteristics of the chip: its blocking capability and its on-resistance.

Unfortunately, these homoepitaxial layers can inherit many forms of extended defects from the substrate, including dislocations and stacking faults, which may hamper device yield and reduce reliability. So how do variations in substrate quality influence the epilayers? And can the substrate quality also influence the point defect concentration, and ultimately the carrier lifetime of homoepitaxial layers and devices?

Working on the answers to these important questions, and related issues, is our team from Fraunhofer IISB, MOCVD manufacturer Aixtron, and Intego, a producer of metrology equipment. Using 100 mm and 150 mm diameter 4H-SiC substrates from a variety of vendors, we have grown SiC epilayers by CVD and scrutinised the resulting material. This work sheds new light on concerns over wafer quality that are common within the SiC industry – many of those that work within it know that there is a specific defect signature for each vendor, associated with the densities and lateral distributions of dislocations and stacking faults.

Extended defects

Common dislocations in SiC substrates include threading edge or screw dislocations, which lie nearly perpendicular to the surface (along the [0001] *c*-axis); and basal plane dislocations, which are orientated almost parallel to the wafer surface on the *c*-plane (compare Figure 1).

During epilayer growth, the threading dislocations in the substrate tend to make their way into the epilayer. Some threading screw dislocations convert to Frank-type stacking faults, and some to stacking fault complexes like carrots and comets. Fortunately, engineers don't have to worry about these threading dislocations in the epilayers, as they are harmless in most forms of power electronic device. Stacking faults, however, are a major concern, as they impair device performance and reliability.

The most notorious defect is the basal plane dislocation. It can propagate into the epilayer, where it is transformed into a Shockley-type stacking fault or a threading edge dislocation. The former is a menace, causing severe degradation in bipolar devices. Due to this, great strides can be made by uncovering the origins of the stacking faults in these epilayers, and devising appropriate ways and means to minimize their presence.

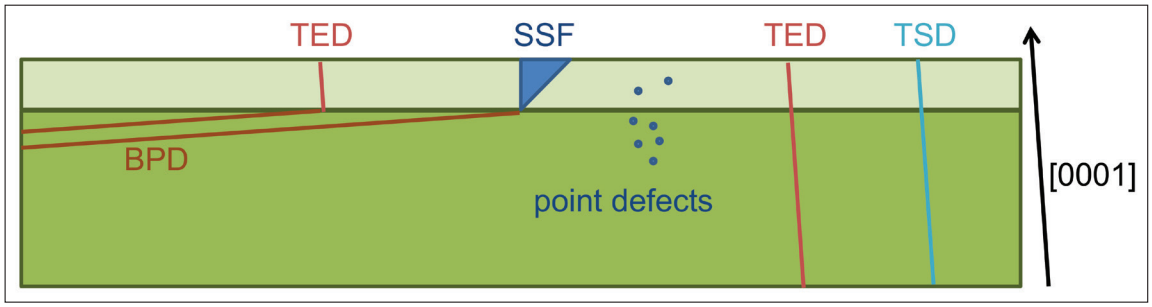


Figure 1. SiC substrates and epiwafers contain many forms of defects, including point defects, stacking faults (Shockley stacking fault, SSF), and various types of dislocations, including: the basal plane dislocation, BPD; the threading edge dislocation, TED; and the threading screw dislocation, TSD

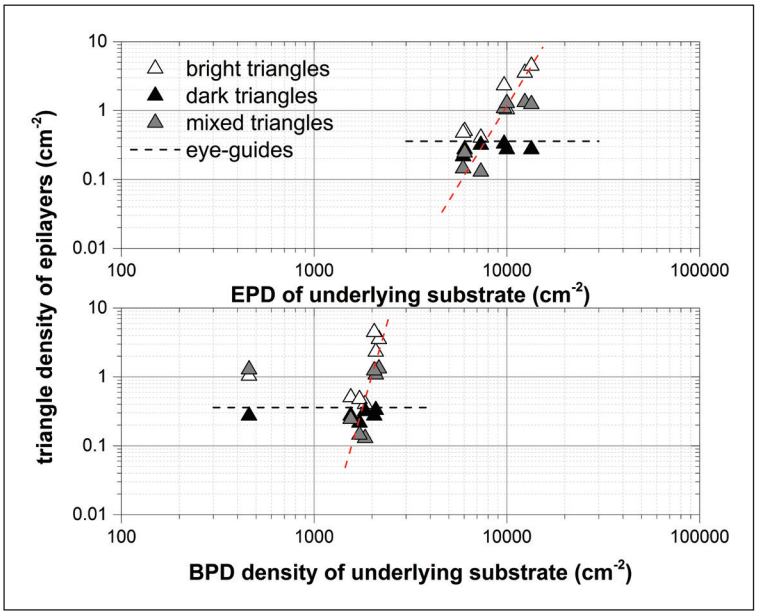


Figure 2. The densities of triangular-shaped stacking faults ("triangles") in 4H-SiC epilayers and the dislocation densities in the underlying substrates. The triangle densities of epilayers were determined with ultraviolet photoluminescence imaging, while the dislocation densities of underlying substrates were interpolated from defect selectively etched reference wafers.

Motivated by this goal, we have recently turned our attention to comparing the density of triangular-shaped stacking faults in epilayers with the density of dislocations in the underlying substrates. To do this, we have exposed these stacking faults with ultra-violet photoluminescence imaging. This technique produces images with darker and brighter triangles than their background, and features triangular defects with both bright and dark regions – so-called mixed triangles. By inspecting these images, we can see that the triangular shape of the stacking faults in the epilayers originates from the off-axis growth and the hexagonal symmetry of 4H-SiC. We have also undertaken defect-selective etching of reference wafers, to determine the dislocation densities of the underlying substrates (see Figure 2).

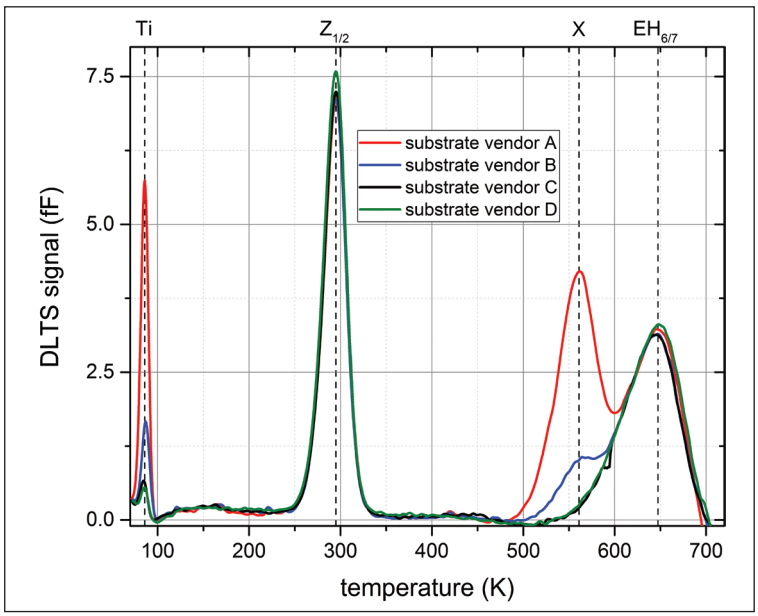


Figure 3. Deep-level transient spectroscopy has been used to probe epilayers grown on substrates from different vendors under identical epigrowth conditions. All the epilayers contain the titanium (Ti) defect and carbon vacancies (represented by $Z_{1/2}$ and $EH_{6/7}$). The X defect occurs only in epilayers grown on substrates from vendors A and B.

The densities of the bright and mixed triangular defects appear to be related to the dislocation density of the substrate. This implies that these triangular defects originate from either basal plane dislocations or threading screw dislocations in the substrate. However, for dark triangles, their density is independent of the dislocation densities in the substrate. That's because the dark triangles originate from ingrown particles, which can be controlled in the epitaxial growth process.

There is still more work to do. Our plan is to undertake a further, more detailed investigation of the densities and the origin of extended defects in epilayers, using a pair of new lab tools: an X-ray topography tool XRT Micron from Rigaku, and an ultra-violet photoluminescence imaging system from Intego, equipped with surface inspection. Armed with the insights these instruments will bring, we aim to identify the critical defects for high-quality, reliable devices. This should lead to guidelines for acceptable defect densities for substrates on one hand and for optimum epitaxial growth parameters on the other hand.

Point defects

When a process engineer dials in the growth temperature, gas flows and pressures, as well as influencing the impact of extended defects, their choices determine the doping concentration and thickness of the epilayers, as well as homogeneities across the wafer.

Using a modern reactor, the Aixtron G5WW, we can produce epilayers with very good doping homogeneities and a wafer-to-wafer reproducibility of less than ± 6 percent. Even more impressive results, however, are realised with Aixtron's AutoSat technology. On 150 mm wafers, this addition reduces the wafer-to-wafer temperature uniformity from ± 3K to just ± 0.5 K. This drops the wafer-to-wafer doping deviation to less than ± 3 percent, which is an excellent result for an 8 x 150 mm production reactor.

The extremely homogeneous, reproducible temperature distribution that occurs in our epitaxial growth chamber enables some of the intrinsic point defects in the epilayers to be controlled very well, as they are generated thermodynamically. Take, for example, the carbon vacancy. It exerts the greatest

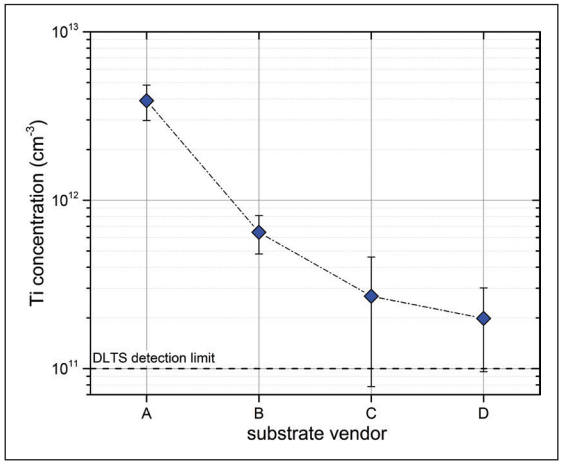


Figure 4. Data obtained from deep-level transient spectroscopy of epitaxial wafers from four growth runs shows that the titanium concentration at the top of the epilayers depends on the vendors of the substrates. Data points represent mean values, while error bars define the minimum and maximum values.

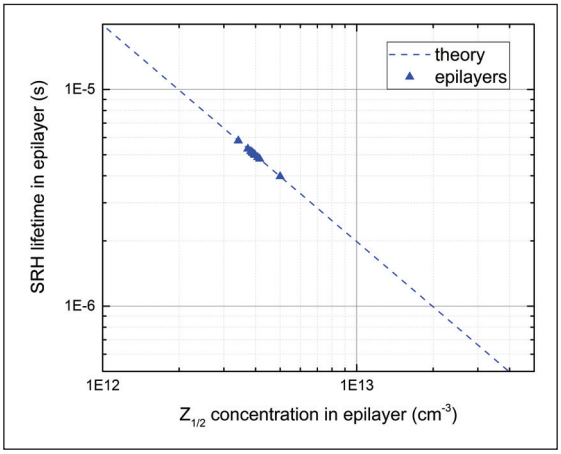


Figure 5. The Shockley-Read-Hall (SRH) lifetime as a function of the carbon vacancy concentration, calculated for microwave-detected photoconductivity decay measurement conditions (line) and individual epilayers. The $Z_{1/2}$ concentration obtained from deep-level transient spectroscopy provides values used for the carbon vacancy concentration.

influence on the carrier lifetime in *n*-type epilayers, and its abundance is determined by two factors: the extent of carbon excess, and the temperature during epitaxial growth.

To gain insight into the point defects in *n*-type epilayers, we have investigated epilayers grown under identical conditions, on substrates from four different vendors. We probe all these layers, grown under conditions that ensure the same temperature, carbon-to-silicon ratio, and doping concentration, using deep-level transient spectroscopy. This technique uncovers four distinct peaks, including two associated with a carbon vacancy.

For the carbon vacancy known as $Z_{1/2}$, the concentration is very reproducible (see Figure 3). It is independent of the substrate used and has a level of 5 x 10^{12} cm^{-3}. Other groups have also studied this vacancy, and their reports indicate that our level is very competitive. Note that we have found that the concentration of the carbon vacancy can be controlled by epitaxial growth conditions.

The titanium defect is present in all epilayers grown under identical growth conditions, but its concentration varies by a factor of 25, from 2 x 10^{11} cm^{-3} to 5 x 10^{12} cm^{-3} (see Figure 4). Its defect level is governed by the make of the substrate.

We have also studied the influence of epigrowth conditions, such as the carbon-to-silicon ratio and the temperature, on the concentration of titanium in epilayers grown on substrates supplied by one vendor. This investigation reveals that the levels of titanium are not related to the conditions during the epigrowth process or the reactor hardware. We are still investigating the mechanism for the transfer of titanium from the substrate to the epilayer.

Deep-level transient spectroscopy also uncovered a defect that is found only in the epilayers grown on substrates provided by two of the four vendors. We are yet to determine the nature and origin of this defect, labelled X, but we plan further investigations.

Carrier lifetimes

Another insight provided by deep level transient spectroscopy is that the concentration of all point defects in the *n*-type epilayers is, compared to the typical doping, lower by two-to-three orders of magnitude. This verifies the high quality associated with the epitaxial growth processes and the hardware.

Point defects influence the carrier lifetime in the epilayers, and can ultimately govern device performance. For example, the carbon vacancy is a known lifetime killer, and its impact on the carrier lifetime can be predicted with Shockley-Read-Hall statistics. With typical growth conditions, the concentration of the carbon vacancy varies from 1 x 10^{12} cm^{-3} to 3 x 10^{13} cm^{-3} — depending on the growth temperature and the carbon supply – and this produces variations in the carrier lifetimes from longer than 10 μs to less than 1 μs (see Figure 5). For our epilayers, the lifetime is about 5 μs, a competitive value.

The most common method for determining carrier lifetime is the microwave-detected photoconductivity decay. This method yields a value for the lifetime that depends on the Shockley-Read-Hall lifetime of the epilayer itself, but also contains contributions related to surface recombination and interface effects between the epilayer and the substrate. The value for this effective lifetime is always less than that for the Shockley-Read-Hall lifetime of the epilayer.

Fraunhofer IISB and its partners in SiC development

FRAUNHOFER IISB is Germany's leading institute for applied research and development of SiC technology. Working with international partners for more than 20 years, IISB offers internationally recognized expertise in terms of SiC services and contract research – starting from materials development and characterization, and on to device manufacturing, module assembly and power electronic systems. IISB operates the π-Fab, a prototyping service which comprises a continuous silicon CMOS and SiC process line in an industry-compatible environment.

Recently, IISB and Aixtron SE have been co-operating closely in the field of SiC epitaxy – running a demonstration lab with two Aixtron G5WW reactors and IISB's sophisticated material characterization. IISB is able to provide a fast feedback loop regarding the epilayer thickness, doping, and defect concentrations (next generation Intego ultra-violet photoluminescence imaging and surface inspection), which is one of the key factors for a successful development of epigrowth processes and hardware. IISB recently started a strategic partnership with Rigaku for beyond state-of-the-art X-ray topography of semiconductor wafers.

Birgit Kallinger is a senior scientist in the materials department of Fraunhofer IISB with about 15 years practical experience in SiC epitaxy and material characterization. She studied comprehensively SiC epitaxial growth and its impact on extended defects, mainly dislocations and stacking faults, in epilayers. In recent years, the focus of her work moved on to the impact of epigrowth parameters on point defects and carrier lifetime. Her work has been published in many research papers and been awarded several times.

We have measured the carrier lifetimes on 16 epiwafers. These are taken from four runs, each containing one substrate from each of the four vendors. The results show significant differences in lifetime, dependent on the source of the substrate (see Figure 6). We are still to uncover the reason for this.

Our efforts show that today's multi-wafer reactors are capable of providing excellent homogeneities and reproducibility with regard to temperature, epiwafer thickness and doping uniformity. This enables engineers to control intrinsic point defects, such as the carbon vacancy. However, the control of some extended defects, or some influences on the effective lifetime are governed by the substrate.

Further reading

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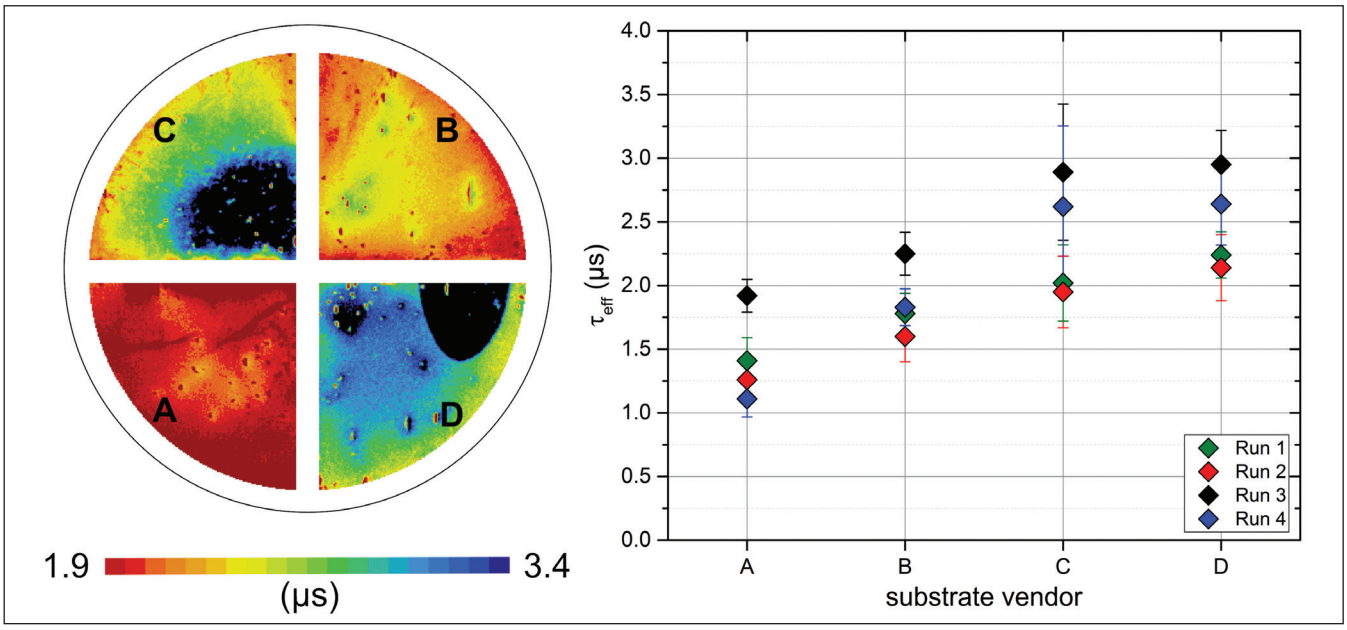

Figure 6. Effective lifetimes of 65 µm-thick, low *n*-doped epilayers obtained from microwave-detected photoconductivity decay. Note in wafer quarter 'D' the presence of extended defects as small regions with a lower lifetime and the wafer facet. Left: exemplary set of wafer quarters. Right: Effective lifetimes of 16 wafer quarters from four epigrowth runs.

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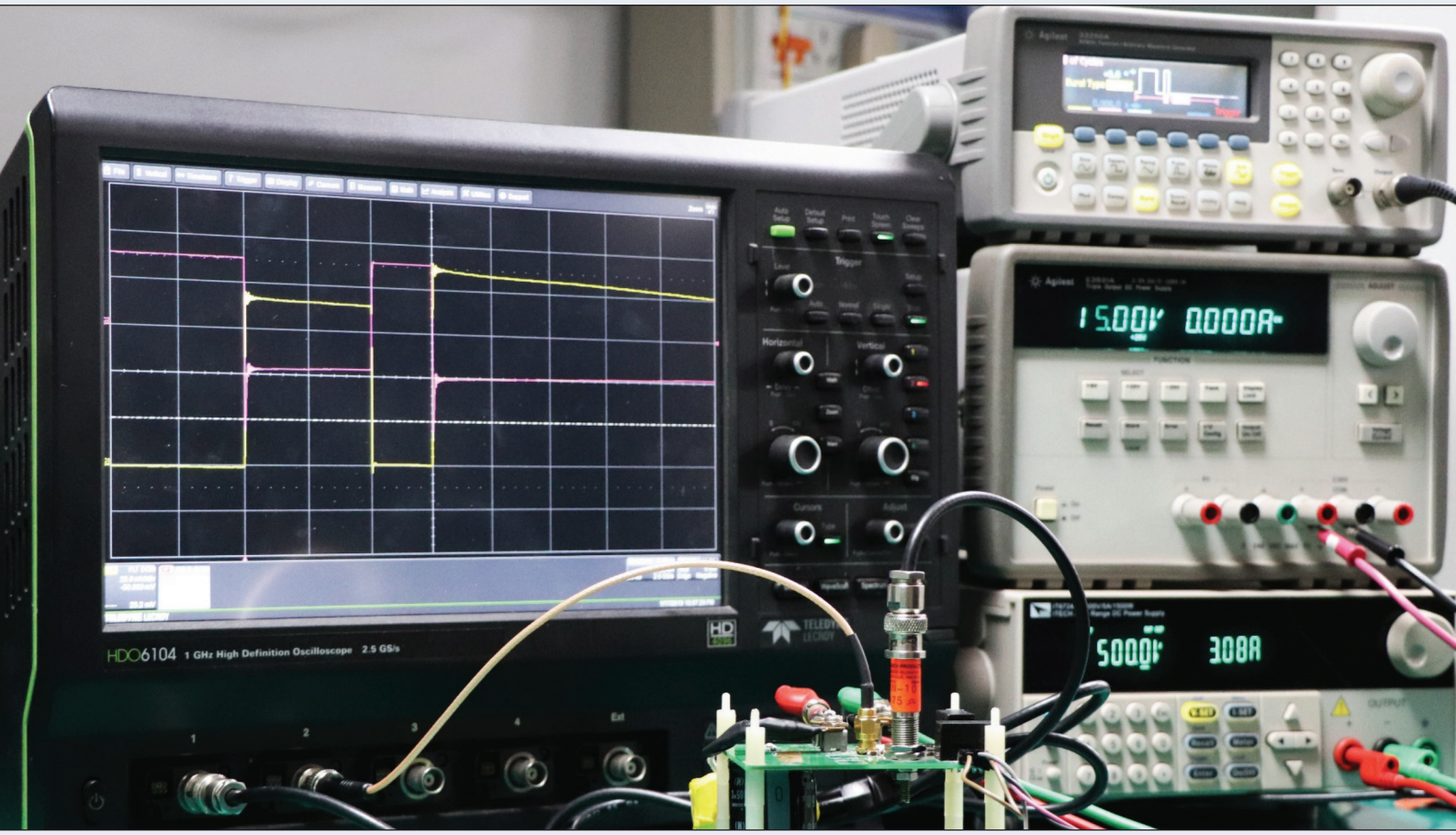

Obliterating dynamic on-resistance degradation

Vertical GaN-on-GaN power devices enable current-collapse-free performance

BY SHU YANG AND SHAOWEN HAN FROM ZHEJIANG UNIVERSITY

GaN IS DESTINED to revolutionise the power electronics industry. Devices that are made from this material can operate at high frequencies while offering low conduction and switching losses – attributes that allow the production of electrical units that combine enhanced energy efficiency with increased power density and a reduction in the size and weight of the system. It is these strengths that enable a hike in the performance of smartphone and laptop chargers, photovoltaic inverters, power supplies for data centres, on-board chargers and charging stations for electric vehicles and hybrids.

The most common form of this class of device is the GaN-on-silicon transistor. It has come on in leaps and bounds over the last decade, and is now driving the commercialisation of this technology.

One of the merits of GaN-on-silicon is the low cost of 150 mm and 200 mm silicon substrates.

But that's not the only reason behind low-cost production: the epiwafers can be processed in fully-depreciated 150 mm and 200 mm silicon fabrication lines.

These GaN-on-silicon devices, however, are usually confronted with a challenge that could cause excess power loss, known as either dynamic on-resistance degradation or current collapse.

Recently, our team at Zhejiang University in China has shown that it is possible to overcome this issue by turning to GaN-on-GaN devices with a vertical architecture and nitridation-based termination.

Trapping issues in GaN-on-silicon

To block high voltages, conventional lateral power devices comprise of a semi-insulating III-nitride buffer stack, located between the GaN channel layer and the silicon substrate. This buffer stack tends to contain a high density of bulk traps, some of which originate from crystalline defects and dislocations due to the lattice and thermal expansion coefficient mismatch between the nitride layers and silicon.

There are also deep-level acceptor traps, resulting from carbon atoms sitting on nitrogen sites. During the growth of epilayers, carbon is intentionally/unintentionally incorporated to compensate for donor-type background impurities, such as silicon and oxygen. This enables the buffer stack to exhibit a high resistivity with a low leakage.

In these lateral devices, the high-density two-dimensional electron gas, which features a high electron mobility, equips the transistor with a low static on-resistance. But when this device is switched from a high-voltage off-state, excess power loss results, due to the ailment known as either current collapse, or an increase in dynamic on-resistance.

Several factors contribute to this degradation (see Figure 1). When this lateral device is operated in its off-state with a high drain bias, the large negative gate-to-drain bias can lead to electron injection and trapping at the polarized III-nitride surface in the gate-to-drain access region. Meanwhile, in the vertical direction, the large positive drain-to-substrate voltage could cause electrons to be injected from the silicon substrate and trapped in the GaN buffer stack.

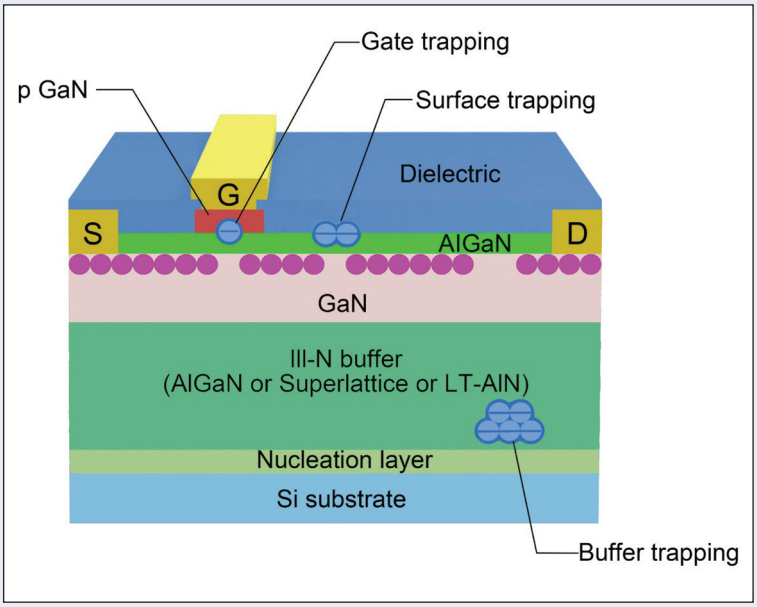

Figure 1. An illustration of trapping-induced current collapse, using a *p*-GaN HEMT as an example.

Another issue is that when this device is running in a high power state, a hard-switching transition can generate hot electrons in the channel. From here, these electrons may then be injected and trapped at either the III-nitride surface or the III-nitride buffer stack. When switching the device on, it may take considerable time to release electrons from surface states and buffer traps. If this happens, the two-dimensional electron gas in the gate-to-drain access region could remain partially depleted, resulting in current collapse and conduction loss.

A third factor at play is that when a lateral *p*-GaN HEMT or insulated-gate GaN power transistor is operated in its on-state with a gate overdrive, trapping

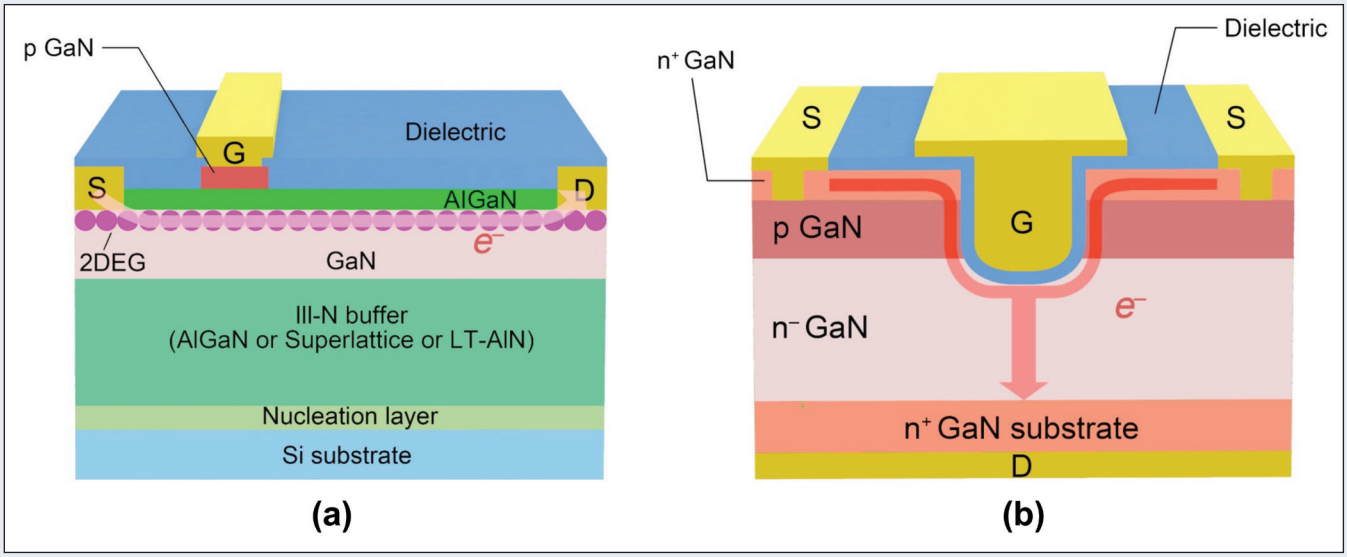

Figure 2. Schematic cross sections of (a) lateral GaN-on-silicon and (b) vertical GaN-on-GaN power devices showing different electron flows.

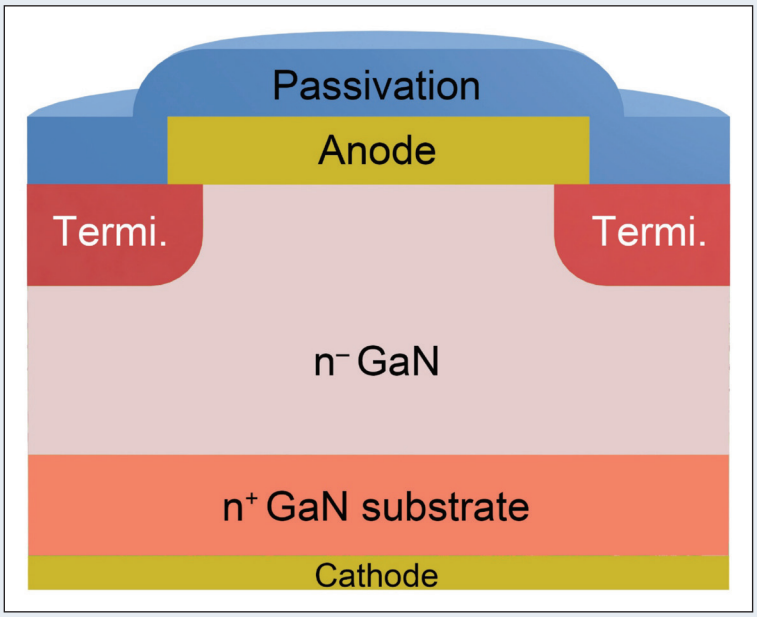

Figure 3. Researchers at Zhejiang University, China, have developed the vertical GaN-on-GaN Schottky barrier diode with nitridation-based termination.

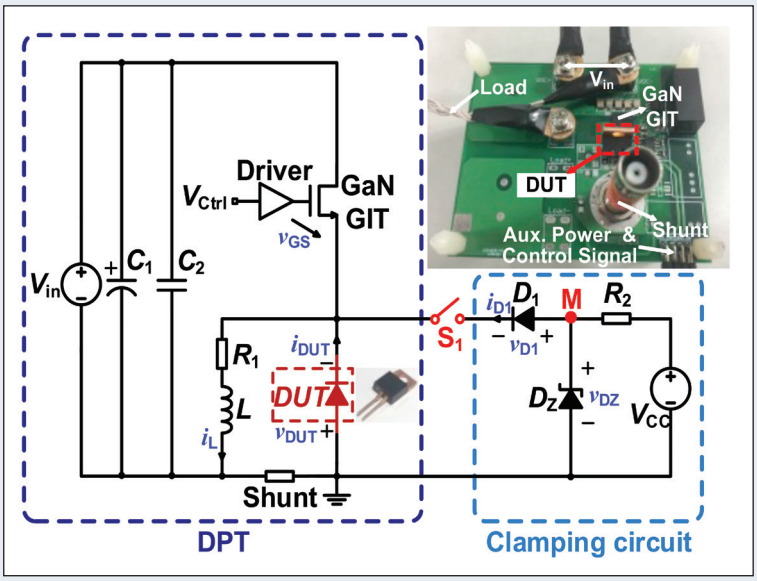

Figure 4. The team at Zhejiang University has developed a high-speed double pulse tester with a clamping circuit to provide quantitative, precise extraction of dynamic on-resistance, R_{ON}, in GaN devices.

can occur in the interface and border region beneath the gate electrode. A positive shift in threshold voltage could result, creating a reduced gate overdrive at a pre-set on-state gate bias and an increase in the on-resistance.

To combat all these issues, researchers have developed multiple field plates, advanced dielectric passivation, buffer stack optimization and hybrid drain techniques for mitigating trapping effects. Despite the effectiveness of these approaches to some extent, it's relatively difficult to completely eliminate the root cause for trapping effects, and current collapse is still regarded as one of the biggest challenges for lateral GaN-on-silicon power devices.

From lateral to vertical

The recent emergence of high-quality, free-standing GaN substrates has opened the door to the development of vertical GaN-on-GaN power devices. Merits of growth on a native substrate include the elimination of lattice- and thermal-mismatch between the epitaxial layer and the substrate, making it possible to produce thicker GaN drift layers with a lower dislocation density. This architecture also trims thermal resistance, thanks to the removal of a thermal boundary resistance in the nucleation layer between the III-nitride buffer and the silicon substrate (see Figure 2). Armed with all these attributes, the vertical GaN-on-GaN power devices can deliver high current capacity, a high breakdown voltage, more efficient chip area utilization, and superior thermal performance.

A significant challenge for high-voltage vertical power devices is to address electric field crowding at the junction edge. Left unchecked, this crowding can result in excess reverse leakage and premature breakdown. The conventional approach to suppressing edge-effect-induced reverse leakage and enhancing breakdown voltage is to apply edge termination techniques. However, in GaN devices, it is not easy to implement junction-based edge termination techniques, such as junction termination extension and field-limiting rings, due to the low-efficiency of selective *p*-type doping and activation.

To address this issue, we have recently developed a nitridation-based termination technique that is well suited to vertical GaN devices (see Figure 3). We form the nitridation-based termination structure by applying a low-damage nitrogen plasma treatment to the periphery of the device area with an optimal RF power and time.

According to experiment, this approach shifts the Fermi-level in the nitridation-based termination region towards the valence band. This shift is most likely to result from a favourable modification of the surface conditions, such as the enhanced adsorption of nitrogen atoms and passivation of gallium dangling bonds.

One of the benefits of applying nitridation-based termination around the device periphery is that it produces an enlarged energy barrier height and/or effective barrier thickness at the junction edge. In turn, this suppresses electron transport via thermionic field emission or tunnelling, and ultimately slashes reverse leakage by four orders of magnitude while enhancing breakdown voltage – the later increases to around

All of these tests demonstrate that our vertical GaN-on-GaN power rectifier is free from dynamic on-resistance degradation just 200 ns after switching from a high-voltage off-state, outperforming the state-of-the-art lateral GaN-on-silicon devices

1 kV. In addition to these benefits, our vertical GaN-on-GaN diode exhibits a nearly ideal Schottky contact, an on-resistance of 1.2 mΩ·cm², and an on/off current ratio of 13 orders of magnitude.

Testing challenges

There are a lack of reports providing quantitative, systematic characterisation of the dynamic on-resistance of vertical GaN devices. To gain insight into the dynamic on-resistance, some researchers have undertaken on-wafer pulsed current-voltage measurements. However, such wafer-level test tends to exhibit a relatively long measurement delay, due to parasitics in the commutation loop. This delay allows time-dependent recovery – or de-trapping – to occur, threatening an underestimation of the trapping effects, alongside inaccurate evaluation of the dynamic on-resistance.

One way to overcome this limitation is to use a custom-designed board-level test that is capable of capturing fast transients on a sub-microsecond timescale. Note that an accurate assessment of the dynamic on-resistance on a timescale of hundreds of nanoseconds is of particular interest and importance to GaN devices, as they are expected to switch at frequencies of more than a megahertz.

We have developed a double pulse test circuit with an optimized layout and minimised parasitics to obtain an accurate assessment of the dynamic on-resistance (see Figure 4). In this set-up, the device under test, the vertical GaN Schottky barrier diode, acts as a freewheeling diode, while a commercial 600 V, GaN HEMT serves as the control switch.

This configuration provides an accurate, precise extraction of dynamic on-resistance. Thanks to the diode-based clamping circuit, a precise measurement of the low on-state voltage after switching from a high-voltage off-state can be provided. Because of the ultrashort delay of 200 ns in the high-speed test board, the possible trap recovery during measurement can be minimised such that dynamic on-resistance can be accurately extracted.

To evaluate the benefit of our device, we wish to compare its performance to that of a state-of-the-art lateral GaN-on-silicon device. A commercial, lateral GaN-on-silicon diode is not currently available. But we can make a comparison with state-of-the-art E-mode GaN-on-silicon transistors, by electrically shorting the gate and source terminals. With this modification – enabling the transistor to operate as a power diode when operating in the reverse conduction mode –

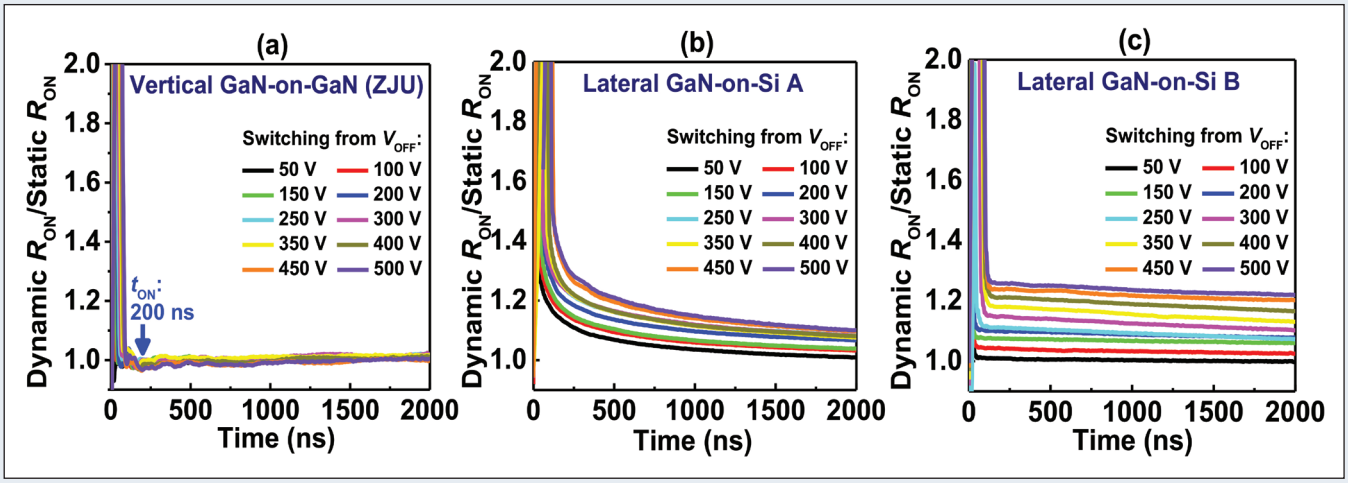

Figure 5. Time-resolved dynamic R_{ON}/static R_{ON} of: (a) a vertical GaN-on-GaN Schottky barrier diode developed by Zhejiang University; (b) a commercial lateral GaN-on-silicon device A; and (c) a commercial lateral GaN-on-silicon device B with off-state bias (V_{OFF}) varying from 50 to 500 V.

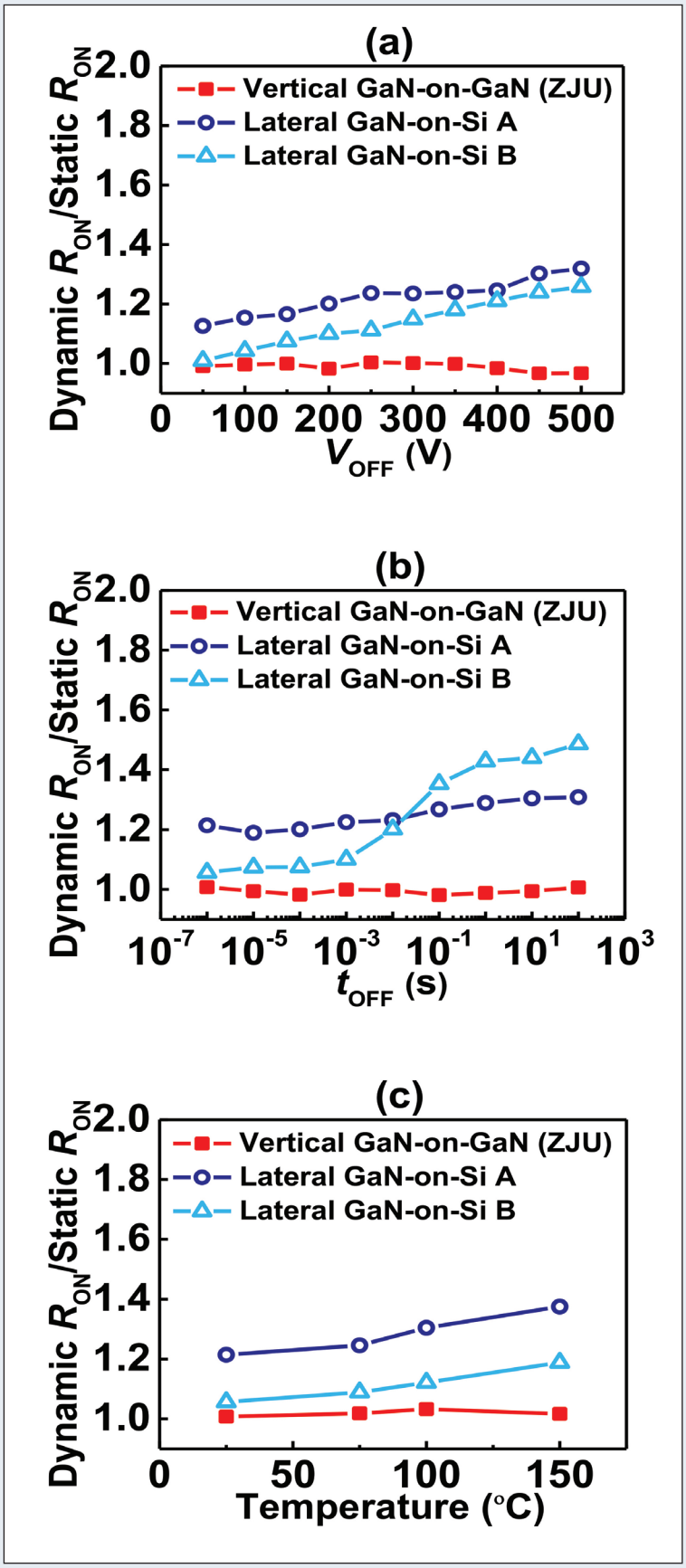

Figure 6. Dynamic R_{ON} of the three types of GaN devices extracted at only 200 ns after switching from: (a) varying off-state bias (V_{OFF}) up to 500 V, (b) t_{OFF} of 10^{-6}~10^{2} s and (c) high temperature up to 150 °C.

any surface- or buffer-trapping that will impair on the conductivity of the two-dimensional electron gas leads to a change in dynamic on-resistance.

Current-collapse-free performance

We have systematically and quantitatively evaluated the dynamic on-resistance under different switching conditions. Tests include: an off-state stress bias evaluation up to 500 V; an off-state stress time, over the range 10^{-6} s to 10^{2} s; and elevated temperatures of up to 150 °C. The higher off-voltages and longer off-state times in the tests could impose more severe stress on devices by inducing field-enhanced electron injection and accumulated charge trapping.

All of these tests demonstrate that our vertical GaN-on-GaN power rectifier is free from dynamic on-resistance degradation just 200 ns after switching from a high-voltage off-state, outperforming the state-of-the-art lateral GaN-on-silicon devices (see Figure 5 and 6).

This result is significant – it is the first time that there has been quantitative experimental verification that vertical GaN-on-GaN devices are capable of delivering a current-collapse-free performance and overcoming the grand challenge of dynamic on-resistance.

We attribute this superior dynamic performance to several strengths of the device. Firstly, as current flow is along the vertical direction, the diodes are inherently less susceptible to surface-trapping than cousins with a lateral architecture. In addition, there is minimal bulk trapping, thanks to the high crystalline quality in the homoepitaxial epilayers and the well-controlled background/compensation doping in the drift layer; and our nitridation-based termination technique can suppress edge leakage and enhance breakdown voltage through a favourable surface modification, rather than creating deep-level traps which could adversely influence the dynamic performance.

All these merits have helped our GaN-on-GaN devices to obliterate dynamic on-resistance degradation, a breakthrough that equips them with the potential to deliver high-efficiency and high-frequency energy conversion.

Further reading

S. Han *et al*. "Current-collapse-free and fast reverse recovery performance in vertical GaN-on-GaN Schottky barrier diode," IEEE Transactions on Power Electronics, early access, DOI: 10.1109/TPEL.2018.2876444.

S. Han *et al*. IEEE Electron Device Letters **39** 572 (2018)

S. Yang *et al*. IEEE Transactions on Electron Devices **64** 5048 (2017)

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Understanding limitations in deep UV LEDs

Experiments expose a decline in carrier-injection efficiency as a major barrier to high-performance, deep UV LEDs

RESEARCHERS at TU Berlin have identified a fall in carrier-injection efficiency as a significant contributor to the decline in efficiency of the deep UV LED as its emission is stretched to shorter wavelengths.

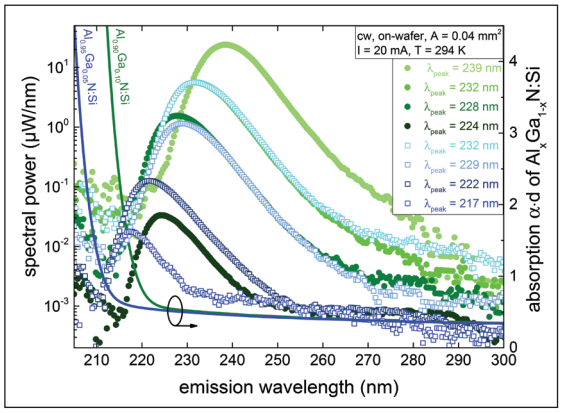
The team's insight promises to aid attempts to increase the optical efficiency of these emitters, which are used for medical diagnostics and the sensing of gases such as nitrogen monoxide.

Over the years, much effort has been devoted to understanding the limitations of UV LEDs. It is now well established that the resistivity of the silicon-doped AlGaN current-spreading layer exponentially increases with aluminium mole fraction, driving up the operating voltage of the device and reducing its efficiency. It is also common knowledge that the absorption edge of AlGaN shifts to a shorter wavelength as the aluminium mole fraction increases.

However, according to Frank Mehnke, spokesman for the team at TU Berlin, up until now there has been no comprehensive study on the interplay of the aluminium mole fraction of the silicon-doped AlGaN current-spreading layer and the spectral emission power and the operating voltage of the deep UV LEDs.

Mehnke and his co-workers have addressed this with a series of experiments on deep UV LEDs with emission wavelengths between 239 nm and 217 nm. These efforts uncovered reduced carrier injection efficiency as the root-cause for the decline in emission power with shortening wavelength.

This carrier injection efficiency is a measure of the proportion of electrons and holes that reach the active region. Injection efficiency is compromised when a significant number of electrons are not stopped by the electron-blocking layer, but traverse into the *p*-side of the LED, where they recombine with holes.



There is a dramatic fall in the efficiency of LEDs with decreasing wavelength. Increases in absorption can contribute to this, along with declines in injection efficiency and light extraction efficiency.

"The main problem for short-emission-wavelength devices is the material limitation of the AlGaN material system," says Mehnke, who points out that the bandgap of the electron-blocking layer cannot be extended beyond the bandgap of AlN.

Since the energy of the electron-blocking layer is fixed, cranking up the aluminium content in the active region to reach a shorter emission wavelength leads to a hike in the electron-leakage and a fall in injection-efficiency.

To investigate the performance of UV LEDs with different emission wavelengths and current-spreading layers, the team produced a portfolio of devices on AlN-on-sapphire templates. On this they added epistructures that included 1.2 μm-thick current-spreading layers with compositions ranging from $Al_{0.79}Ga_{0.21}N$ to $Al_{0.95}Ga_{0.05}N$, and an active region with three 1 nm-thick wells separated by 5 nm-thick barriers.

The team's measurements included plots of spectral power as a function of emission wavelength (see figure).

A sub-set of the devices produced by the team are not influenced by absorption. By looking at the results from just these LEDs, the researchers restricted the causes behind the reduction in device efficiency at shorter wavelengths to a decline in internal quantum efficiency, a decline in light extraction efficiency, and a decline in carrier injection efficiency.

Mehnke and co-workers argue that the internal quantum efficiency is not the primary culprit, as it is highly unlikely to fall by over three orders of magnitude between 239 nm and 217 nm. Changes in light extraction efficiency can also be ruled out as the dominant cause, as ray tracing suggests that over this spectral range this will only decline from 2.9 percent to 1.7 percent. So, by deduction, a plummeting carrier injection efficiency must be to the leading loss mechanism.

The team are currently working on increasing the conductivity of aluminium-rich current spreading layers. After this they plan to improve the *p*-side of the LEDs, and the device's carrier injection efficiency.

Reference

F. Mehnke *et al.* Appl. Phys Express **12** 012008 (2019)

Assessing the optimal GaN HEMT

For great gate controllability and operation stability, make and anneal GaN MISHEMTs

THE ROLL-OUT of 5G infrastructure will be aided by an increase in the output power and operational stability of the GaN HEMT.

To assess the true potential of this transistor, researchers at Hokkaido University and Nagoya University, Japan, have measured the characteristics of devices sporting what is considered to be the ultimate architecture. The team's focus has been gate controllability and operation stability.

One of the hallmarks of the researchers' devices is its foundation, the native GaN substrate. This platform, which leads to a low threading dislocation density, has been reported to trim leakage currents in Schottky gate structures and current collapse in GaN HEMTs.

The other key feature is the metal-insulator-semiconductor (MIS) structure. This addresses an important issue impairing the more common GaN HEMTs with a Schottky gate: reduced gain and efficiency with increasing input RF power.

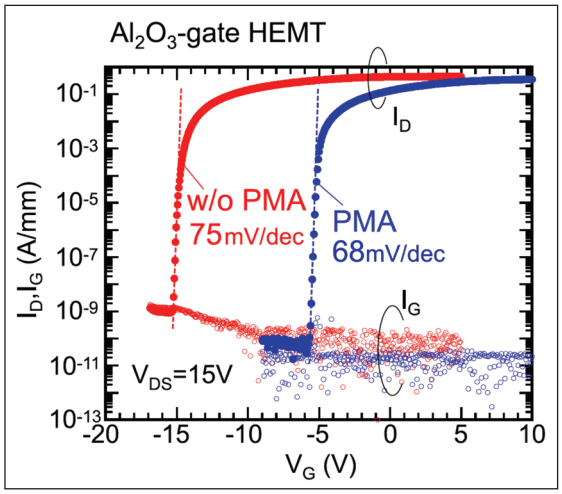
The team produced devices by loading GaN substrates into an MOCVD chamber, and depositing: a 900 nm-thick layer of carbon-doped GaN that acts as a high-resistivity layer; a 600 nm-thick layer of undoped GaN; and finally, a 20 nm-thick layer of $Al_{0.2}Ga_{0.8}N$.

Source and drain electrodes were formed on the epistructure by depositing a stack of titanium and aluminium layers, and annealing this sample under nitrogen for 1 minute at 830 °C. To protect the AlGaN surface during the annealing step, the team applied a 20 nm-thick film of SiN, and subsequently removed it with a buffered HF solution.

Fabrication of the HEMT finished with the addition of a 30 nm-thick Al_2O_3 film by atomic layer deposition, and the addition of a gate electrode to create a transistor with a 10 μm gate length, a 100 μm gate width, and gate-drain and gate-source distances of 10 μm.

The team went on to anneal some of the samples at 300 °C, before comparing their performance with those that had not been subjected to this step.

Both types of device exhibit relatively good current-voltage behaviour at a negative gate bias. Increase bias beyond 0 V, and drain current is limited in the unannealed device. However, for the annealed cousin, good gate control of the drain current is maintained at forward bias.



The sub-threshold transfer characteristics of the GaN MISHEMT improves with post-metallisation annealing (PMA).

According to the team, this difference in behaviour is probably due to a reduction in the interface states in the gate-drain and gate-source access regions during the annealing process. This could lead to a change in the surface potential of AlGaN, and in turn a slight increase in the density of the two-dimensional electron gas, reducing the access resistance to the device.

Transfer characteristics also benefit from annealing, which produces an increase in current linearity, particularly at forward bias, resulting in a broader plateau of transconductance. The maximum drain current also increases. These improvements should aid RF power HEMTs, by improving the input dynamic range at forward bias.

The researchers have also investigated the sub-threshold characteristics of their MIS-HEMTs (see figure). Before annealing, the sub-threshold slope is 75 mV dec^{-1}, a value lower than that for equivalents formed on sapphire. With annealing, the sub-threshold slope drops to a near-record 68 mV dec^{-1}, despite the relatively thick insulating layer. Again, the benefit of annealing is attributed to a reduction in interface states.

Annealing also led to encouraging transfer characteristics at elevated temperatures. Operating at 150 °C, the sub-threshold curve of the HEMT is said to be "excellent", with a drift in threshold voltage from its room-temperature value of just 0.25 V.

Reference

Y. Ando *et al*. Appl. Phys. Express **12** 024002 (2019)

GaSb laser combines power with spectral purity

Chromium gratings create lasers with a 40 mW single-mode output and a ground-breaking side-mode suppression ratio

RESEARCHERS at the Chinese Academy of Sciences, Beijing, are claiming to have significantly increased the output power of high-spectral-purity GaSb lasers emitting at around 2 μm.

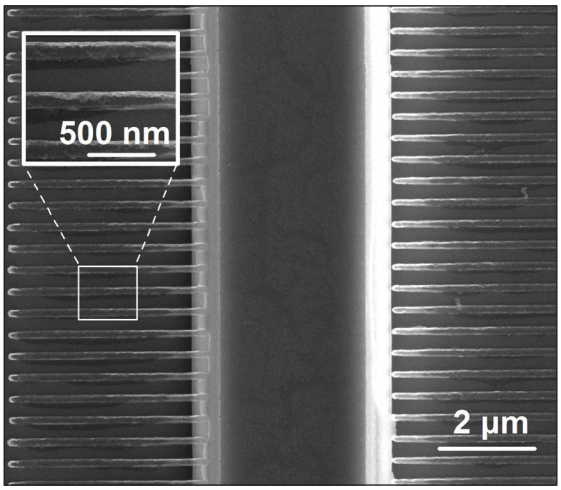
The team's lasers, which emit up three-to-four times the power of their predecessors, are also claimed to break new ground for the side-mode suppression ratio. For the latest devices, this figure can reach 53 dB.

Combining the powerful output with a high spectral purity makes these lasers an attractive candidate for the light source in LIDAR systems fitted to satellites and used to monitor greenhouse gases. Today, the power requirements for this application are most often met by pairing an optically pumped, single-frequency seed laser with an optical amplifier.

"By replacing the solid-state seed laser with a single-frequency semiconductor laser, the transmitter architectures can be greatly improved in volume and weight," argue teams spokesman Zhi-Chuan Niu.

The spectral range at around 2 μm can also be reached with InP lasers. However, single-mode operation, which is required for gas sensing, is only possible for powers up to 10 mW.

GaSb lasers are preferred, because they can deliver a far higher single-mode output power at these wavelengths. According to work published in 2012 from the Jet Propulsion Laboratory, a maximum output of 80 mW is possible at -10 °C with an index-coupled, laterally coupled distributed-feedback laser. However, when operating at peak power, the side-mode suppression ratio from this device can fall to just 20 dB.



A top view of the laterally coupled, distributed-feedback laser produced by the team from the Chinese Academy of Sciences, Beijing. This device features a metallic grating, and combines a high output power with a high side-mode suppression ratio.

To address this weakness while maintaining a high output power, Niu and co-workers have turned to a laterally coupled, distributed-feedback laser featuring a metallic grating.

This architecture has many merits. By carefully selecting the dimensions of the grating, emission can be tuned to coincide with an absorption line of a particular gas molecule – for example, for carbon dioxide, the target is 2.05 μm. What's more, the addition of the grating increases the side-mode suppression ratio, by extenuating the difference between the gain of the primary laser mode and the loss of the adjacent modes.

The team produces its laser by loading an *n*-type GaSb substrate into an MBE chamber and growing an epistructure, which includes waveguide and cladding layers and a pair of 9 nm-thick $In_{0.22}Ga_{0.78}As_{0.1}Sb_{0.9}$ quantum wells.

Contact lithography and etching to a depth of 1.65 μm creates a ridge-waveguide, before a 50 nm-thick layer of Si_3N_4 is added, to provide insulation between the epitaxial layer and the second-order, chromium-based gratings, which are formed with a lift-off process.

Measurements on 1 mm-long chips, mounted up-side down and without facet coatings, reveal a peak output power of up to 40 mW at 10°C. This falls to 24 mW at 50 °C. Threshold current for the GaSb laser is just 26.7 mA, while power conversion efficiency reaches 8.1 percent per facet and slope efficiency can hit 0.15 W/A.

According to Niu, the goals for the future are: to optimise the device for laser stability and reliability; to introduce cavity coatings, a move that should increase output power and improve single-mode operation; and to integrate these lasers with laser arrays and power amplifiers, such as master-oscillator power amplifiers.

Reference

C.-A. Yang *et. al*. Appl. Phys. Lett. **114** 021102 (2019)

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To find out more, contact:

Stephen Whitehurst
CEO
stephen.whitehurst@angelbc.com
T:+44 (0) 2476 718970

Jackie Cannon
Publisher
jackie.cannon@angelbc.com
T: +44 (0) 1923 690200

Adam Richardson
Marketing Manager
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