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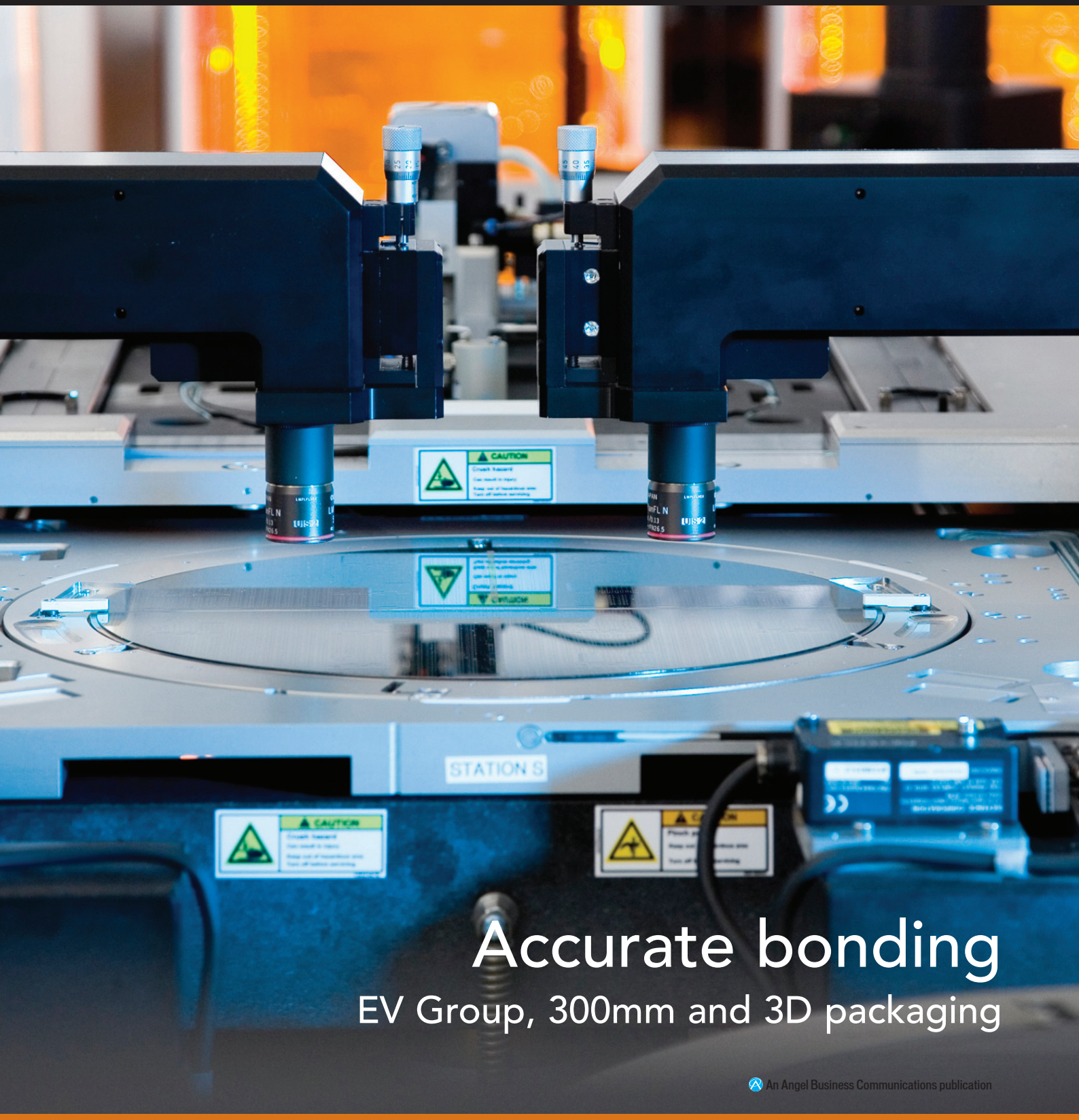

Accurate bonding

EV Group, 300mm and 3D packaging

An Angel Business Communications publication

450mm economics

The state of the industry

Growth returns

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editor's word

Editor-in-Chief David Ridsdale
+44 (0)1923 690210 dr@angelbcl.co.uk

Director of SOLAR & IC Publishing
Jackie Cannon
+44 (0)1923 690205 jc@angelbcl.co.uk

Account Managers
Shehzad Munshi
+44 (0)1923 690215 sm@angelbcl.co.uk
Tommy Beazley
+44 (0)1923 690222 tb@angelbcl.co.uk

Director of Logistics
Sharon Cowley
+44 (0)1923 690200 sc@angelbcl.co.uk

Design & Production Manager
Mitchell Gaynor
+44 (0)1923 690214 mg@angelbcl.co.uk

Subscriptions Manager
Debbie Higham
+44 (0)1923 690220 dh@angelbcl.co.uk

USA Representatives:
Tom Brun, Tom Brun Media,
T: 724 539-2404, E: tbrun@brunmedia.com
Janice Jenkins, Tom Brun Media.
T: 724 929-3550, E: jjenkins@brunmedia.com
Japan Representative:
Katsuhiro Ishii, ACE MEDIA SERVICE INC.,
T: 81-3-5691-3335, E: amskatsu@dream.com
China Representative:
Parker XU, Unionbandy Limited,
T: 86-755-83753881, E: xp@unionbandy.net

Directors:
Bill Dunlop Uprichard – CEO
Stephen Whitehurst – COO
Jan Smoothy – CFO
Haroon Malik, Jackie Cannon, Scott Adams,
Sharon Cowley, Sukhi Bhadal

Published by
Angel Business Communications Ltd Hannay House,
39 Clarendon Road, Watford, Herts WD17 1JA, UK
T: +44 (0)1923 690200
F: +44 (0)1923 690201
E: euroasia@angelbcl.co.uk

Angel Business Communications Ltd
Unit 6, Bow Court, Fletchworth Gate, Burnsall Road,
Coventry CV5 6SP
T: +44 (0)2476 718 970
F: +44 (0)2476 718 971
E: info@angelbc.co.uk

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Growth returns

There has been a recent flurry of excitement as analysts predictions for the rate of growth of the global semiconductor industry are constantly being revised to heady numbers not seen in the industry for a number of years. There is also the psychological impact of the overall industry output finally catching up with the previous industry zenith.

However exciting this data has been it would be premature for observers to start to believe that the industry is back to full power or that the figures are representative of what has occurred in the past. Especially the rapid growth and drastic falls around the turn of the millennium. While the focus remains on short term financial outputs of quarters and year on year comparisons it is extremely difficult to read the industry temperature as these statistics only tell you how deep the hole you are coming out of.

The figures are also misleading in terms of company or segment success as the raw data only concerns the output of IC devices rather than the profits of companies, many of whom are still trying to recoup research costs for the move to 300mm fabrication. Some segments are definitely returning to form on the back of expected consumer interest in mobile devices and gaming but only if impacted by these segments. Of course the analyst predictions that are based on many market assumptions, including the idea that the recent financial turmoil has been fixed with the band-aid of cash thrown to the cause of the problem. The amount of profit cited by financial institutions in the last couple of weeks suggests lessons are to be learned.

Another key factor to continues success will be the industry's ability to provide the ICs that will be required for this massive expected growth throughout the consumer electronic world. The semiconductor industry has a bad history in dealing with inventories around the cyclical changes and although evidence suggests it is improving I think that is more to do with the reduced number of players than clever management. Nissan has already pointed fingers towards IC manufacturing as the reason for their recent shutdown of manufacturing facilities.

So while it is true that growth has returned and will continue to develop for the electronic's industry, only time will tell if a semiconductor industry with less players and more risk will be able to respond to the market changes we will see over the next 24 months.

David Ridsdale
Editor-in-Chief

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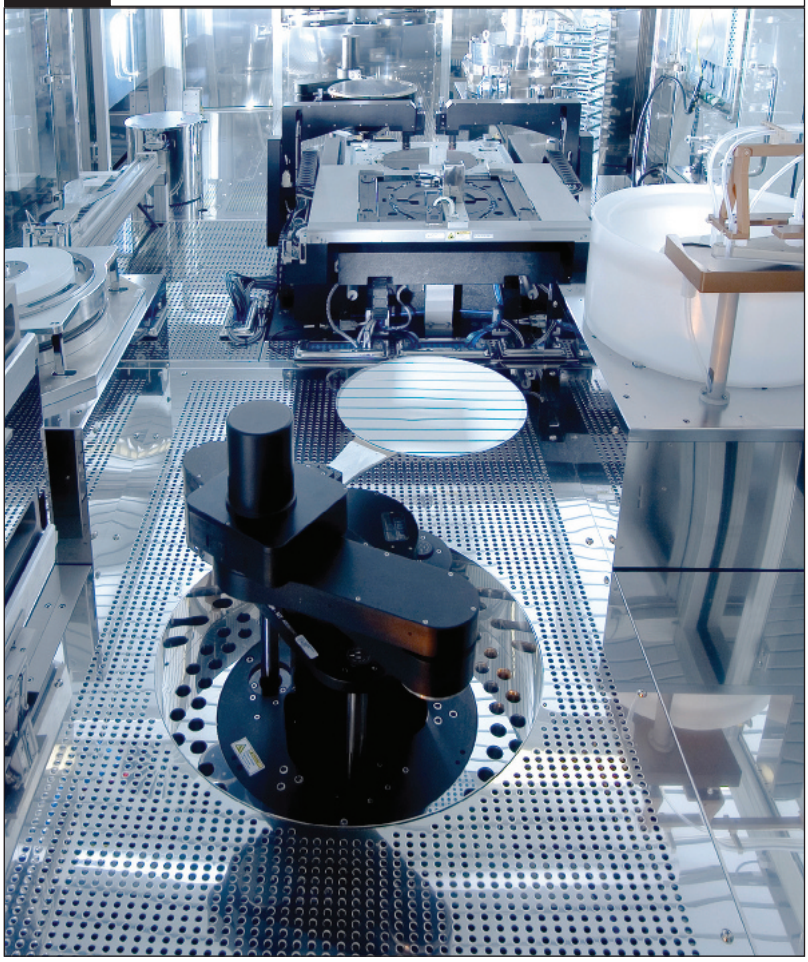

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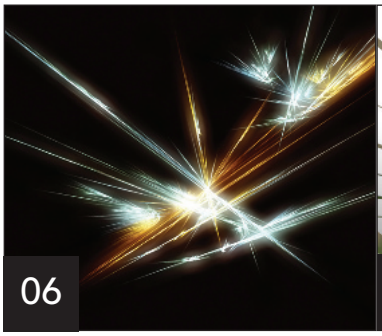
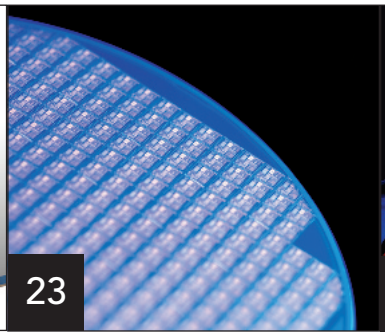
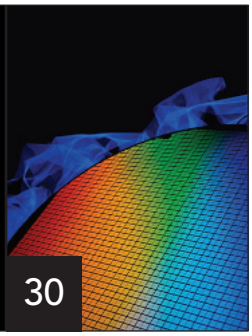


Double patterned

State of the industry



Power supply efficiency



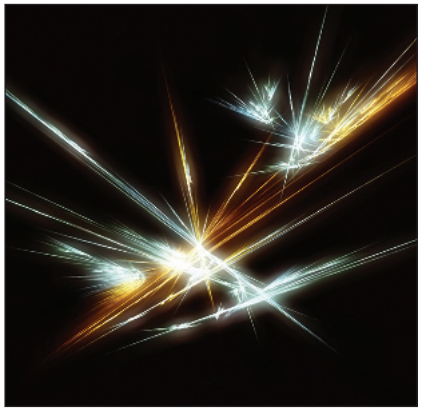
The chips are back

Double patterned mask

SEMATECH and the Semiconductor Metrology Systems (SMS) division from Carl Zeiss announced that Zeiss' photomask registration and overlay metrology system has successfully passed a key development milestone. The jointly developed system, called PROVE, demonstrated measurement capability for advanced photomasks for the 32 nm node and below. In a series of test runs, the key specifications, 0.5 nm repeatability and 1.0 nm accuracy in image placement, registration and overlay measurement, were verified.

"The mask pattern placement metrology tool project builds upon an already successful partnership between Carl Zeiss SMS and SEMATECH for past work on mask Aerial Image Metrology Systems (AIMS) tool platforms. The partnership has resulted in a working metrology tool that is meeting specifications for repeatability, reproducibility, and accuracy at the 32 nm half-pitch node," said Bryan Rice, director of lithography at SEMATECH.

The performance targets of the tool were driven by the requirements for advanced memory and double exposure/double patterning mask pattern placement and overlay that will



help extend 193nm lithography according to the ITRS.

"To achieve the performance specification of the PROVE system is a major milestone in the project and crucial for our customers in the mask making industry. The system is based on a completely new developed platform enabling in-die and sub-nanometer pattern placement metrology in a most versatile way. The measurements can be done on arbitrary production features in the active area of the photomask for accurate and cost efficient metrology and is extendable to EUV technology," said Dr. Oliver Kienzle, Managing Director of Carl Zeiss SMS. "We will now roll-out the PROVE product with deliveries to our customers."

This technology represents a significant improvement over previous capability due primarily to the incorporation of high-resolution 193nm wavelength imaging optics, a flexible illuminator that maximizes image contrast, a highly versatile in-die registration analysis algorithm, and a state-of-the-art metrology platform. The system can be fully extended to measure EUV photomasks. The tool will play a vital role in enabling next generation mask-making technology.

SEMATECH's Lithography Program is leading the industry in providing critical information about and solutions to current and emerging lithography systems. Carl Zeiss was chosen to develop the system in April 2007 by an evaluation team of mask makers and SEMATECH member companies. Carl Zeiss' proposal included a novel design allowing mask manufacturers to measure position deviation of photomask features with high precision and accuracy. Since that time Carl Zeiss and SEMATECH engineers have partnered to develop the concept into a working metrology tool.

Silicon photonics research

10 EUROPEAN R&D project consortia focusing on silicon photonics will coordinate their efforts to facilitate the transfer of knowledge and technology and strengthen the European electronics industry's ability to compete globally. Under the umbrella of the European Silicon Photonics Cluster, the 10 main projects will coordinate efforts to:

- Raise awareness of the potential of silicon photonics among chip foundries, end-users, start-ups and other companies
- Broadly disseminate the results of their projects
- Train young scientists, engineers and researchers in this emerging field

Silicon photonics, which uses CMOS techniques to integrate optics technology onto chips, can substantially lower the cost, size and power consumption compared to existing photonics technologies, while improving device performance.

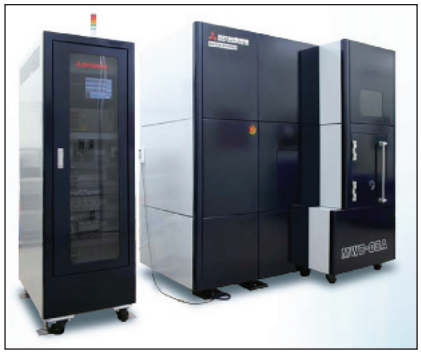
CMOS photonics may lead to low-cost solutions for a number of applications, including optical communications, optical interconnects between semiconductor chips and circuit boards, optical signal processing, optical sensing, and biological applications. It is considered to be the only viable technology to meet the cost and volume demand of such markets.

In addition to submitting articles to industry publications, cluster members will organize a silicon photonics workshop for the industry in 2011 and

cooperate on training programs.

The European Silicon Photonics Cluster represents more than 30M€ (36M$) in investment by the EU and European countries. In establishing the cluster, the members agree that it is of strategic importance to maintain photonic chip design and chip integration functions in Europe to improve Europe's ability to compete on a global stage.

MHI Bond SiC & GaN with Si at Room Temperature



MITSUBISHI HEAVY INDUSTRIES (MHI) claims to have achieved the world's first direct bonding of silicon carbide (SiC) and gallium nitride (GaN) with silicon (Si) respectively at room temperature. The company has also previously directly bonded sapphire with Si at room temperature.

Realized by a room-temperature wafer bonding machine developed by MHI which enables highly efficient, high-quality bonding of these materials, the achievement promises possibilities for various applications. The machine should further facilitate and pave the way for new device development while dramatically enhancing productivity.

MHI looks to expand applications of room-temperature bonding to new fields. MHI's room-temperature bonding machine uses a method to bond atoms of various materials at room temperature by activating the surface of the materials with ion beam radiation in a vacuum.

The machine is capable of bonding various materials, for which optimized ion beam radiation set according to characteristics of each material is a critical factor. Room-temperature bonding of SiC, GaN and sapphire with silicon were achieved through optimized precise ion radiation, respectively.

For all three materials, solid and rigid bonding has been confirmed by the company.

Due to its characteristic high-voltage durability and suitability for high-speed and high-efficiency switching, SiC has been in the spotlight for applications for next-generation power devices (power semiconductor devices), including a component of inverters for electric vehicles (EV).

Application of GaN for blue light-emitting diodes (LED), as well as high-frequency wave and low-loss power devices has been growing. Sapphire, which is expanding as a material in optical devices, is also applicable as a substrate for high-frequency circuits when bonded with silicon to produce silicon on sapphire (SOS).

Eliminating the heating process required in conventional heated bonding, room-temperature bonding not only frees devices from heat stress and strain, thereby enabling rigid and highly reliable bonding, but also significantly reduces the processing time that previously included a heating/cooling cycle.

With these advantages significantly shortening production time and securing a higher yield ratio, the room-temperature bonding machine realizes reductions in device production costs.

MBSP is a program to support MHI's room-temperature bonding machine users at each stage of development: conceptual design, functional prototype production, trial mass production and mass production. In implementing the program, MHI will utilize its own engineers and facilities to liaise closely with customers and provide support relating to device bonding and evaluation.



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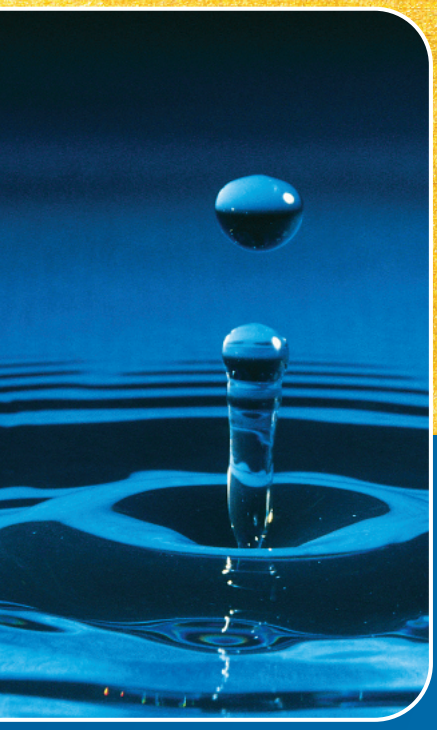

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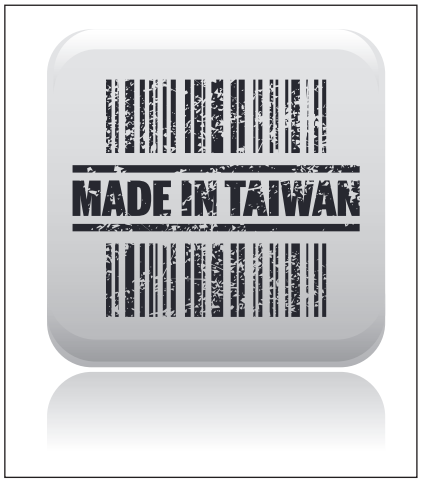
TSMC announces Gigafab

TSMC has held a groundbreaking ceremony in Taichung's Central Taiwan Science Park for Fab 15, TSMC's third 12 inch (300mm) Gigafab(tm) and an important milestone in the company's pledge to expand investment in Taiwan. The groundbreaking ceremony was conducted by TSMC Chairman and CEO Dr. Morris Chang. "Science parks have played a critical role in the development of Taiwan's high-tech industry.

They have also provided important support to TSMC as we grew to become a leading global semiconductor company with its roots in Taiwan," Dr. Chang said. "Over the past two decades, TSMC has flourished in the Hsinchu and Tainan science parks, and our groundbreaking for Fab 15 today sets the foundation for TSMC to reach new heights."

"TSMC has worked unceasingly to improve its technology leadership, manufacturing excellence, and customer partnership to join together with our fabless and IDM customers to forge a powerful competitive force in the semiconductor industry.

This groundbreaking for Fab 15 in the central Taiwan science park shows our commitment to providing our customers with advanced technology



and satisfying their capacity needs. And as capacity in Fab 15 grows, it will create 8,000 high quality job opportunities, demonstrating TSMC's dedication to corporate social responsibility," Dr. Chang added.

Fab 15 will be TSMC's third Gigafab(tm), or fab with capacity of more than 100,000 12 inch wafers per month, and will also be TSMC's second Gigafab(tm) equipped for 28nm technology.

Construction will be divided into four phases, and total investment over the next several years is expected to exceed NT$300 billion.

TSMC is scheduled to begin equipment move in for the phase 1 facility in June 2011, with volume production of 40nm and 28nm technology products for customers in the first quarter of 2012. More advanced process nodes will be introduced as TSMC's technology development continues to advance.

In addition, to meet strong customer demand as we build Fab 15, TSMC will continue to expand capacity at Fab 12 in Hsinchu and Fab 14 in Tainan.

Combined capacity of Fab 12 and Fab 14 currently exceeds 200,000 12 inch wafers per month, and is scheduled to exceed 240,000 12 inch wafers per month by the end of this year, underscoring our commitment to providing steadfast support to our customers.

Fab 15 will be TSMC's next "green fab" following Fab 12 and Fab 14, incorporating green concepts in energy conservation and pollution control in its design, including a process water conservation rate of 85%, reclamation of rainwater, recirculation and reuse of general exhaust heat, and development of solar power generation and LED lighting applications. TSMC's goal is to reach zero emissions of greenhouse gases.

Intel reports best ever quarter

INTEL CORPORATION has reported second-quarter revenue of $10.8 billion, up 34 percent year-over-year. The company reported operating income of $4.0 billion, net income of $2.9 billion and EPS of 51 cents. The company did not release volume of product and only presented fiscal details.

"Strong demand from corporate customers for our most advanced microprocessors helped Intel achieve the best quarter in the company's 42-year history," said Paul Otellini, Intel president and CEO. "Our process technology lead plus compelling architectural designs increasingly differentiate Intel-based products in the marketplace. The PC and server segments are healthy and the demand for leading-edge technology will continue to increase for the foreseeable future."

Q2 2010 Highlights

- PC Client Group revenue was up 2% sequentially, with record mobile microprocessor revenue.
- Data Center Group revenue was up 13 percent sequentially, with record server microprocessor revenue.
- Intel Atom microprocessor and chipset revenue of $413 million, up 16 percent sequentially.
- The average selling price (ASP) for microprocessors was slightly up sequentially.
- Gross margin was 67 percent, 3 percentage points higher than the midpoint of the company's expected range of 62 to 66%.
- R&D plus MG&A spending was $3.25 billion, higher than the company's prior expectation of approximately $3.1 billion.
- The net gain from equity investments and interest and other was $204 million, higher than the company's revised expectation of $180 million.
- The effective tax rate was 31 percent, slightly below the company's revised expectation of approximately 32 percent.

TV semiconductors to enjoys re runs

LED backlighting and other advanced television architectures making their way into an ever larger number of LCD-TVs will power the global television semiconductor market toward its biggest year yet in 2010, according to iSuppli Corp. Coming off a robust $9.3 billion turn in 2009, the TV semiconductor space is headed for an even stronger year in 2010, finishing the year at a spectacular $12.2 billion.

"To support the various sophisticated features that today's consumers are demanding, LCD-TVs are incorporating more semiconductor content, a phenomenon that will benefit the chip industry enormously in 2010 and beyond," said Randy Lawson, manager and principal analyst for display and consumer electronics at iSuppli. Such a high water mark, the first time revenue will pass the $10 billion threshold—equates to an annualized growth level of approximately 29 percent for 2010—almost six times the 5.5 percent expansion rate posted by the market in 2009, Lawson observed.

Not unexpectedly, chips used in LCD-TVs will ship in the greatest quantities during the next four years, far ahead of all other TV display technologies. In comparison, chip shipments will hold steady at the low 10,000 level for plasma, continue on a path of irreversible decline for CRT and be all but nil by 2012 for rear projection types.

The most lucrative growth for the TV semiconductor market centres on the use of LED backlights for LCD-TV panels. Compared to Cold Cathode Fluorescent Lamps (CCFLs), LED backlights offer higher image contrast, lower power consumption and improved product styling by allowing a thinner panel profile. More than 150 LCD-TV models in the North American market alone feature LED backlighting.

As LED penetration deepens, LED related semiconductor revenue will enjoy a corresponding surge in growth, rising from just $400 million in 2009 to more than $4 billion by 2014. All told, shipments of LED backlit TVs are projected to hit 25 million units in 2010—an increase of more than 400 percent from 2009 shipment levels.

In addition to LED backlighting, a number of advanced television features will drive the TV semiconductor space in the years to come, Lawson said. These features include full High Definition (HD) 1080p resolution, Internet access, wireless connectivity and frame rate conversion to support 120Hz/240Hz playback—all of which will require the use of greater quantities of advanced video processor chips.

Surprisingly, 3-D technology—despite the enormous publicity and hype surrounding this coveted TV feature—is not expected to be a major growth driver for TV semiconductors, according to Lawson. Nonetheless, OEM and consumer interest in 3-D enabled models will spur faster penetration of 240Hz support in LCD-TVs, due to the image crosstalk issue of current 3-D solutions. And current initiatives by LCD-TV manufacturers and panel suppliers to incorporate higher frame rates, such as 120Hz and 240Hz, will subsume onto the overall bill of materials the new additional functionality required by 3-D technology.

"While 3-D heralds a new era of advanced TV viewing for consumers, the technology itself will not significantly impact TV semiconductor revenue in general, or the market revenue for video processors in particular," Lawson remarked.

Revenue for power ICs is expected to increase to $1.8 billion in 2010, up 38.5 percent from $1.3 billion last year, iSuppli data show, with growth to continue until at least 2012, when revenue hits $2.5 billion. This represents one of the hottest growth segments of the semiconductor industry. A dip to $2.4 billion then is projected in 2013, after which revenue levels pick up again and climb in 2014 to $2.7 billion.

Nissan blames IC shortage for stoppage

NISSAN is blaming a recent shut down of car manufacturing sites for four days on Hitachi inability to supply enough parts.
This type of shutdown is unprecedented for a major car manufacturer, excepting natural disasters, and observers expect the car giant to seek compensation from Hitachi.

It appears Hitachi has been caught with the recent rise in global demand. This situation suggests that many in the industry were also unsure of how far the growth potential was. This is not caused so much by poor analysis but trepidation in an industry that has just suffered the largest recession in its history.

Hitachi officials have stated their problems arose when one of the semiconductor manufacturers announced there was a cut in production. Hitachi has been sourcing their ICs from a single manufacturer, STMicroelectronics.

A spokesperson for STMicro said "It is not ST's policy to comment on customer statements."

They did however note that, "We can only recall it's a known fact that the recovery of the automotive business after the crisis is taking place at a faster rate than expected and that the whole automotive electronics supply chain is currently under pressure to keep up with the market's demand."

WHAT NEXT FOR THE COMPOUND SEMICONDUCTOR INDUSTRY?

CS industry awards 2011

From backlighting TVs to empowering mobile devices and harnessing the sun's energy, compound semiconductor chips are playing an ever-increasing role in modern life. This is set to continue, but what will be the biggest breakthroughs over the next five years? And what's needed to tap into these new markets?

The CS Europe Conference, situated in the heart of Europe, will be exploring these issues and many more. During this 1 day, dual track conference, pioneering companies from around the globe will give their take on the best opportunities for compound semiconductors, and what has to be done to seize these opportunities.

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Keynote Speaker

Professional Career:

- Senior research scientist at University of Bonn and Research Center Juelich
- Senior research scientist/head of MBE Research Group/ Associate professor at Max Planck Institute for Solid State Research in Stuttgart for 17 years.
- University professor of Materials Science at Darmstadt University of Technology
- Director of Paul Drude Institute for Solid State Electronics in Berlin
- University Professor at Physics Department of Humboldt University Berlin

Visiting research professor at:

- NTT Electrical Communication Laboratories, Tokyo
- NTT Basic Research Laboratories, Tokyo
- Mitsubishi Central Research Laboratories, Amagasaki (Hyogo Prefecture)
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- Philip-Morris Research Award (together with 9 colleagues of Max Planck Institute)
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Klaus H. Ploog

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Chip sales respond to May growth

The indicator from e-forecasting for semiconductor business activity in Europe, a forward-looking composite index that forecasts on the average five to six months ahead sales of chips, rose in May 2010.

Following an increase of 1.1 percent in April 2010, the early bird of semiconductor sales in Europe increased by 1.1 percent to a reading of 200.4 in May 2010. The index is set to average 100 in 2000.

Looking at the six-month growth rate of the leading indicator, which is used in business cycle analysis for both signalling impending turning points in business activity and as a recession monitor, the semiconductor leading indicator rose 18.3 percent in May 2010, after an increase of 19.7 percent in April 2010.

Consecutive negative values in the six-month growth rate predict an end to an economic expansion and the beginning of an upcoming recession.

Five of the seven components that make up the leading indicator for semiconductor sales in the European market improved in May

Productivity Barometer
- US Manufacturing;

Productivity Barometer
- European Manufacturing

Non-EU Demand Prospects
- Top-10 partner-countries

US Monetary Conditions
- Yield Spread

Change in Profit Margins
- US Semiconductors;

The two components that had a negative contribution to the leading indicator for semiconductor sales in the European market were

Orders to Inventories Ratio
US Electronics;
European Short-term Interest Rates

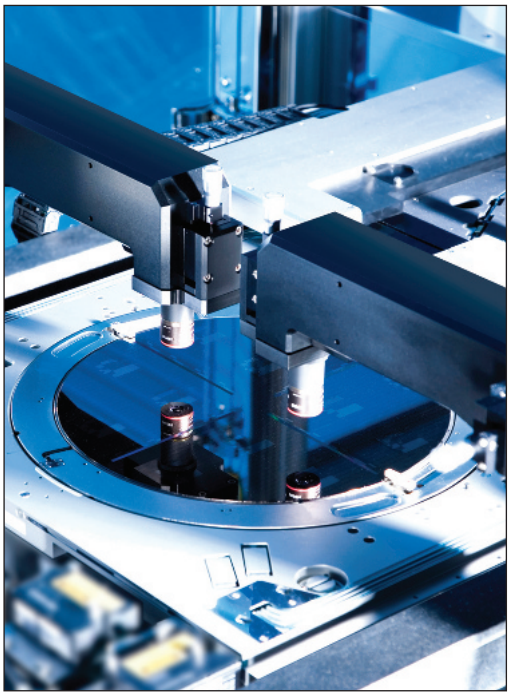
Accurate bonding

Advanced packaging for the semiconductor industry is expected to realize its market potential over the next couple of years as manufacturers begin to utilize methods such as Through Silicon Vias (TSV) in a move toward 3D packaging. One company's efforts developing a bonding machine incorporating four techniques in one system have paid dividends with a recent research announcement. **EuroAsia Semiconductor** looks at **EV Group.**

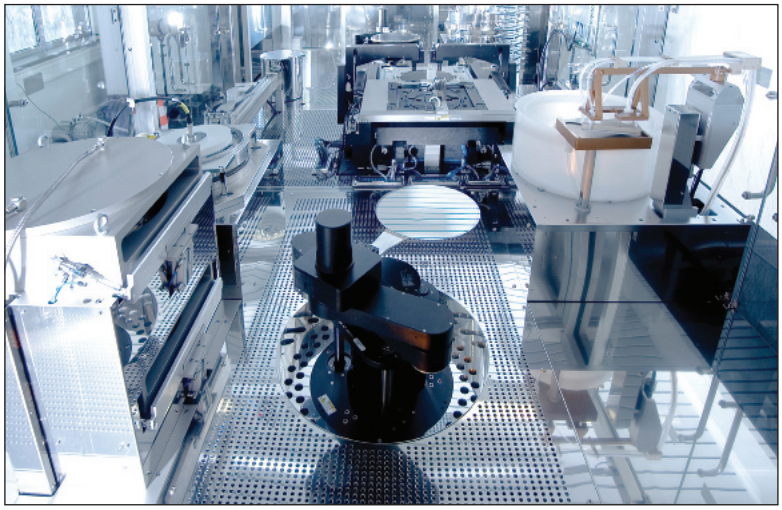
The semiconductor industry moved towards 300mm wafer sizes for manufacturing IC devices a number of years ago in the continuous push to improve performance while reducing cost. Although there is discussion of the potential of 450mm wafers at present, there is still a great deal to be gained from 300mm manufacturing as line widths shrink at an even faster rate than before. As these shrinkages have taken manufacturing to the atomic scale there have been new challenges in the industry with smaller dimensions providing greater risk of electromigration or device issues with material degradation that may not have caused issue in the larger line widths.

The carrot of the semiconductor industry has been Moore's Law and has been a useful tool for providing a goal for the industry by doubling the amount of transistors while halving the cost. Despite the physical limitations that are nearing for the traditional methods of manufacturing, the industry continues to devise innovative ways to maintain a path along Moore's prescient assertions.

One of the novel methods of manufacturing that is providing ways to extend Moore's Law despite the manufacturing limitations can be found in advanced packaging. Realizing the difficulties facing manufacturing in finding production ready methods to continue the traditional shrinking methods, engineers began to see the benefit of connecting semiconductors onto a single device platform thereby achieving the Moore's Law goals using the same technology. Techniques such as wafer bumping, 3D Interconnect, and chip scale packaging allow different components of an integrated circuit (IC)



EVG SmartViewNT 300mm wafer aligner



Inside view of EVG's modular 300mm GEMINI system

to be stacked on each other and directly connected, rather than side by side on a printed circuit board. These new packaging methods enable the production of ICs with reduced cost, lower power consumption and higher performance.

In developing this new method of packaging the industry found its own gremlins lurking behind the engineering ideas. One area that was causing concern was the ability to perform advanced packaging methods at the 300mm diameter. The reason was the accuracy required in lining up devices either singularly or at a wafer level. The level of accuracy required is at the atomic scale and although this type of manufacturing has been achieved in laboratory conditions the real test is being able to ramp up the process to an acceptable manufacturing level. The industry has never been wont to move to new processes unless there is an overall improvement in yield and ASP and road maps are no longer seen as gospel but rather guidance. To understand the change in dynamics you only have to realise that the industry spent at least 10 billion dollars, possibly as high as 13, in developing 300mm technologies. An investment many are still struggling to recoup. This sort of financial environment tends to make people more cautious. Rather than rushing down the Moore's Law path with the eternal optimism that has been a common feature for the industry, there has been a statelier pace towards new technologies as they have to prove themselves before being taken onboard. As it turns out, it would appear advanced packaging will be a key enabler in continuous IC improvements. At least until they work out another way.

Precise approach

One company that saw the growth in advanced packaging and chose to leverage its expertise in the area has been EV Group. Originally founded in 1980 as Electronic Visions by Austrian husband and wife team Erich and Aya Maria Thallner, EV Group has grown into a global manufacturer of extremely precise systems for semiconductor manufacturing. Initially focused on MEMS devices as they were being developed for the automotive industry with products such as air bag sensors and electronic vehicle stabilizing systems.

Building on this expertise, EV Group developed a process separation between wafer alignment and bonding back in 1990. This has now become the industry standard and forms the basis for recent achievements in 300mm advanced packaging techniques. EV Group has consistently investigated industry needs long before needed by manufacturers. They introduced the SmartView wafer-to-wafer alignment system which incorporates a face-to-face alignment technology for wafer-level packaging and 3D interconnects way back in 1999. The combination of these expert technologies is only now beginning to come to the fore.

EV Group has made a number of announcements in the last couple of months demonstrating the increasing interest in advanced packaging as well as the pivotal role the company is playing in the development of technologies that will enable continued advancement of semiconductor technology at the 300mm level. At least a dozen announcements in July alone show EV Group joining global research efforts or providing tools to research and developments projects around the world.

A key announcement for EV Group as they built towards the recent interest in EV Group's tools was the selection of EVG's fully automated 300mm GEMINI wafer bonder for enabling next generation TSV and 3D interconnects. The order from Sematech's 3D interconnect program at UAlbany Nanocollege last year enabled EV Group to further their own research and development in a multidisciplinary team. The

order represented the industry's first fully automated 300mm wafer bonder to integrate all four types of wafer bonding techniques into one system: thermo compression bonding, fusion bonding, temporary bonding and chip-to-wafer bonding.

With the rising demand for smaller, more functional and lower-power chips, 3D architecture has emerged as the best approach for meeting leading edge consumer device requirements. The collaboration on TSV/3D at SEMATECH was instrumental in breaking down manufacturing barriers thereby speeding industry wide technology adoption among memory and CMOS manufacturers.

"SEMATECH has been involved in 3D research for several years, and we are committed to building a strong infrastructure to pave the way for volume production of TSVs," noted Sitaram Arkalgud, director of SEMATECH's 3D Interconnect Program at the time of the announcement. "Wafer and die bonding are key processes for 3D interconnects, and the EVG wafer bonding technology will provide various bonding capabilities that allow our researchers to aggressively address technical challenges in bonding next-generation TSVs, a critical requirement for successful introduction of 3D interconnects."

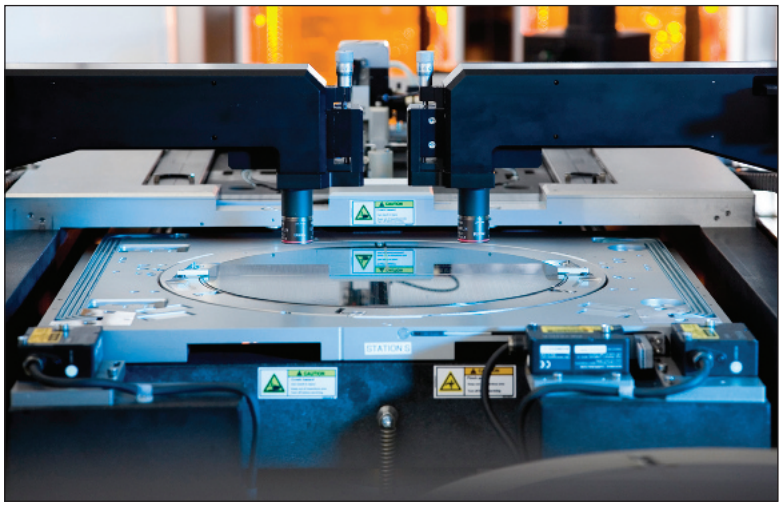
Paul Lindner, EVG's executive technology director was also upbeat at what could be achieved, "SEMATECH has one of the world's most advanced R&D programs on 3D interconnect technology. This is a tremendous opportunity for EV Group to contribute to this top-level program, which includes the industry's leading experts throughout the 3D IC value chain. We've already achieved copper/copper bond alignment results well in advance of our 2010 targets, and we look forward to this important collaboration with SEMATECH and seeing 3D technology continue to gain traction as the technology of choice for high-volume memory and CMOS manufacturers."

EVG's fully automated 300mm GEMINI wafer bonder systems are used for high-volume wafer bonding applications for MEMS, 3D IC integration and advanced packaging, as well as compound semiconductor applications. The system purchased by SEMATECH is based on the flexible GEMINI platform and integrates the company's SmartViewNT series announced in December 2008. Up until now, room-temperature fusion bonding and high-temperature, high-force thermo compression bonding were processed on two separate tools. This next-generation design can combine all of these bonding capabilities into one system for maximum R&D flexibility. Alternatively, it can be configured for a specific process flow to maximize productivity in a manufacturing environment.

Bonded results

Wafer-to-wafer bond aligners support micron level face-to-face alignment for 3D interconnects and this is the area that SEMATECH developed with EV Group and the results of this research has led to EV Group receiving orders for their tool to be involved in ongoing research and now development with companies and consortia around the world. Wafer stacking has become a viable solution to reduce actual die size for new IC packaging applications. The SmartView Aligners offers a proprietary method for micron level face-to-face wafer level alignment. This alignment technique is key to achieving the required accuracy in multiple wafer stacking for leading edge technologies. SmartViewNT technology combined with the Gemini wafer bonding systems allows stacking of wafers through face-to-face

EVG GEMINI system for 300mm



300mm wafer pair being aligned on the SmartView wafer alignment system

alignment and subsequent permanent bonding to form electrical or optical interconnects between wafers.

To be successful, 3-D ultrathin wafer stacking technologies require the development of reliable through-die interconnects with varying aspect ratios depending on the application. This type of integration poses forward new challenges in the development of new TSV processes suitable for thin-wafer handling technologies.

EV Group and SEMATECH, along with other consortium members, recently presented results from the R&D at Albany reporting on recent experimental studies performed as part of a 3D integrated circuit (3DIC) production-worthy process module roadmap check for 300mm wafer-to-wafer (WtW) copper-to-copper thermocompression bonding and face-to-face (F2F) aligning. Specifically, they demonstrated submicron alignment capabilities (3sigma alignment variability ~ 1μm) post Cu bonding on topography M1V1-to-M2 Cu wafers with no interfacial voids observed and complete Cu interdiffusion, as supported by transmission electron microscopy (TEM) and electron back scatter diffraction (EBSD) data. Also, less than 0.1% clustered voids bonding uniformity were observed on bonded blanket Cu wafers. In addition to bonding quality characterization studies involving scanning acoustic microscopy (SAM) and confocal infra-red (IR) laser scanning microscopy. The report covered the development of a prototype integrated IR, highspeed focused-ion-beam (FIB) technique with CAD overlay capabilities, developed with consortium participants that enable the creation of site specific cross-sections and TEM samples to better observe bonding structures of interest.

Production-worthy WtW Cu bonding and F2F alignment solutions are major enablers of 3-D integrated circuit (3DIC) technology enabling the vertical stacking of multiple processed wafers containing ICs, by electrically connecting them in the z-direction. The 3D fabrication approach researched in Albany provided evidence of a production worthy 300mm alignment and bonding process that integrated metrology process enabling successful wafer level bonding with copper metallization process layers. Although not the complete picture for 3D integration of ICs these results demonstrate an enabling process that will help drive this industry to industry acceptance and positive growth for the companies concerned.

Long term goals

EV Group's success with their GEMINI platform is a positive tale of developing strong technology in response to your customer's needs but before they are required. In an industry that changes so dramatically it is imperative to be aware of your technology's strengths married to an awareness of the technical challenges for the industry. A patient approach and a belief in the strength of their technology platform has enabled EV Group to not only build a strong tool for a given segment, MEMS in this case, but to also extend that technology's reach into a growing number of new and emerging areas.

This has combined to strengthen the company's reputation and bank balance. Although there are a number of issues to be dealt with for 3D ICs, process development continues across the industry with companies installing and qualifying 300mm production lines, the first true 3D IC is not expected before 2012, following on after 22nm node technology.

Despite this timing, industry analysts are still tipping advanced packaging tools to show strong market growth over the next few years. EV Group is one company that will look forward to enjoy the spoils of their labour.

The state of the semiconductor industry

The semiconductor has suffered one of the biggest downturns in its history as the world's financial markets teetered on the edge. Recent figures suggests the industry is back to positive growth but what is the state of the industry after such a fiscal knock. **Sandra Winkler of New Venture Research** reports on how the recovery is shaping.

The Great Recession which began in the fourth quarter of 2008, at the height of the holiday spending season, had an enormous effect on world economies in 2009. The bursting of the bubble housing market in the U.S. resulted in the meltdown of financial institutions around the world.

Electronic Trend Publications (ETP, now New Venture Research) predicted 2009 to be a year in which the industry would dovetail a bit due to the normal cycles in the industry, but the depth of the downturn in world economies was certainly not predicted. ETP had also predicted a downturn in 2001 also due to normal industry cycles, but again had not predicted the depth of its downward slide, as the bursting of the dot com industry had not been predicted, which also came about when

Year	2001	2009
Revenue($M)	118,490	190,341
Rev Change	-33.0%	-8.8%
Units (M)	68,550	144,630
Unit Change	-20.8%	-6.9%
ASP ($)	1.73	1.32
ASP Change	-15.5%	-2.1%

a normal softening due to industry cycles was expected.

However, the semiconductor industry faired better than many industries this time around, with the industry pulling back up in the second half of 2009. Why did the recovery in this industry come about so quickly in comparison to the downturn in 2001? The table above compares the two downturns:

First of all, what can be seen was that between the two downturns, the industry did come back up, with both revenue and units considerably higher in 2009 when compared with 2001, but ASPs are lower. But the turnaround for the semiconductor industry came back up considerably faster in the 2009/2008 downturn than in the 2000/2001 downturn. Why?

Inventories

Inventories were considerably higher in 2000 than in 2008. Prior to the downturn at the end of 2000 there had been a massive build-up of inventories of lesser-priced parts, to ensure that these lesser-priced parts didn't slow down the assembly of completed printed circuit boards (PCBs). These parts had to be burned off or discarded due to obsolescence before new purchases would be made. Inventories have been leaner since, so there were no inventories to be burned off in 2009 before new purchases of semiconductors would take place.

Consumer Spending

Consumer spending turned downwards in 2009, as many people in all industries found themselves unemployed. Even for those who kept their jobs, uncertainty in continued employment kept wallets from freely opening.

To combat this, all leading world governments put forth stimulus packages to step up consumer spending. In the U.S., the cash for clunkers program turned up demand for automobiles, although spending in this area dropped off after the program ended. But it did get the money to start flowing again, and U.S. consumer spending rose twice as fast as income in March of 2010[1].

While the downturn reduced expenditure on larger computer products, the invention and sale of smaller, less expensive computers such as netbooks and notebooks did well. Tablets such as e-readers and the iPad have become instant successes, due to their low price. Products under only a few hundred dollars seem to do well, even in a downturn.

Further Influences

Fluctuating oil prices and the value of the Euro are "need to watch" items. The higher the price of oil results in higher prices for all goods that require transportation by a gasoline-driven machine, plus more money is spent at the pump. This results in less monies left over for other items, such as computers, televisions, and other luxury consumer items. The economies of Spain and Greece are threatening the stability of the Euro, and Greece was recently bailed out by European partners. The net effects of these on global spending and economic health are yet to be seen.

Unemployment rates remain high, but with new inventions and new employment opportunities, more people will enter or re-enter the work force, boosting spending on products that undoubtedly will contain semiconductors. Indeed, semiconductors are prevalent in products sold around the world, touching the lives of even remote peoples on this planet. Even indigenous people living in rainforests now are being visited by people bringing them the Internet so that they can view the rest of the world and how they fit into the larger picture.

The explosion of products demanded in every day lives is actually quite impressive. One generation ago a home with a single television was the norm, and automobiles quite simple with engines with catalytic converters and a radio with both AM and FM stations a luxury. Today's automobiles are laden with ICs, and incorporate creature comforts and safety features not heard of a generation ago.

Seems like nearly everyone carries around at least a cell phone with them at all times, and smart phones are growing faster in popularity than "dumb" phones.

Nearly every home also has not only at least one television set, but a minimum of one PC as well, and likely one PC per family member! Digital cameras are quickly replacing film cameras, and to get the best in print quality of those pictures, an upgraded printer is necessary as well. Indeed, the demand for ICs (integrated circuits) has continued to climb upwards, despite the occasional downturn which always seems to give way to an upturn.

With world economies continuing to gain steam, so will the IC industry continue to gain momentum, for an even brighter future in the years ahead.

Reference

1. News Alert from The Wall Street Journal May 3, 2010

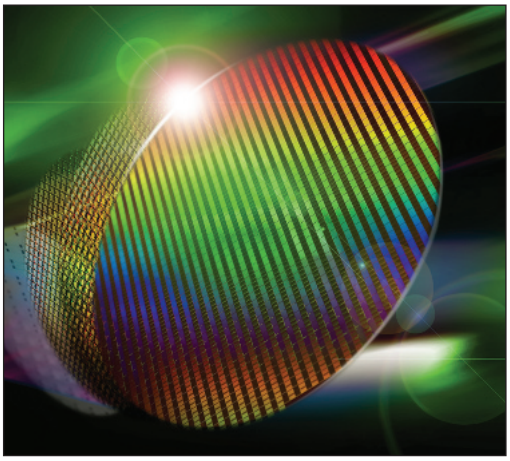
Will 450mm transition smoothly?

The transition to 300mm manufacturing is not a happy memory for many tool and material suppliers in the semiconductor value chain. Research costs were higher than anticipated and the time was marked by the attempts of companies to continue to move the cost of research to someone else. Now there is talk of 450mm manufacturing and not everyone is happy that this expensive move could come when there is plenty of opportunites remaining in the current production methods. **Joanne Itow, Managing Director at Semico Research Corp** points out that there is more at stake than just a new wafer size.

As the semiconductor industry grows its way out of the 2008/2009 downturn, it's inevitable that the debate over 450mm wafers will rear its head again. The major objection to 450mm wafers lies in the R&D cost, and the ability of all involved to benefit from the investment.

We haven't exhausted our technology options! Let's get back to an innovative mindset

The industry cannot stagnate at the existing 300mm wafer technology. Consumer demands for more memory will push NAND and DRAM to ever increasing product densities and increased unit volumes. Logic products will continue to move up the performance curve, while offering more features and performance in a system-on-chip or multi-core product. The ability to produce chips on a more economical manufacturing process is good for the overall industry's future. It's the availability of low cost memory and high performance and/or low power processors that enables the creation of new applications, increasing demand for electronic



goods and more semiconductors, a cycle that keeps our industry ticking.

And don't forget, it's the availability of mature capacity that enables a plethora of new features. When DRAM vendors moved to 300mm wafers, they used their old 200mm capacity to produce cost-effective CMOS image sensors. LED, medical applications and smart grid are being enabled because of efficient 200mm capacity which is available as advanced products move on.

In order to meet our next generation technology demands, the industry will have to find a revolutionary solution.

Whether it is 450mm wafers or not, the solution will most likely be expensive and disruptive. But every time an industry executive says we can't afford the R&D, it sends a discouraging message to all the young, creative engineers: the semiconductor industry is stagnant, protecting profit margins instead of forging new markets.

Competitive markets are designed to weed out the poor performers, but we are weeding out the risk-takers and we're no longer attracting the best of the young, innovative entrepreneurs. We all need to be sending a positive message that the magic in the black box, whether it is a cell phone or an iPad, starts with the manufacturing of the semiconductor chips.

Improving efficiency through power supply

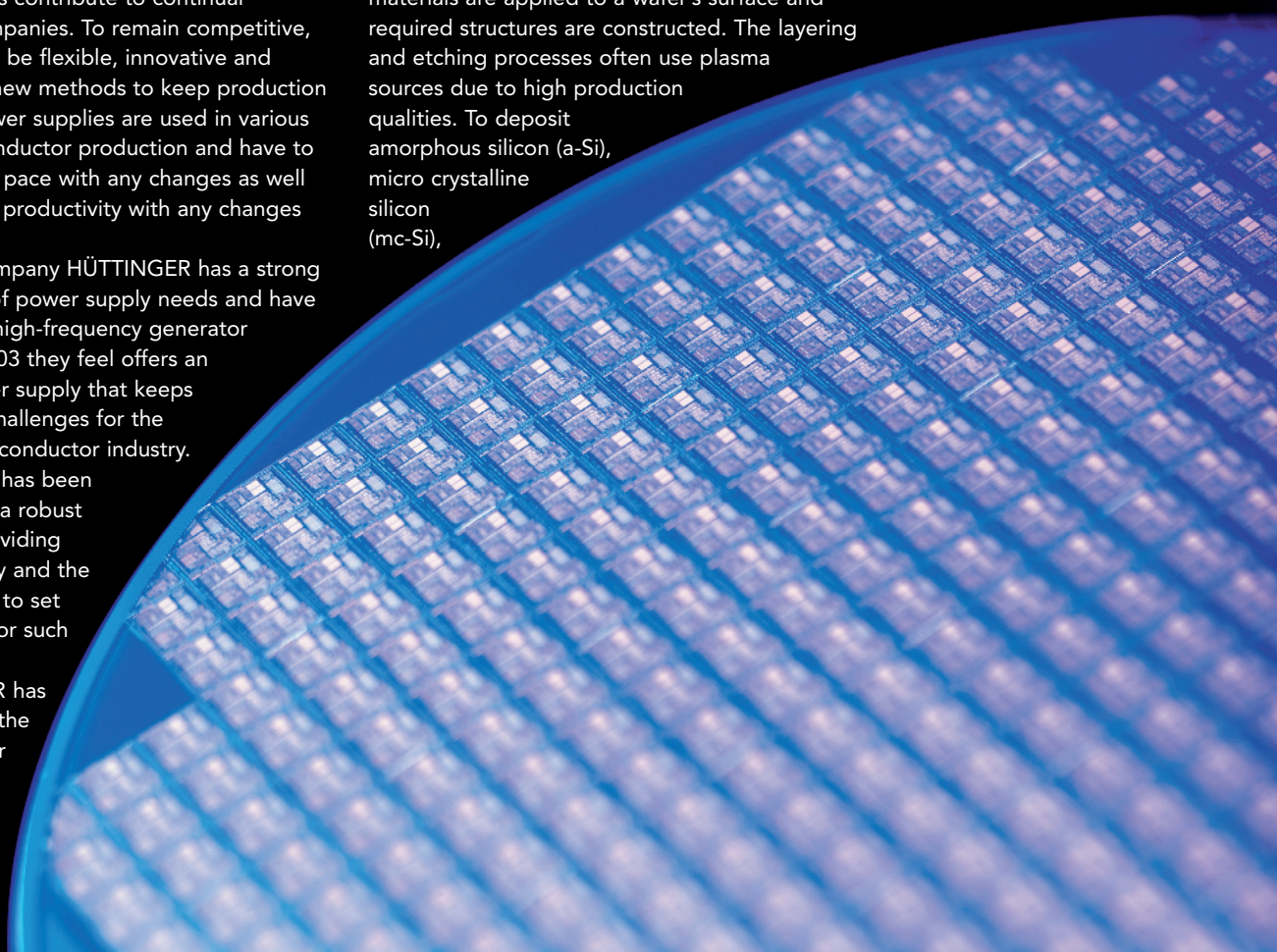
Manufacturers of compound semiconductors look for every opportunity to improve process or yield. **HÜTTINGER** discusses the energy supply needs for manufacturers and decide that efficiency and robustness are the main requirements for power supplies in semiconductor production.

The semiconductor industry is constantly faced with significant change as the industry continues to scale devices and develop new manufacturing techniques. Extreme fluctuations in supply and demand, merciless price wars and short innovation cycles contribute to continual pressure on companies. To remain competitive, companies must be flexible, innovative and constantly find new methods to keep production costs down. Power supplies are used in various steps of semiconductor production and have to be able to keep pace with any changes as well as contribute to productivity with any changes themselves.

German company HÜTTINGER has a strong understanding of power supply needs and have introduced the high-frequency generator TruPlasma RF1003 they feel offers an innovative power supply that keeps abreast of the challenges for the compound semiconductor industry. The new device has been developed with a robust approach to providing energy efficiency and the company hopes to set new standards for such devices.

HÜTTINGER has also developed the ideal solution for cutting-edge trench-filling process using HIPIMS (high power impulse magnetron sputtering). DC generators from the TruPlasma Highpulse Series 4000 are designed to reliably and accurately supply the necessary energy for these processes.

In fabricating IC circuits, thin layers of materials are applied to a wafer's surface and required structures are constructed. The layering and etching processes often use plasma sources due to high production qualities. To deposit amorphous silicon (a-Si), micro crystalline silicon (mc-Si),



Right: HE_2313
The power supply generating the plasma is a key component of plasma based processes

SiO2 and SiNx onto the wafer, PECVD (plasma-enhanced chemical vapor deposition) processes are used. HÜTTINGER developed the TruPlasma RF 1003 especially for this purpose. This power supply produces outputs ranging from 1 watt to 3000 watts at a frequency of 13.56 megahertz, in addition to PECVD, it also reliably supplies precise power for etching processes.

The TruPlasma RF 1003 has new power combiner technology, called CombineLine, that allows extreme stability for processes.

CombineLine delivers a 50-Ohm output impedance from the power supply, enabling CombineLine to adjust the process optimally at any time. Adjustment networks keep the process constant at an impedance of 50 Ohm. When ideally adjusted, the optimum HF output is introduced into the process.

However, in actual plasma processes, fluctuations always occur that change plasma impedance. The matchboxes can react during a limited error adjustment time and re-establish the 50-Ohm state in a matter of seconds. During the error adjustment phases, reflected outputs flow back to the power supply, calling for a quick, precise surge in the power output to hold the energy input steady for the plasma. The reflected output needs to be absorbed into the power supply without damaging it.

TruPlasma RF 1003

This can be done as the combiner technology has a dedicated absorber that can continuously deflect an output of 600 watts. For short-term total reflections of output (short circuit with up to 3 kilowatts of reflected output), the internal components are sufficiently shielded to ensure no damage occurs and that the power supply is operating at the highest plasma stability. CombineLine ensures the defined output is accurately delivered by means of a very broad impedance range.

The results are stable processes for all output ranges. Deposition and etching processes are supplied with precise energy required which allows less energy to be used while achieving reproducible results and a higher yield.

An additional benefit of the TruPlasma RF 1003 is an efficiency factor level of more than 80 percent. Due to this efficient energy conversion, the generator is able to reduce energy costs for the user. The source of this high energy conversion level is a special design for internal HF switching phases.

The D converter class employs an optimally adjusted conversion principle produced by interconnecting the high-performance MOSFETs and a low-loss output network. The power supply therefore makes a major contribution to energy efficiency, protecting the environment as well as the customer's bottom line.

With its compact housing in a half 19" design (216 mm x 133 mm x 381 mm), the TruPlasma RF 1003 is ideal for system integration in plasma deposition tools. The CombineLine technology provides a choice of cable length for connecting the matchbox and processing chamber that makes integration unbelievably easy and sets new benchmarks for efficiency.

HIPIMS generators for efficient and high-level trench-filling

Trench-filling with the help of HIPIMS processes is a cutting-edge process in semiconductor manufacturing. As semiconductors become smaller and smaller, the depth-width ratio of the film layers applied to the wafer changes. This change is making it increasingly difficult to fill the trenches. The use of HIPIMS processes makes it much easier to do this.

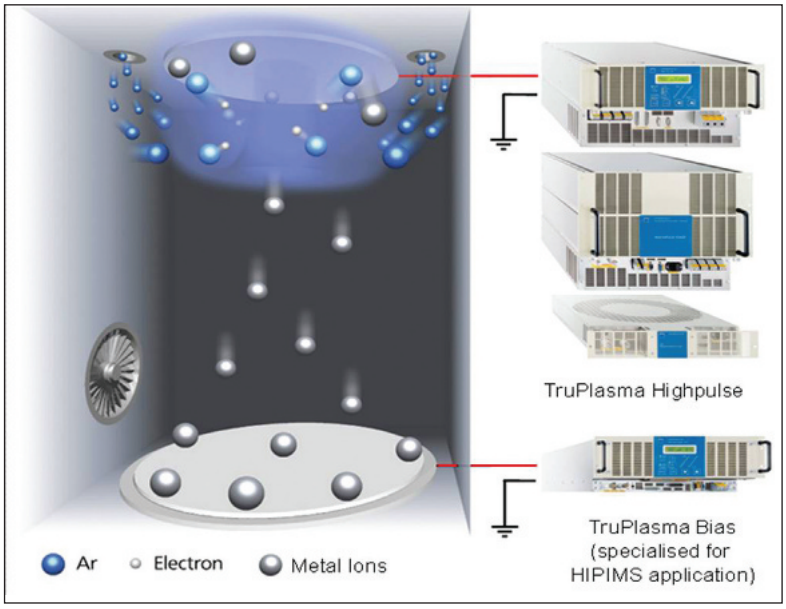
The essential difference between DC and HIPIMS plasmas is the percentage of ions in the sputtered material. While no ionization occurs in DC plasma, HIPIMS plasma has an ionization rate of up to 90 percent, the result of highly energetic pulses in the megawatt range from the HIPIMS power supply. Ionized particles lead to

other mechanisms in growing layers. Moreover, an ionized particle stream with a calculated bias voltage travels directly to the substrate. This is how high filling grades are achieved on uneven substrate surfaces for targeted deposition

The TruPlasma Highpulse Series 4000 from HÜTTINGER offers the right power supply for both the lab and volume production plants. Pulse outputs from 1 megawatt to 8 megawatts allow for a broad range of scaling. And with little effort, conventional DC cathodes can be run with the HIPIMS power supply, so the new process can be tested and future volume production implemented.

Summary

The use of power supplies offers advantages in semiconductor production. Whether for deposition by means of PECVD or for trench-filling through HIPIMS, modern generators provide for stable processes, an increased film quality and fewer defects. They reduce costs and make production processes efficient contributing to easing price pressures in the industry and creating a competitive advantage for companies.



Above: Schematic set up of HIPIMS

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Continued increase in wafers

SEMI releases latest figures showing silicon wafer shipments increased in the second quarter.

WORLDWIDE silicon wafer area shipments increased during the second quarter 2010 when compared to first quarter 2010 area shipments, according to the SEMI Silicon Manufacturers Group (SMG) in its quarterly analysis of the silicon wafer industry.

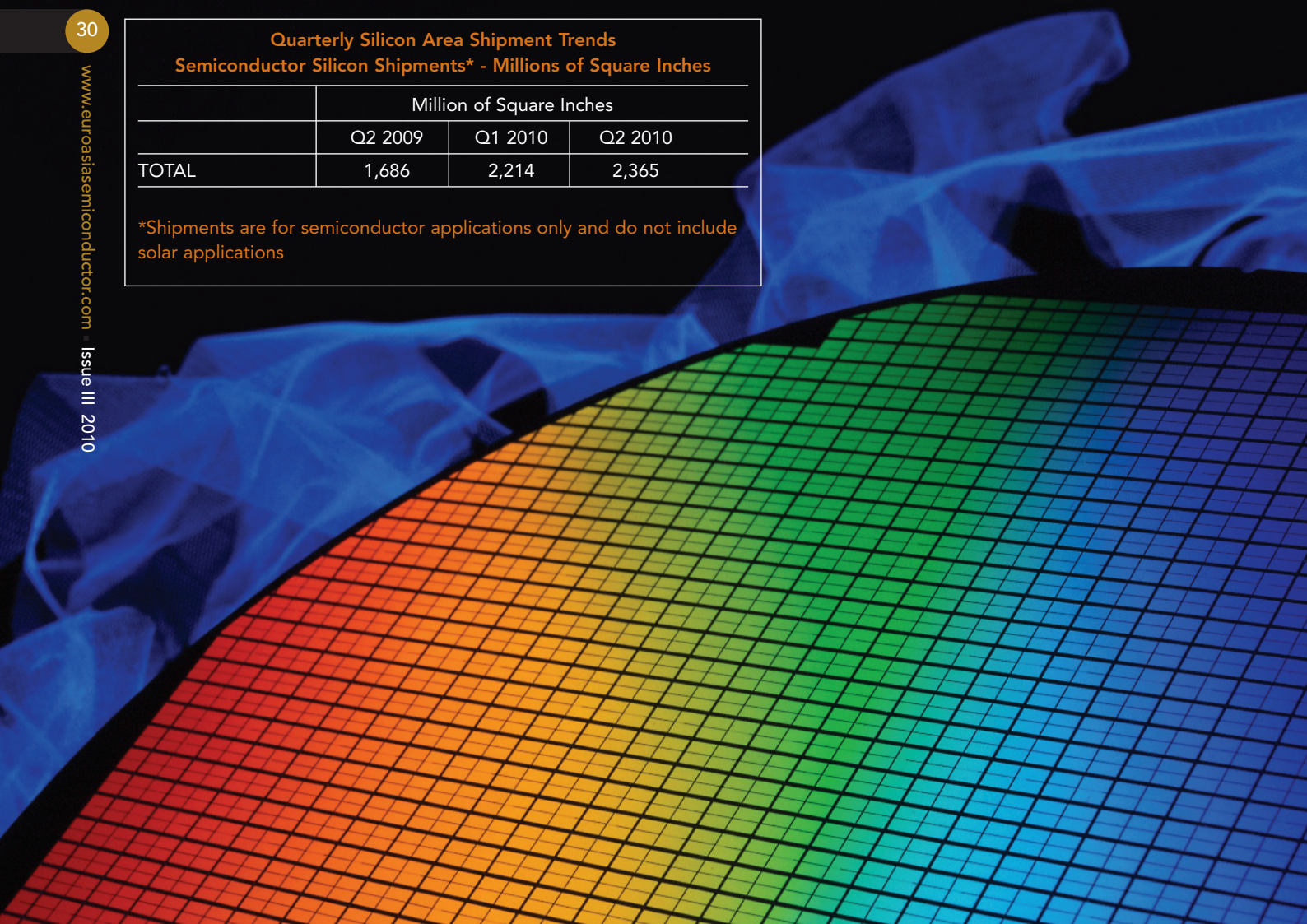
Total silicon wafer area shipments were 2,365 million square inches during the most recent quarter, a 7 percent increase from the 2,214 million square inches shipped during the previous quarter. New quarterly total area shipments are 40 percent greater than second quarter 2009 shipments and are at their highest levels ever.

"Total silicon shipped in terms of MSI has finally exceeded the high-water mark set in the second quarter of 2008," said Takashi Yamada, chairman of SEMI SMG and General Manager SUMCO. "We are encouraged by five consecutive quarters of growth in silicon shipments and expect silicon shipments to continue to trend with devices."

Quarterly Silicon Area Shipment Trends
Semiconductor Silicon Shipments* - Millions of Square Inches

	Million of Square Inches		
	Q2 2009	Q1 2010	Q2 2010
TOTAL	1,686	2,214	2,365

*Shipments are for semiconductor applications only and do not include solar applications



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