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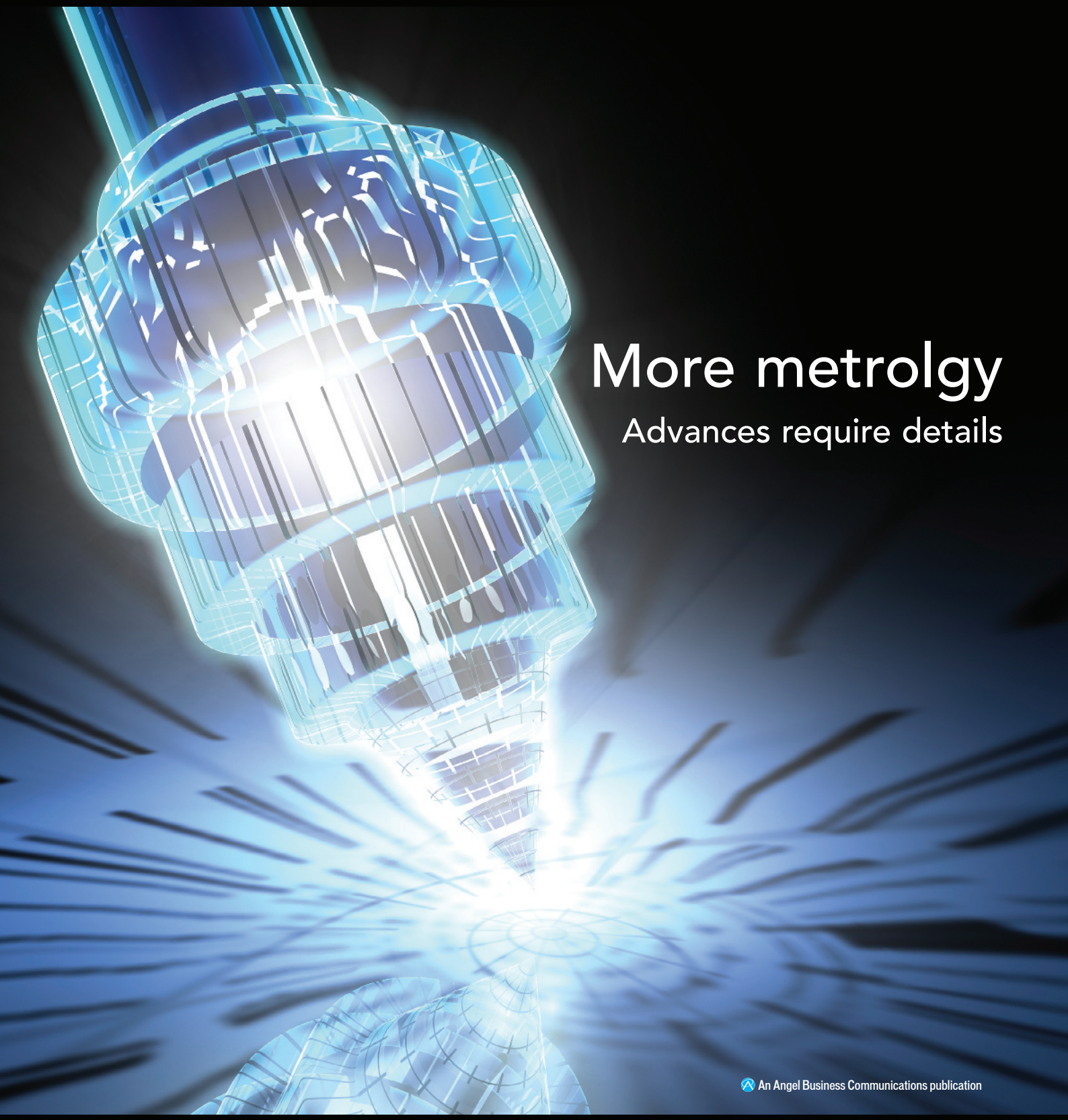

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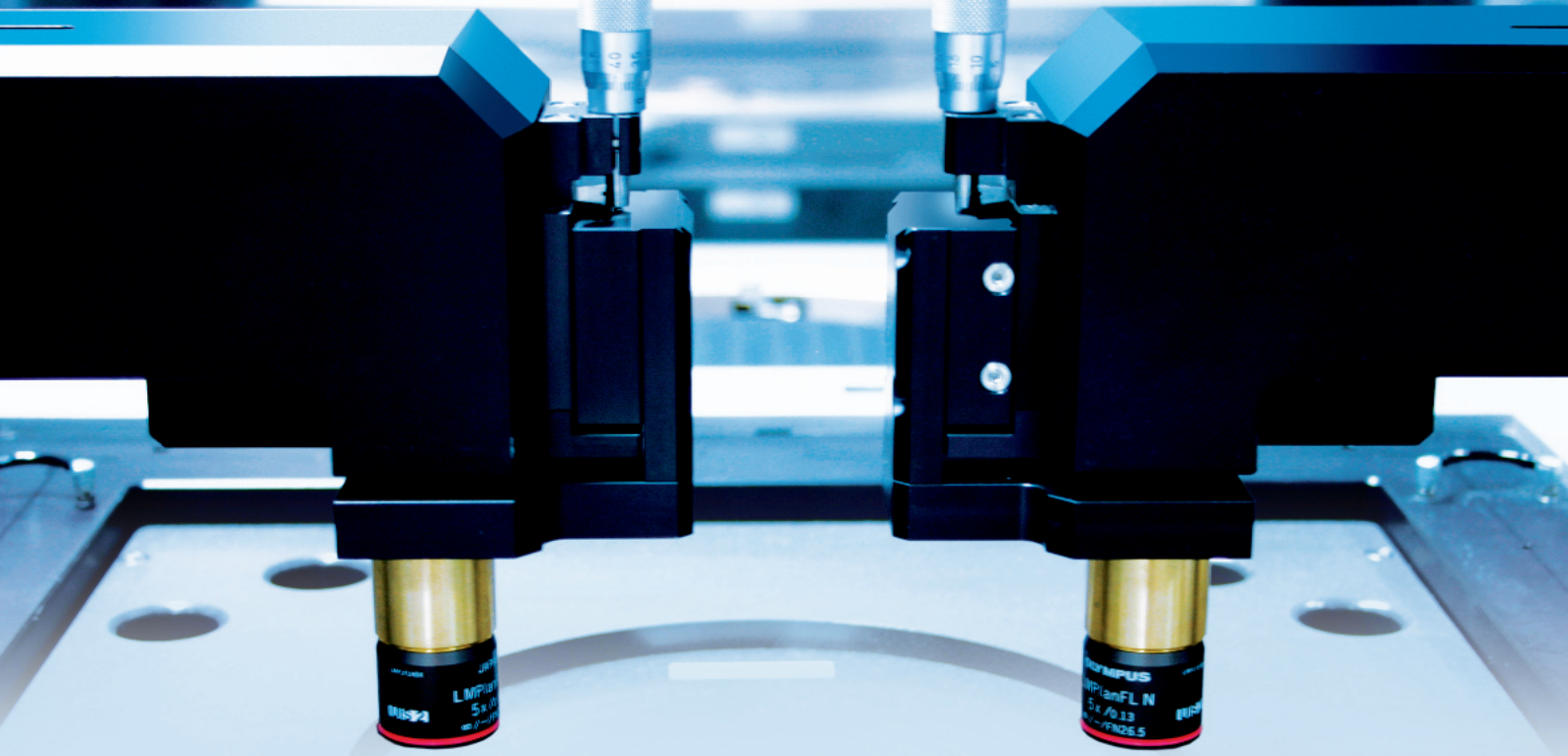

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Conflicting clues

The semiconductor industry used to have relatively simple statistics attached to it and one could be comfortable with average growth rates of 17% along the value chain. That simple world does not exist as the industry has grown to develop specialist niches as well as the emerging technologies that threaten to expand their reach.

Two stories in the news this edition highlight the conflicting data as capex is expected to reach record levels at the same time there is a warning that inventories are reaching dangerous levels last seen prior to a major downturn.

It would be easy to dismiss the differences as the usual crystal ball gazing but the problem, as described in this column many times, is the desire to rely on simple statistics. The overall industry figures no longer provide a reliable bellweather for all parts of the industry and the need to have more specific figures and focus along the value chain is more important than ever for companies wanting to make positive use of the forecasting tools available available.

Generic knowledge is not as useful as it once was and rather than wait for a report that covers all needs, as you will be awake for days deciphering, companies need to identify the markets and directions they intend to go and then request segment and regional specific news from the analysts avaible to the community.

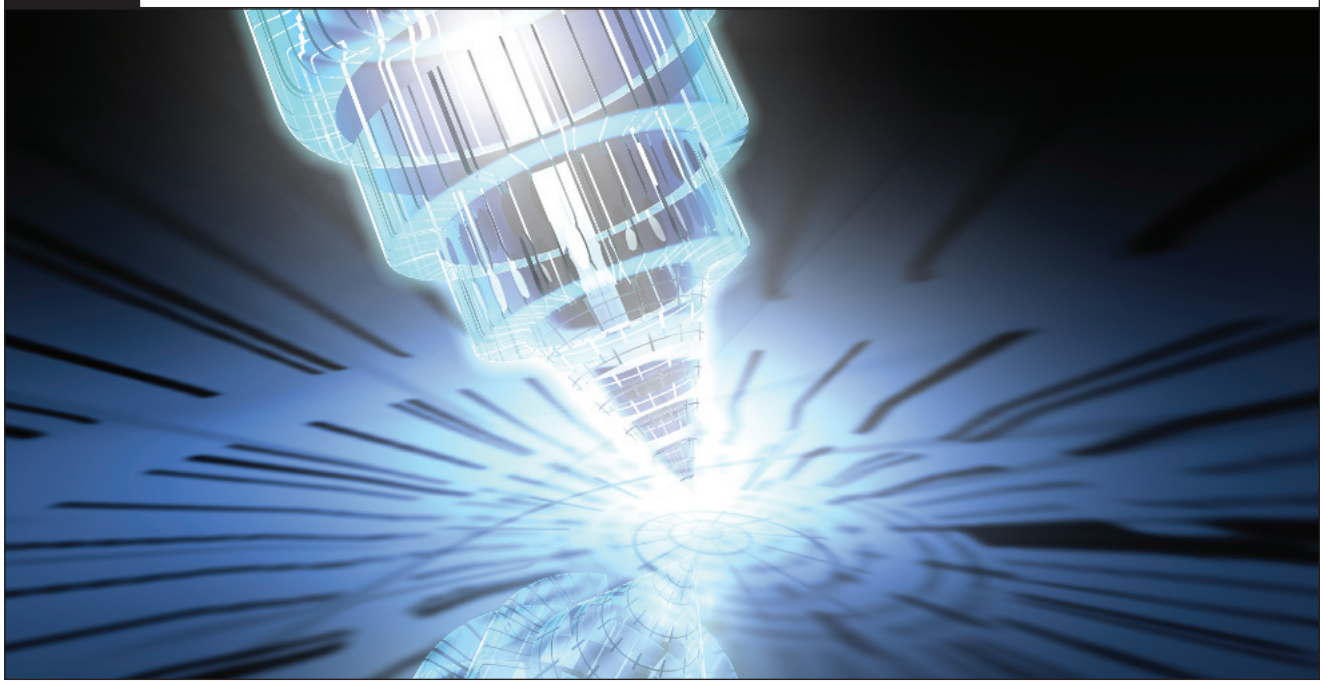
The recent ISS in Europe also showed there is a changing focus to each region and whereas before they were all competing for the same piece of the same pie there seems to be a realisation that regions must develop strengths as much as companies need to. No-one can be all things for all needs and the European industry is making a concerted effort to get back on track with a goal to develop advanced manufacturing in Europe; and not just for the labs.

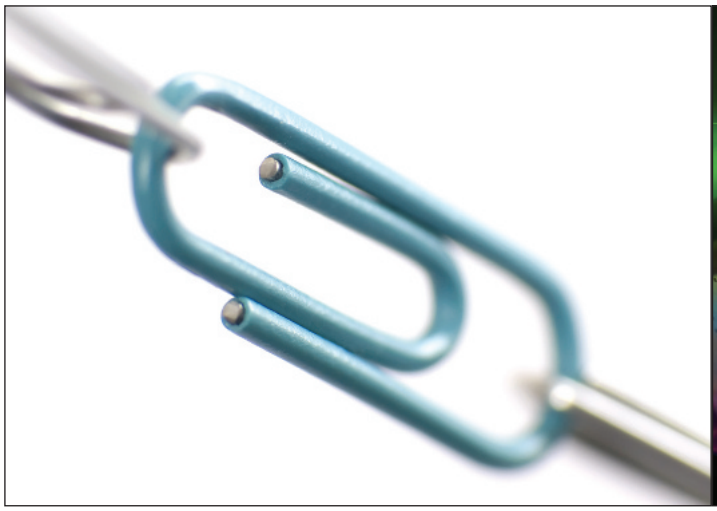
Europe has always had a strong research capacity but also tried to compete and compare to other regions of the semiconductor world and would focus more on the differences than the strengths. The new approach seen at the ISS seems a more sensible goal and has the support of industry and government suggesting that the advocacy work done by the European SEMI team is starting to pay off.

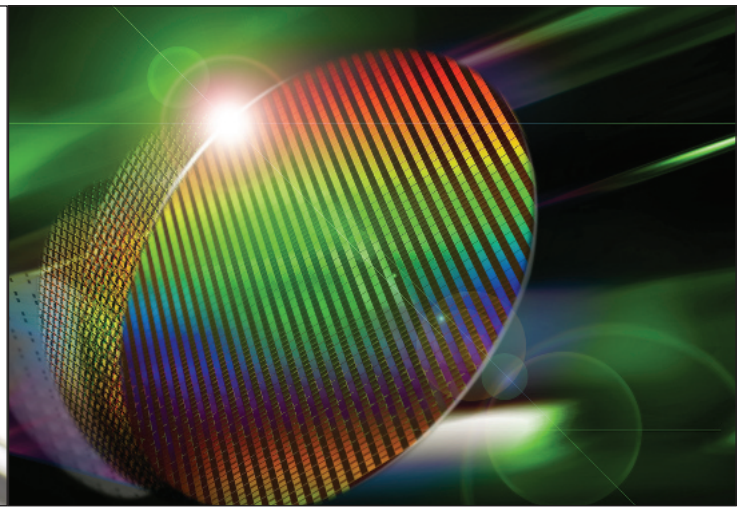
The semiconductor world hasn't so much changed as divided into multiple opportunities requiring a more focused approach.

David Ridsdale
Editor-in-Chief

contents







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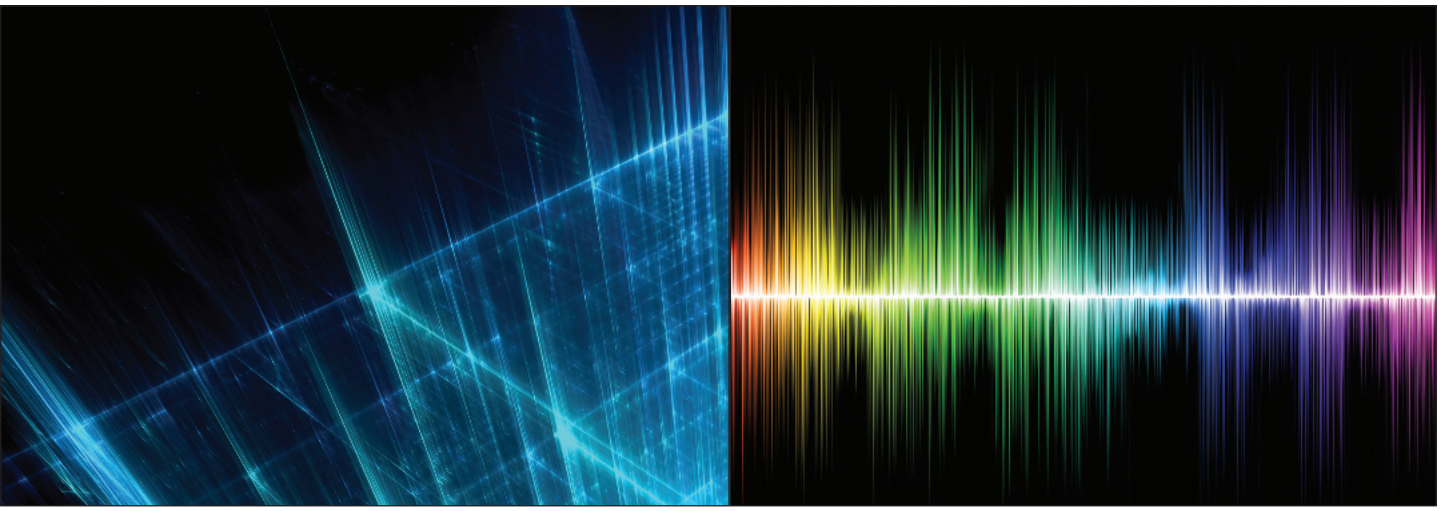

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Centre for Renewable Energy Systems Technology (CREST), Loughborough University

Topic: Practical Applications of PV in the UK
Kerry Burns
General Manager, Solarsense

Topic: Concentrating Photovoltaic Systems
Dr Roger Bentley,
Whitfield Solar

Topic: PV in 2011: Global markets, technology trends, and supply and demand dynamics
Finlay Colville,
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Topic: Building with PV
Hamish Watson
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Topic: Light Tuning For Solar Cells
Dr Daniel R. Johnson FRSC, C.Chem,
MInstP. C.Phys, FRMS, MIMMM, MBA.
Technology Manager, Intrinsiq Materials Ltd.

Topic: Reducing the risk in photovoltaic systems by means of type testing
Peter Khoury
CEO, IPSOL Energy Ltd
Dr Ralph Gottschalg Dipl.-Phys, MSc, PhD, CPhys, FHEA, MInsP, Loughborough University

Topic: Energy Management Control
Marc Stanton
Director, Clean Power Solutions

Topic: Trends in UK PV industry
Harish Dabasia
CEO, Act On Solar Power

Topic: Financing trends and models in solar PV
David Kipling FCA
Founder, Clean Earth Capital

Topic: PV Standards
Martin Zennig,
Co-chair, SEMI Europe PV Automation Standards Technical Committee

Topic: Integrating solar PV into the built environment
Dr Daniel Davies
Chief Technology Officer, Solarcentury

Topic: Why Policy is everything to the UK solar industry
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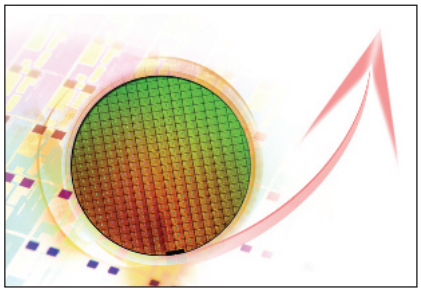
SEMI looks to record Capex

ACCORDING to the SEMI World Fab Forecast report spending on worldwide fab projects, including construction, facilities, and equipping, could grow by 22 percent over 2010 levels with fab equipment spending (new and used) to grow by 28 percent over 2010 levels. This latest projection is based on analyses of recently announced increases in capital spending plans, mainly by foundries and memory companies.

"Total spending on fab projects could approach $47.2 billion this year, above the estimated $38.6 billion spent in 2010," said Christian Gregor Dieseldorff, senior analyst of fab information in the SEMI Industry Research and Statistics group. "2011 spending will finally exceed the peak year's 2007 fab spending of $46.4 billion."

Some companies will spend record amounts in 2011, reaching historic record levels. For example, TSMC



increased capex from a record $5.9 billion in 2010 to another record high of $7.8 billion in 2011. Intel increased capex from $5.2 billion in 2010 to $9.0 billion in 2011. GLOBALFOUNDRIES doubled its 2010 capex from $2.7 billion to $5.4 billion in 2011.

Most spending is directed towards upgrading existing facilities, as companies try to avoid overcapacity and oversupply. Prior to the economic downturn, capacity growth from 2004 to 2007 ranged from 14 to 23 percent per year. SEMI's World Fab Forecast predicts slower but steady growth in capacity, about 9 percent for 2011 and 7 percent for 2012.

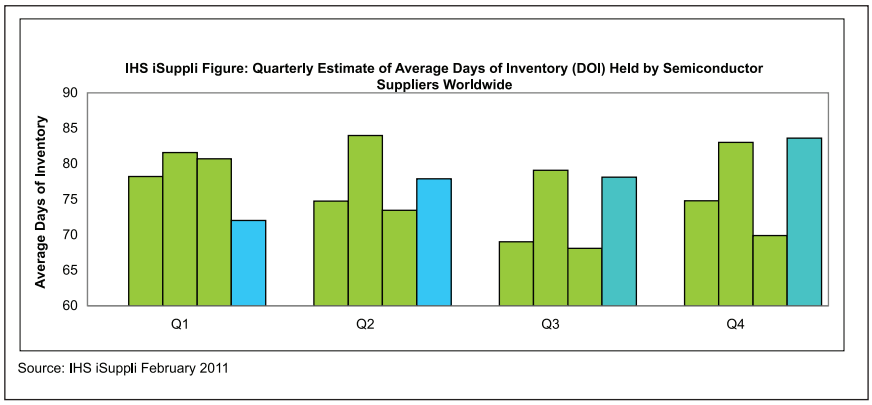
While there is record spending on Fab equipment, few new facilities are on the horizon. In 2010, 34 new volume fabs began construction, most of them for LED fabs. In 2011, only seven facilities have a high probability of being realized. Comparing new construction projects over the past 10 years to the coming two years, we see a slow down, especially for new 300 mm fabs. In 2012, three 300 mm fabs will begin constructio, two of which are potential candidates for 450 mm-ready cleanrooms.

For the first time, SEMI's World Fab Forecast data identifies seven facilities (R&Ds, pilots and volume fabs) in the near future that are candidates for 450 mm readiness. The first facilities are expected to come on line in 2013, though it remains to be seen if enough mature 450 mm tools will be available to fully equip a high-volume fab.

iSuppli warns of inventory growth

GLOBAL inventories presently held by semiconductor suppliers surged to the highest level in two-and-a-half years during the fourth quarter of 2010, a development that could spell trouble if chip industry growth loses steam this year, new IHS iSuppli research indicates. Semiconductor suppliers had 83.6 days of inventory (DOI) at the end of the fourth quarter of 2010, up 5.5 days, or 7 percent, from 78.1 days in the previous quarter. Inventory was at its highest level since the second quarter of 2008, right before the onset of the last semiconductor downtur, when DOI reached 84 days.

"Inventory levels arguably now are high by any standard, illustrating the difficulty of controlling chip stockpiles even with semiconductor suppliers' arduous efforts to keep them in check,"



Source: IHS iSuppli February 2011

said Sharon Stiefel, semiconductor market intelligence, at IHS.

The rise in inventory came as a surprise, given that IHS iSuppli forecasts had predicted stockpiles would decrease by 2.5 DOI in the fourth quarter. The actual fourth-quarter results indicate an eight DOI swing compared to expectations. The current IHS iSuppli semiconductor forecast calls for revenue growth of 5.6 percent in 2011, following a 31.8 percent increase in 2010. Assuming our forecast holds, the current inventory level should be manageable.

However, if growth is lower than expected then the high inventories could cause oversupply in the global marketplace, causing chip prices to decline faster than normal. This could amplify the size and duration of a downturn or slowdown in the semiconductor market.

Hot segments like smart phones and media tablets continue to generate strong growth for semiconductors. Furthermore, other segments like the automotive and industrial markets, which tend to get less visibility also are generating encouraging chip sales.

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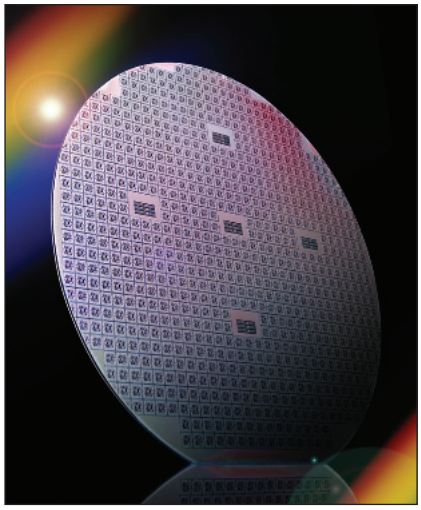
Semico points to change of MOS guard



IT should come as no surprise that semiconductor foundry manufacturers are booming. The semiconductor industry has been transformed. But it's not just fabless versus IDM (Integrated Device Manufacturer). Revenue has shifted from Embedded MPUs, MCUs, DSPs and Standard Cell ASICs to Special Purpose Logic chips. Integration has taken over MOS Logic sales, creating a huge increase in the sales of fully integrated semiconductors. Most of these chips are being manufactured by foundries.

Let's take a closer look at MOS Logic markets over the last eleven years, beginning with the year 1999 rather than 2000 to eliminate the effects of the dot-com boom-and-bust in 2000 and 2001. From 1999 through 2010 Special Purpose Logic sales increased from $16.5 billion to $59.3 billion, a CAGR of 12.3%. During the same time period computing MPU sales grew from $27.2 billion to $38.8 billion, a CAGR of only 3.6%. No other MOS logic category had significant growth, either because the sales base was too low or because the CAGR was too low.

Special Purpose Logic is now by far the largest MOS Logic device category. Special Purpose Logic sales are greater than MPU, MCU and DSP sales combined and nearly five times the sales of standard cell ASICs and FPGAs combined. In fact, Special Purpose Logic sales in 2010 were greater than sales for any other semiconductor device type.

Special purpose logic is a hodge-podge of different semiconductor types that include ASICS, ASSPs, SoCs and core based ICs for specific markets. Parsing the differences is beyond the scope of this article; but the unifying characteristic is that, no matter what the definition, design methodology or type of CPU core, Special Purpose Logic semiconductors are highly integrated chips in volume production as standard or semi-standard products.

Following Moore's Law, doubling roughly every two years, the number of transistors that can be manufactured on a chip has increased more than 100 times from 1999 to 2010. As a result, more functions, including multiple MPU, MCU or DSP cores, other logic functions, and I/O can be integrated onto a chip. This has changed the design of end-use products.

Ten or more years ago, most end-use product designs used a CPU (an embedded MPU, an MCU or a DSP) surrounded by several other logic and I/O devices. Today, the level of integration has increased dramatically. While not all systems can be reduced to one chip, the level of integration possible can reduce the chip count for almost all systems. There are other potential benefits. The functionality can be increased, the system footprint can be reduced or costs can be reduced. In addition, performance can be increased or power consumption reduced. Any combination of these benefits or all can be realized.

NRE (Non-Recurring Engineering) costs have always been an issue for ASICs, but the semiconductor industry has found ways to reduce this limitation for highly-integrated devices. One has been the re-use of blocks of logic, spreading NRE across several designs. A second has been the use of IP (Intellectual Property), blocks of logic designed by small, independent companies. By selling their IP to multiple parties, these companies can, again, spread the NRE across several designs. Purchasing IP from an IP vendor has an added benefit. Design engineers can add functionality beyond their own expertise or experience.

President Obama views atoms

ON a recent trip to Silicon Valley, President Obama received a wish when he was given the opportunity to view atoms thanks to a transmission electron microscope from FEI. The president made the trip to meet with technology leaders from the area to continue his push for innovation growth for the United States with a push to increase exports based on technological innovation.

While on the ambassadorial trip the President was able to see samples at the sub-Angstrom level through an FEI

Titan S/TEM. In addition to his tour of the TEM lab, the President also met with boys from the Beaverton-Hillsboro Science Expo and students from Robert Gray Middle School, including six girls who are members of Intel's First Lego Robotics Team.

"It gave them a chance to talk about things like quantum ternary algorithms," he said to audience laughter, "and it gave me a chance to nod my head and pretend that I understood what they were talking about."

"They deserve our applause and our praise, and they make me optimistic about America's future," he said.

The visit ended with a rousing speech to a crowd of 350 Intel workers, politicians and other dignitaries, including Oregon Governor John Kitzhaber, Intel CEO Paul Otellini, and Hillsboro Mayor Jerry Willey.

Carbon nanotache with 3D Symmetry

RESEARCHERS at the University of Surrey show the controlled synthesis of nanomaterials by subjecting pure organic molecular gas to high temperatures and pressures that allow symmetry breaking events to create the different carbon nanostructures. Spheres, nanotubes and mirrored spirals can be created under the appropriate isovolumetric conditions that show the versatility of this unique growth system. The report is published in the January 2011 issue of the premiere journal in nanotechnology, Nano Letters.

Self-organisation of matter is essential for natural pattern formation, chemical synthesis, as well as modern material science. Mechanisms governing natural formation of symmetric patterns have long intrigued scientists and remain central to modern science from attempts to understand spirals and twists of climbing plants to the studies of bacterial macrofibers and DNA.

Self-assembly of atoms and molecules is the key to understanding the natural shape formation and is elemental to the production of modern materials, such as silicon, synthetic polymers, and various nano- and microstructures.

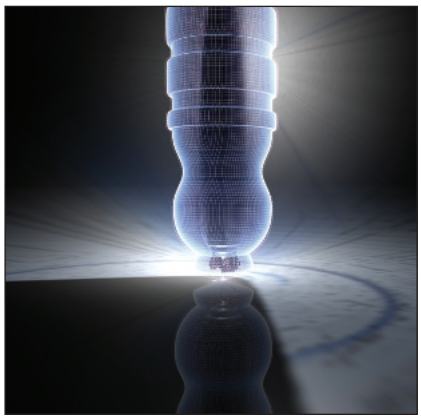
Dr Hidetsugu Shiozawa, of the Advanced Technology Institute (ATI) at the University of Surrey, said: "The work represents a concept to experiment with self-assembly process and demonstrates how morphological symmetry of nano and microstructures can be controlled. The study of such physical phenomena helps us understand why certain symmetry of structure emerges amongst others, and how this is correlated with physical quantities of thermodynamic equilibrium such as temperature and pressure."

Professor Ravi Silva, FREng, Director of the ATI and co-author, indicated: "The creation of new technologies and businesses are highly dependent on this ability to create designer materials of the highest quality. The UK is renowned for its highly creative and innovative research force, for which this is a prime example. To create a strong manufacturing base, we must back high quality research that has potential to create new markets and novel products such as those enabled by these symmetric carbon nanostructures. It will lead to transformative technologies."

Advance material characterising

CEA-Leti announced the they have entered an agreement with FEI for a three year agreement to characterize advanced semiconductor materials for the 22nm technology node and beyond. European-based CEA-Leti, with its two partners on the NanoCharacterization Platform of MINATEC Campus, CEA-Liten (new materials for new energies) and CEA-INAC (Nanoscience Institute), will apply their expertise in holography and nanobeam diffraction. FEI will provide advanced nanobeam diffraction technology with its Titan scanning transmission electron microscope (S/TEM).

"The research will focus on two important areas: use of holography with the Titan's unique XFEG electron source to improve the sensitivity of dopant profiling, and the use of nanobeam diffraction techniques to measure changes in strain and other crystallographic parameters," said



George Scholes, vice president and general manager for FEI's S/TEM product line. "With the Titan, FEI is a leader in these areas and we look forward to partnering with CEA-Leti on their unique platform for characterization and nanoscale in continuing to advance the technology."

"We must improve the sensitivity, accuracy and throughput of dopant profiling in order to continue supporting shrinking device dimensions. And a better understanding of the effects of strain is critical in the development of higher performance IC devices as we continue to push the technology to the 22nm technology node and beyond," stated Rudy Kellner, vice president and general manager of FEI's Electronics Division.

According to Laurent Malier, CEO of CEA-Leti, "We chose to work with FEI on this three year research project, not only because of their powerful, commercially-available microscope, but also because of their special expertise in nanobeam diffraction applications. Together, we expect to address several critical technical roadblocks facing the semiconductor industry as it continues to push the device size and performance envelope and also challenges in the characterization of materials used in nanoelectronics and more generally for nanosciences."

Chip with copper in mind

STATS ChipPAC announced the fcCuBE technology, an advanced flip chip packaging technology that features copper (Cu) column bumps, Bond-on-Lead (BOL) interconnection and Enhanced assembly processes. fcCuBE technology delivers high input/output (I/O) density, high performance and superior reliability in advanced silicon nodes. The fcCuBE technology offers enhanced flip chip packaging with a 20-40% lower cost over standard flip chip packaging, a compelling value with price points comparable to mainstream semiconductor packaging solutions.

"We have taken our innovative Low Cost Flip Chip technology and enhanced it to achieve greater design flexibility and performance across a broader range of applications, I/O requirements and fab nodes. The compatibility of fcCuBE technology with advanced silicon nodes has been proven down to 45/40nm, and early testing at the 28nm silicon node have shown equally promising results. The significance of fcCuBE comes from the combination of advancements we have made in materials, structure and manufacturing process capabilities," said Dr. Han Byung Joon, Executive Vice President and Chief Technology Officer, STATS ChipPAC.

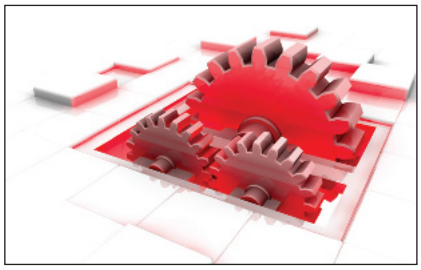
fcCuBE technology is based on STATS ChipPAC's BOL interconnect structure which has been combined with Cu column bump to deliver an ultra high I/O escape routing density with a finer bump pitch compared to standard solder bumps. The advancement enables more relaxed substrate design rules than standard flip chip packaging and provides scalability to very fine bump pitches of 80 micron and below. The fcCuBE solution also offers a reduction of flip chip packaging stress on ELK/ULK structures in advanced silicon nodes and a higher resistance to the electromigration phenomenon which can result from the higher current density induced by the scaling of features.

Energy efficiency in the subfab

CEA-Leti and Edwards announced that they have demonstrated the efficiency of a system controller to indirectly monitor the activity of the process tool and put in 'idle' mode its sub systems, vacuum pumps and abatement system, during the non process time: to save energy and natural resources.

CEA-Leti is involved in sustainability and green microelectronics. They observed that vacuum pumps and abatement systems in their subfab had the same consumption of energy whatever the working state of the process tools, since there is generally no direct communication on the tool status with the subfab.

Edwards collaborated with the CEA-Leti from January 2010, on a one year co-development program to develop a controller system capable of monitoring indirectly the status of the process tool so as to provide a signal for idle mode to the process pumps and abatement system.



Edwards' latest-generation pumps and abatement systems are designed to maximize energy savings by allowing process tools or factory automation systems to automatically switch among various low energy or high performance operating modes.

The system uses information from the load lock and process pumps to determine the process status of the tool and can provide a signal for idle mode control to the subfab abatement equipment. During a low activity period an energy saving of 75 percent of fuel and water on the abatement system was recorded.

90nm flash

CSR and TSMC have announced they are collaborating on the adoption of TSMC's leading edge 90-nm embedded flash process technology, IP and RF CMOS processes for CSR's next-generation wireless products.

The 90-nm embedded flash process technology and IP can deliver twice the speed of previous generation 0.18-micron process technology and IP. It is ideal for portable communications, smart card and high-speed micro-controller applications.

CSR has validated a broad range of proprietary connectivity IP blocks based on the new process technology and IP, and incorporated them into its recently launched CSR8600 consumer wireless audio platform that delivers significant speed, power consumption and form factor advantages.

"This technical collaboration with CSR reinforces TSMC's commitment to be the foundation for Europe's Logic IC innovation," said Jason Chen, senior vice president of worldwide sales and marketing at TSMC. "Our 90-nm embedded flash process technology and IP support high-performance, low-power and high-density memory that, along with our RF CMOS process, enables CSR to deliver next-generation SoC products."

"Our collaboration with TSMC on this 90-nm embedded flash technology enables CSR to continue developing flexible, highly integrated SoC platforms for consumer audio applications with superior system performance and minimal footprint," said Chris Ladas, executive vice president of operations for CSR.

Semi apprentices sought

ONE of Scotland's leading high tech electronics players is putting down markers on the future by re-establishing its apprenticeship programme as a medium to long term solution to an increasingly worrying skills gap. Semi Scenic, one of the few remaining serious participants in the Scottish semiconductor equipment sector, will take on two apprentices to add to a headcount which has increased from 13 to 25 in the past year.

Based in East Kilbride's Technology Park, Semi Scenic is riding a wave of optimism in the semiconductor sector, where sentiment indicates that the notoriously volatile industry may be entering a cycle of sustained growth.

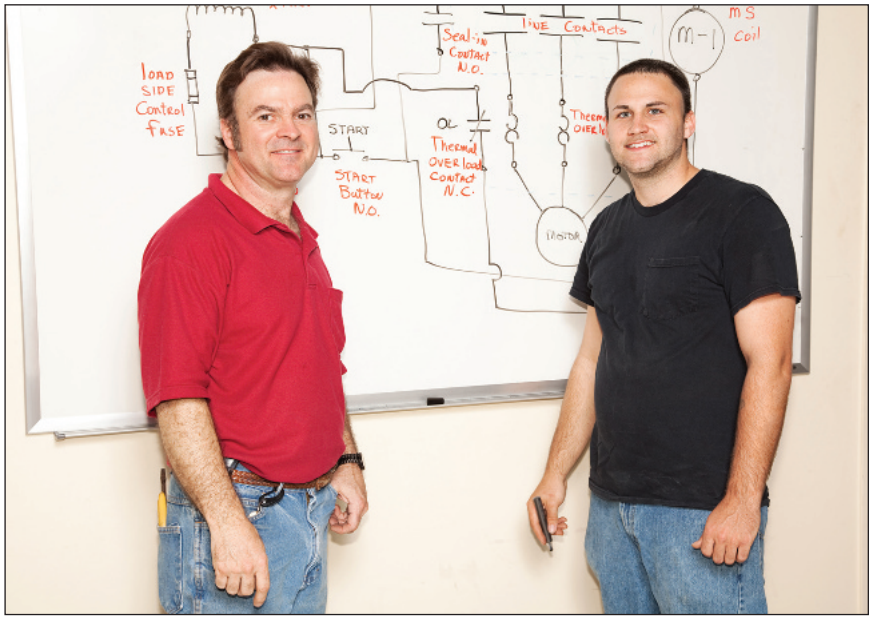
Nicholson said: "I would like to thank NMI (National Microelectronics Institute) & SDI (Scottish Development International) for their invaluable support in promoting Scottish suppliers at the Dresden event. It was an outstanding success for us in terms of excellent contacts and potential for future orders, but what was really remarkable was the sense of optimism across the board.

"All the indicators are saying that growth in 2011 will range from flat, at worst, to steady increase of between 5% and 10%. I know that forecasts can be misleading, but everything at the moment points to 2012 continuing the upward trend."

However, one of the major challenges facing Semi Scenic is sourcing the extensive skill sets required by engineers in an industry which is always at the forefront of technological advance and is now dealing in minituarisation technology so intricate that in many cases it is indistinguishable from magic.

Nicolson, who worked with Lam Research, the US original equipment manufacturer for nine years and built a career at NEC in Livingston and Hughes Micro at Glenrothes, said that despite the worldwide semiconductor boom, the outlook for the industry in Scotland could be hampered by a lack of the requisite skills.

He said: "Since the Silicon Glen cull in the last 10 to 15 years, when we lost



major players such as NEC, Motorola and Freescale, it has been left to people like National Semiconductor & Semefab to carry the flag. There is still a lot of semiconductor talent out there, but it is employed in other sectors and is reluctant to take another chance on the industry.

"As a result, we have an ageing workforce – engineers are typically now in their forties and fifties – and no new talent, apart from those we train ourselves, coming through to provide the skill sets of the future."

In order to reduce his reliance on a diminishing skills pool, Nicolson has embarked on a tailored programme with the respected East Kilbride Group Training Association, which takes students directly from school and tries to match them with relevant and suitable employers.

Out of a shortlist of 12, Nicolson chose two, who will undergo a Modern Apprenticeship training with EKGTA to Higher National Certificate standard, then spend the next two years working with Semi Scenic's qualified engineers while attending college once a week.

Nicolson said: "The apprentices realise that if they are successful, they will gain a set of skills which are not only transferrable but actively sought after all over the world. A positive example is the apprentice we took on four years ago who has just completed his training with our OEM partner in California and is now travelling and working all over Europe.

"What makes this apprenticeship stand out is the enormous range of skills which are required. As well as electrical and mechanical engineering, the apprentices have to learn how to deal with toxic gases, pneumatics, hydraulics and radio frequency power which generates the plasma used in chip manufacture."

He said the apprentices will complete their final training in Silicon Valley in California before becoming fully fledged field service engineers, dealing with issues raised by customers all over the UK and Europe.

Nicolson said: "My generation of engineers is very conscious that there is no one coming up behind us to take the skills we have learned on to a new level. If we want these skills in the future, we will have to nurture them ourselves.

"We have great expectations of this apprenticeship opportunity and we would hope to extend it in the future. In many ways, the candidates we have taken on are not only our future in Semi Scenic, but the core of the future of the industry in Scotland."

AMAT records 6 fold increase

APPLIED MATERIALS has released 2010 figures pointing to an increased year of production for the industry. Recording a six times increase in income the company stated that the semiconductor industry was a stronger than expected performer.

Applied Materials' net income for the quarter advanced to $506 million or $0.38 per share from $83 million or $0.06 per share in the fourth quarter of previous year.

Adjusting for one-time items, net income surged to $484 million or $0.36 per share from $179 million or $0.13 per share last year.

On average, 19 analysts polled by Thomson Reuters expected the company to earn $0.33 per share in the quarter. Analysts' estimates typically excludes special items.

Net sales increased to $2.69 billion from $1.85 billion in the comparable quarter a year ago. Analysts were looking for revenue of $2.59 billion for the quarter.

Looking ahead to the second quarter, Applied expects adjusted earnings to be in the range of $0.34 to $0.38 per share.

For the full year, the company expects adjusted earnings to by $1.50 per share.

Analysts currently expects the company to earn $0.31 per share in the second quarter, and $1.27 per share in full year 2011.

Avantor open new laboratory

AVANTOR PERFORMANCE MATERIALS (formerly Mallinckrodt Baker, Inc.) has announced plans to open an electronics applications laboratory in Taiwan during the second quarter of 2011. The new laboratory will be used to conduct customer demonstrations, perform process of record (POR) development and support Avantor's global electronics technologies development.

Avantor manufactures and markets high-performance chemistries and materials around the world under two well-known and respected brand names, J.T.Baker and Macron Chemicals (formerly Mallinckrodt Chemicals). These products are widely used in electronics and photovoltaic manufacturing; biotechnology and pharmaceutical production; and in research, academic and quality control laboratories.

Avantor is opening the Asia-based electronics laboratory to support global customers more quickly with access to advanced wafer processing and metrology tools. Customers will now be able to use Avantor's state-of-the-art equipment to test chemistries and materials in a class 100 clean room fab environment, rather than disrupting operations by taking their own production equipment off-line for testing purposes.

"This high-tech facility will allow Avantor to provide convenient localized support to our global electronics customers," said Director of Marketing, Electronic Materials, John Bubel. "As customers implement our performance chemistries into their processes, they can test and make refinements on Avantor's laboratory tools and transfer those processes back to their fabs, without ever having to interrupt their workflow."

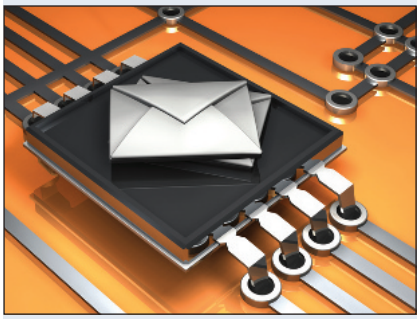
Tessera terminates Amkor license

TESSERA has released a statement announcing the company sent Amkor an notice of termination of their license agreement with Tessera. The companies are in arbitration regarding multiple issues, including breaches of the license agreement.

"We have concluded that the best course of action is to terminate Amkor's license agreement with us," stated Henry R. Nothhaft, chairman and chief executive officer, Tessera. "We will take the necessary steps to protect our innovation, technology, shareholders and licensees ."

Amkor Technology responded with a release of their own.

"This latest letter is just another part of Amkor's ongoing dispute with Tessera regarding the License Agreement and does not affect our



business," said Ken Joyce, Amkor's president and chief executive officer.

As disclosed Amkor filed a request for arbitration in the International Court of Arbitration of the International Chamber of Commerce against Tessera in August 2009 seeking relief confirming that it is a licensee in good standing, that the License Agreement remains in effect, and seeking damages and injunctive relief against Tessera. Tessera has denied Amkor's claims, and alleges that Amkor has breached the Agreement seeking termination of the Agreement and asserts that Amkor owes Tessera royalties under the License Agreement as well as other damages.

Health of the supply chain

The supply chain for the semiconductor market can be a confusing beast but one that impacts along the entire value chain. Frederic Gomer, Senior Supply Chain Consultant at the research department of Singapore based iCognitive provides and overview of their 2010 State of Supply Chain Performance Report.

Every year iCognitive publishes a benchmarking report that reveals the state of the supply chain performance for a specific sector. This year, the 2010 report is focused on the performance of the Supply chain in the Semiconductor sector. The report provides detailed results and clear insight about the median and best-in-class performance in this industry segment. The objective of this report is to help organizations to understand better their current supply chain performance and value proposition in the context of the market place, in order to launch initiatives that improve and develop their competitive advantage.

Supply chain concerns

In a context of high demand volatility, the top 3 supply chain concerns expressed by the respondents are:

1. Improving the demand forecasting (96%)
2. Increasing the delivery reliability (88%)
3. Reducing the inventory levels (78.5%)

Unsurprisingly, these three challenges are the direct consequences of the lack of visibility of the demand signal. Inaccurate forecasts generally lead to higher inventory levels and a significant decrease in the service level, due to the inability of the company to plan and align its resources accordingly.

Supply chain strategies

In the top 3 list, best practices cited are:

- Supplier's collaboration (95%)
- Sales and Operations Planning Process (92%)
- End-to-end supply chain visibility tool (74.5%)

These are mainly the best practices that can improve the demand visibility and the collaboration with the supply chain partners.

Aside, there is a growing trend to use financial supply chain concepts to optimize cash flow management with supply chain levers. In addition, companies seem to pay more attention on training their supply chain staff on advanced concepts such as SCOR Model.

Performance benchmark

For perfect order fulfillment, Best-in-class companies reach higher level of performance, with an average of 98.5%, compared to median companies (85%) and compared to laggards (50%).

Considering the order fulfillment cycle time, Best-in-Class companies manage to fulfill their orders 10 days earlier than median companies and 25 days earlier than laggard companies.

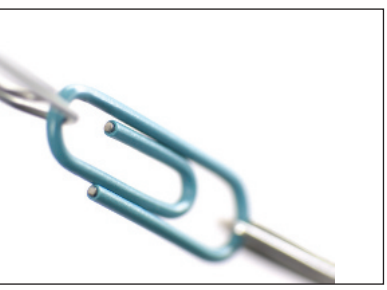
With 8% on average, Best-in-Class companies demonstrate a better control of their total supply chain management cost, compared to median companies and laggard which respectively score 10% and 12%.

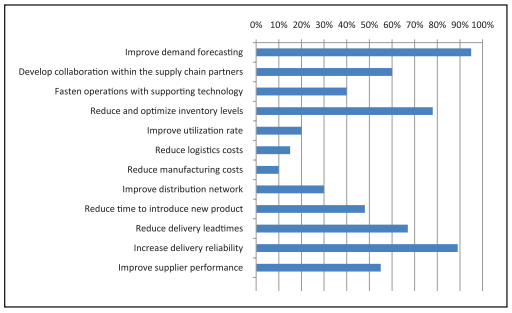
Semiconductor industry supply chain

In order to identify the main supply chain challenges in the semiconductor industry, the participants were asked to state which supply chain concerns their organization was currently facing.

In a context of high demand volatility, the top 3 supply chain concerns expressed by the respondents as expressed above were improving the demand forecasting (96%), increasing the delivery reliability (88%) and reducing the inventory levels (78.5%)

Unsurprisingly, these three challenges are the direct consequences of the lack of visibility of the demand signal. Inaccurate forecasting can lead to higher inventory levels and significant decrease in the service level (ex: delivery performance) due to the inability of the company to plan and align its resources





accordingly. Amongst the recurring challenges, the respondents cited developing collaboration with supply chain partners, reducing time to introduce new products and improving utilization rate.

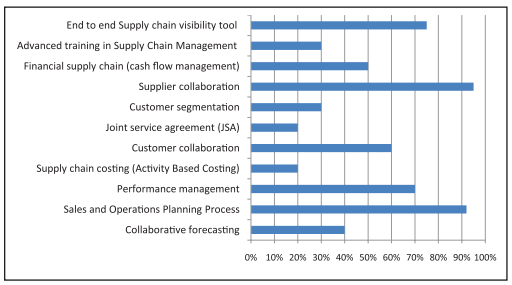
Best-in-class strategies

To respond to their specific challenges, most of the industry key players have indicated which best practices they are currently using in their organizations.

In the top 3 list, best practices that can improve the demand visibility and the collaboration with supply chain partners are mainly cited such as Sales and Operations Planning Process, end-to-end supply chain visibility tool or supplier's collaboration. Few companies are using customers' segmentation, where significant profit can be leveraged. The challenge then is to be able to calculate the real supply chain costs (versus the traditional cost allocation) with models such as activity based costing for instance.

There is a growing trend to use financial supply chain concepts to optimize cash flow management with supply chain levers. In addition, companies seem to pay more attention on training their supply chain staff on advanced concepts such as SCOR Model, as they are realizing that technology and best practices alone without well trained personnel cannot help much their organization.

- Supplier's collaboration (95%)
- Sales and Operations Planning Process (92%)
- End-to-end supply chain visibility tool (74.5%)



Supply chain configuration

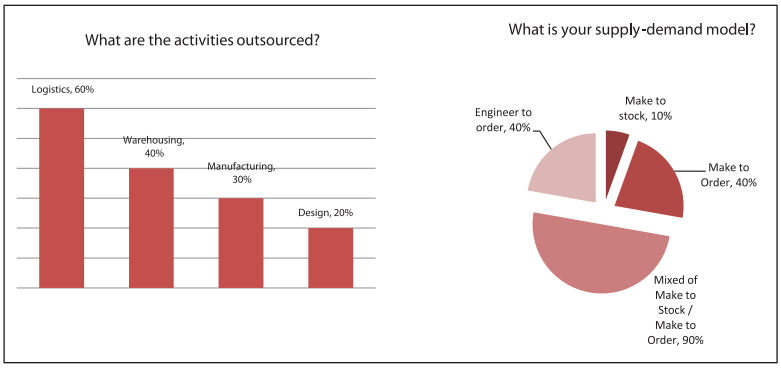
In this section the participants were asked to describe the structure of their supply chain model and which of their activities were outsourced.The large majority of respondents mentioned that they primarily outsourced the logistics and warehousing activities, and then followed by contract manufacturing.

This trend in manufacturing is accentuated by the constant disintegration of the semiconductor supply chain for the past 10 years with the emergence of contract services such as system design, foundry, assembly & test.

Performance benchmark

To evaluate the supply chain performance, the participants were asked to describe the performance levels of their supply chain, in terms of reliability, responsiveness, costs and asset management. SCOR level 1 metrics were used to make the results comparable between companies. Included here are a few sample metrics results.

For perfect order fulfillment, Best-in-class companies reach higher level of performance, with an average of 98.5%, compared to median companies which show 85% and compared to laggard with 50%.Considering the order fulfillment cycle time, Best-in-Class companies



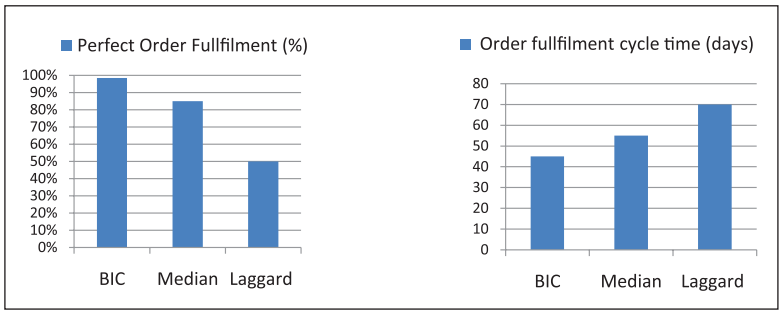
manage to fulfill their orders 10 days earlier than median companies and 25 days earlier than laggard companies.

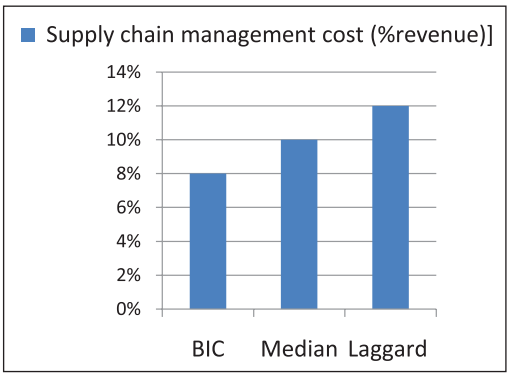
Best in class show the way

With 8% on average, Best-in-Class companies demonstrate a better control of their total supply chain management cost, compared to median companies and laggard which respectively score at 10% and 12%.

Note that the level 1 SCOR metric 'total scm cost' can be further broken down into six components:

- SCM IT related cost
- SCM Finance related cost

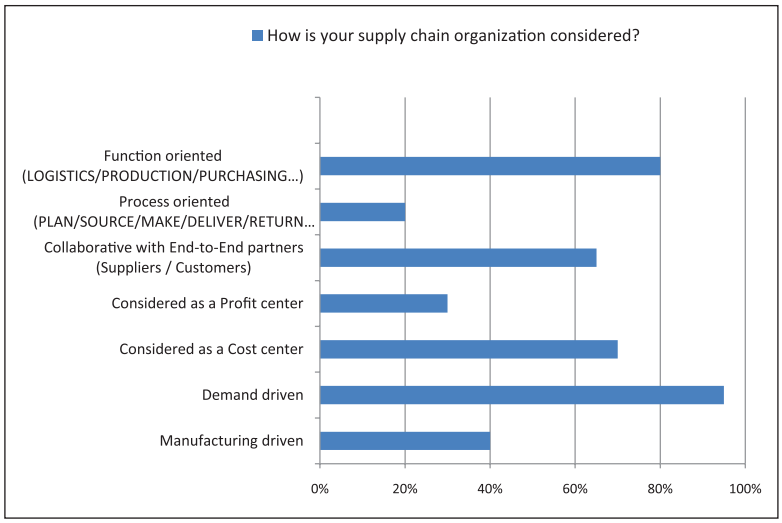




- SCM Planning related cost
- Inventory carrying cost
- Material acquisition cost
- Order management cost

Benchmark results on these 6 components are also available for the participants.

The excellent performance of the best-in-class companies is due to their end-to-end supply chain which integrates processes and systems with suppliers, customers and partners. The early adoption of advanced models such as SCOR helped them to reach superior performance levels with a more customer-centric supply chain. The use of state-of-the-art supply chain information systems (decentralized ERP, advanced planner and optimizer, constraint based production planner, collaborative supply chain portal etc…) provides them with up-to-the-minute information, fast and reliable service and streamlined and transparent business processes along the end-to-end supply chain.



Process and Organizational Enablers

In this section, the participants were asked to evaluate the level of their supply chain process and organizational capabilities.

In a context of fluctuating demand signal, the majority of respondents clearly stated that their supply chain was demand driven and highly collaborative with end-to-end partners.

Most of the respondents considered that the supply chain was regarded as a cost center rather than a profit center.

The respondents said that their supply chain was still organized in a functional mode (logistics, production, purchasing etc…) while Best-in-class respondents reported that their supply chain organization was process oriented. Best-in-class companies have reshaped their organization in a more customer-centric supply chain supported by master processes such as 'Customer fulfillment, planning and logistics' or 'Customer value chain', rather than in functions.

Training

The majority of the respondents say that their organization provides training in supply chain management between 5 to 10 times a year. Regarding best-in-class companies they received training above 10 times a year generally supported with customized e-learning portal and in-house workshops. On the other hand, laggard companies represent 20% of the respondents who do not provide any supply chain training.

Technology Enablers

In the last section, the participants were asked to describe what technology they are using to support their operations. In the top 3 IT tools used by the respondents were mentioned:

- Forecasting tools (86%)
- Supplier management portal (75.2%)
- Performance measurement (60%)

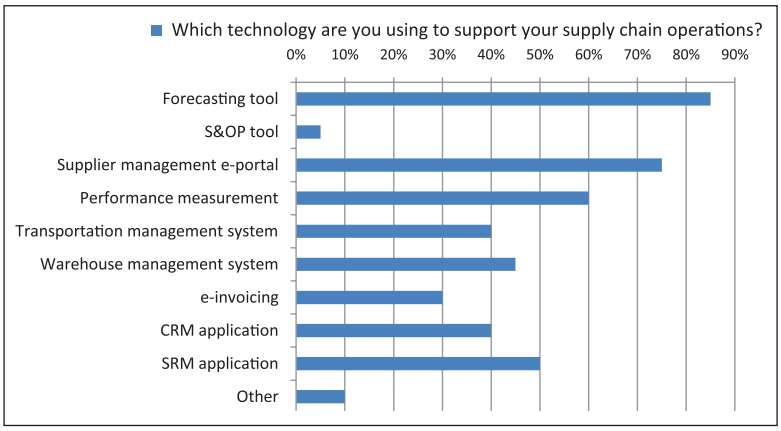
Even though the forecasting tool has been the number 1 system cited, the level of automation is very disparate, spanning from excel spreadsheets to advanced planner and optimizer. Many respondents mentioned using supply chain collaborative portal to fasten communication and improve reliability along the end-to-end supply chain, such as RosettaNet or

in-house developed supply chain enterprise portal. Although widely used, the shop floor production systems were not considered by the respondents as part of the supply chain scope.

Most respondents mention that their effort , for the next six months, will be focused on:

1. forecasting tool (77%)
2. performance measurement (60%)
3. CRM application (60%)

There is also an increasing interest in supply chain finance tools such as e-invoicing / self-billing to optimize the working capital and S&OP tools to enhance the sales & operations process.



Conclusion

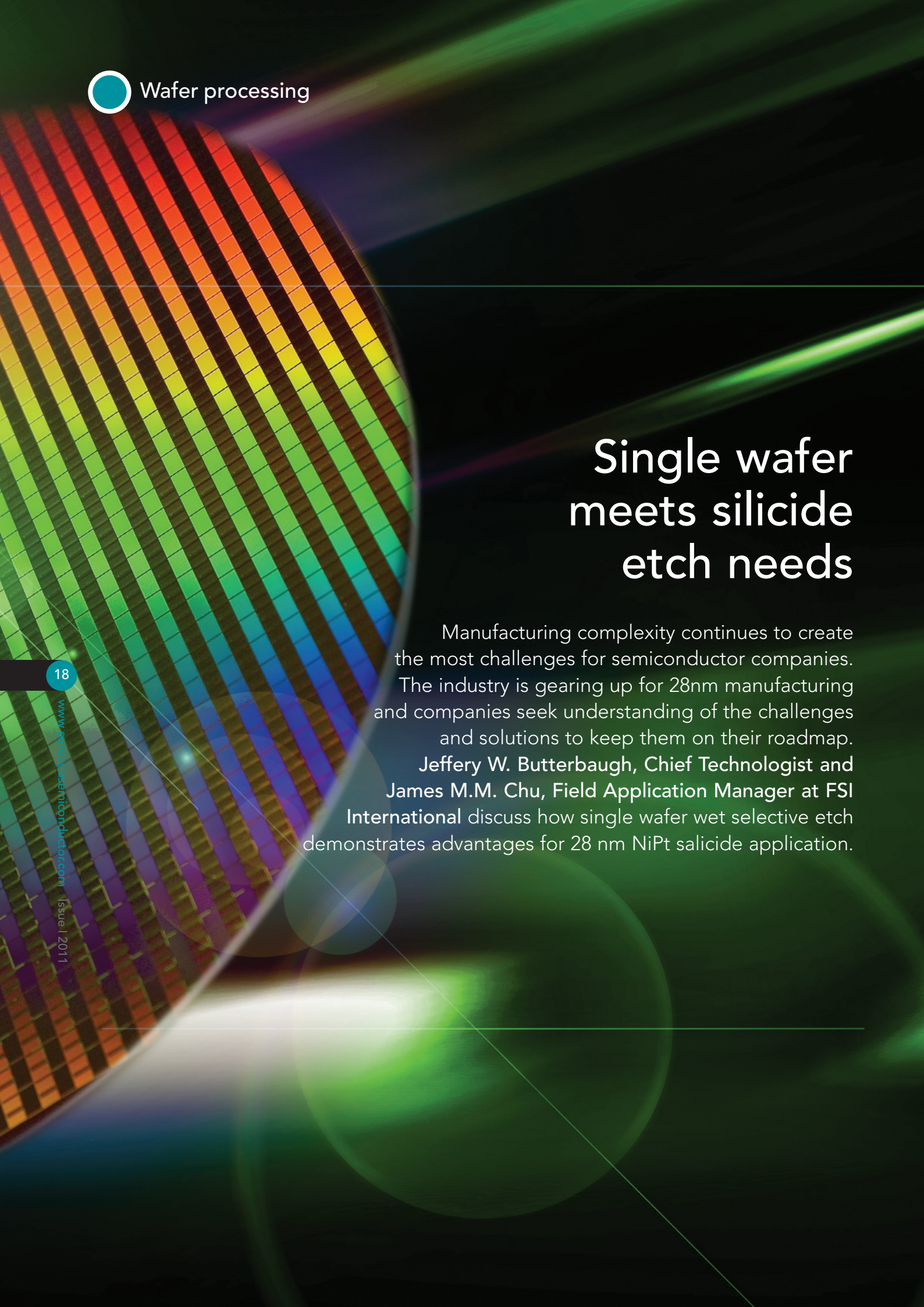
The semiconductor industry has always been focused on process technology, design and manufacturing tools for its advancement. Until recently, managing the supply chain was not very critical to maintaining a company's competitive edge. This could be attributed to a number of factors such as innovation as it is a company's core competency, dedicated and captive manufacturing facilities, fewer products, small package sizes, more demand than supply, and the industry being in allocation mode for a long period of time. The past decade has witnessed a major change in the characteristics of the semiconductor supply chain. The industry experienced supply and demand equilibrium, which oscillated every three to four years. The high capital costs required to start and operate a manufacturing facility, combined with the reduction in average selling prices, made it a challenging environment to operate in. A large number of entrepreneurs had great ideas, but not enough resources to establish a company with manufacturing facilities, so they instead set-up design houses. This one movement was a major contributor to the development of the fabless industry.

The emergence of fabless manufacturing made the supply chain model more complex because a product underwent manufacturing in multiple companies across the globe. It has had its benefits and challenges. It allowed a number of small companies to start operations without having to heavily invest in manufacturing facilities. It also allowed companies to have flexible capacity. On the other hand, this model came with longer lead times and lead time variability saw product proliferation occur, resulting in a larger product mix. In addition, the product lifecycle was getting increasingly shorter, and the pressure to introduce new products to the market every four to six months was getting higher.

The industry also saw product proliferation occur, resulting in a larger product mix. In addition, the product lifecycle was getting increasingly shorter, and the pressure to introduce new products to the market every four to six months was getting higher. As such, the need for greater control of the supply chain has increased and supply chain management has become vital. Many semiconductor companies are now attempting to apply advanced methods and tools for semiconductor supply chain management. However, optimizing this supply chain comes with its own set of business challenges, including:

- Achieving accurate supply and demand picture, by improving predictability and velocity of demand signals
- Leveraging demand variability and improving customer service levels
- Implementing strategies for maximizing supply chain responsiveness
- Sustaining lead-time reduction while reducing inventory
- Integrating shop floor execution for global visibility

This survey shows that there is a substantial gap between best-in-class performers and median companies when it comes to supply chain management. The survey provides practical insights that allows your company to compare itself with others in the industry and identify potential opportunities for improvement. By drawing on the broad experience of the participants, the Survey provides a perspective that can help your company strengthen its ability to use the supply chain as a key driver of high performance.



Single wafer meets silicide etch needs

Manufacturing complexity continues to create the most challenges for semiconductor companies. The industry is gearing up for 28nm manufacturing and companies seek understanding of the challenges and solutions to keep them on their roadmap. **Jeffery W. Butterbaugh, Chief Technologist and James M.M. Chu, Field Application Manager at FSI International** discuss how single wafer wet selective etch demonstrates advantages for 28 nm NiPt salicide application.

The diversification of CMOS process integration at the 28 nm node is driving increases in process complexity and, as a result, manufacturing costs. This is largely due to the introduction of new materials, such as high k dielectrics and metal gates. To the extent that existing processes and materials can be extended to the 28 nm node, the impact of diversification on cost can be limited.

For example, the nickel platinum (NiPt) self-aligned silicidation (salicide) process has been extended as far as 22 nm devices. However, at these smaller dimensions, yield becomes much more sensitive to process variations, resulting in narrower process windows. Any technology that can reopen the process window, providing greater latitude for process variability as well as increased flexibility for tuning the process to specific device requirements, will ultimately improve yields and reduce manufacturing costs.

In a recent study designed to optimize NiPt salicide processing in 28 nm device manufacturing, single wafer wet etch proved to be just such a technology, delivering significantly faster etch rate than batch processing while maintaining uniformity and selectivity over a broad process window [1]. The study evaluated various combinations of film thickness, platinum additive concentration and wet etch processing (single wafer vs. batch) to determine optimal process parameters.

Optimization of thickness and platinum levels yielded a 15x reduction in NiSi encroachment. Both single wafer and batch wet etch processes were effective, however the single wafer process cleared unreacted metal fifteen times faster than the batch process while providing good sheet resistance levels and uniformity. Extended exposure to process chemicals did not degrade sheet resistance (Rs) performance, confirming high selectivity in the etch process. Both its speed and uniformity suggest that the single wafer processor can provide a robust selective etch process and give a larger process window for silicide process optimization with other parameters; such as Pt additive level, rapid thermal processing and NiPt film thickness.

NiPt Silicides

Metal silicides are used to reduce the resistivity of polysilicon (p-Si) gate electrodes and source/drain contacts in CMOS devices. Nickel (Ni), yielding nickel silicide (NiSi), is the preferred metal for silicide processes. The addition of low levels (5%) of platinum (Pt) to form nickel platinum silicide (NiPtSi) offers a number of benefits, including improved thermal stability, reduced nickel migration [2], and lower interface resistance. Increasing the Pt concentration to 10% offers additional benefits. A study comparing 5% and 10% Pt in NiPtSi films having the same thickness demonstrated 50~80% reduction in brightness voltage contrast (BVC) defects (primarily associated with the formation of NiSi pipes) and a 3% improvement in P-FET gain in 28nm devices. However, increasing the Pt concentration increases the difficulty of removing unreacted Pt metal after the silicide formation step.

NiPt silicide is scalable down to 22nm, where it can deliver low sheet resistivity without introducing new materials and processes [3]. However, control of process variation becomes more challenging in 28 nm high volume production since the sensitivity of device performance to process variation increases as critical dimensions decrease [4].

Different device types, for example low power versus high performance, require different integration schemes [5, 6]. Furthermore, since

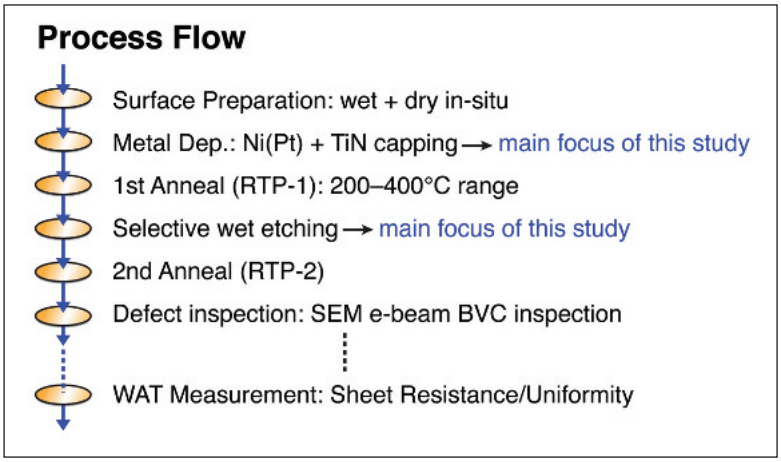


Fig. 1 28nm NiPt salicide process flow

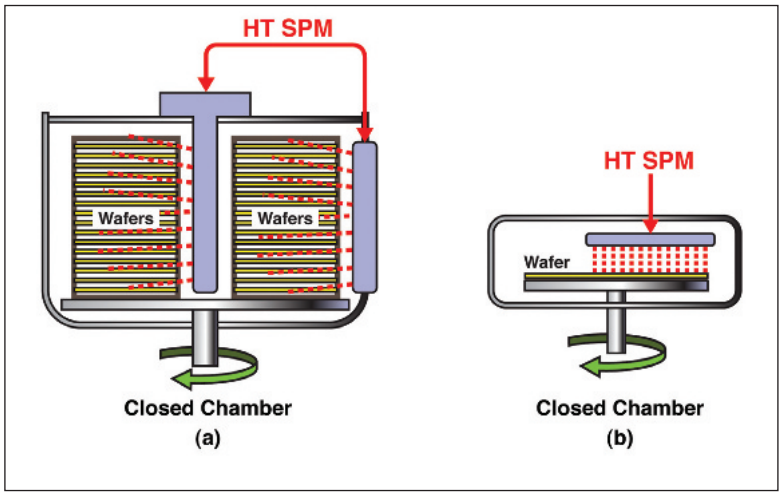
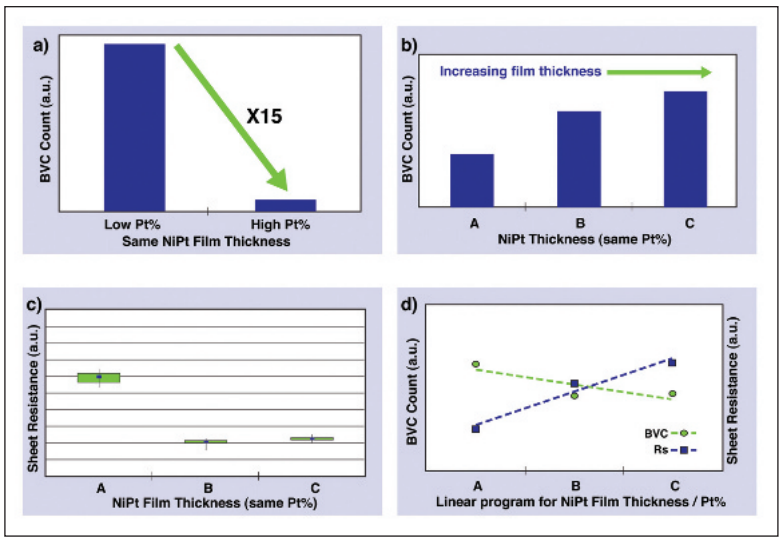


Fig. 2 Wet chemical etch processor comparison (a) Batch wafer type, (b) Single wafer type

NiPt silicide resistivity varies with the feature size and CMOS layout geometry [7], separate optimization of silicide sheet resistance (Rs) may be required not only for different device types but also for different areas within an integrated circuit that have different layout characteristics, such as Poly, Diff, Cell, and I/O.

NiPt film thickness and Pt additive concentration are two variables that may be optimized for specific performance characteristics. Since thicker NiPt films and higher Pt additive both increase the difficulty for the wet selective etch process to clear unreacted metal, these three parameters, thickness, additive concentration and wet selective etch, must be analyzed together in any optimization of NiPt silicide processes.

Fig. 3 (a) Effect of Pt additive level on BVC performance (b) NiPt thickness vs. BVC (c) NiPt thickness vs. Rs (d) linear program for Pt additive to NiPt film thickness for BVC and Rs



Optimizing the process

Test wafers were prepared in a standard 28nm process flow on 300mm wafers with a two-step silicidation process scheme. First, the surface is prepared by wet chemical and in-situ ion bombardment to remove native silicon dioxide; then, a plasma enhanced physical deposition process is used to deposit various thicknesses of NiPt film including a titanium nitride (TiN) capping layer. The wafers then proceed to identical rapid thermal anneal processes (RTP 1) at relatively lower temperature (200-400°C) to form preliminary NiPt silicide. Next, the wafers move to a wet chemical selective etch processor to remove non reacted metal alloy (NiPt/TiN) from the surface and clean the wafer. Finally, an identical thermal process (RTP 2) with higher temperature (> 500°C) is used to form low resistive nickel monosilicide (NiSi) and complete the NiPt salicide process.

A patterned wafer defect scan tool is used to detect defects and an e-beam brightness voltage contrast (BVC) scan measurement tool is used to characterize the NiSi encroachment behavior. The CMOS device electrical performance is measured by in-line automatic prober through standard wafer acceptance tests (WAT). Fig 1 shows the wafer process flow.

Surface preparation and RTP are the same for all wafers, allowing the optimization to focus on NiPt film thickness, Pt additive level and wet selective etch process. For metal film deposition, NiPt (10~20nm, Pt additive 5~10%) and a TiN (1~3nm) cap are used to investigate the effect on the NiPt silicide formation quality. The wet selective metal etch process uses high temperature sulfuric acid and hydrogen peroxide mixture (HT SPM) [8]. Both a batch type processor (FSI ZETA System) and a single wafer type processor (FSI ORION System) are used (Fig. 2) to compare the process efficiency on the different NiPt film deposition conditions. The defect scan is used to characterize the wet etch process result after the RTP 2 step. After contact formation, the e-beam brightness voltage contrast (BVC) method is used to measure NiPt silicide encroachment behavior, which has been shown to lead to higher device leakage [9]. Sheet resistance and uniformity are measured by in-line automatic prober on the Metal 2 layer.

Sheet resistance and defectivity

Two levels of Pt additive in the NiPt alloy are

used in the wafers split with the same deposited NiPt film thickness. The e-beam BVC measurement result is summarized in Fig. 3a. The results show a significantly reduced number of BVC defects detected at the higher Pt additive level, suggesting that the higher Pt level can retard NiSi encroachment and reduce device leakage.

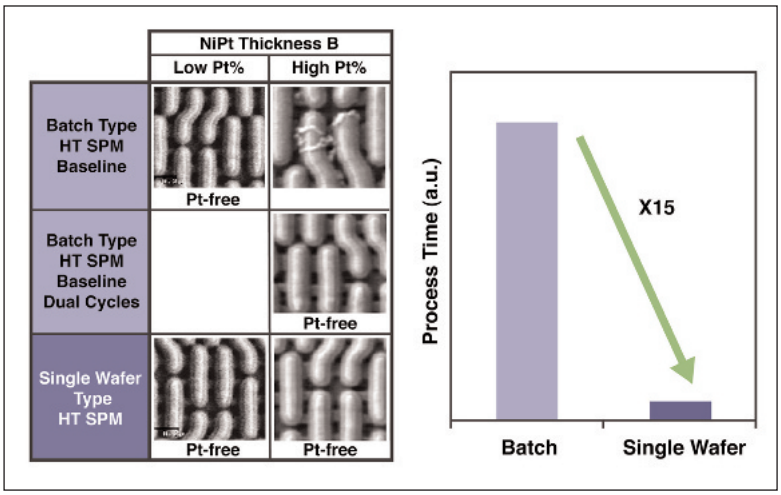
For overall film thickness influence on BVC behavior, three levels of NiPt alloy deposition thickness were split with the same lower Pt additive level. The BVC measurement, summarized in Fig.3b, indicates that thicker deposited NiPt film leads to higher BVC counts. This could be caused by excess Ni atoms, driven into the silicon lattice or along the silicon grain boundaries in the RTP 1 process, that are not able to form a stable silicide phase. Secondary diffusion takes place in following RTP 2 process and results in NiSi encroachment and higher BVC count.

On the same split, the silicide Rs is measured on the M2 layer and the measurement result is summarized in Fig. 3c. The result shows that increasing NiPt film thickness reduces sheet resistance (Rs), but the effect saturates above a certain thickness.

In summary, increasing NiPt thickness, over a certain range, reduces sheet resistance but increases NiSi encroachment, and increasing platinum additive levels reduces encroachment. Therefore, a linear programming approach was used to optimize the film thickness to achieve lowest possible Rs and then improve the BVC performance with higher Pt additive. The co-optimization result is shown in Fig. 3d.

The wet selective etch process will complement various Pt additive and NiPt film thickness and during the determining tests, the time required to clear unreacted Pt is used to characterize the wet chemical etch process efficiency. First, for the same thickness of deposited NiPt, films with higher Pt additive levels take longer to clear (Fig. 4a). In addition, the result shows the single wafer type processor takes much less time to clear Pt (Fig. 4b), providing a 15X improvement compared to the current baseline on a batch type tool.

Three attributes of the single wafer etch system likely contribute to its enhanced performance. First, the system's low-volume closed process chamber, unique among currently available single wafer tools, confines the process



chemicals within the chamber and permits the use of aggressive chemical agents at high temperature. Second, the system dispenses the process chemicals with significant velocity perpendicular to the wafer surface for higher mass transport. Finally, its higher spinning speed (1000 RPM compared to 300 RPM for the batch tool) provides greater mechanical force.

Fig. 4 (a) Process time comparison of batch type to single wafer type wet chemical etch processor. (b) Process cycle time improvement

Selectivity by Single Wafer Processor

To verify the process window, wafers were split with identical high Pt additive; three levels of NiPt thickness (condition A, B, C) and five HT SPM process time settings (90, 120, 150, 180, 210s). The times required to clear the unreacted metal, summarized in Table. 1, verify a broad process window with good clearance over the full range of conditions likely to be used in NiPt

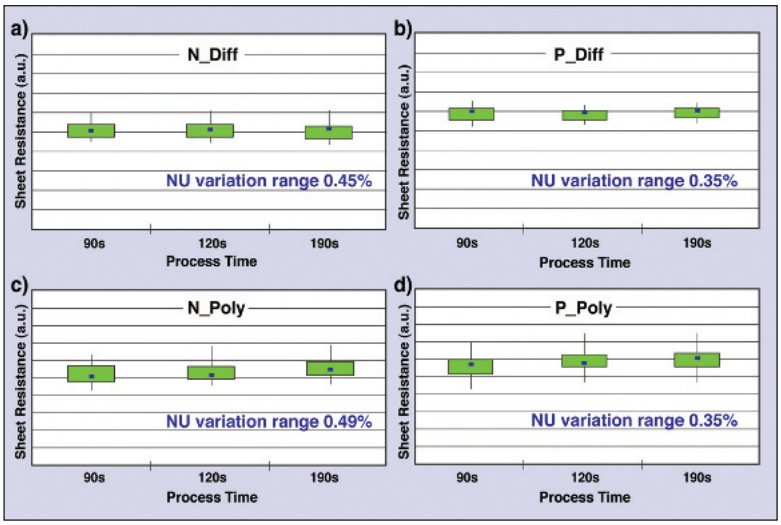


Fig. 5 Rs uniformity variation range by different wet etch process time on (a) N-Diff (b) P-Diff, (c) N-Poly and (d) P-Poly

Table 1 Process window of single wafer wet etch processor over various Pt additive and NiPt film thickness

	SPM Process Time (s)	90	120	150	180	210
High Pt% NiPt Thickness (Å)	A	Pt-free	Pt-free	Pt-free		
	B		Pt-free	Pt-free	Pt-free	
	C			Pt-free	Pt-free	Pt-free

silicide integration. To evaluate the selectivity of the wet etch, the sheet resistance (Rs) of condition A is used to confirm that longer process time (90s, 120s and 150s) does not lead to silicide damage and increased sheet resistance (Rs). The results, summarized in Fig. 5, show the same level of Rs and good Rs uniformity for all explored process times; demonstrating an absence of Rs degradation with extended chemical exposure and confirming good selectivity for the wet chemical etch process. Both time to clear and Rs/Rs uniformity results suggest the single wafer processor delivers a robust selective etch process and provides a larger process window for silicide process optimization with other parameters; such as Pt additive level, RTPs and NiPt film thickness.

Conclusion

NiPt silicide processes can be successfully extended to 28 nm devices in high volume production. Film thickness, Pt additive level and the wet selective etch process must be co-optimized to attain the best combination of sheet resistance and device leakage performance. The results of the optimization show satisfactory Rs performance, a significant improvement in leakage performance (15x reduction in BVC defects indicative of encroachment) and a 15x reduction in wet selective etch process time with single wafer processing.

Importantly, single wafer processing offers a broad process window providing increased immunity to process variability giving engineers greater flexibility in adapting the process to the requirements of varying device designs.

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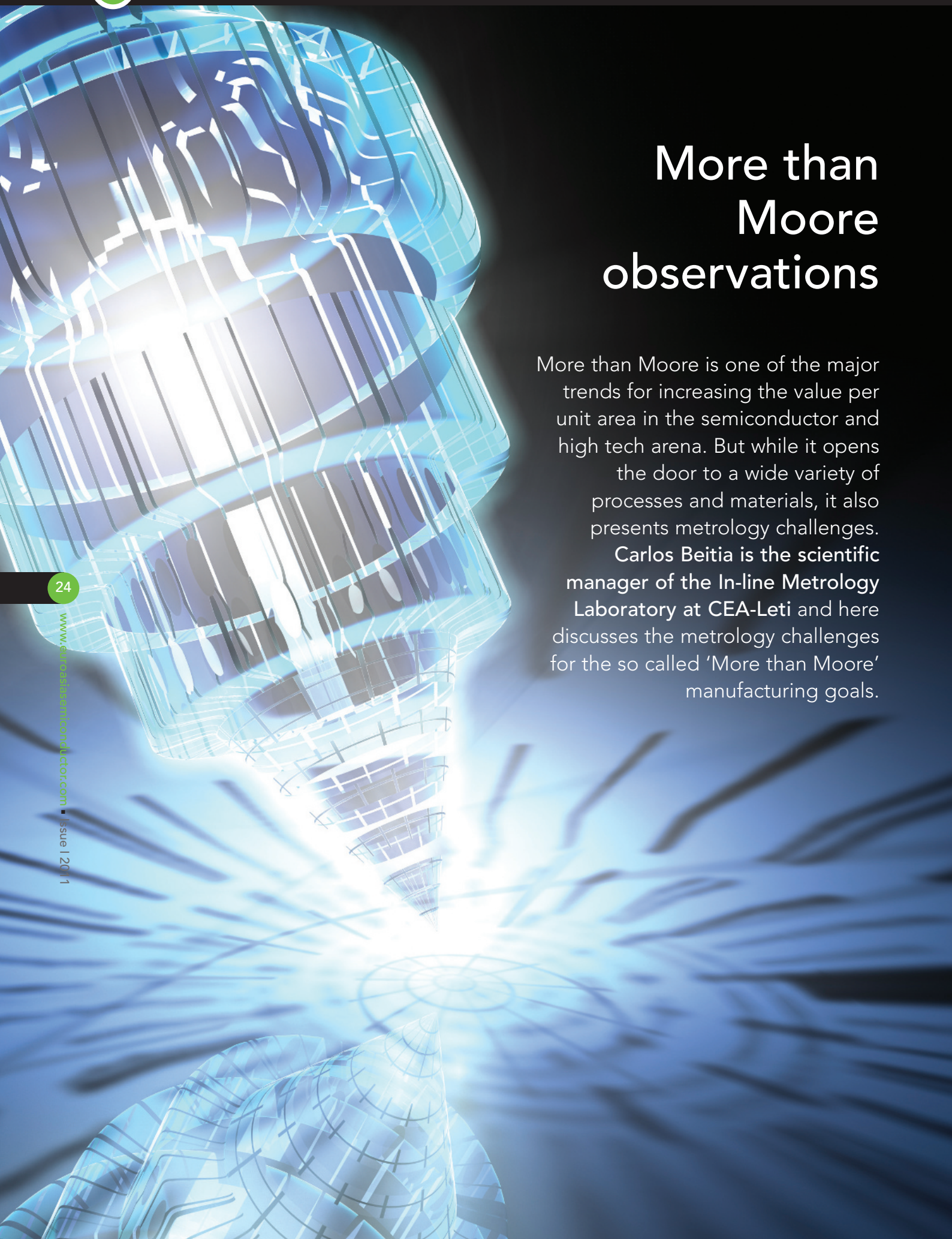


More than Moore observations

More than Moore is one of the major trends for increasing the value per unit area in the semiconductor and high tech arena. But while it opens the door to a wide variety of processes and materials, it also presents metrology challenges. **Carlos Beitia is the scientific manager of the In-line Metrology Laboratory at CEA-Leti** and here discusses the metrology challenges for the so called 'More than Moore' manufacturing goals.

One of the relevant announcements at last summer's ITRS meeting was the presentation of the More than Moore roadmap update together with a white paper draft [1]. Figure 1, from the ITRS document, illustrates the three mains approaches in the semiconductor industry.

This clearly shows consensus between the main actors confirming the trend toward More than Moore. In recent decades, CEA-Leti has developed expertise in this area and today has a toolbox of technologies that allow it to move and lead in innovation in this area [2,3].

Key enabling technologies

Adding and diversifying functions on the IC has to be thought of as a complete system. Roy K. et al [4] proposed the interesting concept of "Micro-computing City" achievable by means of heterogeneous integration. The future IC will be a system of systems where the subsystems (buildings in the city) will be in charge of:

- sensing the outside world (MEMS, NEMS sensors)
- analysing data (lab-on-chip analysers)
- processing and calculation (multicore microprocessors)
- storing data (stacked memory)
- communication with the outside world (RF, Wireless, IR) and
- power management and energy harvesting (μ-fuel cells, nano-materials super-capacitor, MEMS)

All these functions will be connected by an internal hybrid through-silicon via (TSV) wireless network (the city's roads and highways). This concept is pushed to its limits by including redundancy and health-healing subsystems. It focuses attention on technologies that will enable an increase in the number of More than Moore devices going from lab to market. So TSV, wafer thinning (WT), wafer-to-wafer bonding (W2W) as well as MEMS-NEMS technologies are keys. They introduce a wide range of processes and materials that will need characterization, metrology and inspection to insure high yield and reliability.

TSV metrology

Depth value, mask undercut, scalloping shape, filling conformity and voids are important parameters for TSVs and potential metrology and inspection solutions need to address them. All this has to be done with the appropriate statistics and within wafer-uniformity measurements because one important aspect is high density TSVs.

Depending on the aspect ratio and pitch, depth measurements could be more or less problematic. A set of established optical techniques that are new to the semiconductor industry could eventually be the solution. We have evaluated interferometer and confocal techniques. For them, wavelength range, lateral and vertical resolutions and optical setup are important. White light interferometer parallel light displays capabilities of depth measurement on high aspect ratio TSVs (Figure 2).

Chromatic confocal microscopy has also shown some capabilities. However, for both of them the question whether they will have the capability to look at TSV shape details like mask undercut, CD measurements and scalloping remains to be answered. Some backside interferometer infrared studies also have been realized but need further development in order to improve resolution of vias in array depending on their pitch [5]. Another problem that cannot be addressed easily is the metal filling conformity and voids presence. X-ray and acoustic tomography look promising for this but they require more effort in taking them to an in-line platform level. The FIB slide-and-view method is available but has the disadvantage of

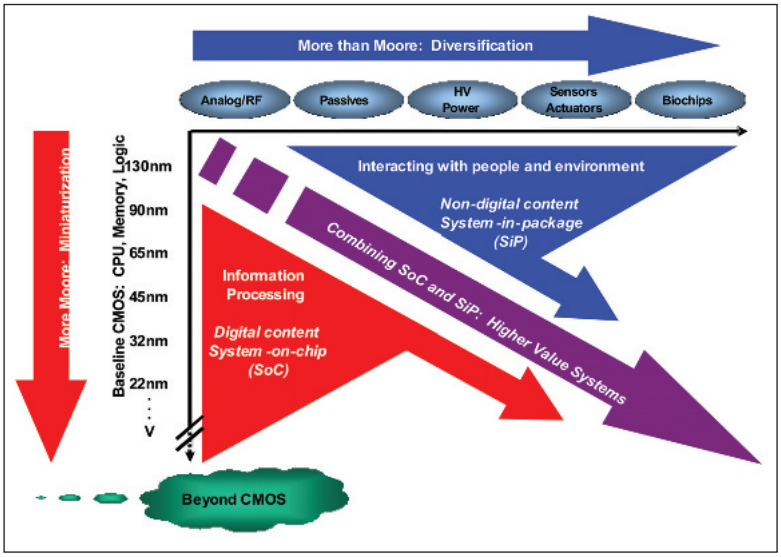


Fig. 1 - ITRS roadmap trends

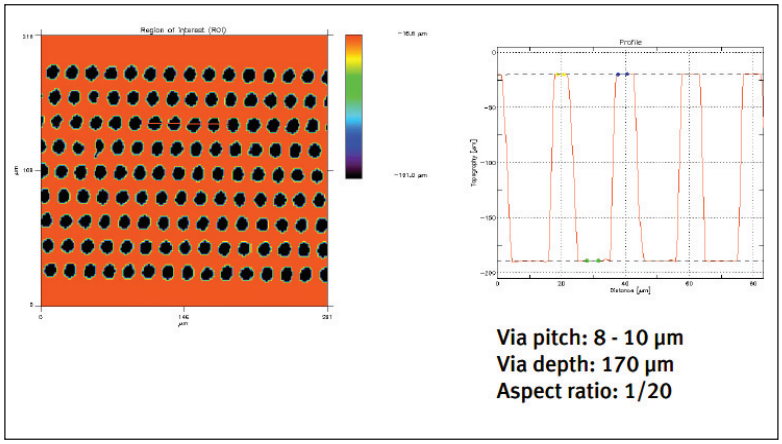


Fig. 2 - White light interferometer parallel light in high aspect ratio vias

being destructive and at the same time compiling statistics is too expensive.

Wafer thinning and wafer bonding

Heterogeneous integration also introduces the mixture of different kinds of substrates in the same devices, such as III-V substrates used for power devices or glass and sapphire used for lab on chip. In addition, to have reasonable thickness while stacking several heterogeneous devices, each of the integrated stacks has to be thin enough. This requirement creates carrier handling and bonding challenges. Consequently, control of properties like total thickness, total thickness variations, bow and warp has to be performed in order to insure the proper process performances.

Capacitance measurements, even if they are very well suited for silicon substrates, lack on versatility for other materials. Double-sensor chromatic confocal microscopy could be a good technique for managing such a diversity of materials.

It partially avoids dependence in optical properties of the material stacks compared to interferometers. The former exhibits measurement-artifact problems each time we have optical properties of material variation, as well as when we measure transparent materials. But, lately some improvement has been achieved to take into consideration material properties and interface problems [6]. Another problem requiring attention from metrologists is the control of bonding quality. Acoustic microscopy is a real help detecting voids and delamination problems. However, a wider use of this technique might be limited by the fact that it requires working in liquid.

The use of techniques like TEM, SEM for observation of Cu-Cu interfaces from room temperature bonding process is also of interest. In addition, coupling them to spectroscopic analysis like EELS and EDX is an added value. Figure 4 shows copper-oxide nodules evidence at the Cu-Cu interface using EDX [7]. Leti is investigating quantification improvement by means of principal components analysis coupled to model based quantification on EELS spectra analysis.

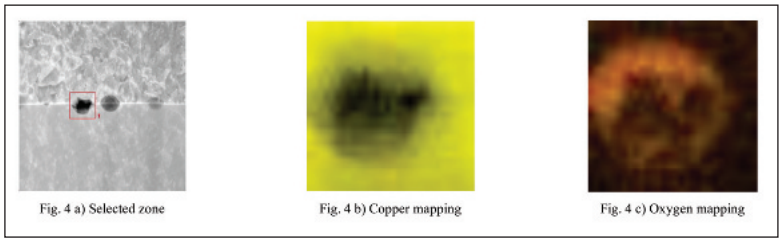
Wafer-to-wafer alignment needs to address such a variety of substrates; infrared microscopy for silicon is currently done with appropriate sample preparation for metal but will need more automation. We are also facing more basic problems like being able to handle such a diversity of materials (polymers, glass, sapphire etc.) and wafer thickness (~100 µm up to ~3 mm). Systems with Bernoulli end effectors for non-contact wafer handling might be a solution.

MEMS and CMOS metrology cohabitation

3D heterogeneous integration in the More than Moore approach has to deal with the MEMS integration, as mentioned above. This yields to the cohabitation problem between CMOS and MEMS metrology. In order to optimise and rationalise cleanroom space and cost of ownership of the metrology tools, techniques have to cover the widest range of material, scales and applications. So, thickness and optical-characterisation tools for CMOS applications like spectroscopic ellipsometry and reflectometry will be challenged to measure very thick transparent materials.

They will need to have improved spectral resolution and extended wavelength range in order to be able to resolve interference fringes and get thickness information; even then, we will face SE limits. (Figure 4 shows typical spectra for reflectometry in a thick layer). To fill the gap, we have seen the appearance of different flavours of interferometer techniques.

Fig. 3 - EDX mapping of a ~20 nm nodule (400°C 30 minutes post bonding anneal)



Some of them have already moved from the lab to production line, like sense pupil plane white light interferometer. However, imaging ellipsometry and confocal spectral interferometer (with Fourier transformed white light interferograms analysis) are interesting candidates to keep in mind and evaluate [8].

Another major trend we are seeing is the increasing need for mechanical characterization. Stress integration problems are related to the mechanical strain induced by thinning and TSV opening, but as well as the global thermal budget in such a heterogeneous material stack. Thus techniques like Raman and chromatographic ultrasonic picoseconds will play an important role as references, while other faster and easy-to-implement techniques like interferometers might serve for monitor and control process. All these techniques will have to include standard semi-compliant measurements for bow in order to properly address stress determination.

Last but not the least, there is the issue of contamination from the interaction between the MEMS and CMOS worlds. In fact in MEMS processes, we are looking through the whole Mendeleev table for new and interesting properties. For example, noble metals like gold and platinum are currently used for MEMS but they impact at trace level CMOS performances. So, cross contamination is a real issue and more strict controls should be put into place. However, we expect some detection and collection problems for noble metals for techniques like VPD-TXRF or VPD-ICPMS, which are needed for such low detection levels [9].

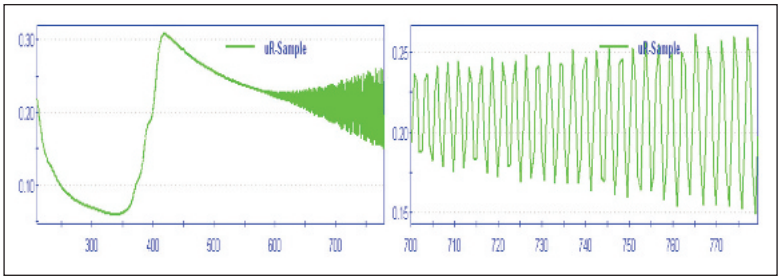


Fig. 4 - Reflectometer data on thick 70µm transparent layer

It is clear that we are witnessing a shift in importance in the high technology sector from More Moore to More than Moore. Due to their very important roles, TSV and wafer bonding technologies are becoming almost synonymous with or 3D heterogeneous integration. CEA-Leti underscored its commitment to this area with the opening of its 3D-300 mm line this year.

In the future, we will see more instances of where new materials will have to cohabitate with traditional CMOS materials, and metrology will have to adapt to CMOS, MEMS and integration specific needs.

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European sales up 27.4% in 2010

ACCORDING the WSTS report from January 31st semiconductor sales on the European market for 2010 were up 27.4 percent compared to the previous year. Fourth quarter sales in Europe increased by 2.1% versus the previous quarter. In all other regions seasonal effects led to a small decrease quarter over quarter.

In Europe remarkable positive growth rates were observed throughout the year for some of the main product categories, in particular for discrete, optoelectronics, total analog and MOS microprocessors.

Among application specific chips, devices used in consumer and automotive applications showed the biggest growth rates in the year 2010. Overall the European semiconductor sales in December 2010 amounted to US$ 3.301 billion which represents 13,1 % of the worldwide market. For 2010 in total the European share summed up to US$ 38.054 billion.

Measured in Euro the semiconductor sales in Europe totalled at 2.429 billion Euros in December 2010, 4.0% down compared to November 10 and 22.1% up versus December 2009. Due to the strong US$ in 2010 the year over year increase of the semiconductor sales in Europe expressed in Euro increased even by 34.7%.

On a worldwide basis, semiconductor sales in December 2010 were at US$ 25.154 billion, seasonally down 3.0% versus the previous month. For 2010 in total the sales summed up to US$ 298.315 billion.

Comparing the last quarter 2010 to the last quarter in 2009 the semiconductor sales show an increase of 12.2%, year over year the sales went up by 31.8%.

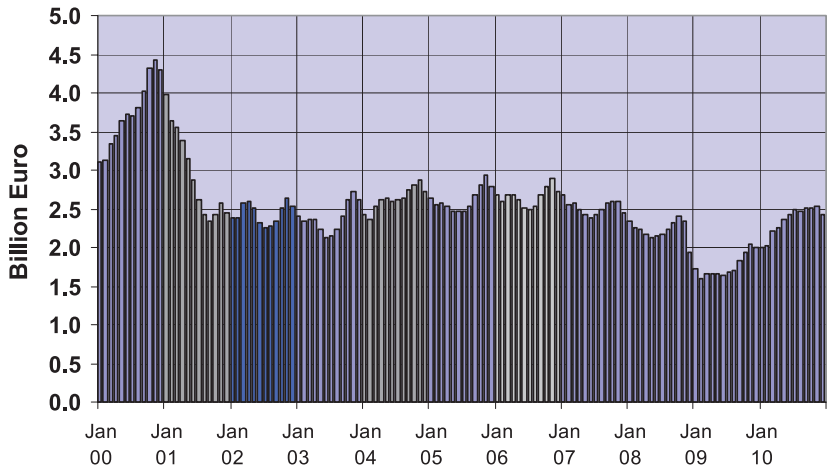
All data kindly supplied by EECA-ESIA and WSTS: ESIA

Market data by region (Net Billings for total semiconductors) 1)

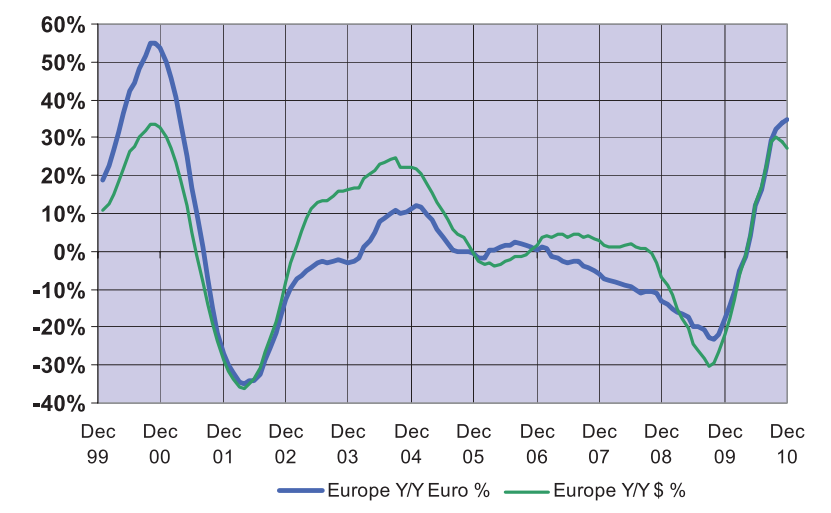
Market data for the 3 month moving average ending:								
Region	sales (in billions)		Month on Month growth		Year on Year growth		YTD growth	
	Nov 10	Dec 10	Nov 10	Dec 10	Nov 10	Dec 10	Nov 10	Dec 10
in $:								
Europe	3.419	3.301	2.4%	-3.4%	13.2%	12.1%	28.7%	27.4%
Americas	4.705	4.573	-1.8%	-2.8%	21.1%	19.3%	41.2%	39.3%
Japan	4.159	3.967	-1.0%	-4.6%	8.2%	9.8%	22.4%	21.6%
Asia Pacific	13.645	13.313	-1.6%	-2.4%	14.1%	10.6%	36.8%	33.8%
of which China	5.537	5.362	-0.5%	-3.2%	17.4%	11.4%	41.8%	38.5%
World	**25.927**	**25.154**	**-1.0%**	**-3.0%**	**14.2%**	**12.2%**	**34.0%**	**31.8%**
In EURO:								
Europe	2.532	2.429	0.5%	-4.0%	23.6%	22.1%	35.3%	34.7%
Rate ($/Euro)	1.369	1.321	-8.1%	-9.9%	< Euro against $ versus prev. Year			

1) Unless otherwise indicated, all figures are 3-month-average data except YTD growth

EUROPE - Monthly European Semiconductor sales in billion Euro
(3-month-average data)



European Semiconductor sales growth in % - Annualized growth trend (Y/Y) in Euro and Dollar
(12-month-average data)



Lasers and Moore's Law

Lasers have been a key part of semiconductor manufacturing from the start and the importance to the industry only increases as the industry seeks to stay on the track determined by Moore's Law. **Bruno La Fontaine, senior director of EUV lithography applications at Cymer** provides an overview on the use of lasers in manufacturing to keep the industry on the desired track.

During the last four decades, society has seen an explosion of the capabilities of microelectronics devices, such as computing power and data storage capacity. This tremendous improvement in performance has had a profound impact on the global economy and almost all areas of human activity.

At the heart of this improvement is the exponential increase in the number of devices on semiconductor chips over time, as described by Moore's Law. The principal factor enabling such scaling has been the relentless progress of lithography.

To achieve a higher density of devices on a microelectronics chip, which leads to faster switching times, larger memory and lower cost, the circuits need be delineated with a finer and finer brush. In optical lithography, the size of this brush, or the resolution, is defined by the following equation:

$$W = k_1 \frac{\lambda}{NA}$$

In this equation, ω is the width of the finest feature that can be resolved in a dense pattern, λ is the wavelength of the light source used, NA is the numerical aperture of the lens used to image the circuit patterns onto the silicon chip, and k1 (known as the k-factor) is a factor describing the ability of the recording process to resolve small features.

While the lens of the lithographic exposure tool dictates the NA, and the photoresist process used largely determines the minimum achievable value of k1, it is the light source that defines the wavelength used. As such, the progression to light sources with shorter and shorter wavelengths is a key driver of the miniaturization of microelectronics devices.

Overall improvements in resolution typically follow this trend. For a given wavelength, the lens NA is increased and the k-factor reduced. Once the cost of increasing the lens NA or reducing the k-factor is deemed excessive, a shorter wavelength is introduced.

End of mercury arc lamps

Initially, mercury arc lamps were used as light sources of lithography exposure tools. Narrowband filters were used to select single emission lines. The g-line (λ = 436 nm) was used first until i-line (λ = 365 nm) lithography was adopted for production in the late 1980s.

Below 365 nm, the choice of optical materials became much more limited and chromatic aberrations could not be compensated as effectively in the lens design.

This led to the introduction of excimer lasers, which have a significantly narrower bandwidth than the mercury arc lamps. Krypton-Fluoride (KrF) lasers (λ = 248 nm), introduced in the late '80s as lithography sources, became broadly used in the mid-1990s. Argon- Fluoride (ArF) lasers (λ = 193 nm) were introduced in the late '90s but were used more widely starting at the 90 nm node (around 2003) for patterning critical layers.

Since the introduction of excimer lasers as lithography light sources, their performance has improved greatly in two key areas: power and bandwidth.

The higher power levels enable higher productivity (throughput) while narrower spectral widths reduce chromatic aberration, providing better resolution and larger depth-of-focus. Since their introduction, the spectral power metric (power/bandwidth) of KrF and ArF lasers has increased by 20x and 100x respectively (see Figure 1).

This trend has required significant development of new technologies to maintain or improve laser component lifetime and to maintain stable operation at higher power levels.

The first KrF lasers for lithography operated at 500 Hz, a power of 5 W, and had a bandwidth of 3 pm. Nowadays a state-of-the-art 193 nm light source, such as the Cymer XLR 600ix, operates at a repetition rate of 6 kHz, a power of up to 90 W, and has an E95 integral bandwidth of less than 0.35 pm over its entire lifetime (see Figure 2).

The development and introduction of two-stage Master Oscillator Power Amplifier (MOPA) sources enabled this continued power and the spectral power-scaling required to support higher productivity, high-resolution 193-nm exposure tools. Scaling is enabled by generating the narrow bandwidth light at lower power in one chamber (MO) then amplifying the power in a second chamber (PA) while retaining and stabilizing the spectral characteristics.

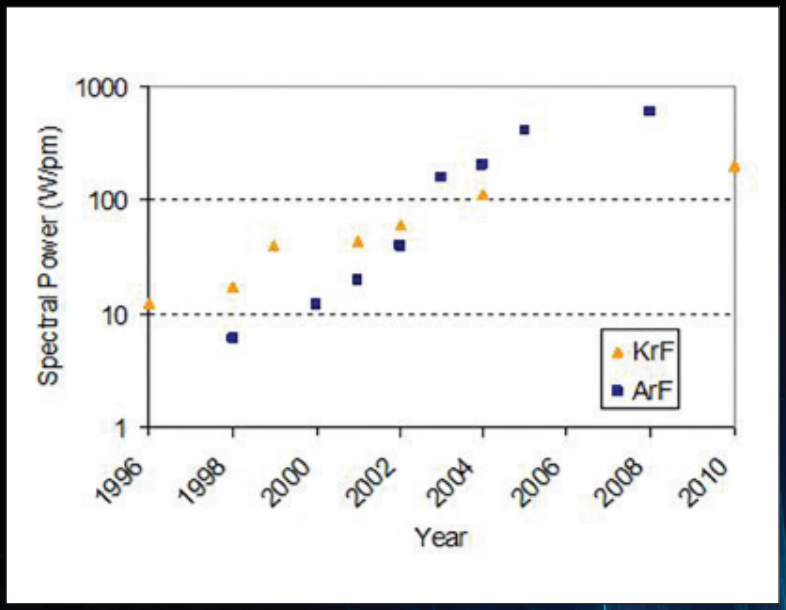


Figure 1: Evolution of spectral power for KrF and ArF excimer lasers

Excimer laser developments

Recent excimer laser developments continue to support the race to manufacture circuits of ever-increasing density. With hyper-NA (NA=1.35)

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immersion lithography being the last ArF-based lithography solution to be used in production, the k-factor is being pushed to its limits and the lithography process control becomes excessively difficult.

The active control of the laser bandwidth allows lithographers to match the critical dimensions (CDs) of various features on their chips, for different exposure tools over time. This is based on the fact that the projected or aerial image of different features has a systematic dependence on the level of chromatic aberrations, which can be adjusted through bandwidth control.

In a similar fashion, the laser can be tuned to larger bandwidth values to provide larger overall depth of focus for specific circuit layouts. This application, known as laser focus drilling, works especially well for 2D features where the contrast of the aerial image is very good at best focus but tends to deteriorate rapidly at out-of-focus conditions. By deliberately introducing a larger spectral width, chromatic aberrations in the lens generate a series of aerial images at a broader range of focus positions, improving the overall depth of focus at a very modest expense of image contrast.

Pushing ArF immersion lithography further requires the use of double-patterning techniques, which is based on more than one exposure per level and potentially reduces the throughput of the lithographic process. ArF lasers with higher power levels are being developed to help maintain a high level of productivity when using double-patterning techniques.

EUV lithography challenges

Although ArF immersion has extended optical lithography beyond expectations through double patterning techniques, it has come at the price of higher process cost, complex restricted design rules, and the explosion of mask costs. EUV lithography offers the promise of a much simpler lithography process (single exposure, large k-factor and greater depth-of-focus).

One of the key challenges of EUV lithography is throughput. Because the reflective optics used for this technology has a finite reflectivity of approximately 70%, the transmission of the light from the source to the wafer, which is typically achieved with more than

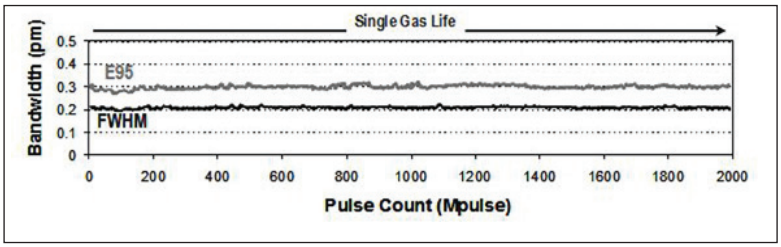

Figure 2: Bandwidth stability over 2 billion pulse gas lifetime. (FWHM: full width at half of the maximum energy; E95: bandwidth containing 95% of the laser energy)

11 reflections, is very small. This puts stringent power requirements on the EUV lithography light source.

EUV sources capable of delivering sufficient power to support high-volume manufacturing are achieved using laser-produced plasmas (LPPs). The LPP source uses a pulsed high-power RF-pumped CO2 laser system (>10 kW power) operating at a wavelength of 10.6 μm and repetition rates of typically 50 kHz. The laser beam is focused to a waist diameter of ~100 μm onto tin-droplet targets inside a vacuum vessel. A droplet generator produces droplet sizes of about 30 μm in diameter at the same repetition rate as the laser. The small droplet size minimizes the cost of the tin fuel and improves the effectiveness of debris mitigation by reducing the quantity of residual tin within the source chamber.

Droplets are generated at a speed in excess of 60 m/s with inter-droplet timing stability better than 0.2% of the period. Droplet position

Figure 3: First LPP EUV source for use in commercial EUV exposure tool, shown here integrated in an ASML NXE:3100 scanner

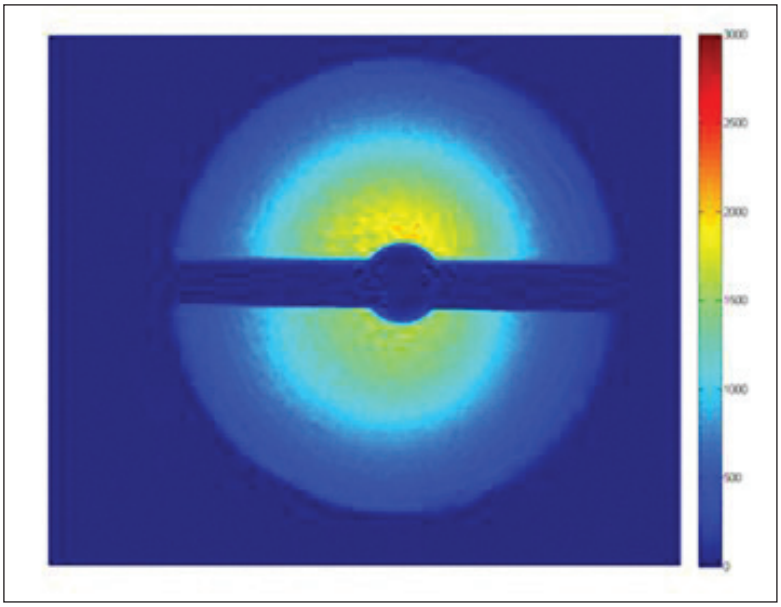

Figure 4: EUV light reflected by the multi-layer collector, past the intermediate focus (IF) point

is controlled with a closed-loop steering system using a feedback signal from targeting cameras in the plasma chamber. When irradiated by the laser, each tin droplet is evaporated, ionized and heated to the optimal temperature at which the plasma produces EUV photons most efficiently. These photons are collected by a multi-layer coated ellipsoidal collector mirror, covering approximately 5 sr solid angle, and refocused to a point known as the intermediate focus (IF) where they can be used by the lithography exposure tool.

Debris mitigation consisting of a hydrogen gas curtain is incorporated to protect the multi-layer coating on the collector from tin deposition and etching due to plasma ions, both of which would result in reflectivity loss and ultimately reduce collection efficiency and power output.Earlier this year, Cymer shipped the first LPP EUV source for use in commercial EUV exposure tools to ASML. This EUV source is integrated in an ASML NXE:3100 scanner at their facility in Veldhoven, The Netherlands. Since then, Cymer has shipped a total of three EUV sources to ASML, with an additional source installation at a chipmaker to take place in the near future.

An image of the EUV light reflected by the multi-layer collector, past the IF point (see Figure 4). The EUV exposure power produced by this source is currently of the order of 10-20 W and is expected to be 40W in the first quarter of 2011 and exceed 100 W by mid-2011. Second- and third-generation sources are planned with clean EUV exposure power levels exceeding 250 W and 350 W, respectively. These are expected to support high-volume manufacturing starting in the 2012-2013 timeframe.

Volume and cost considerations

The need for cost-effective lithography drives high productivity from the lithography exposure tool and high power from the light source, whether it is an excimer laser or an EUV laser-produced plasma source.

Excimer laser power and performance has contributed to the outstanding gains in lithography productivity and extendibility over the last two decades. The successful development of current EUV LPP source technology is the beginning of a similar journey from development to high volume manufacturing that will enable the continuation of Moore's Law.

● The author acknowledges the input of Nigel Farrar, Daniel Brown, David Brandt of Cymer.

Droplets are generated at a speed in excess of 60 m/s with inter-droplet timing stability better than 0.2% of the period. Droplet position is controlled with a closed-loop steering system using a feedback signal from targeting cameras in the plasma chamber

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Listening to error

Acoustic methods of observation have become more important to semiconductor manufacturing as the industry moves to smaller geometries requiring greater observational techniques without damaging the device. **Tom Adams, a consultant for Sonoscan** looks at critical acoustic imaging of flip chip solder bumps and underfill.

Far more than most other surface-mounted components, flip chips are vulnerable to field failure caused by very tiny gap-type packaging anomalies such as delaminations, voids and cracks. Broadly speaking, a delamination in a PQFP or SOIC must be relatively large - depending on its location - to present much of a reliability threat. For many plastic-encapsulated microcircuits (PEMs), delaminations or other gap-type anomalies larger than 150 microns are the ones that assembly engineers worry about.

Flip chips, though, can be disabled by a void with a diameter as small as 20 microns, or by very small cracks and delaminations. For such anomalies, the critical parts of the flip chip "package" are the underfill layer and the solder bumps, and the immediately adjacent layers of circuitry on the die. These are the regions where acoustic micro imaging is used to hunt out delaminations and other defects. Because many flip chips are key processors in relatively expensive assemblies, acoustic imaging is commonly used during the development of a new flip chip device, and prior to mounting on a printed wiring board. During development the goal is to isolate the process parameters that are causing the defects. During production the goal is to remove flawed flip chips before assembly.

Acoustic systems pulse VHF or UHF ultrasound down through the back side of the silicon and receive the return echoes, from which

an acoustic image is assembled. The transducer that is raster-scanning the back side of the die carries out its pulse-echo function thousands of times per second. The silicon through which the ultrasound is pulsed sends back no echoes (which are returned only by the interfaces between materials) except in the very rare instance where there is a crack in the silicon.

Gap pulse

The real targets of the ultrasonic pulse are gaps between a solder bump and its pad, a crack in the body of a solder bump, delaminations between the underfill and either the die face and the substrate, and voids (trapped bubbles) in the underfill. All of these are gaps - meaning that they include an interface between a solid and a gas such as air. The solid-to-gas interface sends back return echoes of the highest possible amplitude, which is actually >99.99% of the pulsed ultrasonic energy that strikes the solid-to-gas interface.

In some flip chips ultrasound makes images of cracks in the very thin, very fragile regions of low-k dielectric material underlying circuits on the face of the chip or of delaminations in the passivation layer, but in most cases the targets for acoustic imaging lie within the underfill material and the solder bumps.

In searching for gap-type defects at the underfill/solder bump depth, the operator of an acoustic microscope may begin by including the entire thickness of the underfill and bumps (or more precisely all of the underfill and bumps plus a small portion of the die face and substrate) to make the acoustic image. He does this by setting a gate based on the arrival time of the return echoes; i.e., by using only the return echoes whose arrival time indicates that the interface from which they were reflected lies within the desired depth range. In the acoustic image individual solder bumps are normally more or less medium gray (solid-to-solid interface). If one solder bump is white, the operator knows that this solder bump has a crack or disbond and is defective.

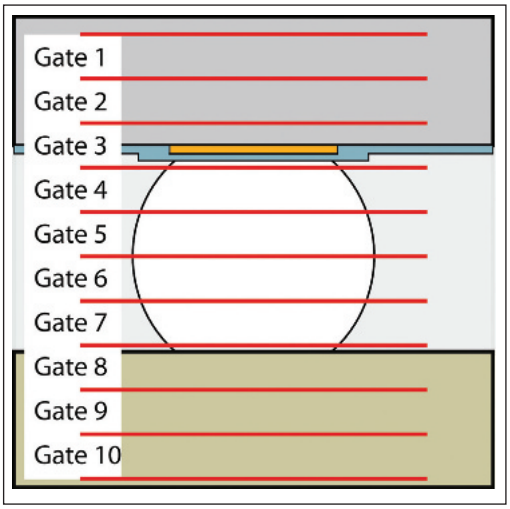

Figure 1: Return echo signals from each gate are used to make an acoustic image limited to that gate's z dimension

Depth determination

What the operator does not know is the precise depth of the defect. It might be at the very top of the bump, where it is disbonded from its pad. Or it might be at the pad on the substrate. Or it might be a crack in the body of the bump anywhere between the die and the substrate. The "defect" might even consist of multiple cracks at different depth within the bump. These cracks will appear as a single feature if gating encompasses the entire height of the bump. To learn the vertical location of the defect, the operator needs to use a narrower gate.

He can do this manually, one gate at a time, but the work would be time-consuming. Multiple gates are more conveniently set automatically, and from a single scan of the flip chip. On the control screen, the operator divides the waveform representation for the overall depth of interest into the number of gates that he thinks will give the most diagnostic data. He can select a handful of gates, or as many as 100. The gates can be adjacent, or they can overlap. He will wind up with as many images as there are gates. Simply looking at the images in sequence lets the operator see features, including defects, from top to bottom. The vertical location of the bump crack can now be determined precisely.

The diagram in Figure 1 shows in side view 10 equally-spaced, non-overlapping gates that will produce 10 acoustic images. The acoustic image from gate 5, for example, will not include echoes from gate 4 or gate 6. But if there is a gap-type defect such as a crack in gate 4, some of the echoes returning from gate 5 will be blocked by that crack. The gate 5 image will show the outline of the gate 4 crack as a dark shadow.

Figure 2 shows the acoustic images from gates 4, 5, 6 and 7 in a small area along one edge of a flip chip. The 10 gates were arranged as shown in Figure 1, so that the gates at the

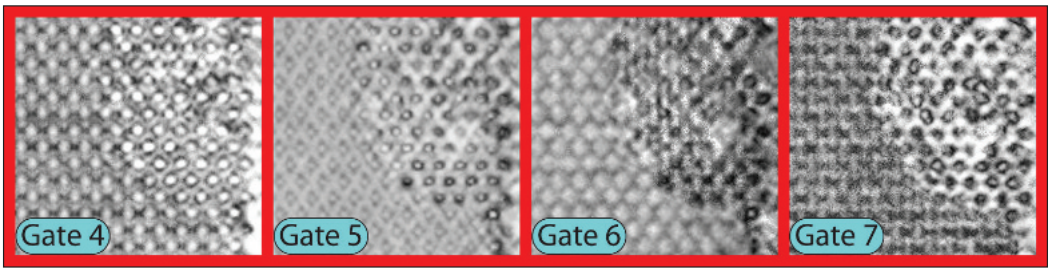

Figure 2: Images from gates 4 through 7 of a flip chip reveal the changing extent of a void and the depths at which individual solder bumps have been cracked by the void

top and bottom of the group are in the die and substrate respectively. These images were made with a 230 MHz transducer designed and built by Sonoscan. Gates 4, 5, 6, and 7 encompass most of the underfill; small portions of gates 3 and 8 capture the top and bottom of the underfill. Gates 1 and 2 cover the die, while gates 9 and 10 cover the substrate. The underfill thickness is about 60 microns, and each gate within the underfill has a vertical extent of about 15 microns. In terms of the travel time for the ultrasonic pulse, the whole underfill has a thickness of about 40 nanoseconds and a single gate has a thickness of about 10 nanoseconds. In some materials, Sonoscan has been able to achieve meaningful imaging with gates as narrow as 1 nanosecond.

Feature focus

The images in gates 4, 5, 6 and 7 reveal these features:

- In the gate 4 image, both the solder bumps (small circles) and underfill are brighter in the right portion of the image. This brightness of the underfill is the first suggestion of a large void that lies at and below the gate 4 depth. The void was not visible in the images made at gates 1, 2 and 3.
- In gate 5, the underfill is still brighter than in areas to the left, but the solder bumps range from bright to dark. It is common for voids to cause cracks in solder bumps. This void may have an irregular vertical topography that has varying local impact on solder bump integrity.
- In gate 6 more solder bumps have a dark color as imaging move deeper into the body of the void. At this depth, some of the solder bumps probably appear dark because they have cracks above the gate 6 depth that cast shadows.
- In gate 7. the bright color of areas between the solder bumps suggest that the underfill material was replaced by air at this depth during the underfilling process. Most of the solder bumps appear cracked at this depth.

Conclusion

The techniques described here have two advantages. First, multiple gates can be generated from a single scanning of the flip chip by the transducer. Parameters for the gates can be set quickly, and the method is compatible with high-speed transducer scanning and high-throughput handling of parts.

Second, the use of multiple gates tells the operator not merely the x-y extent of a feature, but also its vertical position. For example, setting a single gate that includes the entire underfill/bump layer may show that a bump contains a crack. But setting multiple gates and obtaining multiple gate-specific images may reveal that the bump actually has three separate cracks at different depths.

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Industry to bound into new year

KPMG has released its sixth global semiconductor survey and finds optimism for 2011 from industry executives with increases in key semiconductor indicators including workforce but execs are mixed on when latest growth cycle will peak.

Despite the uneven overall global economic recovery, semiconductor executives see their industry breaking the historical boom-and-bust performance trend in the short term with solid increases expected in 2011 in sales, and most importantly, workforce growth.

However, according to KPMG's global survey of 118 senior level executives in the semiconductor industry, 53 percent of respondents anticipate the semiconductor cycle will peak within the next 12 months, ultimately reinforcing the inherent cyclicality of the industry.

Historically, the semiconductor's industry's largest boom years are followed by sharp declines in the next year. Yet, the industry appears confident that continued product demand in 2011 will break that pattern, even as it follows a 2010 year that many analysts are forecasting as the third highest ever in the semiconductor industry.

In fact, according to the survey, 78 percent of global semiconductor executives expect that revenue will grow by more than 5 percent next year. This is a sign of resiliency, as 87 percent of 2009 respondents projected similar revenue increases for 2010.

In looking at the jobs picture, 29 percent of the respondents predict workforce growth of greater than 5 percent, compared to 23 percent in 2009 and 17 percent in 2008 - reflecting increased confidence in the resilient semiconductor industry.

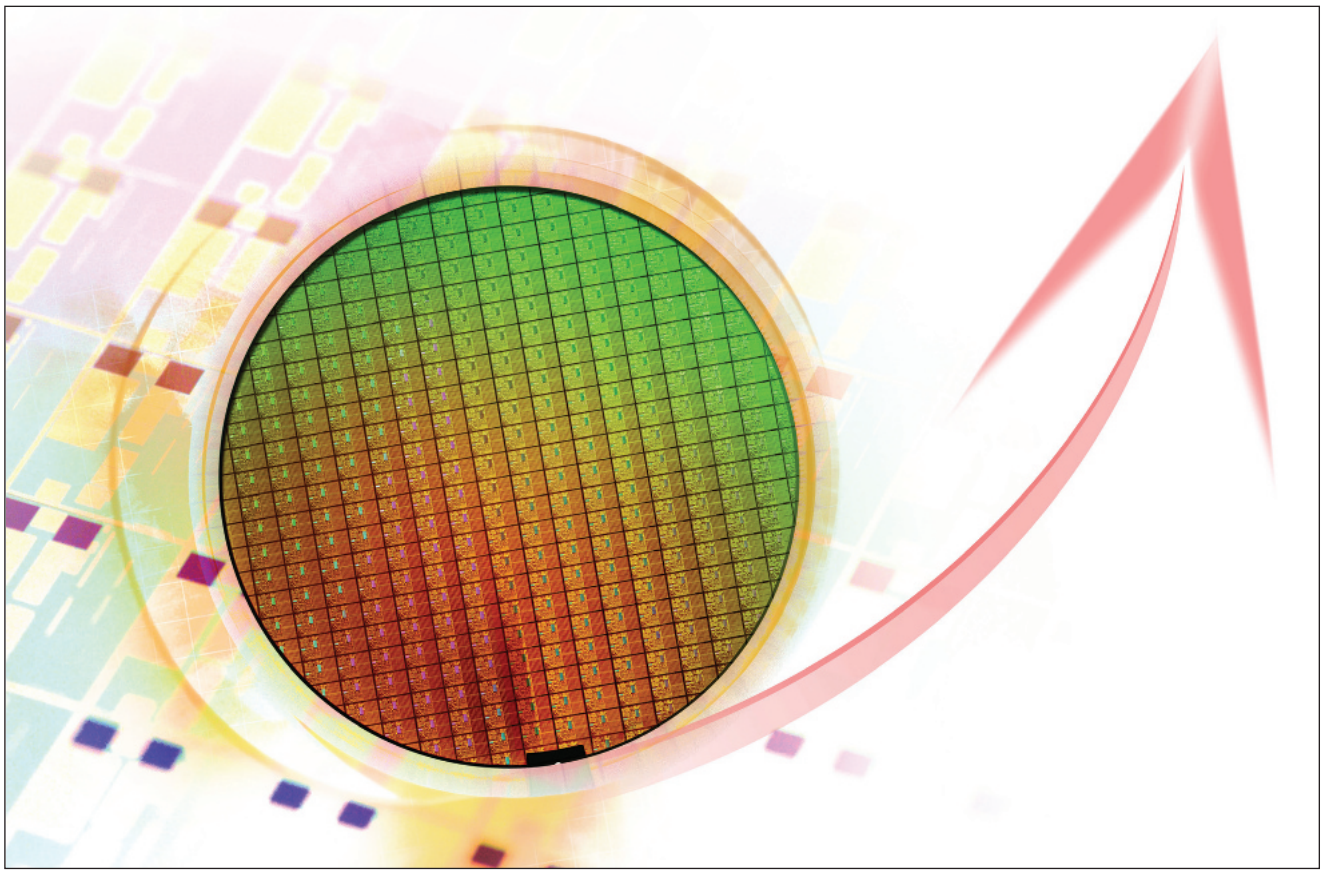
"Our findings show an industry that expects moderate growth next year, which is extraordinary in the context of an uneven global economic recovery," said David Leaver, Head of KPMG's Semiconductor practice in Singapore. "The continuing demand for electronic products ranging from tablets to smartphones, and an increased demand for technology integration in automobiles will buoy semiconductor manufacturers even as the economy fluctuates. "

The results of the survey translated to strength in KPMG's companion Semiconductor Industry Business Confidence Index, a measure derived from specific survey responses on revenue, capital spending, workforce change and R&D spending.

This year the Index registered 60, nearly matching last year's 61, which was also the pre-recession level three years ago. The Index dropped to 36 in 2008. An Index of 50 represents a neutral perception about the industry's prospects, and above 50 represents a positive perception, while below 50 represents a negative perception.

"The executives' confidence also appears to be fueled by recovering economies in a couple of key regions," said Mr Leaver. "China still is viewed as most important for semiconductor product growth, but more executives also foresee the US and European economies recovering and having important roles in industry growth."

Reflecting the fundamental strength of the semiconductor industry, 39 percent of the industry executives expect their company's semiconductor revenue to increase by 10 percent or more in the next fiscal year, compared to 54 percent for the previous year.



Growth Drivers

Survey respondents also identified the top drivers of current revenue growth for 2011. They are:

- Wireless handsets and other wireless communications devices (68 percent)
- Consumer products (65 percent)
- Computing (55 percent)

Also, more executives believe industrial products (43 percent vs. 39 percent in 2009) and automotive products (38 percent vs. 30 percent) will be important revenue drivers over the next year. The expected profitability growth for 2011 reflects continued confidence in industry fundamentals, but a less bullish view than last year's survey.

Thirty-seven percent of respondents anticipate profitability growth in excess of 5 percent for 2011, and a year ago 76 percent expected that level of growth for 2010. Although China is still considered to be the most important geographic area for semiconductor revenue growth three years from today (70 percent of respondents gave the highest rating of 8-10), the survey found that its significance has diminished slightly, dropping from 78 percent last year and 79 percent in 2008.

Both the US and Europe appear poised to play a role in industry growth over the next three years. 47% of executives gave the US an eight to 10 rating compared with a 42 percent in last year's survey. Europe increased to 30 percent in this year's survey from 25 percent a year ago. In this year's findings, more executives (83 percent) expect semiconductor R&D spending to increase in the next calendar year, with 47% saying the increase will be greater than 5%, compared to 72%and 45%, respectively, last year.

Cyclicality

The KPMG semiconductor industry survey results show that 53 percent of respondents anticipate the semiconductor cycle will peak within the next 12 months, which is somewhat contradictory to the responses received in the areas of revenue and profitability growth. Sixty-two percent indicate a high or extremely high level of interest from customers for energy efficient and/or energy renewable products compared to 65 percent last year.

To have your entry included in the Company Contacts please send a logo and contact details to: Tommy Beazley,
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