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Technological foundation

The recent news for the semiconductor industry has not been very positive of late. That is if shares and stocks are your major concern. Analysts are again in a spin as signs indicate another oscillation of industry fortunes appears on the horizon. There is nothing new in the see saw ride of output that the industry has had to deal with from the very first chip was made. The real pressures turn up for the industry when these oscillations are amplified by external events such as international debt concerns or the ever increasing competition for resources that is developing around the globe.

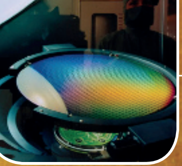
While these are the sort of issues that are likely to impact on your bank balance they tell very little of the continual innovative progress that the industry continues to make. The fact is the semiconductor industry forms the backbone and foundation of all technology and the advances made in this industry provide the building blocks for all technologies and will continue to do some for some time to come.

While technology minded financial experts lead investors toward the new and exciting emerging markets like solar and other renewable energies, MEMS, nanotechnology and biotechnology there is a lack of understanding of how all these ventures rely on the ubiquitous nature of semiconductors. In fact most of the emerging technologies not only rely on semiconductor principles but are manufactured on processes that were developed in the semiconductor industry. New opportunities will only continue to rise as long as the continued progression of the microelectronics industry is supported and recognised for the invasive growth and impact that it brings.

With this in mind it is pleasing to see the European Union release its report on Key Enabling Technologies and the goal to incorporate their importance through out the value chain from education, concepts through to commercialisation of the product. Europe has had a bad reputation for inventing great things but losing the manufacturing benefits and it is a positive sign that there is a growing understanding that this industry brings a great deal more than computer chips. The EU is a notoriously slow beast and the parties involved should be commended in achieving such a strong statement.

Now is the time of implementation and any success is surely to attract interest from other regions further emphasising the need for areas to develop their abilities to not only research but manufacture the potential that comes from a concerted approach.

David Ridsdale
Editor-in-Chief



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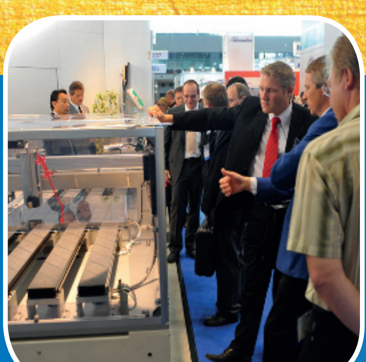

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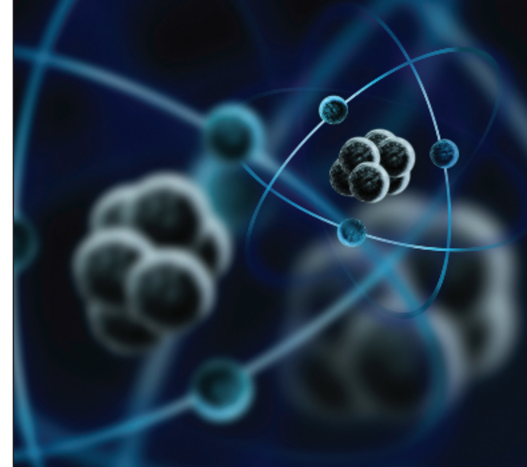

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DRAM price reductions decelerate in 2012

SLOWER advancements in semiconductor manufacturing technology this year will cause a deceleration in price reductions for dynamic random access memory (DRAM), according to the IHS iSuppli Memory and Storage Service from information and analysis provider HIS. Following a drop of 14.2 percent in the first quarter of 2011, the global average decline in pricing for DRAM slowed to 12 percent in the second quarter.

The rate of decrease is expected to decline to 9 percent in the third quarter and then dwindle to just 4 percent in the fourth quarter. The rate of decrease will further slow to just 1 percent in the first quarter of 2012, and then remain in the 3 to 4 percent range during the rest of 2012. The slowdown in price reductions parallels a deceleration in the rate of migration to more advanced lithography used for manufacturing DRAM. To a large degree, DRAM pricing trends are driven by the progression of manufacturing technology to smaller geometries.

Average lithography geometry for global DRAM manufacturing shrunk by a near-term high of 5.6 percent in the first quarter. However, that rate of shrinkage will decrease to 5.2 percent in the second quarter, to 4.8 percent in the third quarter and to 3.7 percent in the fourth quarter. After declining to 2.9 percent in the first quarter of 2012, lithography will shrink in a range of 3.8 percent to 4 percent for the remainder of the year.

"In the wake of forcefully pursuing lithography reductions in late 2010 and early 2011, the DRAM industry is expected to employ a less aggressive approach to lithography migration throughout the rest of the year," said Dee Nguyen, memory analyst at HIS. "DRAM capital expenditures are expected decline by 30 percent in 2011 compared to 2010. As a result, the rate of DRAM cost reductions also will slow during the remainder of 2011 and 2012. However, IHS expects that DRAM cost reductions will speed up again in 2013 as lithography shrinks return, due to increased capital spending. Spending will increase by 23 percent in 2012, which may spur steeper price reductions in 2013."

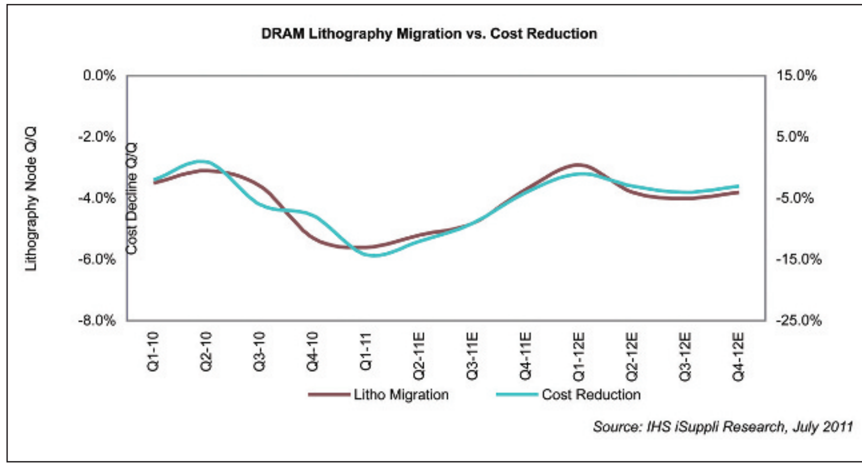
The DRAM industry is undergoing several transitions, including the strategic shift away from commodity DRAM among many suppliers, new manufacturing and foundry alliances, as well as by the continued migration to 40-nanometer (nm) technology and beyond. All these factors will have an impact on supply-and-demand dynamics, which will affect profitability and supplier earnings, IHS believes.

Surprisingly, DRAM suppliers remained profitable in the first quarter, boosted by the substantial margin built up during the previous up cycle for the market, which began in the second quarter of 2009 and lasted until the end of the rally a year later. And despite the downward streak in the average street prices of DRAM, the current cycle is no exception to historical patterns that have seen the ebb and flow of demand cycles, accompanied by fluctuations in chip prices and DRAM company earnings.

In particular, the cost declines projected for the industry are expected to come from technology migration, with DRAM chips increasingly made with new lithography equipment and technology. From the fourth quarter of 2010 to the first quarter this year, the main drivers of lithography change were Inotera, whose average lithography mode crossed over to 50 nm, and Rexchip, which went to 40 nm.

And while DRAM cost declines also can be driven by factors other than lithography migration, those extra considerations can be safely ruled out for the time being, IHS research shows. One factor, capacity growth in order to maximize efficiencies of scale, will be limited as companies continue to exercise caution on expansion-specific capital expenditure. Another factor, operational efficiencies, is not expected to make much of a dent in further cost savings, given that companies remain relatively lean from the previous as well as current downturns.

As the transition to 4x-nanometer fully completes next year, cost declines will level off even more, IHS estimates show. Cost reductions relative to lithography migration will reach 6.5 percent per quarter during the remainder of 2011, and then narrow to 3.3 percent in 2012. With lithography migrations becoming less spirited in the coming quarters, cost declines will mirror the pattern: strong for now, and then fading in 2012.



Source: IHS iSuppli Research, July 2011

IHS iSuppli Figure: DRAM Lithography Migration vs. Cost Reduction

	Q1-10	Q2-10	Q3-10	Q4-10	Q1-11	Q2-11E	Q3-11E	Q4-11E	Q1-12E	Q2-12E	Q3-12E
Litho Migration	-3.5%	-3.1%	-3.6%	-5.3%	-5.6%	-5.2%	-4.8%	-3.7%	-2.9%	-3.8%	-4.0%
Cost Reduction	-2.0%	1.0%	-6.0%	-7.8%	-14.2%	-12.0%	-9.0%	-4.0%	-1.0%	-3.0%	-4.0%

Source: IHS iSuppli Research, July 2011

Semiconductor advanced packaging set for strong growth

ADVANCED packaging is currently growing at a 18% compound annual rate, and equipment manufacturers will be major beneficiaries according to the report Lithography and Etch Market Analysis for Flip Chip manufacturing, recently published by The Information Network.

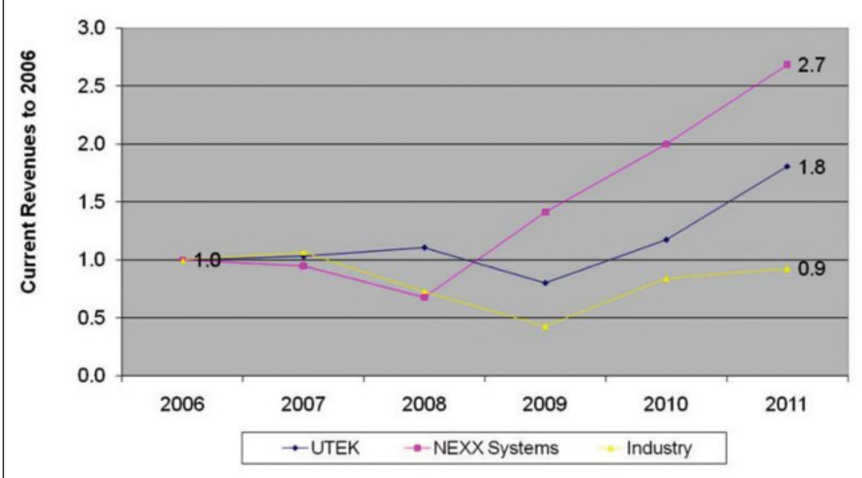
"Our leading indicators are pointing to a downturn in semiconductor equipment sales for the second half of 2011 and through 2012,", noted Dr. Robert Castellano, President of The Information Network. "These data are corroborated by SEMI's (Semiconductor Equipment and Materials International (SEMI) is a trade organization of manufacturers of equipment and materials used in the fabrication of ICs) recent mid-year consensus forecast."

But all semiconductor equipment markets are not created equal, and there is a sector market that equipment vendors, large and small, public and private, have in their crosshairs that is projected to show strength while the rest of the equipment market falters. Flip chip technology, an advanced form of packaging of ICs. The stakes are big. Total flip chip sales represented 11% of worldwide IC production in 2010 but will grow to more than 18% in 2015. Flip chip comprised only 5% of IC production in 2005.

Intel (INTC) is the leader in the industry, followed by Chipbond Technology (TPO:6147), TSMC (TSMC), Samsung (005930.KS), NEPES Corp. (033640:KOSDAQ), and ASE (ASX).

Equipment vendors are taking advantage of the booming market. Estimates are that the front-end (before the flip chip packaging steps) will exhibit a compound annual growth rate (CAGR) of 4% between 2010 and 2013. In contrast, sputtering and copper electro-deposition equipment, main sectors of the flip chip equipment market, will exhibit a CAGR of 17%.

In researching further the market for flip chip technology, the chart below shows UTEK's revenues for its equipment normalized to 2006 in comparison to front-end equipment and privately held NEXX systems. Interestingly, despite growth of 148% in 2010 according to SEMI, semiconductor equipment through 2011 is projected to reach only 90% of 2006 levels of revenue. UTEK through Q1 2011 has grown 1.8 times its revenue of 2006. NEXX Systems, according to their S-1/A filing of June 2011, has exhibited revenue growth 2.7 times their 2006 revenue.



Analysts predict slow down

ECONOMIC research firm e-forecasting.com announced that the European Semiconductor Sales leading indicator went down 0.4 percent in May to a reading of 202.3 after a decline of 0.9 percent in April. The index was set to average 100 in 2000. The indicator, comparable to the company's other global regional semiconductor industry indicators for North America, Asia Pacific and Japan, is a forward-looking composite index that forecasts six months ahead, on average, business activity in the region for sales for semiconductors.

"The European semiconductor industry leading indicator has slowed the last four months, with a significant decrease in its six month growth rate. Now nearing zero, it shows that this region will decline later this year, " commented Dr. Evangelos Simos, Chief Economist of e-forecasting.com.

The semiconductor leading indicator's six month growth rate went recorded 0.8 percent in May 2011, after reaching 2 percent in April. Consecutive positive values in the six-month growth rate predict an end to an economic recession and the beginning of an upcoming expansion.

Two of the seven components that make up the leading indicator for semiconductor sales in the European market improved in May: US Monetary Conditions, Yield Spread and Orders to Inventories Ratio, US Electronics. The five components that had a negative contribution to the leading indicator for semiconductor sales in the European market were: Productivity Barometer, US Manufacturing; Productivity Barometer, European Manufacturing; Non-EU Demand Prospects, Top-10 partner-countries; Change in Profit Margins, US Semiconductors and European Short-term Interest Rates.

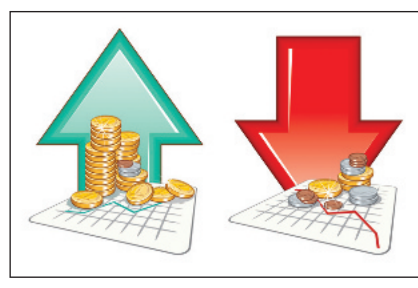
IHS predicts climbing inventory

SEMICONDUCTOR inventory levels at chip suppliers worldwide are believed to have risen for the seventh consecutive month in a row in the second quarter, as the industry rebuilds depleted stockpiles and prepares for expected increases in demand, the latest IHS iSuppli Inventory Market Brief report from information and analysis provider IHS.

The total stockpile level for all semiconductor suppliers—excluding the volatile memory segment—is projected to rise to 81.5 days in the second quarter, up 1.5 percent from 80.3 days in the first quarter, according to the most recent IHS forecast. With this increase, inventories will have risen during every quarter since the last three months of 2009.

"Increases in stockpiles during the first quarter reflect efforts by semiconductor suppliers to rebuild inventory for products that were in short supply during the capacity crunch of 2010," said Sharon Stiefel, analyst for semiconductor intelligence at IHS.

"Suppliers also are moving to strategically build for the higher demand expected later this year. In a fortuitous stroke of good timing, semiconductor component manufacturers were able to take advantage of the reduced demand environment during the seasonally slow first quarter to build their stockpiles."



Inventories throughout the electronics supply chain—including at semiconductor suppliers, distributors, contract manufacturers and original equipment manufacturers (OEM)—during the first quarter rose for all sectors except for computer makers. Computer OEM stockpiles declined more than 8 percent, likely because they shipped most of their products to retail outlets for restocking following the busy holiday season in the fourth quarter of 2010.

In comparison, memory and analogue companies had the highest percentage increases in their internal inventory, with growth of almost 15 percent, while fabless companies and distributors experienced more muted increases.

With macroeconomic factors feeding the growth of the overall electronics industry and generally trending positive semiconductor inventories are likely to continue rising throughout 2011. Growth will be stimulated by market demand for popular consumer items like smartphones and tablets, as well as for perennial reliables such as PCs.

The Japan quake disaster in March will have a minimal effect on inventories throughout the electronics supply chain, given that inventories had been built up during the prior two quarters, IHS research shows. In fact, a more widespread disruption that had threatened to unfold was held at bay by opportune supplies on hand, the timely repair and restart of production facilities and agile moves among manufacturers to shift production from Japan to facilities outside the country.

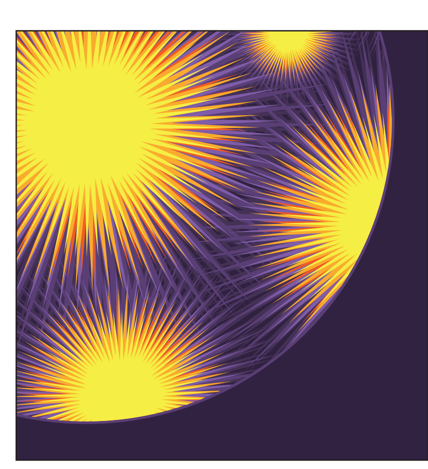
One continuing area of concern might be the supply of raw wafers because Japan provides approximately 60 percent of the global supply of semiconductor wafers. However, in a positive indicator, leading semiconductor foundry Taiwan Semiconductor Manufacturing Co. announced that it will not experience any detrimental effects from the aftermath of the disaster. Areas of potential impact will continue to be closely monitored by IHS.

Just the same, manufacturers may increase orders as a cushion in light of the recent turbulence to guard against future supply chain disruptions. Maintaining higher inventory could become the new normal in the future, a calculated measure deployed to mitigate the disrupting effects of natural disasters and political upheavals.

Semiconductor SiC Parts Fall Short of 2008 Peak

THE 2010 market for silicon carbide (SiC) fabricated parts for semiconductor applications totalled $200M, sharply up 38% over the 2009 low, according to a new report from Techcet Group, "Silicon Carbide As Used in the Semiconductor Industry 2011, A Techcet Group Critical Materials Report." This is still 5% shy of the 2008 peak, but the 2011 outlook is for continuing growth of 12% or more to between $225M and $240M, according to Techcet's latest forecast.

Many OEMs and fab users allowed their SiC parts inventory to run low during the recession, and are now scrambling to restock. Field experience with SiC has also matured to the point where the longer product life and superior performance over quartz for 300mm chip manufacturing have been adequately demonstrated, creating new market demand. While there is no shortage of SiC material overall, some CVD SiC suppliers have pushed lead times out to six months and are working to double their capacity. Roughly 60% of the SiC demand is for wafer carriers, boats and related fabware, with the remainder going to OEM components.



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Long term planning from Europe

A KEY expert group set up by the European Commission sets out guidelines on giving European industry a competitive edge in deploying the industrial technologies of the future (Key Enabling Technologies). The main conclusions call on decision-makers to adopt radical policy objectives to retain critical capability and capacity in Europe through a single and comprehensive approach to KETs. In particular, the group recommends that the vital importance of KETs should be reflected in the structure and funding balance in the upcoming framework for research and innovation and in the priorities of the EU's future regional policy.

European Commission Vice-President Antonio Tajani warned that Europe's industry "would suffer losses in competitiveness", if it fails to successfully exploit the six following important KETs (micro- and nanoelectronics, advanced materials, industrial biotechnology, photonics, nanotechnology and advanced manufacturing systems). "Europe's

innovation depends on the development and growth of Key Enabling Technologies. We need to focus our policies better and align them to create more synergies between our instruments to boost Europe's capabilities in the area of KETS. I am convinced KET's follow-through applications will allow Europe to create more jobs and growth. The commitment of private stakeholders to investing in Europe will also be vital for success", he said.

Technological research and product demonstration projects should be given a high priority. Further recommendations cover the combination of funding mechanisms at EU and national level and a set of actions to enhance technological skills in Europe. An "in Europe first" Intellectual Property policy is called for and a monitoring mechanism to analyse market developments on KETs is also proposed.

KETs are embedded at the core of advanced products. An electric car is a combination of advanced materials for batteries, microelectronics components for power electronics in order to reduce the weight of the car, photonics for low consumption lighting, industrial biotechnologies for low friction tyres and manufacturing systems to produce electrical vehicles at a competitive cost. Similarly a mobile phone incorporates microelectronic chips for communications, photonics enabled camera and optics, advanced materials for new tactile screens, and so forth.

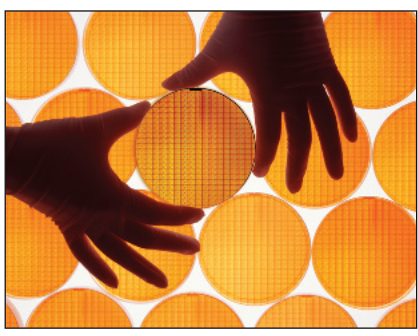
imec produces first EUV lithography wafer

IMEC has announced that it has successfully printed first Extreme-Ultraviolet (EUV)-light wafers with the ASML NXE:3100 preproduction scanner using XTREME technologies Laser assisted Discharge Plasma (LDP) source. The tool shows significant improvement in throughput and overlay compared to ASML's Alpha Demo Tool (ADT).

The ASML NXE:3100 is interfaced with a TEL Lithius Pro EUV process track. It is the only preproduction tool in the world equipped with a laser assisted discharge plasma (LDP) source from XTREME technologies. The source power is expected to scale to 100 Watts by early 2012, increasing the scanner throughput from the current level to 60 wafers (300mm) per hour.

The exposure rate of the NXE:3100 is already 20 times faster than that of the EUV ADT. A first test of dedicated chuck overlay showed the potential to achieve the <4nm target, which is significantly better than the ADT. The NXE:3100 integrates 4 image and 4 dose control sensors which were developed within imec's CMORE development and prototyping service. Installation of these new sensors combined with new wafer tables made both chucks equivalent for overlay, enabling full twinstage-type operation. At the same time, off-axis illumination options have been installed, which have proven to resolve sub-20nm features using dipole illumination.

"The availability of the NXE:3100 at imec is an important milestone," said Luc Van den hove, President and CEO of imec. "We are excited with the current results and throughput we achieve. Our decision to implement the LDP source from XTREME technologies is an important added value for our partners since it allows them to test both our LDP (laser assisted discharge plasma) and the LPP (laser produced plasma) sources currently installed at other sites. We are convinced that our



program will bring contributions to bringing EUV to mass manufacturing for the 16nm node by 2013."

Ron Kool, ASML Senior Vice President EUV said "The work at imec exemplifies the industry momentum behind EUV and will help prepare the ground for the introduction of EUV into high-volume manufacturing."

This work was executed with imec's key partners in its core CMOS programs Globalfoundries, Intel, Micron, Panasonic, Samsung, TSMC, Elpida, Hynix, Fujitsu, Sony and Powerchip.

A modest May

Recent figures from the SIA suggest that global growth for the semiconductor industry was steady for the month of May.

The Semiconductor Industry Association (SIA), said that sales of semiconductors were $25 billion for the month of May 2011, a 1.8% increase from April when sales were $24.6 billion and a 1.3 % growth from May 2010. All sales numbers are a three month average.

"Taking into consideration macroeconomic factors impacting confidence, the modest growth that the industry demonstrated in May is encouraging," said Brian Toohey, president, SIA. "Global demand for high-end electronics, the continuing proliferation of semiconductor technology into a wider range of products, growth in emerging economies and better than expected recovery from the Japan earthquake will be continued drivers of industry growth in 2011."

The industry continues to see demand for tablets and e-readers grow, as well as increased demand for industrial processors that enable devices to harness renewable energy like solar panels and e-meters. Additionally, the industry has seen strong demand for electronic systems included across all ranges of vehicles.

Economic uncertainty around the world bears close watching, while further opportunities for sales growth will be concentrated in emerging markets like China and India. Results are in line with projections recently reported in the Spring Semiconductor Sales Forecast from WSTS that indicate global industry sales will increase 5.4 percent for 2011, 7.6 percent in 2012 and 5.4 percent in 2013, with a 3-year compound annual growth rate of 6.13 percent from 2010 to 2013.

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May 2011
Billions

Month-to-Month Sales

Market	Last Month	Current Month	% Change
Americas	4.48	4.52	0.9%
Europe	3.26	3.24	-0.3%
Japan	3.41	3.34	-2.1%
Asia Pacific	13.44	13.92	3.6%
Total	**24.59**	**25.03**	**1.8%**

Year-to-Year Sales

Market	Last Year	Current Month	% Change
Americas	4.38	4.52	3.2%
Europe	3.12	3.24	3.8%
Japan	3.71	3.34	-9.9%
Asia Pacific	13.49	13.92	3.2%
Total	**24.70**	**25.03**	**1.3%**

Three-Month-Moving Average Sales

Market	Dec /Jan /Feb	Mar /Apr /May	% Change
Americas	4.60	4.52	-1.7%
Europe	3.24	3.24	0.3%
Japan	3.59	3.34	-7.0%
Asia Pacific	13.21	13.92	5.4%
Total	**24.63**	**25.03**	**1.6%**

The key to low temperature bonding for 3D integration

Pressure and temperature are key requirements in the interconnect bonding process for low resistance, high yielding and reliable interconnects. Jason D. Reed, Matthew Lueck, Chris Gregory, Alan Huffman, John M. Lannon, Jr. and Dorota S. Temple, **Centre for Materials and Electronic Technologies, RTI International** discuss results of bond and stress testing of Cu/Sn-Cu bonded dice and Cu-Cu thermocompression bonded dice in large area arrays and show that in the case of Cu/Sn-Cu, the use of a mechanical key was found to improve yield.

High density interconnects enable further miniaturization, reduced power consumption and enhanced functionality of microsystems. Heterogeneous technologies such as sensors, imaging arrays and others can be implemented in their optimal process flows and then integrated using the high density interconnects. Several research groups have presented work in the area of metal-metal interconnects [1-4]. In this paper we review the status of the development of high yield bonding at 10µm pitch, highlighting the use of a mechanical key to prevent misalignment and slippage during thermocompression. These results represent an order of magnitude increase in density (10^6 interconnects per square centimeter) as compared with the state-of-the-art in traditional flip-chip bonding.

Design and Fabrication

Three test vehicle devices were fabricated based on the following approaches:

- Cu/Sn - Cu bond with no mechanical key.
- Cu/Sn - Cu bonding with a mechanical key on one of the dice to prevent misalignment and slippage during bonding. The keys also prevent Sn from bridging acrossbonds, an issue noted in previous work [5].
- Cu - Cu thermocompression bonding with chemically-mechanically polished (CMP'd) Cu bond pad surfaces and with CMP'd Cu to as-plated Cu bond pad surfaces. The as-plated Cu pads also had a mechanical key.

These approaches were designed to be compatible with post-CMOS processing on 200mm wafers. To test these bonding approaches, RTI fabricated test vehicles containing 512 x 640 area arrays of bond pads with 10µm pitch on 200mm diameter wafers. Each test vehicle provided 256 daisy chain channels, with 1272 individual chip-to-chip bonds per channel, giving good spatial resolution of potential defects.

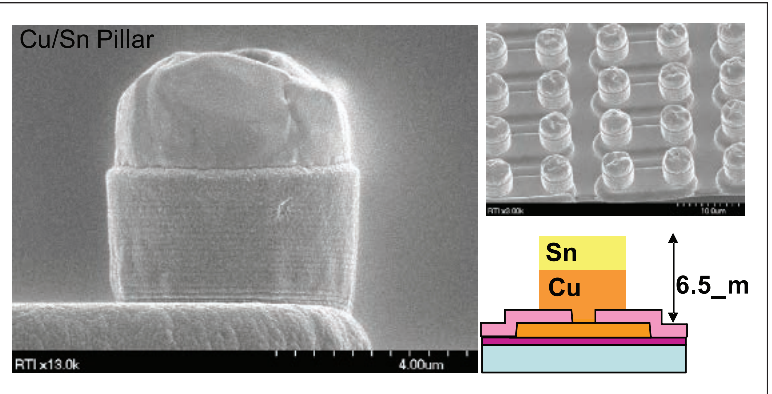

Fig. 1. (left) SEM of top die pillar after tin plating, (above right) SEM of the top die 10_m pitch array, (below right) scaled drawing of Cu/Sn pillars (3.5um copper and 2.5um tin)

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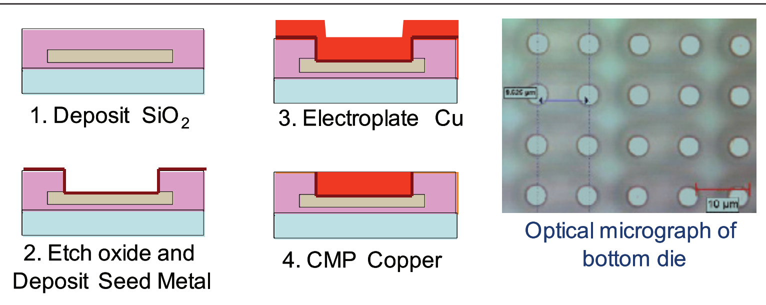


Fig. 2. Schematic diagram of top and bottom dice (left) and optical microscope image (right) used to fabricate Cu-Cu thermocompression test vehicles with 10µm pitch in area arrays of 512 x 640.

For the Cu/Sn-Cu vehicle without a mechanical key, the bottom routing layer was formed using lithography, Ti/Cu/Ti evaporation and liftoff. Oxide was deposited by plasma enhanced chemical vapor deposition (PECVD) and patterned by reactive ion etching (RIE). Bond pads were formed by the combination of seed layer sputtering, lithography, electroplating and seed layer etching. The seedlayer etching was done with an ion mill. The top die consisted of 4µm diameter Cu pads plated 4µm thick. The bottom die consisted of 6µm diameter pads plated with 4µm of Cu and 2µm of Sn.

For Cu/Sn-Cu with a mechanical key, the top die was fabricated in a process similar to the one described above, with 4µm diameter pads plated with 3.5µm of Cu and 2.5µm of Sn. The bottom die consisted of metal links terminated with 6µm diameter pads that were plated with 4µm of Cu and then coated with BCB. Vias were etched in the BCB to create openings for bonding to the bottom pads. The BCB sidewalls created a mechanical key to prevent lateral slippage during bonding.

An SEM of an individual Cu/Sn pillar, an SEM of the 10µm pitch array and a scaled schematic diagram of the top dice pillars are shown in Fig. 1.

For Cu-Cu thermocompression bonding of CMP'd Cu surfaces, the top and bottom pads were formed in 5µm thick SiO^2 by RIE, filled with Cu by Ti/Cu seed sputtering and Cu blanket electroplating and then planarized with CMP to remove the Cu overburden. Pad diameters for top and bottom die were 4µm. After CMP, the oxide was partially etched (recessed) to expose the tops of the pillars for bonding. As noted above, in this vehicle the Cu bonding surfaces are both produced by CMP. A schematic diagram of the fabrication sequence is depicted in Fig. 2.

For Cu-Cu thermocompression bonding with CMP'd Cu to as-plated Cu, the top die was formed by CMP as above. The bottom die consisted of metal links terminated with 6µm diameter pads that were plated with 4µm of Cu and then coated with BCB. Vias were etched in the BCB to create openings for the top pads to bond to the copper bottom pads. After fabrication, roughness and uniformity were characterized as reported in [6].

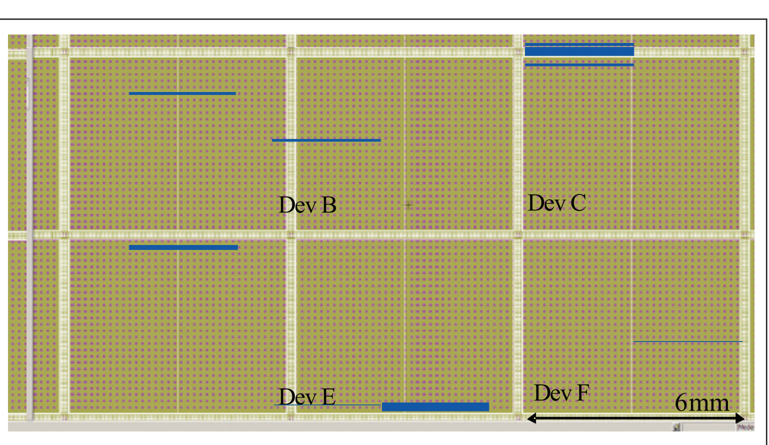
Sample bonding was performed using a SET FC150 precision bonder with split optics, allowing for alignment in "cold placement" with accuracy of ±1 µm.

Cu/Sn-Cu Temperature Optimization

Prior to bonding, the Cu bottom pads were stripped of copper oxide with a dilute acid solution. The Cu/Sn top pads were fluorine plasma treated with the PADS process (Plasma Assisted Dry Soldering), which enables fluxless bonding [7]. The tin pads were flattened using an in situ coining process.

For Cu/Sn-Cu dice without mechanical key, six consecutive die pairs with pads on 15µm pitch were bonded using 275°C bonding temperature for 180s and bonding pressure of $5x10^6$ kg/m^2. All six pairs exhibited electrical opens. Die shear and inspection revealed that the top pads had slipped laterally off the bottom pads during bonding. This result confirmed the expectation that without mechanical keying, the Cu/Sn bonding process will be difficult to scale

Fig. 3. Graphical map of defective channels in six consecutively bonded 10µm pitch samples. Blue lines show electrical opens. Individual bond yield is >99.99%



to pitch dimensions below approximately 20 μm due to slippage during bonding [8].

For Cu/Sn-Cu dice with a mechanical key, the effect of bonding temperature was studied on samples at 10μm pitch. The bonding process was performed using a pressure of 5*106 kg/m^2 at a temperature of 275 and 300°C for 180s under N_2 purging. Electrical testing showed high channel yields were achieved at both 275°C and 300°C bonding temperature.

Average channel yield (each channel contains 1272 bonds) was 93% and did not depend strongly on bonding temperature. The parts bonded at 300°C had similar median resistance (103 mΩ/bond, with standard deviation of 8mΩ) to those bonded at 275°C (96 mΩ/bond, with standard deviation of 15mΩ). Resistances include the wiring and pad structures. The two results are within one standard deviation.

Cu/Sn-Cu Bonding Qualification Run

To demonstrate the repeatability and test the robustness of the Cu/Sn-Cu bonding process with mechanical keying, a qualification of 22 bonding runs at 10μm pitch was done. This run used standard bonding conditions: in situ coining of the Sn, followed by bonding at 275°C for 180s at a pressure 5x10^6 kg/m^2 (32.2kgf) over an array of pads 512 x 640 on a 10μm pitch.

After bonding, electrical testing on the 22 bonded pairs was done and the median channel yield was 98.4% and the median channel resistance was 65Ω. Each channel contains 1272 interconnections in a daisy chain format. The average resistance of each interconnect including the wiring and pad structures was <100 mΩ.

The wiring and pad structures were modeled and their calculated resistance was subtracted from the raw resistance value to give approximately 20mΩ per bond and a contact resistance of 5x10^{-8} Ohm-cm^2. This result is compared with Cu-Cu bonding in the Comparison of Electrical Results Section.

A yield map of six consecutively bonded Cu/Sn-Cu 10μm pitch dice is shown in Fig. 3. The blue lines mark the channels that were electrically open after bonding. The location of defects is not random, with most defects clustered near the device edges. The opens are most likely due to handling damage. Aside from the edge defects, assuming that each open channel is caused by a single open bond, then the individual bond yield is >99.99%.

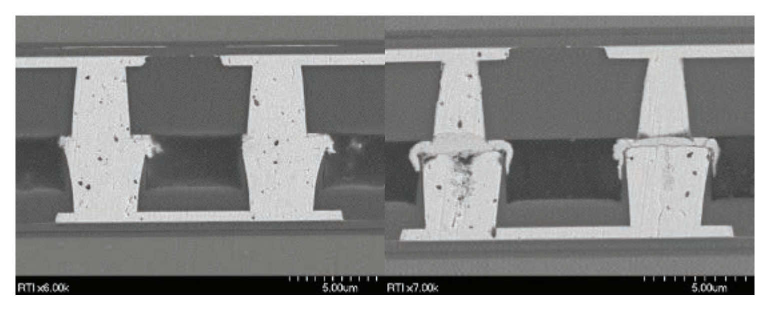


Fig. 4. SEM cross section thermocompression bonded sample with CMP Cu top die and CMP Cu bottom die

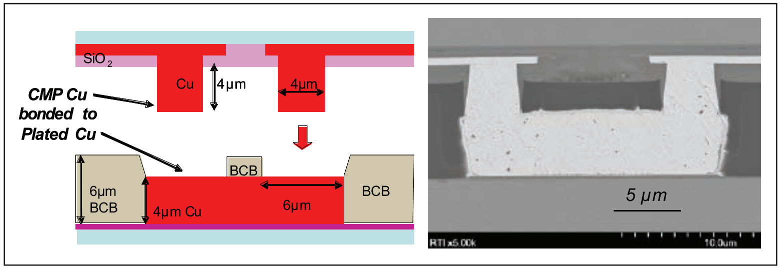
Samples were cross-sectioned for SEM and energy dispersive spectroscopy (EDS) analysis. SEM analysis of cross-sections was done with a backscattered electron detector. Quantitative EDS was performed to identify intermetallic phases at the bondline (Fig. 8). The IMC is the Cu_3Sn phase. This phase is thermodynamically stable up to 650°C. There was no Cu_6Sn_5 or unreacted Sn. The BCB mechanical key was important for achieving high yield by constraining slippage during bonding. The presence of the Sn layer was important for achieving high yield by accommodating the non-planarity of the bonding surfaces through in situ coining prior to bonding.

Cu-Cu Bonding (CMP'd Cu to CMP'd Cu)

CMP'd Cu to CMP'd Cu bonding was done with varied mechanical pressure and temperature. Typical bonding conditions were a temperature of 325°C and a pressure of 32.2 kgf, equivalent to 5x10^6 kg/m^2. As with the Cu/Sn-Cu test vehicle, this vehicle had 512 x 640 array of pads on 10μm pitch for an interconnect density of 10^6/cm^2.

Electrical measurement of bond chains gave a resistance of 95.9 mΩ and 44.5% channel yield

Fig. 5. Schematic and SEM cross-section of CMP Cu to Plated Cu metal bonding at 15μm pitch



(1272 daisy chained connections per channel). This channel yield was much lower than the yields achieved with Cu/Sn-Cu bonding primarily due to non planarity of the Cu pillars as a result of dishing during the CMP planarization process.

The amount of non planarity of the Cu pillars was measured after CMP. For the corner pillar, the average dishing was 0.35µm below the die center. The minimum value observed was 0.20µm and the maximum was 0.60µm. The corner pillar exhibited a larger amount of dishing because it is the most exposed pillar in the die during CMP. The amount of edge pillar and corner pillar dishing did not depend on wafer location to a significant degree.

The non-planarity reduced bonding yield by preventing physical contact of edge pillars during the thermocompression process. The effect of the nonuniformity can be seen in Fig. 4 which shows CMP Cu to CMP Cu at 10µm pitch at the center of the die (left image) and the edge (right image).

At the center the Cu to Cu thermocompression bond has been made, but at the edge the nonuniformity in the copper pillar created a gap between the Cu surfaces.

Prior to bonding, the oxide on the bottom die was recessed by 3µm to expose the copper pillars, and the oxide on the top die was recessed to expose the copper pillars by 0.2µm. During the bond process at 325°C, copper oxide forms on the exposed surfaces, visible in the image.

The recess (or dishing) occurred during the CMP process and may be reduced by adding dummy features or pillars outside the active die area. The lack of dummy features caused the outer rows of Cu pillars to recess more than the inner rows, resulting in a non planar bonding surface. The majority of the bonds formed were good in each channel, as confirmed by cross-sectional SEM, but the links at the die edge were electrically open due to the edge dishing. This was confirmed by optical inspection after shear testing (see Shear Testing section).

Table I. Contact resistance comparison of three metal to metal bonding types

Bond Type	Array size	Bond Diameter (um)	Bond Temp [°C]	Bonding Pressure [MPa]	Yield	Contact resistance ($10^{-8}\ \Omega-cm^2$)
Cu/Sn to Plated Cu w/ BCB key	640x512 10 um pitch	4	275	50	98% channel 99.99% ass. point defects	4,7
CMP Cu to CMP Cu	640x512 10 um pitch	4	300	50	44.5% channel.	1,5
CMP Cu to Plated Cu w/ BCB key	430x344 15 um pitch	4	325	100	94.7% channel 99.99% ass. point defects	2,7

Cu-Cu Bonding (CMP'd Cu to as-plated Cu)

In part to try to achieve higher channel yield with Cu-Cu, devices with CMP'd Cu on the top die were bonded to devices with plated Cu and BCB mechanical key on the bottom die. This process is shown schematically and with SEM in Fig. 5.

This approach was taken because by mating the CMP Cu die with the plated Cu die, the non-uniformities in thickness were expected to offset partially. The CMP Cu pillars are lower at the die corners due to CMP dishing, whereas the plated Cu pillars are higher at the corners.

Typical bonding pressure was 10.5 kg/m^2 (30 kgf) for the 15µm pitch samples. Samples were bonded at 325°C for 900s. Electrical measurements gave 94.8% channel yield with median resistance of 62Ω, for a resistance of 73 mΩ per bond and routing segment.

Underfill

Cu/Sn-Cu parts were underfilled with epoxy to prevent oxidation of exposed copper surfaces and increase bond strength. The epoxy (LORD Exp A) was unfilled, with low viscosity (5600 cPs at 25°C) and low Young's Modulus (0.2 GPa at 100°C). Seven Cu/Sn-Cu bonded samples were underfilled. The underfill process consisted of a vacuum-assisted application of the epoxy at 60°C to promote capillary flow, followed by oven cure (1hr at 180°C).

Reliability Testing

The Cu/Sn-Cu devices with underfill were subjected to 100 thermal cycles (+125°C to -40°C) and re-probed, and then 100 hours 85% RH / 85°C stress testing and reprobed.

There were no significant changes in the electrical yield or channel. The average yield was 93% before and after stress testing and the average resistance was 156Ω before and after stress testing.

After stress testing, samples were cross-sectioned for SEM and EDS analysis. EDS was used to quantify the elements in the IMC phase at the bonding interface. The IMC is the Cu_3Sn phase. There was no Cu_6Sn_5 or unreacted Sn. There was no visible corrosion on underfilled

devices and the bondline has not changed significantly after stress testing.

Comparison of Electrical Results

Table I summarizes and compares the electrical resistance results for three types of metal to metal bonding: Cu/Sn - Cu, CMP Cu - CMP Cu, and CMP Cu - Plated Cu.

As expected the contact resistance of the Cu-Cu bonded samples was lower because there is no intermetallic compound formed. The Cu/Sn intermetallic increases the bond resistance by a factor of approximately three compared with CMP'd Cu-Cu. The total bond resistance for Cu/Sn-Cu bonding remains less than 100mΩ per bond.

Comparison of Shear Testing Results

Table II summarizes and compares the bond strength results for the three types of metal to metal bonding that were used in this study: Cu/Sn - Cu, CMP Cu - CMP Cu and CMP Cu - Plated Cu. Die shear strength was measured using a Royce 550 instrument with maximum range of 10kg.

The devices were not underfilled for this test. All three types of samples exhibited a bond strength of approximately 8kg +/- 1kg. For this die size, the minimum shear strength specified in MIL-STD-883E is 2.5kg. Failure occurred at the bond interface, as shown in Figs. 6 and 7.

Cu/Sn-Cu Shear Testing

Fig. 6 shows representative top and bottom die surfaces from a Cu/Sn-Cu part after shear testing. The bottom die, right, shows the mechanical BCB key (dark circles around copper landing pads). Sn is visible on the copper pads and it can be seen to be offset towards the upper right corner, where further slippage was restrained by the BCB mechanical key. Shear failure occurred in the Cu/Sn IMC. The shear strength was above 10 kg.

Cu - Cu Shear Testing

Fig. 7 shows representative top and bottom die surfaces from a CMP Cu - CMP Cu part after shear testing. The shear test result was 6 kg. All of the pads in this photo show unoxidized copper at the Cu-Cu bond. Shear failure occurred at the bondline.

Fig. 8 shows the bottom die surface for a Cu-Cu part after shear testing, revealing that the corner and edge pads on the device did not bond, as shown by the surface oxidation on the pads. The lack of metal-metal bonding was caused by the within-die nonuniformity caused by dishing during CMP.

Bond Type	Array size	Bond strength
Cu/Sn to Plated Cu w/ BCB key	640x512 10 um pitch	Die shear strength of 8.54 kg (median). Min = 3.34kg; Max > 10kg (n=6)
CMP Cu to CMP Cu	640x512 10 um pitch	Die shear strength of 8.53kg (median). Min = 5.63kg; Max > 10kg (n=4)
CMP Cu to Plated Cu w/ BCB key	430x344 15um pitch	Die shear strength of 8.7kg (median). Min = 7.4kg; Max > 10kg (n=2)

Table II. Comparison of the bond strength as measured by shear testing for 3 types of metal to metal bonding: Cu/Sn - Cu, CMP Cu - CMP Cu and CMP Cu - Plated Cu

Low Temperature Bonding at 25µm

To explore the feasibility of low temperature bonding, a set of devices was bonded at 210°C and compared with a set of devices otherwise similar but bonded at standard temperature (300°C).

These devices were similar in design to the devices tested for reliability above (325,632 interconnects in area array format) but were 25µm pitch instead of 10µm. The devices were measured for electrical yield, shear strength, and were cross sectioned for SEM and quantitative EDS analysis.

For both 300°C and 210°C bonding, electrical testing showed high channel yields were achieved. Average channel yield (each channel contains 1272 bonds) was 87%. The median resistance per bond was 127 mΩ/bond which includes the wiring and pad structures.

In terms of yield and resistance the electrical behavior of the two sample sets was not significantly different.

Graphical maps of the Cu/Sn-Cu electrical yield show a random distribution, indicating a lack of misalignment, across-die nonuniformity or other systematic defects. Opens are most likely due to point defects. Individual bond yield is higher than 99.99%.

Fig. 9 shows cross-sectional SEMs of dice bonded at 300°C and 210°C. The 300°C bonded sample used the standard process conditions described. The 210°C sample was bonded at 210°C for 5 min using 50MPa of pressure and

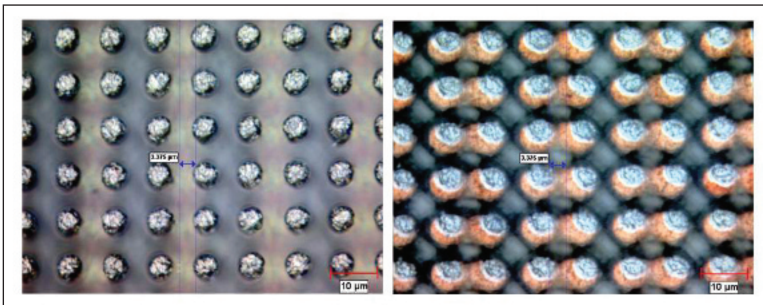


Fig. 6. *Optical micrographs of a 10µm pitch die after shear test. Left: Top die. Right: Bottom die*

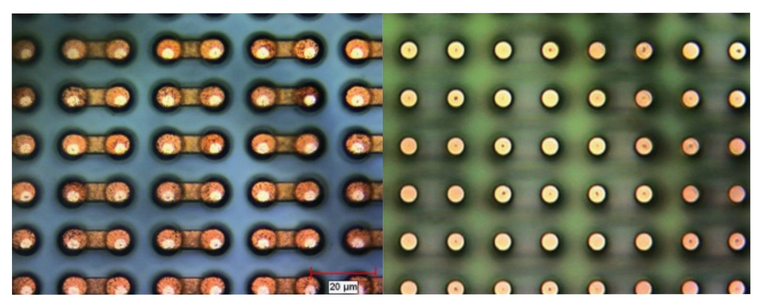


Fig. 7. *Optical micrographs of a typical plated Cu (bottom die, left) to CMP Cu (top die, right, same scale) after shear testing*

then oven annealed at 200°C for 20 minutes in N2 atmosphere without pressure.

Quantitative energy dispersive x-ray spectroscopy (EDS) was performed on cross-sections to identify the different Cu/Sn intermetallic compounds that are present in the bonds. The four different material regions, labeled A, B, C, and D in Fig. 9, were analyzed by EDS.

The sample bonded at 300°C did not exhibit unreacted Sn, whereas the sample bonded at 210°C exhibited a region of unreacted Sn (region D in Fig. 18). The Cu_3Sn phase (B) and Cu_6Sn_5 phase (C) are present in both. In the 210°C sample, the Cu_3Sn phase on top and bottom Cu pillars is separated by a thin (0.2µm) Cu_6Sn_5 intermetallic.

Shear testing of the 300°C and 210°C bonded devices was performed. The shear test result was ≥10 kg for both types.

Low Temperature Bonding at 10µm

To demonstrate the repeatability and test the robustness of the low temperature Cu/Sn-Cu bonding process at 10µm pitch, a qualification of seven bonding runs was done. This run used the low temperature bonding conditions: in situ coining at room temperature with 40kgf force, bonding at 210°C for 180s at $5x10^6$ kg/m^2 pressure (32.2kgf) over a 512 x 640 array on 10µm pitch. Post bond annealing was performed at 200°C for 20 minutes.

After annealing, electrical testing on the seven bonded devices was done and the median channel yield (1272 daisy chained interconnects/channel) was 92.2% and the median channel resistance was 86Ω. The average resistance of each interconnect including the wiring and pad structures was 68mΩ.

Fig. 10 shows a cross-sectional SEM of a 10µm pitch device bonded at 210°C showing similar structure to devices bonded at 300°C. Quantitative energy dispersive x-ray spectroscopy (EDS) was performed on the cross-section to identify the Cu/Sn intermetallic compound present in the bond.

EDS spectra and quantitative results for 10µm pitch bonded sample, at the bondline, showed 61% wt. Cu and 39% wt. Sn, indicating the Cu_3Sn intermetallic phase. There is no Cu_6Sn_5 intermetallic phase or unreacted Sn present.

Shear Testing of Cu/Sn-Cu Bonded at 210°C

Fig. 11 shows representative top and bottom die surfaces from a Cu/Sn-Cu part at 10µm pitch bonded at 210°C after shear testing. The bottom die, right, shows the mechanical BCB key (dark circles around copper landing pads). Cu/Sn intermetallic is visible on the copper pads. Shear failure occurred in the Cu/Sn IMC. The shear strength was 6.0 kg, exceeding the 2.5kg specification without underfill.

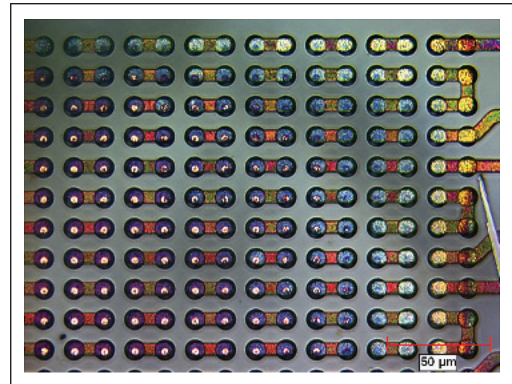


Fig. 8. *CMP Cu - CMP Cu device after shear testing, showing oxidized bond pads along the edges and corner of the Plated Cu bottom die after shear testing*

Conclusion

We have demonstrated a high yielding bonding process for the fabrication of die-to-die interconnects in dense area arrays at 10µm pitch. Use of a mechanical key created by patterning an overcoat of BCB was found to improve yield. Bonded samples, underfilled with epoxy to prevent oxidation of Cu pads, were subjected to thermal cycling and humidity-temperature testing. No significant changes in performance occurred as a result of the test

Cu-Cu thermocompression bonding resulted in demonstrated high yield on individual devices, but not on long runs of consecutive bonds. The lower average yield is due to the dishing obtained during the CMP of Cu pads. This dishing can be reduced by laying out the bond pad arrays so the area density of metal changes gradually between the array and field regions. Comparison of the electrical and shear test performance of Cu/Sn-Cu and Cu-Cu bonds shows that highly conductive (<100mΩ) and mechanically strong (8kg for ~6 mm x 5 mm die) bonds can be achieved in both metal systems.

Low temperature bonding in Cu/Sn-Cu devices (at 210°C, below the melting point of tin) was demonstrated to produce high electrical yield, high shear strength and similar IMC formation to devices bonded at 300°C. Such a process may prove useful for bonding dice that have low thermal budgets such as memory or detectors.

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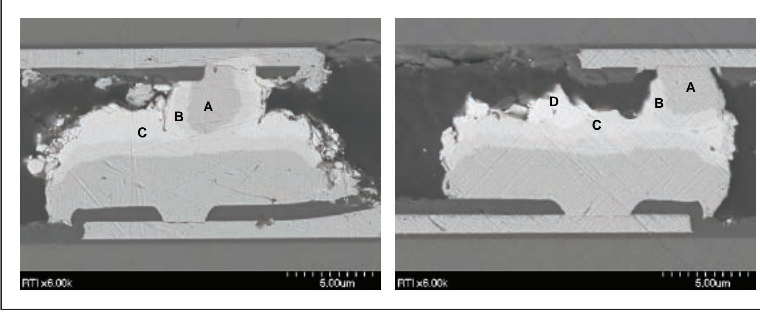

Fig 9. SEMs of samples bonded at 300°C (left) and 210°C (right). Region D marks the location of unreacted Sn.

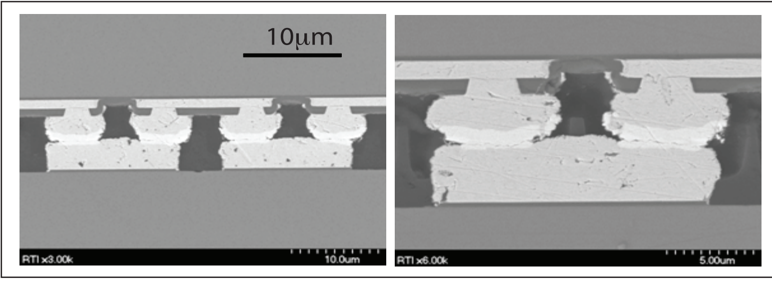

Fig 10. Cross-sectional SEM of sample with 10µm pitch bonded at 210°C.

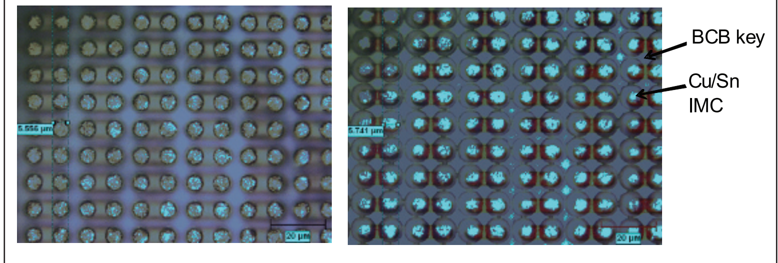

Fig. 11. Optical micrographs of a typical die from the qualification group (Device 501, 10µm pitch Cu/Sn-Cu bonded at 210°C) after shear testing. Left: Top die. Right: Bottom die.

Acknowledgments

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Cooperative improvement

Advances in semiconductor manufacturing require cost benefits as much as technology innovation. Surface preparation processes are an area were both issues need addressing and there are calls for cooperation along the value chain. **John Bubel**, Director of Marketing, Electronic Materials at **Avantor Performance Materials** discusses strategies for reducing costs and provides a case study with SSMC to show how cooperation leads to better materials, tools and processes

In past nodes, when traditional wet chemistries were initially tried in new equipment or with new substrate materials and integration schemes, costs could increase and added time was required to rework processes in order to reach optimum process stability and yield.

Problems significantly impacting yield and ROI often arose, due to incompatibility between chemistry, tool functionality and device compatibility. As a result, both captive and foundry fab operators, as well as others in the supply chain, have been seeking novel interaction models to speed new node ramp through faster development of wafer surface preparation solutions. There are fundamental advantages associated with pursuing a new

cooperative model with all three parties participating, led by fab operators and organized to meet their goals. The proposed model offers a path for improving yields and process ROI as an alternative to a system driven primarily by demands for reduced material and tool costs, by focusing on the total cost (time and money) of inefficient processes.

Genuine savings and verifiable improvements in total cost of ownership can be achieved by establishing early collaboration interactions before final technology integration is locked down – before final chemistry formulations are established, before final tool characteristics are established and before key process step decisions are made.

Better Integration Will Drive Innovation

The implementation of sub-22 nm nodes creates increasing pressure on both tool builders and wet chemistry suppliers to create more innovative solutions to key process steps, such as wet etch, photoresist strip and post-etch residue removal. Ever-more complex geometries and a wider range of substrate materials represent two examples of the types of challenges both face.

Equally challenging is the fact that, too often, as new nodes and new process steps are developed by fab operators, chemistry suppliers and tool builders work separately from each other, developing solutions at the direction of

the fab operators, governed by their approach to tightly control proprietary IP and technical data about a given node, geometry or process.

This has led to a marked tendency for new tools to be created, or existing tools to be modified/substantially updated, in isolation from and without a significant amount of consultation with chemistry suppliers. It has inhibited the chance to integrate innovations in tool designs with advances in the performance characteristics of engineered chemistries to optimize the results of a given process step.

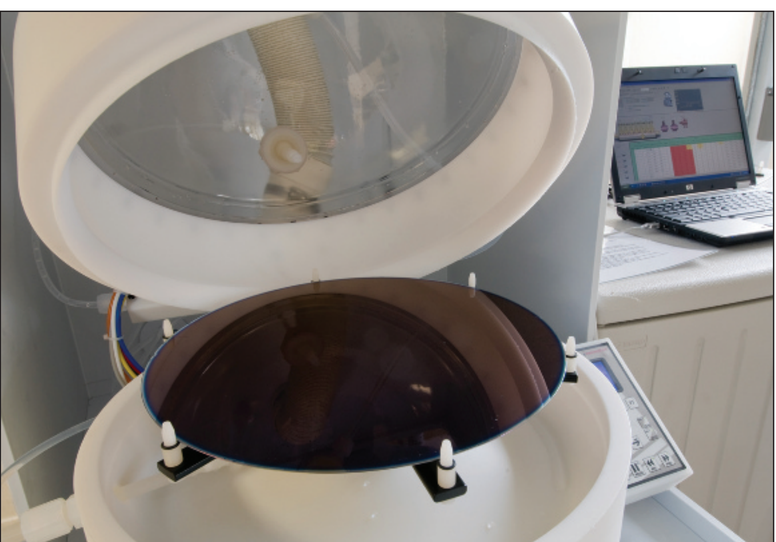
The Standard Model: Parallel Development Can Hinder

In response to technical direction from the semiconductor manufacturer, a chemistry supplier may develop new performance chemistries with characteristics engineered to solve specific challenges: improved viscosity, improved recyclability, formulations that reduce environmental impact, and most recently, chemistries selective to a specific layer.

At the same time, in parallel, tool builders frequently develop systems that are not compatible with these new chemistries, missing the opportunity to design tools that leverage the performance of these newly developed chemistries, such as broader process temperature latitude or sensitivity to certain materials of construction.

After testing offerings from multiple suppliers, the semiconductor manufacturer generally chooses a new chemistry for its process of record, based on results in lab testing or pilot runs. But when this chemistry is utilized in the process tool, costly modifications are often required to optimize the process step:

Wafer bath



chemistry temperatures, circulation rates, bath times and additives have to be added or adjusted, and can typically require some level of tool redesign to reach desired yield and performance targets.

A classic example is the introduction of high-dose ion implantation of photoresists. The exposed photoresists are transformed into carbonized-hardened crusts, which necessitated new stripping techniques and chemistries as standard mechanical or chemical processes were not fully effective.

To remove these hardened resists, a next-generation process was needed. The industry-accepted solution called for a process that utilized special, high-temperature chemistries first to loosen and soften hardened photoresist, and then precisely attuned mechanical motion to lift the residue without impacting very small geometries to which they were adhered. From the chemistry supplier's perspective, certain performance characteristics were crucial. The strippers needed to be:

- Very stable and not interact with the substrate
- Compatible with high-k dielectrics
- Able to chemically modify and break down the densified resist without affecting the morphology of the surrounding structures.

Multiple companies submitted similar aggressive chemistries designed to break-up and attack the "crusty" post implant resist. Commensurate with these chemistries, a major modification of the tools was needed, such as high temperature mixing tanks and segregation of the active components prior to addition to the mixing tanks. Non-standard metallic and plastic components to minimize corrosion needed to be fitted as well.

These complexities, which arose out of the unique characteristics of the newer chemistries, led to tool delivery delays and in some cases a withdrawal of some tool developers from participation. For some manufacturers, an unworkable solution was introduced into the process, producing delays in ramping to full yield.

Joint Efforts

A better approach would have been for tool builders and chemistry suppliers to be teamed by the semiconductor manufacturer to solve the hardened photoresist removal challenge as a combined effort. All three participants will need

to make strong commitments: The semiconductor manufacturer must be prepared to build a long-term relationship with both tool builder and chemistry supplier; in turn, they must commit resources to see the new surface preparation solution to a successful launch.

Under the old model, a development process that took 70 weeks, with 100-300 additional pilot wafer runs and testing, would have been replaced with a process that hypothetically should have taken 40 weeks or less to reach full ramp. By saving time, it might have been possible to eliminate 25-30 percent in additional development costs for the tool builder, the chemistry supplier and the manufacturer, by refining cleaning processes and tooling and chemical formulation characteristics as a single effort.

Another example is that of implementing a new process for post-ash residue removal in vias in a new node or new geometry. In this hypothetical example, the semiconductor manufacturer establishes pre-conditions that limit the best technological solution:

- They may specify an immersion tool or a single wafer spray tool, due to familiarity with the system and a perception that it is a lower cost solution overall.
- The manufacturer may also set a maximum unit cost for the wet tool chemistry — $30/gallon, for example.

This immediately limits the chemistry supplier's technology choices; the manufacturer may even specify an "in-house" formulation of commodity chemistries, rather than opening the door to the chemical company's engineered options.

A standard rule of thumb is that wet processes have lower indirect and direct costs per wafer, compared to dry process tools. However, chemistries designed for bath tools do not directly transfer to spray tools or other tools using novel delivery methods. If the semiconductor manufacturer directs the tool builder to utilize a single wafer spray tool (possibly by modifying a toolset already in use at the manufacturer's fab) then the chemistry used in that tool must be optimized to that toolset.

All the risks rest squarely with the chemistry supplier: They must optimize the performance of their chemistry with the decision to use a single wafer tool — and at a price point that may force the use of a less effective chemistry for that tool. Development costs could increase, due to additional fine-tuning of process variables to minimize impact on vias and substrates, or more frequent bath changes, or increasing material and waste treatment costs. Costs could also increase for the chip manufacturer as it may need to unexpectedly retrofit its cleaning tools to be compatible with these new chemistries.

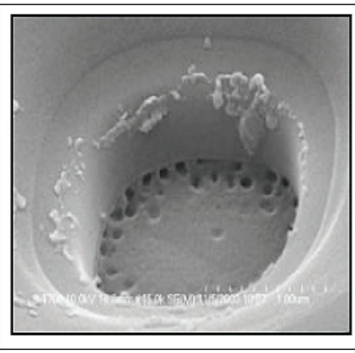
Semiconductor manufacturing requires intense material know how

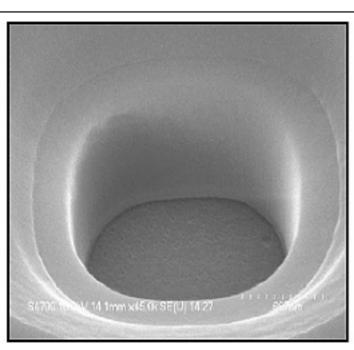
Collaborative Solutions

In a collaborative model, the tool builder and chemistry supplier will get a detailed understanding from the semiconductor manufacturer of the total yield and process goals, on a per-wafer-pass basis, for the post-etch residue removal process; then together they develop the solution, which might (or might not) match the manufacturer's original tooling and chemistry assumptions.

The chemistry supplier could propose an engineered chemistry that works in a particular type of tool — a wet bench immersion tool, for example - that has a bath life three times longer than the chemistry used in a spray tool, and generates similar or even better yields. The tooling is different, and the chemistry unit price is higher than what the manufacturer originally assumed; but since the chemistry has a longer life and the tool uses it much more efficiently, total process cost can be shown to be lower.

This approach will not only help chemistry suppliers — tool builders have an equal potential to benefit. They won't be forced to re-design tools with materials of construction that are incompatible with new chemistries, or have insufficient capabilities for broad temperature settings, flow rates and mixing features. Given the full scope of the challenge, the chemistry supplier and tool builder could propose the optimum solution based on process times, and tool, materials and ancillary costs (waste





The team theorized that one reason for the improved yields was that the HA-based chemistry, when used at higher temperatures (i.e. 85 C), can cause excessive etching pitting of metal layers, as can be seen in this SEM image.

treatment) — one that fully satisfies the manufacturers yield and total cost of ownership goals.

The New Model: Cooperative Efforts Lead to Higher Yields

As a framework for advancing this collaborative model, a recent project to assess alternatives to hydroxyl-amine (HA)-based post-etch ash residue removal chemistries that Avantor Performance Materials pursued with the Singapore-based foundry, SSMC, Inc., suggests that increased levels of openness and collaboration can yield significant benefits.

Avantor, formerly Mallinckrodt Baker, Inc., has supplied innovative, high-purity, high-performance surface cleaning chemistries and other products for photoresist stripping, residue removal and other surface modification applications to the semiconductor industry for more than 25 years.

SSMC Inc. provides foundry services processing 200mm wafers in the 0.25 down to 0.14 µm technology node. Seeking to control costs and achieve better process control, the company approached Avantor to investigate alternatives to its existing post-etch ash residue removal chemistry.

In the past, a foundry like SSMC would have requested proposals from multiple chemistry suppliers, focusing almost exclusively on reducing unit costs compared to its existing process-of-record chemistry, while seeking comparable process performance. In this case, SSMC partnered exclusively with Avantor to fully investigate and test at both lab and pilot line level the potential value of Avantor's BAKER ALEG-380 post-etch ash residue removal product. ALEG-380 residue remover is an engineered blend of organic solvents and semi-aqueous components suitable for bulk photoresist and post-etch ash residue and sidewall polymer removal. It is designed to provide wider process latitudes than those supported by 100 percent organic chemistries such as HA-based products.

Cost Control Surprises

Although cost control was the initial reason SSMC chose to collaborate with Avantor, the technical expertise and insight into wafer surface treatment chemistries and processes Avantor supplied help create an effective collaborative process. Avantor applications engineers worked with SSMC process engineers to conduct multiple comparison analyses on test wafers to assess ALEG-380's viability and compare its performance with the existing POR chemistry. After a first detailed round of lab testing, ALEG-380 was placed on one of the eight lines at the SSMC's foundry in Singapore. Test wafers were sent through the standard manufacturing steps.

The test results were better than expected: via and metal line yields were better for the Avantor performance chemistry compared to the existing HA-based chemistry, when SSMC was only expecting to achieve comparable yields. In addition, bath process temperature latitude was broader, and further testing and SEM imaging determined that ALEG-380 demonstrated much lower etch rates on both metal lines (Al and Cu) and on substrate materials.

Pilot Awareness

Based on these test results, SSMC worked with Avantor to conduct a pilot run of ALEG-380 under full process conditions. The pilot production run validated the test results, and SSMC determined that it could achieve a 2-3 percent improvement in yield, and a corresponding 25-30 percent cost reduction in their post-etch ash residue removal process using ALEG-380. This led SSMC to change its process of record (POR) and implement use of ALEG-380 on all eight production lines.[1]

The collaboration was a success because SSMC communicated to Avantor the key chemistry performance requirements, such as broader process latitude and reductions in metal and substrate etch, as well as cost-reduction goals, and engaged Avantor fully in the process of wafer testing, pilot production run and full implementation of the new chemistry.

This enabled Avantor applications engineers, working alongside SSMC's fab engineers, to contribute significant insight into optimization steps and methodologies for effectively comparing ALEG-380 with the HA-

based product — ultimately resulting in both cost savings and yield increases for SSMC.

The insight offered by applications engineers from Avantor, who specialize in utilizing and refining the performance of semiconductor surface preparation processes, was crucial: SSMC process engineers are not necessarily experts in formulated chemistry development and the interactions of their process conditions to the chemistry's performance. The specialized knowledge that Avantor's personnel supplied enabled the SSMC/Avantor team to better analyze the interaction between the lab results and the chemistry parameters that drove those results.

The team's combined expertise also allowed them to theorize more effectively why a semi-aqueous product would reduce the etching and deliver better cleaning results compared to the HA-chemistry. With this knowledge and a more integrated approach in understanding these challenges, the team was able to further develop a wafer test plan including variations in process temperatures and post-residue removal SEM imaging, to validate assumptions about the improved yields being demonstrated.

This insight, combined with the improved yields, gave SSMC the confidence to modify its POR, eliminate the HA-based chemistry (with its continually escalating costs) and implement a new chemistry with a better yield. Investing the time and effort, by both companies, to pursue a collaborative approach, generated a major benefit: SSMC initially anticipated incremental savings, just on unit cost basis, from replacing the HA chemistry with a less expensive solution from Avantor; instead, the in-depth interaction led to a significant yield gain for SSMC, which is potentially worth millions of dollars per year.

Eliminate Waste, Improve Process, Increase Yields

Increased collaboration between tool builders, chemistry suppliers and manufacturers can improve FEOL and BEOL wafer cleaning and surface modification processes. It will enable the faster development of toolsets and processes for the next technology node, offering the potential to significantly reduce development costs, shorten the time to optimize processes and ultimately enable faster ramps to full production.

It could also lead to significant costs savings in legacy processes due to yield improvements or dramatic decreases in chemistry usage or process time. These are far more significant opportunities for improving profitability and return on investment compared to pitting chemistry suppliers against each other for cost reductions, but to achieve those benefits requires the in-depth collaboration that was highlighted in the SSMC example.

Increased collaboration between tool builders, chemistry suppliers and manufacturers can improve FEOL and BEOL wafer cleaning and surface modification processes

Collaboration Provides Success

The key to the success of this model is the leadership provided by the fab operator: Earlier engagement and cooperation before final developments are locked down is essential. It will enable performance chemistry suppliers like Avantor to apply a full range of applications expertise and insight to refine engineered performance materials to work with today's advanced substrate materials and sub-22nm structures. Even when this model is applied to older, legacy processes (as in the SSMC example), it resulted in significantly increased yields and enhanced total cost of ownership.

Tool builders will also benefit: They will have a more focused development process from the outset, benefitting from the technical synergies that will result from a working partnership with chemistry suppliers, which will enable them to build tools that work from the beginning with the chemistries that have been developed for that process step.

This success will also help improve their industry standing and differentiate their offerings by highlighting close working relationships with leading chemistry suppliers. Most importantly, this model offers fundamental competitive advantages for semiconductor manufacturers: Anything that can be done to reduce the cost and speed the ramp of the next node to full yield will deliver value that goes right to the bottom line.

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Notes:

1. S.I. Kim, H.P Lim, L. Liu, N. Mustapha, T.T. Seng, "Replacing Hydroxyl-Amine-based chemistries with semi-aqueous-based cleaning formulations generates improved yields in post-etch metal and oxide residue removal," 2011.

Semiconductor industry applauds EU

The EU has released the final report of the expert group on Key Enabling Technologies (pg 11) and semiconductor leaders urge swift reaction to the plan's development.

Over the past year a select group of European industrialists engaged in a strategic planning process with government representatives from key EU Member States and several Directorates General of the European Commission to define a competitive framework to facilitate the success of these crucial key enabling technologies in the EU. The group was chaired by Jean Therme, CEO of the French research organisation CEA.

Central to these discussions were the role KETs can play in tackling Europe's societal challenges such as energy efficiency or ageing population, as well as the global competitive positioning of KETs in Europe. This process led to a final report which delivers recommendations for the advancement of KETs in Europe. The recommendations span the entire value chain from the generation of ideas to their commercialisation, and cover the areas of technological research, product development and globally competitive manufacturing.

The reaction of Carlo Bozotti, President of ESIA and CEO of STMicroelectronics to the final KETs report was: "With this report we are seeing the emergence of a comprehensive and practical blueprint of a European industrial innovation and manufacturing policy for key enabling technologies. This has the potential of boosting innovation in Europe and ensuring that key enabling technologies like microelectronics can fulfil their enabling role in and for Europe for the benefit of strategic industries."

In the area of product development, the report shows Europe devotes more resources to fundamental research than other competitor regions but is not competitive when it comes to supporting more product based research.

Says CEO of Infineon Technologies Peter Bauer: "The ability to be more competitive regarding the installation of pilot lines in Europe would be one direct consequence if the recommendations are implemented."

There are recommendations to enhance competitive manufacturing, including the introduction of a matching clause to attract investment in production in and into Europe, or adapting EU state aid to industries competing in globalized economies. The recommendations are supported by Intel VP and Intel Ireland's General Manager Eamonn Sinnott and the CEO of Soitec André-Jacques Auberton-Hervé.

Says Sinnott: "We support the report's recommendations to create a global level playing field for advanced manufacturing in Europe, with particular emphasis on the crucial contributions of the semiconductor industry."

Auberton-Hervé states: "One of Europe's strengths is the successful cooperation between suppliers and chip makers. The report recognizes the strategic importance of the value chain from raw materials to final products."

Recommendations to enhance technological research call for integrated R&D programmes 'from the lab to the pilot line' for KETs and a focus on inclusion of the value chain in R&D.

"Integrated programmes to guide technological research via technology validation to pilot lines and demonstrators in the field of KETs are needed. They would be an innovation in their own right ", says Professor Hans-Jörg Bullinger, President of Fraunhofer Gesellschaft.

The discussions and reactions reflect the enthusiastic response coming out of the report from the semiconductor industrial leaders who were all members of the high level group. At the same time there was also the realization that the High Level Expert Group's Final Report is a vital milestone but not the end result. They and ESIA remain committed to continue to support this strategic initiative and therefore now urge EU decision-makers to ensure its speedy implementation.

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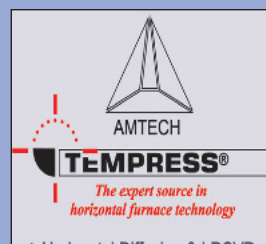
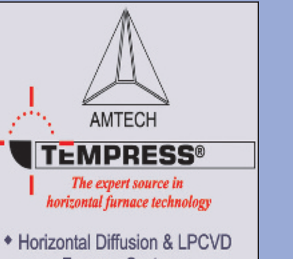

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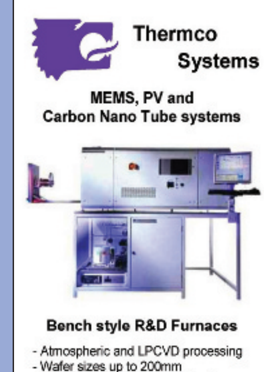

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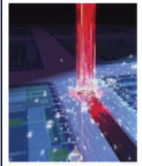

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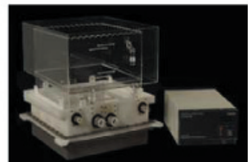

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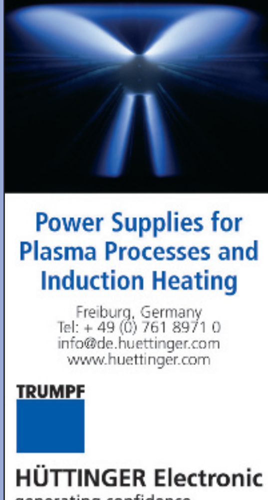

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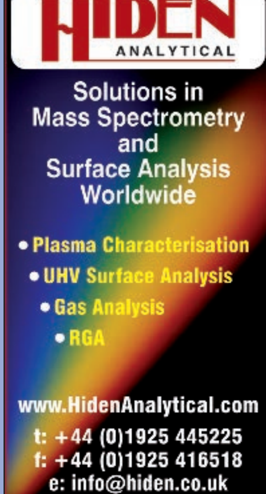

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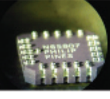

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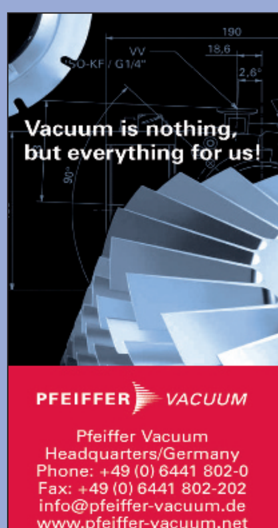

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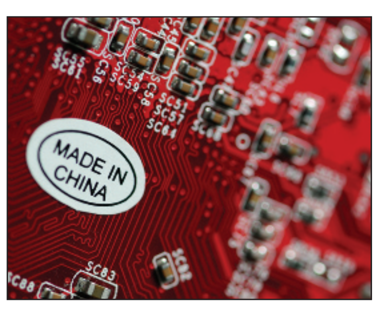
China's Fabless Market Set to Double



Driven by strong domestic demand and soaring exports, China's fabless semiconductor market is on a high-growth trajectory, with revenue set to double from 2010 to 2015, new IHS iSuppli research indicates.

Operations by fabless semiconductor companies in China will generate $10.7 billion in revenue in 2015, up from $5.2 billion in 2010. The growth comes on top of a 23.6% expansion in 2010, with revenue rising from $4.2 billion in 2009. Revenue will reach $5.74 billion in 2011.

"China's fabless industry in 2010 benefited from the booming demand for semiconductors used in cell phones, as shipments last year of mobile handsets designed in China surged by nearly 60 percent," said Vincent Gu, senior analyst for China research at IHS.

Chinese fabless supplier Spreadtrum Communications designed a range of semiconductors for cell phones including core chipsets, radio frequency transceivers and total wireless solutions for mobile handsets. The company posted $346 million in revenue in 2010, making it the first fabless semiconductor supplier in the country to surpass the $300 million mark. Spreadtrum is likely to retain leadership in 2011 with revenue of more than $500 million.

Fabless firms must emphasize the domestic Chinese technology industry, allowing local tech companies to cash in on the expansion of the burgeoning market. Fabless firms also need to leverage China's home advantages, such as the vast demand within the country.

IHS iSuppli Figure: China Fabless Industry Revenue Forecast (Millions of U.S. Dollars)

	2008	2009	2010	2011	2012	2013	2014	2015
Millions of U.S. Dollars	$3,411	$4,172	$5,158	$5,739	$7,117	$7,939	$9,127	$10,716
Annual Percentage Growth	10.6%	22.3%	23.6%	11.3%	24.0%	11.5%	15.0%	17.4%

Source: IHS iSuppli June 2011

Moreover, China's fabless semiconductor suppliers must focus on consumer electronics because the major characteristics of the consumer electronics market play to the strengths of Chinese chip designers. On a third front, Chinese fabless suppliers now must engage in the convergence of features in their products. They also must pay attention to the changes to business models wrought by the convergence of features in products.

However, to take the next step and surpass their worldwide competitors, China's fabless firms also may want to pay attention to three more C's: Culture, Content and Contribution, Gu observed.

The companies must accommodate and adjust to the differing cultures of overseas customers. They must learn more about end-content sectors that drive the growth of technology markets. And China's fabless firms must take advantage of government contributions to the industry.

Despite strong growth prospects for the fabless business, the industry faces several obstacles. For one, penetrating the market for logic semiconductors is difficult. Another challenge is obtaining sufficient semiconductor manufacturing fab capacity, which has been a problem for the companies in the past.

The fabless firms also must contend with the semiconductor industry's oligopolistic structure, with market share dominated by a small group of large competitors. The very small size of the fabless Chinese fabless companies makes it harder for them to compete with the worldwide giants.

A bright spot for the fabless industry remains the support it enjoys from the government, which launched a new policy this year on software and integrated circuit industry. The new policy is more flexible, and the Chinese fabless industry appears set on a fast track to growth in the future.

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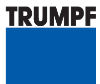

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